Technical Reference Manual

AM275x Signal Processors Technical Reference Manual

TEXAS INSTRUMENTS

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Read This First

About This Manual

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers can be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Related Documentation

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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1 Introduction

1.1 Overview

This chapter introduces the features, subsystems, and architecture of the AM275 device.

1.2 Module Allocation and Instances within Device Domains

AM275 has three kind of domains, and each domain has a specific set of modules, configuration functions, and resets. The below list and table give an quick introduction to domains and modules.

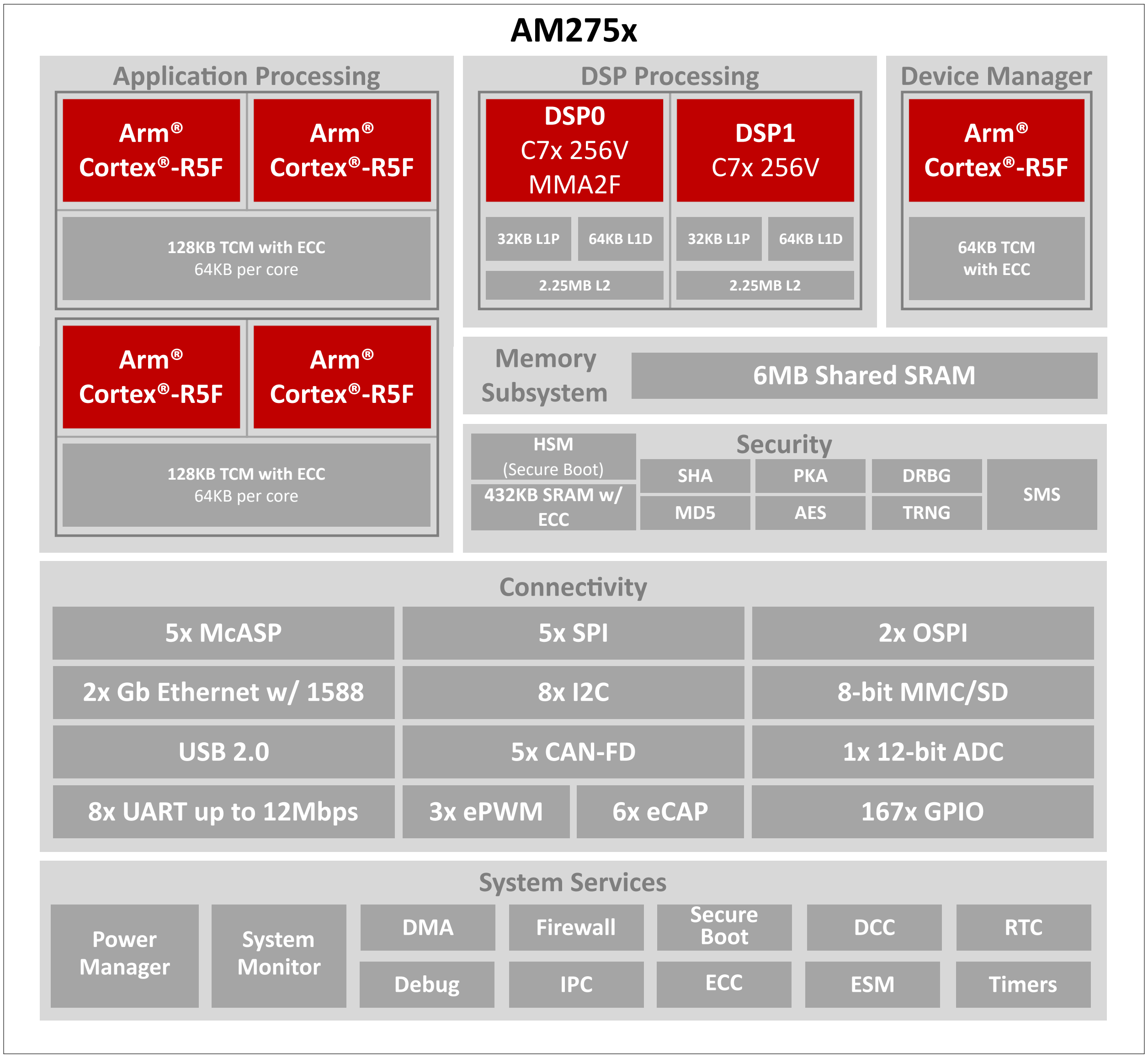
- MAIN: Provides high-performance computing cores including to digital signal processors and audio related modules
- WKUP: Also known as Wake Up. This is the primary domain for Device Manager and safety.
- Top Level: This TRM uses the prefix of "MCU_" for items that refer to the device as a whole instead of a specific domain.

Module Full Name	**Module Abbreviation**	**Device Domain**		
		MAIN	**Top Level**	**WKUP**
Audio Asynchronous Sample Rate Converter	AASRC	2		
Analog-to-Digital Converter	ADC	1		
Audio Tracking Logic	ATL	1		
DSP0 - C7x with MMA	C7X256V	1		
DSP1 - C7x	C7X256V	1		
Ethernet Switch	CPSW	1		
Dual Clock Comparator	DCC	9	2	
Data Movement Subsystem	DMSS	1		
Enhanced Capture Module	ECAP	6		
Enhanced Pulse Width Modulation Module	EPWM	3		
Error Signaling Module	ESM	1	1	
Flash Subsystem	FSS	2		
General Purpose Input/Output	GPIO	2	1	
Global Time Counter	GTC			1
Inter-Integrated Circuit	I2C	7		1
Single-Core Arm Cortex - R5F Subsystem	R5FSS			1
Dual-Core Arm Cortex -R5F Subsystem	R5FSS	2		
Real Time Interrupt	RTI	6		1
Interprocessor Communication - Mailbox	MAILBOX	1		
Controller Area Network Interface	MCAN	5		
Multi-Channel Audio Serial Port	MCASP	5		
Memory Cyclic Redundancy Check Controller	MCRC	1		
Multi-Media Card/Secure Digital Interface	MMCSD	1		
Peripheral DMA	PDMA	8		
Serial Peripheral Interface	SPI	5		

Interprocessor Communication - Spinlock	SPINLOCK	1		
Dual-Mode Timer	TIMER	16		2
Universal Asynchronous Receiver/ Transmitter	UART	7		1
Universal Serial Bus Subsystem	USB	1		

For more detailed view of domains, please refer to the *Interconnect* chapter

1.3 Functional Block Diagram



1.4 Device MAIN Domain

This section describes the modules integrated in the device MAIN domain.

1.4.1 Audio Asynchronous Sample Rate Converter

Instantiated in MAIN domain two Audio Asynchronous Sample Rate Converter (AASRC) module supports the following main features:

- High performance Asynchronous Sample Rate Converter with 140dB Signal-to-Noise (SNR)
- Supports up to 16 audio channels - 8 input and 8 output stereo streams
- 4 input and output clock zones
- Support for input and output audio sample rates from 8 kHz to 216 kHz
- Automatically sensing/detection of input sample frequencies
- Attenuation of sampling clock jitter
- Support of 16-, 18-, 20-, 24-bit data input/output
- Supports Input/output sampling ratios from 16:1 to 1:16
- 128 sample input and 32 sample output FIFO for each channel
- Supports system clock more than or equal to 200 MHz
- Support of group mode, where multiple AASRC blocks use the same timing loop for input or output
- Linear phase FIR filter
- Controllable soft mute
- Separate DMA events for input and output, for each channel and group
- Interrupts for input, output, and error for channels and groups of channels
- Independent clock generator for each input and output clock zone
- Independent rate and stamp generator for each input and output clock zone

1.4.2 Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels) and supports the following main features:

- 4 MSPS rate with a 60 MHz sample clock
- Single-ended or differential input options
- ADC module can be configured and transformed into digital test inputs
- Programmable 16 steps Finite State Machine (FSM) sequencer

1.4.3 Audio Tracking Logic

The Audio Tracking Logic (ATL) module, which is used by HD Radio™ applications to synchronize the digital audio output to the baseband clock, supports the following main features:

- Contains four ATL instances, for HD Radio support and asynchronous sample rate conversion assistance
- Each instance tracks the time error between two syncs (local Audio Word Select [AWS] and Baseband Word Select [BWS])
- Each instance selects between 8 mux choices for BWS and 8 mux choices for AWS
- Each instance generates modulated ATCLK clock signals with software-initiated pulse stealing
- Selection between interface or functional clock to run error counting timers and to derive modulated clock outputs
- Clock and reset management: receives clock and reset signals from the device PSC module
- Hardware reset
- Local software reset

1.4.4 DSP C7x

Single or Dual Core DSP C7x256V (DSP C7x) Subsystem has the following features:

- C7x ISA and RISC-V G ISA extensions
  - Vector DSP, 40 GFLOPS
  - 256-bit vector width
- L1 memory architecture
  - 32KB I-cache
  - 64KB D-cache
- L2 memory architecture
  - Repurposing of L2/EL2 embedded memory for use by SOC resources when C7x/MMA/DRU are disabled
  - 2.25MB L2 with ECC protection on L2 SRAM which is managed as 2MB segment named "Main" and 256KB segment named "Auxiliary". A continuous L2 memory view via tie off.

  - Unified Memory Controller (UMC) facilitates L2 SRAM accesses from CPU and SOC (DMAs) as well as EMIF accesses from CPU.
  - Full ECC Support with RMW
  - DRU (DMA engine) integrated that facilitates data transfer between L2, VPAC and EMIF.
    - Event bus interface integrates with SOC DMSS
    - Tightly coupled with C7x/MMA (DRU is not available for use when the C7x/MMA is disabled)
- Interrupts
  - Local event controller (CLEC) integrated within CorePac for routing and handling of DRU interrupts, CPU generated IPC events to SOC, interrupts coming from SOC
- Security
  - Support for C7x Authenticated Boot. Security is in-context during boot to facilitate the authentication and loading of the C7x image. (per approved CR: PROC_SOC-4890)
  - C7x native security level (TrustZone equivalent) is not supported on the device, and the core executes code in non-secure state of C7x. The secure sideband signal (output) from the C7x data plane initiator interface can be left floating.
  - The C7x L2 SRAM (UMC) can not be used for storing security content as there is no protection of UMC memory from C7x. In a threat scenario, the C7x can be activated if in reset to execute malicious code to access data in UMC thereby defeating a protection for security data in UMC.
  - No security can be inferred from DRU as this IP is out of scope for security.
  - TrustZone debug controls (DBGEN, NIDEN, SPIDEN, SPNIDEN) are supported
- Safety
  - Support for reporting safety errors to SOC via interrupt
- Debug
  - Independent debug interface supporting access to embedded features
  - Debug features include: Core debug, Advanced Event Triggering, Trace, CTSETs, and an embedded CP Tracer Aggregator with bus probes on internal memory interfaces
- Power Management
  - Support for granular gated clock domains to support low power modes and to support memory interface utilization while IP disabled.

- Dedicated PLL for full flexibility in performance and power trade-offs
- Dedicated windowed watchdog timer per core
- DSP0 C7x supports Deep-learning Matrix Multiply Accelerator (MMA2F) with floating support

1.4.5 3-port Gigabit Ethernet Switch (CPSW3G)

Integrated in MAIN domain: One instance of the 3-port Gigabit Ethernet Switch (CPSW3G) subsystem provides Ethernet packet communication for the device. The CPSW3G subsystem provides the following main features:

- Two external Ethernet ports with selectable RGMII and RMII interfaces and one internal Communications Port Programming Interface (CPPI) port.
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Support of eight priority level Quality Of Service (QOS) - 802.1p
- Support for Audio/Video Bridging (P802.1Qav/D6.0 and 802.1Qaz)
- Ethernet port reset isolation
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
- Differentiated Services Code Point (DSCP) Priority Mapping (IPv4 and IPv6)
- IPV4/IPV6 UDP/TCP checksum offload
- Priority Based Flow Control (801.1QBB) and Flow Control (802.3x) Support
- Wire rate switching (802.1d)
- Store and Forward Switching
- Non-Blocking switch fabric
- Support of Time Sensitive Network - IEEE P902.3br/D2.0 Interspersing Express Traffic and IEEE 802.1Qbv/D2.2 Enhancements for Scheduled Traffic
- Address Lookup Engine (ALE) with 512 ALE table entries
- EtherStats and 802.3 Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)

- Maximum frame size of 2020 bytes
- Management Data Input/Output (MDIO) module for PHY Management
- Host port CPPI Streaming Packet Interface
- Emulation support
- Chip-to-Chip direct MAC interconnect via RGMII
  - For enabling on board chip-to-chip connectivity, PHY less MAC-MAC interface utilizing CPSW3G shall be supported via RGMII. This configuration shall be fully verified and validated.

1.4.6 Dual Clock Comparator

- Dual Clock Comparator (DCC) modules, used to determine the accuracy of a clock signal during the time execution of an application, each having the following main features:
  - Two independent counter blocks count clock pulses from each clock source
  - Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
  - Configurable time base for error signal
  - Error signal generation when one of the clocks is out of spec
  - Clock frequency measurement

1.4.7 Data Movement Subsystem (DMSS)

Integrated in the MAIN domain: One Data Movement Subsystem (DMSS) can be used for efficient transfer of data support between software, firmware, and hardware in all combinations. It consists of the following main modules:

- Packet DMA Controller
- Block Copy DMA Controller
- Ring Accelerator provides hardware acceleration to enable straightforward passing of work between a producer and a consumer and has the following main features:
  - Supports up to 20 independent memory-mapped ring structures
  - Supports various modes for each ring based on usage and compatibility
  - Provides single-word deep shared incoming Transfer Response FIFO
  - Provides bit-wide source VBUSM read/write target interface for accesses from DMA controller entities
- Secure proxy module is a modified version of the proxy module and in addition has the following main features:
  - Provides proxy function to store large data bursts that a host can only access in smaller amounts
  - Supports a configurable number of threads, where each has their own independent proxy function
  - Keeps the large data burst coherent until the complete data has been accessed
  - Allows for interleaved access between multiple hosts or tasks using multiple proxy threads
  - Supports a configurable target resource. The target has a configurable number of channels, size of each channel and base address
  - Supports a programmable fixed queue for each proxy thread
  - Supports multiple producers all writing to the same queue
  - Supports programmable thresholds for when to generate events
  - Supports a max message count for outbound proxy threads limiting the number of messages a thread can produce
  - Optionally supports dynamic clock gating
- Interrupt Aggregator modules provide a centralized machine which handles the termination of system events to that they can be coherently processed by the host(s) in the system. Main features are as follows:
  - 64-bit VBUSP target using 64-bit registers
  - Provide a set of TI Interrupt Architecture compliant interrupt status and mask registers which are used to pass specific event status to one or more host blocks.
  - Provides an optional set of Unmapped event (UNMAP) which can take an 'unmapped' event from the ingress ETL and generate a Global event on the egress Event Transport Lane (ETL) interface.
  - Provides an optional set of Global Event Input (GEVI) counters which can count events delivered via an ingress Event Transport Lane (ETL)

  - Provides an optional set of Local Event Input (LEVI) to Global event registers which can be used to convert pulsed discrete interrupt inputs or clock synchronous rising edge events into Global events on an egress ETL
  - Provides an optional set of Global Event Input (GEVI) 'Multicast' registers which can take a Global event from an ingress ETL and generate two egress Global events on two egress ETL interfaces

1.4.8 Enhanced Capture Module (ECAP)

Integrated in MAIN domain: Six Enhanced Capture (ECAP) modules provide accurate timing for different events. When not being used for event capture, its resources can be used to generate a single channel of asymmetrical PWM waveforms (configurable as either one capture input, or as one auxiliary PWM output). Each ECAP module supports the following main features:

- 32-bit time base counter
- 4 x 32 bits event time-stamp capture registers
- 4 stage sequencer (Mod4 counter), synchronized to external events
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- Interrupt capabilities on any of the four capture events
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or delta mode time-stamp capture)

1.4.9 Enhanced Pulse-Width Modulation Module (EPWM)

Integrated in MAIN domain: Three Enhanced Pulse-Width Modulation (EPWM) modules, each with the following main features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs that can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

1.4.10 Error Signaling Module (ESM)

Error Signaling Module (ESM) for safety-related events and/or errors aggregation from throughout the device into one location supports the following main features:

- Selectable low and high priority interrupt error pin prioritization of each error event
- Up to 1024 level or pulse error event inputs
- Error signal routed out of device through MCU_ESM error signal
- Configurable time base for error signal
- Error forcing capability
- Internal redundant flops on safety critical fields

1.4.11 Flash Subsystem (FSS) Peripheral

Integrated in MAIN domain is two different Flash Subsystem (FSS) providing access to external memory devices via Octal Serial Peripheral Interface (OSPI) along with encryption/decryption and in-line ECC protection. To summarize:

- OSPI_0 (FSS0)
  - Supports TI OptiFlash, including XIP, for external flash devices
- OSPI_1 (FSS1)
  - Supports HyperRAM based external RAM devices
  - OR: Supports standard external flash device operation (i.e no OptiFlash)
  - OR: Supports standard external RAM device operation

Separately, the FSS supports the following main features:

- FSS0
  - 4Gbytes memory address support
  - Firmware Over The Air (FOTA) accelerator functionality to support configuration and data interface access to flash Controller (OSPI)
  - Support for single, dual, quad (Quad-SPI mode) or octal (on Octal-SPI0 only) I/O instructions
  - Support for OptiFlash
  - In Quad-SPI and Octal-SPI modes, support single data rate up to 166MHz SDR
  - Memory mapped ‘direct’ mode of operation for performing flash data transfers and executing code from flash memory
  - Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers
  - Local SRAM of configurable size to reduce advanced high-performance bus overhead and buffer flash data during indirect transfers
  - Set of software advanced peripheral bus accessible flash control registers to perform any flash command, including data transfers up to 8-bytes at a time
  - Additional addressable memory bank to accommodate more than 8-bytes at a time.
  - Support for XIP, sometimes referred to as continuous mode.
  - Programmable device sizes
  - Programmable write protected regions to block system writes from taking effect
  - Programmable delays between transactions
  - Legacy mode allowing software direct access to low level transmit and receive FIFOs, bypassing the higher layer processes
  - An independent reference clock to decouple bus clock from SPI clock – allows slow system clocks
  - Programmable baud rate generator to generate OSPI clocks
  - Features included to improve high speed read data capture mechanism
  - Option to use adapted clocks or DQS to further improve read data capturing
  - Programmable interrupt generation
  - Up to four external device selects - OSPI and QSPI devices can be mixed
  - Programmable data decoder, enables continuous addressing mode for each of the connected devices and auto-detection of boundaries between devices
  - Supports BOOT mode
  - Bidirectional CRC on Multiple-SPI
  - Handling ECC errors for flash devices with embedded correction engine
  - Full integration with PHY module dedicated to more flexible and power efficient transfers
  - Supports RESET_OUT[1-0] and ECC_FAIL pins for external flash devices where ECC is checked on the flash
  - Automatic Flash device status polling for programming operation (Auto HW Polling)
- FSS1
  - Secondary OSPI supports
    - 32-byte block (BC) operation
    - ECC
  - OSPIs support single, dual, quad, or octal SPI devices
  - OSPIs support up to 4 devices
  - HyperBus interface supports up to 2 devices
  - The OSPIs and HyperBus interface have independent power management for low power operations
  - Support for XIP, sometimes referred to as continuous mode.

1.4.12 General Purpose Input/Output Interface (GPIO)

Integrated in MAIN domain: General Purpose Input/Output (GPIO) module that provide dedicated general-purpose pins that can be configured as either inputs or outputs. The GPIO module main features include:

- Support of 9 banks x 16 GPIO pins
- Support of up to 9 banks of interrupt capable GPIOs
- Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO pin
- Set/clear functionality per individual GPIO pin

1.4.13 Inter-Integrated Circuit Interface (I2C)

Integrated the device are instances of the multi-controller Inter-Integrated Circuit (I2C) interface module, each with the following main features:

- 1x Instance with open-drain voltage buffers in compliance with the Philips I2C-bus specification version 2.1
- Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Support of 7-bit and 10-bit device addressing modes
- 8-bit-wide data access
- Support of multi-controller transmitter/peripheral receiver and receiver/peripheral transmitter modes
- Built-in FIFOs with fixed size of 32 bytes.
- Support of Auto Idle, Idle Request/Idle Acknowledge handshake, and Asynchronous wake-up mechanisms

1.4.14 Dual-Core Arm Cortex-R5F Processor (R5FSS)

The ARM Cortex-R5F processor subsystem (R5FSS) supports the following main features:

- Armv7-R architecture
- R5FSS Memory System
  - 32KB Instruction Cache
    - 4x8KB ways
    - SECDED ECC protected per 64 bits
  - 32KB Data Cache
    - 4x8KB ways
    - SECDED ECC protected per 64 bits
  - 64KB tightly-coupled memory (TCM) per CPU
    - SECDED ECC protected per 32 bits
    - TCM hard error cache Implemented in CPU
    - Readable/writable from system
    - TCMs initialized (to 0's) at reset
    - 32KB TCMA (ATCM)
    - 16KB TCMB0 (B0TCM)
    - 16KB TCMB1 (B1TCM)
- Full-precision Floating Point (VFPv3)
- 16-region Memory Protection Unit (MPU)
- 8 breakpoints, 8 watch points
- CoreSight Debug Access Port (DAP)
- CoreSight ETM-R5 interface (CTI, ETM)
- Performance Monitoring Unit (PMU)
- 32-bit to 36-bit Region-based Address Translation (RAT) on memory access initiators
- Integrated Vectored Interrupt Manager (VIM) per core with 256 Interrupt Inputs each
  - Programmable interrupt priority (4-bit)
  - Programmable interrupt enable mask
  - Software-generated interrupts
  - Synchronous clock domain crossing on all core interfaces
- MAIN Domain R5FSSs are dual core and are also known as MCUSS

Note

CORE0 has 64KB of TCM.

Note

These details describe a superset of the R5FSS memory configuration. For additional details on device memory availability, please refer to the device-specific Datasheet.

1.4.15 Mailbox (MAILBOX)

Integrated in MAIN domain: One Mailbox (MAILBOX) module to facilitate the communication between the various on-chip processor cores of the device by providing a queued one-way mailbox-interrupt mechanism with senders and receivers. The MAILBOX has the following main features:

- 1x clusters
- 32-bit message width
- Message reception and queue-not-full notification using interrupts
- Non-intrusive emulation
- Generic (up to 16) mailbox fifos per cluster
- Generic (up to 64) maximum number of messages per mailbox fifo

1.4.16 Controller Area Network (MCAN)

Integrated in the Main domain: Five Controller Area Network interfaces (MCAN) supporting both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications and having the following main features:

- Conforms with CAN Protocol version 2.0 part A, B and ISO 11898-1:2015
- Full CAN FD (up to 64 data bytes) support
- SAE J1939 support
- AUTOSAR support
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs, up to 64 elements each
- Configurable transmit FIFO, up to 32 elements
- Configurable transmit queue, up to 32 elements
- Configurable transmit event FIFO, up to 32 elements
- Up to 128 filter elements
- Maskable interrupts, two interrupt lines
- Timestamp Counter

1.4.17 Multi-Channel Audio Serial Port

The Multi-Channel Audio Serial Port (MCASP) is a general purpose audio serial port, useful for Time-Division Multiplexd (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for inter-component Digial audio Interface Transmission (DIT). MCASP modules have the following main features:

- Connection to audio Analog-to-Digital Converters (ADC), Digital-to-Analog Converters (DAC), codec, digital audio interface receiver (DIR), and Sony/Philips Digital Interface (S/PDIF) transmit physical layer components
- Support of Time Division Multiplexed (TDM) interface, Inter-IC Sound (I2S) standard, and similar bit stream formats
- Integrated Digital Audio Interface Transmitter (DIT) with enhanced channel status/user data RAM and support of S/PDIF, IEC60958-1, and AES-3 formats
- Independent serializer for each AXRx channel of each MCASP module
- A single 32-bit buffer per serializer for transmit and receive operations
- Support for two DMA requests (one per direction)
- One transmit and one receive interrupt requests common for all serializers
- Two independent clock generator modules for transmit and receive allowing the MCASP to receive and transmit at different rates

1.4.18 Cyclic Redundancy Check

- Memory Cyclic Redundancy Check module used to perform CRC to verify the integrity of a memory system. The MCRC module has the following main feature:
  - Four Channels of CRC Compression based Signature Generation
  - 8, 16, 32, or 64-bit Data Size
  - Maximum Length PSA based on 64-bit Polynomial
  - Programmable 20 bit pattern counter per channel
  - Three Operating Modes: Auto, Semi-CPU, Full CPU
  - MCRC or CPU can perform signature verification for each Channel

  - Timeout Interrupt if CRC is not performed within the time limit

1.4.19 Multi-Media Card/Secure Digital Interface (MMCSD)

Integrated in MAIN domain:

- One controller with 8-bit wide data bus and LVCMOS IO Support
  - Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3
  - Support of eMMC5.1 Host Specification (JESD84-B51)
- Support of SD Host Controller Standard Specification - SDIO 3.00
- eMMC Electrical Standard 5.1 (JESD84-B51)
- Multi-Media card features:
  - Backward compatible with earlier eMMC standards
  - Legacy MMC SDR: 3.3/1.8 V, 8/4/1-bit bus width, 0-25 MHz, 25/12.5/3.125 MB/s
  - High Speed SDR: 3.3/1.8 V, 8/4/1-bit bus width, 0-50 MHz, 50/25/6.25 MB/s
  - HS200 SDR: 1.8 V, 0-200 MHz, 8/4-bit bus width, 200/100 MB/ss
- SD card support: SDIO, SDR12, SDR25, SDR50, SDR104, DDR50

1.4.20 Windowed Watchdog Timer/Real Time Interrupt

- Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module providing timer functionality for operation systems and benchmarking code with the following main features:
  - Two independent 64 bit counter blocks
  - Four configurable compare registers for generating operating system ticks
  - Free running counter 0 can be incremented by either the internal pre-scale counter or by an external event
  - Selectable RTI clock input (derived from any of the available clock sources)
  - Fast enabling/disabling of events

1.4.21 Serial Peripheral Interface (SPI)

Integrated the device are instances of the Serial Peripheral Interface (SPI) module with the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four channels in controller mode, or single channel in receiver mode
- Support for various controller multichannel modes
- Single interrupt line for multiple interrupt source events
- Support of start-bit write command
- Support of start-bit pause and break sequence
- Built-in FIFO available for a single channel

Note

SPI also goes by MCSPI. Learn more about SPI instances in *Multichannel Serial Peripheral Interface (MCSPI)*.

1.4.22 Spinlock (SPINLOCK)

One Spinlock module with (256 hardware semaphores) for synchronizing the processes running on multiple cores in the device.

1.4.23 Universal Asynchronous Receiver/Transmitter (UART)

The device has several instances of the configurable Universal Asynchronous Receiver/Transmitter (UART) interface module have the following main features:

- 16C750-compatible interface
- Support of RS-485 external transceiver auto flow control
- Dual 64-byte FIFOs – one per each received and transmitted data paths
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode

- Baud-rate from 300 bits/s up to 3.6864 Mbits/s with 48 MHz functional clock
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Support of IrDA 1.4 Slow Infrared (SIR), Medium Infrared (MIR), and Fast Infrared (FIR) communications
- Support of Consumer Infrared Remote control mode (CIR) with programmable data encoding

Note

Only one UART instance has support for support full modem control functions. All other UART instances will support only the TX, RX, RTS, and CTS signals.

1.4.24 Universal Serial Bus (USB) Subsystem 2.0

Instantiated in MAIN domain: Two instances One instance of the Universal Serial Bus (USB) subsystem with integrated USB2.0 PHY module has the following main features:

- Dual-Role Device (DRD) capability
- Support of Peripheral (aka Device) mode at High Speed (HS at 480 Mbps) and Full Speed (FS at 12 Mbps)
- Support of Host mode at High Speed (HS at 480 Mbps), Full Speed (FS at 12 Mbps), and Low Speed (LS at 1.5 Mbps)
- Support of Host Negotiation Protocol (HNP)
- Support of USB3 low power protocol states (U1, U2, and U3)
- USB instance contains a single xHCI compliant with xHCI 1.0 specification with internal DMA controller
- Embedded USB 2.0 PHY

1.4.25 TIMER

- Dual mode Timer (TIMER) module with support of the following main features:
  - Free running 32-bit upward counter
  - Generates a 1-ms tick with a 32.768-kHz functional clock
  - Interrupts generated on overflow, compare and capture
  - Supported modes of operation: compare and capture, auto-reload and start-stop
  - Programmable divider clock source (2^n, where n = [0-8])
  - Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
  - On-the-fly read/write register (while counting) for systems operation and benchmarking code

1.5 Device Top Level Domain

This section describes the modules integrated in the device Top Level Domain

1.5.1 Dual Clock Comparator

- Dual Clock Comparator (DCC) modules, used to determine the accuracy of a clock signal during the time execution of an application, each having the following main features:
  - Two independent counter blocks count clock pulses from each clock source
  - Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
  - Configurable time base for error signal
  - Error signal generation when one of the clocks is out of spec
  - Clock frequency measurement

1.5.2 MCU Error Signaling Module

- Error Signaling Module (MCU_ESM) for safety-related events and/or errors aggregation from throughout the device into one location supports the following main features:
  - Up to 1024 level or pulse error event inputs
  - Selectable low and high priority interrupt error pin prioritization of each error event
  - Single Error Pin output to signal severe device failure to outside world
  - Configurable time base for error signal
  - Triple Redundant Pulse Inputs
  - Two Priority Levels

  - Error Forcing capability
  - Internal redundant flops on safety critical fields

1.5.3 General Purpose Input/Output Interface

General Purpose Input/Output (GPIO) module provide dedicated general-purpose pins that can be configured as either inputs or outputs. The GPIO module main features includes:

- Support of 9 banks x 16 GPIO pins
- Support of up to 9 banks of interrupt capable GPIOs
- Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO pin
- Set/clear functionality per individual GPIO pin

1.6 Device WKUP Domain

This section describes the modules integrated in the device WKUP domain.

1.6.1 Global Time Counter

- Global Time Counter (GTC) module that can be used for time synchronization and debug trace time stamping with the following main features:
  - 64-bit up counter
  - No rollover during the lifetime of the device
  - Compatible with Armv8 system counter requirements
  - Outputs reflected binary (Gray) encoded timer value for system timer bus distribution to other modules
  - Selectable counter bit output as a push event that can be used by CPTS modules, timers or interface protocols

1.6.2 Inter-Integrated Circuit Interface (I2C)

One Multi-controller Inter-Integrated Circuit (I2C) interface module, with the following main features:

- 1x Instances with open-drain voltage buffers in compliance with the Philips I2C-bus specification version 2.1
- Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Support of 7-bit and 10-bit device addressing modes
- 8-bit-wide data access
- Support of multi-controller transmitter/peripheral receiver and receiver/peripheral transmitter modes
- Built-in FIFOs with fixed size of 32 bytes.
- Support of Auto Idle, Idle Request/Idle Acknowledge handshake, and Asynchronous wake-up mechanisms
- Low power consumption

1.6.3 Arm Cortex-R5F Processor (R5FSS)

The ARM Cortex-R5F processor subsystem (R5FSS) supports the following main features:

- Armv7-R architecture
- R5FSS Memory System
  - 32KB Instruction Cache
    - 4x8KB ways
    - SECDED ECC protected per 64 bits
  - 32KB Data Cache
    - 4x8KB ways
    - SECDED ECC protected per 64 bits
  - 64KB tightly-coupled memory (TCM) per CPU
    - SECDED ECC protected per 32 bits
    - TCM hard error cache Implemented in CPU
    - Readable/writable from system
    - TCMs initialized (to 0's) at reset
    - 32KB TCMA (ATCM)
    - 16KB TCMB0 (B0TCM)

    - 16KB TCMB1 (B1TCM)
- Full-precision Floating Point (VFPv3)
- 16-region Memory Protection Unit (MPU)
- 8 breakpoints, 8 watch points
- CoreSight Debug Access Port (DAP)
- CoreSight ETM-R5 interface (CTI, ETM)
- Performance Monitoring Unit (PMU)
- 32-bit to 36-bit Region-based Address Translation (RAT) on memory access initiators
- Integrated Vectored Interrupt Manager (VIM) per core with 256 Interrupt Inputs each
  - Programmable interrupt priority (4-bit)
  - Programmable interrupt enable mask
  - Software-generated interrupts
  - Synchronous clock domain crossing on all core interfaces

Note

CORE0 has 64KB of TCM.

Note

These details describe a superset of the R5FSS memory configuration. For additional details on device memory availability, please refer to the device-specific Datasheet.

1.6.4 Universal Asynchronous Receiver/Transmitter (UART)

Instances of the configurable Universal Asynchronous Receiver/Transmitter (UART) interface module have the following main features:

- 16C750-compatible interface
- Support of RS-485 external transceiver auto flow control
- Dual 64-byte FIFOs – one per each received and transmitted data paths
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode
- Baud-rate from 300 bits/s up to 3.6864 Mbits/s with 48 MHz functional clock
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Support of IrDA 1.4 Slow Infrared (SIR), Medium Infrared (MIR), and Fast Infrared (FIR) communications
- Support of Consumer Infrared Remote control mode (CIR) with programmable data encoding

1.6.5 MCU Windowed Watchdog Timer/Real Time Interrupt

- Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module providing timer functionality for operation systems and benchmarking code with the following main features:
  - Two independent 64 bit counter blocks
  - Four configurable compare registers for generating operating system ticks
  - Free running counter 0 can be incremented by either the internal pre-scale counter or by an external event
  - Selectable RTI clock input (derived from any of the available clock sources)
  - Windowed Watchdog Timer (WWDT) feature
  - Some RTI modules are pre-dedicated to specific processor cores

1.6.6 MCU TIMER

- Timer modules with support of the following main features:
  - Free running 32-bit upward counter
  - Generates a 1-ms tick with a 32.768-kHz functional clock
  - Interrupts generated on overflow, compare and capture
  - Supported modes of operation: compare and capture, auto-reload and start-stop
  - Programmable divider clock source (2n, where n = [0-8])

- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- On-the-fly read/write register (while counting) for systems operation and benchmarking code
- Each odd numbered timer instance may be optionally cascaded with the previous even numbered timer instance to form up to a 64-bit timer

1.7 Device Identification

The device part number identification data can be read in the WKUP_CTRL_MMR_CFG0_JTAG_USER_ID register. See the below table for more information.

Table 1-1. Device Part Number Identifier

WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register Field	Value and Description	Comment
[31:24] RESERVED	Reserved	
[23:18] PART	Number of R5 Cores	
	1 = AM2751 = 1 R5 instance	
	2 = AM2752 = 2 R5 instances	
	4 = AM2754 = 4 R5 instances	
	Others = Reserved	
[17:13] SRAM Memory and Speed	1 = A designator	Refer to *SRAM Memory and Speed* table below for details on the designator
	2 = B designator	
	3 = C designator	
	4 = D designator	
	5 = E designator	
	6 = F designator	
[12:11] DSP	1 = 1 DSP instance	
	2 = 2 DSP instances	
	Others = Reserved	
[10:7] SW Bundle	Software Bundle Type 0 = Z and F SW Bundle designator 1 = W SW Bundle designator	F as the 11th character is only present in the preproduction material.
[6:4] TEMP	Temperature grade. 4 = -40°C to 105°C 5 = -40°C to 125°C	Operating junction temperature range.
	Others = Reserved	
[3:0] PKG	5= ANJ Others = Reserved	Device Package type.

Table 1-2. SRAM Memory and Speed

Designator	SRAM Memory Size	R5 Speed	C7 Speed
A	1MB	400MHz	250MHz
B	2MB	400MHz	400MHz
C	2.5MB	800MHz	400MHz
D	4.5MB	800MHz	500MHz
E	5.5MB	800MHz	750MHz
F	6MB	1000MHz	1000MHz

Note

Pre-production material follows a different format in WKUP_CTRL_MMR_CFG0_JTAG_USER_ID.

2 Memory Map

Note

This TRM uses the prefix of "MCU_" for items that refer to the device as a whole instead of a specific domain. "MCU_" is the equivalent of Top Level from Section 1.5.

2.1 SoC Memory Map View

Since AM275 is built on 36b physical address. The R5 processors support only a 32b physical address space. In order to allow these micro controllers accessing the full 36b physical address space, a region based remapping module is dedicated for each processor.

Table 2-1. MAIN Memory Map

Region Name	Start Address	End Address	Size
PSRAMECC0_RAM	0x0000000000	0x00000003FF	1KB
PADCFG_CTRL0_CFG0	0x00000F0000	0x00000F7FFF	32KB
CTRL_MMR0_CFG0	0x0000100000	0x000011FFFF	128KB
CBASS_DBG0_ERR	0x0000200000	0x00002003FF	1KB
CBASS_INFRA1_ERR	0x0000210000	0x00002103FF	1KB
CBASS_FW0_ERR	0x0000220000	0x00002203FF	1KB
AM275_MAIN_IPCSS_CBASS0_ERR	0x0000230000	0x00002303FF	1KB
EFUSE0	0x0000300000	0x00003000FF	256B
PBIST7	0x0000340000	0x00003403FF	1KB
PBIST8	0x0000350000	0x00003503FF	1KB
C7X256V0_PBIST	0x0000360000	0x00003603FF	1KB
C7X256V1_PBIST	0x0000370000	0x00003703FF	1KB
PBIST0	0x0000390000	0x00003903FF	1KB
PBIST1	0x00003A0000	0x00003A03FF	1KB
PBIST2	0x00003B0000	0x00003B03FF	1KB
PBIST3	0x00003C0000	0x00003C03FF	1KB
PBIST4	0x00003D0000	0x00003D03FF	1KB
PBIST5	0x00003E0000	0x00003E03FF	1KB
PBIST6	0x00003F0000	0x00003F03FF	1KB
MAIN_PSC0_PSC	0x0000400000	0x0000400FFF	4KB
PLLCTRL0	0x0000410000	0x00004101FF	512B
ESM0_CFG	0x0000420000	0x0000420FFF	4KB
DFTSS0_MEM	0x0000500000	0x00005003FF	1KB
DDPA0	0x0000580000	0x00005803FF	1KB
GPIO0	0x0000600000	0x00006000FF	256B
GPIO1	0x0000601000	0x00006010FF	256B
PLL0_CFG	0x0000680000	0x000068FFFF	64KB
PSRAMECC0_ECC_AGGR	0x0000700000	0x00007003FF	1KB
USB0_DEBUG_TRACE_MMR_TRACE_VBUSP_USB2SS_DEBUG_TRACE	0x0000703000	0x00007031FF	512B
CPSW0_CPSW_NUSS_VBUSP_ECC	0x0000704000	0x00007043FF	1KB
MMCSD0_ECC_AGGR_RXMEM	0x0000708000	0x00007083FF	1KB
MMCSD0_ECC_AGGR_TXMEM	0x0000709000	0x00007093FF	1KB
SA3_SS0_ECC_AGGR	0x0000712000	0x00007123FF	1KB
FSS0_OSPI0_ECC_AGGR	0x0000716000	0x00007163FF	1KB
FSS0_FSAS_ECC_AGGR	0x0000717000	0x00007173FF	1KB
C7X256V0_ECC_AGGR	0x000071A000	0x000071A3FF	1KB
C7X256V1_ECC_AGGR	0x000071B000	0x000071B3FF	1KB
MSRAM_1MB0_ECC_AGGR_REGS	0x000071C000	0x000071C3FF	1KB
MSRAM_1MB1_ECC_AGGR_REGS	0x000071D000	0x000071D3FF	1KB
MSRAM_1MB2_ECC_AGGR_REGS	0x000071E000	0x000071E3FF	1KB
MSRAM_1MB3_ECC_AGGR_REGS	0x000071F000	0x000071F3FF	1KB
MSRAM_1MB4_ECC_AGGR_REGS	0x0000720000	0x00007203FF	1KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
MSRAM_1MB5_ECC_AGGR_REGS	0x0000721000	0x00007213FF	1KB
FSS1_HPB_ECC_AGGR	0x0000722000	0x00007223FF	1KB
FSS1_OSPI1_ECC_AGGR	0x0000723000	0x00007233FF	1KB
ADC0_ECC	0x0000729000	0x00007293FF	1KB
R5FSS0_CORE0_ECC_AGGR	0x0000730000	0x00007303FF	1KB
R5FSS1_CORE0_ECC_AGGR	0x0000731000	0x00007313FF	1KB
DCC0	0x0000800000	0x000080003F	64B
DCC1	0x0000804000	0x000080403F	64B
DCC2	0x0000808000	0x000080803F	64B
DCC3	0x000080C000	0x000080C03F	64B
DCC4	0x0000810000	0x000081003F	64B
DCC5	0x0000814000	0x000081403F	64B
DCC6	0x0000818000	0x000081803F	64B
DCC7	0x000081C000	0x000081C03F	64B
DCC8	0x0000820000	0x000082003F	64B
MAIN_GPIOMUX_INTROUTER0_INTR_ROUTER_CFG	0x0000A00000	0x0000A00FFF	4KB
TIMESYNC_EVENT_INTROUTER0_INTR_ROUTER_CFG	0x0000A40000	0x0000A403FF	1KB
WKUP_GTC0_CFG0	0x0000A80000	0x0000A803FF	1KB
WKUP_GTC0_CFG1	0x0000A90000	0x0000A93FFF	16KB
WKUP_GTC0_CFG2	0x0000AA0000	0x0000AA3FFF	16KB
WKUP_GTC0_CFG3	0x0000AB0000	0x0000AB3FFF	16KB
WKUP_VTM0_VTM_CFG1	0x0000B00000	0x0000B003FF	1KB
WKUP_VTM0_VTM_CFG2	0x0000B01000	0x0000B013FF	1KB
WKUP_VTM0_ECCAGGR_CFG	0x0000B02000	0x0000B023FF	1KB
PDMA0	0x0000C00000	0x0000C003FF	1KB
PDMA1	0x0000C01000	0x0000C013FF	1KB
PDMA4_REGS	0x0000C02000	0x0000C023FF	1KB
TIMER0_CFG	0x0002400000	0x00024003FF	1KB
TIMER1_CFG	0x0002410000	0x00024103FF	1KB
TIMER2_CFG	0x0002420000	0x00024203FF	1KB
TIMER3_CFG	0x0002430000	0x00024303FF	1KB
TIMER4_CFG	0x0002440000	0x00024403FF	1KB
TIMER5_CFG	0x0002450000	0x00024503FF	1KB
TIMER6_CFG	0x0002460000	0x00024603FF	1KB
TIMER7_CFG	0x0002470000	0x00024703FF	1KB
TIMER8_CFG	0x0002480000	0x00024803FF	1KB
TIMER9_CFG	0x0002490000	0x00024903FF	1KB
TIMER10_CFG	0x00024A0000	0x00024A03FF	1KB
TIMER11_CFG	0x00024B0000	0x00024B03FF	1KB
TIMER12_CFG	0x00024C0000	0x00024C03FF	1KB
TIMER13_CFG	0x00024D0000	0x00024D03FF	1KB
TIMER14_CFG	0x00024E0000	0x00024E03FF	1KB
TIMER15_CFG	0x00024F0000	0x00024F03FF	1KB
UART0	0x0002800000	0x00028001FF	512B
UART1	0x0002810000	0x00028101FF	512B
UART2	0x0002820000	0x00028201FF	512B
UART3	0x0002830000	0x00028301FF	512B

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
UART4	0x0002840000	0x00028401FF	512B
UART5	0x0002850000	0x00028501FF	512B
UART6	0x0002860000	0x00028601FF	512B
MCASP0_CFG	0x0002B00000	0x0002B01FFF	8KB
MCASP0_DMA	0x0002B08000	0x0002B083FF	1KB
MCASP1_CFG	0x0002B10000	0x0002B11FFF	8KB
MCASP1_DMA	0x0002B18000	0x0002B183FF	1KB
MCASP2_CFG	0x0002B20000	0x0002B21FFF	8KB
MCASP2_DMA	0x0002B28000	0x0002B283FF	1KB
MCASP3_CFG	0x0002B30000	0x0002B31FFF	8KB
MCASP3_DMA	0x0002B38000	0x0002B383FF	1KB
MCASP4_CFG	0x0002B40000	0x0002B41FFF	8KB
MCASP4_DMA	0x0002B48000	0x0002B483FF	1KB
AASRC0_CFG	0x0002D00000	0x0002D03FFF	16KB
AASRC0_DATA_R0	0x0002D10000	0x0002D13FFF	16KB
AASRC0_DATA_R1	0x0002D20000	0x0002D23FFF	16KB
AASRC1_CFG	0x0002D40000	0x0002D43FFF	16KB
AASRC1_DATA_R0	0x0002D50000	0x0002D53FFF	16KB
AASRC1_DATA_R1	0x0002D60000	0x0002D63FFF	16KB
MLB0_MMR_MMRVBP	0x0002F80000	0x0002F801FF	512B
MLB0_VBP2APB_WRAP_MLB_CFG_VBP_MLBDIM	0x0002F82000	0x0002F823FF	1KB
MLB0_RAT_WRAP_RAT_CFG_VBP_MMRS	0x0002F83000	0x0002F83FFF	4KB
WKUP_PSC0_PSC	0x0004000000	0x0004000FFF	4KB
MCU_PLLCTRL0	0x0004020000	0x00040201FF	512B
WKUP_ECC_AGGR2_ECC_AGGR	0x0004030000	0x00040303FF	1KB
WKUP_PLL0_CFG	0x0004040000	0x0004040FFF	4KB
MCU_PADCFG_CTRL0_CFG0	0x0004080000	0x0004087FFF	32KB
WKUP_ESM0_CFG	0x0004100000	0x0004100FFF	4KB
MCU_GPIO0	0x0004201000	0x00042010FF	256B
MCU_MCU_GPIOMUX_INTROUTER0_INTR_ROUTER_CFG	0x0004210000	0x00042103FF	1KB
MCU_CTRL_MMR0_CFG0	0x0004500000	0x000451FFFF	128KB
WKUP_CBASS_SAFE1_ERR	0x0004600000	0x00046003FF	1KB
MCU_DCC0	0x0004C00000	0x0004C0003F	64B
MCU_DCC1	0x0004C10000	0x0004C1003F	64B
R5FSS0_COMPARE_CFG	0x0005B00000	0x0005B000FF	256B
R5FSS0_EVNT_BUS_VBUSP_MMRS	0x0005B01000	0x0005B010FF	256B
R5FSS0_CORE1_ECC_AGGR	0x0005B02000	0x0005B023FF	1KB
R5FSS1_COMPARE_CFG	0x0005B20000	0x0005B200FF	256B
R5FSS1_EVNT_BUS_VBUSP_MMRS	0x0005B21000	0x0005B210FF	256B
R5FSS1_CORE1_ECC_AGGR	0x0005B22000	0x0005B223FF	1KB
R5FSS0_CORE0_ATCM	0x0005C00000	0x0005C0FFFF	64KB
R5FSS0_CORE0_BTCM	0x0005C10000	0x0005C1FFFF	64KB
R5FSS0_CORE1_ATCM	0x0005D00000	0x0005D07FFF	32KB
R5FSS0_CORE1_BTCM	0x0005D10000	0x0005D17FFF	32KB
R5FSS1_CORE0_ATCM	0x0005E00000	0x0005E0FFFF	64KB
R5FSS1_CORE0_BTCM	0x0005E10000	0x0005E1FFFF	64KB
R5FSS1_CORE1_ATCM	0x0005F00000	0x0005F07FFF	32KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
R5FSS1_CORE1_BTCM	0x0005F10000	0x0005F17FFF	32KB
MLB0_MLBDIM_WRAP_ECC_AGGR_VBP	0x00072A0000	0x00072A03FF	1KB
CPSW0_CPSW_NUSS_VBUSP	0x0008000000	0x00081FFFFF	2MB
RTI4_CFG	0x000E000000	0x000E0000FF	256B
RTI5_CFG	0x000E010000	0x000E0100FF	256B
USB0_MMR_MMRVBP_USB2SS_CFG	0x000F900000	0x000F9007FF	2KB
USB0_PHY2	0x000F908000	0x000F9083FF	1KB
USB0_ECC_AGGR	0x000F980000	0x000F9803FF	1KB
MMCSD0_CTL_CFG	0x000FA00000	0x000FA00FFF	4KB
MMCSD0_SS_CFG	0x000FA08000	0x000FA083FF	1KB
FSS0_CFG	0x000FC00000	0x000FC000FF	256B
FSS0_FSAS_CFG	0x000FC10000	0x000FC100FF	256B
FSS0_OTFA_CFG	0x000FC20000	0x000FC20FFF	4KB
FSS1_HPB_SS_CFG	0x000FC30000	0x000FC300FF	256B
FSS1_HPB_CTRL	0x000FC34000	0x000FC340FF	256B
FSS0_OSPI0_CTRL	0x000FC40000	0x000FC400FF	256B
FSS0_OSPI0_SS_CFG	0x000FC44000	0x000FC441FF	512B
FSS0_FOTA_CFG	0x000FC60000	0x000FC600FF	256B
FSS0_FOTA_PDMEM_CFG	0x000FC61000	0x000FC617FF	2KB
FSS0_FOTA_IMEM_CFG	0x000FC62000	0x000FC620FF	256B
FSS0_WBUF_CFG	0x000FC63000	0x000FC631FF	512B
FSS1_CFG	0x000FC80000	0x000FC800FF	256B
FSS1_FSAS_CFG	0x000FC90000	0x000FC900FF	256B
FSS1_OTFA_CFG	0x000FCA0000	0x000FCA0FFF	4KB
FSS1_OSPI1_CTRL	0x000FCC0000	0x000FCC00FF	256B
FSS1_OSPI1_SS_CFG	0x000FCC4000	0x000FCC41FF	512B
ATL0_REG	0x000FEE0000	0x000FEE03FF	1KB
CBASS_MCASP0_ERR	0x000FEF0000	0x000FEF03FF	1KB
I2C0_CFG	0x0020000000	0x00200000FF	256B
I2C1_CFG	0x0020010000	0x00200100FF	256B
I2C2_CFG	0x0020020000	0x00200200FF	256B
I2C3_CFG	0x0020030000	0x00200300FF	256B
I2C4_CFG	0x0020040000	0x00200400FF	256B
I2C5_CFG	0x0020050000	0x00200500FF	256B
I2C6_CFG	0x0020060000	0x00200600FF	256B
MCSPI0_CFG	0x0020100000	0x00201003FF	1KB
MCSPI1_CFG	0x0020110000	0x00201103FF	1KB
MCSPI2_CFG	0x0020120000	0x00201203FF	1KB
MCSPI3_CFG	0x0020130000	0x00201303FF	1KB
MCSPI4_CFG	0x0020140000	0x00201403FF	1KB
CBASS_MISC_PERI0_ERR	0x00201F0000	0x00201F03FF	1KB
CBASS_MEM0_ERR	0x0020200000	0x00202003FF	1KB
ADC0_ADC	0x0020600000	0x00206003FF	1KB
ADC0_ADC12_FIFO_DMA	0x0020608000	0x00206083FF	1KB
MCAN0_SS	0x0020700000	0x00207000FF	256B
MCAN0_CFG	0x0020701000	0x00207011FF	512B
MCAN0_MSGMEM_RAM	0x0020708000	0x002070FFFF	32KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
MCAN1_SS	0x0020710000	0x00207100FF	256B
MCAN1_CFG	0x0020711000	0x00207111FF	512B
MCAN1_MSGMEM_RAM	0x0020718000	0x002071FFFF	32KB
MCAN2_SS	0x0020720000	0x00207200FF	256B
MCAN2_CFG	0x0020721000	0x00207211FF	512B
MCAN2_MSGMEM_RAM	0x0020728000	0x002072FFFF	32KB
MCAN3_SS	0x0020730000	0x00207300FF	256B
MCAN3_CFG	0x0020731000	0x00207311FF	512B
MCAN3_MSGMEM_RAM	0x0020738000	0x002073FFFF	32KB
MCAN4_SS	0x0020740000	0x00207400FF	256B
MCAN4_CFG	0x0020741000	0x00207411FF	512B
MCAN4_MSGMEM_RAM	0x0020748000	0x002074FFFF	32KB
RTI0_CFG	0x0020800000	0x00208000FF	256B
RTI1_CFG	0x0020810000	0x00208100FF	256B
RTI2_CFG	0x0020820000	0x00208200FF	256B
RTI3_CFG	0x0020830000	0x00208300FF	256B
EPWM0_EPWM	0x0023000000	0x00230000FF	256B
EPWM1_EPWM	0x0023010000	0x00230100FF	256B
EPWM2_EPWM	0x0023020000	0x00230200FF	256B
ECAP0_CTL_STS	0x0023100000	0x00231000FF	256B
ECAP1_CTL_STS	0x0023110000	0x00231100FF	256B
ECAP2_CTL_STS	0x0023120000	0x00231200FF	256B
ECAP3_CTL_STS	0x0023130000	0x00231300FF	256B
ECAP4_CTL_STS	0x0023140000	0x00231400FF	256B
ECAP5_CTL_STS	0x0023150000	0x00231500FF	256B
MCAN0_ECC_AGGR	0x0024018000	0x00240183FF	1KB
MCAN1_ECC_AGGR	0x0024019000	0x00240193FF	1KB
MCAN2_ECC_AGGR	0x002401A000	0x002401A3FF	1KB
MCAN3_ECC_AGGR	0x002401B000	0x002401B3FF	1KB
MCAN4_ECC_AGGR	0x002401C000	0x002401C3FF	1KB
RL2_0_RL2_OF_CBA4	0x0025000000	0x00250003FF	1KB
RL2_2_RL2_OF_CBA4	0x0025002000	0x00250023FF	1KB
RL2_3_RL2_OF_CBA4	0x0025003000	0x00250033FF	1KB
MAILBOX0_REGS0	0x0029000000	0x00290001FF	1KB
MAILBOX0_REGS1	0x0029010000	0x00290101FF	512B
MAILBOX0_REGS2	0x0029020000	0x00290201FF	512B
MAILBOX0_REGS3	0x0029030000	0x00290301FF	512B
MAILBOX0_REGS4	0x0029040000	0x00290401FF	512B
MAILBOX0_REGS5	0x0029050000	0x00290501FF	512B
MAILBOX0_REGS6	0x0029060000	0x00290601FF	512B
MAILBOX0_REGS7	0x0029070000	0x00290701FF	512B
SPINLOCK0	0x002A000000	0x002A007FFF	512B
WKUP_RTI0_CFG	0x002B000000	0x002B0000FF	32KB
WKUP_TIMER0_CFG	0x002B100000	0x002B1003FF	256B
WKUP_TIMER1_CFG	0x002B110000	0x002B1103FF	1KB
WKUP_RTCSS0_RTC	0x002B1F0000	0x002B1F007F	1KB
WKUP_I2C0_CFG	0x002B200000	0x002B2000FF	128B

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
WKUP_UART0	0x002B300000	0x002B3001FF	256B
WKUP_CBASS0_ERR	0x002B400000	0x002B4003FF	512B
WKUP_PBIST0	0x002B500000	0x002B5003FF	1KB
WKUP_PBIST1	0x002B501000	0x002B5013FF	1KB
WKUP_ECC_AGGR0_ECC_AGGR	0x002B600000	0x002B6003FF	1KB
WKUP_ECC_AGGR1_ECC_AGGR	0x002B601000	0x002B6013FF	1KB
WKUP_PSRAMECC_8K0_REGS	0x002B608000	0x002B6083FF	1KB
WKUP_PSRAM2KX32E0_REGS	0x002B609000	0x002B6093FF	1KB
C7X256V0	0x0030240000	0x003024FFFF	1KB
C7X256V1	0x0030250000	0x003025FFFF	64KB
MCRC64_0_REGS	0x0030300000	0x0030300FFF	64KB
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_CAP	0x0031000000	0x003100001F	4KB
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_OPER	0x0031000020	0x003100005F	32B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_PORT	0x0031000420	0x003100043F	64B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_RUNTIME	0x0031000440	0x003100045F	32B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_INTR	0x0031000460	0x003100049F	32B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DB	0x0031000560	0x003100075F	64B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_EXTCAP	0x0031000960	0x003100096F	512B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_SUPPRTCAP2	0x0031000970	0x003100097F	16B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_SUPPRTCAP3	0x0031000980	0x003100099F	16B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_GBL	0x003100C100	0x003100C8FF	32B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEV	0x003100C700	0x003100CEFF	2KB
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_LINK	0x003100D000	0x003100D07F	2KB
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEBUG	0x003100D800	0x003100D9FF	128B
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEBUG_RAM0	0x0031040000	0x003104FFFF	512B
CBASS0_ERR	0x003A000000	0x003A0003FF	64KB
WKUP_R5FSS0_EVNT_BUS_VBUSP_MMRS	0x003C018000	0x003C0180FF	1KB
DMASS0_ECCAGGR	0x003F005000	0x003F0053FF	256B
WKUP_R5FSS0_CORE0_ECC_AGGR	0x003F00D000	0x003F00D3FF	1KB
ECC_AGGR1_REGS	0x003F00F000	0x003F00F3FF	1KB
CBASS_CENTRAL2_ERR	0x003F012000	0x003F0123FF	1KB
ECC_AGGR2_ECC_AGGR	0x003F013000	0x003F0133FF	1KB
ECC_AGGR3_REGS	0x003F014000	0x003F0143FF	1KB
IDOM0_MAIN_PLL_ECC_AGGR4_REGS	0x003F015000	0x003F0153FF	1KB
IDOM0_PULSAR_PLL_ECC_AGGR8_REGS	0x003F016000	0x003F0163FF	1KB
IDOM1_MAIN_PLL_ECC_AGGR5_REGS	0x003F017000	0x003F0173FF	1KB
IDOM1_PULSAR_PLL_ECC_AGGR9_REGS	0x003F018000	0x003F0183FF	1KB
IDOM0_MAIN_PLL_ECC_AGGR6_REGS	0x003F019000	0x003F0193FF	1KB
IDOM0_PULSAR_PLL_ECC_AGGR10_REGS	0x003F01A000	0x003F01A3FF	1KB
IDOM1_MAIN_PLL_ECC_AGGR7_REGS	0x003F01B000	0x003F01B3FF	1KB
IDOM1_PULSAR_PLL_ECC_AGGR11_REGS	0x003F01C000	0x003F01C3FF	1KB
SA3_SS0_REGS	0x0040900000	0x0040900FFF	1KB
SA3_SS0_MMRA	0x0040901000	0x00409011FF	4KB
SA3_SS0_EIP_76	0x0040910000	0x004091007F	512B
SA3_SS0_EIP_29T2	0x0040920000	0x004092FFFF	128B
DEBUGSS0_SYS	0x0041000000	0x0041000FFF	64KB
WKUP_ROM0	0x0041800000	0x004183FFFF	4KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
WKUP_PSRAMECC_8K0_RAM	0x0041880000	0x0041887FFF	256KB
WKUP_PSRAM2KX32E0_RAM	0x0041888000	0x0041889FFF	32KB
STM0_STIMULUS	0x0042000000	0x0042FFFFFF	8KB
WKUP_CTRL_MMR0_CFG0	0x0043000000	0x004301FFFF	16MB
SA3_SS0_SEC_PROXY_SRC_TARGET_DATA	0x0043600000	0x004360FFFF	128KB
SA3_SS0_ECCAGGR_CFG	0x0043702000	0x00437023FF	1KB
MSRAM_1MB0_RAM	0x0043C40000	0x0043C7FFFF	64KB
SA3_SS0_PSILCFG_CFG_PROXY	0x0044801000	0x00448011FF	8MB
SA3_SS0_PSILSS_CFG_MMRS	0x0044802000	0x0044802FFF	512B
SA3_SS0_IPCSS_SEC_PROXY_CFG_MMRS	0x0044804000	0x00448040FF	4KB
SA3_SS0_IPCSS_RINGACC_CFG_GCFG	0x0044805000	0x00448053FF	256B
SA3_SS0_INTAGGR_CFG	0x0044808000	0x004480801F	1KB
SA3_SS0_INTAGGR_CFG_IMAP	0x0044809000	0x00448093FF	32B
SA3_SS0_INTAGGR_CFG_MCAST	0x004480A000	0x004480A3FF	1KB
SA3_SS0_INTAGGR_CFG_GCNTCFG	0x004480B000	0x004480B3FF	1KB
SA3_SS0_INTAGGR_CFG_INTR	0x0044810000	0x0044817FFF	1KB
SA3_SS0_INTAGGR_CFG_GCNTRTI	0x0044820000	0x004483FFFF	32KB
SA3_SS0_INTAGGR_CFG_UNMAP	0x0044840000	0x004484FFFF	128KB
SA3_SS0_IPCSS_SEC_PROXY_CFG_SCFG	0x0044860000	0x004487FFFF	64KB
SA3_SS0_IPCSS_SEC_PROXY_CFG_RT	0x0044880000	0x004489FFFF	128KB
SA3_SS0_IPCSS_RINGACC_CFG	0x00448C0000	0x00448FFFFF	128KB
SA3_SS0_PKTDMA_CFG_GCFG	0x0044910000	0x00449100FF	256KB
SA3_SS0_PKTDMA_CFG_RFLOW	0x0044911000	0x00449113FF	256B
SA3_SS0_PKTDMA_CFG_RCHAN	0x0044912000	0x00449123FF	1KB
SA3_SS0_PKTDMA_CFG_TCHAN	0x0044913000	0x00449131FF	1KB
SA3_SS0_PKTDMA_CFG_RCHANRT	0x0044914000	0x0044917FFF	512B
SA3_SS0_PKTDMA_CFG_TCHANRT	0x0044918000	0x0044919FFF	16KB
SA3_SS0_PKTDMA_CFG_RING	0x004491A000	0x004491BFFF	8KB
SA3_SS0_PKTDMA_CFG_RINGRT	0x0044940000	0x004497FFFF	8KB
SA3_SS0_IPCSS_RINGACC_CFG_RT	0x0044C00000	0x0044FFFFFF	256KB
CBASS0_FW	0x0045000000	0x0045007FFF	4MB
WKUP_CBASS0_FW	0x0045008000	0x004500BFFF	16MB
CBASS_CENTRAL2_FW	0x0045010000	0x0045010FFF	16KB
CBASS_INFRA1_FW	0x0045020000	0x00450203FF	4KB
AM275_MAIN_IPCSS_CBASS0_FW	0x0045028000	0x00450287FF	1KB
CBASS_MISC_PERI0_FW	0x0045030000	0x004503FFFF	2KB
CBASS_MEM0_FW	0x0045040000	0x0045041FFF	64KB
DMASS0_PKTDMA_CRED	0x0045810000	0x0045810FFF	1KB
DMASS0_BCDMA_CRED	0x0045812000	0x00458127FF	4KB
WKUP_CBASS0_ISC	0x0045814000	0x0045814FFF	2KB
CBASS0_ISC	0x0045820000	0x0045823FFF	4KB
CBASS_MEM0_ISC	0x0045830000	0x0045833FFF	16KB
CBASS_MISC_PERI0_ISC	0x0045840000	0x0045840FFF	16KB
MAIN_SEC_MMR0_CFG2	0x0045900000	0x004590FFFF	4KB
WKUP_WKUP_SEC_MMR0_CFG2	0x0045920000	0x004593FFFF	64KB
MAIN_SEC_MMR0_CFG0	0x0045A00000	0x0045A0FFFF	128KB
WKUP_WKUP_SEC_MMR0_CFG0	0x0045A20000	0x0045A3FFFF	64KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
AM275_MAIN_IPCSS_CBASS0_GLB	0x0045B01000	0x0045B013FF	1KB
CBASS_MEM0_GLB	0x0045B02000	0x0045B023FF	1KB
WKUP_CBASS0_GLB	0x0045B03000	0x0045B033FF	1KB
CBASS_CENTRAL2_GLB	0x0045B04000	0x0045B043FF	1KB
CBASS0_GLB	0x0045B08000	0x0045B083FF	1KB
CBASS_INFRA1_GLB	0x0045B09000	0x0045B093FF	1KB
CBASS_MISC_PERI0_GLB	0x0045B0A000	0x0045B0A3FF	1KB
WKUP_CBASS0_QOS	0x0045D14000	0x0045D14FFF	1KB
CBASS0_QOS	0x0045D20000	0x0045D23FFF	4KB
CBASS_MEM0_QOS	0x0045D30000	0x0045D33FFF	16KB
CBASS_MISC_PERI0_QOS	0x0045D40000	0x0045D40FFF	16KB
DMASS0_INTAGGR_INTR	0x0048000000	0x00480FFFFF	4KB
DMASS0_INTAGGR_IMAP	0x0048100000	0x0048103FFF	1MB
DMASS0_INTAGGR_CFG	0x0048110000	0x004811001F	16KB
DMASS0_INTAGGR_L2G	0x0048120000	0x00481203FF	32B
DMASS0_PSILCFG_PROXY	0x0048130000	0x00481301FF	1KB
DMASS0_PSILSS_MMRS	0x0048140000	0x0048140FFF	512B
DMASS0_INTAGGR_UNMAP	0x0048180000	0x004819FFFF	4KB
DMASS0_INTAGGR_MCAST	0x0048210000	0x0048210FFF	128KB
DMASS0_INTAGGR_GCNTCFG	0x0048220000	0x0048221FFF	4KB
DMASS0_RINGACC_GCFG	0x0048240000	0x00482403FF	8KB
DMASS0_SEC_PROXY_MMRS	0x0048250000	0x00482500FF	1KB
DMASS0_BCDMA_BCHAN	0x0048420000	0x0048421FFF	256B
DMASS0_PKTDMA_RFLOW	0x0048430000	0x0048430FFF	8KB
DMASS0_PKTDMA_TCHAN	0x00484A0000	0x00484A3FFF	4KB
DMASS0_BCDMA_TCHAN	0x00484A4000	0x00484A7FFF	16KB
DMASS0_PKTDMA_RCHAN	0x00484C0000	0x00484C1FFF	16KB
DMASS0_BCDMA_RCHAN	0x00484C4000	0x00484C7FFF	8KB
DMASS0_PKTDMA_GCFG	0x00485C0000	0x00485C00FF	16KB
DMASS0_BCDMA_GCFG	0x00485C0100	0x00485C01FF	256B
DMASS0_PKTDMA_RING	0x00485E0000	0x00485EFFFF	256B
DMASS0_BCDMA_RING	0x0048600000	0x0048607FFF	64KB
DMASS0_RINGACC_RT	0x0049000000	0x00493FFFFF	32KB
DMASS0_RINGACC_CFG	0x0049800000	0x004983FFFF	4MB
DMASS0_INTAGGR_GCNTRTI	0x004A000000	0x004A0FFFFF	256KB
DMASS0_SEC_PROXY_SCFG	0x004A400000	0x004A47FFFF	1MB
DMASS0_SEC_PROXY_RT	0x004A600000	0x004A67FFFF	512KB
DMASS0_PKTDMA_RCHANRT	0x004A800000	0x004A81FFFF	512KB
DMASS0_BCDMA_RCHANRT	0x004A840000	0x004A87FFFF	128KB
DMASS0_PKTDMA_TCHANRT	0x004AA00000	0x004AA3FFFF	256KB
DMASS0_BCDMA_TCHANRT	0x004AA40000	0x004AA7FFFF	256KB
DMASS0_PKTDMA_RINGRT	0x004B800000	0x004B9FFFFF	256KB
DMASS0_BCDMA_RINGRT	0x004BC00000	0x004BCFFFFF	2MB
DMASS0_BCDMA_BCHANRT	0x004C000000	0x004C03FFFF	1MB
DMASS0_SEC_PROXY_SRC_TARGET_DATA	0x004D000000	0x004D07FFFF	256KB
FSS1_OSPI1_R1	0x0058000000	0x005FFFFFFF	512KB
FSS0_DAT_REG1	0x0060000000	0x0067FFFFFF	128MB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
FSS1_DAT_REG1	0x0068000000	0x006FFFFFFF	128MB
MSRAM_1MB0_RAM	0x0072000000	0x00720FFFFF	128MB
MSRAM_1MB1_RAM	0x0072100000	0x00721FFFFF	1MB
MSRAM_1MB2_RAM	0x0072200000	0x00722FFFFF	1MB
MSRAM_1MB3_RAM	0x0072300000	0x00723FFFFF	1MB
MSRAM_1MB4_RAM	0x0072400000	0x00724FFFFF	1MB
MSRAM_1MB5_RAM	0x0072500000	0x00725FFFFF	1MB
WKUP_R5FSS0_CORE0_ICACHE	0x0074000000	0x00747FFFFF	1MB
WKUP_R5FSS0_CORE0_DCACHE	0x0074800000	0x0074FFFFFF	8MB
R5FSS0_CORE0_ICACHE	0x0076000000	0x00767FFFFF	8MB
R5FSS0_CORE0_DCACHE	0x0076800000	0x0076FFFFFF	8MB
R5FSS0_CORE1_ICACHE	0x0077000000	0x00777FFFFF	8MB
R5FSS0_CORE1_DCACHE	0x0077800000	0x0077FFFFFF	8MB
WKUP_R5FSS0_CORE0_ATCM	0x0078000000	0x0078007FFF	8MB
WKUP_R5FSS0_CORE0_BTCM	0x0078100000	0x0078107FFF	32KB
R5FSS1_CORE0_ICACHE	0x0079000000	0x00797FFFFF	32KB
R5FSS1_CORE0_DCACHE	0x0079800000	0x0079FFFFFF	8MB
R5FSS1_CORE1_ICACHE	0x007A000000	0x007A7FFFFF	8MB
R5FSS1_CORE1_DCACHE	0x007A800000	0x007AFFFFFF	8MB
C7X256V0_UMC	0x007C000000	0x007C01FFFF	8MB
C7X256V0_CLEC	0x007C200000	0x007C2FFFFF	128KB
C7X256V0_DRU	0x007C400000	0x007C403FFF	1MB
C7X256V0_DRU_SET	0x007C404000	0x007C407FFF	16KB
C7X256V0_DRU_QUEUE	0x007C408000	0x007C40FFFF	16KB
C7X256V0_DRU_CHNRT	0x007C440000	0x007C45FFFF	32KB
C7X256V0_DRU_CHRT	0x007C460000	0x007C47FFFF	128KB
C7X256V0_DRU_CHATOMIC_DEBUG	0x007C480000	0x007C49FFFF	128KB
C7X256V0_DRU_CHCORE	0x007C4A0000	0x007C4BFFFF	128KB
C7X256V0_DRU	0x007C4E0000	0x007C4FFFFF	128KB
C7X256V1_UMC	0x007D000000	0x007D01FFFF	128KB
C7X256V1_CLEC	0x007D200000	0x007D2FFFFF	128KB
C7X256V1_DRU	0x007D400000	0x007D403FFF	1MB
C7X256V1_DRU_SET	0x007D404000	0x007D407FFF	16KB
C7X256V1_DRU_QUEUE	0x007D408000	0x007D40FFFF	16KB
C7X256V1_DRU_CHNRT	0x007D440000	0x007D45FFFF	32KB
C7X256V1_DRU_CHRT	0x007D460000	0x007D47FFFF	128KB
C7X256V1_DRU_CHATOMIC_DEBUG	0x007D480000	0x007D49FFFF	128KB
C7X256V1_DRU_CHCORE	0x007D4A0000	0x007D4BFFFF	128KB
C7X256V1_DRU	0x007D4E0000	0x007D4FFFFF	128KB
C7X256V0_UMC_MEM_MAIN	0x007E000000	0x007E1FFFFF	128KB
C7X256V0_UMC_MEM_AUX	0x007E200000	0x007E23FFFF	2MB
C7X256V1_UMC_MEM_MAIN	0x007F000000	0x007F1FFFFF	256KB
C7X256V1_UMC_MEM_AUX	0x007F200000	0x007F23FFFF	2MB
FSS1_DAT_REG0	0x0200000000	0x02FFFFFFFF	256KB
FSS1_DAT_REG3	0x0300000000	0x03FFFFFFFF	4GB
FSS0_DAT_REG0	0x0400000000	0x04FFFFFFFF	4GB
FSS0_DAT_REG3	0x0500000000	0x05FFFFFFFF	4GB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
FSS1_OSPI1_R0	0x0600000000	0x06FFFFFFFF	4GB
DEBUGSS_WRAP0_ROM_TABLE_0_0	0x0700000000	0x0700000FFF	4GB
DEBUGSS_WRAP0_RESV0_0	0x0700001000	0x0700001FFF	4KB
DEBUGSS_WRAP0_CFGAP0	0x0700002000	0x07000020FF	4KB
DEBUGSS_WRAP0_APBAP0	0x0700002100	0x07000021FF	256B
DEBUGSS_WRAP0_AXIAP0	0x0700002200	0x07000022FF	256B
DEBUGSS_WRAP0_PWRAP0	0x0700002300	0x07000023FF	256B
DEBUGSS_WRAP0_PVIEW0	0x0700002400	0x07000024FF	256B
DEBUGSS_WRAP0_JTAGAP0	0x0700002500	0x07000025FF	256B
DEBUGSS_WRAP0_SECAP0	0x0700002600	0x07000026FF	256B
DEBUGSS_WRAP0_CORTEX0_CFG0	0x0700002700	0x07000027FF	256B
DEBUGSS_WRAP0_CORTEX1_CFG0	0x0700002800	0x07000028FF	256B
DEBUGSS_WRAP0_CORTEX2_CFG0	0x0700002900	0x07000029FF	256B
DEBUGSS_WRAP0_CORTEX3_CFG0	0x0700002A00	0x0700002AFF	256B
DEBUGSS_WRAP0_CORTEX4_CFG0	0x0700002B00	0x0700002BFF	256B
DEBUGSS_WRAP0_CORTEX5_CFG0	0x0700002C00	0x0700002CFF	256B
DEBUGSS_WRAP0_CORTEX6_CFG0	0x0700002D00	0x0700002DFF	256B
DEBUGSS_WRAP0_CORTEX7_CFG0	0x0700002E00	0x0700002EFF	256B
DEBUGSS_WRAP0_CORTEX8_CFG0	0x0700002F00	0x0700002FFF	256B
DEBUGSS_WRAP0_RESV1_0	0x0700003000	0x0700003FFF	256B
DEBUGSS_WRAP0_RESV2_0	0x0700004000	0x0702003FFF	4KB
DEBUGSS_WRAP0_ROM_TABLE_1_0	0x0720000000	0x0720000FFF	32MB
DEBUGSS_WRAP0_CSCTI	0x0720001000	0x0720001FFF	4KB
DEBUGSS_WRAP0_DRM0	0x0720002000	0x0720002FFF	4KB
DEBUGSS_WRAP0_RESV3_0	0x0720003000	0x0720003FFF	4KB
DEBUGSS_WRAP0_CSTPIU0	0x0720004000	0x0720004FFF	4KB
DEBUGSS_WRAP0_CTF0	0x0720005000	0x0720005FFF	4KB
DEBUGSS_WRAP0_RESV4_0	0x0720006000	0x0721005FFF	4KB
DEBUGSS_WRAP0_EXT_APB0	0x0730000000	0x073FFFFFFF	16MB
C7X256V0_THINMAN	0x0734000000	0x0734001FFF	256MB
C7X256V0_COLOMBO	0x0734001000	0x0734002FFF	8KB
C7X256V0_MATLOCK	0x0734002000	0x0734003FFF	8KB
C7X256V0_CSCTI	0x0734003000	0x0734003FFF	8KB
C7X256V0_CTSET2	0x0734008000	0x0734009FFF	4KB
C7X256V0_CSCTI	0x073400A000	0x073400AFFF	8KB
C7X256V0_CSCTI	0x073400B000	0x073400BFFF	4KB
C7X256V0_DBG_AGR0_MMR	0x0734040000	0x07340400FF	4KB
C7X256V0_DBG_AGR0_MEM_CFG	0x0734040100	0x07340401FF	256B
C7X256V0_DBG_AGR0_MEM0	0x0734060000	0x0734060FFF	256B
C7X256V0_DBG_AGR0_MEM1	0x0734061000	0x0734061FFF	4KB
C7X256V0_DBG_AGR0_MEM2	0x0734062000	0x0734062FFF	4KB
C7X256V0_DBG_AGR0_MEM3	0x0734063000	0x0734063FFF	4KB
C7X256V0_DBG_AGR0_MEM4	0x0734064000	0x0734064FFF	4KB
C7X256V0_DBG_AGR0_MEM5	0x0734065000	0x0734065FFF	4KB
C7X256V0_DBG_AGR0_MEM6	0x0734066000	0x0734066FFF	4KB
C7X256V0_DBG_AGR0_MEM7	0x0734067000	0x0734067FFF	4KB
C7X256V0_DBG_AGR0_MEM8	0x0734068000	0x0734068FFF	4KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
C7X256V0_DBG_AGR0_MEM9	0x0734069000	0x0734069FFF	4KB
C7X256V0_DBG_AGR0_MEM10	0x073406A000	0x073406AFFF	4KB
C7X256V0_DBG_AGR0_MEM11	0x073406B000	0x073406BFFF	4KB
C7X256V0_DBG_AGR0_MEM12	0x073406C000	0x073406CFFF	4KB
C7X256V0_DBG_AGR0_MEM13	0x073406D000	0x073406DFFF	4KB
C7X256V0_DBG_AGR0_MEM14	0x073406E000	0x073406EFFF	4KB
C7X256V0_DBG_AGR0_MEM15	0x073406F000	0x073406FFFF	4KB
C7X256V0_DBG_AGR0_MEM16	0x0734070000	0x0734070FFF	4KB
C7X256V0_DBG_AGR0_MEM17	0x0734071000	0x0734071FFF	4KB
C7X256V0_DBG_AGR0_MEM18	0x0734072000	0x0734072FFF	4KB
C7X256V0_DBG_AGR0_MEM19	0x0734073000	0x0734073FFF	4KB
C7X256V0_DBG_AGR0_MEM20	0x0734074000	0x0734074FFF	4KB
C7X256V0_DBG_AGR0_MEM21	0x0734075000	0x0734075FFF	4KB
C7X256V0_DBG_AGR0_MEM22	0x0734076000	0x0734076FFF	4KB
C7X256V0_DBG_AGR0_MEM23	0x0734077000	0x0734077FFF	4KB
C7X256V0_DBG_AGR0_MEM24	0x0734078000	0x0734078FFF	4KB
C7X256V0_DBG_AGR0_MEM25	0x0734079000	0x0734079FFF	4KB
C7X256V0_DBG_AGR0_MEM26	0x073407A000	0x073407AFFF	4KB
C7X256V0_DBG_AGR0_MEM27	0x073407B000	0x073407BFFF	4KB
C7X256V0_DBG_AGR0_MEM28	0x073407C000	0x073407CFFF	4KB
C7X256V0_DBG_AGR0_MEM29	0x073407D000	0x073407DFFF	4KB
C7X256V0_DBG_AGR0_MEM30	0x073407E000	0x073407EFFF	4KB
C7X256V0_DBG_AGR0_MEM31	0x073407F000	0x073407FFFF	4KB
C7X256V1_THINMAN	0x0738000000	0x0738001FFF	4KB
C7X256V1_COLOMBO	0x0738001000	0x0738002FFF	8KB
C7X256V1_MATLOCK	0x0738002000	0x0738003FFF	8KB
C7X256V1_CSCTI	0x0738003000	0x0738003FFF	8KB
C7X256V1_CTSET2	0x0738008000	0x0738009FFF	4KB
C7X256V1_CSCTI	0x073800A000	0x073800AFFF	8KB
C7X256V1_CSCTI	0x073800B000	0x073800BFFF	4KB
C7X256V1_DBG_AGR0_MMR	0x0738040000	0x07380400FF	4KB
C7X256V1_DBG_AGR0_MEM_CFG	0x0738040100	0x07380401FF	256B
C7X256V1_DBG_AGR0_MEM0	0x0738060000	0x0738060FFF	256B
C7X256V1_DBG_AGR0_MEM1	0x0738061000	0x0738061FFF	4KB
C7X256V1_DBG_AGR0_MEM2	0x0738062000	0x0738062FFF	4KB
C7X256V1_DBG_AGR0_MEM3	0x0738063000	0x0738063FFF	4KB
C7X256V1_DBG_AGR0_MEM4	0x0738064000	0x0738064FFF	4KB
C7X256V1_DBG_AGR0_MEM5	0x0738065000	0x0738065FFF	4KB
C7X256V1_DBG_AGR0_MEM6	0x0738066000	0x0738066FFF	4KB
C7X256V1_DBG_AGR0_MEM7	0x0738067000	0x0738067FFF	4KB
C7X256V1_DBG_AGR0_MEM8	0x0738068000	0x0738068FFF	4KB
C7X256V1_DBG_AGR0_MEM9	0x0738069000	0x0738069FFF	4KB
C7X256V1_DBG_AGR0_MEM10	0x073806A000	0x073806AFFF	4KB
C7X256V1_DBG_AGR0_MEM11	0x073806B000	0x073806BFFF	4KB
C7X256V1_DBG_AGR0_MEM12	0x073806C000	0x073806CFFF	4KB
C7X256V1_DBG_AGR0_MEM13	0x073806D000	0x073806DFFF	4KB
C7X256V1_DBG_AGR0_MEM14	0x073806E000	0x073806EFFF	4KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
C7X256V1_DBG_AGR0_MEM15	0x073806F000	0x073806FFFF	4KB
C7X256V1_DBG_AGR0_MEM16	0x0738070000	0x0738070FFF	4KB
C7X256V1_DBG_AGR0_MEM17	0x0738071000	0x0738071FFF	4KB
C7X256V1_DBG_AGR0_MEM18	0x0738072000	0x0738072FFF	4KB
C7X256V1_DBG_AGR0_MEM19	0x0738073000	0x0738073FFF	4KB
C7X256V1_DBG_AGR0_MEM20	0x0738074000	0x0738074FFF	4KB
C7X256V1_DBG_AGR0_MEM21	0x0738075000	0x0738075FFF	4KB
C7X256V1_DBG_AGR0_MEM22	0x0738076000	0x0738076FFF	4KB
C7X256V1_DBG_AGR0_MEM23	0x0738077000	0x0738077FFF	4KB
C7X256V1_DBG_AGR0_MEM24	0x0738078000	0x0738078FFF	4KB
C7X256V1_DBG_AGR0_MEM25	0x0738079000	0x0738079FFF	4KB
C7X256V1_DBG_AGR0_MEM26	0x073807A000	0x073807AFFF	4KB
C7X256V1_DBG_AGR0_MEM27	0x073807B000	0x073807BFFF	4KB
C7X256V1_DBG_AGR0_MEM28	0x073807C000	0x073807CFFF	4KB
C7X256V1_DBG_AGR0_MEM29	0x073807D000	0x073807DFFF	4KB
C7X256V1_DBG_AGR0_MEM30	0x073807E000	0x073807EFFF	4KB
C7X256V1_DBG_AGR0_MEM31	0x073807F000	0x073807FFFF	4KB
DEBUGSS0_DEBUG_CELL_ROM_SLV	0x073C020000	0x073C020FFF	4KB
DEBUGSS0_CTSET2_WRAP_CFG_CTSET2_CFG	0x073C022000	0x073C023FFF	4KB
DEBUGSS0_ATB_REPLICATOR_CFG_CXATBREPLICATOR_CFG	0x073C024000	0x073C024FFF	8KB
DEBUGSS0_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG	0x073C025000	0x073C025FFF	4KB
DEBUGSS0_ARM_CTI_0_CFG_CSCTI_CFG	0x073C026000	0x073C026FFF	4KB
DEBUGSS0_ARM_CTI_1_CFG_CSCTI_CFG	0x073C028000	0x073C028FFF	4KB
DEBUGSS0_ARM_CTI_2_CFG_CSCTI_CFG	0x073C029000	0x073C029FFF	4KB
DEBUGSS0_ARM_CTI_3_CFG_CSCTI_CFG	0x073C02A000	0x073C02AFFF	4KB
DEBUGSS0_ARM_CTI_4_CFG_CSCTI_CFG	0x073C02B000	0x073C02BFFF	4KB
DEBUGSS0_ARM_CTI_5_CFG_CSCTI_CFG	0x073C02C000	0x073C02CFFF	4KB
DEBUGSS0_ARM_CTI_6_CFG_CSCTI_CFG	0x073C02D000	0x073C02DFFF	4KB
DEBUGSS0_ARM_CTI_7_CFG_CSCTI_CFG	0x073C02E000	0x073C02EFFF	4KB
DEBUGSS0_ARM_CTI_8_CFG_CSCTI_CFG	0x073C02F000	0x073C02FFFF	4KB
STM0_CSSTM	0x073D200000	0x073D200FFF	4KB
STM0_CTI_CSCTI	0x073D201000	0x073D201FFF	4KB
DBG_INTROUTER0_INTR_ROUTER_CFG	0x073D300000	0x073D300FFF	4KB
CPT2_AGGR0_MMR	0x073E100000	0x073E1000FF	4KB
CPT2_AGGR0_STP2ATB_CFG	0x073E100100	0x073E1001FF	256B
CPT2_AGGR0_MEM0	0x073E120000	0x073E120FFF	256B
CPT2_AGGR0_MEM1	0x073E121000	0x073E121FFF	4KB
CPT2_AGGR0_MEM2	0x073E122000	0x073E122FFF	4KB
CPT2_AGGR0_MEM3	0x073E123000	0x073E123FFF	4KB
CPT2_AGGR0_MEM4	0x073E124000	0x073E124FFF	4KB
CPT2_AGGR0_MEM5	0x073E125000	0x073E125FFF	4KB
CPT2_AGGR0_MEM6	0x073E126000	0x073E126FFF	4KB
CPT2_AGGR0_MEM7	0x073E127000	0x073E127FFF	4KB
CPT2_AGGR0_MEM8	0x073E128000	0x073E128FFF	4KB
CPT2_AGGR0_MEM9	0x073E129000	0x073E129FFF	4KB
CPT2_AGGR0_MEM10	0x073E12A000	0x073E12AFFF	4KB
CPT2_AGGR0_MEM11	0x073E12B000	0x073E12BFFF	4KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
CPT2_AGGR0_MEM12	0x073E12C000	0x073E12CFFF	4KB
CPT2_AGGR0_MEM13	0x073E12D000	0x073E12DFFF	4KB
CPT2_AGGR0_MEM14	0x073E12E000	0x073E12EFFF	4KB
CPT2_AGGR0_MEM15	0x073E12F000	0x073E12FFFF	4KB
CPT2_AGGR0_MEM16	0x073E130000	0x073E130FFF	4KB
CPT2_AGGR0_MEM17	0x073E131000	0x073E131FFF	4KB
CPT2_AGGR0_MEM18	0x073E132000	0x073E132FFF	4KB
CPT2_AGGR0_MEM19	0x073E133000	0x073E133FFF	4KB
CPT2_AGGR0_MEM20	0x073E134000	0x073E134FFF	4KB
CPT2_AGGR0_MEM21	0x073E135000	0x073E135FFF	4KB
CPT2_AGGR0_MEM22	0x073E136000	0x073E136FFF	4KB
CPT2_AGGR0_MEM23	0x073E137000	0x073E137FFF	4KB
CPT2_AGGR0_MEM24	0x073E138000	0x073E138FFF	4KB
CPT2_AGGR0_MEM25	0x073E139000	0x073E139FFF	4KB
CPT2_AGGR0_MEM26	0x073E13A000	0x073E13AFFF	4KB
CPT2_AGGR0_MEM27	0x073E13B000	0x073E13BFFF	4KB
CPT2_AGGR0_MEM28	0x073E13C000	0x073E13CFFF	4KB
CPT2_AGGR0_MEM29	0x073E13D000	0x073E13DFFF	4KB
CPT2_AGGR0_MEM30	0x073E13E000	0x073E13EFFF	4KB
CPT2_AGGR0_MEM31	0x073E13F000	0x073E13FFFF	4KB
CPT2_AGGR1_MMR	0x073E140000	0x073E1400FF	4KB
CPT2_AGGR1_STP2ATB_CFG	0x073E140100	0x073E1401FF	256B
CPT2_AGGR1_MEM0	0x073E160000	0x073E160FFF	256B
CPT2_AGGR1_MEM1	0x073E161000	0x073E161FFF	4KB
CPT2_AGGR1_MEM2	0x073E162000	0x073E162FFF	4KB
CPT2_AGGR1_MEM3	0x073E163000	0x073E163FFF	4KB
CPT2_AGGR1_MEM4	0x073E164000	0x073E164FFF	4KB
CPT2_AGGR1_MEM5	0x073E165000	0x073E165FFF	4KB
CPT2_AGGR1_MEM6	0x073E166000	0x073E166FFF	4KB
CPT2_AGGR1_MEM7	0x073E167000	0x073E167FFF	4KB
CPT2_AGGR1_MEM8	0x073E168000	0x073E168FFF	4KB
CPT2_AGGR1_MEM9	0x073E169000	0x073E169FFF	4KB
CPT2_AGGR1_MEM10	0x073E16A000	0x073E16AFFF	4KB
CPT2_AGGR1_MEM11	0x073E16B000	0x073E16BFFF	4KB
CPT2_AGGR1_MEM12	0x073E16C000	0x073E16CFFF	4KB
CPT2_AGGR1_MEM13	0x073E16D000	0x073E16DFFF	4KB
CPT2_AGGR1_MEM14	0x073E16E000	0x073E16EFFF	4KB
CPT2_AGGR1_MEM15	0x073E16F000	0x073E16FFFF	4KB
CPT2_AGGR1_MEM16	0x073E170000	0x073E170FFF	4KB
CPT2_AGGR1_MEM17	0x073E171000	0x073E171FFF	4KB
CPT2_AGGR1_MEM18	0x073E172000	0x073E172FFF	4KB
CPT2_AGGR1_MEM19	0x073E173000	0x073E173FFF	4KB
CPT2_AGGR1_MEM20	0x073E174000	0x073E174FFF	4KB
CPT2_AGGR1_MEM21	0x073E175000	0x073E175FFF	4KB
CPT2_AGGR1_MEM22	0x073E176000	0x073E176FFF	4KB
CPT2_AGGR1_MEM23	0x073E177000	0x073E177FFF	4KB
CPT2_AGGR1_MEM24	0x073E178000	0x073E178FFF	4KB

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
CPT2_AGGR1_MEM25	0x073E179000	0x073E179FFF	4KB
CPT2_AGGR1_MEM26	0x073E17A000	0x073E17AFFF	4KB
CPT2_AGGR1_MEM27	0x073E17B000	0x073E17BFFF	4KB
CPT2_AGGR1_MEM28	0x073E17C000	0x073E17CFFF	4KB
CPT2_AGGR1_MEM29	0x073E17D000	0x073E17DFFF	4KB
CPT2_AGGR1_MEM30	0x073E17E000	0x073E17EFFF	4KB
CPT2_AGGR1_MEM31	0x073E17F000	0x073E17FFFF	4KB
CPT2_AGGR2_MMR	0x073E180000	0x073E1800FF	4KB
CPT2_AGGR2_STP2ATB_CFG	0x073E180100	0x073E1801FF	256B
CPT2_AGGR2_MEM0	0x073E1A0000	0x073E1A0FFF	256B
CPT2_AGGR2_MEM1	0x073E1A1000	0x073E1A1FFF	4KB
CPT2_AGGR2_MEM2	0x073E1A2000	0x073E1A2FFF	4KB
CPT2_AGGR2_MEM3	0x073E1A3000	0x073E1A3FFF	4KB
CPT2_AGGR2_MEM4	0x073E1A4000	0x073E1A4FFF	4KB
CPT2_AGGR2_MEM5	0x073E1A5000	0x073E1A5FFF	4KB
CPT2_AGGR2_MEM6	0x073E1A6000	0x073E1A6FFF	4KB
CPT2_AGGR2_MEM7	0x073E1A7000	0x073E1A7FFF	4KB
CPT2_AGGR2_MEM8	0x073E1A8000	0x073E1A8FFF	4KB
CPT2_AGGR2_MEM9	0x073E1A9000	0x073E1A9FFF	4KB
CPT2_AGGR2_MEM10	0x073E1AA000	0x073E1AAFFF	4KB
CPT2_AGGR2_MEM11	0x073E1AB000	0x073E1ABFFF	4KB
CPT2_AGGR2_MEM12	0x073E1AC000	0x073E1ACFFF	4KB
CPT2_AGGR2_MEM13	0x073E1AD000	0x073E1ADFFF	4KB
CPT2_AGGR2_MEM14	0x073E1AE000	0x073E1AEFFF	4KB
CPT2_AGGR2_MEM15	0x073E1AF000	0x073E1AFFFF	4KB
CPT2_AGGR2_MEM16	0x073E1B0000	0x073E1B0FFF	4KB
CPT2_AGGR2_MEM17	0x073E1B1000	0x073E1B1FFF	4KB
CPT2_AGGR2_MEM18	0x073E1B2000	0x073E1B2FFF	4KB
CPT2_AGGR2_MEM19	0x073E1B3000	0x073E1B3FFF	4KB
CPT2_AGGR2_MEM20	0x073E1B4000	0x073E1B4FFF	4KB
CPT2_AGGR2_MEM21	0x073E1B5000	0x073E1B5FFF	4KB
CPT2_AGGR2_MEM22	0x073E1B6000	0x073E1B6FFF	4KB
CPT2_AGGR2_MEM23	0x073E1B7000	0x073E1B7FFF	4KB
CPT2_AGGR2_MEM24	0x073E1B8000	0x073E1B8FFF	4KB
CPT2_AGGR2_MEM25	0x073E1B9000	0x073E1B9FFF	4KB
CPT2_AGGR2_MEM26	0x073E1BA000	0x073E1BAFFF	4KB
CPT2_AGGR2_MEM27	0x073E1BB000	0x073E1BBFFF	4KB
CPT2_AGGR2_MEM28	0x073E1BC000	0x073E1BCFFF	4KB
CPT2_AGGR2_MEM29	0x073E1BD000	0x073E1BDFFF	4KB
CPT2_AGGR2_MEM30	0x073E1BE000	0x073E1BEFFF	4KB
CPT2_AGGR2_MEM31	0x073E1BF000	0x073E1BFFFF	4KB
DEBUGSS_WRAP0_ROM_TABLE_0_1	0x0740000000	0x0740000FFF	4KB
DEBUGSS_WRAP0_RESV0_1	0x0740001000	0x0740001FFF	4KB
DEBUGSS_WRAP0_CFGAP1	0x0740002000	0x07400020FF	4KB
DEBUGSS_WRAP0_APBAP1	0x0740002100	0x07400021FF	256B
DEBUGSS_WRAP0_AXIAP1	0x0740002200	0x07400022FF	256B
DEBUGSS_WRAP0_PWRAP1	0x0740002300	0x07400023FF	256B

Table 2-1. MAIN Memory Map (continued)

Region Name	Start Address	End Address	Size
DEBUGSS_WRAP0_PVIEW1	0x0740002400	0x07400024FF	256B
DEBUGSS_WRAP0_JTAGAP1	0x0740002500	0x07400025FF	256B
DEBUGSS_WRAP0_SECAP1	0x0740002600	0x07400026FF	256B
DEBUGSS_WRAP0_CORTEX0_CFG1	0x0740002700	0x07400027FF	256B
DEBUGSS_WRAP0_CORTEX1_CFG1	0x0740002800	0x07400028FF	256B
DEBUGSS_WRAP0_CORTEX2_CFG1	0x0740002900	0x07400029FF	256B
DEBUGSS_WRAP0_CORTEX3_CFG1	0x0740002A00	0x0740002AFF	256B
DEBUGSS_WRAP0_CORTEX4_CFG1	0x0740002B00	0x0740002BFF	256B
DEBUGSS_WRAP0_CORTEX5_CFG1	0x0740002C00	0x0740002CFF	256B
DEBUGSS_WRAP0_CORTEX6_CFG1	0x0740002D00	0x0740002DFF	256B
DEBUGSS_WRAP0_CORTEX7_CFG1	0x0740002E00	0x0740002EFF	256B
DEBUGSS_WRAP0_CORTEX8_CFG1	0x0740002F00	0x0740002FFF	256B
DEBUGSS_WRAP0_RESV1_1	0x0740003000	0x0740003FFF	256B
DEBUGSS_WRAP0_RESV2_1	0x0740004000	0x0742003FFF	4KB
DEBUGSS_WRAP0_ROM_TABLE_1_1	0x0760000000	0x0760000FFF	32MB
DEBUGSS_WRAP0_CSCTI	0x0760001000	0x0760001FFF	4KB
DEBUGSS_WRAP0_DRM1	0x0760002000	0x0760002FFF	4KB
DEBUGSS_WRAP0_RESV3_1	0x0760003000	0x0760003FFF	4KB
DEBUGSS_WRAP0_CSTPIU1	0x0760004000	0x0760004FFF	4KB
DEBUGSS_WRAP0_CTF1	0x0760005000	0x0760005FFF	4KB
DEBUGSS_WRAP0_RESV4_1	0x0760006000	0x0761005FFF	4KB
DEBUGSS_WRAP0_EXT_APB1	0x0770000000	0x077FFFFFFF	16MB
FSS1_OSPI1_R3	0x0A00000000	0x0AFFFFFFFF	256MB

2.2 C7x Memory View

C7x core can access 6MB on-chip SRAM using two sets of addresses, one set address starting at 0x7200 0000 and the second address starting 0x8000 0000. When C7x access the on-chip SRAM using the address range between 0x7200 0000 to 0x725F FFFF, L1D only supports write through capability. When C7x access the on-chip SRAM using address range between 0x8000 0000 to 0x805F FFFF, the L1D cache write back feature can be supported. DRU inside C7x and the streaming engine for C7x can also use both address ranges to access on-chip SRAM.

For all the other initiators in SoC such as Pulsar R5F, DMSS, USB, EMMC, DAP and etc, the on-chip SRAM can only be accessed using address 0x7200 0000 to 0x725F FFFF. Any access to address range 0x8000 0000 to 0x805F FFFF from initiators other than C7x core, DRU inside C7x, and streaming engine inside C7x, can cause a transaction error.

The below table summarizes the different addresses needed for C7x access to SRAM.

Table 2-2. C7 and SOC SRAM Addresses

Region Name	L1D Cache Address	All Other Initiators	Size
MSRAM_1MB0_RAM	0x8000 0000	0x7200 0000	1MB
MSRAM_1MB1_RAM	0x8010 0000	0x7210 0000	1MB
MSRAM_1MB2_RAM	0x8020 0000	0x7220 0000	1MB
MSRAM_1MB3_RAM	0x8030 0000	0x7230 0000	1MB
MSRAM_1MB4_RAM	0x8040 0000	0x7240 0000	1MB
MSRAM_1MB5_RAM	0x8050 0000	0x7250 0000	1MB

Note

Best practices are:

- **Only one set of addresses** from C7 and SOC SRAM Addresses shall be used at any given time. If C7x uses both address ranges in parallel, data corruption can occur.
- When L1D cache write back feature is enabled:
  - C7x shall use the virtual address of 0x8000 0000 to access 6MB on-chip SRAM
  - MMU maps 0x8000 0000 to 0x8000 0000
- When L1D cache write feature is disable:
  - C7x shall only use the virtual address of 0x7200 0000 to access 6MB on-chip SRAM.
  - MMU maps 0x7200 0000 to 0x8000 0000
- L1D cache shall be flushed before C7x switches cache write back feature setting. Without the flush, data corruption can occur.

2.3 Device Manager R5F and Main R5F Memory View

AM275 has one single R5F core in the wakeup domain. The R5F is a native 32b processor, which the R5F core itself can only generate transactions using 32b address. A dedicated RAT module is integrated for this single core R5F to allow the R5F software to remap the 32b R5F address into the common 36b SoC address.

In addition, the R5F core has its own TCM, which the R5F core can access with its TCM with a single R5F core cycle. Those TCM memories have two sets of address, one set address is used for the R5F core for a single cycle access to those TCM. The second set of address is used by other initiators outside this R5F subsystem to access those TCM. The R5F core shall always uses the first set of address to access its TCM. If the R5F core utilizes the second set of address to those TCM, the R5F core will receives an exception, since those transactions will be routed to be terminated by sending them to the null end point.

While the SoC level address for TCM is fixed, the address used by the R5F to access to its own TCM can be remapped by software. By default, AM275 puts the R5F's ATCM at address 0x0 and the BTCM address at 0x4101_0000.

The R5F also has one section of the region dedicated for peripheral access from address 0x2000_0000 to 0x2FFF_FFFF. This memory region is treated as normally memory, which can't be cached. The R5F accesses this memory region through a dedicated single-issue interface, and none of the transactions accessing this memory region can be remapped by using RAT module.

R5F accesses its own ATCM and BTCM in a single cycle directly without address remapping and without going out to SoC. R5F accesses its own VIC and RAT configuration internally without address remapping and without going out to SoC. For the rest of end points in address range 0x2000_0000 to 0x2FFF_FFFF, R5F can access those end points through the low latency peripheral interface without going through address remapping. For the access to the rest end points, including the ATCM/BTCM from another R5F core, R5F sends transaction through its memory interface and could remapp its own address to SoC memory address.

Table 2-3. Device Manager R5FSS0 Memory Map

Region Name	Start Address	End Address	Size	Notes
R5FSS0_ATCM	0x0000 0000	0x0000 7FFF	32KB	The R5F can re-map its ATCM to a different address internally. After the R5F re-maps its ATCM address, any transaction hitting this region can also go through RAT remapping function.
R5FSS0_RAT_REGION0	0x0001 0000	0x1FFF FFFF	512MB	
R5FSS0_NON_RAT_SOC_REGION0	0x2000 0000	0x2FFF FFFF	256MB	
R5FSS0_RAT_CFG	0x2FFE 0000	0x2FFE 0FFF	4KB	This is within the non_RAT region
R5FSS0_VIM_CFG	0x2FFF 0000	0x2FFF 3FFF	16KB	This is within the non_RAT region
R5FSS0_RAT_SOC_REGION1	0x3000 0000	0x4100 FFFF	272MB	

Table 2-3. Device Manager R5FSS0 Memory Map (continued)

Region Name	Start Address	End Address	Size	Notes
R5FSS0_BTCM	0x4101 0000	0x4101 7FFF	32KB	The R5F can re-map its BTCM to a different address internally. After the R5F re-maps its ATCM address, any transaction hitting this region can also go through RAT remapping function
R5FSS0_RAT_REGION2	0x4101 8000	0x7FFF FFFF	1008MB	
R5FSS0_RAT_REGION3	0x8000 0000	0xFFFF FFFF	2GB	

The common SoC memory map assigns the R5F's ATCM and BTCM to address 0x7800_0000 and 0x7810_0000. The R5F software can optionally reprogram the its internal ATCM and BTCM address to match the address assigned by the common SoC memory map as well. Regardless where the R5F puts its own ATCM and BTCM, the R5F accesses its own ATCM and BTCM directly without going through RAT.

ATCM is by default disabled at address 0x0. BTCM is by default enabled and the default address for BTCM is 0x4101_0000. The base address of VIM is at 0x2FFF_0000 and the base address for RAT configuration is at 0x2FFE_0000.

All the R5F transactions can go through RAT for address re-mapping function except the transactions targeted to address range 0x2000_0000 to 0x2FFF_FFFF and its own ATCM and BTCM. It is highly recommended only remap the R5F's address range from 0x8000_0000 to 0xFFFF_FFFF to access the target region located at the common memory map between 0x8000_0000 and 0xF_FFFF_FFFF.

2.4 Memory Map Summary

Since different type of the processors have different memory map views, this section provides a summary on how each type of processor and initiator access various target end points in the SoC.

Table 2-4. SoC Memory Map

Region Name	Start Address	DM R5F and Main R5F Access
PSRAMECC0	0x0000000000	VIA RAT
PADCFG_CTRL0	0x00000F0000	VIA RAT
CTRL_MMR0_CFG0	0x0000100000	VIA RAT
CBASS_DBG0_ERR	0x0000200000	VIA RAT
CBASS_INFRA1_ERR	0x0000210000	VIA RAT
CBASS_FW0_ERR	0x0000220000	VIA RAT
AM275_MAIN_IPCSS_CBASS0_ERR	0x0000230000	VIA RAT
EFUSE0	0x0000300000	VIA RAT
PBIST7	0x0000340000	VIA RAT
PBIST8	0x0000350000	VIA RAT
C7X256V0_PBIST	0x0000360000	VIA RAT
C7X256V1_PBIST	0x0000370000	VIA RAT
PBIST0	0x0000390000	VIA RAT
PBIST1	0x00003A0000	VIA RAT
PBIST2	0x00003B0000	VIA RAT
PBIST3	0x00003C0000	VIA RAT
PBIST4	0x00003D0000	VIA RAT
PBIST5	0x00003E0000	VIA RAT
PBIST6	0x00003F0000	VIA RAT
MAIN_PSC0_PSC	0x0000400000	VIA RAT
PLLCTRL0	0x0000410000	VIA RAT
ESM0_CFG	0x0000420000	VIA RAT
DFTSS0_MEM	0x0000500000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
DDPA0	0x0000580000	VIA RAT
GPIO0	0x0000600000	VIA RAT
GPIO1	0x0000601000	VIA RAT
PLL0_CFG	0x0000680000	VIA RAT
PSRAMECC0_ECC_AGGR	0x0000700000	VIA RAT
USB0_DEBUG_TRACE_MMR_TRACE_VBUSP_USB2SS_DEBUG_TRACE	0x0000703000	VIA RAT
CPSW0_CPSW_NUSS_VBUSP_ECC	0x0000704000	VIA RAT
MMCSD0_ECC_AGGR_RXMEM	0x0000708000	VIA RAT
MMCSD0_ECC_AGGR_TXMEM	0x0000709000	VIA RAT
SA3_SS0_ECC_AGGR	0x0000712000	VIA RAT
FSS0_OSPI0_ECC_AGGR	0x0000716000	VIA RAT
FSS0_FSAS_ECC_AGGR	0x0000717000	VIA RAT
C7X256V0_ECC_AGGR	0x000071A000	VIA RAT
C7X256V1_ECC_AGGR	0x000071B000	VIA RAT
MSRAM_1MB0_ECC_AGGR_REGS	0x000071C000	VIA RAT
MSRAM_1MB1_ECC_AGGR_REGS	0x000071D000	VIA RAT
MSRAM_1MB2_ECC_AGGR_REGS	0x000071E000	VIA RAT
MSRAM_1MB3_ECC_AGGR_REGS	0x000071F000	VIA RAT
MSRAM_1MB4_ECC_AGGR_REGS	0x0000720000	VIA RAT
MSRAM_1MB5_ECC_AGGR_REGS	0x0000721000	VIA RAT
FSS1_HPB_ECC_AGGR	0x0000722000	VIA RAT
FSS1_OSPI0_ECC_AGGR	0x0000723000	VIA RAT
FSS1_OSPI1_ECC_AGGR	0x0000724000	VIA RAT
ADC0_ECC	0x0000729000	VIA RAT
R5FSS0_CORE0_ECC_AGGR	0x0000730000	VIA RAT
R5FSS1_CORE0_ECC_AGGR	0x0000731000	VIA RAT
DCC0	0x0000800000	VIA RAT
DCC1	0x0000804000	VIA RAT
DCC2	0x0000808000	VIA RAT
DCC3	0x000080C000	VIA RAT
DCC4	0x0000810000	VIA RAT
DCC5	0x0000814000	VIA RAT
DCC6	0x0000818000	VIA RAT
DCC7	0x000081C000	VIA RAT
DCC8	0x0000820000	VIA RAT
MAIN_GPIOMUX_INTROUTER0_INTR_ROUTER_CFG	0x0000A00000	VIA RAT
TIMESYNC_EVENT_INTROUTER0_INTR_ROUTER_CFG	0x0000A40000	VIA RAT
WKUP_GTC0_CFG0	0x0000A80000	VIA RAT
WKUP_GTC0_CFG1	0x0000A90000	VIA RAT
WKUP_GTC0_CFG2	0x0000AA0000	VIA RAT
WKUP_GTC0_CFG3	0x0000AB0000	VIA RAT
WKUP_VTM0_VTM_CFG1	0x0000B00000	VIA RAT
WKUP_VTM0_VTM_CFG2	0x0000B01000	VIA RAT
WKUP_VTM0_ECCAGGR_CFG	0x0000B02000	VIA RAT
PDMA0	0x0000C00000	VIA RAT
PDMA1	0x0000C01000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
PDMA4_REGS	0x0000C02000	VIA RAT
TIMER0_CFG	0x0002400000	VIA RAT
TIMER1_CFG	0x0002410000	VIA RAT
TIMER2_CFG	0x0002420000	VIA RAT
TIMER3_CFG	0x0002430000	VIA RAT
TIMER4_CFG	0x0002440000	VIA RAT
TIMER5_CFG	0x0002450000	VIA RAT
TIMER6_CFG	0x0002460000	VIA RAT
TIMER7_CFG	0x0002470000	VIA RAT
TIMER8_CFG	0x0002480000	VIA RAT
TIMER9_CFG	0x0002490000	VIA RAT
TIMER10_CFG	0x00024A0000	VIA RAT
TIMER11_CFG	0x00024B0000	VIA RAT
TIMER12_CFG	0x00024C0000	VIA RAT
TIMER13_CFG	0x00024D0000	VIA RAT
TIMER14_CFG	0x00024E0000	VIA RAT
TIMER15_CFG	0x00024F0000	VIA RAT
UART0	0x0002800000	VIA RAT
UART1	0x0002810000	VIA RAT
UART2	0x0002820000	VIA RAT
UART3	0x0002830000	VIA RAT
UART4	0x0002840000	VIA RAT
UART5	0x0002850000	VIA RAT
UART6	0x0002860000	VIA RAT
MCASP0_CFG	0x0002B00000	VIA RAT
MCASP0_DMA	0x0002B08000	VIA RAT
MCASP1_CFG	0x0002B10000	VIA RAT
MCASP1_DMA	0x0002B18000	VIA RAT
MCASP2_CFG	0x0002B20000	VIA RAT
MCASP2_DMA	0x0002B28000	VIA RAT
MCASP3_CFG	0x0002B30000	VIA RAT
MCASP3_DMA	0x0002B38000	VIA RAT
MCASP4_CFG	0x0002B40000	VIA RAT
MCASP4_DMA	0x0002B48000	VIA RAT
AASRC0_CFG	0x0002D00000	VIA RAT
AASRC0_DATA_R0	0x0002D10000	VIA RAT
AASRC0_DATA_R1	0x0002D20000	VIA RAT
AASRC1_CFG	0x0002D40000	VIA RAT
AASRC1_DATA_R0	0x0002D50000	VIA RAT
AASRC1_DATA_R1	0x0002D60000	VIA RAT
MLB0_MMR_MMRVBP	0x0002F80000	VIA RAT
MLB0_VBP2APB_WRAP_MLB_CFG_VBP_MLBDIM	0x0002F82000	VIA RAT
MLB0_RAT_WRAP_RAT_CFG_VBP_MMRS	0x0002F83000	VIA RAT
WKUP_PSC0_PSC	0x0004000000	VIA RAT
MCU_PLLCTRL0	0x0004020000	VIA RAT
WKUP_ECC_AGGR2_ECC_AGGR	0x0004030000	VIA RAT
WKUP_PLL0_CFG	0x0004040000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
MCU_PADCFG_CTRL0_CFG0	0x0004080000	VIA RAT
WKUP_ESM0_CFG	0x0004100000	VIA RAT
MCU_GPIO0	0x0004201000	VIA RAT
MCU_MCU_GPIOMUX_INTROUTER0_INTR_ROUTER_CFG	0x0004210000	VIA RAT
MCU_CTRL_MMR0_CFG0	0x0004500000	VIA RAT
WKUP_CBASS_SAFE1_ERR	0x0004600000	VIA RAT
MCU_DCC0	0x0004C00000	VIA RAT
MCU_DCC1	0x0004C10000	VIA RAT
R5FSS0_COMPARE_CFG	0x0005B00000	VIA RAT
R5FSS0_EVNT_BUS_VBUSP_MMRS	0x0005B01000	VIA RAT
R5FSS0_CORE1_ECC_AGGR	0x0005B02000	VIA RAT
R5FSS1_COMPARE_CFG	0x0005B20000	VIA RAT
R5FSS1_EVNT_BUS_VBUSP_MMRS	0x0005B21000	VIA RAT
R5FSS1_CORE1_ECC_AGGR	0x0005B22000	VIA RAT
R5FSS0_CORE0_ATCM	0x0005C00000	VIA RAT
R5FSS0_CORE0_BTCM	0x0005C10000	VIA RAT
R5FSS0_CORE1_ATCM	0x0005D00000	VIA RAT
R5FSS0_CORE1_BTCM	0x0005D10000	VIA RAT
R5FSS1_CORE0_ATCM	0x0005E00000	VIA RAT
R5FSS1_CORE0_BTCM	0x0005E10000	VIA RAT
R5FSS1_CORE1_ATCM	0x0005F00000	VIA RAT
R5FSS1_CORE1_BTCM	0x0005F10000	VIA RAT
MLB0_MLBDIM_WRAP_ECC_AGGR_VBP	0x00072A0000	VIA RAT
CPSW0_CPSW_NUSS_VBUSP	0x0008000000	VIA RAT
RTI4_CFG	0x000E000000	VIA RAT
RTI5_CFG	0x000E010000	VIA RAT
USB0_MMR_MMRVBP_USB2SS_CFG	0x000F900000	VIA RAT
USB0_PHY2	0x000F908000	VIA RAT
USB0_ECC_AGGR	0x000F980000	VIA RAT
MMCSD0_CTL_CFG	0x000FA00000	VIA RAT
MMCSD0_SS_CFG	0x000FA08000	VIA RAT
FSS0_CFG	0x000FC00000	VIA RAT
FSS0_FSAS_CFG	0x000FC10000	VIA RAT
FSS0_OTFA_CFG	0x000FC20000	VIA RAT
FSS1_HPB_SS_CFG	0x000FC30000	VIA RAT
FSS1_HPB_CTRL	0x000FC34000	VIA RAT
FSS0_OSPI0_CTRL	0x000FC40000	VIA RAT
FSS0_OSPI0_SS_CFG	0x000FC44000	VIA RAT
FSS1_OSPI1_CTRL	0x000FC50000	VIA RAT
FSS1_OSPI1_SS_CFG	0x000FC54000	VIA RAT
FSS0_FOTA_CFG	0x000FC60000	VIA RAT
FSS0_FOTA_PDMEM_CFG	0x000FC61000	VIA RAT
FSS0_FOTA_IMEM_CFG	0x000FC62000	VIA RAT
FSS0_WBUF_CFG	0x000FC63000	VIA RAT
FSS1_CFG	0x000FC80000	VIA RAT
FSS1_FSAS_CFG	0x000FC90000	VIA RAT
FSS1_OTFA_CFG	0x000FCA0000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
FSS1_OSPI0_CTRL	0x000FCC0000	VIA RAT
FSS1_OSPI0_SS_CFG	0x000FCC4000	VIA RAT
ATL0_REG	0x000FEE0000	VIA RAT
CBASS_MCASP0_ERR	0x000FEF0000	VIA RAT
I2C0_CFG	0x0020000000	VIA RAT
I2C1_CFG	0x0020010000	VIA RAT
I2C2_CFG	0x0020020000	VIA RAT
I2C3_CFG	0x0020030000	VIA RAT
I2C4_CFG	0x0020040000	VIA RAT
I2C5_CFG	0x0020050000	VIA RAT
I2C6_CFG	0x0020060000	VIA RAT
MCSPI0_CFG	0x0020100000	VIA RAT
MCSPI1_CFG	0x0020110000	VIA RAT
MCSPI2_CFG	0x0020120000	VIA RAT
MCSPI3_CFG	0x0020130000	VIA RAT
MCSPI4_CFG	0x0020140000	VIA RAT
CBASS_MISC_PERI0_ERR	0x00201F0000	VIA RAT
CBASS_MEM0_ERR	0x0020200000	VIA RAT
ADC0_ADC	0x0020600000	VIA RAT
ADC0_ADC12_FIFO_DMA	0x0020608000	VIA RAT
MCAN0_SS	0x0020700000	VIA RAT
MCAN0_CFG	0x0020701000	VIA RAT
MCAN0_MSGMEM_RAM	0x0020708000	VIA RAT
MCAN1_SS	0x0020710000	VIA RAT
MCAN1_CFG	0x0020711000	VIA RAT
MCAN1_MSGMEM_RAM	0x0020718000	VIA RAT
MCAN2_SS	0x0020720000	VIA RAT
MCAN2_CFG	0x0020721000	VIA RAT
MCAN2_MSGMEM_RAM	0x0020728000	VIA RAT
MCAN3_SS	0x0020730000	VIA RAT
MCAN3_CFG	0x0020731000	VIA RAT
MCAN3_MSGMEM_RAM	0x0020738000	VIA RAT
MCAN4_SS	0x0020740000	VIA RAT
MCAN4_CFG	0x0020741000	VIA RAT
MCAN4_MSGMEM_RAM	0x0020748000	VIA RAT
RTI0_CFG	0x0020800000	VIA RAT
RTI1_CFG	0x0020810000	VIA RAT
RTI2_CFG	0x0020820000	VIA RAT
RTI3_CFG	0x0020830000	VIA RAT
EPWM0_EPWM	0x0023000000	VIA RAT
EPWM1_EPWM	0x0023010000	VIA RAT
EPWM2_EPWM	0x0023020000	VIA RAT
ECAP0_CTL_STS	0x0023100000	VIA RAT
ECAP1_CTL_STS	0x0023110000	VIA RAT
ECAP2_CTL_STS	0x0023120000	VIA RAT
ECAP3_CTL_STS	0x0023130000	VIA RAT
ECAP4_CTL_STS	0x0023140000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
ECAP5_CTL_STS	0x0023150000	VIA RAT
MCAN0_ECC_AGGR	0x0024018000	VIA RAT
MCAN1_ECC_AGGR	0x0024019000	VIA RAT
MCAN2_ECC_AGGR	0x002401A000	VIA RAT
MCAN3_ECC_AGGR	0x002401B000	VIA RAT
MCAN4_ECC_AGGR	0x002401C000	VIA RAT
RL2_0_RL2_OF_CBA4	0x0025000000	VIA RAT
RL2_2_RL2_OF_CBA4	0x0025002000	VIA RAT
RL2_3_RL2_OF_CBA4	0x0025003000	VIA RAT
MAILBOX0_REGS0	0x0029000000	VIA RAT
MAILBOX0_REGS1	0x0029010000	VIA RAT
MAILBOX0_REGS2	0x0029020000	VIA RAT
MAILBOX0_REGS3	0x0029030000	VIA RAT
MAILBOX0_REGS4	0x0029040000	VIA RAT
MAILBOX0_REGS5	0x0029050000	VIA RAT
MAILBOX0_REGS6	0x0029060000	VIA RAT
MAILBOX0_REGS7	0x0029070000	VIA RAT
SPINLOCK0	0x002A000000	VIA RAT
WKUP_RTI0_CFG	0x002B000000	VIA RAT
WKUP_TIMER0_CFG	0x002B100000	VIA RAT
WKUP_TIMER1_CFG	0x002B110000	VIA RAT
WKUP_RTCSS0_RTC	0x002B1F0000	VIA RAT
WKUP_I2C0_CFG	0x002B200000	VIA RAT
WKUP_UART0	0x002B300000	DIRECT
WKUP_CBASS0_ERR	0x002B400000	DIRECT
WKUP_PBIST0	0x002B500000	DIRECT
WKUP_PBIST1	0x002B501000	VIA RAT
WKUP_ECC_AGGR0_ECC_AGGR	0x002B600000	DIRECT
WKUP_ECC_AGGR1_ECC_AGGR	0x002B601000	DIRECT
WKUP_PSRAMECC_8K0_REGS	0x002B608000	VIA RAT
WKUP_PSRAM2KX32E0_REGS	0x002B609000	VIA RAT
C7X256V0	0x0030240000	VIA RAT
C7X256V1	0x0030250000	VIA RAT
MCRC64_0_REGS	0x0030300000	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_CAP	0x0031000000	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_OPER	0x0031000020	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_PORT	0x0031000420	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_RUNTIME	0x0031000440	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_INTR	0x0031000460	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DB	0x0031000560	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_EXTCAP	0x0031000960	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_SUPPRTCAP2	0x0031000970	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_SUPPRTCAP3	0x0031000980	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_GBL	0x003100C100	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEV	0x003100C700	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_LINK	0x003100D000	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEBUG	0x003100D800	VIA RAT
USB0_VBP2AHB_WRAP_CONTROLLER_VBP_USB3_CORE_DEBUG_RAM0	0x0031040000	VIA RAT
CBASS0_ERR	0x003A000000	VIA RAT
WKUP_R5FSS0_EVNT_BUS_VBUSP_MMRS	0x003C018000	VIA RAT
DMASS0_ECCAGGR	0x003F005000	VIA RAT
WKUP_R5FSS0_CORE0_ECC_AGGR	0x003F00D000	VIA RAT
ECC_AGGR1_REGS	0x003F00F000	VIA RAT
CBASS_CENTRAL2_ERR	0x003F012000	VIA RAT
ECC_AGGR2_ECC_AGGR	0x003F013000	VIA RAT
ECC_AGGR3_REGS	0x003F014000	VIA RAT
IDOM0_MAIN_PLL_ECC_AGGR4_REGS	0x003F015000	VIA RAT
IDOM0_PULSAR_PLL_ECC_AGGR8_REGS	0x003F016000	VIA RAT
IDOM1_MAIN_PLL_ECC_AGGR5_REGS	0x003F017000	VIA RAT
IDOM1_PULSAR_PLL_ECC_AGGR9_REGS	0x003F018000	VIA RAT
IDOM0_MAIN_PLL_ECC_AGGR6_REGS	0x003F019000	VIA RAT
IDOM0_PULSAR_PLL_ECC_AGGR10_REGS	0x003F01A000	VIA RAT
IDOM1_MAIN_PLL_ECC_AGGR7_REGS	0x003F01B000	VIA RAT
IDOM1_PULSAR_PLL_ECC_AGGR11_REGS	0x003F01C000	VIA RAT
SA3_SS0_REGS	0x0040900000	VIA RAT
SA3_SS0_MMRA	0x0040901000	VIA RAT
SA3_SS0_EIP_76	0x0040910000	VIA RAT
SA3_SS0_EIP_29T2	0x0040920000	VIA RAT
DEBUGSS0_SYS	0x0041000000	VIA RAT
WKUP_ROM0	0x0041800000	VIA RAT
WKUP_PSRAMECC_8K0_RAM	0x0041880000	VIA RAT
WKUP_PSRAM2KX32E0_RAM	0x0041888000	VIA RAT
STM0_STIMULUS	0x0042000000	VIA RAT
WKUP_CTRL_MMR0_CFG0	0x0043000000	VIA RAT
SA3_SS0_SEC_PROXY_SRC_TARGET_DATA	0x0043600000	VIA RAT
SA3_SS0_ECCAGGR_CFG	0x0043702000	VIA RAT
MSRAM_1MB0_RAM	0x0043C40000	VIA RAT
SA3_SS0_PSILCFG_CFG_PROXY	0x0044801000	VIA RAT
SA3_SS0_PSILSS_CFG_MMRS	0x0044802000	VIA RAT
SA3_SS0_IPCSS_SEC_PROXY_CFG_MMRS	0x0044804000	VIA RAT
SA3_SS0_IPCSS_RINGACC_CFG_GCFG	0x0044805000	VIA RAT
SA3_SS0_INTAGGR_CFG	0x0044808000	VIA RAT
SA3_SS0_INTAGGR_CFG_IMAP	0x0044809000	VIA RAT
SA3_SS0_INTAGGR_CFG_MCAST	0x004480A000	VIA RAT
SA3_SS0_INTAGGR_CFG_GCNTCFG	0x004480B000	VIA RAT
SA3_SS0_INTAGGR_CFG_INTR	0x0044810000	VIA RAT
SA3_SS0_INTAGGR_CFG_GCNTRTI	0x0044820000	VIA RAT
SA3_SS0_INTAGGR_CFG_UNMAP	0x0044840000	VIA RAT
SA3_SS0_IPCSS_SEC_PROXY_CFG_SCFG	0x0044860000	VIA RAT
SA3_SS0_IPCSS_SEC_PROXY_CFG_RT	0x0044880000	VIA RAT
SA3_SS0_IPCSS_RINGACC_CFG	0x00448C0000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
SA3_SS0_PKTDMA_CFG_GCFG	0x0044910000	VIA RAT
SA3_SS0_PKTDMA_CFG_RFLOW	0x0044911000	VIA RAT
SA3_SS0_PKTDMA_CFG_RCHAN	0x0044912000	VIA RAT
SA3_SS0_PKTDMA_CFG_TCHAN	0x0044913000	VIA RAT
SA3_SS0_PKTDMA_CFG_RCHANRT	0x0044914000	VIA RAT
SA3_SS0_PKTDMA_CFG_TCHANRT	0x0044918000	VIA RAT
SA3_SS0_PKTDMA_CFG_RING	0x004491A000	VIA RAT
SA3_SS0_PKTDMA_CFG_RINGRT	0x0044940000	VIA RAT
SA3_SS0_IPCSS_RINGACC_CFG_RT	0x0044C00000	VIA RAT
CBASS0_FW	0x0045000000	VIA RAT
WKUP_CBASS0_FW	0x0045008000	VIA RAT
CBASS_CENTRAL2_FW	0x0045010000	VIA RAT
CBASS_INFRA1_FW	0x0045020000	VIA RAT
AM275_MAIN_IPCSS_CBASS0_FW	0x0045028000	VIA RAT
CBASS_MISC_PERI0_FW	0x0045030000	VIA RAT
CBASS_MEM0_FW	0x0045040000	VIA RAT
DMASS0_PKTDMA_CRED	0x0045810000	VIA RAT
DMASS0_BCDMA_CRED	0x0045812000	VIA RAT
WKUP_CBASS0_ISC	0x0045814000	VIA RAT
CBASS0_ISC	0x0045820000	VIA RAT
CBASS_MEM0_ISC	0x0045830000	VIA RAT
CBASS_MISC_PERI0_ISC	0x0045840000	VIA RAT
MAIN_SEC_MMR0_CFG2	0x0045900000	VIA RAT
WKUP_WKUP_SEC_MMR0_CFG2	0x0045920000	VIA RAT
MAIN_SEC_MMR0_CFG0	0x0045A00000	VIA RAT
WKUP_WKUP_SEC_MMR0_CFG0	0x0045A20000	VIA RAT
AM275_MAIN_IPCSS_CBASS0_GLB	0x0045B01000	VIA RAT
CBASS_MEM0_GLB	0x0045B02000	VIA RAT
WKUP_CBASS0_GLB	0x0045B03000	VIA RAT
CBASS_CENTRAL2_GLB	0x0045B04000	VIA RAT
CBASS0_GLB	0x0045B08000	VIA RAT
CBASS_INFRA1_GLB	0x0045B09000	VIA RAT
CBASS_MISC_PERI0_GLB	0x0045B0A000	VIA RAT
WKUP_CBASS0_QOS	0x0045D14000	VIA RAT
CBASS0_QOS	0x0045D20000	VIA RAT
CBASS_MEM0_QOS	0x0045D30000	VIA RAT
CBASS_MISC_PERI0_QOS	0x0045D40000	VIA RAT
DMASS0_INTAGGR_INTR	0x0048000000	VIA RAT
DMASS0_INTAGGR_IMAP	0x0048100000	VIA RAT
DMASS0_INTAGGR_CFG	0x0048110000	VIA RAT
DMASS0_INTAGGR_L2G	0x0048120000	VIA RAT
DMASS0_PSILCFG_PROXY	0x0048130000	VIA RAT
DMASS0_PSILSS_MMRS	0x0048140000	VIA RAT
DMASS0_INTAGGR_UNMAP	0x0048180000	VIA RAT
DMASS0_INTAGGR_MCAST	0x0048210000	VIA RAT
DMASS0_INTAGGR_GCNTCFG	0x0048220000	VIA RAT
DMASS0_RINGACC_GCFG	0x0048240000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
DMASS0_SEC_PROXY_MMRS	0x0048250000	VIA RAT
DMASS0_BCDMA_BCHAN	0x0048420000	VIA RAT
DMASS0_PKTDMA_RFLOW	0x0048430000	VIA RAT
DMASS0_PKTDMA_TCHAN	0x00484A0000	VIA RAT
DMASS0_BCDMA_TCHAN	0x00484A4000	VIA RAT
DMASS0_PKTDMA_RCHAN	0x00484C0000	VIA RAT
DMASS0_BCDMA_RCHAN	0x00484C4000	VIA RAT
DMASS0_PKTDMA_GCFG	0x00485C0000	VIA RAT
DMASS0_BCDMA_GCFG	0x00485C0100	VIA RAT
DMASS0_PKTDMA_RING	0x00485E0000	VIA RAT
DMASS0_BCDMA_RING	0x0048600000	VIA RAT
DMASS0_RINGACC_RT	0x0049000000	VIA RAT
DMASS0_RINGACC_CFG	0x0049800000	VIA RAT
DMASS0_INTAGGR_GCNTRTI	0x004A000000	VIA RAT
DMASS0_SEC_PROXY_SCFG	0x004A400000	VIA RAT
DMASS0_SEC_PROXY_RT	0x004A600000	VIA RAT
DMASS0_PKTDMA_RCHANRT	0x004A800000	VIA RAT
DMASS0_BCDMA_RCHANRT	0x004A840000	VIA RAT
DMASS0_PKTDMA_TCHANRT	0x004AA00000	VIA RAT
DMASS0_BCDMA_TCHANRT	0x004AA40000	VIA RAT
DMASS0_PKTDMA_RINGRT	0x004B800000	VIA RAT
DMASS0_BCDMA_RINGRT	0x004BC00000	VIA RAT
DMASS0_BCDMA_BCHANRT	0x004C000000	VIA RAT
DMASS0_SEC_PROXY_SRC_TARGET_DATA	0x004D000000	VIA RAT
FSS1_OSPI1_R1	0x0058000000	VIA RAT
FSS0_DAT_REG1	0x0060000000	VIA RAT
FSS1_DAT_REG1	0x0068000000	VIA RAT
MSRAM_1MB0_RAM	0x0072000000	VIA RAT
MSRAM_1MB1_RAM	0x0072100000	VIA RAT
MSRAM_1MB2_RAM	0x0072200000	VIA RAT
MSRAM_1MB3_RAM	0x0072300000	VIA RAT
MSRAM_1MB4_RAM	0x0072400000	VIA RAT
MSRAM_1MB5_RAM	0x0072500000	VIA RAT
WKUP_R5FSS0_CORE0_ICACHE	0x0074000000	VIA RAT
WKUP_R5FSS0_CORE0_DCACHE	0x0074800000	VIA RAT
R5FSS0_CORE0_ICACHE	0x0076000000	VIA RAT
R5FSS0_CORE0_DCACHE	0x0076800000	VIA RAT
R5FSS0_CORE1_ICACHE	0x0077000000	VIA RAT
R5FSS0_CORE1_DCACHE	0x0077800000	VIA RAT
WKUP_R5FSS0_CORE0_ATCM	0x0078000000	VIA RAT
WKUP_R5FSS0_CORE0_BTCM	0x0078100000	VIA RAT
R5FSS1_CORE0_ICACHE	0x0079000000	VIA RAT
R5FSS1_CORE0_DCACHE	0x0079800000	VIA RAT
R5FSS1_CORE1_ICACHE	0x007A000000	VIA RAT
R5FSS1_CORE1_DCACHE	0x007A800000	VIA RAT
C7X256V0_UMC	0x007C000000	VIA RAT
C7X256V0_CLEC	0x007C200000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
C7X256V0_DRU	0x007C400000	VIA RAT
C7X256V0_DRU_SET	0x007C404000	VIA RAT
C7X256V0_DRU_QUEUE	0x007C408000	VIA RAT
C7X256V0_DRU_CHNRT	0x007C440000	VIA RAT
C7X256V0_DRU_CHRT	0x007C460000	VIA RAT
C7X256V0_DRU_CHATOMIC_DEBUG	0x007C480000	VIA RAT
C7X256V0_DRU_CHCORE	0x007C4A0000	VIA RAT
C7X256V0_DRU	0x007C4E0000	VIA RAT
C7X256V1_UMC	0x007D000000	VIA RAT
C7X256V1_CLEC	0x007D200000	VIA RAT
C7X256V1_DRU	0x007D400000	VIA RAT
C7X256V1_DRU_SET	0x007D404000	VIA RAT
C7X256V1_DRU_QUEUE	0x007D408000	VIA RAT
C7X256V1_DRU_CHNRT	0x007D440000	VIA RAT
C7X256V1_DRU_CHRT	0x007D460000	VIA RAT
C7X256V1_DRU_CHATOMIC_DEBUG	0x007D480000	VIA RAT
C7X256V1_DRU_CHCORE	0x007D4A0000	VIA RAT
C7X256V1_DRU	0x007D4E0000	VIA RAT
C7X256V0_UMC_MEM_MAIN	0x007E000000	VIA RAT
C7X256V0_UMC_MEM_AUX	0x007E200000	VIA RAT
C7X256V1_UMC_MEM_MAIN	0x007F000000	VIA RAT
C7X256V1_UMC_MEM_AUX	0x007F200000	VIA RAT
FSS1_DAT_REG0	0x0200000000	VIA RAT
FSS1_DAT_REG3	0x0300000000	VIA RAT
FSS0_DAT_REG0	0x0400000000	VIA RAT
FSS0_DAT_REG3	0x0500000000	VIA RAT
FSS1_OSPI1_R0	0x0600000000	VIA RAT
DEBUGSS_WRAP0_ROM_TABLE_0_0	0x0700000000	VIA RAT
DEBUGSS_WRAP0_RESV0_0	0x0700001000	VIA RAT
DEBUGSS_WRAP0_CFGAP0	0x0700002000	VIA RAT
DEBUGSS_WRAP0_APBAP0	0x0700002100	VIA RAT
DEBUGSS_WRAP0_AXIAP0	0x0700002200	VIA RAT
DEBUGSS_WRAP0_PWRAP0	0x0700002300	VIA RAT
DEBUGSS_WRAP0_PVIEW0	0x0700002400	VIA RAT
DEBUGSS_WRAP0_JTAGAP0	0x0700002500	VIA RAT
DEBUGSS_WRAP0_SECAP0	0x0700002600	VIA RAT
DEBUGSS_WRAP0_CORTEX0_CFG0	0x0700002700	VIA RAT
DEBUGSS_WRAP0_CORTEX1_CFG0	0x0700002800	VIA RAT
DEBUGSS_WRAP0_CORTEX2_CFG0	0x0700002900	VIA RAT
DEBUGSS_WRAP0_CORTEX3_CFG0	0x0700002A00	VIA RAT
DEBUGSS_WRAP0_CORTEX4_CFG0	0x0700002B00	VIA RAT
DEBUGSS_WRAP0_CORTEX5_CFG0	0x0700002C00	VIA RAT
DEBUGSS_WRAP0_CORTEX6_CFG0	0x0700002D00	VIA RAT
DEBUGSS_WRAP0_CORTEX7_CFG0	0x0700002E00	VIA RAT
DEBUGSS_WRAP0_CORTEX8_CFG0	0x0700002F00	VIA RAT
DEBUGSS_WRAP0_RESV1_0	0x0700003000	VIA RAT
DEBUGSS_WRAP0_RESV2_0	0x0700004000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
DEBUGSS_WRAP0_ROM_TABLE_1_0	0x0720000000	VIA RAT
DEBUGSS_WRAP0_CSCTI	0x0720001000	VIA RAT
DEBUGSS_WRAP0_DRM0	0x0720002000	VIA RAT
DEBUGSS_WRAP0_RESV3_0	0x0720003000	VIA RAT
DEBUGSS_WRAP0_CSTPIU0	0x0720004000	VIA RAT
DEBUGSS_WRAP0_CTF0	0x0720005000	VIA RAT
DEBUGSS_WRAP0_RESV4_0	0x0720006000	VIA RAT
DEBUGSS_WRAP0_EXT_APB0	0x0730000000	VIA RAT
C7X256V0_THINMAN	0x0734000000	VIA RAT
C7X256V0_COLOMBO	0x0734001000	VIA RAT
C7X256V0_MATLOCK	0x0734002000	VIA RAT
C7X256V0_CSCTI	0x0734003000	VIA RAT
C7X256V0_CTSET2	0x0734008000	VIA RAT
C7X256V0_CSCTI	0x073400A000	VIA RAT
C7X256V0_CSCTI	0x073400B000	VIA RAT
C7X256V0_DBG_AGR0_MMR	0x0734040000	VIA RAT
C7X256V0_DBG_AGR0_MEM_CFG	0x0734040100	VIA RAT
C7X256V0_DBG_AGR0_MEM0	0x0734060000	VIA RAT
C7X256V0_DBG_AGR0_MEM1	0x0734061000	VIA RAT
C7X256V0_DBG_AGR0_MEM2	0x0734062000	VIA RAT
C7X256V0_DBG_AGR0_MEM3	0x0734063000	VIA RAT
C7X256V0_DBG_AGR0_MEM4	0x0734064000	VIA RAT
C7X256V0_DBG_AGR0_MEM5	0x0734065000	VIA RAT
C7X256V0_DBG_AGR0_MEM6	0x0734066000	VIA RAT
C7X256V0_DBG_AGR0_MEM7	0x0734067000	VIA RAT
C7X256V0_DBG_AGR0_MEM8	0x0734068000	VIA RAT
C7X256V0_DBG_AGR0_MEM9	0x0734069000	VIA RAT
C7X256V0_DBG_AGR0_MEM10	0x073406A000	VIA RAT
C7X256V0_DBG_AGR0_MEM11	0x073406B000	VIA RAT
C7X256V0_DBG_AGR0_MEM12	0x073406C000	VIA RAT
C7X256V0_DBG_AGR0_MEM13	0x073406D000	VIA RAT
C7X256V0_DBG_AGR0_MEM14	0x073406E000	VIA RAT
C7X256V0_DBG_AGR0_MEM15	0x073406F000	VIA RAT
C7X256V0_DBG_AGR0_MEM16	0x0734070000	VIA RAT
C7X256V0_DBG_AGR0_MEM17	0x0734071000	VIA RAT
C7X256V0_DBG_AGR0_MEM18	0x0734072000	VIA RAT
C7X256V0_DBG_AGR0_MEM19	0x0734073000	VIA RAT
C7X256V0_DBG_AGR0_MEM20	0x0734074000	VIA RAT
C7X256V0_DBG_AGR0_MEM21	0x0734075000	VIA RAT
C7X256V0_DBG_AGR0_MEM22	0x0734076000	VIA RAT
C7X256V0_DBG_AGR0_MEM23	0x0734077000	VIA RAT
C7X256V0_DBG_AGR0_MEM24	0x0734078000	VIA RAT
C7X256V0_DBG_AGR0_MEM25	0x0734079000	VIA RAT
C7X256V0_DBG_AGR0_MEM26	0x073407A000	VIA RAT
C7X256V0_DBG_AGR0_MEM27	0x073407B000	VIA RAT
C7X256V0_DBG_AGR0_MEM28	0x073407C000	VIA RAT
C7X256V0_DBG_AGR0_MEM29	0x073407D000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
C7X256V0_DBG_AGR0_MEM30	0x073407E000	VIA RAT
C7X256V0_DBG_AGR0_MEM31	0x073407F000	VIA RAT
C7X256V1_THINMAN	0x0738000000	VIA RAT
C7X256V1_COLOMBO	0x0738001000	VIA RAT
C7X256V1_MATLOCK	0x0738002000	VIA RAT
C7X256V1_CSCTI	0x0738003000	VIA RAT
C7X256V1_CTSET2	0x0738008000	VIA RAT
C7X256V1_CSCTI	0x073800A000	VIA RAT
C7X256V1_CSCTI	0x073800B000	VIA RAT
C7X256V1_DBG_AGR0_MMR	0x0738040000	VIA RAT
C7X256V1_DBG_AGR0_MEM_CFG	0x0738040100	VIA RAT
C7X256V1_DBG_AGR0_MEM0	0x0738060000	VIA RAT
C7X256V1_DBG_AGR0_MEM1	0x0738061000	VIA RAT
C7X256V1_DBG_AGR0_MEM2	0x0738062000	VIA RAT
C7X256V1_DBG_AGR0_MEM3	0x0738063000	VIA RAT
C7X256V1_DBG_AGR0_MEM4	0x0738064000	VIA RAT
C7X256V1_DBG_AGR0_MEM5	0x0738065000	VIA RAT
C7X256V1_DBG_AGR0_MEM6	0x0738066000	VIA RAT
C7X256V1_DBG_AGR0_MEM7	0x0738067000	VIA RAT
C7X256V1_DBG_AGR0_MEM8	0x0738068000	VIA RAT
C7X256V1_DBG_AGR0_MEM9	0x0738069000	VIA RAT
C7X256V1_DBG_AGR0_MEM10	0x073806A000	VIA RAT
C7X256V1_DBG_AGR0_MEM11	0x073806B000	VIA RAT
C7X256V1_DBG_AGR0_MEM12	0x073806C000	VIA RAT
C7X256V1_DBG_AGR0_MEM13	0x073806D000	VIA RAT
C7X256V1_DBG_AGR0_MEM14	0x073806E000	VIA RAT
C7X256V1_DBG_AGR0_MEM15	0x073806F000	VIA RAT
C7X256V1_DBG_AGR0_MEM16	0x0738070000	VIA RAT
C7X256V1_DBG_AGR0_MEM17	0x0738071000	VIA RAT
C7X256V1_DBG_AGR0_MEM18	0x0738072000	VIA RAT
C7X256V1_DBG_AGR0_MEM19	0x0738073000	VIA RAT
C7X256V1_DBG_AGR0_MEM20	0x0738074000	VIA RAT
C7X256V1_DBG_AGR0_MEM21	0x0738075000	VIA RAT
C7X256V1_DBG_AGR0_MEM22	0x0738076000	VIA RAT
C7X256V1_DBG_AGR0_MEM23	0x0738077000	VIA RAT
C7X256V1_DBG_AGR0_MEM24	0x0738078000	VIA RAT
C7X256V1_DBG_AGR0_MEM25	0x0738079000	VIA RAT
C7X256V1_DBG_AGR0_MEM26	0x073807A000	VIA RAT
C7X256V1_DBG_AGR0_MEM27	0x073807B000	VIA RAT
C7X256V1_DBG_AGR0_MEM28	0x073807C000	VIA RAT
C7X256V1_DBG_AGR0_MEM29	0x073807D000	VIA RAT
C7X256V1_DBG_AGR0_MEM30	0x073807E000	VIA RAT
C7X256V1_DBG_AGR0_MEM31	0x073807F000	VIA RAT
DEBUGSS0_DEBUG_CELL_ROM_SLV	0x073C020000	VIA RAT
DEBUGSS0_CTSET2_WRAP_CFG_CTSET2_CFG	0x073C022000	VIA RAT
DEBUGSS0_ATB_REPLICATOR_CFG_CXATBREPLICATOR_CFG	0x073C024000	VIA RAT
DEBUGSS0_TBR_VBUSP_WRAP_TBR_CFG_TBR_CFG	0x073C025000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
DEBUGSS0_ARM_CTI_0_CFG_CSCTI_CFG	0x073C026000	VIA RAT
DEBUGSS0_ARM_CTI_1_CFG_CSCTI_CFG	0x073C028000	VIA RAT
DEBUGSS0_ARM_CTI_2_CFG_CSCTI_CFG	0x073C029000	VIA RAT
DEBUGSS0_ARM_CTI_3_CFG_CSCTI_CFG	0x073C02A000	VIA RAT
DEBUGSS0_ARM_CTI_4_CFG_CSCTI_CFG	0x073C02B000	VIA RAT
DEBUGSS0_ARM_CTI_5_CFG_CSCTI_CFG	0x073C02C000	VIA RAT
DEBUGSS0_ARM_CTI_6_CFG_CSCTI_CFG	0x073C02D000	VIA RAT
DEBUGSS0_ARM_CTI_7_CFG_CSCTI_CFG	0x073C02E000	VIA RAT
DEBUGSS0_ARM_CTI_8_CFG_CSCTI_CFG	0x073C02F000	VIA RAT
STM0_CSSTM	0x073D200000	VIA RAT
STM0_CTI_CSCTI	0x073D201000	VIA RAT
DBG_INTROUTER0_INTR_ROUTER_CFG	0x073D300000	VIA RAT
CPT2_AGGR0_MMR	0x073E100000	VIA RAT
CPT2_AGGR0_STP2ATB_CFG	0x073E100100	VIA RAT
CPT2_AGGR0_MEM0	0x073E120000	VIA RAT
CPT2_AGGR0_MEM1	0x073E121000	VIA RAT
CPT2_AGGR0_MEM2	0x073E122000	VIA RAT
CPT2_AGGR0_MEM3	0x073E123000	VIA RAT
CPT2_AGGR0_MEM4	0x073E124000	VIA RAT
CPT2_AGGR0_MEM5	0x073E125000	VIA RAT
CPT2_AGGR0_MEM6	0x073E126000	VIA RAT
CPT2_AGGR0_MEM7	0x073E127000	VIA RAT
CPT2_AGGR0_MEM8	0x073E128000	VIA RAT
CPT2_AGGR0_MEM9	0x073E129000	VIA RAT
CPT2_AGGR0_MEM10	0x073E12A000	VIA RAT
CPT2_AGGR0_MEM11	0x073E12B000	VIA RAT
CPT2_AGGR0_MEM12	0x073E12C000	VIA RAT
CPT2_AGGR0_MEM13	0x073E12D000	VIA RAT
CPT2_AGGR0_MEM14	0x073E12E000	VIA RAT
CPT2_AGGR0_MEM15	0x073E12F000	VIA RAT
CPT2_AGGR0_MEM16	0x073E130000	VIA RAT
CPT2_AGGR0_MEM17	0x073E131000	VIA RAT
CPT2_AGGR0_MEM18	0x073E132000	VIA RAT
CPT2_AGGR0_MEM19	0x073E133000	VIA RAT
CPT2_AGGR0_MEM20	0x073E134000	VIA RAT
CPT2_AGGR0_MEM21	0x073E135000	VIA RAT
CPT2_AGGR0_MEM22	0x073E136000	VIA RAT
CPT2_AGGR0_MEM23	0x073E137000	VIA RAT
CPT2_AGGR0_MEM24	0x073E138000	VIA RAT
CPT2_AGGR0_MEM25	0x073E139000	VIA RAT
CPT2_AGGR0_MEM26	0x073E13A000	VIA RAT
CPT2_AGGR0_MEM27	0x073E13B000	VIA RAT
CPT2_AGGR0_MEM28	0x073E13C000	VIA RAT
CPT2_AGGR0_MEM29	0x073E13D000	VIA RAT
CPT2_AGGR0_MEM30	0x073E13E000	VIA RAT
CPT2_AGGR0_MEM31	0x073E13F000	VIA RAT
CPT2_AGGR1_MMR	0x073E140000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
CPT2_AGGR1_STP2ATB_CFG	0x073E140100	VIA RAT
CPT2_AGGR1_MEM0	0x073E160000	VIA RAT
CPT2_AGGR1_MEM1	0x073E161000	VIA RAT
CPT2_AGGR1_MEM2	0x073E162000	VIA RAT
CPT2_AGGR1_MEM3	0x073E163000	VIA RAT
CPT2_AGGR1_MEM4	0x073E164000	VIA RAT
CPT2_AGGR1_MEM5	0x073E165000	VIA RAT
CPT2_AGGR1_MEM6	0x073E166000	VIA RAT
CPT2_AGGR1_MEM7	0x073E167000	VIA RAT
CPT2_AGGR1_MEM8	0x073E168000	VIA RAT
CPT2_AGGR1_MEM9	0x073E169000	VIA RAT
CPT2_AGGR1_MEM10	0x073E16A000	VIA RAT
CPT2_AGGR1_MEM11	0x073E16B000	VIA RAT
CPT2_AGGR1_MEM12	0x073E16C000	VIA RAT
CPT2_AGGR1_MEM13	0x073E16D000	VIA RAT
CPT2_AGGR1_MEM14	0x073E16E000	VIA RAT
CPT2_AGGR1_MEM15	0x073E16F000	VIA RAT
CPT2_AGGR1_MEM16	0x073E170000	VIA RAT
CPT2_AGGR1_MEM17	0x073E171000	VIA RAT
CPT2_AGGR1_MEM18	0x073E172000	VIA RAT
CPT2_AGGR1_MEM19	0x073E173000	VIA RAT
CPT2_AGGR1_MEM20	0x073E174000	VIA RAT
CPT2_AGGR1_MEM21	0x073E175000	VIA RAT
CPT2_AGGR1_MEM22	0x073E176000	VIA RAT
CPT2_AGGR1_MEM23	0x073E177000	VIA RAT
CPT2_AGGR1_MEM24	0x073E178000	VIA RAT
CPT2_AGGR1_MEM25	0x073E179000	VIA RAT
CPT2_AGGR1_MEM26	0x073E17A000	VIA RAT
CPT2_AGGR1_MEM27	0x073E17B000	VIA RAT
CPT2_AGGR1_MEM28	0x073E17C000	VIA RAT
CPT2_AGGR1_MEM29	0x073E17D000	VIA RAT
CPT2_AGGR1_MEM30	0x073E17E000	VIA RAT
CPT2_AGGR1_MEM31	0x073E17F000	VIA RAT
CPT2_AGGR2_MMR	0x073E180000	VIA RAT
CPT2_AGGR2_STP2ATB_CFG	0x073E180100	VIA RAT
CPT2_AGGR2_MEM0	0x073E1A0000	VIA RAT
CPT2_AGGR2_MEM1	0x073E1A1000	VIA RAT
CPT2_AGGR2_MEM2	0x073E1A2000	VIA RAT
CPT2_AGGR2_MEM3	0x073E1A3000	VIA RAT
CPT2_AGGR2_MEM4	0x073E1A4000	VIA RAT
CPT2_AGGR2_MEM5	0x073E1A5000	VIA RAT
CPT2_AGGR2_MEM6	0x073E1A6000	VIA RAT
CPT2_AGGR2_MEM7	0x073E1A7000	VIA RAT
CPT2_AGGR2_MEM8	0x073E1A8000	VIA RAT
CPT2_AGGR2_MEM9	0x073E1A9000	VIA RAT
CPT2_AGGR2_MEM10	0x073E1AA000	VIA RAT
CPT2_AGGR2_MEM11	0x073E1AB000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
CPT2_AGGR2_MEM12	0x073E1AC000	VIA RAT
CPT2_AGGR2_MEM13	0x073E1AD000	VIA RAT
CPT2_AGGR2_MEM14	0x073E1AE000	VIA RAT
CPT2_AGGR2_MEM15	0x073E1AF000	VIA RAT
CPT2_AGGR2_MEM16	0x073E1B0000	VIA RAT
CPT2_AGGR2_MEM17	0x073E1B1000	VIA RAT
CPT2_AGGR2_MEM18	0x073E1B2000	VIA RAT
CPT2_AGGR2_MEM19	0x073E1B3000	VIA RAT
CPT2_AGGR2_MEM20	0x073E1B4000	VIA RAT
CPT2_AGGR2_MEM21	0x073E1B5000	VIA RAT
CPT2_AGGR2_MEM22	0x073E1B6000	VIA RAT
CPT2_AGGR2_MEM23	0x073E1B7000	VIA RAT
CPT2_AGGR2_MEM24	0x073E1B8000	VIA RAT
CPT2_AGGR2_MEM25	0x073E1B9000	VIA RAT
CPT2_AGGR2_MEM26	0x073E1BA000	VIA RAT
CPT2_AGGR2_MEM27	0x073E1BB000	VIA RAT
CPT2_AGGR2_MEM28	0x073E1BC000	VIA RAT
CPT2_AGGR2_MEM29	0x073E1BD000	VIA RAT
CPT2_AGGR2_MEM30	0x073E1BE000	VIA RAT
CPT2_AGGR2_MEM31	0x073E1BF000	VIA RAT
DEBUGSS_WRAP0_ROM_TABLE_0_1	0x0740000000	VIA RAT
DEBUGSS_WRAP0_RESV0_1	0x0740001000	VIA RAT
DEBUGSS_WRAP0_CFGAP1	0x0740002000	VIA RAT
DEBUGSS_WRAP0_APBAP1	0x0740002100	VIA RAT
DEBUGSS_WRAP0_AXIAP1	0x0740002200	VIA RAT
DEBUGSS_WRAP0_PWRAP1	0x0740002300	VIA RAT
DEBUGSS_WRAP0_PVIEW1	0x0740002400	VIA RAT
DEBUGSS_WRAP0_JTAGAP1	0x0740002500	VIA RAT
DEBUGSS_WRAP0_SECAP1	0x0740002600	VIA RAT
DEBUGSS_WRAP0_CORTEX0_CFG1	0x0740002700	VIA RAT
DEBUGSS_WRAP0_CORTEX1_CFG1	0x0740002800	VIA RAT
DEBUGSS_WRAP0_CORTEX2_CFG1	0x0740002900	VIA RAT
DEBUGSS_WRAP0_CORTEX3_CFG1	0x0740002A00	VIA RAT
DEBUGSS_WRAP0_CORTEX4_CFG1	0x0740002B00	VIA RAT
DEBUGSS_WRAP0_CORTEX5_CFG1	0x0740002C00	VIA RAT
DEBUGSS_WRAP0_CORTEX6_CFG1	0x0740002D00	VIA RAT
DEBUGSS_WRAP0_CORTEX7_CFG1	0x0740002E00	VIA RAT
DEBUGSS_WRAP0_CORTEX8_CFG1	0x0740002F00	VIA RAT
DEBUGSS_WRAP0_RESV1_1	0x0740003000	VIA RAT
DEBUGSS_WRAP0_RESV2_1	0x0740004000	VIA RAT
DEBUGSS_WRAP0_ROM_TABLE_1_1	0x0760000000	VIA RAT
DEBUGSS_WRAP0_CSCTI	0x0760001000	VIA RAT
DEBUGSS_WRAP0_DRM1	0x0760002000	VIA RAT
DEBUGSS_WRAP0_RESV3_1	0x0760003000	VIA RAT
DEBUGSS_WRAP0_CSTPIU1	0x0760004000	VIA RAT
DEBUGSS_WRAP0_CTF1	0x0760005000	VIA RAT
DEBUGSS_WRAP0_RESV4_1	0x0760006000	VIA RAT

Table 2-4. SoC Memory Map (continued)

Region Name	Start Address	DM R5F and Main R5F Access
DEBUGSS_WRAP0_EXT_APB1	0x0770000000	VIA RAT
FSS1_OSPI1_R3	0x0A00000000	VIA RAT

3 Interconnect

Note

This TRM uses the prefix of "MCU_" for items that refer to the device as a whole instead of a specific domain. "MCU_" is the equivalent of Top Level from Section 1.5.

3.1 System Interconnect Overview

3.1.1 Terminology

- CBASS: this is a crossbar module to provide physical connection among the initiators and targets
- VBUSP interface: a single-issue interface
- VBUSM interface: a multi-issue interface
- Channel ID: channel ID for interface indicates a logical flow. All the transactions with the same channel ID coming from the same initiator interface are consider orthogonal and independent flow.
- OrderID: a 4 bits value associated with each transaction. All the transactions from the same initiator to the same target end point with the same orderID needs to be executed in order. OrderID is also to be used to select real-time and non-real time path for the transaction. OrderID 8-15 reserved for real-time path.
- Asel: Address Selection. Asel can be either used for select a unique memory map or be used to indicate the IO coherent transactions.
- PrivID: indicates the security access group. PrivID is assigned by the ISC block.
- ISC: stands for Initiator Security Control.
- Region based firewall: this is firewall block based on address region.
- Channelized firewall: firewall block with finer granularity down to register level with fixed region size.
- QoS: Quality of Service block is a feature which can be enabled for each CBA initiator port. Each initiator can choose to enable the QoS feature in the CBA configuration file. If an initiator port supports channel ID, the QoS block provides priority and order ID for each channel, otherwise all the transactions from that initiator port share the same priority and order ID value.

CAUTION

Since OrderID is used for ordering purpose in CBASS, changing the order ID when the system is running can cause system deadlock. Therefore, QoS configuration shall be part of the initialization steps, if the application wants to change the QoS setting from the default value.

3.2 Domain Partition

SoC is partitioned into several domains which are connected by interconnect modules.

- **MAIN Domain**: there are multiple interconnect components providing the connectivity among initiators and target interfaces for the processors and peripherals in the MAIN domain. The main application processors, such as Main R5FSS, are located in the MAIN domain.
- **WKUP domain**: WKUP domain refers to the domain containing Device Management
- **Top Level domain**: Device level items are considered Top Level and begins with the "MCU_" prefix

All modules connected to WKUP_safe interconnect can belong to both Top Level domain and WKUP domain depending on the use case. When the Top Level domain is configured for a safety use case, all of the modules connected to WKUP_safe interconnect are be part of the Top Level domain.

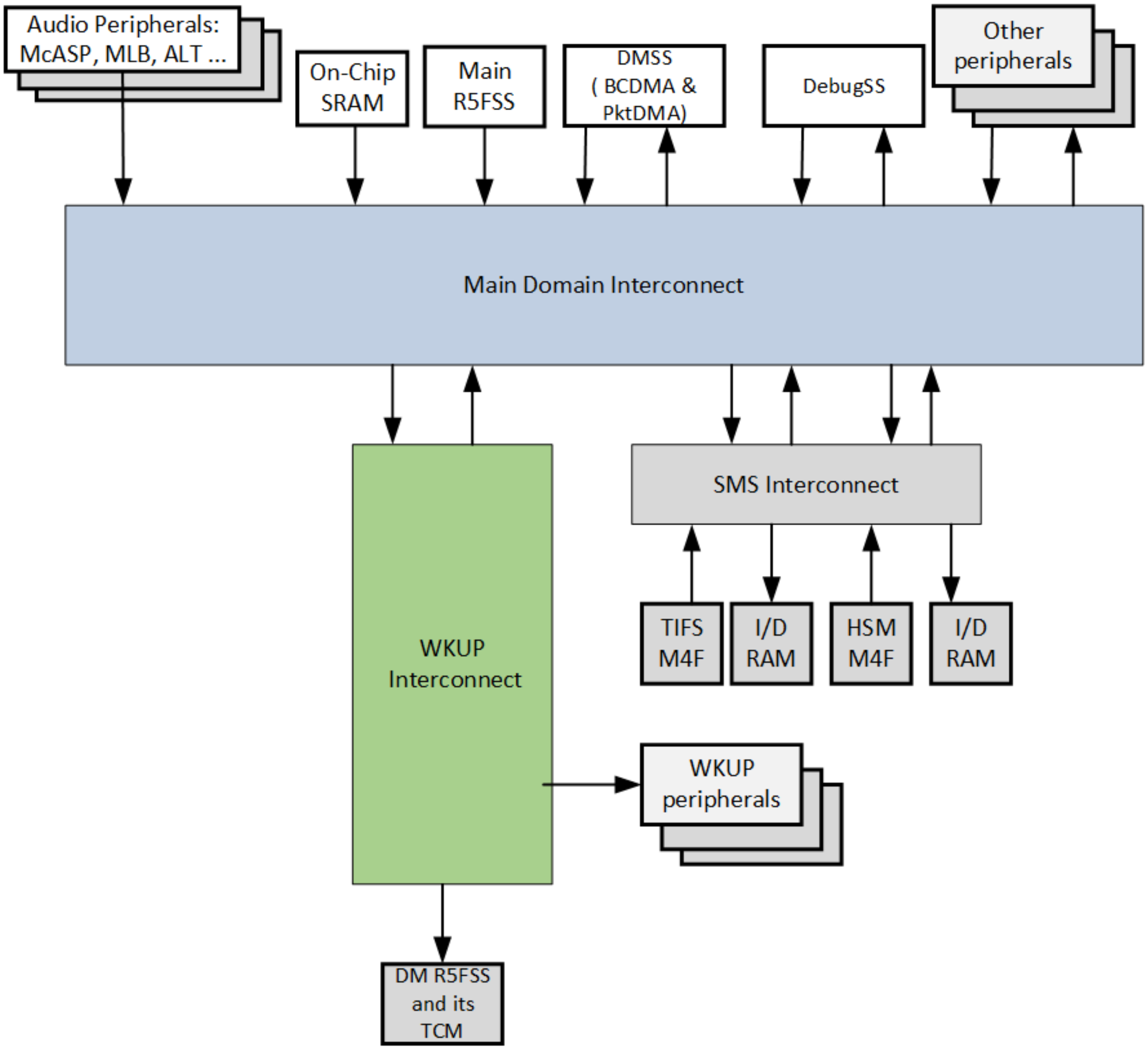


Figure 3-1. System Interconnect Overview

3.3 Initiator/Target Connectivity

All processors and the DMA can communicate with all SoC memory mapped peripherals.

3.4 Performance Tuning

3.4.1 Latency Reduction

The auto clock gating feature of WKUP domain peripherals is enabled by default for all expected for the CBA_NOGATE bits that have the default value of 0x1.

The disabling of auto clock gating may result in improved performance.

The auto clock gating control can be modified during device initialization time through registers CLKGATE_CTRL0 and CLKGATE_CTRL1 in the WKUP_CTRL_MMR and CLKGATE_CTRL regsiter in the MCU_CTRL_MMR.

3.4.2 Using Quality of Service (QoS) MMR

The majority of the initiator has a dedicated QoS block to provide the configurability of the transaction characteristic, such as OrderID, priority/epriority, asel and etc. The user can utilize the OrderID and priority/epriority fields to fine tune the performance.

OrderID is a 4 bits value, which is associated with each transaction. By default, all the transactions have orderID value set to 0x0. The OrderID is used as a mechanism to load balance the traffic to DDR through two parallel paths. The transactions with order ID 0-7 share one path, while transactions with 8-15 share a separate path. The OrderID value can be changed through QoS block for the initiators or through BCDMA and pktDMA configuration.

Each transaction in the system carries 3 bits priority information. The priority information is used for interconnect for arbitration decision, which implements typical priority based round robin. Priority value 0x0 is the highest priority, while 0x7 is the lowest priority. By default, QoS has priority value set to 0x7(lowest priority). The priority and epriority can be changed through the QoS block for each initiator.

Some of the modules such as DSS is able to adjust the priority of the transaction based on the system congestion condition. But majority of the transactions have static priority level set by the QoS block. But the priority setting through QoS block can be tuned to fit certain use case scenarios.

CAUTION

Priority, orderID and asel value from the QoS block shall only be modified as part of the initialization steps, when the SoC is idle. Changing the QoS block configuration during the run time is prohibited, and may cause system error or other undefined behavior.

3.4.3 QoS MMR Programming Guide

The QoS MMR is integrated as part of data plane interconnect to provide programmability of priority, orderID and QoS sideband signals for each initiator port in the data plane. Currently the QoS sideband signal is not used for any routing or schedule purpose. For most of the initiator ports, it has only one setting of the orderID and QoS field. For the initiator port supports with multiple channels, the transactions in each channel can be programmed to have different sets of priority, orderID and QoS. The orderID is a four-bit field value. All the transactions coming from the same initiator ports with the same orderID expect to receive the read data in order.

In the previous generation of the interconnect, how the traffic is split among parallel paths to the same end points was hard coded. The traffic from a certain initiator port was hard coded to choose one of the parallel paths. Due to the nature of hard coded, the system could not load balance based on the use case. The current generation of interconnect removes this limitation by splitting traffic using the OrderID value. Since the orderID value for the traffic from each initiator port is programmable, the user can load balance based on the use case scenario.

Each target port in each SCR has its own arbiter. The SoC interconnect arbitration is based on priority. For the ports with equal priority, the arbiter uses round robin to break the tie.

3.5 Interconnect Debugging Feature

Interconnect routes the transaction to null end point for graceful termination under the following situation:

- There is no physical connection between initiator and target end points
- Or target interface is in disabled state
- Or the transaction is sent to an unpopulated address

The null end point returns the error status back to the initiator to prevent the interconnect hang. At the same time, the interconnect module logs this transaction information in err_reg region and issues an error interrupt (default_err_intr). This default_err_intr is sent to all of the application processors for debug purposes.

If the transaction is sent to a valid target interface, however the firewall in front of the target interface can prohibit the transaction, the transaction will be logged in the glb_regs region and the interconnect will assert a default_exp interrupt.

4 Module Integration

4.1 Integration Overview

This section goes over the integration (clock, power, resets, and interrupts) of features in the device.

Note

PSC0 is also known as MAIN_PSC0 and PSCSS

4.2 Processors and Accelerators

4.2.1 DSP (C7X256V)

This section contains the integration details for the DSP module on this device. For Further information, see the DSP (C7X256V) section of the Processors and Accelerators chapter.

4.2.1.1 C7X256V Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.2.1.2 Module Allocations

Table 4-1. C7X256V Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
C7X256V0 (DSP0 C7x)			✓
C7X256V1 (DSP1 C7x)			✓

4.2.1.3 Resets, Interrupts, and Clocks

Table 4-2. C7X256V Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
C7X256V0	MAIN_PSC0	PD_C7X0	LPSC_C7X0_CORE	59	OFF	YES	LPSC_C7X0_COMMON
C7X256V1	MAIN_PSC0	PD_C7X1	LPSC_C7X1_CORE	62	OFF	YES	LPSC_C7X1_COMMON
C7X256V0_PBIST	MAIN_PSC0	PD_C7X0	LPSC_MAIN_C7X0_PBIST	60	OFF	YES	LPSC_C7X0_COMMON
C7X256V1_PBIST	MAIN_PSC0	PD_C7X1	LPSC_MAIN_C7X1_PBIST	63	OFF	YES	LPSC_C7X1_COMMON

Table 4-3. C7X256V Resets

Module Instance	Source	Description
C7X256V0	MAIN_PSC0	C7X256V0_C7XV_CORE_0 reset
C7X256V1	MAIN_PSC0	C7X256V1_C7XV_CORE_0 reset

Table 4-4. C7X256V Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event0_IN_226	ESM0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event1_IN_226	ESM0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event2_IN_226	ESM0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	R5FSS0_CORE0_intr_IN_113	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	R5FSS0_CORE1_intr_IN_113	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	R5FSS1_CORE0_intr_IN_113	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	pulse

Table 4-4. C7X256V Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	R5FSS1_CORE1_intr_IN_113	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_cpu_0	WKUP_R5FSS0_CORE0_intr_IN_113	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	pulse
C7X256V0_CLEC	C7X256V0_CLEC_dft_pbist_safety_error_0	ESM0_esm_lvl_event_IN_149	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_[7:0]	ESM0_esm_lvl_event_IN_160	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_[7:0]	ESM0_esm_lvl_event_IN_161	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_[7:0]	ESM0_esm_lvl_event_IN_162	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_[7:0]	ESM0_esm_lvl_event_IN_163	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_[7:0]	ESM0_esm_lvl_event_IN_164	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_[7:0]	ESM0_esm_lvl_event_IN_165	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_[7:0]	ESM0_esm_lvl_event_IN_166	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_esm_events_out_level_[7:0]	ESM0_esm_lvl_event_IN_167	ESM0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	C7X256V1_CLEC_soc_events_in_IN_12	C7X256V1_CLEC	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	C7X256V1_CLEC_soc_events_in_IN_13	C7X256V1_CLEC	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	C7X256V1_CLEC_soc_events_in_IN_14	C7X256V1_CLEC	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	C7X256V1_CLEC_soc_events_in_IN_15	C7X256V1_CLEC	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE0_intr_IN_248	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level

Table 4-4. C7X256V Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE0_intr_IN_249	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE0_intr_IN_250	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE0_intr_IN_251	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE0_intr_IN_252	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE0_intr_IN_253	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE0_intr_IN_254	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE0_intr_IN_255	R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE1_intr_IN_248	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE1_intr_IN_249	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE1_intr_IN_250	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE1_intr_IN_251	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE1_intr_IN_252	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE1_intr_IN_253	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE1_intr_IN_254	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS0_CORE1_intr_IN_255	R5FSS0_CORE1	C7X256V0_CLEC interrupt request	level

Table 4-4. C7X256V Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE0_intr_IN_248	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE0_intr_IN_249	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE0_intr_IN_250	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE0_intr_IN_251	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE0_intr_IN_252	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE0_intr_IN_253	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE0_intr_IN_254	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE0_intr_IN_255	R5FSS1_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE1_intr_IN_248	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE1_intr_IN_249	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE1_intr_IN_250	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE1_intr_IN_251	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE1_intr_IN_252	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE1_intr_IN_253	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE1_intr_IN_254	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	level

Table 4-4. C7X256V Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	R5FSS1_CORE1_intr_IN_255	R5FSS1_CORE1	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	WKUP_R5FSS0_CORE0_intr_IN_249	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	WKUP_R5FSS0_CORE0_intr_IN_250	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	WKUP_R5FSS0_CORE0_intr_IN_254	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V0_CLEC	C7X256V0_CLEC_soc_events_out_level_[63:0]	WKUP_R5FSS0_CORE0_intr_IN_255	WKUP_R5FSS0_CORE0	C7X256V0_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_cpu_0	C7X256V1_CLEC_dft_pbist_cpu_0	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	pulse
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_cpu_0	R5FSS0_CORE1_intr_IN_113	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	pulse
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_cpu_0	R5FSS1_CORE0_intr_IN_113	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	pulse
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_cpu_0	R5FSS1_CORE1_intr_IN_113	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	pulse
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_cpu_0	WKUP_R5FSS0_CORE0_intr_IN_113	WKUP_R5FSS0_CORE0	C7X256V1_CLEC interrupt request	pulse
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event0_IN_245	ESM0	C7X256V1_CLEC interrupt request	pulse
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event1_IN_245	ESM0	C7X256V1_CLEC interrupt request	pulse
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_cpu_0	ESM0_esm_pls_event2_IN_245	ESM0	C7X256V1_CLEC interrupt request	pulse
C7X256V1_CLEC	C7X256V1_CLEC_dft_pbist_safety_error_0	ESM0_esm_lvl_event_IN_64	ESM0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_esm_events_out_level_[0:7]	ESM0_esm_lvl_event_IN_192	ESM0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_esm_events_out_level_[0:7]	ESM0_esm_lvl_event_IN_193	ESM0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_esm_events_out_level_[0:7]	ESM0_esm_lvl_event_IN_194	ESM0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_esm_events_out_level_[0:7]	ESM0_esm_lvl_event_IN_195	ESM0	C7X256V1_CLEC interrupt request	level

Table 4-4. C7X256V Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V1_CLEC	C7X256V1_CLEC_esm_events_out_level_[0:7]	ESM0_esm_lvl_event_IN_196	ESM0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_esm_events_out_level_[0:7]	ESM0_esm_lvl_event_IN_197	ESM0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_esm_events_out_level_[0:7]	ESM0_esm_lvl_event_IN_198	ESM0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_esm_events_out_level_[0:7]	ESM0_esm_lvl_event_IN_199	ESM0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	C7X256V0_CLEC_soc_events_in_IN_12	C7X256V0_CLEC	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	C7X256V0_CLEC_soc_events_in_IN_13	C7X256V0_CLEC	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	C7X256V0_CLEC_soc_events_in_IN_14	C7X256V0_CLEC	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	C7X256V0_CLEC_soc_events_in_IN_15	C7X256V0_CLEC	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE0_intr_IN_256	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE0_intr_IN_257	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE0_intr_IN_258	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE0_intr_IN_259	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE0_intr_IN_260	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE0_intr_IN_261	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE0_intr_IN_262	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level

Table 4-4. C7X256V Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE0_intr_IN_263	R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE1_intr_IN_256	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE1_intr_IN_257	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE1_intr_IN_258	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE1_intr_IN_259	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE1_intr_IN_260	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE1_intr_IN_261	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE1_intr_IN_262	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS0_CORE1_intr_IN_263	R5FSS0_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE0_intr_IN_256	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE0_intr_IN_257	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE0_intr_IN_258	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE0_intr_IN_259	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE0_intr_IN_260	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE0_intr_IN_261	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	level

Table 4-4. C7X256V Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE0_intr_IN_262	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE0_intr_IN_263	R5FSS1_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE1_intr_IN_256	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE1_intr_IN_257	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE1_intr_IN_258	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE1_intr_IN_259	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE1_intr_IN_260	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE1_intr_IN_261	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE1_intr_IN_262	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	R5FSS1_CORE1_intr_IN_263	R5FSS1_CORE1	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	WKUP_R5FSS0_CORE0_intr_IN_120	WKUP_R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	WKUP_R5FSS0_CORE0_intr_IN_121	WKUP_R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	WKUP_R5FSS0_CORE0_intr_IN_122	WKUP_R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level
C7X256V1_CLEC	C7X256V1_CLEC_soc_events_out_level_[0:63]	WKUP_R5FSS0_CORE0_intr_IN_165	WKUP_R5FSS0_CORE0	C7X256V1_CLEC interrupt request	level

Table 4-5. C7X256V Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
C7X256V0	PULSAR_PLL_CLK_CLK	MAIN_R5SS_CLK/2		
	DIVH_CLK2_PULSAR_GCLK	MAIN_PLL7_HSDIV0_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		
	DIVH_CLK2_SOC_GCLK	MAIN_PLL7_HSDIV0_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		
	DIVH_CLK4_GCLK	MAIN_PLL7_HSDIV0_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		
	DIVH_CLK4_SOC_GCLK	MAIN_PLL7_HSDIV0_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		
	DIVP_CLK1_GCLK	MAIN_PLL7_HSDIV0_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		

Table 4-5. C7X256V Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
C7X256V1	PULSAR_PLL_CLK_CLK	MAIN_R5SS_CLK/2		
	DIVH_CLK2_PULSAR_GCLK	MAIN_PLL7_HSDIV1_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		
	DIVH_CLK2_SOC_GCLK	MAIN_PLL7_HSDIV1_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		
	DIVH_CLK4_GCLK	MAIN_PLL7_HSDIV1_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		
	DIVH_CLK4_SOC_GCLK	MAIN_PLL7_HSDIV1_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		
	DIVP_CLK1_GCLK	MAIN_PLL7_HSDIV1_CLKOUT		
		MAIN_SYSCLK0		
		MAIN_R5SS_CLK/2		

4.2.2 Arm Cortex R5F Subsystem (R5FSS)

This section contains the integration details for the R5FSS module on this device which is also know as Pulsar and MCUSS. For Further information, see the *Dual-R5F MCU Subsystem* section of the Processors and Accelerators chapter.

4.2.2.1 R5FSS Unsupported Features

The following features are not supported on this family of devices:

- For WKUP_R5FSS0, CPU1 is not supported. This family of devices only supports a single core R5F implementaion

4.2.2.2 Module Allocations

Table 4-6. R5FSS Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
R5FSS0			✓
R5FSS1			✓
WKUP_R5FSS0	✓		

4.2.2.3 Resets, Interrupts, and Clocks

Table 4-7. R5FSS Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
R5FSS0_CORE0	MAIN_PSC0	R5SS_0	PSC_MAIN_R5SS0_CORE0	52	OFF	Yes	LPSC_MAIN_IP0
R5FSS0_CORE1	MAIN_PSC0	R5SS_0	PSC_MAIN_R5SS0_CORE1	53	OFF	Yes	LPSC_MAIN_IP0
R5FSS1_CORE0	MAIN_PSC0	R5SS_1	LPSC_MAIN_R5SS1_CORE0	55	OFF	Yes	LPSC_MAIN_IP0
R5FSS1_CORE1	MAIN_PSC0	R5SS_1	LPSC_MAIN_R5SS1_CORE1	56	OFF	Yes	LPSC_MAIN_IP0
WKUP_R5FSS0	MAIN_PSC0	GP_CORE	LPSC_MAIN_DM	1	ON	Yes	LPSC_MAIN_ALWAYSON

Table 4-8. R5FSS Resets

Module Instance	Source	Description
R5FSS0_CORE0	MAIN_PSC0	R5FSS0_CORE0 reset
R5FSS0_CORE1	MAIN_PSC0	R5FSS0_CORE1 reset
R5FSS1_CORE0	MAIN_PSC0	R5FSS1_CORE0 reset
R5FSS1_CORE1	MAIN_PSC0	R5FSS1_CORE1 reset
WKUP_R5FSS0	MAIN_PSC0	WKUP_R5FSS0 reset

Table 4-9. R5FSS Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
R5FSS0_CORE0	R5FSS0_CORE0_cti_0	R5FSS0_CORE0_intr_IN_175	R5FSS0_CORE0	R5FSS0_CORE0 interrupt request	level
R5FSS0_CORE0	R5FSS0_CORE0_cti_0	R5FSS0_CORE1_intr_IN_175	R5FSS0_CORE1	R5FSS0_CORE0 interrupt request	level

Table 4-9. R5FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
R5FSS0_CORE0	R5FSS0_CORE0_exp_intr_0	ESM0_esm_lvl_event_IN_210	ESM0	R5FSS0_CORE0 interrupt request	level
R5FSS0_CORE0	R5FSS0_CORE0_exp_intr_0	R5FSS0_CORE0_intr_IN_4	R5FSS0_CORE0	R5FSS0_CORE0 interrupt request	level
R5FSS0_CORE0	R5FSS0_CORE0_pmu_0	R5FSS0_CORE0_intr_IN_94	R5FSS0_CORE0	R5FSS0_CORE0 interrupt request	level
R5FSS0_CORE0	R5FSS0_CORE0_pmu_0	R5FSS0_CORE1_intr_IN_94	R5FSS0_CORE1	R5FSS0_CORE0 interrupt request	level
R5FSS0_CORE0	R5FSS0_CORE0_valfiq_0	R5FSS0_CORE0_intr_IN_95	R5FSS0_CORE0	R5FSS0_CORE0 interrupt request	level
R5FSS0_CORE0	R5FSS0_CORE0_valirq_0	R5FSS0_CORE0_intr_IN_96	R5FSS0_CORE0	R5FSS0_CORE0 interrupt request	level
R5FSS0_CORE1	R5FSS0_CORE1_cti_0	R5FSS0_CORE0_intr_IN_176	R5FSS0_CORE0	R5FSS0_CORE1 interrupt request	level
R5FSS0_CORE1	R5FSS0_CORE1_cti_0	R5FSS0_CORE1_intr_IN_176	R5FSS0_CORE1	R5FSS0_CORE1 interrupt request	level
R5FSS0_CORE1	R5FSS0_CORE1_exp_intr_0	ESM0_esm_lvl_event_IN_6	ESM0	R5FSS0_CORE1 interrupt request	level
R5FSS0_CORE1	R5FSS0_CORE1_exp_intr_0	R5FSS0_CORE1_intr_IN_4	R5FSS0_CORE1	R5FSS0_CORE1 interrupt request	level
R5FSS0_CORE1	R5FSS0_CORE1_pmu_0	R5FSS0_CORE0_intr_IN_93	R5FSS0_CORE0	R5FSS0_CORE1 interrupt request	level
R5FSS0_CORE1	R5FSS0_CORE1_pmu_0	R5FSS0_CORE1_intr_IN_93	R5FSS0_CORE1	R5FSS0_CORE1 interrupt request	level
R5FSS0_CORE1	R5FSS0_CORE1_valfiq_0	R5FSS0_CORE1_intr_IN_95	R5FSS0_CORE1	R5FSS0_CORE1 interrupt request	level
R5FSS0_CORE1	R5FSS0_CORE1_valirq_0	R5FSS0_CORE1_intr_IN_96	R5FSS0_CORE1	R5FSS0_CORE1 interrupt request	level
R5FSS1_CORE0	R5FSS1_CORE0_cti_0	R5FSS1_CORE1_intr_IN_175	R5FSS1_CORE1	R5FSS1_CORE0 interrupt request	level
R5FSS1_CORE0	R5FSS1_CORE0_exp_intr_0	ESM0_esm_lvl_event_IN_126	ESM0	R5FSS1_CORE0 interrupt request	level
R5FSS1_CORE0	R5FSS1_CORE0_exp_intr_0	R5FSS1_CORE0_intr_IN_4	R5FSS1_CORE0	R5FSS1_CORE0 interrupt request	level
R5FSS1_CORE0	R5FSS1_CORE0_pmu_0	R5FSS1_CORE0_intr_IN_94	R5FSS1_CORE0	R5FSS1_CORE0 interrupt request	level
R5FSS1_CORE0	R5FSS1_CORE0_pmu_0	R5FSS1_CORE1_intr_IN_94	R5FSS1_CORE1	R5FSS1_CORE0 interrupt request	level
R5FSS1_CORE0	R5FSS1_CORE0_valfiq_0	R5FSS1_CORE0_intr_IN_95	R5FSS1_CORE0	R5FSS1_CORE0 interrupt request	level
R5FSS1_CORE0	R5FSS1_CORE0_valirq_0	R5FSS1_CORE0_intr_IN_96	R5FSS1_CORE0	R5FSS1_CORE0 interrupt request	level
R5FSS1_CORE1	R5FSS1_CORE1_cti_0	R5FSS1_CORE0_intr_IN_176	R5FSS1_CORE0	R5FSS1_CORE1 interrupt request	level

Table 4-9. R5FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
R5FSS1_CORE1	R5FSS1_CORE1_cti_0	R5FSS1_CORE1_intr_IN_176	R5FSS1_CORE1	R5FSS1_CORE1 interrupt request	level
R5FSS1_CORE1	R5FSS1_CORE1_exp_intr_0	ESM0_esm_lvl_event_IN_127	ESM0	R5FSS1_CORE1 interrupt request	level
R5FSS1_CORE1	R5FSS1_CORE1_exp_intr_0	R5FSS1_CORE1_intr_IN_4	R5FSS1_CORE1	R5FSS1_CORE1 interrupt request	level
R5FSS1_CORE1	R5FSS1_CORE1_pmu_0	R5FSS1_CORE0_intr_IN_93	R5FSS1_CORE0	R5FSS1_CORE1 interrupt request	level
R5FSS1_CORE1	R5FSS1_CORE1_pmu_0	R5FSS1_CORE1_intr_IN_93	R5FSS1_CORE1	R5FSS1_CORE1 interrupt request	level
R5FSS1_CORE1	R5FSS1_CORE1_valfiq_0	R5FSS1_CORE1_intr_IN_95	R5FSS1_CORE1	R5FSS1_CORE1 interrupt request	level
R5FSS1_CORE1	R5FSS1_CORE1_valirq_0	R5FSS1_CORE1_intr_IN_96	R5FSS1_CORE1	R5FSS1_CORE1 interrupt request	level
WKUP_R5FSS0	WKUP_R5FSS0_CORE0_ecc_corrected_level_0	ESM0_esm_lvl_event_IN_30	ESM0	WKUP_R5FSS0 interrupt request	level
WKUP_R5FSS0	WKUP_R5FSS0_CORE0_ecc_uncorrected_level_0	ESM0_esm_lvl_event_IN_91	ESM0	WKUP_R5FSS0 interrupt request	level
WKUP_R5FSS0	WKUP_R5FSS0_CORE0_exp_intr_0	ESM0_esm_lvl_event_IN_124	ESM0	WKUP_R5FSS0 interrupt request	level
WKUP_R5FSS0	WKUP_R5FSS0_CORE0_exp_intr_0	WKUP_R5FSS0_CORE0_intr_IN_4	WKUP_R5FSS0_CORE0	WKUP_R5FSS interrupt request	level
WKUP_R5FSS0	WKUP_R5FSS0_CORE0_pmu_0	WKUP_R5FSS0_CORE0_intr_IN_58	WKUP_R5FSS0_CORE0	WKUP_R5FSS0 interrupt request	level
WKUP_R5FSS0	WKUP_R5FSS0_CORE0_valfiq_0	WKUP_R5FSS0_CORE0_intr_IN_59	WKUP_R5FSS0_CORE0	WKUP_R5FSS0 interrupt request	level
WKUP_R5FSS0	WKUP_R5FSS0_CORE0_valirq_0	WKUP_R5FSS0_CORE0_intr_IN_60	WKUP_R5FSS0_CORE0	WKUP_R5FSS0 interrupt request	level
WKUP_R5FSS0	WKUP_R5FSS0_CORE0_cti_0	WKUP_R5FSS0_CORE0_intr_IN_175	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0 interrupt request	level
R5FSS0_COMMON0	R5FSS0_COMMON0_bus_monitor_err_pulse_0	ESM0_esm_pls_event0_IN_229	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_bus_monitor_err_pulse_0	ESM0_esm_pls_event1_IN_229	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_bus_monitor_err_pulse_0	ESM0_esm_pls_event2_IN_229	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_commrx_level_0_0	R5FSS0_CORE0_intr_IN_5	R5FSS0_CORE0	R5FSS0_COMMON0 interrupt request	level
R5FSS0_COMMON0	R5FSS0_COMMON0_commrx_level_1_0	R5FSS0_CORE1_intr_IN_5	R5FSS0_CORE1	R5FSS0_COMMON0 interrupt request	level

Table 4-9. R5FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
R5FSS0_COMMON0	R5FSS0_COMMON0_commtx_level_0_0	R5FSS0_CORE0_intr_IN_6	R5FSS0_CORE0	R5FSS0_COMMON0 interrupt request	level
R5FSS0_COMMON0	R5FSS0_COMMON0_commtx_level_1_0	R5FSS0_CORE1_intr_IN_6	R5FSS0_CORE1	R5FSS0_COMMON0 interrupt request	level
R5FSS0_COMMON0	R5FSS0_COMMON0_compare_err_pulse_0	ESM0_esm_pls_event0_IN_231	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_compare_err_pulse_0	ESM0_esm_pls_event1_IN_231	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_compare_err_pulse_0	ESM0_esm_pls_event2_IN_231	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_ecc_de_to_esm_0_0	ESM0_esm_lvl_event_IN_211	ESM0	R5FSS0_COMMON0 interrupt request	level
R5FSS0_COMMON0	R5FSS0_COMMON0_ecc_de_to_esm_1_0	ESM0_esm_lvl_event_IN_221	ESM0	R5FSS0_COMMON0 interrupt request	level
R5FSS0_COMMON0	R5FSS0_COMMON0_ecc_se_to_esm_0_0	ESM0_esm_lvl_event_IN_212	ESM0	R5FSS0_COMMON0 interrupt request	level
R5FSS0_COMMON0	R5FSS0_COMMON0_ecc_se_to_esm_1_0	ESM0_esm_lvl_event_IN_222	ESM0	R5FSS0_COMMON0 interrupt request	level
R5FSS0_COMMON0	R5FSS0_COMMON0_selftest_err_pulse_0	ESM0_esm_pls_event0_IN_232	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_selftest_err_pulse_0	ESM0_esm_pls_event1_IN_232	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_selftest_err_pulse_0	ESM0_esm_pls_event2_IN_232	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_vim_compare_err_pulse_0	ESM0_esm_pls_event0_IN_233	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_vim_compare_err_pulse_0	ESM0_esm_pls_event1_IN_233	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS0_COMMON0	R5FSS0_COMMON0_vim_compare_err_pulse_0	ESM0_esm_pls_event2_IN_233	ESM0	R5FSS0_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_bus_monitor_err_pulse_0	ESM0_esm_pls_event0_IN_235	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_bus_monitor_err_pulse_0	ESM0_esm_pls_event1_IN_235	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_bus_monitor_err_pulse_0	ESM0_esm_pls_event2_IN_235	ESM0	R5FSS1_COMMON0 interrupt request	pulse

Table 4-9. R5FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
R5FSS1_COMMON0	R5FSS1_COMMON0_commrx_level_0_0	R5FSS1_CORE0_intr_IN_5	R5FSS1_CORE0	R5FSS1_COMMON0 interrupt request	level
R5FSS1_COMMON0	R5FSS1_COMMON0_commrx_level_1_0	R5FSS1_CORE1_intr_IN_5	R5FSS1_CORE1	R5FSS1_COMMON0 interrupt request	level
R5FSS1_COMMON0	R5FSS1_COMMON0_commtx_level_0_0	R5FSS1_CORE0_intr_IN_6	R5FSS1_CORE0	R5FSS1_COMMON0 interrupt request	level
R5FSS1_COMMON0	R5FSS1_COMMON0_commtx_level_1_0	R5FSS1_CORE1_intr_IN_6	R5FSS1_CORE1	R5FSS1_COMMON0 interrupt request	level
R5FSS1_COMMON0	R5FSS1_COMMON0_compare_err_pulse_0	ESM0_esm_pls_event0_IN_237	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_compare_err_pulse_0	ESM0_esm_pls_event1_IN_237	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_compare_err_pulse_0	ESM0_esm_pls_event2_IN_237	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_ecc_de_to_esm_0_0	ESM0_esm_lvl_event_IN_46	ESM0	R5FSS1_COMMON0 interrupt request	level
R5FSS1_COMMON0	R5FSS1_COMMON0_ecc_de_to_esm_1_0	ESM0_esm_lvl_event_IN_47	ESM0	R5FSS1_COMMON0 interrupt request	level
R5FSS1_COMMON0	R5FSS1_COMMON0_ecc_se_to_esm_0_0	ESM0_esm_lvl_event_IN_48	ESM0	R5FSS1_COMMON0 interrupt request	level
R5FSS1_COMMON0	R5FSS1_COMMON0_ecc_se_to_esm_1_0	ESM0_esm_lvl_event_IN_49	ESM0	R5FSS1_COMMON0 interrupt request	level
R5FSS1_COMMON0	R5FSS1_COMMON0_selftest_err_pulse_0	ESM0_esm_pls_event0_IN_238	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_selftest_err_pulse_0	ESM0_esm_pls_event1_IN_238	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_selftest_err_pulse_0	ESM0_esm_pls_event2_IN_238	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_vim_compare_err_pulse_0	ESM0_esm_pls_event0_IN_239	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_vim_compare_err_pulse_0	ESM0_esm_pls_event1_IN_239	ESM0	R5FSS1_COMMON0 interrupt request	pulse
R5FSS1_COMMON0	R5FSS1_COMMON0_vim_compare_err_pulse_0	ESM0_esm_pls_event2_IN_239	ESM0	R5FSS1_COMMON0 interrupt request	pulse
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_commrx_level_0_0	WKUP_R5FSS0_CORE0_intr_IN_5	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_COMMON0 interrupt request	level

Table 4-9. R5FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_commtx_level_0_0	WKUP_R5FSS0_CORE0_intr_IN_6	WKUP_R5FSS0_CORE0	WKUP_R5FSS0_COMMON0 interrupt request	level
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_ecc_de_to_esm_0_0	ESM0_esm_lvl_event_IN_40	ESM0	WKUP_R5FSS0_COMMON0 interrupt request	level
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_ecc_se_to_esm_0_0	ESM0_esm_lvl_event_IN_41	ESM0	WKUP_R5FSS0_COMMON0 interrupt request	level

Table 4-10. R5FSS Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
R5FSS0_CORE0	FCLK	MAIN_R5SS_CLK	R5SS0_CLKSEL[0:0]	R5FSS0_CORE0 Functional Clock
		MAIN_R5SS_CLK/2		
	ICLK	MAIN_R5SS_CLK	R5SS0_CLKSEL[0:0]	R5FSS0_CORE0 Interface Clock
		MAIN_R5SS_CLK/2		
R5FSS0_CORE1	FCLK	MAIN_R5SS_CLK	R5SS0_CLKSEL[0:0]	R5FSS0_CORE1 Functional Clock
		MAIN_R5SS_CLK/2		
	ICLK	MAIN_R5SS_CLK	R5SS0_CLKSEL[0:0]	R5FSS0_CORE1 Interface Clock
		MAIN_R5SS_CLK/2		
R5FSS1_CORE0	FCLK	MAIN_R5SS_CLK	R5SS0_CLKSEL[0:0]	R5FSS1_CORE0 Functional Clock
		MAIN_R5SS_CLK/2		
	ICLK	MAIN_R5SS_CLK	R5SS0_CLKSEL[0:0]	R5FSS1_CORE0 Interface Clock
		MAIN_R5SS_CLK/2		
R5FSS1_CORE1	FCLK	MAIN_R5SS_CLK	R5SS0_CLKSEL[0:0]	R5FSS1_CORE1 Functional Clock
		MAIN_R5SS_CLK/2		
	ICLK	MAIN_R5SS_CLK	R5SS0_CLKSEL[0:0]	R5FSS1_CORE1 Interface Clock
		MAIN_R5SS_CLK/2		
WKUP_R5FSS0	FCLK	MAIN_PLL15_HSDIV2_CLKOUT	WKUP_CLKSEL[0:0]	WKUP_R5FSS0 Functional Clock
		MCU_PLL0_HSDIV0_CLKOUT		
	ICLK	MAIN_PLL15_HSDIV2_CLKOUT	WKUP_CLKSEL[0:0]	WKUP_R5FSS0 Interface Clock
		MCU_PLL0_HSDIV0_CLKOUT		

4.3 Device Configuration

4.3.1 Control Module (CTRL_MMR)

This section contains the integration details for the CTRL_MMR module on this device. For further information, see the *Memory Mapped Control Register Modules (CTRL_MMR)* section of the *Device Configuration* chapter.

4.3.1.1 Module Allocations

Table 4-11. CTRL_MMR Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
MAIN_CTRL_MMR0			✓
MCU_CTRL_MMR0		✓	
WKUP_CTRL_MMR0	✓		

4.3.1.2 Resets, Interrupts, and Clocks

Table 4-12. Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MAIN_CTRL_MMR0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
MCU_CTRL_MMR0	WKUP_PSC0	GP_CORE_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	NONE
WKUP_CTRL_MMR0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE

Table 4-13. Resets

Module Instance	Source	Description
MAIN_CTRL_MMR0	MAIN_PSC0	MAIN_CTRL_MMR0 reset
	PLLCTRL0	
MCU_CTRL_MMR0	WKUP_PSC0	MCU_CTRL_MMR0 reset
	MCU_PLLCTRL0	
WKUP_CTRL_MMR0	MAIN_PSC0	WKUP_CTRL_MMR0 reset
	PLLCTRL0	

Table 4-14. Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_CTRL_MMR0	MAIN_CTRL_MMR0_IPC_SET0_ipc_set_ipcfg_0	C7X256V0_CLEC_soc_events_in_IN_5	C7X256V0_CLEC	MAIN_CTRL_MMR0 interrupt request	level
	MAIN_CTRL_MMR0_IPC_SET16_ipc_set_ipcfg_0	R5FSS0_CORE0_intr_IN_0	R5FSS0_CORE0	MAIN_CTRL_MMR0 interrupt request	level
	MAIN_CTRL_MMR0_IPC_SET17_ipc_set_ipcfg_0	R5FSS0_CORE1_intr_IN_0	R5FSS0_CORE1	MAIN_CTRL_MMR0 interrupt request	level
	MAIN_CTRL_MMR0_IPC_SET18_ipc_set_ipcfg_0	R5FSS1_CORE0_intr_IN_0	R5FSS1_CORE0	MAIN_CTRL_MMR0 interrupt request	level
	MAIN_CTRL_MMR0_IPC_SET19_ipc_set_ipcfg_0	R5FSS1_CORE1_intr_IN_0	R5FSS1_CORE1	MAIN_CTRL_MMR0 interrupt request	level
	MAIN_CTRL_MMR0_IPC_SET1_ipc_set_ipcfg_0	C7X256V1_CLEC_soc_events_in_IN_5	C7X256V1_CLEC	MAIN_CTRL_MMR0 interrupt request	level
	MAIN_CTRL_MMR0_access_err_0	C7X256V0_CLEC_gic_spi_IN_129	C7X256V0_CLEC	MAIN_CTRL_MMR0 interrupt request	level
		C7X256V1_CLEC_gic_spi_IN_129	C7X256V1_CLEC	MAIN_CTRL_MMR0 interrupt request	level
		R5FSS0_CORE0_intr_IN_128	R5FSS0_CORE0	MAIN_CTRL_MMR0 interrupt request	level
		R5FSS0_CORE1_intr_IN_128	R5FSS0_CORE1	MAIN_CTRL_MMR0 interrupt request	level
		R5FSS1_CORE0_intr_IN_128	R5FSS1_CORE0	MAIN_CTRL_MMR0 interrupt request	level
		R5FSS1_CORE1_intr_IN_128	R5FSS1_CORE1	MAIN_CTRL_MMR0 interrupt request	level
		WKUP_R5FSS0_CORE0_intr_IN_128	WKUP_R5FSS0_CORE0	MAIN_CTRL_MMR0 interrupt request	level

Table 4-14. Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_CTRL_MMR0	MCU_CTRL_MMR0_IPC_SET0_ipc_set_ipcfg_0	WKUP_R5FSS0_CORE0_intr_IN_0	WKUP_R5FSS0_CORE0	MCU_CTRL_MMR0 interrupt request	level
	MCU_CTRL_MMR0_access_err_0	C7X256V0_CLEC_gic_spi_IN_129	C7X256V0_CLEC	MCU_CTRL_MMR0 interrupt request	level
		C7X256V1_CLEC_gic_spi_IN_129	C7X256V1_CLEC	MCU_CTRL_MMR0 interrupt request	level
		R5FSS0_CORE0_intr_IN_128	R5FSS0_CORE0	MCU_CTRL_MMR0 interrupt request	level
		R5FSS0_CORE1_intr_IN_128	R5FSS0_CORE1	MCU_CTRL_MMR0 interrupt request	level
		R5FSS1_CORE0_intr_IN_128	R5FSS1_CORE0	MCU_CTRL_MMR0 interrupt request	level
		R5FSS1_CORE1_intr_IN_128	R5FSS1_CORE1	MCU_CTRL_MMR0 interrupt request	level
		WKUP_R5FSS0_CORE0_intr_IN_128	WKUP_R5FSS0_CORE0	MCU_CTRL_MMR0 interrupt request	level
WKUP_CTRL_MMR0	WKUP_CTRL_MMR0_access_err_0	C7X256V0_CLEC_gic_spi_IN_129	C7X256V0_CLEC	WKUP_CTRL_MMR0 interrupt request	level
		C7X256V1_CLEC_gic_spi_IN_129	C7X256V1_CLEC	WKUP_CTRL_MMR0 interrupt request	level
		R5FSS0_CORE0_intr_IN_128	R5FSS0_CORE0	WKUP_CTRL_MMR0 interrupt request	level
		R5FSS0_CORE1_intr_IN_128	R5FSS0_CORE1	WKUP_CTRL_MMR0 interrupt request	level
		R5FSS1_CORE0_intr_IN_128	R5FSS1_CORE0	WKUP_CTRL_MMR0 interrupt request	level
		R5FSS1_CORE1_intr_IN_128	R5FSS1_CORE1	WKUP_CTRL_MMR0 interrupt request	level
		WKUP_R5FSS0_CORE0_intr_IN_128	WKUP_R5FSS0_CORE0	WKUP_CTRL_MMR0 interrupt request	level

Table 4-15. Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MAIN_CTRL_MMR0	FICLK	MAIN_SYSCLK0/4		MAIN_CTRL_MMR0 Functional and Interface Clock
WKUP_CTRL_MMR1	FICLK	MCU_SYSCLK0/4		MCU_CTRL_MMR0 Functional and Interface Clock
	P1500_WRCK	MCU_DFT_SCAN_CLK		
WKUP_CTRL_MMR0	FICLK	DM_CLK/4	WKUP_CLKSEL[0:0]	WKUP_CTRL_MMR0 Functional and Interface Clock

4.3.2 Voltage and Thermal Manager (VTM)

This section contains the integration details for the VTM module on this device. For further information, see the *Voltage and Thermal Manager (VTM)* in *Power* section of the *Device Configuration* chapter.

4.3.2.1 Voltage and Thermal Manager Locations

There is 1 Voltage and Thermal Monitor (VTM) located on AM275: WKUP_VTM0. For more details on VTM, see *Voltage and Thermal Manager (VTM)* section.

4.3.3 Power Glitch Detect (PGD)/Power OK (POK)

This section contains the integration details for the PGD/POK module on this device. For further information, see the *Power Glitch Detect (PGD)* section of the *Device Configuration* chapter.

4.3.3.1 Resets, Interrupts, and Clocks

Table 4-16. PGD Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 4-17. PGD Resets

Module Instance	Source	Description
N/A	N/A	N/A

Table 4-18. PGD Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_ov_out_n_to_esm_0	WKUP_ESM0_esm_pls_event0_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_ov_out_n_to_esm_1	WKUP_ESM0_esm_pls_event0_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level

Table 4-18. PGD Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_ov_out_n_to_esm_2	WKUP_ESM0_esm_pls_event0_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_ov_out_n_to_esm_3	WKUP_ESM0_esm_pls_event0_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_ov_out_n_to_esm_4	WKUP_ESM0_esm_pls_event0_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[70:64]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_uv_out_n_to_esm_0	WKUP_ESM0_esm_pls_event0_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event0_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level

Table 4-18. PGD Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_uv_out_n_to_esm_1	WKUP_ESM0_esm_pls_event0_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event0_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_uv_out_n_to_esm_2	WKUP_ESM0_esm_pls_event0_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event0_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level

Table 4-18. PGD Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_uv_out_n_to_esm_3	WKUP_ESM0_esm_pls_event0_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event0_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0	MCU_PRG_MCU_5POKS0_pok_pgood_uv_out_n_to_esm_4	WKUP_ESM0_esm_pls_event0_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event0_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event1_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[73:71]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level
POKS0		WKUP_ESM0_esm_pls_event2_IN_[77:76]	WKUP_ESM0	MCU_PRG_MCU_5POKS0 interrupt request	level

Table 4-19. PGD Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCU_PRG_MCU_5POKS0	CLK	CLK_12_RC	N/A	N/A

4.4 Interprocessor Communication

4.4.1 Mailbox

This section contains the integration details for the Mailbox module on this device. For further information, see the *Mailbox* section of the *Interprocessor Communication* chapter.

4.4.1.1 Mailbox Unsupported Features

The following features are not supported on this family of devices:

- 'User' protection of mailbox in hardware. If required, must be implemented by software.

4.4.1.2 Resets, Interrupts, and Clocks

Table 4-20. Mailbox Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MAILBOX0_MAILBOX_CLUSTER_0	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON
MAILBOX0_MAILBOX_CLUSTER_1	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON
MAILBOX0_MAILBOX_CLUSTER_2	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON
MAILBOX0_MAILBOX_CLUSTER_3	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON
MAILBOX0_MAILBOX_CLUSTER_4	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON
MAILBOX0_MAILBOX_CLUSTER_5	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON
MAILBOX0_MAILBOX_CLUSTER_6	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON
MAILBOX0_MAILBOX_CLUSTER_7	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON

Table 4-21. Mailbox Resets

Module Instance	Source	Description
MAILBOX0_MAILBOX_CLUSTER_0	MAIN_PSC0	MAILBOX0_MAILBOX_CLUSTER_0 reset
MAILBOX0_MAILBOX_CLUSTER_1	MAIN_PSC0	MAILBOX0_MAILBOX_CLUSTER_1 reset
MAILBOX0_MAILBOX_CLUSTER_2	MAIN_PSC0	MAILBOX0_MAILBOX_CLUSTER_2 reset
MAILBOX0_MAILBOX_CLUSTER_3	MAIN_PSC0	MAILBOX0_MAILBOX_CLUSTER_3 reset
MAILBOX0_MAILBOX_CLUSTER_4	MAIN_PSC0	MAILBOX0_MAILBOX_CLUSTER_4 reset
MAILBOX0_MAILBOX_CLUSTER_5	MAIN_PSC0	MAILBOX0_MAILBOX_CLUSTER_5 reset
MAILBOX0_MAILBOX_CLUSTER_6	MAIN_PSC0	MAILBOX0_MAILBOX_CLUSTER_6 reset

Table 4-21. Mailbox Resets (continued)

Module Instance	Source	Description
MAILBOX0_MAILBOX_CLUSTER_7	MAIN_PSC0	MAILBOX0_MAILBOX_CLUSTER_7 reset

Table 4-22. Mailbox Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster_pend_[3:0]	R5FSS0_CORE0_intr_IN_240	R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster_pend_[3:0]	R5FSS0_CORE1_intr_IN_240	R5FSS0_CORE1	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster_pend_[3:0]	R5FSS1_CORE0_intr_IN_240	R5FSS1_CORE0	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_mailbox_cluster_pend_[3:0]	R5FSS1_CORE1_intr_IN_240	R5FSS1_CORE1	MAILBOX0_MAILBOX_CLUSTER_0 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_1	MAILBOX0_MAILBOX_CLUSTER_1_mailbox_cluster_pend_[3:0]	C7X256V0_CLEC_soc_events_in_IN_6	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_1 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_1	MAILBOX0_MAILBOX_CLUSTER_1_mailbox_cluster_pend_[3:0]	C7X256V1_CLEC_soc_events_in_IN_6	C7X256V1_CLEC	MAILBOX0_MAILBOX_CLUSTER_1 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_1	MAILBOX0_MAILBOX_CLUSTER_1_mailbox_cluster_pend_[3:0]	R5FSS0_CORE0_intr_IN_241	R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_1 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_1	MAILBOX0_MAILBOX_CLUSTER_1_mailbox_cluster_pend_[3:0]	R5FSS1_CORE0_intr_IN_241	R5FSS1_CORE0	MAILBOX0_MAILBOX_CLUSTER_1 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_2	MAILBOX0_MAILBOX_CLUSTER_2_mailbox_cluster_pend_[3:0]	C7X256V0_CLEC_soc_events_in_IN_7	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_2 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_2	MAILBOX0_MAILBOX_CLUSTER_2_mailbox_cluster_pend_[3:0]	C7X256V1_CLEC_soc_events_in_IN_7	C7X256V1_CLEC	MAILBOX0_MAILBOX_CLUSTER_2 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_2	MAILBOX0_MAILBOX_CLUSTER_2_mailbox_cluster_pend_[3:0]	R5FSS0_CORE1_intr_IN_241	R5FSS0_CORE1	MAILBOX0_MAILBOX_CLUSTER_2 interrupt request	level

Table 4-22. Mailbox Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAILBOX0_MAILBOX_CLUSTER_2	MAILBOX0_MAILBOX_CLUSTER_2_mailbox_cluster_pend_[3:0]	R5FSS1_CORE1_intr_IN_241	R5FSS1_CORE1	MAILBOX0_MAILBOX_CLUSTER_2 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_3	MAILBOX0_MAILBOX_CLUSTER_3_mailbox_cluster_pend_[3:0]	C7X256V0_CLEC_soc_events_in_IN_8	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_3 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_3	MAILBOX0_MAILBOX_CLUSTER_3_mailbox_cluster_pend_[3:0]	C7X256V1_CLEC_soc_events_in_IN_8	C7X256V1_CLEC	MAILBOX0_MAILBOX_CLUSTER_3 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_3	MAILBOX0_MAILBOX_CLUSTER_3_mailbox_cluster_pend_[3:0]	R5FSS0_CORE0_intr_IN_242	R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_3 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_3	MAILBOX0_MAILBOX_CLUSTER_3_mailbox_cluster_pend_[3:0]	R5FSS0_CORE1_intr_IN_242	R5FSS1_CORE0	MAILBOX0_MAILBOX_CLUSTER_3 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_4	MAILBOX0_MAILBOX_CLUSTER_4_mailbox_cluster_pend_[3:0]	C7X256V0_CLEC_soc_events_in_IN_9	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_4 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_4	MAILBOX0_MAILBOX_CLUSTER_4_mailbox_cluster_pend_[3:0]	C7X256V1_CLEC_soc_events_in_IN_9	C7X256V1_CLEC	MAILBOX0_MAILBOX_CLUSTER_4 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_4	MAILBOX0_MAILBOX_CLUSTER_4_mailbox_cluster_pend_[3:0]	R5FSS1_CORE0_intr_IN_242	R5FSS1_CORE0	MAILBOX0_MAILBOX_CLUSTER_4 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_4	MAILBOX0_MAILBOX_CLUSTER_4_mailbox_cluster_pend_[3:0]	R5FSS1_CORE1_intr_IN_242	R5FSS1_CORE1	MAILBOX0_MAILBOX_CLUSTER_4 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_5	MAILBOX0_MAILBOX_CLUSTER_5_mailbox_cluster_pend_[3:0]	R5FSS0_CORE0_intr_IN_243	R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_5 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_5	MAILBOX0_MAILBOX_CLUSTER_5_mailbox_cluster_pend_[3:0]	R5FSS1_CORE1_intr_IN_243	R5FSS1_CORE1	MAILBOX0_MAILBOX_CLUSTER_5 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_5	MAILBOX0_MAILBOX_CLUSTER_5_mailbox_cluster_pend_[3:0]	WKUP_R5FSS0_CORE0_intr_IN_240	WKUP_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_5 interrupt request	level

Table 4-22. Mailbox Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAILBOX0_MAILBOX_CLUSTER_6	MAILBOX0_MAILBOX_CLUSTER_6_mailbox_cluster_pend_[3:0]	R5FSS0_CORE1_intr_IN_243	R5FSS0_CORE1	MAILBOX0_MAILBOX_CLUSTER_6 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_6	MAILBOX0_MAILBOX_CLUSTER_6_mailbox_cluster_pend_[3:0]	R5FSS1_CORE0_intr_IN_243	R5FSS1_CORE0	MAILBOX0_MAILBOX_CLUSTER_6 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_6	MAILBOX0_MAILBOX_CLUSTER_6_mailbox_cluster_pend_[3:0]	WKUP_R5FSS0_CORE0_intr_IN_241	WKUP_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_6 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_7	MAILBOX0_MAILBOX_CLUSTER_7_mailbox_cluster_pend_[3:0]	C7X256V0_CLEC_soc_events_in_IN_10	C7X256V0_CLEC	MAILBOX0_MAILBOX_CLUSTER_7 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_7	MAILBOX0_MAILBOX_CLUSTER_7_mailbox_cluster_pend_[3:0]	C7X256V1_CLEC_soc_events_in_IN_10	C7X256V1_CLEC	MAILBOX0_MAILBOX_CLUSTER_7 interrupt request	level
MAILBOX0_MAILBOX_CLUSTER_7	MAILBOX0_MAILBOX_CLUSTER_7_mailbox_cluster_pend_[3:0]	WKUP_R5FSS0_CORE0_intr_IN_242	WKUP_R5FSS0_CORE0	MAILBOX0_MAILBOX_CLUSTER_7 interrupt request	level

Table 4-23. Mailbox Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MAILBOX0_MAILBOX_CLUSTER_0	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2	N/A	N/A
MAILBOX0_MAILBOX_CLUSTER_1	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2	N/A	N/A
MAILBOX0_MAILBOX_CLUSTER_2	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2	N/A	N/A
MAILBOX0_MAILBOX_CLUSTER_3	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2	N/A	N/A
MAILBOX0_MAILBOX_CLUSTER_4	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2	N/A	N/A
MAILBOX0_MAILBOX_CLUSTER_5	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2	N/A	N/A
MAILBOX0_MAILBOX_CLUSTER_6	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2	N/A	N/A
MAILBOX0_MAILBOX_CLUSTER_7	VCLK_CLK	MAIN_PLL15_HSDIV0_CLKOUT/2	N/A	N/A

4.4.2 Spinlock

This section contains the integration details for the Spinlock module on this device. For further information, see the *Spinlock* section of the *Interprocessor Communication* chapter.

4.4.2.1 SPINLOCK Unsupported Features

The following features are not supported on this family of devices:

- ARM architectural Spinlock instructions (LDREX,STREX)
- Any use model other than binary mutex (for example, counting semaphore, lockless programming): Spinlock MMR is a single binary 0,1 implemented by a state machine.
- 64-bit accesses: Spinlock MMRs are aligned on 32-bit boundaries meaning a 64-bit access affects the state of 2 Spinlocks.

4.4.2.2 Module Allocations

Table 4-24. Spinlock Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
SPINLOCK0			✓

4.4.2.3 Resets, Interrupts, and Clocks

Table 4-25. Spinlock Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
SPINLOCK0	MAIN_PSC0	GP_CORE	LPSC_SMS_COM	14	ON	YES	LPSC_MAIN_ALWAYSON

Table 4-26. Spinlock Resets

Module Instance	Source	Description
SPINLOCK0	MAIN_PSC0	SPINLOCK0 reset

Table 4-27. Spinlock Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
N/A	N/A	N/A	N/A	N/A	N/A

Table 4-28. Spinlock Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
SPINLOCK0	VBUS_FCLK	MAIN_PLL15_HSDIV0_CLKOUT/2		SPINLOCK0 clock. This clock is used for all interface and functional operations

4.5 Interrupts

4.5.1 GPIOMUX_INTROUTER

This section contains the integration details for the GPIOMUX_INTROUTER modules on this device. For Further information, see the GPIOMUX_INTROUTER section of the Interrupts chapter

4.5.1.1 Module Allocation

Table 4-29. GPIOMUX_INTROUTER Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
MAIN_GPIOMUX_INTROUTER0			✓
MCU_MCU_GPIOMUX_INTROUTER0		✓	

4.5.1.2 Resets, Interrupts, and Clocks

Table 4-30. GPIOMUX_INTROUTER Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MAIN_GPIOMUX_INTROUTER0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
MCU_MCU_GPIOMUX_INTROUTER0	WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	NONE

Table 4-31. GPIOMUX_INTROUTER Resets

Module Instance	Source	Description
MAIN_GPIOMUX_INTROUTER0	MAIN_PSC0	MAIN_GPIOMUX_INTROUTER0 reset
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_PSC0	MCU_MCU_GPIOMUX_INTROUTER0 reset

Table 4-32. GPIOMUX_INTROUTER Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_32	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_33	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_34	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_35	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_36	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_37	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_38	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_39	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_40	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_41	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_42	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_43	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_44	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_45	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_46	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V0_CLEC_gic_spi_IN_47	C7X256V0_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_32	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_33	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_34	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_35	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_36	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_37	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_38	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_39	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_40	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_41	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_42	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_43	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_44	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_45	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_46	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	C7X256V1_CLEC_gic_spi_IN_47	C7X256V1_CLEC	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_16	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_17	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_18	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_19	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_20	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_21	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_22	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_23	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_24	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_25	DMASS0_INTAGGR_0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_32	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_33	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_34	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_35	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_36	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_37	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_38	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_39	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_40	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_41	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_42	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_43	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_44	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_45	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_46	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE0_intr_IN_47	R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_32	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_33	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_34	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_35	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_36	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_37	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_38	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_39	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_40	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_41	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_42	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_43	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_44	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_45	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_46	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS0_CORE1_intr_IN_47	R5FSS0_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_32	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_33	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_34	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_35	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_36	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_37	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_38	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_39	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_40	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_41	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_42	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_43	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_44	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_45	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_46	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE0_intr_IN_47	R5FSS1_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_32	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_33	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_34	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_35	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_36	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_37	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_38	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_39	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_40	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_41	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_42	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_43	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_44	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_45	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_46	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	R5FSS1_CORE1_intr_IN_47	R5FSS1_CORE1	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_32	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_33	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_34	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_35	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_36	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_37	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_38	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_39	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_40	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_41	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_42	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_43	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_44	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_45	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_46	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MAIN_GPIO_INTROUTER0	MAIN_GPIO_INTROUTER0_outp_[79:0]	WKUP_R5FSS0_CORE0_intr_IN_47	WKUP_R5FSS0_CORE0	MAIN_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	C7X256V0_CLEC_gic_spi_IN_104	C7X256V0_CLEC	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	C7X256V0_CLEC_gic_spi_IN_105	C7X256V0_CLEC	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	C7X256V0_CLEC_gic_spi_IN_106	C7X256V0_CLEC	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	C7X256V0_CLEC_gic_spi_IN_107	C7X256V0_CLEC	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	C7X256V1_CLEC_gic_spi_IN_104	C7X256V1_CLEC	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	C7X256V1_CLEC_gic_spi_IN_105	C7X256V1_CLEC	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	C7X256V1_CLEC_gic_spi_IN_106	C7X256V1_CLEC	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	C7X256V1_CLEC_gic_spi_IN_107	C7X256V1_CLEC	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event0_IN_88	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event0_IN_89	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event0_IN_90	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event0_IN_91	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event1_IN_88	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event1_IN_89	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event1_IN_90	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event1_IN_91	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event2_IN_88	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event2_IN_89	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event2_IN_90	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_ESM0_esm_pls_event2_IN_91	WKUP_ESM0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE0_intr_IN_100	R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE0_intr_IN_101	R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE0_intr_IN_102	R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE0_intr_IN_103	R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE0_intr_IN_104	R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE0_intr_IN_105	R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE0_intr_IN_106	R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE0_intr_IN_107	R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE1_intr_IN_100	R5FSS0_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE1_intr_IN_101	R5FSS0_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE1_intr_IN_102	R5FSS0_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE1_intr_IN_103	R5FSS0_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE1_intr_IN_104	R5FSS0_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE1_intr_IN_105	R5FSS0_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE1_intr_IN_106	R5FSS0_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS0_CORE1_intr_IN_107	R5FSS0_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE0_intr_IN_100	R5FSS1_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE0_intr_IN_101	R5FSS1_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE0_intr_IN_102	R5FSS1_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE0_intr_IN_103	R5FSS1_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE0_intr_IN_104	R5FSS1_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE0_intr_IN_105	R5FSS1_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE0_intr_IN_106	R5FSS1_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE0_intr_IN_107	R5FSS1_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE1_intr_IN_100	R5FSS1_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE1_intr_IN_101	R5FSS1_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE1_intr_IN_102	R5FSS1_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE1_intr_IN_103	R5FSS1_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE1_intr_IN_104	R5FSS1_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE1_intr_IN_105	R5FSS1_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse

Table 4-32. GPIOMUX_INTROUTER Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE1_intr_IN_106	R5FSS1_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	R5FSS1_CORE1_intr_IN_107	R5FSS1_CORE1	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_R5FSS0_CORE0_intr_IN_50	WKUP_R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_R5FSS0_CORE0_intr_IN_51	WKUP_R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_R5FSS0_CORE0_intr_IN_52	WKUP_R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_R5FSS0_CORE0_intr_IN_53	WKUP_R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_R5FSS0_CORE0_intr_IN_104	WKUP_R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_R5FSS0_CORE0_intr_IN_105	WKUP_R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_R5FSS0_CORE0_intr_IN_106	WKUP_R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse
MCU_MCU_GPIO_INTROUTER0	MCU_MCU_GPIO_INTROUTER0_outp_[31:0]	WKUP_R5FSS0_CORE0_intr_IN_107	WKUP_R5FSS0_CORE0	MCU_MCU_GPIO_INTROUTER0 interrupt request	pulse

Table 4-33. GPIOMUX_INTROUTER Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MAIN_GPIOMUX_INTROUTER0	FICLK	MAIN_SYSCLK0/4		
MCU_MCU_GPIOMUX_INTROUTER0	INTR_CLK	MCU_SYSCLK0/4		

4.6 Data Movement Architecture

4.6.1 Data Movement Subsystem (DMSS)

This section contains the integration details for the DMSS module on this device. For Further information, see the Data Movement Subsystem (DMSS) section of the Data Movement Architecture chapter

4.6.1.1 DMSS Unsupported Features

The following features are not supported on this family of devices:

- No unsupported features

4.6.1.2 Module Allocations

Table 4-34. DMSS Module Allocations within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
DMSS0	-	-	✓

4.6.1.3 Global Event Map

The global event map for all DMSS events is shown in *Global Event Map*.

Table 4-35. Global Event Map

Destination		Offset	PSIL Routed Slots	Actual Slots
DMSS Instance or External	Port			
DMSS	DMSS INTAGGR SEVI	0 (0k)	8192 (8k)	1536
DMSS	DMSS INTAGGR MEVI	8192 (8k)	2048 (2k)	128
DMSS	DMSS INTAGGR GEVI	10240 (10k)	2048 (2k)	256
External	DMSC IA SEVI	18432 (18k)	2048 (2k)	-
DMSS	DMSS INTAGGR LEVI	32768 (32k)	32 (0.03k)	32
External	PDMA_MAIN0 LEVI	41984 (41.000k)	128	-
External	PDMA_MAIN1 LEVI	42112 (41.125k)	128	-
DMSS	DMSS BCDMA Triggers	50176 (49k)	1024 (1k)	244
External	DRU0	62976 (61.5k)	64	-
External	DRU1	63232	64	-

4.6.1.4 PSI-L System Thread Map

Table 4-36. DMSS PSILSS Thread Map

Thread Number	NAV Instance	Endpoint
0x0000	DMSS	PSILCFG CFGSTRM
0x0020	DMSS	PKTDMA CFGSTRM
0x0021	DMSS	BCDMA CFGSTRM
0x1000-0x1FFF	DMSS	PKTDMA Threads
0x2000-0x2FFF	DMSS	BCDMA Threads
0x3000-0x3FFF	DMSS	Reserved
0x4000-0x40FF	DMSS	PDMA_ADC
0x4100-0x417F	DMSS	PDMA_ASRC0
0x4180-0x41FF	DMSS	PDMA_ASRC1
0x4300-0x43F	DMSS	PDMA_MAIN0
0x4400-0x447F	DMSS	PDMA_MAIN1
0x4480-0x44FF	DMSS	PDMA_MAIN2
0x4500-0x457F	DMSS	PDMA_MCASP0
0x4580-0x45FF	DMSS	PDMA_MCASP1
0x4600-0x46FF	DMSS	CPSW2

Table 4-36. DMSS PSILSS Thread Map (continued)

Thread Number	NAV Instance	Endpoint
0x4700-0x74FF	DMSS	Reserved
0x7500-0x7506	DMSS	SAUL0

4.6.2 Block Copy DMA (BCDMA)

4.6.2.1 Block Copy DMA (BCDMA)

Table 4-37. BCDMA Allocation within Device Domains

	Domain		
	WKUP	Top Level	MAIN
DMSS_BCDMA	-	-	✓ (DMSS)

Table 4-38. BCDMA Configuration Parameters

Module Instance	Parameters		
	chan_cnt	tchan_cnt	rchan_cnt
DMSS_BCDMA	32	22	22

4.6.3 Peripheral DMA (PDMA)

This section contains the integration details for the PDMA module on this device. For Further information, see the Peripheral DMA (PDMA) section of the Data Movement Architecture chapter

4.6.3.1 PDMA Unsupported Features

The following features are not supported on this family of devices:

- Dynamic Transfer Requests
- Cross-Channel Triggering

4.6.3.2 Module Allocations

Table 4-39. PDMA Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
PDMA0			✓
PDMA1			✓
PDMA2			✓
PDMA3			✓
PDMA4			✓
PDMA5			✓
PDMA6			✓
PDMA7			✓

4.6.4 Packet DMA (PKTDMA)

4.6.4.1 Packet DMA (PKTDMA)

Table 4-40. PKTDMA Allocation Within Device Domains

Module Instance	Domain		
	WKUP	Top Level	MAIN
DMSS_PKTDMA	-	-	✓ (DMSS)

Table 4-41. PKTDMA Parameters

Module Instance	Parameters	
	tchan_cnt	rchan_cnt
DMSS_PKTDMA	29	24

Table 4-42. PKTDMA TX Channel Configuration

Channel	Description	Flow Start	Flow Count
0	Periph Tx Ch 0	0	1
1	Periph Tx Ch 1	1	1
2	Periph Tx Ch 2	2	1
3	Periph Tx Ch 3	3	1
4	Periph Tx Ch 4	4	1
5	Periph Tx Ch 5	5	1
6	Periph Tx Ch 6	6	1
7	Periph Tx Ch 7	7	1
8	Periph Tx Ch 8	8	1
9	Periph Tx Ch 9	9	1
10	Periph Tx Ch 10	10	1

Table 4-42. PKTDMA TX Channel Configuration (continued)

Channel	Description	Flow Start	Flow Count
11	Periph Tx Ch 11	11	1
12	Periph Tx Ch 12	12	1
13	Periph Tx Ch 13	13	1
14	Periph Tx Ch 14	14	1
15	Periph Tx Ch 15	15	1
16	Periph Tx Ch 16	16	1
17	Periph Tx Ch 17	17	1
18	Periph Tx Ch 18	18	1
19	CPSW Tx Ch 0	19	8
20	CPSW Tx Ch 1	27	8
21	CPSW Tx Ch 2	35	8
22	CPSW Tx Ch 3	43	8
23	CPSW Tx Ch 4	51	8
24	CPSW Tx Ch 5	59	8
25	CPSW Tx Ch 6	67	8
26	CPSW Tx Ch 7	75	8
27	SAUL Tx Ch 0	83	8
28	SAUL Tx Ch 1	91	8

Table 4-43. PKTDMA RX Channel Configuration

Channel	Description	Flow Start	Flow Count
0	Periph Rx Ch 0	0	1
1	Periph Rx Ch 1	1	1
2	Periph Rx Ch 2	2	1
3	Periph Rx Ch 3	3	1
4	Periph Rx Ch 4	4	1
5	Periph Rx Ch 5	5	1
6	Periph Rx Ch 6	6	1
7	Periph Rx Ch 7	7	1
8	Periph Rx Ch 8	8	1
9	Periph Rx Ch 9	9	1
10	Periph Rx Ch 10	10	1
11	Periph Rx Ch 11	11	1
12	Periph Rx Ch 12	12	1
13	Periph Rx Ch 13	13	1
14	Periph Rx Ch 14	14	1
15	Periph Rx Ch 15	15	1
16	Periph Rx Ch 16	16	1
17	Periph Rx Ch 17	17	1
18	Periph Rx Ch 18	18	1
19	CPSW Rx Ch 0	19	16
20	SAUL Rx Ch 0	35	8
21	SAUL Rx Ch 1	35	8
22	SAUL Rx Ch 2	43	8
23	SAUL Rx Ch 3	43	8

4.6.5 Interrupt Aggregator (INTR_AGGR)

4.6.5.1 Interrupt Aggregator (INTR_AGGR)

Table 4-44. Module Allocation

Module Instance	Domain		
	WKUP	Top Level	MAIN
DMSS_INTR_AGGR	-	-	✓ (DMSS)

Table 4-45. Interrupt Aggregator Parameters

Module Instace	Parameters				
	VINTR	SEVI	GEVI	LEVI	MEVI
DMSS_INTR_AGGR	184	1536	256	32	128

4.7 Audio

4.7.1 Multichannel Audio Serial Port (MCASP)

This section contains the integration details for the MCASP module on this device. For further information, see the *Multichannel Audio Serial Port (MCASP)* section of the *Peripherals* chapter.

4.7.1.1 MCASP Unsupported Features

The following features are not supported on this family of devices:

- Muting output (AMUTE)
- Muting input (AMUTEIN)
- Instances may not support all pin options. See device specific datasheet for details on which McASP instance support which pins

4.7.1.2 Module Allocations

Table 4-46. MCASP Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
MCASP0			✓
MCASP1			✓
MCASP2			✓
MCASP3			✓
MCASP4			✓

4.7.1.3 Resets, Interrupts, and Clocks

Table 4-47. MCASP Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCASP0	MAIN_PSC0	GP_CORE_CTL	LPSC_MAIN_MCASP_0	32	OFF	YES	LPSC_MAIN_IP
MCASP1	MAIN_PSC0	GP_CORE_CTL	LPSC_MAIN_MCASP_1	33	OFF	YES	LPSC_MAIN_IP
MCASP2	MAIN_PSC0	GP_CORE_CTL	LPSC_MAIN_MCASP_2	34	OFF	YES	LPSC_MAIN_IP
MCASP3	MAIN_PSC0	GP_CORE_CTL	LPSC_MAIN_MCASP_3	35	OFF	YES	LPSC_MAIN_IP
MCASP4	MAIN_PSC0	GP_CORE_CTL	LPSC_MAIN_MCASP_4	36	OFF	YES	LPSC_MAIN_IP

Table 4-48. MCASP Resets

Module Instance	Source	Description
MCASP0	MAIN_PSC0	MCASP0 reset
MCASP1	MAIN_PSC0	MCASP1 reset
MCASP2	MAIN_PSC0	MCASP2 reset
MCASP3	MAIN_PSC0	MCASP3 reset
MCASP4	MAIN_PSC0	MCASP4 reset

Table 4-49. MCASP Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCASP0	MCASP0_rec_dma_event_req_0	PDMA2_mcasp_main_0_rx_IN_0	PDMA2	MCASP0 interrupt request	pulse
MCASP0	MCASP0_rec_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_267	C7X256V0_CLEC	MCASP0 interrupt request	level
MCASP0	MCASP0_rec_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_267	C7X256V1_CLEC	MCASP0 interrupt request	level
MCASP0	MCASP0_rec_intr_pend_0	R5FSS0_CORE0_intr_IN_120	R5FSS0_CORE0	MCASP0 interrupt request	level
MCASP0	MCASP0_rec_intr_pend_0	R5FSS0_CORE1_intr_IN_120	R5FSS0_CORE1	MCASP0 interrupt request	level
MCASP0	MCASP0_rec_intr_pend_0	R5FSS1_CORE0_intr_IN_120	R5FSS1_CORE0	MCASP0 interrupt request	level
MCASP0	MCASP0_rec_intr_pend_0	R5FSS1_CORE1_intr_IN_120	R5FSS1_CORE1	MCASP0 interrupt request	level
MCASP0	CASP0_xmit_dma_event_req_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_	DMASS0_INTAGGR_0	MCASP0 interrupt request	pulse
MCASP0	MCASP0_xmit_dma_event_req_0	PDMA2_mcasp_main_0_tx_IN_0	PDMA2	MCASP0 interrupt request	pulse
MCASP0	MCASP0_xmit_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_268	C7X256V0_CLEC	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_268	C7X256V1_CLEC	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_intr_pend_0	R5FSS0_CORE0_intr_IN_121	R5FSS0_CORE0	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_intr_pend_0	R5FSS0_CORE1_intr_IN_121	R5FSS0_CORE1	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_intr_pend_0	R5FSS1_CORE0_intr_IN_121	R5FSS1_CORE0	MCASP0 interrupt request	level
MCASP0	MCASP0_xmit_intr_pend_0	R5FSS1_CORE1_intr_IN_121	R5FSS1_CORE1	MCASP0 interrupt request	level
MCASP1	MCASP1_rec_dma_event_req_0	PDMA2_mcasp_main_1_rx_IN_0	PDMA2	MCASP1 interrupt request	pulse
MCASP1	MCASP1_rec_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_269	C7X256V0_CLEC	MCASP1 interrupt request	level
MCASP1	MCASP1_rec_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_269	C7X256V1_CLEC	MCASP1 interrupt request	level
MCASP1	MCASP1_rec_intr_pend_0	R5FSS0_CORE0_intr_IN_122	R5FSS0_CORE0	MCASP1 interrupt request	level
MCASP1	MCASP1_rec_intr_pend_0	R5FSS0_CORE1_intr_IN_122	R5FSS0_CORE1	MCASP1 interrupt request	level
MCASP1	MCASP1_rec_intr_pend_0	R5FSS1_CORE0_intr_IN_122	R5FSS1_CORE0	MCASP1 interrupt request	level

Table 4-49. MCASP Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCASP1	MCASP1_rec_intr_pend_0	R5FSS1_CORE1_intr_IN_122	R5FSS1_CORE1	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_dma_event_req_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_2	DMASS0_INTAGGR_0	MCASP1 interrupt request	pulse
MCASP1	MCASP1_xmit_dma_event_req_0	PDMA2_mcasp_main_1_tx_IN_0	PDMA2	MCASP1 interrupt request	pulse
MCASP1	MCASP1_xmit_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_270	C7X256V0_CLEC	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_270	C7X256V1_CLEC	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_intr_pend_0	R5FSS0_CORE0_intr_IN_123	R5FSS0_CORE0	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_intr_pend_0	R5FSS0_CORE1_intr_IN_123	R5FSS0_CORE1	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_intr_pend_0	R5FSS1_CORE0_intr_IN_123	R5FSS1_CORE0	MCASP1 interrupt request	level
MCASP1	MCASP1_xmit_intr_pend_0	R5FSS1_CORE1_intr_IN_123	R5FSS1_CORE1	MCASP1 interrupt request	level
MCASP2	MCASP2_rec_dma_event_req_0	PDMA2_mcasp_main_2_rx_IN_0	PDMA2	MCASP2 interrupt request	pulse
MCASP2	MCASP2_rec_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_271	C7X256V0_CLEC	MCASP2 interrupt request	level
MCASP2	MCASP2_rec_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_271	C7X256V1_CLEC	MCASP2 interrupt request	level
MCASP2	MCASP2_rec_intr_pend_0	R5FSS0_CORE0_intr_IN_124	R5FSS0_CORE0	MCASP2 interrupt request	level
MCASP2	MCASP2_rec_intr_pend_0	R5FSS0_CORE1_intr_IN_124	R5FSS0_CORE1	MCASP2 interrupt request	level
MCASP2	MCASP2_rec_intr_pend_0	R5FSS1_CORE0_intr_IN_124	R5FSS1_CORE0	MCASP2 interrupt request	level
MCASP2	MCASP2_rec_intr_pend_0	R5FSS1_CORE1_intr_IN_124	R5FSS1_CORE1	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_dma_event_req_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_3	DMASS0_INTAGGR_0	MCASP2 interrupt request	pulse
MCASP2	MCASP2_xmit_dma_event_req_0	PDMA2_mcasp_main_2_tx_IN_0	PDMA2	MCASP2 interrupt request	pulse
MCASP2	MCASP2_xmit_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_272	C7X256V0_CLEC	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_272	C7X256V1_CLEC	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_intr_pend_0	R5FSS0_CORE0_intr_IN_125	R5FSS0_CORE0	MCASP2 interrupt request	level

Table 4-49. MCASP Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCASP2	MCASP2_xmit_intr_pend_0	R5FSS0_CORE1_intr_IN_125	R5FSS0_CORE1	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_intr_pend_0	R5FSS1_CORE0_intr_IN_125	R5FSS1_CORE0	MCASP2 interrupt request	level
MCASP2	MCASP2_xmit_intr_pend_0	R5FSS1_CORE1_intr_IN_125	R5FSS1_CORE1	MCASP2 interrupt request	level
MCASP3	MCASP3_rec_dma_event_req_0	PDMA3_mcasp_main_3_rx_IN_0	PDMA3	MCASP3 interrupt request	pulse
MCASP3	MCASP3_rec_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_273	C7X256V0_CLEC	MCASP3 interrupt request	level
MCASP3	MCASP3_rec_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_273	C7X256V1_CLEC	MCASP3 interrupt request	level
MCASP3	MCASP3_rec_intr_pend_0	R5FSS0_CORE0_intr_IN_126	R5FSS0_CORE0	MCASP3 interrupt request	level
MCASP3	MCASP3_rec_intr_pend_0	R5FSS0_CORE1_intr_IN_126	R5FSS0_CORE1	MCASP3 interrupt request	level
MCASP3	MCASP3_rec_intr_pend_0	R5FSS1_CORE0_intr_IN_126	R5FSS1_CORE0	MCASP3 interrupt request	level
MCASP3	MCASP3_rec_intr_pend_0	R5FSS1_CORE1_intr_IN_126	R5FSS1_CORE1	MCASP3 interrupt request	level
MCASP3	MCASP3_xmit_dma_event_req_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_5	DMASS0_INTAGGR_0	MCASP3 interrupt request	pulse
MCASP3	MCASP3_xmit_dma_event_req_0	PDMA3_mcasp_main_3_tx_IN_0	PDMA3	MCASP3 interrupt request	pulse
MCASP3	MCASP3_xmit_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_274	C7X256V0_CLEC	MCASP3 interrupt request	level
MCASP3	MCASP3_xmit_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_274	C7X256V1_CLEC	MCASP3 interrupt request	level
MCASP3	MCASP3_xmit_intr_pend_0	R5FSS0_CORE0_intr_IN_127	R5FSS0_CORE0	MCASP3 interrupt request	level
MCASP3	MCASP3_xmit_intr_pend_0	R5FSS0_CORE1_intr_IN_127	R5FSS0_CORE1	MCASP3 interrupt request	level
MCASP3	MCASP3_xmit_intr_pend_0	R5FSS1_CORE0_intr_IN_127	R5FSS1_CORE0	MCASP3 interrupt request	level
MCASP3	MCASP3_xmit_intr_pend_0	R5FSS1_CORE1_intr_IN_127	R5FSS1_CORE1	MCASP3 interrupt request	level
MCASP4	MCASP4_rec_dma_event_req_0	PDMA3_mcasp_main_4_rx_IN_0	PDMA3	MCASP4 interrupt request	pulse
MCASP4	MCASP4_rec_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_275	C7X256V0_CLEC	MCASP4 interrupt request	level
MCASP4	MCASP4_rec_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_275	C7X256V1_CLEC	MCASP4 interrupt request	level

Table 4-49. MCASP Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCASP4	MCASP4_rec_intr_pend_0	R5FSS0_CORE0_intr_IN_130	R5FSS0_CORE0	MCASP4 interrupt request	level
MCASP4	MCASP4_rec_intr_pend_0	R5FSS0_CORE1_intr_IN_130	R5FSS0_CORE1	MCASP4 interrupt request	level
MCASP4	MCASP4_rec_intr_pend_0	R5FSS1_CORE0_intr_IN_130	R5FSS1_CORE0	MCASP4 interrupt request	level
MCASP4	MCASP4_rec_intr_pend_0	R5FSS1_CORE1_intr_IN_130	R5FSS1_CORE1	MCASP4 interrupt request	level
MCASP4	MCASP4_xmit_dma_event_req_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_5	DMASS0_INTAGGR_0	MCASP4 interrupt request	pulse
MCASP4	MCASP4_xmit_dma_event_req_0	PDMA3_mcasp_main_4_tx_IN_0	PDMA3	MCASP4 interrupt request	pulse
MCASP4	MCASP4_xmit_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_276	C7X256V0_CLEC	MCASP4 interrupt request	level
MCASP4	MCASP4_xmit_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_276	C7X256V1_CLEC	MCASP4 interrupt request	level
MCASP4	MCASP4_xmit_intr_pend_0	R5FSS0_CORE0_intr_IN_131	R5FSS0_CORE0	MCASP4 interrupt request	level
MCASP4	MCASP4_xmit_intr_pend_0	R5FSS0_CORE1_intr_IN_131	R5FSS0_CORE1	MCASP4 interrupt request	level
MCASP4	MCASP4_xmit_intr_pend_0	R5FSS1_CORE0_intr_IN_131	R5FSS1_CORE0	MCASP4 interrupt request	level
MCASP4	MCASP4_xmit_intr_pend_0	R5FSS1_CORE1_intr_IN_131	R5FSS1_CORE1	MCASP4 interrupt request	level

Table 4-50. MCASP Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCASP0	AUX_CLK	MAIN_PLL4_HSDIV0_CLKOUT	MCASP0_CLKSEL[9:8]	
		MAIN_PLL2_HSDIV8_CLKOUT	MCASP0_CLKSEL[2:0]	
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP0_AHCLKSEL[3:0]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP0_AHCLKSEL[11:8]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		

Table 4-50. MCASP Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCASP1	AUX_CLK	MAIN_PLL4_HSDIV0_CLKOUT	MCASP1_CLKSEL[9:8]	
		MAIN_PLL2_HSDIV8_CLKOUT	MCASP1_CLKSEL[2:0]	
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP1_AHCLKSEL[3:0]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP1_AHCLKSEL[11:8]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		

Table 4-50. MCASP Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCASP2	AUX_CLK	MAIN_PLL4_HSDIV0_CLKOUT	MCASP2_CLKSEL[9:8]	
		MAIN_PLL2_HSDIV8_CLKOUT	MCASP2_CLKSEL[2:0]	
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP2_AHCLKSEL[3:0]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP2_AHCLKSEL[11:8]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		

Table 4-50. MCASP Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCASP3	AUX_CLK	MAIN_PLL4_HSDIV0_CLKOUT	MCASP3_CLKSEL[9:8]	
		MAIN_PLL2_HSDIV8_CLKOUT	MCASP3_CLKSEL[2:0]	
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP3_AHCLKSEL[3:0]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP3_AHCLKSEL[11:8]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		

Table 4-50. MCASP Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCASP4	AUX_CLK	MAIN_PLL4_HSDIV0_CLKOUT	MCASP4_CLKSEL[9:8]	
		MAIN_PLL2_HSDIV8_CLKOUT	MCASP4_CLKSEL[2:0]	
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP4_AHCLKSEL[3:0]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		
	MCASP_AHCLKR_PIN	EXT_REFCLK1	MCASP4_AHCLKSEL[11:8]	
		HFOSC0_CLKOUT		
		MAIN_PLL2_HSDIV8_CLKOUT		
		MAIN_PLL1_HSDIV6_CLKOUT		
		MAIN_PLL2_HSDIV0_CLKOUT		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_PLL0_HSDIV7_CLKOUT		

4.7.2 Asynchronous Audio Sample Rate Converter (ASRC)

4.7.2.1 ASRC Unsupported Features

The following features are not supported on this family of devices:

- None

4.7.2.2 Module Allocations

Table 4-51. ASRC Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
AASRC0			✓
AASRC1			✓

4.7.2.3 Resets, Interrupts, and Clocks

Table 4-52. AASRC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
AASRC0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ASRC0	38	OFF	YES	LPSC_MAIN_IP0
AASRC1	MAIN_PSC0	GP_CORE	LPSC_MAIN_ASRC1	39	OFF	YES	LPSC_MAIN_IP0

Table 4-53. AASRC Resets

Module Instance	Source	Description
AASRC0	MAIN_PSC0	AASRC0 reset
AASRC1	MAIN_PSC0	AASRC1 reset

Table 4-54. AASRC Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
AASRC0	AASRC0_err_level_0	C7X256V0_CLEC_gic_spi_IN_54	C7X256V0_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_err_level_0	C7X256V1_CLEC_gic_spi_IN_54	C7X256V1_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_err_level_0	R5FSS0_CORE0_intr_IN_54	R5FSS0_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_err_level_0	R5FSS0_CORE1_intr_IN_54	R5FSS0_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_err_level_0	R5FSS1_CORE0_intr_IN_54	R5FSS1_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_err_level_0	R5FSS1_CORE1_intr_IN_54	R5FSS1_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_infifo_dma_[15:0]	PDMA_AASRC0_6_infifo_evt_IN_[15:0]	PDMA_AASRC0_6	AASRC0 interrupt request	pulse
AASRC0	AASRC0_infifo_level_0	C7X256V0_CLEC_gic_spi_IN_50	C7X256V0_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_infifo_level_0	C7X256V1_CLEC_gic_spi_IN_50	C7X256V1_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_infifo_level_0	R5FSS0_CORE0_intr_IN_50	R5FSS0_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_infifo_level_0	R5FSS0_CORE1_intr_IN_50	R5FSS0_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_infifo_level_0	R5FSS1_CORE0_intr_IN_50	R5FSS1_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_infifo_level_0	R5FSS1_CORE1_intr_IN_50	R5FSS1_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_ingroup_level_0	C7X256V0_CLEC_gic_spi_IN_51	C7X256V0_CLEC	AASRC0 interrupt request	level

Table 4-54. AASRC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
AASRC0	AASRC0_ingroup_level_0	C7X256V1_CLEC_gic_spi_IN_51	C7X256V1_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_ingroup_level_0	R5FSS0_CORE0_intr_IN_51	R5FSS0_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_ingroup_level_0	R5FSS0_CORE1_intr_IN_51	R5FSS0_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_ingroup_level_0	R5FSS1_CORE0_intr_IN_51	R5FSS1_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_ingroup_level_0	R5FSS1_CORE1_intr_IN_51	R5FSS1_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_ingrp_dma_[3:0]	PDMA_AASRC0_6_ingrp_evt_IN_[3:0]	PDMA_AASRC0_6	AASRC0 interrupt request	pulse
AASRC0	AASRC0_outfifo_dma_[15:0]	PDMA_AASRC0_6_outfifo_evt_IN_[15:0]	PDMA_AASRC0_6	AASRC0 interrupt request	pulse
AASRC0	AASRC0_outfifo_level_0	C7X256V0_CLEC_gic_spi_IN_52	C7X256V0_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_outfifo_level_0	C7X256V1_CLEC_gic_spi_IN_52	C7X256V1_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_outfifo_level_0	R5FSS0_CORE0_intr_IN_52	R5FSS0_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_outfifo_level_0	R5FSS0_CORE1_intr_IN_52	R5FSS0_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_outfifo_level_0	R5FSS1_CORE0_intr_IN_52	R5FSS1_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_outfifo_level_0	R5FSS1_CORE1_intr_IN_52	R5FSS1_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_outgroup_level_0	C7X256V0_CLEC_gic_spi_IN_53	C7X256V0_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_outgroup_level_0	C7X256V1_CLEC_gic_spi_IN_53	C7X256V1_CLEC	AASRC0 interrupt request	level
AASRC0	AASRC0_outgroup_level_0	R5FSS0_CORE0_intr_IN_53	R5FSS0_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_outgroup_level_0	R5FSS0_CORE1_intr_IN_53	R5FSS0_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_outgroup_level_0	R5FSS1_CORE0_intr_IN_53	R5FSS1_CORE0	AASRC0 interrupt request	level
AASRC0	AASRC0_outgroup_level_0	R5FSS1_CORE1_intr_IN_53	R5FSS1_CORE1	AASRC0 interrupt request	level
AASRC0	AASRC0_outgrp_dma_[3:0]	PDMA_AASRC0_6_outgrp_evt_IN_[3:0]	PDMA_AASRC0_6	AASRC0 interrupt request	pulse
AASRC1	AASRC1_err_level_0	C7X256V0_CLEC_gic_spi_IN_59	C7X256V0_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_err_level_0	C7X256V1_CLEC_gic_spi_IN_59	C7X256V1_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_err_level_0	R5FSS0_CORE0_intr_IN_59	R5FSS0_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_err_level_0	R5FSS0_CORE1_intr_IN_59	R5FSS0_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_err_level_0	R5FSS1_CORE0_intr_IN_59	R5FSS1_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_err_level_0	R5FSS1_CORE1_intr_IN_59	R5FSS1_CORE1	AASRC1 interrupt request	level

Table 4-54. AASRC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
AASRC1	AASRC1_infifo_dma_[15:0]	PDMA_AASRC1_7_infifo_evt_IN_[15:0]	PDMA_AASRC1_7	AASRC1 interrupt request	pulse
AASRC1	AASRC1_infifo_level_0	C7X256V0_CLEC_gic_spi_IN_55	C7X256V0_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_infifo_level_0	C7X256V1_CLEC_gic_spi_IN_55	C7X256V1_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_infifo_level_0	R5FSS0_CORE0_intr_IN_55	R5FSS0_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_infifo_level_0	R5FSS0_CORE1_intr_IN_55	R5FSS0_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_infifo_level_0	R5FSS1_CORE0_intr_IN_55	R5FSS1_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_infifo_level_0	R5FSS1_CORE1_intr_IN_55	R5FSS1_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_ingroup_level_0	C7X256V0_CLEC_gic_spi_IN_56	C7X256V0_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_ingroup_level_0	C7X256V1_CLEC_gic_spi_IN_56	C7X256V1_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_ingroup_level_0	R5FSS0_CORE0_intr_IN_56	R5FSS0_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_ingroup_level_0	R5FSS0_CORE1_intr_IN_56	R5FSS0_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_ingroup_level_0	R5FSS1_CORE0_intr_IN_56	R5FSS1_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_ingroup_level_0	R5FSS1_CORE1_intr_IN_56	R5FSS1_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_ingrp_dma_[3:0]	PDMA_AASRC1_7_ingrp_evt_IN_[3:0]	PDMA_AASRC1_7	AASRC1 interrupt request	pulse
AASRC1	AASRC1_outfifo_dma_[15:0]	PDMA_AASRC1_7_outfifo_evt_IN_[15:0]	PDMA_AASRC1_7	AASRC1 interrupt request	pulse
AASRC1	AASRC1_outfifo_level_0	C7X256V0_CLEC_gic_spi_IN_57	C7X256V0_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_outfifo_level_0	C7X256V1_CLEC_gic_spi_IN_57	C7X256V1_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_outfifo_level_0	R5FSS0_CORE0_intr_IN_57	R5FSS0_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_outfifo_level_0	R5FSS0_CORE1_intr_IN_57	R5FSS0_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_outfifo_level_0	R5FSS1_CORE0_intr_IN_57	R5FSS1_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_outfifo_level_0	R5FSS1_CORE1_intr_IN_57	R5FSS1_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_outgroup_level_0	C7X256V0_CLEC_gic_spi_IN_58	C7X256V0_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_outgroup_level_0	C7X256V1_CLEC_gic_spi_IN_58	C7X256V1_CLEC	AASRC1 interrupt request	level
AASRC1	AASRC1_outgroup_level_0	R5FSS0_CORE0_intr_IN_58	R5FSS0_CORE0	AASRC1 interrupt request	level
AASRC1	AASRC1_outgroup_level_0	R5FSS0_CORE1_intr_IN_58	R5FSS0_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_outgroup_level_0	R5FSS1_CORE0_intr_IN_58	R5FSS1_CORE0	AASRC1 interrupt request	level

Table 4-54. AASRC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
AASRC1	AASRC1_outgroup_level_0	R5FSS1_CORE1_intr_IN_58	R5FSS1_CORE1	AASRC1 interrupt request	level
AASRC1	AASRC1_outgrp_dma_[3:0]	PDMA_AASRC1_7_outgrp_evt_IN_[3:0]	PDMA_AASRC1_7	AASRC1 interrupt request	pulse

Table 4-55. AASRC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC0	RX0_SYNC_CLK	HFOSC0_CLKOUT	ASRC0_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC0_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC0_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC0_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC0_RXSYNC0_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC0_RXSYNC0_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC0_RXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC0_RXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC0_RXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC0_RXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC0_RXSYNC0_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC0_RXSYNC0_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC0	RX1_SYNC_CLK	HFOSC0_CLKOUT	ASRC0_RXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC0_RXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC0_RXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC0_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC0_RXSYNC1_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC0_RXSYNC1_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC0_RXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC0_RXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC0_RXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC0_RXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC0_RXSYNC1_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC0_RXSYNC1_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC0	RX2_SYNC_CLK	HFOSC0_CLKOUT	ASRC0_RXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC0_RXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC0_RXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC0_RXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC0_RXSYNC2_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC0_RXSYNC2_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC0_RXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC0_RXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC0_RXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC0_RXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC0_RXSYNC2_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC0_RXSYNC2_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC0	RX3_SYNC_CLK	HFOSC0_CLKOUT	ASRC0_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC0_RXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC0_RXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC0_RXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC0_RXSYNC3_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC0_RXSYNC3_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC0_RXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC0_RXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC0_RXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC0_RXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC0_RXSYNC3_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC0_RXSYNC3_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC0	TX0_SYNC_CLK	HFOSC0_CLKOUT	ASRC0_TXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC0_TXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC0_TXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC0_TXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC0_TXSYNC0_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC0_TXSYNC0_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC0_TXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC0_TXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC0_TXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC0_TXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC0_TXSYNC0_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC0_TXSYNC0_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC0	TX1_SYNC_CLK	HFOSC0_CLKOUT	ASRC0_TXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC0_TXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC0_TXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC0_TXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC0_TXSYNC1_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC0_TXSYNC1_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC0_TXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC0_TXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC0_TXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC0_TXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC0_TXSYNC1_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC0_TXSYNC1_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC0	TX2_SYNC_CLK	HFOSC0_CLKOUT	ASRC0_TXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC0_TXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC0_TXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC0_TXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC0_TXSYNC2_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC0_TXSYNC2_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC0_TXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC0_TXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC0_TXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC0_TXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC0_TXSYNC2_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC0_TXSYNC2_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC0	TX3_SYNC_CLK	HFOSC0_CLKOUT	ASRC0_TXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC0_TXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC0_TXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC0_TXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC0_TXSYNC3_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC0_TXSYNC3_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC0_TXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC0_TXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC0_TXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC0_TXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC0_TXSYNC3_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC0_TXSYNC3_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC1	RX0_SYNC_CLK	HFOSC0_CLKOUT	ASRC1_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC1_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC1_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC1_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC1_RXSYNC0_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC1_RXSYNC0_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC1_RXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC1_RXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC1_RXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC1_RXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC1_RXSYNC0_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC1_RXSYNC0_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC1	RX1_SYNC_CLK	HFOSC0_CLKOUT	ASRC1_RXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC1_RXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC1_RXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC1_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC1_RXSYNC1_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC1_RXSYNC1_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC1_RXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC1_RXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC1_RXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC1_RXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC1_RXSYNC1_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC1_RXSYNC1_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC1	RX2_SYNC_CLK	HFOSC0_CLKOUT	ASRC1_RXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC1_RXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC1_RXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC1_RXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC1_RXSYNC2_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC1_RXSYNC2_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC1_RXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC1_RXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC1_RXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC1_RXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC1_RXSYNC2_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC1_RXSYNC2_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC1	RX3_SYNC_CLK	HFOSC0_CLKOUT	ASRC1_RXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC1_RXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC1_RXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC1_RXSYNC3_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC1_RXSYNC3_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC1_RXSYNC3_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC1_RXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC1_RXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC1_RXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC1_RXSYNC3_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC1_RXSYNC3_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC1_RXSYNC3_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC1	TX0_SYNC_CLK	HFOSC0_CLKOUT	ASRC1_TXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC1_TXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC1_TXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC1_TXSYNC0_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC1_TXSYNC0_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC1_TXSYNC0_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC1_TXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC1_TXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC1_TXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC1_TXSYNC0_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC1_TXSYNC0_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC1_TXSYNC0_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC1	TX1_SYNC_CLK	HFOSC0_CLKOUT	ASRC1_TXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC1_TXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC1_TXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC1_TXSYNC1_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC1_TXSYNC1_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC1_TXSYNC1_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC1_TXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC1_TXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC1_TXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC1_TXSYNC1_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC1_TXSYNC1_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC1_TXSYNC1_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC1	TX2_SYNC_CLK	HFOSC0_CLKOUT	ASRC1_TXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC1_TXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC1_TXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC1_TXSYNC2_SEL[4:0]	
			ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC1_TXSYNC2_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC1_TXSYNC2_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC1_TXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC1_TXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC1_TXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC1_TXSYNC2_SEL[4:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC1_TXSYNC2_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC1_TXSYNC2_SEL[4:0	

Table 4-55. AASRC Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
AASRC1	TX3_SYNC_CLK	HFOSC0_CLKOUT	ASRC1_TXSYNC3_SEL[4:0] ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ASRC1_TXSYNC3_SEL[4:0] ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ASRC1_TXSYNC3_SEL[4:0] ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ASRC1_TXSYNC3_SEL[4:0] ADC0_CLKSEL[1:0]	
		MAIN_PLL4_HSDIV3_CLKOUT	ASRC1_TXSYNC3_SEL[4:0]	
		MAIN_SYSCLK0/2	ASRC1_TXSYNC3_SEL[4:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	ASRC1_TXSYNC3_SEL[4:0] CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	ASRC1_TXSYNC3_SEL[4:0] CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ASRC1_TXSYNC3_SEL[4:0] CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	ASRC1_TXSYNC3_SEL[4:0] CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	ASRC1_TXSYNC3_SEL[4:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	ASRC1_TXSYNC3_SEL[4:0	

4.7.3 Analog to Digital Converter Integration (ADC)

This section contains the integration details for ADC module on this device. For Further information, see the ADC section of the Peripherals chapter

4.7.3.1 ADC Unsupported Features

The following features are not supported on this family of devices:

- 12-bit resolution

4.7.3.2 Module Allocations

Table 4-56. ADC Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
ADC0 (adc12fc_16ffc0)			✓

4.7.3.3 Resets, Interrupts, and Clocks

Table 4-57. ADC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
ADC0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ADC	41	OFF	YES	LPSC_MAIN_IP0

Table 4-58. ADC Resets

Module Instance	Source	Description
ADC0	MAIN_PSC0	ADC0 reset

Table 4-59. ADC Hardware Request

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ADC0	ADC0_ecc_corrected_err_level_0	ESM0_esm_lvl_event_IN_33	ESM0	ADC0 interrupt request	level
ADC0	ADC0_ecc_uncorrected_err_level_0	ESM0_esm_lvl_event_IN_34	ESM0	ADC0 interrupt request	level
ADC0	ADC0_fifo0_pulse_0	PDMA5_adc12_0_rx_IN_0	PDMA5	ADC0 interrupt request	pulse
ADC0	ADC0_fifo1_pulse_0	PDMA5_adc12_0_rx_IN_1	PDMA5	ADC0 interrupt request	pulse
ADC0	ADC0_gen_level_0	C7X256V0_CLEC_gic_spi_IN_151	C7X256V0_CLEC	ADC0 interrupt request	level
ADC0	ADC0_gen_level_0	C7X256V1_CLEC_gic_spi_IN_151	C7X256V1_CLEC	ADC0 interrupt request	level
ADC0	ADC0_gen_level_0	R5FSS0_CORE0_intr_IN_151	R5FSS0_CORE0	ADC0 interrupt request	level
ADC0	ADC0_gen_level_0	R5FSS0_CORE1_intr_IN_151	R5FSS0_CORE1	ADC0 interrupt request	level
ADC0	ADC0_gen_level_0	R5FSS1_CORE0_intr_IN_151	R5FSS1_CORE0	ADC0 interrupt request	level
ADC0	ADC0_gen_level_0	R5FSS1_CORE1_intr_IN_151	R5FSS1_CORE1	ADC0 interrupt request	level
ADC0	ADC0_gen_level_0	WKUP_R5FSS0_CORE0_intr_IN_151	WKUP_R5FSS0_CORE0	ADC0 interrupt request	level

Table 4-60. ADC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
ADC	ADC_CLK	HFOSC0_CLKOUT	ADC0_CLKSEL[1:0]	
		HFOSC1_CLKOUT	ADC0_CLKSEL[1:0]	
		MAIN_PLL1_HSDIV4_CLKOUT	ADC0_CLKSEL[1:0]	
		EXT_REFCLK1	ADC0_CLKSEL[1:0]	
	SYS_CLK	MAIN_SYSCLK0		
	VBUS_CLK	MAIN_SYSCLK0/2		

4.7.4 ATL Integration

4.7.4.1 ATL Unsupported Features

The following features are not supported on this family of devices:

- Smart ATL_CLK_STOP
- ATL_MOD_OUT[3-0] clock outputs

4.7.4.2 ATL Module Allocations

Table 4-61. ATL Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
ATL0			✓

4.7.4.3 Resets, Interrupts, and Clocks

Table 4-62. ATL Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
ATL0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ATL	37	OFF	YES	LPSC_MAIN_IP0

Table 4-63. ATL Resets

Module Instance	Source	Description
ATL0	MAIN_PSC0	ATL0 reset

Table 4-64. ATL Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
ATL0	ATL_CLK	MAIN_PLL2_HSDIV8_CLKOUT	ATL_CLKSEL[2:0]	
		MAIN_PLL1_HSDIV6_CLKOUT	ATL_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV0_CLKOUT	ATL_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	ATL_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	ATL_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	ATL_CLKSEL[2:0]	
		EXT_REFCLK1	ATL_CLKSEL[2:0]	
	VBUS_CLK	MAIN_SYSCLK0/2		

4.7.5 MLB Integration

4.7.5.1 MLB Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.7.5.2 MLB Module Allocations

Table 4-65. MLB Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
MLB0			✓

4.7.5.3 Resets, Interrupts, and Clocks

Table 4-66. MLB Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MLB0	MAIN_PSC0	GP_CORE	LPSC_MAIN_MLB	40	OFF	YES	LPSC_MAIN_IP0

Table 4-67. MLB Resets

Module Instance	Source	Description
MLB0	MAIN_PSC0	MLB0 reset

Table 4-68. MLB Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MLB0	MLBSS_AMLB_CLK	MCU_TIEOFF0		
	MLBSS_HCLK_CLK	MAIN_SYSCLK0/2		
	MLBSS_PCLK_CLK	MAIN_SYSCLK0/2		
	MLBSS_SCLK_CLK	MAIN_SYSCLK0/2		

Table 4-69. MLB Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MLB0	MLB0_mlbss_ecc_corr_lvl_0	ESM0_esm_lvl_event_IN_77	ESM0	MLB0 interrupt request	level
	MLB0_mlbss_ecc_uncorr_lvl_0	ESM0_esm_lvl_event_IN_78	ESM0	MLB0 interrupt request	level
	MLB0_mlbss_mlb_ahb_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_61	C7X256V0_CLEC	MLB0 interrupt request	level
		C7X256V0_CLEC_gic_spi_IN_62	C7X256V0_CLEC	MLB0 interrupt request	level
		C7X256V1_CLEC_gic_spi_IN_61	C7X256V1_CLEC	MLB0 interrupt request	level
		C7X256V1_CLEC_gic_spi_IN_62	C7X256V1_CLEC	MLB0 interrupt request	level
		R5FSS0_CORE0_intr_IN_61	R5FSS0_CORE0	MLB0 interrupt request	level
		R5FSS0_CORE0_intr_IN_62	R5FSS0_CORE0	MLB0 interrupt request	level
		R5FSS0_CORE1_intr_IN_61	R5FSS0_CORE1	MLB0 interrupt request	level
		R5FSS0_CORE1_intr_IN_62	R5FSS0_CORE1	MLB0 interrupt request	level
		R5FSS1_CORE0_intr_IN_61	R5FSS1_CORE0	MLB0 interrupt request	level
		R5FSS1_CORE0_intr_IN_62	R5FSS1_CORE0	MLB0 interrupt request	level
		R5FSS1_CORE1_intr_IN_61	R5FSS1_CORE1	MLB0 interrupt request	level
		R5FSS1_CORE1_intr_IN_62	R5FSS1_CORE1	MLB0 interrupt request	level
	MLB0_mlbss_mlb_int_0	C7X256V0_CLEC_gic_spi_IN_60	C7X256V0_CLEC	MLB0 interrupt request	level
		C7X256V1_CLEC_gic_spi_IN_60	C7X256V1_CLEC	MLB0 interrupt request	level
		R5FSS0_CORE0_intr_IN_60	R5FSS0_CORE0	MLB0 interrupt request	level
		R5FSS0_CORE1_intr_IN_60	R5FSS0_CORE1	MLB0 interrupt request	level
		R5FSS1_CORE0_intr_IN_60	R5FSS1_CORE0	MLB0 interrupt request	level
		R5FSS1_CORE1_intr_IN_60	R5FSS1_CORE1	MLB0 interrupt request	level

4.8 General Connectivity

4.8.1 General Purpose Input/Output (GPIO)

This section contains the integration details for the GPIO modules on this device. For further information, see the *General-Purpose Interface* section of the *Peripherals* chapter.

4.8.1.1 GPIO Unsupported Features

The following features are not supported on this family of devices:

- The following apply to MCU_GPIO0:
  - MCU_GPIO0_[143:24] are not pinned out.
  - Interrupts [143:24] are not pinned out.
  - Bank Interrupts [8:2] are not pinned out.
- The following apply to GPIO0:
  - GPIO0_[143:92] are not pinned out.
  - Interrupts [143:92] are not pinned out.
  - Bank Interrupts [8:6] are not pinned out.
- The following apply to GPIO1:
  - GPIO1_[143:52] are not pinned out.
  - Interrupts [143:52] are not pinned out.
  - Bank Interrupts [8:4] are not pinned out.

4.8.1.2 Module Allocation

Table 4-70. GPIO Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
GPIO0			✓
GPIO1			✓
MCU_GPIO0		✓	

4.8.1.3 Resets, Interrupts, and Clocks

Table 4-71. GPIO Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
GPIO0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
GPIO1	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
MCU_GPIO0	WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	NONE

Table 4-72. GPIO Resets

Module Instance	Source	Description
GPIO0	MAIN_PSC0	GPIO0 reset
GPIO1	MAIN_PSC0	GPIO1 reset
MCU_GPIO0	WKUP_PSC0	MCU_GPIO0 reset

Table 4-73. GPIO Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
GPIO0	GPIO0_gpio_[143:0]	MAIN_GPIOMUX_INTROUTER0_in_IN_[92:0]	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_[8:0]	MAIN_GPIOMUX_INTROUTER0_in_IN_[197:192]	MAIN_GPIOMUX_INTROUTER0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_[8:0]	WKUP_R5FSS0_CORE0_intr_IN_56	R5FSS0_CORE0	GPIO0 interrupt request	pulse
GPIO0	GPIO0_gpio_bank_[8:0]	WKUP_R5FSS0_CORE0_intr_IN_57	R5FSS0_CORE0	GPIO0 interrupt request	pulse
GPIO1	GPIO1_gpio_[143:0]	MAIN_GPIOMUX_INTROUTER0_in_IN_[181:96]	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
GPIO1	GPIO1_gpio_bank_[8:0]	MAIN_GPIOMUX_INTROUTER0_in_IN_[205:200]	MAIN_GPIOMUX_INTROUTER0	GPIO1 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_[143:0]	MCU_MCU_GPIOMUX_INTROUTER0_in_IN_[25:0]	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_bank_[8:0]	MCU_MCU_GPIOMUX_INTROUTER0_in_IN_[31:30]	WKUP_MCU_GPIOMUX_INTROUTER0	MCU_GPIO0 interrupt request	pulse
MCU_GPIO0	MCU_GPIO0_gpio_lvl_0	WKUP_R5FSS0_CORE0_intr_IN_18	R5FSS0_CORE0	MCU_GPIO0 interrupt request	level

Table 4-74. GPIO Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
GPIO0	FICLK	MAIN_SYSCLK0/4		GPIO0 Functional and Interface Clock
GPIO1	FICLK	MAIN_SYSCLK0/4		GPIO1 Functional and Interface Clock
MCU_GPIO0	FICLK	MCU_SYSCLK0/4	MCU_GPIO_CLKSEL[1:0]	MCU_GPIO0 Functional and Interface Clock
		LFOSC0_CLKOUT		
		CLK_32K_RC		
		CLK_12M_RC		

4.8.1.4 GPIO1 Register/Pin Mapping

Signal	Bank	GPIO0_*_DATA	Register Bit		Signal	Bank	GPIO0_*_DATA	Register Bit		Signal	Bank	GPIO0_*_DATA	Register Bit
GPIO0_0	Bank 0	GPIO0_*_DATA	0		GPIO0_32	Bank 2	GPIO0_*_DATA	0		GPIO0_64	Bank 4	GPIO0_*_DATA	0
GPIO0_1	Bank 0	GPIO0_*_DATA	1		GPIO0_33	Bank 2	GPIO0_*_DATA	1		GPIO0_65	Bank 4	GPIO0_*_DATA	1
GPIO0_2	Bank 0	GPIO0_*_DATA	2		GPIO0_34	Bank 2	GPIO0_*_DATA	2		GPIO0_66	Bank 4	GPIO0_*_DATA	2
GPIO0_3	Bank 0	GPIO0_*_DATA	3		GPIO0_35	Bank 2	GPIO0_*_DATA	3		GPIO0_67	Bank 4	GPIO0_*_DATA	3

Signal	Bank	GPIO0_*_DATA	Register Bit		Signal	Bank	GPIO0_*_DATA	Register Bit		Signal	Bank	GPIO0_*_DATA	Register Bit
GPIO0_4	Bank 0	GPIO0_*_DATA	4		GPIO0_36	Bank 2	GPIO0_*_DATA	4		GPIO0_68	Bank 4	GPIO0_*_DATA	4
GPIO0_5	Bank 0	GPIO0_*_DATA	5		GPIO0_37	Bank 2	GPIO0_*_DATA	5		GPIO0_69	Bank 4	GPIO0_*_DATA	5
GPIO0_6	Bank 0	GPIO0_*_DATA	6		GPIO0_38	Bank 2	GPIO0_*_DATA	6		GPIO0_70	Bank 4	GPIO0_*_DATA	6
GPIO0_7	Bank 0	GPIO0_*_DATA	7		GPIO0_39	Bank 2	GPIO0_*_DATA	7		GPIO0_71	Bank 4	GPIO0_*_DATA	7
GPIO0_8	Bank 0	GPIO0_*_DATA	8		GPIO0_40	Bank 2	GPIO0_*_DATA	8		GPIO0_72	Bank 4	GPIO0_*_DATA	8
GPIO0_9	Bank 0	GPIO0_*_DATA	9		GPIO0_41	Bank 2	GPIO0_*_DATA	9		GPIO0_73	Bank 4	GPIO0_*_DATA	9
GPIO0_10	Bank 0	GPIO0_*_DATA	10		GPIO0_42	Bank 2	GPIO0_*_DATA	10		GPIO0_74	Bank 4	GPIO0_*_DATA	10
GPIO0_11	Bank 0	GPIO0_*_DATA	11		GPIO0_43	Bank 2	GPIO0_*_DATA	11		GPIO0_75	Bank 4	GPIO0_*_DATA	11
GPIO0_12	Bank 0	GPIO0_*_DATA	12		GPIO0_44	Bank 2	GPIO0_*_DATA	12		GPIO0_76	Bank 4	GPIO0_*_DATA	12
GPIO0_13	Bank 0	GPIO0_*_DATA	13		GPIO0_45	Bank 2	GPIO0_*_DATA	13		GPIO0_77	Bank 4	GPIO0_*_DATA	13
GPIO0_14	Bank 0	GPIO0_*_DATA	14		GPIO0_46	Bank 2	GPIO0_*_DATA	14		GPIO0_78	Bank 4	GPIO0_*_DATA	14
GPIO0_15	Bank 0	GPIO0_*_DATA	15		GPIO0_47	Bank 2	GPIO0_*_DATA	15		GPIO0_79	Bank 4	GPIO0_*_DATA	15
GPIO0_16	Bank 1	GPIO0_*_DATA	16		GPIO0_48	Bank 3	GPIO0_*_DATA	16		GPIO0_80	Bank 5	GPIO0_*_DATA	16
GPIO0_17	Bank 1	GPIO0_*_DATA	17		GPIO0_49	Bank 3	GPIO0_*_DATA	17		GPIO0_81	Bank 5	GPIO0_*_DATA	17
GPIO0_18	Bank 1	GPIO0_*_DATA	18		GPIO0_50	Bank 3	GPIO0_*_DATA	18		GPIO0_82	Bank 5	GPIO0_*_DATA	18
GPIO0_19	Bank 1	GPIO0_*_DATA	19		GPIO0_51	Bank 3	GPIO0_*_DATA	19		GPIO0_83	Bank 5	GPIO0_*_DATA	19
GPIO0_20	Bank 1	GPIO0_*_DATA	20		GPIO0_52	Bank 3	GPIO0_*_DATA	20		GPIO0_84	Bank 5	GPIO0_*_DATA	20
GPIO0_21	Bank 1	GPIO0_*_DATA	21		GPIO0_53	Bank 3	GPIO0_*_DATA	21		GPIO0_85	Bank 5	GPIO0_*_DATA	21
GPIO0_22	Bank 1	GPIO0_*_DATA	22		GPIO0_54	Bank 3	GPIO0_*_DATA	22		GPIO0_86	Bank 5	GPIO0_*_DATA	22
GPIO0_23	Bank 1	GPIO0_*_DATA	23		GPIO0_55	Bank 3	GPIO0_*_DATA	23		GPIO0_87	Bank 5	GPIO0_*_DATA	23
GPIO0_24	Bank 1	GPIO0_*_DATA	24		GPIO0_56	Bank 3	GPIO0_*_DATA	24		GPIO0_88	Bank 5	GPIO0_*_DATA	24
GPIO0_25	Bank 1	GPIO0_*_DATA	25		GPIO0_57	Bank 3	GPIO0_*_DATA	25		GPIO0_89	Bank 5	GPIO0_*_DATA	25
GPIO0_26	Bank 1	GPIO0_*_DATA	26		GPIO0_58	Bank 3	GPIO0_*_DATA	26		GPIO0_90	Bank 5	GPIO0_*_DATA	26
GPIO0_27	Bank 1	GPIO0_*_DATA	27		GPIO0_59	Bank 3	GPIO0_*_DATA	27		GPIO0_91	Bank 5	GPIO0_*_DATA	27
GPIO0_28	Bank 1	GPIO0_*_DATA	28		GPIO0_60	Bank 3	GPIO0_*_DATA	28					
GPIO0_29	Bank 1	GPIO0_*_DATA	29		GPIO0_61	Bank 3	GPIO0_*_DATA	29					
GPIO0_30	Bank 1	GPIO0_*_DATA	30		GPIO0_62	Bank 3	GPIO0_*_DATA	30					

Signal	Bank	GPIO0_*_DATA	Register Bit		Signal	Bank	GPIO0_*_DATA	Register Bit		Signal	Bank	GPIO0_*_DATA	Register Bit
GPIO0_31	Bank 1	GPIO0_*_DATA	31		GPIO0_63	Bank 3	GPIO0_*_DATA	31					

4.8.1.5 GPIO1 Register/Pin Mapping

Signal	Bank	GPIO1_*_DATA	Register Bit		Signal	Bank	GPIO1_*_DATA	Register Bit		Signal	Bank	GPIO1_*_DATA	Register Bit
GPIO1_0	Bank 0	GPIO1_*_DATA	0		GPIO1_16	Bank 1	GPIO1_*_DATA	16		GPIO1_48	Bank 3	GPIO1_*_DATA	16
GPIO1_1	Bank 0	GPIO1_*_DATA	1		GPIO1_17	Bank 1	GPIO1_*_DATA	17		GPIO1_49	Bank 3	GPIO1_*_DATA	17
GPIO1_2	Bank 0	GPIO1_*_DATA	2		GPIO1_18	Bank 1	GPIO1_*_DATA	18		GPIO1_50	Bank 3	GPIO1_*_DATA	18
GPIO1_3	Bank 0	GPIO1_*_DATA	3		GPIO1_19	Bank 1	GPIO1_*_DATA	19		GPIO1_51	Bank 3	GPIO1_*_DATA	19
GPIO1_4	Bank 0	GPIO1_*_DATA	4		GPIO1_20	Bank 1	GPIO1_*_DATA	20					
GPIO1_5	Bank 0	GPIO1_*_DATA	5		GPIO1_21	Bank 1	GPIO1_*_DATA	21					
GPIO1_6	Bank 0	GPIO1_*_DATA	6		GPIO1_22	Bank 1	GPIO1_*_DATA	22					
GPIO1_7	Bank 0	GPIO1_*_DATA	7		GPIO1_23	Bank 1	GPIO1_*_DATA	23					
GPIO1_8	Bank 0	GPIO1_*_DATA	8		GPIO1_24	Bank 1	GPIO1_*_DATA	24					
GPIO1_9	Bank 0	GPIO1_*_DATA	9		GPIO1_25	Bank 1	GPIO1_*_DATA	25					
GPIO1_10	Bank 0	GPIO1_*_DATA	10		GPIO1_26	Bank 1	GPIO1_*_DATA	26					
GPIO1_11	Bank 0	GPIO1_*_DATA	11		GPIO1_27	Bank 1	GPIO1_*_DATA	27					
GPIO1_12	Bank 0	GPIO1_*_DATA	12		GPIO1_28	Bank 1	GPIO1_*_DATA	28					
GPIO1_13	Bank 0	GPIO1_*_DATA	13		GPIO1_29	Bank 1	GPIO1_*_DATA	29					
GPIO1_14	Bank 0	GPIO1_*_DATA	14		GPIO1_30	Bank 1	GPIO1_*_DATA	30					
GPIO1_15	Bank 0	GPIO1_*_DATA	15		GPIO1_31	Bank 1	GPIO1_*_DATA	31					

4.8.1.6 MCU_GPIO0 Register/Pin Mapping

Signal	Bank	MCU_GPIO0_*_DATA	Register Bit		Signal	Bank	MCU_GPIO0_*_DATA	Register Bit
MCU_GPIO0_0	Bank 0	MCU_GPIO0_*_DATA	0		MCU_GPIO0_16	Bank 1	MCU_GPIO0_*_DATA	16
MCU_GPIO0_1	Bank 0	MCU_GPIO0_*_DATA	1		MCU_GPIO0_17	Bank 1	MCU_GPIO0_*_DATA	17

Signal	Bank	MCU_GPIO0_*_DATA	Register Bit		Signal	Bank	MCU_GPIO0_*_DATA	Register Bit
MCU_GPIO0_2	Bank 0	MCU_GPIO0_*_DATA	2		MCU_GPIO0_18	Bank 1	MCU_GPIO0_*_DATA	18
MCU_GPIO0_3	Bank 0	MCU_GPIO0_*_DATA	3		MCU_GPIO0_19	Bank 1	MCU_GPIO0_*_DATA	19
MCU_GPIO0_4	Bank 0	MCU_GPIO0_*_DATA	4		MCU_GPIO0_20	Bank 1	MCU_GPIO0_*_DATA	20
MCU_GPIO0_5	Bank 0	MCU_GPIO0_*_DATA	5		MCU_GPIO0_21	Bank 1	MCU_GPIO0_*_DATA	21
MCU_GPIO0_6	Bank 0	MCU_GPIO0_*_DATA	6		MCU_GPIO0_22	Bank 1	MCU_GPIO0_*_DATA	22
MCU_GPIO0_7	Bank 0	MCU_GPIO0_*_DATA	7		MCU_GPIO0_23	Bank 1	MCU_GPIO0_*_DATA	23
MCU_GPIO0_8	Bank 0	MCU_GPIO0_*_DATA	8					
MCU_GPIO0_9	Bank 0	MCU_GPIO0_*_DATA	9					
MCU_GPIO0_10	Bank 0	MCU_GPIO0_*_DATA	10					
MCU_GPIO0_11	Bank 0	MCU_GPIO0_*_DATA	11					
MCU_GPIO0_12	Bank 0	MCU_GPIO0_*_DATA	12					
MCU_GPIO0_13	Bank 0	MCU_GPIO0_*_DATA	13					
MCU_GPIO0_14	Bank 0	MCU_GPIO0_*_DATA	14					
MCU_GPIO0_15	Bank 0	MCU_GPIO0_*_DATA	15					

4.8.2 Inter-Integrated Circuit (I2C)

This section contains the integration details for the I2C module on this device. For further information, see the *Inter-Integrated Circuit (I2C)* section of the *Peripherals* chapter.

4.8.2.1 I2C Unsupported Features

The following features are not supported on this family of devices:

- Serial Camera Control Bus (SCCB) Protocol
- DMA Mode
- Full I^{2}C electrical compliance for I2C modules using device pins with LVCMOS voltage buffers (Refer to *Terminal Configuration and Functions* in Datasheet for details)
- High-speed (3.4-Mbps) operation for I2C modules using device pins with LVCMOS voltage buffers (Refer to *Terminal Configuration and Functions* in Datasheet for details)
- Debug suspend mode
- Asynchronous wakeup (via IO Daisy Chain) not supported by Main domain instances.

4.8.2.2 Module Allocations

Table 4-75. I2C Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
I2C0			✓
I2C1			✓
I2C2			✓
I2C3			✓
I2C4			✓
I2C5			✓
IC26			✓
WKUP_I2C0	✓		

4.8.2.3 Resets, Interrupts, and Clocks

Table 4-76. I2C Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
I2C0	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
I2C1	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
I2C2	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
I2C3	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
I2C4	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO

Table 4-76. I2C Integration Attributes (continued)

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
I2C5	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
I2C6	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
WKUP_I2C0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE

Table 4-77. I2C Resets

Module Instance	Source	Description
I2C0	MAIN_PSC0	I2C0 reset
I2C1	MAIN_PSC0	I2C1 reset
I2C2	MAIN_PSC0	I2C2 reset
I2C3	MAIN_PSC0	I2C3 reset
I2C4	MAIN_PSC0	I2C4 reset
I2C5	MAIN_PSC0	I2C5 reset
I2C6	MAIN_PSC0	I2C6 reset
WKUP_I2C0	MAIN_PSC0	WKUP_I2C0 reset

Table 4-78. I2C Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
I2C0	I2C0_pointrpend_0	C7X256V0_CLEC_gic_spi_IN_193	C7X256V0_CLEC	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	C7X256V1_CLEC_gic_spi_IN_193	C7X256V1_CLEC	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	R5FSS0_CORE0_intr_IN_193	R5FSS0_CORE0	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	R5FSS0_CORE1_intr_IN_193	R5FSS0_CORE1	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	R5FSS1_CORE0_intr_IN_193	R5FSS1_CORE0	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	R5FSS1_CORE1_intr_IN_193	R5FSS1_CORE1	I2C0 interrupt request	level
I2C0	I2C0_pointrpend_0	WKUP_R5FSS0_CORE0_intr_IN_193	WKUP_R5FSS0_CORE0	I2C0 interrupt request	level
I2C1	I2C1_pointrpend_0	C7X256V0_CLEC_gic_spi_IN_194	C7X256V0_CLEC	I2C1 interrupt request	level
I2C1	I2C1_pointrpend_0	C7X256V1_CLEC_gic_spi_IN_194	C7X256V1_CLEC	I2C1 interrupt request	level
I2C1	I2C1_pointrpend_0	R5FSS0_CORE0_intr_IN_194	R5FSS0_CORE0	I2C1 interrupt request	level

Table 4-78. I2C Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
I2C1	I2C1_pointrpend_0	R5FSS0_CORE1_intr_IN_194	R5FSS0_CORE1	I2C1 interrupt request	level
I2C1	I2C1_pointrpend_0	R5FSS1_CORE0_intr_IN_194	R5FSS1_CORE0	I2C1 interrupt request	level
I2C1	I2C1_pointrpend_0	R5FSS1_CORE1_intr_IN_194	R5FSS1_CORE1	I2C1 interrupt request	level
I2C1	I2C1_pointrpend_0	WKUP_R5FSS0_CORE0_intr_IN_194	WKUP_R5FSS0_CORE0	I2C1 interrupt request	level
I2C2	I2C2_pointrpend_0	C7X256V0_CLEC_gic_spi_IN_195	C7X256V0_CLEC	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	C7X256V1_CLEC_gic_spi_IN_195	C7X256V1_CLEC	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	R5FSS0_CORE0_intr_IN_195	R5FSS0_CORE0	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	R5FSS0_CORE1_intr_IN_195	R5FSS0_CORE1	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	R5FSS1_CORE0_intr_IN_195	R5FSS1_CORE0	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	R5FSS1_CORE1_intr_IN_195	R5FSS1_CORE1	I2C2 interrupt request	level
I2C2	I2C2_pointrpend_0	WKUP_R5FSS0_CORE0_intr_IN_195	WKUP_R5FSS0_CORE0	I2C2 interrupt request	level
I2C3	I2C3_pointrpend_0	C7X256V0_CLEC_gic_spi_IN_196	C7X256V0_CLEC	I2C3 interrupt request	level
I2C3	I2C3_pointrpend_0	C7X256V1_CLEC_gic_spi_IN_196	C7X256V1_CLEC	I2C3 interrupt request	level
I2C3	I2C3_pointrpend_0	R5FSS0_CORE0_intr_IN_196	R5FSS0_CORE0	I2C3 interrupt request	level
I2C3	I2C3_pointrpend_0	R5FSS0_CORE1_intr_IN_196	R5FSS0_CORE1	I2C3 interrupt request	level
I2C3	I2C3_pointrpend_0	R5FSS1_CORE0_intr_IN_196	R5FSS1_CORE0	I2C3 interrupt request	level
I2C3	I2C3_pointrpend_0	R5FSS1_CORE1_intr_IN_196	R5FSS1_CORE1	I2C3 interrupt request	level
I2C3	I2C3_pointrpend_0	WKUP_R5FSS0_CORE0_intr_IN_196	WKUP_R5FSS0_CORE0	I2C3 interrupt request	level
I2C4	I2C4_pointrpend_0	R5FSS0_CORE0_intr_IN_197	R5FSS0_CORE0	I2C4 interrupt request	level
I2C4	I2C4_pointrpend_0	R5FSS0_CORE1_intr_IN_197	R5FSS0_CORE1	I2C4 interrupt request	level
I2C4	I2C4_pointrpend_0	R5FSS1_CORE0_intr_IN_197	R5FSS1_CORE0	I2C4 interrupt request	level
I2C4	I2C4_pointrpend_0	R5FSS1_CORE1_intr_IN_197	R5FSS1_CORE1	I2C4 interrupt request	level

Table 4-78. I2C Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
I2C4	I2C4_pointrpend_0	WKUP_R5FSS0_CORE0_intr_IN_197	WKUP_R5FSS0_CORE0	I2C4 interrupt request	level
I2C5	I2C5_pointrpend_0	R5FSS0_CORE0_intr_IN_198	R5FSS0_CORE0	I2C5 interrupt request	level
I2C5	I2C5_pointrpend_0	R5FSS0_CORE1_intr_IN_198	R5FSS0_CORE1	I2C5 interrupt request	level
I2C5	I2C5_pointrpend_0	R5FSS1_CORE0_intr_IN_198	R5FSS1_CORE0	I2C5 interrupt request	level
I2C5	I2C5_pointrpend_0	R5FSS1_CORE1_intr_IN_198	R5FSS1_CORE1	I2C5 interrupt request	level
I2C5	I2C5_pointrpend_0	WKUP_R5FSS0_CORE0_intr_IN_198	WKUP_R5FSS0_CORE0	I2C5 interrupt request	level
I2C6	I2C6_pointrpend_0	R5FSS0_CORE0_intr_IN_199	R5FSS0_CORE0	I2C6 interrupt request	level
I2C6	I2C6_pointrpend_0	R5FSS0_CORE1_intr_IN_199	R5FSS0_CORE1	I2C6 interrupt request	level
I2C6	I2C6_pointrpend_0	R5FSS1_CORE0_intr_IN_199	R5FSS1_CORE0	I2C6 interrupt request	level
I2C6	I2C6_pointrpend_0	R5FSS1_CORE1_intr_IN_199	R5FSS1_CORE1	I2C6 interrupt request	level
I2C6	I2C6_pointrpend_0	WKUP_R5FSS0_CORE0_intr_IN_199	WKUP_R5FSS0_CORE0	I2C6 interrupt request	level
WKUP_I2C0	WKUP_I2C0_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_IN_143	WKUP_R5FSS0_CORE0	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	C7X256V0_CLEC_gic_spi_IN_197	C7X256V0_CLEC	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	C7X256V1_CLEC_gic_spi_IN_197	C7X256V1_CLEC	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	R5FSS0_CORE0_intr_IN_190	R5FSS0_CORE0	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	R5FSS0_CORE1_intr_IN_190	R5FSS0_CORE1	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	R5FSS1_CORE0_intr_IN_190	R5FSS1_CORE0	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	R5FSS1_CORE1_intr_IN_190	R5FSS1_CORE1	WKUP_I2C0 interrupt request	level
WKUP_I2C0	WKUP_I2C0_pointrpend_0	WKUP_R5FSS0_CORE0_intr_IN_190	WKUP_R5FSS0_CORE0	WKUP_I2C0 interrupt request	level

Table 4-79. I2C Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
I2C0	OCP_CLK	MAIN_SYSCLK0/4		I2C0 Interface Clock
	SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2		I2C0 Functional Clock

Table 4-79. I2C Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
I2C1	OCP_CLK	MAIN_SYSCLK0/4		I2C1 Interface Clock
	SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2		I2C1 Functional Clock
I2C2	OCP_CLK	MAIN_SYSCLK0/4		I2C2 Interface Clock
	SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2		I2C2 Functional Clock
I2C3	OCP_CLK	MAIN_SYSCLK0/4		I2C3 Interface Clock
	SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2		I2C3 Functional Clock
I2C4	OCP_CLK	MAIN_SYSCLK0/4		I2C4 Interface Clock
	SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2		I2C4 Functional Clock
I2C5	OCP_CLK	MAIN_SYSCLK0/4		I2C5 Interface Clock
	SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2		I2C5 Functional Clock
I2C6	OCP_CLK	MAIN_SYSCLK0/4		I2C6 Interface Clock
	SYS_CLK	MAIN_PLL1_HSDIV0_CLKOUT/2		I2C6 Functional Clock
WKUP_I2C0	OCP_CLK	DM_CLK/4	WKUP_CLKSEL[0:0]	WKUP_I2C0 Interface Clock
	SYS_CLK	MCU_PLL0_HSDIV1_CLKOUT		WKUP_I2C0 Functional Clock

4.8.2.4 I2C Additional Integration Details

Additional Integration Details for I2C.

I2C HS Mode

The MCU_I2C0 and WKUP_I2C0 IOs are a special IIC Open Drain Cell I2C_OD_FS. This cell supports I2C High Speed Mode when operating at 1.8V. (Note: At 3.3V the IO does not operate in HS Mode

4.8.3 Multichannel Serial Peripheral Interface (MCSPI)

This section contains the integration details for the MCSPI module on this device. For further information, see the *Multichannel Serial Peripheral Interface (MCSPI)* section of the *Peripherals* chapter.

4.8.3.1 MCSPI Unsupported Features

The following features are not supported on this family of devices:

- Peripheral mode wakeup.
- Retention during power down

4.8.3.2 Module Allocations

Table 4-80. MCSPI Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
MCSPI0			✓
MCSPI1			✓
MCSPI2			✓
MCSPI3			✓
MCSPI4			✓

4.8.3.3 Resets, Interrupts, and Clocks

Table 4-81. MCSPI Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCSPI0	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
MCSPI1	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
MCSPI2	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
MCSPI3	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
MCSPI4	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO

Table 4-82. MCSPI Resets

Module Instance	Source	Description
MCSPI0	MAIN_PSC0	MCSPI0 reset
MCSPI1	MAIN_PSC0	MCSPI1 reset
MCSPI2	MAIN_PSC0	MCSPI2 reset
MCSPI3	MAIN_PSC0	MCSPI3 reset
MCSPI4	MAIN_PSC0	MCSPI4 reset

Table 4-83. MCSPI Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI0	MCSPI0_dma_read_event_0	PDMA0_spi_main_0_rx_IN_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_0	PDMA0_spi_main_0_rx_IN_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_0	PDMA0_spi_main_0_rx_IN_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_0	PDMA0_spi_main_0_rx_IN_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_1	PDMA0_spi_main_0_rx_IN_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_1	PDMA0_spi_main_0_rx_IN_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_1	PDMA0_spi_main_0_rx_IN_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_1	PDMA0_spi_main_0_rx_IN_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_2	PDMA0_spi_main_0_rx_IN_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_2	PDMA0_spi_main_0_rx_IN_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_2	PDMA0_spi_main_0_rx_IN_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_2	PDMA0_spi_main_0_rx_IN_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_3	PDMA0_spi_main_0_rx_IN_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_3	PDMA0_spi_main_0_rx_IN_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_3	PDMA0_spi_main_0_rx_IN_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_read_event_3	PDMA0_spi_main_0_rx_IN_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_0	PDMA0_spi_main_0_tx_IN_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_0	PDMA0_spi_main_0_tx_IN_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_0	PDMA0_spi_main_0_tx_IN_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_0	PDMA0_spi_main_0_tx_IN_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_1	PDMA0_spi_main_0_tx_IN_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_1	PDMA0_spi_main_0_tx_IN_1	PDMA0	MCSPI0 interrupt request	pulse

Table 4-83. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI0	MCSPI0_dma_write_event_1	PDMA0_spi_main_0_tx_IN_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_1	PDMA0_spi_main_0_tx_IN_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_2	PDMA0_spi_main_0_tx_IN_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_2	PDMA0_spi_main_0_tx_IN_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_2	PDMA0_spi_main_0_tx_IN_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_2	PDMA0_spi_main_0_tx_IN_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_3	PDMA0_spi_main_0_tx_IN_0	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_3	PDMA0_spi_main_0_tx_IN_1	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_3	PDMA0_spi_main_0_tx_IN_2	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_dma_write_event_3	PDMA0_spi_main_0_tx_IN_3	PDMA0	MCSPI0 interrupt request	pulse
MCSPI0	MCSPI0_intr_spi_0	C7X256V0_CLEC_gic_spi_IN_204	C7X256V0_CLEC	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	C7X256V1_CLEC_gic_spi_IN_204	C7X256V1_CLEC	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	R5FSS0_CORE0_intr_IN_204	R5FSS0_CORE0	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	R5FSS0_CORE1_intr_IN_204	R5FSS0_CORE1	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	R5FSS1_CORE0_intr_IN_204	R5FSS1_CORE0	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	R5FSS1_CORE1_intr_IN_204	R5FSS1_CORE1	MCSPI0 interrupt request	level
MCSPI0	MCSPI0_intr_spi_0	WKUP_R5FSS0_CORE0_intr_IN_204	WKUP_R5FSS0_CORE0	MCSPI0 interrupt request	level
MCSPI1	MCSPI1_dma_read_event_0	PDMA0_spi_main_1_rx_IN_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_0	PDMA0_spi_main_1_rx_IN_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_0	PDMA0_spi_main_1_rx_IN_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_0	PDMA0_spi_main_1_rx_IN_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_1	PDMA0_spi_main_1_rx_IN_0	PDMA0	MCSPI1 interrupt request	pulse

Table 4-83. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI1	MCSPI1_dma_read_event_1	PDMA0_spi_main_1_rx_IN_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_1	PDMA0_spi_main_1_rx_IN_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_1	PDMA0_spi_main_1_rx_IN_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_2	PDMA0_spi_main_1_rx_IN_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_2	PDMA0_spi_main_1_rx_IN_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_2	PDMA0_spi_main_1_rx_IN_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_2	PDMA0_spi_main_1_rx_IN_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_3	PDMA0_spi_main_1_rx_IN_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_3	PDMA0_spi_main_1_rx_IN_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_3	PDMA0_spi_main_1_rx_IN_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_read_event_3	PDMA0_spi_main_1_rx_IN_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_0	PDMA0_spi_main_1_tx_IN_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_0	PDMA0_spi_main_1_tx_IN_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_0	PDMA0_spi_main_1_tx_IN_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_0	PDMA0_spi_main_1_tx_IN_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_1	PDMA0_spi_main_1_tx_IN_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_1	PDMA0_spi_main_1_tx_IN_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_1	PDMA0_spi_main_1_tx_IN_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_1	PDMA0_spi_main_1_tx_IN_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_2	PDMA0_spi_main_1_tx_IN_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_2	PDMA0_spi_main_1_tx_IN_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_2	PDMA0_spi_main_1_tx_IN_2	PDMA0	MCSPI1 interrupt request	pulse

Table 4-83. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI1	MCSPI1_dma_write_event_2	PDMA0_spi_main_1_tx_IN_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_3	PDMA0_spi_main_1_tx_IN_0	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_3	PDMA0_spi_main_1_tx_IN_1	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_3	PDMA0_spi_main_1_tx_IN_2	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_dma_write_event_3	PDMA0_spi_main_1_tx_IN_3	PDMA0	MCSPI1 interrupt request	pulse
MCSPI1	MCSPI1_intr_spi_0	C7X256V0_CLEC_gic_spi_IN_205	C7X256V0_CLEC	MCSPI1 interrupt request	level
MCSPI1	MCSPI1_intr_spi_0	C7X256V1_CLEC_gic_spi_IN_205	C7X256V1_CLEC	MCSPI1 interrupt request	level
MCSPI1	MCSPI1_intr_spi_0	R5FSS0_CORE0_intr_IN_205	R5FSS0_CORE0	MCSPI1 interrupt request	level
MCSPI1	MCSPI1_intr_spi_0	R5FSS0_CORE1_intr_IN_205	R5FSS0_CORE1	MCSPI1 interrupt request	level
MCSPI1	MCSPI1_intr_spi_0	R5FSS1_CORE0_intr_IN_205	R5FSS1_CORE0	MCSPI1 interrupt request	level
MCSPI1	MCSPI1_intr_spi_0	R5FSS1_CORE1_intr_IN_205	R5FSS1_CORE1	MCSPI1 interrupt request	level
MCSPI1	MCSPI1_intr_spi_0	WKUP_R5FSS0_CORE0_intr_IN_205	WKUP_R5FSS0_CORE0	MCSPI1 interrupt request	level
MCSPI2	MCSPI2_dma_read_event_0	PDMA0_spi_main_2_rx_IN_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_0	PDMA0_spi_main_2_rx_IN_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_0	PDMA0_spi_main_2_rx_IN_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_0	PDMA0_spi_main_2_rx_IN_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_1	PDMA0_spi_main_2_rx_IN_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_1	PDMA0_spi_main_2_rx_IN_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_1	PDMA0_spi_main_2_rx_IN_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_1	PDMA0_spi_main_2_rx_IN_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_2	PDMA0_spi_main_2_rx_IN_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_2	PDMA0_spi_main_2_rx_IN_1	PDMA0	MCSPI2 interrupt request	pulse

Table 4-83. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI2	MCSPI2_dma_read_event_2	PDMA0_spi_main_2_rx_IN_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_2	PDMA0_spi_main_2_rx_IN_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_3	PDMA0_spi_main_2_rx_IN_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_3	PDMA0_spi_main_2_rx_IN_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_3	PDMA0_spi_main_2_rx_IN_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_read_event_3	PDMA0_spi_main_2_rx_IN_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_0	PDMA0_spi_main_2_tx_IN_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_0	PDMA0_spi_main_2_tx_IN_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_0	PDMA0_spi_main_2_tx_IN_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_0	PDMA0_spi_main_2_tx_IN_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_1	PDMA0_spi_main_2_tx_IN_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_1	PDMA0_spi_main_2_tx_IN_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_1	PDMA0_spi_main_2_tx_IN_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_1	PDMA0_spi_main_2_tx_IN_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_2	PDMA0_spi_main_2_tx_IN_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_2	PDMA0_spi_main_2_tx_IN_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_2	PDMA0_spi_main_2_tx_IN_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_2	PDMA0_spi_main_2_tx_IN_3	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_3	PDMA0_spi_main_2_tx_IN_0	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_3	PDMA0_spi_main_2_tx_IN_1	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_3	PDMA0_spi_main_2_tx_IN_2	PDMA0	MCSPI2 interrupt request	pulse
MCSPI2	MCSPI2_dma_write_event_3	PDMA0_spi_main_2_tx_IN_3	PDMA0	MCSPI2 interrupt request	pulse

Table 4-83. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI2	MCSPI2_intr_spi_0	C7X256V0_CLEC_gic_spi_IN_206	C7X256V0_CLEC	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	C7X256V1_CLEC_gic_spi_IN_206	C7X256V1_CLEC	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	R5FSS0_CORE0_intr_IN_206	R5FSS0_CORE0	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	R5FSS0_CORE1_intr_IN_206	R5FSS0_CORE1	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	R5FSS1_CORE0_intr_IN_206	R5FSS1_CORE0	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	R5FSS1_CORE1_intr_IN_206	R5FSS1_CORE1	MCSPI2 interrupt request	level
MCSPI2	MCSPI2_intr_spi_0	WKUP_R5FSS0_CORE0_intr_IN_206	WKUP_R5FSS0_CORE0	MCSPI2 interrupt request	level
MCSPI3	MCSPI3_dma_read_event_0	PDMA4_spi_main_3_rx_IN_0	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_0	PDMA4_spi_main_3_rx_IN_1	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_0	PDMA4_spi_main_3_rx_IN_2	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_0	PDMA4_spi_main_3_rx_IN_3	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_1	PDMA4_spi_main_3_rx_IN_0	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_1	PDMA4_spi_main_3_rx_IN_1	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_1	PDMA4_spi_main_3_rx_IN_2	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_1	PDMA4_spi_main_3_rx_IN_3	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_2	PDMA4_spi_main_3_rx_IN_0	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_2	PDMA4_spi_main_3_rx_IN_1	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_2	PDMA4_spi_main_3_rx_IN_2	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_2	PDMA4_spi_main_3_rx_IN_3	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_3	PDMA4_spi_main_3_rx_IN_0	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_3	PDMA4_spi_main_3_rx_IN_1	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_read_event_3	PDMA4_spi_main_3_rx_IN_2	PDMA4	MCSPI3 interrupt request	pulse

Table 4-83. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI3	MCSPI3_dma_read_event_3	PDMA4_spi_main_3_rx_IN_3	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_0	PDMA4_spi_main_3_tx_IN_0	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_0	PDMA4_spi_main_3_tx_IN_1	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_0	PDMA4_spi_main_3_tx_IN_2	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_0	PDMA4_spi_main_3_tx_IN_3	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_1	PDMA4_spi_main_3_tx_IN_0	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_1	PDMA4_spi_main_3_tx_IN_1	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_1	PDMA4_spi_main_3_tx_IN_2	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_1	PDMA4_spi_main_3_tx_IN_3	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_2	PDMA4_spi_main_3_tx_IN_0	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_2	PDMA4_spi_main_3_tx_IN_1	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_2	PDMA4_spi_main_3_tx_IN_2	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_2	PDMA4_spi_main_3_tx_IN_3	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_3	PDMA4_spi_main_3_tx_IN_0	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_3	PDMA4_spi_main_3_tx_IN_1	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_3	PDMA4_spi_main_3_tx_IN_2	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_dma_write_event_3	PDMA4_spi_main_3_tx_IN_3	PDMA4	MCSPI3 interrupt request	pulse
MCSPI3	MCSPI3_intr_spi_0	C7X256V0_CLEC_gic_spi_IN_207	C7X256V0_CLEC	MCSPI3 interrupt request	level
MCSPI3	MCSPI3_intr_spi_0	C7X256V1_CLEC_gic_spi_IN_207	C7X256V1_CLEC	MCSPI3 interrupt request	level
MCSPI3	MCSPI3_intr_spi_0	R5FSS0_CORE0_intr_IN_207	R5FSS0_CORE0	MCSPI3 interrupt request	level
MCSPI3	MCSPI3_intr_spi_0	R5FSS0_CORE1_intr_IN_207	R5FSS0_CORE1	MCSPI3 interrupt request	level
MCSPI3	MCSPI3_intr_spi_0	R5FSS1_CORE0_intr_IN_207	R5FSS1_CORE0	MCSPI3 interrupt request	level

Table 4-83. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI3	MCSPI3_intr_spi_0	R5FSS1_CORE1_intr_IN_207	R5FSS1_CORE1	MCSPI3 interrupt request	level
MCSPI3	MCSPI3_intr_spi_0	WKUP_R5FSS0_CORE0_intr_IN_207	WKUP_R5FSS0_CORE0	MCSPI3 interrupt request	level
MCSPI4	MCSPI4_dma_read_event_0	PDMA4_spi_main_4_rx_IN_0	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_0	PDMA4_spi_main_4_rx_IN_1	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_0	PDMA4_spi_main_4_rx_IN_2	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_0	PDMA4_spi_main_4_rx_IN_3	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_1	PDMA4_spi_main_4_rx_IN_0	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_1	PDMA4_spi_main_4_rx_IN_1	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_1	PDMA4_spi_main_4_rx_IN_2	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_1	PDMA4_spi_main_4_rx_IN_3	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_2	PDMA4_spi_main_4_rx_IN_0	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_2	PDMA4_spi_main_4_rx_IN_1	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_2	PDMA4_spi_main_4_rx_IN_2	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_2	PDMA4_spi_main_4_rx_IN_3	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_3	PDMA4_spi_main_4_rx_IN_0	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_3	PDMA4_spi_main_4_rx_IN_1	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_3	PDMA4_spi_main_4_rx_IN_2	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_read_event_3	PDMA4_spi_main_4_rx_IN_3	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_0	PDMA4_spi_main_4_tx_IN_0	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_0	PDMA4_spi_main_4_tx_IN_1	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_0	PDMA4_spi_main_4_tx_IN_2	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_0	PDMA4_spi_main_4_tx_IN_3	PDMA4	MCSPI4 interrupt request	pulse

Table 4-83. MCSPI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCSPI4	MCSPI4_dma_write_event_1	PDMA4_spi_main_4_tx_IN_0	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_1	PDMA4_spi_main_4_tx_IN_1	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_1	PDMA4_spi_main_4_tx_IN_2	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_1	PDMA4_spi_main_4_tx_IN_3	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_2	PDMA4_spi_main_4_tx_IN_0	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_2	PDMA4_spi_main_4_tx_IN_1	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_2	PDMA4_spi_main_4_tx_IN_2	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_2	PDMA4_spi_main_4_tx_IN_3	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_3	PDMA4_spi_main_4_tx_IN_0	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_3	PDMA4_spi_main_4_tx_IN_1	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_3	PDMA4_spi_main_4_tx_IN_2	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_dma_write_event_3	PDMA4_spi_main_4_tx_IN_3	PDMA4	MCSPI4 interrupt request	pulse
MCSPI4	MCSPI4_intr_spi_0	C7X256V0_CLEC_gic_spi_IN_208	C7X256V0_CLEC	MCSPI4 interrupt request	level
MCSPI4	MCSPI4_intr_spi_0	C7X256V1_CLEC_gic_spi_IN_208	C7X256V1_CLEC	MCSPI4 interrupt request	level
MCSPI4	MCSPI4_intr_spi_0	R5FSS0_CORE0_intr_IN_208	R5FSS0_CORE0	MCSPI4 interrupt request	level
MCSPI4	MCSPI4_intr_spi_0	R5FSS0_CORE1_intr_IN_208	R5FSS0_CORE1	MCSPI4 interrupt request	level
MCSPI4	MCSPI4_intr_spi_0	R5FSS1_CORE0_intr_IN_208	R5FSS1_CORE0	MCSPI4 interrupt request	level
MCSPI4	MCSPI4_intr_spi_0	R5FSS1_CORE1_intr_IN_208	R5FSS1_CORE1	MCSPI4 interrupt request	level
MCSPI4	MCSPI4_intr_spi_0	WKUP_R5FSS0_CORE0_intr_IN_208	WKUP_R5FSS0_CORE0	MCSPI4 interrupt request	level

Table 4-84. MCSPI Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCSPI0	FCLK	MAIN_PLL2_HSDIV5_CLKOUT/10		MCSPI0 Functional Clock
	IO_CLKSPII_CLK	MAIN_PLL2_HSDIV5_CLKOUT/10		
		MAIN_PBIST_CLK		
		MAIN_SYSCLK0/4		
	ICLK	MAIN_SYSCLK0/4		MCSPI0 Interface Clock
MCSPI1	FCLK	MAIN_PLL2_HSDIV5_CLKOUT/10		MCSPI1 Functional Clock
	IO_CLKSPII_CLK	MAIN_PLL2_HSDIV5_CLKOUT/10		
		MAIN_PBIST_CLK		
		MAIN_SYSCLK0/4		
	ICLK	MAIN_SYSCLK0/4		MCSPI1 Interface Clock
MCSPI2	FCLK	MAIN_PLL2_HSDIV5_CLKOUT/10		MCSPI2 Functional Clock
	IO_CLKSPII_CLK	MAIN_PLL2_HSDIV5_CLKOUT/10		
		MAIN_PBIST_CLK		
		MAIN_SYSCLK0/4		
	ICLK	MAIN_SYSCLK0/4		MCSPI2 Interface Clock
MCSPI3	FCLK	MAIN_PLL2_HSDIV5_CLKOUT/10		MCSPI3 Functional Clock
	IO_CLKSPII_CLK	MAIN_PLL2_HSDIV5_CLKOUT/10		
		MAIN_PBIST_CLK		
		MAIN_SYSCLK0/4		
	ICLK	MAIN_SYSCLK0/4		MCSPI3 Interface Clock
MCSPI4	FCLK	MAIN_PLL2_HSDIV5_CLKOUT/10		MCSPI4 Functional Clock
	IO_CLKSPII_CLK	MAIN_PLL2_HSDIV5_CLKOUT/10		
		MAIN_PBIST_CLK		
		MAIN_SYSCLK0/4		
	ICLK	MAIN_SYSCLK0/4		MCSPI4 Interface Clock

4.8.4 Universal Asynchronous Receiver/Transmitter (UART)

This section contains the integration details for the UART module on this device. For further information, see the *Universal Asynchronous Receiver/Transmitter (UART)* section of the *Peripherals* chapter.

4.8.4.1 UART Unsupported Features

The following features are not supported on this family of devices:

- 12Mbps not supported for WKUP_UART instances
- Full modem handshaking is not available on all instances. See device datasheet for instances supporting full modem handshaking.
- Synchronous mode - SCLK not pinned out
- ISO7816 Mode
- SCR DMA Mode 2
- Multi-drop Transmission
- 9-bit Mode

4.8.4.2 Module Allocations

Table 4-85. UART Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
UART0			✓
UART1			✓
UART2			✓
UART3			✓
UART4			✓
UART5			✓
UART6			✓
WKUP_UART0	✓		

4.8.4.3 Resets, Interrupts, and Clocks

Table 4-86. UART Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
UART0	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
UART1	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
UART2	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
UART3	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
UART4	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO

Table 4-86. UART Integration Attributes (continued)

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
UART5	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
UART6	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
WKUP_UART0	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO

Table 4-87. UART Resets

Module Instance	Source	Description
UART0	MAIN_PSC0	UART0 reset
UART1	MAIN_PSC0	UART1 reset
UART2	MAIN_PSC0	UART2 reset
UART3	MAIN_PSC0	UART3 reset
UART4	MAIN_PSC0	UART4 reset
UART5	MAIN_PSC0	UART5 reset
UART6	MAIN_PSC0	UART6 reset
WKUP_UART0	MAIN_PSC0	WKUP_UART0 reset

Table 4-88. UART Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART0	UART0_usart_dma_0	PDMA1_usart_main_0_rx_IN_0	PDMA1	UART0 interrupt request	level
UART0	UART0_usart_dma_0	PDMA1_usart_main_0_tx_IN_0	PDMA1	UART0 interrupt request	level
UART0	UART0_usart_dma_1	PDMA1_usart_main_0_rx_IN_0	PDMA1	UART0 interrupt request	level
UART0	UART0_usart_dma_1	PDMA1_usart_main_0_tx_IN_0	PDMA1	UART0 interrupt request	level
UART0	UART0_usart_irq_0	C7X256V0_CLEC_gic_spi_IN_210	C7X256V0_CLEC	UART0 interrupt request	level
UART0	UART0_usart_irq_0	C7X256V1_CLEC_gic_spi_IN_210	C7X256V1_CLEC	UART0 interrupt request	level
UART0	UART0_usart_irq_0	R5FSS0_CORE0_intr_IN_210	R5FSS0_CORE0	UART0 interrupt request	level
UART0	UART0_usart_irq_0	R5FSS0_CORE1_intr_IN_210	R5FSS0_CORE1	UART0 interrupt request	level
UART0	UART0_usart_irq_0	R5FSS1_CORE0_intr_IN_210	R5FSS1_CORE0	UART0 interrupt request	level
UART0	UART0_usart_irq_0	R5FSS1_CORE1_intr_IN_210	R5FSS1_CORE1	UART0 interrupt request	level

Table 4-88. UART Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART0	UART0_usart_irq_0	WKUP_R5FSS0_CORE0_intr_IN_210	WKUP_R5FSS0_CORE0	UART0 interrupt request	level
UART1	UART1_usart_dma_0	PDMA1_usart_main_1_rx_IN_0	PDMA1	UART1 interrupt request	level
UART1	UART1_usart_dma_0	PDMA1_usart_main_1_tx_IN_0	PDMA1	UART1 interrupt request	level
UART1	UART1_usart_dma_1	PDMA1_usart_main_1_rx_IN_0	PDMA1	UART1 interrupt request	level
UART1	UART1_usart_dma_1	PDMA1_usart_main_1_tx_IN_0	PDMA1	UART1 interrupt request	level
UART1	UART1_usart_irq_0	C7X256V0_CLEC_gic_spi_IN_211	C7X256V0_CLEC	UART1 interrupt request	level
UART1	UART1_usart_irq_0	C7X256V1_CLEC_gic_spi_IN_211	C7X256V1_CLEC	UART1 interrupt request	level
UART1	UART1_usart_irq_0	R5FSS0_CORE0_intr_IN_211	R5FSS0_CORE0	UART1 interrupt request	level
UART1	UART1_usart_irq_0	R5FSS0_CORE1_intr_IN_211	R5FSS0_CORE1	UART1 interrupt request	level
UART1	UART1_usart_irq_0	R5FSS1_CORE0_intr_IN_211	R5FSS1_CORE0	UART1 interrupt request	level
UART1	UART1_usart_irq_0	R5FSS1_CORE1_intr_IN_211	R5FSS1_CORE1	UART1 interrupt request	level
UART1	UART1_usart_irq_0	WKUP_R5FSS0_CORE0_intr_IN_211	WKUP_R5FSS0_CORE0	UART1 interrupt request	level
UART2	UART2_usart_dma_0	PDMA1_usart_main_2_rx_IN_0	PDMA1	UART2 interrupt request	level
UART2	UART2_usart_dma_0	PDMA1_usart_main_2_tx_IN_0	PDMA1	UART2 interrupt request	level
UART2	UART2_usart_dma_1	PDMA1_usart_main_2_rx_IN_0	PDMA1	UART2 interrupt request	level
UART2	UART2_usart_dma_1	PDMA1_usart_main_2_tx_IN_0	PDMA1	UART2 interrupt request	level
UART2	UART2_usart_irq_0	C7X256V0_CLEC_gic_spi_IN_212	C7X256V0_CLEC	UART2 interrupt request	level
UART2	UART2_usart_irq_0	C7X256V1_CLEC_gic_spi_IN_212	C7X256V1_CLEC	UART2 interrupt request	level
UART2	UART2_usart_irq_0	R5FSS0_CORE0_intr_IN_212	R5FSS0_CORE0	UART2 interrupt request	level
UART2	UART2_usart_irq_0	R5FSS0_CORE1_intr_IN_212	R5FSS0_CORE1	UART2 interrupt request	level
UART2	UART2_usart_irq_0	R5FSS1_CORE0_intr_IN_212	R5FSS1_CORE0	UART2 interrupt request	level
UART2	UART2_usart_irq_0	R5FSS1_CORE1_intr_IN_212	R5FSS1_CORE1	UART2 interrupt request	level

Table 4-88. UART Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART2	UART2_usart_irq_0	WKUP_R5FSS0_CORE0_intr_IN_212	WKUP_R5FSS0_CORE0	UART2 interrupt request	level
UART3	UART3_usart_dma_0	PDMA1_usart_main_3_rx_IN_0	PDMA1	UART3 interrupt request	level
UART3	UART3_usart_dma_0	PDMA1_usart_main_3_tx_IN_0	PDMA1	UART3 interrupt request	level
UART3	UART3_usart_dma_1	PDMA1_usart_main_3_rx_IN_0	PDMA1	UART3 interrupt request	level
UART3	UART3_usart_dma_1	PDMA1_usart_main_3_tx_IN_0	PDMA1	UART3 interrupt request	level
UART3	UART3_usart_irq_0	C7X256V0_CLEC_gic_spi_IN_213	C7X256V0_CLEC	UART3 interrupt request	level
UART3	UART3_usart_irq_0	C7X256V1_CLEC_gic_spi_IN_213	C7X256V1_CLEC	UART3 interrupt request	level
UART3	UART3_usart_irq_0	R5FSS0_CORE0_intr_IN_213	R5FSS0_CORE0	UART3 interrupt request	level
UART3	UART3_usart_irq_0	R5FSS0_CORE1_intr_IN_213	R5FSS0_CORE1	UART3 interrupt request	level
UART3	UART3_usart_irq_0	R5FSS1_CORE0_intr_IN_213	R5FSS1_CORE0	UART3 interrupt request	level
UART3	UART3_usart_irq_0	R5FSS1_CORE1_intr_IN_213	R5FSS1_CORE1	UART3 interrupt request	level
UART3	UART3_usart_irq_0	WKUP_R5FSS0_CORE0_intr_IN_213	WKUP_R5FSS0_CORE0	UART3 interrupt request	level
UART4	UART4_usart_dma_0	PDMA1_usart_main_4_rx_IN_0	PDMA1	UART4 interrupt request	level
UART4	UART4_usart_dma_0	PDMA1_usart_main_4_tx_IN_0	PDMA1	UART4 interrupt request	level
UART4	UART4_usart_dma_1	PDMA1_usart_main_4_rx_IN_0	PDMA1	UART4 interrupt request	level
UART4	UART4_usart_dma_1	PDMA1_usart_main_4_tx_IN_0	PDMA1	UART4 interrupt request	level
UART4	UART4_usart_irq_0	C7X256V0_CLEC_gic_spi_IN_214	C7X256V0_CLEC	UART4 interrupt request	level
UART4	UART4_usart_irq_0	C7X256V1_CLEC_gic_spi_IN_214	C7X256V1_CLEC	UART4 interrupt request	level
UART4	UART4_usart_irq_0	R5FSS0_CORE0_intr_IN_214	R5FSS0_CORE0	UART4 interrupt request	level
UART4	UART4_usart_irq_0	R5FSS0_CORE1_intr_IN_214	R5FSS0_CORE1	UART4 interrupt request	level
UART4	UART4_usart_irq_0	R5FSS1_CORE0_intr_IN_214	R5FSS1_CORE0	UART4 interrupt request	level
UART4	UART4_usart_irq_0	R5FSS1_CORE1_intr_IN_214	R5FSS1_CORE1	UART4 interrupt request	level

Table 4-88. UART Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART4	UART4_usart_irq_0	WKUP_R5FSS0_CORE0_intr_IN_214	WKUP_R5FSS0_CORE0	UART4 interrupt request	level
UART5	UART5_usart_dma_0	PDMA1_usart_main_5_rx_IN_0	PDMA1	UART5 interrupt request	level
UART5	UART5_usart_dma_0	PDMA1_usart_main_5_tx_IN_0	PDMA1	UART5 interrupt request	level
UART5	UART5_usart_dma_1	PDMA1_usart_main_5_rx_IN_0	PDMA1	UART5 interrupt request	level
UART5	UART5_usart_dma_1	PDMA1_usart_main_5_tx_IN_0	PDMA1	UART5 interrupt request	level
UART5	UART5_usart_irq_0	C7X256V0_CLEC_gic_spi_IN_215	C7X256V0_CLEC	UART5 interrupt request	level
UART5	UART5_usart_irq_0	C7X256V1_CLEC_gic_spi_IN_215	C7X256V1_CLEC	UART5 interrupt request	level
UART5	UART5_usart_irq_0	R5FSS0_CORE0_intr_IN_215	R5FSS0_CORE0	UART5 interrupt request	level
UART5	UART5_usart_irq_0	R5FSS0_CORE1_intr_IN_215	R5FSS0_CORE1	UART5 interrupt request	level
UART5	UART5_usart_irq_0	R5FSS1_CORE0_intr_IN_215	R5FSS1_CORE0	UART5 interrupt request	level
UART5	UART5_usart_irq_0	R5FSS1_CORE1_intr_IN_215	R5FSS1_CORE1	UART5 interrupt request	level
UART5	UART5_usart_irq_0	WKUP_R5FSS0_CORE0_intr_IN_215	WKUP_R5FSS0_CORE0	UART5 interrupt request	level
UART6	UART6_usart_dma_0	PDMA1_usart_main_6_rx_IN_0	PDMA1	UART6 interrupt request	level
UART6	UART6_usart_dma_0	PDMA1_usart_main_6_tx_IN_0	PDMA1	UART6 interrupt request	level
UART6	UART6_usart_dma_1	PDMA1_usart_main_6_rx_IN_0	PDMA1	UART6 interrupt request	level
UART6	UART6_usart_dma_1	PDMA1_usart_main_6_tx_IN_0	PDMA1	UART6 interrupt request	level
UART6	UART6_usart_irq_0	C7X256V0_CLEC_gic_spi_IN_216	C7X256V0_CLEC	UART6 interrupt request	level
UART6	UART6_usart_irq_0	C7X256V1_CLEC_gic_spi_IN_216	C7X256V1_CLEC	UART6 interrupt request	level
UART6	UART6_usart_irq_0	R5FSS0_CORE0_intr_IN_216	R5FSS0_CORE0	UART6 interrupt request	level
UART6	UART6_usart_irq_0	R5FSS0_CORE1_intr_IN_216	R5FSS0_CORE1	UART6 interrupt request	level
UART6	UART6_usart_irq_0	R5FSS1_CORE0_intr_IN_216	R5FSS1_CORE0	UART6 interrupt request	level
UART6	UART6_usart_irq_0	R5FSS1_CORE1_intr_IN_216	R5FSS1_CORE1	UART6 interrupt request	level

Table 4-88. UART Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
UART6	UART6_usart_irq_0	WKUP_R5FSS0_CORE0_intr_IN_216	WKUP_R5FSS0_CORE0	UART6 interrupt request	level
WKUP_UART0	WKUP_UART0_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_IN_144	WKUP_R5FSS0_CORE0	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	C7X256V0_CLEC_gic_spi_IN_218	C7X256V0_CLEC	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	C7X256V1_CLEC_gic_spi_IN_218	C7X256V1_CLEC	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	R5FSS0_CORE0_intr_IN_219	R5FSS0_CORE0	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	R5FSS0_CORE1_intr_IN_219	R5FSS0_CORE1	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	R5FSS1_CORE0_intr_IN_219	R5FSS1_CORE0	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	R5FSS1_CORE1_intr_IN_219	R5FSS1_CORE1	WKUP_UART0 interrupt request	level
WKUP_UART0	WKUP_UART0_usart_irq_0	WKUP_R5FSS0_CORE0_intr_IN_219	WKUP_R5FSS0_CORE0	WKUP_UART0 interrupt request	level

Table 4-89. UART Clocks

Module Instance	Module Clock Input	Source Clock Signal		Description
UART0	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	USART0_CLKSEL[0:0]	UART0 Functional Clock
		MAIN_PLL1_HSDIV1_CLKOUT		
	CLK	MAIN_SYSCLK0/4		UART0 Interface Clock
UART1	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	USART1_CLKSEL[0:0]	UART1 Functional Clock
		MAIN_PLL1_HSDIV1_CLKOUT		
	CLK	MAIN_SYSCLK0/4		UART1 Interface Clock
UART2	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	USART2_CLKSEL[0:0]	UART2 Functional Clock
		MAIN_PLL1_HSDIV1_CLKOUT		
	CLK	MAIN_SYSCLK0/4		UART2 Interface Clock
UART3	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	USART3_CLKSEL[0:0]	UART3 Functional Clock
		MAIN_PLL1_HSDIV1_CLKOUT		
	CLK	MAIN_SYSCLK0/4		UART3 Interface Clock

Table 4-89. UART Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal		Description
UART4	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	USART4_CLKSEL[0:0]	UART4 Functional Clock
		MAIN_PLL1_HSDIV1_CLKOUT		
	CLK	MAIN_SYSCLK0/4		UART4 Interface Clock
UART5	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	USART5_CLKSEL[0:0]	UART5 Functional Clock
		MAIN_PLL1_HSDIV1_CLKOUT		
	CLK	MAIN_SYSCLK0/4		UART5 Interface Clock
UART6	FCLK	MAIN_PLL1_HSDIV0_CLKOUT	USART6_CLKSEL[0:0]	UART6 Functional Clock
		MAIN_PLL1_HSDIV1_CLKOUT		
	CLK	MAIN_SYSCLK0/4		UART6 Interface Clock
WKUP_UART0	FCLK	MCU_PLL0_HSDIV2_CLKOUT		WKUP_UART0 Functional Clock
	CLK	DM_CLK/4	WKUP_CLKSEL[0:0]	WKUP_UART0 Interface Clock

4.9 High-speed Serial Interfaces

4.9.1 Gigabit Ethernet Switch (CPSW)

This section contains the integration details for the CPSW module on this device. For further information, see the *Gigabit Ethernet Switch (CPSW)* section of the *Peripherals* chapter.

4.9.1.1 CPSW Unsupported Features

The following features are not supported by the CPSW switch:

- Maximum frame size of 9600 bytes
- GMII Mode
- SGMII Mode
- MACSEC
- Synchronous Ethernet

4.9.1.2 Module Allocations

Table 4-90. CPSW Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
CPSW0			✓

4.9.1.3 Resets, Interrupts, and Clocks

Table 4-91. CPSW Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
CPSW0	MAIN_PSC0	GP_CORE	LPSC_MAIN_CPSW	21	OFF	YES	LPSC_MAIN_IP0

Table 4-92. CPSW Resets

Module Instance	Source	Description
CPSW0	MAIN_PSC0	CPSW0 reset

Table 4-93. CPSW Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CPSW0	CPSW0_cpts_comp_0	GLUELOGIC_epwm0_sync_mux_glue_input3_IN_0	GLUELOGIC_epwm0_sync_mux_glue	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_comp_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPout_CP_GEMAC_CPTS0_TS_COMP_IN_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPout	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_comp_0	C7X256V0_CLEC_gic_spi_IN_48	C7X256V0_CLEC	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_comp_0	C7X256V1_CLEC_gic_spi_IN_48	C7X256V1_CLEC	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_comp_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_0	DMASS0_INTAGGR_0	CPSW0 interrupt request	pulse

Table 4-93. CPSW Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CPSW0	CPSW0_cpts_comp_0	R5FSS0_CORE0_intr_IN_48	R5FSS0_CORE0	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_comp_0	R5FSS0_CORE1_intr_IN_48	R5FSS0_CORE1	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_comp_0	R5FSS1_CORE0_intr_IN_48	R5FSS1_CORE0	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_comp_0	R5FSS1_CORE1_intr_IN_48	R5FSS1_CORE1	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_comp_0	WKUP_R5FSS0_CORE0_intr_IN_48	WKUP_R5FSS0_CORE0	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_genf0_0	TIMESYNC_INTROUTER0_in_IN_16	TIMESYNC_INTROUTER0	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_genf1_0	TIMESYNC_INTROUTER0_in_IN_17	TIMESYNC_INTROUTER0	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_sync_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCout_CP_GEMAC_CPTS0_TS_SYNC_IN_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCout	CPSW0 interrupt request	pulse
CPSW0	CPSW0_cpts_sync_0	TIMESYNC_INTROUTER0_in_IN_18	TIMESYNC_INTROUTER0	CPSW0 interrupt request	pulse
CPSW0	CPSW0_ecc_ded_pend_0	ESM0_esm_lvl_event_IN_67	ESM0	CPSW0 interrupt request	level
CPSW0	CPSW0_ecc_sec_pend_0	ESM0_esm_lvl_event_IN_3	ESM0	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	C7X256V0_CLEC_gic_spi_IN_134	C7X256V0_CLEC	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	C7X256V1_CLEC_gic_spi_IN_134	C7X256V1_CLEC	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	R5FSS0_CORE0_intr_IN_134	R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	R5FSS0_CORE1_intr_IN_134	R5FSS0_CORE1	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	R5FSS1_CORE0_intr_IN_134	R5FSS1_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	R5FSS1_CORE1_intr_IN_134	R5FSS1_CORE1	CPSW0 interrupt request	level
CPSW0	CPSW0_evnt_pend_0	WKUP_R5FSS0_CORE0_intr_IN_134	WKUP_R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	C7X256V0_CLEC_gic_spi_IN_135	C7X256V0_CLEC	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	C7X256V1_CLEC_gic_spi_IN_135	C7X256V1_CLEC	CPSW0 interrupt request	level

Table 4-93. CPSW Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
CPSW0	CPSW0_mdio_pend_0	R5FSS0_CORE0_intr_IN_135	R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	R5FSS0_CORE1_intr_IN_135	R5FSS0_CORE1	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	R5FSS1_CORE0_intr_IN_135	R5FSS1_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	R5FSS1_CORE1_intr_IN_135	R5FSS1_CORE1	CPSW0 interrupt request	level
CPSW0	CPSW0_mdio_pend_0	WKUP_R5FSS0_CORE0_intr_IN_135	WKUP_R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	C7X256V0_CLEC_gic_spi_IN_136	C7X256V0_CLEC	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	C7X256V1_CLEC_gic_spi_IN_136	C7X256V1_CLEC	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	R5FSS0_CORE0_intr_IN_136	R5FSS0_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	R5FSS0_CORE1_intr_IN_136	R5FSS0_CORE1	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	R5FSS1_CORE0_intr_IN_136	R5FSS1_CORE0	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	R5FSS1_CORE1_intr_IN_136	R5FSS1_CORE1	CPSW0 interrupt request	level
CPSW0	CPSW0_stat_pend_0	WKUP_R5FSS0_CORE0_intr_IN_136	WKUP_R5FSS0_CORE0	CPSW0 interrupt request	level

Table 4-94. CPSW Clocks

Module Instance	Module Clock Input	Source Clock Signal		Description
CPSW0	CPPI_CLK	MAIN_SYSCLK0/2		CPSW0 CPPI packet streaming interface clock
	CPTS_RFT_CLK	MAIN_PLL2_HSDIV5_CLKOUT	CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT		
		CP_GEMAC_CPTS_REF_CLK		
		MCU_EXT_REFCLK0		
		EXT_REFCLK1		
		MAIN_PLL4_HSDIV1_CLKOUT		
		MAIN_SYSCLK0		
	GMII1_MR_CLK	MAIN_PLL2_HSDIV1_CLKOUT/10		
	GMII1_MT_CLK	MAIN_PLL2_HSDIV1_CLKOUT/10		
	GMII2_MR_CLK	MAIN_PLL2_HSDIV1_CLKOUT/10		
	GMII2_MT_CLK	MAIN_PLL2_HSDIV1_CLKOUT/10		
	GMII_RFT_CLK	MAIN_PLL2_HSDIV1_CLKOUT/2		CPSW0 125MHz Gigabit Mode Clock
	RGMII_MHZ_250_CLK	MAIN_PLL2_HSDIV1_CLKOUT		CPSW0 250-MHz Reference clock
	RGMII_MHZ_50_CLK	MAIN_PLL2_HSDIV1_CLKOUT/5		CPSW0 50-MHz Reference Clock
	RGMII_MHZ_5_CLK	MAIN_PLL2_HSDIV1_CLKOUT/50		CPSW0 5-MHz Reference Clock

4.9.2 Universal Serial Bus Subsystem (USB)

This section contains the integration details for the USB module on this device. For further information, see the *Universal Serial Bus Subsystem (USBSS)* section of the *Peripherals* chapter.

4.9.2.1 USB2SS Unsupported Features

The following features are not supported on this family of devices:

- Battery Charger Support
- Accessory Charger Adaptor Support
- On-The-Go (OTG)
- No Virtualization Support
- SuperSpeed (5Gb/s) operation
- USB 2.0 ECN: Link Power Management (LPM)
- Low Speed operation in device mode
- Charger Detection

4.9.2.2 Module Allocations

Table 4-95. USB Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
USB0			✓

4.9.2.3 Resets, Interrupts, and Clocks

Table 4-96. USB Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
USB0	MAIN_PSC0	GP_CORE	LPSC_MAIN_USB0	12	OFF	YES	LPSC_MAIN_IP0

Table 4-97. USB Resets

Module Instance	Source	Description
USB0	MAIN_PSC0	USB0 reset

Table 4-98. USB Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
USB0	USB0_a_ecc_aggr_corrected_err_level_0	ESM0_esm_lvl_event_IN_35	ESM0	USB0 interrupt request	level
USB0	USB0_a_ecc_aggr_uncorrected_err_level_0	ESM0_esm_lvl_event_IN_111	ESM0	USB0 interrupt request	level
USB0	USB0_host_system_error_0	ESM0_esm_lvl_event_IN_32	ESM0	USB0 interrupt request	level
USB0	USB0_irq_[7:0]	C7X256V0_CLEC_gic_spi_IN_[227:220]	C7X256V0_CLEC	USB0 interrupt request	level
USB0	USB0_irq_[7:0]	C7X256V1_CLEC_gic_spi_IN_[227:220]	C7X256V1_CLEC	USB0 interrupt request	level
USB0	USB0_irq_[7:0]	R5FSS0_CORE0_intr_IN_[227:220]	R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_irq_[7:0]	R5FSS0_CORE1_intr_IN_[227:220]	R5FSS0_CORE1	USB0 interrupt request	level

Table 4-98. USB Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
USB0	USB0_irq_[7:0]	R5FSS1_CORE0_intr_IN_[227:220]	R5FSS1_CORE0	USB0 interrupt request	level
USB0	USB0_irq_[7:0]	R5FSS1_CORE1_intr_IN_[227:220]	R5FSS1_CORE1	USB0 interrupt request	level
USB0	USB0_irq_[7:0]	WKUP_R5FSS0_CORE0_intr_IN_[227:220]	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_misc_level_0	C7X256V0_CLEC_gic_spi_IN_228	USB0	USB0 interrupt request	level
USB0	USB0_misc_level_0	C7X256V1_CLEC_gic_spi_IN_228	USB0	USB0 interrupt request	level
USB0	USB0_misc_level_0	R5FSS0_CORE0_intr_IN_228	USB0	USB0 interrupt request	level
USB0	USB0_misc_level_0	R5FSS0_CORE1_intr_IN_228	R5FSS0_CORE1	USB0 interrupt request	level
USB0	USB0_misc_level_0	R5FSS1_CORE0_intr_IN_228	R5FSS1_CORE0	USB0 interrupt request	level
USB0	USB0_misc_level_0	R5FSS1_CORE1_intr_IN_228	R5FSS1_CORE1	USB0 interrupt request	level
USB0	USB0_misc_level_0	WKUP_R5FSS0_CORE0_intr_IN_228	WKUP_R5FSS0_CORE0	USB0 interrupt request	level
USB0	USB0_usb_wakeup_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_IN_61	WKUP_R5FSS0_CORE0	USB0 interrupt request	level

Table 4-99. USB Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
USB0	BUS_CLK	MAIN_SYSCLK0/2		
	USB2_TAP_TCK	MAIN_TAP_BS_JTAG__CLK		
	CFG_CLK	MAIN_SYSCLK0/4		
	USB2_APB_PCLK_CLK	MAIN_SYSCLK0/4		
	USB2_REFCLOCK_CLK	HFOSC0_CLKOUT	USB0_CLKSEL[0:0]	
		MAIN_PLL0_HSDIV8_CLKOUT		

4.10 Memory Interfaces

4.10.1 Octal Serial Peripheral Interface (OSPI)

This section contains the integration details for the OSPI module on this device. For Further information, see the *Octal Serial Peripheral Interface (OSPI)* section of the *Peripherals* chapter, and *Flash Subsystem (FSS)* of the *Module Integration* chapter.

OSPI Unsupported Features

- OSPI Clock Phase/Polarity Modes 1,2,3
- OSPI PDMA. Use CPU-triggered block DMA
- Flash device status polling for programing operation using STIG

4.10.2 Flash Subsystem (FSS)

This section contains the integration details for the Flash Subsystem on this device. For further information, see the *Flash Subsystem (FSS)* section of the *Peripherals* chapter.

4.10.2.1 FSS Unsupported Features

For more information, see, *OSPI Unsupported Features*.

4.10.2.2 Module Allocations

Table 4-100. FSS Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
fss_of_ul0 (FSS0)			✓
FSS1			✓

4.10.2.3 Resets, Interrupts, and Clocks

Table 4-101. FSS Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
FSS0	MAIN_PSC0	GP_CORE	LPSC_MAIN_OSPI0	28	ON	YES	LPSC_MAIN_IP0
FSS1	MAIN_PSC0	GP_CORE	LPSC_MAIN_OSPI1	29	ON	YES	LPSC_MAIN_IP0
FSS1_HYPERBUS1P0_0	MAIN_PSC0	GP_CORE	LPSC_MAIN_HYPERBUS	30	ON	YES	LPSC_MAIN_OSPI1

Table 4-102. FSS Resets

Module Instance	Source	Description
FSS0	MAIN_PSC0	FSS0 reset
FSS1	MAIN_PSC0	FSS1 reset

Table 4-103. FSS Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
FSS0	FSS0_ecc_corr_level_0	ESM0_esm_lvl_event_IN_145	ESM0	FSS0 interrupt request	level
FSS0	FSS0_ecc_uncorr_level_0	ESM0_esm_lvl_event_IN_146	ESM0	FSS0 interrupt request	level
FSS0	FSS0_fsas_ecc_intr_err_pend_0	C7X256V0_CLEC_gic_spi_IN_170	C7X256V0_CLEC	FSS0 interrupt request	level

Table 4-103. FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
FSS0	FSS0_fsas_ecc_intr_err_pend_0	C7X256V1_CLEC_gic_spi_IN_170	C7X256V1_CLEC	FSS0 interrupt request	level
FSS0	FSS0_fsas_ecc_intr_err_pend_0	ESM0_esm_lvl_event_IN_141	ESM0	FSS0 interrupt request	level
FSS0	FSS0_fsas_ecc_intr_err_pend_0	R5FSS0_CORE0_intr_IN_182	R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_fsas_ecc_intr_err_pend_0	R5FSS0_CORE1_intr_IN_182	R5FSS0_CORE1	FSS0 interrupt request	level
FSS0	FSS0_fsas_ecc_intr_err_pend_0	R5FSS1_CORE0_intr_IN_182	R5FSS1_CORE0	FSS0 interrupt request	level
FSS0	FSS0_fsas_ecc_intr_err_pend_0	R5FSS1_CORE1_intr_IN_182	R5FSS1_CORE1	FSS0 interrupt request	level
FSS0	FSS0_fsas_ecc_intr_err_pend_0	WKUP_R5FSS0_CORE0_intr_IN_182	WKUP_R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_err_pend_0	C7X256V0_CLEC_gic_spi_IN_173	C7X256V0_CLEC	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_err_pend_0	C7X256V1_CLEC_gic_spi_IN_173	C7X256V1_CLEC	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_err_pend_0	R5FSS0_CORE0_intr_IN_173	R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_err_pend_0	R5FSS0_CORE1_intr_IN_173	R5FSS0_CORE1	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_err_pend_0	R5FSS1_CORE0_intr_IN_173	R5FSS1_CORE0	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_err_pend_0	R5FSS1_CORE1_intr_IN_173	R5FSS1_CORE1	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_err_pend_0	WKUP_R5FSS0_CORE0_intr_IN_173	WKUP_R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_172	C7X256V0_CLEC	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_172	C7X256V1_CLEC	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_intr_pend_0	R5FSS0_CORE0_intr_IN_172	R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_intr_pend_0	R5FSS0_CORE1_intr_IN_172	R5FSS0_CORE1	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_intr_pend_0	R5FSS1_CORE0_intr_IN_172	R5FSS1_CORE0	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_intr_pend_0	R5FSS1_CORE1_intr_IN_172	R5FSS1_CORE1	FSS0 interrupt request	level
FSS0	FSS0_fsas_fota_stat_intr_pend_0	WKUP_R5FSS0_CORE0_intr_IN_172	WKUP_R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_ospi0_ecc_corr_lvl_intr_0	ESM0_esm_lvl_event_IN_11	ESM0	FSS0 interrupt request	level

Table 4-103. FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
FSS0	FSS0_ospi0_ecc_uncorr_lvl_intr_0	ESM0_esm_lvl_event_IN_74	ESM0	FSS0 interrupt request	level
FSS0	FSS0_ospi0_lvl_intr_0	C7X256V0_CLEC_gic_spi_IN_171	C7X256V0_CLEC	FSS0 interrupt request	level
FSS0	FSS0_ospi0_lvl_intr_0	C7X256V1_CLEC_gic_spi_IN_171	C7X256V1_CLEC	FSS0 interrupt request	level
FSS0	FSS0_ospi0_lvl_intr_0	R5FSS0_CORE0_intr_IN_171	R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_ospi0_lvl_intr_0	R5FSS0_CORE1_intr_IN_171	R5FSS0_CORE1	FSS0 interrupt request	level
FSS0	FSS0_ospi0_lvl_intr_0	R5FSS1_CORE0_intr_IN_171	R5FSS1_CORE0	FSS0 interrupt request	level
FSS0	FSS0_ospi0_lvl_intr_0	R5FSS1_CORE1_intr_IN_171	R5FSS1_CORE1	FSS0 interrupt request	level
FSS0	FSS0_ospi0_lvl_intr_0	WKUP_R5FSS0_CORE0_intr_IN_171	WKUP_R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_otfa_intr_err_pend_0	C7X256V0_CLEC_gic_spi_IN_174	C7X256V0_CLEC	FSS0 interrupt request	level
FSS0	FSS0_otfa_intr_err_pend_0	C7X256V1_CLEC_gic_spi_IN_174	C7X256V1_CLEC	FSS0 interrupt request	level
FSS0	FSS0_otfa_intr_err_pend_0	R5FSS0_CORE0_intr_IN_174	R5FSS0_CORE0	FSS0 interrupt request	level
FSS0	FSS0_otfa_intr_err_pend_0	R5FSS0_CORE1_intr_IN_174	R5FSS0_CORE1	FSS0 interrupt request	level
FSS0	FSS0_otfa_intr_err_pend_0	R5FSS1_CORE0_intr_IN_174	R5FSS1_CORE0	FSS0 interrupt request	level
FSS0	FSS0_otfa_intr_err_pend_0	R5FSS1_CORE1_intr_IN_174	R5FSS1_CORE1	FSS0 interrupt request	level
FSS0	FSS0_otfa_intr_err_pend_0	WKUP_R5FSS0_CORE0_intr_IN_174	WKUP_R5FSS0_CORE0	FSS0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_ecc_intr_err_pend_0	C7X256V0_CLEC_gic_spi_IN_169	C7X256V0_CLEC	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_ecc_intr_err_pend_0	C7X256V1_CLEC_gic_spi_IN_169	C7X256V1_CLEC	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_ecc_intr_err_pend_0	ESM0_esm_lvl_event_IN_142	ESM0	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_ecc_intr_err_pend_0	R5FSS0_CORE0_intr_IN_181	R5FSS0_CORE0	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_ecc_intr_err_pend_0	R5FSS0_CORE1_intr_IN_181	R5FSS0_CORE1	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_ecc_intr_err_pend_0	R5FSS1_CORE0_intr_IN_181	R5FSS1_CORE0	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_ecc_intr_err_pend_0	R5FSS1_CORE1_intr_IN_181	R5FSS1_CORE1	FSS1_FSAS_0 interrupt request	level

Table 4-103. FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
FSS1_FSAS_0	FSS1_FSAS_0_ecc_intr_err_pend_0	WKUP_R5FSS0_CORE0_intr_IN_181	WKUP_R5FSS0_CORE0	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_otfa_intr_err_pend_0	C7X256V0_CLEC_gic_spi_IN_175	C7X256V0_CLEC	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_otfa_intr_err_pend_0	C7X256V1_CLEC_gic_spi_IN_175	C7X256V1_CLEC	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_otfa_intr_err_pend_0	R5FSS0_CORE0_intr_IN_180	R5FSS0_CORE0	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_otfa_intr_err_pend_0	R5FSS0_CORE1_intr_IN_180	R5FSS0_CORE1	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_otfa_intr_err_pend_0	R5FSS1_CORE0_intr_IN_180	R5FSS1_CORE0	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_otfa_intr_err_pend_0	R5FSS1_CORE1_intr_IN_180	R5FSS1_CORE1	FSS1_FSAS_0 interrupt request	level
FSS1_FSAS_0	FSS1_FSAS_0_otfa_intr_err_pend_0	WKUP_R5FSS0_CORE0_intr_IN_180	WKUP_R5FSS0_CORE0	FSS1_FSAS_0 interrupt request	level
FSS1_HYPERBUS1P0_0	FSS1_HYPERBUS1P0_0_hpb_intr_0	C7X256V0_CLEC_gic_spi_IN_179	C7X256V0_CLEC	FSS1_HYPERBUS1P0_0 interrupt request	level
FSS1_HYPERBUS1P0_0	FSS1_HYPERBUS1P0_0_hpb_intr_0	C7X256V1_CLEC_gic_spi_IN_179	C7X256V1_CLEC	FSS1_HYPERBUS1P0_0 interrupt request	level
FSS1_HYPERBUS1P0_0	FSS1_HYPERBUS1P0_0_hpb_intr_0	R5FSS0_CORE0_intr_IN_179	R5FSS0_CORE0	FSS1_HYPERBUS1P0_0 interrupt request	level
FSS1_HYPERBUS1P0_0	FSS1_HYPERBUS1P0_0_hpb_intr_0	R5FSS0_CORE1_intr_IN_179	R5FSS0_CORE1	FSS1_HYPERBUS1P0_0 interrupt request	level
FSS1_HYPERBUS1P0_0	FSS1_HYPERBUS1P0_0_hpb_intr_0	R5FSS1_CORE0_intr_IN_179	R5FSS1_CORE0	FSS1_HYPERBUS1P0_0 interrupt request	level
FSS1_HYPERBUS1P0_0	FSS1_HYPERBUS1P0_0_hpb_intr_0	R5FSS1_CORE1_intr_IN_179	R5FSS1_CORE1	FSS1_HYPERBUS1P0_0 interrupt request	level
FSS1_HYPERBUS1P0_0	FSS1_HYPERBUS1P0_0_hpb_intr_0	WKUP_R5FSS0_CORE0_intr_IN_179	WKUP_R5FSS0_CORE0	FSS1_HYPERBUS1P0_0 interrupt request	level
FSS1_OSPI_0	FSS1_OSPI_0_ospi_lvl_intr_0	C7X256V0_CLEC_gic_spi_IN_178	C7X256V0_CLEC	FSS1_OSPI_0 interrupt request	level
FSS1_OSPI_0	FSS1_OSPI_0_ospi_lvl_intr_0	C7X256V1_CLEC_gic_spi_IN_178	C7X256V1_CLEC	FSS1_OSPI_0 interrupt request	level
FSS1_OSPI_0	FSS1_OSPI_0_ospi_lvl_intr_0	R5FSS0_CORE0_intr_IN_178	R5FSS0_CORE0	FSS1_OSPI_0 interrupt request	level
FSS1_OSPI_0	FSS1_OSPI_0_ospi_lvl_intr_0	R5FSS0_CORE1_intr_IN_178	R5FSS0_CORE1	FSS1_OSPI_0 interrupt request	level
FSS1_OSPI_0	FSS1_OSPI_0_ospi_lvl_intr_0	R5FSS1_CORE0_intr_IN_178	R5FSS1_CORE0	FSS1_OSPI_0 interrupt request	level
FSS1_OSPI_0	FSS1_OSPI_0_ospi_lvl_intr_0	R5FSS1_CORE1_intr_IN_178	R5FSS1_CORE1	FSS1_OSPI_0 interrupt request	level
FSS1_OSPI_0	FSS1_OSPI_0_ospi_lvl_intr_0	WKUP_R5FSS0_CORE0_intr_IN_178	WKUP_R5FSS0_CORE0	FSS1_OSPI_0 interrupt request	level

Table 4-103. FSS Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
FSS1_OSPI_ECC_AGGR_0	FSS1_OSPI_ECC_AGGR_0_ospi_ecc_corr_lvl_intr_0	ESM0_esm_lvl_event_IN_12	ESM0	FSS1_OSPI_ECC_AGGR_0 interrupt request	level
FSS1_OSPI_ECC_AGGR_0	FSS1_OSPI_ECC_AGGR_0_ospi_ecc_uncorr_lvl_intr_0	ESM0_esm_lvl_event_IN_75	ESM0	FSS1_OSPI_ECC_AGGR_0 interrupt request	level

Table 4-104. FSS Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
FSS0_FSAS_0	ICLK	MAIN_SYSCLK0		FSS0_FSAS_0 Interface Clock
FSS0_HYPERBUS1P0_0	CBA_CLK	MAIN_SYSCLK0		
	HPB_CLKX1_CLK	MAIN_PLL2_HSDIV4_CLKOUT/2		
	HPB_CLKX1_INV_CLK	MAIN_PLL2_HSDIV4_CLKOUT/2		
	HPB_CLKX2_CLK	MAIN_PLL2_HSDIV4_CLKOUT		
	HPB_CLKX2_INV_CLK	MAIN_PLL2_HSDIV4_CLKOUT		
FSS0_OSPI_0	HCLK	MAIN_SYSCLK0		FSS0_OSPI_0 Data Transfer Clock
	PCLK	MAIN_SYSCLK0		FSS0_OSPI_0 Configuration clock
	RCLK	MAIN_PLL0_HSDIV1_CLKOUT	OSPI1_CLKSEL[0:0]	FSS0_OSPI_0 Reference Clock
		MAIN_PLL1_HSDIV5_CLKOUT	OSPI1_CLKSEL[0:0]	
FSS0_of_ul0	OSPI0_RCLK_CLK	MAIN_PLL0_HSDIV1_CLKOUT	OSPI0_CLKSEL[0:0]	
		MAIN_PLL1_HSDIV5_CLKOUT	OSPI0_CLKSEL[0:0]	
	VBUS_CLK	MAIN_SYSCLK0/2		
FSS0_OSPI_1	OSPI_HCLK	MAIN_SYSCLK0		

4.10.3 Multimedia Card Secure Digital (MMCSD)

This section contains the integration details for the MMCSD module on this device. For further information, see the *Multimedia Card Secure Digital (MMCSD*) section of the *Peripherals* chapter.

4.10.3.1 MMCSD Unsupported Features

The following features are not supported on this family of devices:

- The following apply to 4-bit MMCSD instances:
  - SD Card busy LED - Not pinned out
  - High Speed DDR
- The following apply to 8-bit MMCSD instances:
  - SD Card busy LED - Not pinned out
  - SD/SDIO/MMC Cards (Removable) - no support for 4-pin/8-pin muxing
  - SD Card Detect Pin - Not pinned out
  - SD Card Write Protect Pin - Not pinned out

4.10.3.2 Module Allocations

Table 4-105. MMCSD Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
MMCSD0			✓

4.10.3.3 Resets, Interrupts, and Clocks

Table 4-106. MMCSD Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MMCSD0	MAIN_PSC0	GP_CORE	LPSC_EMMC8B	20	OFF	YES	LPSC_MAIN_IP0

Table 4-107. MMCSD Resets

Module Instance	Source	Description
MMCSD0	MAIN_PSC0	MMCSD0 reset

Table 4-108. MMCSD Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MMCSD0	MMCSD0_emmcsdss_intr_0	C7X256V0_CLEC_gic_spi_IN_165	C7X256V0_CLEC	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	C7X256V1_CLEC_gic_spi_IN_165	C7X256V1_CLEC	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	R5FSS0_CORE0_intr_IN_161	R5FSS0_CORE0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	R5FSS0_CORE1_intr_IN_161	R5FSS0_CORE1	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	R5FSS1_CORE0_intr_IN_161	R5FSS1_CORE0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	R5FSS1_CORE1_intr_IN_161	R5FSS1_CORE1	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_intr_0	WKUP_R5FSS0_CORE0_intr_IN_161	WKUP_R5FSS0_CORE0	MMCSD0 interrupt request	level

Table 4-108. MMCSD Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MMCSD0	MMCSD0_emmcsdss_rxmem_corr_err_lvl_0	ESM0_esm_lvl_event_IN_54	ESM0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_rxmem_uncorr_err_lvl_0	ESM0_esm_lvl_event_IN_55	ESM0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_txmem_corr_err_lvl_0	ESM0_esm_lvl_event_IN_56	ESM0	MMCSD0 interrupt request	level
MMCSD0	MMCSD0_emmcsdss_txmem_uncorr_err_lvl_0	ESM0_esm_lvl_event_IN_57	ESM0	MMCSD0 interrupt request	level

Table 4-109. MMCSD Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MMCSD0	ICLK	MAIN_SYSCLK0/2		MMCSD Interface Clock
	FCLK	MAIN_PLL0_HSDIV5_CLKOUT	EMMC0_CLKSEL[0:0]	MMCSD Functional Clock
		MAIN_PLL2_HSDIV2_CLKOUT		

4.11 Industrial and Control Interfaces

4.11.1 Modular Controller Area Network (MCAN)

This section contains the integration details for the MCAN module on this device. For further information, see the *Modular Controller Area Network (MCAN)* section of the *Peripherals* chapter.

4.11.1.1 MCAN Unsupported Features

- Debug DMAs - DMA Ack not supported by PDMA architecture. Debug messages can be traced through the RX FIFO.
- TX DMA channels 3-31 are not supported by the Main domain instance (MCAN0)- Only TX_DMA[2:0] have associated PDMA channels

4.11.1.2 Module Allocations

Table 4-110. MCAN Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
MCAN0			✓
MCAN1			✓
MCAN2			✓
MCAN3			✓
MCAN4			✓

4.11.1.3 Resets, Interrupts, and Clocks

Table 4-111. MCAN Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCAN0	MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN0	23	OFF	YES	LPSC_MAIN_IP0
MCAN1	MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN1	24	OFF	YES	LPSC_MAIN_IP0
MCAN2	MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN2	25	OFF	YES	LPSC_MAIN_IP0
MCAN3	MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN3	26	OFF	YES	LPSC_MAIN_IP0
MCAN4	MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN4	27	OFF	YES	LPSC_MAIN_IP0

Table 4-112. MCAN Resets

Module Instance	Source	Description
MCAN0	MAIN_PSC0	MCAN0 reset
MCAN1	MAIN_PSC0	MCAN1 reset
MCAN2	MAIN_PSC0	MCAN2 reset
MCAN3	MAIN_PSC0	MCAN3 reset
MCAN4	MAIN_PSC0	MCAN4 reset

Table 4-113. MCAN Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN0	MCAN0_mcanss_ecc_corr_lvl_int_0	ESM0_esm_lvl_event_IN_58	ESM0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ecc_uncorr_lvl_int_0	ESM0_esm_lvl_event_IN_59	ESM0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	C7X256V0_CLEC_gic_spi_IN_186	C7X256V0_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	C7X256V1_CLEC_gic_spi_IN_186	C7X256V1_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE0_intr_IN_186	R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE1_intr_IN_186	R5FSS0_CORE1	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE0_intr_IN_186	R5FSS1_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE1_intr_IN_186	R5FSS1_CORE1	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_ext_ts_rollover_lvl_int_0	WKUP_R5FSS0_CORE0_intr_IN_186	WKUP_R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_fe_[2:0]	PDMA0_mcanss_main_0_fe_IN_[2:0]	PDMA0	MCAN0 interrupt request	pulse
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_187	C7X256V0_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_188	C7X256V0_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_187	C7X256V1_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_188	C7X256V1_CLEC	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_230	R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_231	R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_230	R5FSS0_CORE1	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_231	R5FSS0_CORE1	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_230	R5FSS1_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_231	R5FSS1_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_230	R5FSS1_CORE1	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_231	R5FSS1_CORE1	MCAN0 interrupt request	level

Table 4-113. MCAN Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_230	WKUP_R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_231	WKUP_R5FSS0_CORE0	MCAN0 interrupt request	level
MCAN0	MCAN0_mcanss_tx_dma_[31:0]	PDMA0_mcanss_main_0_tx_IN_[2:0]	PDMA0	MCAN0 interrupt request	pulse
MCAN1	MCAN1_mcanss_ecc_corr_lvl_int_0	ESM0_esm_lvl_event_IN_60	ESM0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_ecc_uncorr_lvl_int_0	ESM0_esm_lvl_event_IN_61	ESM0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_ext_ts_rollover_lvl_int_0	C7X256V0_CLEC_gic_spi_IN_199	C7X256V0_CLEC	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_ext_ts_rollover_lvl_int_0	C7X256V1_CLEC_gic_spi_IN_199	C7X256V1_CLEC	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE0_intr_IN_229	R5FSS0_CORE0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE1_intr_IN_229	R5FSS0_CORE1	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE0_intr_IN_229	R5FSS1_CORE0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE1_intr_IN_229	R5FSS1_CORE1	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_ext_ts_rollover_lvl_int_0	WKUP_R5FSS0_CORE0_intr_IN_229	WKUP_R5FSS0_CORE0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_fe_[2:0]	PDMA0_mcanss_main_1_fe_IN_[2:0]	PDMA0	MCAN1 interrupt request	pulse
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_245	C7X256V0_CLEC	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_246	C7X256V0_CLEC	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_245	C7X256V1_CLEC	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_246	C7X256V1_CLEC	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_232	R5FSS0_CORE0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_233	R5FSS0_CORE0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_232	R5FSS0_CORE1	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_233	R5FSS0_CORE1	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_232	R5FSS1_CORE0	MCAN1 interrupt request	level

Table 4-113. MCAN Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_233	R5FSS1_CORE0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_232	R5FSS1_CORE1	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_233	R5FSS1_CORE1	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_232	WKUP_R5FSS0_CORE0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_233	WKUP_R5FSS0_CORE0	MCAN1 interrupt request	level
MCAN1	MCAN1_mcanss_tx_dma_[31:0]	PDMA0_mcanss_main_1_tx_IN_0	PDMA0	MCAN1 interrupt request	pulse
MCAN1	MCAN1_mcanss_tx_dma_[31:0]	PDMA0_mcanss_main_1_tx_IN_1	PDMA0	MCAN1 interrupt request	pulse
MCAN1	MCAN1_mcanss_tx_dma_[31:0]	PDMA0_mcanss_main_1_tx_IN_2	PDMA0	MCAN1 interrupt request	pulse
MCAN2	MCAN2_mcanss_ecc_corr_lvl_int_0	ESM0_esm_lvl_event_IN_62	ESM0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_ecc_uncorr_lvl_int_0	ESM0_esm_lvl_event_IN_63	ESM0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_ext_ts_rollover_lvl_int_0	C7X256V0_CLEC_gic_spi_IN_189	C7X256V0_CLEC	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_ext_ts_rollover_lvl_int_0	C7X256V1_CLEC_gic_spi_IN_189	C7X256V1_CLEC	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE0_intr_IN_187	R5FSS0_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE1_intr_IN_187	R5FSS0_CORE1	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE0_intr_IN_187	R5FSS1_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE1_intr_IN_187	R5FSS1_CORE1	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_ext_ts_rollover_lvl_int_0	WKUP_R5FSS0_CORE0_intr_IN_187	WKUP_R5FSS0_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_fe_[2:0]	PDMA4_mcanss_main_2_fe_IN_[2:0]	PDMA4	MCAN2 interrupt request	pulse
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_247	C7X256V0_CLEC	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_248	C7X256V0_CLEC	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_247	C7X256V1_CLEC	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_248	C7X256V1_CLEC	MCAN2 interrupt request	level

Table 4-113. MCAN Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_234	R5FSS0_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_235	R5FSS0_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_234	R5FSS0_CORE1	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_235	R5FSS0_CORE1	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_234	R5FSS1_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_235	R5FSS1_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_234	R5FSS1_CORE1	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_235	R5FSS1_CORE1	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_234	WKUP_R5FSS0_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_235	WKUP_R5FSS0_CORE0	MCAN2 interrupt request	level
MCAN2	MCAN2_mcanss_tx_dma_[31:0]	PDMA4_mcanss_main_2_tx_IN_[2:0]	PDMA4	MCAN2 interrupt request	pulse
MCAN3	MCAN3_mcanss_ecc_corr_lvl_int_0	ESM0_esm_lvl_event_IN_68	ESM0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_ecc_uncorr_lvl_int_0	ESM0_esm_lvl_event_IN_69	ESM0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_ext_ts_rollover_lvl_int_0	C7X256V0_CLEC_gic_spi_IN_190	C7X256V0_CLEC	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_ext_ts_rollover_lvl_int_0	C7X256V1_CLEC_gic_spi_IN_190	C7X256V1_CLEC	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE0_intr_IN_188	R5FSS0_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE1_intr_IN_188	R5FSS0_CORE1	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE0_intr_IN_188	R5FSS1_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE1_intr_IN_188	R5FSS1_CORE1	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_ext_ts_rollover_lvl_int_0	WKUP_R5FSS0_CORE0_intr_IN_188	WKUP_R5FSS0_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_fe_[2:0]	PDMA4_mcanss_main_3_fe_IN_[2:0]	PDMA4	MCAN3 interrupt request	pulse
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_249	C7X256V0_CLEC	MCAN3 interrupt request	level

Table 4-113. MCAN Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_250	C7X256V0_CLEC	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_249	C7X256V1_CLEC	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_250	C7X256V1_CLEC	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_236	R5FSS0_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_237	R5FSS0_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_236	R5FSS0_CORE1	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_237	R5FSS0_CORE1	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_236	R5FSS1_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_237	R5FSS1_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_236	R5FSS1_CORE1	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_237	R5FSS1_CORE1	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_236	WKUP_R5FSS0_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_237	WKUP_R5FSS0_CORE0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_mcan_lvl_int_[1:0]	HSM0_nvic_IN_110	HSM0	MCAN3 interrupt request	level
MCAN3	MCAN3_mcanss_tx_dma_[31:0]	PDMA4_mcanss_main_3_tx_IN_[2:0]	PDMA4	MCAN3 interrupt request	pulse
MCAN4	MCAN4_mcanss_ecc_corr_lvl_int_0	ESM0_esm_lvl_event_IN_70	ESM0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_ecc_uncorr_lvl_int_0	ESM0_esm_lvl_event_IN_71	ESM0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_ext_ts_rollover_lvl_int_0	C7X256V0_CLEC_gic_spi_IN_191	C7X256V0_CLEC	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_ext_ts_rollover_lvl_int_0	C7X256V1_CLEC_gic_spi_IN_191	C7X256V1_CLEC	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE0_intr_IN_189	R5FSS0_CORE0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_ext_ts_rollover_lvl_int_0	R5FSS0_CORE1_intr_IN_189	R5FSS0_CORE1	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE0_intr_IN_189	R5FSS1_CORE0	MCAN4 interrupt request	level

Table 4-113. MCAN Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCAN4	MCAN4_mcanss_ext_ts_rollover_lvl_int_0	R5FSS1_CORE1_intr_IN_189	R5FSS1_CORE1	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_ext_ts_rollover_lvl_int_0	WKUP_R5FSS0_CORE0_intr_IN_189	WKUP_R5FSS0_CORE0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_fe_[2:0]	PDMA4_mcanss_main_4_fe_IN_[2:0]	PDMA4	MCAN4 interrupt request	pulse
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_251	C7X256V0_CLEC	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	C7X256V0_CLEC_gic_spi_IN_252	C7X256V0_CLEC	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_251	C7X256V1_CLEC	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	C7X256V1_CLEC_gic_spi_IN_252	C7X256V1_CLEC	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_238	R5FSS0_CORE0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE0_intr_IN_239	R5FSS0_CORE0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_238	R5FSS0_CORE1	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	R5FSS0_CORE1_intr_IN_239	R5FSS0_CORE1	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_238	R5FSS1_CORE0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE0_intr_IN_239	R5FSS1_CORE0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_238	R5FSS1_CORE1	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	R5FSS1_CORE1_intr_IN_239	R5FSS1_CORE1	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_238	WKUP_R5FSS0_CORE0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_mcan_lvl_int_[1:0]	WKUP_R5FSS0_CORE0_intr_IN_239	WKUP_R5FSS0_CORE0	MCAN4 interrupt request	level
MCAN4	MCAN4_mcanss_tx_dma_[31:0]	PDMA4_mcanss_main_4_tx_IN_[2:0]	PDMA4	MCAN4 interrupt request	pulse

Table 4-114. MCAN Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCAN0	MCANSS_CAN_RXD	MAIN_PBIST_CLK		
	ICLK	MAIN_PLL0_HSDIV4_CLKOUT	MCAN0_CLKSEL[1:0]	
		MCU_EXT_REFCLK0	MCAN0_CLKSEL[1:0]	
		EXT_REFCLK1	MCAN0_CLKSEL[1:0]	
		HFOSC0_CLKOUT	MCAN0_CLKSEL[1:0]	
	FCLK	MAIN_SYSCLK0/4		
MCAN1	MCANSS_CAN_RXD	MAIN_PBIST_CLK		
	ICLK	MAIN_PLL0_HSDIV4_CLKOUT	MCAN1_CLKSEL[1:0]	
		MCU_EXT_REFCLK0	MCAN1_CLKSEL[1:0]	
		EXT_REFCLK1	MCAN1_CLKSEL[1:0]	
		HFOSC0_CLKOUT	MCAN1_CLKSEL[1:0]	
	FCLK	MAIN_SYSCLK0/4		
MCAN2	MCANSS_CAN_RXD	MAIN_PBIST_CLK		
	ICLK	MAIN_PLL0_HSDIV4_CLKOUT	MCAN2_CLKSEL[1:0]	
		MCU_EXT_REFCLK0	MCAN2_CLKSEL[1:0]	
		EXT_REFCLK1	MCAN2_CLKSEL[1:0]	
		HFOSC0_CLKOUT	MCAN2_CLKSEL[1:0]	
	FCLK	MAIN_SYSCLK0/4		
MCAN3	MCANSS_CAN_RXD	MAIN_PBIST_CLK		
	ICLK	MAIN_PLL0_HSDIV4_CLKOUT	MCAN3_CLKSEL[1:0]	
		MCU_EXT_REFCLK0	MCAN3_CLKSEL[1:0]	
		EXT_REFCLK1	MCAN3_CLKSEL[1:0]	
		HFOSC0_CLKOUT	MCAN3_CLKSEL[1:0]	
	FCLK	MAIN_SYSCLK0/4		
MCAN4	MCANSS_CAN_RXD	MAIN_PBIST_CLK		
	ICLK	MAIN_PLL0_HSDIV4_CLKOUT	MCAN4_CLKSEL[1:0]	
		MCU_EXT_REFCLK0	MCAN4_CLKSEL[1:0]	
		EXT_REFCLK1	MCAN4_CLKSEL[1:0]	
		HFOSC0_CLKOUT	MCAN4_CLKSEL[1:0]	
	FCLK	MAIN_SYSCLK0/4		

4.11.2 Enhanced Capture (ECAP)

This section contains the integration details for the ECAP module on this device. For further information, see the *Enhanced Capture (ECAP)* section of the *Peripherals* chapter.

4.11.2.1 ECAP Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.11.2.2 Module Allocations

Table 4-115. ECAP Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
ECAP0			✓
ECAP1			✓
ECAP2			✓
ECAP3			✓
ECAP4			✓
ECAP5			✓

4.11.2.3 Resets, Interrupts, and Clocks

Table 4-116. ECAP Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
ECAP0	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
ECAP1	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
ECAP2	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
ECAP3	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
ECAP4	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
ECAP5	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO

Table 4-117. ECAP Resets

Module Instance	Source	Description
ECAP0	MAIN_PSC0	ECAP0 reset
ECAP1	MAIN_PSC0	ECAP1 reset
ECAP2	MAIN_PSC0	ECAP2 reset
ECAP3	MAIN_PSC0	ECAP3 reset

Table 4-117. ECAP Resets (continued)

Module Instance	Source	Description
ECAP4	MAIN_PSC0	ECAP4 reset
ECAP5	MAIN_PSC0	ECAP5 reset

Table 4-118. ECAP Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ECAP0	ECAP0_ecap_int_0	C7X256V0_CLEC_gic_spi_IN_145	C7X256V0_CLEC	ECAP0 interrupt request	pulse
ECAP0	ECAP0_ecap_int_0	C7X256V1_CLEC_gic_spi_IN_145	C7X256V1_CLEC	ECAP0 interrupt request	pulse
ECAP0	ECAP0_ecap_int_0	R5FSS0_CORE0_intr_IN_83	R5FSS0_CORE0	ECAP0 interrupt request	pulse
ECAP0	ECAP0_ecap_int_0	R5FSS0_CORE1_intr_IN_83	R5FSS0_CORE1	ECAP0 interrupt request	pulse
ECAP0	ECAP0_ecap_int_0	R5FSS1_CORE0_intr_IN_83	R5FSS1_CORE0	ECAP0 interrupt request	pulse
ECAP0	ECAP0_ecap_int_0	R5FSS1_CORE1_intr_IN_83	R5FSS1_CORE1	ECAP0 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	C7X256V0_CLEC_gic_spi_IN_146	C7X256V0_CLEC	ECAP1 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	C7X256V1_CLEC_gic_spi_IN_146	C7X256V1_CLEC	ECAP1 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	R5FSS0_CORE0_intr_IN_84	R5FSS0_CORE0	ECAP1 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	R5FSS0_CORE1_intr_IN_84	R5FSS0_CORE1	ECAP1 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	R5FSS1_CORE0_intr_IN_84	R5FSS1_CORE0	ECAP1 interrupt request	pulse
ECAP1	ECAP1_ecap_int_0	R5FSS1_CORE1_intr_IN_84	R5FSS1_CORE1	ECAP1 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	C7X256V0_CLEC_gic_spi_IN_147	C7X256V0_CLEC	ECAP2 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	C7X256V1_CLEC_gic_spi_IN_147	C7X256V1_CLEC	ECAP2 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	R5FSS0_CORE0_intr_IN_85	R5FSS0_CORE0	ECAP2 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	R5FSS0_CORE1_intr_IN_85	R5FSS0_CORE1	ECAP2 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	R5FSS1_CORE0_intr_IN_85	R5FSS1_CORE0	ECAP2 interrupt request	pulse
ECAP2	ECAP2_ecap_int_0	R5FSS1_CORE1_intr_IN_85	R5FSS1_CORE1	ECAP2 interrupt request	pulse
ECAP3	ECAP3_ecap_int_0	C7X256V0_CLEC_gic_spi_IN_148	C7X256V0_CLEC	ECAP3 interrupt request	pulse

Table 4-118. ECAP Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ECAP3	ECAP3_ecap_int_0	C7X256V1_CLEC_gic_spi_IN_148	C7X256V1_CLEC	ECAP3 interrupt request	pulse
ECAP3	ECAP3_ecap_int_0	R5FSS0_CORE0_intr_IN_86	R5FSS0_CORE0	ECAP3 interrupt request	pulse
ECAP3	ECAP3_ecap_int_0	R5FSS0_CORE1_intr_IN_86	R5FSS0_CORE1	ECAP3 interrupt request	pulse
ECAP3	ECAP3_ecap_int_0	R5FSS1_CORE0_intr_IN_86	R5FSS1_CORE0	ECAP3 interrupt request	pulse
ECAP3	ECAP3_ecap_int_0	R5FSS1_CORE1_intr_IN_86	R5FSS1_CORE1	ECAP3 interrupt request	pulse
ECAP4	ECAP4_ecap_int_0	C7X256V0_CLEC_gic_spi_IN_149	C7X256V0_CLEC	ECAP4 interrupt request	pulse
ECAP4	ECAP4_ecap_int_0	C7X256V1_CLEC_gic_spi_IN_149	C7X256V1_CLEC	ECAP4 interrupt request	pulse
ECAP4	ECAP4_ecap_int_0	R5FSS0_CORE0_intr_IN_87	R5FSS0_CORE0	ECAP4 interrupt request	pulse
ECAP4	ECAP4_ecap_int_0	R5FSS0_CORE1_intr_IN_87	R5FSS0_CORE1	ECAP4 interrupt request	pulse
ECAP4	ECAP4_ecap_int_0	R5FSS1_CORE0_intr_IN_87	R5FSS1_CORE0	ECAP4 interrupt request	pulse
ECAP4	ECAP4_ecap_int_0	R5FSS1_CORE1_intr_IN_87	R5FSS1_CORE1	ECAP4 interrupt request	pulse
ECAP5	ECAP5_ecap_int_0	C7X256V0_CLEC_gic_spi_IN_150	C7X256V0_CLEC	ECAP5 interrupt request	pulse
ECAP5	ECAP5_ecap_int_0	C7X256V1_CLEC_gic_spi_IN_150	C7X256V1_CLEC	ECAP5 interrupt request	pulse
ECAP5	ECAP5_ecap_int_0	R5FSS0_CORE0_intr_IN_88	R5FSS0_CORE0	ECAP5 interrupt request	pulse
ECAP5	ECAP5_ecap_int_0	R5FSS0_CORE1_intr_IN_88	R5FSS0_CORE1	ECAP5 interrupt request	pulse
ECAP5	ECAP5_ecap_int_0	R5FSS1_CORE0_intr_IN_88	R5FSS1_CORE0	ECAP5 interrupt request	pulse
ECAP5	ECAP5_ecap_int_0	R5FSS1_CORE1_intr_IN_88	R5FSS1_CORE1	ECAP5 interrupt request	pulse

Table 4-119. ECAP Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
ECAP0	FICLK	MAIN_SYSCLK0/2		ECAP0 Functional and Interface Clock
ECAP1	FICLK	MAIN_SYSCLK0/2		ECAP1 Functional and Interface Clock
ECAP2	FICLK	MAIN_SYSCLK0/2		ECAP2 Functional and Interface Clock

Table 4-119. ECAP Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
ECAP3	FICLK	MAIN_SYSCLK0/2		ECAP3 Functional and Interface Clock
ECAP4	FICLK	MAIN_SYSCLK0/2		ECAP4 Functional and Interface Clock
ECAP5	FICLK	MAIN_SYSCLK0/2		ECAP5 Functional and Interface Clock

4.11.3 Enhanced Pulse Width Modulation (EPWM)

This section contains the integration details for the EPWM module on this device. For further information, see the *Enhanced Pulse Width Modulation (EPWM)* section of the *Peripherals* chapter.

4.11.3.1 EPWM Unsupported Features

The following features are not supported on this family of devices:

- EPWM digital comparators
- High resolution extension (delay-line based)

4.11.3.2 Module Allocations

Table 4-120. EPWM Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
EPWM0			✓
EPWM1			✓
EPWM2			✓

4.11.3.3 Resets, Interrupts, and Clocks

Table 4-121. EPWM Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
EPWM0	PSC0	GP_CORE_CTL	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
EPWM1	PSC0	GP_CORE_CTL	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
EPWM2	PSC0	GP_CORE_CTL	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO

Table 4-122. EPWM Resets

Module Instance	Source	Description
EPWM0	PSC0	EPWM0 reset
EPWM1	PSC0	EPWM1 reset
EPWM2	PSC0	EPWM2 reset

Table 4-123. EPWM Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
EPWM0	EPWM0_epwm_etint_0	C7X256V0_CLEC_gic_spi_IN_229	C7X256V0_CLEC	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_etint_0	C7X256V1_CLEC_gic_spi_IN_229	C7X256V1_CLEC	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_etint_0	WKUP_R5FSS0_CORE0_intr_IN_123	WKUP_R5FSS0_CORE0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_synco_o_0	TIMESYNC_INTROUTER0_in_IN_9	TIMESYNC_INTROUTER0	EPWM0 interrupt request	level

Table 4-123. EPWM Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
EPWM0	EPWM0_epwm_syncout_0	EPWM1_epwm_syncin_IN_0	EPWM1	EPWM0 interrupt request	level
EPWM0	EPWM0_epwm_tripzint_0	C7X256V0_CLEC_gic_spi_IN_230	C7X256V0_CLEC	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	C7X256V1_CLEC_gic_spi_IN_230	C7X256V1_CLEC	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	R5FSS0_CORE0_intr_IN_80	R5FSS0_CORE0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	R5FSS0_CORE1_intr_IN_80	R5FSS0_CORE1	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	R5FSS1_CORE0_intr_IN_80	R5FSS1_CORE0	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	R5FSS1_CORE1_intr_IN_80	R5FSS1_CORE1	EPWM0 interrupt request	pulse
EPWM0	EPWM0_epwm_tripzint_0	WKUP_R5FSS0_CORE0_intr_IN_124	WKUP_R5FSS0_CORE0	EPWM0 interrupt request	pulse
EPWM1	EPWM1_epwm_etint_0	C7X256V0_CLEC_gic_spi_IN_231	C7X256V0_CLEC	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_etint_0	C7X256V1_CLEC_gic_spi_IN_231	C7X256V1_CLEC	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_etint_0	WKUP_R5FSS0_CORE0_intr_IN_125	WKUP_R5FSS0_CORE0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_syncout_0	EPWM2_epwm_syncin_IN_0	EPWM2	EPWM1 interrupt request	level
EPWM1	EPWM1_epwm_tripzint_0	C7X256V0_CLEC_gic_spi_IN_233	C7X256V0_CLEC	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	C7X256V1_CLEC_gic_spi_IN_233	C7X256V1_CLEC	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	R5FSS0_CORE0_intr_IN_81	R5FSS0_CORE0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	R5FSS0_CORE1_intr_IN_81	R5FSS0_CORE1	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	R5FSS1_CORE0_intr_IN_81	R5FSS1_CORE0	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	R5FSS1_CORE1_intr_IN_81	R5FSS1_CORE1	EPWM1 interrupt request	pulse
EPWM1	EPWM1_epwm_tripzint_0	WKUP_R5FSS0_CORE0_intr_IN_126	WKUP_R5FSS0_CORE0	EPWM1 interrupt request	pulse
EPWM2	EPWM2_epwm_etint_0	C7X256V0_CLEC_gic_spi_IN_234	C7X256V0_CLEC	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_etint_0	C7X256V1_CLEC_gic_spi_IN_234	C7X256V1_CLEC	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_etint_0	WKUP_R5FSS0_CORE0_intr_IN_127	WKUP_R5FSS0_CORE0	EPWM2 interrupt request	pulse

Table 4-123. EPWM Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
EPWM2	EPWM2_epwm_tripzint_0	C7X256V0_CLEC_gic_spi_IN_235	C7X256V0_CLEC	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	C7X256V1_CLEC_gic_spi_IN_235	C7X256V1_CLEC	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	R5FSS0_CORE0_intr_IN_82	R5FSS0_CORE0	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	R5FSS0_CORE1_intr_IN_82	R5FSS0_CORE1	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	R5FSS1_CORE0_intr_IN_82	R5FSS1_CORE0	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	R5FSS1_CORE1_intr_IN_82	R5FSS1_CORE1	EPWM2 interrupt request	pulse
EPWM2	EPWM2_epwm_tripzint_0	WKUP_R5FSS0_CORE0_intr_IN_148	WKUP_R5FSS0_CORE0	EPWM2 interrupt request	pulse

Table 4-124. EPWM Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
EPWM0	FICLK	MAIN_SYSCLK0/2		EPWM0 Functional and Interface Clock
EPWM1	FICLK	MAIN_SYSCLK0/2		EPWM1 Functional and Interface Clock
EPWM2	FICLK	MAIN_SYSCLK0/2		EPWM2 Functional and Interface Clock

4.12 Timer Modules

4.12.1 Global Timebase Counter (GTC)

This section contains the integration details for the GTC module on this device. For further information, see the *Global Timebase Counter (GTC)* section of the *Peripherals* chapter.

4.12.1.1 GTC Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.12.1.2 Module Allocations

Table 4-125. GTC Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
WKUP_GTC0	✓		

4.12.1.3 Resets, Interrupts, and Clocks

Table 4-126. GTC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
WKUP_GTC0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE

Table 4-127. GTC Resets

Module Instance	Source	Description
WKUP_GTC0	MAIN_PSC0	WKUP_GTC0 reset
WKUP_GTC0	PLLCTRL0	WKUP_GTC0 reset

Table 4-128. GTC Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_GTC0	WKUP_GTC0_gtc_push_event_0	TIMESYNC_EVENT_ROUTER0_in_IN_11	TIMESYNC_EVENT_ROUTER0	WKUP_GTC0 interrupt request	pulse

Table 4-129. GTC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
WKUP_GTC0	CLK	MAIN_PLL2_HSDIV5_CLKOUT	WKUP_GTC_CLKSEL[2:0]	WKUP_GTC0 Functional Clock
		MAIN_PLL0_HSDIV6_CLKOUT		
		CP_GEMAC_CPTS_REF_CLK		
		MCU_EXT_REFCLK0		
		EXT_REFCLK1		
		MCU_SYSCLK0/2		
		MAIN_SYSCLK0		
	ICLK	DM_CLK/4	WKUP_CLKSEL[0:0]	WKUP_GTC0 Interface Clock

4.12.2 Real Time Interrupt (RTI)

This section contains the integration details for the RTI module on this device. For further information, see the *Real Time Interrupt (RTI)* section of the *Peripherals* chapter.

4.12.2.1 RTI Not Supported Features

The following features are not supported on this family of devices:

- Analog watchdog timer
- External clock supervision
- Periodic interrupt
- Timestamp (Capture registers)

4.12.2.2 Module Allocations

Table 4-130. RTI Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
RTI0			✓
RTI1			✓
RTI2			✓
RTI3			✓
RTI4			✓
RTI5			✓
WKUP_RTI0	✓		

4.12.2.3 Resets, Interrupts, and Clocks

Table 4-131. RTI Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
RTI0	MAIN_PSC0	R5SS_0	LPSC_MAIN_R5SS0_CORE0	52	OFF	YES	LPSC_MAIN_IP0
RTI1	MAIN_PSC0	R5SS_0	LPSC_MAIN_R5SS0_CORE1	53	OFF	YES	LPSC_MAIN_IP0
RTI2	MAIN_PSC0	R5SS_1	LPSC_MAIN_R5SS1_CORE0	55	OFF	YES	LPSC_MAIN_IP0
RTI3	MAIN_PSC0	R5SS_1	LPSC_MAIN_R5SS1_CORE1	56	OFF	YES	LPSC_MAIN_IP0
RTI4	MAIN_PSC0	C7X0	LPSC_MAIN_C7X0_CORE	59	OFF	YES	LPSC_MAIN_C7X0_COMMON
RTI5	MAIN_PSC0	C7X1	LPSC_MAIN_C7X1_CORE	62	OFF	YES	LPSC_MAIN_C7X1_COMMON
WKUP_RTI0	MAIN_PSC0	GP_CORE	LPSC_MAIN_DM	1	OFF	YES	LPSC_MAIN_ALWAYSON

Table 4-132. RTI Resets

Module Instance	Source	Description
RTI0	MAIN_PSC0	RTI0 reset
RTI1	MAIN_PSC0	RTI1 reset
RTI2	MAIN_PSC0	RTI2 reset

Table 4-132. RTI Resets (continued)

Module Instance	Source	Description
RTI3	MAIN_PSC0	RTI3 reset
RTI4	MAIN_PSC0	RTI4 reset
RTI5	MAIN_PSC0	RTI5 reset
WKUP_RTI0	MAIN_PSC0	WKUP_RTI0 reset

Table 4-133. RTI Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
RTI0	RTI0_intr_wwd_0	ESM0_esm_pls_event0_IN_224	ESM0	RTI0 interrupt request	pulse
RTI0	RTI0_intr_wwd_0	ESM0_esm_pls_event1_IN_224	ESM0	RTI0 interrupt request	pulse
RTI0	RTI0_intr_wwd_0	ESM0_esm_pls_event2_IN_224	ESM0	RTI0 interrupt request	pulse
RTI0	RTI0_intr_wwd_0	R5FSS0_CORE0_intr_IN_30	R5FSS0_CORE0	RTI0 interrupt request	pulse
RTI1	RTI1_intr_wwd_0	ESM0_esm_pls_event0_IN_225	ESM0	RTI1 interrupt request	pulse
RTI1	RTI1_intr_wwd_0	ESM0_esm_pls_event1_IN_225	ESM0	RTI1 interrupt request	pulse
RTI1	RTI1_intr_wwd_0	ESM0_esm_pls_event2_IN_225	ESM0	RTI1 interrupt request	pulse
RTI1	RTI1_intr_wwd_0	R5FSS0_CORE1_intr_IN_30	R5FSS0_CORE1	RTI1 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	ESM0_esm_pls_event0_IN_241	ESM0	RTI2 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	ESM0_esm_pls_event1_IN_241	ESM0	RTI2 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	ESM0_esm_pls_event2_IN_241	ESM0	RTI2 interrupt request	pulse
RTI2	RTI2_intr_wwd_0	R5FSS1_CORE0_intr_IN_30	R5FSS1_CORE0	RTI2 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	ESM0_esm_pls_event0_IN_242	ESM0	RTI3 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	ESM0_esm_pls_event1_IN_242	ESM0	RTI3 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	ESM0_esm_pls_event2_IN_242	ESM0	RTI3 interrupt request	pulse
RTI3	RTI3_intr_wwd_0	R5FSS1_CORE1_intr_IN_30	R5FSS1_CORE1	RTI3 interrupt request	pulse
RTI4	RTI4_intr_wwd_0	C7X256V0_CLEC_soc_events_in_IN_4	C7X256V0_CLEC	RTI4 interrupt request	pulse
RTI4	RTI4_intr_wwd_0	ESM0_esm_pls_event0_IN_252	ESM0	RTI4 interrupt request	pulse

Table 4-133. RTI Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
RTI4	RTI4_intr_wwd_0	ESM0_esm_pls_event1_IN_252	ESM0	RTI4 interrupt request	pulse
RTI4	RTI4_intr_wwd_0	ESM0_esm_pls_event2_IN_252	ESM0	RTI4 interrupt request	pulse
RTI5	RTI5_intr_wwd_0	C7X256V1_CLEC_soc_events_in_IN_4	C7X256V1_CLEC	RTI5 interrupt request	pulse
RTI5	RTI5_intr_wwd_0	ESM0_esm_pls_event0_IN_253	ESM0	RTI5 interrupt request	pulse
RTI5	RTI5_intr_wwd_0	ESM0_esm_pls_event1_IN_253	ESM0	RTI5 interrupt request	pulse
RTI5	RTI5_intr_wwd_0	ESM0_esm_pls_event2_IN_253	ESM0	RTI5 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	WKUP_ESM0_esm_pls_event0_IN_86	WKUP_ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	WKUP_ESM0_esm_pls_event1_IN_86	WKUP_ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	WKUP_ESM0_esm_pls_event2_IN_86	WKUP_ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	ESM0_esm_pls_event0_IN_227	ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	ESM0_esm_pls_event1_IN_227	ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	ESM0_esm_pls_event2_IN_227	ESM0	WKUP_RTI0 interrupt request	pulse
WKUP_RTI0	WKUP_RTI0_intr_wwd_0	WKUP_R5FSS0_CORE0_intr_IN_30	WKUP_R5FSS0_CORE0	WKUP_RTI0 interrupt request	pulse

Table 4-134. RTI Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
RTI0	FCLK	HFOSC0_CLKOUT	WWD0_CLKSEL[1:0]	RTI0 Functional Clock
		DEVICE_CLKOUT_32K	WWD0_CLKSEL[1:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		CLK_12M_RC	WWD0_CLKSEL[1:0]	
		CLK_32K_RC	WWD0_CLKSEL[1:0]	
	ICLK	MAIN_SYSCLK0/4		RTI0 Interface Clock
RTI1	FCLK	HFOSC0_CLKOUT	WWD1_CLKSEL[1:0]	RTI1 Functional Clock
		DEVICE_CLKOUT_32K	WWD1_CLKSEL[1:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		CLK_12M_RC	WWD1_CLKSEL[1:0]	
		CLK_32K_RC	WWD1_CLKSEL[1:0]	
	ICLK	MAIN_SYSCLK0/4		RTI1 Interface Clock

Table 4-134. RTI Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
RTI2	FCLK	HFOSC0_CLKOUT	WWD2_CLKSEL[1:0]	RTI2 Functional Clock
		DEVICE_CLKOUT_32K	WWD2_CLKSEL[1:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		CLK_12M_RC	WWD2_CLKSEL[1:0]	
		CLK_32K_RC	WWD2_CLKSEL[1:0]	
	ICLK	MAIN_SYSCLK0/4		RTI2 Interface Clock
RTI3	FCLK	HFOSC0_CLKOUT	WWD3_CLKSEL[1:0]	RTI3 Functional Clock
		DEVICE_CLKOUT_32K	WWD3_CLKSEL[1:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		CLK_12M_RC	WWD3_CLKSEL[1:0]	
		CLK_32K_RC	WWD3_CLKSEL[1:0]	
	ICLK	MAIN_SYSCLK0/4		RTI3 Interface Clock
RTI4	FCLK	HFOSC0_CLKOUT	WWD4_CLKSEL[1:0]	RTI4 Functional Clock
		DEVICE_CLKOUT_32K	WWD4_CLKSEL[1:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		CLK_12M_RC	WWD4_CLKSEL[1:0]	
		CLK_32K_RC	WWD4_CLKSEL[1:0]	
	ICLK	MAIN_SYSCLK0/4		RTI4 Interface Clock
RTI5	FCLK	HFOSC0_CLKOUT	WWD5_CLKSEL[1:0]	RTI5 Functional Clock
		DEVICE_CLKOUT_32K	WWD5_CLKSEL[1:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		CLK_12M_RC	WWD5_CLKSEL[1:0]	
		CLK_32K_RC	WWD5_CLKSEL[1:0]	
	ICLK	MAIN_SYSCLK0/4		RTI5 Interface Clock
WKUP_RTI0	FCLK	HFOSC0_CLKOUT	WKUP_WWD0_CLKSEL[1:0]	WKUP_RTI0 Functional Clock
		DEVICE_CLKOUT_32K	WKUP_WWD0_CLKSEL[1:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		CLK_12M_RC	WKUP_WWD0_CLKSEL[1:0]	
		CLK_32K_RC	WKUP_WWD0_CLKSEL[1:0]	
	ICLK	DM_CLK/4	WKUP_CLKSEL[0:0]	WKUP_RTI0 Interface Clock

4.12.3 Real-Time Clock (RTC)

This section contains the integration details for the RTC module on this device. For further information, see the *Real-Time Clock (RTC)* section of the *Peripherals* chapter.

4.12.3.1 RTC Unsupported Features

The following features are not supported on this family of devices:

- PMIC enable support
- Analog IP support
- External IO
- Two digital voltage domains

4.12.3.2 Module Allocations

Table 4-135. RTC Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
WKUP_rtcss0	✓		

4.12.3.3 Resets, Interrupts, and Clocks

Table 4-136. RTC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
WKUP_rtcss0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE

Table 4-137. RTC Resets

Module Instance	Source	Description
WKUP_rtcss0	MAIN_PSC0	WKUP_rtcss0 reset

Table 4-138. RTC Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	C7X256V0_CLEC_gic_spi_IN_132	C7X256V0_CLEC	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	C7X256V1_CLEC_gic_spi_IN_132	C7X256V1_CLEC	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	R5FSS0_CORE0_intr_IN_97	R5FSS0_CORE0	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	R5FSS0_CORE1_intr_IN_97	R5FSS0_CORE1	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	R5FSS1_CORE0_intr_IN_97	R5FSS1_CORE0	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	R5FSS1_CORE1_intr_IN_97	R5FSS1_CORE1	WKUP_rtcss0 interrupt request	level
WKUP_rtcss0	WKUP_rtcss0_rtc_event_pend_0	WKUP_R5FSS0_CORE0_intr_IN_97	WKUP_R5FSS0_CORE0	WKUP_rtcss0 interrupt request	level

Table 4-139. RTC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
WKUP_rtcss0	ANA_OSC32K_CLK	DEVICE_CLKOUT_32K	WKUP_RTC_CLKSEL[0:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		CLK_32K_RC	WKUP_RTC_CLKSEL[0:0]	
	VCLK_CLK	DM_CLK/8	WKUP_CLKSEL[0:0]	

4.12.4 Timer

This section contains the integration details for the Timer module on this device. For further information, see the *Timer* section of the *Peripherals* chapter.

4.12.4.1 Timer Unsupported Features

The following features are not supported on this family of devices:

- Cascading of timer instances

4.12.4.2 Module Allocations

Table 4-140. Timer Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
TIMER0			✓
TIMER1			✓
TIMER2			✓
TIMER3			✓
TIMER4			✓
TIMER5			✓
TIMER6			✓
TIMER7			✓
TIMER8			✓
TIMER9			✓
TIMER10			✓
TIMER11			✓
TIMER12			✓
TIMER13			✓
TIMER14			✓
TIMER15			✓
WKUP_TIMER0	✓		
WKUP_TIMER1	✓		

4.12.4.3 Resets, Interrupts, and Clocks

Table 4-141. Timer Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
TIMER0	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER1	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER10	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO

Table 4-141. Timer Integration Attributes (continued)

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
TIMER11	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER12	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER13	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER14	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER15	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER2	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER3	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER4	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER5	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER6	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER7	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER8	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
TIMER9	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO
WKUP_TIMER0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
WKUP_TIMER1	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE

Table 4-142. Timer Resets

Module Instance	Source	Description
TIMER0	MAIN_PSC0	TIMER0 reset
TIMER1	MAIN_PSC0	TIMER1 reset
TIMER2	MAIN_PSC0	TIMER2 reset
TIMER3	MAIN_PSC0	TIMER3 reset
TIMER4	MAIN_PSC0	TIMER4 reset
TIMER5	MAIN_PSC0	TIMER5 reset
TIMER6	MAIN_PSC0	TIMER6 reset
TIMER7	MAIN_PSC0	TIMER7 reset
TIMER8	MAIN_PSC0	TIMER8 reset
TIMER9	MAIN_PSC0	TIMER9 reset
TIMER10	MAIN_PSC0	TIMER10 reset
TIMER11	MAIN_PSC0	TIMER11 reset
TIMER12	MAIN_PSC0	TIMER12 reset
TIMER13	MAIN_PSC0	TIMER13 reset
TIMER14	MAIN_PSC0	TIMER14 reset
TIMER15	MAIN_PSC0	TIMER15 reset
WKUP_TIMER0	MAIN_PSC0	WKUP_TIMER0 reset
WKUP_TIMER1	MAIN_PSC0	WKUP_TIMER1 reset

Table 4-143. Timer Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER0	TIMER0_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_152	C7X256V0_CLEC	TIMER0 interrupt request	level
TIMER0	TIMER0_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_152	C7X256V1_CLEC	TIMER0 interrupt request	level
TIMER0	TIMER0_intr_pend_0	R5FSS0_CORE0_intr_IN_24	R5FSS0_CORE0	TIMER0 interrupt request	level
TIMER0	TIMER0_intr_pend_0	R5FSS0_CORE1_intr_IN_24	R5FSS0_CORE1	TIMER0 interrupt request	level
TIMER0	TIMER0_intr_pend_0	R5FSS1_CORE0_intr_IN_24	R5FSS1_CORE0	TIMER0 interrupt request	level
TIMER0	TIMER0_intr_pend_0	R5FSS1_CORE1_intr_IN_24	R5FSS1_CORE1	TIMER0 interrupt request	level
TIMER0	TIMER0_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_216	MAIN_GPIO_INTROUTER0	TIMER0 interrupt request	pulse
TIMER0	TIMER0_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_0	TIMESYNC_INTROUTER0	TIMER0 interrupt request	pulse
TIMER1	TIMER1_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_153	C7X256V0_CLEC	TIMER1 interrupt request	level
TIMER1	TIMER1_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_153	C7X256V1_CLEC	TIMER1 interrupt request	level

Table 4-143. Timer Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER1	TIMER1_intr_pend_0	R5FSS0_CORE0_intr_IN_25	R5FSS0_CORE0	TIMER1 interrupt request	level
TIMER1	TIMER1_intr_pend_0	R5FSS0_CORE1_intr_IN_25	R5FSS0_CORE1	TIMER1 interrupt request	level
TIMER1	TIMER1_intr_pend_0	R5FSS1_CORE0_intr_IN_25	R5FSS1_CORE0	TIMER1 interrupt request	level
TIMER1	TIMER1_intr_pend_0	R5FSS1_CORE1_intr_IN_25	R5FSS1_CORE1	TIMER1 interrupt request	level
TIMER1	TIMER1_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_217	MAIN_GPIO_INTROUTER0	TIMER1 interrupt request	pulse
TIMER1	TIMER1_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_1	TIMESYNC_INTROUTER0	TIMER1 interrupt request	pulse
TIMER2	TIMER2_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_154	C7X256V0_CLEC	TIMER2 interrupt request	level
TIMER2	TIMER2_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_154	C7X256V1_CLEC	TIMER2 interrupt request	level
TIMER2	TIMER2_intr_pend_0	R5FSS0_CORE0_intr_IN_26	R5FSS0_CORE0	TIMER2 interrupt request	level
TIMER2	TIMER2_intr_pend_0	R5FSS0_CORE1_intr_IN_26	R5FSS0_CORE1	TIMER2 interrupt request	level
TIMER2	TIMER2_intr_pend_0	R5FSS1_CORE0_intr_IN_26	R5FSS1_CORE0	TIMER2 interrupt request	level
TIMER2	TIMER2_intr_pend_0	R5FSS1_CORE1_intr_IN_26	R5FSS1_CORE1	TIMER2 interrupt request	level
TIMER2	TIMER2_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_218	MAIN_GPIO_INTROUTER0	TIMER2 interrupt request	pulse
TIMER2	TIMER2_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_2	TIMESYNC_INTROUTER0	TIMER2 interrupt request	pulse
TIMER3	TIMER3_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_155	C7X256V0_CLEC	TIMER3 interrupt request	level
TIMER3	TIMER3_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_155	C7X256V1_CLEC	TIMER3 interrupt request	level
TIMER3	TIMER3_intr_pend_0	R5FSS0_CORE0_intr_IN_27	R5FSS0_CORE0	TIMER3 interrupt request	level
TIMER3	TIMER3_intr_pend_0	R5FSS0_CORE1_intr_IN_27	R5FSS0_CORE1	TIMER3 interrupt request	level
TIMER3	TIMER3_intr_pend_0	R5FSS1_CORE0_intr_IN_27	R5FSS1_CORE0	TIMER3 interrupt request	level
TIMER3	TIMER3_intr_pend_0	R5FSS1_CORE1_intr_IN_27	R5FSS1_CORE1	TIMER3 interrupt request	level
TIMER3	TIMER3_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_219	MAIN_GPIO_INTROUTER0	TIMER3 interrupt request	pulse
TIMER3	TIMER3_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_3	TIMESYNC_INTROUTER0	TIMER3 interrupt request	pulse

Table 4-143. Timer Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER4	TIMER4_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_156	C7X256V0_CLEC	TIMER4 interrupt request	level
TIMER4	TIMER4_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_156	C7X256V1_CLEC	TIMER4 interrupt request	level
TIMER4	TIMER4_intr_pend_0	R5FSS0_CORE0_intr_IN_28	R5FSS0_CORE0	TIMER4 interrupt request	level
TIMER4	TIMER4_intr_pend_0	R5FSS0_CORE1_intr_IN_28	R5FSS0_CORE1	TIMER4 interrupt request	level
TIMER4	TIMER4_intr_pend_0	R5FSS1_CORE0_intr_IN_28	R5FSS1_CORE0	TIMER4 interrupt request	level
TIMER4	TIMER4_intr_pend_0	R5FSS1_CORE1_intr_IN_28	R5FSS1_CORE1	TIMER4 interrupt request	level
TIMER4	TIMER4_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_220	MAIN_GPIO_INTROUTER0	TIMER4 interrupt request	pulse
TIMER4	TIMER4_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_4	TIMESYNC_INTROUTER0	TIMER4 interrupt request	pulse
TIMER5	TIMER5_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_157	C7X256V0_CLEC	TIMER5 interrupt request	level
TIMER5	TIMER5_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_157	C7X256V1_CLEC	TIMER5 interrupt request	level
TIMER5	TIMER5_intr_pend_0	R5FSS0_CORE0_intr_IN_29	R5FSS0_CORE0	TIMER5 interrupt request	level
TIMER5	TIMER5_intr_pend_0	R5FSS0_CORE1_intr_IN_29	R5FSS0_CORE1	TIMER5 interrupt request	level
TIMER5	TIMER5_intr_pend_0	R5FSS1_CORE0_intr_IN_29	R5FSS1_CORE0	TIMER5 interrupt request	level
TIMER5	TIMER5_intr_pend_0	R5FSS1_CORE1_intr_IN_29	R5FSS1_CORE1	TIMER5 interrupt request	level
TIMER5	TIMER5_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_221	MAIN_GPIO_INTROUTER0	TIMER5 interrupt request	pulse
TIMER5	TIMER5_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_5	TIMESYNC_INTROUTER0	TIMER5 interrupt request	pulse
TIMER6	TIMER6_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_158	C7X256V0_CLEC	TIMER6 interrupt request	level
TIMER6	TIMER6_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_158	C7X256V1_CLEC	TIMER6 interrupt request	level
TIMER6	TIMER6_intr_pend_0	R5FSS0_CORE0_intr_IN_22	R5FSS0_CORE0	TIMER6 interrupt request	level
TIMER6	TIMER6_intr_pend_0	R5FSS0_CORE1_intr_IN_22	R5FSS0_CORE1	TIMER6 interrupt request	level
TIMER6	TIMER6_intr_pend_0	R5FSS1_CORE0_intr_IN_22	R5FSS1_CORE0	TIMER6 interrupt request	level
TIMER6	TIMER6_intr_pend_0	R5FSS1_CORE1_intr_IN_22	R5FSS1_CORE1	TIMER6 interrupt request	level

Table 4-143. Timer Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER6	TIMER6_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_222	MAIN_GPIO_INTROUTER0	TIMER6 interrupt request	pulse
TIMER6	TIMER6_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_6	TIMESYNC_INTROUTER0	TIMER6 interrupt request	pulse
TIMER7	TIMER7_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_159	C7X256V0_CLEC	TIMER7 interrupt request	level
TIMER7	TIMER7_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_159	C7X256V1_CLEC	TIMER7 interrupt request	level
TIMER7	TIMER7_intr_pend_0	R5FSS0_CORE0_intr_IN_23	R5FSS0_CORE0	TIMER7 interrupt request	level
TIMER7	TIMER7_intr_pend_0	R5FSS0_CORE1_intr_IN_23	R5FSS0_CORE1	TIMER7 interrupt request	level
TIMER7	TIMER7_intr_pend_0	R5FSS1_CORE0_intr_IN_23	R5FSS1_CORE0	TIMER7 interrupt request	level
TIMER7	TIMER7_intr_pend_0	R5FSS1_CORE1_intr_IN_23	R5FSS1_CORE1	TIMER7 interrupt request	level
TIMER7	TIMER7_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_223	MAIN_GPIO_INTROUTER0	TIMER7 interrupt request	pulse
TIMER7	TIMER7_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_7	TIMESYNC_INTROUTER0	TIMER7 interrupt request	pulse
TIMER8	TIMER8_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_64	C7X256V0_CLEC	TIMER8 interrupt request	level
TIMER8	TIMER8_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_64	C7X256V1_CLEC	TIMER8 interrupt request	level
TIMER8	TIMER8_intr_pend_0	R5FSS0_CORE0_intr_IN_264	R5FSS0_CORE0	TIMER8 interrupt request	level
TIMER8	TIMER8_intr_pend_0	R5FSS0_CORE1_intr_IN_264	R5FSS0_CORE1	TIMER8 interrupt request	level
TIMER8	TIMER8_intr_pend_0	R5FSS1_CORE0_intr_IN_264	R5FSS1_CORE0	TIMER8 interrupt request	level
TIMER8	TIMER8_intr_pend_0	R5FSS1_CORE1_intr_IN_264	R5FSS1_CORE1	TIMER8 interrupt request	level
TIMER8	TIMER8_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_224	MAIN_GPIO_INTROUTER0	TIMER8 interrupt request	pulse
TIMER8	TIMER8_timer_pwm_0	TIMESYNC_INTROUTER0_in_IN_8	TIMESYNC_INTROUTER0	TIMER8 interrupt request	pulse
TIMER9	TIMER9_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_65	C7X256V0_CLEC	TIMER9 interrupt request	level
TIMER9	TIMER9_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_65	C7X256V1_CLEC	TIMER9 interrupt request	level
TIMER9	TIMER9_intr_pend_0	R5FSS0_CORE0_intr_IN_265	R5FSS0_CORE0	TIMER9 interrupt request	level
TIMER9	TIMER9_intr_pend_0	R5FSS0_CORE1_intr_IN_265	R5FSS0_CORE1	TIMER9 interrupt request	level

Table 4-143. Timer Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER9	TIMER9_intr_pend_0	R5FSS1_CORE0_intr_IN_265	R5FSS1_CORE0	TIMER9 interrupt request	level
TIMER9	TIMER9_intr_pend_0	R5FSS1_CORE1_intr_IN_265	R5FSS1_CORE1	TIMER9 interrupt request	level
TIMER9	TIMER9_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_225	MAIN_GPIO_INTROUTER0	TIMER9 interrupt request	pulse
TIMER10	TIMER10_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_66	C7X256V0_CLEC	TIMER10 interrupt request	level
TIMER10	TIMER10_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_66	C7X256V1_CLEC	TIMER10 interrupt request	level
TIMER10	TIMER10_intr_pend_0	R5FSS0_CORE0_intr_IN_266	R5FSS0_CORE0	TIMER10 interrupt request	level
TIMER10	TIMER10_intr_pend_0	R5FSS0_CORE1_intr_IN_266	R5FSS0_CORE1	TIMER10 interrupt request	level
TIMER10	TIMER10_intr_pend_0	R5FSS1_CORE0_intr_IN_266	R5FSS1_CORE0	TIMER10 interrupt request	level
TIMER10	TIMER10_intr_pend_0	R5FSS1_CORE1_intr_IN_266	R5FSS1_CORE1	TIMER10 interrupt request	level
TIMER10	TIMER10_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_226	MAIN_GPIO_INTROUTER0	TIMER10 interrupt request	pulse
TIMER11	TIMER11_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_67	C7X256V0_CLEC	TIMER11 interrupt request	level
TIMER11	TIMER11_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_67	C7X256V1_CLEC	TIMER11 interrupt request	level
TIMER11	TIMER11_intr_pend_0	R5FSS0_CORE0_intr_IN_267	R5FSS0_CORE0	TIMER11 interrupt request	level
TIMER11	TIMER11_intr_pend_0	R5FSS0_CORE1_intr_IN_267	R5FSS0_CORE1	TIMER11 interrupt request	level
TIMER11	TIMER11_intr_pend_0	R5FSS1_CORE0_intr_IN_267	R5FSS1_CORE0	TIMER11 interrupt request	level
TIMER11	TIMER11_intr_pend_0	R5FSS1_CORE1_intr_IN_267	R5FSS1_CORE1	TIMER11 interrupt request	level
TIMER11	TIMER11_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_227	MAIN_GPIO_INTROUTER0	TIMER11 interrupt request	pulse
TIMER12	TIMER12_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_68	C7X256V0_CLEC	TIMER12 interrupt request	level
TIMER12	TIMER12_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_68	C7X256V1_CLEC	TIMER12 interrupt request	level
TIMER12	TIMER12_intr_pend_0	R5FSS0_CORE0_intr_IN_268	R5FSS0_CORE0	TIMER12 interrupt request	level
TIMER12	TIMER12_intr_pend_0	R5FSS0_CORE1_intr_IN_268	R5FSS0_CORE1	TIMER12 interrupt request	level
TIMER12	TIMER12_intr_pend_0	R5FSS1_CORE0_intr_IN_268	R5FSS1_CORE0	TIMER12 interrupt request	level

Table 4-143. Timer Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER12	TIMER12_intr_pend_0	R5FSS1_CORE1_intr_IN_268	R5FSS1_CORE1	TIMER12 interrupt request	level
TIMER12	TIMER12_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_228	MAIN_GPIO_INTROUTER0	TIMER12 interrupt request	pulse
TIMER13	TIMER13_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_69	C7X256V0_CLEC	TIMER13 interrupt request	level
TIMER13	TIMER13_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_69	C7X256V1_CLEC	TIMER13 interrupt request	level
TIMER13	TIMER13_intr_pend_0	R5FSS0_CORE0_intr_IN_269	R5FSS0_CORE0	TIMER13 interrupt request	level
TIMER13	TIMER13_intr_pend_0	R5FSS0_CORE1_intr_IN_269	R5FSS0_CORE1	TIMER13 interrupt request	level
TIMER13	TIMER13_intr_pend_0	R5FSS1_CORE0_intr_IN_269	R5FSS1_CORE0	TIMER13 interrupt request	level
TIMER13	TIMER13_intr_pend_0	R5FSS1_CORE1_intr_IN_269	R5FSS1_CORE1	TIMER13 interrupt request	level
TIMER13	TIMER13_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_229	MAIN_GPIO_INTROUTER0	TIMER13 interrupt request	pulse
TIMER14	TIMER14_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_70	C7X256V0_CLEC	TIMER14 interrupt request	level
TIMER14	TIMER14_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_70	C7X256V1_CLEC	TIMER14 interrupt request	level
TIMER14	TIMER14_intr_pend_0	R5FSS0_CORE0_intr_IN_270	R5FSS0_CORE0	TIMER14 interrupt request	level
TIMER14	TIMER14_intr_pend_0	R5FSS0_CORE1_intr_IN_270	R5FSS0_CORE1	TIMER14 interrupt request	level
TIMER14	TIMER14_intr_pend_0	R5FSS1_CORE0_intr_IN_270	R5FSS1_CORE0	TIMER14 interrupt request	level
TIMER14	TIMER14_intr_pend_0	R5FSS1_CORE1_intr_IN_270	R5FSS1_CORE1	TIMER14 interrupt request	level
TIMER14	TIMER14_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_230	MAIN_GPIO_INTROUTER0	TIMER14 interrupt request	pulse
TIMER15	TIMER15_intr_pend_0	C7X256V0_CLEC_gic_spi_IN_71	C7X256V0_CLEC	TIMER15 interrupt request	level
TIMER15	TIMER15_intr_pend_0	C7X256V1_CLEC_gic_spi_IN_71	C7X256V1_CLEC	TIMER15 interrupt request	level
TIMER15	TIMER15_intr_pend_0	R5FSS0_CORE0_intr_IN_271	R5FSS0_CORE0	TIMER15 interrupt request	level
TIMER15	TIMER15_intr_pend_0	R5FSS0_CORE1_intr_IN_271	R5FSS0_CORE1	TIMER15 interrupt request	level
TIMER15	TIMER15_intr_pend_0	R5FSS1_CORE0_intr_IN_271	R5FSS1_CORE0	TIMER15 interrupt request	level
TIMER15	TIMER15_intr_pend_0	R5FSS1_CORE1_intr_IN_271	R5FSS1_CORE1	TIMER15 interrupt request	level

Table 4-143. Timer Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
TIMER15	TIMER15_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_231	MAIN_GPIO_INTROUTER0	TIMER15 interrupt request	pulse
WKUP_TIMER0	WKUP_TIMER0_intr_pend_0	WKUP_R5FSS0_CORE0_intr_IN_138	WKUP_R5FSS0_CORE0	WKUP_TIMER0 interrupt request	level
WKUP_TIMER0	WKUP_TIMER0_timer_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_IN_28	WKUP_R5FSS0_CORE0	WKUP_TIMER0 interrupt request	level
WKUP_TIMER0	WKUP_TIMER0_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_214	MAIN_GPIO_INTROUTER0	WKUP_TIMER0 interrupt request	pulse
WKUP_TIMER1	WKUP_TIMER1_intr_pend_0	WKUP_R5FSS0_CORE0_intr_IN_139	WKUP_R5FSS0_CORE0	WKUP_TIMER1 interrupt request	level
WKUP_TIMER1	WKUP_TIMER1_timer_clkstop_wakeup_0	WKUP_R5FSS0_CORE0_intr_IN_29	WKUP_R5FSS0_CORE0	WKUP_TIMER1 interrupt request	level
WKUP_TIMER1	WKUP_TIMER1_timer_pwm_0	MAIN_GPIO_INTROUTER0_in_IN_215	MAIN_GPIO_INTROUTER0	WKUP_TIMER1 interrupt request	pulse

Table 4-144. Timer Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER0	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER0 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER0_CLKSEL[3:0]	TIMER0 Functional Clock
		DEVICE_CLKOUT_32K	TIMER0_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER0_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER0_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER0_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER0_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER0_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER0_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER0_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER0_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER0_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER0_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER0_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER0_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER0_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER0_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER0_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER0_CLKSEL[3:0]	
		CLK_12M_RC	TIMER0_CLKSEL[3:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER0_CLKSEL[3:0]	
		MAIN_PLL1_HSDIV3_CLKOUT	TIMER0_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV6_CLKOUT	TIMER0_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER1	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER1 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER1_CTRL[8:8]	TIMER1 Functional Clock
			TIMER1_CLKSEL[3:0]	
		DEVICE_CLKOUT_32K	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER1_CTRL[8:8]	
			TIMER1_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER2	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER2 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER2_CLKSEL[3:0]	TIMER2 Functional Clock
		DEVICE_CLKOUT_32K	TIMER2_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER2_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER2_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER2_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER2_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER2_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER2_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER2_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER2_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER2_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER2_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER2_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER2_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER2_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER2_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER2_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER2_CLKSEL[3:0]	
		CLK_12M_RC	TIMER2_CLKSEL[3:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER2_CLKSEL[3:0]	
		MAIN_PLL1_HSDIV3_CLKOUT	TIMER2_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV6_CLKOUT	TIMER2_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER3	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER3 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER3_CTRL[8:8]	TIMER3 Functional Clock
			TIMER3_CLKSEL[3:0]	
		DEVICE_CLKOUT_32K	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER3_CTRL[8:8]	
			TIMER3_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER4	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER4 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER4_CLKSEL[3:0]	TIMER4 Functional Clock
		DEVICE_CLKOUT_32K	TIMER4_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER4_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER4_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER4_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER4_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER4_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER4_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER4_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER4_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER4_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER4_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER4_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER4_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER4_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER4_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER4_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER4_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER4_CLKSEL[3:0]	
		CLK_12M_RC	TIMER4_CLKSEL[3:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER4_CLKSEL[3:0]	
		MAIN_PLL1_HSDIV3_CLKOUT	TIMER4_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV6_CLKOUT	TIMER4_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER5	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER5 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER5_CTRL[8:8]	TIMER5 Functional Clock
			TIMER5_CLKSEL[3:0]	
		DEVICE_CLKOUT_32K	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER5_CTRL[8:8]	
			TIMER5_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER6	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER6 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER6_CLKSEL[3:0]	TIMER6 Functional Clock
		DEVICE_CLKOUT_32K	TIMER6_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER6_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER6_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER6_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER6_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER6_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER6_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER6_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER6_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER6_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER6_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER6_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER6_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER6_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER6_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER6_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER6_CLKSEL[3:0]	
		CLK_12M_RC	TIMER6_CLKSEL[3:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER6_CLKSEL[3:0]	
		MAIN_PLL1_HSDIV3_CLKOUT	TIMER6_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV6_CLKOUT	TIMER6_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER7	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER7 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER7_CTRL[8:8]	TIMER7 Functional Clock
			TIMER7_CLKSEL[3:0]	
		DEVICE_CLKOUT_32K	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER7_CTRL[8:8]	
			TIMER7_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER8	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER8 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER8_CLKSEL[3:0]	TIMER8 Functional Clock
		DEVICE_CLKOUT_32K	TIMER8_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER8_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER8_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER8_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER8_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER8_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER8_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER8_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER8_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER8_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER8_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER8_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER8_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER8_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER8_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER8_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER8_CLKSEL[3:0]	
		CLK_12M_RC	TIMER8_CLKSEL[3:0]	
		MCU_EXT_REFCLK0	TIMER8_CLKSEL[3:0]	
		EXT_REFCLK1	TIMER8_CLKSEL[3:0]	
		MCU_TIEOFF0	TIMER8_CLKSEL[3:0]	
		MAIN_PLL1_HSDIV3_CLKOUT	TIMER8_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV6_CLKOUT	TIMER8_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER9	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER9 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER9_CTRL[8:8]	TIMER9 Functional Clock
			TIMER9_CLKSEL[3:0]	
		DEVICE_CLKOUT_32K	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER9_CTRL[8:8]	
			TIMER9_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER10	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER10 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER10_CLKSEL[3:0]	TIMER10 Functional Clock
		DEVICE_CLKOUT_32K	TIMER10_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER10_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER10_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER10_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER10_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER10_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER10_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER10_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER10_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER10_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER10_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER10_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER10_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER10_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER10_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER10_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER10_CLKSEL[3:0]	
		CLK_12M_RC	TIMER10_CLKSEL[3:0]	
		MCU_EXT_REFCLK0	TIMER10_CLKSEL[3:0]	
		MAIN_PLL1_HSDIV3_CLKOUT	TIMER10_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV6_CLKOUT	TIMER10_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER11	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER11 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER11_CTRL[8:8]	TIMER11 Functional Clock
			TIMER11_CLKSEL[3:0]	
		DEVICE_CLKOUT_32K	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
			]	
		MAIN_SYSCLK0/2	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER11_CTRL[8:8]	
			TIMER11_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER12	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER12 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER12_CLKSEL[3:0]	TIMER12 Functional Clock
		DEVICE_CLKOUT_32K	TIMER12_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER12_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER12_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER12_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER12_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER12_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER12_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER12_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER12_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER12_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER12_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER12_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER12_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER12_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER12_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER12_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER12_CLKSEL[3:0]	
		CLK_12M_RC	TIMER12_CLKSEL[3:0]	
		MAIN_PLL1_HSDIV3_CLKOUT	TIMER12_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV6_CLKOUT	TIMER12_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER13	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER13 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER13_CTRL[8:8]	TIMER13 Functional Clock
			TIMER13_CLKSEL[3:0]	
		DEVICE_CLKOUT_32K	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER13_CTRL[8:8]	
			TIMER13_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER14	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER14 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER14_CLKSEL[3:0]	TIMER14 Functional Clock
		DEVICE_CLKOUT_32K	TIMER14_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER14_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER14_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER14_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER14_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER14_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER14_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER14_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER14_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER14_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER14_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER14_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER14_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER14_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER14_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER14_CLKSEL[3:0]	
		MAIN_PLL0_HSDIV7_CLKOUT	TIMER14_CLKSEL[3:0]	
		CLK_12M_RC	TIMER14_CLKSEL[3:0]	
		MAIN_PLL1_HSDIV3_CLKOUT	TIMER14_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV6_CLKOUT	TIMER14_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
TIMER15	TIMER_ICLK	MAIN_SYSCLK0/4		TIMER15 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	TIMER15_CTRL[8:8]	TIMER15 Functional Clock
			TIMER15_CLKSEL[3:0]	
		DEVICE_CLKOUT_32K	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
		MAIN_PBIST_CLK	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/50	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	
		MAIN_PLL4_HSDIV2_CLKOUT	TIMER15_CTRL[8:8]	
			TIMER15_CLKSEL[3:0]	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
WKUP_TIMER0	TIMER_ICLK	DM_CLK/2	WKUP_CLKSEL[0:0]	WKUP_TIMER0 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	WKUP_TIMER0_CLKSEL[2:0]	WKUP_TIMER0 Functional Clock
		DM_CLK/2	WKUP_TIMER0_CLKSEL[2:0]	
			WKUP_CLKSEL[0:0]	
		CLK_12M_RC	WKUP_TIMER0_CLKSEL[2:0]	
		MCU_PLL0_HSDIV5_CLKOUT	WKUP_TIMER0_CLKSEL[2:0]	
		DEVICE_CLKOUT_32K	WKUP_TIMER0_CLKSEL[2:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	WKUP_TIMER0_CLKSEL[2:0]	
		MAIN_PBIST_CLK	WKUP_TIMER0_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	WKUP_TIMER0_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	WKUP_TIMER0_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	WKUP_TIMER0_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	WKUP_TIMER0_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		EXT_REFCLK1	WKUP_TIMER0_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL4_HSDIV1_CLKOUT	WKUP_TIMER0_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_SYSCLK0	WKUP_TIMER0_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/10	WKUP_TIMER0_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/2	WKUP_TIMER0_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT	WKUP_TIMER0_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CLKOUT/5	WKUP_TIMER0_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV1_CL	WKUP_TIMER0_CLKSEL[	

Table 4-144. Timer Clocks (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
WKUP_TIMER1	TIMER_ICLK	DM_CLK/2	WKUP_CLKSEL[0:0]	WKUP_TIMER1 Interface Clock
	TIMER_FCLK	HFOSC0_CLKOUT	WKUP_TIMER1_CTRL[8:8]	WKUP_TIMER1 Functional Clock
			WKUP_TIMER1_CLKSEL[2:0]	
		DM_CLK/2	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
			WKUP_CLKSEL[0:0]	
		CLK_12M_RC	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
		MCU_PLL0_HSDIV5_CLKOUT	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
		MCU_EXT_REFCLK0	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
		DEVICE_CLKOUT_32K	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
			DEVICE_CLKOUT_32K_CTRL[1:0]	
		MAIN_SYSCLK0/2	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
		MAIN_PBIST_CLK	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
		MAIN_PLL2_HSDIV5_CLKOUT	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		MAIN_PLL0_HSDIV6_CLKOUT	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[2:0]	
			CPSW_CLKSEL[2:0]	
		CP_GEMAC_CPTS_REF_CLK	WKUP_TIMER1_CTRL[8:8]	
			WKUP_TIMER1_CLKSEL[	

4.13 Internal Diagnostic Modules

4.13.1 Dual Clock Comparator (DCC)

This section contains the integration details for the DCC module on this device. For further information, see the *Dual Clock Comparator (DCC)* section of the *Peripherals* chapter.

4.13.1.1 DCC Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.13.1.2 Module Allocations

Table 4-145. DCC Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
DCC0			✓
DCC1			✓
DCC2			✓
DCC3			✓
DCC4			✓
DCC5			✓
DCC6			✓
DCC7			✓
DCC*			✓
MCU_DCC0		✓	
MCU_DCC1		✓	

4.13.1.3 Resets, Interrupts, and Clocks

Table 4-146. DCC Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
DCC0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
DCC1	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
DCC2	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
DCC3	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
DCC4	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
DCC5	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
DCC6	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
DCC7	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE

Table 4-146. DCC Integration Attributes (continued)

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
DCC8	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
MCU_DCC0	WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	NONE
MCU_DCC1	WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	NONE

Table 4-147. DCC Resets

Module Instance	Source	Description
DCC0	MAIN_PSC0	DCC0 reset
DCC1	MAIN_PSC0	DCC1 reset
DCC2	MAIN_PSC0	DCC2 reset
DCC3	MAIN_PSC0	DCC3 reset
DCC4	MAIN_PSC0	DCC4 reset
DCC5	MAIN_PSC0	DCC5 reset
DCC6	MAIN_PSC0	DCC6 reset
DCC7	MAIN_PSC0	DCC7 reset
DCC8	MAIN_PSC0	DCC8 reset
MCU_DCC0	WKUP_PSC0	MCU_DCC0 reset
MCU_DCC1	WKUP_PSC0	MCU_DCC1 reset

Table 4-148. DCC Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DCC0	DCC0_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC0 interrupt request	level
DCC0	DCC0_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC0 interrupt request	level
DCC0	DCC0_intr_err_level_0	ESM0_esm_lvl_event_IN_112	ESM0	DCC0 interrupt request	level
DCC1	DCC1_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC1 interrupt request	level

Table 4-148. DCC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DCC1	DCC1_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC1 interrupt request	level
DCC1	DCC1_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC1 interrupt request	level
DCC1	DCC1_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC1 interrupt request	level
DCC1	DCC1_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC1 interrupt request	level
DCC1	DCC1_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC1 interrupt request	level
DCC1	DCC1_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC1 interrupt request	level
DCC1	DCC1_intr_err_level_0	ESM0_esm_lvl_event_IN_113	ESM0	DCC1 interrupt request	level
DCC2	DCC2_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC2 interrupt request	level
DCC2	DCC2_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC2 interrupt request	level
DCC2	DCC2_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC2 interrupt request	level
DCC2	DCC2_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC2 interrupt request	level
DCC2	DCC2_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC2 interrupt request	level
DCC2	DCC2_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC2 interrupt request	level
DCC2	DCC2_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC2 interrupt request	level
DCC2	DCC2_intr_err_level_0	ESM0_esm_lvl_event_IN_114	ESM0	DCC2 interrupt request	level
DCC3	DCC3_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC3 interrupt request	level
DCC3	DCC3_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC3 interrupt request	level

Table 4-148. DCC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DCC3	DCC3_intr_err_level_0	ESM0_esm_lvl_event_IN_115	ESM0	DCC3 interrupt request	level
DCC4	DCC4_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC4 interrupt request	level
DCC4	DCC4_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC4 interrupt request	level
DCC4	DCC4_intr_err_level_0	ESM0_esm_lvl_event_IN_116	ESM0	DCC4 interrupt request	level
DCC5	DCC5_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC5 interrupt request	level
DCC5	DCC5_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC5 interrupt request	level
DCC5	DCC5_intr_err_level_0	ESM0_esm_lvl_event_IN_117	ESM0	DCC5 interrupt request	level
DCC6	DCC6_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC6 interrupt request	level
DCC6	DCC6_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC6 interrupt request	level
DCC6	DCC6_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC6 interrupt request	level
DCC6	DCC6_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC6 interrupt request	level
DCC6	DCC6_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC6 interrupt request	level

Table 4-148. DCC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DCC6	DCC6_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC6 interrupt request	level
DCC6	DCC6_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC6 interrupt request	level
DCC6	DCC6_intr_err_level_0	ESM0_esm_lvl_event_IN_79	ESM0	DCC6 interrupt request	level
DCC7	DCC7_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC7 interrupt request	level
DCC7	DCC7_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC7 interrupt request	level
DCC7	DCC7_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC7 interrupt request	level
DCC7	DCC7_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC7 interrupt request	level
DCC7	DCC7_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC7 interrupt request	level
DCC7	DCC7_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC7 interrupt request	level
DCC7	DCC7_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC7 interrupt request	level
DCC7	DCC7_intr_err_level_0	ESM0_esm_lvl_event_IN_73	ESM0	DCC7 interrupt request	level
DCC8	DCC8_intr_done_level_0	C7X256V0_CLEC_gic_spi_IN_128	C7X256V0_CLEC	DCC8 interrupt request	level
DCC8	DCC8_intr_done_level_0	C7X256V1_CLEC_gic_spi_IN_128	C7X256V1_CLEC	DCC8 interrupt request	level
DCC8	DCC8_intr_done_level_0	R5FSS0_CORE0_intr_IN_109	R5FSS0_CORE0	DCC8 interrupt request	level
DCC8	DCC8_intr_done_level_0	R5FSS0_CORE1_intr_IN_109	R5FSS0_CORE1	DCC8 interrupt request	level
DCC8	DCC8_intr_done_level_0	R5FSS1_CORE0_intr_IN_109	R5FSS1_CORE0	DCC8 interrupt request	level
DCC8	DCC8_intr_done_level_0	R5FSS1_CORE1_intr_IN_109	R5FSS1_CORE1	DCC8 interrupt request	level
DCC8	DCC8_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_109	WKUP_R5FSS0_CORE0	DCC8 interrupt request	level
DCC8	DCC8_intr_err_level_0	ESM0_esm_lvl_event_IN_223	ESM0	DCC8 interrupt request	level
MCU_DCC0	MCU_DCC0_intr_done_level_0	R5FSS0_CORE0_intr_IN_108	R5FSS0_CORE0	MCU_DCC0 interrupt request	level
MCU_DCC0	MCU_DCC0_intr_done_level_0	R5FSS0_CORE1_intr_IN_108	R5FSS0_CORE1	MCU_DCC0 interrupt request	level
MCU_DCC0	MCU_DCC0_intr_done_level_0	R5FSS1_CORE0_intr_IN_108	R5FSS1_CORE0	MCU_DCC0 interrupt request	level

Table 4-148. DCC Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCU_DCC0	MCU_DCC0_intr_done_level_0	R5FSS1_CORE1_intr_IN_108	R5FSS1_CORE1	MCU_DCC0 interrupt request	level
MCU_DCC0	MCU_DCC0_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_108	WKUP_R5FSS0_CORE0	MCU_DCC0 interrupt request	level
MCU_DCC0	MCU_DCC0_intr_err_level_0	WKUP_ESM0_esm_lvl_event_IN_37	WKUP_ESM0	MCU_DCC0 interrupt request	level
MCU_DCC1	MCU_DCC1_intr_done_level_0	R5FSS0_CORE0_intr_IN_137	R5FSS0_CORE0	MCU_DCC1 interrupt request	level
MCU_DCC1	MCU_DCC1_intr_done_level_0	R5FSS0_CORE1_intr_IN_137	R5FSS0_CORE1	MCU_DCC1 interrupt request	level
MCU_DCC1	MCU_DCC1_intr_done_level_0	R5FSS1_CORE0_intr_IN_137	R5FSS1_CORE0	MCU_DCC1 interrupt request	level
MCU_DCC1	MCU_DCC1_intr_done_level_0	R5FSS1_CORE1_intr_IN_137	R5FSS1_CORE1	MCU_DCC1 interrupt request	level
MCU_DCC1	MCU_DCC1_intr_done_level_0	WKUP_R5FSS0_CORE0_intr_IN_137	WKUP_R5FSS0_CORE0	MCU_DCC1 interrupt request	level
MCU_DCC1	MCU_DCC1_intr_err_level_0	WKUP_ESM0_esm_lvl_event_IN_36	WKUP_ESM0	MCU_DCC1 interrupt request	level

Table 4-149. DCC Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
DCC0	FICLK	MAIN_SYSCLK0/4		DCC0 Functional and Interface Clock
DCC1	FICLK	MAIN_SYSCLK0/4		DCC1 Functional and Interface Clock
DCC2	FICLK	MAIN_SYSCLK0/4		DCC2 Functional and Interface Clock
DCC3	FICLK	MAIN_SYSCLK0/4		DCC3 Functional and Interface Clock
DCC4	FICLK	MAIN_SYSCLK0/4		DCC4 Functional and Interface Clock
DCC5	FICLK	MAIN_SYSCLK0/4		DCC5 Functional and Interface Clock
DCC6	FICLK	MAIN_SYSCLK0/4		DCC6 Functional and Interface Clock
DCC7	FICLK	MAIN_SYSCLK0/4		DCC7 Functional and Interface Clock
DCC8	FICLK	MAIN_SYSCLK0/4		DCC8 Functional and Interface Clock
MCU_DCC0	FICLK	MCU_SYSCLK0/4		MCU_DCC0 Functional and Interface Clock
MCU_DCC1	FICLK	MCU_SYSCLK0/4		MCU_DCC1 Functional and Interface Clock

4.13.1.4 Input Source Clock Mapping

See the following tables for DCC Input Source Clock Mapping:

- Table 4-150
- Table 4-151
- Table 4-152
- Table 4-153
- Table 4-154
- Table 4-155
- Table 4-156
- Table 4-157
- Table 4-158

Table 4-150. MAIN_DCC0 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC0	dcc_clksrc0_clk	1	1	hsdiv4_16fft_main_0	hsdivout1_clk	MAIN_PLL0_HSDIV1_CLKOUT	
DCC0	dcc_clksrc1_clk	1	2	hsdiv4_16fft_main_0	hsdivout2_clk	MAIN_PLL0_HSDIV2_CLKOUT	
DCC0	dcc_clksrc2_clk	1	3	hsdiv4_16fft_main_0	hsdivout3_clk	MAIN_PLL0_HSDIV3_CLKOUT	
DCC0	dcc_clksrc3_clk	1	4	hsdiv4_16fft_main_0	hsdivout4_clk	MAIN_PLL0_HSDIV4_CLKOUT	
DCC0	dcc_clksrc4_clk	1	5	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
DCC0	dcc_clksrc5_clk	1	6	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1	
DCC0	dcc_clksrc6_clk	1	7	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	
DCC0	dcc_clksrc7_clk	1	8	postdiv4_16ff_main_2	hsdivout8_clk	MAIN_PLL2_HSDIV8_CLKOUT	
DCC0	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
DCC0	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1	
DCC0	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	
DCC0	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/2
DCC0	vbus_clk	1	9	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4

Table 4-151. MAIN_DCC1 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC1	dcc_clksrc0_clk	1	1	postdiv4_16ff_main_0	hsdivout5_clk	MAIN_PLL0_HSDIV5_CLKOUT	

Table 4-151. MAIN_DCC1 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC1	dcc_clksrc1_clk	1	2	postdiv4_16ff_main_0	hsdivout6_clk	MAIN_PLL0_HSDIV6_CLKOUT	
DCC1	dcc_clksrc2_clk	1	3	postdiv4_16ff_main_0	hsdivout7_clk	MAIN_PLL0_HSDIV7_CLKOUT	
DCC1	dcc_clksrc3_clk	1	4	hsdiv4_16fft_main_1	hsdivout1_clk	MAIN_PLL1_HSDIV1_CLKOUT	
DCC1	dcc_clksrc4_clk	1	5	hsdiv2_16fft_main_15	hsdivout2_clk	MAIN_PLL15_HSDIV2_CLKOUT	/4
DCC1	dcc_clksrc5_clk	1	6	hsdiv4_16fft_main_1	hsdivout0_clk	MAIN_PLL1_HSDIV0_CLKOUT	
DCC1	dcc_clksrc6_clk	1	7	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	
DCC1	dcc_clksrc7_clk	1	8	hsdiv4_16fft_main_1	hsdivout2_clk	MAIN_PLL1_HSDIV2_CLKOUT	
DCC1	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
DCC1	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1	
DCC1	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	
DCC1	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4
DCC1	vbus_clk	1	9	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4

Table 4-152. MAIN_DCC2 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC2	dcc_clksrc0_clk	1	1	hsdiv4_16fft_main_1	hsdivout3_clk	MAIN_PLL1_HSDIV3_CLKOUT	
DCC2	dcc_clksrc1_clk	1	2	hsdiv2_16fft_main_15	hsdivout0_clk	MAIN_PLL15_HSDIV0_CLKOUT	
DCC2	dcc_clksrc2_clk	1	3	postdiv1_16fft_main_1	hsdivout5_clk	MAIN_PLL1_HSDIV5_CLKOUT	
DCC2	dcc_clksrc3_clk	1	4	postdiv1_16fft_main_1	hsdivout6_clk	MAIN_PLL1_HSDIV6_CLKOUT	
DCC2	dcc_clksrc4_clk	1	5	hsdiv2_16fft_main_5	hsdivout1_clk	MAIN_PLL5_HSDIV1_CLKOUT	
DCC2	dcc_clksrc5_clk	1	6	hsdiv2_16fft_main_15	hsdivout1_clk	MAIN_PLL15_HSDIV1_CLKOUT	
DCC2	dcc_clksrc6_clk	1	7	hsdiv4_16fft_main_2	hsdivout2_clk	MAIN_PLL2_HSDIV2_CLKOUT	
DCC2	dcc_clksrc7_clk	1	8	PINFUNCTION_RMII2_REF_CLKin	RMII2_REF_CLK	RMII2_REF_CLK	
DCC2	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
DCC2	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1	
DCC2	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	

Table 4-152. MAIN_DCC2 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC2	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4
DCC2	vbus_clk	1	9	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4

Table 4-153. MAIN_DCC3 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC3	dcc_clksrc0_clk	1	1	hsdiv4_16fft_main_1	hsdivout0_clk	MAIN_PLL1_HSDIV0_CLKOUT	
DCC3	dcc_clksrc1_clk	1	2	postdiv4_16ff_main_2	hsdivout5_clk	MAIN_PLL2_HSDIV5_CLKOUT	
DCC3	dcc_clksrc2_clk	1	3	sam62a_c7xv_wrap_main_0_clock_control_0	c7xv_divh_clk4_obsclk_out_clk	c7xv_divh_clk4_obsclk_out_clk	
DCC3	dcc_clksrc3_clk	1	4	postdiv4_16ff_main_2	hsdivout7_clk	MAIN_PLL2_HSDIV7_CLKOUT	
DCC3	dcc_clksrc4_clk	1	5	postdiv4_16ff_main_2	hsdivout6_clk	MAIN_PLL2_HSDIV6_CLKOUT	
DCC3	dcc_clksrc5_clk	1	6	postdiv4_16ff_main_2	hsdivout9_clk	MAIN_PLL2_HSDIV9_CLKOUT	
DCC3	dcc_clksrc6_clk	1	7	sam62a_a53_512kb_wrap_main_0_arm_corepack_0	a53_divh_clk4_obsclk_out_clk	a53_divh_clk4_obsclk_out_clk	/4
DCC3	dcc_clksrc7_clk	1	8	sam62a_ddr_wrap_main_0	ddr_pll_divh_clk4_obsclk_out_clk	ddr_pll_divh_clk4_obsclk_out_clk	
DCC3	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
DCC3	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1	
DCC3	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	
DCC3	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4
DCC3	vbus_clk	1	9	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4

Table 4-154. MAIN_DCC4 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC4	dcc_clksrc0_clk	1	1	PINFUNCTION_GPMC0_CLKLBin	GPMC0_CLKLB	GPMC0_CLKLB	

Table 4-154. MAIN_DCC4 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC4	dcc_clksrc1_clk	1	2	PINFUNCTION_CP_GEMAC_CPTS0_RFT_CLKin	CP_GEMAC_CPTS0_RFT_CLK	CP_GEMAC_CPTS_REF_CLK	
DCC4	dcc_clksrc2_clk	1	3	PINFUNCTION_AUDIO_EXT_REFCLK1in	AUDIO_EXT_REFCLK1	AUDIO_EXT_REFCLK1	
DCC4	dcc_clksrc3_clk	1	4	K3_DPHY_RX_main_0	ppi_rx_byte_clk	ppi_rx_byte_clk	
DCC4	dcc_clksrc4_clk	1	5	PINFUNCTION_MCU_EXT_REFCLK0in	MCU_EXT_REFCLK0	MCU_EXT_REFCLK0	
DCC4	dcc_clksrc5_clk	1	6	PINFUNCTION_RMII1_REF_CLKin	RMII1_REF_CLK	RMII1_REF_CLK	/4
DCC4	dcc_clksrc6_clk	1	7	PINFUNCTION_RGMII1_RXCin	RGMII1_RXC	RGMII1_RXC	
DCC4	dcc_clksrc7_clk	1	8	CLK_32K_RC_SEL	out0	DEVICE_CLKOUT_32K	
DCC4	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
DCC4	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1	
DCC4	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	
DCC4	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/2
DCC4	vbus_clk	1	9	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4

Table 4-155. MAIN_DCC5 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC5	dcc_clksrc0_clk	1	1	postdiv4_16ff_main_0	hsdivout8_clk	MAIN_PLL0_HSDIV8_CLKOUT	
DCC5	dcc_clksrc2_clk	1	3	hsdiv4_16fft_main_2	hsdivout1_clk	MAIN_PLL2_HSDIV1_CLKOUT	
DCC5	dcc_clksrc3_clk	1	4	hsdiv4_16fft_main_2	hsdivout3_clk	MAIN_PLL2_HSDIV3_CLKOUT	
DCC5	dcc_clksrc4_clk	1	5	hsdiv4_16fft_main_2	hsdivout4_clk	MAIN_PLL2_HSDIV4_CLKOUT	
DCC5	dcc_clksrc5_clk	1	6	hsdiv2_16fft_main_5	hsdivout0_clk	MAIN_PLL5_HSDIV0_CLKOUT	
DCC5	dcc_clksrc6_clk	1	7	hsdiv0_16fft_main_17	hsdivout0_clk	MAIN_PLL17_HSDIV0_CLKOUT	
DCC5	dcc_clksrc7_clk	1	8	PINFUNCTION_RGMII2_RXCin	RGMII2_RXC	RGMII2_RXC	
DCC5	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
DCC5	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1	
DCC5	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	

Table 4-155. MAIN_DCC5 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC5	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	
DCC5	vbus_clk	1	9	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4

Table 4-156. MAIN_DCC6 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
DCC6	dcc_clksrc0_clk	1	1	PINFUNCTION_VOUT0_EXTPCLKINin	VOUT0_EXTPCLKIN	VOUT_EXTPCLKIN	
DCC6	dcc_clksrc1_clk	1	2	PINFUNCTION_MCASP0_ACLKXin	MCASP0_ACLKX	MCASP0_ACLKX	
DCC6	dcc_clksrc2_clk	1	3	PINFUNCTION_MCASP0_ACLKRin	MCASP0_ACLKR	MCASP0_ACLKR	
DCC6	dcc_clksrc3_clk	1	4	PINFUNCTION_MCASP1_ACLKXin	MCASP1_ACLKX	MCASP1_ACLKX	
DCC6	dcc_clksrc4_clk	1	5	PINFUNCTION_MCASP1_ACLKRin	MCASP1_ACLKR	MCASP1_ACLKR	
DCC6	dcc_clksrc5_clk	1	6	PINFUNCTION_MCASP2_ACLKXin	MCASP2_ACLKX	MCASP2_ACLKX	
DCC6	dcc_clksrc6_clk	1	7	PINFUNCTION_MCASP2_ACLKRin	MCASP2_ACLKR	MCASP2_ACLKR	
DCC6	dcc_clksrc7_clk	1	8	PINFUNCTION_AUDIO_EXT_REFCLK0in	AUDIO_EXT_REFCLK0	AUDIO_EXT_REFCLK0	
DCC6	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
DCC6	dcc_input01_clk	0	1	PINFUNCTION_EXT_REFCLK1in	EXT_REFCLK1	EXT_REFCLK1	
DCC6	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	
DCC6	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	
DCC6	vbus_clk	1	9	sam62_pll_ctrl_wrap_main_0	chip_div1_clk_clk	main_SYSCLK0	/4

Table 4-157. MCU_DCC0 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
MCU_DCC0	dcc_clksrc0_clk	1	1	hsdiv4_16fft_mcu_0	hsdivout0_clk	MCU_PLL0_HSDIV0_CLKOUT	
MCU_DCC0	dcc_clksrc1_clk	1	2	hsdiv4_16fft_mcu_0	hsdivout1_clk	MCU_PLL0_HSDIV1_CLKOUT	
MCU_DCC0	dcc_clksrc2_clk	1	3	hsdiv4_16fft_mcu_0	hsdivout2_clk	MCU_PLL0_HSDIV2_CLKOUT	
MCU_DCC0	dcc_clksrc3_clk	1	4	hsdiv4_16fft_mcu_0	hsdivout3_clk	MCU_PLL0_HSDIV3_CLKOUT	/4

Table 4-157. MCU_DCC0 Input Source Clock Mapping (continued)

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
MCU_DCC0	dcc_clksrc4_clk	1	5	hsdiv4_16fft_mcu_0	hsdivout4_clk	MCU_PLL0_HSDIV4_CLKOUT	
MCU_DCC0	dcc_clksrc5_clk	1	6	RCOSC_32KHz_GEN_DIV3	out0	CLK_32K_RC	
MCU_DCC0	dcc_clksrc6_clk	1	7	CLK_32K_RC_SEL	out0	DEVICE_CLKOUT_32K	
MCU_DCC0	dcc_clksrc7_clk	1	8	PINFUNCTION_MCU_EXT_REFCLK0in	MCU_EXT_REFCLK0	MCU_EXT_REFCLK0	
MCU_DCC0	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
MCU_DCC0	dcc_input01_clk	0	1	RCOSC_32KHz_GEN_DIV3	out0	CLK_32K_RC	
MCU_DCC0	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	
MCU_DCC0	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_mcu_0	chip_div1_clk_clk	MCU_SYSCLK0	/2
MCU_DCC0	vbus_clk	1	9	sam62_pll_ctrl_wrap_mcu_0	chip_div1_clk_clk	MCU_SYSCLK0	/4

Table 4-158. MCU_DCC1 Input Source Clock Mapping

Domain Instance	Domain Input	Input/ MUX	DCCCLKSRC0/ DCCCLKSRC1 Value	Source Instance	Source Interface	Clock Source	Divide By
MCU_DCC1	dcc_clksrc0_clk	1	1	postdiv1_16fft_mcu_0	hsdivout5_clk	MCU_PLL0_HSDIV5_CLKOUT	
MCU_DCC1	dcc_clksrc1_clk	1	2	postdiv1_16fft_mcu_0	hsdivout6_clk	MCU_PLL0_HSDIV6_CLKOUT	
MCU_DCC1	dcc_clksrc5_clk	1	6	RCOSC_32KHz_GEN_DIV3	out0	CLK_32K_RC	
MCU_DCC1	dcc_clksrc6_clk	1	7	CLK_32K_RC_SEL	out0	DEVICE_CLKOUT_32K	
MCU_DCC1	dcc_clksrc7_clk	1	8	PINFUNCTION_MCU_EXT_REFCLK0in	MCU_EXT_REFCLK0	MCU_EXT_REFCLK0	
MCU_DCC1	dcc_input00_clk	0	0	GLUELOGIC_HFOSC0_CLOCKLOSS_DETECTION	HFOSC0_CLKOUT	HFOSC0_CLKOUT	
MCU_DCC1	dcc_input01_clk	0	1	RCOSC_32KHz_GEN_DIV3	out0	CLK_32K_RC	
MCU_DCC1	dcc_input02_clk	0	2	GLUELOGIC_RCOSC	CLKOUT	CLK_12M_RC	
MCU_DCC1	dcc_input10_clk	1	0	sam62_pll_ctrl_wrap_mcu_0	chip_div1_clk_clk	MCU_SYSCLK0	/2
MCU_DCC1	vbus_clk	1	9	sam62_pll_ctrl_wrap_mcu_0	chip_div1_clk_clk	MCU_SYSCLK0	/4

4.13.2 Error Signaling Module (ESM)

This section contains the integration details for the ESM module on this device. For further information, see the *Error Signaling Module (ESM)* section of the *Peripherals* chapter.

4.13.2.1 ESM Unsupported Features

The following features are not supported on this family of devices:

- No Dedicated ERROR Pin for MAIN domain ESM. MAIN ESM error interrupts are routed to the WKUP ESM - the WKUP ESM drives the MCU_ERROR pin and can factor in errors from MAIN ESM if programmed to do so.

4.13.2.2 Module Allocations

Table 4-159. ESM Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
ESM0			✓
WKUP_ESM0	✓		

4.13.2.3 Resets, Interrupts, and Clocks

Table 4-160. ESM Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
ESM0	MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	NONE
WKUP_ESM0	WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	NONE

Table 4-161. ESM Resets

Module Instance	Source	Description
ESM0	MAIN_PSC0	ESM0 reset
WKUP_ESM0	WKUP_PSC0	WKUP_ESM0 reset

Table 4-162. ESM Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	ESM0_esm_lvl_event_IN_37	ESM0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	R5FSS0_CORE0_intr_IN_140	R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	R5FSS0_CORE1_intr_IN_140	R5FSS0_CORE1	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	R5FSS1_CORE0_intr_IN_140	R5FSS1_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	R5FSS1_CORE1_intr_IN_140	R5FSS1_CORE1	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_cfg_lvl_0	WKUP_R5FSS0_CORE0_intr_IN_140	WKUP_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level

Table 4-162. ESM Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	ESM0_esm_lvl_event_IN_38	ESM0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	R5FSS0_CORE0_intr_IN_141	R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	R5FSS0_CORE1_intr_IN_141	R5FSS0_CORE1	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	R5FSS1_CORE0_intr_IN_141	R5FSS1_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	R5FSS1_CORE1_intr_IN_141	R5FSS1_CORE1	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_hi_lvl_0	WKUP_R5FSS0_CORE0_intr_IN_141	WKUP_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	ESM0_esm_lvl_event_IN_39	ESM0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	R5FSS0_CORE0_intr_IN_142	R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	R5FSS0_CORE1_intr_IN_142	R5FSS0_CORE1	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	R5FSS1_CORE0_intr_IN_142	R5FSS1_CORE0	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	R5FSS1_CORE1_intr_IN_142	R5FSS1_CORE1	WKUP_ESM0 interrupt request	level
WKUP_ESM0	WKUP_ESM0_esm_int_low_lvl_0	WKUP_R5FSS0_CORE0_intr_IN_142	WKUP_R5FSS0_CORE0	WKUP_ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	C7X256V0_CLEC_gic_spi_IN_180	C7X256V0_CLEC	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	C7X256V1_CLEC_gic_spi_IN_180	C7X256V1_CLEC	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	WKUP_ESM0_esm_lvl_event_IN_0	WKUP_ESM0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	R5FSS0_CORE0_intr_IN_167	R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	R5FSS0_CORE1_intr_IN_167	R5FSS0_CORE1	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	R5FSS1_CORE0_intr_IN_167	R5FSS1_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	R5FSS1_CORE1_intr_IN_167	R5FSS1_CORE1	ESM0 interrupt request	level
ESM0	ESM0_esm_int_cfg_lvl_0	WKUP_R5FSS0_CORE0_intr_IN_167	WKUP_R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	C7X256V0_CLEC_gic_spi_IN_181	C7X256V0_CLEC	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	C7X256V1_CLEC_gic_spi_IN_181	C7X256V1_CLEC	ESM0 interrupt request	level

Table 4-162. ESM Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
ESM0	ESM0_esm_int_hi_lvl_0	WKUP_ESM0_esm_lvl_event_IN_1	WKUP_ESM0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	R5FSS0_CORE0_intr_IN_168	R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	R5FSS0_CORE1_intr_IN_168	R5FSS0_CORE1	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	R5FSS1_CORE0_intr_IN_168	R5FSS1_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	R5FSS1_CORE1_intr_IN_168	R5FSS1_CORE1	ESM0 interrupt request	level
ESM0	ESM0_esm_int_hi_lvl_0	WKUP_R5FSS0_CORE0_intr_IN_168	WKUP_R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	C7X256V0_CLEC_gic_spi_IN_182	C7X256V0_CLEC	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	C7X256V1_CLEC_gic_spi_IN_182	C7X256V1_CLEC	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	WKUP_ESM0_esm_lvl_event_IN_2	WKUP_ESM0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	R5FSS0_CORE0_intr_IN_169	R5FSS0_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	R5FSS0_CORE1_intr_IN_169	R5FSS0_CORE1	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	R5FSS1_CORE0_intr_IN_169	R5FSS1_CORE0	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	R5FSS1_CORE1_intr_IN_169	R5FSS1_CORE1	ESM0 interrupt request	level
ESM0	ESM0_esm_int_low_lvl_0	WKUP_R5FSS0_CORE0_intr_IN_169	WKUP_R5FSS0_CORE0	ESM0 interrupt request	level

Table 4-163. ESM Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
ESM0	FICLK	MAIN_SYSCLK0/4		ESM0 Functional and Interface Clock
WKUP_ESM0	FICLK	MCU_SYSCLK0/4		WKUP_ESM0 Functional and Interface Clock

4.13.3 Memory Cyclic Redundancy Check (MCRC64)

This section contains the integration details for the MCRC64 module on this device. For further information, see the *Memory Cyclic Redundancy Check (MCRC)* section of the *Peripherals* chapter.

4.13.3.1 MCRC64 Unsupported Features

The following features are not supported on this family of devices:

- Data Trace Mode (Automatic PSA on CPU Instruction and Data TCM busses) - Wrapper only supports VBUSM Signature Analysis. ITCM, DTCM designed for Cortex R5F
- DMA is not supported by the MCU instances

4.13.3.2 Module Allocations

Table 4-164. MCRC64 Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
MCRC64_0			✓

4.13.3.3 Resets, Interrupts, and Clocks

Table 4-165. MCRC64 Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
MCRC64_0	MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	LPSC_MAIN_DM2MAIN_INFRA_ISO

Table 4-166. MCRC64 Resets

Module Instance	Source	Description
MCRC64_0	MAIN_PSC0	MCRC64_0 reset

Table 4-167. MCRC64 Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCRC64_0	MCRC64_0_dma_event_[3:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_28	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	pulse
MCRC64_0	MCRC64_0_dma_event_[3:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_29	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	pulse
MCRC64_0	MCRC64_0_dma_event_[3:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_30	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	pulse
MCRC64_0	MCRC64_0_dma_event_[3:0]	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_31	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	pulse
MCRC64_0	MCRC64_0_int_mcrc_0	C7X256V0_CLEC_gic_spi_IN_166	C7X256V0_CLEC	MCRC64_0 interrupt request	level
MCRC64_0	MCRC64_0_int_mcrc_0	C7X256V1_CLEC_gic_spi_IN_166	C7X256V1_CLEC	MCRC64_0 interrupt request	level
MCRC64_0	MCRC64_0_int_mcrc_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_7	DMASS0_INTAGGR_0	MCRC64_0 interrupt request	level

Table 4-167. MCRC64 Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
MCRC64_0	MCRC64_0_int_mcrc_0	R5FSS0_CORE0_intr_IN_119	R5FSS0_CORE0	MCRC64_0 interrupt request	level
MCRC64_0	MCRC64_0_int_mcrc_0	R5FSS0_CORE1_intr_IN_119	R5FSS0_CORE1	MCRC64_0 interrupt request	level
MCRC64_0	MCRC64_0_int_mcrc_0	R5FSS1_CORE0_intr_IN_119	R5FSS1_CORE0	MCRC64_0 interrupt request	level
MCRC64_0	MCRC64_0_int_mcrc_0	R5FSS1_CORE1_intr_IN_119	R5FSS1_CORE1	MCRC64_0 interrupt request	level
MCRC64_0	MCRC64_0_int_mcrc_0	WKUP_R5FSS0_CORE0_intr_IN_119	WKUP_R5FSS0_CORE0	MCRC64_0 interrupt request	level

Table 4-168. MCRC64 Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
MCRC64_0	FICLK	MAIN_SYSCLK0/2		MCRC64_0 Functional and Interface Clock

4.13.4 ECC Aggregator (ECC_AGGR)

This section contains the integration details for the ECC_AGGR module on this device. For further information, see the *ECC Aggregator (ECC_AGGR)* section of the *Peripherals* chapter.

4.13.4.1 Module Allocations

Table 4-169. ECC_AGGR Modules Allocation within Device Domains

Instance	Domain		
	WKUP	Top Level	MAIN
ECC_AGGR0			✓
WKUP_ECC_AGGR0	✓		
WKUP_ECC_AGGR1	✓		
WKUP_ECC_AGGR1	✓		

4.13.4.2 Resets, Interrupts, and Clocks

Table 4-170. ECC_AGGR Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies

Table 4-171. ECC_AGGR Resets

Module Instance	Source	Description
WKUP_ECC_AGGR0	PSC0	WKUP_ECC_AGGR0 reset
WKUP_ECC_AGGR1	PSC0	WKUP_ECC_AGGR1 reset
WKUP_ECC_AGGR2	WKUP_PSC0	WKUP_ECC_AGGR2 reset
ECC_AGGR0	PSC0	ECC_AGGR0 reset

Table 4-172. ECC_AGGR Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_corr_level_0	WKUP_ESM0_esm_lvl_event_IN_23	WKUP_ESM0	WKUP_ECC_AGGR0 interrupt request	level
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_corr_level_0	ESM0_esm_lvl_event_IN_20	ESM0	WKUP_ECC_AGGR0 interrupt request	level
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_uncorr_level_0	WKUP_ESM0_esm_lvl_event_IN_24	WKUP_ESM0	WKUP_ECC_AGGR0 interrupt request	level
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_uncorr_level_0	ESM0_esm_lvl_event_IN_21	ESM0	WKUP_ECC_AGGR0 interrupt request	level
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_corr_level_0	WKUP_ESM0_esm_lvl_event_IN_38	WKUP_ESM0	WKUP_ECC_AGGR1 interrupt request	level
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_corr_level_0	ESM0_esm_lvl_event_IN_104	ESM0	WKUP_ECC_AGGR1 interrupt request	level
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_uncorr_level_0	WKUP_ESM0_esm_lvl_event_IN_39	WKUP_ESM0	WKUP_ECC_AGGR1 interrupt request	level
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_uncorr_level_0	ESM0_esm_lvl_event_IN_105	ESM0	WKUP_ECC_AGGR1 interrupt request	level
WKUP_ECC_AGGR2	WKUP_ECC_AGGR2_corr_level_0	WKUP_ESM0_esm_lvl_event_IN_20	WKUP_ESM0	WKUP_ECC_AGGR2 interrupt request	level

Table 4-172. ECC_AGGR Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
WKUP_ECC_AGGR2	WKUP_ECC_AGGR2_uncorr_level_0	WKUP_ESM0_esm_lvl_event_IN_21	WKUP_ESM0	WKUP_ECC_AGGR2 interrupt request	level
ECC_AGGR0	ECC_AGGR0_corr_level_0	ESM0_esm_lvl_event_IN_24	ESM0	ECC_AGGR0 interrupt request	level
ECC_AGGR0	ECC_AGGR0_uncorr_level_0	ESM0_esm_lvl_event_IN_25	ESM0	ECC_AGGR0 interrupt request	level
ECC_AGGR0	ECC_AGGR0_corr_level_0	ESM0_esm_lvl_event_IN_26	ESM0	ECC_AGGR0 interrupt request	level
ECC_AGGR0	ECC_AGGR0_uncorr_level_0	ESM0_esm_lvl_event_IN_27	ESM0	ECC_AGGR0 interrupt request	level
ECC_AGGR0	ECC_AGGR0_corr_level_0	ESM0_esm_lvl_event_IN_2	ESM0	ECC_AGGR0 interrupt request	level
ECC_AGGR0	ECC_AGGR0_uncorr_level_0	ESM0_esm_lvl_event_IN_1	ESM0	ECC_AGGR0 interrupt request	level

Table 4-173. ECC_AGGR Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
WKUP_ECC_AGGR0	CLK	DM_CLK/2	WKUP_CLKSEL[0:0]	
WKUP_ECC_AGGR1	CLK	MCU_SYSCLK0/4		
WKUP_ECC_AGGR2	CLK	MCU_SYSCLK0/4		
ECC_AGGR0	CLK	MAIN_SYSCLK0/4		
ECC_AGGR0	CLK	MAIN_R5SS_CLK/8		
ECC_AGGR0	CLK	MAIN_PLL15_HSDIV0_CLKOUT/2		

4.13.4.3 Device Modules and Subsystems with ECC Aggregator

Table 4-174. Device Modules and Subsystems with ECC Aggregator

Instance Name	MAIN	MCU	WKUP
CSI_RX_IF0	X		
MMCSD1	X		
MMCSD2	X		
MMCSD0	X		
GICSS0	X		
WKUP_VTM0			X
MCAN0	X		
MCU_MCAN0		X	
MCU_MCAN1		X	
PSRAMECC0	X		
PSRAMECC1	X		
R5FSS0			X
PDMA0	X		
PDMA1	X		
VPAC0	X		
USB0	X		
USB1	X		

4.14 On-Chip Debug

This section contains the integration details for the On-Chip Debug module on this device. For Further information, see the On-Chip Debug chapter.

4.14.1 On-Chip Debug Unsupported Features

The following features are not supported on this family of devices:

- There are no unsupported features

4.14.2 Resets, Interrupts, Clocks

Table 4-175. On-Chip Debug Integration Attributes

Module Instance	Power Sleep Controller	Power Domain	Module Domain	Index	Default	Controllable	Dependencies
DEBUGSS_WRAP0	MAIN_PSC0	GP_CORE	LPSC_MAIN_DEBUGSS	10	ON	NO	LPSC_MAIN_IP0
DEBUGSS0	MAIN_PSC0	GP_CORE	LPSC_MAIN_DEBUGSS	10	ON	NO	LPSC_MAIN_IP0

Table 4-176. On-Chip Resets

Module Instance	Source	Description
DEBUGSS_WRAP0	MAIN_PSC0	DEBUGSS_WRAP0 reset
DEBUGSS_WRAP0	PLLCTRL0	DEBUGSS_WRAP0 reset
DEBUGSS0	MAIN_PSC0	DEBUGSS0 reset

Table 4-177. On-Chip Hardware Requests

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	C7X256V0_CLEC_gic_spi_IN_201	C7X256V0_CLEC	DEBUGSS0 interrupt request	level

Table 4-177. On-Chip Hardware Requests (continued)

Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	C7X256V1_CLEC_gic_spi_IN_201	C7X256V1_CLEC	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	R5FSS0_CORE0_intr_IN_201	R5FSS0_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	R5FSS0_CORE1_intr_IN_201	R5FSS0_CORE1	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	R5FSS1_CORE0_intr_IN_201	R5FSS1_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	R5FSS1_CORE1_intr_IN_201	R5FSS1_CORE1	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_aqcmpintr_level_0	WKUP_R5FSS0_CORE0_intr_IN_201	WKUP_R5FSS0_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	C7X256V0_CLEC_gic_spi_IN_202	C7X256V0_CLEC	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	C7X256V1_CLEC_gic_spi_IN_202	C7X256V1_CLEC	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	R5FSS0_CORE0_intr_IN_202	R5FSS0_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	R5FSS0_CORE1_intr_IN_202	R5FSS0_CORE1	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	R5FSS1_CORE0_intr_IN_202	R5FSS1_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	R5FSS1_CORE1_intr_IN_202	R5FSS1_CORE1	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_ctm_level_0	WKUP_R5FSS0_CORE0_intr_IN_202	WKUP_R5FSS0_CORE0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_davdma_level_0	DMASS0_INTAGGR_0_intaggr_levi_pend_IN_27	DMASS0_INTAGGR_0	DEBUGSS0 interrupt request	level
DEBUGSS0	DEBUGSS0_davdma_level_0	USB0_trace_inep_pkt_buff_avail_IN_0	USB0	DEBUGSS0 interrupt request	level

Table 4-178. On-Chip Clocks

Module Instance	Module Clock Input	Source Clock Signal	Source Control Register	Description
DEBUGSS_WRAP0	ATB_CLK	DM_CLK/2		
	CORE_CLK	MCU_SYSCLK0/4		
	P1500_WRCK	MCU_SYSCLK0/4		
	TREXPT_CLK	MAIN_SYSCLK0/4		
DEBUGSS0	CFG_CLK	MAIN_SYSCLK0/4		
	DBG_CLK	MAIN_SYSCLK0/2		
	SYS_CLK	MAIN_SYSCLK0/2		

5 Initialization

This chapter describes the steps for device initialization.

Note

This TRM uses the prefix of "MCU_" for items that refer to the device as a whole instead of a specific domain. "MCU_" is the equivalent of Top Level from Section 1.5.

5.1 Initialization Overview

Initialization Process is an overview of the initialization process and its steps:

- **Preinitialization:** Power, clock, and control connections must be present, and the boot configuration pins must be held at the desired logical levels.
- **Power, clock, reset ramp sequence:** Specific sequence that is applied by the power-management chip(s)
- **ROM code:** Responsible for finding, for downloading, and for executing the initial software (SBL)
- **Initial software:** Software that loads, prepares, and passes control to application software or to the high-level operating system (HLOS)
- **High-Level Operating System** or bare-metal application which runs on main processor(s)

Figure 5-1. Initialization Process

The first two steps in the initialization process are hardware-oriented; however, they require an understanding of the process of configuring these system interface pins (balls on the device), which have software-configurable functionality. This configuration is an essential part of the chip configuration and is application-dependent. This chapter discusses these system-interface pins, the associated configuration registers, and memory structures that are vital to the correct initialization of the device.

5.1.1 ROM Code Overview

ROM bootloader (or ROM Code) is a software that resides in a on-chip read-only memory (ROM) to assist the customer in transferring and executing their application code. The device has two ROM codes operating in tandem – the Public ROM code, and the secure ROM code.

In order to accommodate various system scenarios, the ROM Code supports several boot modes. These boot modes can be broadly classified as:

- Primary boot interface
- Backup boot interface

During a host boot, the device is configured to receive code from a host via the selected interface. Either the host writes the application code directly into internal memory or the ROM Code receives the application code on the selected interface and stores it in internal memory.

During a memory boot, the device transfers code from non-volatile memory to internal memory for execution.

In all boot modes, the entire boot operation can be partitioned into two sections:

1. Hardware initialization phase
2. Boot process.

During initialization, the ROM Code configures the device resources (PLLs, peripherals, pins) as needed to support the boot process. The resources used depend on the boot mode requirements.

During the boot process the boot image can be loaded into device memory and executed, or executed in place, depending on the boot peripheral. DM R5 will perform code verification and allow, or forbid, the image execution.

Main configuration source for boot after power-up are the BOOTMODE pins sampled automatically after reset release and stored in device status registers. At ROM Code startup, these pin values are read from the registers to create the boot peripheral list and the boot configuration tables used later to initialize and startup the PLLs and boot peripherals.

5.1.2 Bootloader Modes

ROM Code Boot Modes shows the boot modes supported by ROM code.

Table 5-1. ROM Code Boot Modes

Boot Mode	Boot Media/Host	SoC Peripheral	Can be a Backup Mode?(1)	Notes
UART	Peripheral Boot	Main UART0	Y	
OSPI	OSPI	OSPI0	N	
	QSPI	OSPI0	N	
	SPI	OSPI0	Y	
	xSPI	OSPI0	N	
	Serial NAND	OSPI0	N	
MMCSD	eMMC	MMCSD	Y	
MMCSD	SD Card	MMCSD	Y	
USB	USB Device	USB Device	Y	
CPSW	Ethernet	RGMII	Y	Port 1 only
		RMII1	Y	Port 1 only

(1) The peripheral can be selected also as a backup boot mode. A backup mode is tried if primary boot mode fails.

Note

Because different devices support different sets of peripherals, see the *device-specific Datasheet* to obtain the list of peripherals supported in your device.

5.1.3 Terminology

- **Boot Mode Pins:** Boot mode pins provide vital information to ROM code for boot. These pins must be properly set up before power ramp.
- **Bootstrap:** Initial software launched by the ROM code during the memory booting phase.
- **Boot Header:** Optional structure that precedes the initial software and allows the redefinition of the ROM code default settings.
- **Downloaded software:** Initial software downloaded into on-chip RAM by the ROM code during the peripheral booting phase.
- **eFuse:** A one-time programmable memory location usually set at the factory.
- **Flash loader:** Downloaded software launched by the ROM code during the preflashing stage. It also programs an image in external memories.
- **GP device:** General-purpose device (SoC) or a non-secure device.
- **Initial software:** Software executed by any of the ROM code mechanisms (memory booting or peripheral booting). Initial software is a generic term for bootstrap and downloaded software. This can be the SBL (secondary bootloader) responsible for loading an OS.
- **Memory booting:** ROM code mechanism that consists of executing initial software from external memory.
- **Controller CPU:** The Arm® Cortex® CPU for which CPU-ID is 0. It configures the multicore platform and starts the ROM code to ensure device booting from a mass storage memory (memory booting) or a peripheral interface (peripheral booting).
- **Peripheral booting:** ROM code mechanism that consists of polling selected interfaces, downloading, and executing initial software (in this case, downloaded software) in the internal RAM.
- **Preflashing:** A specific case of peripheral booting where the ROM code mechanism is used to program the external flash memory.

- **ROM Code:** or ROM bootloader (RBL), the on-chip software in device ROM that executes first and implements booting.
- **ROM Code-controlled Boot Phase:** This phase covers the sequence operations from the time the platform releases the reset to the time first user- or customer-owned software starts execution. This phase is fully controlled by the device ROM code.
- **Booting Parameter Table:** A logical structure stored in the on-chip RAM memory and contains information for the boot, such as the boot file name or an address to boot from.

5.2 Boot Process

5.2.1 Public ROM Code Architecture

The Public ROM code has the following components (see Figure 5-2):

- Main
- Buffer manager
- X.509
- Log and Trace
- System
- Protocol
- Driver

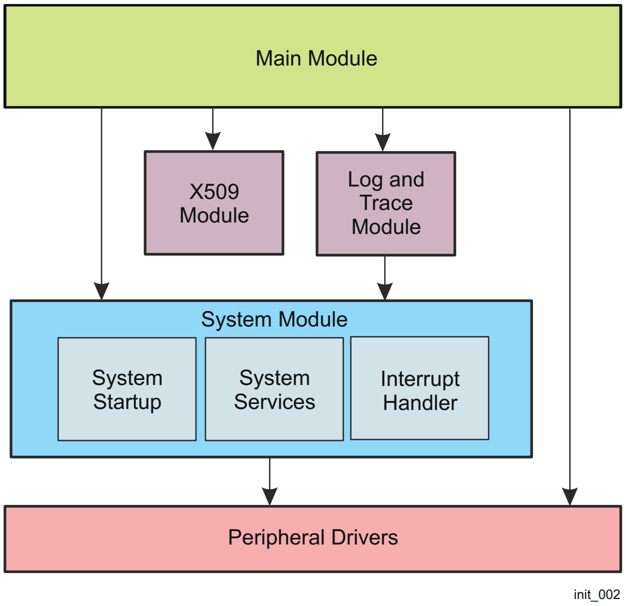


Figure 5-2. Public ROM Code Architecture

5.2.1.1 Main Module

The Main module contains the top level execution loop. This loop repeats until a boot image has been received or directed to sleep by the M4. The main loop has three different execution sub-paths based on the boot peripheral.

- **Image Path** This path is used by the OSPI, QSPI, SPI, and xSPI boot modes. In these cases the image data can be directly read by both the R5 and the M4 in place.
- **Block Path** This path is used by the I2C, USB-DFU, UART, eMMC, Ethernet, eMMC/SD cards in raw mode. In this mode data is received from the peripheral in blocks. Blocks are accumulated in the boot buffer until a full X.509 certificate header has been received, at which point this full certificate and any subsequent blocks are passed to the M4 as they arrive.
- **Filesystem Path** This path is used by the eMMC/SD cards in filesystem mode. This mode executes exactly like in the block path, except that the boot image location is defined by a filesystem.

The main level is able to detect if a received boot image is in the correct format and reject non-conforming images. In some cases, detection of an invalid image is done after the initial data buffer has been sent to the M4. In that case the R5 must inform the M4 that the image was in fact invalid and it will be looking for the next image and try again.

5.2.1.2 X509 Module

The X509 module parses the boot header. The boot header is an X.509 certificate as defined in RFC5280. Extensions specific to boot are described in *X.509 Certificate*.

This module also includes an OID decoder as well as defines OID values as C #define constants for any values that can be used during boot.

5.2.1.3 Buffer Manager Module

The buffer manager module is used to allocate buffers to hold boot data. The R5 code allocates a buffer when it is ready to read a block of data from the boot peripheral. Once the data is read the buffer ownership is passed to the M4. When the M4 has completed processing the data in the buffer ownership is returned to the R5, which then frees the buffer.

5.2.1.4 Log and Trace Module

The Log and Trace modules are not integral to the boot process. Instead, they provide ability to record operation of the ROM code and track unexpected occurrences.

Log and trace function is currently TI internal.

5.2.1.5 System Module

The system module provides services to other modules. These services are not directly related to boot drivers. The system module is the only module that operates in the supervisor mode of the R5 (a few services will run in user). The system module supports the following functions:

- Interrupt enable, disable, and service
- IPC
- Power
- Pinmux
- Clock
- Task switch

The main level is able to detect if a received boot image is in the correct format and reject non-conforming images.

5.2.1.6 Protocol Module

The protocol modules provide implementation of high-level data transfer protocols. The BOOTP/TFTP and XMODEM protocols reside in this layer. These modules provide services as defined in well-known standards.

5.2.1.7 Driver Module

The driver module implements the low level peripheral drivers.

5.2.2 R5 ROM Description

In a general-purpose (GP) device, R5 ROM performs the following functions:

- Device management
- Configures the boot vectors (in BOOT_CFG) and controls reset release of R5 core.
- IPC configuration via Main DMSS rings and Secure Proxy
- PLL configuration (R5 and SA2UL)
- X509 certificate parsing
- SA2UL configuration to SHA512 for image integrity checks
- Copy SBL in OCMC RAM from Booting Media

5.2.3 Boot Process Flow

The device boot process flow is shown in *Boot Process*.

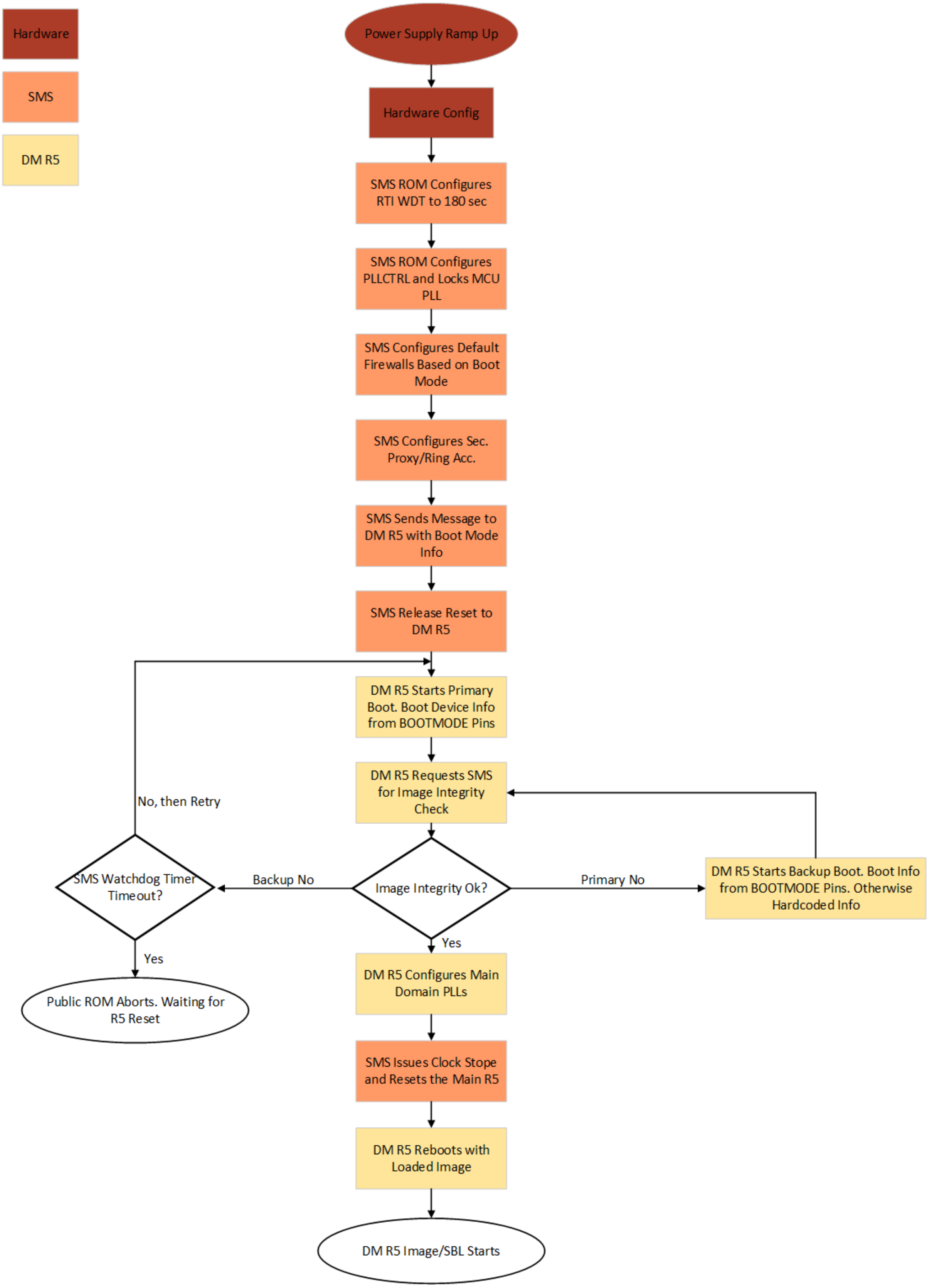


Figure 5-3. Boot Process

The values of BOOTMODE[15:0] pins are latched into the Device Status register MAIN_DEVSTAT[15:0] by hardware as the device comes out of global cold reset, sampled after MCU_PORz deassertion. For more information how to set BOOTMODE pins, see *Boot Mode Pins Mapping*.

The M4 (also known as SMS or SMS M4) is the boot controller for the Public ROM. M4 performs the necessary configurations and releases R5's reset for CPU0.

The DM R5 checks the boot mode pins and then configures the appropriate peripheral interface to get access to a boot image. A cursory check of the image is made, and the image is passed to SMS M4. M4 ROM then will perform code verification and route the boot image to the on-chip RAM. Once the image has been received, R5 enters a clean state and idles. SMS M4 ROM code will assert reset to the R5, redirect the boot vector to the newly loaded image, and release the reset. This restarts the R5 with the Public ROM code fully disconnected.

The Public ROM code executes after a cold or warm reset.

Note

M4 ROM sets up a 3-minute watchdog timer (RTI0) timeout. During this time, the R5 boot needs to get completed, otherwise a WDT reset will occur. Once the R5 image is loaded (SBL/SPL), M4 ROM will restart the watchdog timer for additional 3 minutes upon entering the R5 SBL. The customer-provided R5 image needs to load and install the TI-provided SYSFW image into the M4, which will manage the watchdog timer during run time.

Note

The following system conditions must be met at POR to perform device boot:

- USB cable plug must be inserted
- Ethernet PHY is powered up and out of reset
- The SD card cage must be powered before entering the SD card boot mode. A SD/MMC card with pre-loaded image must be inserted
- Memory devices must be up and ready (power ramped up and reset completed) at device startup:
  - eMMC
  - xSPI/OSPI/QSPI/SPI and Serial flash
  - NOR/NAND flash

Failing to meet these requirements may result in boot fail and performing a backup boot (if available for that mode).

External Bootloader Tasks describes the external bootloader (SBL) typical tasks.

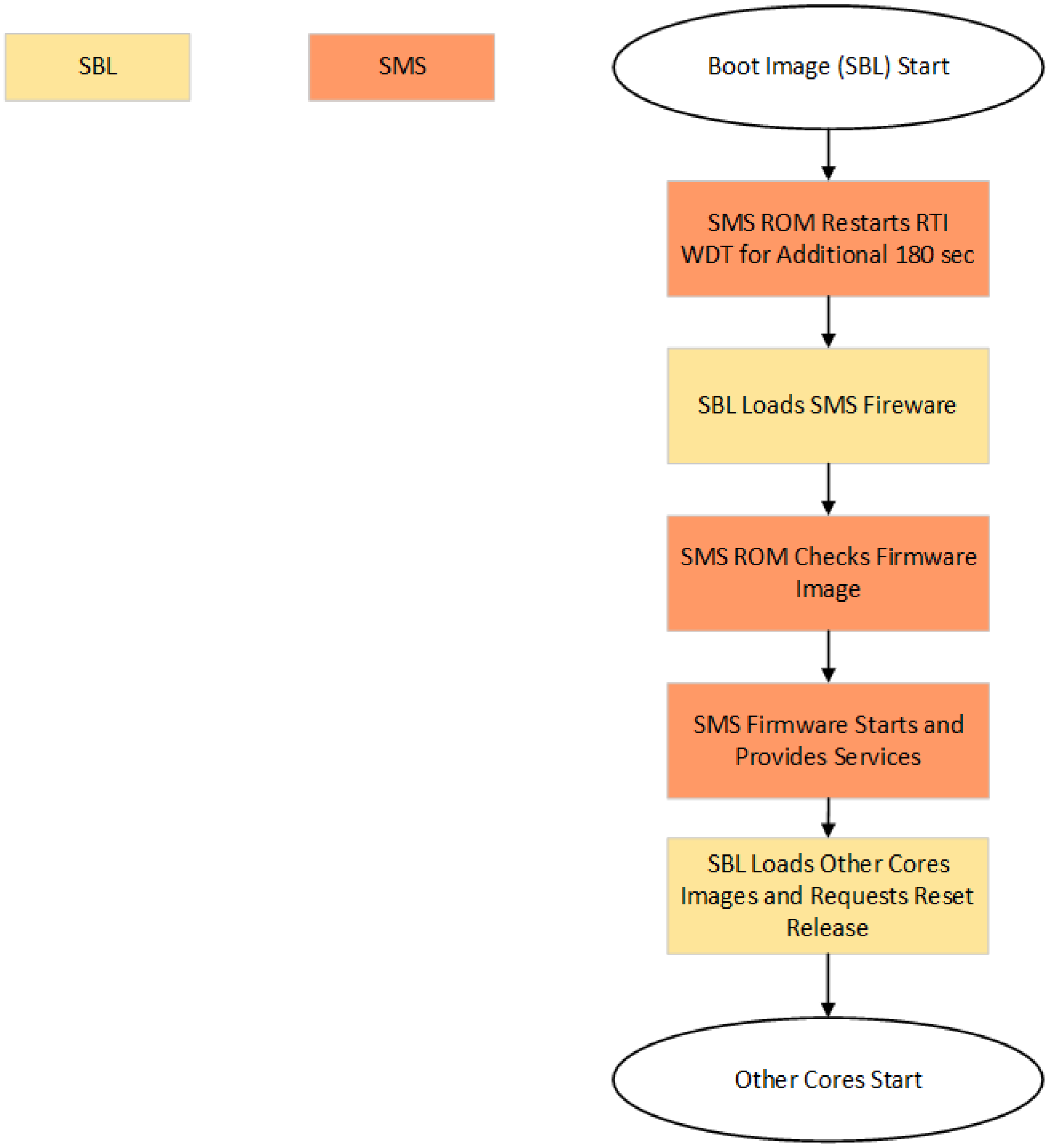


Figure 5-4. External Bootloader Tasks

Upon R5 reset and SBL execution start, M4 ROM restarts the RTI watchdog timer for additional 180 seconds of timeout. During that time, SBL must load the M4 firmware provided by TI otherwise an R5 reset will occur as a preventive measure against software misbehavior.

One of the SBL's main tasks is to load the M4 firmware. Only after this task is performed, SBL can load the other processors' image and request a reset release from M4 firmware for those cores.

5.3 BOOTMODE Pin Mapping

The ROM execution is directed through the main boot mode pins. This provides more flexibility and more booting peripherals to boot from. The Main domain must be powered and functional.

Main boot mode pins are shown in *BOOTMODE Pin Mapping*.

Any Bootmode pins marked as Reserved or not used must be tied high or low with pull resistors. They should not be left floating.

Table 5-2. BOOTMODE Pin Mapping

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

PLL Reference Clock Selection describes the BOOTMODE pins that need to be set according to the system clock provided to the device.

The ROM Code will configure any PLLs required during the boot process.

Note

Reference clock selections may be limited by the device. Please consult the device specific datasheet to determine which system clock frequencies are valid.

Table 5-3. PLL Reference Clock Selection

PLL Config Pins			Ref Clock (MHz)
B2	**B1**	**B0**	
0	0	0	Reserved
0	0	1	Reserved
0	1	0	24
0	1	1	25
1	0	0	26
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

5.3.1 Primary Boot Mode Selection and Configuration

The primary boot mode is the first mode attempted after reset. *Primary Boot Mode Selection* lists all possible primary boot modes. All pins marked as reserved can be either 0 or 1. All boot mode signals must be pulled low or high through a pull resistor on the board, they must not be left floating

Note

All BOOTMODE[15:00] signals must be pulled high through a resistor to VDDSHV3, or pulled low to ground, including Reserved signals. Reserved BOOTMODE signals must not be left floating.

Table 5-4. Primary Boot Mode Selection

Primary Boot Mode Config							Primary Boot Mode
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	
Reserved	Read Mode 2	Read Mode 1	0	0	0	0	Serial NAND
Reserved	Reserved	Csel	0	0	0	1	OSPI
Reserved	Reserved	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
0	0	Link stat	0	1	0	0	Ethernet RGMII

Table 5-4. Primary Boot Mode Selection (continued)

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Reserved	Reserved	Reserved	0	1	1	1	UART
0	Reserved	Fs/raw	1	0	0	0	MMCSD Boot
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	Reserved
Reserved	Reserved	Reserved	1	1	0	0	Reserved
Reserved	Reserved	Reserved	1	1	0	1	Fast-xSPI
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	ARM/Thumb	No/Dev	1	1	1	1	No-boot/Dev boot

5.3.2 Backup Boot Mode Selection and Configuration

The backup boot mode is selected via pins within the main BOOTMODE map. *Backup Mode Selection* lists all possible backup boot modes.

Table 5-5. Backup Mode Selection

Backup Boot Config	Backup Boot Mode Selection			Backup Boot Mode Selected
B13	B12	B11	B10	
Reserved	0	0	0	None
Mode	0	0	1	USB
Reserved	0	1	0	Reserved
Reserved	0	1	1	UART
IF	1	0	0	Ethernet
Port	1	0	1	MMCSD Boot
Reserved	1	1	0	SPI

5.4 Boot Modes

5.4.1 OSPI\xSPI\QSPI\SPI Boot

5.4.1.1 OSPI Boot

OSPI Boot Configuration Fields shows configuration pins assignment to functions when boot mode is the Octal SPI using the OSPI module.

Table 5-6. OSPI Boot Configuration Fields

Field	Value	Description
Csel	0	Boot Flash is on CS 0
	1	Boot Flash is on CS 1

OSPI Boot Pin Usage summarizes the OSPI pin configuration done by ROM code for OSPI boot device.

Table 5-7. OSPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_DQS	OSPI0_DQS	Disable	NA	0	Enable	0	PADCONFIG2
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG6
OSPI0_D4	OSPI0_D4	Disable	NA	0	Enable	0	PADCONFIG7
OSPI0_D5	OSPI0_D5	Disable	NA	0	Enable	0	PADCONFIG8
OSPI0_D6	OSPI0_D6	Disable	NA	0	Enable	0	PADCONFIG9
OSPI0_D7	OSPI0_D7	Disable	NA	0	Enable	0	PADCONFIG10
OSPI0_CSn0	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.1.1 OSPI Bootloader Operation

Please refer to *OSPI\SPI Boot* for more information that applies to OSPI boot mode

The OSPI boot mode supports 1S-1S-8S mode only. The ROM will issue a Read Command (0x8B) followed by a 24 bit (3 byte) address (the starting address is all zeros), followed by 8 dummy cycles. The flash device should then respond with 8-bit data. The frequency of operation during the read portion is 50 MHz.

5.4.1.1.1.1 OSPI Initialization Process

In the OSPI boot mode, the ROM Code initializes the OSPI module and the image is read from the OSPI flash connected to the selected chip-select. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM. See *OSPI Boot*, *OSPI Boot Device Configuration* for OSPI port settings.

A detailed summary of the OSPI boot parameter table and the boot configuration definitions are listed in *OSPI\SPI*, *OSPI Boot Parameter Table*.

5.4.1.1.1.2 OSPI Loading Process

OSPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

5.4.1.2 xSPI Boot

xSPI Boot Configuration Fields shows configuration pins assignment to functions when boot mode is xSPI using the OSPI module.

Table 5-8. xSPI Boot Configuration Fields

Field	Value	Description
SFDP	0	SFDP disabled
	1	SFDP enabled
Read cmd	0	0x0B Read Command
	1	0xEE Read Command
Mode	0	1S-1S-1S mode @ 50MHz
	1	8D-8D-8D mode @ 25MHz

*xSPI Boot Pin Usag*e summarizes the OSPI pin configuration done by ROM code for xSPI boot device on port 0.

Table 5-9. xSPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_DQS	OSPI0_DQS	Disable	NA	0	Enable	0	PADCONFIG2
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG6
OSPI0_D4	OSPI0_D4	Disable	NA	0	Enable	0	PADCONFIG7
OSPI0_D5	OSPI0_D5	Disable	NA	0	Enable	0	PADCONFIG8
OSPI0_D6	OSPI0_D6	Disable	NA	0	Enable	0	PADCONFIG9
OSPI0_D7	OSPI0_D7	Disable	NA	0	Enable	0	PADCONFIG10
OSPI0_CSn0	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.2.1 xSPI Bootloader Operation

Please refer to *OSPI\xSPI\QSPI\SPI Boot* for more information that applies to xSPI boot mode

The xSPI protocol defines 1S-1S-1S mode for general backwards compatibility, and 8D-8D-8D for maximum throughput.

For 1S-1S-1S mode of operation, the ROM will issue a Fast Read Output command (0x0B) followed by a 24 bit (3 byte) address (the starting address is all zeros), followed by 8 dummy cycles. The frequency of operation is 50MHz.

For 8D-8D-8D mode of operation, the ROM will issue a Fast Read command (0x0B or 0xEE, depending on BOOTMODE signal), followed by a 32 bit (4 byte) address (the starting address is all zeros). The frequency of operation is 25MHz.

When SFDP is enabled using a BOOTMODE signal, the ROM starts operation in 1S-1S-1S mode reads SFDP header from flash memory to get 8D-8D-8D switching sequence, Read Command, CMD Extension and Byte Order. SFDP parsing of ROM is described below and on successful parsing ROM will issue 8D-8D-8D command switching sequence and then will read the boot image in 8D-8D-8D mode with read command specified in SFDP header

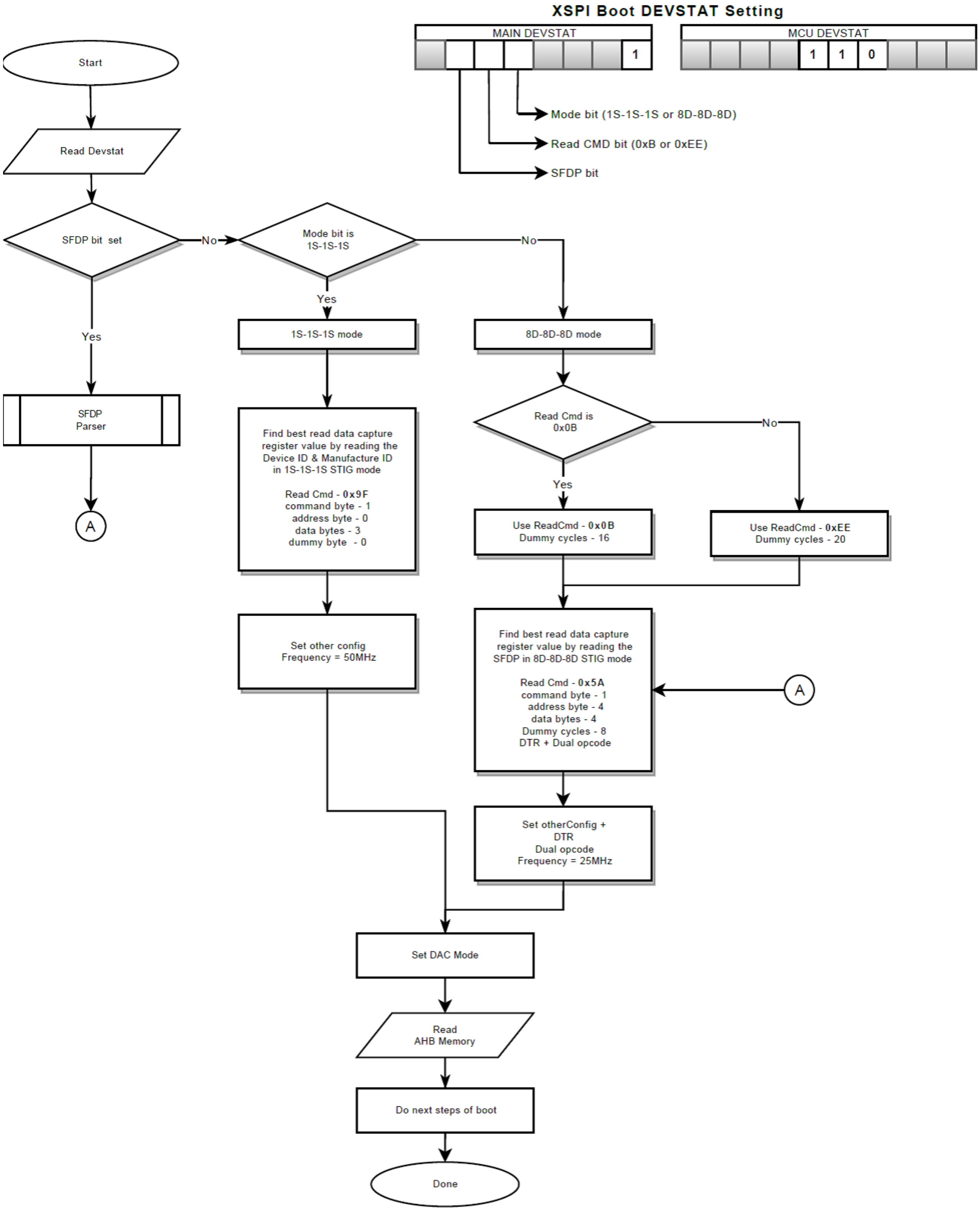


Figure 5-5. ROM SFDP Parser Flow

5.4.1.3 QSPI Boot

QSPI Boot Configuration Fields shows configuration pins assignment to functions when boot mode is QSPI using the OSPI module.

Table 5-10. QSPI Boot Configuration Fields

Field	Value	Description
Csel	0	CSel 0
	1	Csel 1

QSPI Boot Pin Usage summarizes the OSPI pin configuration done by ROM code for QSPI boot device on port 0.

Table 5-11. QSPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Strength Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG_6
OSPI0_CSn0	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.3.1 QSPI Bootloader Operation

The QSPI boot mode supports 1S-1S-4S mode only. The ROM issues a Read Command (0x6B) through the DAC interface of the controller followed by a 24 bit (3 byte) address (the starting address is all zeros) and then 8 dummy cycles. The flash device can then respond with 4-bit data from the starting address. The data reads linearly (and read commands possibly re-issued) until the end of the image has been reached. The frequency of operation supported is 50MHz.

5.4.1.3.2 QSPI Initialization Process

In the QSPI boot mode, the ROM Code initializes the OSPI module and the image is read from the QSPI flash connected to the selected chip-select. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM. See *QSPI Boot Device Configuration* for OSPI port settings.

A detailed summary of the QSPI boot parameter table and the boot configuration definitions are listed in*QSPI Boot Parameter Table*.

5.4.1.3.3 QSPI Loading Process

QSPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

5.4.1.4 SPI Boot

SPI Boot Configuration Fields shows configuration pins assignment to functions when boot mode is SPI using the OSPI module.

Table 5-12. SPI Boot Configuration Fields

Field	Value	Description
Mode	0	SPI Mode 0
	1	SPI Mode 3
Csel	0	Boot Flash is on CS 0
	1	Boot Flash is on CS 1

SPI Boot Pin Usage summarizes the OSPI pin configuration done by ROM code for SPI boot device on port 0.

Table 5-13. SPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_CSn0	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.1.4.1 SPI Bootloader Operation

Please refer to *OSPI\SPI Boot* for more information that applies to SPI boot mode

The SPI boot mode supports the 1S-1S-1S mode only. The Read Command is 8-bits (0x03) followed by a 24 bit (3 byte) address. There are no dummy cycles issued after the read command. The frequency of operation supported is 6.250 MHz. OSPI0_D0 will have data transfers **FROM** the processor **TO** the flash device, and OSPI0_D1 will have data transfers **TO** the processor **FROM** the flash device

5.4.2 SD Card Boot

SD Card Boot Configuration Fields shows configuration pins assignment to functions when boot mode is the SD card boot mode.

Table 5-14. SD Card Boot Configuration Fields

SD Card Boot Configuration Fields		
Field	**Value**	**Description**
Port	0	Port0 (8/4 Bit Width)
	1	Reserved
FS/Raw	0	Filesystem mode
	1	Raw Mode

SD Card (MMCSD1) Pin Usage summarizes the MMCSD pin configuration done by ROM code for SD Card boot on port1 (MMCSD1). SD Card boot on Port 0 (MMCSD0) is not supported.

Table 5-15. SD Card (MMCSD1) Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
MMC0_DAT7	MMC0_DAT7	Disable	NA	0	Enable	0	PADCONFIG126
MMC0_DAT6	MMC0_DAT6	Disable	NA	0	Enable	0	PADCONFIG127
MMC0_DAT5	MMC0_DAT5	Disable	NA	0	Enable	0	PADCONFIG128
MMC0_DAT4	MMC0_DAT4	Disable	NA	0	Enable	0	PADCONFIG129
MMC0_DAT3	MMC0_DAT3	Disable	NA	0	Enable	0	PADCONFIG130
MMC0_DAT2	MMC0_DAT2	Disable	NA	0	Enable	0	PADCONFIG131
MMC0_DAT1	MMC0_DAT1	Disable	NA	0	Enable	0	PADCONFIG132
MMC0_DAT0	MMC0_DAT0	Disable	NA	0	Enable	0	PADCONFIG133
MMC0_CLK	MMC0_CLK	Disable	NA	0	Enable	0	PADCONFIG134
MMC0_CLKLB	MMC0_CLKLB	Disable	NA	0	Enable	0	PADCONFIG135
MMC0_CMD	MMC0_CMD	Disable	NA	0	Enable	0	PADCONFIG136

Note

MMC0_CLKLB signal is not pinned out on the device. The pinmux configuration enables the input buffer of the internal loopback clock.

Note

MMC0_SDWP is not configured by ROM since the ROM never writes to the SD card.

5.4.2.1 SD Card Bootloader Operation

The ROM will boot from SD cards using one of these methods:

- User Data Area (UDA) in raw mode
- User Data Area (UDA) in filesystem mode

The ROM is capable of booting from any size SD card because the MMCSD controller is responsible for addressing. Only single data rate with backward compatible interface timing is supported.

The MMCSD module depends on proper voltage level on the SD card detect signal (SDCD). If SDCD=1, the ROM will assume the card is not present and will fail the boot mode.The SDCD must be 0 for the ROM to continue to attempt to boot. Card detect using DAT3 is not supported. If the card is detected, the initial discovery phase is performed:

1. Send CMD 0. (GO IDLE, both for MMC and SD)

2. Send CMD 55. If the card responds then the card type is assumed to be SD. On timeout the code sends CMD 1. If there is a response then the card type is MMC.

The ROM Code will start reading from the MMCSD memory boot sector, or filesystem, as specified by the BOOTMODE pin (FS/Raw). Only FAT32 and FAT16 formats are supported in filesystem mode. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. In RAW mode, the ROM supports a redundant image at offset 0x400000 in case the initial image fails to be recognized. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

When SD Card boot is used as a backup boot option, only User Data Area (UDA) in filesystem mode is supported. Raw mode is not supported. Additionally, boot will only occur in 1-bit mode during backup booting.

5.4.3 eMMC Boot

eMMC uses the same pins as the MMC card. See *SD Card Boot* for details

5.4.3.1 eMMC Bootloader Operation

Booting from an eMMC device is available on the MMCSD controller.

The ROM will boot from eMMC devices using one of these methods:

- User Data Area (UDA) in raw mode
- User Data Area (UDA) in filesystem mode
- eMMC bootmode (alternate)

To boot from UDA in either raw or filesystem mode, choose bootmode "MMCSD Boot" (see *Primary Boot Mode Selection*).

A special alternate boot mode is available with eMMC devices which allows the ROM to boot from an image that is in a separate boot partition in the eMMC. To boot from this mode, choose "eMMC Boot" (see *Primary Boot Mode Selection*).

The ROM Code will start reading from the memory boot sector, or filesystem, as specified by the BOOTMODE pin (FS/Raw). Only FAT32 and FAT16 formats are supported in filesystem mode. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. In RAW mode, the ROM supports a redundant image at offset 0x400000 in case the initial image fails to be recognized. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

When eMMC boot is used as a backup boot option, only User Data Area (UDA) in filesystem mode is supported. Raw mode is not supported. Additionally, boot will only occur in 1-bit mode during backup booting.

5.4.4 Ethernet Boot

*Ethernet RGMII Boot Configuration Field*s shows configuration pins assignment to functions when boot mode is the Ethernet RGMII mode.

Table 5-16. Ethernet RGMII Boot Configuration Fields

Field	Value	Description
Link Stat	0	Phy scan used for speed and duplex set up
	1	RHMII status register used for speed and duplex set up

Ethernet RMII Boot Configuration Fields shows configuration pins assignment to functions when boot mode is the Ethernet RMII mode.

Table 5-17. Ethernet RMII Boot Configuration Fields

Field	Value	Description
Clkout	0	50 MHz clock not generated on CLKOUT0
	1	50 MHz clock generated on CLKOUT0
Clk src	0	External clock source for RMII1_REF_CLK
	1	Internal clock source for RMII1_REF_CLK

Table 5-18 shows configuration pins assignment to functions when the backup boot mode Ethernet. The Interface configuration field chooses which interface will be used (RGMII or RMII)

Table 5-18. Ethernet Backup Boot Configuration Field

Field	Value	Description
Interface	0	RGMII with internal TX delay
	1	RMII with external clock source

Table 5-19 summarizes the RGMII pin configuration done by ROM code for Ethernet boot device on RGMII port.

Table 5-19. RGMII Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
RGMII1_TX_CTL	RGMII1_TX_CTL	Disable	NA	0	Disable	0	PADCONFIG75
RGMII1_TXC	RGMII1_TXC	Disable	NA	0	Disable	0	PADCONFIG76
RGMII1_TD0	RGMII1_TD0	Disable	NA	0	Disable	0	PADCONFIG77
RGMII1_TD1	RGMII1_TD1	Disable	NA	0	Disable	0	PADCONFIG78
RGMII1_TD2	RGMII1_TD2	Disable	NA	0	Disable	0	PADCONFIG79
RGMII1_TD3	RGMII1_TD3	Disable	NA	0	Disable	0	PADCONFIG80
RGMII1_RX_CTL	RGMII1_RX_CTL	Disable	NA	0	Enable	0	PADCONFIG81
RGMII1_RXC	RGMII1_RXC	Disable	NA	0	Enable	0	PADCONFIG82
RGMII1_RD0	RGMII1_RD0	Disable	NA	0	Enable	0	PADCONFIG83
RGMII1_RD1	RGMII1_RD1	Disable	NA	0	Enable	0	PADCONFIG84
RGMII1_RD2	RGMII1_RD2	Disable	NA	0	Enable	0	PADCONFIG85

Table 5-19. RGMII Pin Usage (continued)

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
RGMII1_RD3	RGMII1_RD3	Disable	NA	0	Enable	0	PADCONFIG86
MDIO0_MDIO	MDIO0_MDIO	Disable	NA	0	Enable	0	PADCONFIG87
MDIO0_MDC	MDIO0_MDC	Disable	NA	0	Disable	0	PADCONFIG88

Table 5-20 summarizes the RMII pin configuration done by ROM code for Ethernet boot device on RMII port.

Table 5-20. RMII Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
RGMII1_RX_CTL	RMII1_RX_ER	Disable	NA	0	Enable	1	PADCONFIG81
RGMII1_RXC	RMII1_REF_CLK	Disable	NA	0	Enable	1	PADCONFIG82
RGMII1_RD0	RMII1_RXD0	Disable	NA	0	Enable	1	PADCONFIG83
RGMII1_RD1	RMII1_RXD1	Disable	NA	0	Enable	1	PADCONFIG84
RGMII1_TD0	RMII1_TXD0	Disable	NA	0	Disable	1	PADCONFIG77
RGMII1_TD1	RMII1_TXD1	Disable	NA	0	Disable	1	PADCONFIG78
RGMII1_TX_CTL	RMII1_TX_EN	Disable	NA	0	Disable	1	PADCONFIG75
RGMII1_TXC	RMII1_CRS_DV	Disable	NA	0	Enable	1	PADCONFIG76
RGMII1_TD3(1)	CLKOUT0	Disable	NA	0	Enable	1	PADCONFIG80
MDIO0_MDIO	MDIO0_MDIO	Disable	NA	0	Enable	1	PADCONFIG87
MDIO0_MDC	MDIO0_MDC	Disable	NA	0	Disable	1	PADCONFIG88

(1) Enabled when CLKOUT0 option is selected from boot pin selection.

5.4.4.1 Ethernet Bootloader Operation

5.4.4.1.1 Ethernet Initialization Process

When the device is set to boot through the Ethernet mode, the ROM Code configures the Ethernet module and the interface mode (RMII, RGMII) according the the BOOTMODE pin settings, see *Ethernet Boot Device Configuration*. Also consult the boot parameter table for the Ethernet boot, see *Ethernet Boot Parameter Table*.

When Link Info = 0, the link parameters are read using MDIO scan. This is the typical setting when using an external PHY. With these parameters, the ROM identifies the PHY and establishes link with the supported speed and duplex mode.

When Link Info = 1, no MDIO scan is performed, and the link parameters are programmed by the ROM based on the RGMII status register. This is the typical setting when configured as a MAC to MAC RGMII interface whereby RGMII pins of two devices can be connected diretly and establish link in force mode. The chosen configuration will be Gigabit, full duplex mode.

Note that booting from RGMII requires that an attached PHY be configured for RGMII-ID Mode immediately upon exiting reset. The ROM will not make this configuration change to the PHY.

The ROM will setup RGMII mode enabling internal delay mode.

5.4.4.1.2 Ethernet Loading Process

After device configuration, the bootloader performs a standard BOOTP/TFTP boot. The device sends a BOOTP request with its MAC address to a host TFTP server to be assigned an IP from a pool of addresses. The timeout for each BOOTP packet is 4 seconds, and the ROM will attempt 10 BOOTP retries, after which the boot mode will fail. If the connection is established, the device initiates a TFTP download and is able to receive image data encapsulated in Ethernet packets, see *Ethernet Boot Data Formats*. There is a timeout of 1 second to receive a response for the READ request, and the ROM will retry the READ request 10 times, after which the boot mode will fail. If TFTP download is successful, data received is stripped of its network headers and the boot data is stored in internal RAM. When the transfer completes and the image is found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

5.4.4.1.3 Ethernet Boot Data Formats

Ethernet boot uses the BOOTP/TFTP protocol for downloads. Only IPv4 is supported.

5.4.4.1.3.1 Limitations

- Received packets cannot be IP fragmented (should not be a problem in most systems since the BOOTP/TFTP packets have fixed lengths of small size)
- Only DIX Ethernet headers are supported.
  - 802.3 with SNAP/LLC not supported
  - DIX Ethernet with VLAN not supported
  - 802.3 with VLAN and SNAP/LLC not supported

5.4.4.1.3.2 BOOTP Request

5.4.4.1.3.2.1 MAC Header (DIX)

- Destination MAC = value from parameter table (default is broadcast)
- Source MAC = value from parameter table (default is e-fuse value)
- Type = IPv4 (0x0800)

5.4.4.1.3.2.2 IPv4 Header

- Version = 4
- Header length = 0
- TOS = 0
- Len = computed during operation
- ID = 0x0001
- Flags + Fragment offset = 0
- TTL = 0x10
- Protocol = UDP (17)
- Header checksum = Computed during operation
- SRC IP = 0.0.0.0
- Dest IP = 255.255.255.255

5.4.4.1.3.2.3 UDP Header

- Source port = BOOTP client (68 decimal)
- Destination Port = BOOTP server (67 decimal)
- Length = computed during operation
- Checksum = computed during operation

5.4.4.1.3.2.4 BOOTP Payload

- Opcode = Request (1)
- HW Type = Ethernet (1)
- HW Addr Len = 6
- Hop Count = 0
- Transaction ID = 1
- Number of seconds = 0
- Client IP = 0.0.0.0
- Your IP = 0.0.0.0
- Server IP = 0.0.0.0
- Gateway IP = 0.0.0.0
- Client HW Address = Device MAC address (from parameter table)
- Server hostname = NULL
- Filename = NULL
- Option 60, Vendor ID string, from parameter table
- Option 61, Client ID string, from parameter table

5.4.4.1.3.2.5 TFTP

There are no ROM code specific TFTP configurations.

5.4.5 USB Boot

USB Boot Configuration Fields shows configuration pins assignment to functions when boot mode is the USB mode.

Table 5-21. USB Boot Configuration Fields

USB Configuration Fields for Primary Boot Mode		
Field	**Value**	**Description**
Mode	0	DFU
Lane Swap	0	No swapping of DP/DM
	1	DP/DM is swapped
Core Voltage	0	VDD_CORE is .85
	1	VDD_CORE is .75

USB Port 0 Pin Usage summarizes the USB pin configuration done by ROM code for USB boot device on port 0.

Table 5-22. USB Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
USB0_DRVVBUS	USB0_DRVVBUS	Disable	NA	0	Disable	0	PADCONFIG149

Note

Note that other USB pins do not have pin mux options. USB_DRVVBUS is configured in DFU mode even though it is not used.

Note on USB backup boot:

- Lane Swap (D+/D- lines) are not allowed

Configurability (pins) of these options do not exist in the USB backup boot mode.

CAUTION
A USB Type-AB connector should not be connected to another host when the device is booting as a USB Host. This will prevent two USB power sources from being connected together.

5.4.5.1 USB Bootloader Operation

The USB boot mode is used to read the boot image from external USB host.

See *USB Boot Device Configuration* and *USB Boot Parameter Table* for the available configuration options.

More information about USB DFU protocol can be found at http://www.usb.org/sites/default/files/DFU_1.1.pdf.

In DFU mode, the ROM will attempt an enumeration for 60 seconds, after which the boot mode will fail. If a successful enumeration is achieved, the ROM Code will start reading from the external host as specified by the BOOTMODE pins. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

5.4.5.1.1 USB-Specific Attributes

5.4.5.1.1.1 DFU Device Mode

- Vendor ID = 0x451
- Product ID = 0x6165
- Device ID = 0

5.4.6 UART Boot

ROM Code always configures the UART port to 115200 kbaud, 8-n-1 mode, and the XMODEM protocol is used to transfer the boot data.

UART Port 0 Pin Usage summarizes the UART pin configuration done by ROM code for UART host on port 0.

Table 5-23. UART Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
UART0_TXD	UART0_TXD	Disable	NA	0	Disable	0	PADCONFIG115
UART0_RXD	UART0_RXD	Disable	NA	0	Enable	0	PADCONFIG114

5.4.6.1 UART Bootloader Operation

5.4.6.1.1 Initialization Process

In the UART boot mode, the selected UART module (port) is the only peripheral configured. The baud rate, data, parity, and stop bits are configured based on the information in the UART boot parameter table. The boot parameter table definitions and the boot configuration values that can be set are in *UART Boot Device Configuration* and *UART Boot Parameter Table*.

Once the ROM Code configures the UART, it sends the UART pings for few seconds, which can be seen in the host. The pings consist of an ASCII capital *C* character. The UART boot mode supports only the CRC mode of XMODEM and does not support CHECKSUM mode. Both 128 and 1024 byte block sizes are supported.

5.4.6.1.2 UART Loading Process

Before the ping from the device stops, load the boot image from the host using the XMODEM protocol.

5.4.6.1.2.1 UART XMODEM

The XMODEM protocol is used to transfer boot data. Only CRC mode is supported (not checksum), with both 128- and 1024-byte block sizes. The general, format of received frames is shown in *XMODEM 1024- and 128-byte Data Frames* and *XMODEM Data Frame Fields*.

Table 5-24. XMODEM 1024- and 128-byte Data Frames

<table>
<tr><td>STX</td><td>Block Num</td><td>Inv Block Num</td><td colspan="4">1024 data bytes</td><td>CRC</td><td>CRC</td></tr>
<tr><td>SOH</td><td>Block Num</td><td>Inv Block Num</td><td>128 data bytes</td><td>CRC</td><td>CRC</td><td colspan="3"></td></tr>
</table>

Table 5-25. XMODEM Data Frame Fields

Field	Value	Description
STX	0x02	The start character for 1024-byte CRC data blocks
SOH	0x01	The start character for 128-byte CRC data block
Block Num	0x01-0xFF – 0x00	The block number. The first block has value 1, and the block number wraps around 0xFF to 0
Inv Block Num	0xFE-0x00	The inverse block number (bit inverse of the block number)
CRC	Calculated	The 16-bit CRC generated from the polynomial 0x1021

The XMODEM protocol is implemented as a half-duplex protocol as shown in *Example of XMODEM Transfer protocol*.

Table 5-26. Example of XMODEM Transfer protocol

Transmitter Sends		Receiver Sends
	←	Ping (‘C’)
Frame 1	→	
	←	ACK (or NACK)
Frame 2	→	
	←	ACK (or NACK)
EOT	→	

Table 5-26. Example of XMODEM Transfer protocol (continued)

Transmitter Sends		Receiver Sends
	←	ACK (or NACK)

5.4.6.1.3 UART Hand-Over Process

Once the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

5.4.7 Serial NAND Boot

Serial NAND Configuration Fields table shows configuration pins assignment to functions when boot mode is Serial NAND.

Table 5-27. Serial NAND Configuration Fields

Field	Value	Description
Read Mode 2	0	Reserved (Read mode is taken from Read Mode 1
	1	SPI/ 1-1-1 mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)
Read Mode 1	0	OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)
	1	OSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)

Serial NAND Pin Usage table summarizes the pin configuration done by ROM code for the Serial NAND device.

Table 5-28. Serial NAND Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_DQS	OSPI0_DQS	Disable	NA	0	Enable	0	PADCONFIG2
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG6
OSPI0_D4	OSPI0_D4	Disable	NA	0	Enable	0	PADCONFIG7
OSPI0_D5	OSPI0_D5	Disable	NA	0	Enable	0	PADCONFIG8
OSPI0_D6	OSPI0_D6	Disable	NA	0	Enable	0	PADCONFIG9
OSPI0_D7	OSPI0_D7	Disable	NA	0	Enable	0	PADCONFIG10
OSPI0_CSn0	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.4.7.1 Serial NAND Bootloader Operation

Serial NAND defines 1S-1S-1S mode for general backwards compatibility, and 1S-1S-8S for maximum throughput (S here means *S*ingle Data rate). Serial NAND memory array is organized into pages of size 2KB/4KB. Read is a two-step process where a complete page is first read into flash's internal buffer/cache using Page read command and then the host controller reads from internal buffer in 1- or 4- or 8-bit mode using the read commands. Page read command that is issued is 0x13, followed by 24 address bits. The frequency of operation supported is 50 MHz.

For 1S-1S-1S mode of operation (Bit-width =1, Single Data Rate). The Command and Address issued are 8 bits and 16 bits respectively. The Read Command that is issued is 0x0B, followed by address bits and 8 dummy cycles.

For 1S-1S-8S mode of operation (Bit-width =8, Single Data Rate). The Command and Address issued are 8 bits and 16 bits respectively. The Read Command that is issued is 0x8B, followed by address bits and 8 dummy cycles. Additionally, flash is configured in 8-bit mode after POR through volatile configuration register if the manufacturer is Winbond.

For 1S-1S-4S mode of operation (Bit-width =4, Single Data Rate). The Command and Address issued are 8 bits and 16 bits respectively. The Read Command that is issued is 0x6B, followed by address bits and 8 dummy cycles. Note that in 8-bit mode pin mux is done for all 8 OSPI data lines and in 4-bit/1-bit mode pin mux is done for 4 OSPI data lines. This is done to disable the HOLD functionality feature in 1-bit mode.

Serial NAND boot expects ECC to be auto-managed by the flash. Most of the flashes have the ECC enabled by default and can do 1-bit correction and 2-bit detection for ECC errors. ROM checks for 2-bit ECC error via status register 3 (address 0xC0) bit 5 after every page load. In case of 2-bit ECC error the boot will fail and ROM will take the fallback option.

Serial NAND boot also manages bad blocks that can be present in the flash at time of shipment or develop during the lifetime. Bad block marker is a non-FFh data byte stored at Byte 0 of spare area of Page 0 for each bad block and ROM checks for the same while reading the first page of a memory block. ROM will skip the particular block if it is marked as bad and move to the next one.

The Serial NAND driver in ROM does not support devices that have multiple planes as they require special handling to read even numbered blocks

5.4.7.2 Serial NAND Initialization Process

In the OSPI boot mode, the ROM Code initializes the OSPI module and the image is read from the OSPI flash connected to the selected chip-select. If the image fails to be read correctly from offset 0x0 of the flash memory, the ROM will attempt to obtain the image at offset 0x400000. This is the only redundant image location supported by the ROM. See *OSPI Boot Device Configuration* for OSPI port settings.

A detailed summary of the OSPI boot parameter table and the boot configuration definitions are listed in *OSPI Boot Parameter Table*.

5.4.7.3 Serial NAND Loading Process

OSPI boot mode is not eXecute-In-Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

5.4.8 No boot/Development boot

No-boot/Dev-boot Configuration Fields shows configuration pins assignment to functions when boot mode is the No-boot mode.

Table 5-29. No-boot/Dev-boot Configuration Fields

Field	Value	Description
No/Dev	0	Development Boot
	1	No boot
ARM/Thumb	0	ARM mode
	1	Thumb mode

These boot modes are useful for debugging purposes to preclude the execution of the ROM.

5.5 PLL Configuration

ROM code must be aware of the reference clock provided to PLLs. That is, the speed of the quartz crystal, or the clock supplied by an external clock oscillator. On how to indicate the PLL reference clock, see *PLL Reference Clock Selection*.

ROM code configures only PLLs which are required during boot. Therefore, if a PLL is required for the backup boot mode but not the primary boot mode, and if the backup boot mode never executes, then the PLLs required for backup boot are not enabled.

The following tables show the HSDIV values that are programmed by the R5 ROM if a boot mode uses it. A value of NA means that the ROM does not program that HSDIV.

For details on where these values come from, please refer to *PLL Configuration Background*.

Table 5-30. MAIN_PLL0 (MAIN PLL) (2000MHz)

PLL POSTDIV	HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
0	HSDIV0	4	500	MAIN SYSCLK0
0	HSDIV1	10	200	OSPI
0	HSDIV2	0	NA	WKUP_CLKOUT
0	HSDIV3	0	NA	Reserved
0	HSDIV4	0	NA	MCAN
1	HSDIV5	5	200	eMMC0
1	HSDIV6	0	NA	CPTS
1	HSDIV7	4	250	TIMER
1	HSDIV8	0	NA	USB0
1	HSDIV9	0	NA	ASRC

Table 5-31. MAIN_PLL1 (PER0 PLL) (1920MHz)

PLL POSTDIV	HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
0	HSDIV0	10	192	UART
0	HSDIV1	12	160	Not Used
0	HSDIV2	0	NA	WKUP_CLKOUT
0	HSDIV3	0	NA	TIMER
0	HSDIV4	0	NA	ADC
1	HSDIV5	6	NA	OSPI
1	HSDIV6	0	NA	McASP

Table 5-32. MAIN_PLL2 (PER1 PLL) (2000MHz)

PLL POSTDIV	HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
0	HSDIV0	0	NA	ATL
0	HSDIV1	8	250	CPSW_3GUSS
0	HSDIV2	10	200	eMMC SD
0	HSDIV3	0	NA	DebugSS
0	HSDIV4	0	NA	Hyperbuss
1	HSDIV5	0	NA	SPI
1	HSDIV6	0	NA	TIMER
1	HSDIV7	0	NA	Reserved
1	HSDIV8	0	NA	McASP
1	HSDIV9	0	NA	WKUP_CLKOUT

Table 5-33. MAIN_PLL15 (2400MHz)

HSDIV	Value	Frequency(MHz)	Boot Peripheral/IP
HSDIV0	6	400	HSM/SMS
HSDIV1	6	400	SA3_UL PKA
HSDIV5	3	800	DM

Table 5-34. MAIN_PLL14 (2400MHz)

HSDIV	Value	Frequency	Boot Peripheral/IP
HSDIV0	3	800	Pulsar

Note

All other PLLs are not used or programmed by the ROM

Note

The bringup and configuration of bootmode-specific PLLs by ROM code will result in a bootmode-specific device clocking setup which for example has an impact on which peripheral modules can readily be clocked and used by SBL/SPL prior to loading and bringing up System Firmware (SYSFW)

5.5.1 PLL Configuration Background

PLL Configuration shows the HSDIV values that are programmed by the R5 ROM. This section shows all HSDIV calculations for PLL including items **not** programmed by ROM. For details on FOUTVCO_P and FOUTPOSTDIV, see *PLL Output Clocks*.

Table 5-35. MAIN_PLL0 (MAIN PLL) (2000MHz)

PLL POSTDIV	HSDIV	Formula	Notes
0	MAIN_PLL0_HSDIV0_CLKOUT	FOUTVCO_P/HSDIV0	FOUTVCO_P default value is 2000MHz
0	MAIN_PLL0_HSDIV1_CLKOUT	FOUTVCO_P/HSDIV1	FOUTVCO_P default value is 2000MHz
0	MAIN_PLL0_HSDIV2_CLKOUT	FOUTVCO_P/HSDIV2	FOUTVCO_P default value is 2000MHz
0	MAIN_PLL0_HSDIV3_CLKOUT	Reserved	Reserved
0	MAIN_PLL0_HSDIV4_CLKOUT	FOUTVCO_P/HSDIV4	FOUTVCO_P default value is 2000MHz
1	MAIN_PLL0_HSDIV5_CLKOUT	FOUTPOSTDIV/HSDIV5	FOUTPOSTDIV default value is 1000MHz
1	MAIN_PLL0_HSDIV6_CLKOUT	FOUTPOSTDIV/HSDIV6	FOUTPOSTDIV default value is 1000MHz
1	MAIN_PLL0_HSDIV7_CLKOUT	FOUTPOSTDIV/HSDIV7	FOUTPOSTDIV default value is 1000MHz
1	MAIN_PLL0_HSDIV8_CLKOUT	FOUTPOSTDIV/HSDIV8	FOUTPOSTDIV default value is 1000MHz
1	MAIN_PLL0_HSDIV9_CLKOUT	FOUTPOSTDIV/HSDIV9	FOUTPOSTDIV default value is 1000MHz

Table 5-36. MAIN_PLL1 (PER0 PLL) (1920MHz)

PLL POSTDIV	HSDIV	Formula	Notes
0	MAIN_PLL1_HSDIV0_CLKOUT	FOUTVCO_P/HSDIV0	FOUTVCO_P default value is 1920MHz
0	MAIN_PLL1_HSDIV1_CLKOUT	FOUTVCO_P/HSDIV1	FOUTVCO_P default value is 1920MHz
0	MAIN_PLL1_HSDIV2_CLKOUT	FOUTVCO_P/HSDIV2	FOUTVCO_P default value is 1920MHz
0	MAIN_PLL1_HSDIV3_CLKOUT	FOUTVCO_P/HSDIV3	FOUTVCO_P default value is 1920MHz
0	MAIN_PLL1_HSDIV4_CLKOUT	FOUTVCO_P/HSDIV4	FOUTVCO_P default value is 1920MHz

Table 5-36. MAIN_PLL1 (PER0 PLL) (1920MHz) (continued)

PLL POSTDIV	HSDIV	Formula	Notes
1	MAIN_PLL1_HSDIV5_CLKOUT	FOUTPOSTDIV/HSDIV5	FOUTPOSTDIV default value is 960MHz
1	MAIN_PLL1_HSDIV6_CLKOUT	FOUTPOSTDIV/HSDIV6	FOUTPOSTDIV default value is 960MHz

Table 5-37. MAIN_PLL2 (PER1 PLL) (2000MHz)

PLL POSTDIV	HSDIV	Formula	Notes
0	MAIN_PLL2_HSDIV0_CLKOUT	FOUTVCO_P/HSDIV0	FOUTVCO_P default value is 2000MHz
0	MAIN_PLL2_HSDIV1_CLKOUT	FOUTVCO_P/HSDIV1	FOUTVCO_P default value is 2000MHz
0	MAIN_PLL2_HSDIV2_CLKOUT	FOUTVCO_P/HSDIV2	FOUTVCO_P default value is 2000MHz
0	MAIN_PLL2_HSDIV3_CLKOUT	FOUTVCO_P/HSDIV3	FOUTVCO_P default value is 2000MHz
0	MAIN_PLL2_HSDIV4_CLKOUT	FOUTVCO_P/HSDIV4	FOUTVCO_P default value is 2000MHz
1	MAIN_PLL2_HSDIV5_CLKOUT	FOUTPOSTDIV/HSDIV5	FOUTPOSTDIV default value is 1000MHz
1	MAIN_PLL2_HSDIV6_CLKOUT	FOUTPOSTDIV/HSDIV6	FOUTPOSTDIV default value is 1000MHz
1	MAIN_PLL2_HSDIV7_CLKOUT	Reserved	Reserved
1	MAIN_PLL2_HSDIV8_CLKOUT	FOUTPOSTDIV/HSDIV8	FOUTPOSTDIV default value is 1000MHz
1	MAIN_PLL2_HSDIV9_CLKOUT	FOUTPOSTDIV/HSDIV9	FOUTPOSTDIV default value is 1000MHz

Table 5-38. MAIN_PLL4 (Audio PLL) (2359.296MHz)

PLL POSTDIV	HSDIV	Formula	Notes
0	MAIN_PLL4_HSDIV0_CLKOUT	FOUTVCO_P/HSDIV0	FOUTVCO_P default value is 2539.296MHz
0	MAIN_PLL4_HSDIV1_CLKOUT	FOUTVCO_P/HSDIV1	FOUTVCO_P default value is 2539.296MHz
0	MAIN_PLL4_HSDIV2_CLKOUT	FOUTVCO_P/HSDIV2	FOUTVCO_P default value is 2539.296MHz
0	MAIN_PLL4_HSDIV3_CLKOUT	FOUTVCO_P/HSDIV3	FOUTVCO_P default value is 2539.296MHz

Table 5-39. MAIN_PLL7 (C7x PLL)

PLL POSTDIV	HSDIV	Formula	Notes
0	MAIN_PLL7_HSDIV0_CLKOUT	FOUTVCO_P/HSDIV0	FOUTVCO_P default value is 2550MHz
0	MAIN_PLL7_HSDIV1_CLKOUT	FOUTVCO_P/HSDIV1	FOUTVCO_P default value is 2550MHz

Table 5-40. MAIN_PLL14 (R5FSS PLL)

PLL POSTDIV	HSDIV	Formula	Notes
0	MAIN_PLL14_HSDIV0_CLKOUT	FOUTVCO_P/HSDIV0	FOUTVCO_P default value is 2400MHz

Table 5-41. MAIN_PLL5 (SMS PLL) (2400MHz)

PLL POSTDIV	HSDIV	Formula	Notes
0	MAIN_PLL15_HSDIV0_CLKOUT	FOUTVCO_P/HSDIV0	FOUTVCO_P default value is 2400MHz
0	MAIN_PLL15_HSDIV1_CLKOUT	FOUTVCO_P/HSDIV1	FOUTVCO_P default value is 2400MHz
0	MAIN_PLL15_HSDIV2_CLKOUT	FOUTVCO_P/HSDIV2	FOUTVCO_P default value is 2400MHz

Note

HSDIV_CTRL registers set the divider to HSDIV bit value + 1

5.6 Boot Parameter Tables

The boot parameter tables direct the main module boot process. On cold boot the tables are created based on pin strapped values (see *Boot Mode Pins* and built-in data. The ROM Code supports two parameter tables stored as an array in a fixed memory address in the MSRAM, each of size 512 bytes. The ROM will attempt to boot using the primary table. On boot failure, ROM Code will retry using the second table.

Using two tables handles two cases.

- The first is in initial board manufacture where the primary boot table specifies boot from a flash device, and the flash is blank. ROM Code would then switch to the secondary boot mode which would receive the image externally (Ethernet, USB, UART) and this image would flash the boot image.
- The second case is failure due to total flash corruption. In all flash parameter tables there exist backup addresses within the primary boot mode. This covers the problem of a flash update failure with a backup image present on the same flash device.

The boot tables reside at a fixed location in memory which is described in *Global Memory Addresses Used by ROM Code*.

5.6.1 Common Header

These boot parameter tables have certain parameters common across all the boot modes, while the rest of the parameters are unique to the boot modes. The common entries in the boot parameter table are shown in *Boot Parameter Table Common Header*.

Table 5-42. Boot Parameter Table Common Header

Byte Offset	Size (bytes)	Name	Description
0	2	Length	The length of the table
2	2	Checksum	Ones complement checksum over length bytes in the table. If 0 the checksum is not validated.
4	2	Peripheral	Identifies the boot peripheral and format of the table after the common header. See *Boot Peripheral Selection*
6	2	Reserved	Reserved
8	4	Timeout	Timeout for this boot mode, in milliseconds
12	4	Magic	Magic value 0x01AD0911
16	40	PLL Config 0	PLL Configuration 0. See *Boot Parameter Table PLL Configuration*
56	40	PLL Config 1	PLL Configuration 1
96	40	PLL Config 2	PLL Configuraiton 2
136	40	PLL Config 3	PLL Configuration 3
176	40	PLL Config 4	PLL Configuration 4
216	40	PLL Config 5	PLL Configuration 5

Boot Peripheral Selection lists the possible boot modes used in the boot parameter tables.

Table 5-43. Boot Peripheral Selection

Peripheral Field Value	Description
0	Sleep (No boot)
10	Ethernet Reserved
20	Ethernet BOOTP/TFTP (general)
21	Ethernet RGMII specific
22	Ethernet RMII specific
30	Reserved
31	Reserved
32	Reserved
50	SPI
60	UART

Table 5-43. Boot Peripheral Selection (continued)

Peripheral Field Value	Description
70	USB DFU
71	USB Reserved
80	QSPI
85	OSPI
90	Reserved
100	MMCSD Card (general)
101	eMMC (general)
102	MMC 1-bit
103	MMC 4-bit
104	MMC 8-bit
120	Reserved
130	xSPI
150	Serial NAN
160	Fast-xSPI

5.6.2 PLL Setup

Boot Parameter Table PLL Configuration through *PLL Reference Source Field Description* describe the PLL configuration fields.

Table 5-44. Boot Parameter Table PLL Configuration

Byte Offset	Size (bytes)	Name	Description
0	1	Domain/cfg	See *PLL Domain and Enable Configuration*
1	1	Pll number	PLL number indexed from 0.
2	1	Input source	See *PLL Reference Source Bit Fields*
3	1	Pll Type	This field must be 1 to indicate an SCPLL
4	4	Input Ref Clock	The PLL input clock, in Q16.16 format
8	4	Feed back divider, integer part	Integer value of feedback divider
12	4	Feed back divider, fractional part	Fractional portion of feedback divider. Total divider is the Integer part + (Fractional part / 2^{24})
16	1	Ref divider	Input clock pre-divider
17	1	Post divider 1	Output post divider 1
18	1	Post divider 2	Output post divider 2
19	1	Reserved	Reserved
20	2	Hsdiv Enable	Bit map. A set bit indicates that the corresponding hsdiv is enabled.
22	2	Reserved	Reserved
24	16	Hsdiv[16]	Array of hs divider values.

Table 5-45. PLL Domain and Enable Configuration

7	6	5	4	3	2	1	0
Reserved		Enable		Reserved			Domain

Table 5-46. PLL Domain and Enable Field Description

Field	Value	Description
Enable	0	PLL not configured
	1	PLL enabled only if currently disabled or in bypass
	2	PLL is unconditionally enabled. If currently enabled with a different configuration the PLL is first disabled
	3	PLL is unconditionally disabled
Domain	0	PLL is in the Top Level domain

Table 5-46. PLL Domain and Enable Field Description (continued)

Field	Value	Description
	1	PLL is in the MAIN domain

Table 5-47. PLL Reference Source Bit Fields

7	6	5	4	3	2	1	0
Source Type				Source Index			

Table 5-48. PLL Reference Source Field Description

Field	Value	Description
Source Type	0	Source is HFOSC
	1	Source is external pin
	2	Reserved
	3-7	Reserved
Source Index	0-31	Source index (HFOSC[0-31] or pin[0-31], depending on Source Type) HFOSC[0] – WKUP_HFOSC0 HFOSC[1] – HFOSC1 (in MAIN domain) PIN[1] – EXT_REFCLK1 pin (not all PLLs, see *Clocking*

5.6.3 OSPI/QSPI/SPI Boot Parameter Table

OSPI/SPI Boot Parameter Table shows the boot parameter table for OSPI, QSPI, or SPI boot. Must be preceded with the common boot parameters described in *Boot Parameter Table Common Header*.

Table 5-49. OSPI/SPI Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode on	From Pins	If non-zero, the mode byte will be sent
258	1	Instruct Width	From Pins	Number of pins used to send instructions (1, 2, 4, 8)
259	1	Address Width	From Pins	Number of pins used to send address (1, 2, 4, 8)
260	1	Data Width	From Pins	Number of pins used to received data (1, 2, 4, 8)
261	1	Address Size	24	24, and 32 bits are the valid address sizes
262	1	Mode	0	OSPI clock polarity and phase mode
263	1	CSEL	From Pins	Chip select number (0–3)
264	1	Read Cmd	From Pins	Command used to read read data
265	1	Mode byte	0	Value used for the mode byte (when active)
266	1	Dummy Cycles	From pins	Number of dummy cycles sent after the read command
267	1	clkRecovery	From pins	Clock recovery
268	1	dqsEnable	0	Enable DQS
269	1	Reserved	0	Reserved
270	2	Module Freq	0	The OSPI module frequency after PLL enable, in kHz. If 0, ROM code uses the value from the module clock tables.
272	4	Bus Frequency	From pins	The OSPI bus frequency, in kHz
276	4	Delay	0x08080808 or 0x01010101	The chip select read delays. Default value is based on the read command
280	4	Tap Delay	0xFFFFFFFF	The read tap selection. If 0xFFFFFFFF, the ROM code will scan the taps to find the best delay. The result will then overwrite the value in this table.
284	4	Internal Clk	From pins	0 = external (dqs) 1 = internal
288	4	notDAC	From pins	When 0, DAC mode is used
292	4	Read Index	0	Index to the active read address (0-1)
296	4	Read Addr 0	0x000000	The initial flash read address

Table 5-49. OSPI/SPI Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
300	4	Read Addr 1	0x400000 (0x4000 SPI)	Backup read address
304	4	Reserved	0	Reserved
308	4	Reserved	0	Reserved

5.6.4 UART Boot Parameter Table

UART Boot Parameter Table shows the boot parameter table for UART boot. Must be preceded with the common boot parameters described in *Boot Parameter Table Common Header*.

Table 5-50. UART Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Magic	0x49	Required Magic value
257	1	Protocol	63 (0x3F)	Specifies the transfer protocol = XMODEM
258	2	Reserved	0	Reserved
260	1	Max error Count	10	Error count resulting in boot abort
261	1	Ack timeout	3	Timeout in seconds on ack
262	1	Char timeout	20	Inter-character timeout in milliseconds
263	1	Reserved	0	Reserved
264	4	Port	From Pins	Physical port number
268	4	Mod Ref Clk	48000	Module reference clock, in kHz
272	4	Data Rate	115200	Baud rate (bps)
276	1	Parity	0	0=none, 1=odd, 2=even
277	1	Data bits	8	Only 8 data bit width is supported
278	1	Stop bits	2	Stop bits in Q7.1 format (2 = 1 stop bit)
279	1	Flow Control	0	0=none, 1= RTS/CTS
280	1	Over sample	16	Only 16× and 13× oversample are supported
281	1	Magic 2	0xB7	Required magic value

5.6.5 MMCSD/eMMC Boot Parameter Table

MMCSD/eMMC Boot Parameter Table shows the boot parameter table for eMMC, MMC or SD card boot. Must be preceded with the common boot parameters described in *Boot Parameter Table Common Header.*

Table 5-51. MMCSD/eMMC Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	From Pins	Port for emmc and SD/MMC
257	1	eMMC	From Pins	0 = SD/MMC, else eMMC
258	1	bootAck	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode the controller expects a boot ack from the eMMC
259	1	Media	1 for eMMC 0 for SD/MMC	0 = auto detect card type 1 = MMC 2 = SD
260	1	busWidth	8 for eMMC From Pins for SD/MMC	Number of data pins (1, 4, or 8). If 0, max supported pins of the port are used.
261	1	bootAlt	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode, the controller uses the alt boot method (CMD1 with arg 0xFFFF_FFFA) to initiate data transfer
262	1	sigVolt	0x18 for port0 0x33 for port1	Sets the signal voltage for the controller. 0x18 = 1.8V 0x33 = 3.3V

Table 5-51. MMCSD/eMMC Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
263	1	Reserved	0	Reserved
264	4	Max Bus Freq	0	Max bus frequency in kHz. If 0, the value is determined by reading the CSD register from the card (still maxes out at 25 MHz)
268	4	refClkkHz	0	Module reference clock frequency, in kHz. If 0, the ROM code computes the value.
272	4	respTimeout	40000	The timeout period on initial card read, in milli-seconds, Q3 number format
276	128	Filename	"\tiboot3.bin"	For SD/MMC, boot filename in 16-bit Unicode characters (max 64)
404	4	Mode	0x1144D091	0x1144D091 = file system boot 0x1144C180 = raw image boot
408	4	CardIsInit	0	0 = card not yet initialized 1 = card has been initialized
412	4	Rsvd	0	Reserved
416	4	RawIndex	0	Current active read offset (0 or 1)
420	4	Rsvd	0	Reserved
424	4	Raw Offset 0	0x000000	Raw read offset
428	4	Raw Offset 1	0x400000	Backup raw read offset
432	4	Rsvd	0	Reserved
436	4	Rsvd	0	Reserved

5.6.6 Ethernet Boot Parameter Table

Ethernet Boot Parameter Table is shown segmented into four sections:

1. The first section contains information required to configure the device hardware
2. The second section contains information used by the top level Ethernet module to execute the boot
3. The third section contains information for the Ethernet stack code.
4. The fourth section contains information for creating the BOOTP packet (vendor string, ID string and debug string), and holds information returned in the BOOTP response (Default route and file name)

Ethernet Boot Parameter Table shows the boot parameter table for Ethernet boot. Must be preceded with the common boot parameters described in *Boot Parameter Table Common Heade*r.

Table 5-52. Ethernet Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
Hardware Configuration Options				
256	2	Mod Freq	0	Module clock frequency, kHz. If 0, ROM code computes the value.
258	1	Port Num	0	Physical port number
259	1	Interface	From Pins	0 = RGMII with internal delay 1 = RGMII with external delay 2 = RMII
260	1	Init Level	0	0 = Initialize only not enabled modules 1 = Full ethernet sub-system initialization
261	1	Clock out enable	From pins	0x10 = CLKOUT0 enable 0x11 = CLKOUT0 disable
262	1	Clk out freq	From pins	0x20 = CLKOUT0 25 MHz (RGMII) 0x21 = CLKOUT0 50 MHz (RMII)
263	1	RMII Clk In	From pins	0x60 = RMII internal (SoC) clock 0x61 = RMII external clock
264	1	Port Enable	0x01	Bit map. A set bit indicates that the corresponding physical port will be enabled

Table 5-52. Ethernet Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
265	1	Phy Query	From pins	0x30 = speed/duplex determined from RGMII status register 0x31 = MDIO used to query PHY 0x32 = Use fixed speed/duplex values from offset 266/267.
266	1	Speed		0x40 = full speed (1Gbit for RGMII, 100Mbit for RMII) 0x41 = slow speed (100Mbit for RGMII, 10Mbit for RMII)
267	1	Duplex		0x50 = full duplex 0x51 = half duplex
Main Level Boot Control				
268	1	Bootp enable	1	0 = Image information already in this structure 1 = Use BOOTP to get boot image information
269	1	Reserved	0	Reserved
270	2	Bootp Timeout	4000	BOOTP timeout in milli-seconds
272	2	TFTP timeout	1000	TFTP timeout in milli-seconds
274	2	Bootp retries	10	Number of BOOTP retries before fail
276	2	TFTP retries	10	Number of TFTP retries before fail
278	2	Reserved	0	Reserved
Network Stack Configuration (plus TFTP server ID)				
280	6	MAC Address	From E-fuse	MAC address of the device
286	2	Reserved	0	Reserved
288	4	Device IP	0	IP address of the device. Valid only if BOOTP not enabled
292	4	Net Mask	0	Net mask. Valid only if BOOTP not enabled
296	4	Tftp server IP	0	TFTP server IP. Valid only if BOOTP not enabled
BOOTP send and receive Information				
300	20	Vendor String	"TI K3 Bootp Boot"	BOOTP request vendor string. Valid only if BOOTP not enabled
320	9	Client ID	1-mac-address-0	Client ID. See *RFC1700*
329	1	ID len	7	Client ID length
330	45	Debug array	SOC ID up to size available	Debug array output
375	1	Debug len	Varies	The number of valid bytes in debug array
376	4	Next hop	0	Next hop IP address. Valid only if bootp not enabled
380	4	Default Route	0	IP default route IP address. Valid only if bootp not enabled
384	128	Boot filename	0	Boot filename. Valid only if bootp not enabled

5.6.7 xSPI Boot

xSPI Boot Configuration Fields shows configuration pins assignment to functions when boot mode is xSPI using the OSPI module.

Table 5-53. xSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9	SFDP	0	SFDP disabled
		1	SFDP enabled
8	Read cmd	0	0x0B Read Command
		1	0xEE Read Command
7	Mode	0	1S-1S-1S mode @ 50MHz
		1	8D-8D-8D mode @ 25MHz

xSPI Boot Pin Usage summarizes the OSPI pin configuration done by ROM code for xSPI boot device on port 0.

Table 5-54. xSPI Boot Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Pinmux Sel	Pad Configuration Register
OSPI0_CLK	OSPI0_CLK	Disable	NA	0	Disable	0	PADCONFIG0
OSPI0_DQS	OSPI0_DQS	Disable	NA	0	Enable	0	PADCONFIG2
OSPI0_D0	OSPI0_D0	Disable	NA	0	Enable	0	PADCONFIG3
OSPI0_D1	OSPI0_D1	Disable	NA	0	Enable	0	PADCONFIG4
OSPI0_D2	OSPI0_D2	Disable	NA	0	Enable	0	PADCONFIG5
OSPI0_D3	OSPI0_D3	Disable	NA	0	Enable	0	PADCONFIG6
OSPI0_D4	OSPI0_D4	Disable	NA	0	Enable	0	PADCONFIG7
OSPI0_D5	OSPI0_D5	Disable	NA	0	Enable	0	PADCONFIG8
OSPI0_D6	OSPI0_D6	Disable	NA	0	Enable	0	PADCONFIG9
OSPI0_D7	OSPI0_D7	Disable	NA	0	Enable	0	PADCONFIG10
OSPI0_CSn0	OSPI0_CSn0	Disable	NA	0	Disable	0	PADCONFIG11
OSPI0_CSn1	OSPI0_CSn1	Disable	NA	0	Disable	0	PADCONFIG12

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

5.6.8 USB DFU Boot Parameter Table

USB DFU Boot Parameter Table shows the boot parameter table for USB DFU boot. Must be preceded with the common boot parameters described in *Boot Parameter Table Common Header*.

Table 5-55. USB DFU Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Port	From pins	Physical port number. Always set to 0.
260	4	Base address 0	From pins (port)	Base address of USB subsystem (CMN)
264	4	Base address 1	From pins (port)	Base address of controller
268	4	phyBaseAddress	From pins (port)	Base address of USB PHY module
272	4	modRefClkkHz	varies	Module reference clock, in kHz
276	2	Vendor ID	0x0451	USB vendor ID. Read from control registers.
278	2	Product ID	0x6165	USB product ID. Read from control registers.
280	2	BCD Device	0x200	Binary Coded Decimal device release number
284	4	String Table addr	0x4182A76C	Pointer to the string table in RAM

Table 5-55. USB DFU Boot Parameter Table (continued)

Byte Offset	Size (bytes)	Name	Default Value	Description
288	2	Vendor String offset	0	Offset to vendor string in string table
290	2	Prod string offset	32	Offset to product string in string table
292	2	Serial num string offset	64	Offset to serial number string in string table
294	2	Timeout	5000	USB timeout in milliseconds
296	2	Mode	1	1 = DFU ≠1 = MSC Mode 1 = backup DFU, 2 = backup MSC
298	1	Lane reverse	From pins	Set to non-zero for lane reverse
299	1	CoreVoltage	From pins	USB Core Voltage 0 = 0.85V, 1 = 0.75V
300	4	Block Size	4096	DFU Block Size

5.7 Boot Image Format

5.7.1 Overall Structure

The boot image consists of an X.509 Certificate, which is optional for GP devices, followed immediately by a boot image blob.

X.509 Certificate (Variable Size) (Optional)
Boot Image Blob (Variable Size)

5.7.2 X.509 Certificate

The X.509 certificate is described in RFC5280. Section 4.1 of the specification describes the format.

The X.509 fields relevant to the public boot (taken from RFC5280) are shown below.

```
Certificate  ::=  SEQUENCE  {
        tbsCertificate       TBSCertificate,
        signatureAlgorithm   AlgorithmIdentifier,
        signatureValue       BIT STRING  }
   TBSCertificate  ::=  SEQUENCE  {
        version         [0]  EXPLICIT Version DEFAULT v1,
        serialNumber         CertificateSerialNumber,
        signature            AlgorithmIdentifier,
        issuer               Name,
        validity             Validity,
        subject              Name,
        subjectPublicKeyInfo SubjectPublicKeyInfo,
        issuerUniqueID  [1]  IMPLICIT UniqueIdentifier OPTIONAL,
                             -- If present, version MUST be v2 or v3
        subjectUniqueID [2]  IMPLICIT UniqueIdentifier OPTIONAL,
                             -- If present, version MUST be v2 or v3
        extensions      [3]  EXPLICIT Extensions OPTIONAL
                             -- If present, version MUST be v3
        }
  Extensions  ::=  SEQUENCE SIZE (1..MAX) OF Extension
   Extension  ::=  SEQUENCE  {
        extnID      OBJECT IDENTIFIER,
        critical    BOOLEAN DEFAULT FALSE,
        extnValue   OCTET STRING
                    -- contains the DER encoding of an ASN.1 value
                    -- corresponding to the extension type identified
                    -- by extnID
        }
```

In general, an X.509 certificate contains a public key which has been signed by a private key. The public ROM code does not directly use the keys. In non-secure devices, the public key value is in general a don't care condition. The exception is certificates containing a degenerate RSA public key. GP devices with a degenerate RSA key allow for integrity checking of most (but not all) of the certificate.

The public ROM only needs to extract some of information from the X.509 formatted structure:

- The total size of the X.509 Certificate
- The total size of the boot image

The total size of the X.509 Certificate is determined by reading the length of the sequence containing the certificate. The length of the image is determined by parsing the certificate to find the extension field which holds the image length.

The ROM defines several extensions that are used only by TI for boot. These are placed in the extensions field of the TBS certificate.

5.7.3 Organizational Identifier (OID)

OID (organizational identifier) values are represented as a tree structure. TI has the following node registered:

1.3.6.1.4.1.294: iso(1), identified-organization(3), dod(6), internet(1), private(4), enterprise(1), Texas Instruments(294)

ROM code adds the following branch after *Texas Instruments*: *device-boot(1)*. The OID values shown in this section are leaves off the device boot branch.

5.7.4 X.509 Extensions Specific to Boot

These values are not defined in any standard, but created by TI for boot.

5.7.4.1 Boot Info (OID 1.3.6.1.4.1.294.1.1)

This extension must be present on all boot images. It is from this extension that the image length is extracted.

```
bootInfo ::=  SEQUENCE {
   cert_type: INTEGER,-- identifies the certificate type
   boot_core:INTEGER,-- identifies the boot core
   core_opts:INTEGER,-- 32 or 64 bit boot core target
   load_addr:OCTET STRING,-- Global address image destination
   image_size:INTEGER,-- Image size in bytes
}
```

Table 5-56. Certificate Type Values

Value	Description
0x0000_0001	Primary boot image
0x0000_0002	Firmware image

Table 5-57. Boot Core Values

Value	Description
0x00	Firmware (M4) image
0x08	M4 certificate
0x10	R5 image
0x20	Reserved

Table 5-58. Core Options Bit Fields

31	2	1	0
Reserved		Split	Mode

Table 5-59. Core Options Field Description

Bits	Field	Value	Description
1	Split	0	Dual MCU set to lockstep (two cores in lockstep)
		1	Dual MCU set to split mode (two independent cores)
0	Mode	0	MCU starts execution in Arm® mode
		1	MCU starts execution in Thumb® mode

5.7.4.2 Image Integrity (OID 1.3.6.1.4.1.294.1.2)

```
imageIntegrity ::= SEQUENCE {
   sha_type:OID,-- Identifies the SHA type
   hash:OCTET STRING-- The SHA of the boot image
}
```

5.7.5 Generating X.509 Certificates

X.509 Certificates are generated using OpenSSL and a configuration script to supply values in the extension fields.

5.7.5.1 Key Generation

The SBL must always be signed with a given OpenSSL key - Secure and GP devices. Secure must have encryption and authentication, GP device must only have authentication. The key used for authentication can be random or specific. If a random key is generated and SBL is signed with this,the ROM will copy the SBL image for authentication using memcopy. With this key, ROM code will be directed to use DMA to load the SBL for authentication which saves boot time.

5.7.5.1.1 Degenerate RSA Keys

Degenerate RSA keys are valid RSA keys with the private exponent set to 1. This results in the signature field being equal to the digest, since in RSA:

$$\text{Signature = digestprivExp mod nprivExp mod n}^{\text{privExp}} \qquad (1)$$

Where n is the key size. Since the hash used is SHA-512 and the signature is an ASN.1 sequence containing the OID defining which has was used as well as the hash value, the degenerate RSA must have a value of n greater than the maximum digest size. Typically 1024-bit is chosen.

The following sequence is used to generate degenerate RSA keys:

1. Create a random RSA key:

   ```
   openssl genrsa -out key.pm 1024
   ```

2. Convert to text:

   ```
   openssl rsa -in key.pem -text -noout > key.txt
   ```

3. Create an asn1 template for the degenerate key called degenerateKey.txt. Simply copy the values for modulus, prime (listed as p in key.txt), prime 2 (listed as q), and coefficient (listed as coeff). Set the public and private key exponents to 1, as well as the values for e1 and e2. See the example below.
4. Convert the template to DER:

   ```
   openssl asn1parse -genconf degenerateKey.txt -out degenerateKey.der
   ```

5. Sanity check the key:

   ```
    openssl rsa -in degenerateKey.der -inform der -text -check
   ```

6. If there are no errors create the degenerate key pem file:

   ```
   openssl rsa -in degenerateKey.der -inform der -outform pem -out degenerateKey.pem
   ```

An example degenerateKey.txt file is shown.

```
asn1=SEQUENCE:rsa_key
[rsa_key]
version=INTEGER:0
modulus=INTEGER<copied from key.txt>
pubExp=INTEGER:1
privExp=INTEGER:1
p=INTEGER:<copied from key.txt>
q=INTEGER<copied from key.txt>
e1=INTEGER:1
e2=INTEGER:1
coeff=INTEGER<copied from key.txt>
```

Note that when copying the multi-byte fields from key.txt it is necessary to remove the colons, catenate the lines and add a preceding 0x.

5.7.5.2 Configuration Script

An example openssl configuration script is shown below. Not all extensions are required, but all possible are shown.

```
[ req ]
distinguished_name = req_distinguished_name
x509_extensions = v3_ca
prompt = no
dirstring_type = nobmp
[ req_distinguished_name ]
C = GB
ST = HI
L = Boston
O = Texas Instruments., Inc.
OU = DSP
CN = Bob
emailAddress = Bob@hou.ti.com
[ v3_ca ]
basicConstraints = CA:true
1.3.6.1.4.1.294.1.1 = ASN1:SEQUENCE:boot_seq
1.3.6.1.4.1.294.1.2 = ASN1:SEQUENCE:image_integrity
1.3.6.1.4.1.294.1.3 = ASN1:SEQUENCE:swrv
1.3.6.1.4.1.294.1.4 = ASN1:SEQUENCE:encryption
1.3.6.1.4.1.294.1.5 = ASN1:SEQUENCE:key_derivation
1.3.6.1.4.1.294.1.7 = ANSI:SEQUENCE:pllControl
1.3.6.1.4.1.294.1.8 = ANSI:SEQUENCE:debug
[ boot_seq ]
certType =INTEGER:1
bootCore = INTEGER:16
bootArchWidth = INTEGER:32
destAddr = FORMAT:HEX,OCT:bc934b00
imageSize = INTEGER:0x00004860
[ image_integrity ]
shaType = OID:1.3.14.3.2.26
shaValue = FORMAT:HEX,OCT:4cf4d59ef77b5d9ab28d2ceb3c9fe83cb52ae6d2
[ swrv ]
rollback = INTEGER:0x00010001
[ encryption ]
Iv =FORMAT:HEX,OCT:00112233445566778899aabbccddeeff
Rstring = FORMAT:HEX,OCT:00112233445566778899aabbccddeeff101112131415161718191a1b1c1d1e1f
Icount = INTEGER:1
Salt = FORMAT:HEX,OCT:00112233445566778899aabbccddeeff
[ pllControl ]
pll0_num = INTEGER:0
pll0_cfg = FORMAT:HEX,OCT:00345678900
pll1_num = INTEGER:1
pll0_cfg = FORMAT:HEX,OCT:00345678900
[ debug ]
uid = FORMAT:HEX,OCT:00345678900
type = INTEGER:1
dbgE = INTEGER:0
secDbgEn = INTEGER:0
```

The certificate is then generated using the following openssl command:

```
openssl req -new -x509 -key <private_key_pem_file> -nodes -out <output_X.509_pem_file> -config
<config_file> -sha512
```

If a delegate key is being signed, then add the option -signkey <sign_key_pem_file> to the command above.

5.7.5.3 Image Data

The image data (blob) is considered simply as a byte stream. On devices that are multiple bytes wide the image must be formatted so that all multi-byte fields match the endianness of the device. The R5 will always run in little endian mode.

5.8 Boot Memory Maps

5.8.1 Memory Layout/MPU

Memory Layout/MPU shows an overview of the MPU configuration. In the R5 MPU, higher numbered regions have priority, therefore in the table, where two regions overlap, the region on the right defines the memory attributes.

5.8.2 Global Memory Addresses Used by ROM Code

The ROM code uses several global memory addresses that are useful for debugging. They are shown in *Global Memory Addresses*.

Table 5-60. Global Memory Addresses

Group	Address	Size (bytes)	Content
SMS0_HSM_SRAM0_0	0x7200 0000	0xF7800	Loadable memory space for SBL
Warning/Error logs	0x720F E480	0x200	Warning Entries
Warning/Error logs	0x720F E680	0x200	Severe Entries
Warning/Error logs	0x720F E880	0x100	Critical Entries
Warning/Error logs	0x720F EB80	0x14	Circular message buffer
Warning/Error logs	0x720F EB94	0x54	Boot log context
Trace	0x720F EBE8	0x18	Boot trace context
Trace	0x720F EC00	0x400	Boot trace entry buffers
Parameter tables	0x720F F290	0x4	Parameter tables index for R5 bootloader
Parameter tables	0x720F F298	0x400	Boot Parameter table for R5 bootloader
Parameter tables	0x720F F1E0	0xB0	Extended boot data for R5 bootloader

Note

Bootloader size in case of Filesystem boot (emmc/sd), is limited to 352KB (512-160). This is due to FAT library memory requirements.

6 Device Configuration

Note

This TRM uses the prefix of "MCU_" for items that refer to the device as a whole instead of a specific domain. "MCU_" is the equivalent of Top Level from Section 1.5.

6.1 Control Module (CTRLMMR)

Note

Some features may not be available. See *Module Integration* for more information.

6.1.1 Memory Mapped Control Register Modules (CTRL_MMR)

This chapter covers three categories of device level control register modules:

- General-Purpose Control Register Modules
- Pad Configuration Register Modules
- Security Control Register Modules

Each category of module is described in its own section, along with detailed register descriptions for each module.

6.1.2 General-Purpose Control Registers Modules

There are three General Purpose Control Register Modules on the Device:

- MAIN_CTRL_MMR0 for the MAIN domain
- WKUP_CTRL_MMR for the WKUP domain
- MCU_CTRL_MMR0 for the Top Level

The following sub-sections provide a summary and description for several of the registers in the General Purpose Control space. The rest of the registers are described in the *Registers* chapter in the *CTRL_MMR Registers* section.

6.1.2.1 Kick Protection Registers

General Purpose Control Register Modules (and also Pad Configuration Register Modules) are organized into different partitions. Partitions can be locked to prevent unintended changes to the register value that might occur due to uncontrolled or malfunctioning software.

Each partition has two registers associated with partition locking - LOCKi_KICK0 and LOCKi_KICK1 registers are used for this purpose. A write is required first to the LOCKi_KICK0[31-1] KEY field and then to the LOCKi_KICK1[31-0] KEY field with exact data values to unlock the protection mechanism. Once released then all registers within Partition "i" having write permissions can be written to. The read only registers are still read only. An indication for unlocked Partition "i" is when the LOCKi_KICK0[0] UNLOCKED bit is set to 1h. When the protection mechanism is locked (indicated by LOCKi_KICK0[0] UNLOCKED = 0h) none of the registers within Partition "i" can be written to. They can only be read.

The key values for all partitions are:

- LOCKi_KICK0 Key: 68EF 3490h
- LOCKi_KICK1 Key: D172 BC5Ah

Writing any other data value to either of these registers locks the protection mechanism and blocks any writes to the registers that reside in Partition "i".

6.1.2.2 I/O Debounce Control Registers

Some device pads have debounce logic. The following MCU_CTRL_MMR0 registers are used to configure the debounce period:

- MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1
- MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2
- MCU_CTRL_MMR_CFG0_DBOUNCE_CFG3
- MCU_CTRL_MMR_CFG0_DBOUNCE_CFG4
- MCU_CTRL_MMR_CFG0_DBOUNCE_CFG5
- MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6

The MCU_CTRL_MMR_CFG0_DBOUNCE_CFG1 register contains the debounce period for pads with PADCONFIGx[13-11] DEBOUNCE_SEL fields set to 1h. The MCU_CTRL_MMR_CFG0_DBOUNCE_CFG2 register contains the debounce period for pads with PADCONFIGx[13-11] DEBOUNCE_SEL fields set to 2h and so on. The MCU_CTRL_MMR_CFG0_DBOUNCE_CFG6 register contains the debounce period for pads with PADCONFIGx[13-11] DEBOUNCE_SEL fields set to 6h.

Note

The debounce logic is not associated with all signals that can be multiplexed on a pad. Only certain signals can use it.

For information about each signal that has associated debounce logic, see the device Datasheet.

For information about the PADCONFIGx registers, see *Pad Configuration PADCONFIG Registers*.

Debounce Period Values shows the debounce period values to load in the MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5-0] DB_CFG field.

Note

The debounce clock selection should happen before the consumer of the debounced signals is enabled as the clock multiplexers for the debounce logic are NOT glitch-free.

Table 6-1. Debounce Period Values

MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5-0] DB_CFG Decimal Value	GPIO Case (32.768kHz(1))	EQEP Case (20MHz(1))	MCU_CTRL_MMR_CFG0_DBOUNCE_CFGx[5-0] DB_CFG Decimal Value	GPIO Case (20MHz(1))	EQEP Case (250MHz(1))
	Delay[ms]	**Delay[μs]**		**Delay[μs]**	**Delay[ns]**
0	bypassed	bypassed	32	0.05	4
1	1.95	3.20	33	0.10	8
2	2.93	4.80	34	0.15	12
3	3.91	6.40	35	0.20	16
4	4.88	8.00	36	0.25	20
5	5.86	9.60	37	0.30	24
6	6.84	11.20	38	0.35	28
7	7.81	12.80	39	0.40	32
8	8.79	14.40	40	0.45	36
9	9.77	16.00	41	0.50	40
10	10.74	17.60	42	0.55	44
11	11.72	19.20	43	0.60	48
12	12.7	20.80	44	0.65	52
13	13.67	22.40	45	0.70	56
14	14.65	24.00	46	0.75	60
15	15.63	25.60	47	0.80	64
16	16.6	27.20	48	0.85	68
17	17.58	28.80	49	0.90	72
18	18.55	30.40	50	0.95	76
19	19.53	32.00	51	1.00	80
20	20.51	33.60	52	1.05	84
21	21.48	35.20	53	1.10	88
	Delay[ms]	**Delay[μs]**		**Delay[μs]**	**Delay[μs]**
22	15.63	25.60	54	25.60	2.048
23	31.25	51.20	55	51.20	4.096
24	46.88	76.80	56	76.80	6.144
25	62.5	102.40	57	102.40	8.192
26	78.13	128.00	58	128.00	10.24
27	93.75	153.60	59	153.60	12.288
28	109.38	179.20	60	179.20	14.336
29	125	204.80	61	204.80	16.384
30	140.63	230.40	62	230.40	18.432
31	156.25	256.00	63	256.00	20.48

(1) These are the debounce logic clock frequencies.

6.1.3 Pad Configuration Resister Modules

There are three Pad Configuration related General Purpose Control Register Modules on the device:

- PADCFG_CTRL for MAIN domain
- MCU_PADCFG_CTRL for the Top Level and WKUP domains

6.1.4 Security Control Register Modules

The following sections describe the CTRL_MMR0 and PADCFG_CTRL0_CFG0 modules.

6.1.4.1 Security Control Register Modules Overview

There are three Security Control Register Modules on the Device:

- MAIN_SEC_MMR0 for the MAIN domain
- WKUP_SEC_MMR0 for the WKUP domain

6.2 Power

This chapter describes the power-management architecture implemented in the device.

6.2.1 Power Management Overview

To provide a versatile architecture that supports multiple power-management techniques, the power management framework is built with three levels of resource management: clock, power, and voltage.

These management levels are enforced by defining the managed entities or building blocks of the power management architecture, called the clock, power, and voltage domains. A domain is a group of modules or subsections of the device that share a common entity (for example, common clock source, common voltage source, or common power switch).

To minimize device power consumption, the clocks can be gated (turned off), or the power to the modules can be switched off, when they are not in use. Independent power and clock control of sections of the device allows for turning on and off specific sections of the device without affecting other sections.

6.2.2 Power Control Modules

The Power Control Modules are divided into two sections, dependent on their functionality - Power Sleep Controller section and Device Manager section.

6.2.2.1 Power Sleep Controller

6.2.2.1.1 PSC Architecture

Power Sleep Controller (PSC) is a control component to manage the power domain and module’s clock and reset transition. Each PSC module contains multiple power domains, within each power domain, it can contain multiple LPSC. Each LPSC can be used to manage the one or multiple module’s reset and clock stop status, see *PSC Architecture*.

Each power domain has a unique index, starting from number 0. The power domain 0 is a special power domain, which is always on. The status of power domain 0 can’t be changed after the device is out of reset.

Each power domain can have one or more Local Power Sleep Control (LPSC). Each LPSC in the same PSC has a unique index value as well. LPSC 0 is special, which user can’t change its status. LPSC 0 is always set to be enabled after the device is out of reset.

One LPSC can be used to control the reset and clock status for one or more modules. Some of the LPSC can be used to provide local reset function for the processors. LPSC can also be used to manage the clock stop interface for the interfaces between two interconnect IPs. This is mainly used for providing isolation features required by some special features such as security isolation, functional safety isolation or reset isolation between different parts of the SoC.

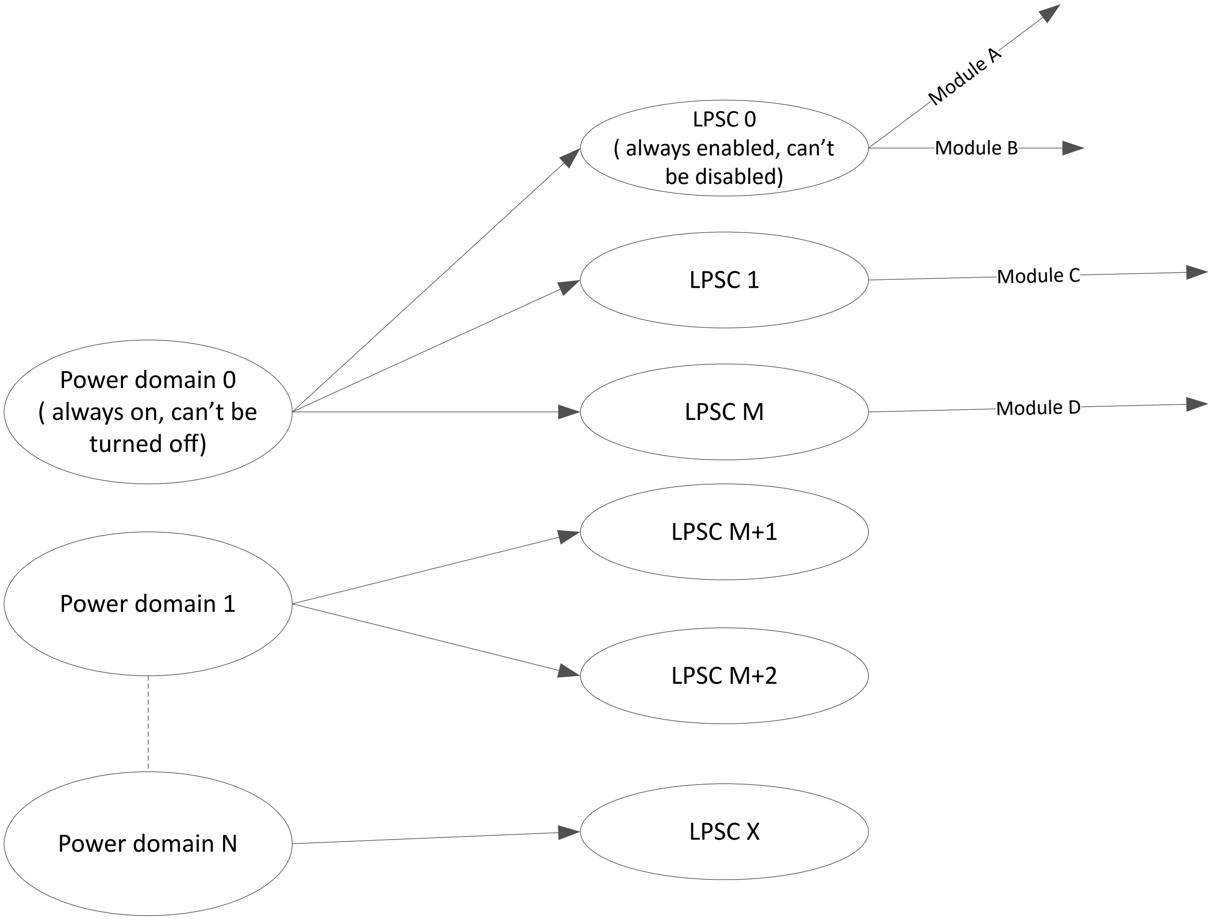


Figure 6-1. PSC Architecture

Note

PSC functions are controlled via Device Manager. For more information how to use Device Manager, see TISCI API available at ti.com.

6.2.2.2 LPSC Features

Table 6-2. LPSC Feature

PSC	Power Domain	LPSC Name	LPSC Index	Default State	Software	Modules
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_ALWAYSON	0	ON	NO	MCU_CTRL_MMR0
WKUP_PSC0	GP_CORE_CTL_MCU					MCU_MCU_GPIO_INTROUTER0
WKUP_PSC0	GP_CORE_CTL_MCU					MCU_PADCFG_CTRL0
WKUP_PSC0	GP_CORE_CTL_MCU					WKUP_PLL0
WKUP_PSC0	GP_CORE_CTL_MCU					MCU_DCC0
WKUP_PSC0	GP_CORE_CTL_MCU					MCU_DCC1
WKUP_PSC0	GP_CORE_CTL_MCU					WKUP_ESM0
WKUP_PSC0	GP_CORE_CTL_MCU					MCU_GPIO0
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_DM2SAFE_ISO	3	ON	YES	
WKUP_PSC0	GP_CORE_CTL_MCU	LPSC_MCU_TEST	5	ON	YES	
WKUP_PSC0	PD_MCUSS	LPSC_MCU_COMMON	9	ON	YES	WKUP_PSRAM2KX32E0
WKUP_PSC0	PD_MCUSS	LPSC_MCU_PBIST	10	OFF	YES	WKUP_PBIST1

Table 6-2. LPSC Feature (continued)

PSC	Power Domain	LPSC Name	LPSC Index	Default State	Software	Modules
MAIN_PSC0	GP_CORE	LPSC_MAIN_ALWAYSON	0	ON	NO	MAIN_CTRL_MMR0
MAIN_PSC0	GP_CORE					MAIN_GPIO_INTROUTER0
MAIN_PSC0	GP_CORE					PADCFG_CTRL0
MAIN_PSC0	GP_CORE					PLL0
MAIN_PSC0	GP_CORE					TIMESYNC_INTROUTER0
MAIN_PSC0	GP_CORE					WKUP_CTRL_MMR0
MAIN_PSC0	GP_CORE					WKUP_WKUP_SEC_MMR0
MAIN_PSC0	GP_CORE					CPT2_AGGR1
MAIN_PSC0	GP_CORE					DCC0
MAIN_PSC0	GP_CORE					DCC1
MAIN_PSC0	GP_CORE					DCC2
MAIN_PSC0	GP_CORE					DCC3
MAIN_PSC0	GP_CORE					DCC4
MAIN_PSC0	GP_CORE					DCC5
MAIN_PSC0	GP_CORE					DCC6
MAIN_PSC0	GP_CORE					DCC7
MAIN_PSC0	GP_CORE					DCC8
MAIN_PSC0	GP_CORE					WKUP_TIMER0
MAIN_PSC0	GP_CORE					WKUP_TIMER1
MAIN_PSC0	GP_CORE					ESM0
MAIN_PSC0	GP_CORE					GPIO0
MAIN_PSC0	GP_CORE					GPIO1
MAIN_PSC0	GP_CORE					WKUP_GTC0
MAIN_PSC0	GP_CORE					DDPA0
MAIN_PSC0	GP_CORE					WKUP_VTM0
MAIN_PSC0	GP_CORE					WKUP_I2C0
MAIN_PSC0	GP_CORE					PSRAMECC0
MAIN_PSC0	GP_CORE					WKUP_PSRAMECC_8K0
MAIN_PSC0	GP_CORE					WKUP_ROM0
MAIN_PSC0	GP_CORE					WKUP_RTCSS0
MAIN_PSC0	GP_CORE					EFUSE0
MAIN_PSC0	GP_CORE	LPSC_MAIN_DM	1	OFF	YES	WKUP_R5FSS0
MAIN_PSC0	GP_CORE					WKUP_RTI0
MAIN_PSC0	GP_CORE	LPSC_MAIN_DM_PBIST0	2	ON	YES	WKUP_PBIST0
MAIN_PSC0	GP_CORE	LPSC_MAIN_MAIN2DM_ISO	3	ON	YES	
MAIN_PSC0	GP_CORE	LPSC_MAIN_DM2MAIN_ISO	4	ON	YES	
MAIN_PSC0	GP_CORE	LPSC_MAIN_DM2MAIN_INFRA_ISO	5	ON	YES	
MAIN_PSC0	GP_CORE	LPSC_MAIN_DM2CENTRAL_ISO	6	ON	YES	

Table 6-2. LPSC Feature (continued)

PSC	Power Domain	LPSC Name	LPSC Index	Default State	Software	Modules
MAIN_PSC0	GP_CORE	LPSC_MAIN_CENTRAL2DM_ISO	7	ON	YES	
MAIN_PSC0	GP_CORE	LPSC_MAIN_DM_PBIST1	8	ON	YES	
MAIN_PSC0	GP_CORE	LPSC_MAIN_TEST	9	ON	YES	DFTSS0
MAIN_PSC0	GP_CORE	LPSC_MAIN_DEBUGSS	10	ON	YES	DBG_INTROUTER0
MAIN_PSC0	GP_CORE					STM0
MAIN_PSC0	GP_CORE					DEBUGSS_WRAP0
MAIN_PSC0	GP_CORE					DEBUGSS0
MAIN_PSC0	GP_CORE	LPSC_MAIN_PBIST0	11	OFF	YES	PBIST0
MAIN_PSC0	GP_CORE	LPSC_MAIN_USB0	12	OFF	YES	USB0
MAIN_PSC0	GP_CORE	LPSC_MAIN_USB0_ISO	13	OFF	YES	
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	PDMA_AASRC0_6
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	PDMA_AASRC1_7
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	PDMA5
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	PDMA3
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	CPT2_AGGR0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	CPT2_AGGR2
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER1
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER10
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER11
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER12
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER13
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER14
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER15
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER2
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER3
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER4
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER5
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER6
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER7
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER8
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	TIMER9
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	ECAP0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	ECAP1
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	ECAP2
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	ECAP3
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	ECAP4
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	ECAP5
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	EPWM0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	EPWM1

Table 6-2. LPSC Feature (continued)

PSC	Power Domain	LPSC Name	LPSC Index	Default State	Software	Modules
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	EPWM2
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	MCRC64_0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	I2C0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	I2C1
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	I2C2
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	I2C3
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	I2C4
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	I2C5
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	I2C6
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	PDMA2
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	MCSPI0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	MCSPI1
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	MCSPI2
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	MCSPI3
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	MCSPI4
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	UART0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	UART1
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	UART2
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	UART3
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	UART4
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	UART5
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	UART6
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP0	18	ON	YES	WKUP_UART0
MAIN_PSC0	GP_CORE	LPSC_MAIN_IP1_RSVD	19	OFF	YES	PDMA4
MAIN_PSC0	GP_CORE					DMASS0
MAIN_PSC0	GP_CORE					PDMA1
MAIN_PSC0	GP_CORE					PDMA0
MAIN_PSC0	GP_CORE	LPSC_MAIN_EMMC8B	20	OFF	YES	MMCSD0
MAIN_PSC0	GP_CORE	LPSC_MAIN_CPSW	21	OFF	YES	CPSW0
MAIN_PSC0	GP_CORE	LPSC_MAIN_OSPI2_RSVD	22	OFF	YES	
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN0	23	OFF	YES	MCAN0
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN1	24	OFF	YES	MCAN1
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN2	25	OFF	YES	MCAN2
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN3	26	OFF	YES	MCAN3
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCAN4	27	OFF	YES	MCAN4
MAIN_PSC0	GP_CORE	LPSC_MAIN_OSPI0	28	ON	YES	FSS_OF_UL0
MAIN_PSC0	GP_CORE	LPSC_MAIN_OPSI1	29	ON	YES	FSS0_FSAS_0
MAIN_PSC0	GP_CORE					FSS0_HYPERBUS1P0_0
MAIN_PSC0	GP_CORE					FSS0_OSPI_0
MAIN_PSC0	GP_CORE					FSS0_OSPI_1

Table 6-2. LPSC Feature (continued)

PSC	Power Domain	LPSC Name	LPSC Index	Default State	Software	Modules
MAIN_PSC0	GP_CORE	LPSC_MAIN_HYPERBUS	30	ON	YES	FSS0_HYPERBUS1P0_0
MAIN_PSC0	GP_CORE	LPSC_MAIN_SA3UL	31	ON	YES	SA3_SS0
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCASP0	32	OFF	YES	MCASP0
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCASP1	33	OFF	YES	MCASP1
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCASP2	34	OFF	YES	MCASP2
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCASP3	35	OFF	YES	MCASP3
MAIN_PSC0	GP_CORE	LPSC_MAIN_MCASP4	36	OFF	YES	MCASP4
MAIN_PSC0	GP_CORE	LPSC_MAIN_ATL	37	OFF	YES	ATL0
MAIN_PSC0	GP_CORE	LPSC_MAIN_ASRC0	38	OFF	YES	AASRC0
MAIN_PSC0	GP_CORE	LPSC_MAIN_ASRC1	39	OFF	YES	AASRC1
MAIN_PSC0	GP_CORE	LPSC_MAIN_MLB	40	OFF	YES	MLB0
MAIN_PSC0	GP_CORE	LPSC_MAIN_ADC	41	OFF	YES	ADC12FC_16FFC0
MAIN_PSC0	MAIN_SRAM0	LPSC_MAIN_SRAM_0_1	43	ON	YES	MSRAM_1MB0
MAIN_PSC0	MAIN_SRAM0					MSRAM_1MB1
MAIN_PSC0	MAIN_SRAM0	LPSC_MAIN_SRAM_PBIST0	44	OFF	YES	PBIST3
MAIN_PSC0	MAIN_SRAM0	LPSC_MAIN_SRAM_PBIST1	45	OFF	YES	PBIST4
MAIN_PSC0	MAIN_SRAM1	LPSC_MAIN_SRAM_2_3	46	ON	YES	MSRAM_1MB2
MAIN_PSC0	MAIN_SRAM1					MSRAM_1MB3
MAIN_PSC0	MAIN_SRAM1	LPSC_MAIN_SRAM_PBIST2	47	OFF	YES	PBIST5
MAIN_PSC0	MAIN_SRAM1	LPSC_MAIN_SRAM_PBIST3	48	OFF	YES	PBIST6
MAIN_PSC0	MAIN_SRAM2	LPSC_MAIN_SRAM_4_5	49	ON	YES	MSRAM_1MB4
MAIN_PSC0	MAIN_SRAM2					MSRAM_1MB5
MAIN_PSC0	MAIN_SRAM2	LPSC_MAIN_SRAM_PBIST4	50	OFF	YES	PBIST7
MAIN_PSC0	MAIN_SRAM2	LPSC_MAIN_SRAM_PBIST5	51	OFF	YES	PBIST8
MAIN_PSC0	R5SS_0	LPSC_MAIN_R5SS0_CORE0	52	OFF	YES	R5FSS0_CORE0
MAIN_PSC0	R5SS_0					RL2_OF_CBA4_0
MAIN_PSC0	R5SS_0					RTI0
MAIN_PSC0	R5SS_0	LPSC_MAIN_R5SS0_CORE1	53	OFF	YES	R5FSS0_CORE1
MAIN_PSC0	R5SS_0					RL2_OF_CBA4_1
MAIN_PSC0	R5SS_0					RTI1
MAIN_PSC0	R5SS_0	LPSC_MAIN_R5SS0_PBIST	54	OFF	YES	PBIST1
MAIN_PSC0	R5SS_1	LPSC_MAIN_R5SS1_CORE0	55	OFF	YES	R5FSS1_CORE0
MAIN_PSC0	R5SS_1					RL2_OF_CBA4_2
MAIN_PSC0	R5SS_1					RTI2

Table 6-2. LPSC Feature (continued)

PSC	Power Domain	LPSC Name	LPSC Index	Default State	Software	Modules
MAIN_PSC0	R5SS_1	LPSC_MAIN_R5SS1_CORE1	56	OFF	YES	R5FSS1_CORE1
MAIN_PSC0	R5SS_1					RL2_OF_CBA4_3
MAIN_PSC0	R5SS_1					RTI3
MAIN_PSC0	R5SS_1	LPSC_MAIN_R5SS1_PBIST	57	OFF	YES	PBIST2
MAIN_PSC0	C7X0	LPSC_MAIN_C7X0_COMMON	58	OFF	YES	C7X256V0_CORE0
MAIN_PSC0	C7X0	LPSC_MAIN_C7X0_CORE	59	OFF	YES	C7X256V_0_0_C7XV_CORE_0
MAIN_PSC0	C7X0					RTI4
MAIN_PSC0	C7X0	LPSC_MAIN_C7X0_PBIST	60	OFF	YES	C7X256V0_PBIST
MAIN_PSC0	C7X1	LPSC_MAIN_C7X1_COMMON	61	OFF	YES	C7X256V1_CORE0
MAIN_PSC0	C7X1	LPSC_MAIN_C7X1_CORE	62	OFF	YES	C7X256V_1_1_C7XV_CORE_0
MAIN_PSC0	C7X1					RTI5
MAIN_PSC0	C7X1	LPSC_MAIN_C7X1_PBIST	63	OFF	YES	C7X256V1_PBIST

6.2.2.3 Software Sequence to enable an IP through PSC

In order to enable a module, user needs to program the PSC to put LPSC into enable state. There is dependence between power domain and LPSC and among different LPSC controls.

First of all, in order to enable any LPSC, the power domain which that LPSC belongs needs to be enabled first. The LPSC can't put into any state other than disable if the power domain is not enabled.

Among different LPSC, there is also a special sequence needs to be followed to make sure the device is not getting into undefined state.

Similarly, a special sequence shall be followed to disable the LPSC to prevent device getting into undefined states. Before a power domain can be turned off, all the LPSCs within that power domain shall be disabled first. Normally, user can turn off the power domain to save power. However, it is not necessary to turn off the power domain when all the LPSCs inside that power domain are disabled.

Figure 6-2 shows how to understand the dependent relationship between two LPSCs. In order to enable LPSC_2, LPSC_1 shall be enabled first.

If user wants to disable LPSC_1, LPSC_2 shall be disabled first.

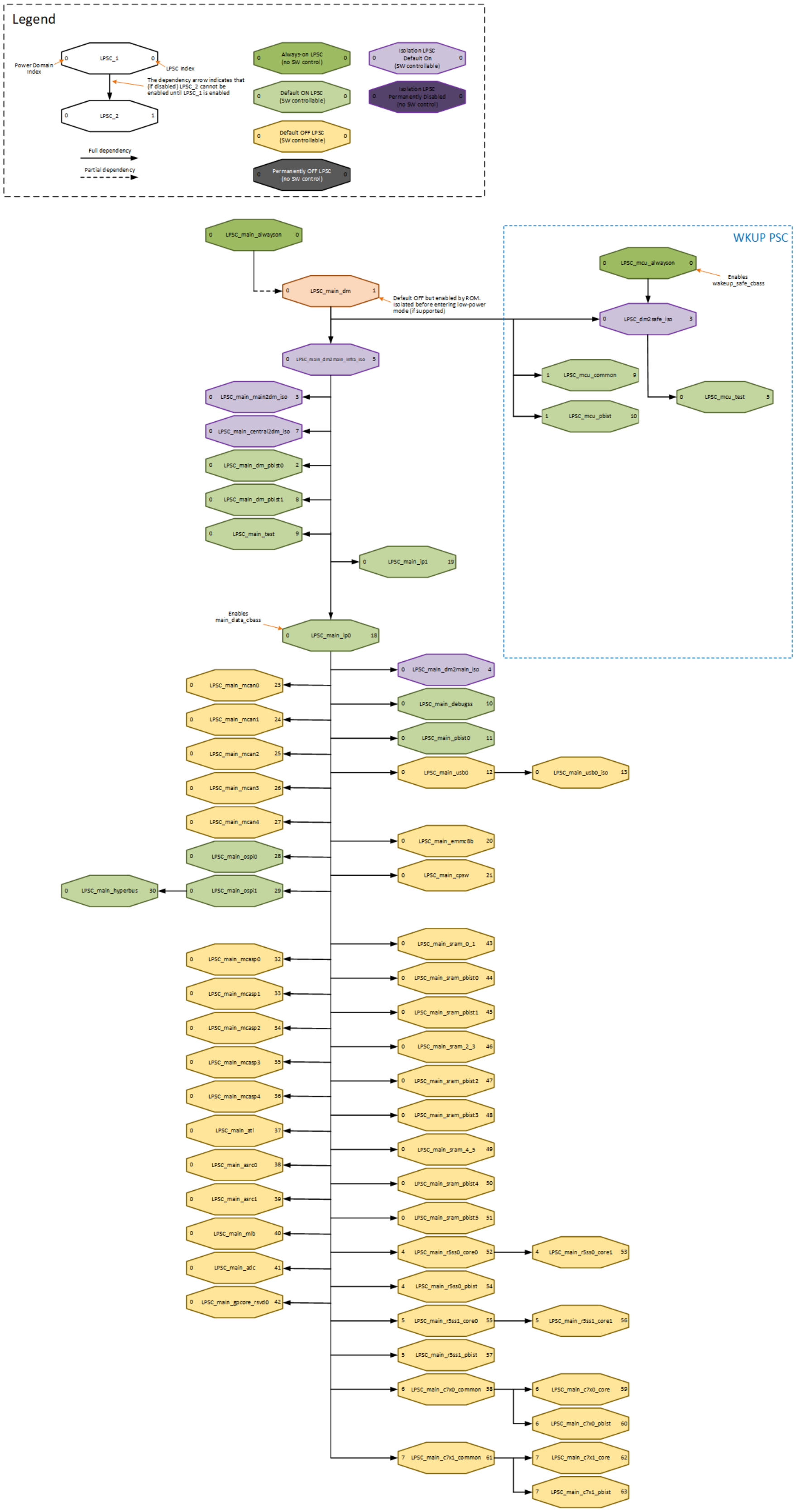


Figure 6-2. LPSC Dependence

6.2.2.4 Device Manager

The device has one Device Manager located in WKUP domain. Device Manager is responsible for entry/exit to low power modes. Also, Device Manager hosts RM/PM (Resource Manager/Power Manager) SYSFW code for providing RM/PM services to HLOS. As part of boot, public ROM is executed over Device Manager.

Device Manager Features

- Single Core Cortex-R5 subsystem
  - ARMv7-R architecture with following extensions
    - Advanced SIMD extension for integer and floating-point vector operations
    - Vector Floating Point Version 3 (VFPv3)
  - L1 memory architecture
    - 32KB I-cache with 64-bit ECC error checking
    - 32KB D-cache with 64-bit ECC error checking
  - 64Kbyte TCM(L2) with 32-bit ECC error checking
  - 32-bit AXI3 initiator interface for accessing local peripherals
- 1x RTI/WWDT
- 2x Timer
- 1x UART
- 1x I2C
- Wake-up logic
- Public ROM
- RTC digital
- VTM
- LFOSC

Note

PSC functions are controlled via Device Manager. For more information how to use Device Manager, see TISCI API available at ti.com.

6.2.3 Power Modes

The following sections describe different power modes of the device. Specific values are detailed in the device-specific data sheet. Note that not all modes are supported by software packages supplied by Texas Instruments.

Table 6-3. Low Power Modes

Low Power Modes	Wakeup Sources	Application State and Use Case
IORET	External IO activities	The entire SoC is OFF except I/O pins in CANUART I/O Bank to maintain I/O wakeup capability. Contents in a bank of SRAM (RAM Retention) is preserved during this low power mode.
Standby	Any SoC interrupt event	On-chip contents are fully preserved. Any SoC interrupt event can cause a wakeup event from this low power mode. Cores are in WFI The device can run low-level processing with non-Wakeup domain peripherals and support wakeup from those peripherals.

6.2.3.1 Active

In Active mode, the supply to all voltage rails must be maintained. All power domains come up in ON state and the device is fully functional.

6.2.3.2 Standby

The device can be placed in Standby mode to reduce power consumption during low activity levels. This first level of power management allows you to maintain the device context for fast resume times. The main characteristics of this mode that distinguish it from Active mode are:

- All modules are clock gated except GPIOs
- PLLs may be placed in bypass mode if downstream clocking does not require full performance

- The VDD_CORE voltage level is maintained.
- Power domain may be turned off if it's not used for the contexts can be saved and restored.

The above conditions result in lower power consumption than Active mode but require the user to save the switched-off power domain context to On-Chip Memory and restore the contexts to resume properly upon wakeup.

Wakeup in Standby mode is achieved using any GPIO. GPIO wakeup is possible by switching the pad to GPIO mode and configuring the corresponding GPIO bank for generating an interrupt to the Device Manager. Note that pads that do not have a GPIO muxmode (for example, USB) cannot cause these wakeups. If additional or other wakeup sources are required, the associated peripheral module clock and interconnect clock domain should remain enabled (this may require the associated PLL to remain locked) and the module must be configured appropriately for wakeup by configuring it to generate an interrupt to the Device Manager.

6.2.3.3 IO Retention Mode

IO Retention (IORET) is the lowest system state where the device can be waken up external IO activities. The main characteristics of this mode are:

- Main OSC and DPLLs are powered off
- All power domains are off
- All IO supplies are off except for:
  - VDD_CANUART
  - VDDR_CANUART
  - VDDSHV_CANUART
- RAM Retention (8KB)

VDD_CANUART and VDDR_CANUART can be tied to the same supply when using OPP_HIGH. The two supplies should be kept on during IORET.

6.2.3.4 Power States and Transitions

The Low power mode transition always starts from the active state. If the device needs to transition from one low power mode to another low power mode, the device must go through the active state first. Typically, the software initiates a transition from active mode to a low power mode and a wakeup event triggers a transition from a low power mode to active.

Power States Transition Diagram shows the power state transition supported by the device.

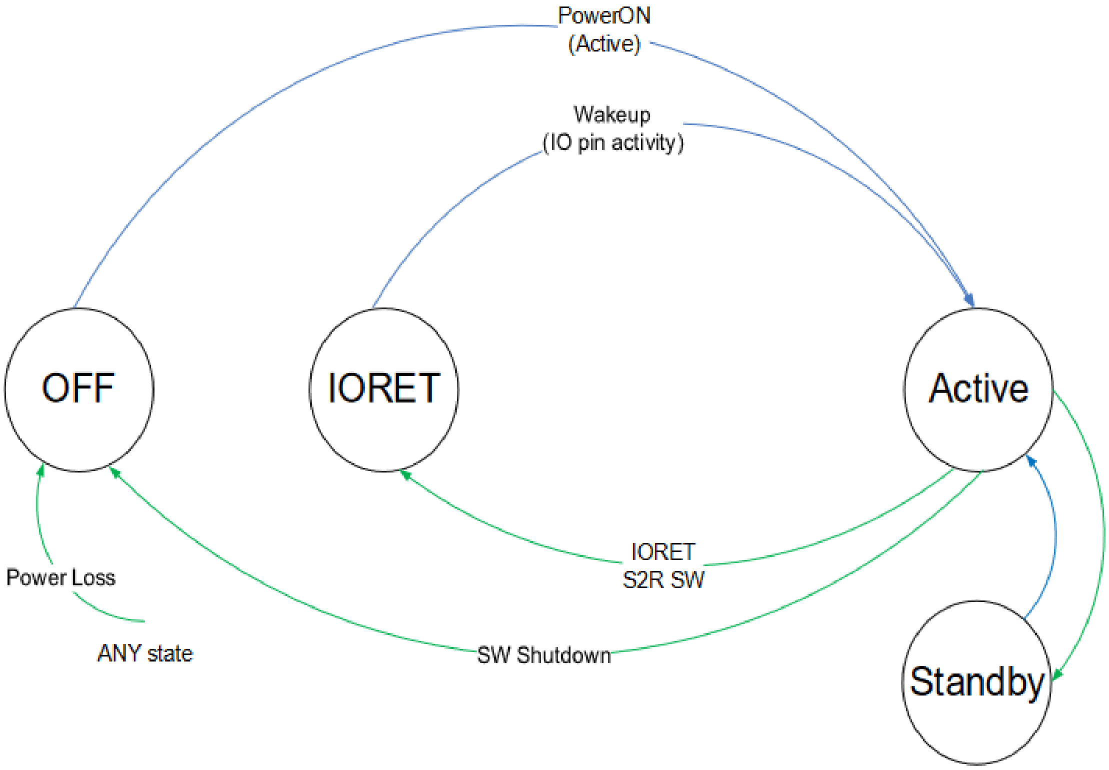


Figure 6-3. Power States Transition Diagram

6.2.3.5 Wakeup Sources/Events

Low Power Mode Wakeup Events shows the wake sources supported in each low power mode. .

Table 6-4. Low Power Mode Wakeup Events

Low Power Modes	Wakeup Events
IORET	External IO activities including CAN RX, UART, GPIO signals
Standby	Any SoC interrupt event

6.2.3.6 IORET Sequencing with Device Manager

The device contains a Device Manager (DM) to handle all of the low-level power management control of the device including the Low Power Mode transitions. A firmware is provided by Texas Instruments that includes all of the necessary functions to achieve low power modes. Inter-processor Communication (IPC) registers are available to communicate with the Device Manager so the user can provide certain configuration parameters based on the level of low power that is required.

1. By default PMIC_LPM_EN must be pulled HIGH externally to power-up SoC (when used as PMIC ENABLE control). As soon as supplies are ON, the device drives HIGH on this signal.
2. Device powers up with CANUART IO Daisy Chain mode disabled. CAN_ONLY_IO status (CANUART_WAKE_STAT*) will read '0' indicating that CANUART IO Daisy chain mode is not enabled. All PORx and HHV signals propage without any gating
3. After MCU_PORz goes High, device boots-up as per BOOT Config pin setup
4. DM SBL reads, CAN_ONLY_IO status to determine if the CAN ONLY IO daisy chain is enabled. Since this is the first boot-up, this status bit reads '0'.
5. DM completes boot-up and configures device as per SBL code
6. Device enters steady state operation
7. At this point, if the application needs to enter CANUART IO mode, application first write the desired retention data to the Retention ROM, upon completion, the corresponding core shall perform a full cache writeback data, and perform a CPU fencing to the physical memory. Application shall ensure no other cores accessing

the retention RAM. Then, DM kicks-off the IO daisy chain sequence to put the CANUART IOs in retention state. DM programs PADCFG MMRs to put IO in desired state (IO direction, IO level, Pulls), WUEN for wakup and writes into the WKUP MMR to set the global_wu_en bits. DM then writes to asserts ISOIN[0] control to a High.

8. DM the programs CAN ONLY IO DAISY CHAIN WORD also known as Magic Word (CANUART_WAKE_OFF_MODE) . DM toggles the Load Enable bit High and Low (steps below). This latches the Magic Word in VDD_CAN domain. At this point, CAN_ONLY_IO signal (CANUART_WAKE_CTRL) must read as a '1'
    a. DM writes to CANUART_WAKE_STAT0 with Magic Word and CANUART_WAKE_CTRL_mw_load_en with 1
    b. DM polls to CANUART_WAKE_STAT1 for IORET mode to be set. This insures spacing for the async interface to write the correct Magic Word value
    c. DM writes to CANUART_WAKE_STAT0 with the !(Magic Word) and CANUART_WAKE_CTRL_mw_load_en with 0
9. Once CAN_ONLY_IO is HIGH, it latches the ISOIN[0] control signal in the VDDU domain blocks and forces the porz and hhvz signals HIGH (inactive state).
10. At the point the device is ready to support CAN Only IO mode
11. DM writes into the pmic_en bit to '0'. This de-assers PMIC_LPM_EN from a High to a Low. PMIC detects this High to Low transition will power off SoC supplies. Note that VDDSHV_CAN and VDDU_CAN are still powered on.
12. Now device should be in the lowers power mode with just the CANUART IOs in Daisy chain mode.
13. Any event on these pins will cause an wakeup event out of CANUART IO daisy chain. This wakeup event forces the PMIC_LPM_EN to go HIGH. (PMCTRL_SYS register)
14. PMIC detects this Low to High transition on PMIC_LPM_EN signal and powers up SoC supply rails.
15. Device boots-up as defined in steps 3 to 5. DM SBL pills CAN_ONLY_IO status MMR to determine if the IORET mode was enabled. In addition, it can also compare the CAN ONLY IO WORD LATCHED to expected value to confirm the validity of CAN IO Voltages while the device was in IORET mode.
16. DM reads the WKUP PADCFG bits to determine which pin caused the wake-up event
17. DM writes in the Magic Word to disable IORET mode. DM then removes the ISO mode on the IOs, so they can go into normal mode of operation. This clears the IO buffer latches to reset state
18. Device enters steady state operation

Note

Low Power Mode sequencing is controlled via Device Manager. For more information how to use Device Manager, see TISCI API available at ti.com.

6.2.4 Power Supply Modules

6.2.4.1 Power OK (POK) Modules

Note

In this family of devices, the Power-on-reset module is used only for voltage monitoring, as three additional POK modules. For more information about POK functionality in POR module - voltage being monitored and type (under voltage or over voltage), see Section 6.2.4.2.

POK modules are responsible for accurately detecting the voltage levels. Each module is trimmed to account for process and temperature variations. The trim values are provided by eFuse chains enabled by a POR/Reset Generator (PRG) module.

Two types of POK modules are implemented in this family of devices - POK and POK_SA. See Table 6-5 about the type of a POK and the voltage it is monitoring. More information about the two types of POKs is given further in this section.

Table 6-5. POK Module Overview

POK Module Instance Name	PRG Index (3)	POK Index (1)	Voltage Monitored	Module Type	OV/ UV(2)	Description
IPOK_VDD_CORE_OV	PRG0	4	VDD_CORE	POK_CORE	OV	Voltage Monitor for VDD_CORE
IPOK_VDDA_PMIC_IN_UV	PRG0	3	VMON_ER_VSYS	POK_SA	UV	Voltage Monitor for PMIC_IN
IPOK_VDDR_CORE	PRG1	3	VDDR_CORE	POK_CORE	UV/OV	Voltage Monitors for VDDR_CORE
IPOK_VMON_CAP_MCU_GENERAL	PRG1	2	CAP_VDDS_MCU	POK_CORE	UV/OV	Voltage Monitors for MCU mid-rail
IPOK_VDDSHSV_MAIN_1P8	PRG1	1	VMON_1P8_SOC	POK_1P8	UV/OV	Voltage Monitors for 1.8-V I/O supply in MCU
IPOK_VDDSHSV_MAIN_3P3	PRG1	0	VMON_3P3_SOC	POK_3P3	UV/OV	Voltage Monitors for 3.3-V I/O supply in MCU

(1) The POK Index also represents the mapping index for relevant under and overvoltage status and interrupts where applicable.
(2) UV: POK is set for undervoltage detection. OV: POK is set for overvoltage detection. UV/OV: POK monitors both OV and UV through a Ping-Pong mechanism.
(3) Ping-pong mechanism is only applicable to PRG1.

Figure 6-4 and Figure 6-5 represent the block diagrams of the two POK types.

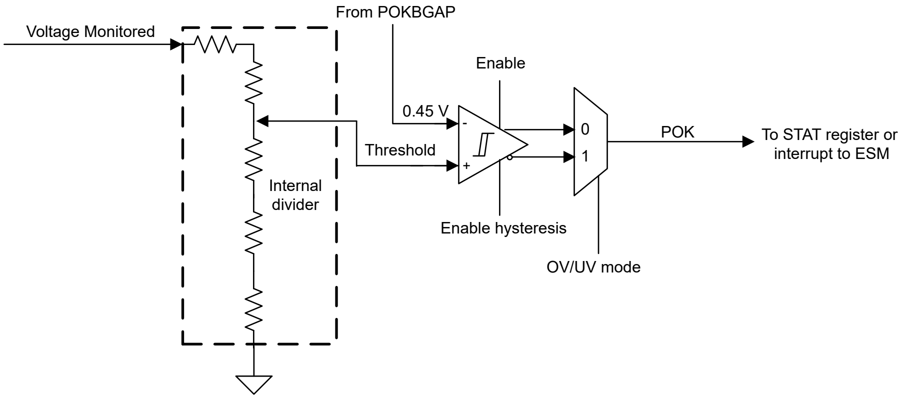


Figure 6-4. POK Block Diagram

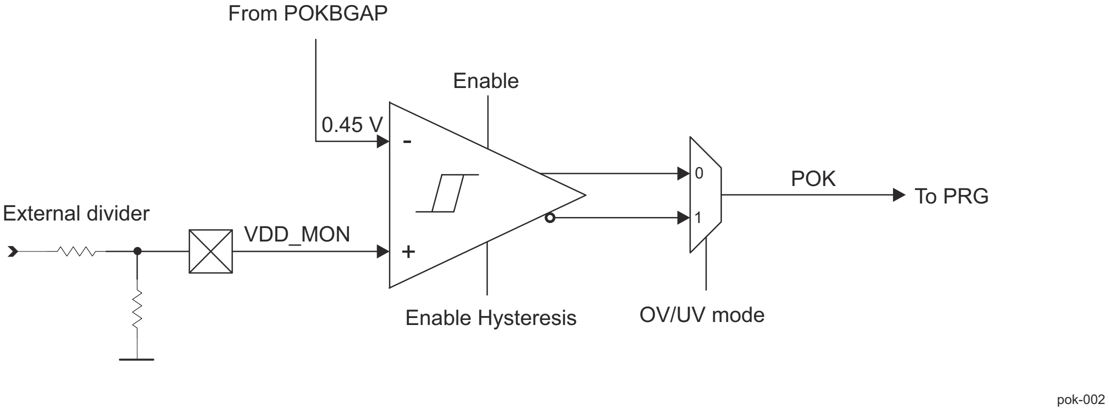


Figure 6-5. POK_SA Block Diagram

Vref for both POK and POK_SA types in Figure 6-4 and Figure 6-5 is supplied from POK module, see Section 6.2.4.2

6.2.4.1.1 Configuration Registers

Configuration registers needed for POK (Supervisor Module) are given in Table 6-6. For each POK there is one comparator that is controlled through the registers. These registers decide the functionality of the POK Comparator. It decides if it is UV/OV mode and also the threshold voltages.

Comparator threshold levels and corresponding configuration register settings are given in the following tables:

- POK_CORE: Table 6-7
- POK_1P8: Table 6-8
- POK_3P3: Table 6-9

Table 6-6. POK Configuration Registers

Register Name	POK Type
MCU_CTRL_MMR0_POK_VDD_CORE_OV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR0_POK_VDDR_CORE_UV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR0_POK_VDDR_CORE_OV_CTRL[7:0]	POK_CORE
MCU_CTRL_MMR0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR0_POK_VDDSHV_MAIN_1P8_UV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR0_POK_VDDSHV_MAIN_1P8_OV_CTRL[7:0]	POK_1P8
MCU_CTRL_MMR0_POK_VDDSHV_MAIN_3P3_UV_CTRL[7:0]	POK_3P3
MCU_CTRL_MMR0_POK_VDDSHV_MAIN_3P3_OV_CTRL[7:0]	POK_3P3

Table 6-7. Bit Settings of POK_CORE with VMON Threshold Values

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Under Voltage Detection) hys_en=0	0	000 0000	0.4743
	0	000 0001	0.4875
	0	000 0010	0.5000
	0	000 0011	0.5125
	0	000 0100	0.5250
	0	000 0101	0.5375
	0	000 0110	0.5513
	0	000 0111	0.5631
	0	000 1000	0.5754
	0	000 1001	0.5883
	0	000 1010	0.6017
	0	000 1011	0.6122
	0	000 1100	0.6268
	0	000 1101	0.6382
	0	000 1110	0.6500
	0	000 1111	0.6623
	0	001 0000	0.6750
	0	001 0001	0.6882
	0	001 0010	0.7020
	0	001 0011	0.7115
	0	001 0100	0.7262
	0	001 0101	0.7363
	0	001 0110	0.7521
	0	001 0111	0.7630
	0	001 1000	0.7742
	0	001 1001	0.7858
	0	001 1010	0.7977
	0	001 1011	0.8100
	0	001 1100	0.8226
	0	001 1101	0.8356
	0	001 1110	0.8491
	0	001 1111	0.8630
	0	010 0000	0.8774
	0	010 0001	0.8848
	0	010 0010	0.8999
	0	010 0011	0.9155
	0	010 0100	0.9235
	0	010 0101	0.9400
	0	010 0110	0.9485
	0	010 0111	0.9659
	0	010 1000	0.9748
	0	010 1001	0.9839
	0	010 1010	1.0030

Table 6-7. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Under Voltage Detection) hys_en=0	0	010 1011	1.0120
	0	010 1100	1.0220
	0	010 1101	1.0320
	0	010 1110	1.0530
	0	010 1111	1.0630
	0	011 0000	1.0740
	0	011 0001	1.0850
	0	011 0010	1.0970
	0	011 0011	1.1140
	0	011 0100	1.1260
	0	011 0101	1.1380
	0	011 0110	1.1510
	0	011 0111	1.1630
	0	011 1000	1.1760
	0	011 1001	1.1900
	0	011 1010	1.1960
	0	011 1011	1.2100
	0	011 1100	1.2240
	0	011 1101	1.2380
	0	011 1110	1.2530
	0	011 1111	1.2610
	0	100 0000	1.2760
	0	100 0001	1.2920
	0	100 0010	1.3000
	0	100 0011	1.3160
	0	100 0100	1.3240
	0	100 0101	1.3410
	0	100 0110	1.3500

Table 6-7. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	000 0000	0.7262
	1	000 0001	0.7363
	1	000 0010	0.7521
	1	000 0011	0.7630
	1	000 0100	0.7743
	1	000 0101	0.7858
	1	000 0110	0.7977
	1	000 0111	0.8100
	1	000 1000	0.8226
	1	000 1001	0.8357
	1	000 1010	0.8491
	1	000 1011	0.8630
	1	000 1100	0.8774
	1	000 1101	0.8848
	1	000 1110	0.8999
	1	000 1111	0.9155
	1	001 0000	0.9236
	1	001 0001	0.9400
	1	001 0010	0.9485
	1	001 0011	0.9659
	1	001 0100	0.9748
	1	001 0101	0.9839
	1	001 0110	1.0030
	1	001 0111	1.0120
	1	001 1000	1.0220
	1	001 1001	1.0320
	1	001 1010	1.0530
	1	001 1011	1.0630
	1	001 1100	1.0740
	1	001 1101	1.0850
	1	001 1110	1.0970
	1	001 1111	1.1140
	1	010 0000	1.1260
	1	010 0001	1.1380
	1	010 0010	1.1510
	1	010 0011	1.1630
	1	010 0100	1.1760
	1	010 0101	1.1900
	1	010 0110	1.1960
	1	010 0111	1.2100
	1	010 1000	1.2240
	1	010 1001	1.2380
	1	010 1010	1.2530

Table 6-7. Bit Settings of POK_CORE with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**474mV - 1.35V**
Over Voltage Detection	**1**	**XXX XXXX**	**726mV - 1.645V**
POK_CORE VMON Selection (Over Voltage Detection) hys_en=0	1	010 1011	1.2610
	1	010 1100	1.2760
	1	010 1101	1.2920
	1	010 1110	1.3000
	1	010 1111	1.3160
	1	011 0000	1.3240
	1	011 0001	1.3410
	1	011 0010	1.3500
	1	011 0011	1.3670
	1	011 0100	1.3760
	1	011 0101	1.3850
	1	011 0110	1.4040
	1	011 0111	1.4130
	1	011 1000	1.4230
	1	011 1001	1.4420
	1	011 1010	1.4520
	1	011 1011	1.4620
	1	011 1100	1.4720
	1	011 1101	1.4830
	1	011 1110	1.5040
	1	011 1111	1.5150
	1	100 0000	1.5260
	1	100 0001	1.5370
	1	100 0010	1.5480
	1	100 0011	1.5600
	1	100 0100	1.5710
	1	100 0101	1.5830
	1	100 0110	1.5950
	1	100 0111	1.6070
	1	100 1000	1.6200
	1	100 1001	1.6320
	1	100 1010	1.6450

Table 6-8. Bit Settings of POK_1P8 with VMON Threshold Values

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.44V - 2.173V**
Over Voltage Detection	**1**	**XXX XXXX**	**1.44V - 2.173V**
POK_1P8 (Under Voltage Detection) hys_en=0	0	010 0000	1.44
	0	010 0001	1.452
	0	010 0010	1.477
	0	010 0011	1.502
	0	010 0100	1.515
	0	010 0101	1.543
	0	010 0110	1.556
	0	010 0111	1.585
	0	010 1000	1.6
	0	010 1001	1.615
	0	010 1010	1.645
	0	010 1011	1.661
	0	010 1100	1.677
	0	010 1101	1.694
	0	010 1110	1.728
	0	010 1111	1.745
	0	011 0000	1.763
	0	011 0001	1.781
	0	011 0010	1.799
	0	011 0011	1.828
	0	011 0100	1.848
	0	011 0101	1.868
	0	011 0110	1.888
	0	011 0111	1.909
	0	011 1000	1.93
	0	011 1001	1.952
	0	011 1010	1.963
	0	011 1011	1.986
	0	011 1100	2.009
	0	011 1101	2.032
	0	011 1110	2.056
	0	011 1111	2.069
	0	100 0000	2.094
	0	100 0001	2.12
	0	100 0010	2.133
	0	100 0011	2.159
	0	100 0100	2.173

Table 6-8. Bit Settings of POK_1P8 with VMON Threshold Values (continued)

POK Programmability	**POK Configuration Register bits**		**THRESHOLD (V)**
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**1.44V - 2.173V**
Over Voltage Detection	**1**	**XXX XXXX**	**1.44V - 2.173V**
POK_1P8 (Under Voltage Detection) hys_en=0	1	000 1100	1.44
	1	000 1101	1.452
	1	000 1110	1.477
	1	000 1111	1.502
	1	001 0000	1.515
	1	001 0001	1.543
	1	001 0010	1.556
	1	001 0011	1.585
	1	001 0100	1.6
	1	001 0101	1.615
	1	001 0110	1.645
	1	001 0111	1.661
	1	001 1000	1.677
	1	001 1001	1.694
	1	001 1010	1.728
	1	001 1011	1.745
	1	001 1100	1.763
	1	001 1101	1.781
	1	001 1110	1.799
	1	001 1111	1.828
	1	010 0000	1.848
	1	010 0001	1.868
	1	010 0010	1.888
	1	010 0011	1.909
	1	010 0100	1.93
	1	010 0101	1.952
	1	010 0110	1.963
	1	010 0111	1.986
	1	010 1000	2.009
	1	010 1001	2.032
	1	010 1010	2.056
	1	010 1011	2.069
	1	010 1100	2.094
	1	010 1101	2.12
	1	010 1110	2.133
	1	010 1111	2.159
	1	011 0000	2.173

Table 6-9. Bit Settings of POK_3P3 with VMON Threshold Values

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Under Voltage Detection) hys_en=0	0	000 0000	1.427
	0	000 0001	1.466
	0	000 0010	1.501
	0	000 0011	1.545
	0	000 0100	1.576
	0	000 0101	1.616
	0	000 0110	1.658
	0	000 0111	1.694
	0	000 1000	1.731
	0	000 1001	1.769
	0	000 1010	1.81
	0	000 1011	1.841
	0	000 1100	1.885
	0	000 1101	1.919
	0	000 1110	1.955
	0	000 1111	1.992
	0	001 0000	2.03
	0	001 0001	2.07
	0	001 0010	2.111
	0	001 0011	2.14
	0	001 0100	2.184
	0	001 0101	2.215
	0	001 0110	2.262
	0	001 0111	2.295
	0	001 1000	2.329
	0	001 1001	2.363
	0	001 1010	2.399
	0	001 1011	2.436
	0	001 1100	2.474
	0	001 1101	2.513
	0	001 1110	2.554
	0	001 1111	2.596
	0	010 0000	2.639
	0	010 0001	2.661
	0	010 0010	2.706
	0	010 0011	2.753
	0	010 0100	2.778
	0	010 0101	2.827
	0	010 0110	2.853
	0	010 0111	2.905
	0	010 1000	2.932
	0	010 1001	2.959

Table 6-9. Bit Settings of POK_3P3 with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Under Voltage Detection) hys_en=0	0	010 1010	3.015
	0	010 1011	3.044
	0	010 1100	3.074
	0	010 1101	3.104
	0	010 1110	3.166
	0	010 1111	3.198
	0	011 0000	3.231
	0	011 0001	3.264
	0	011 0010	3.298
	0	011 0011	3.35
	0	011 0100	3.386
	0	011 0101	3.423
	0	011 0110	3.46
	0	011 0111	3.498
	0	011 1000	3.538
	0	011 1001	3.577
	0	011 1010	3.598
	0	011 1011	3.639
	0	011 1100	3.681
	0	011 1101	3.724
	0	011 1110	3.769
	0	011 1111	3.791
	0	100 0000	3.837
	0	100 0001	3.884
	0	100 0010	3.908
	0	100 0011	3.957
	0	100 0100	3.982

Table 6-9. Bit Settings of POK_3P3 with VMON Threshold Values (continued)

POK Programmability	**POK Configuration Register bits**		**THRESHOLD (V)**
	[7]	**[6:0]**	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Over Voltage Detection) hys_en=0	1	000 0000	2.184
	1	000 0001	2.215
	1	000 0010	2.262
	1	000 0011	2.295
	1	000 0100	2.329
	1	000 0101	2.363
	1	000 0110	2.399
	1	000 0111	2.436
	1	000 1000	2.474
	1	000 1001	2.513
	1	000 1010	2.554
	1	000 1011	2.596
	1	000 1100	2.639
	1	000 1101	2.661
	1	000 1110	2.707
	1	000 1111	2.754
	1	001 0000	2.778
	1	001 0001	2.827
	1	001 0010	2.853
	1	001 0011	2.905
	1	001 0100	2.932
	1	001 0101	2.959
	1	001 0110	3.016
	1	001 0111	3.045
	1	001 1000	3.074
	1	001 1001	3.104
	1	001 1010	3.166
	1	001 1011	3.198
	1	001 1100	3.231
	1	001 1101	3.264
	1	001 1110	3.298
	1	001 1111	3.35
	1	010 0000	3.386
	1	010 0001	3.423
	1	010 0010	3.46
	1	010 0011	3.499
	1	010 0100	3.538
	1	010 0101	3.578
	1	010 0110	3.598
	1	010 0111	3.639
	1	010 1000	3.682
	1	010 1001	3.725

Table 6-9. Bit Settings of POK_3P3 with VMON Threshold Values (continued)

POK Programmability	POK Configuration Register bits		THRESHOLD (V)
	[7]	[6:0]	
Under Voltage Detection	**0**	**XXX XXXX**	**1.427V - 3.982V**
Over Voltage Detection	**1**	**XXX XXXX**	**2.184V - 3.958V**
POK_3P3 (Over Voltage Detection) hys_en=0	1	010 1010	3.769
	1	010 1011	3.792
	1	010 1100	3.838
	1	010 1101	3.885
	1	010 1110	3.909
	1	010 1111	3.958

6.2.4.2 Power on Reset (POR) Module

This section describes the Power on Reset (POR) module.

6.2.4.2.1 POR Overview

POR module in this family of devices is responsible for detecting proper operating voltage levels on VDDA_MCU (under voltage), and both under and over voltages for analog supply in Top Level and MCU_CTRL MMR.

POR Modules Allocation within Device Domains shows POR modules allocation within device domains.

Table 6-10. POR Modules Allocation within Device Domains

Module Instance	Domain	
	Top Level	MAIN
POR0		-

6.2.4.2.2 POR Integration

The device supports one instance of a Power on Reset (POR) module - MCU_POR0. MCU_POR0 is located in the Top Level Domain. *POR Integration* shows the integration of MCU_POR0.

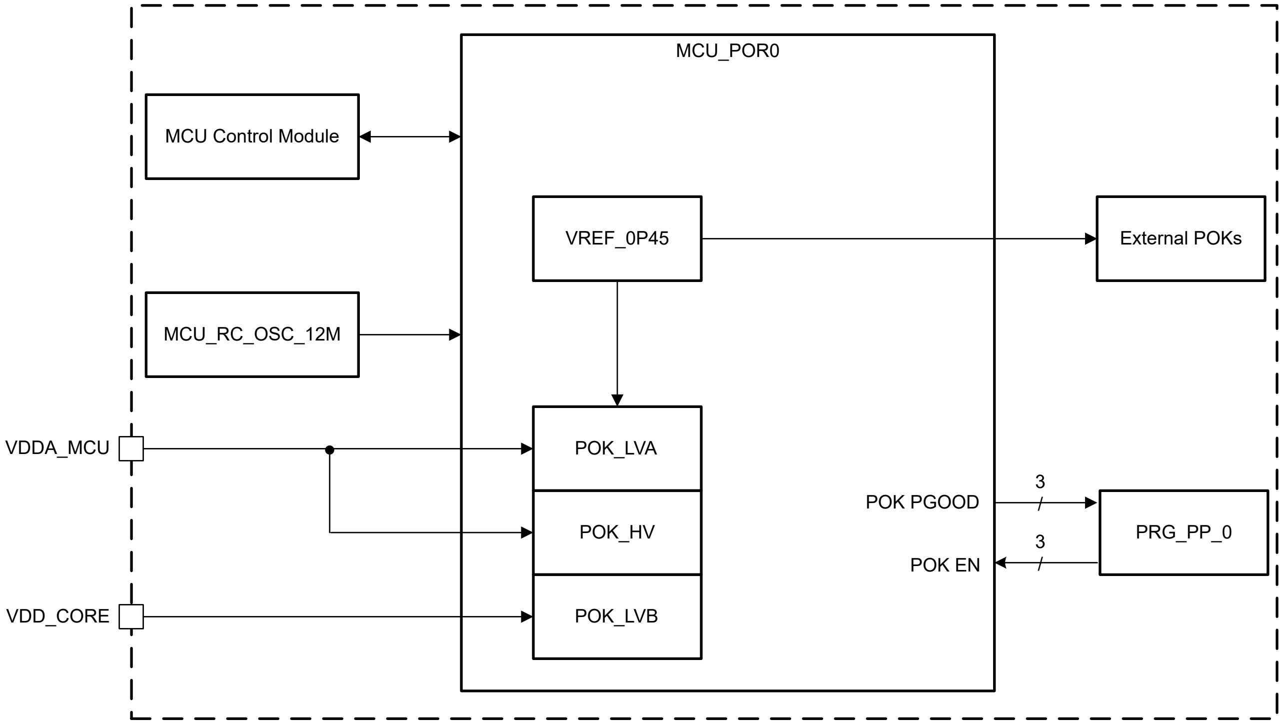


Figure 6-6. POR Integration

Table 6-11. POR Modules

POR Module Instance Name	PRG Index	POK Index	Voltage Monitored	Module Type	OV/ UV[1]	Description
POKHV	PRG0	2	VDDA_MCU	POR	UV	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE
POKLVA	PRG0	1	VDDA_MCU	POR	OV	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE
POKLVB	PRG0	0	VDD_CORE	POR	UV	Internal POR generation and power monitoring for 1.8-V supply and VDD_CORE

(1) UV: POK is set for under voltage detection. OV: POK is set for over voltage detection. UV/OV: POK monitors both OV and UV via Ping-Pong mechanism.

6.2.4.3 PoR/Reset Generator (PRG) Modules

6.2.4.3.1 PRG Overview

A PRG module is responsible for implementing enable/disable controls and event/interrupt masking logic on all POK outputs.

Figure 6-7 shows the PRG module overview.

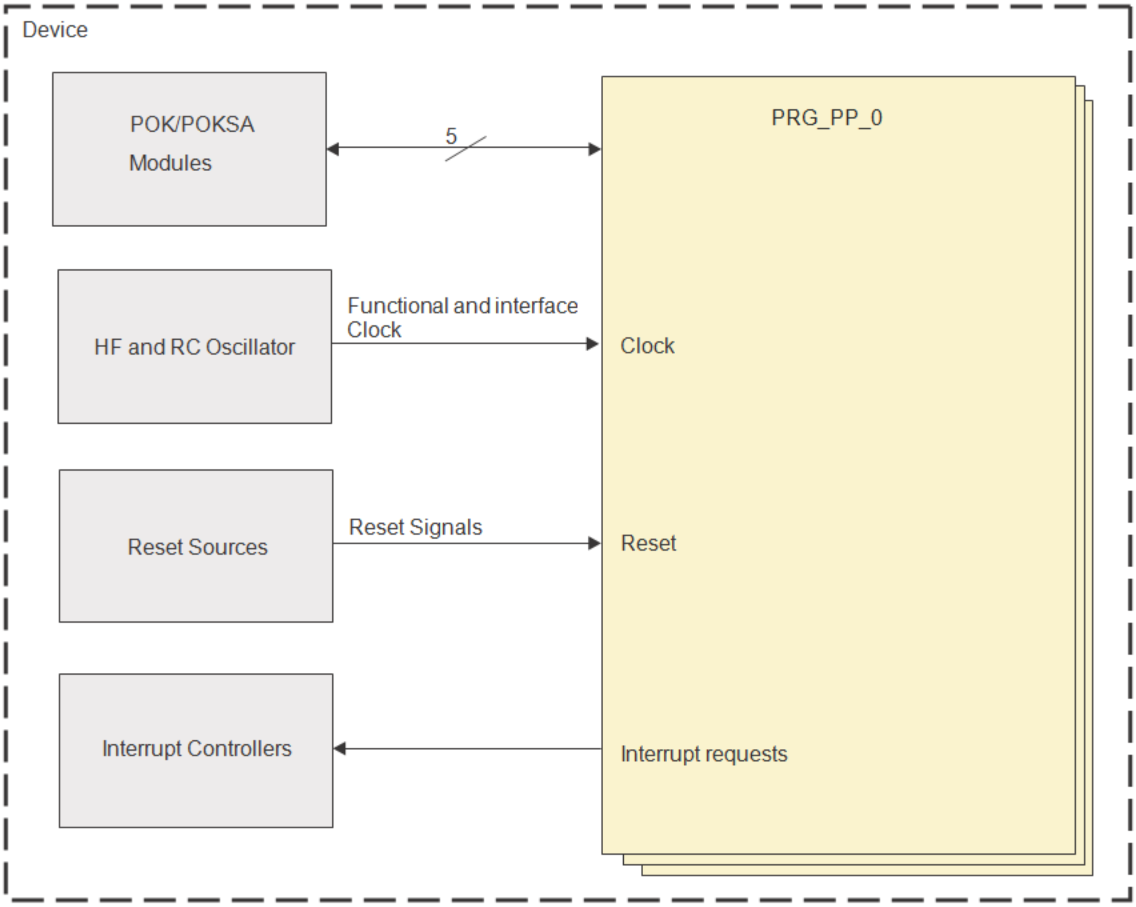


Figure 6-7. PRG0 Overview

Figure 6-8 shows the PRG module overview.

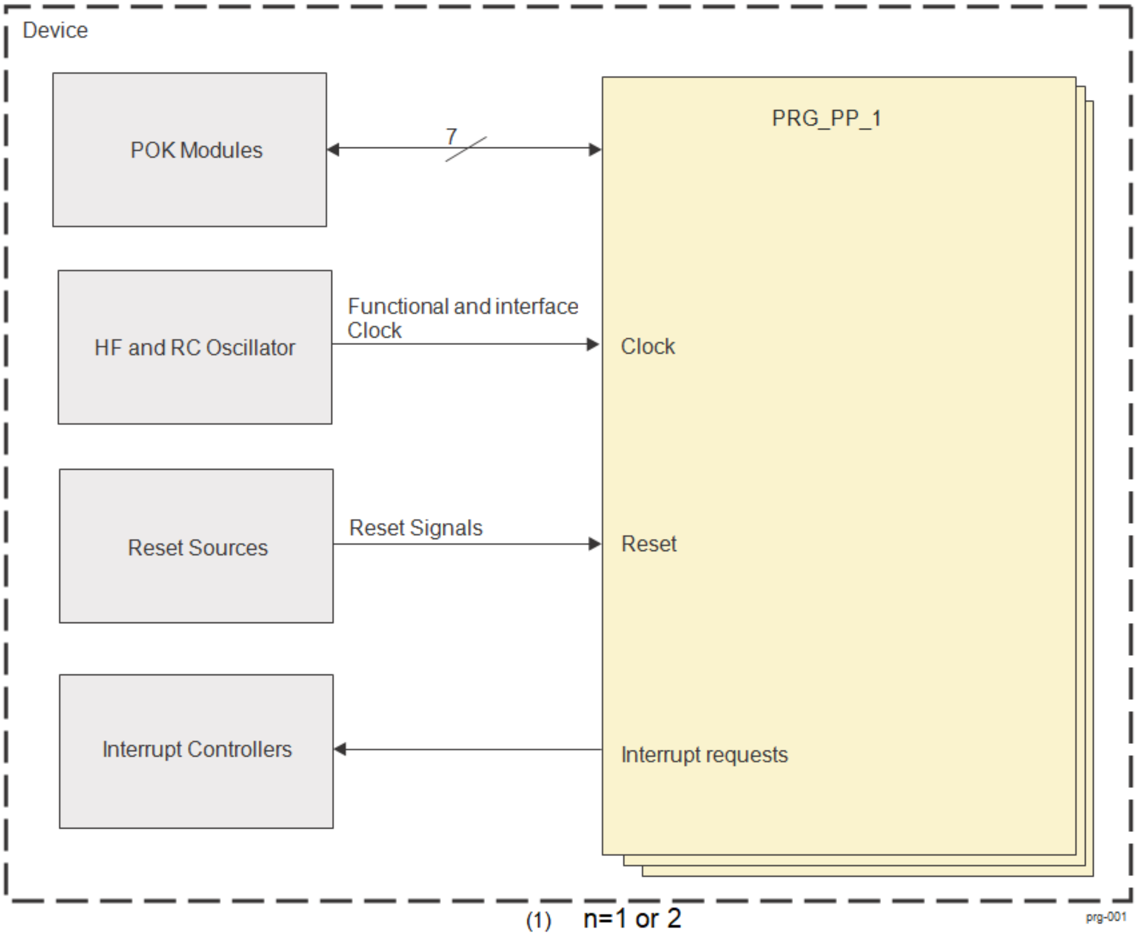


Figure 6-8. PRG1 Overview

6.2.4.4 Power Glitch Detect (PGD) Modules

A Power Glitch Detect (PGD) circuit is used to detect short duration “glitches” on the core and MPU power supplies. The PGD provides a low output when no glitch is detected and a high output when a glitch is detected.

PGD Allocation withing Device Domains shows PGD modules allocation within device domains.

Table 6-12. PGD Allocation within Device Domains

Module Instance	Domain		
	WKUP	Top Level	MAIN
IPGD_VDD_CORE	-	✓	-

PGD Block Diagram shows the PGD block diagram.

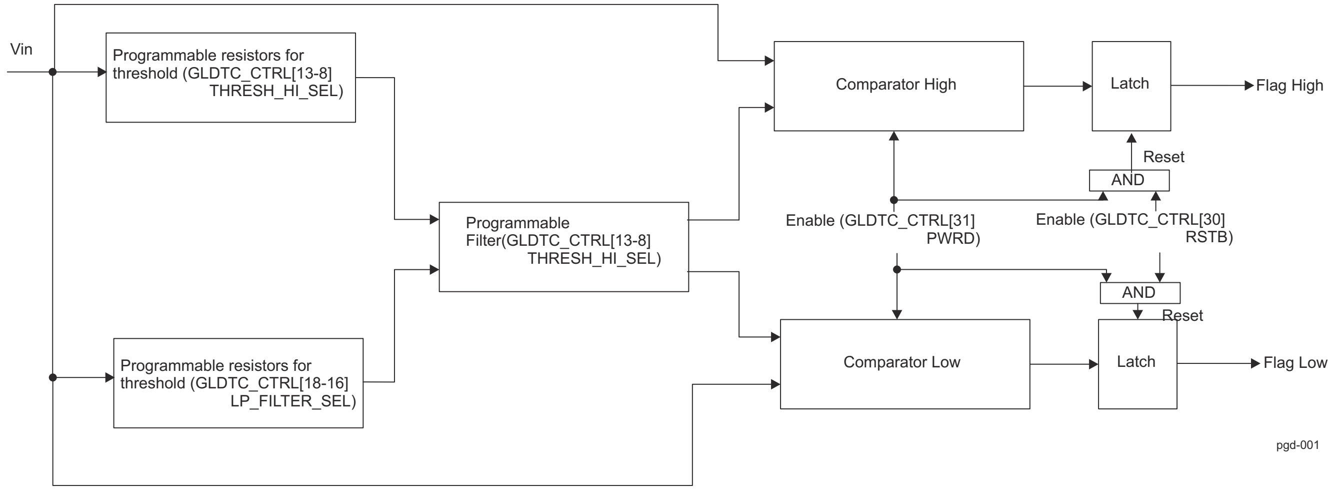


Figure 6-9. PGD Block Diagram

PGD Integration Summary summarizes the PGD integration.

Table 6-13. PGD Integration Summary

Module Instance	Monitored Voltage	PGD Control/Status Registers[1]
IPGD_VDD_CORE	VDD_CORE	

(1) For more information about control registers, see , *Control Module (CTRL_MMR)*.

Note

A flag status bit in corresponding STAT register is cleared by clearing the [30] RSTB bit in the corresponding CTRL register, see for STAT and CTRL registers for a certain PGD module.

6.2.4.5 Voltage and Thermal Manager (VTM)

6.2.4.5.1 VTM Overview

This section describes the Voltage and Thermal Manager (VTM) module in the device.

The VTM module supports voltage and thermal management of the device by providing control of on-chip temperature sensors.

The device supports a single VTM module, VTM0, which is located in the WKUP domain. VTM0 has two associated temperature monitors, Temp_Sensor_Main_0, and Temp_Sensor_Main_1, each of which are located near hotspots in the device die.

VTM Overview shows VTM module allocation within device domains.

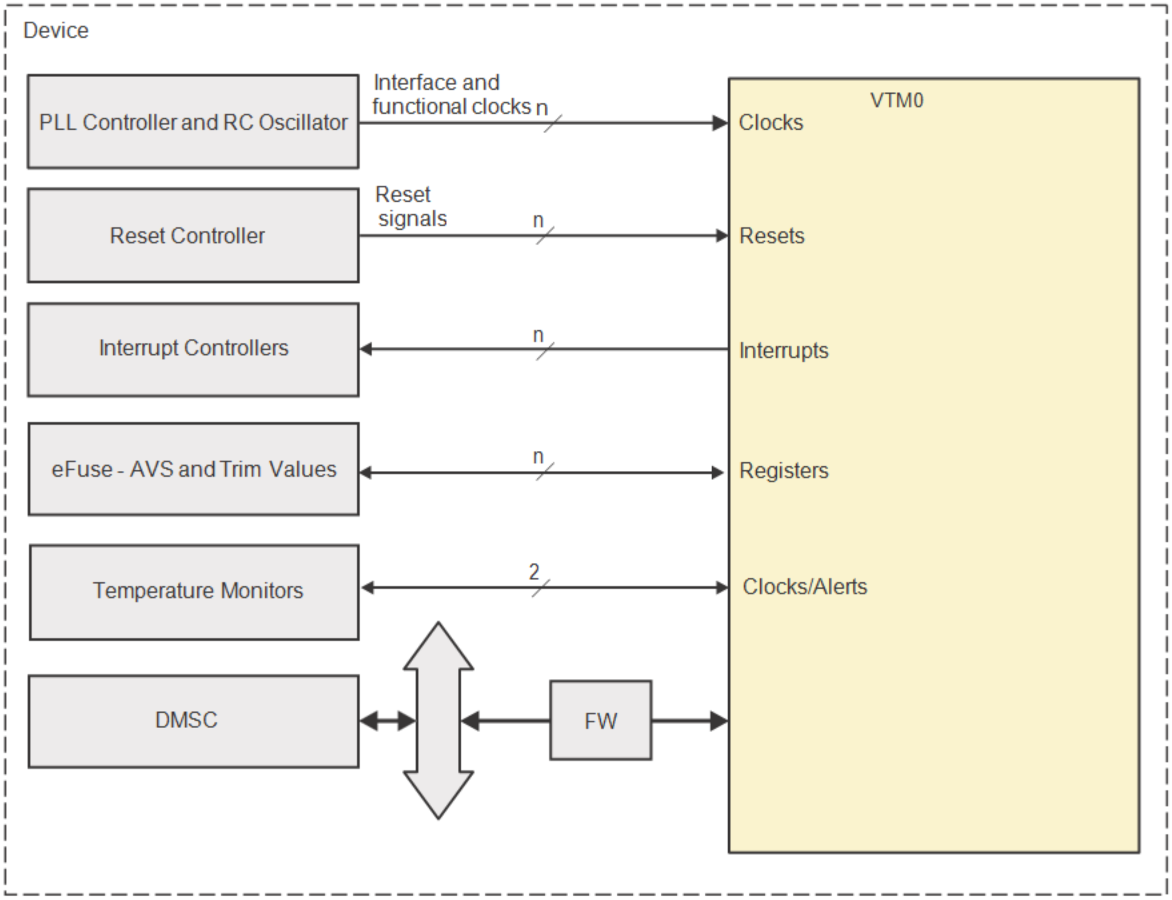


Figure 6-10. VTM Overview

6.2.4.5.1.1 VTM Features

VTM module supports the following features:

- Programming of temperature-crossing thresholds
- Signals when programed thresholds are exceeded - up to 3 alerts:
  - Three full reference 10-bit temperature threshold points, THPT1, THPT2 and THPT0.
  - Two relative 4-bit delta values vs THPT1 (one an increment and another a decrement), each able to set additional threshold point, THPT2 and THPT0.
- Supports up to 8 temperature monitors
- Allows resolution of 0.5°C for temperature reading and threshold point temperature alert/interrupt generation.
- Supports PMIC/LDO set-up with Class-0 VDD-VID settings
- Support of tentative customization of OPP voltage per device (in support of multiple OPPs)
- AVS-voltage or thermal management for up to 8 voltage domains
- Maximum temperature alert

- Supports one shot sampling mode and continuous monitoring mode for the sensors
- Contains registers with reset defaults from e-fuse values needed to supports SR-Class0 via e-fuse/ manufacturing calibration and firmware and/or software using those values to program the PMIC/LDO with the Class-0 VDD-VID setting.
- Contains registers with reset defaults from e-fuse values per SOC for a tentative customization of OPP voltage per device (in support of multiple OPPs/DVFS).
- Supports a group of registers for up to 8 core voltage domains that require AVS-voltage management or thermal management in a contiguous memory region to support access privilege control by Firewall within the address space.
- Core voltage domains that don’t require any SR-Class0 or thermal management shall not be controlled or map to any of the WKUP_VTM0 voltage domain group.
- Contains registers with reset defaults from e-fuse values or TIE-OFFs to provide control for temperature monitors and interrupt generation needed to support thermal management customized if necessary in a per voltage domain basis.
- Provides register control, status and interrupt generation, and alerts for up to 8 temperature monitors.
- Stores in the registers the defaults for temperature detection threshold points and other temperature monitor control values for Firmware usage.
- Samples, captures, and allows for register read of the on-die temperature monitor present reading.
- Provides interrupt and status for out of range temperature reading.
- Provides one full reference 10-bit temperature threshold point, THPT1.
- Provides 2 relative 3-bit delta values versus THPT1, one an increment and another a decrement, which yields 2 additional threshold points, THPT2 and THPT0, in close proximity to THPT1.
- Provides 3 temperature threshold point alert signals (level), GT_TH1_ALERT, GT_TH2_ALERT and LT_TH0_ALERT, for each one of the up to 8 temperature monitors.
- Provides 3 temperature threshold point interrupt flags, GT_TH1_INT, GT_TH2_INT and LT_TH0_INT, for each one of the up to 8 voltage domains.
- Provides 3 temperature threshold point interrupts (level-only) for the entire MCU_VTM0, GT_TH1_INT, GT_TH2_INT and LT_TH0_INT, which are driven out of WKUP_VTM0 and are shared by the 8 voltage domains. The output port interrupts correspond to the OR function of the contributions of the 8 voltage domains. See *VTM Summaries* for additional details on these interrupts.
- Software must read the corresponding flags in each of the 8 voltage domains to identify which voltage domain is active.
- Allows for temperature reading and threshold point temperature alert and interrupt generation with 0.5°C of resolution.

Note

The VTM in this family of devices implements two temperature monitors.

6.2.4.5.1.2 VTM Not Supported Features

- No support for AVS-Class0 with temperature compensation (AVS0 + TC)
- No support internal to MCU_VTM0 for any AVS Class technology other than Class0
- No support for K1 or K2 4/6-bit VCNTL/VID parallel or 2-step interfaces.
- No integrated I2C inside VTM
- No direct hardware triggering of I2C transactions by VTM. Only interrupt and event generation is supported.
- No support for voltage and thermal management of I/O voltage domains. Only core domain voltage/thermal management is supported.
- VTM0 does not contain or support register groups or control hooks for I/O voltage domains.
- Core voltage domains that do not require any voltage or thermal management are not controlled or mapped to any of the VTM0 voltage domain groups.
- Everything else not explicitly listed in *VTM Features* is not supported.
- No oversampling of the temperature reading
- No support for eFuse defaults of all register values

6.2.4.5.2 VTM Functional Description

In the same way that PRGs control and provide output from the POKs, the VTM controls and outputs signals from several temperature sensors that are spread around the die. The VTM provides three interrupts / ESM inputs to the system as well as a warm reset.

When the temperature sensor is enabled, it senses the temperature and reports the temperature as a 10-bit value.

- The raw 10-bit value is reported in VTM_CFG1_TMPSENS_STAT_J
- It is also compared to pre-defined thresholds (each temperature sensor has its own set thresholds set in VTM_CFG1_TMPSENS_TH_J and VTM_CFG1_TMPSENS_TH2_J
- It is also compared to a pre-defined global threshold set in VTM_CFG2_MISC_CTRL2.

Each of these comparisons can be individually enabled (VTM_CFG1_TMPSENS_CTRL_J and VTM_CFG1_TMPSENS_CTRL_J within mmr_vbusp_cfg2). Additionally, each temperature sensor has status bits for these comparator outputs in VTM_CFG1_TMPSENS_STAT_J.

The comparator functionality that drives the interrupts and warm reset work only when the sensor is configured for continuous mode; continuous operation becomes a de facto requirement (and is set in VTM_CFG1_TMPSENS_CTRL_J [4].CONT within mmr_vbusp_cfg2 – that is, the mode is set for *each* temperature sensor).

Interrupts / ESM inputs:

The comparator thresholds shall always configured so that TH2 > TH1 > TH0. The concept is:

- TH1 is configured as an early alarm to indicate that the temperature is greater than the threshold defined in VTM_CFG1_TMPSENS_TH_J[25-16] TH1_VAL.
- TH2 is configured as a warning to indicate that the temperature is greater than the threshold defined in VTM_CFG1_TMPSENS_TH2_J[9-0] TH2_VAL. The concept is that TH1 indicates that the processor is getting hot; TH2 demands immediate attention.
- TH0 is configured to trigger when the sensor detects the temperature less than the threshold defined in VTM_CFG1_TMPSENS_TH_J[9-0] TH0_VAL. This interrupt indicates that the thermal mitigations can be relaxed because the temperature has fallen below the original TH1 level.

LT_TH0_INT, if enabled, will get triggered always when the temperature being read is less than TH0, regardless of whether TH1 interrupt and TH2 interrupt are enabled or have ever been triggered. Therefore if TH0 interrupt is generated, then firmware/software is responsible to enable the TH0 interrupt only as part of the interrupt service routine of TH1 and TH2. Otherwise it will keep triggering when is not needed.

Warm Reset input:

Similar to the interrupts / ESM inputs, the warm reset generation is triggered off a threshold defined in VTM_CFG2_MISC_CTRL2[9-0] MAXT_OUTRG_ALERT_THR. The reset will be released when the compared temperature drops below VTM_CFG2_MISC_CTRL2[25-16] MAXT_OUTRG_ALERT_THR0.

VTM muxing of the temperature comparisons:

The VTM is configured by voltage domains. At this level, all the interrupt / ESM inputs from each temperature sensor can be enabled or disabled; as an example, the comparator outputs from temperature sensor 0 can be ignored in voltage domain 0. The enable is configured with the VTM_CFG1_VD_EVT_SET_J and VTM_CFG1_VD_EVT_CLR_J registers. At the voltage domain-level, the enabled comparator results are combined by interrupt / ESM signal. The combined comparator result can be observed in VTM_CFG1_VD_EVT_STAT_J. As is shown in the following table, j increments over voltage domains for these registers (see *VTM Voltage Domains*). The registers TMPSENS_*_j map to the individual temp sensors.

Table 6-14. VTM Voltage Domains

Register Group	Voltage Domain
WKUP_VTM_*_VD_*_0	VDD_MCU
WKUP_VTM_*_VD_*_1	VDD_CORE
others	Unused

After the temperature sensors are combined at a voltage domain level, the outputs from each voltage domain are enabled at the top level of the VTM with VTM_CFG1_GT_TH2_INT_EN_SET / VTM_CFG1_GT_TH2_INT_EN_CLR, VTM_CFG1_GT_TH1_INT_EN_SET / VTM_CFG1_GT_TH1_INT_EN_CLR, and VTM_CFG1_LT_TH0_INT_EN_SET / VTM_CFG1_LT_TH0_INT_EN_CLR. At this top level of the VTM, the status of these signals is checked and cleared with VTM_CFG1_GT_TH2_INT_RAW_STAT_SET / VTM_CFG1_GT_TH2_INT_EN_STAT_CLR, VTM_CFG1_GT_TH1_INT_RAW_STAT_SET / VTM_CFG1_GT_TH1_INT_EN_STAT_CLR, and VTM_CFG1_LT_TH0_INT_RAW_STAT_SET / VTM_CFG1_LT_TH0_INT_EN_STAT_CLR.

6.2.4.5.2.1 VTM Temperature Status and Thermal Management

VTM module provides temperature reading and interrupt/alert information for thermal management.

VTM controls the temperature monitors in the die. A single VTM can control up to 8 monitors via its registers. The VTM enables the sensors periodically to keep the reported data continually updated becuase the device sensors are not periodical. The temperature value coming back from the monitor is captured and reported by the VTM registers. The VTM keeps the sensors in reset state when not enabled to save power and reduce sensor usage to maximize the sensor life.

Note

A temperature diode sensor is used to measure silicon junction temperature, for more information about temperature diode, see the device-specific Datasheet.

6.2.4.5.2.1.1 10-bit Temperature Values Versus Temperature

Table 6-15 shows a table lookup method for translating code to temperature from temperature monitors which correspond to the temperature measured read from the VTM0_VTM_TMPSENS_STAT_J [9-0] DATA_OUT bitfields. Table 6-15 also provides the values for the temperatures coded in VTM0_VTM_MISC_CTRL2 [25-16] MAXT_OUTRG_ALERT_THR0 and VTM0_VTM_MISC_CTRL2 [9-0] MAXT_OUTRG_ALERT_THR thresholds.

Table 6-15. Temperature Translation Table

Parameter Type	Value								
Temperature [°C] (rounded)	-40	-25	0	25	50	75	100	125	150
Temperature [°C] (unrounded)	-40.03	-24.95	0.01	25.02	49.94	75.03	100.02	124.97	150.00
DATA_OUT Code	28	77	164	260	366	485	620	773	949

Table 6-16 shows a table that gives coefficients of polynomial to calculate code or temperature. The equation to calculate code or temperature is:

$y = a4 \times x^4 + a3 \times x^3 + a2 \times x^2 + a1 \times x + a0$

Table 6-16. Equation Method to Calculate Code or Temperature

Function	Unit	Coefficient				
		a4	a3	a2	a1	a0
Code = f(Temperature)	Decimal value of code	4.9847E-08	1.6972E-05	6.8759E-03	3.6509E+00	1.6407E+02
Temperature = f(Code)	°C	-9.2627E-12	6.0373E-08	-1.7058E-04	3.2512E-01	-4.9002E+01

6.3 Reset

This chapter describes the device reset signals and contains details on reset management.

6.3.1 Overview

Reset Introduction

A reset is designed to bring a device or subsystem into a known state. Resets occur after power up events, as well as through software and hardware reset requests. This section introduces the device reset capabilities and functionality.

Device Resets

The Device Power-on-Reset (POR) is controlled by the external pin MCU_PORz. This pin is driven by an external (off-chip) "Power-Good" Circuit or Power Management IC (PMIC). The MCU_PORz pin should be held active LOW (0) during the entire power-up phase. The device should be held in reset until all power supplies are stable with an additional delay for the High Frequency Oscillator (HFOSC0) clock to stabilize.

The SoC is divided into two separate functional Reset Domains: MCU Reset Domain and MAIN Reset Domain (each containing specific processing cores and peripherals).

- MCU Reset Domain: Managed by the Top Level Domain, PLLCTRL and PSC
- MAIN Reset Domain: Managed by the MAIN Domain, PLLCTRL and PSC, this includes the high performance application cores, Device Management and Low Power Management (DM R5F)

High Level Reset Control illustrates the high-level reset domain partition.

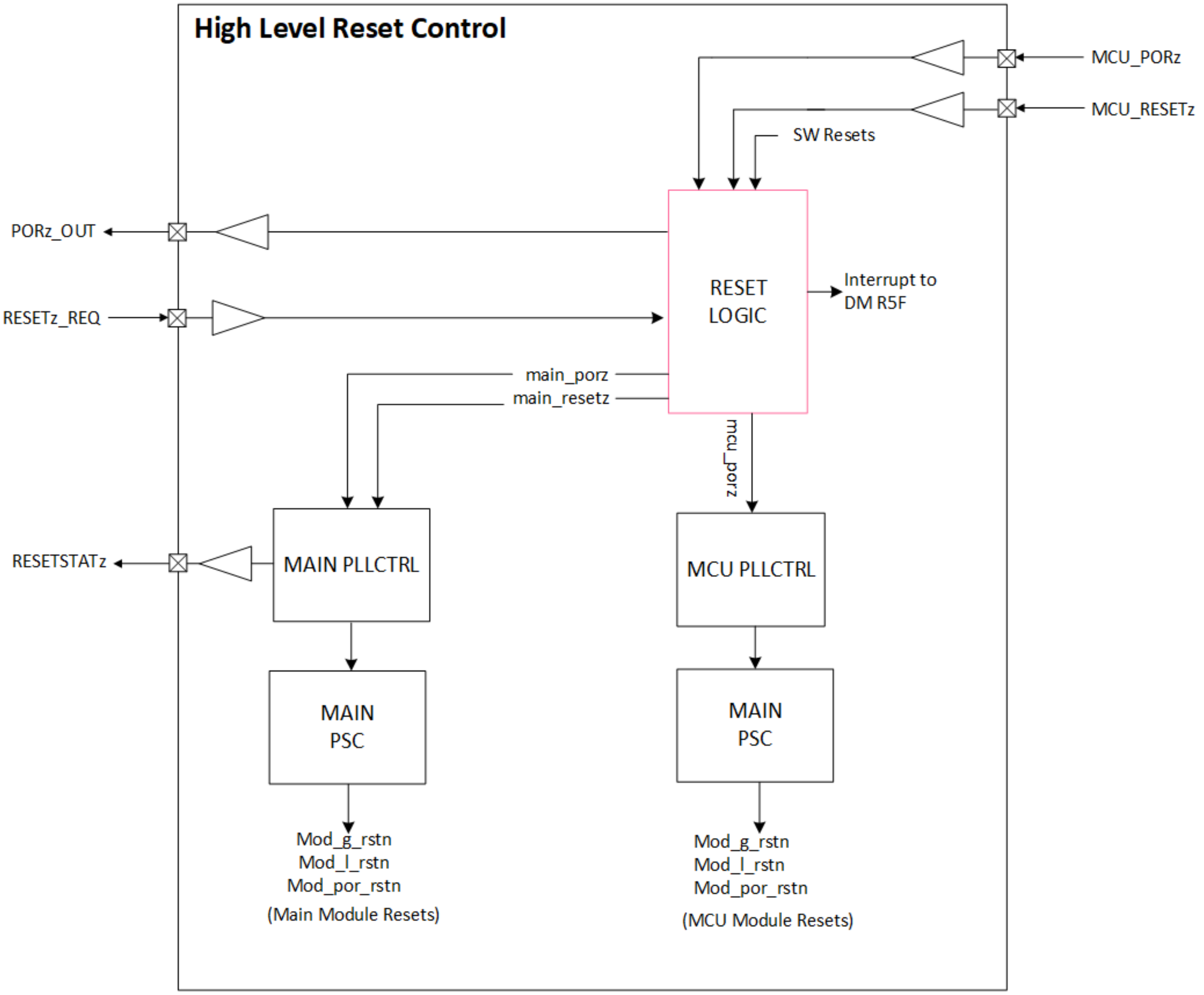


Figure 6-11. High Level Reset Control

6.3.1.1 Top Level Domain Supported Resets

- Power-On-Resets
  - MCU_PORx device pin: This power-on-reset will reset the entire device including Top Level and MAIN domains.
- Warm Resets
  - MCU_RESETz device pin
  - Top Level domain software warm reset
  - Top Level domain ESM error reset
  - SMS cold reset
  - The warm resets listed above will reset the entire device including Top Level and MAIN domains.
- Local Module Resets
  - LPSC module local reset: This reset is generated by the PSCs to locally reset the cores

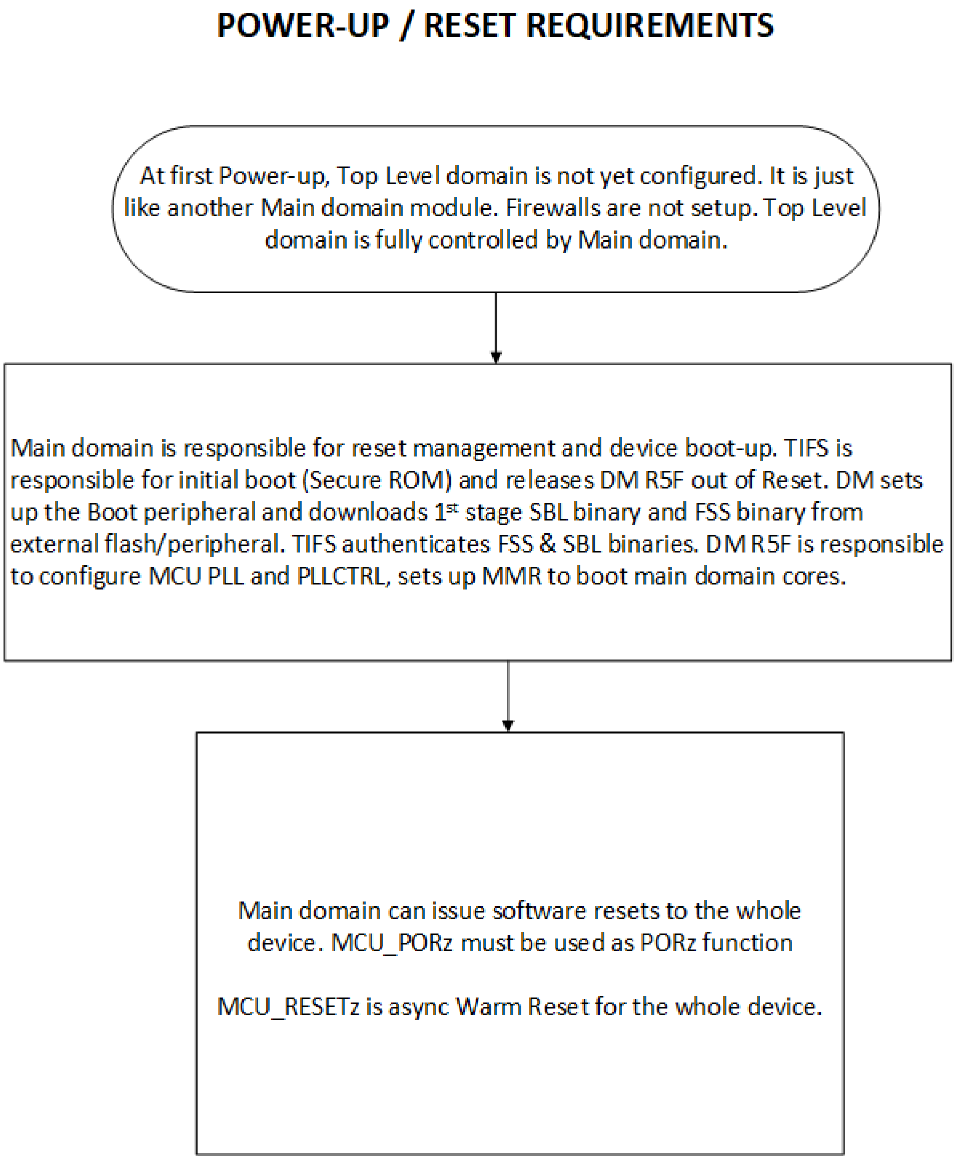
6.3.1.2 MAIN Domain Supported Resets

- Power-On-Resets
  - MAIN domain software POR reset
  - MAIN domain hardware POR reset generated by MCU_PORz
- Warm Resets
  - RESETz_REQ device pin
  - MAIN domain ESM error reset
  - MAIN domain software warm reset
  - SMS cold reset
  - Top Level domain warm reset will also generate a MAIN domain warm reset
- Local Module Resets
  - MAIN domain LPSC module local reset: This reset is generated by the MAIN PSC to locally reset the Processor cores

The device can be configured via software such that a Main domain resets can be isolated from Top Level domain. When the Top Level domain is configured for reset isolation, MAIN domain resets will only reset the MAIN domain and the Top Level domain will remain unaffected by all MAIN domain resets. All Top Level domain resets will cause a reset to the entire device (including MAIN and Top Level domains).

6.3.1.3 High-Level Reset Flow

High Level Reset Flow explains the high-level device power-up and reset use cases.



POWER-UP / RESET REQUIREMENTS

At first Power-up, Top Level domain is not yet configured. It is just like another Main domain module. Firewalls are not setup. Top Level domain is fully controlled by Main domain.

Main domain is responsible for reset management and device boot-up. TIFS is responsible for initial boot (Secure ROM) and releases DM R5F out of Reset. DM sets up the Boot peripheral and downloads 1st stage SBL binary and FSS binary from external flash/peripheral. TIFS authenticates FSS & SBL binaries. DM R5F is responsible to configure MCU PLL and PLLCTRL, sets up MMR to boot main domain cores.

Main domain can issue software resets to the whole device. MCU_PORz must be used as PORz function

MCU_RESETz is async Warm Reset for the whole device.

Figure 6-12. High Level Reset Flow

6.3.1.4 Reset Terminology

DM	Device Management (including Low Power Management)
POR	Power-On-Reset
ESM	Error Signaling Module
Reset Isolation	The module or domain is exempt from specific resets
PSC	Power Sleep Controller
LPSC	Local Power Sleep Controller
PD	Power Domain
VD	Voltage Domain
PRG	Power Reset Generator
POK	Power OK
PGD	Power Glitch Detector
PLLCTRL	PLL and Reset Controller
HHV	High Heating Value mode (IO Pin Fail-safe Control (Tri-State Output))
VTM	Voltage and Temperature Monitor
HFOSC	Internal Device High-Frequency Oscillator
SMS	Security Management Subsystem
TIFS	Texas Instruments Foundational Security
HSM	Hardware Security Module

6.3.1.5 Reset Architecture

6.3.1.5.1 Reset Architecture Block Diagram

Reset Architecture Block Diagrams hows the device reset architecture block diagram. It describes the device reset sub-modules and critical internal signal interconnections.

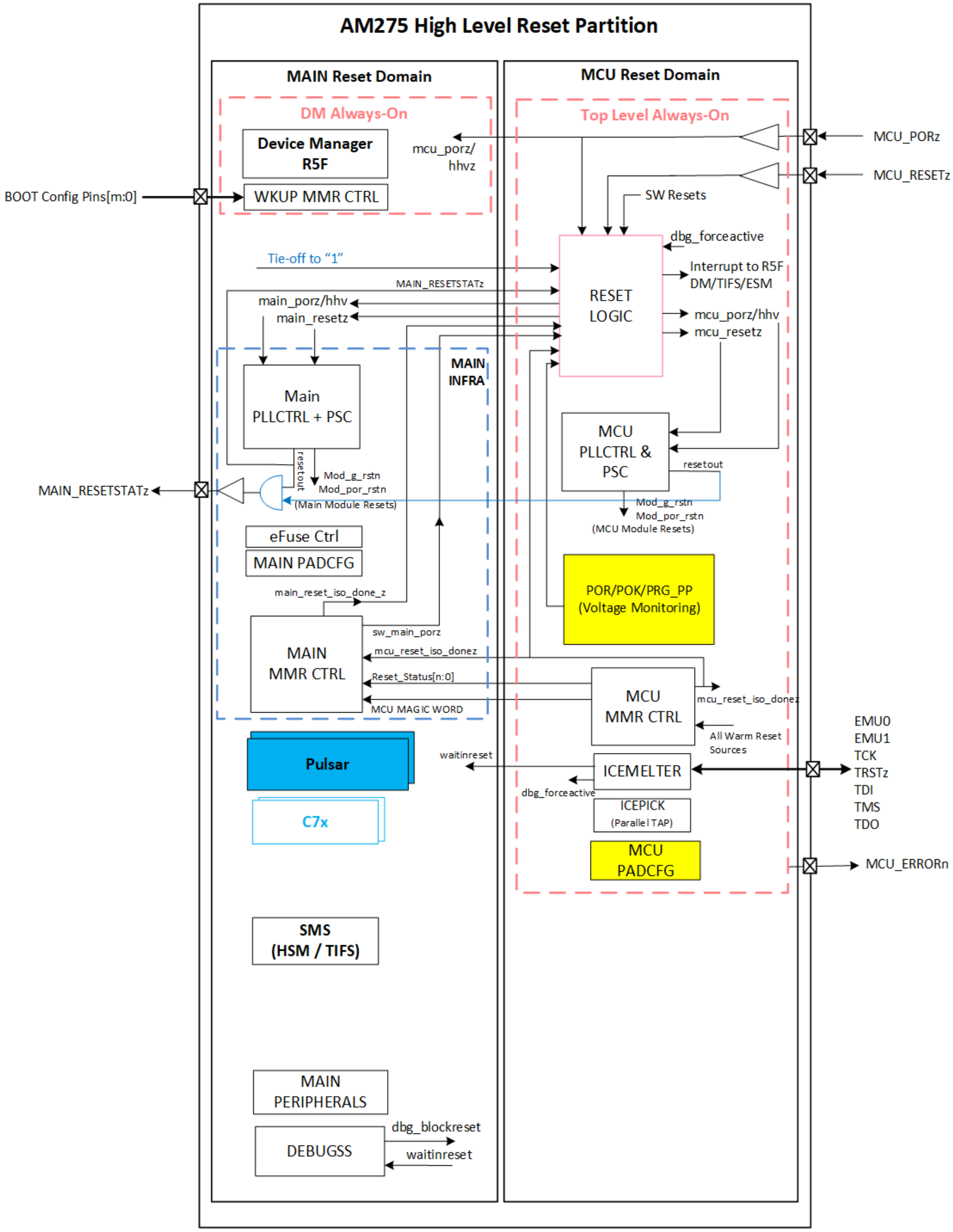


Figure 6-13. Reset Architecture Block Diagrams

6.3.1.5.2 SoC Reset Hardware Logic Diagram

Soc Reset Hardware Logic Diagram shows the reset hardware logic diagram. It describes the MAIN and Top Level domains and processors connections as well as the available reset sources including reset pins and CTRLMMRs.

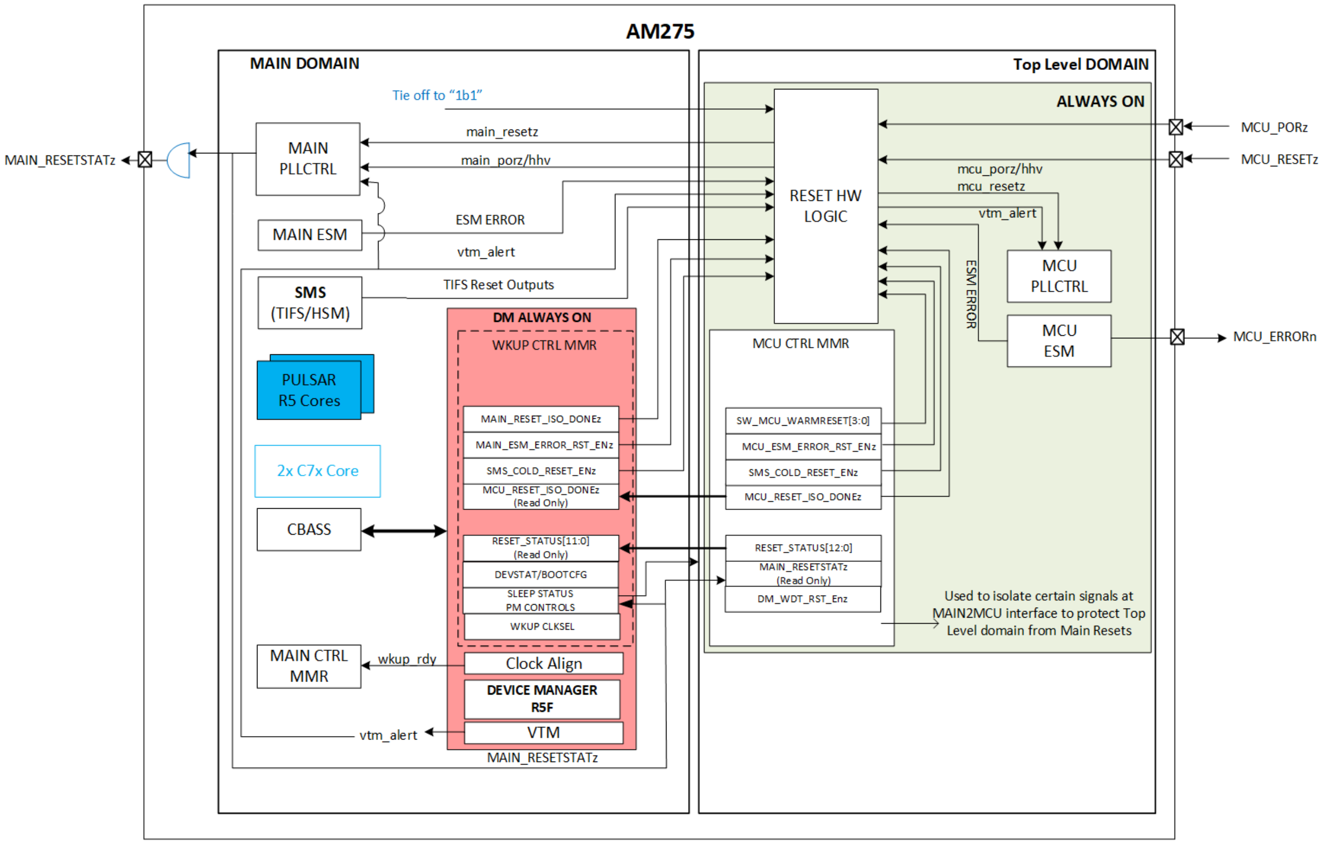


Figure 6-14. SoC Reset Hardware Logic Diagram

6.3.1.5.3 MAIN Domain Reset and PORz Hardware Logic Diagrams

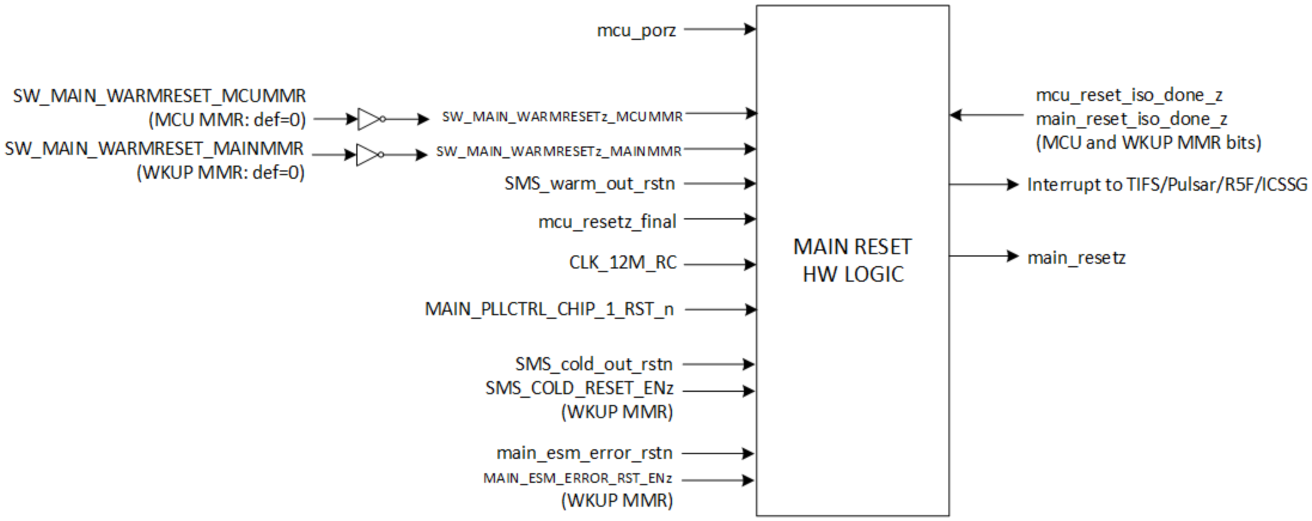


Figure 6-15. MAIN Domain Resetz Hardware Logic Diagram

6.3.2 Reset Sources

Table 6-17 summarizes the available reset sources that are supported by the device.

Table 6-17. Device Reset Sources

Reset Name	Reset Type	Sync/ Async	Pin/ Register/ Internal	Details
MCU_PORz	Hardware POR	Async	MCU_PORz HW Pin	*MCU_PORz Details*
MCU_RESETz	Hardware warm reset	Async	MCU_RESETz HW Pin	*MCU_RESETz Details*
SW_MCU_WARMRSTz	Software warm reset	Sync	MCU_CTRL_MMR_CFG0_RST_CTRL	*SW_MCU_WARMRSTz Details*
VTM Thermal Reset	Thermal error warm reset	Async	Internal Signal	*VTM Thermal Alert Reset Details*
ESM_ERRORz	ESM error warm reset	Async	Internal Signal	*ESM_ERRORz Reset Details*
SMS_COLD_OUT_RST_n	SMS0 cold reset	Async	Internal Signal	*SMS Reset Details*
SMS_WARM_OUT_RST_n	SMS0 warm reset	Async	Internal Signal	*SMS Reset Details*
DM_WDT_RST_n	DM Watchdog Timeout Reset	Async	Internal Signal	*MCU_RESETz Details*

6.3.3 Reset Status

Reset Status shows the Reset Status functionality. An output pin or software bit is used to represent the status of a specific individual reset.

Table 6-18. Reset Status

Reset Status Name	Reset Status Source	Reset Status Info	Signal Active Level	Reset Signal Details
WKUP_CTRL_MMR1 Status Register	Register	4 bits in CTRLMMR on MCU warm reset status and assertion.	Status bits read active HIGH (1) when a particular reset is asserted.	
WKUP_CTRL_MMR0 Status Register	Register	4 bits in CTRLMMR on WKUP warm reset status and assertion.	Status bits read active HIGH (1) when a particular reset is asserted.	
PORz_OUTz	Output Pin	On/Off pin status of MAIN PORz reset	Active LOW (0)	*MAIN_PORz_OUT Status Pin*
RESETSTATz	Output Pin	On/Off pin status of MAIN warm reset	Active LOW (0)	*MAIN_RESETSTATz Status Pin*
MCU_ERRORn	Output Pin	On/Off pin status of MCU ESM_ERROR reset	Active LOW (0)	*MCU_SAFETY_ERRORn Status Pin*

6.3.3.1 Reset Source Status Registers

All warm reset sources which trigger a device/domain warm reset are captured in the MCU_CTRL RST_CTRL This register is only reset on MCU_PORz.

The MCU_CTRL RST_SRC MCU domain CTRLMMR register is shadowed in WKUP domain CTRLMMR RST_SRC so that MAIN domain processors can read it without directly accessing other domains.

After recovery from warm reset, software can read the CTRLMMR reset source register CTRLMMR RST_SRC to identify the source of previous reset. After reading this reset source register, software must clear the register.

Reset status bits read active HIGH (1) when a particular reset is triggered.

The following reset sources, which cause MCU and MAIN domain resets, are captured in the MCU domain CTRLMMR reset source register:

- MCU_RESETz (Reset by Hardware Pin)
- SW_MCU_WARMRSTz (Reset by MCU domain CTRLMMR [1])
- SMS_COLD_OUT_RST_n (Reset by SMS)
- SMS_WARM_OUT_RST_n (Reset by SMS)
- THERM_MAXTEMP_OUTRANGE_ALERT (Reset by VTM Max Temperature Alert)
- SYSR_ASSERTRESET_n (Reset by DEBUGSS)
- MCU_ESM_ERROR_RST_n (Reset by ESM Error)
- MAIN_ESM_ERROR_RST_n (Reset by ESM Error)
- DM_WDT RST_n (Reset by WKUP WDT Timeout)
- DM_MAIN_PORz (Reset by DS_MAIN_POR_PDOFF a WKUP domain CTRLMMR [1])
  - MCU ESM Error will reset entire device
  - MAIN ESM Error will only reset MAIN domain when MCU domain is isolated. When MCU domain is not isolated, it will warm reset both MCU and MAIN domains.

Note

1. MAIN domain software WARMRSTz and PORz control registers are defined in both WKUP domain CTRLMMR and Top Level domain CTRLMMR.

When a MAIN domain processor needs to issue resets to MAIN domain on error detection they will use the WARMRESETz and PORz MMR bits defined in the WKUP domain CTRLMMR.

6.3.3.2 MCU_ERRORn Status Pin

The MCU_ERRORn pin indicates the Top Domain domain ESM status. This Output is used to signal an external agent that it needs to (or may need to) intervene because of an error. The Error Pin Output is active Low or PWM, based on the ESM Error Pin Control register pwm_en field (Refer ESM IP) . This pwm_en field should only be modified when the ESM is disabled, based on the Global Enable register. Refer ESM chapter for details.

While in Power-On-Reset, the Error Pin is active (asserted low). SoC drives a Low via a weak internal pull-down. After Power-On-Reset condition is removed, ESM will drive the Error Pin. During a Warm Reset the state of the Error Pin is unchanged (i.e. the Error Pin logic is only reset by asserting MCU_PORz low).

When MCU_ERRORn output pin is configured to operate in level mode, a LOW indicates the MCU ESM module has registered an error. A HIGH indicates that there are no MCU ESM errors.

When MCU_ERRORn output pin is configured to operate in PWM mode, no error is indicated by continuous toggle according to programmable MMR widths for high and low periods. When an error occurs, the error pin stops toggling and remains constant until the error is cleared. An external device (such as a PMIC) that is detecting the PWM toggles can identify the error if the pin stops toggling. The periods should be programmed such that they fit within the expectation of the external device.

Note

This signal can be used by external safety devices to determine the device status and assert MCU_PORz if necessary.

6.3.3.3 RESETSTATz Status Pin

This pin indicates warm reset status (active LOW) of the MAIN domain.

When LOW, it indicates that the MAIN domain is in a warm reset state.

When HIGH, it indicates that the MAIN domain is out of reset.

The status of this signal will be captured in CTRL MMR registers.

6.3.3.4 PORz_OUT Status Pin

This pin indicates the POR status of the MAIN domain (active LOW).

When LOW, it indicates the MAIN domain is in the POR state.

When HIGH, it indicates the MAIN domain is out of the POR state.

Note

PORz_OUT may be used to enable and/or disable output buffers of attached devices that share pins associated with BOOTMODE inputs, such that appropriate boot configuration values are allowed to propagate into the device without contention.

6.3.4 Reset Controls

The reset control registers enable, disable, and adjust specific reset operations. This section explains how to control certain device resets.

6.3.4.1 Reset Control Registers

The below tables show the CTRLMMR registers that are able to enable and disable reset abilities and options.

Table 6-19. Top Level Domain Reset Control Registers

Control Name	Control Action	Control Register
MCU_ESM_ERROR_RST_ENz	Enable MCU ESM_ERRORz reset	MCU CTRL RST_CTRL
SMS_COLD_RESET_ENz	Enable SMS cold reset of Top Level domain	MCU CTRL RST_CTRL

Table 6-20. MAIN Domain Reset Control Registers

Control Name	Control Action	Control Register
MAIN_ESM_ERROR_RST_ENz	Enable MAIN ESM_ERRORz Reset	MCU CTRL RST_CTRL
SMS_COLD_RESET_ENz	Enable SMS Cold Reset of MAIN Domain	MCU CTRL RST_CTRL

Note

For more information, see *Control Module (CTRLMMR)*.

6.3.4.2 Reset Isolation

Reset isolation is provided by LPSCs, and the feature is turned off by default. If an IP needs to be reset isolated, then SMS needs to enable this feature through the MMR configurations of that LPSC. If that LPSC supports multiple IPs, then all those IPs will be reset isolated. LPSC settings go back to default srata when the device goes through a power on reset. If reset isolation is not enabled, the LPSC returns back to the default start during warm resets.

Note

The device does not support reset isolation on CPSW

6.3.5 Reset Details

Reset Details Introduction

The Reset Details section will break down the available device resets and explain operating details such as sequencing and reset logic diagrams. It also includes any additional information related to the device resets.

6.3.5.1 POR Resets

6.3.5.1.1 MCU_PORz Reset

Reset Overview

This is the POR reset signal (active LOW) for the entire device, controlled by the MCU_PORz HW Pin.

When LOW, it performs a POR reset on the entire device (Top Level and MAIN domains) and puts IOs in a safe state (as defined in the BALL STATE DURING RESET column of the datasheet Pin Attributes table).

Top Level Domain Effect

All modules in the domain are reset.

Top Level IOs (IOs beginning with MCU_) are in HHV state (Reset State).

When MCU_PORz is de-asserted, the Os will enter the default state defined in the device Datasheet. The domain will be reconfigured by the device boot processor (secondary boot loader).

MAIN Domain Effect

All modules in the MAIN domain are reset.

MAIN domain IOs are in HHV state (as defined in the BALL STATE DURING RESET column of the datasheet Pin Attributes table).

When MCU_PORz is de-asserted, the MAIN domain IOs will enter default state as defined in the BALL STATE AFTER RESET column of the datasheet Pin Attributes table.

The device boot processor (secondary boot loader) will setup R5FSS as Safety or General-Purpose Processor.

6.3.5.2 Warm Resets

6.3.5.2.1 MCU_RESETz Reset

Reset Overview

MCU_RESETz is the Initiator Warm Reset inpit (active low) to the entire device. When active, it resets all modules in the Top Level and Main domains. MCU_RESETz will **not** reset:

- CTRL MMR register bits white are only resettable by PORz events
- Debugss

Boot Mode pins are multiplexed on Main domain IOs. Hence the Boot Mode pins must be latched internally on the rising edge of main_porz. Boot Mode pins get reset only on MCU_PORz or main_porz events

MCU_RESETz Timing

The below images demonstrate the MCU_RESET timing

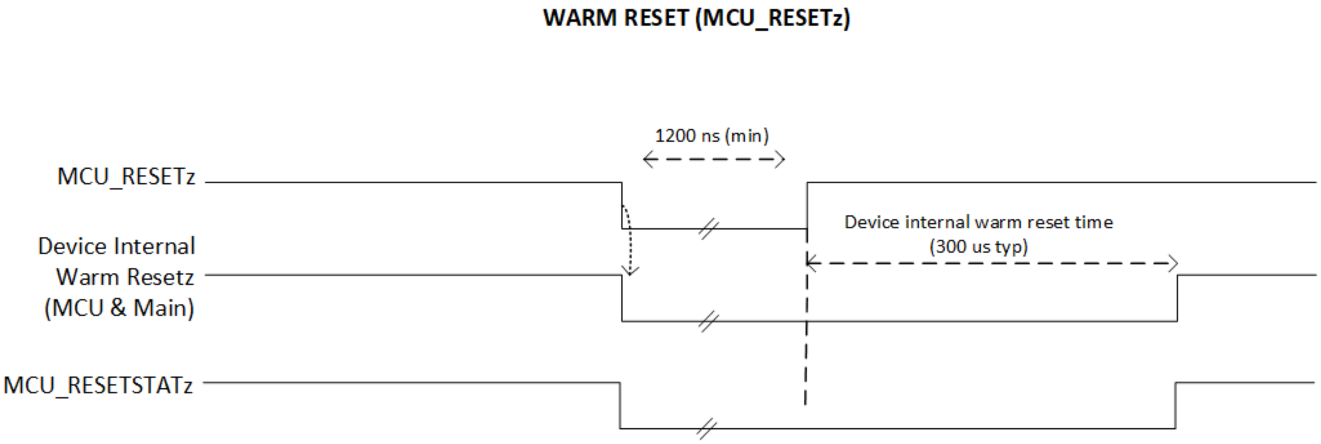


Figure 6-16. MCU_RESETz Timing

Note

MCU Internal Warm Reset (mcu_resetz) will be connected to MCU PLLCTRL

6.3.5.2.2 SW_MCU_WARMRSTz Reset

Reset Overview

This is a software Top Level domain warm reset defined in Top Level domain CTRLMMR.

MCU CTRLMMR defines a 4-bit field, SW_MCU_WARMRST[11:8] (MCU_CTRL_MMR_CFG0_RST_CTRL Register) for generating a software warm reset in the MCU domain (SW_MCU_WARMRSTz).

When SW_MCU_WARMRST[11:8] field is set to “0110”, MCU warm reset is active (SW_MCU_WARMRSTz = LOW).

When SW_MCU_WARMRST[11:8] is set to any other value, MCU warm reset is inactive (SW_MCU_WARMRSTz = HIGH).

This bit field is reset to “1111” (Inactive State) by default.

Note

This software reset is equivalent to MCU_RESETz warm reset signal (MCU_RESETz HW Pin) functionality.

Top Level Domain Effect

All modules in the Top Level domain are reset except for MCU domain CTRLMMR bits which are reset only on MCU_PORz.

IOs are not affected.

R5FSS processor is reset.

When MCU_RESETz is de-asserted, the MCU domain needs to be reconfigured by the R5FSS (secondary boot loader) in the MAIN domain.

MAIN Domain Effect

All modules in the MAIN domain are reset except for CTRLMMR bits which are reset only on PORz.

IOs are not affected.

All processor cores are reset (SMS, and R5FSS).

When MCU_RESETz is de-asserted, the device goes through full boot. The reason for this reset is captured in CTRLMMR reset source register MCU_CTRL RST_SRC

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD and reconfigure the domains and R5FSS processor accordingly.

6.3.5.3 SMS Resets

6.3.5.3.1 SMS_WARM_OUT_RST_n Reset

Reset Overview

The SMS will issue this reset upon a security error.

When this reset is enabled in MAIN domain, it causes a MAIN domain warm reset.

This is a synchronous reset type (needs to complete reset isolation sequence).

Note

This reset behavior is same as the RESETz_REQ reset signal (RESET_REQz HW Pin).

Top Level Domain Effect

When Top Level domain is configured to operate independently, Top Level domain reset isolation sequence is completed before propagating the RESETz to main domain.

Top Level IOs are not affected.

When MCU domain is not configured as independent then, this reset will also warm reset MCU domain.

MAIN Domain Effect

This is a MAIN domain warm reset request. First, the reset isolation sequence is applied and then the reset is propagated.

All modules in MAIN domain are reset except for CTRLMMR register bits which are reset only on PORz.

IOs are not affected.

All processor cores are reset

Reason for this reset is captured in CTRLMMR reset source status register MCU CTRLMMR, and the reset isolation sequence status in the main_iso_done bit. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and reconfigure the domains and processor accordingly.

6.3.5.3.2 SMS_COLD_OUT_RST_n Reset

Reset Overview

This reset is a MAIN domain warm reset that is executed from the SMS. This is an asynchronous reset type (takes effect immediately). This SMS reset of the Main domain is enabled only when the SMS_COLD_RESET_EN_z bit in WKUP domain CTRLMMR is '0'.

Note

This reset behavior is same as the RESETz_REQ reset signal (RESET_REQz HW Pin) with the exception that it takes effect immediately without need for any reset isolation sequence.

Top Level Domain Effect

When the domain is configured to operate independently, the domain is configured as a safety domain, and the domain is reset isolated from Main domain resets.

Top Level IOs are not affected.

When the domain is not configured as independent then, this reset will also warm reset the domain.

MAIN Domain Effect

This is a MAIN domain asynchronous warm reset. Propagates immediately without any reset isolation sequence.

All modules in MAIN domain are reset except CTRLMMR register bits which are reset only on PORz.

IOs are not affected.

All processor cores are reset.

Reason for this reset is captured in CTRLMMR reset status register.

6.3.5.4 VTM Thermal Alert Reset

Reset Overview

The VTM module outputs an alert signal (THERM_MAXTEMP_OUTRANGE_ALERT), when the device temperature goes beyond a maximum threshold.

This reset signal is used to warm reset the whole device which will cause a device warm reset similar to MCU_RESETz.

VTM alert will be active as long as the error condition (Device Temperature > Maximum Temperature Threshold) is still TRUE.

When the error goes away, VTM alert will be de-asserted and device will come out of warm reset.

VTM Over-Temp alert signal is connect to Reset Request input of Main and MCU PLLCTRL. This reset is non-blockable VTM Over-Temp alert also causes ESM error pin to trigger.

Additional Reset Details - VTM Alert Use-Case Example

VTM sends out a warning signal before generating the Max Temp Alert.

There are 2 different threshold settings for max temperature limits.

The first one has a lower threshold which will generate an interrupt to the processor for taking action to reduce frequency, turn-off power domains, etc. This should eventually lower the temperature and avoid the Max Temp Alert.

If the interrupt does not fix the rising temperature, then VTM will issue a Max Temp Alert. This will cause a device warm reset. The VTM Max Temp Alert will be active as long as die temperature is above the programmed threshold.

Device warm reset will default certain power domains to off mode (default at power-up). This should eventually lower the die temperature further.

Software can read the reset status register to poll on the cause of the warm reset. If it is from VTM, then it can wait for additional time before turning on the power domains.

6.3.5.5 ESM Error Reset

Reset Overview

ESM modules in the Top Level domain and Main domains can be configured to trigger ESM error pin on critical error conditions. MCU_ESM's reset is triggered when the high prioty interrupt or configuration error interrupts is asserted. Similarly, MAIN_ESM's reset is triggered when the MCU ESM High priority interrupt on configuration error interrupt is asserted. These ESM resets can be enabled by configuring either of these MCU MMR CTRL MCU_ESM_ERROR_RST_ENz and WKUP MMRT CTRL MAIN_ESM_ERROR_RST_ENz MMR bits to 0.

MCU_ERRORn Pin

The MCU_ERRORn pin indicates the MCU domain ESM status. The output signals to an external agent that it needs to (or may need to) intervene because of an error. The Error Pin Output is active Low or PWM, based on the ESM Error Pin Control register pwm_en field. The field should only be modified when the ESM is disabled, based on the Global Enable register.

While in Power-On-Reset, the Error Pin is active (assert low). SoC drives a Low via a weak internal pull-down. After Power-On-Reset condition is removed, ESM will drive the Error Pin. During a warm reset, the state of the error pin is unchanged.

When MCU_ERRORn output pin is configured to operate in a level mode, a LOW indicates the MCU_ESM module has registers as error. A HIGH indicates that there are no MCU_ESM errors. When the pin is configured to operate in PWM mode, no error is indicated by continuous toggle according to programmable MMR with for high and low periods. When an error occurs, the error pin stops toggling and remain constant until the error is clear. An external device that is detecting the PWM toggles can identify the error if the pin stops toggling. The periods should be programmed such that they fit within the expectation of the external device

6.3.5.6 HHV

IOs support HHV mode during power up. HHV is active when PORz signal is driven LOW.

HHV allows IO cells to be tri-stated and is an IO feature. All IO cells have HHV which is asserted (driven) by HHV generated during PORz assertion. There are default pull values during this HHV/PORz assertion specified in the device Datasheet for each pin. All HHV logic controlling the buffer output enable and associated default internal pull for each IO will be applied.

HHV Timing Diagram demonstrates the timing sequence for the device HHV signals.

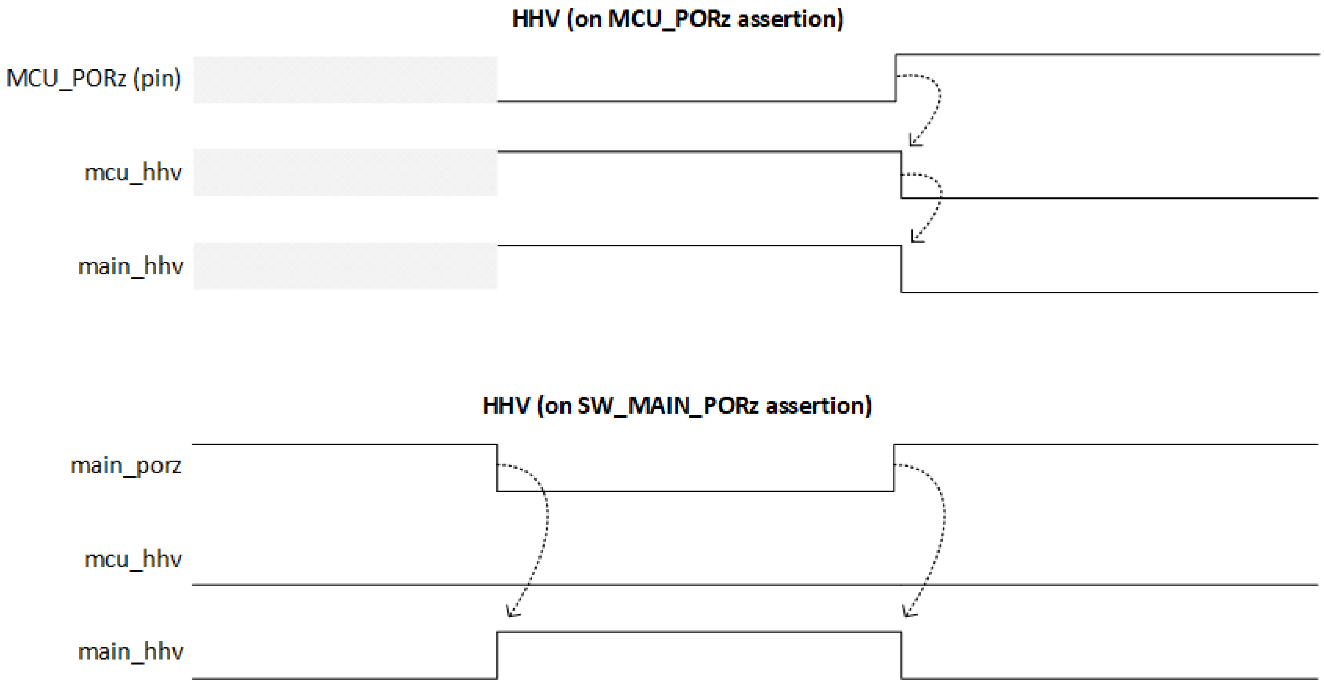
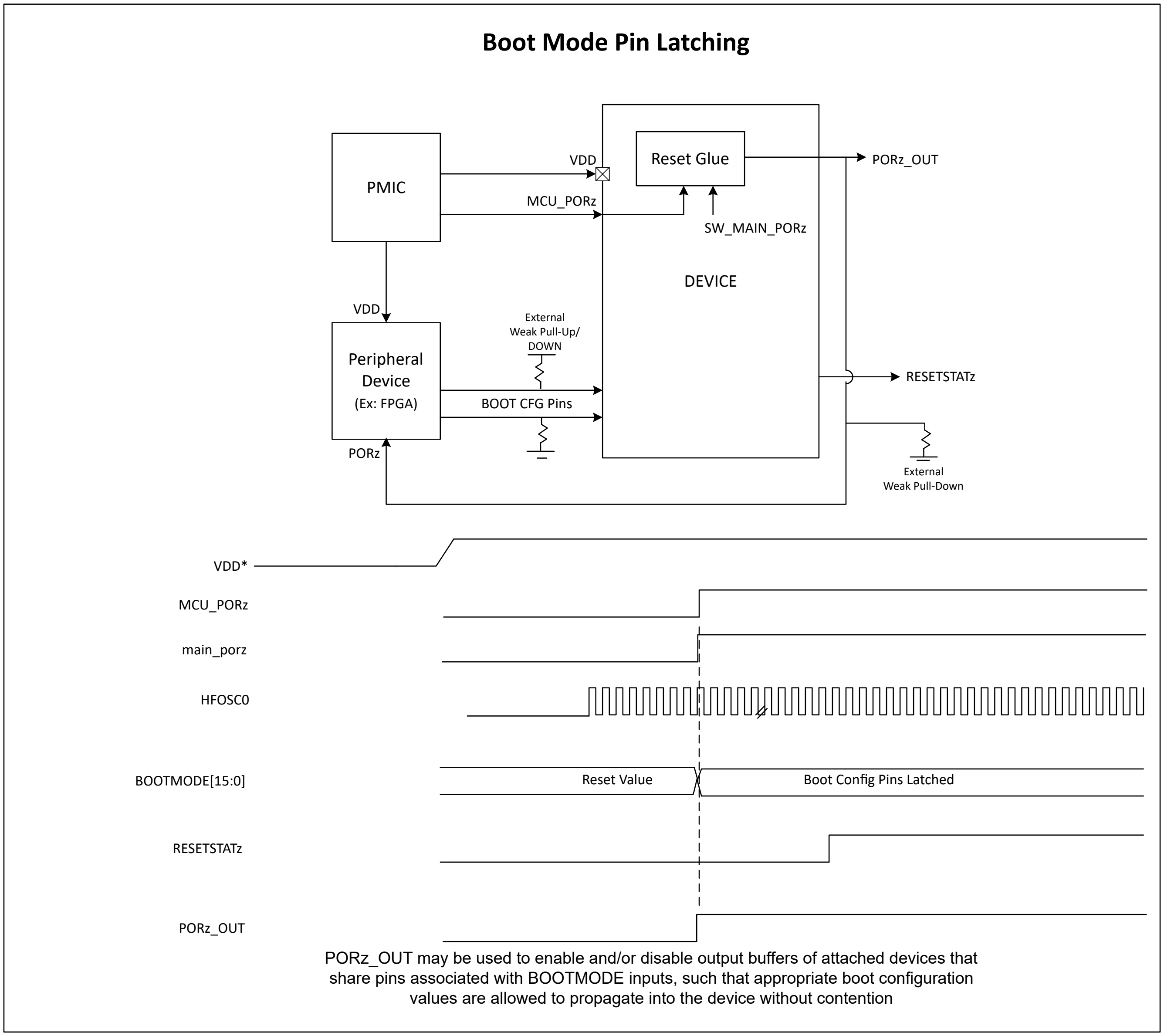


Figure 6-17. HHV Timing Diagram

6.3.5.7 BOOTMODE Pin Latching

This device requires several Boot Mode controls to enable device boot. The BOOTMODE inputs are not implemented on dedicated pins. They are multiplexed with other signal functions, where pins associated with the BOOTMODE inputs are defined in the Pin Attributes table. The logic state of the BOOTMODE inputs are latched on the rising edge of PORz_OUT. Valid logic states must be maintain as long as PORz_OUT is held low. The latched values are reflected in WKUP CTRL MMRs for read/write access.



PORz_OUT may be used to enable and/or disable output buffers of attached devices that share pins associated with BOOTMODE inputs, such that appropriate boot configuration values are allowed to propagate into the device without contention

Figure 6-18. BOOTMODE Pin Latching

6.3.5.8 Power-on-Reset Sequence

The below images give a high-level overview of the device power-up sequence.

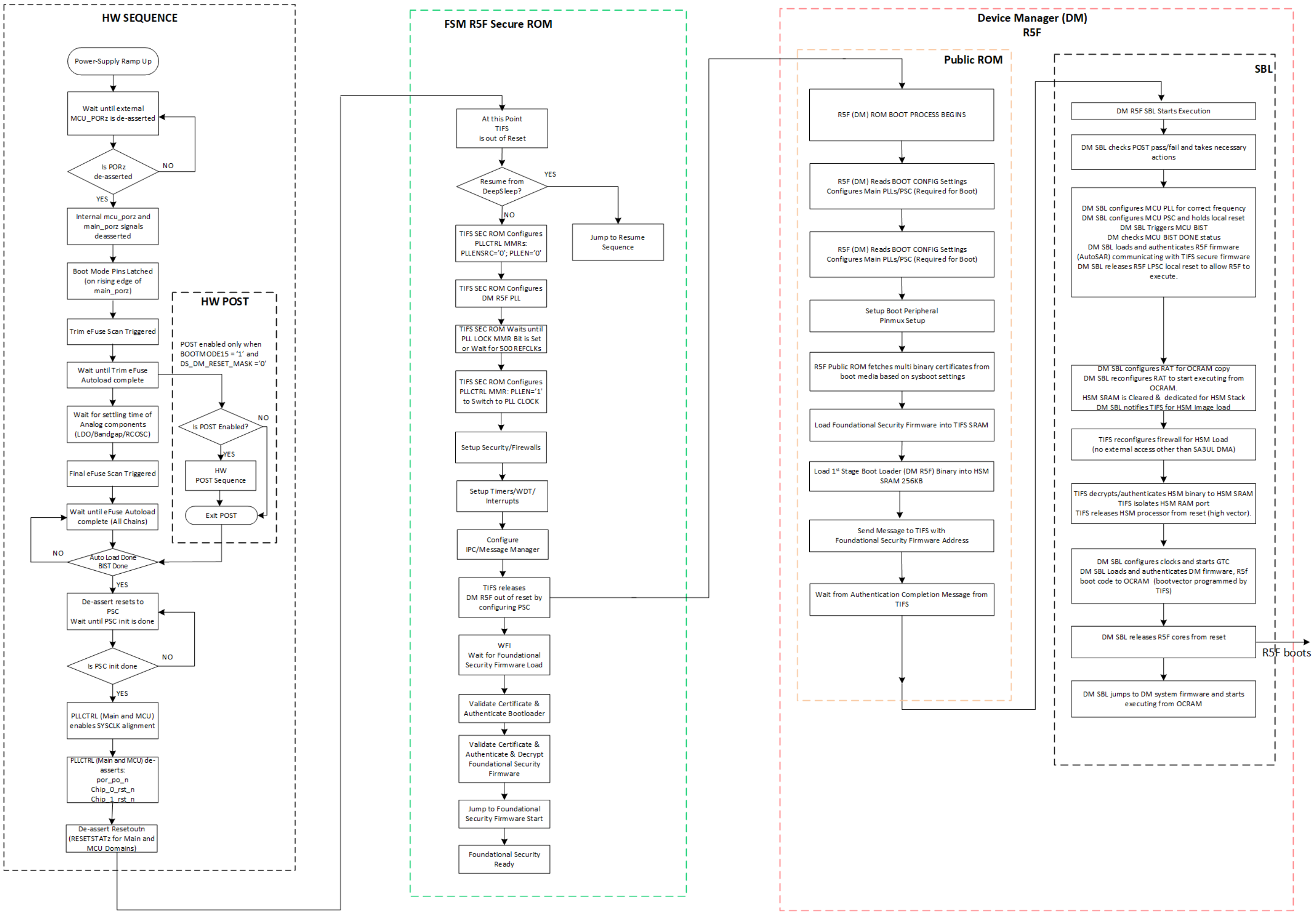


Figure 6-19. Power Up Flow

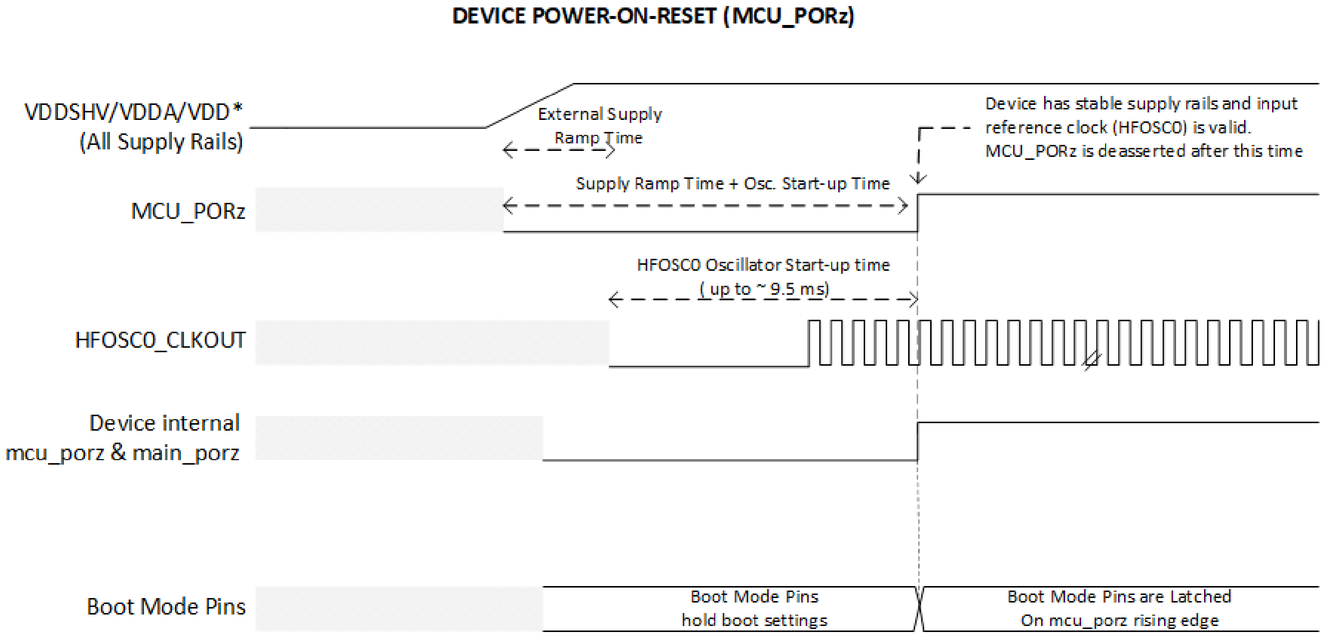


Figure 6-20. At Power Up

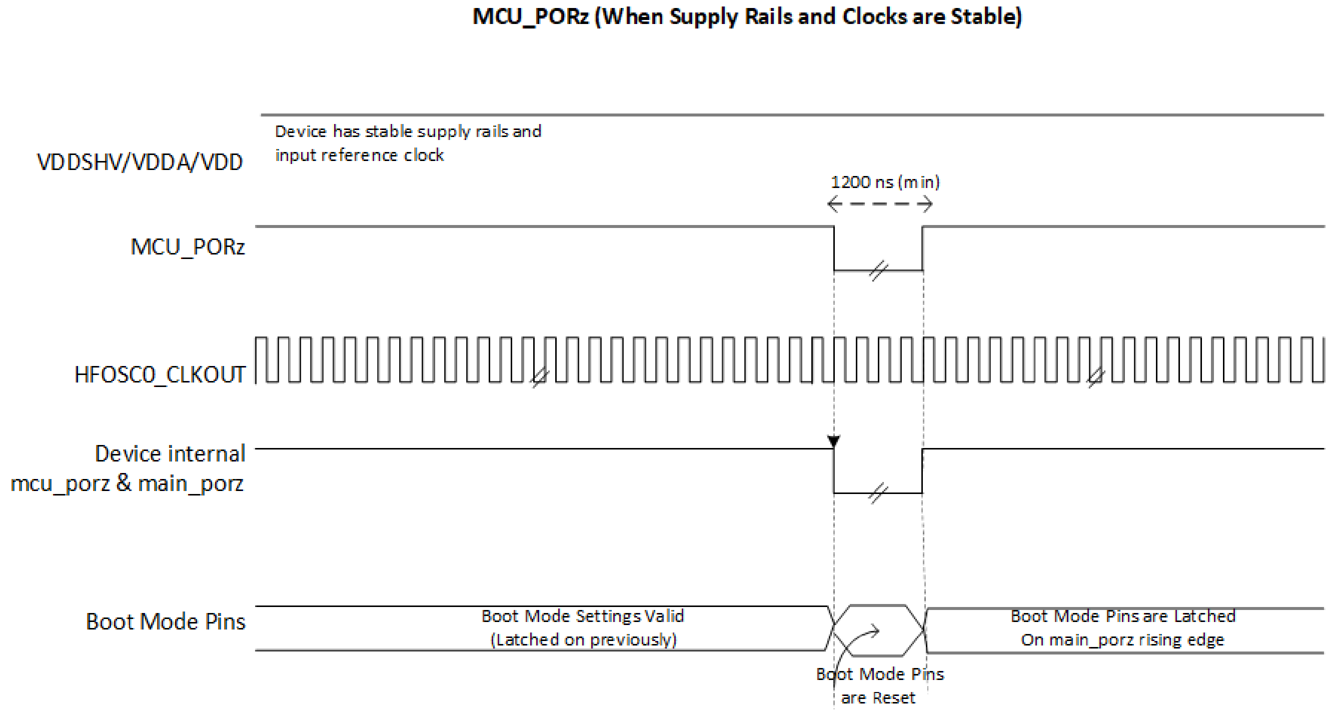


Figure 6-21. After Power Up

6.3.5.9 Low Power Mode Reset Handling

This device supports IORET mode. To support this mode, the device is partitioned (seen below) so that the WKUP Domain is active and can bring the device out of IORET mode. PORz will be asserted in MAIN Domain while in IORET mode.

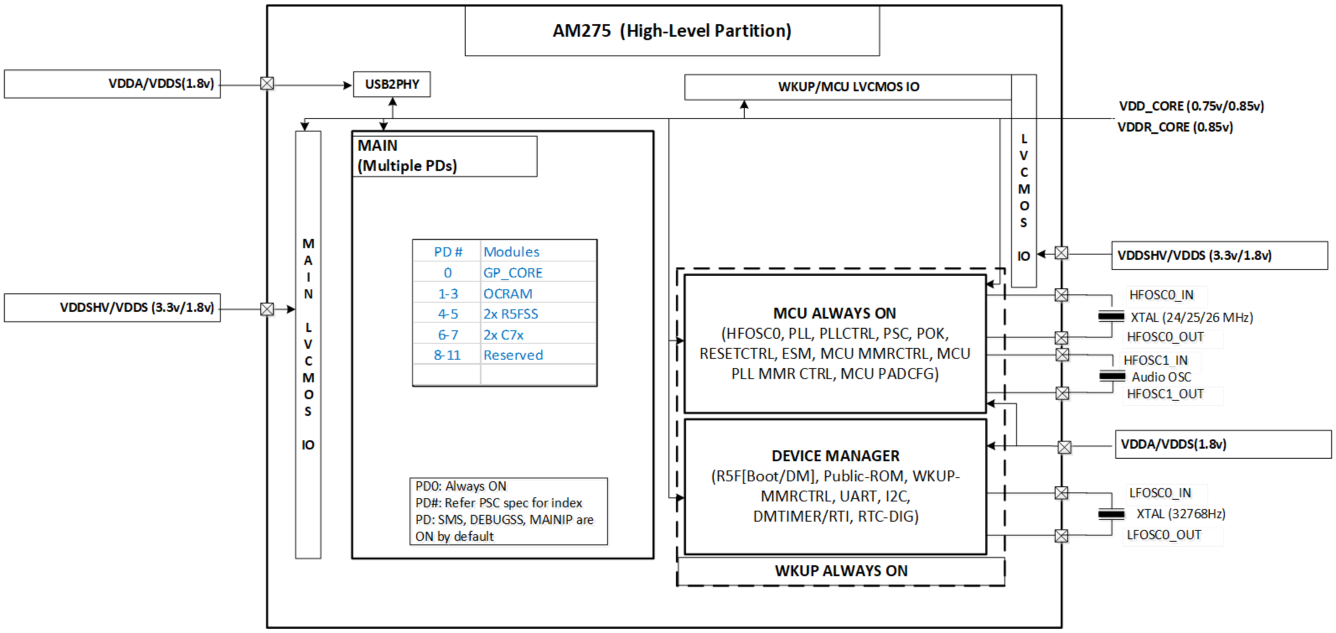


Figure 6-22. Reset Partition View

6.4 Clocking

This chapter describes the clock architecture of the device.

6.4.1 Overview

To satisfy the various subsystems requirements, the device features multiple clock sources and clock generators:

- External Crystal Driver
- Internal Oscillator
- Phase-Locked Loop circuits (PLLs)
- Dividers

Top-Level Clock Diagram shows the device top-level clock diagram. The clocking is divided into three domains, WKUP Domain, Top Level Domain, and Main Domain

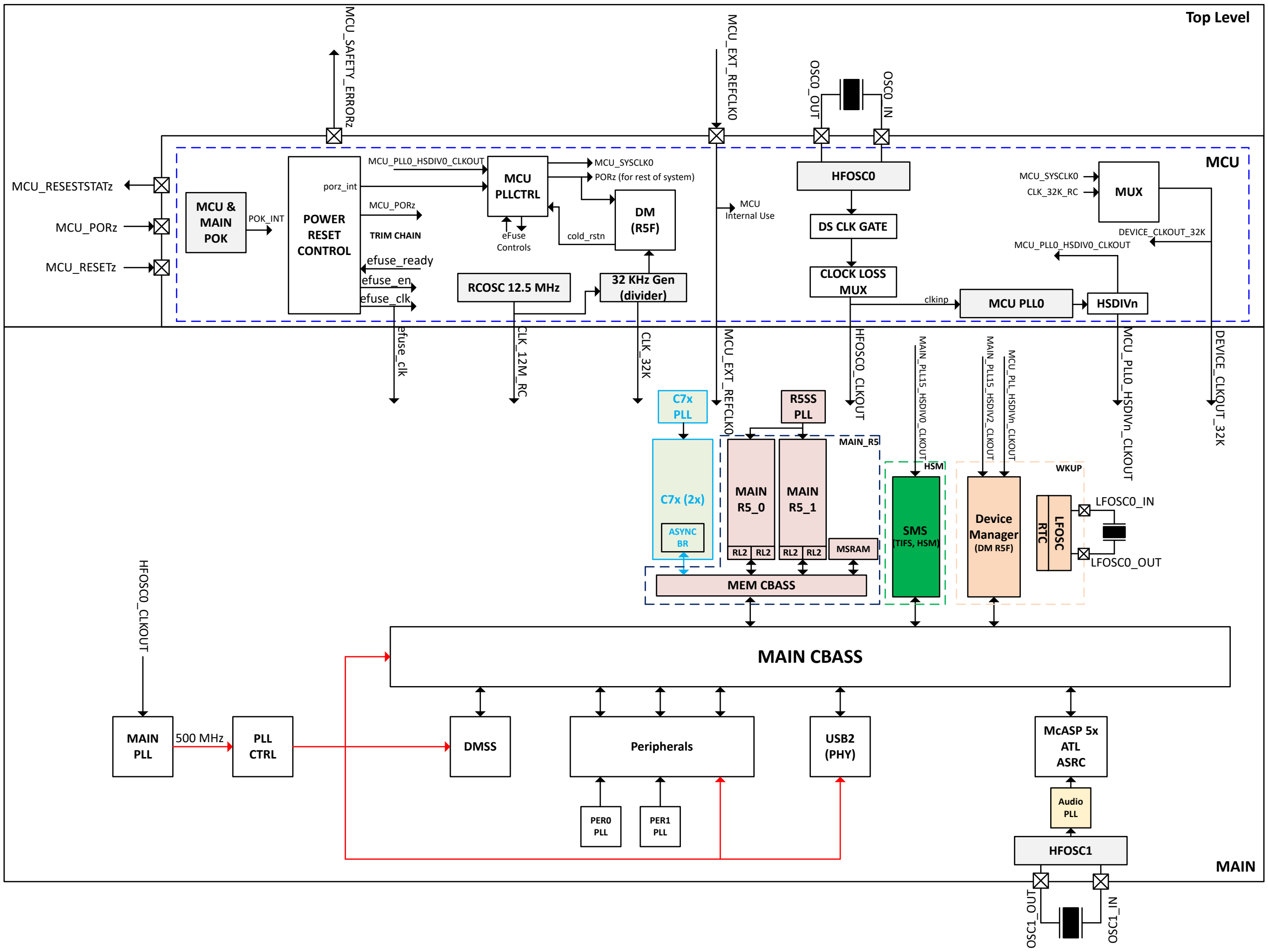


Figure 6-23. Top-Level Clock Diagram

6.4.2 Clock Inputs

6.4.2.1 Overview

Various external clock inputs are needed to drive the device. Summary of these input clock signals is as follows:

- High frequency oscillators
  - HFOSC0 — the primary system oscillator of the device, and the oscillator is located in the Top Level Domain
  - HFOSC1— An auxiliary oscillator that supports audio specific crystal frequencies. The oscillator is located in the Top Level Domain
- Low frequency oscillators
  - LSOSC0:— external 32.768KHz crystal interface pins to provide an accurate low frequency clock for use during lower power modes.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — optional external system clock input (Top Level domain).
  - EXT_REFCLK1— optional external system clock input (MAIN domain).
- External CPTS reference clock inputs
  - CP_GEMAC_CPTS0_RFT_CLK — CPTS reference clock input for CPSW and Timers in MAIN.
- External audio reference clock inputs/outputs
  - AUDIO_EXT_REFCLK[2:0] — optional McASP high-frequency input clocks when configured to operate as an input.

Note

Other clock inputs that are routed directly to the subsystems are described in the respective subsystem chapters.

6.4.3 Clock Outputs

The device provides several system clock outputs. Summary of these output clock signals is as follows:

- MCU_OBSCLK0 - Used as clock reference for external Ethernet
- OBSCLK[1:0] -Can be used as a reference for external audio device
- WKUP_CLKOUT0 - Used as WIFI clock source
- CLKOUT0 - Used as RMII reference clock

6.4.3.1 Observation Clock Pins

6.4.3.1.1 MCU_OBSCLK0 Pin

MCU_OBSCLK0 output is controlled by MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL register in the MCU_CTRL_MMR0 module; for more information about control registers, refer to *CTRL_MMR Registers*. Two muxes are connected in series - MCU_OBSCLK0_MUX0 and MCU_OBSCLK0_MUX1, see *MCU_OBSCLK Muxes Diagram*.

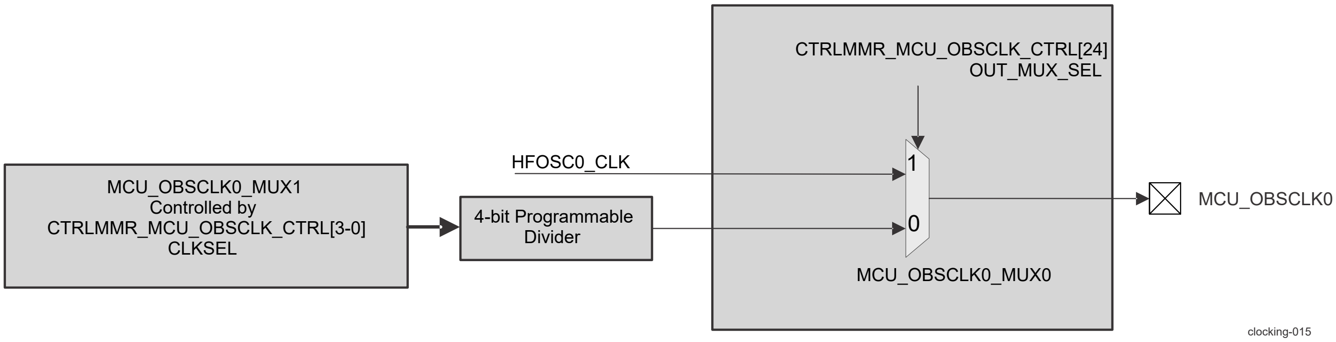


Figure 6-24. MCU_OBSCLK Muxes Diagram

How to select the output of MCU_OBSCLK0_MUX1 is described in *MCU_OBSCLK0_MUX1 Output Clock Selection*.

Table 6-21. MCU_OBSCLK0_MUX1 Output Clock Selection

MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL(2)[3-0] CLK_SEL	MCU_OBSCLK0_MUX1 Output Clock Selection(1)
0x0	MCU_CLK_12M_RC
0x1	0 (GND)(3)
0x2	MCU_PLL0_HSDIV0_CLKOUT
0x3	MCU_PLL0_HSDIV4_CLKOUT
0x4	MCU_PLLCTRL_OBSCLK_CLK
0x5	CLK_32K_RC
0x6	HFOSC0_CLKOUT
0x7	MCU_HFOSC0_CLKOUT_32K
0x8	MCU_SYSCLK0
0x9	DEVICE_CLKOUT_32K
0xA-0xF	RESERVED(3)

(1) Software-controlled 4-bit divider is used to obtain the divided versions of the clocks passed to MCU_OBSCLK1 mux
(2) For more information about control registers, refer to *CTRL_MMR Registers*.
(3) GND - ground

The value of the software-controlled 4-bit divider is determined by the MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL[11-8] CLK _DIV field; for more information about control registers, see *CTRL_MMR Registers*.

Note

MCU_OBSCLK1_MUX0 is provided as a low jitter output for HFOSC0_CLK. In this configuration, MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL[3-0] should be configured as 0x1 (1, selecting a logical low signal) and MCU_CTRL_MMR_CFG0_MCU_OBSCLK_CTRL[24] should be configured as 0x1.

6.4.3.1.2 OBSCLK0 Pin

The OBSCLK0 output pin is controlled by MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL register in the CTRL_MMR0 module; for more information about control registers, refer to *CTRL_MMR Registers*. Figure 6-25 shows a block diagram of internal OBSCLK0 mux connections.

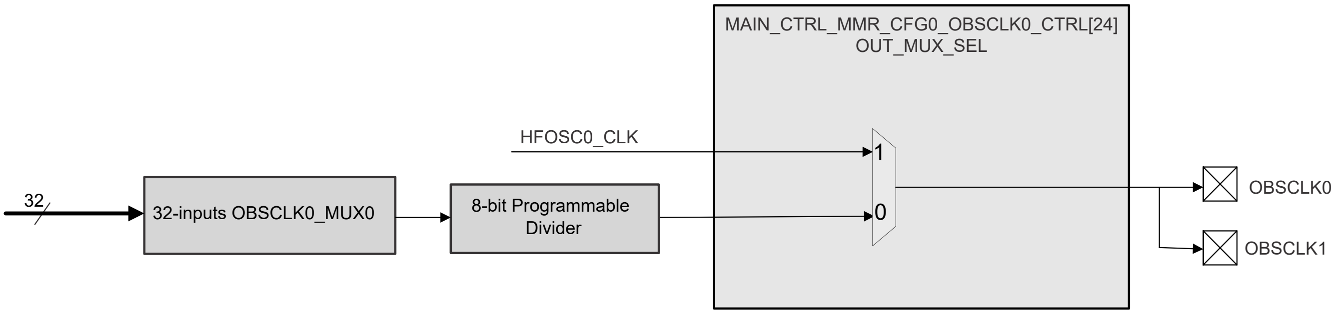


Figure 6-25. OBSCLK0 Muxes Diagram

Table 6-22. OBSCLK0 Clock Selection

MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL(2)[4-0] CLK_SEL	OBSCLK0 Selection (1)
0x0	MAIN_PLL0_HSDIV0_CLKOUT
0x1	MAIN_PLL1_HSDIV0_CLKOUT
0x2	MAIN_PLL2_HSDIV0_CLKOUT
0x3	MAIN_PLL4_HSDIV0_CLKOUT
0x4	MAIN_PLL14_HSDIV0_CLKOUT
0x5	CLK_12M_RC
0x6	HFOSC0_CLKOUT_32K
0x7	PLLCTRL_OBSCLK
0x8	HFOSC0_CLKOUT
0x9	CLK_32K_RC
0xA	CPSW0_CPTS_GENF0
0xB	CPSW0_CPTS_GENF1
0xC	MCU_PLL0_HSDIV0_CLKOUT
0xD	MAIN_PLL15_HSDIV0_CLKOUT
0x10	MAIN_SYSCLK0
0x11	DEVICE_CLKOUT_32K

(1) Software-controlled 8-bit divider is used to obtain the divided versions of the clocks passed to output pins
(2) For more information about control registers, refer to *CTRL_MMR Registers*.

The value of the software-controlled 8-bit divider is determined by register MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL[15-8] CLK_DIV; for more information about control registers, refer to *CTRL_MMR Registers*.

6.4.3.2 System Clock Pins

6.4.3.2.1 MCU_SYSCLKOUT0

MCU_SYSCLK0 is divided by 4 and then send out of the device as a LVCMOS clock signal (MCU_SYSCLKOUT0). This signal can be used to test if the specific device clock is functioning or not.

Note

MCU_SYSCLKOUT0 cannot be used as a clock source for external devices on the board.

6.4.3.2.2 SYSCLKOUT0

SYSCLK0 is divided by 4 and then send out of the device as a LVCMOS clock signal (SYSCLKOUT0). This signal can be used to test if the specific device clock is functioning or not.

Note

SYSCLKOUT0 cannot be used as a clock source for external devices on the board.

6.4.3.2.3 WKUP_CLKOUT0

The WKUP_CLKOUT0 output pin is controlled by the WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL register in the WKUP_CTRL_MMR0 module; for more information about control registers, refer *CTRL_MMR Registers*. The following diagram shows a block diagram of internal WKUP_CLKOUT0 mux connections.

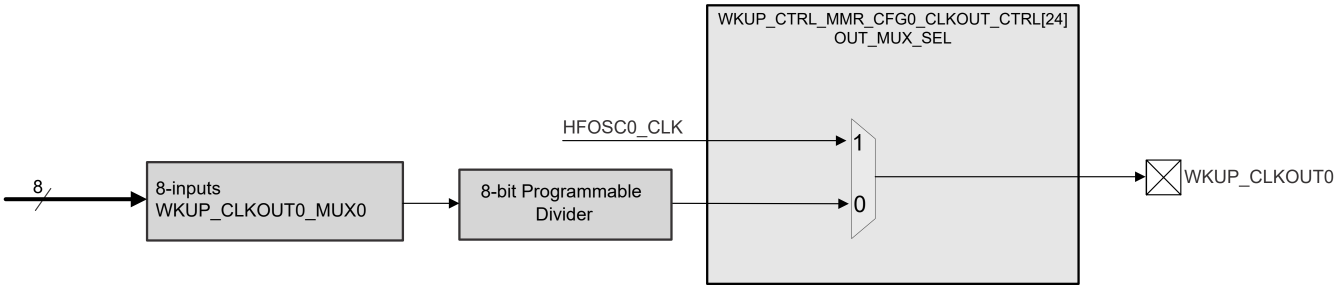


Figure 6-26. WKUP_CLKOUT0 Mux Diagram

Table 6-23. WKUP_CLKOUT0_MUX Output Clock Selection

WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL[2][2-0] WKUP_CLKOUT_SEL	WKUP_CLKOUT0_MUX Output Clock Selection[1]
0x0	0
0x1	LFOSC0_CLKOUT
0x2	MAIN_PLL0_HSDIV2_CLKOUT
0x3	MAIN_PLL1_HSDIV2_CLKOUT
0x4	MAIN_PLL2_HSDIV9_CLKOUT
0x5	DEVICE_CLKOUT_32K
0x6	CLK_12M_RC
0x7	HFOSC0_CLKOUT

(1) Software-controlled 8-bit divider is used to obtain the divided versions of the clocks passed to output pins.
(2) For more information about control registers, refer to *CTRL_MMR Registers*.

6.4.4 Device Oscillators

The device has the possibility to source clocks of an external high-frequency oscillator - HFOSC0 and external 32.768KHz oscillator - LFOSC0. The device has also one internal RC oscillator - CLK_12M_RC.

6.4.4.1 Device Oscillators Integration

6.4.4.1.1 High-Frequency Oscillator with External Crystal

By default, HFOSC0 is enabled after PORz. It supports a bypass mode. In this mode, an external clock can be driven on the XI Pin.

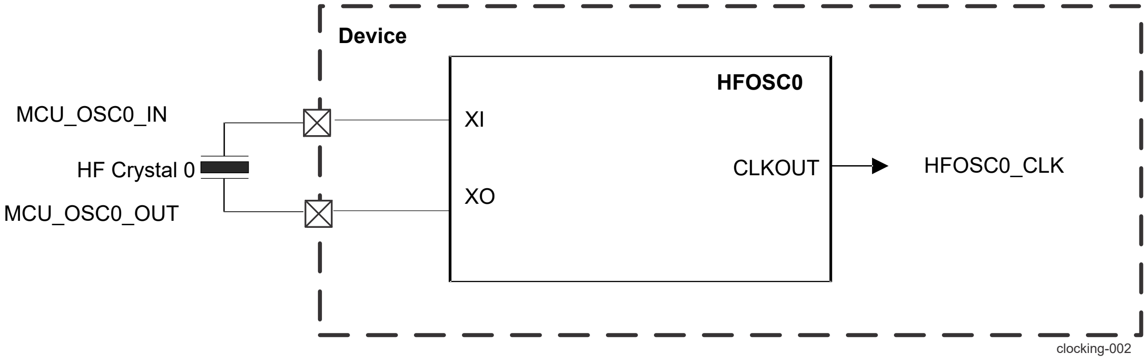


Figure 6-27. HFOSC0 Integration Diagram

6.4.4.1.2 Low-Frequency Oscillator with External Crystal

By default, LFOSC0 is disabled after PORz. It supports a bypass mode. In this mode, an external clock can be driven on the XI Pin.

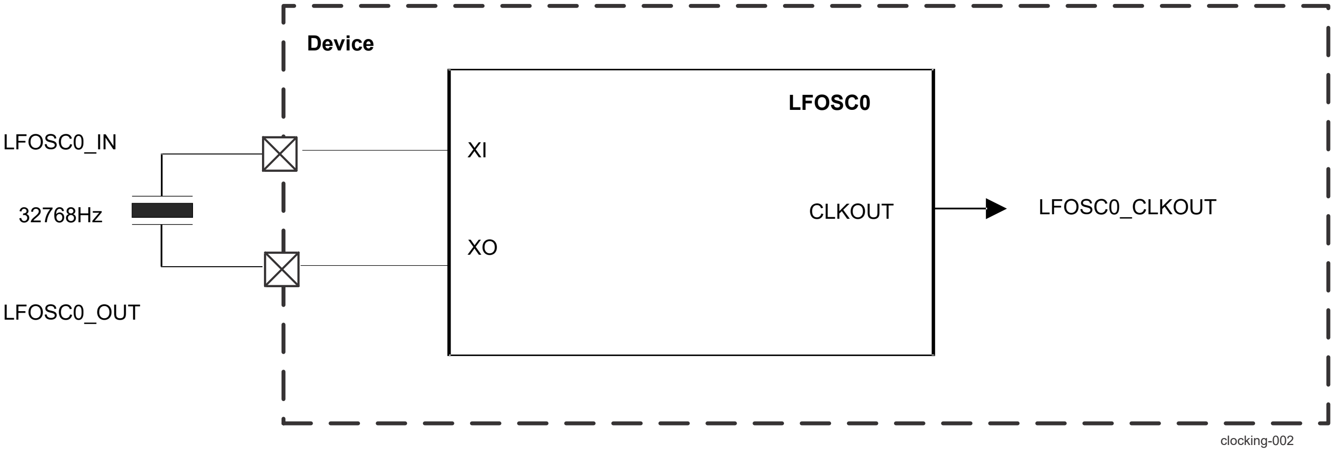


Figure 6-28. LFOSC0 Integration Diagram

6.4.4.1.3 Internal RC Oscillator

CLK_12M_RC in always oscillate mode.

The 12.5-MHz RC clock output (CLK_12M_RC) is used by the on-chip Reset Glue logic, Power Reset Generator (PRG) circuits, HFOSC0 Loss Circuits, Dual Clock Comparator (DCC) and Timer Modules.

Note

An output clock of CLK_12M_RC is further divided down to generate a 32-kHz clock (CLK_32K_RC). This clock is used by SMS and Timer Modules.

The actual value of the derived CLK_32K_RC will vary with PVT variations.

6.4.4.2 Oscillator Clock Loss Detection

The device supports HFOSC0 clock loss circuitry to detect when HFOSC0_CLK stops toggling. Dedicated hardware logic monitors HFOSC0 clock using CLK_12M_RC clock. When HFOSC0_CLK stops toggling for 9 CLK_12M_RC clock periods, a HFOSC0 clock stop loss condition is detected. If CTRLMMR_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN is set , the reference clock is switched from HFOSC0_CLKOUT to CLK_12M_RC to allow the device to operate with a slower clock. The HFOSC0_CLK clock loss condition is reported as an error to MCU_ESM0 regardless of the value of MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN. Integration diagram of HFOSC0 clock loss detection is presented in Figure 6-29.

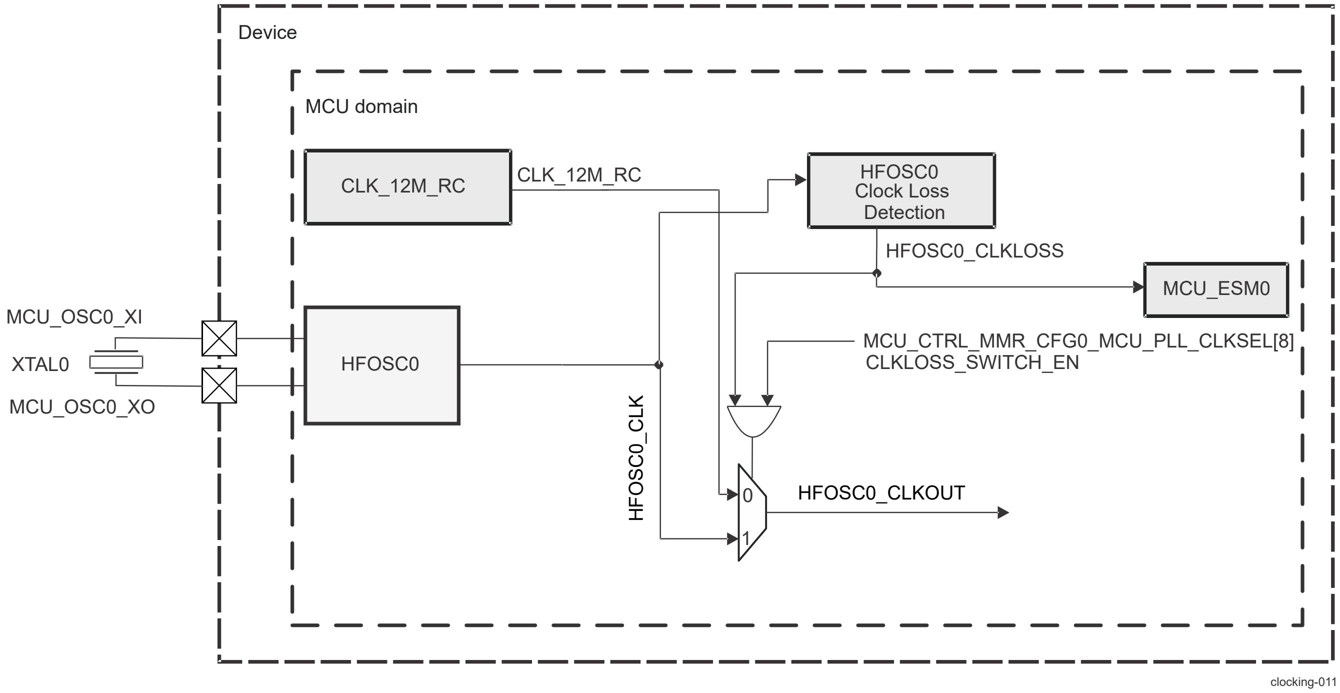


Figure 6-29. HFOSC0 Clock Loss Detection Integration Diagram

MCU_ESM0 can optionally generate an interrupt to MCU_R5FSS and DM_R5FSS0 so they can save some critical contents such as error logging to scratch pad memory or external flash. ESM must also be configured to report this error on the MCU_ERRORn pin.

HFOSC0 clock loss is a catastrophic failure since this clock is the most critical system clock. During the clock loss condition an external system intervention is required.

The clock loss mux is not a glitch free mux. The mux control is synchronized to the CLK_12M_RC clock. Since HFOSC0_CLK has stopped switching the mux should transition to RC Clock without producing glitches.

During clock-loss condition, the device reports the error to the external device through MCU_ERRORn pin - the pin is driven Low. The recovery mechanism is up to the external system (such as a PMIC to take action). For example, it can try a full system power cycle to see if the system recovers. If the system does not recover then, it has to take some other action such as to check system clocks, external crystal or supply rails.

Device PLLs will lose lock when clock loss is detected. During this time 12.5-MHz RC clock is output through the bypass muxes. The PLL will relock to a new frequency based on 12.5 MHz RC clock.

In an event of clock glitch which may potentially hang the device, then the SMS watchdog timer will expire and will generate an internal reset for the whole device.

6.5 PLLs

Phase-Locked Loop circuits (PLLs) in the device are clock generator PLLs, which multiply the lower-frequency reference clock up to the operating frequency of the respective subsystem(s).

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

6.5.1 MAIN Domain PLLs Overview

The following are the PLLs in the device in MAIN domain:

- PLL0 (MAIN PLL)
- PLL1 (PER0 PLL)
- PLL2 (PER1 PLL)
- PLL4 (Audio PLL)
- PLL7 (C7x PLL)
- PLL14 (R5SS PLL)
- PLL15 (SMS PLL)

Overview of the device PLLs with the reference clock options in MAIN domain is shown on *MAIN Domain PLLs Integration*. For more specific information about PLLs see *PLLs Device-Specific Information*.

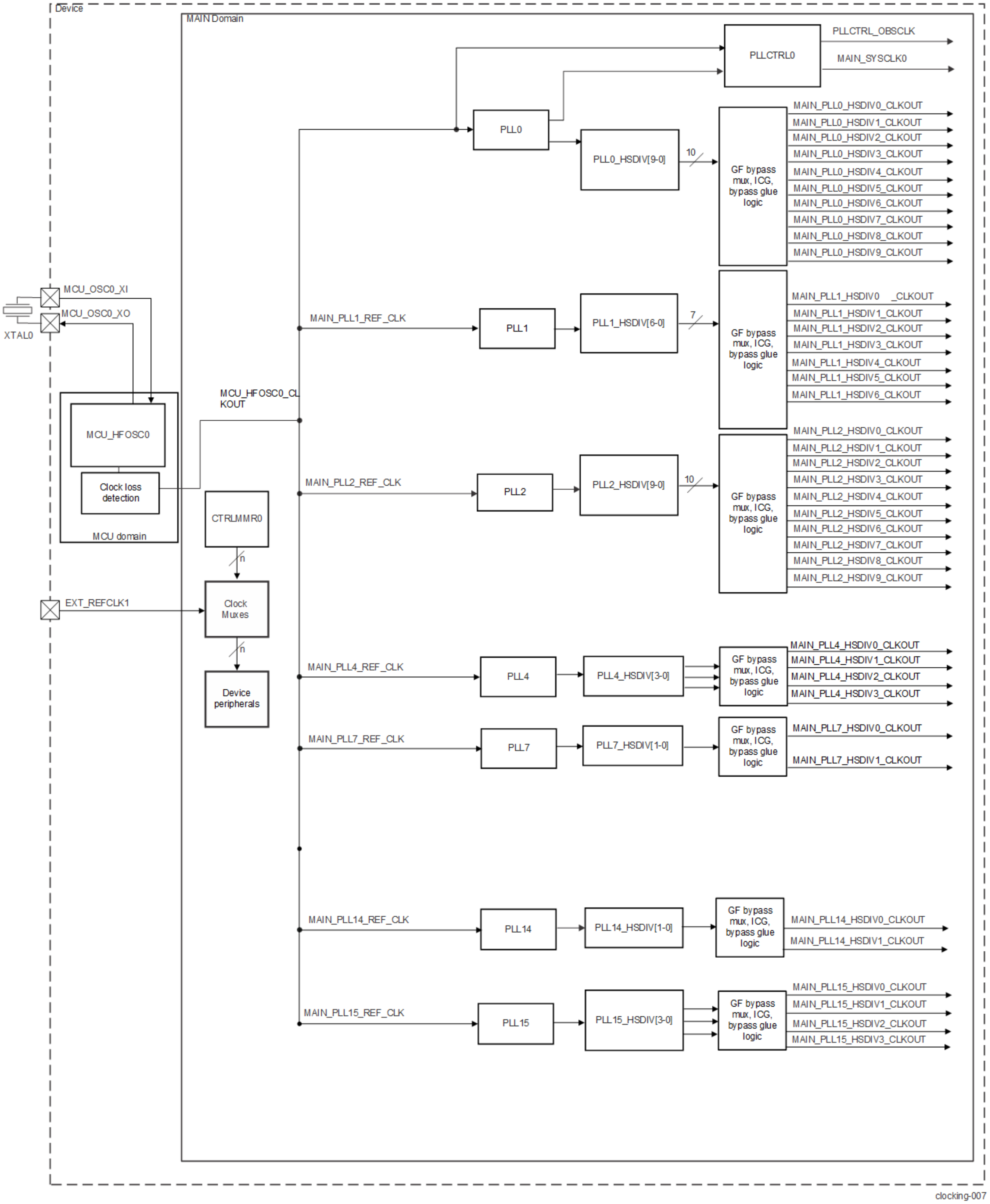


Figure 6-30. MAIN Domain PLLs Integration

Note

The external muxes of choosing the reference clocks are glitch-free muxes.

Note

MAIN_PLL0_HSDIV3, MAIN_PLL2_HSDIV7, MAIN_PLL14_HSDIV1, MAIN_PLL15_HSDIV3 are reserved on the device.

6.5.2 Top Level Domain PLL Overview

MCU_PLL0 (MCU PLL) with MCU_PLLCTRL0 are present in the device in the Top Level domain. An overview is shown on *Top Level Domain PLL Integration*. For more specific information about PLLs see, *PLLs Device-Specific Information*.

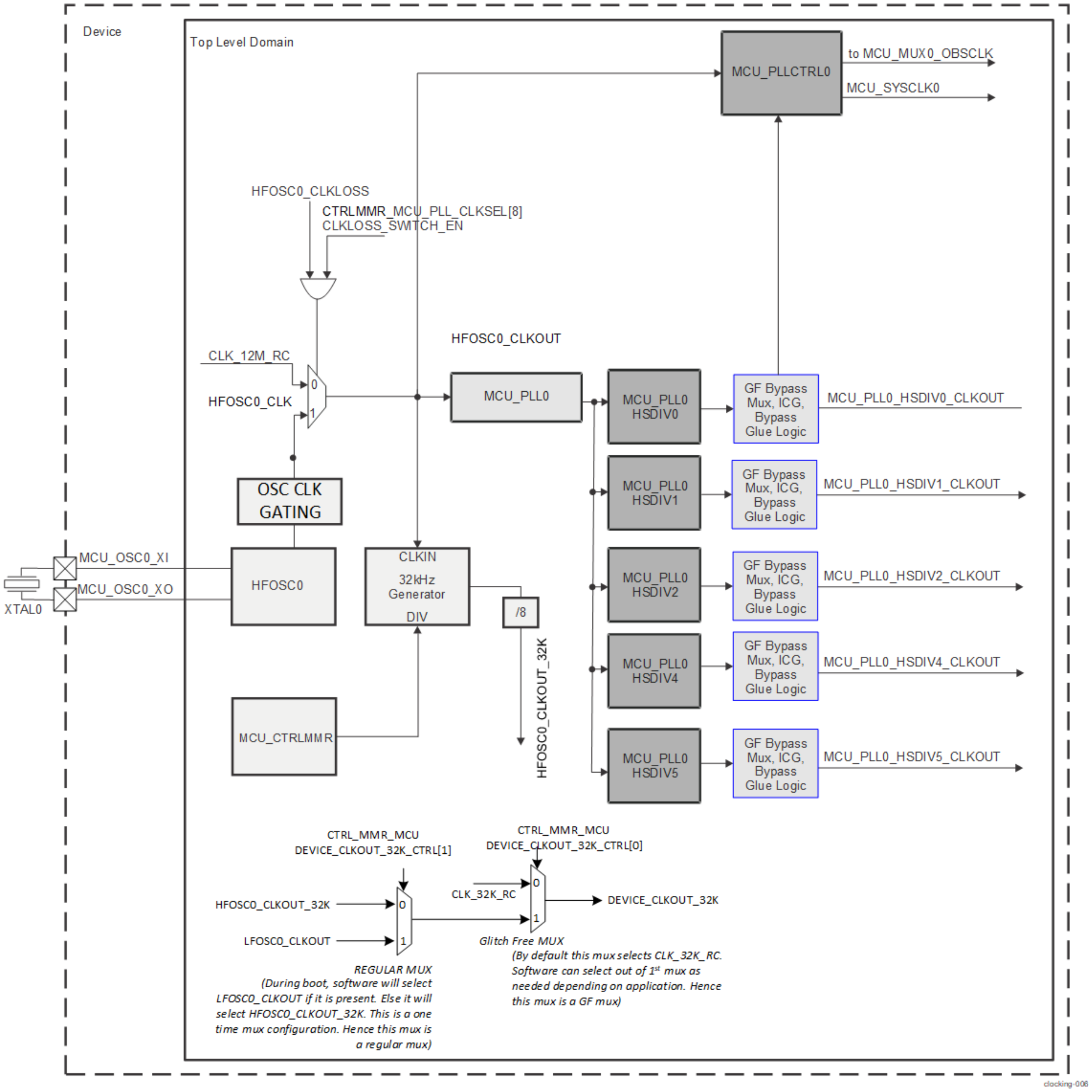


Figure 6-31. Top Level Domain PLL Integration

6.5.3 PLL Reference Clocks

6.5.3.1 PLLs in Top Level Domain

The reference clock MCU_PLL0_REF_CLK for the PLL in MCU domain is chosen between the internal high-frequency (HF) oscillator with external crystal (HFOSC0) and 12.5-MHz free-running RC oscillator. The selection is made through MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL[8] MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN, see *PLL Top Level Domain Reference Clock Selection*.

Table 6-24. PLL MCU Domain Reference Clock Selection - HFOSC0_CLKOUT Selection

MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL(1)[8] MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN	MCU_PLL0_REF_CLK
0 (default)	HFOSC0_CLK

Table 6-24. PLL MCU Domain Reference Clock Selection - HFOSC0_CLKOUT Selection (continued)

MCU_CTRL_MMR_CFG0_MCU_PLL_CLKSEL[1][8] MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN	MCU_PLL0_REF_CLK
1	CLK_12M_RC if clock loss is detected or HFOSC0_CLK if clock loss is not detected

[1] For more information about control registers, see *Control Module (CTRL_MMR)*.

6.5.3.2 PLLs in MAIN Domain

Each PLL in MAIN domain has a dedicated register, MAIN_CTRL_MMR_CFG0_MAIN_PLL**n**_CLKSEL, where n = 0, 1, 2, 4, 7, 14, 15.

6.5.4 Generic PLL Overview

To generate high-frequency clocks, the device supports multiple on-chip PLLs controlled directly by the Top-level Clocking. Their type is Fractional PLL with Calibration (PLLTS16FFCLAFRACF2).

Note

This chapter discusses only the PLLs that are directly controlled by the Top-level Clocking. The other PLLs embedded in and managed by other subsystems are described in their respective subsystems.

6.5.4.1 PLLs Output Clocks Parameters

Figure 6-32 shows the functional architecture of a generic PLL for PLLTS16FFCLAFRACF2 type.

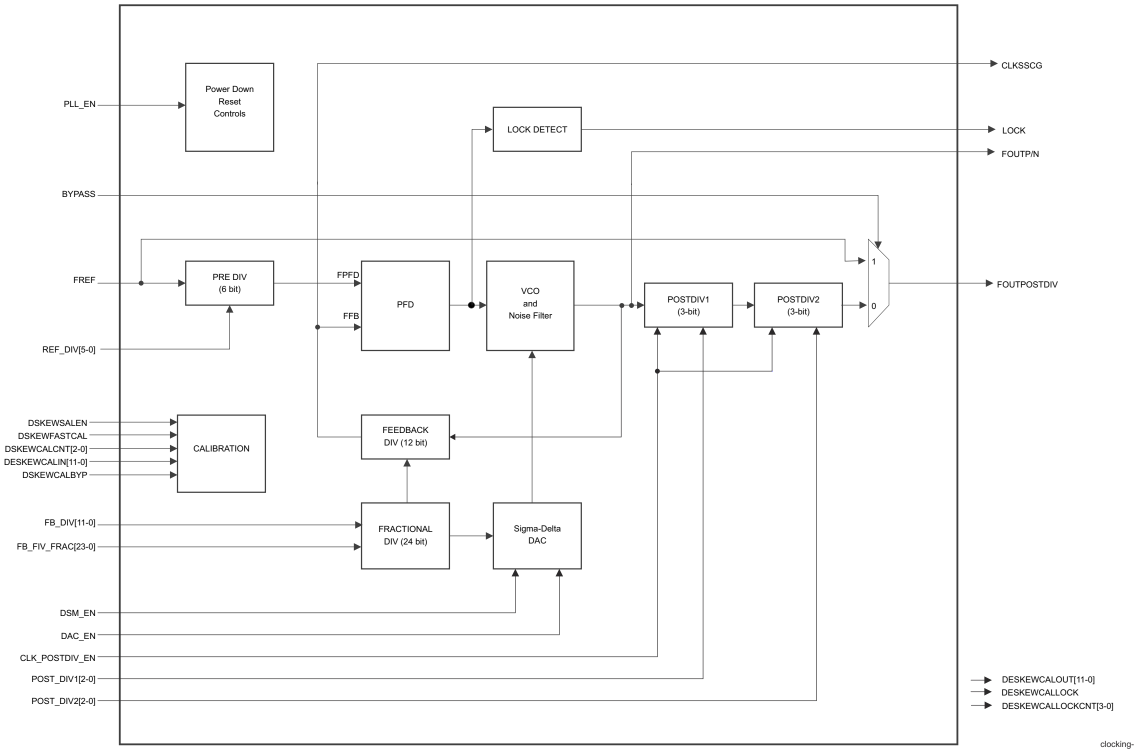


Figure 6-32. Generic PLL Functional Diagram for PLLTS16FFCLAFRACF2 Type

6.5.4.1.1 PLLs Input Clocks

As shown in Figure 6-32 the reference clock (FREF) input is used to generate the synthesized clock, but can also be used as the bypass clock for some outputs of the PLL whenever the PLL enters bypass mode. It is mandatory for the PLL clock synthesis.

6.5.4.1.2 PLL Output Clocks

6.5.4.1.2.1 PLLTS16FFCLAFRACF2 Type Output Clocks

Table 6-25 describes the output clocks of PLLTS16FFCLAFRACF2.

Table 6-25. PLLTS16FFCLAFRACF2 Output Clocks

Output	Description	Frequency
FOUTP	Positive phase VCO output (no post divider)	(FREF / REF_DIV) * (FB_DIV + FB_DIV_FRAC)
FOUTN	Negative phase VCO output (no post divider)	(FREF / REF_DIV) * (FB_DIV + FB_DIV_FRAC)
FOUTPOSTDIV	VCO-divided clock output.	FOUTP / (POST_DIV1*POST_DIV2)
CLKSSCG	Clock to SSMOD	(FREF / REF_DIV)

Where:

- REF_DIV is the software-configured division ratio binary value.
- FB_DIV is the software-configured division ratio binary value.
- FB_DIV_FRAC is the software-configured fractional division.
- POST_DIV1 is the software-configured division ratio binary value.
- POST_DIV2 is the software-configured division ratio binary value.

Note

POST_DIV1 and POST_DIV2 valid values are from 1 to 7. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater than POST_DIV2.

Note

For device-specific information about clock output parameters and synthesized clocks, see Table 6-30 and Table 6-31.

6.5.4.1.2.2 PLL Lock

PLL module outputs a lock status signal to indicate that the PLL has achieved frequency lock. When the PLL detects no cycle slips between the feedback clock (FFB) and reference clock FPFD (FREF/ REF_DIV[5-0]) for 128 consecutive cycles, it asserts the lock signal high. When the PLL detects any cycle slip, lock signal will go low and stays low until it detects no cycle slip for 128 consecutive cycles. This lock signal is captured in <PLL_name>_STAT[0] LOCK bit. Software can read this bit to determine if the PLL has achieved frequency lock before selecting the PLL clock through external bypass mux.

When PLL losses lock, there is a hardware mechanism to automatically bypass the PLL clock to the reference clock (FREF) using the external glitch free mux. BYP_ON_LOCKLOSS bit in <PLL_name>_CTRL register enables this automatic bypass mode on PLL lock loss. When the PLL re-locks, the glitch free mux switches to PLL clock out.

The PLL Lock signal is also routed to ESM module for error reporting. ESM can be configured to generate interrupts to MCU_R5FSS and R5FSS0/1 and assert Low on MCU_ERRORn pin on PLL Lock loss for further action.

6.5.4.1.2.3 HSDIVIDER

A PLL may contain up to 10 HSDIVIDER modules to produce more clocks with divided ratio based on the PLL synthesized clock frequency. HSDIVIDER provides only one output. The HSDIVIDER output clock frequency is given by the equations in Table 6-26.

Table 6-26. HSDIV_CLKOUT Frequency With PLL State

Equation	PLL Mode
HSDIV_CLKOUT = FOUTP / (HSDIV + 1)	Locked

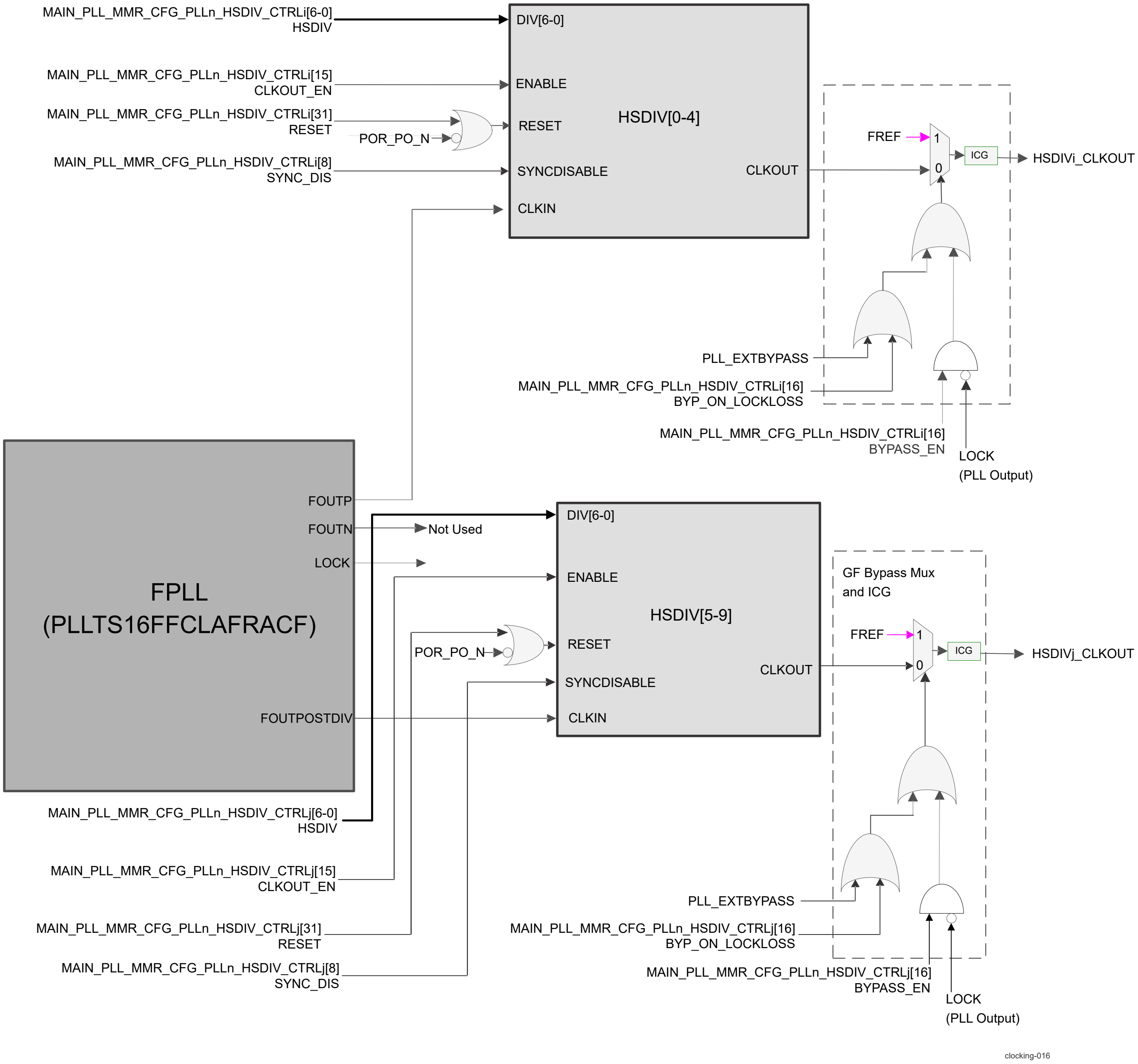
Table 6-26. HSDIV_CLKOUT Frequency With PLL State (continued)

Equation	PLL Mode
HSDIV_CLKOUT = FREF	Before lock or during relock

Where:

- FOUTP is the PLL lock frequency.
- HSDIV is the software-configured division ratio binary value.

Figure 6-33 describes the connection between a HSDIV and a specific type of PLL. Signals related only to this connections are shown in both figures.



[1] i = 0 to 4; j = 5 to 9

Figure 6-33. PLLTS16FFCLAFRACF2 and HSDIV Connection

6.5.4.1.2.4 ICG Module

ICG module ensures that when a particular HSDIV is not enabled the HSDIV clock output is gated off. This is a hardware module with no software control.

6.5.4.1.2.5 PLL Power Down

PLLTS16FFCLAFRACF2 is disabled with MCU_PLL_MMR_CFG_PLL0_CTRL[15] PLL_EN or MAIN_PLL_MMR_CFG_PLLn_CTRL[15] PLL_EN.

6.5.4.1.2.6 PLL Calibration

PLLTS16FFCLAFRACF2 has calibration feature. The calibration settings are done via <PLL_Name>_CAL_CTRL register. The calibration status can be monitored by reading <PLL_Name>_CAL_STAT register. For more information about device-specific information about calibration feature, see Table 6-32.

6.5.4.2 PLL Spread Spectrum Modulation Module

Spread Spectrum Modulation (SSMOD) modules on the device reduces Electro Magnetic Interference (EMI). It is a fully-digital circuit, used to modulate the frequency of the selected fractional PLLs. Programming options include selection of center spread or down spread, modulation depth, and modulation shape. The default modulation profile is triangular.

See *Spread Spectrum PLLs* for a list of PLLs that support Spread Spectrum.

SSMOD in the PLL is performed by changing the feedback divider (FRAC and FB_DIV) in a triangular pattern. This varies the frequency of the output clock in a triangular pattern. The frequency of this pattern is the modulation frequency (f_m). It is programmed as a ratio of the CLKIN/4.

Figure 6-34 shows a diagram of the spreading generation block.

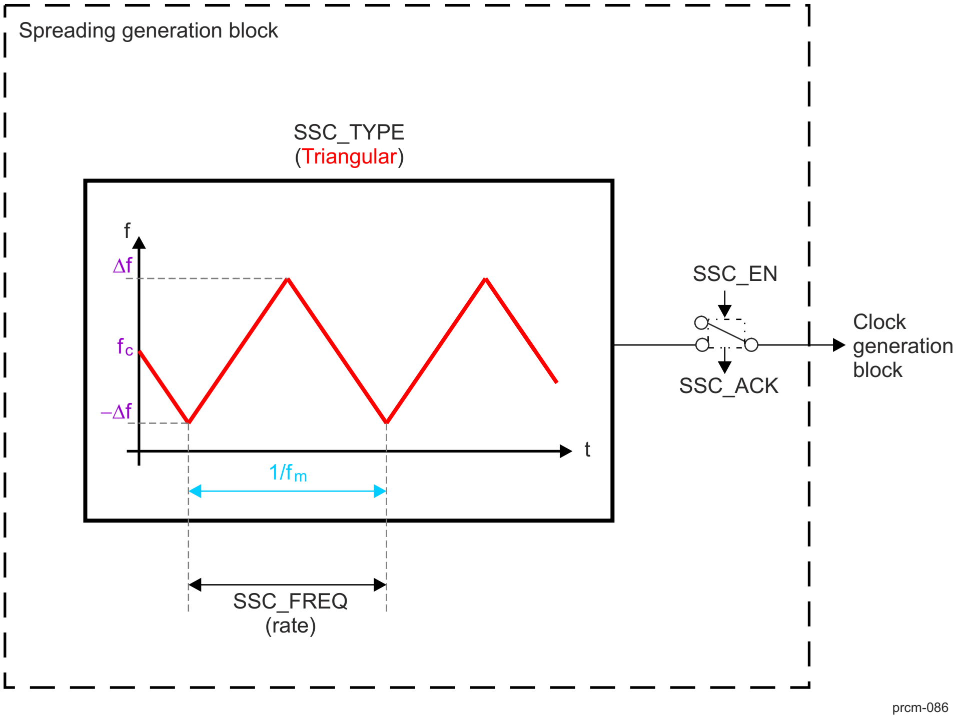


Figure 6-34. Spreading Generation Block Diagram

Note

Δf is the deviation from the center frequency. The total spreading deviation is equal to twice Δf. The peak (ΔM) or the amplitude of the triangular/square pattern as a percent of M would be equal to the percent of the frequency spread (Δf), $\Delta M/M = \Delta f/f_c$.

f_c is the original output clock frequency.

f_m is the spreading frequency.

This additional block generates the required waveform used to reduce EMI. This waveform is then modulated with the initial signal to add some controlled deviation to the clock signal frequency, which spreads the energy of the clock and its harmonics into a band of frequencies, and then reduces EMI. SSMOD_DOWNSPREAD can control the position of the generated signal. It is controlled by the <PLL_name>_CTRL[4] DOWNSPREAD_EN bit of the corresponding registers. If the DOWNSPREAD_EN bit is set to 1, the frequency spread on the lower side is twice the programmed value. The frequency spread on the higher side is 0.

The value of SSMOD_FREQ controls the rate of the generated signal. It can be programmed as a ratio of the reference clock: $f_{ref} / 4$. The value that must be programmed is calculated as follows:
ModFreqDivider = $f_{ref} / (4 \times f_m)$, where $f_m < f_{ref} / 70$, $f_{ref} = f_{inp} / (1+N)$, and f_{inp} is the input clock for the PLL.

6.5.4.2.1 Definition of SSMOD

The aim of the SSMOD is to add a variation to the frequency of an original clock, which spreads the generated interference over a larger band of frequencies.
In theory, SSMOD means that the clock signal is varied around the desired frequency. For example, for a 1 GHz clock, the frequency might be 999.5 MHz at one time and 1.0005 GHz at another. Doing this constantly causes the power of the tone to be spread out more over a broader band of tight frequencies (centered at the desired tone). To realize this constant variation on the original signal, a modulation with an additional signal (called spreading waveform) is realized.
Creating an SSMOD by spreading the initial clock frequency is done by defining the following parameters:

- The spreading frequency (deviation), which is the ratio of the range of spreading frequency over the original clock frequency.

6.5.4.2.2 SSMOD Configuration

Table 6-27 describes the PLL SSMOD control bitfields. Figure 6-35 describes the connection between a SSMOD and a PLL.

Table 6-27. SSMOD related bitfields

Parameter	Register	Description
SSMOD enable control	<PLL_name>n_SS_CTRL[31][(1)] BYPASS_EN (For example, MCU_PLL0 - MCU_PLL0_SS_CTRL[31] BYPASS_EN)	Enable/disable the PLL SSMOD feature.
Wave table maximum address	<PLL_name>n_SS_CTRL[25-18][(1)] WV_TBL_MAXADDR (For example, MCU_PLL0 - MCU_PLL0_SS_CTRL[25-18] WV_TBL_MAXADDR)	Wave table maximum address. Indicates the maximum number of address bits used to access the externalwave table. These bits are not used if <PLL_name>n_SS_CTRL[0] WAVE_SEL = 0
Type of spread	<PLL_name>n_SS_CTRL[4][(1)] DOWNSPREAD_EN (For example, MCU_PLL0 - MCU_PLL0_SS_CTRL[4] DOWNSPREAD_EN)	Selects center spread or down spread clock variance
Wave table selection	<PLL_name>n_SS_CTRL[0] [(1)] WAVE_SEL (For example, MCU_PLL0 - MCU_PLL0_SS_CTRL[0] WAVE_SEL)	Wave pattern select External wave table should only be selected

Table 6-27. SSMOD related bitfields (continued)

Parameter	Register	Description
Modulation dvider	<PLL_name>n_SS_SPREAD[19-16] (1) MOD_DIV (For example, MCU_PLL0 - MCU_PLL0_SS_SPREAD[19-16] MOD_DIV)	Input clock divider. This divider sets the modulation frequency.
Spread Depth	<PLL_name>n_SS_SPREAD[4-0] (1) SPREAD (For example, MCU_PLL0 - MCU_PLL0_SS_SPREAD[4-0] SPREAD)	Sets the spread modulation depth.

(1) n = 0 for MCU domain and n = 0 - 2, 5, 7, 8, 12, 15, and 17 for MAIN domain n = 0 for Top Level domain and n = 0 - 2, 5, 7, 8, 12, 15, and 17 for MAIN domain

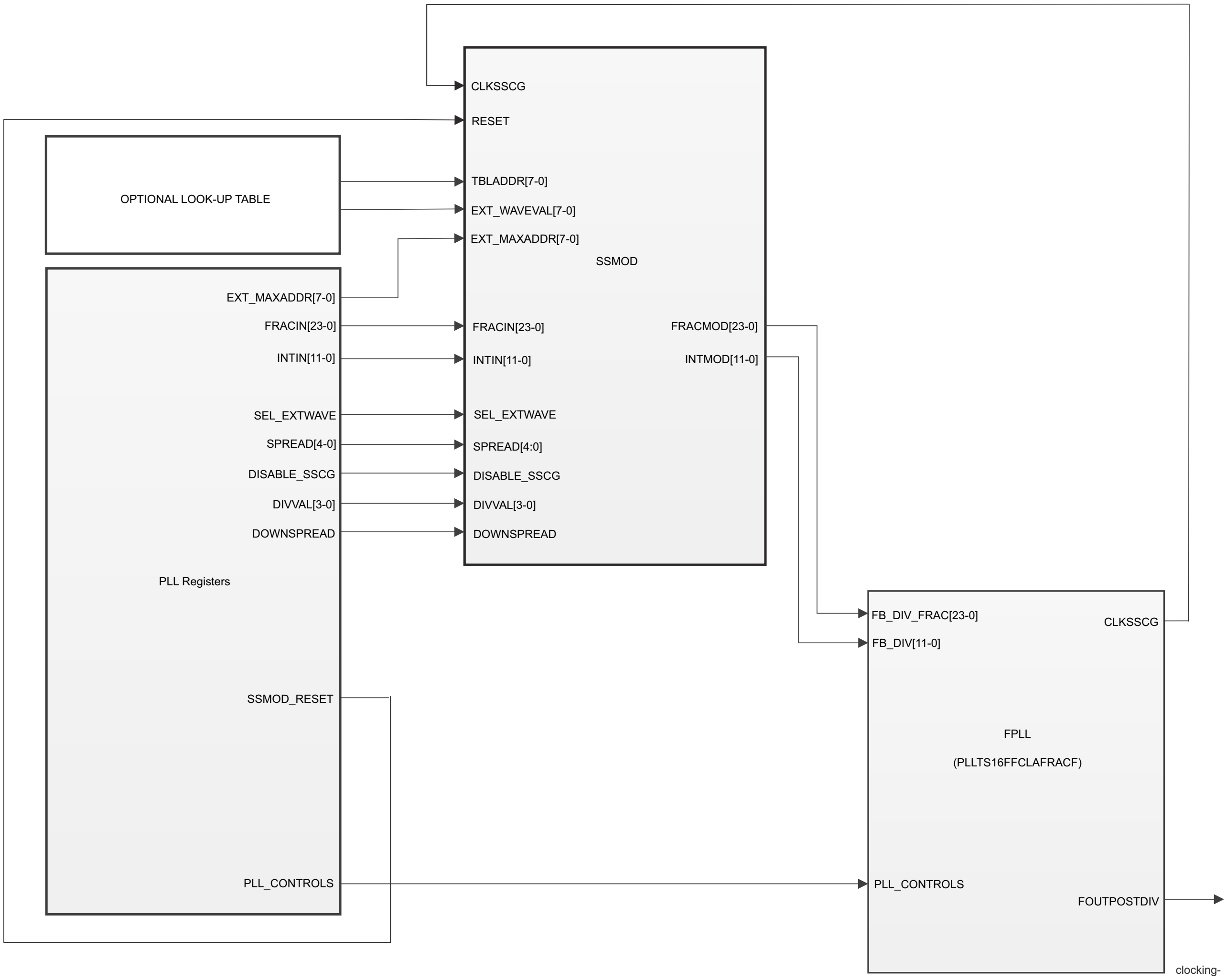


Figure 6-35. PLL and SSMOD Connection

6.5.5 PLLs Device-Specific Information

Basic Information of MCU_PLL0 lists the basic information of the MCU PLL.

Table 6-28. Basic Information of MCU_PLL0

PLL name	Type	SSMOD Available	HSDIV Available	Input clock	Comments
MCU_PLL0	PLLTS16FFCLAFRACF2	Yes, see *SSMOD related bitfields* for more information on SSMOD related bitfields/bits	HSDIV0, HSDIV1, HSDIV2, HSDIV4, HSDIV5	HFOSC0_CLKOUT	See the list below

Basic Information of MAIN Domain PLLs lists the basic information of each of the MAIN PLLs.

Table 6-29. Basic Information of MAIN Domain PLLs

PLL name	Type	SSMOD Available	HSDIV Available	Input clock	Comments
PLL0	PLLTS16FFCLAFRACF2	Yes, see *SSMOD related bitfields* for more information on SSMOD related bitfields/bits	HSDIV0, HSDIV1, HSDIV2, HSDIV4, HSDIV5, HSDIV6, HSDIV7, HSDIV8, HSDIV9	MAIN_PLL0_REF_CLK	See the list below
PLL1	PLLTS16FFCLAFRACF2	Yes, see *SSMOD related bitfields* for more information on SSMOD related bitfields/bits	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4, HSDIV5, HSDIV6	MAIN_PLL1_REF_CLK	See the list below
PLL2	PLLTS16FFCLAFRACF2	Yes, see *SSMOD related bitfields* for more information on SSMOD related bitfields/bits	HSDIV0, HSDIV1, HSDIV2, HSDIV3, HSDIV4, HSDIV5, HSDIV6, HSDIV8, HSDIV9	MAIN_PLL2_REF_CLK	See the list below
PLL4	PLLTS16FFCLAFRACF2	Yes, see *SSMOD related bitfields* for more information on SSMOD related bitfields/bits	HSDIV0, HSDIV1, HSDIV2, HSDIV4	MAIN_PLL4_REF_CLK	See the list below
PLL17	PLLTS16FFCLAFRACF2	Yes, see *SSMOD related bitfields* for more information on SSMOD related bitfields/bits	HSDIV0, HSDIV1	MAIN_PLL7_REF_CLK	See the list below
PLL14	FPLLTS16FFCLAFRACF2	Yes, see *SSMOD related bitfields* for more information on SSMOD related bitfields/bits	HSDIV0, HSDIV1	MAIN_PLL14_REF_CLK	See the list below
PLL15	PLLTS16FFCLAFRACF2	Yes, see *SSMOD related bitfields* for more information on SSMOD related bitfields/bits	HSDIV0, HSDIV1, HSDIV2, HSDIV3	MAIN_PLL15_REF_CLK	See the list below

1. See Figure 6-32, *Generic PLL Functional Diagram for PLLTS16FFCLAFRACF2 type* for overview of the PLL.
2. See Section 6.5.5.2 for synthesized clock parameters.
3. See Section 6.5.5.3 for clock output parameters.

6.5.5.1 SSMOD Related Bitfields Table

Table 6-27 lists SSMOD related bitfields for all types of PLLs.

6.5.5.2 Clock Synthesis Inputs to the PLLs

Table 6-30 lists the clock synthesis parameters for PLLTS16FFCLAFRACF2 type.

Table 6-30. Clock synthesis Parameters for PLLTS16FFCLAFRACF2 Type

Parameter Name	Register
FB_DIV	<PLL_name>_FREQ_CTRL0[11-0] FB_DIV_INT (For example, MCU_PLL0 - MCU_PLL0_FREQ_CTRL0[11-0] FB_DIV_INT)
FB_DIV_FRAC	<PLL_name>_FREQ_CTRL1[23-0] FB_DIV_FRAC (For example, MCU_PLL0 - MCU_PLL0_FREQ_CTRL1[23-0] FB_DIV_FRAC)
POST_DIV2	<PLL_name>_DIV_CTRL[26-24] POST_DIV2 (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[26-24] POST_DIV2)
POST_DIV1	<PLL_name>_DIV_CTRL[18-16] POST_DIV1 (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[18-16] POST_DIV1)
REF_DIV	<PLL_name>_DIV_CTRL[5-0] REF_DIV (For example, MCU_PLL0 - MCU_PLL0_DIV_CTRL[5-0] REF_DIV)

Note

For PLLTS16FFCLAFRACF2 type - POST_DIV1 and POST_DIV2 values are from 1 to 7. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2.

6.5.5.3 Clock Output Parameter

Table 6-31 lists the control/status bit fields for output clocks.

Table 6-31. Clock Output Parameter for PLLTS16FFCLAFRACF2 Type

Clock Output/Divider	Parameter Name	Control/Status Bit Field
<PLL_name>_CLKOUT, <PLL_name>_HSDIVj_CLKOUT(1)	Control	<PLL_name>_CTRL[31] BYPASS_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[31] BYPASS_EN)
<PLL_name>_HSDIVj_CLKOUT(1)	Control	<PLL_name>_HSDIV_CTRLj[15] CLKOUT_EN (For example, MCU_PLL0 - MCU_PLL0_HSDIV_CTRL0[15] CLKOUT_EN and MCU_PLL0_HSDIV_CTRL1[15] CLKOUT_EN)
<PLL_name>_HSDIVj_CLKOUT(1)	Divider control	<PLL_name>_HSDIV_CTRLj[6-0] HSDIV (For example, MCU_PLL0 - MCU_PLL0_HSDIV_CTRL0[6-0] HSDIV and MCU_PLL0_HSDIV_CTRL1[6-0] HSDIV)
PLL bypass mux	Control	<PLL_name>_CTRL[16] BYP_ON_LOCKLOSS (For example, MCU_PLL0 - MCU_PLL0_CTRL[16] BYP_ON_LOCKLOSS)
Enable 4-phase clock generator	Control	<PLL_name>_CTRL[5] CLK_4PH_EN (ignored if <PLL_name>_CTRL[4] CLK_POSTDIV_EN = 0) (For example, MCU_PLL0 - MCU_PLL0_CTRL[5] CLK_4PH_EN)
Post divide CLK enable	Control	<PLL_name>_CTRL[4] CLK_POSTDIV_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[4] CLK_POSTDIV_EN)
Delta-Sigma modulator enable	Control	<PLL_name>_CTRL[1] DSM_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[1] DSM_EN)

Table 6-31. Clock Output Parameter for PLLTS16FFCLAFRACF2 Type (continued)

Clock Output/Divider	Parameter Name	Control/Status Bit Field
Enable fractional noise canceling DAC	Control	<PLL_name>_CTRL[0] DAC_EN (For example, MCU_PLL0 - MCU_PLL0_CTRL[0] DAC_EN)

(1) j is the number of HSDIV for the current PLL.

6.5.5.4 Calibration Related Bitfields

Table 6-32 lists the calibration related bitfields/bits.

Table 6-32. Recalibration Feature Parameters

Recalibration feture	Parameter Name	Control/Status Bit Field
Calibration enable to actively adjust for input skew	Control	<PLL_name>_CAL_CTRL[31] CAL_EN (For example, PLL12 - PLL12_CAL_CTRL[31] CAL_EN)
Fast calibration enabled	Control	<PLL_name>_CAL_CTRL[20] FAST_CAL (For example, PLL12 - PLL12_CAL_CTRL[20] FAST_CAL)
Calibration loop programmable counter	Control	<PLL_name>_CAL_CTRL[18-16] CAL_CNT (For example, PLL12 - PLL12_CAL_CTRL[18-16] CAL_CNT)
Calibration bypass	Control	<PLL_name>_CAL_CTRL[15] CAL_BYP (For example, PLL12 - PLL12_CAL_CTRL[15] CAL_BYP)
Calibration input	Control	<PLL_name>_CAL_CTRL[11-0] CAL_IN (For example, PLL12 - PLL12_CAL_CTRL[11-0] CAL_IN)
Output of the calibration block	Status	<PLL_name>_CAL_STAT[11-0] CAL_OUT (For example, PLL12 - PLL12_CAL_STAT[11-0] CAL_OUT)

6.5.6 PLL Controller (PLLCTRL)

The PLLCTRL manages clock alignment of CBASS clocks to the peripherals in Main and MCU domains. In addition PLLCTRL is also responsible for controlling reset propagation through the chip and providing DFT hooks for testability. Two PLL Controllers are implemented in the device - PLLCTRL0 and MCU_PLLCTRL0. They are respectively related to PLL0 and MCU_PLL0.

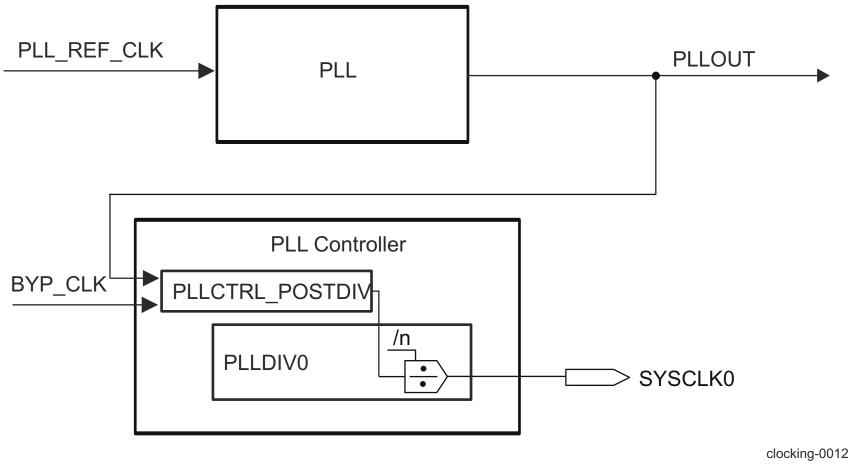


Figure 6-36. PLL Controller

Note

PLLCTRL_POSTDIV is not supported in this family of devices.

Note

The PLL Controllers registers can be accessed by any controller in the device.

A SYSCLK0 clock out of a PLLCTRL is the only synchronous clock in that domain. That means - MCU_SYSCLK0 out of MCU_PLLCTRL is the synchronous CBASS clock in MCU domain and SYSCLK0 out of Main PLLCTRL is the synchronous CBASS clock in Main domain.

6.5.7 PLL, PLLCTRL, and HSDIV Controllers Programming Guide

WARNING

PLL register descriptions are provided for debug purposes only. These registers should not be manipulated directly from software. PLL programming and configuration should only be performed using the appropriate APIs provided by TISCI services in TI's Processor Software Development Kits (SDKs). TISCI: Power Management (PM)

6.5.7.1 PLL Initialization

6.5.7.1.1 Kick Protection Mechanism

Note

PLL configuration registers are write-protected at power-up. Software must first un-lock the PLLn_LOCKKEY0 and PLLn_LOCKKEY1 registers prior to writing to any chip-level registers.

The un-lock process shall follow the steps:

1. Write value 0x68EF3490 to PLLn_LOCKKEY0 register.
2. Write value 0xD172BC5A to PLLn_LOCKKEY1 register.

After these two steps a write access to the PLL registers is allowed. Writing any other data value to either of these two registers locks the kicker mechanism and blocks any writes to the PLL registers.

Note

In order to ensure that all PLL registers are write protected, software must always re-lock the kicker mechanism after completing the register writes.

6.5.7.1.2 PLLCTRL Initialization

Note

For validated set of parameters that can be programmed to PLLs, please refer to the device-specific Datasheet.

Initially, the device powers up in PLL bypass mode. The bypass mux is a glitch free mux and is located outside the PLL module. BYPASS_EN bit controls the bypass mux section. During Power-up, the bypass mux defaults to select FREF clock (PLL clock bypass mode).

The following shows the PLL initialization sequence.

1. Wait until supplies are stable and PORz is de-asserted. By this time the reference clock source must be up and running.
2. Default controls settings:
   - By default PLL_EN signal is Low provided by <PLL_name>_CTRL register default state. This signal behaves like a reset control to the PLL.

  - By default INTL_BYP_EN signal is low provided by <PLL_name>_CTRL register default state.
  - By default BYPASS_EN signal is high provided by PLL MMR CTRL default state. PLL clock will be bypassed externally by a glitch free mux. The output of the mux will be the reference clock FREF.
  - LOCK output of PLL will be Low.
3. Program the PLL to a valid setting that runs the VCO within the specified range. The following bits/bitfields must be programmed appropriately by software: DSM_EN, DAC_EN, CLK_POSTDIV_EN, CLK_4PH_EN, REF_DIV[5-0], FB_DIV[11-0], FB_DIV_FRAC[23-0], POST_DIV1[2-0], POST_DIV2[2-0].
4. Wait for 1 µs to allow the PLL internal reset to complete (PLL powerdown switch pulls the loop filter voltage from rail-to-rail, which ensures the PLL will be completely powered down from any state).
5. Assert PLL_EN to a High (by writing a '1' into PLL_EN bit in <PLL_name>_CTRL register).
6. Wait for PLL Lock output to go high. Software can read the LOCK bit in <PLL_name>_STATS register to check if PLL has locked.
7. De-assert BYPASS_EN signal to a Low by writing 0 into BYPASS_EN bit in <PLL_name>_CTRL register.
8. Glitch free mux safely switches to the PLL clock output.

Note

In the case of brown out (supply dips below datasheet minimum) or loss of the reference clock, the state of the PLL will be undetermined. A full reset sequence should be initiated.

Changing PLL setting: During normal operation, before changing PLL settings, the PLL clock must be bypassed by setting BYPASS_EN control to a high. Then follow steps 2 to 8 from the above sequence.

6.5.7.1.3 PLL Programming Requirements

- A PLL VCO frequency must be set to > 1500 MHz
  - For best PLL performance, maximize VCO frequency where possible.
- A PLL must always operate in Fractional Mode (DAC_EN and DSM_EN set to ‘1’). This is true even when the FB_DIV is a integer.
- A PLL Reference clock frequency must be > 10 MHz.
- REF_DIV[5:0] must be set to “000001”.
- Calibration procedures for FRACF PLLs in integer mode or fractional mode:
  - **Programming FRACF in Integer Mode with calibration (Static or Auto Calibration)**
    - Set all the common PLL settings (PREDIV, FBDIV, …)
    - DACEN: 0
    - DSMEN = 0 (INT MODE)
    - FASTCAL=1
    - CALBYPASS=0
    - CALCNT[2:0]=2
    - CALIN[11:0]=0
    - CAL_EN=1
    - SET PLL_EN = 1
    - WAIT FOR PLL_LOCK AND CAL_LOCK GO HI
    - CAPTURE AND STORE CALCODE WHEN CAL_LOCK GOES HI IF IT WILL BE USED LATER
    - IF CAL_LOCK times out (> 2 ms) then continue
    - CAL_EN=0 (OPTIONAL, THIS WILL FREEZE CALIBRATION & INTERNAL CALCODE)
  - **Programming FRACF in Fractional Mode (with Static Calcode)**
    - Set all common PLL settings to nearest integer (PREDIV, FBDIV,...)
    - Run calibration as outlined in integer mode
    - CAPTURE AND STORE CALCODE WHEN CAL_LOCK GOES HI IF IT WILL BE USED LATER
    - IF CAL_LOCK times out (> 2 ms) then continue
    - CAL_EN=0 (THIS WILL FREEZE CALIBRATION & INTERNAL CALCODE)
    - IF CAL_LOCK timed out, keep CALBYPASS=0
    - IF CAL_LOCK IS ASSERTED AND CALCODE IS CAPTURED APPLY CALCODE TO CALIN
    - CALBYPASS=1 CALCODE IS SET BY CALIN
    - ENABLE FRACTIONAL MODE
  - **Programming FRACF in Fractional Mode (Auto-Calibration Not Allowed)**

- Set all the common PLL settings (PREDIV, FBDIV, …)
- DACEN=1
- DSMEN=1 (FRAC MODE)
- FASTCAL =X
- CALBYPASS=1 CALCODE IS SET BY CALIN
- CALCNT[2:0]=XX
- CALIN[11:0] = 0 (OR DESIRED CALCODE)
- CAL_EN = 0
- SET PLL_EN = 1
- WAIT FOR PLL_LOCK

PLL Integer mode with Calibration enabled is recommended for applications sensitive to phase noise or jitter: Examples include Refclk for SerDes, PHY, DDR etc. See individual product datasheets for specific SoC requirements. Calibration can be bypassed for digital clocks like ARM. If Calibration is bypassed, CALIN needs to be set to 0.

When Calibration is enabled, PLL Lock time will be longer since SOC needs to wait for CAL_LOCK. Applications sensitive to phase noise must wait for CAL_LOCK to go high.

6.5.7.2 HSDIV PLL Programming

<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 0 cleanly disables the HSDIV output clock

<PLL_Name>_HSDIV_CTRLk[6-0] HSDIV = <value> for divider

<PLL_Name>_HSDIV_CTRLk[8] SYNC_DIS = 0 insures that the divider changes occur synchronously to the internal divider of the HSDIV block.

when the clock is required,

<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 1 cleanly enables the HSDIV output clock

6.5.7.3 PLL Controllers Programming - Dividers PLLDIVn and GO Operation

The GO operation is required to change the divider ratios of the PLLDIVn registers. Section 6.5.7.3.1, *GO Operation*, discusses the GO operation. Section 6.5.7.3.2, *Software Steps to Modify PLLDIVn Ratios*, provides the software steps required to change the divider ratios.

6.5.7.3.1 GO Operation

The GO operation writes to the RATIO field in the PLLDIVn. Registers do not change the dividers' divide ratios immediately. The PLLDIV dividers change to the new RATIO rates only during a GO operation. This section discusses the GO operation and alignment of the SYSCLKs.

The PLL Controller clock align control register (ALNCTL) determines which SYSCLKs must be aligned. Before a GO operation, program ALNCTL so that the appropriate clocks are aligned during the GO operation.

A GO operation is initiated by setting the GOSET bit in PLLCMD to 1. During a GO operation:

- Any SYSCLK *n* with the corresponding ALN *n* bit in ALNCTL and SYS *n* bit in DCHANGE set to 1 is paused at the low edge. Then the PLL Controller restarts all these SYSCLKs simultaneously, aligned at the rising edge. When the SYSCLKs are restarted, SYSCLK *n* toggles at the rate programmed in the RATIO field in PLLDIVn.
- Any SYSCLK *n* with the corresponding ALN *n* bit in ALNCTL cleared and the SYS *n* bit in DCHANGE set immediately changes to the new rate programmed in the RATIO field.
- The GOSTAT bit in PLLSTAT is set throughout the duration of a GO operation.

CAUTION

To help prevent errors, all device operation must be stopped before the GO operation.

6.5.7.3.2 Software Steps to Modify PLLDIV Ratios

Perform the following steps to modify PLLDIV.

1. Check that the GOSTAT bit in PLLSTAT is cleared to show that no GO operation is currently in progress.
2. Program the RATIO field in PLLDIVn to the desired new divide-down rate. If the RATIO field changed, the PLL Controller will flag the change in the corresponding bit of DCHANGE.
3. Set the respective ALN *n* bits in ALNCTL to align any SYSCLKs after the GO operation.
4. Set the GOSET bit in PLLCMD to initiate the GO operation to change the divide values and align the SYSCLKs as programmed.
5. Read the GOSTAT bit in PLLSTAT to make sure the bit returns to 0 to indicate that the GO operation has completed.

6.5.7.4 Entire Sequence for Programming PLLCTRL, HSDIV, and PLL

Table 6-33 shows the entire sequence of programming PLLCTRL, HSDIV, and PLL from an unknown state to a defined non-spread-spectrum state.

Table 6-33. Programming Sequence of PLLCTRL, HSDIV, and PLL

Step	Description
Unlock PLL registers	<PLL_Name>_LOCKKEY0 (= 0x68EF3490)
	<PLL_Name>_LOCKKEY1 (= 0xD172BC5A)
If PLL0	Configure PLLCTRL block into bypass mode
	PLLCTL[0]PLLEN = 0
	PLLCTL[5] PLLENSRC = 0
Configure external bypass so that no transient clock propagates	<PLL_Name>_CTRL[31] BYPASS_EN = 1
Delay	
Disable HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN =0
Delay	
Disable PLL	<PLL_Name>_CTRL[15] PLL_EN =0
Delay	
Reset HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[31] RESET = 1
If PLL0	Check PLLSTAT[0] GOSTAT to make sure that divider change is not currently in-progress GOSTAT should equal 0.
	Clear GOSET bit PLLCMD[0] GOSET = 0
	Configure divider in PLLCTRL to /1 PLLDIV1 = 0x8000 (enable divider and divide by 1) PLLDIV2 = 0x00 (disable divider and divide by 1)
	Set alignment control bits ALNCTL = 3
	Set GOSET bit to initiate the divider change PLLCMD[0] GOSET = 1
	Check PLLSTAT[0] GOSTAT to make sure that divider change has completed GOSTAT should equal 0.
Configure HSDIV(s) divider value	<PLL_Name>_HSDIV_CTRLk[6-0] HSDIV (=val)
Clear HSDIV(s) SYNC_DIS	<PLL_Name>_HSDIV_CTRLk[8] SYNC_DIS = 0
Delay	
Clear Reset HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[31] RESET = 0
Configure PLL multiplier	Integer portion of divider <PLL_Name>_FREQ_CTRL0[11-0] (=val) Fractional portion of divider <PLL_Name>_FREQ_CTRL1[23-0] (=val)
Configure PLL dividers	Reference clock divider <PLL_Name>_DIV_CTRL[5-0] REF_DIV = 1
	Post divider 1 <PLL_Name>_DIV_CTRL[18-16] POST_DIV1 = 1

Table 6-33. Programming Sequence of PLLCTRL, HSDIV, and PLL (continued)

Step	Description
	Post divider 2 <PLL_Name>_DIV_CTRL[26-24] POST_DIV2 = 1
Configure “random” PLL controls	<PLL_Name>_CTRL[8] INTL_BYP_EN = 0
	<PLL_Name>_CTRL[5] CLK_4PH_EN = 0
	<PLL_Name>_DIV_CTRL[26-24] POST_DIV2 = 1
	<PLL_Name>_DIV_CTRL[18-16] POST_DIV1 = 1
	<PLL_Name>_DIV_CTRL[5-0] REF_DIV = 1
	<PLL_Name>_CTRL[1] DSM_EN = 1
	<PLL_Name>_CTRL[0] DAC_EN = 1
	<PLL_Name>_SS_CTRL[31] BYPASS_EN (SSMOD) = 1
	<PLL_Name>_CTRL[4] CLK_POSTDIV_EN – if PLL has more than 5 HSDIV blocks, 1; else 0.
	<PLL_Name>_CTRL[16] BYP_ON_LOCKLOSS (= {0, 1})
Delay	
Enable PLL	<PLL_Name>_CTRL[15] PLL_EN = 1
Wait for Lock	Wait for MCU_PLL0_STAT[0] LOCK = 1
Enable HSDIV(s)	<PLL_Name>_HSDIV_CTRLk[15] CLKOUT_EN = 1
Delay	
Configure external bypass to pass PLL	<PLL_Name>_CTRL[31] BYPASS_EN = 0
Delay	
If PLL0	Configure PLLCTRL block into PLL mode PLLCTL[0] PLLEN = 0
Lock PLL registers	<PLL_Name>_LOCKKEY0 (= any value)
	<PLL_Name>_LOCKKEY1 (= any value)

6.5.7.5 Dual Clock Comparator (DCC)

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference. Internal 12.5 MHz RC oscillator (RC OSC) clock is used to validate HFOSC0_CLKOUT and monitor for clock loss. If a fault is detected on HFOSC0, the device shall automatically transition to the back up clock (RC OSC).

In addition, HFOSC0_CLKOUT (most accurate clock) is used to validate/track all other clocks in the device. An additional use of this module is to measure the frequency of a selectable clock source, using an external input clock source of known frequency (MCU_EXT_REFCLK0, EXT_REFCLK1 pins). There is one instance of DCC module in MCU domain and seven instances of DCC modules in Main domain to monitor critical clocks. Refer to DCC chapter for details.

7 Processors and Accelerators

Note

This TRM uses the prefix of "MCU_" for items that refer to the device as a whole instead of a specific domain. "MCU_" is the equivalent of Top Level from Section 1.5.

7.1 Dual-R5F MCU Subsystem

This chapter describes the dual-R5F microcontroller unit subsystem (R5FSS) in the device.

7.1.1 R5FSS Overview

The R5FSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for split/lock operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm CoreSight™ debug and trace architecture, integrated vectored interrupt manager (VIM), ECC aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

There are two R5FSS modules in the device. Table 7-1 shows R5FSS modules allocation within device domains.

Table 7-1. R5FSS Modules Allocation within Device Domains

Module Instance	Domain		
	WKUP	Top Level	MAIN
R5FSS0	–	–	✓
R5FSS1	–	–	✓

7.1.1.1 R5FSS Features

Each R5FSS supports the following features:

- Dual-core Arm Cortex-R5F
  - Core revision: r1p3
  - Armv7-R profile
  - Advanced SIMD extension for integer and floating point vector operations
  - Split/lock operation
    - Split mode: Two independently operating cores (asymmetric multi processing, no coherence)
    - Lock (lockstep) mode: One main operating core with the other operating in lockstep
    - Boot-time configurable to be in split or lock mode
  - L1 memory system
    - 32KB instruction cache
      - 4x8KB ways
      - SECDED ECC protected per 64 bits
    - 32KB data cache
      - 4x8KB ways
      - SECDED ECC protected per 64 bits
    - 64KB tightly-coupled memory (TCM) per CPU in split mode
      - SECDED ECC protected per 32 bits
      - Readable/writable from system
      - Split into A and B banks (with B further splitting into B0 and B1 interleaved banks)
        - 32KB TCMA (ATCM)
        - 16KB TCMB0 (B0TCM)
        - 16KB TCMB1 (B1TCM)
    - 128KB of TCM for CPU0 in lock mode
  - Low interrupt latency with restartable instructions
  - Non-maskable interrupt (NMI)
  - Full-precision floating point (VFPv3)
  - 16 region memory protection unit (MPU)
  - 8 breakpoints
  - 8 watchpoints
  - Dynamic branch prediction with global history buffer and 4-entry return stack
  - CoreSight debug access port (DAP)
  - CoreSight embedded trace macrocell (ETM-R5) interface
  - Performance monitoring unit (PMU)
- Interfaces
  - 64-bit VBUSM controller pair (1 read, 1 write) for L3 memory accesses (per core)

  - 64-bit VBUSM peripheral for TCM access (per core)
    - Also allows access to cache for debug purposes
  - 32-bit VBUSM controller pair (1 read, 1 write) for peripheral access
  - 32-bit VBUSP controller for peripheral access (per core)
  - 32-bit VBUSP peripheral configuration port (per core)
  - 32-bit VBUSP peripheral debug port
  - Allows access to all R5FSS internal debug logic
- Synchronous clock domain crossing on all interfaces
  - Interfaces can run at an integer division of the core frequency
- Error detection logic (in lockstep mode only)
- 32-bit to 48-bit region-based address translation (RAT) on memory access controllers
  - 16 regions
    - Base address + size
    - Must be size aligned
- Integrated vectored interrupt manager (VIM)
  - 512 interrupts per core
    - Only interrupts connected to R5F core 0 are available in lock mode
    - Each interrupt programmable as either IRQ or FIQ
    - Each interrupt has a programmable enable mask
    - Each interrupt has a programmable 4-bit priority
  - Priority interrupt supported
  - Vectored interrupt interface
    - Compatible with R5F VIC port
    - Programmable 32-bit vector address per interrupt
      - Address is SECDED error protected
      - Default vector addresses provided on DED
    - Split or lockstep capable
    - Software interrupt generation
- Integrated ECC aggregators
  - Support for error injection to all supported ECC memory blocks to test ECC functionality (add-on function from TI)
  - One ECC aggregator per core to cover all RAMs and caches associated with that core
- Standard Arm CoreSight debug and trace architecture at the R5FSS level
  - Cross triggering: Supported by cross trigger interface (CTI) (per CPU) and cross trigger matrix (CTM) components
  - Processor trace: Supported by embedded trace macrocell (ETM) (per CPU) and advanced trace bus (ATB) funnel components
- Boot
  - From ROM or external memory via XIP, or HyperRAM
  - From TCM

Unsupported Features:

- See the Module Integration section of this document for a list of module features not supported by the integration on this Device.

7.1.1.2 R5FSS Not Supported Features

The R5FSS does *not* support the following native R5F features in this device:

- ACP port (no coherence)
- Bus parity / ECC

7.1.2 R5FSS Functional Description

7.1.2.1 R5FSS Block Diagram

Figure 7-1 shows the R5FSS block diagram.

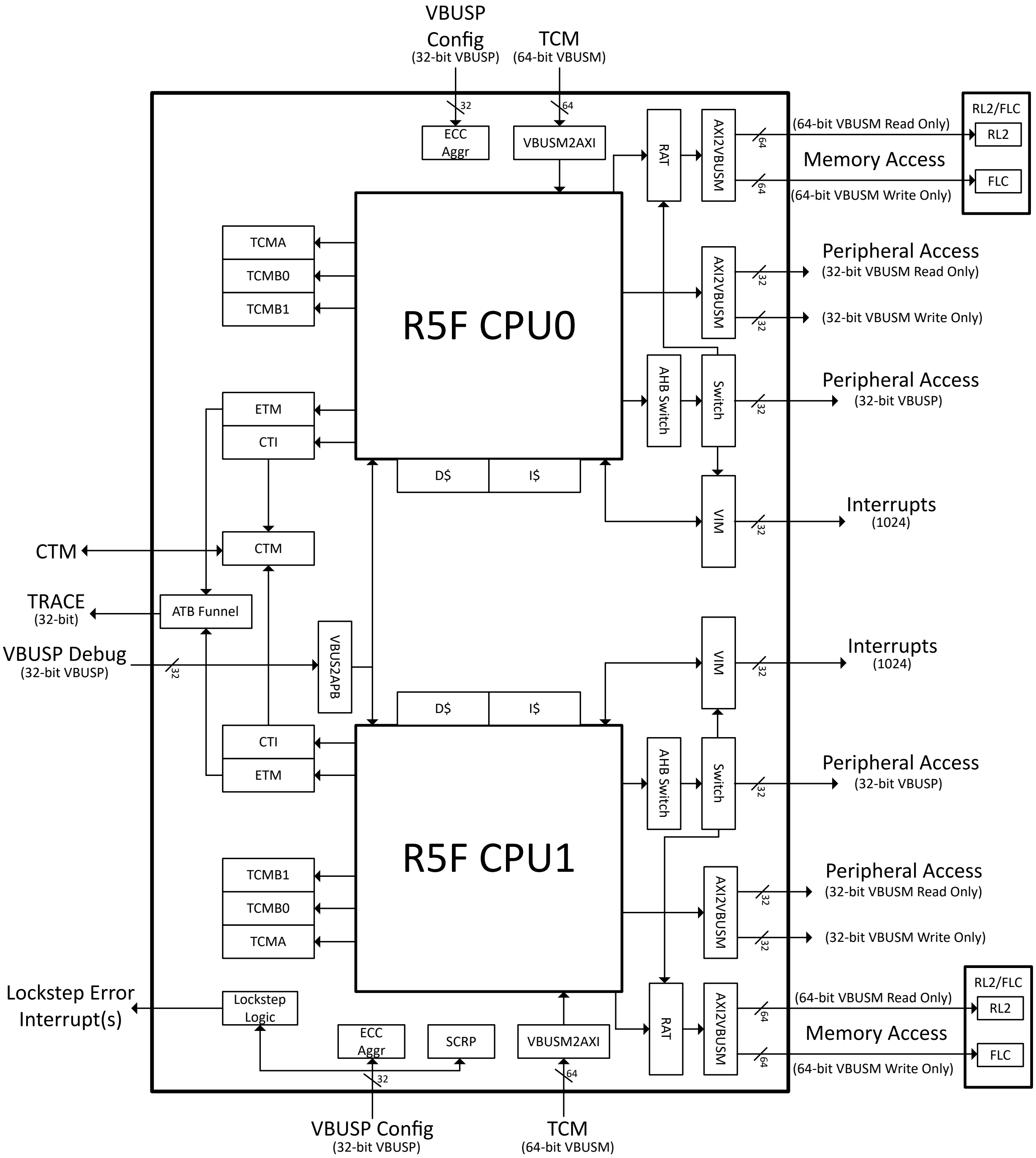


Figure 7-1. R5FSS Block Diagram

A. R5FSS Block Diagram applies for both R5FSS0 and R5FSS1

7.1.2.2 R5FSS Cortex-R5F Core

The Cortex-R5F is a processor from Arm, which is based on the Armv7-R profile. Each R5FSS implements two R5F cores, CPU0 and CPU1, each with their own RAMs and interfaces. While in reset, they can be bootstrapped to work in one of two modes: split or lockstep.

In split mode, each R5F core works completely independent from the other (asymmetric multi-processing, or AMP). Each core uses its own RAMs and interfaces, with no coherence between the two cores. The only restriction is that CPU0 must be in a higher power/reset state than CPU1. For instance, CPU1 cannot be out of reset if CPU0 is not.

In lock mode, the core logic from CPU1 is used as redundant logic to check for errors in CPU0. Comparison logic automatically checks the redundant logic against the primary logic and flags any errors. The CPU1 interfaces are not used in this mode. In previous generations of R5FSS, the CPU1 TCMs were unused in lock mode. In this generation of R5FSS, for more efficient use of available memories, the CPU1 TCMs are stacked on CPU0 TCMs in lock mode and are accessible only by CPU0 and CPU0 TCM interface. The TCM size for CPU0 is essentially doubled in lock mode (128KB).

For more detailed description of this processor, see the *Arm Cortex-R5 Technical Reference Manual*. A brief list of features supported by the R5F processor in this device is given in Section 7.1.1.1, *R5FSS Features*.

7.1.2.2.1 L1 Caches

The R5F has a Harvard cache architecture, which means it has an independent L1 instruction cache (32KB) and L1 data cache (32KB). The instruction cache is protected by SECDED ECC per 64 bits. The data cache is protected by SECDED ECC per 32 bits.

7.1.2.2.2 Tightly-Coupled Memories (TCMs)

The R5F has two tightly-coupled memories (TCMs), ATCM and BTCM. The BTCM is further broken down into two interleaved banks, B0TCM and B1TCM.

TCMs are low-latency, tightly integrated memories for the R5F to use. Either TCM can be used for any combination of instruction and/or data. TCM performance is equal to performance on instructions/data that are in cache. However, TCMs have some additional advantages over cache. TCMs can be loaded with instructions that do not cache well (such as ISRs) or preloaded with code by an external source, before that code is needed, to save cache miss time. TCMs are also a good place for blocks of data for intense processing. They can be loaded (or pre-loaded by an external source) before the data is needed, saving cache miss time. The data can then be directly accessed by an external source, instead of needing to do cache evicts.

As mentioned, TCMs can be accessed (either read or written) by an external source over the TCM VBUSM slave interface. This allows instructions or data to be preloaded, or for data to be read out after the R5F has processed it. The VBUSM slave has a lower priority to accessing TCMs than the R5F but care must be taken to keep an external source from reading or writing TCM data that the R5F is working on. This handshaking is external to any of the R5FSS hardware.

TCMs are protected by ECC per 32 bits. For this to work, ECC must be enabled before data is written in to the TCMs (either externally or from the R5F). ECC is enabled via the following R5F system control bits: ACTLR.ATCMPCEN, ACTLR.B0TCMPCEN, and ACTLR.B1TCMPCEN, respectively.

Whether or not the TCMs are enabled is controlled by the ENABLE bit in the corresponding ATCM/BTCM region register. The default (reset) value of this bit is determined by the CPUn_INITRAMA and CPUn_INITRAMB bootstraps, respectively. Both ATCM and BTCM are configured for a size of 32KB in this device. Note that the BTCM size is the total of both B0TCM and B1TCM (16KB each).

If a TCM is not enabled, then it does not appear in the R5F memory view, but it can be accessed by an external source. If a TCM is enabled, then its place in the R5F memory map is determined by a combination of bootstrap signal and system register. If the CPUn_LOCZRAMA bootstrap signal is high, then the initial base address of ATCM is 0x0000_0000 and the initial address of BTCM is 20’h41010. If the CPUn_LOCZRAMA bootstrap signal is low, then the initial base address of BTCM is 0x0000_0000 and the initial base address of ATCM is 20’h41010.

Note

This base address of 0x41010 for ATCM/BTCM based on the CPUn_LOCZRAMA bootstrap only affects the R5F's memory view. The SoC will see the ATCM/BTCM based on the TCM slave interface regions, as defined in Section 7.1.2.3.2. The base address of either TCM may be overwritten via the ATCM or BTCM region register. Care must be taken not to move the base address of a TCM when it may be being accessed.

It is possible to preload a TCM with instructions and boot from it. For more details, see Section 7.1.2.12, *R5FSS Boot Options*.

7.1.2.2.3 Remote L2 Cache (RL2)

The AXI L2 port of each R5F core integrates a remote L2 cache controller with integrated tag RAM. AXI is a bus protocol defined by ARM and stands for Advanced eXtensible Interface. The L2 cache is remote which means the cache data memory is allocated from the available L2 SRAM in the device. Once allocated, this SRAM space is unavailable for application code / data.

RL2 supports the following features:

- Integrated tag RAM with 4096 cache lines support
- Eight-way set associative with LRU policy
- RL2 cache line size is aligned with R5F cache line size (32 bytes)
- ECC protection on tag RAM
- Software programmable cache lines to enable application configurable remote cache size of 8KB, 16KB, 32KB, 64KB or 128KB
  - The cache-able target space varies proportionately based on the cache size.
- Dual mode support to enable sharing two cache lines the same way which increases the remote cache size to 256kB while reducing the cache-able region of tag RAM
- Pass-through for addresses not within the cache-able region
- Pass-through for accesses originating from FLC DMA
- Supports signaling of XIP read pending signal that allows automatic hardware priority of XIP during read-while-write operations for flash firmware-over-the-air update (FOTA)

7.1.2.2.4 Fast Local Copy (FLC)

The AXI L2 port of each R5F core integrates a Fast Local Copy (FLC) engine to accelerate boot up. Reducing boot time of R5F is essential to achieve 50ms CAN response.

The FLC engine is designed to leverage how application execution from internal SRAM is significantly faster than execution from external flash. A typical boot process involves critical application code getting copied over from flash to SRAM before executing from SRAM. The copy phase of this process results in increased boot time.

With the FLC engine, boot up is accelerated by redirecting the core access to flash when the copy is in progress and redirecting the access to SRAM when the content is in valid in SRAM. This enables core to execute immediately without waiting for the copy to complete. The operation is transparent to core.

The FLC supports the following features:

- Support up to four flash regions per FLC with 64kB granularity
- Internal DMA engine to copy code from flash to SRAM sequentially for all regions
- Redirect access to flash when the data is not yet available in SRAM
- Redirect access to SRAM when the data is available in SRAM
- Transparent to core after initial configuration of regions
- Pass-through for addresses not in the programmed regions
- The SRAM redirection does not wait till the entire region is mirrored, but is enabled as soon as the content at that address is valid in SRAM
- Interrupt generation when mirroring of region is complete
- Option to disable DMA copy and only enable SRAM redirection

7.1.2.2.5 R5FSS Special Signals

The following tables list some R5FSS features associated with special signals. Note that in lockstep mode only those for CPU0 apply.

Table 7-2. R5FSS0 Special Features

Feature	Comment
Cluster affinity group ID	R5F Cluster 1 (ID = 0x1)
Exception handling state at reset 0 = Arm 1 = Thumb	Controlled via MAIN_SEC_MMR register setting. Defaults to Arm mode
Split or lockstep mode 0 = Split mode 1 = Lockstep mode	Controlled via MAIN_SEC_MMR register setting. Defaults to a value defined by eFuse
CPUn execution halt when coming out of reset (CPUn_HALT)	Controlled via MAIN_SEC_MMR register setting. Defaults to halted state
CPUn exception vectors base address	Controlled via MAIN_SEC_MMR register setting. Defaults to Bootvector RAM address 0x0000_0000_0200
CPUn VIM base address	0x0FF8_0000
CPUn RAT base address	0x0FF9_0000
CPUn RAT accesses ID	0x4 (CPU0); 0x5 (CPU1)
CPUn ATCM enable at reset (CPUn_INITRAMA)	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn BTCM enable at reset (CPUn_INITRAMB)	Controlled via MAIN_SEC_MMR register setting. Defaults to enabled state
CPUn A/BTCM reset base address indicator (CPUn_LOCZRAMA) 0 = B at 0x0 1 = A at 0x0	Controlled via MAIN_SEC_MMR register setting. Defaults to 1
CPUn non-maskable fast interrupts enable	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn VBUSM peripheral port enabled at reset	Enabled
CPUn VBUSP peripheral port enable at reset	Enabled
CPUn VBUSP peripheral port base address	Mapped to 0x0_0F80_0000 for low latency MAIN peripherals
CPUn VBUSP peripheral port size	8MB for MAIN peripherals (0x0_0F80_0000 to 0x0_0FFF_FFFF)
CPUn VBUSM normal peripheral port base address	Mapped to 0x0200_0000 for MAIN peripherals
CPUn VBUSM normal peripheral port size	32MB for MAIN peripherals (0x0_0200_0000 to 0x0_03FF_FFFF)
CPUn VBUSM virtual peripheral port base address	Mapped to 0x0200_0000 for MAIN peripherals
CPUn VBUSM virtual peripheral port size	32MB for MAIN peripherals (0x0_0200_0000 to 0x0_03FF_FFFF)
CPUn clock stopped indication	Status logged into MAIN_SEC_MMR register bit
CPUn WFI state	Status logged into MAIN_SEC_MMR register bit
CPUn WFE state	Status logged into MAIN_SEC_MMR register bit
CPU clockstop behavior 0: CPU clocks stopped in standby 1: CPU clocks not stopped in standby	Controlled via MAIN_SEC_MMR register setting. Defaults to 0

Table 7-3. R5FSS1 Special Features

Feature	Comment
Cluster affinity group ID	R5F Cluster 2 (ID = 0x2)
Exception handling state at reset 0 = Arm 1 = Thumb	Controlled via MAIN_SEC_MMR register setting. Defaults to Arm mode
Split or lockstep mode 0 = Split mode 1 = Lockstep mode	Controlled via MAIN_SEC_MMR register setting. Defaults to a value defined by eFuse
CPUn execution halt when coming out of reset (CPUn_HALT)	Controlled via MAIN_SEC_MMR register setting. Defaults to halted state

Table 7-3. R5FSS1 Special Features (continued)

Feature	Comment
CPUn exception vectors base address	Controlled via MAIN_SEC_MMR register setting. Defaults to Bootvector RAM address 0x0000_0000_0200
CPUn VIM base address	0x0FF8_0000
CPUn RAT base address	0x0FF9_0000
CPUn RAT accesses ID	0x6 (CPU0); 0x7 (CPU1)
CPUn ATCM enable at reset (CPUn_INITRAMA)	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn BTCM enable at reset (CPUn_INITRAMB)	Controlled via MAIN_SEC_MMR register setting. Defaults to enabled state
CPUn A/BTCM reset base address indicator (CPUn_LOCZRAMA) 0 = B at 0x0 1 = A at 0x0	Controlled via MAIN_SEC_MMR register setting. Defaults to 1
CPUn non-maskable fast interrupts enable	Controlled via MAIN_SEC_MMR register setting. Defaults to disabled state
CPUn VBUSM peripheral port enabled at reset	Enabled
CPUn VBUSP peripheral port enable at reset	Enabled
CPUn VBUSP peripheral port base address	Mapped to 0x0_0F80_0000 for low latency MAIN peripherals
CPUn VBUSP peripheral port size	8MB for MAIN peripherals (0x0_0F80_0000 to 0x0_0FFF_FFFF)
CPUn VBUSM normal peripheral port base address	Mapped to 0x0200_0000 for MAIN peripherals
CPUn VBUSM normal peripheral port size	32MB for MAIN peripherals (0x0_0200_0000 to 0x0_03FF_FFFF)
CPUn VBUSM virtual peripheral port base address	Mapped to 0x0200_0000 for MAIN peripherals
CPUn VBUSM virtual peripheral port size	32MB for MAIN peripherals (0x0_0200_0000 to 0x0_03FF_FFFF)
CPUn clock stopped indication	Status logged into MAIN_SEC_MMR register bit
CPUn WFI state	Status logged into MAIN_SEC_MMR register bit
CPUn WFE state	Status logged into MAIN_SEC_MMR register bit
CPU clockstop behavior 0: CPU clocks stopped in standby 1: CPU clocks not stopped in standby	Controlled via MAIN_SEC_MMR register setting. Defaults to 0

7.1.2.3 R5FSS Interfaces

7.1.2.3.1 R5FSS Controller Interfaces

The R5FSS has several master interfaces per core:

- 64-bit VBUSM master pair (1 read – “RMST”, 1 write – “WMST”) for L3 memory accesses; this is the main memory interface
  - Includes region-based address translation (RAT)
- 32-bit VBUSM master pair (1 read – “PRMST”, 1 write – “PWMST”) for peripheral access
  - Enabled at reset
  - Supported for R5FSS0 and R5FSS1
- 32-bit VBUSP master “PMST” for peripheral access
  - Includes logic that provides the R5F CPU with a private access to VIM and RAT
  - Enabled at reset

7.1.2.3.2 R5FSS Peripheral Interfaces

The R5FSS has several peripheral interfaces that define its internal memory space:

- 32-bit VBUSP configuration peripheral (per core)
  - Region [0]: ECC aggregator block
  - Region [1]: Lockstep comparator block (CCMR5); this region is only applicable to CORE0
- 64-bit TCM peripheral (per core)
  - Region [0]: ATCM
  - Region [1]: BTCM

  - Region [2]: Instruction cache RAMs
  - Region [3]: Data cache RAMs
- 32-bit VBUSP debug peripheral
  - Provides access to all R5FSS internal debug logic

Regions [0] and [1] of the TCM peripheral interface provide direct access to the TCM RAMs. Access to the RAMs is arbitrated with access from the R5F's L1 memory system. Excessive access while the R5F is also attempting access will degrade performance.

Regions [2] and [3] of the TCM peripheral interface provide access to the cache RAMs for testing purposes. Access to the cache RAMs can only be done while the caches are disabled and should only be done for test purposes.

In addition to the peripheral interfaces, there are peripherals (RAT and VIM) that are only accessible by the R5F. The R5F has an access to these modules via the VBUSP peripheral interface.

7.1.2.4 R5FSS Power, Clocking and Reset

7.1.2.4.1 R5FSS Power

The following R5FSS power considerations should be noted:

- R5FSS has a single power domain for all its internal logic
- When operating in split mode, CPU0 must be in a higher power/reset state than CPU1.

For more details on R5FSS power management, including power-up and power-down sequences, see *Power*.

7.1.2.4.2 R5FSS Clocking

The R5FSS has four clock inputs:

- CPU0_CLK: This is the clock for CPU0 logic
- CPU1_CLK: This is the clock for CPU1 logic
- CPU0_ICLK: This is the clock for CPU0 interfaces
- CPU1_ICLK: This is the clock for CPU1 interfaces

CPU0_CLK and CPU1_CLK are the clocks for all of the internal CPU logic. They are provided separately so that:

- In split mode, CPU1's clock may be turned off, while CPU0 is still in active mode
- In lock mode, they are sourced separately

CPU0_ICLK and CPU1_ICLK are the clocks for all of the interfaces for their associated CPU (for example: VBUSM and VBUSP bridges, exception generation, debug and trace logic). They are provided separately so that CPU1_ICLK can be gated if CPU1 is in a lower power state, while CPU0 is ON, or when in lock mode.

The interface clock is an integer ratio of the CPU clock. See *R5FSS Integration*.

7.1.2.4.3 R5FSS Reset

The R5FSS has four reset inputs:

- CPU0_RST: This is the reset for the non-debug logic of CPU0
- CPU0_DBG_RST: This resets the CPU0 debug logic, excluding the APB interface
- CPU1_RST: This is the reset for the non-debug logic of CPU1
- CPU1_DBG_RST: This resets the CPU1 debug logic, excluding the APB interface

In addition to the reset signals, there are two halt signals:

- CPU0_HALT
- CPU1_HALT

These halt signals keep the CPUs from fetching instructions when they come out of reset. The main use is to have the CPUs halted until the TCMs are loaded (when booting from TCM), though halt could be used for any other purpose.

7.1.2.5 R5FSS Lockstep Error Detection Logic

When bootstrapped to lockstep mode, there is a logic that compares the outputs of the two cores. Whenever an error is detected, an interrupt is asserted. A logic is also included to test the comparison logic.

In lockstep mode, the logic from CPU1 is used to check CPU0. CPU1's RAMs and L1 memory system are not used. Instead, all inputs to CPU0 are copied, delayed by two cycles, and fed into CPU1's logic. All outputs from CPU0 are copied, delayed by two cycles, and compared to the outputs of CPU1.

The lockstep error detection logic in the R5FSS is implemented via the CPU compare module (CCMR5). The CCMR5 performs two main functions:

- CPU output compare: Compares the core compare bus outputs of the two R5F processor cores in lockstep mode
- Inactivity monitoring: This is to detect any transaction initiated by the diagnostic R5F core (CPU1) in lockstep mode. The diagnostic core is expected *not* to initiate any transaction in lockstep mode

7.1.2.5.1 CPU Output Compare Block

To implement a lockstep CPU cluster, a diagnostic checker block is included. The diagnostic checker block compares the CPU compare outputs on every cycle. A difference in the CPU output signals is indicated by an error signal.

As the CPUs are working with a two-cycle phase difference, there should be no compare errors generated when the CPUs are reset two cycles apart. For the various CPU interfaces, the comparison will start on the first valid transaction on key control signals.

Note

While R5 is in lockstep and CCM is active, debug using external debugger is not supported.

7.1.2.5.1.1 Operating Modes

The CPU compare block can run in one out of four operating modes:

- Compare active block
- Self test
- Error forcing
- Self test error forcing

To select an operating mode for the CPU compare block, a dedicated key must be written to the key register R5FSS_CCMKEYR1. R5FSS_CCMSR1 is the status register associated with this block.

Table 7-4 provides details on the operating modes of the CPU compare block.

Table 7-4. CPU Compare Block Operating Modes

Mode	Key(1)	Self Test Error Signal	Compare Error Signal	CMPE1(2)	STC1(3)	STET1(4)	STE1(5)
Compare block active	0000	Enabled	Enabled	Enabled	Disabled	Disabled	Disabled
Self test	0110	Enabled	Disabled	Disabled	Enabled	Enabled	Enabled
Error forcing	1001	Error	Error	Disabled	Disabled	Disabled	Disabled
Self test error forcing	1111	Error	Enabled	Enabled	Disabled	Disabled	Disabled

7.1.2.5.1.2 Compare Block Active Mode

In compare block active mode, the output signals of both CPUs are compared, and any difference in the outputs is indicated by the compare error signal. Additionally, as indicated in Section 7.1.2.5.1.1, the self test error signal is also asserted.

Note

The self test error signal is shared by both the CCMR5's CPU compare and inactivity monitor blocks.

Note

Not all flops inside the R5F CPU(s) are initialized at reset. To avoid an erroneous CCMR5 compare error, the application software needs to ensure that the CPU registers of both CPUs are initialized with the same values before the registers are used. This is to ensure that the programmer's model CPU registers of both CPU are initialized properly.

7.1.2.5.1.3 Self Test Mode

In self test mode, the CCMR5 compare block is checked for faults by applying internally generated series of test patterns. During self test, the core compare disabled signal is deactivated. If a fault on the CCMR5 module gets detected, a self test error is generated.

When self test mode is entered, the CCMR5 module will generate predetermined test patterns to look for any hardware faults inside it. If a fault is detected, then a self test error flag (STE1) is set, a self test error signal is asserted, and the self test is terminated immediately after entering compare mismatch mode. If no fault is found during self test, the self test complete flag (STC1) will be set. The user needs to poll the R5FSS_CCMSR1 status register to find out the self test status. In both cases – self test terminated and self test completed – the CCMR5 will remain in self test mode and will be idle, and therefore the R5FSS_CCMKEYR1 key register will show the self test key until the mode is switched by writing another key to this register. During the self test operation, the compare error signal output is inactive, irrespective of the compare result. When switched out of self test mode, the core compare disabled signal is de-asserted.

There are two types of patterns generated by CCMR5 during self test mode: compare match test, and compare mismatch test. The CCMR5 first generates compare match test patterns followed by compare mismatch test patterns. During self test, each test pattern is applied on CPU output signal ports of the CCMR5's compare block and clocked for one cycle.

Self test of CPU output compare logic is done with respect to CPU clock. As mentioned, self test error is indicated by the self test error signal. Whether the self test failed during compare match test or compare mismatch test is indicated by the self test error type flag (STET1) in the R5FSS_CCMSR1 status register. When the block's self test is completed, the corresponding self test complete flag (STC1) is set.

Note

During self test, both CPUs can execute normally, but the compare logic will not be checking any CPU signals. Also, during self test, only the compare unit logic is tested. The self test is not interruptible.

7.1.2.5.1.4 Compare Match Test

During compare match test, there are four different test patterns generated to stimulate the hardware. An identical vector is applied to both input ports (CPU0 and CPU1 output signals, which are inputs to the CCMR5 block) at the same time expecting a compare match. These patterns cause the self test logic to exercise every CPU output signal. This test can be independently enabled by programming the CCMR5 registers. If the compare unit produces a compare mismatch then the self test error flag is set and the self test error signal is generated. If an error is detected during compare match, then CCMR5 enters compare mismatch mode before terminating the test.

The four test patterns are:

- All 0's on both CPUs
- All 1's on both CPUs
- 0xA's on both CPUs
- 0x5's on both CPUs

These four test patterns will take four clock cycles to complete.

Table 7-5 illustrates the compare match test sequence. The core compare disabled signal is asserted on entry and de-asserted when complete.

Table 7-5. Compare Match Test Sequence

CPU0 Signal Position									CPU1 Signal Position									Cycle
n:8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**n:8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
0x5	0	1	0	1	0	1	0	1	0x5	0	1	0	1	0	1	0	1	0
0xA	1	0	1	0	1	0	1	0	0xA	1	0	1	0	1	0	1	0	1
0's	0	0	0	0	0	0	0	0	0's	0	0	0	0	0	0	0	0	2
1's	1	1	1	1	1	1	1	1	1's	1	1	1	1	1	1	1	1	3

7.1.2.5.1.5 Compare Mismatch Test

In compare mismatch test, the number of test patterns is equal to two times the number of CPU output signals to compare in compare mode active. The core compare disabled signal is asserted on entry and de-asserted when complete. An 'all-ones' vector is applied to the CCMR5's CPU0 input port and the same pattern is also applied to the CCMR5's CPU1 input port but with one bit flipped starting from signal position 0. The un-equal vector should cause the CCMR5 module to expect a compare mismatch at signal position 0. Note that a mismatch is an expected good result, while a match will indicate hardware fault. When a fault is detected, which means that a compare match is produced by the compare logic, the self test error flag is set and the self test error signal is asserted.

The above compare mismatch test algorithm repeats itself again in a domino fashion with next signal position flipped, while forcing all other signals to logic level '1'. This process is repeated until every single signal position is verified on both CPU signal ports.

The compare mismatch test is terminated if a compare match is detected and the module becomes idle. The compare mismatch test ensures that the compare unit is able to detect a mismatch on every CPU signal being compared.

Table 7-6 illustrates the compare mismatch test sequence.

Table 7-6. Compare Mismatch Test Sequence

CPU0 Signal Position										CPU1 Signal Position										Cycle
n	**...**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**n**	**...**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
1	1's	1	1	1	1	1	1	1	1	1	1's	1	1	1	1	1	1	1	0	0
1	1's	1	1	1	1	1	1	1	1	1	1's	1	1	1	1	1	1	0	1	1
1	1's	1	1	1	1	1	1	1	1	1	1's	1	1	1	1	1	0	1	1	2
1	1's	1	1	1	1	1	1	1	1	1	1's	1	1	1	1	0	1	1	1	3
										. .										
1	1's	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	n-1
1	1's	1	1	1	1	1	1	1	1	0	1's	1	1	1	1	1	1	1	1	n
1	1's	1	1	1	1	1	1	1	0	1	1's	1	1	1	1	1	1	1	1	n+1
1	1's	1	1	1	1	1	1	0	1	1	1's	1	1	1	1	1	1	1	1	n+2
1	1's	1	1	1	1	1	0	1	1	1	1's	1	1	1	1	1	1	1	1	n+3
1	1's	1	1	1	1	0	1	1	1	1	1's	1	1	1	1	1	1	1	1	n+4
										. .										
0	1's	1	1	1	1	1	1	1	1	1	1's	1	1	1	1	1	1	1	1	2n

7.1.2.5.1.6 Error Forcing Mode

In error forcing mode, a test pattern is applied to the CPU related inputs of the compare logic to force an error at the compare error signal of the compare unit. The core compare disabled signal is asserted on entry and de-asserted when complete.

This mode is enabled by writing the dedicated key in the R5FSS_CCMKEYR1 key register (see Table 7-4). The error signal is generated by asserting the CPU compare error signal.

Error forcing mode is similar to the compare mismatch test operation of self test mode, in which an un-equal vector is injected into the CCMR5 CPU signal ports. Instead of setting a self test error flag and asserting self test error signal, the error forcing mode forces the compare mismatch to set the compare error flag (CMPE1) and assert the compare error signal.

Only one hardcoded test pattern is applied into CCMR5 during error forcing mode. A repeated 0x5 pattern is applied to CPU0 signal port, while a repeated 0xA pattern is applied to the CPU1 signal port. The error forcing mode takes one cycle to complete. Hence, the failing signature is presented for one clock cycle and the mode is automatically switched to lockstep mode and the R5FSS_CCMKEYR1 key register will show the lockstep key (0000). During this cycle the CPUs are not compared. The user should expect to receive the error signal from CCMR5 module once the error forcing mode is entered. If no error signal is set, then a hardware fault is present.

7.1.2.5.1.7 Self Test Error Forcing Mode

In self test error forcing mode, an error is forced at the self test error signal. The compare unit is still running in lockstep mode and the key is switched to lockstep after one clock cycle. The core compare disabled signal is asserted on entry and de-asserted when complete.

7.1.2.5.2 Inactivity Monitor Block

Another function of the CCMR5 module is to monitor the inputs of bus matrix coming from the diagnostic R5F core (CPU1) in lockstep mode, to detect any transaction initiated by diagnostic core. Output signals from the diagnostic core, which indicate a valid transaction on a controller interface, are compared against their clamped values. If any signal value is different from its clamped value, an error signal is generated.

Table 7-7 shows the R5F diagnostic core output signals, which are being monitored to detect any activity in the processor bus.

Table 7-7. Inactivity Monitor Block Signals

Signal Name	Interface	Description	Clamp Value
AWVALIDM1	L2 AXI controller	Indicates write address and control are valid	0
ARVALIDM1	L2 AXI controller	Indicates read address and control are valid	0
AWVALIDP1	AXI PP(1)	Indicates write address and control are valid	0
ARVALIDP1	AXI PP(1)	Indicates read address and control are valid	0
HTRANSP1[1:0]	AHB PP	Indicates the type of transfer – idle (00), busy (01), non-sequential (10), sequential (11)	0
BVALIDS1	AXI peripheral	Indicates valid write response is available	0
RVALIDS1	AXI peripheral	Indicates Read Data Channel Address and Control are valid	0
ATCEN01	ATCM	Enable for ATCM lower word	0
ATCEN11	ATCM	Enable for ATCM upper word	0
B0TCEN01	B0TCM	Enable for B0TCM lower word	0
B0TCEN11	B0TCM	Enable for B0TCM upper word	0
B1TCEN01	B1TCM	Enable for B1TCM lower word	0
B1TCEN11	B1TCM	Enable for B1TCM upper word	0

(1) Not supported for R5FSS0

More details on these signals can be found in the *Arm Cortex-R5 Technical Reference Manual*.

The error response in case of a detected transaction is indicated by the bus monitor error signal.

7.1.2.5.2.1 Operating Modes

The inactivity monitor block can run in one out of four operating modes:

- Compare active block
- Self test
- Error forcing
- Self test error forcing

To select an operating mode for the inactivity monitor block, a dedicated key must be written to the key register R5FSS_CCMKEYR3. R5FSS_CCMSR3 is the status register associated with this block.

Table 7-8 provides details on the operating modes of the inactivity monitor block.

Table 7-8. Inactivity Monitor Block Operating Modes

Mode	Key[1]	Self Test Error Signal	Compare Error Signal[2]	CMPE3[3]	STC3[4]	STET3[5]	STE3[6]
Compare block active	0000	Enabled	Enabled	Enabled	Disabled	Disabled	Disabled
Self test	0110	Enabled	Disabled	Disabled	Enabled	Enabled	Enabled
Error forcing	1001	Error	Error	Disabled	Disabled	Disabled	Disabled
Self test error forcing	1111	Error	Enabled	Enabled	Disabled	Disabled	Disabled

(1) R5FSS_CCMKEYR3[3:0] MKEY3 bit field
(2) Corresponds to bus monitor error signal for inactivity monitoring
(3) R5FSS_CCMSR3[16] CMPE3: Compare error (bus monitor error) flag
(4) R5FSS_CCMSR3[8] STC3: Self test complete flag
(5) R5FSS_CCMSR3[1] STET3: Self test error type flag
(6) R5FSS_CCMSR3[0] STE3: Self test error flag

7.1.2.5.2.2 Compare Block Active Mode

In compare block active mode, the output signals of CPU1 (after clamping) are compared against their clamped values, and a mismatch is indicated by the bus monitor error signal. Additionally, as indicated in Table 7-8, the self test error signal is also asserted.

Note

The self test error signal is shared by both the CCMR5's CPU compare and inactivity monitor blocks.

7.1.2.5.2.3 Self Test Mode

Inactivity monitor has a self test feature and self test is done by applying a predetermined set of internally generated test patterns on the Inactivity Monitor inputs. For the fault detection, the comparison is done against the clamped values. The generated patterns are same as output compare block test patterns, but they are applied on every HCLK cycles. Any fault detected is indicated by the self test error signal. If no fault is found during self test, the self test complete flag (STC3) will be set. The user needs to poll the R5FSS_CCMSR3 status register to find out the self test status. In both cases – self test terminated and self test completed – inactivity monitor will remain in self test mode and will be idle, and therefore the R5FSS_CCMKEYR3 key register will show the self test key until the mode is switched by writing another key to this register.

Note

Bus monitor error is disabled during self test mode.

Two types of test patterns are applied for inactivity monitor self test:

- Compare match pattern
- Compare mismatch pattern

Self test takes 16 cycles to complete. Self test error is indicated by the self test error signal. Whether the self test failed during compare match test or compare mismatch test is indicated by the self test error type flag (STET3) in the R5FSS_CCMSR3 status register. When the block’s self test is completed, the corresponding self test complete flag (STC3) is set.

7.1.2.5.2.4 Compare Match Test

In compare match test, patterns are applied such that no compare error is generated. Because the comparison is done against the clamped values, and all compared signals are clamped to zero, only one test pattern is applicable for compare match test. A pattern of 'all-zeros' is applied for compare match test. If a compare mismatch is found, then self test error flag (STE3) is set and self test error is asserted. If an error is detected during compare match, then CCMR5 enters compare mismatch mode before terminating the test. If no mismatch is found, compare mismatch test is done next.

7.1.2.5.2.5 Compare Mismatch Test

In compare mismatch test, a series of un-equal test patterns are applied on inactivity monitor inputs. Un-equal vectors are expected to generate a compare mismatch and a compare match indicates a fault. If a compare match is found, self test error flag is set and a self test error is indicated. Self test is terminated as well. If all patterns are generating mismatch, self test complete flag (STC3) is set.

Table 7-9 shows the patterns used for compare mismatch test.

Table 7-9. Inactivity Monitor Compare Mismatch Patterns

Inactivity Monitor Compare Mismatch Patterns												Cycle
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	1	0	0	2
0	0	0	0	0	0	0	0	1	0	0	0	3
0	0	0	0	0	0	0	1	0	0	0	0	4
0	0	0	0	0	0	1	0	0	0	0	0	5
0	0	0	0	0	1	0	0	0	0	0	0	6
0	0	0	0	1	0	0	0	0	0	0	0	7
0	0	0	1	0	0	0	0	0	0	0	0	8
0	0	1	0	0	0	0	0	0	0	0	0	9
0	1	0	0	0	0	0	0	0	0	0	0	10
1	0	0	0	0	0	0	0	0	0	0	0	11

7.1.2.5.2.6 Error Forcing Mode

In error forcing mode, a test pattern is applied to inactivity monitor inputs of the compare logic to force an error at the compare error signal of the compare unit. Only one hardcoded test pattern of 'all-ones' is applied into CCMR5 during error forcing mode. The error forcing mode takes one cycle to complete. Hence, the failing signature is presented for one clock cycle and the mode is automatically switched to lockstep mode and the R5FSS_CCMKEYR3 key register will show the lockstep key (0000). During this cycle the bus monitoring is disabled.

7.1.2.5.2.7 Self Test Error Forcing Mode

In self test error forcing mode, an error is forced at the self test error signal. The compare unit is still running in lockstep mode and the key is switched to lockstep after one clock cycle.

7.1.2.5.3 Polarity Inversion Logic

As already mentioned, there is logic (implemented via XOR) to test the comparison logic itself. The CCMR5 block can be configured to be in self test to check the integrity of the final XOR error generation logic, and can be switched back to functional compare mode after self test completion. To ensure that switching back to functional mode has happened, user can program CCMR5 polarity control register (R5FSS_CCMPOLCNTRL) to invert the polarity of eight CPU output signals, which will cause a CPU compare error generation. The eight signals that are chosen to be able to control the polarity are: AWVALIDMm, RVALIDSm, ATCEN0m, B0TCEN0m, BITCWEm, IRQACKm, AWVALIDPm, HWRITEP. See the *Arm Cortex-R5 Technical Reference Manual* for details on these signals.

The XOR inversion is placed between the two back-to-back delay flops of CPU1 outputs. Note that the XOR inversion logic is a diagnostic feature. If user does not observe a CPU compare error generation after programming the R5FSS_CCMPOLCNTRL[7:0] POL_INV inversion bits, this means that:

1. All eight signals of the inversion logics (XOR) are faulty and CPU compare error signal is not asserted. This is a very difficult case to hit but theoretically it could happen if a hard fault gets accumulated over times on these polarity inversion XOR gates; OR

2. The CCMR5 block has not switched back to functional mode yet

User can perform self test again to identify whether the issue is #1 or #2. If the second self test passes that means the issue is #1.

7.1.2.6 R5FSS Vectored Interrupt Manager (VIM)

7.1.2.6.1 VIM Overview

The VIM aggregates device interrupts and sends them to the R5F CPU(s). It can be used in either split or lockstep configuration. In split, it has two independent interrupt cores, one per CPU. In lockstep, CPU1 acts as a diagnostic on CPU0; only CPU0's outputs are used but all outputs are compared to CPU1 to provide diagnostic coverage.

The VIM module supports the following features:

- 512 interrupt inputs per R5F core
- Each interrupt has its own 4-bit programmable priority
  - Defined via the R5FSS_VIM_PRI_INT_j register
  - The VIM provides support for priority interruption of interrupts
- Each interrupt has its own enable mask
  - Interrupt enable is done via the R5FSS_VIM_INTR_EN_SET_j register
  - Interrupt disable is done via the R5FSS_VIM_INTR_EN_CLR_j register
- Each interrupt can be programmed as either an IRQ or FIQ
  - Defined via the R5FSS_VIM_INTMAP_j register
- Each interrupt has its own programmable 32-bit vector address associated with it
  - Defined via the R5FSS_VIM_VEC_INT_j register
  - Protected with SECDED
- One IRQn and one FIQn output per core
- Vectored interrupt interface
  - Compatible with R5F VIC port
- Default vector provided when a double-bit error is detected
- Split or lockstep capable
  - In lockstep mode, only interrupts connected to VIM interrupt core 0 are available
- Software interrupt generation

7.1.2.6.2 VIM Interrupt Inputs

The VIM supports 512 interrupt inputs per core. Each interrupt can be either a level or a pulse (both active-high). The interrupt mapping for the two R5F cores can be found in *Interrupt Sources*.

7.1.2.6.3 VIM Interrupt Outputs

The VIM has two interrupt outputs per core:

- *CoreN_IRQn*: This is a normal interrupt for core *N* (active-low level). It can be serviced via the VIC interface or through the MMR interface. Whenever an interrupt input goes high, if that interrupt is mapped as an IRQ (via the R5FSS_VIM_INTMAP_j register) and is enabled (via the R5FSS_VIM_INTR_EN_SET_j register), then it will cause an IRQ to assert
- *CoreN_FIQn*: This is a fast (or non-maskable) interrupt for core *N* (active-low level). FIQs always have priority over IRQs. An FIQ can be serviced through the MMR interface. Whenever an interrupt input goes high, if that interrupt is mapped as an FIQ and is enabled, then it will cause an FIQ to assert

7.1.2.6.4 VIM Interrupt Vector Table (VIM RAM)

For each VIM interrupt core, there is an associated interrupt vector table (VIM RAM) that is used to store the address of ISRs. During register vectored interrupt and hardware vectored interrupt, VIM accesses the interrupt vector table using the vector value to fetch the address of the corresponding ISR. Note that both interrupt vector tables are identical in their memory organization.

The VIM RAM is basically comprised of a set of interrupt vector registers (R5FSS_VIM_VEC_INT_j). Hence, the interrupt vector table is organized in 512 words of 30 bits, with a base address corresponding to the physical address of the first register in the group.

Note

The lower two bits of the 32-bit interrupt vector are always 0s.

Figure 7-2 shows the VIM RAM interrupt vector map.

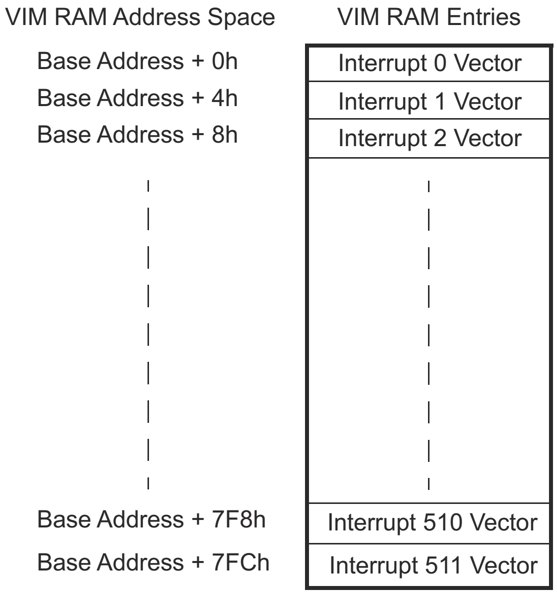


Figure 7-2. VIM RAM Interrupt Vector Map

The interrupt vector table has protection by ECC to indicate corruption due to soft errors. The ECC logic inside VIM supports SECDED. See Table 7-10 for the VIM RAM ID in the ECC aggregator map.

7.1.2.6.5 VIM Interrupt Prioritization

Each interrupt has a priority number assigned to it (set using the R5FSS_VIM_PRI_INT_j register). Legal values are 0 to 15, where 0 is the highest priority and 15 is the lowest priority. The highest priority interrupt is the pending interrupt with the smallest priority number. If two pending interrupts have the same priority, the interrupt lowest numerically (0 through maximum number of interrupts) is prioritized. IRQs and FIQs are prioritized separately.

The VIM supports the interruption of the currently active interrupt by one with a higher priority. FIQs and IRQs are completely separate but both use the same mechanism.

When an interrupt goes from pending to active (FIQ: reading the R5FSS_VIM_FIQVEC register; IRQ: reading the R5FSS_VIM_IRQVEC register, or the *coreN_IRQACK* going high), then the interrupt is loaded into the corresponding active register (R5FSS_VIM_ACTFIQ / R5FSS_VIM_ACTIRQ), and all interrupts of an equal or lesser priority are masked (discarded). If prior to this interrupt being cleared (by writing to the R5FSS_VIM_FIQVEC register, or R5FSS_VIM_IRQVEC register) another interrupt of higher priority arrives, then the FIQn/IRQn will be asserted and that interrupt made pending as normal. The CPU may or may not service the higher priority interrupt. If the CPU switches this interrupt to active (by reading the R5FSS_VIM_FIQVEC / R5FSS_VIM_IRQVEC register, or (or *coreN_IRQACK* going high for an IRQ), then the currently active interrupt will be pushed onto a stack. When an interrupt is cleared by writing to the R5FSS_VIM_FIQVEC / R5FSS_VIM_IRQVEC register, if there are any interrupts on the stack, the first entry is popped off and put back into the R5FSS_VIM_ACTFIQ / R5FSS_VIM_ACTIRQ register, so that software may continue where it left off. Note that the R5FSS_VIM_IRQVEC / R5FSS_VIM_FIQVEC address registers are not repopulated with the old vector as it is assumed that the ISR is picking back up where it left off. Only the interrupt number and priority are restored to the R5FSS_VIM_ACTIRQ / R5FSS_VIM_ACTFIQ registers. If software needs the vector again, it will have to read it by using the interrupt number.

7.1.2.6.6 VIM ECC Support

The memory that holds the interrupt vector for each interrupt is protected by SECDED ECC. Single-bit errors are corrected and written back. Double-bit errors are not corrected. If a double-bit error occurs while trying to load a vector, then the R5FSS_VIM_DEDVEC register is used to provide the default vector for the *coreN_IRQADDRV* signal, the R5FSS_VIM_IRQVEC register, and the R5FSS_VIM_FIQVEC register. The R5FSS_VIM_DEDVEC should point to an ISR that handles the fact that there was an uncorrectable error in the interrupt handling.

Some possible remediating actions would be to:

1. Reconstruct the vector table and re-start the application
   a. Potentially switch to a completely software interrupt handler in the mean time
2. Restart the application from scratch
3. Reset the device
4. Sit in a loop (or WFI) while something external (for example, the ESM) responds to the DED interrupt that will be generated

It is up to the user and the application to determine the appropriate action.

Note

An interrupt that has an uncorrectable vector error (and thus uses the DED vector) will still have the priority of the original interrupt . This makes it possible for a higher priority interrupt to supercede the handling of the error.

Control and reporting are done by the R5FSS ECC aggregator.

7.1.2.6.7 VIM Lockstep Mode

In lockstep mode, CPU1 is used as a diagnostic for CPU0. In this mode, only the interrupt inputs for CPU0 are used. Besides to CPU0, these interrupt inputs are also internally routed to CPU1 (through the level-sync / edge-detect logic dedicated to CPU1, and additionally through some delay circuits). The outputs from both VIM interrupt cores are then sent to the R5FSS CCMR5 module through dedicated compare buses (with CPU0's outputs delayed). The CCMR5 module is responsible for comparing the two sets of output signals and for reporting any mismatches by generating a VIM bus compare interrupt.

Note

In lockstep mode, only the VIM RAM dedicated to CPU0 is used, so software *must not* do anything with the ECC interface on the VIM RAM dedicated to CPU1.

7.1.2.6.8 VIM IDLE State

The VIM will indicate IDLE when there are no pending unmasked interrupts or MMR accesses. The VIM does not have a clock stop interface.

7.1.2.6.9 VIM Interrupt Handling

There are multiple ways to service an interrupt depending on how much of the hardware assistance offered by the VIM the software wants to take advantage of.

For IRQs, it is recommended to use the procedure in Section 7.1.2.6.9.1, but the procedures in Section 7.1.2.6.9.2 or Section 7.1.2.6.9.3 (if a user wants to implement a fully software prioritization scheme) may be used as alternatives.

For FIQs, it is recommended to use the procedure in Section 7.1.2.6.9.4, but the procedure in Section 7.1.2.6.9.5 may be used as an alternative.

Note

These descriptions do not include steps such as stack pushes and state retention that software must take in order to return from the ISR. It is assumed that the programmer is aware of these steps.

7.1.2.6.9.1 Servicing IRQ Through Vector Interface

If the associated CPU has the vector (VIC) interface enabled, then the following method is used for servicing IRQs:

1. Hardware handshake
    a. CPU asserts *coreN_IRQACK* high
    b. VIM asserts *coreN_IRQADDRV* to indicate that the *coreN_IRQADDR* bus is stable with the correct vector address
    c. CPU reads *coreN_IRQADDR*, jumps to that address, and de-asserts *coreN_IRQACK* low
    d. VIM de-asserts *coreN_IRQn* and *coreN_IRQADDRV*, VIM masks (discards) all IRQs with the same or lower priority
    e. VIM loads the value from the R5FSS_VIM_PRIIRQ[9:0] NUM bit field (which corresponds to the vector address) into the R5FSS_VIM_ACTIRQ[9:0] NUM bit field, which causes the R5FSS_VIM_ACTIRQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (determined by reading the R5FSS_VIM_ACTIRQ[9:0] NUM bit field to determine number, and reading the appropriate bit in the R5FSS_VIM_INTTYPE_j register to determine type)
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_IRQSTS_j register, or R5FSS_VIM_STS_j register
        ii. Clear the interrupt at the source. This way, the source can generate another pulse, if it needs to, and the VIM will process this as a new interrupt
    b. Level
        i. Clear the interrupt at the source
        ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_IRQSTS_j register, or R5FSS_VIM_STS_j register. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt. If the source maintains the level, then it means there is another interrupt
4. Write any value to the R5FSS_VIM_IRQVEC register
    a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    b. This will also clear the R5FSS_VIM_ACTIRQ[31] VALID bit

7.1.2.6.9.2 Servicing IRQ Through MMR Interface

When an IRQ interrupt is received, the CPU should follow these steps if not using the vector interface:

1. Read the R5FSS_VIM_IRQVEC register and jump to that address to service the ISR
    a. Reading this register will mask (discard) all interrupts of an equal or lower priority and de-assert the *coreN_IRQn* output. If another interrupt of a higher priority becomes available, the *coreN_IRQn* will re-assert, allowing priority interruption of an interrupt
    b. Reading this register will cause the value from the R5FSS_VIM_PRIIRQ[9:0] NUM bit field to be loaded into the R5FSS_VIM_ACTIRQ[9:0] NUM bit field, and the R5FSS_VIM_ACTIRQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
    a. Pulse
        i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register

        - ii. Clear the interrupt at the source
    - b. Level
        - i. Clear the interrupt at the source
        - ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register

4. Write any value to the R5FSS_VIM_IRQVEC register
    - a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
    - b. This will also clear the R5FSS_VIM_ACTIRQ[31] VALID bit

7.1.2.6.9.3 Servicing IRQ Through MMR Interface (Alternative)

If a user does not want to use the R5FSS_VIM_IRQVEC register, the VIM may be used as a more traditional interrupt controller. Note that in this mode, priority masking will not work if route 1b is used (see below) as the hardware prioritization may not match the software prioritization scheme. In this case, software would be responsible for doing all priority operations.

1. Determine which interrupt to service
    - a. Read the R5FSS_VIM_PRIIRQ register to determine which interrupt is the highest priority IRQ currently asserted, OR
    - b. Optionally read the R5FSS_VIM_IRQGSTS register to determine which groups have IRQs pending, then read the R5FSS_VIM_IRQSTS_j register and use a software prioritization scheme to determine which IRQ to service
2. Service the interrupt
3. Read the R5FSS_VIM_IRQVEC register
    - a. Note that this step can be done any time before step 4
    - b. Value is ignored
4. Depending on whether the original source of the interrupt was a pulse or a level
    - a. Pulse
        - i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
        - ii. Clear the interrupt at the source.
    - b. Level
        - i. Clear the interrupt at the source
        - ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_IRQSTS_j register
5. Write any value to the R5FSS_VIM_IRQVEC register

7.1.2.6.9.4 Servicing FIQ

When an FIQ interrupt is received, the CPU should follow these steps:

1. Read the R5FSS_VIM_FIQVEC register and jump to that address to service the ISR
    - a. Reading this register will mask (discard) all interrupts of an equal or lower priority and de-assert the *coreN_FIQn* output. If another interrupt of a higher priority becomes available, the *coreN_FIQn* will re-assert, allowing priority interruption of an interrupt.
    - b. Reading this register will cause the value from the R5FSS_VIM_PRIFIQ[9:0] NUM bit field to be loaded into the R5FSS_VIM_ACTFIQ[9:0] NUM bit field, and the R5FSS_VIM_ACTFIQ[31] VALID bit to be set
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level (determined by reading the R5FSS_VIM_ACTFIQ[9:0] NUM bit field to determine number, and reading the appropriate bit in the R5FSS_VIM_INTTYPE_j register to determine type)

   a. Pulse
      i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register
      ii. Clear the interrupt at the source. This way, the source can generate another pulse, if it needs to, and the VIM will process this as a new interrupt
   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register. This way, the level should be gone at the input to the VIM, it will avoid falsely re-calling the interrupt. If the source maintains the level, then it means there is another interrupt

4. Write any value to the R5FSS_VIM_FIQVEC register
   a. This will clear the priority mask and will cause all interrupts to be re-evaluated for the new highest priority interrupt
   b. This will also clear the R5FSS_VIM_ACTFIQ[31] VALID bit

7.1.2.6.9.5 Servicing FIQ (Alternative)

If a user does not want to use the R5FSS_VIM_FIQVEC register, the VIM may be used as a more traditional interrupt controller. Note that in this mode, there is no hardware priority masking (because the R5FSS_VIM_FIQVEC register is never read). Software would be responsible for doing all priority operations.

1. Determine which interrupt to service
   a. Read the R5FSS_VIM_FIQVEC register to determine which interrupt is the highest priority FIQ currently asserted, OR
   b. Optionally read the R5FSS_VIM_FIQGSTS register to determine which groups have IRQs pending, then read the R5FSS_VIM_FIQSTS_j register and use a software prioritization scheme to determine which FIQ to service
2. Service the interrupt
3. Depending on whether the original source of the interrupt was a pulse or a level
   a. Pulse
      i. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register
      ii. Clear the interrupt at the source.
   b. Level
      i. Clear the interrupt at the source
      ii. Clear the status by writing a '1' to the appropriate bit in the R5FSS_VIM_STS_j register, or R5FSS_VIM_FIQSTS_j register.

7.1.2.7 R5FSS Region Address Translation (RAT)

7.1.2.7.1 RAT Overview

The R5F is a 32-bit processor, which means it can only access 4GB of directly addressable memory. The SoC is a 64-bit virtual (48-bit physical) address system. The R5FSS integrates a standard region-based address translation (RAT) unit (per core) to allow some of its address space to be remapped into the 64-bit world.

The RAT has 16 regions, with each region having dedicated MMRs that define its attributes:

- Base address of the region, defined via R5FSS_RAT_BASE_j[31-0] BASE
- Size of the region, defined via R5FSS_RAT_CTRL_j[5-0] SIZE
- Translated base address, defined via R5FSS_RAT_TRANS_U_j[15-0] UPPER and R5FSS_RAT_TRANS_L_j[31-0] LOWER

Regions can have any base address and size, as long as the base address is size aligned. The maximum region size is 4GB.

Note

The RAT does not provide any logic for checking if base address is size aligned, so it is software's responsibility to ensure that. Regions that are not aligned may have unpredictable results.

7.1.2.7.2 RAT Operation

The RAT works by translating a 32-bit input address into a 48-bit output address. Any input transaction that starts inside of a programmed region will have its address translated, if the region is enabled. Any disabled region is ignored from the translation lookup.

The input addresses are compared against all the enabled regions in parallel. The region size defines how many of the lowest address bits are included in the region space, starting from a 1B space to a 4GB space. Then the upper bits not part of the region are used for the lookup and comparison, matching those bits of the input addresses against the region base address. The region matches when it is enabled and the compare matches. The first region that matches has the output address set with the region's translated base address upper bits. The lower bits that are part of the region size are copied from the input address to the output address. If there are no region matches then the input address is copied to the output address entirely.

Note

Multiple region definitions must not overlap in their covered address space. The RAT does not check for this, so it is software's responsibility to take care of it. Overlapping regions may have unpredictable results.

Here is an example of a region-based address translation, assuming that region [0] is programmed as follows:

- Region [0] base address = 0x1234_5XXX
- Region [0] size = 4KB
- Region [0] translation upper address = 0x0000_ABCD
- Region [0] translation lower address = 0x5432_1XXX

If a transaction comes in with the address 0x1234_5678, then the output transaction will have the address 0x0000_ABCD_5432_1678.

7.1.2.7.3 RAT Error Logging

The RAT does not provide any protection against transactions that cross region boundaries, that is, start inside of a region and end outside of it, or start outside of a region and end inside of it. If a boundary crossing transaction is detected, then the transaction will be flagged as an error (exception) and a log will be made. The log consists of a series of MMRs that captures the details of the transaction, including the input address that caused the error. The RAT module can capture one error before it is cleared by software. Here is the list of exception logging registers:

- Control:
  - R5FSS_RAT_EXCEPTION_LOGGING_CONTROL
- Header:
  - R5FSS_RAT_EXCEPTION_LOGGING_HEADER0
  - R5FSS_RAT_EXCEPTION_LOGGING_HEADER1
- Data:
  - R5FSS_RAT_EXCEPTION_LOGGING_DATA0
  - R5FSS_RAT_EXCEPTION_LOGGING_DATA1
  - R5FSS_RAT_EXCEPTION_LOGGING_DATA2
  - R5FSS_RAT_EXCEPTION_LOGGING_DATA3

The log also produces an interrupt. To clear the log, software must either read the final error logging register, or manually clear the interrupt status bit. This will clear the error status, and not the actual log MMRs, but it does allow the next error to be captured into the log MMRs. If the status is not cleared and additional errors are detected, they are not logged.

The error reports use the value from a dedicated bootstrap (see Section 7.1.2.2.5) as the value for the R5FSS_RAT_EXCEPTION_LOGGING_HEADER0[23-8] SRC_ID field.

7.1.2.7.4 RAT Protection

As mentioned, the RAT module does not provide any protection by itself. The intention is that RAT is used in conjunction with memory protection unit (MPU) and system firewalls for protection. It is recommended that one or more RAT regions are directly mapped to an MPU region to provide 'MMU-like' behavior.

7.1.2.8 R5FSS ECC Support

The R5F provides native ECC and parity support on all related memories, generating and checking the redundancy automatically. The methods for checking and reporting errors are available in the *Arm Cortex-R5 Technical Reference Manual*.

The R5FSS adds the capability of testing this logic by allowing errors (single and double bit) to be injected into memories (for testing purposes) via an ECC aggregator (per core). Note that because the R5FSS ECC aggregator is only used in error-injection mode, it only supports a subset of the generic ECC aggregator functionality in the device.

For a detailed description of the generic ECC aggregator functionality, see , *ECC Aggregator*. For register descriptions of R5FSS CPU0 and CPU1 ECC aggregators, see *ECC Registers*.

Table 7-10 provides the RAM ID for each core. This is needed for bit field [10-0] ECC_VECTOR in the corresponding R5FSS_CPU0_VECTOR / R5FSS_CPU1_VECTOR register.

Table 7-10. RAM ID Map for ECC Aggregator (Per Core)

RAM ID	Memory Name
0	CPU0/1 ITAG RAM0
1	CPU0/1 ITAG RAM1
2	CPU0/1 ITAG RAM2
3	CPU0/1 ITAG RAM3
4	CPU0/1 IDATA BANK0
5	CPU0/1 IDATA BANK1
6	CPU0/1 IDATA BANK2
7	CPU0/1 IDATA BANK3
8	CPU0/1 DTAG RAM0
9	CPU0/1 DTAG RAM1
10	CPU0/1 DTAG RAM2
11	CPU0/1 DTAG RAM3
12	CPU0/1 DDIRTY RAM
13	CPU0/1 DDATA RAM0
14	CPU0/1 DDATA RAM1
15	CPU0/1 DDATA RAM2
16	CPU0/1 DDATA RAM3
17	CPU0/1 DDATA RAM4
18	CPU0/1 DDATA RAM5
19	CPU0/1 DDATA RAM6
20	CPU0/1 DDATA RAM7
21	CPU0/1 ATCM BANK0
22	CPU0/1 ATCM BANK1
23	CPU0/1 B0TCM BANK0

Table 7-10. RAM ID Map for ECC Aggregator (Per Core) (continued)

RAM ID	Memory Name
24	CPU0/1 B0TCM BANK1
25	CPU0/1 B1TCM BANK0
26	CPU0/1 B1TCM BANK1
27	CPU0/1 VIM RAM

7.1.2.9 R5FSS Memory View

The memory view of each R5F (that is, the memory map as seen by each R5F) is a function of several things:

- Exception vector bootstrap: The R5F exception table (including boot vector) is always 32 bytes at address 0x00000000 as seen by the R5F. If not booting from a TCM, then boot is done over the main memory interface. The exception vector bootstrap is under software control, which allows these 32 bytes at address 0x00000000 to be remapped somewhere else in the SoC memory map.
- TCM locations: TCMs can be enabled or disabled and located at different places in the memory map, depending on bootstrap configuration. For more details, see Section 7.1.2.2.5, and Section 7.1.2.2.2.
- Peripheral interface locatons: The RF5 natively supports three interfaces for peripheral access. Each can be enabled/disabled and located based on bootstrap configuration. Note that the VBUSP peripheral interface must be enabled in order to use RAT and VIM.
- RAT base address: This is determined by a bootstrap. This address is located within the VBUSP peripheral interface address space.
- VIM base address: This is determined by a bootstrap. This address is located within the VBUSP peripheral interface address space.
- RAT programming: The RAT can take regions of memory accessible by the main memory interface and map them to different addresses.

The combination of the above determines what the R5F sees where in the memory map, and over what interface different transactions come out. Every transaction that does not directly address a TCM or a peripheral interface comes over the main memory interface. Transactions on the main memory interface can be further remapped with the RAT.

See *Memory Map*, for the complete R5F memory view for this device.

7.1.2.10 R5FSS Interrupts

All interrupts that are generated by the R5FSS are summarized in *MCU_R5FSS0 Hardware Requests*, along with their mapping. They can be divided into the following groups:

- R5F CPU internal interrupts: These are described in *Arm Cortex-R5 Technical Reference Manual*.
- CCMR5 interrupts: These are described in Section 7.1.2.5.
- ECC aggregator interrupts: These are described in the *ECC Aggregator* chapter.
- RAT exception interrupt: This is described in Section 7.1.2.7.

7.1.2.11 R5FSS Debug and Trace

The R5FSS supports standard Arm CoreSight debug and trace architecture. For more details, see the *On-chip Debug* chapter.

7.1.2.12 R5FSS Boot Options

There are two methods of booting the R5F, or rather, two methods of placing the exception vectors (of which the boot vector is one).

The first method is to have the exception vectors external to the R5F. The user can place the exception vectors at the address indicated by the exception vector bootstrap and then program the boot vector there. When the processor exits reset, it will fetch the boot vector from this location.

The second method is to boot from a TCM. To do this, software should take the following steps:

1. Assert the correct bootstraps
    a. To boot from ATCM, set CPUn_INITRAMA (or CPUn_INITRAMB to boot from BTCM)

   b. Assert CPUn_LOCZRAMA properly for the desired TCM

2. Assert CPUn_HALT
3. Release the CPU from reset
4. Load the desired code into the TCM via the TCM slave port
   a. Exception vectors should be located at address 0x00000000 of the TCM
5. De-assert CPUn_HALT

7.1.2.13 R5FSS Core Memory ECC Events

The R5F core generates several events as part of event bus that can be monitored by the PMU for debugging. The memory ECC related events from the event bus are exported to ESM for monitoring.

There are four ECC interrupts to the ESM that aggregate different categories of ECC events – CPU0 single error, CPU0 multi error, CPU1 single error, and CPU1 multi error events. Each ECC event has a 2-bit event bus counter associated with it. Everytime an event occurs, the counter is incremented by 1 till it reaches the max value of 3. The interrupt is asserted if the bus counter of any event associated with the interrupt is non-zero.

Each event bus counter has a MMR decrement control to decrement the counter by 1. So, for example, if a counter value is 2, the MMR to decrement the counter would need to be written 2 times to decrement the counter to 0. The reason decrement control has been added instead of clear control is if a new error occurs between the time the status register is read and the clear MMR is written, the new error would be lost. Write-to-decrement ensures that this does not happen.

When all event bus counters of an associated interrupt are zero, the interrupt is cleared. It takes three clock cycles for the event bus counter to be decremented once the write to the decrement control MMR presents itself at the R5FSS boundary.

Since each of the four ECC interrupts have single bit control to set the interrupt but multiple bits for clearing it, note that once an interrupt is set using the R5FSS_EVNT_BUS_ESM_SET register, it can be cleared by setting all the bits of the R5FSS_EVNT_BUS_ESM_CLR register that correspond to that particular interrupt. For example, if bit [0] of the R5FSS_EVNT_BUS_ESM_SET register is set, it can be cleared by setting bits [7-0] of the R5FSS_EVNT_BUS_ESM_CLR register to clear the interrupt.

The R5F core event bus only signals event when it is enabled. Non-invasive or invasive debug mode needs to be enabled to enable the PMU counters.

The export of the events to the event bus can be enabled by setting the X bit in the Performance Monitor Control Register of the R5F core. For more details, refer to *Arm R5 TRM*.

Table 7-11. R5FSS Event Bus Single-Bit Error Events

Event Bus Bit #	Description	Associated Status Register
22	Instruction cache tag RAM parity or correctable ECC error	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS0 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS0
23	Instruction cache data RAM parity or correctable ECC error	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS1 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS1
24	Data cache tag or dirty RAM parity error or correctable ECC error, from data-side or ACP	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS2 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS2
25	Data cache data RAM parity error or correctable ECC error	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS3 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS3
40	ATCM single-bit ECC error	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS4 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS4
41	B0TCM single-bit ECC error	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS5 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS5
42	B1TCM single-bit ECC error	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS6 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS6
43	TCM correctable ECC error reported by load/ store unit	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS7 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS7

Table 7-11. R5FSS Event Bus Single-Bit Error Events (continued)

Event Bus Bit #	Description	Associated Status Register
44	TCM correctable ECC error reported by prefetch unit	R5FSS_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS8 R5FSS_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS[0] EVNT_BUS8

Table 7-12. R5FSS Event Bus Multi-Bit Error Events

Event Bus Bit #	Description	Associated Status Register
26	TCM fatal ECC error reported from the prefetch unit	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS0 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS0
27	TCM fatal ECC error reported from the load/ store unit	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS1 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS1
33	Data cache data RAM fatal ECC error	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS2 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS2
34	Data caches tag/dirty RAM fatal ECC error, from data-side or ACP	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS3 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS3
37	ATCM multi-bit ECC error	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS4 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS4
38	B0TCM multi-bit ECC error	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS5 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS5
39	B1TCM multi-bit ECC error	R5FSS_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS6 R5FSS_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS[0] EVNT_BUS6

7.2 DSP Processing (C7x256v)

DSP features:

Note

Features are common to DSP0 and DSP1 unless otherwise specified

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- 1.0 GHz at 0.85V and 850MHz at 0.75V
- C7x ISA and RISC-V G ISA extensions
  - Vector DSP, 40 GFLOPS
  - 256-bit vector width
  - **DSP0 Only:** Deep-learning Matrix Multiply Accelerator Version 2F (MMA2F) with floating point support
- L1 memory architecture
  - 32KB I-cache
  - 64KB D-cache
- L2 memory architecture
  - 2.25 MB L2 with ECC protection on L2 SRAM
    - 2.25MB is managed as 2MB segment named "Main" and a 256KB segment named "Auxiliary"
    - Continuous L2 memory view
  - Unified Memory Controller (UMC) facilitates L2 SRAM accesses from CPU and SOC (DMAs) as well as EMIF accesses from CPU.
  - DRU (DMA engine) integrated that facilitates data transfer between L2 and system memories
    - Event bus interfaces integrates with SOC DMS
    - Tightly couples with C7x/MMA (DRU is not available for use when the C7x/MMA is disabled) and indirect predictor
  - Full ECC support with RMW
- Interrupts
  - Local event controller (CLEC) integrated within CorePac for routing and handling of DRU interrupts, CPU generated IPC events to SOC, interrupts coming from SOC
- Security
  - Support for C7x Authenticated Boot. Security is in-context during boot to facilitate the authentication and loading of the C7x image.
  - The C7x L2 SRAM (UMC) should not be used for storing security content as there is no protection of UMC memory from C7x itself. In a threat scenario, the C7x can be activated if in reset to execute malicious code to access data in UMC thereby defeating a protection for security data in UMC.
  - No security should be inferred from DRU as this IP is out of scope for security.
  - TrustZone debug controls (DBGEN, NIDEN, SPIDEN, SPNIDEN) are supported
  - C7x data and configuration paths are not in-scope from security standpoint
    - SOC shall support overriding the credentials (secure, priv-id) of all IP initiator ports. (e.g. via ISC)
- Safety
  - Support for reporting safety errors to SOC via interrupt
- Debug
  - Independent debug interface supporting access to embedded features
  - Debug features include: Core debug, Advanced Event Triggering, Trace, CTSETs, and an embedded CP Tracer Aggregator with bus probes on internal memory interfaces
- Power Management
  - Support for granular gated clock domains to support low power modes and to support memory interface utilization while IP disabled.

- Advanced SOC Integration
  - Dedicated PLL for full flexibility in performance and power trade-offs
    - Provides full asynchronous frequency independence between C7x and all other cores and Peripherals
  - Dedicated windowed watchdog timer per core

7.2.1 C7x Functional Description

7.2.1.1 C7x Block Diagram

The below image shows the functional block diagram of C7x.

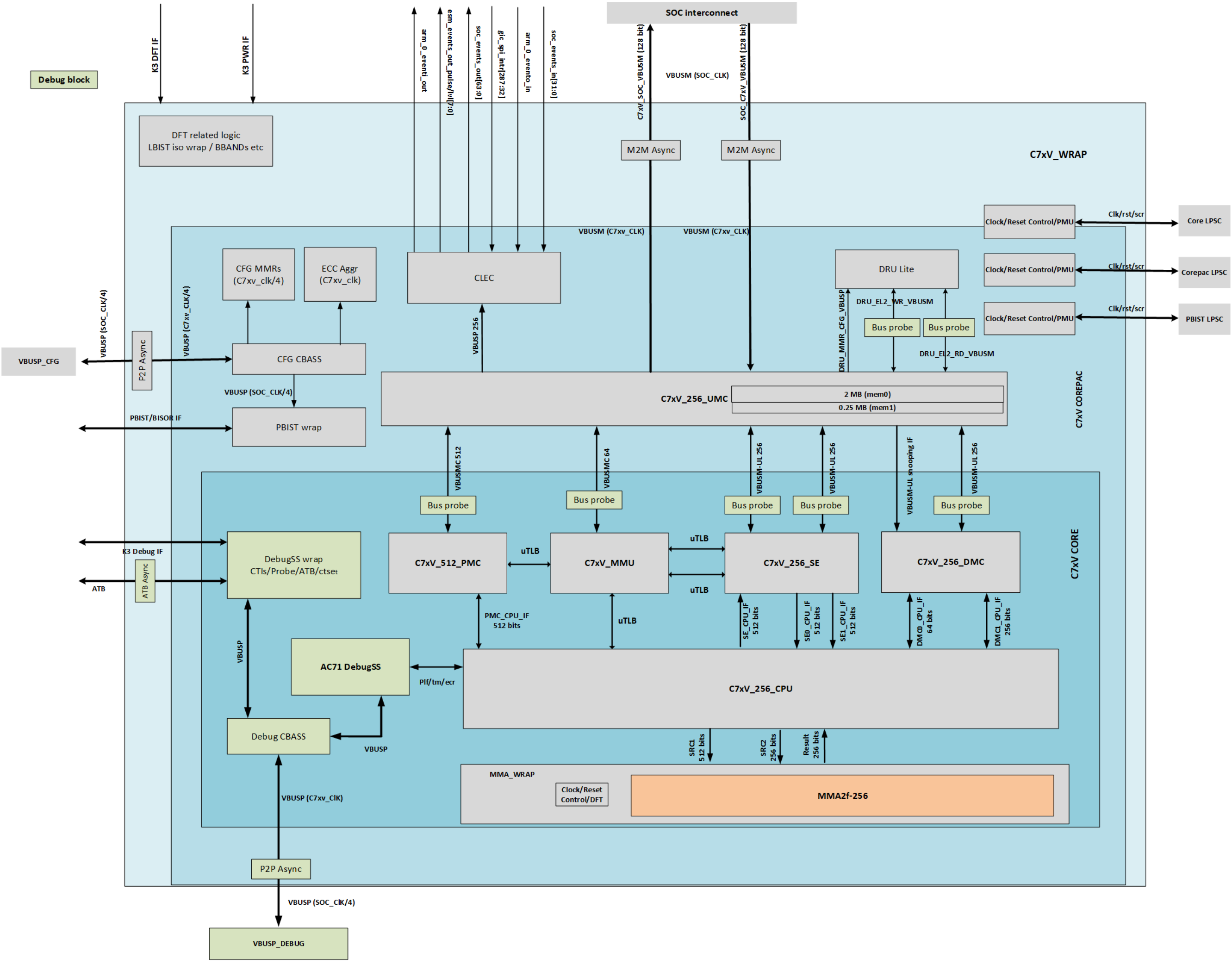

Figure 7-3. C7x Block Diagram

7.2.1.2 C7x DSP CPU

The C7x CPU is a true 64-bit core which provides the following key features:

- Instruction fetch unit
- Instruction dispatch unit, advanced instruction packing
- Instruction decode unit
- CPU dual datapath
  - One 64-bit scalar side (side A) and one 256-bit vector side (side B)
  - Side A includes the following functional units
    - Four main scalar processing units (.L1, .S1, .M1, .N1) capable of operating on up to 64-bit wide data
    - Two units (.D1, .D2) for address calculations, enabling parallel load/store operations
    - The following operations can be executed at the same time in a single clock cycle
      - One non-aligned 64-bit load or store operation
      - Two 64-bit arithmetic/logical operations (non-multiply arithmetic instructions)
      - One 128-bit multiply operation
  - Side B includes the following functional units
    - Five main vector processing units (.L2, .S2, .M2, .N2, .C) capable of operating on up to 256-bit wide vector data

    - A predication processing unit (.P) for vector predication
    - The following vector operations can be executed at the same time in a single clock cycle
      - One non-aligned 256-bit load or store operation
      - Two 256-bit arithmetic/logical operations (non-multiply arithmetic instructions)
      - One 512-bit multiply operation
      - One 256-bit correlation operation or regular arithmetic operation
      - One vector predicate manipulation operation
  - Vector side B can perform up to 64×16-bit fixed-point multiply-accumulate (MAC), 2.0 times the MAC capacity compared to C66x
  - Vector side B can perform up to 40 single precision FLOPs/cycle or 16 double precision FLOPs/cycle, 2.5 times the floating point compared to C66x
  - The C7x CPU can load or store in parallel 32 bits and 256 bits of data per clock cycle, more than two times the bandwidth compared to C66x. In addition, a novel streaming data interface can read an additional 512 bits of data per clock cycle, providing a total of 6 times more bandwidth compared to the C66x
  - Large set of machine registers:
    - Up to 16x256-bit global vector registers
    - Up to 16x64-bit global scalar registers
    - Local registers
  - Register file cross paths
    - Two cross paths, 64-bit each
    - Allow functional units from one data path to access a 64-bit operand from the opposite side global register file
    - The cross paths can not access the local register files directly
- CPU control logic
  - Support for four privilege and execution levels for security and virtualization support with banked control registers for full isolation and protection
    - Non-secure root supervisor
    - Non-secure root user
    - Non-secure guest supervisor
    - Non-secure guest user
  - Pipeline can operate in both unprotected and protected modes
    - Unprotected mode: Traditional C6x VLIW DSP operating mode with exposed instruction delay slots
    - Protected mode: Control code execution mode where instructions delay slots are not exposed
  - Scoreboarding mechanism to help hide memory system stalls and to allow the compiler to generate more efficient control codes
  - Supports recoverable interrupts and internal precise exception
    - No need to disable interrupts during multiple assignment code. In-flight results in multiple-assignment code are recorded by pipeline capture queues. These queues allow all programs to be interrupted at any arbitrary cycle, even during software pipelined loops, and then to be restarted correctly upon return from the interrupt or exception handler
    - Pipeline capture queues may be unloaded and reloaded, allowing the OS to swap out tasks regardless of whether the task was operating in protected or unprotected pipeline mode
    - Programmable event priority, hardware automatic event mask based on priority levels
    - Hardware performs automatic stacking at even handler entry and automatic unstacking at event exiting
  - Nested loop counters (NLC): Hardware mechanism to facilitate low-overhead loop collapsing by providing the computations associated with nested loop counters and predicates, avoid the needs of using explicit instructions
- Test, debug, and interrupt logic
- Enhanced instruction set architecture (ISA)
  - Single-cycle 64-bit arithmetic, logical, and shift instructions
  - Improvements to load/store instructions
    - Endian aware vector load instructions
    - Unpacking load / packing store instructions
    - Vector load/store with element reversal

    - Vector load with data duplications
  - Specialized instructions to speed up key benchmarks
    - Horizontal MAX/MIN search acceleration instructions
    - Horizontal ADD, SUB instructions
    - Dedicated FIR instructions
    - Sliding window sum of absolute differences (SAD)
    - Maskable complex dot products
  - Circular comparison instructions to accelerate Viterbi
  - New and improved atomic instructions to replace LL/SC/CL combination
  - Increases orthogonality between 32-bit, 64-bit, and vector operations compared to C66x
  - Supports binlog instruction for vision algorithms
  - Specialized instructions only allowed to execute at required privilege level and secure state
- C7x OpenCL features
  - Full compliance with IEEE 754 floating point standard
    - Support subnormal numbers
  - DVM support
    - Support fencing for uTLB transactions

The matrix multiply accelerator (MMA) is included as a special functional unit in the C7x CorePac and is tightly coupled to CPU operation.

7.2.1.3 C7x DSP Matrix Multiply Accelerator

The matrix multiply accelerator (MMA) provides the following key features:

- Support for fully connected layer using matrix multiply with arbitrary dimension
- Support for convolution layer using 2D convolution with matrix multiply with read panel
- Support for ReLU non-linearity layer OTF
- Support for high utilization (>85%) for typical convolutional neural network (CNN), such as AlexNet, ResNet, and others
- Ability to support any CNN network topologies limited only by memory size and bandwidth
- Coupled with C7x CPU using DSP chassis for data formatting
- MMA and C7x CPU are on a shared power domain
  - MMA cannot be independently powered off or clock gated at LPSC level (although it has extensive clock gating within the IP)

- Supports 256-bit vector width
- Supports the following input operand types:
  - 4-bit unsigned integer
  - 8-bit unsigned integer
  - 8-bit signed integer
  - 16-bit unsigned integer
  - 16-bit signed integer
  - 32-bit unsigned integer
  - 32-bit signed integer
  - 32-bit single precision float
- Supports the following data types for accumulation:
  - 32-bit unsigned integer for 8-bit unsigned operands
  - 32-bit signed integer for 8-bit signed or mixed signed/unsigned operands
  - 64-bit unsigned integer for 16-bit unsigned operands
  - 64-bit signed integer for 16-bit signed or mixed signed/unsigned operands
  - 128-bit unsigned integer for 32-bit unsigned operands (compiler support for this type is not expected)
  - 128-bit signed integer for 32-bit signed or mixed signed/unsigned operands (compiler support for this type is not expected)
  - 32-bit single precision float
- Supports the following types on output:
  - 4-bit unsigned integer – compiler support for this type is not expected
  - 4-bit signed integer – compiler support for this type is not expected

  - 8-bit unsigned integer
  - 8-bit signed integer
  - 16-bit unsigned integer
  - 16-bit signed integer
  - 32-bit unsigned integer
  - 32-bit signed integer
  - 64-bit unsigned integer
  - 64-bit signed integer
  - 128-bit unsigned integer – compiler support for this type is not expected
  - 128-bit signed integer – compiler support for this type is not expected
  - 32-bit single precision float

Note

DSP1 does not support MMA

7.2.1.4 C7x DSP Cache Memory System

The C7x CorePac implements a hierarchical cache memory system with the following levels:

- Level 1 (L1):
  - L1 program memory controller (PMC) with associated L1 program memory (L1P)
  - L1 data memory controller (DMC) with associated L1 data memory (L1D)
- Level 2 (L2):
  - L2 unified memory controller (UMC) with associated L2 memory

7.2.1.4.1 C7x DSP L1 Program Memory

The L1P cache controller supports a fixed cache size of 32KB. The purpose of the L1P cache is to maximize performance of the code execution. L1P cache is necessary to facilitate fetching program code at a fast clock rate in order to maintain a large system memory. The cache is responsible for hiding the latency associated with executing code from the slower system memory.

The L1P memory system provides the following key features:

- L1 program memory controller (PMC) with 32KB L1P memory, all cache (no support for L1P SRAM)
- L1P cache
  - 4-way set associative
  - 64-byte line size
  - Virtually indexed, virtually tagged (48-bit virtual address)
  - Auto-prefetching on L1P misses from L2
  - Capability to queue multiple fetch packet requests (64 bytes) to UMC to enable deeper prefetch in program pipeline
- Parity protection on Data and Tag rams with 1-bit error detection
- Data RAM parity protection is on instruction width granularity with 1 parity bit every 32 bits
- Auto-Invalidate and Re-Fetch on errors in TAG RAM
- Single cycle cache invalidates with support for three modes
- Virtual to Physical addressin on misses
- Extended Control Register (ECR) Access

7.2.1.4.2 C7x DSP L1 Data Memory

The L1D cache supports 2 data paths that service one DSP core. The data path connected to the DSPs scalar side is 64 bits wide while the one connect to the vector side is configurable and matches the CPU vector width. The L1D controls a 2-way cache and is also connected to the unified memory controller (UMC) which is then connected to the rest of the DSP system.

The L1D memory system provides the following key features:

- L1 data memory controller (DMC) with 64 KB L1D memory, configurable as cache
- L1D cache
  - Dual data path

  - 64-bit and 256-bit data paths
  - 64-byte cache line size
  - Read-allocate cache
  - Write-through cache for L2/EL2 accesses
  - Physically Indexed, Physically Tagged
  - LRU replacement policy
  - Non-aligned access support
  - Hit under Miss
  - FENCE operation on outstanding transactions with support for two types of transactions
  - Atomic operation support - C7x and RISC-V opcodes
  - ECR access from the CPU. Accessed with a CPU MVC instruction
  - 320-bit/cycle (256+64) bandwidth to/from the DSP core
  - 256-bit/cycle RAM bandwidth
  - 256-bit/cycle bandwidth to UMC and bandwidth
  - Per byte ECC Protection od data stored in the cache
  - 1 parity bit per tag entry

7.2.1.4.3 C7x DSP L2 Memory

The L2 memory system provides the following key features:

- L2 unified memory controller (UMC) with 2.25MB L2 memory, configurable as SRAM
- MS banking for two blocks memory partition
- Port based design with 2-read and 2-write ports rather than crossbar
- Provides SRAM access path to SoC Interconnect
- Facilitates SRAM access from DRU
- Provides memory mapped configuration register access

7.2.1.5 C7x Streaming Engine

The streaming engine (SE) supports the following key features:

- Provides a flexible, high bandwidth mechanism for reading large quantities of data into C7x CPU
- Supplies two 256-bit data streams (S0, S1) directly from L2 to the vector units
- Provides two stream address generators, supporting the two data streams
  - Flexible multi-dimensional address calculators
  - Provide offset addresses for load and store instructions
- Supports element promotion, decimation, duplication, transpose loads, predication
- LEZR feature can be enabled to return N number of zero vectors to CPU after selected dimension ends. LEZR and transposed mode are not supported together. LEZR is still supported when transposed mode is disabled..
- Provides 6D addressing
  - Access patterns up to 6D can be programmed ahead
  - 6D data is presented as 512-bit vector per cycle
- Communicates with L2 memory controller for requests beyond L2 (MSMC, DDR)
- Coherent with L1D data at stream open/close boundaries
- ECC SECDED support

The SE can sustain 512-bits/cycle total bandwidth (256 bits/cycle on each of two streams) to the DSP CPU. When combined with its 256-bit/cycle vector load unit and 256-bit/cycle store unit, the DSP CPU can access 1024 bits/cycle of data.

7.2.1.6 C7x DSP Memory Management Unit (MMU)

The CorePac Memory Management Unit (CMMU) extends the C7x architecture with support for address translation, access permission and protections and memory attributes determination and checking. It is implemented per C7x cluster as a two-level TLB structure. The CMMU works with the C7x L1 caches, stream buffers in each processor and CorePac memory system of CorePac cluster to translate virtual addresses to physical addresses, controls tablewalk hardware that accesses translation tables in main memory. The CMMU enables fine-grained memory system control through a set of virtual-to-physical address mappings and memory attributes held in the L1 level micro translation look-aside buffer (uTLB) and CorePac cluster level translation look-aside buffers (TLBs).

The CMMU provides the following key features:

- Supports AArch32 LPAE and AArch64 page table format
  - Programmable levels of page table translation
  - 4KB, 16KB, 64KB translation granules
- Supports multiple page sizes: 4KB, 16KB, 64KB, 2MB, 32MB, 512MB, 1GB, 16GB
- Supports both hardware and software managed table walks
- Hierarchical Table Lookaside Buffer (TLB) caching page entries, intermediate page walk pointers for optimum address translation performance
  - Micro-TLB (uTLB) as first level TLB
    - 16-entry fully associative dual interface L1 data uTLB
    - 8-entry fully associative L1 instruction uTLB
  - CorePac (L2) TLB as second level TLB
    - 512-entry 4-way associative TLB cache, caching both instruction and data page translations with virtual-to-physical address mapping
    - Intermediate table walk caches to reduce memory access during multi-level page walk
    - Allows caching and sharing of intermediate table walks and page tables in the system cache hierarchy
- Security extensions that facilitate the development of secure applications
- Soft-error protection on all RAM and data storage structures

7.2.1.7 C7x ECC Support

Table 7-13 provides the RAM ID for the C7x DSP ECC aggregator.

Table 7-13. RAM ID Map for C7x DSP ECC Aggregator

RAM ID	Endpoint
0	Program Memory Controller
1	Data Memeory Controller
2	Data Memeory Controller
3	Data Routing Unit
4	Data Routing Unit
5	Data Routing Unit
6	Cluster Level Event Controller
7	Unified Memory Controler

7.2.1.8 C7x Boot Configuration

In this device, the C7x boots from system memory instead of booting from ROM. A 1KB boot RAM (PSRAM1KECC) is used to store boot vectors for the C7x CPU.

Note

By default, the C7x CPU boots in C7x ISA mode but if riscv_mode bit is set in the corepac cfg regiseter, then CPU boots in RISVC ISA mode

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7.2.1.9 C7x DSP Power-Up/Down Sequences

The power-up and power-down sequences for the C7x DSP can be found in *Power*.

8 Inter-processor Communication Scheme (IPC)

Device has multiple hardware mechanisms to provide inter-processor level communication.

8.1 IPC Overview

This chapter gives an overview on Mailbox, Spinlock, and Secure Proxy.

8.2 Mailbox

This chapter describes the Mailbox module of the device.

8.2.1 Mailbox Overview

Mailbox module serves to facilitate the communication between the various on-chip processors of the device by providing a queued mailbox-interrupt mechanism.

The queued mailbox-interrupt mechanism allows the software to establish a communication channel between two processors (users) through a set of registers and associated interrupt signals.

8.2.1.1 Mailbox Features

Each mailbox module supports the following features:

- Parameters configured at design time:
  - Number of mailbox clusters
    - Each mailbox cluster has the same configuration
    - Clusters are accessed via separate VBUS regions. Clusters can be treated as mailbox module instances.
  - Number of users
  - Number of mailbox message queues
  - Number of messages (FIFO depth) for each message queue
- 32-bit message width
- Partial writes do not advance the FIFO pointers
- Message reception and queue-not-full notification using interrupts
- Non-intrusive emulation

Note

Some features may not be available. See *Module Integration* for more information.

8.2.2 Mailbox Functional Description

The mailbox module provides a means of communication through message queues among the users. The individual mailbox modules, or FIFOs, can associate (or de-associate) with any of the processors using the MAILBOX_IRQ_ENABLE_SET_j (or MAILBOX_IRQ_ENABLE_CLR_j) register.

Each user has a dedicated interrupt signal from the corresponding mailbox module instance and dedicated interrupt enabling and status registers.

Each MAILBOX_IRQ_STATUS_RAW_j/MAILBOX_IRQ_STATUS_CLR_j interrupt status register corresponds to a particular user.

8.2.2.1 Mailbox Block Diagram

Figure 8-1 shows the mailbox internal block diagram.

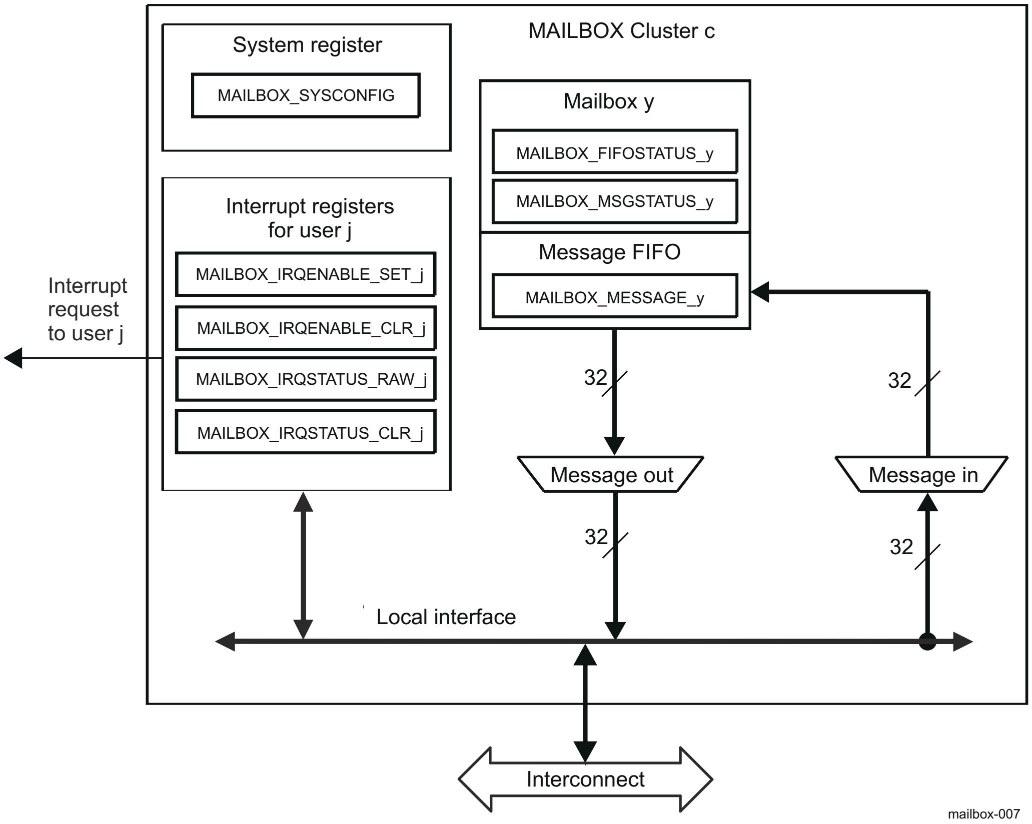


Figure 8-1. Mailbox Block Diagram

c = 0 to 11

j = 0 to 3

y = 0 to 15

8.2.2.2 Mailbox Software Reset

The mailbox module supports a software reset through the MAILBOX_SYSCONFIG[0] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. Reading the MAILBOX_SYSCONFIG[0] SOFTRESET bit gives the status of the software reset:

- Read 1: the software reset is on-going.
- Read 0: the software reset is complete.

The software must ensure that the software reset completes before doing mailbox operations.

8.2.2.3 Mailbox Power Management

The clkstop_idle will be asserted if all of the following are true:

- The VBUSP interface is inactive
- All mailboxes are empty
- There are no enabled events or outstanding interrupts

An enabled event means there is pending action required from one of the users, and it means one or more mailboxes still expect data.

8.2.2.4 Mailbox Interrupt Requests

An interrupt request allows the user of the mailbox to be notified when a message is received or when the message queue is not full. There is one interrupt per user.

Table 8-1 lists the event flags, and their mask, that can cause module interrupts.

Table 8-1. Interrupt Events

Non-Maskable Event Flag(1)	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
MAILBOX_IRQ_STATUS_RAW_j[0+y*2] NEWMSGSTATUSMBy	MAILBOX_IRQ_STATUS_CLR_j[0+y*2] NEWMSG_STATUSMBy	MAILBOX_IRQ_ENABLE_CLR_j[0+y*2] NEWMSG_STATUSMBy	MAILBOX_IRQ_ENABLE_SET_j[0+y*2] NEWMSG_STATUSMBy	Mailbox *y* receives a new message.
MAILBOX_IRQ_STATUS_RAW_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_STATUS_CLR_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_ENABLE_CLR_j[1+y*2] NOTFULLSTATUSMBy	MAILBOX_IRQ_ENABLE_SET_j[1+y*2] NOTFULLSTATUSMBy	Mailbox *y* message queue is not full.

(1) MAILBOX_IRQ_STATUS_RAW_j register is mostly used for debug purposes.

CAUTION

Once an event generating the interrupt request has been processed by the software, it must be cleared by writing a logical 1 in the corresponding bit of the MAILBOX_IRQ_STATUS_CLR_j register.

Writing a logical 1 in a bit of the MAILBOX_IRQ_STATUS_CLR_j register will also clear to 0 the corresponding bit in the appropriate MAILBOX_IRQ_STATUS_RAW_j register.

An event can generate an interrupt request when a logical 1 is written to the corresponding unmask bit in the MAILBOX_IRQ_ENABLE_SET_j register. Events are reported in the appropriate MAILBOX_IRQ_ENABLE_CLR_j and MAILBOX_IRQ_STATUS_RAW_j registers.

An event stops generating interrupt requests when a logical 1 is written to the corresponding mask bit in the MAILBOX_IRQ_ENABLE_CLR_j register. Events are only reported in the appropriate MAILBOX_IRQ_STATUS_RAW_j register.

In case of the MAILBOX_IRQ_STATUS_RAW_j register, the event is reported in the corresponding bit even if the interrupt request generation is disabled for this event.

8.2.2.5 Mailbox Assignment

8.2.2.5.1 Description

To assign a receiver to a mailbox, set the new message interrupt enable bit corresponding to the desired mailbox in the MAILBOX_IRQ_ENABLE_SET_j register. The receiver reads the MAILBOX_MESSAGE_y register to retrieve a message from the mailbox.

An alternate method for the receiver that does not use the interrupts is to poll the MAILBOX_FIFO_STATUS_y and/or MAILBOX_MSG_STATUS_y registers to know when to send or retrieve a message to or from the mailbox. This method does not require assigning a receiver to a mailbox. Because this method does not include the explicit assignment of the mailbox, the software must avoid having multiple receivers use the same mailbox, which can result in incoherency.

To assign a sender to a mailbox, set the queue-not-full interrupt enable bit of the desired mailbox in the MAILBOX_IRQ_ENABLE_SET_j register, where *u* is the number of the sending user. However, direct allocation of a mailbox to a sender is not recommended because it can cause the sending processor to be constantly interrupted.

It is recommended that register polling be used to:

- Check the status of either the MAILBOX_FIFO_STATUS_y or MAILBOX_MSG_STATUS_y registers
- Write the message to the corresponding MAILBOX_MESSAGE_y register, if space is available.

The sender might use the queue-not-full interrupt when the initial mailbox status check indicates the mailbox is full. In this case, the sender can enable the queue-not-full interrupt for its mailbox in the appropriate MAILBOX_IRQ_ENABLE_SET_j register. This allows the sender to be notified by interrupt only when a FIFO queue has at least one available entry.

Reading the MAILBOX_IRQ_STATUS_CLR_j register determines the status of the new message and the queue-not-full interrupts for a particular user. Writing 1 to the corresponding bit in the MAILBOX_IRQ_STATUS_CLR_j register acknowledges, and subsequently clears, an interrupt.

CAUTION

Assigning multiple senders or multiple receivers to the same mailbox is not recommended.

8.2.2.6 Sending and Receiving Messages

8.2.2.6.1 Description

When a 32-bit message is written to the MAILBOX_MESSAGE_y register, the message is appended into the FIFO queue. This queue holds four messages. If the queue is full, the message is discarded.

Queue overflow can be avoided by first reading the MAILBOX_FIFO_STATUS_y register to check that the mailbox message queue is not full before writing a new message to it.

Reading the MAILBOX_MESSAGE_y register returns the message at the beginning of the FIFO queue and removes it from the queue. If the FIFO queue is empty when the MAILBOX_MESSAGE_y register is read, the value 0 is returned.

The new message interrupt is asserted when at least one message is in the mailbox message FIFO queue. To determine the number of messages in the mailbox message FIFO queue, read the MAILBOX_MSG_STATUS_y register.

8.2.2.7 Example of Communication

Figure 8-2 shows an example of communication between two processors.

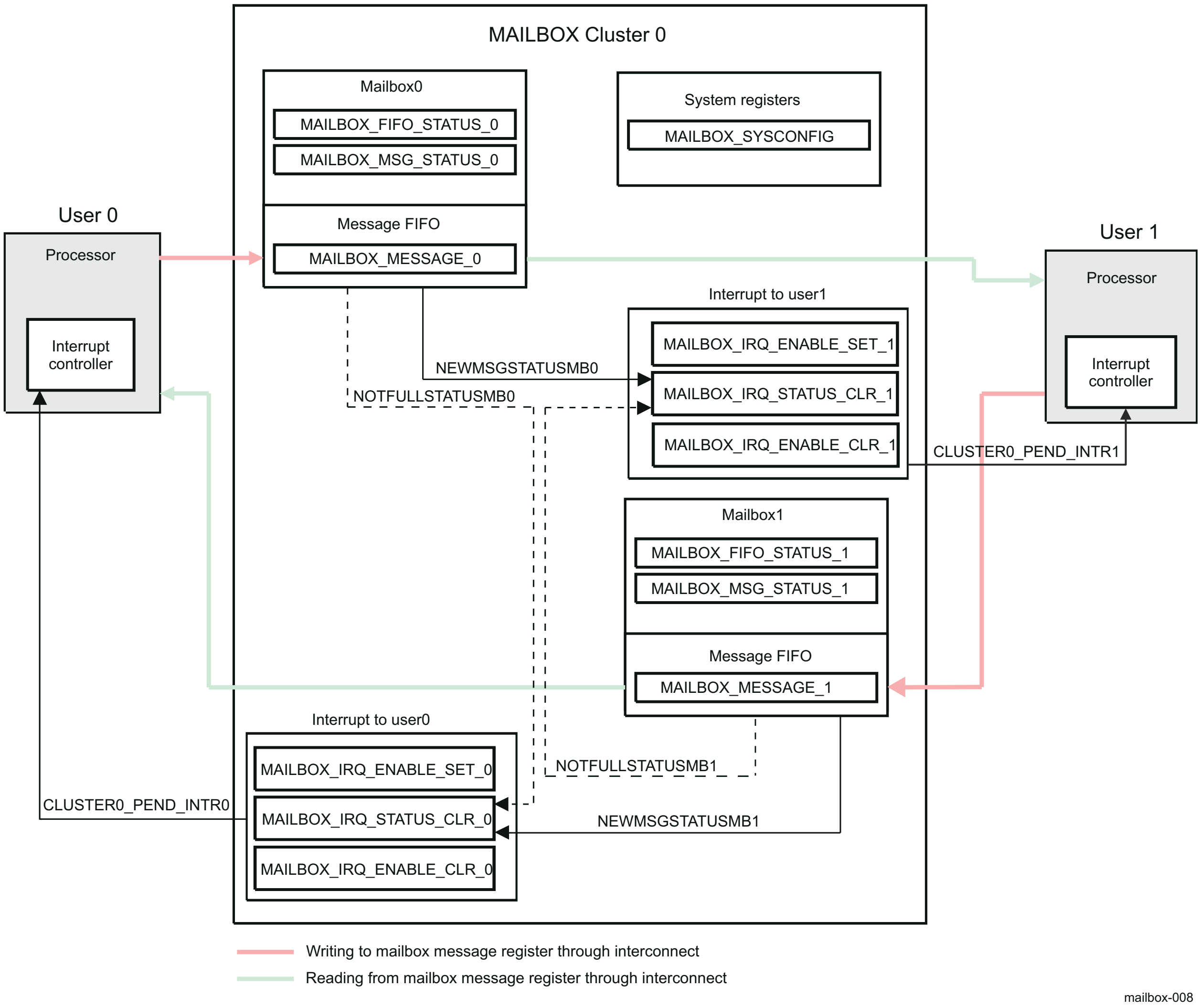


Figure 8-2. Example of Communication

8.2.3 Mailbox Programming Guide

8.2.3.1 Mailbox Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the mailbox module.

8.2.3.1.1 Global Initialization

8.2.3.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the mailbox module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the mailbox.

See *Mailbox Integration*, for further information.

Table 8-2. Global Initialization of Surrounding Modules for MAILBOX

Surrounding Modules	Comments
LPSC	The MAILBOX functional and interface clock must be enabled.
Interrupt Controllers	Processor's (user's) interrupt controller must be configured to enable the interrupt request generation.

8.2.3.1.1.2 Mailbox Global Initialization

8.2.3.1.1.2.1 Main Sequence - Mailbox Global Initialization

This procedure initializes the mailbox module after a power-on or software reset.

Table 8-3. Mailbox Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset	MAILBOX_SYSCONFIG[0] SOFT_RESET	0x1
Wait until reset is complete	MAILBOX_SYSCONFIG[0] SOFT_RESET	=0x0

8.2.3.1.2 Mailbox Operational Modes Configuration

8.2.3.1.2.1 Mailbox Processing modes

8.2.3.1.2.1.1 Main Sequence - Sending a Message (Polling Method)

Table 8-4. Sending a Message (Polling Method)

Step	Register/Bit Field/Programming Model	Value
IF: Is FIFO full?	MAILBOX_FIFO_STATUS_y[0] FULL	=0x1
Wait until at least one message slot is available	MAILBOX_FIFO_STATUS_y[0] FULL	=0x0
ELSE		
Write message	MAILBOX_MESSAGE_y[31:0] VALUE	0x-
ENDIF		

8.2.3.1.2.1.2 Main Sequence - Sending a Message (Interrupt Method)

Table 8-5. Sending a Message (Interrupt Method)

Step	Register/Bit Field/Programming Model	Value
IF: Is FIFO full?	MAILBOX_FIFO_STATUS_y**MAILBOX_FIFO_STATUS_y**[0] FULL	=0x1
Enable interrupt event	MAILBOX_IRQ_ENABLE_SET_j**MAILBOX_IRQ_ENABLE_SET_j**[1+ y*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 8.2.3.1.3.1 for interrupt handling in sending mode		
ELSE		
Write message	MAILBOX_MESSAGE_y**MAILBOX_MESSAGE_y**[31:0] VALUE	0x-

Table 8-5. Sending a Message (Interrupt Method) (continued)

Step	Register/Bit Field/Programming Model	Value
ENDIF		

8.2.3.1.2.1.3 Main Sequence - Receiving a Message (Polling Method)

Table 8-6. Receiving a Message (Polling Method)

Step	Register/Bit Field/Programming Model	Value
IF: Number of messages is not equal to 0	MAILBOX_MSG_STATUS_y[2:0] NUM_MESSAGES	≠0x0
Read message	MAILBOX_MESSAGE_y[31:0] VALUE	0x-
ENDIF		

8.2.3.1.2.1.4 Main Sequence - Receiving a Message (Interrupt Method)

Table 8-7. Receiving a Message (Interrupt Method)

Step	Register/Bit Field/Programming Model	Value
Enable interrupt event	MAILBOX_IRQ_ENABLE_SET_j[0 + y*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 8.2.3.1.3.2 for interrupt handling in receiving mode		

8.2.3.1.3 Mailbox Events Servicing

8.2.3.1.3.1 Events Servicing in Sending Mode

Table 8-8 describes the events servicing in sending mode.

Table 8-8. Events Servicing in Sending Mode

Step	Register/Bit Field/Programming Model	Value
Read interrupt status bit	MAILBOX_IRQ_STATUS_CLR_j[1 + y*2]	0x1
Write message	MAILBOX_MESSAGE_y[31:0] VALUE	0x--
Write 1 to acknowledge interrupt	MAILBOX_IRQ_STATUS_CLR_j[1 + y*2]	0x1

8.2.3.1.3.2 Events Servicing in Receiving Mode

Table 8-9 describes the events servicing in receiving mode.

Table 8-9. Events Servicing in Receiving Mode

Step	Register/Bit Field/Programming Model	Value
Read interrupt status bit	MAILBOX_IRQ_STATUS_CLR_j[0 + y*2]	0x1
IF: Number of messages is not equal to 0?	MAILBOX_MSG_STATUS_y[2:0] NUM_MESSAGES	≠0x0
Read message	MAILBOX_MESSAGE_y[31:0] VALUE	0x--
ELSE		
Write 1 to acknowledge interrupt	MAILBOX_IRQ_STATUS_CLR_j[0 + y*2]	0x1
ENDIF		

8.3 Spinlock

This chapter describes the Spinlock module of the device.

8.3.1 Spinlock Overview

The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device.

The Spinlock module implements 256 spinlocks (or hardware semaphores), which provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need of a read-modify-write bus transfer that the programmable cores are not capable of.

Figure 8-3 shows an overview of the Spinlock module.

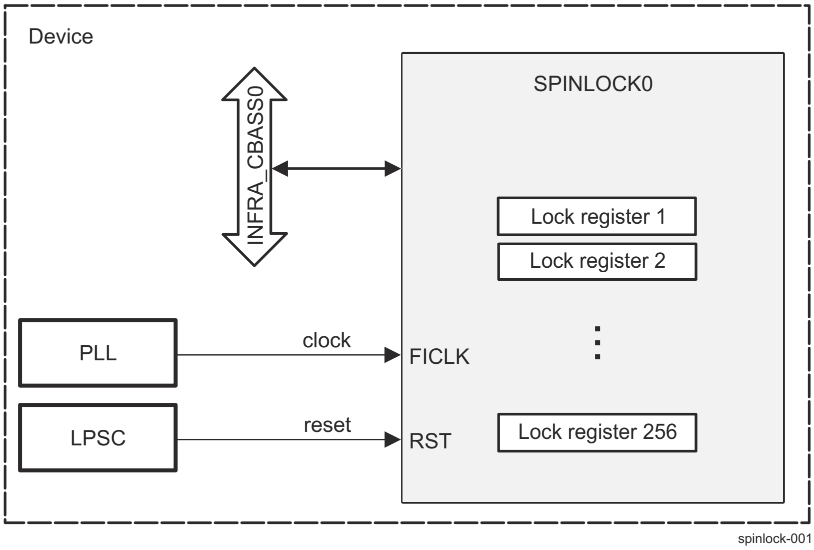


Figure 8-3. Spinlock Overview

Note

Some features may not be available. See *Module Integration* for more information.

8.3.2 Spinlock Functional Description

8.3.2.1 Spinlock Software Reset

The Spinlock module can be reset by software through the SPINLOCK_SYSCONFIG[1] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. The SPINLOCK_SYSTATUS[0] RESETDONE bit can be polled to check the reset status (reading 1 indicates that reset sequence is done; reading 0 indicates that reset sequence is in progress). The software must ensure that the software reset completes before doing Spinlock operations.

8.3.2.2 Spinlock Power Management

The Spinlock module supports the Power Idle interface. Software must arrange to only power off the Spinlock module when no locks would be lost. In general, the steps to powering down the Spinlock module are:

1. Software must check that all controllers that may be using the Spinlock module are either:
    a. Already powered off (all in-use flags are 0)
    b. Notified that Spinlock is not available and the notification is acknowledged
2. If desired, check that no locks are currently held in the Spinlock module. The status of each bank of 32 locks can be read from the SPINLOCK_SYSTATUS register. If any locks are held, they are orphaned because they are not held by any controller that is still active. Alternatively, you may decide to wait a timeout period to allow any active controller to clean up its locks before powering down.

The Spinlock module may now be powered off.

8.3.2.3 About Spinlocks

Spinlocks are present to solve the need for synchronization and mutual exclusion between heterogeneous processors and those not operating under a single, shared operating system. There is no alternative mechanism to accomplish these operations between processors in separate subsystems.

Spinlocks are not the best way to synchronize between tasks or threads on one CPU. Instead, spinlocks are for use in synchronization between different subsystems in the device that don't have any other means of hardware-based synchronization.

Spinlocks do not solve all system synchronization issues. They have limited applicability and should be used with care to implement higher level synchronization protocols.

A spinlock is appropriate for mutual exclusion for access to a shared data structure. It should be used only when:

1. The time to hold the lock is predictable and small (for example, a maximum hold time of less than 200 CPU cycles may be acceptable).
2. The locking task cannot be preempted, suspended, or interrupted while holding the lock (this would make the hold time large and unpredictable).
3. The lock is lightly contended, that is the chance of any other process (or processor) trying to acquire the lock while it is held is small.

If these conditions are met, then the locking code can retry a failed attempt to acquire the lock until success.

If the conditions are not met, then a spinlock is not a good candidate. One alternative is to use a spinlock for critical section control (engineered to meet the conditions) to implement a higher level semaphore that can support preemption, notification, timeout or other higher level properties.

8.3.2.4 Spinlock Functional Operation

The Spinlock module supports 256 spinlocks. It accepts only a single command at a time and processes the command fully before accepting the next command. A lock is requested by reading the SPINLOCK_LOCK_REG_i[0] TAKEN bit. There are two states: Taken (SPINLOCK_LOCK_REG_y[0] TAKEN = 1) or Not Taken (SPINLOCK_LOCK_REG_y[0] TAKEN = 0), where y = 0h to FFh.

When the status of lock *y* (where y = 0 to 255) is Not Taken (free), a read from the SPINLOCK_LOCK_REG_y register returns 0 and sets the lock to Taken (locked). When the status of lock *y* is Taken, a read returns 1 and does not change the state of the lock.

A write to the SPINLOCK_LOCK_REG_y register does not change the state of lock, unless when writing 0 when the lock is in Taken state. By doing this, the requester frees the lock.

Figure 8-4 shows the SPINLOCK_LOCK_REG_y register state diagram.

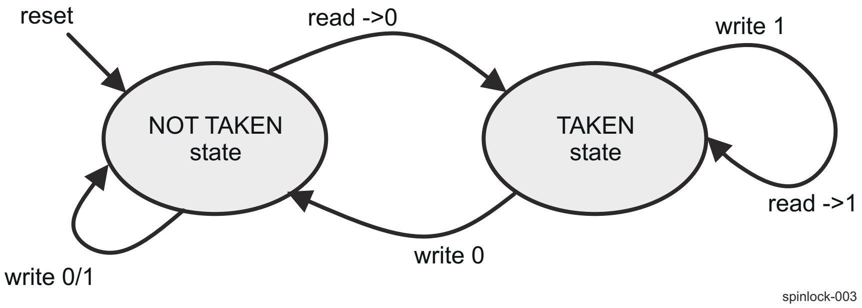


Figure 8-4. Lock Register State Diagram

Note

- There is no support to ensure that a lock register is locked and unlocked by the same process. This must be ensured in software.
- There is no support to check that the same initiator that acquired the lock is the one that is freeing the lock.

8.3.3 Spinlock Programming Guide

8.3.3.1 Spinlock Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

8.3.3.1.1 Surrounding Modules Global Initialization

This procedure initializes the surrounding modules when the Spinlock module is used for the first time after a device reset.

Table 8-10. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC	Spinlock functional and interface clock must be enabled. For more information, see *Clocking*

8.3.3.1.2 Basic Spinlock Operations

The main Spinlock operations are:

- Clear all the Taken spinlocks (only after a system bug recovery)
- Take a spinlock
- Release spinlock

8.3.3.1.2.1 Spinlocks Clearing After a System Bug Recovery

Module initialization (after reset) is not needed, except after system bug recovery. The following table presents the Spinlock initialization after a system bug recovery. Software should store 0 into each of the SPINLOCK_LOCK_REG_y registers at system startup to insure that all locks are initialized to Not Taken.

Table 8-11. Spinlock System Bug Recovery

Step	Register	Value
IF: SPINLOCK_SYSTATUS[0] IU0 = 1?	SPINLOCK_SYSTATUS[0] IU0	=1
Free the 256 locks	SPINLOCK_LOCK_REG_y[0] TAKEN (y = 0 to 255)	0x0
END		

8.3.3.1.2.2 Take and Release Spinlock

This procedure configures the take and release (free) operations for the Spinlock module. A spinlock should only be held with interrupts disabled. So, before attempting to obtain the spinlock, software must disable interrupts. Then it must read the SPINLOCK_LOCK_REG_y[0] TAKEN bit to attempt to obtain the lock. If it succeeds, it must proceed directly through the critical section then unlock and re-enable interrupts. If the acquisition attempt fails, the acquisition must be reattempted. To prevent unknown interrupt disabled time, interrupts must be re-enabled and then disabled before reattempting to acquire the lock. Figure 8-5 shows the described above procedure.

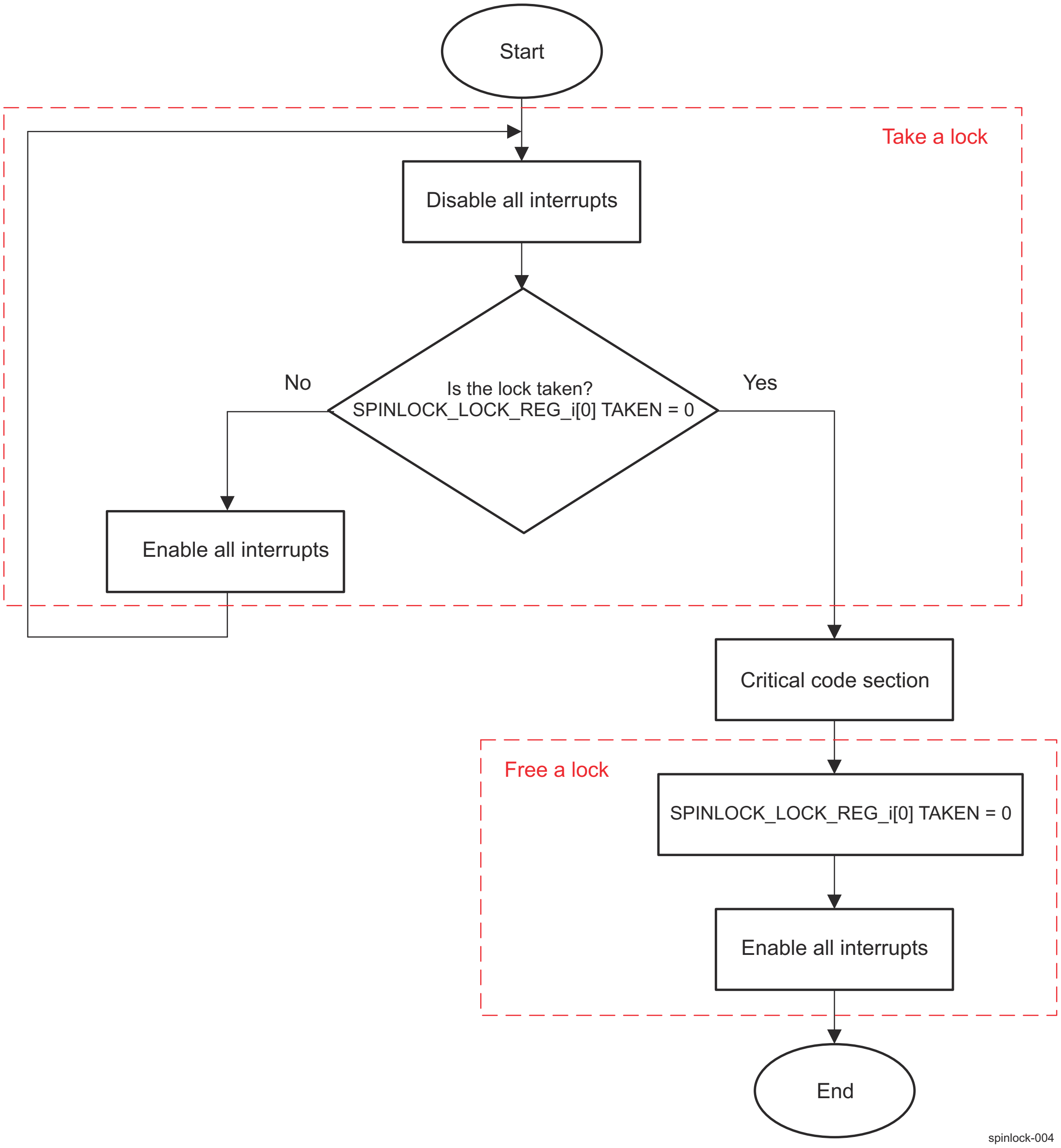


Figure 8-5. Take and Release Spinlock

Table 8-12. Register Call Summary

Register Name
SPINLOCK_LOCK_REG_y[0] TAKEN

Table 8-13. Subprocess Call Summary

Subprocess Name	Description
Disable (Mask) All Interrupts	For information about disabling/enabling all interrupts in an Arm® processor, refer to Arm *Technical Reference Manual*, available at infocenter.arm.com/help/index.jsp. For information about disabling/enabling all interrupts in other processors, refer to the corresponding processor chapter.
Enable (Unmask) All Interrupts	

8.4 Secure Proxy (SEC_PROXY)

The third IPC hardware mechanism is to use SEC_PROXY, which provides an IPC mechanism which carries a large message for complex communications among processors. It allows processors to read and write a message in small chunks.

There are two sets of SEC_PROXY in the device, one SEC_PROXY is dedicated for IPC for HSM M4F, and the second SEC_PROXY is for the rest. When the SEC_PROXY generates events, an IPC message is received or sent, and events are sent to interrupt aggregators before those events are converted into interrupts to the processors. The utilization of SEC_PROXY is user defined through memory map allocation. Each processor can be allocated with its own SEC_PROXY region to receive and send IPC messages.

9 Memory Controllers

This chapter describes the memory controllers in the device.

9.1 Region-based Address Translation (RAT) Module

This section describes the RAT functionality.

9.1.1 RAT Functional Description

9.1.1.1 RAT Operation

The RAT module performs a region based address translation. It translates a 32-bit input address into a 48-bit output address. Any input transaction that starts inside of a programmed region will have its address translated, if the region is enabled. Any disabled region is ignored from the translation lookup.

RAT has 16 regions, with each region having dedicated registers that define its attributes:

- Base address of the region, via the RAT_BASE_k register.
- Size of the region, via the RAT_CTRL_k register.
- Translated base address (48-bit). It is defined by 32-bit lower address via the RAT_TRANS_L_k register, and 16-bit upper address via the RAT_TRANS_U_k register.

The input addresses are compared against all the enabled regions in parallel. The region size defines how many of the lowest address bits are included in the region space, starting from a 1B space to a 4GB space. Then the upper bits not part of the region are used for the lookup and comparison, matching those bits of the input addresses against the region base address. The region matches when it is enabled and the compare matches. The first region that matches has the output address set with the region translated base address upper bits. The lower bits that are part of the region size are copied from the input address to the output address. If there are no region matches then the input address is copied to the output address entirely.

RAT does not automatically correct transactions that cross region boundaries, that is, start inside of a region and end outside of it, or start outside of a region and end inside of it. If a boundary crossing transaction is detected, then RAT annuls the transaction as illegal, generates an interrupt and logs an error, as explained in *RAT Error Logging*.

Note

The region base address and translated base address must be aligned to the defined region size. For example, if the defined region size is 64KB, then the two addresses must be 64KB aligned. This is software responsibility as RAT does not perform such alignment check. Regions that are not aligned have unpredictable results.

Moreover, multiple region definitions must not overlap in their covered address space. RAT does not check for this, so it is software responsibility to take care of it. Overlapping regions may lead to unpredictable results.

9.1.1.2 RAT Error Logging

The error log consists of a series of registers that capture the details of the transaction, including the input address that caused the error. These registers are the following:

- RAT_EXCEPTION_LOGGING_HEADER0 and RAT_EXCEPTION_LOGGING_HEADER1
  RAT_EXCEPTION_LOGGING_DATA0 through RAT_EXCEPTION_LOGGING_DATA3

The RAT module can capture one error before it is cleared by software. The error logging is enabled by default, but can be disabled via the RAT_EXCEPTION_LOGGING_CONTROL[0] DISABLE_F bit. Upon error logging an interrupt is also generated. To clear the log, software must either read the final error logging register, or manually clear the RAT_EXCEPTION_PEND_CLEAR[0] PEND_CLR bit by setting it to 0x1. This will clear the error status, and not the actual log registers, but it does allow the next error to be captured into the log registers. If the status is not cleared and additional errors are detected, they are not logged.

After an error occurs and is cleared (whether by reading the final error logging register or by clearing the status bit), the RAT_EOI_REG register must be written to guarantee the next interrupt pulse will be produced.

See the RAT section of the Module Integration chapter of this document for the RAT Source ID mapping which is associated with the EXCEPTION_LOGGING_HEADER0[23-8] SRC_ID field for each RAT module.

9.2 OCSRAM Overview

The device utilize an integrated On-Chip Static Random Access Memory (OCSRAM). Controllers for external memory sources such as DDR are **not** included. The key functionality of the OCSRAM module includes:

- Total of up to 6 MB of RAM
  - Can be used as code and data memory by the R5FSS cores
  - Can be used as data buffers accessible by DMA
- Six, 256-bit wide independent banks of size 1MB with an operating frequency that is the R5F Core Frequency divided by 2 (500MHz for the highest operating performance grade: F)
- Accessible by all initiator modules via the CORE_VBUSM interconnect as detailed in
- Protected with MPU firewalls as detailed in MPU
- Loadable space for the Secondary Bootloader (SBL) as detailed in
- 64-bit ECC Support
  - Read-Modify-Write mechanism to support ECC update on memory writes less then 64-bits. Read-Modify-Write operation works independently per bank and requires one additional cycle to update.

10 Interrupts

Note

This TRM uses the prefix of "MCU_" for items that refer to the device as a whole instead of a specific domain. "MCU_" is the equivalent of Top Level from Section 1.5.

10.1 Interrupt Architecture

AM275x Interrupt Architecture includes information on how to utilize various interrupts and events in the system and relationships between interrupts and events.

An interrupt is defined as a physical signal which can be routed to the interrupt controller of various processors, which can cause the Interrupt Service Routine (ISR). This physical signal can be either a pulse or level and the polarity can be either negative or positive. And an interrupt is correspondent to an individual wire.

An event is defined as information transported by the event bus or PSI_L bus. Events are coded using an event index. The same event bus or PSI_L bus is used to transport multiple events. An event can also be routed and multiplexed to different locations. Events can't trigger a processor's ISR directly. They must go through the Interrupt Aggregator (IA) to convert the event into an interrupt line. For more information, see *Interrupt Aggregator (INTAGGR)*.

The DMA transfer using BCDMA and PktDMA in AM275x can only be triggered using an event. The SoC level interrupt could be used as a BCDMA trigger using L2G logic. Interrupts in the SoC level can't be used to trigger a pktDMA transfer.

Table 10-1. Interrupt Controllers

Processors	Interrupt Controllers
R5 core inside R5FSS	Dedicated VIM inside R5FSS
HSM	Dedicated NVIC for HSM. HSM receives the same sets of interrupt as TIFS

AM275x also contains multiple SoC level interrupt routers. The main function of those SoC level interrupt routers is to provide flexibility to select interrupt sources from a large group of interrupt sources. Many places use this feature, such as GPIO interrupts and some time synchronization related interrupts.

AM275x contains two ESM modules. ESM is used to consolidate/monitor the error events in the device. In this document, ESM may also be referred to as ESM0 and WKUP_ESM0.

AM275x also has some chip level glue logic to convert some miscellaneous signals used as interrupt sources. Those miscellaneous signals are normally self-clear signals and do not need to clear after the Interrupt Service Routine (ISR) like the normal interrupts generated by the peripherals.

Interrupt Architecture shows the high level interrupt architecture in AM275x.

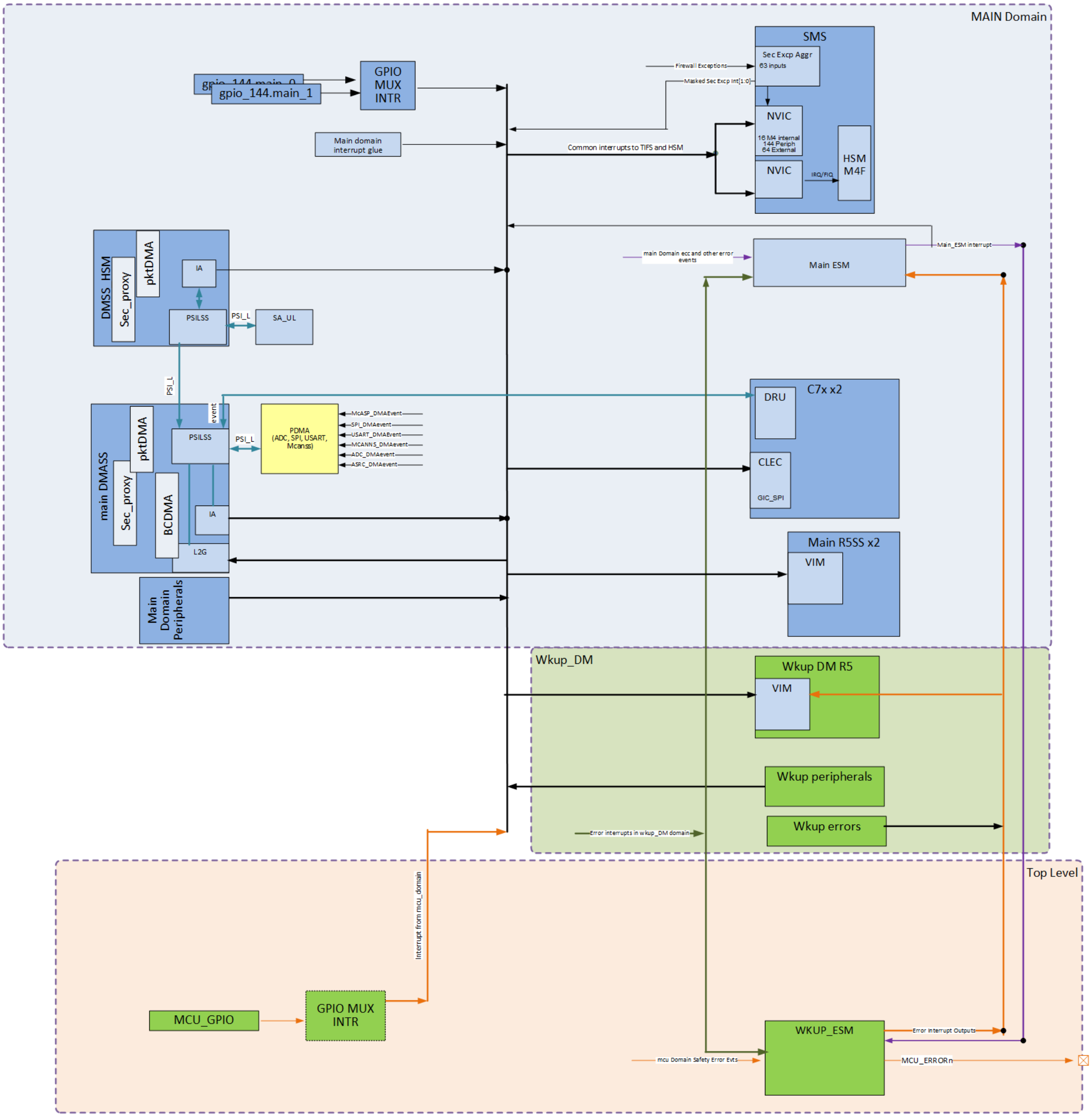


Figure 10-1. AM275x Interrupt Architecture

10.1.1 ESM Connectivity

AM275x contains two ESM modules to consolidate the error interrupts in SoC. One is in the MAIN domain and one is in the WKUP domain. *ESM Connections* shows how error interrupts are connected to these two ESM. .

The error interrupts from the WKUP_R5FSS domain are routed to both MAIN_ESM and WKUP_ESM. Users can configure ESM to cause ESM generating interrupt output from the interrupt inputs. The interrupt outputs of the MAIN_ESM are routed as interrupt inputs to the WKUP_ESM. The interrupt outputs of the WKUP_ESM are routed as the interrupt inputs to the MAIN_ESM. This means that user can configure the device to use one ESM to monitor the error interrupts for the whole device.

10.1.1.1 Using MAIN_ESM to Monitor All Error Interrupts in SoC

In this configuration, the WKUP_ESM is used to consolidate all the error interrupts from the WKUP domain and the WKUP_safe domain as interrupt outputs, and those interrupt outputs from the WKUP_ESM are routed as interrupt inputs to the MAIN_ESM. In order to avoid the interrupt dependence loop, the WKUP_ESM shall disable the interrupt inputs from ESM0.

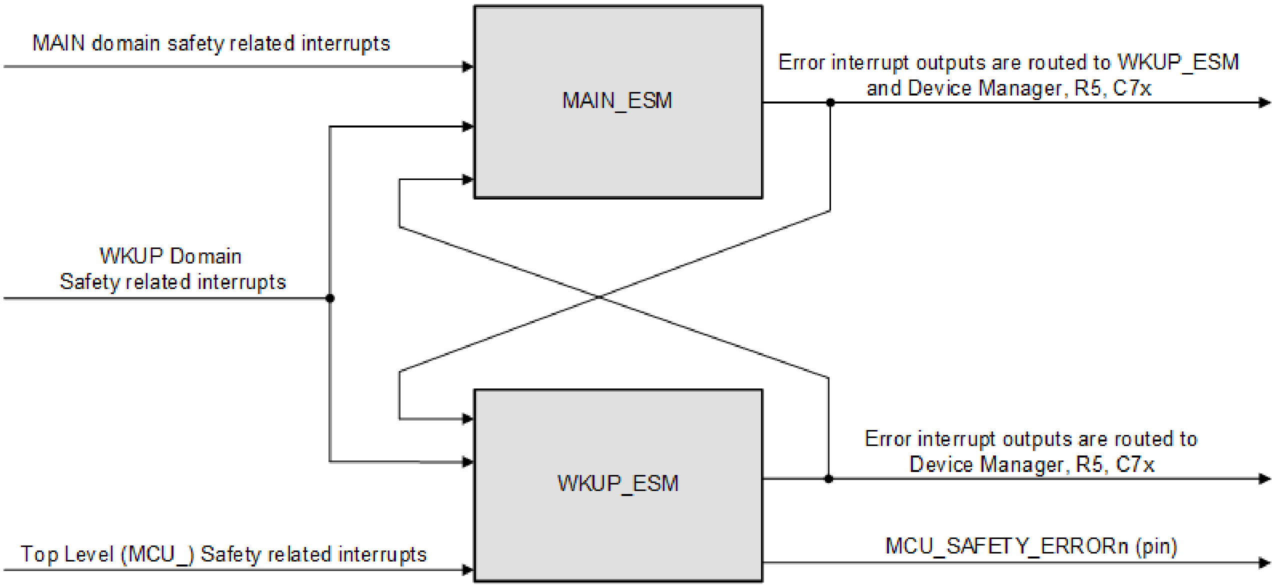


Figure 10-2. Using MAIN_ESM to Monitor All Error Interrupts in SoC

10.1.2 PSIL Events

PSIL Events are mainly generated by the BCDMA and the pktDMA. In addition, the SEC_PROXY IPC module also generates event outputs. PSIL Events can be directly utilized by the BCDMA and the pktDMA. If those events need to be processed by processor, the events need to be converted to interrupts through the Interrupt Aggregator (IA) Module. Refer to *Interrupt Aggregator (INTAGGR)* for information on how IA is used. *Event Handling* shows which modules generates events and how the events are converted to the interrupt.

BCDMA transfer can only be triggered through an event or by software. There are 32 SoC level interrupt signals that can be used to trigger a BCDMA transfer.

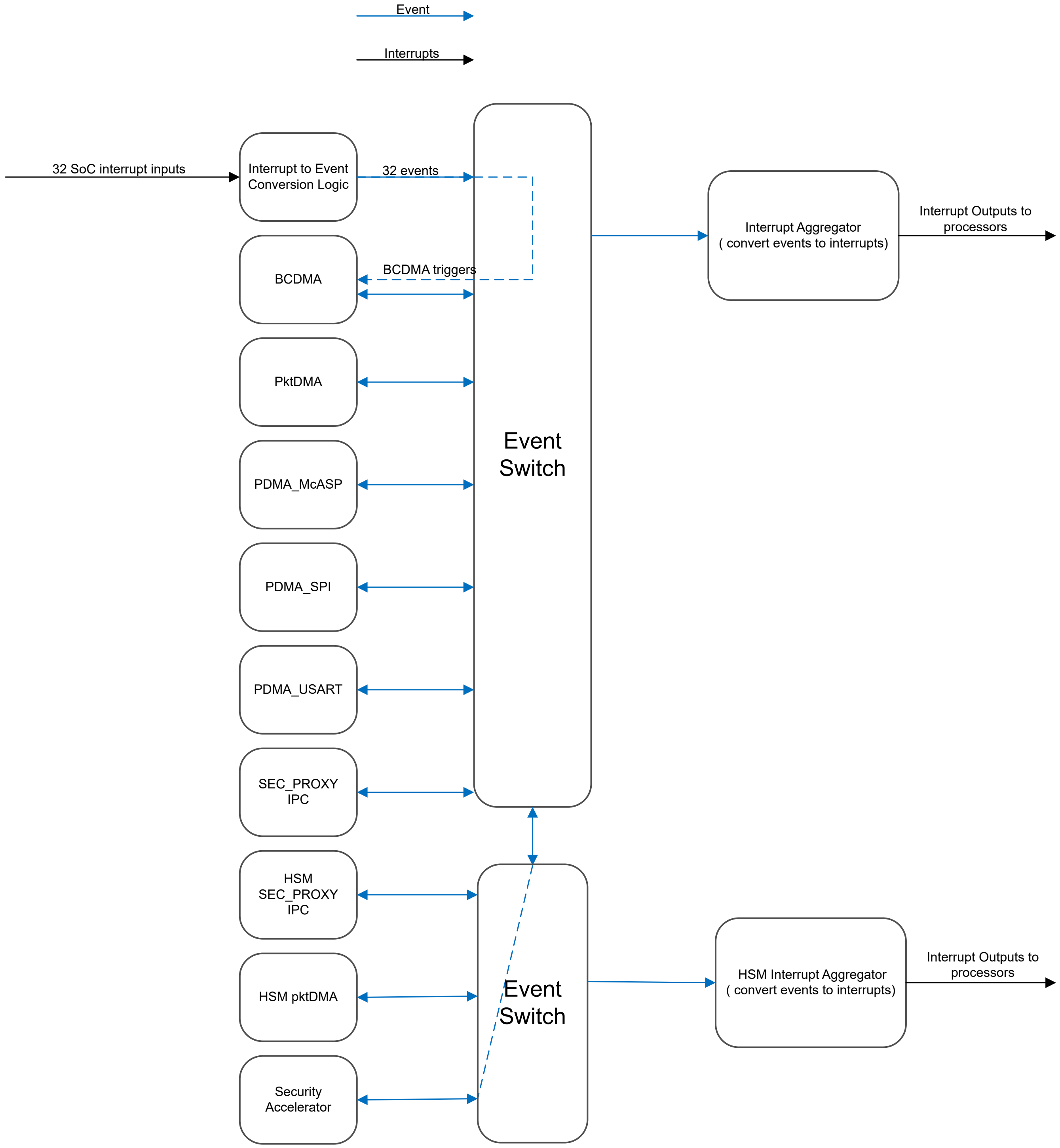


Figure 10-3. Event Handling

BCDMA Triggers shows all the possible interrupt sources which can be used as BCDMA triggers.

10.1.2.1 BCDMA Triggers

Table 10-2. Interrupts Can be Used as BCDMA Triggers

Input Index	Interrupt Source
7	MCRC64.MAIN_0.INT_MCRC.0
8	TIMESYNC_INTROUTER.MAIN_0.OUTL.0
9	TIMESYNC_INTROUTER.MAIN_0.OUTL.1

Table 10-2. Interrupts Can be Used as BCDMA Triggers (continued)

Input Index	Interrupt Source
10	TIMESYNC_INTROUTER.MAIN_0.OUTL.2
11	TIMESYNC_INTROUTER.MAIN_0.OUTL.3
12	TIMESYNC_INTROUTER.MAIN_0.OUTL.4
13	TIMESYNC_INTROUTER.MAIN_0.OUTL.5
14	TIMESYNC_INTROUTER.MAIN_0.OUTL.6
15	TIMESYNC_INTROUTER.MAIN_0.OUTL.7
16	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.48
17	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.49
18	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.50
19	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.51
20	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.52
21	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.53
22	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.54
23	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.55
24	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.56
25	MAIN_GPIO_INTROUTER.MAIN_0.OUTP.57

10.1.3 GPIO Interrupt Handling

There are three GPIO modules in the device, which could generate almost 200 interrupts. Those GPIO interrupt outputs are routed to the GPIO interrupt router first before they are routed to the final interrupt destination. The GPIO interrupt router allows each output to select each GPIO interrupt independently.

The two GPIO modules in the Main domain use one GPIO interrupt router while
the GPIO module in the Top Level domain has its own dedicated GPIO router.
See *GPIO Interrupt Routing*. See also *MAIN_GPIOMUX_INTEROUTER0_INTERRUPT_MAP* and
MCU_GPIOMUX_INTROUTER0_INTERRUPT_MAP

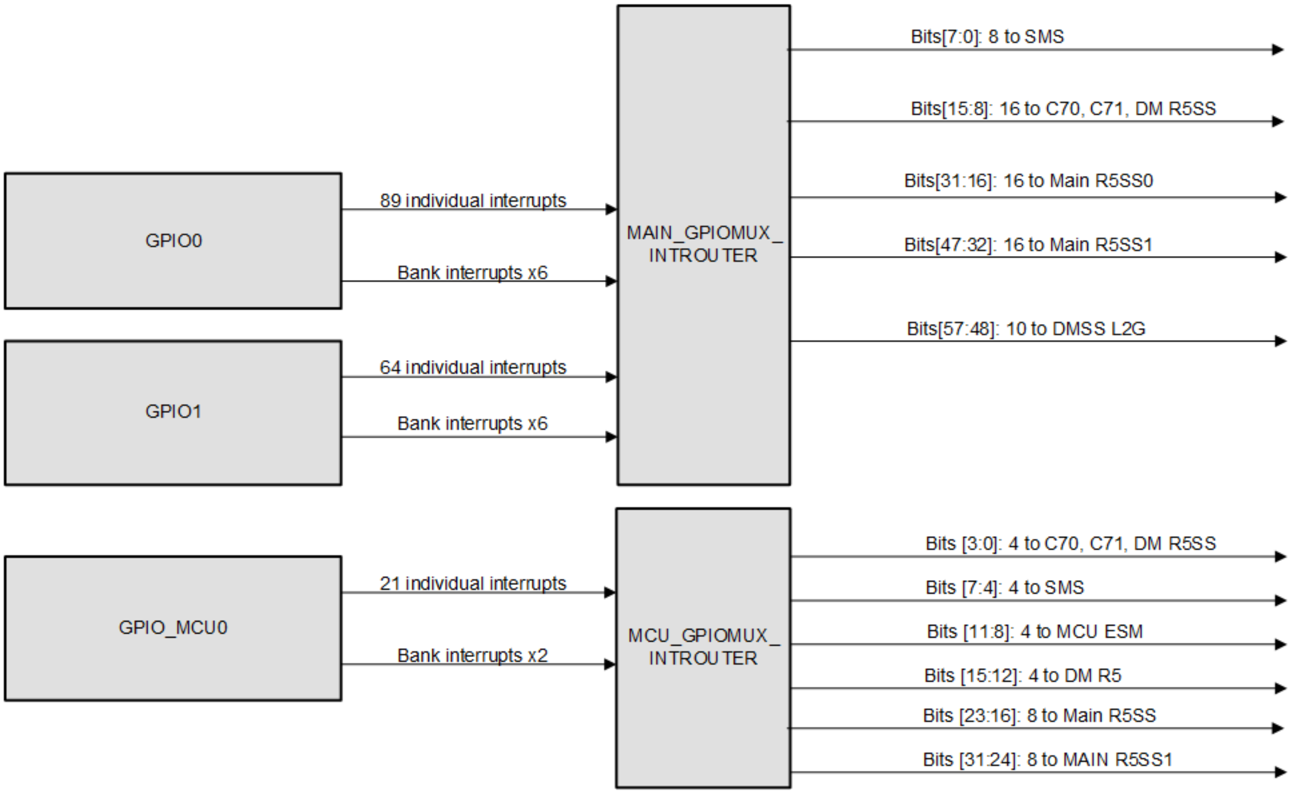


Figure 10-4. GPIO Interrupt Routing

10.1.4 Utilizing Miscellaneous Signals as Interrupt

Some of the signals are aggregated through glue logic and need to be handled separately.

10.1.4.1 Aggregated DCC Interrupt

There are multiple DCC modules in the main domain and each DCC module generates its own DCC_done interrupt. The DCC_done interrupt from all the DCC modules in the main domain are aggregated (ORed) together before it is routed to all the processors, refer to *DCC Intr_done Interrupt Aggregation*.

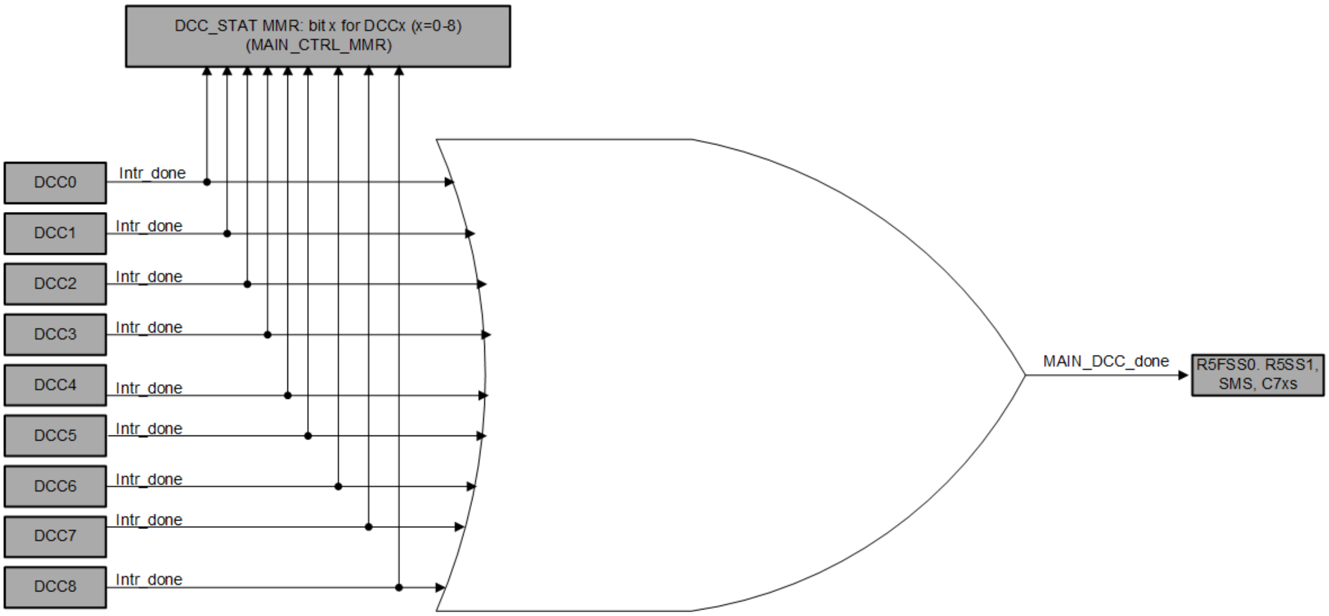


Figure 10-5. DCC Intr_done Interrupt Aggregation

10.1.4.2 Aggregated Access Error Interrupt from CBASS

CBASS modules are the interconnection blocks on the SoC level to provide access path between initiators and targets. When the transaction is not completed successfully, an interrupt is generated by the CBASS and the error transaction is logged by the CBASS module.

There are multiple CBASS modules on the SoC level to provide three layers of interconnect: the data plane, security configuration plane and debug configuration plane. The CBASS access error from the security configuration plane is only routed to HSM, and the other CBASS access errors are aggregated before routing it to the processors, refer to *Aggregated CBASS Access Error*.

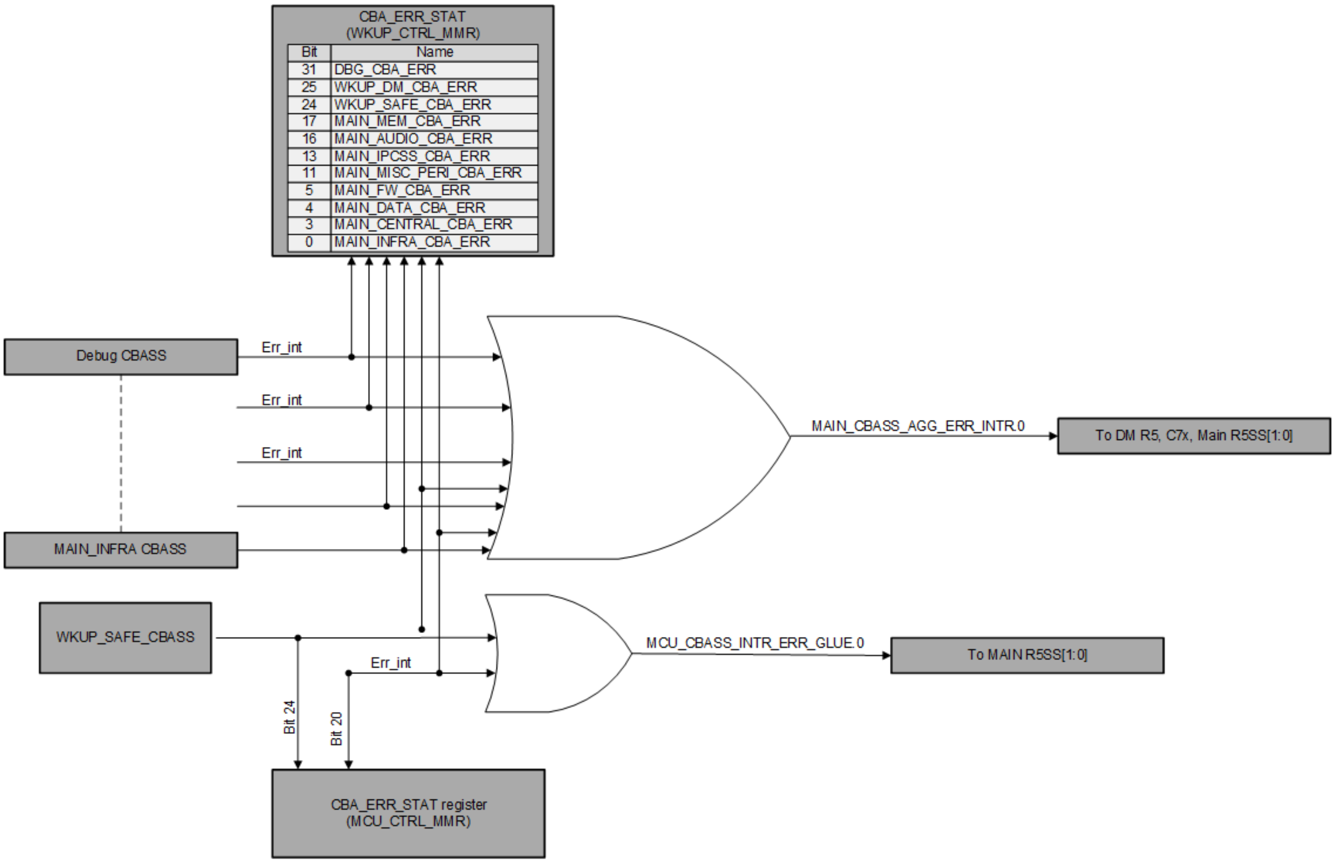


Figure 10-6. Aggregated CBASS Access Error

10.1.4.3 Access Error to Control Register Block Interrupt Aggregation

There are multiple register blocks on the SoC level, and each register block generates an error interrupt when there is an access error. Those access error interrupts are aggregated together before they are routed to processor, refer to *Access Error Aggregation*.

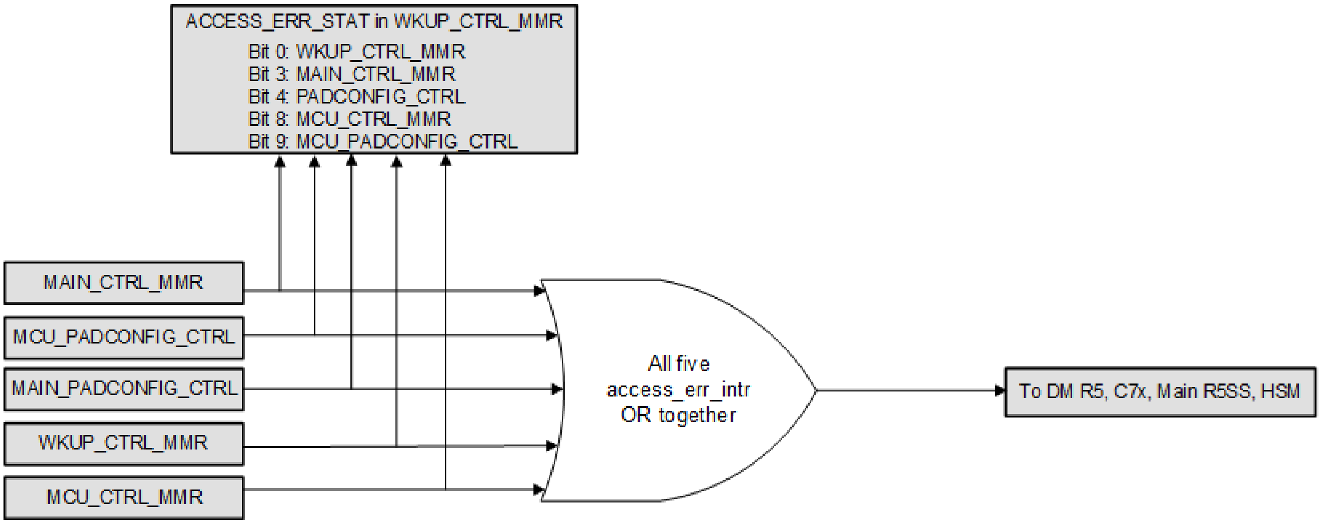


Figure 10-7. Access Error Aggregation

10.2 Interrupt Router (INTROUTER)

10.2.1 INTROUTER Integration

See the Interrupts section of the Module Integration Chapter for details on clocks, resets and hardware requests.

10.3 Interrupt Sources

Interrupts are divided into five subsections

1. Time Synchronization Introuter: Used to provide interrupt muxing function for the time synchronization related interrupts.
2. R5 Interrupts: R5FSS and WKUP R5 processor interrupts
3. C7 Interrupts: C7x Local event controller's (CLEC) routing and handling for C7x processor interrupts
4. Device IN Interrupts: SoC's interrupt output source connections
5. Device OUT Interrupts: SoC's interrupt destination inputs

10.3.1 Time Synchronization Introuter

Table 10-3. TIMESYNC_EVENT_INTROUTER0 OUT Interrupts

Source	Connected To
PINFUNCTION_SYNC0_OUTOUT_SYNC0_OUT_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_16
PINFUNCTION_SYNC1_OUTOUT_SYNC1_OUT_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_17
PINFUNCTION_SYNC2_OUTOUT_SYNC2_OUT_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_18
PINFUNCTION_SYNC3_OUTOUT_SYNC3_OUT_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_19
CPSW0_CPTS_HW1_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_8
CPSW0_CPTS_HW2_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_9
CPSW0_CPTS_HW3_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_10
CPSW0_CPTS_HW4_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_11
CPSW0_CPTS_HW5_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_12
CPSW0_CPTS_HW6_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_13
CPSW0_CPTS_HW7_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_14
CPSW0_CPTS_HW8_PUSH_IN_0	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_15
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_8	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_9	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_1
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_10	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_2
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_11	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_3
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_12	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_4
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_13	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_5
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_14	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_6
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_15	TIMESYNC_EVENT_INTROUTER0_OUTL_OUT_7

Table 10-4. TIMESYNC_EVENT_INTROUTER0 IN Interrupts

IN Interrupt	Connected To
TIMESYNC_EVENT_INTROUTER0_IN_IN_0	TIMER0_TIMER_PWM_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_1	TIMER1_TIMER_PWM_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_2	TIMER2_TIMER_PWM_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_3	TIMER3_TIMER_PWM_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_4	TIMER4_TIMER_PWM_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_5	TIMER5_TIMER_PWM_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_6	TIMER6_TIMER_PWM_OUT_0

Table 10-4. TIMESYNC_EVENT_INTROUTER0 IN Interrupts (continued)

IN Interrupt	Connected To
TIMESYNC_EVENT_INTROUTER0_IN_IN_7	TIMER7_TIMER_PWM_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_8	TIMER8_TIMER_PWM_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_9	EPWM0_EPWM_SYNCO_O_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_11	WKUP_GTC0_GTC_PUSH_EVENT_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_12	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_13	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_16	CPSW0_CPTS_GENF0_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_17	CPSW0_CPTS_GENF1_OUT_0
TIMESYNC_EVENT_INTROUTER0_IN_IN_18	CPSW0_CPTS_SYNC_OUT_0

10.3.2 R5 Interrupts

Table 10-5. R5FSS0_CORE0 IN Interrupts

IN Interrupt	Connected To
R5FSS0_CORE0_INTR_IN_0	MAIN_CTRL_MMR0_IPC_SET16_IPC_SET_IPCFG_OUT_0
R5FSS0_CORE0_INTR_IN_3	EPWM0_EPWM_ETINT_OUT_0
R5FSS0_CORE0_INTR_IN_4	R5FSS0_CORE0_EXP_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_5	R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0
R5FSS0_CORE0_INTR_IN_6	R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0
R5FSS0_CORE0_INTR_IN_7	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7
R5FSS0_CORE0_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168
R5FSS0_CORE0_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169
R5FSS0_CORE0_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170
R5FSS0_CORE0_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171
R5FSS0_CORE0_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172
R5FSS0_CORE0_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173
R5FSS0_CORE0_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174
R5FSS0_CORE0_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175
R5FSS0_CORE0_INTR_IN_16	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
R5FSS0_CORE0_INTR_IN_17	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
R5FSS0_CORE0_INTR_IN_22	TIMER6_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_23	TIMER7_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_24	TIMER0_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_25	TIMER1_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_26	TIMER2_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_27	TIMER3_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_28	TIMER4_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_29	TIMER5_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_30	RTI0_INTR_WWD_OUT_0

Table 10-5. R5FSS0_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE0_INTR_IN_31	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_16
R5FSS0_CORE0_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_17
R5FSS0_CORE0_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18
R5FSS0_CORE0_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19
R5FSS0_CORE0_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20
R5FSS0_CORE0_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21
R5FSS0_CORE0_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22
R5FSS0_CORE0_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23
R5FSS0_CORE0_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24
R5FSS0_CORE0_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25
R5FSS0_CORE0_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26
R5FSS0_CORE0_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27
R5FSS0_CORE0_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28
R5FSS0_CORE0_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29
R5FSS0_CORE0_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30
R5FSS0_CORE0_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31
R5FSS0_CORE0_INTR_IN_48	CPSW0_CPTS_COMP_OUT_0
R5FSS0_CORE0_INTR_IN_50	AASRC0_INFIFO_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_51	AASRC0_INGROUP_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_52	AASRC0_OUTFIFO_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_53	AASRC0_OUTGROUP_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_54	AASRC0_ERR_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_55	AASRC1_INFIFO_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_56	AASRC1_INGROUP_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_57	AASRC1_OUTFIFO_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_58	AASRC1_OUTGROUP_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_59	AASRC1_ERR_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_60	MLB0_MLBSS_MLB_INT_OUT_0
R5FSS0_CORE0_INTR_IN_61	MLB0_MLBSS_MLB_AHB_INT_OUT_0
R5FSS0_CORE0_INTR_IN_62	MLB0_MLBSS_MLB_AHB_INT_OUT_1
R5FSS0_CORE0_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_152
R5FSS0_CORE0_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_153
R5FSS0_CORE0_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_154
R5FSS0_CORE0_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_155
R5FSS0_CORE0_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_156
R5FSS0_CORE0_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_157
R5FSS0_CORE0_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_158
R5FSS0_CORE0_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_159

Table 10-5. R5FSS0_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE0_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_160
R5FSS0_CORE0_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_161
R5FSS0_CORE0_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_162
R5FSS0_CORE0_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_163
R5FSS0_CORE0_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_164
R5FSS0_CORE0_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_165
R5FSS0_CORE0_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_166
R5FSS0_CORE0_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_167
R5FSS0_CORE0_INTR_IN_80	EPWM0_EPWM_TRIPZINT_OUT_0
R5FSS0_CORE0_INTR_IN_81	EPWM1_EPWM_TRIPZINT_OUT_0
R5FSS0_CORE0_INTR_IN_82	EPWM2_EPWM_TRIPZINT_OUT_0
R5FSS0_CORE0_INTR_IN_83	ECAP0_ECAP_INT_OUT_0
R5FSS0_CORE0_INTR_IN_84	ECAP1_ECAP_INT_OUT_0
R5FSS0_CORE0_INTR_IN_85	ECAP2_ECAP_INT_OUT_0
R5FSS0_CORE0_INTR_IN_86	ECAP3_ECAP_INT_OUT_0
R5FSS0_CORE0_INTR_IN_87	ECAP4_ECAP_INT_OUT_0
R5FSS0_CORE0_INTR_IN_88	ECAP5_ECAP_INT_OUT_0
R5FSS0_CORE0_INTR_IN_90	RL2_0_ERR_LVL_OUT_0
R5FSS0_CORE0_INTR_IN_91	RL2_2_ERR_LVL_OUT_0
R5FSS0_CORE0_INTR_IN_92	RL2_3_ERR_LVL_OUT_0
R5FSS0_CORE0_INTR_IN_93	R5FSS0_CORE1_PMU_OUT_0
R5FSS0_CORE0_INTR_IN_94	R5FSS0_CORE0_PMU_OUT_0
R5FSS0_CORE0_INTR_IN_95	R5FSS0_CORE0_VALFIQ_OUT_0
R5FSS0_CORE0_INTR_IN_96	R5FSS0_CORE0_VALIRQ_OUT_0
R5FSS0_CORE0_INTR_IN_97	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_98	EFUSE0_EFC_ERROR_OUT_0
R5FSS0_CORE0_INTR_IN_100	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_16
R5FSS0_CORE0_INTR_IN_101	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_17
R5FSS0_CORE0_INTR_IN_102	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_18
R5FSS0_CORE0_INTR_IN_103	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_19
R5FSS0_CORE0_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_20
R5FSS0_CORE0_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_21
R5FSS0_CORE0_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_22
R5FSS0_CORE0_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_23
R5FSS0_CORE0_INTR_IN_108	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_109	DCC0_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_109	DCC1_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_109	DCC2_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_109	DCC3_INTR_DONE_LEVEL_OUT_0

Table 10-5. R5FSS0_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE0_INTR_IN_109	DCC4_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_109	DCC5_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_109	DCC6_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_109	DCC7_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_109	DCC8_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST0_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST5_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST6_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST7_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST8_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST1_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST2_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST3_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_113	PBIST4_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_114	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_114	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE0_INTR_IN_119	MCRC64_0_INT_MCRC_OUT_0
R5FSS0_CORE0_INTR_IN_120	MCASP0_REC_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_121	MCASP0_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_122	MCASP1_REC_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_123	MCASP1_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_124	MCASP2_REC_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_125	MCASP2_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_126	MCASP3_REC_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_127	MCASP3_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_128	MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS0_CORE0_INTR_IN_128	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS0_CORE0_INTR_IN_128	PADCFG_CTRL0_ACCESS_ERR_OUT_0
R5FSS0_CORE0_INTR_IN_128	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS0_CORE0_INTR_IN_128	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
R5FSS0_CORE0_INTR_IN_130	MCASP4_REC_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_131	MCASP4_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_137	MCU_DCC1_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_140	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0

Table 10-5. R5FSS0_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE0_INTR_IN_141	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
R5FSS0_CORE0_INTR_IN_142	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
R5FSS0_CORE0_INTR_IN_145	WKUP_PSC0_PSC_ALLINT_OUT_0
R5FSS0_CORE0_INTR_IN_146	MAIN_PSC0_PSC_ALLINT_OUT_0
R5FSS0_CORE0_INTR_IN_147	CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_147	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_151	ADC0_GEN_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_153	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_176
R5FSS0_CORE0_INTR_IN_154	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_177
R5FSS0_CORE0_INTR_IN_155	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_178
R5FSS0_CORE0_INTR_IN_156	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_179
R5FSS0_CORE0_INTR_IN_157	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_180
R5FSS0_CORE0_INTR_IN_158	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_181
R5FSS0_CORE0_INTR_IN_159	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_182
R5FSS0_CORE0_INTR_IN_160	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_183
R5FSS0_CORE0_INTR_IN_161	MMCSD0_EMMCSDSS_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
R5FSS0_CORE0_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
R5FSS0_CORE0_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
R5FSS0_CORE0_INTR_IN_171	FSS0_OSPI0_LVL_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_172	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_173	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_174	FSS0_OTFA_INTR_ERR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_175	R5FSS0_CORE0_CTI_OUT_0
R5FSS0_CORE0_INTR_IN_176	R5FSS0_CORE1_CTI_OUT_0
R5FSS0_CORE0_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_178	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_179	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_180	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_181	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_182	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0

Table 10-5. R5FSS0_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE0_INTR_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
R5FSS0_CORE0_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_187	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_188	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_189	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_190	WKUP_I2C0_POINTRPEND_OUT_0
R5FSS0_CORE0_INTR_IN_193	I2C0_POINTRPEND_OUT_0
R5FSS0_CORE0_INTR_IN_194	I2C1_POINTRPEND_OUT_0
R5FSS0_CORE0_INTR_IN_195	I2C2_POINTRPEND_OUT_0
R5FSS0_CORE0_INTR_IN_196	I2C3_POINTRPEND_OUT_0
R5FSS0_CORE0_INTR_IN_197	I2C4_POINTRPEND_OUT_0
R5FSS0_CORE0_INTR_IN_198	I2C5_POINTRPEND_OUT_0
R5FSS0_CORE0_INTR_IN_199	I2C6_POINTRPEND_OUT_0
R5FSS0_CORE0_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_203	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
R5FSS0_CORE0_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
R5FSS0_CORE0_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
R5FSS0_CORE0_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
R5FSS0_CORE0_INTR_IN_207	MCSPI3_INTR_SPI_OUT_0
R5FSS0_CORE0_INTR_IN_208	MCSPI4_INTR_SPI_OUT_0
R5FSS0_CORE0_INTR_IN_210	UART0_USART_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_211	UART1_USART_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_212	UART2_USART_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_213	UART3_USART_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_214	UART4_USART_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_215	UART5_USART_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_216	UART6_USART_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_219	WKUP_UART0_USART_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_220	USB0_IRQ_OUT_0
R5FSS0_CORE0_INTR_IN_221	USB0_IRQ_OUT_1
R5FSS0_CORE0_INTR_IN_222	USB0_IRQ_OUT_2
R5FSS0_CORE0_INTR_IN_223	USB0_IRQ_OUT_3
R5FSS0_CORE0_INTR_IN_224	USB0_IRQ_OUT_4
R5FSS0_CORE0_INTR_IN_225	USB0_IRQ_OUT_5
R5FSS0_CORE0_INTR_IN_226	USB0_IRQ_OUT_6
R5FSS0_CORE0_INTR_IN_227	USB0_IRQ_OUT_7

Table 10-5. R5FSS0_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE0_INTR_IN_228	USB0_MISC_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_229	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_230	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_231	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE0_INTR_IN_232	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_233	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE0_INTR_IN_234	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_235	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE0_INTR_IN_236	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_237	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE0_INTR_IN_238	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE0_INTR_IN_239	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE0_INTR_IN_240	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_241	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_242	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_243	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_1
R5FSS0_CORE0_INTR_IN_248	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_249	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1
R5FSS0_CORE0_INTR_IN_250	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2
R5FSS0_CORE0_INTR_IN_251	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3
R5FSS0_CORE0_INTR_IN_252	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4
R5FSS0_CORE0_INTR_IN_253	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5
R5FSS0_CORE0_INTR_IN_254	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6
R5FSS0_CORE0_INTR_IN_255	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7
R5FSS0_CORE0_INTR_IN_256	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0
R5FSS0_CORE0_INTR_IN_257	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1
R5FSS0_CORE0_INTR_IN_258	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2
R5FSS0_CORE0_INTR_IN_259	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3
R5FSS0_CORE0_INTR_IN_260	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4
R5FSS0_CORE0_INTR_IN_261	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5
R5FSS0_CORE0_INTR_IN_262	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6
R5FSS0_CORE0_INTR_IN_263	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7
R5FSS0_CORE0_INTR_IN_264	TIMER8_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_265	TIMER9_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_266	TIMER10_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_267	TIMER11_INTR_PEND_OUT_0

Table 10-5. R5FSS0_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE0_INTR_IN_268	TIMER12_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_269	TIMER13_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_270	TIMER14_INTR_PEND_OUT_0
R5FSS0_CORE0_INTR_IN_271	TIMER15_INTR_PEND_OUT_0

Table 10-6. R5FSS0_CORE1 IN Interrupts

IN Interrupt	Connected To
R5FSS0_CORE1_INTR_IN_0	MAIN_CTRL_MMR0_IPC_SET17_IPC_SET_IPCFG_OUT_0
R5FSS0_CORE1_INTR_IN_4	R5FSS0_CORE1_EXP_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_5	R5FSS0_COMMON0_COMMRX_LEVEL_1_OUT_0
R5FSS0_CORE1_INTR_IN_6	R5FSS0_COMMON0_COMMTX_LEVEL_1_OUT_0
R5FSS0_CORE1_INTR_IN_7	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7
R5FSS0_CORE1_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168
R5FSS0_CORE1_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169
R5FSS0_CORE1_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170
R5FSS0_CORE1_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171
R5FSS0_CORE1_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172
R5FSS0_CORE1_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173
R5FSS0_CORE1_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174
R5FSS0_CORE1_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175
R5FSS0_CORE1_INTR_IN_16	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
R5FSS0_CORE1_INTR_IN_17	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
R5FSS0_CORE1_INTR_IN_22	TIMER6_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_23	TIMER7_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_24	TIMER0_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_25	TIMER1_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_26	TIMER2_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_27	TIMER3_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_28	TIMER4_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_29	TIMER5_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_30	RTI1_INTR_WWD_OUT_0
R5FSS0_CORE1_INTR_IN_31	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_16
R5FSS0_CORE1_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_17
R5FSS0_CORE1_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18
R5FSS0_CORE1_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19
R5FSS0_CORE1_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20
R5FSS0_CORE1_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21
R5FSS0_CORE1_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22

Table 10-6. R5FSS0_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE1_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23
R5FSS0_CORE1_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24
R5FSS0_CORE1_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25
R5FSS0_CORE1_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26
R5FSS0_CORE1_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27
R5FSS0_CORE1_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28
R5FSS0_CORE1_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29
R5FSS0_CORE1_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30
R5FSS0_CORE1_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31
R5FSS0_CORE1_INTR_IN_48	CPSW0_CPTS_COMP_OUT_0
R5FSS0_CORE1_INTR_IN_49	RL2_0_ERR_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_50	AASRC0_INFIFO_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_51	AASRC0_INGROUP_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_52	AASRC0_OUTFIFO_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_53	AASRC0_OUTGROUP_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_54	AASRC0_ERR_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_55	AASRC1_INFIFO_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_56	AASRC1_INGROUP_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_57	AASRC1_OUTFIFO_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_58	AASRC1_OUTGROUP_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_59	AASRC1_ERR_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_60	MLB0_MLBSS_MLB_INT_OUT_0
R5FSS0_CORE1_INTR_IN_61	MLB0_MLBSS_MLB_AHB_INT_OUT_0
R5FSS0_CORE1_INTR_IN_62	MLB0_MLBSS_MLB_AHB_INT_OUT_1
R5FSS0_CORE1_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_152
R5FSS0_CORE1_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_153
R5FSS0_CORE1_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_154
R5FSS0_CORE1_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_155
R5FSS0_CORE1_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_156
R5FSS0_CORE1_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_157
R5FSS0_CORE1_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_158
R5FSS0_CORE1_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_159
R5FSS0_CORE1_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_160
R5FSS0_CORE1_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_161
R5FSS0_CORE1_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_162
R5FSS0_CORE1_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_163
R5FSS0_CORE1_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_164
R5FSS0_CORE1_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_165
R5FSS0_CORE1_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_166

Table 10-6. R5FSS0_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE1_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_167
R5FSS0_CORE1_INTR_IN_80	EPWM0_EPWM_TRIPZINT_OUT_0
R5FSS0_CORE1_INTR_IN_81	EPWM1_EPWM_TRIPZINT_OUT_0
R5FSS0_CORE1_INTR_IN_82	EPWM2_EPWM_TRIPZINT_OUT_0
R5FSS0_CORE1_INTR_IN_83	ECAP0_ECAP_INT_OUT_0
R5FSS0_CORE1_INTR_IN_84	ECAP1_ECAP_INT_OUT_0
R5FSS0_CORE1_INTR_IN_85	ECAP2_ECAP_INT_OUT_0
R5FSS0_CORE1_INTR_IN_86	ECAP3_ECAP_INT_OUT_0
R5FSS0_CORE1_INTR_IN_87	ECAP4_ECAP_INT_OUT_0
R5FSS0_CORE1_INTR_IN_88	ECAP5_ECAP_INT_OUT_0
R5FSS0_CORE1_INTR_IN_90	RL2_0_ERR_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_91	RL2_2_ERR_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_92	RL2_3_ERR_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_93	R5FSS0_CORE1_PMU_OUT_0
R5FSS0_CORE1_INTR_IN_94	R5FSS0_CORE0_PMU_OUT_0
R5FSS0_CORE1_INTR_IN_95	R5FSS0_CORE1_VALFIQ_OUT_0
R5FSS0_CORE1_INTR_IN_96	R5FSS0_CORE1_VALIRQ_OUT_0
R5FSS0_CORE1_INTR_IN_97	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_98	EFUSE0_EFC_ERROR_OUT_0
R5FSS0_CORE1_INTR_IN_100	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_16
R5FSS0_CORE1_INTR_IN_101	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_17
R5FSS0_CORE1_INTR_IN_102	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_18
R5FSS0_CORE1_INTR_IN_103	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_19
R5FSS0_CORE1_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_20
R5FSS0_CORE1_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_21
R5FSS0_CORE1_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_22
R5FSS0_CORE1_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_23
R5FSS0_CORE1_INTR_IN_108	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC0_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC1_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC2_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC3_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC4_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC5_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC6_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC7_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_109	DCC8_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_113	PBIST0_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	PBIST5_DFT_PBIST_CPU_OUT_0

Table 10-6. R5FSS0_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE1_INTR_IN_113	PBIST6_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	PBIST7_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	PBIST8_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	PBIST1_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	PBIST2_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	PBIST3_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_113	PBIST4_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_114	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_114	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
R5FSS0_CORE1_INTR_IN_119	MCRC64_0_INT_MCRC_OUT_0
R5FSS0_CORE1_INTR_IN_120	MCASP0_REC_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_121	MCASP0_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_122	MCASP1_REC_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_123	MCASP1_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_124	MCASP2_REC_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_125	MCASP2_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_126	MCASP3_REC_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_127	MCASP3_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_128	MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS0_CORE1_INTR_IN_128	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS0_CORE1_INTR_IN_128	PADCFG_CTRL0_ACCESS_ERR_OUT_0
R5FSS0_CORE1_INTR_IN_128	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS0_CORE1_INTR_IN_128	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
R5FSS0_CORE1_INTR_IN_130	MCASP4_REC_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_131	MCASP4_XMIT_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_137	MCU_DCC1_INTR_DONE_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_140	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_141	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_142	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_145	WKUP_PSC0_PSC_ALLINT_OUT_0
R5FSS0_CORE1_INTR_IN_146	MAIN_PSC0_PSC_ALLINT_OUT_0
R5FSS0_CORE1_INTR_IN_147	CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_147	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_147	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0

Table 10-6. R5FSS0_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE1_INTR_IN_147	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_147	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_147	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_147	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_147	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_147	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_147	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_151	ADC0_GEN_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_153	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_176
R5FSS0_CORE1_INTR_IN_154	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_177
R5FSS0_CORE1_INTR_IN_155	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_178
R5FSS0_CORE1_INTR_IN_156	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_179
R5FSS0_CORE1_INTR_IN_157	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_180
R5FSS0_CORE1_INTR_IN_158	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_181
R5FSS0_CORE1_INTR_IN_159	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_182
R5FSS0_CORE1_INTR_IN_160	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_183
R5FSS0_CORE1_INTR_IN_161	MMCSD0_EMMCSDSS_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
R5FSS0_CORE1_INTR_IN_171	FSS0_OSPI0_LVL_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_172	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_173	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_174	FSS0_OTFA_INTR_ERR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_175	R5FSS0_CORE0_CTI_OUT_0
R5FSS0_CORE1_INTR_IN_176	R5FSS0_CORE1_CTI_OUT_0
R5FSS0_CORE1_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_178	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_179	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_180	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_181	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_182	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
R5FSS0_CORE1_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE1_INTR_IN_187	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE1_INTR_IN_188	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE1_INTR_IN_189	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0

Table 10-6. R5FSS0_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE1_INTR_IN_190	WKUP_I2C0_POINTRPEND_OUT_0
R5FSS0_CORE1_INTR_IN_193	I2C0_POINTRPEND_OUT_0
R5FSS0_CORE1_INTR_IN_194	I2C1_POINTRPEND_OUT_0
R5FSS0_CORE1_INTR_IN_195	I2C2_POINTRPEND_OUT_0
R5FSS0_CORE1_INTR_IN_196	I2C3_POINTRPEND_OUT_0
R5FSS0_CORE1_INTR_IN_197	I2C4_POINTRPEND_OUT_0
R5FSS0_CORE1_INTR_IN_198	I2C5_POINTRPEND_OUT_0
R5FSS0_CORE1_INTR_IN_199	I2C6_POINTRPEND_OUT_0
R5FSS0_CORE1_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_203	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
R5FSS0_CORE1_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
R5FSS0_CORE1_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
R5FSS0_CORE1_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
R5FSS0_CORE1_INTR_IN_207	MCSPI3_INTR_SPI_OUT_0
R5FSS0_CORE1_INTR_IN_208	MCSPI4_INTR_SPI_OUT_0
R5FSS0_CORE1_INTR_IN_210	UART0_USART_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_211	UART1_USART_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_212	UART2_USART_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_213	UART3_USART_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_214	UART4_USART_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_215	UART5_USART_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_216	UART6_USART_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_219	WKUP_UART0_USART_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_220	USB0_IRQ_OUT_0
R5FSS0_CORE1_INTR_IN_221	USB0_IRQ_OUT_1
R5FSS0_CORE1_INTR_IN_222	USB0_IRQ_OUT_2
R5FSS0_CORE1_INTR_IN_223	USB0_IRQ_OUT_3
R5FSS0_CORE1_INTR_IN_224	USB0_IRQ_OUT_4
R5FSS0_CORE1_INTR_IN_225	USB0_IRQ_OUT_5
R5FSS0_CORE1_INTR_IN_226	USB0_IRQ_OUT_6
R5FSS0_CORE1_INTR_IN_227	USB0_IRQ_OUT_7
R5FSS0_CORE1_INTR_IN_228	USB0_MISC_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_229	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS0_CORE1_INTR_IN_230	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE1_INTR_IN_231	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE1_INTR_IN_232	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE1_INTR_IN_233	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE1_INTR_IN_234	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0

Table 10-6. R5FSS0_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS0_CORE1_INTR_IN_235	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE1_INTR_IN_236	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE1_INTR_IN_237	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE1_INTR_IN_238	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS0_CORE1_INTR_IN_239	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS0_CORE1_INTR_IN_240	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_1
R5FSS0_CORE1_INTR_IN_241	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_242	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_1
R5FSS0_CORE1_INTR_IN_243	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_1
R5FSS0_CORE1_INTR_IN_248	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_249	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1
R5FSS0_CORE1_INTR_IN_250	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2
R5FSS0_CORE1_INTR_IN_251	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3
R5FSS0_CORE1_INTR_IN_252	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4
R5FSS0_CORE1_INTR_IN_253	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5
R5FSS0_CORE1_INTR_IN_254	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6
R5FSS0_CORE1_INTR_IN_255	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7
R5FSS0_CORE1_INTR_IN_256	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0
R5FSS0_CORE1_INTR_IN_257	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1
R5FSS0_CORE1_INTR_IN_258	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2
R5FSS0_CORE1_INTR_IN_259	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3
R5FSS0_CORE1_INTR_IN_260	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4
R5FSS0_CORE1_INTR_IN_261	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5
R5FSS0_CORE1_INTR_IN_262	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6
R5FSS0_CORE1_INTR_IN_263	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7
R5FSS0_CORE1_INTR_IN_264	TIMER8_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_265	TIMER9_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_266	TIMER10_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_267	TIMER11_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_268	TIMER12_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_269	TIMER13_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_270	TIMER14_INTR_PEND_OUT_0
R5FSS0_CORE1_INTR_IN_271	TIMER15_INTR_PEND_OUT_0

Table 10-7. R5FSS1_CORE0 IN Interrupts

IN Interrupt	Connected To
R5FSS1_CORE0_INTR_IN_0	MAIN_CTRL_MMR0_IPC_SET18_IPC_SET_IPCFG_OUT_0

Table 10-7. R5FSS1_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE0_INTR_IN_4	R5FSS1_CORE0_EXP_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_5	R5FSS1_COMMON0_COMMRX_LEVEL_0_OUT_0
R5FSS1_CORE0_INTR_IN_6	R5FSS1_COMMON0_COMMTX_LEVEL_0_OUT_0
R5FSS1_CORE0_INTR_IN_7	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7
R5FSS1_CORE0_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16
R5FSS1_CORE0_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17
R5FSS1_CORE0_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18
R5FSS1_CORE0_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19
R5FSS1_CORE0_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20
R5FSS1_CORE0_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21
R5FSS1_CORE0_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22
R5FSS1_CORE0_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23
R5FSS1_CORE0_INTR_IN_16	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
R5FSS1_CORE0_INTR_IN_17	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
R5FSS1_CORE0_INTR_IN_22	TIMER6_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_23	TIMER7_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_24	TIMER0_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_25	TIMER1_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_26	TIMER2_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_27	TIMER3_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_28	TIMER4_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_29	TIMER5_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_30	RTI2_INTR_WWD_OUT_0
R5FSS1_CORE0_INTR_IN_31	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_32
R5FSS1_CORE0_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_33
R5FSS1_CORE0_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34
R5FSS1_CORE0_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35
R5FSS1_CORE0_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_36
R5FSS1_CORE0_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_37
R5FSS1_CORE0_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_38
R5FSS1_CORE0_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_39
R5FSS1_CORE0_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_40
R5FSS1_CORE0_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_41
R5FSS1_CORE0_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_42
R5FSS1_CORE0_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_43
R5FSS1_CORE0_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_44
R5FSS1_CORE0_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_45
R5FSS1_CORE0_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_46

Table 10-7. R5FSS1_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE0_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_47
R5FSS1_CORE0_INTR_IN_48	CPSW0_CPTS_COMP_OUT_0
R5FSS1_CORE0_INTR_IN_49	RL2_2_ERR_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_50	AASRC0_INFIFO_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_51	AASRC0_INGROUP_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_52	AASRC0_OUTFIFO_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_53	AASRC0_OUTGROUP_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_54	AASRC0_ERR_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_55	AASRC1_INFIFO_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_56	AASRC1_INGROUP_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_57	AASRC1_OUTFIFO_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_58	AASRC1_OUTGROUP_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_59	AASRC1_ERR_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_60	MLB0_MLBSS_MLB_INT_OUT_0
R5FSS1_CORE0_INTR_IN_61	MLB0_MLBSS_MLB_AHB_INT_OUT_0
R5FSS1_CORE0_INTR_IN_62	MLB0_MLBSS_MLB_AHB_INT_OUT_1
R5FSS1_CORE0_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1
R5FSS1_CORE0_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2
R5FSS1_CORE0_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3
R5FSS1_CORE0_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4
R5FSS1_CORE0_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5
R5FSS1_CORE0_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6
R5FSS1_CORE0_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7
R5FSS1_CORE0_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8
R5FSS1_CORE0_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9
R5FSS1_CORE0_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10
R5FSS1_CORE0_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11
R5FSS1_CORE0_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12
R5FSS1_CORE0_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13
R5FSS1_CORE0_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14
R5FSS1_CORE0_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15
R5FSS1_CORE0_INTR_IN_80	EPWM0_EPWM_TRIPZINT_OUT_0
R5FSS1_CORE0_INTR_IN_81	EPWM1_EPWM_TRIPZINT_OUT_0
R5FSS1_CORE0_INTR_IN_82	EPWM2_EPWM_TRIPZINT_OUT_0
R5FSS1_CORE0_INTR_IN_83	ECAP0_ECAP_INT_OUT_0
R5FSS1_CORE0_INTR_IN_84	ECAP1_ECAP_INT_OUT_0
R5FSS1_CORE0_INTR_IN_85	ECAP2_ECAP_INT_OUT_0
R5FSS1_CORE0_INTR_IN_86	ECAP3_ECAP_INT_OUT_0

Table 10-7. R5FSS1_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE0_INTR_IN_87	ECAP4_ECAP_INT_OUT_0
R5FSS1_CORE0_INTR_IN_88	ECAP5_ECAP_INT_OUT_0
R5FSS1_CORE0_INTR_IN_90	RL2_0_ERR_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_91	RL2_2_ERR_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_92	RL2_3_ERR_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_93	R5FSS1_CORE1_PMU_OUT_0
R5FSS1_CORE0_INTR_IN_94	R5FSS1_CORE0_PMU_OUT_0
R5FSS1_CORE0_INTR_IN_95	R5FSS1_CORE0_VALFIQ_OUT_0
R5FSS1_CORE0_INTR_IN_96	R5FSS1_CORE0_VALIRQ_OUT_0
R5FSS1_CORE0_INTR_IN_97	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_98	EFUSE0_EFC_ERROR_OUT_0
R5FSS1_CORE0_INTR_IN_100	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_24
R5FSS1_CORE0_INTR_IN_101	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_25
R5FSS1_CORE0_INTR_IN_102	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_26
R5FSS1_CORE0_INTR_IN_103	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_27
R5FSS1_CORE0_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_28
R5FSS1_CORE0_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_29
R5FSS1_CORE0_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_30
R5FSS1_CORE0_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_31
R5FSS1_CORE0_INTR_IN_108	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC0_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC1_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC2_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC3_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC4_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC5_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC6_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC7_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_109	DCC8_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_113	PBIST0_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	PBIST5_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	PBIST6_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	PBIST7_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	PBIST8_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	PBIST1_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	PBIST2_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_113	PBIST3_DFT_PBIST_CPU_OUT_0

Table 10-7. R5FSS1_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE0_INTR_IN_113	PBIST4_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_114	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_114	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE0_INTR_IN_119	MCRC64_0_INT_MCRC_OUT_0
R5FSS1_CORE0_INTR_IN_120	MCASP0_REC_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_121	MCASP0_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_122	MCASP1_REC_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_123	MCASP1_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_124	MCASP2_REC_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_125	MCASP2_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_126	MCASP3_REC_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_127	MCASP3_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_128	MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS1_CORE0_INTR_IN_128	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS1_CORE0_INTR_IN_128	PADCFG_CTRL0_ACCESS_ERR_OUT_0
R5FSS1_CORE0_INTR_IN_128	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS1_CORE0_INTR_IN_128	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
R5FSS1_CORE0_INTR_IN_130	MCASP4_REC_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_131	MCASP4_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_137	MCU_DCC1_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_140	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_141	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_142	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_145	WKUP_PSC0_PSC_ALLINT_OUT_0
R5FSS1_CORE0_INTR_IN_146	MAIN_PSC0_PSC_ALLINT_OUT_0
R5FSS1_CORE0_INTR_IN_147	CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_147	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_151	ADC0_GEN_LEVEL_OUT_0

Table 10-7. R5FSS1_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE0_INTR_IN_153	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24
R5FSS1_CORE0_INTR_IN_154	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25
R5FSS1_CORE0_INTR_IN_155	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26
R5FSS1_CORE0_INTR_IN_156	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27
R5FSS1_CORE0_INTR_IN_157	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28
R5FSS1_CORE0_INTR_IN_158	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29
R5FSS1_CORE0_INTR_IN_159	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30
R5FSS1_CORE0_INTR_IN_160	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31
R5FSS1_CORE0_INTR_IN_161	MMCSD0_EMMCSDSS_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
R5FSS1_CORE0_INTR_IN_171	FSS0_OSPI0_LVL_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_172	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_173	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_174	FSS0_OTFA_INTR_ERR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_175	R5FSS1_CORE0_CTI_OUT_0
R5FSS1_CORE0_INTR_IN_176	R5FSS1_CORE1_CTI_OUT_0
R5FSS1_CORE0_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_178	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_179	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_180	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_181	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_182	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
R5FSS1_CORE0_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_187	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_188	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_189	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_190	WKUP_I2C0_POINTRPEND_OUT_0
R5FSS1_CORE0_INTR_IN_193	I2C0_POINTRPEND_OUT_0
R5FSS1_CORE0_INTR_IN_194	I2C1_POINTRPEND_OUT_0
R5FSS1_CORE0_INTR_IN_195	I2C2_POINTRPEND_OUT_0
R5FSS1_CORE0_INTR_IN_196	I2C3_POINTRPEND_OUT_0
R5FSS1_CORE0_INTR_IN_197	I2C4_POINTRPEND_OUT_0
R5FSS1_CORE0_INTR_IN_198	I2C5_POINTRPEND_OUT_0
R5FSS1_CORE0_INTR_IN_199	I2C6_POINTRPEND_OUT_0

Table 10-7. R5FSS1_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE0_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_203	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
R5FSS1_CORE0_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
R5FSS1_CORE0_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
R5FSS1_CORE0_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
R5FSS1_CORE0_INTR_IN_207	MCSPI3_INTR_SPI_OUT_0
R5FSS1_CORE0_INTR_IN_208	MCSPI4_INTR_SPI_OUT_0
R5FSS1_CORE0_INTR_IN_210	UART0_USART_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_211	UART1_USART_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_212	UART2_USART_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_213	UART3_USART_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_214	UART4_USART_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_215	UART5_USART_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_216	UART6_USART_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_219	WKUP_UART0_USART_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_220	USB0_IRQ_OUT_0
R5FSS1_CORE0_INTR_IN_221	USB0_IRQ_OUT_1
R5FSS1_CORE0_INTR_IN_222	USB0_IRQ_OUT_2
R5FSS1_CORE0_INTR_IN_223	USB0_IRQ_OUT_3
R5FSS1_CORE0_INTR_IN_224	USB0_IRQ_OUT_4
R5FSS1_CORE0_INTR_IN_225	USB0_IRQ_OUT_5
R5FSS1_CORE0_INTR_IN_226	USB0_IRQ_OUT_6
R5FSS1_CORE0_INTR_IN_227	USB0_IRQ_OUT_7
R5FSS1_CORE0_INTR_IN_228	USB0_MISC_LEVEL_OUT_0
R5FSS1_CORE0_INTR_IN_229	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_230	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_231	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE0_INTR_IN_232	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_233	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE0_INTR_IN_234	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_235	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE0_INTR_IN_236	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_237	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE0_INTR_IN_238	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE0_INTR_IN_239	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE0_INTR_IN_240	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_2

Table 10-7. R5FSS1_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE0_INTR_IN_241	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_1
R5FSS1_CORE0_INTR_IN_242	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_243	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_2
R5FSS1_CORE0_INTR_IN_248	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8
R5FSS1_CORE0_INTR_IN_249	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9
R5FSS1_CORE0_INTR_IN_250	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10
R5FSS1_CORE0_INTR_IN_251	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11
R5FSS1_CORE0_INTR_IN_252	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12
R5FSS1_CORE0_INTR_IN_253	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13
R5FSS1_CORE0_INTR_IN_254	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14
R5FSS1_CORE0_INTR_IN_255	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15
R5FSS1_CORE0_INTR_IN_256	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8
R5FSS1_CORE0_INTR_IN_257	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9
R5FSS1_CORE0_INTR_IN_258	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10
R5FSS1_CORE0_INTR_IN_259	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11
R5FSS1_CORE0_INTR_IN_260	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12
R5FSS1_CORE0_INTR_IN_261	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13
R5FSS1_CORE0_INTR_IN_262	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14
R5FSS1_CORE0_INTR_IN_263	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15
R5FSS1_CORE0_INTR_IN_264	TIMER8_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_265	TIMER9_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_266	TIMER10_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_267	TIMER11_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_268	TIMER12_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_269	TIMER13_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_270	TIMER14_INTR_PEND_OUT_0
R5FSS1_CORE0_INTR_IN_271	TIMER15_INTR_PEND_OUT_0

Table 10-8. R5FSS1_CORE1 IN Interrupts

IN Interrupt	Connected To
R5FSS1_CORE1_INTR_IN_0	MAIN_CTRL_MMR0_IPC_SET19_IPC_SET_IPCFG_OUT_0
R5FSS1_CORE1_INTR_IN_4	R5FSS1_CORE1_EXP_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_5	R5FSS1_COMMON0_COMMRX_LEVEL_1_OUT_0
R5FSS1_CORE1_INTR_IN_6	R5FSS1_COMMON0_COMMTX_LEVEL_1_OUT_0
R5FSS1_CORE1_INTR_IN_7	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7
R5FSS1_CORE1_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16
R5FSS1_CORE1_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17

Table 10-8. R5FSS1_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE1_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18
R5FSS1_CORE1_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19
R5FSS1_CORE1_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20
R5FSS1_CORE1_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21
R5FSS1_CORE1_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22
R5FSS1_CORE1_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23
R5FSS1_CORE1_INTR_IN_16	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
R5FSS1_CORE1_INTR_IN_17	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
R5FSS1_CORE1_INTR_IN_22	TIMER6_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_23	TIMER7_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_24	TIMER0_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_25	TIMER1_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_26	TIMER2_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_27	TIMER3_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_28	TIMER4_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_29	TIMER5_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_30	RTI3_INTR_WWD_OUT_0
R5FSS1_CORE1_INTR_IN_31	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_32
R5FSS1_CORE1_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_33
R5FSS1_CORE1_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34
R5FSS1_CORE1_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35
R5FSS1_CORE1_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_36
R5FSS1_CORE1_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_37
R5FSS1_CORE1_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_38
R5FSS1_CORE1_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_39
R5FSS1_CORE1_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_40
R5FSS1_CORE1_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_41
R5FSS1_CORE1_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_42
R5FSS1_CORE1_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_43
R5FSS1_CORE1_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_44
R5FSS1_CORE1_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_45
R5FSS1_CORE1_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_46
R5FSS1_CORE1_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_47
R5FSS1_CORE1_INTR_IN_48	CPSW0_CPTS_COMP_OUT_0
R5FSS1_CORE1_INTR_IN_49	RL2_3_ERR_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_50	AASRC0_INFIFO_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_51	AASRC0_INGROUP_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_52	AASRC0_OUTFIFO_LEVEL_OUT_0

Table 10-8. R5FSS1_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE1_INTR_IN_53	AASRC0_OUTGROUP_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_54	AASRC0_ERR_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_55	AASRC1_INFIFO_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_56	AASRC1_INGROUP_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_57	AASRC1_OUTFIFO_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_58	AASRC1_OUTGROUP_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_59	AASRC1_ERR_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_60	MLB0_MLBSS_MLB_INT_OUT_0
R5FSS1_CORE1_INTR_IN_61	MLB0_MLBSS_MLB_AHB_INT_OUT_0
R5FSS1_CORE1_INTR_IN_62	MLB0_MLBSS_MLB_AHB_INT_OUT_1
R5FSS1_CORE1_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1
R5FSS1_CORE1_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2
R5FSS1_CORE1_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3
R5FSS1_CORE1_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4
R5FSS1_CORE1_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5
R5FSS1_CORE1_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6
R5FSS1_CORE1_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7
R5FSS1_CORE1_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8
R5FSS1_CORE1_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9
R5FSS1_CORE1_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10
R5FSS1_CORE1_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11
R5FSS1_CORE1_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12
R5FSS1_CORE1_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13
R5FSS1_CORE1_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14
R5FSS1_CORE1_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15
R5FSS1_CORE1_INTR_IN_80	EPWM0_EPWM_TRIPZINT_OUT_0
R5FSS1_CORE1_INTR_IN_81	EPWM1_EPWM_TRIPZINT_OUT_0
R5FSS1_CORE1_INTR_IN_82	EPWM2_EPWM_TRIPZINT_OUT_0
R5FSS1_CORE1_INTR_IN_83	ECAP0_ECAP_INT_OUT_0
R5FSS1_CORE1_INTR_IN_84	ECAP1_ECAP_INT_OUT_0
R5FSS1_CORE1_INTR_IN_85	ECAP2_ECAP_INT_OUT_0
R5FSS1_CORE1_INTR_IN_86	ECAP3_ECAP_INT_OUT_0
R5FSS1_CORE1_INTR_IN_87	ECAP4_ECAP_INT_OUT_0
R5FSS1_CORE1_INTR_IN_88	ECAP5_ECAP_INT_OUT_0
R5FSS1_CORE1_INTR_IN_90	RL2_0_ERR_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_91	RL2_2_ERR_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_92	RL2_3_ERR_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_93	R5FSS1_CORE1_PMU_OUT_0

Table 10-8. R5FSS1_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE1_INTR_IN_94	R5FSS1_CORE0_PMU_OUT_0
R5FSS1_CORE1_INTR_IN_95	R5FSS1_CORE1_VALFIQ_OUT_0
R5FSS1_CORE1_INTR_IN_96	R5FSS1_CORE1_VALIRQ_OUT_0
R5FSS1_CORE1_INTR_IN_97	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_98	EFUSE0_EFC_ERROR_OUT_0
R5FSS1_CORE1_INTR_IN_100	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_24
R5FSS1_CORE1_INTR_IN_101	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_25
R5FSS1_CORE1_INTR_IN_102	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_26
R5FSS1_CORE1_INTR_IN_103	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_27
R5FSS1_CORE1_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_28
R5FSS1_CORE1_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_29
R5FSS1_CORE1_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_30
R5FSS1_CORE1_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_31
R5FSS1_CORE1_INTR_IN_108	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC0_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC1_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC2_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC3_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC4_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC5_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC6_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC7_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_109	DCC8_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST0_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST5_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST6_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST7_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST8_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST1_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST2_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST3_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_113	PBIST4_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_114	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_114	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
R5FSS1_CORE1_INTR_IN_119	MCRC64_0_INT_MCRC_OUT_0
R5FSS1_CORE1_INTR_IN_120	MCASP0_REC_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_121	MCASP0_XMIT_INTR_PEND_OUT_0

Table 10-8. R5FSS1_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE1_INTR_IN_122	MCASP1_REC_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_123	MCASP1_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_124	MCASP2_REC_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_125	MCASP2_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_126	MCASP3_REC_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_127	MCASP3_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_128	MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS1_CORE1_INTR_IN_128	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS1_CORE1_INTR_IN_128	PADCFG_CTRL0_ACCESS_ERR_OUT_0
R5FSS1_CORE1_INTR_IN_128	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
R5FSS1_CORE1_INTR_IN_128	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
R5FSS1_CORE1_INTR_IN_130	MCASP4_REC_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_131	MCASP4_XMIT_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_137	MCU_DCC1_INTR_DONE_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_140	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_141	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_142	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_145	WKUP_PSC0_PSC_ALLINT_OUT_0
R5FSS1_CORE1_INTR_IN_146	MAIN_PSC0_PSC_ALLINT_OUT_0
R5FSS1_CORE1_INTR_IN_147	CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_147	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_151	ADC0_GEN_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_153	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24
R5FSS1_CORE1_INTR_IN_154	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25
R5FSS1_CORE1_INTR_IN_155	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26
R5FSS1_CORE1_INTR_IN_156	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27
R5FSS1_CORE1_INTR_IN_157	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28
R5FSS1_CORE1_INTR_IN_158	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29

Table 10-8. R5FSS1_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE1_INTR_IN_159	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30
R5FSS1_CORE1_INTR_IN_160	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31
R5FSS1_CORE1_INTR_IN_161	MMCSD0_EMMCSDSS_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
R5FSS1_CORE1_INTR_IN_171	FSS0_OSPI0_LVL_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_172	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_173	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_174	FSS0_OTFA_INTR_ERR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_175	R5FSS1_CORE0_CTI_OUT_0
R5FSS1_CORE1_INTR_IN_176	R5FSS1_CORE1_CTI_OUT_0
R5FSS1_CORE1_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_178	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_179	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_180	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_181	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_182	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
R5FSS1_CORE1_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_187	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_188	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_189	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_190	WKUP_I2C0_POINTRPEND_OUT_0
R5FSS1_CORE1_INTR_IN_193	I2C0_POINTRPEND_OUT_0
R5FSS1_CORE1_INTR_IN_194	I2C1_POINTRPEND_OUT_0
R5FSS1_CORE1_INTR_IN_195	I2C2_POINTRPEND_OUT_0
R5FSS1_CORE1_INTR_IN_196	I2C3_POINTRPEND_OUT_0
R5FSS1_CORE1_INTR_IN_197	I2C4_POINTRPEND_OUT_0
R5FSS1_CORE1_INTR_IN_198	I2C5_POINTRPEND_OUT_0
R5FSS1_CORE1_INTR_IN_199	I2C6_POINTRPEND_OUT_0
R5FSS1_CORE1_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_203	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
R5FSS1_CORE1_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
R5FSS1_CORE1_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
R5FSS1_CORE1_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0

Table 10-8. R5FSS1_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE1_INTR_IN_207	MCSPI3_INTR_SPI_OUT_0
R5FSS1_CORE1_INTR_IN_208	MCSPI4_INTR_SPI_OUT_0
R5FSS1_CORE1_INTR_IN_210	UART0_USART_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_211	UART1_USART_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_212	UART2_USART_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_213	UART3_USART_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_214	UART4_USART_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_215	UART5_USART_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_216	UART6_USART_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_219	WKUP_UART0_USART_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_220	USB0_IRQ_OUT_0
R5FSS1_CORE1_INTR_IN_221	USB0_IRQ_OUT_1
R5FSS1_CORE1_INTR_IN_222	USB0_IRQ_OUT_2
R5FSS1_CORE1_INTR_IN_223	USB0_IRQ_OUT_3
R5FSS1_CORE1_INTR_IN_224	USB0_IRQ_OUT_4
R5FSS1_CORE1_INTR_IN_225	USB0_IRQ_OUT_5
R5FSS1_CORE1_INTR_IN_226	USB0_IRQ_OUT_6
R5FSS1_CORE1_INTR_IN_227	USB0_IRQ_OUT_7
R5FSS1_CORE1_INTR_IN_228	USB0_MISC_LEVEL_OUT_0
R5FSS1_CORE1_INTR_IN_229	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_230	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_231	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE1_INTR_IN_232	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_233	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE1_INTR_IN_234	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_235	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE1_INTR_IN_236	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_237	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE1_INTR_IN_238	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0
R5FSS1_CORE1_INTR_IN_239	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1
R5FSS1_CORE1_INTR_IN_240	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_3
R5FSS1_CORE1_INTR_IN_241	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_1
R5FSS1_CORE1_INTR_IN_242	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_1
R5FSS1_CORE1_INTR_IN_243	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_2
R5FSS1_CORE1_INTR_IN_248	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8
R5FSS1_CORE1_INTR_IN_249	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9

Table 10-8. R5FSS1_CORE1 IN Interrupts (continued)

IN Interrupt	Connected To
R5FSS1_CORE1_INTR_IN_250	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10
R5FSS1_CORE1_INTR_IN_251	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11
R5FSS1_CORE1_INTR_IN_252	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12
R5FSS1_CORE1_INTR_IN_253	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13
R5FSS1_CORE1_INTR_IN_254	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14
R5FSS1_CORE1_INTR_IN_255	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15
R5FSS1_CORE1_INTR_IN_256	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8
R5FSS1_CORE1_INTR_IN_257	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9
R5FSS1_CORE1_INTR_IN_258	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10
R5FSS1_CORE1_INTR_IN_259	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11
R5FSS1_CORE1_INTR_IN_260	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12
R5FSS1_CORE1_INTR_IN_261	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13
R5FSS1_CORE1_INTR_IN_262	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14
R5FSS1_CORE1_INTR_IN_263	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15
R5FSS1_CORE1_INTR_IN_264	TIMER8_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_265	TIMER9_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_266	TIMER10_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_267	TIMER11_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_268	TIMER12_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_269	TIMER13_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_270	TIMER14_INTR_PEND_OUT_0
R5FSS1_CORE1_INTR_IN_271	TIMER15_INTR_PEND_OUT_0

Table 10-9. WKUP_R5FSS_CORE0 IN Interrupts

IN Interrupt	Connected To
WKUP_R5FSS0_CORE0_INTR_IN_0	MCU_CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_4	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_5	WKUP_R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_6	WKUP_R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_7	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_6
WKUP_R5FSS0_CORE0_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72
WKUP_R5FSS0_CORE0_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73
WKUP_R5FSS0_CORE0_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74
WKUP_R5FSS0_CORE0_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75
WKUP_R5FSS0_CORE0_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76
WKUP_R5FSS0_CORE0_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77
WKUP_R5FSS0_CORE0_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78
WKUP_R5FSS0_CORE0_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79
WKUP_R5FSS0_CORE0_INTR_IN_16	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0

Table 10-9. WKUP_R5FSS_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_R5FSS0_CORE0_INTR_IN_17	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_18	MCU_GPIO0_GPIO_LVL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_23	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_28	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_29	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_30	WKUP_RTI0_INTR_WWD_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
WKUP_R5FSS0_CORE0_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
WKUP_R5FSS0_CORE0_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
WKUP_R5FSS0_CORE0_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
WKUP_R5FSS0_CORE0_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
WKUP_R5FSS0_CORE0_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
WKUP_R5FSS0_CORE0_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
WKUP_R5FSS0_CORE0_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
WKUP_R5FSS0_CORE0_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
WKUP_R5FSS0_CORE0_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
WKUP_R5FSS0_CORE0_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
WKUP_R5FSS0_CORE0_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
WKUP_R5FSS0_CORE0_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
WKUP_R5FSS0_CORE0_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
WKUP_R5FSS0_CORE0_INTR_IN_48	CPSW0_CPTS_COMP_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_50	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_12
WKUP_R5FSS0_CORE0_INTR_IN_51	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_13
WKUP_R5FSS0_CORE0_INTR_IN_52	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_14
WKUP_R5FSS0_CORE0_INTR_IN_53	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_15
WKUP_R5FSS0_CORE0_INTR_IN_56	GPIO0_GPIO_BANK_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_57	GPIO0_GPIO_BANK_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_58	WKUP_R5FSS0_CORE0_PMU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_59	WKUP_R5FSS0_CORE0_VALFIQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_60	WKUP_R5FSS0_CORE0_VALIRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_61	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40
WKUP_R5FSS0_CORE0_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41
WKUP_R5FSS0_CORE0_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42
WKUP_R5FSS0_CORE0_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43
WKUP_R5FSS0_CORE0_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44
WKUP_R5FSS0_CORE0_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45

Table 10-9. WKUP_R5FSS_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_R5FSS0_CORE0_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46
WKUP_R5FSS0_CORE0_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47
WKUP_R5FSS0_CORE0_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48
WKUP_R5FSS0_CORE0_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49
WKUP_R5FSS0_CORE0_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50
WKUP_R5FSS0_CORE0_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51
WKUP_R5FSS0_CORE0_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52
WKUP_R5FSS0_CORE0_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53
WKUP_R5FSS0_CORE0_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54
WKUP_R5FSS0_CORE0_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55
WKUP_R5FSS0_CORE0_INTR_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56
WKUP_R5FSS0_CORE0_INTR_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57
WKUP_R5FSS0_CORE0_INTR_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58
WKUP_R5FSS0_CORE0_INTR_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59
WKUP_R5FSS0_CORE0_INTR_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60
WKUP_R5FSS0_CORE0_INTR_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61
WKUP_R5FSS0_CORE0_INTR_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62
WKUP_R5FSS0_CORE0_INTR_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63
WKUP_R5FSS0_CORE0_INTR_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64
WKUP_R5FSS0_CORE0_INTR_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65
WKUP_R5FSS0_CORE0_INTR_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66
WKUP_R5FSS0_CORE0_INTR_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67
WKUP_R5FSS0_CORE0_INTR_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68
WKUP_R5FSS0_CORE0_INTR_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69
WKUP_R5FSS0_CORE0_INTR_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70
WKUP_R5FSS0_CORE0_INTR_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71
WKUP_R5FSS0_CORE0_INTR_IN_97	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_98	EFUSE0_EFC_ERROR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
WKUP_R5FSS0_CORE0_INTR_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
WKUP_R5FSS0_CORE0_INTR_IN_108	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC0_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC1_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC2_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC3_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC4_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC5_INTR_DONE_LEVEL_OUT_0

Table 10-9. WKUP_R5FSS_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC6_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC7_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_109	DCC8_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST0_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST5_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST6_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST7_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST8_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST1_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST2_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST3_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_113	PBIST4_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_114	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_114	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_119	MCRC64_0_INT_MCRC_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_120	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_24
WKUP_R5FSS0_CORE0_INTR_IN_121	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_25
WKUP_R5FSS0_CORE0_INTR_IN_122	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_26
WKUP_R5FSS0_CORE0_INTR_IN_123	EPWM0_EPWM_ETINT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_124	EPWM0_EPWM_TRIPZINT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_125	EPWM1_EPWM_ETINT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_126	EPWM1_EPWM_TRIPZINT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_127	EPWM2_EPWM_ETINT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_128	MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_128	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_128	PADCFG_CTRL0_ACCESS_ERR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_128	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_128	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_137	MCU_DCC1_INTR_DONE_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_138	WKUP_TIMER0_INTR_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_139	WKUP_TIMER1_INTR_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_140	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_141	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_142	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0

Table 10-9. WKUP_R5FSS_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_R5FSS0_CORE0_INTR_IN_143	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_144	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_145	WKUP_PSC0_PSC_ALLINT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_146	MAIN_PSC0_PSC_ALLINT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS0_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_147	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_148	EPWM2_EPWM_TRIPZINT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_151	ADC0_GEN_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_161	MMCSD0_EMMCSDSS_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_165	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_27
WKUP_R5FSS0_CORE0_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_171	FSS0_OSPI0_LVL_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_172	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_173	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_174	FSS0_OTFA_INTR_ERR_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_175	WKUP_R5FSS0_CORE0_CTI_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_178	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_179	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_180	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_181	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_182	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_187	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_188	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_189	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0

Table 10-9. WKUP_R5FSS_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_R5FSS0_CORE0_INTR_IN_190	WKUP_I2C0_POINTRPEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_193	I2C0_POINTRPEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_194	I2C1_POINTRPEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_195	I2C2_POINTRPEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_196	I2C3_POINTRPEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_197	I2C4_POINTRPEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_198	I2C5_POINTRPEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_199	I2C6_POINTRPEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_203	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_207	MCSPI3_INTR_SPI_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_208	MCSPI4_INTR_SPI_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_210	UART0_USART_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_211	UART1_USART_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_212	UART2_USART_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_213	UART3_USART_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_214	UART4_USART_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_215	UART5_USART_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_216	UART6_USART_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_219	WKUP_UART0_USART_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_220	USB0_IRQ_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_221	USB0_IRQ_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_222	USB0_IRQ_OUT_2
WKUP_R5FSS0_CORE0_INTR_IN_223	USB0_IRQ_OUT_3
WKUP_R5FSS0_CORE0_INTR_IN_224	USB0_IRQ_OUT_4
WKUP_R5FSS0_CORE0_INTR_IN_225	USB0_IRQ_OUT_5
WKUP_R5FSS0_CORE0_INTR_IN_226	USB0_IRQ_OUT_6
WKUP_R5FSS0_CORE0_INTR_IN_227	USB0_IRQ_OUT_7
WKUP_R5FSS0_CORE0_INTR_IN_228	USB0_MISC_LEVEL_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_229	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_230	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_231	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_232	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_233	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_234	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0

Table 10-9. WKUP_R5FSS_CORE0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_R5FSS0_CORE0_INTR_IN_235	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_236	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_237	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_238	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_239	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1
WKUP_R5FSS0_CORE0_INTR_IN_240	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_241	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_242	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_0
WKUP_R5FSS0_CORE0_INTR_IN_249	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_24
WKUP_R5FSS0_CORE0_INTR_IN_250	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_25
WKUP_R5FSS0_CORE0_INTR_IN_254	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_26
WKUP_R5FSS0_CORE0_INTR_IN_255	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_27

Table 10-10. Pulsar R5 Out Interrupts

Instance	OUT Interrupt	Connected To
R5FSS0	R5FSS0_CCM_COMPARE_STAT_PULSE_INTR_OUT_0	ESM0_ESM_PLS_EVENT0_IN_230
	R5FSS0_CCM_COMPARE_STAT_PULSE_INTR_OUT_0	ESM0_ESM_PLS_EVENT1_IN_230
	R5FSS0_CCM_COMPARE_STAT_PULSE_INTR_OUT_0	ESM0_ESM_PLS_EVENT2_IN_230
R5FSS0_CORE0	R5FSS0_CORE0_CTI_OUT_0	R5FSS0_CORE0_INTR_IN_175
	R5FSS0_CORE0_CTI_OUT_0	R5FSS0_CORE1_INTR_IN_175
	R5FSS0_CORE0_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_210
	R5FSS0_CORE0_EXP_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_4
	R5FSS0_CORE0_PMU_OUT_0	R5FSS0_CORE0_INTR_IN_94
	R5FSS0_CORE0_PMU_OUT_0	R5FSS0_CORE1_INTR_IN_94
	R5FSS0_CORE0_VALFIQ_OUT_0	R5FSS0_CORE0_INTR_IN_95
	R5FSS0_CORE0_VALIRQ_OUT_0	R5FSS0_CORE0_INTR_IN_96
R5FSS0_CORE1	R5FSS0_CORE1_CTI_OUT_0	R5FSS0_CORE0_INTR_IN_176
	R5FSS0_CORE1_CTI_OUT_0	R5FSS0_CORE1_INTR_IN_176
	R5FSS0_CORE1_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_6
	R5FSS0_CORE1_EXP_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_4
	R5FSS0_CORE1_PMU_OUT_0	R5FSS0_CORE0_INTR_IN_93
	R5FSS0_CORE1_PMU_OUT_0	R5FSS0_CORE1_INTR_IN_93
	R5FSS0_CORE1_VALFIQ_OUT_0	R5FSS0_CORE1_INTR_IN_95
	R5FSS0_CORE1_VALIRQ_OUT_0	R5FSS0_CORE1_INTR_IN_96

Table 10-10. Pulsar R5 Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
R5FSS0_CORE0_ECC_AGGR	R5FSS0_CORE0_ECC_AGGR_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_208
	R5FSS0_CORE0_ECC_AGGR_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_209
R5FSS0_CORE1_ECC_AGGR	R5FSS0_CORE1_ECC_AGGR_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_219
	R5FSS0_CORE1_ECC_AGGR_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_220

Table 10-10. Pulsar R5 Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
R5FSS0_COMMON0	R5FSS0_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT0_IN_229
	R5FSS0_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT1_IN_229
	R5FSS0_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT2_IN_229
	R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0	R5FSS0_CORE0_INTR_IN_5
	R5FSS0_COMMON0_COMMRX_LEVEL_1_OUT_0	R5FSS0_CORE1_INTR_IN_5
	R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0	R5FSS0_CORE0_INTR_IN_6
	R5FSS0_COMMON0_COMMTX_LEVEL_1_OUT_0	R5FSS0_CORE1_INTR_IN_6
	R5FSS0_COMMON0_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT0_IN_231
	R5FSS0_COMMON0_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT1_IN_231
	R5FSS0_COMMON0_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT2_IN_231
	R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_211
	R5FSS0_COMMON0_ECC_DE_TO_ESM_1_OUT_0	ESM0_ESM_LVL_EVENT_IN_221
	R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_212
	R5FSS0_COMMON0_ECC_SE_TO_ESM_1_OUT_0	ESM0_ESM_LVL_EVENT_IN_222
	R5FSS0_COMMON0_SELFTEST_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT0_IN_232
	R5FSS0_COMMON0_SELFTEST_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT1_IN_232
	R5FSS0_COMMON0_SELFTEST_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT2_IN_232
	R5FSS0_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT0_IN_233
	R5FSS0_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT1_IN_233
	R5FSS0_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT2_IN_233

Table 10-10. Pulsar R5 Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
R5FSS1	R5FSS1_CCM_COMPARE_STAT_PULSE_INTR_OUT_0	ESM0_ESM_PLS_EVENT0_IN_236
	R5FSS1_CCM_COMPARE_STAT_PULSE_INTR_OUT_0	ESM0_ESM_PLS_EVENT1_IN_236
	R5FSS1_CCM_COMPARE_STAT_PULSE_INTR_OUT_0	ESM0_ESM_PLS_EVENT2_IN_236
R5FSS1_CORE0	R5FSS1_CORE0_CTI_OUT_0	R5FSS1_CORE0_INTR_IN_175
	R5FSS1_CORE0_CTI_OUT_0	R5FSS1_CORE1_INTR_IN_175
	R5FSS1_CORE0_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_126
	R5FSS1_CORE0_EXP_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_4
	R5FSS1_CORE0_PMU_OUT_0	R5FSS1_CORE0_INTR_IN_94
	R5FSS1_CORE0_PMU_OUT_0	R5FSS1_CORE1_INTR_IN_94
	R5FSS1_CORE0_VALFIQ_OUT_0	R5FSS1_CORE0_INTR_IN_95
	R5FSS1_CORE0_VALIRQ_OUT_0	R5FSS1_CORE0_INTR_IN_96
R5FSS1_CORE1	R5FSS1_CORE1_CTI_OUT_0	R5FSS1_CORE0_INTR_IN_176
	R5FSS1_CORE1_CTI_OUT_0	R5FSS1_CORE1_INTR_IN_176
	R5FSS1_CORE1_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_127
	R5FSS1_CORE1_EXP_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_4
	R5FSS1_CORE1_PMU_OUT_0	R5FSS1_CORE0_INTR_IN_93
	R5FSS1_CORE1_PMU_OUT_0	R5FSS1_CORE1_INTR_IN_93
	R5FSS1_CORE1_VALFIQ_OUT_0	R5FSS1_CORE1_INTR_IN_95
	R5FSS1_CORE1_VALIRQ_OUT_0	R5FSS1_CORE1_INTR_IN_96
R5FSS1_CORE0_ECC_AGGR	R5FSS1_CORE0_ECC_AGGR_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_42
	R5FSS1_CORE0_ECC_AGGR_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_43
R5FSS1_CORE1_ECC_AGGR	R5FSS1_CORE1_ECC_AGGR_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_44
	R5FSS1_CORE1_ECC_AGGR_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_45

Table 10-10. Pulsar R5 Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
R5FSS1_COMMON0	R5FSS1_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT0_IN_235
	R5FSS1_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT1_IN_235
	R5FSS1_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT2_IN_235
	R5FSS1_COMMON0_COMMRX_LEVEL_0_OUT_0	R5FSS1_CORE0_INTR_IN_5
	R5FSS1_COMMON0_COMMRX_LEVEL_1_OUT_0	R5FSS1_CORE1_INTR_IN_5
	R5FSS1_COMMON0_COMMTX_LEVEL_0_OUT_0	R5FSS1_CORE0_INTR_IN_6
	R5FSS1_COMMON0_COMMTX_LEVEL_1_OUT_0	R5FSS1_CORE1_INTR_IN_6
	R5FSS1_COMMON0_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT0_IN_237
	R5FSS1_COMMON0_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT1_IN_237
	R5FSS1_COMMON0_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT2_IN_237
	R5FSS1_COMMON0_ECC_DE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_46
	R5FSS1_COMMON0_ECC_DE_TO_ESM_1_OUT_0	ESM0_ESM_LVL_EVENT_IN_47
	R5FSS1_COMMON0_ECC_SE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_48
	R5FSS1_COMMON0_ECC_SE_TO_ESM_1_OUT_0	ESM0_ESM_LVL_EVENT_IN_49
	R5FSS1_COMMON0_SELFTEST_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT0_IN_238
	R5FSS1_COMMON0_SELFTEST_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT1_IN_238
	R5FSS1_COMMON0_SELFTEST_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT2_IN_238
	R5FSS1_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT0_IN_239
	R5FSS1_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT1_IN_239
	R5FSS1_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0	ESM0_ESM_PLS_EVENT2_IN_239

Table 10-11. WKUP R5 (DM R5) Out Interrupts

Instance	OUT Interrupt	Connected To
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_CTI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_175
	WKUP_R5FSS0_CORE0_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_30
	WKUP_R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_91
	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_124
	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_4
	WKUP_R5FSS0_CORE0_PMU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_58
	WKUP_R5FSS0_CORE0_VALFIQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_59
	WKUP_R5FSS0_CORE0_VALIRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_60
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_5
	WKUP_R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_6
	WKUP_R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_40
	WKUP_R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_41

10.3.3 C7 Interrupts

Table 10-12. C7x CLEC IN Interrupts

IN Interrupt	Connected To
C7X256V0_CLEC_GIC_SPI_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
C7X256V0_CLEC_GIC_SPI_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
C7X256V0_CLEC_GIC_SPI_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
C7X256V0_CLEC_GIC_SPI_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
C7X256V0_CLEC_GIC_SPI_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
C7X256V0_CLEC_GIC_SPI_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
C7X256V0_CLEC_GIC_SPI_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
C7X256V0_CLEC_GIC_SPI_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
C7X256V0_CLEC_GIC_SPI_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
C7X256V0_CLEC_GIC_SPI_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
C7X256V0_CLEC_GIC_SPI_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
C7X256V0_CLEC_GIC_SPI_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
C7X256V0_CLEC_GIC_SPI_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
C7X256V0_CLEC_GIC_SPI_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
C7X256V0_CLEC_GIC_SPI_IN_48	CPSW0_CPTS_COMP_OUT_0

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V0_CLEC_GIC_SPI_IN_50	AASRC0_INFIFO_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_51	AASRC0_INGROUP_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_52	AASRC0_OUTFIFO_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_53	AASRC0_OUTGROUP_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_54	AASRC0_ERR_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_55	AASRC1_INFIFO_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_56	AASRC1_INGROUP_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_57	AASRC1_OUTFIFO_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_58	AASRC1_OUTGROUP_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_59	AASRC1_ERR_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_60	MLB0_MLBSS_MLB_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_61	MLB0_MLBSS_MLB_AHB_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_62	MLB0_MLBSS_MLB_AHB_INT_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_64	TIMER8_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_65	TIMER9_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_66	TIMER10_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_67	TIMER11_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_68	TIMER12_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_69	TIMER13_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_70	TIMER14_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_71	TIMER15_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_96	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32
C7X256V0_CLEC_GIC_SPI_IN_97	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33
C7X256V0_CLEC_GIC_SPI_IN_98	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34
C7X256V0_CLEC_GIC_SPI_IN_99	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35
C7X256V0_CLEC_GIC_SPI_IN_100	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36
C7X256V0_CLEC_GIC_SPI_IN_101	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37
C7X256V0_CLEC_GIC_SPI_IN_102	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38
C7X256V0_CLEC_GIC_SPI_IN_103	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39
C7X256V0_CLEC_GIC_SPI_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
C7X256V0_CLEC_GIC_SPI_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
C7X256V0_CLEC_GIC_SPI_IN_112	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4
C7X256V0_CLEC_GIC_SPI_IN_113	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5
C7X256V0_CLEC_GIC_SPI_IN_128	DCC0_INTR_DONE_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_128	DCC1_INTR_DONE_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_128	DCC2_INTR_DONE_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_128	DCC3_INTR_DONE_LEVEL_OUT_0

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V0_CLEC_GIC_SPI_IN_128	DCC4_INTR_DONE_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_128	DCC5_INTR_DONE_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_128	DCC6_INTR_DONE_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_128	DCC7_INTR_DONE_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_128	DCC8_INTR_DONE_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_129	MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_129	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_129	PADCFG_CTRL0_ACCESS_ERR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_129	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_129	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_131	EFUSE0_EFC_ERROR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_132	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_133	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_134	CPSW0_EVNT_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_135	CPSW0_MDIO_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_136	CPSW0_STAT_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_145	ECAP0_ECAP_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_146	ECAP1_ECAP_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_147	ECAP2_ECAP_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_148	ECAP3_ECAP_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_149	ECAP4_ECAP_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_150	ECAP5_ECAP_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_151	ADC0_GEN_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_152	TIMER0_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_153	TIMER1_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_154	TIMER2_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_155	TIMER3_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_156	TIMER4_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_157	TIMER5_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_158	TIMER6_INTR_PEND_OUT_0

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V0_CLEC_GIC_SPI_IN_159	TIMER7_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_160	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_161	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_165	MMCSD0_EMMCSDSS_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_166	MCRC64_0_INT_MCRC_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_169	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_170	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_171	FSS0_OSPI0_LVL_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_172	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_173	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_174	FSS0_OTFA_INTR_ERR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_175	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_177	DDPA0_DDPA_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_178	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_179	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_180	ESM0_ESM_INT_CFG_LVL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_181	ESM0_ESM_INT_HI_LVL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_182	ESM0_ESM_INT_LOW_LVL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_189	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_190	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_191	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_193	I2C0_POINTRPEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_194	I2C1_POINTRPEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_195	I2C2_POINTRPEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_196	I2C3_POINTRPEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_197	WKUP_I2C0_POINTRPEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_199	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_203	MAIN_PSC0_PSC_ALLINT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_204	MCSPI0_INTR_SPI_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_205	MCSPI1_INTR_SPI_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_206	MCSPI2_INTR_SPI_OUT_0

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V0_CLEC_GIC_SPI_IN_207	MCSPI3_INTR_SPI_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_208	MCSPI4_INTR_SPI_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_210	UART0_USART_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_211	UART1_USART_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_212	UART2_USART_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_213	UART3_USART_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_214	UART4_USART_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_215	UART5_USART_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_216	UART6_USART_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_218	WKUP_UART0_USART_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_220	USB0_IRQ_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_221	USB0_IRQ_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_222	USB0_IRQ_OUT_2
C7X256V0_CLEC_GIC_SPI_IN_223	USB0_IRQ_OUT_3
C7X256V0_CLEC_GIC_SPI_IN_224	USB0_IRQ_OUT_4
C7X256V0_CLEC_GIC_SPI_IN_225	USB0_IRQ_OUT_5
C7X256V0_CLEC_GIC_SPI_IN_226	USB0_IRQ_OUT_6
C7X256V0_CLEC_GIC_SPI_IN_227	USB0_IRQ_OUT_7
C7X256V0_CLEC_GIC_SPI_IN_228	USB0_MISC_LEVEL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_229	EPWM0_EPWM_ETINT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_230	EPWM0_EPWM_TRIPZINT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_231	EPWM1_EPWM_ETINT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_233	EPWM1_EPWM_TRIPZINT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_234	EPWM2_EPWM_ETINT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_235	EPWM2_EPWM_TRIPZINT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_245	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_246	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_247	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_248	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_249	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_250	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_251	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_252	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V0_CLEC_GIC_SPI_IN_256	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_261	RL2_0_ERR_LVL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_262	RL2_2_ERR_LVL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_263	RL2_3_ERR_LVL_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_267	MCASP0_REC_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_268	MCASP0_XMIT_INTR_PEND_OUT_0

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V0_CLEC_GIC_SPI_IN_269	MCASP1_REC_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_270	MCASP1_XMIT_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_271	MCASP2_REC_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_272	MCASP2_XMIT_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_273	MCASP3_REC_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_274	MCASP3_XMIT_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_275	MCASP4_REC_INTR_PEND_OUT_0
C7X256V0_CLEC_GIC_SPI_IN_276	MCASP4_XMIT_INTR_PEND_OUT_0
C7X256V0_CLEC_SOC_EVENTS_IN_IN_4	RTI4_INTR_WWD_OUT_0
C7X256V0_CLEC_SOC_EVENTS_IN_IN_5	MAIN_CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0
C7X256V0_CLEC_SOC_EVENTS_IN_IN_6	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_2
C7X256V0_CLEC_SOC_EVENTS_IN_IN_7	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_2
C7X256V0_CLEC_SOC_EVENTS_IN_IN_8	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_2
C7X256V0_CLEC_SOC_EVENTS_IN_IN_9	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_2
C7X256V0_CLEC_SOC_EVENTS_IN_IN_10	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_1
C7X256V0_CLEC_SOC_EVENTS_IN_IN_12	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_20
C7X256V0_CLEC_SOC_EVENTS_IN_IN_13	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_21
C7X256V0_CLEC_SOC_EVENTS_IN_IN_14	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_22
C7X256V0_CLEC_SOC_EVENTS_IN_IN_15	C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_23
C7X256V0_CLEC_SOC_EVENTS_IN_IN_16	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_84
C7X256V0_CLEC_SOC_EVENTS_IN_IN_17	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_85
C7X256V0_CLEC_SOC_EVENTS_IN_IN_18	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_86
C7X256V0_CLEC_SOC_EVENTS_IN_IN_19	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_87
C7X256V0_CLEC_SOC_EVENTS_IN_IN_20	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88
C7X256V0_CLEC_SOC_EVENTS_IN_IN_21	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89
C7X256V0_CLEC_SOC_EVENTS_IN_IN_22	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90
C7X256V0_CLEC_SOC_EVENTS_IN_IN_23	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91
C7X256V0_CLEC_SOC_EVENTS_IN_IN_24	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92
C7X256V0_CLEC_SOC_EVENTS_IN_IN_25	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93
C7X256V0_CLEC_SOC_EVENTS_IN_IN_26	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94
C7X256V0_CLEC_SOC_EVENTS_IN_IN_27	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95
C7X256V0_CLEC_SOC_EVENTS_IN_IN_28	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96
C7X256V0_CLEC_SOC_EVENTS_IN_IN_29	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97
C7X256V0_CLEC_SOC_EVENTS_IN_IN_30	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98
C7X256V0_CLEC_SOC_EVENTS_IN_IN_31	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V1_CLEC_GIC_SPI_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
C7X256V1_CLEC_GIC_SPI_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
C7X256V1_CLEC_GIC_SPI_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
C7X256V1_CLEC_GIC_SPI_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
C7X256V1_CLEC_GIC_SPI_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
C7X256V1_CLEC_GIC_SPI_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
C7X256V1_CLEC_GIC_SPI_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
C7X256V1_CLEC_GIC_SPI_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
C7X256V1_CLEC_GIC_SPI_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
C7X256V1_CLEC_GIC_SPI_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
C7X256V1_CLEC_GIC_SPI_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
C7X256V1_CLEC_GIC_SPI_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
C7X256V1_CLEC_GIC_SPI_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
C7X256V1_CLEC_GIC_SPI_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
C7X256V1_CLEC_GIC_SPI_IN_48	CPSW0_CPTS_COMP_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_50	AASRC0_INFIFO_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_51	AASRC0_INGROUP_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_52	AASRC0_OUTFIFO_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_53	AASRC0_OUTGROUP_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_54	AASRC0_ERR_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_55	AASRC1_INFIFO_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_56	AASRC1_INGROUP_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_57	AASRC1_OUTFIFO_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_58	AASRC1_OUTGROUP_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_59	AASRC1_ERR_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_60	MLB0_MLBSS_MLB_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_61	MLB0_MLBSS_MLB_AHB_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_62	MLB0_MLBSS_MLB_AHB_INT_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_64	TIMER8_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_65	TIMER9_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_66	TIMER10_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_67	TIMER11_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_68	TIMER12_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_69	TIMER13_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_70	TIMER14_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_71	TIMER15_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_96	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V1_CLEC_GIC_SPI_IN_97	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33
C7X256V1_CLEC_GIC_SPI_IN_98	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34
C7X256V1_CLEC_GIC_SPI_IN_99	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35
C7X256V1_CLEC_GIC_SPI_IN_100	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36
C7X256V1_CLEC_GIC_SPI_IN_101	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37
C7X256V1_CLEC_GIC_SPI_IN_102	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38
C7X256V1_CLEC_GIC_SPI_IN_103	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39
C7X256V1_CLEC_GIC_SPI_IN_104	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_105	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_106	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
C7X256V1_CLEC_GIC_SPI_IN_107	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
C7X256V1_CLEC_GIC_SPI_IN_112	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4
C7X256V1_CLEC_GIC_SPI_IN_113	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5
C7X256V1_CLEC_GIC_SPI_IN_128	DCC0_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_128	DCC1_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_128	DCC2_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_128	DCC3_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_128	DCC4_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_128	DCC5_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_128	DCC6_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_128	DCC7_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_128	DCC8_INTR_DONE_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_129	MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_129	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_129	PADCFG_CTRL0_ACCESS_ERR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_129	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_129	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_131	EFUSE0_EFC_ERROR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_132	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_133	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V1_CLEC_GIC_SPI_IN_134	CPSW0_EVNT_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_135	CPSW0_MDIO_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_136	CPSW0_STAT_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_145	ECAP0_ECAP_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_146	ECAP1_ECAP_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_147	ECAP2_ECAP_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_148	ECAP3_ECAP_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_149	ECAP4_ECAP_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_150	ECAP5_ECAP_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_151	ADC0_GEN_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_152	TIMER0_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_153	TIMER1_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_154	TIMER2_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_155	TIMER3_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_156	TIMER4_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_157	TIMER5_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_158	TIMER6_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_159	TIMER7_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_160	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_161	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_165	MMCSD0_EMMCSDSS_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_166	MCRC64_0_INT_MCRC_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_169	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_170	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_171	FSS0_OSPI0_LVL_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_172	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_173	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_174	FSS0_OTFA_INTR_ERR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_175	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_177	DDPA0_DDPA_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_178	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_179	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_180	ESM0_ESM_INT_CFG_LVL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_181	ESM0_ESM_INT_HI_LVL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_182	ESM0_ESM_INT_LOW_LVL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V1_CLEC_GIC_SPI_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_189	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_190	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_191	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_193	I2C0_POINTRPEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_194	I2C1_POINTRPEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_195	I2C2_POINTRPEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_196	I2C3_POINTRPEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_197	WKUP_I2C0_POINTRPEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_199	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_203	MAIN_PSC0_PSC_ALLINT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_204	MCSPI0_INTR_SPI_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_205	MCSPI1_INTR_SPI_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_206	MCSPI2_INTR_SPI_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_207	MCSPI3_INTR_SPI_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_208	MCSPI4_INTR_SPI_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_210	UART0_USART_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_211	UART1_USART_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_212	UART2_USART_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_213	UART3_USART_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_214	UART4_USART_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_215	UART5_USART_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_216	UART6_USART_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_218	WKUP_UART0_USART_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_220	USB0_IRQ_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_221	USB0_IRQ_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_222	USB0_IRQ_OUT_2
C7X256V1_CLEC_GIC_SPI_IN_223	USB0_IRQ_OUT_3
C7X256V1_CLEC_GIC_SPI_IN_224	USB0_IRQ_OUT_4
C7X256V1_CLEC_GIC_SPI_IN_225	USB0_IRQ_OUT_5
C7X256V1_CLEC_GIC_SPI_IN_226	USB0_IRQ_OUT_6
C7X256V1_CLEC_GIC_SPI_IN_227	USB0_IRQ_OUT_7
C7X256V1_CLEC_GIC_SPI_IN_228	USB0_MISC_LEVEL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_229	EPWM0_EPWM_ETINT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_230	EPWM0_EPWM_TRIPZINT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_231	EPWM1_EPWM_ETINT_OUT_0

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V1_CLEC_GIC_SPI_IN_233	EPWM1_EPWM_TRIPZINT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_234	EPWM2_EPWM_ETINT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_235	EPWM2_EPWM_TRIPZINT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_245	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_246	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_247	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_248	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_249	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_250	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_251	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_252	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1
C7X256V1_CLEC_GIC_SPI_IN_256	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_261	RL2_0_ERR_LVL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_262	RL2_2_ERR_LVL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_263	RL2_3_ERR_LVL_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_267	MCASP0_REC_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_268	MCASP0_XMIT_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_269	MCASP1_REC_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_270	MCASP1_XMIT_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_271	MCASP2_REC_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_272	MCASP2_XMIT_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_273	MCASP3_REC_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_274	MCASP3_XMIT_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_275	MCASP4_REC_INTR_PEND_OUT_0
C7X256V1_CLEC_GIC_SPI_IN_276	MCASP4_XMIT_INTR_PEND_OUT_0
C7X256V1_CLEC_SOC_EVENTS_IN_IN_4	RTI5_INTR_WWD_OUT_0
C7X256V1_CLEC_SOC_EVENTS_IN_IN_5	MAIN_CTRL_MMR0_IPC_SET1_IPC_SET_IPCFG_OUT_0
C7X256V1_CLEC_SOC_EVENTS_IN_IN_6	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_3
C7X256V1_CLEC_SOC_EVENTS_IN_IN_7	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_3
C7X256V1_CLEC_SOC_EVENTS_IN_IN_8	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_3
C7X256V1_CLEC_SOC_EVENTS_IN_IN_9	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_3
C7X256V1_CLEC_SOC_EVENTS_IN_IN_10	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_2
C7X256V1_CLEC_SOC_EVENTS_IN_IN_12	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_20
C7X256V1_CLEC_SOC_EVENTS_IN_IN_13	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_21
C7X256V1_CLEC_SOC_EVENTS_IN_IN_14	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_22

Table 10-12. C7x CLEC IN Interrupts (continued)

IN Interrupt	Connected To
C7X256V1_CLEC_SOC_EVENTS_IN_IN_15	C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_23
C7X256V1_CLEC_SOC_EVENTS_IN_IN_16	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_100
C7X256V1_CLEC_SOC_EVENTS_IN_IN_17	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_101
C7X256V1_CLEC_SOC_EVENTS_IN_IN_18	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_102
C7X256V1_CLEC_SOC_EVENTS_IN_IN_19	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_103
C7X256V1_CLEC_SOC_EVENTS_IN_IN_20	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_104
C7X256V1_CLEC_SOC_EVENTS_IN_IN_21	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_105
C7X256V1_CLEC_SOC_EVENTS_IN_IN_22	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_106
C7X256V1_CLEC_SOC_EVENTS_IN_IN_23	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_107
C7X256V1_CLEC_SOC_EVENTS_IN_IN_24	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_108
C7X256V1_CLEC_SOC_EVENTS_IN_IN_25	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_109
C7X256V1_CLEC_SOC_EVENTS_IN_IN_26	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_110
C7X256V1_CLEC_SOC_EVENTS_IN_IN_27	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_111
C7X256V1_CLEC_SOC_EVENTS_IN_IN_28	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_112
C7X256V1_CLEC_SOC_EVENTS_IN_IN_29	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_113
C7X256V1_CLEC_SOC_EVENTS_IN_IN_30	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_114
C7X256V1_CLEC_SOC_EVENTS_IN_IN_31	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_115

Table 10-13. C7x CLEC OUT Interrupts

OUT Interrupt	Connected To
C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_226
C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_226
C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_226
C7X256V0_CLEC_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_149
C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_160
C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_1	ESM0_ESM_LVL_EVENT_IN_161
C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_2	ESM0_ESM_LVL_EVENT_IN_162
C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_3	ESM0_ESM_LVL_EVENT_IN_163
C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_4	ESM0_ESM_LVL_EVENT_IN_164
C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_5	ESM0_ESM_LVL_EVENT_IN_165
C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_6	ESM0_ESM_LVL_EVENT_IN_166
C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_7	ESM0_ESM_LVL_EVENT_IN_167
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_248
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_248

Table 10-13. C7x CLEC OUT Interrupts (continued)

OUT Interrupt	Connected To
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1	R5FSS0_CORE0_INTR_IN_249
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1	R5FSS0_CORE1_INTR_IN_249
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2	R5FSS0_CORE0_INTR_IN_250
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2	R5FSS0_CORE1_INTR_IN_250
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3	R5FSS0_CORE0_INTR_IN_251
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3	R5FSS0_CORE1_INTR_IN_251
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4	R5FSS0_CORE0_INTR_IN_252
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4	R5FSS0_CORE1_INTR_IN_252
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5	R5FSS0_CORE0_INTR_IN_253
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5	R5FSS0_CORE1_INTR_IN_253
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6	R5FSS0_CORE0_INTR_IN_254
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6	R5FSS0_CORE1_INTR_IN_254
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7	R5FSS0_CORE0_INTR_IN_255
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7	R5FSS0_CORE1_INTR_IN_255
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8	R5FSS1_CORE0_INTR_IN_248
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8	R5FSS1_CORE1_INTR_IN_248
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9	R5FSS1_CORE0_INTR_IN_249
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9	R5FSS1_CORE1_INTR_IN_249
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10	R5FSS1_CORE0_INTR_IN_250
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10	R5FSS1_CORE1_INTR_IN_250
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11	R5FSS1_CORE0_INTR_IN_251
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11	R5FSS1_CORE1_INTR_IN_251
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12	R5FSS1_CORE0_INTR_IN_252
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12	R5FSS1_CORE1_INTR_IN_252
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13	R5FSS1_CORE0_INTR_IN_253
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13	R5FSS1_CORE1_INTR_IN_253
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14	R5FSS1_CORE0_INTR_IN_254
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14	R5FSS1_CORE1_INTR_IN_254
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15	R5FSS1_CORE0_INTR_IN_255
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15	R5FSS1_CORE1_INTR_IN_255
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_20	C7X256V1_CLEC_SOC_EVENTS_IN_IN_12
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_21	C7X256V1_CLEC_SOC_EVENTS_IN_IN_13
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_22	C7X256V1_CLEC_SOC_EVENTS_IN_IN_14
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_23	C7X256V1_CLEC_SOC_EVENTS_IN_IN_15
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_24	WKUP_R5FSS0_CORE0_INTR_IN_249
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_25	WKUP_R5FSS0_CORE0_INTR_IN_250
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_26	WKUP_R5FSS0_CORE0_INTR_IN_254
C7X256V0_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_27	WKUP_R5FSS0_CORE0_INTR_IN_255
C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113

Table 10-13. C7x CLEC OUT Interrupts (continued)

OUT Interrupt	Connected To
C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_245
C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_245
C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_245
C7X256V1_CLEC_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_64
C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_192
C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_1	ESM0_ESM_LVL_EVENT_IN_193
C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_2	ESM0_ESM_LVL_EVENT_IN_194
C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_3	ESM0_ESM_LVL_EVENT_IN_195
C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_4	ESM0_ESM_LVL_EVENT_IN_196
C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_5	ESM0_ESM_LVL_EVENT_IN_197
C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_6	ESM0_ESM_LVL_EVENT_IN_198
C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_7	ESM0_ESM_LVL_EVENT_IN_199
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_256
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_256
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1	R5FSS0_CORE0_INTR_IN_257
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_1	R5FSS0_CORE1_INTR_IN_257
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2	R5FSS0_CORE0_INTR_IN_258
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_2	R5FSS0_CORE1_INTR_IN_258
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3	R5FSS0_CORE0_INTR_IN_259
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_3	R5FSS0_CORE1_INTR_IN_259
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4	R5FSS0_CORE0_INTR_IN_260
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_4	R5FSS0_CORE1_INTR_IN_260
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5	R5FSS0_CORE0_INTR_IN_261
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_5	R5FSS0_CORE1_INTR_IN_261
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6	R5FSS0_CORE0_INTR_IN_262
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_6	R5FSS0_CORE1_INTR_IN_262
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7	R5FSS0_CORE0_INTR_IN_263
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_7	R5FSS0_CORE1_INTR_IN_263
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8	R5FSS1_CORE0_INTR_IN_256
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_8	R5FSS1_CORE1_INTR_IN_256
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9	R5FSS1_CORE0_INTR_IN_257
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_9	R5FSS1_CORE1_INTR_IN_257
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10	R5FSS1_CORE0_INTR_IN_258
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_10	R5FSS1_CORE1_INTR_IN_258
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11	R5FSS1_CORE0_INTR_IN_259

Table 10-13. C7x CLEC OUT Interrupts (continued)

OUT Interrupt	Connected To
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_11	R5FSS1_CORE1_INTR_IN_259
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12	R5FSS1_CORE0_INTR_IN_260
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_12	R5FSS1_CORE1_INTR_IN_260
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13	R5FSS1_CORE0_INTR_IN_261
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_13	R5FSS1_CORE1_INTR_IN_261
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14	R5FSS1_CORE0_INTR_IN_262
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_14	R5FSS1_CORE1_INTR_IN_262
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15	R5FSS1_CORE0_INTR_IN_263
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_15	R5FSS1_CORE1_INTR_IN_263
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_20	C7X256V0_CLEC_SOC_EVENTS_IN_IN_12
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_21	C7X256V0_CLEC_SOC_EVENTS_IN_IN_13
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_22	C7X256V0_CLEC_SOC_EVENTS_IN_IN_14
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_23	C7X256V0_CLEC_SOC_EVENTS_IN_IN_15
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_24	WKUP_R5FSS0_CORE0_INTR_IN_120
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_25	WKUP_R5FSS0_CORE0_INTR_IN_121
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_26	WKUP_R5FSS0_CORE0_INTR_IN_122
C7X256V1_CLEC_SOC_EVENTS_OUT_LEVEL_OUT_27	WKUP_R5FSS0_CORE0_INTR_IN_165

10.3.4 Device IN Interrupts

Table 10-14. MAIN_GPIOMUX_INTROUTER0 IN Interrupts

IN Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_IN_IN_0	GPIO0_GPIO_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_1	GPIO0_GPIO_OUT_1
MAIN_GPIOMUX_INTROUTER0_IN_IN_2	GPIO0_GPIO_OUT_2
MAIN_GPIOMUX_INTROUTER0_IN_IN_3	GPIO0_GPIO_OUT_3
MAIN_GPIOMUX_INTROUTER0_IN_IN_4	GPIO0_GPIO_OUT_4
MAIN_GPIOMUX_INTROUTER0_IN_IN_5	GPIO0_GPIO_OUT_5
MAIN_GPIOMUX_INTROUTER0_IN_IN_6	GPIO0_GPIO_OUT_6
MAIN_GPIOMUX_INTROUTER0_IN_IN_7	GPIO0_GPIO_OUT_7
MAIN_GPIOMUX_INTROUTER0_IN_IN_8	GPIO0_GPIO_OUT_8
MAIN_GPIOMUX_INTROUTER0_IN_IN_9	GPIO0_GPIO_OUT_9
MAIN_GPIOMUX_INTROUTER0_IN_IN_10	GPIO0_GPIO_OUT_10
MAIN_GPIOMUX_INTROUTER0_IN_IN_11	GPIO0_GPIO_OUT_11
MAIN_GPIOMUX_INTROUTER0_IN_IN_12	GPIO0_GPIO_OUT_12
MAIN_GPIOMUX_INTROUTER0_IN_IN_13	GPIO0_GPIO_OUT_13
MAIN_GPIOMUX_INTROUTER0_IN_IN_14	GPIO0_GPIO_OUT_14
MAIN_GPIOMUX_INTROUTER0_IN_IN_15	GPIO0_GPIO_OUT_15
MAIN_GPIOMUX_INTROUTER0_IN_IN_16	GPIO0_GPIO_OUT_16
MAIN_GPIOMUX_INTROUTER0_IN_IN_17	GPIO0_GPIO_OUT_17
MAIN_GPIOMUX_INTROUTER0_IN_IN_18	GPIO0_GPIO_OUT_18

Table 10-14. MAIN_GPIOMUX_INTROUTER0 IN Interrupts (continued)

IN Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_IN_IN_19	GPIO0_GPIO_OUT_19

Table 10-14. MAIN_GPIOMUX_INTROUTER0 IN Interrupts (continued)

IN Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_IN_IN_20	GPIO0_GPIO_OUT_20
MAIN_GPIOMUX_INTROUTER0_IN_IN_21	GPIO0_GPIO_OUT_21
MAIN_GPIOMUX_INTROUTER0_IN_IN_22	GPIO0_GPIO_OUT_22
MAIN_GPIOMUX_INTROUTER0_IN_IN_23	GPIO0_GPIO_OUT_23
MAIN_GPIOMUX_INTROUTER0_IN_IN_24	GPIO0_GPIO_OUT_24
MAIN_GPIOMUX_INTROUTER0_IN_IN_25	GPIO0_GPIO_OUT_25
MAIN_GPIOMUX_INTROUTER0_IN_IN_26	GPIO0_GPIO_OUT_26
MAIN_GPIOMUX_INTROUTER0_IN_IN_27	GPIO0_GPIO_OUT_27
MAIN_GPIOMUX_INTROUTER0_IN_IN_28	GPIO0_GPIO_OUT_28
MAIN_GPIOMUX_INTROUTER0_IN_IN_29	GPIO0_GPIO_OUT_29
MAIN_GPIOMUX_INTROUTER0_IN_IN_30	GPIO0_GPIO_OUT_30
MAIN_GPIOMUX_INTROUTER0_IN_IN_31	GPIO0_GPIO_OUT_31
MAIN_GPIOMUX_INTROUTER0_IN_IN_32	GPIO0_GPIO_OUT_32
MAIN_GPIOMUX_INTROUTER0_IN_IN_33	GPIO0_GPIO_OUT_33
MAIN_GPIOMUX_INTROUTER0_IN_IN_34	GPIO0_GPIO_OUT_34
MAIN_GPIOMUX_INTROUTER0_IN_IN_35	GPIO0_GPIO_OUT_35
MAIN_GPIOMUX_INTROUTER0_IN_IN_36	GPIO0_GPIO_OUT_36
MAIN_GPIOMUX_INTROUTER0_IN_IN_37	GPIO0_GPIO_OUT_37
MAIN_GPIOMUX_INTROUTER0_IN_IN_38	GPIO0_GPIO_OUT_38
MAIN_GPIOMUX_INTROUTER0_IN_IN_39	GPIO0_GPIO_OUT_39
MAIN_GPIOMUX_INTROUTER0_IN_IN_40	GPIO0_GPIO_OUT_40
MAIN_GPIOMUX_INTROUTER0_IN_IN_41	GPIO0_GPIO_OUT_41
MAIN_GPIOMUX_INTROUTER0_IN_IN_42	GPIO0_GPIO_OUT_42
MAIN_GPIOMUX_INTROUTER0_IN_IN_43	GPIO0_GPIO_OUT_43
MAIN_GPIOMUX_INTROUTER0_IN_IN_44	GPIO0_GPIO_OUT_44
MAIN_GPIOMUX_INTROUTER0_IN_IN_45	GPIO0_GPIO_OUT_45
MAIN_GPIOMUX_INTROUTER0_IN_IN_46	GPIO0_GPIO_OUT_46
MAIN_GPIOMUX_INTROUTER0_IN_IN_47	GPIO0_GPIO_OUT_47
MAIN_GPIOMUX_INTROUTER0_IN_IN_48	GPIO0_GPIO_OUT_48
MAIN_GPIOMUX_INTROUTER0_IN_IN_49	GPIO0_GPIO_OUT_49
MAIN_GPIOMUX_INTROUTER0_IN_IN_50	GPIO0_GPIO_OUT_50
MAIN_GPIOMUX_INTROUTER0_IN_IN_51	GPIO0_GPIO_OUT_51
MAIN_GPIOMUX_INTROUTER0_IN_IN_52	GPIO0_GPIO_OUT_52
MAIN_GPIOMUX_INTROUTER0_IN_IN_55	GPIO0_GPIO_OUT_55

Table 10-14. MAIN_GPIOMUX_INTROUTER0 IN Interrupts (continued)

IN Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_IN_IN_56	GPIO0_GPIO_OUT_56
MAIN_GPIOMUX_INTROUTER0_IN_IN_57	GPIO0_GPIO_OUT_57
MAIN_GPIOMUX_INTROUTER0_IN_IN_58	GPIO0_GPIO_OUT_58
MAIN_GPIOMUX_INTROUTER0_IN_IN_59	GPIO0_GPIO_OUT_59
MAIN_GPIOMUX_INTROUTER0_IN_IN_62	GPIO0_GPIO_OUT_62
MAIN_GPIOMUX_INTROUTER0_IN_IN_63	GPIO0_GPIO_OUT_63
MAIN_GPIOMUX_INTROUTER0_IN_IN_64	GPIO0_GPIO_OUT_64
MAIN_GPIOMUX_INTROUTER0_IN_IN_65	GPIO0_GPIO_OUT_65
MAIN_GPIOMUX_INTROUTER0_IN_IN_66	GPIO0_GPIO_OUT_66
MAIN_GPIOMUX_INTROUTER0_IN_IN_67	GPIO0_GPIO_OUT_67
MAIN_GPIOMUX_INTROUTER0_IN_IN_68	GPIO0_GPIO_OUT_68
MAIN_GPIOMUX_INTROUTER0_IN_IN_69	GPIO0_GPIO_OUT_69
MAIN_GPIOMUX_INTROUTER0_IN_IN_70	GPIO0_GPIO_OUT_70
MAIN_GPIOMUX_INTROUTER0_IN_IN_71	GPIO0_GPIO_OUT_71
MAIN_GPIOMUX_INTROUTER0_IN_IN_72	GPIO0_GPIO_OUT_72
MAIN_GPIOMUX_INTROUTER0_IN_IN_73	GPIO0_GPIO_OUT_73
MAIN_GPIOMUX_INTROUTER0_IN_IN_74	GPIO0_GPIO_OUT_74
MAIN_GPIOMUX_INTROUTER0_IN_IN_75	GPIO0_GPIO_OUT_75
MAIN_GPIOMUX_INTROUTER0_IN_IN_76	GPIO0_GPIO_OUT_76
MAIN_GPIOMUX_INTROUTER0_IN_IN_77	GPIO0_GPIO_OUT_77
MAIN_GPIOMUX_INTROUTER0_IN_IN_78	GPIO0_GPIO_OUT_78
MAIN_GPIOMUX_INTROUTER0_IN_IN_79	GPIO0_GPIO_OUT_79
MAIN_GPIOMUX_INTROUTER0_IN_IN_80	GPIO0_GPIO_OUT_80
MAIN_GPIOMUX_INTROUTER0_IN_IN_81	GPIO0_GPIO_OUT_81
MAIN_GPIOMUX_INTROUTER0_IN_IN_82	GPIO0_GPIO_OUT_82
MAIN_GPIOMUX_INTROUTER0_IN_IN_83	GPIO0_GPIO_OUT_83
MAIN_GPIOMUX_INTROUTER0_IN_IN_84	GPIO0_GPIO_OUT_84
MAIN_GPIOMUX_INTROUTER0_IN_IN_85	GPIO0_GPIO_OUT_85
MAIN_GPIOMUX_INTROUTER0_IN_IN_86	GPIO0_GPIO_OUT_86
MAIN_GPIOMUX_INTROUTER0_IN_IN_87	GPIO0_GPIO_OUT_87
MAIN_GPIOMUX_INTROUTER0_IN_IN_88	GPIO0_GPIO_OUT_88
MAIN_GPIOMUX_INTROUTER0_IN_IN_89	GPIO0_GPIO_OUT_89
MAIN_GPIOMUX_INTROUTER0_IN_IN_90	GPIO0_GPIO_OUT_90
MAIN_GPIOMUX_INTROUTER0_IN_IN_91	GPIO0_GPIO_OUT_91

Table 10-14. MAIN_GPIOMUX_INTROUTER0 IN Interrupts (continued)

IN Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_IN_IN_92	GPIO0_GPIO_OUT_92
MAIN_GPIOMUX_INTROUTER0_IN_IN_96	GPIO1_GPIO_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_97	GPIO1_GPIO_OUT_1
MAIN_GPIOMUX_INTROUTER0_IN_IN_98	GPIO1_GPIO_OUT_2
MAIN_GPIOMUX_INTROUTER0_IN_IN_99	GPIO1_GPIO_OUT_3
MAIN_GPIOMUX_INTROUTER0_IN_IN_100	GPIO1_GPIO_OUT_4
MAIN_GPIOMUX_INTROUTER0_IN_IN_101	GPIO1_GPIO_OUT_5
MAIN_GPIOMUX_INTROUTER0_IN_IN_102	GPIO1_GPIO_OUT_6
MAIN_GPIOMUX_INTROUTER0_IN_IN_103	GPIO1_GPIO_OUT_7
MAIN_GPIOMUX_INTROUTER0_IN_IN_104	GPIO1_GPIO_OUT_8
MAIN_GPIOMUX_INTROUTER0_IN_IN_105	GPIO1_GPIO_OUT_9
MAIN_GPIOMUX_INTROUTER0_IN_IN_106	GPIO1_GPIO_OUT_10
MAIN_GPIOMUX_INTROUTER0_IN_IN_107	GPIO1_GPIO_OUT_11
MAIN_GPIOMUX_INTROUTER0_IN_IN_108	GPIO1_GPIO_OUT_12
MAIN_GPIOMUX_INTROUTER0_IN_IN_109	GPIO1_GPIO_OUT_13
MAIN_GPIOMUX_INTROUTER0_IN_IN_110	GPIO1_GPIO_OUT_14
MAIN_GPIOMUX_INTROUTER0_IN_IN_111	GPIO1_GPIO_OUT_15
MAIN_GPIOMUX_INTROUTER0_IN_IN_112	GPIO1_GPIO_OUT_16
MAIN_GPIOMUX_INTROUTER0_IN_IN_113	GPIO1_GPIO_OUT_17
MAIN_GPIOMUX_INTROUTER0_IN_IN_114	GPIO1_GPIO_OUT_18
MAIN_GPIOMUX_INTROUTER0_IN_IN_115	GPIO1_GPIO_OUT_19
MAIN_GPIOMUX_INTROUTER0_IN_IN_116	GPIO1_GPIO_OUT_20
MAIN_GPIOMUX_INTROUTER0_IN_IN_117	GPIO1_GPIO_OUT_21
MAIN_GPIOMUX_INTROUTER0_IN_IN_118	GPIO1_GPIO_OUT_22
MAIN_GPIOMUX_INTROUTER0_IN_IN_119	GPIO1_GPIO_OUT_23
MAIN_GPIOMUX_INTROUTER0_IN_IN_120	GPIO1_GPIO_OUT_24
MAIN_GPIOMUX_INTROUTER0_IN_IN_121	GPIO1_GPIO_OUT_25
MAIN_GPIOMUX_INTROUTER0_IN_IN_122	GPIO1_GPIO_OUT_26
MAIN_GPIOMUX_INTROUTER0_IN_IN_123	GPIO1_GPIO_OUT_27
MAIN_GPIOMUX_INTROUTER0_IN_IN_124	GPIO1_GPIO_OUT_28
MAIN_GPIOMUX_INTROUTER0_IN_IN_125	GPIO1_GPIO_OUT_29
MAIN_GPIOMUX_INTROUTER0_IN_IN_126	GPIO1_GPIO_OUT_30
MAIN_GPIOMUX_INTROUTER0_IN_IN_127	GPIO1_GPIO_OUT_31
MAIN_GPIOMUX_INTROUTER0_IN_IN_128	GPIO1_GPIO_OUT_32

Table 10-14. MAIN_GPIOMUX_INTROUTER0 IN Interrupts (continued)

IN Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_IN_IN_129	GPIO1_GPIO_OUT_33
MAIN_GPIOMUX_INTROUTER0_IN_IN_130	GPIO1_GPIO_OUT_34
MAIN_GPIOMUX_INTROUTER0_IN_IN_131	GPIO1_GPIO_OUT_35
MAIN_GPIOMUX_INTROUTER0_IN_IN_132	GPIO1_GPIO_OUT_36
MAIN_GPIOMUX_INTROUTER0_IN_IN_133	GPIO1_GPIO_OUT_37
MAIN_GPIOMUX_INTROUTER0_IN_IN_134	GPIO1_GPIO_OUT_38
MAIN_GPIOMUX_INTROUTER0_IN_IN_135	GPIO1_GPIO_OUT_39
MAIN_GPIOMUX_INTROUTER0_IN_IN_136	GPIO1_GPIO_OUT_40
MAIN_GPIOMUX_INTROUTER0_IN_IN_137	GPIO1_GPIO_OUT_41
MAIN_GPIOMUX_INTROUTER0_IN_IN_138	GPIO1_GPIO_OUT_42
MAIN_GPIOMUX_INTROUTER0_IN_IN_139	GPIO1_GPIO_OUT_43
MAIN_GPIOMUX_INTROUTER0_IN_IN_140	GPIO1_GPIO_OUT_44
MAIN_GPIOMUX_INTROUTER0_IN_IN_141	GPIO1_GPIO_OUT_45
MAIN_GPIOMUX_INTROUTER0_IN_IN_142	GPIO1_GPIO_OUT_46
MAIN_GPIOMUX_INTROUTER0_IN_IN_143	GPIO1_GPIO_OUT_47
MAIN_GPIOMUX_INTROUTER0_IN_IN_144	GPIO1_GPIO_OUT_48
MAIN_GPIOMUX_INTROUTER0_IN_IN_145	GPIO1_GPIO_OUT_49
MAIN_GPIOMUX_INTROUTER0_IN_IN_146	GPIO1_GPIO_OUT_50
MAIN_GPIOMUX_INTROUTER0_IN_IN_168	GPIO1_GPIO_OUT_72
MAIN_GPIOMUX_INTROUTER0_IN_IN_170	GPIO1_GPIO_OUT_74
MAIN_GPIOMUX_INTROUTER0_IN_IN_171	GPIO1_GPIO_OUT_75
MAIN_GPIOMUX_INTROUTER0_IN_IN_172	GPIO1_GPIO_OUT_76
MAIN_GPIOMUX_INTROUTER0_IN_IN_173	GPIO1_GPIO_OUT_77
MAIN_GPIOMUX_INTROUTER0_IN_IN_174	GPIO1_GPIO_OUT_78
MAIN_GPIOMUX_INTROUTER0_IN_IN_175	GPIO1_GPIO_OUT_79
MAIN_GPIOMUX_INTROUTER0_IN_IN_176	GPIO1_GPIO_OUT_80
MAIN_GPIOMUX_INTROUTER0_IN_IN_177	GPIO1_GPIO_OUT_81
MAIN_GPIOMUX_INTROUTER0_IN_IN_178	GPIO1_GPIO_OUT_82
MAIN_GPIOMUX_INTROUTER0_IN_IN_179	GPIO1_GPIO_OUT_83
MAIN_GPIOMUX_INTROUTER0_IN_IN_180	GPIO1_GPIO_OUT_84
MAIN_GPIOMUX_INTROUTER0_IN_IN_181	GPIO1_GPIO_OUT_85
MAIN_GPIOMUX_INTROUTER0_IN_IN_192	GPIO0_GPIO_BANK_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_193	GPIO0_GPIO_BANK_OUT_1
MAIN_GPIOMUX_INTROUTER0_IN_IN_194	GPIO0_GPIO_BANK_OUT_2

Table 10-14. MAIN_GPIOMUX_INTROUTER0 IN Interrupts (continued)

IN Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_IN_IN_195	GPIO0_GPIO_BANK_OUT_3
MAIN_GPIOMUX_INTROUTER0_IN_IN_196	GPIO0_GPIO_BANK_OUT_4
MAIN_GPIOMUX_INTROUTER0_IN_IN_197	GPIO0_GPIO_BANK_OUT_5
MAIN_GPIOMUX_INTROUTER0_IN_IN_200	GPIO1_GPIO_BANK_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_201	GPIO1_GPIO_BANK_OUT_1
MAIN_GPIOMUX_INTROUTER0_IN_IN_202	GPIO1_GPIO_BANK_OUT_2
MAIN_GPIOMUX_INTROUTER0_IN_IN_203	GPIO1_GPIO_BANK_OUT_3
MAIN_GPIOMUX_INTROUTER0_IN_IN_204	GPIO1_GPIO_BANK_OUT_4
MAIN_GPIOMUX_INTROUTER0_IN_IN_205	GPIO1_GPIO_BANK_OUT_5
MAIN_GPIOMUX_INTROUTER0_IN_IN_214	WKUP_TIMER0_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_215	WKUP_TIMER1_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_216	TIMER0_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_217	TIMER1_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_218	TIMER2_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_219	TIMER3_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_220	TIMER4_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_221	TIMER5_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_222	TIMER6_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_223	TIMER7_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_224	TIMER8_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_225	TIMER9_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_226	TIMER10_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_227	TIMER11_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_228	TIMER12_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_229	TIMER13_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_230	TIMER14_TIMER_PWM_OUT_0
MAIN_GPIOMUX_INTROUTER0_IN_IN_231	TIMER15_TIMER_PWM_OUT_0

Table 10-15. MCU_MCU_GPIOMUX_INTROUTER0 IN Interrupts

IN Interrupt	Connected To
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_0	MCU_GPIO0_GPIO_OUT_0
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_1	MCU_GPIO0_GPIO_OUT_1
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_2	MCU_GPIO0_GPIO_OUT_2
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_3	MCU_GPIO0_GPIO_OUT_3
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_4	MCU_GPIO0_GPIO_OUT_4
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_5	MCU_GPIO0_GPIO_OUT_5
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_6	MCU_GPIO0_GPIO_OUT_6

Table 10-15. MCU_MCU_GPIOMUX_INTROUTER0 IN Interrupts (continued)

IN Interrupt	Connected To
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_7	MCU_GPIO0_GPIO_OUT_7
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_8	MCU_GPIO0_GPIO_OUT_8
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_9	MCU_GPIO0_GPIO_OUT_9
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_10	MCU_GPIO0_GPIO_OUT_10
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_11	MCU_GPIO0_GPIO_OUT_11
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_12	MCU_GPIO0_GPIO_OUT_12
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_13	MCU_GPIO0_GPIO_OUT_13
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_14	MCU_GPIO0_GPIO_OUT_14
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_15	MCU_GPIO0_GPIO_OUT_15
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_16	MCU_GPIO0_GPIO_OUT_16
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_19	MCU_GPIO0_GPIO_OUT_19
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_20	MCU_GPIO0_GPIO_OUT_20
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_21	MCU_GPIO0_GPIO_OUT_21
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_22	MCU_GPIO0_GPIO_OUT_22
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_23	MCU_GPIO0_GPIO_OUT_23
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_24	MCU_GPIO0_GPIO_OUT_24
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_25	MCU_GPIO0_GPIO_OUT_25
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_30	MCU_GPIO0_GPIO_BANK_OUT_0
MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_31	MCU_GPIO0_GPIO_BANK_OUT_1

Table 10-16. DMASS0_INTAGGR_0 IN Interrupts

IN Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_0	CPSW0_CPTS_COMP_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_1	MCASP0_XMIT_DMA_EVENT_REQ_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_2	MCASP1_XMIT_DMA_EVENT_REQ_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_3	MCASP2_XMIT_DMA_EVENT_REQ_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_4	MCASP3_XMIT_DMA_EVENT_REQ_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_5	MCASP4_XMIT_DMA_EVENT_REQ_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_7	MCRC64_0_INT_MCRC_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_16	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_48
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_17	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_49
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_18	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_50
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_19	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_51
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_20	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_52
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_21	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_53
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_22	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_54
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_23	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_55
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_24	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_56
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_25	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_57
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_27	DEBUGSS0_DAVDMA_LEVEL_OUT_0
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_28	MCRC64_0_DMA_EVENT_OUT_0

Table 10-16. DMASS0_INTAGGR_0 IN Interrupts (continued)

IN Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_29	MCRC64_0_DMA_EVENT_OUT_1
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_30	MCRC64_0_DMA_EVENT_OUT_2
DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_31	MCRC64_0_DMA_EVENT_OUT_3

Table 10-17. WKUP_ESM0 IN Interrupts

IN Interrupt	Connected To
WKUP_ESM0_ESM_LVL_EVENT_IN_0	ESM0_ESM_INT_CFG_LVL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_1	ESM0_ESM_INT_HI_LVL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_2	ESM0_ESM_INT_LOW_LVL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_3	WKUP_CBASS0_DEFAULT_EXP_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_8	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_9	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_10	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_11	WKUP_VTM0_CORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_12	WKUP_VTM0_UNCORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_20	WKUP_ECC_AGGR2_CORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_21	WKUP_ECC_AGGR2_UNCORR_LEVEL_OUT_0

Table 10-17. WKUP_ESM0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_ESM0_ESM_LVL_EVENT_IN_23	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_24	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_25	EFUSE0_EFC_ERROR_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_36	MCU_DCC1_INTR_ERR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_37	MCU_DCC0_INTR_ERR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_38	WKUP_ECC_AGGR1_CORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_39	WKUP_ECC_AGGR1_UNCORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_42	WKUP_PSRAMECC_8K0_ECC_CORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_43	WKUP_PSRAMECC_8K0_ECC_UNCORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_44	WKUP_PSRAM2KX32E0_ECC_CORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_45	WKUP_PSRAM2KX32E0_ECC_UNCORR_LEVEL_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_54	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_55	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_56	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_57	PLLFRACF2_SSMOD_16FFT4_LOCKLOSS_IPCFG_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_58	PLLFRACF2_SSMOD_16FFT14_LOCKLOSS_IPCFG_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_59	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_61	PLLFRACF2_SSMOD_16FFT7_LOCKLOSS_IPCFG_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_63	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT0_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
WKUP_ESM0_ESM_PLS_EVENT0_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
WKUP_ESM0_ESM_PLS_EVENT0_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
WKUP_ESM0_ESM_PLS_EVENT0_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT0_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
WKUP_ESM0_ESM_PLS_EVENT0_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
WKUP_ESM0_ESM_PLS_EVENT0_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
WKUP_ESM0_ESM_PLS_EVENT0_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT0_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2

Table 10-17. WKUP_ESM0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_ESM0_ESM_PLS_EVENT0_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
WKUP_ESM0_ESM_PLS_EVENT0_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4

Table 10-17. WKUP_ESM0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_ESM0_ESM_PLS_EVENT0_IN_86	WKUP_RTI0_INTR_WWD_OUT_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_88	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
WKUP_ESM0_ESM_PLS_EVENT0_IN_89	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
WKUP_ESM0_ESM_PLS_EVENT0_IN_90	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
WKUP_ESM0_ESM_PLS_EVENT0_IN_91	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
WKUP_ESM0_ESM_PLS_EVENT1_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT1_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT1_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
WKUP_ESM0_ESM_PLS_EVENT1_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
WKUP_ESM0_ESM_PLS_EVENT1_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
WKUP_ESM0_ESM_PLS_EVENT1_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT1_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT1_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
WKUP_ESM0_ESM_PLS_EVENT1_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
WKUP_ESM0_ESM_PLS_EVENT1_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
WKUP_ESM0_ESM_PLS_EVENT1_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT1_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT1_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
WKUP_ESM0_ESM_PLS_EVENT1_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
WKUP_ESM0_ESM_PLS_EVENT1_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
WKUP_ESM0_ESM_PLS_EVENT1_IN_86	WKUP_RTI0_INTR_WWD_OUT_0
WKUP_ESM0_ESM_PLS_EVENT1_IN_88	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
WKUP_ESM0_ESM_PLS_EVENT1_IN_89	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
WKUP_ESM0_ESM_PLS_EVENT1_IN_90	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
WKUP_ESM0_ESM_PLS_EVENT1_IN_91	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
WKUP_ESM0_ESM_PLS_EVENT2_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT2_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT2_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
WKUP_ESM0_ESM_PLS_EVENT2_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3

Table 10-17. WKUP_ESM0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_ESM0_ESM_PLS_EVENT2_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
WKUP_ESM0_ESM_PLS_EVENT2_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT2_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT2_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
WKUP_ESM0_ESM_PLS_EVENT2_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3

Table 10-17. WKUP_ESM0 IN Interrupts (continued)

IN Interrupt	Connected To
WKUP_ESM0_ESM_PLS_EVENT2_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
WKUP_ESM0_ESM_PLS_EVENT2_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
WKUP_ESM0_ESM_PLS_EVENT2_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
WKUP_ESM0_ESM_PLS_EVENT2_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
WKUP_ESM0_ESM_PLS_EVENT2_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
WKUP_ESM0_ESM_PLS_EVENT2_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
WKUP_ESM0_ESM_PLS_EVENT2_IN_86	WKUP_RTI0_INTR_WWD_OUT_0
WKUP_ESM0_ESM_PLS_EVENT2_IN_88	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
WKUP_ESM0_ESM_PLS_EVENT2_IN_89	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
WKUP_ESM0_ESM_PLS_EVENT2_IN_90	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
WKUP_ESM0_ESM_PLS_EVENT2_IN_91	MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11

Table 10-18. ESM IN Interrupts

IN Interrupt	Connected To
ESM0_ESM_LVL_EVENT_IN_0	WKUP_CBASS0_DEFAULT_EXP_OUT_0
ESM0_ESM_LVL_EVENT_IN_1	ECC_AGGR1_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_2	ECC_AGGR1_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_3	CPSW0_ECC_SEC_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_5	CBASS_MISC_PERI0_DEFAULT_EXP_OUT_0
ESM0_ESM_LVL_EVENT_IN_6	R5FSS0_CORE1_EXP_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_8	WKUP_PSRAMECC_8K0_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_9	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_10	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_11	FSS0_OSPI0_ECC_CORR_LVL_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_12	FSS1_OSPI_ECC_AGGR_0_OSPI_ECC_CORR_LVL_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_13	WKUP_PSRAMECC_8K0_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_15	PDMA0_ECC_SEC_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_16	WKUP_PSRAM2KX32E0_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_17	WKUP_PSRAM2KX32E0_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_18	PLLFRACF2_SSMOD_16FFT7_LOCKLOSS_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_20	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_21	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_24	ECC_AGGR2_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_25	ECC_AGGR2_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_26	ECC_AGGR3_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_27	ECC_AGGR3_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_28	PDMA1_ECC_SEC_PEND_OUT_0

Table 10-18. ESM IN Interrupts (continued)

IN Interrupt	Connected To
ESM0_ESM_LVL_EVENT_IN_29	PSRAMECC0_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_30	WKUP_R5FSS0_CORE0_ECC_CORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_32	USB0_HOST_SYSTEM_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_33	ADC0_ECC_CORRECTED_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_34	ADC0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_35	USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_37	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_38	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_39	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_40	WKUP_R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0
ESM0_ESM_LVL_EVENT_IN_41	WKUP_R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0
ESM0_ESM_LVL_EVENT_IN_42	R5FSS1_CORE0_ECC_AGGR_ECC_CORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_43	R5FSS1_CORE0_ECC_AGGR_ECC_UNCORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_44	R5FSS1_CORE1_ECC_AGGR_ECC_CORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_45	R5FSS1_CORE1_ECC_AGGR_ECC_UNCORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_46	R5FSS1_COMMON0_ECC_DE_TO_ESM_0_OUT_0
ESM0_ESM_LVL_EVENT_IN_47	R5FSS1_COMMON0_ECC_DE_TO_ESM_1_OUT_0
ESM0_ESM_LVL_EVENT_IN_48	R5FSS1_COMMON0_ECC_SE_TO_ESM_0_OUT_0
ESM0_ESM_LVL_EVENT_IN_49	R5FSS1_COMMON0_ECC_SE_TO_ESM_1_OUT_0
ESM0_ESM_LVL_EVENT_IN_54	MMCSD0_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_55	MMCSD0_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_56	MMCSD0_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_57	MMCSD0_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_58	MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_59	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_60	MCAN1_MCANSS_ECC_CORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_61	MCAN1_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_62	MCAN2_MCANSS_ECC_CORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_63	MCAN2_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_64	C7X256V1_CLEC_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_65	PDMA4_ECC_SEC_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_66	PDMA4_ECC_DED_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_67	CPSW0_ECC_DED_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_68	MCAN3_MCANSS_ECC_CORR_LVL_INT_OUT_0

Table 10-18. ESM IN Interrupts (continued)

IN Interrupt	Connected To
ESM0_ESM_LVL_EVENT_IN_69	MCAN3_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_70	MCAN4_MCANSS_ECC_CORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_71	MCAN4_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
ESM0_ESM_LVL_EVENT_IN_73	DCC7_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_74	FSS0_OSPI0_ECC_UNCORR_LVL_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_75	FSS1_OSPI_ECC_AGGR_0_OSPI_ECC_UNCORR_LVL_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_76	CBASS_INFRA1_DEFAULT_EXP_OUT_0
ESM0_ESM_LVL_EVENT_IN_77	MLB0_MLBSS_ECC_CORR_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_78	MLB0_MLBSS_ECC_UNCORR_LVL_OUT_0
ESM0_ESM_LVL_EVENT_IN_79	DCC6_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_80	CBASS_CENTRAL2_DEFAULT_EXP_OUT_0
ESM0_ESM_LVL_EVENT_IN_86	CBASS0_DEFAULT_EXP_OUT_0
ESM0_ESM_LVL_EVENT_IN_88	PDMA0_ECC_DED_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_89	PDMA1_ECC_DED_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_90	PSRAMECC0_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_91	WKUP_R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_93	CBASS_MEM0_DEFAULT_EXP_OUT_0
ESM0_ESM_LVL_EVENT_IN_98	DFTSS0_DFT_SAFETY_123_OUT_0
ESM0_ESM_LVL_EVENT_IN_99	DFTSS0_DFT_SAFETY_MULTI_OUT_0
ESM0_ESM_LVL_EVENT_IN_100	DFTSS0_DFT_SAFETY_ONE_OUT_0
ESM0_ESM_LVL_EVENT_IN_101	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_102	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_104	WKUP_ECC_AGGR1_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_105	WKUP_ECC_AGGR1_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_110	AM275_MAIN_IPCSS_CBASS0_DEFAULT_EXP_OUT_0
ESM0_ESM_LVL_EVENT_IN_111	USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_112	DCC0_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_113	DCC1_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_114	DCC2_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_115	DCC3_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_116	DCC4_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_117	DCC5_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_118	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_DED_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_119	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_SEC_PEND_OUT_0

Table 10-18. ESM IN Interrupts (continued)

IN Interrupt	Connected To
ESM0_ESM_LVL_EVENT_IN_120	SA3_SS0_SA_UL_0_SA_UL_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_121	SA3_SS0_SA_UL_0_SA_UL_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_124	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_126	R5FSS1_CORE0_EXP_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_127	R5FSS1_CORE1_EXP_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_128	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_129	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_130	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_131	PLLFRACF2_SSMOD_16FFT4_LOCKLOSS_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_132	PLLFRACF2_SSMOD_16FFT14_LOCKLOSS_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_133	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_134	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
ESM0_ESM_LVL_EVENT_IN_136	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_137	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_138	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_139	WKUP_VTM0_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_140	WKUP_VTM0_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_141	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_142	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_143	FSS1_HYPERBUS_ECC_AGGR_0_HPB_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_144	FSS1_HYPERBUS_ECC_AGGR_0_HPB_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_145	FSS0_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_146	FSS0_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_147	FSS1_MISC_0_ECC_INTR_ERR_PEND_OUT_0
ESM0_ESM_LVL_EVENT_IN_149	C7X256V0_CLEC_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_157	PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_158	WKUP_PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_159	WKUP_PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_160	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_161	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_1
ESM0_ESM_LVL_EVENT_IN_162	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_2
ESM0_ESM_LVL_EVENT_IN_163	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_3
ESM0_ESM_LVL_EVENT_IN_164	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_4
ESM0_ESM_LVL_EVENT_IN_165	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_5

Table 10-18. ESM IN Interrupts (continued)

IN Interrupt	Connected To
ESM0_ESM_LVL_EVENT_IN_166	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_6
ESM0_ESM_LVL_EVENT_IN_167	C7X256V0_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_7
ESM0_ESM_LVL_EVENT_IN_168	IDOM0_MAIN_PLL_ECC_AGGR4_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_169	IDOM0_MAIN_PLL_ECC_AGGR4_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_170	IDOM0_MAIN_PLL_ECC_AGGR6_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_171	IDOM0_MAIN_PLL_ECC_AGGR6_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_172	IDOM0_PULSAR_PLL_ECC_AGGR8_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_173	IDOM0_PULSAR_PLL_ECC_AGGR8_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_174	IDOM0_PULSAR_PLL_ECC_AGGR10_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_175	IDOM0_PULSAR_PLL_ECC_AGGR10_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_176	IDOM1_MAIN_PLL_ECC_AGGR5_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_177	IDOM1_MAIN_PLL_ECC_AGGR5_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_178	IDOM1_MAIN_PLL_ECC_AGGR7_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_179	IDOM1_MAIN_PLL_ECC_AGGR7_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_180	IDOM1_PULSAR_PLL_ECC_AGGR9_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_181	IDOM1_PULSAR_PLL_ECC_AGGR9_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_182	IDOM1_PULSAR_PLL_ECC_AGGR11_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_183	IDOM1_PULSAR_PLL_ECC_AGGR11_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_184	MSRAM_1MB0_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_185	MSRAM_1MB0_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_186	MSRAM_1MB1_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_187	MSRAM_1MB1_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_188	MSRAM_1MB2_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_189	MSRAM_1MB2_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_190	MSRAM_1MB3_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_191	MSRAM_1MB3_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_192	C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_193	C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_1
ESM0_ESM_LVL_EVENT_IN_194	C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_2
ESM0_ESM_LVL_EVENT_IN_195	C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_3
ESM0_ESM_LVL_EVENT_IN_196	C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_4
ESM0_ESM_LVL_EVENT_IN_197	C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_5
ESM0_ESM_LVL_EVENT_IN_198	C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_6
ESM0_ESM_LVL_EVENT_IN_199	C7X256V1_CLEC_ESM_EVENTS_OUT_LEVEL_OUT_7

Table 10-18. ESM IN Interrupts (continued)

IN Interrupt	Connected To
ESM0_ESM_LVL_EVENT_IN_202	PBIST3_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_203	PBIST4_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_204	PBIST5_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_205	PBIST6_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_206	PBIST7_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_207	PBIST8_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_208	R5FSS0_CORE0_ECC_AGGR_ECC_CORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_209	R5FSS0_CORE0_ECC_AGGR_ECC_UNCORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_210	R5FSS0_CORE0_EXP_INTR_OUT_0
ESM0_ESM_LVL_EVENT_IN_211	R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0
ESM0_ESM_LVL_EVENT_IN_212	R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0
ESM0_ESM_LVL_EVENT_IN_213	PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_214	PBIST2_DFT_PBIST_SAFETY_ERROR_OUT_0
ESM0_ESM_LVL_EVENT_IN_215	MSRAM_1MB4_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_216	MSRAM_1MB4_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_217	MSRAM_1MB5_ECC_CORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_218	MSRAM_1MB5_ECC_UNCORR_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_219	R5FSS0_CORE1_ECC_AGGR_ECC_CORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_220	R5FSS0_CORE1_ECC_AGGR_ECC_UNCORRECTED_LEVEL_OUT_0
ESM0_ESM_LVL_EVENT_IN_221	R5FSS0_COMMON0_ECC_DE_TO_ESM_1_OUT_0
ESM0_ESM_LVL_EVENT_IN_222	R5FSS0_COMMON0_ECC_SE_TO_ESM_1_OUT_0
ESM0_ESM_LVL_EVENT_IN_223	DCC8_INTR_ERR_LEVEL_OUT_0
ESM0_ESM_PLS_EVENT0_IN_224	RTI0_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT0_IN_225	RTI1_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT0_IN_226	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_227	WKUP_RTI0_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT0_IN_228	PBIST0_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_229	R5FSS0_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT0_IN_230	R5FSS0_CCM_COMPARE_STAT_PULSE_INTR_OUT_0
ESM0_ESM_PLS_EVENT0_IN_231	R5FSS0_COMMON0_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT0_IN_232	R5FSS0_COMMON0_SELFTEST_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT0_IN_233	R5FSS0_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT0_IN_234	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_235	R5FSS1_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0

Table 10-18. ESM IN Interrupts (continued)

IN Interrupt	Connected To
ESM0_ESM_PLS_EVENT0_IN_236	R5FSS1_CCM_COMPARE_STAT_PULSE_INTR_OUT_0
ESM0_ESM_PLS_EVENT0_IN_237	R5FSS1_COMMON0_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT0_IN_238	R5FSS1_COMMON0_SELFTEST_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT0_IN_239	R5FSS1_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT0_IN_240	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_241	RTI2_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT0_IN_242	RTI3_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT0_IN_243	PBIST1_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_244	PBIST2_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_245	C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_246	PBIST3_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_247	PBIST4_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_248	PBIST5_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_249	PBIST6_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_250	PBIST7_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_251	PBIST8_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT0_IN_252	RTI4_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT0_IN_253	RTI5_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT1_IN_224	RTI0_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT1_IN_225	RTI1_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT1_IN_226	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_227	WKUP_RTI0_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT1_IN_228	PBIST0_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_229	R5FSS0_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT1_IN_230	R5FSS0_CCM_COMPARE_STAT_PULSE_INTR_OUT_0
ESM0_ESM_PLS_EVENT1_IN_231	R5FSS0_COMMON0_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT1_IN_232	R5FSS0_COMMON0_SELFTEST_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT1_IN_233	R5FSS0_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT1_IN_234	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_235	R5FSS1_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT1_IN_236	R5FSS1_CCM_COMPARE_STAT_PULSE_INTR_OUT_0
ESM0_ESM_PLS_EVENT1_IN_237	R5FSS1_COMMON0_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT1_IN_238	R5FSS1_COMMON0_SELFTEST_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT1_IN_239	R5FSS1_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0

Table 10-18. ESM IN Interrupts (continued)

IN Interrupt	Connected To
ESM0_ESM_PLS_EVENT1_IN_240	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_241	RTI2_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT1_IN_242	RTI3_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT1_IN_243	PBIST1_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_244	PBIST2_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_245	C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_246	PBIST3_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_247	PBIST4_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_248	PBIST5_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_249	PBIST6_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_250	PBIST7_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_251	PBIST8_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT1_IN_252	RTI4_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT1_IN_253	RTI5_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT2_IN_224	RTI0_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT2_IN_225	RTI1_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT2_IN_226	C7X256V0_CLEC_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_227	WKUP_RTI0_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT2_IN_228	PBIST0_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_229	R5FSS0_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT2_IN_230	R5FSS0_CCM_COMPARE_STAT_PULSE_INTR_OUT_0
ESM0_ESM_PLS_EVENT2_IN_231	R5FSS0_COMMON0_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT2_IN_232	R5FSS0_COMMON0_SELFTEST_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT2_IN_233	R5FSS0_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT2_IN_234	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_235	R5FSS1_COMMON0_BUS_MONITOR_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT2_IN_236	R5FSS1_CCM_COMPARE_STAT_PULSE_INTR_OUT_0
ESM0_ESM_PLS_EVENT2_IN_237	R5FSS1_COMMON0_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT2_IN_238	R5FSS1_COMMON0_SELFTEST_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT2_IN_239	R5FSS1_COMMON0_VIM_COMPARE_ERR_PULSE_OUT_0
ESM0_ESM_PLS_EVENT2_IN_240	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_241	RTI2_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT2_IN_242	RTI3_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT2_IN_243	PBIST1_DFT_PBIST_CPU_OUT_0

Table 10-18. ESM IN Interrupts (continued)

IN Interrupt	Connected To
ESM0_ESM_PLS_EVENT2_IN_244	PBIST2_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_245	C7X256V1_CLEC_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_246	PBIST3_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_247	PBIST4_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_248	PBIST5_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_249	PBIST6_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_250	PBIST7_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_251	PBIST8_DFT_PBIST_CPU_OUT_0
ESM0_ESM_PLS_EVENT2_IN_252	RTI4_INTR_WWD_OUT_0
ESM0_ESM_PLS_EVENT2_IN_253	RTI5_INTR_WWD_OUT_0

Table 10-19. EPWM IN Interrupts

Instance	IN Interrupt	Connected To
EPWM1	EPWM1_EPWM_SYNCIN_IN_0	EPWM0_EPWM_SYNCOUT_OUT_0
EPWM2	EPWM2_EPWM_SYNCIN_IN_0	EPWM1_EPWM_SYNCOUT_OUT_0

Table 10-20. USB0 IN Interrupts

IN Interrupt	Connected To
USB0_TRACE_INEP_PKT_BUFF_AVAIL_IN_0	DEBUGSS0_DAVDMA_LEVEL_OUT_0

10.3.5 Device OUT Interrupts

Table 10-21. Idom0_main Out Interrupts

Instance	OUT Interrupt	Connected To
Idom0_main_pll_ecc_aggr4	IDOM0_MAIN_PLL_ECC_AGGR4_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_168
	IDOM0_MAIN_PLL_ECC_AGGR4_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_169
Idom0_main_pll_ecc_aggr6	IDOM0_MAIN_PLL_ECC_AGGR6_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_170
	IDOM0_MAIN_PLL_ECC_AGGR6_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_171
Idom0_pulsar_pll_ecc_aggr8	IDOM0_PULSAR_PLL_ECC_AGGR8_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_172
	IDOM0_PULSAR_PLL_ECC_AGGR8_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_173
Idom0_pulsar_pll_ecc_aggr10	IDOM0_PULSAR_PLL_ECC_AGGR10_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_174
	IDOM0_PULSAR_PLL_ECC_AGGR10_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_175
Idom1_main_pll_ecc_aggr5	IDOM1_MAIN_PLL_ECC_AGGR5_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_176
	IDOM1_MAIN_PLL_ECC_AGGR5_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_177

Table 10-21. Idom0_main Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
Idom1_main_pll_ecc_aggr7	IDOM1_MAIN_PLL_ECC_AGGR7_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_178
	IDOM1_MAIN_PLL_ECC_AGGR7_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_179
Idom1_pulsar_pll_ecc_aggr9	IDOM1_PULSAR_PLL_ECC_AGGR9_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_180
	IDOM1_PULSAR_PLL_ECC_AGGR9_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_181
Idom1_pulsar_pll_ecc_aggr11	IDOM1_PULSAR_PLL_ECC_AGGR11_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_182
	IDOM1_PULSAR_PLL_ECC_AGGR11_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_183

Table 10-22. ADC Out Interrupts

OUT Interrupt	Connected To
ADC0_ECC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_33
ADC0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_34
ADC0_FIFO0_PULSE_OUT_0	PDMA5_ADC12_0_RX_IN_0
ADC0_FIFO1_PULSE_OUT_0	PDMA5_ADC12_0_RX_IN_1
ADC0_GEN_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_151
ADC0_GEN_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_151
ADC0_GEN_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_151
ADC0_GEN_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_151
ADC0_GEN_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_151

Table 10-22. ADC Out Interrupts (continued)

OUT Interrupt	Connected To
ADC0_GEN_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_151
ADC0_GEN_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_151

Table 10-23. DFTSS Out Interrupts

OUT Interrupt	Connected To
DFTSS0_DFT_SAFETY_123_OUT_0	ESM0_ESM_LVL_EVENT_IN_98
DFTSS0_DFT_SAFETY_MULTI_OUT_0	ESM0_ESM_LVL_EVENT_IN_99
DFTSS0_DFT_SAFETY_ONE_OUT_0	ESM0_ESM_LVL_EVENT_IN_100

Table 10-24. ECC AGG Out Interrupts

Instance	OUT Interrupt	Connected To
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_23
	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_20
	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_24
	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_21
WKUP_ECC_AGGR1	WKUP_ECC_AGGR1_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_38
	WKUP_ECC_AGGR1_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_104
	WKUP_ECC_AGGR1_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_39
	WKUP_ECC_AGGR1_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_105
ECC_AGGR2	ECC_AGGR2_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_24
	ECC_AGGR2_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_25
ECC_AGGR3	ECC_AGGR3_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_26
	ECC_AGGR3_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_27
ECC_AGGR1	ECC_AGGR1_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_2
	ECC_AGGR1_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_1
WKUP_ECC_AGGR2	WKUP_ECC_AGGR2_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_20
	WKUP_ECC_AGGR2_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_21
DMASS0_ECC_AGGR_0	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_9
	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_10

Table 10-25. Cbass Out Interrupts

Instance	OUT Interrupt	Connected To
am275_main_IPCSS_cbass0	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	AM275_MAIN_IPCSS_CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	AM275_MAIN_IPCSS_CBASS0_DEFAULT_EXP_OUT_0	ESM0_ESM_LVL_EVENT_IN_110
CBASS_MCASP0	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
CBASS_CENTRAL2	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147

Table 10-25. Cbass Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
CBASS_CENTRAL2	CBASS_CENTRAL2_DEFAULT_EXP_OUT_0	ESM0_ESM_LVL_EVENT_IN_80
CBASS_INFRA1	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_INFRA1_DEFAULT_EXP_OUT_0	ESM0_ESM_LVL_EVENT_IN_76
CBASS_MEM0	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	CBASS_MEM0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_MEM0_DEFAULT_EXP_OUT_0	ESM0_ESM_LVL_EVENT_IN_93

Table 10-25. Cbass Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
CBASS_MISC_PERI0	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS_MISC_PERI0_DEFAULT_EXP_OUT_0	ESM0_ESM_LVL_EVENT_IN_5
CBASS0	CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	CBASS0_DEFAULT_EXP_OUT_0	ESM0_ESM_LVL_EVENT_IN_86
CBASS_DBG0	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147

Table 10-25. Cbass Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
WKUP_CBASS0	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	WKUP_CBASS0_DEFAULT_EXP_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_3
	WKUP_CBASS0_DEFAULT_EXP_OUT_0	ESM0_ESM_LVL_EVENT_IN_0
WKUP_CBASS_SAFE1	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_31
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_31
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_31
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_31
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_133
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_133
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_147
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_147
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_147
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_147
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147

Table 10-26. MAIN_CTRL_MMR0 Out Interrupts

OUT Interrupt	Connected To
MAIN_CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0	C7X256V0_CLEC_SOC_EVENTS_IN_IN_5
MAIN_CTRL_MMR0_IPC_SET16_IPC_SET_IPCFG_OUT_0	R5FSS0_CORE0_INTR_IN_0
MAIN_CTRL_MMR0_IPC_SET17_IPC_SET_IPCFG_OUT_0	R5FSS0_CORE1_INTR_IN_0
MAIN_CTRL_MMR0_IPC_SET18_IPC_SET_IPCFG_OUT_0	R5FSS1_CORE0_INTR_IN_0

Table 10-26. MAIN_CTRL_MMR0 Out Interrupts (continued)

OUT Interrupt	Connected To
MAIN_CTRL_MMR0_IPC_SET19_IPC_SET_IPCFG_OUT_0	R5FSS1_CORE1_INTR_IN_0
MAIN_CTRL_MMR0_IPC_SET1_IPC_SET_IPCFG_OUT_0	C7X256V1_CLEC_SOC_EVENTS_IN_IN_5
MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_129
MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_129
MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_128
MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_128
MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_128
MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_128
MAIN_CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128

Table 10-27. MAIN_GPIOMUX_INTROUTER0 Out Interrupts

OUT Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_32
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_32
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_32
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_33
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_33
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_33
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_34
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	C7X256V1_CLEC_GIC_SPI_IN_34
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_34
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_35
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	C7X256V1_CLEC_GIC_SPI_IN_35
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_35
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_36
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	C7X256V1_CLEC_GIC_SPI_IN_36
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_36
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_37
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	C7X256V1_CLEC_GIC_SPI_IN_37
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_37
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	C7X256V0_CLEC_GIC_SPI_IN_38
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	C7X256V1_CLEC_GIC_SPI_IN_38
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_38
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	C7X256V0_CLEC_GIC_SPI_IN_39
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	C7X256V1_CLEC_GIC_SPI_IN_39
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_39
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	C7X256V0_CLEC_GIC_SPI_IN_40
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	C7X256V1_CLEC_GIC_SPI_IN_40
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_R5FSS0_CORE0_INTR_IN_40
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	C7X256V0_CLEC_GIC_SPI_IN_41
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	C7X256V1_CLEC_GIC_SPI_IN_41

Table 10-27. MAIN_GPIOMUX_INTROUTER0 Out Interrupts (continued)

OUT Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_R5FSS0_CORE0_INTR_IN_41
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	C7X256V0_CLEC_GIC_SPI_IN_42
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	C7X256V1_CLEC_GIC_SPI_IN_42
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_R5FSS0_CORE0_INTR_IN_42
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	C7X256V0_CLEC_GIC_SPI_IN_43
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	C7X256V1_CLEC_GIC_SPI_IN_43
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_R5FSS0_CORE0_INTR_IN_43
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	C7X256V0_CLEC_GIC_SPI_IN_44
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	C7X256V1_CLEC_GIC_SPI_IN_44
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	WKUP_R5FSS0_CORE0_INTR_IN_44
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	C7X256V0_CLEC_GIC_SPI_IN_45
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	C7X256V1_CLEC_GIC_SPI_IN_45
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	WKUP_R5FSS0_CORE0_INTR_IN_45
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	C7X256V0_CLEC_GIC_SPI_IN_46
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	C7X256V1_CLEC_GIC_SPI_IN_46
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	WKUP_R5FSS0_CORE0_INTR_IN_46
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	C7X256V0_CLEC_GIC_SPI_IN_47
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	C7X256V1_CLEC_GIC_SPI_IN_47
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	WKUP_R5FSS0_CORE0_INTR_IN_47
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_16	R5FSS0_CORE0_INTR_IN_32
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_16	R5FSS0_CORE1_INTR_IN_32
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_17	R5FSS0_CORE0_INTR_IN_33

Table 10-27. MAIN_GPIOMUX_INTROUTER0 Out Interrupts (continued)

OUT Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_17	R5FSS0_CORE1_INTR_IN_33
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18	R5FSS0_CORE0_INTR_IN_34
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18	R5FSS0_CORE1_INTR_IN_34
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19	R5FSS0_CORE0_INTR_IN_35
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19	R5FSS0_CORE1_INTR_IN_35
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20	R5FSS0_CORE0_INTR_IN_36
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20	R5FSS0_CORE1_INTR_IN_36
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21	R5FSS0_CORE0_INTR_IN_37
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21	R5FSS0_CORE1_INTR_IN_37
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22	R5FSS0_CORE0_INTR_IN_38
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22	R5FSS0_CORE1_INTR_IN_38
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23	R5FSS0_CORE0_INTR_IN_39
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23	R5FSS0_CORE1_INTR_IN_39
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24	R5FSS0_CORE0_INTR_IN_40
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24	R5FSS0_CORE1_INTR_IN_40
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25	R5FSS0_CORE0_INTR_IN_41
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25	R5FSS0_CORE1_INTR_IN_41
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26	R5FSS0_CORE0_INTR_IN_42
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26	R5FSS0_CORE1_INTR_IN_42
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27	R5FSS0_CORE0_INTR_IN_43
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27	R5FSS0_CORE1_INTR_IN_43
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28	R5FSS0_CORE0_INTR_IN_44
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28	R5FSS0_CORE1_INTR_IN_44
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29	R5FSS0_CORE0_INTR_IN_45
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29	R5FSS0_CORE1_INTR_IN_45
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30	R5FSS0_CORE0_INTR_IN_46
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30	R5FSS0_CORE1_INTR_IN_46
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31	R5FSS0_CORE0_INTR_IN_47
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31	R5FSS0_CORE1_INTR_IN_47
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_32	R5FSS1_CORE0_INTR_IN_32
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_32	R5FSS1_CORE1_INTR_IN_32
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_33	R5FSS1_CORE0_INTR_IN_33
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_33	R5FSS1_CORE1_INTR_IN_33
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34	R5FSS1_CORE0_INTR_IN_34

Table 10-27. MAIN_GPIOMUX_INTROUTER0 Out Interrupts (continued)

OUT Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34	R5FSS1_CORE1_INTR_IN_34
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35	R5FSS1_CORE0_INTR_IN_35
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35	R5FSS1_CORE1_INTR_IN_35
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_36	R5FSS1_CORE0_INTR_IN_36
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_36	R5FSS1_CORE1_INTR_IN_36
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_37	R5FSS1_CORE0_INTR_IN_37
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_37	R5FSS1_CORE1_INTR_IN_37
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_38	R5FSS1_CORE0_INTR_IN_38
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_38	R5FSS1_CORE1_INTR_IN_38
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_39	R5FSS1_CORE0_INTR_IN_39
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_39	R5FSS1_CORE1_INTR_IN_39
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_40	R5FSS1_CORE0_INTR_IN_40
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_40	R5FSS1_CORE1_INTR_IN_40
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_41	R5FSS1_CORE0_INTR_IN_41
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_41	R5FSS1_CORE1_INTR_IN_41
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_42	R5FSS1_CORE0_INTR_IN_42
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_42	R5FSS1_CORE1_INTR_IN_42
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_43	R5FSS1_CORE0_INTR_IN_43
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_43	R5FSS1_CORE1_INTR_IN_43
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_44	R5FSS1_CORE0_INTR_IN_44
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_44	R5FSS1_CORE1_INTR_IN_44
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_45	R5FSS1_CORE0_INTR_IN_45
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_45	R5FSS1_CORE1_INTR_IN_45
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_46	R5FSS1_CORE0_INTR_IN_46
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_46	R5FSS1_CORE1_INTR_IN_46
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_47	R5FSS1_CORE0_INTR_IN_47
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_47	R5FSS1_CORE1_INTR_IN_47
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_48	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_16
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_49	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_17
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_50	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_18
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_51	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_19
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_52	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_20
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_53	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_21
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_54	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_22

Table 10-27. MAIN_GPIOMUX_INTROUTER0 Out Interrupts (continued)

OUT Interrupt	Connected To
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_55	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_23
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_56	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_24
MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_57	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_25

Table 10-28. PADCFG Out Interrupts

Instance	OUT Interrupt	Connected To
PADCFG_CTRL0	PADCFG_CTRL0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_129
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_129
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_128
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_128

Table 10-28. PADCFG Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_128
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_128
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
MCU_PADCFG_CTRL0	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_129
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_129
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_128
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_128
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_128
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_128

Table 10-28. PADCFG Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128

Table 10-29. MAIN_PSC Out Interrupts

OUT Interrupt	Connected To
MAIN_PSC0_PSC_ALLINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_203
MAIN_PSC0_PSC_ALLINT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_203
MAIN_PSC0_PSC_ALLINT_OUT_0	R5FSS0_CORE0_INTR_IN_146
MAIN_PSC0_PSC_ALLINT_OUT_0	R5FSS0_CORE1_INTR_IN_146
MAIN_PSC0_PSC_ALLINT_OUT_0	R5FSS1_CORE0_INTR_IN_146
MAIN_PSC0_PSC_ALLINT_OUT_0	R5FSS1_CORE1_INTR_IN_146
MAIN_PSC0_PSC_ALLINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_146

Table 10-30. Top Level OUT Interrupts

Instance	OUT Interrupt	Connected To
MCU_MCU_16FF0	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_101
	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_102
MCU_CTRL_MMR0	MCU_CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_0
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_129
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_129
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_128
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_128
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_128
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_128
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128

Table 10-31. MCU_GPIOMUX_INTROUTER0 Out Interrupts

OUT Interrupt	Connected To
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_104
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_104
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_104
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_105
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_105
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_105

Table 10-31. MCU_GPIOMUX_INTROUTER0 Out Interrupts (continued)

OUT Interrupt	Connected To
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_106
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	C7X256V1_CLEC_GIC_SPI_IN_106
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_106
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_107
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	C7X256V1_CLEC_GIC_SPI_IN_107
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_107
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT0_IN_88
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT1_IN_88
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT2_IN_88
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT0_IN_89
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT1_IN_89
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT2_IN_89
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT0_IN_90
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT1_IN_90
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT2_IN_90
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT0_IN_91
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT1_IN_91
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT2_IN_91
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_12	WKUP_R5FSS0_CORE0_INTR_IN_50
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_13	WKUP_R5FSS0_CORE0_INTR_IN_51
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_14	WKUP_R5FSS0_CORE0_INTR_IN_52
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_15	WKUP_R5FSS0_CORE0_INTR_IN_53
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_16	R5FSS0_CORE0_INTR_IN_100
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_16	R5FSS0_CORE1_INTR_IN_100
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_17	R5FSS0_CORE0_INTR_IN_101
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_17	R5FSS0_CORE1_INTR_IN_101

Table 10-31. MCU_GPIOMUX_INTROUTER0 Out Interrupts (continued)

OUT Interrupt	Connected To
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_18	R5FSS0_CORE0_INTR_IN_102
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_18	R5FSS0_CORE1_INTR_IN_102
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_19	R5FSS0_CORE0_INTR_IN_103
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_19	R5FSS0_CORE1_INTR_IN_103
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_20	R5FSS0_CORE0_INTR_IN_104
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_20	R5FSS0_CORE1_INTR_IN_104
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_21	R5FSS0_CORE0_INTR_IN_105
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_21	R5FSS0_CORE1_INTR_IN_105
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_22	R5FSS0_CORE0_INTR_IN_106
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_22	R5FSS0_CORE1_INTR_IN_106
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_23	R5FSS0_CORE0_INTR_IN_107
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_23	R5FSS0_CORE1_INTR_IN_107
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_24	R5FSS1_CORE0_INTR_IN_100
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_24	R5FSS1_CORE1_INTR_IN_100
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_25	R5FSS1_CORE0_INTR_IN_101
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_25	R5FSS1_CORE1_INTR_IN_101
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_26	R5FSS1_CORE0_INTR_IN_102
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_26	R5FSS1_CORE1_INTR_IN_102
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_27	R5FSS1_CORE0_INTR_IN_103
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_27	R5FSS1_CORE1_INTR_IN_103
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_28	R5FSS1_CORE0_INTR_IN_104
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_28	R5FSS1_CORE1_INTR_IN_104
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_29	R5FSS1_CORE0_INTR_IN_105
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_29	R5FSS1_CORE1_INTR_IN_105
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_30	R5FSS1_CORE0_INTR_IN_106
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_30	R5FSS1_CORE1_INTR_IN_106
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_31	R5FSS1_CORE0_INTR_IN_107
MCU_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_31	R5FSS1_CORE1_INTR_IN_107

Table 10-32. WKUP_CTRL_MMR0 Out Interrupts

OUT Interrupt	Connected To
WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_129
WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_129
WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE0_INTR_IN_128
WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS0_CORE1_INTR_IN_128
WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE0_INTR_IN_128

Table 10-32. WKUP_CTRL_MMR0 Out Interrupts (continued)

OUT Interrupt	Connected To
WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	R5FSS1_CORE1_INTR_IN_128
WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128

Table 10-33. CPSW OUT Interrupts

OUT Interrupt	Connected To
CPSW0_CPTS_COMP_OUT_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPOUT_CP_GEMAC_CPTS0_TS_COMP_IN_0
CPSW0_CPTS_COMP_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_48
CPSW0_CPTS_COMP_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_48
CPSW0_CPTS_COMP_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_0
CPSW0_CPTS_COMP_OUT_0	R5FSS0_CORE0_INTR_IN_48
CPSW0_CPTS_COMP_OUT_0	R5FSS0_CORE1_INTR_IN_48
CPSW0_CPTS_COMP_OUT_0	R5FSS1_CORE0_INTR_IN_48

Table 10-33. CPSW OUT Interrupts (continued)

OUT Interrupt	Connected To
CPSW0_CPTS_COMP_OUT_0	R5FSS1_CORE1_INTR_IN_48
CPSW0_CPTS_COMP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_48
CPSW0_CPTS_GENF0_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_16
CPSW0_CPTS_GENF1_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_17
CPSW0_CPTS_SYNC_OUT_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCOUT_CP_GEMAC_CPTS0_TS_SYNC_IN_0
CPSW0_CPTS_SYNC_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_18
CPSW0_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_67
CPSW0_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_3
CPSW0_EVNT_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_134
CPSW0_EVNT_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_134
CPSW0_EVNT_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_134
CPSW0_EVNT_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_134
CPSW0_EVNT_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_134
CPSW0_EVNT_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_134
CPSW0_EVNT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_134
CPSW0_MDIO_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_135
CPSW0_MDIO_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_135
CPSW0_MDIO_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_135
CPSW0_MDIO_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_135
CPSW0_MDIO_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_135
CPSW0_MDIO_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_135
CPSW0_MDIO_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_135
CPSW0_STAT_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_136
CPSW0_STAT_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_136
CPSW0_STAT_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_136
CPSW0_STAT_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_136
CPSW0_STAT_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_136
CPSW0_STAT_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_136
CPSW0_STAT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_136

Table 10-34. DCC Out Interrupts

Instance	OUT Interrupt	Connected To
DCC0	DCC0_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	DCC0_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109

Table 10-34. DCC Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC0_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC0_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_112
DCC1	DCC1_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	DCC1_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109
	DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC1_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC1_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_113
DCC2	DCC2_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	DCC2_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC2_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109
	DCC2_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC2_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC2_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC2_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC2_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_114
DCC3	DCC3_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	DCC3_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC3_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109
	DCC3_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC3_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC3_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC3_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC3_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_115
DCC4	DCC4_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	DCC4_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC4_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109
	DCC4_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC4_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC4_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC4_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC4_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_116

Table 10-34. DCC Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
DCC5	DCC5_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	DCC5_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC5_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109
	DCC5_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC5_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC5_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC5_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC5_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_117
DCC6	DCC6_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	DCC6_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC6_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109
	DCC6_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC6_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC6_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC6_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC6_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_79
DCC7	DCC7_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128

Table 10-34. DCC Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	DCC7_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC7_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109
	DCC7_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC7_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC7_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC7_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC7_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_73
DCC8	DCC8_INTR_DONE_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_128
	DCC8_INTR_DONE_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_128
	DCC8_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_109
	DCC8_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_109
	DCC8_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_109
	DCC8_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_109
	DCC8_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC8_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_223
MCU_DCC0	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_108
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_108
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_108
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_108
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_108
	MCU_DCC0_INTR_ERR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_37
MCU_DCC1	MCU_DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_137
	MCU_DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_137
	MCU_DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_137
	MCU_DCC1_INTR_DONE_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_137
	MCU_DCC1_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_137

Table 10-34. DCC Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCU_DCC1_INTR_ERR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_36

Table 10-35. DMASS0_INTAGGR Out Interrupts

OUT Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_64
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_64
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1	R5FSS1_CORE0_INTR_IN_65
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1	R5FSS1_CORE1_INTR_IN_65
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2	R5FSS1_CORE0_INTR_IN_66
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2	R5FSS1_CORE1_INTR_IN_66
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3	R5FSS1_CORE0_INTR_IN_67
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3	R5FSS1_CORE1_INTR_IN_67
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4	R5FSS1_CORE0_INTR_IN_68
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4	R5FSS1_CORE1_INTR_IN_68
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5	R5FSS1_CORE0_INTR_IN_69
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5	R5FSS1_CORE1_INTR_IN_69
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6	R5FSS1_CORE0_INTR_IN_70
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6	R5FSS1_CORE1_INTR_IN_70
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7	R5FSS1_CORE0_INTR_IN_71
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7	R5FSS1_CORE1_INTR_IN_71
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8	R5FSS1_CORE0_INTR_IN_72
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8	R5FSS1_CORE1_INTR_IN_72
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9	R5FSS1_CORE0_INTR_IN_73
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9	R5FSS1_CORE1_INTR_IN_73
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10	R5FSS1_CORE0_INTR_IN_74
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10	R5FSS1_CORE1_INTR_IN_74
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11	R5FSS1_CORE0_INTR_IN_75
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11	R5FSS1_CORE1_INTR_IN_75
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12	R5FSS1_CORE0_INTR_IN_76
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12	R5FSS1_CORE1_INTR_IN_76
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13	R5FSS1_CORE0_INTR_IN_77
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13	R5FSS1_CORE1_INTR_IN_77
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14	R5FSS1_CORE0_INTR_IN_78
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14	R5FSS1_CORE1_INTR_IN_78
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15	R5FSS1_CORE0_INTR_IN_79

Table 10-35. DMASS0_INTAGGR Out Interrupts (continued)

OUT Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15	R5FSS1_CORE1_INTR_IN_79
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16	R5FSS1_CORE0_INTR_IN_8
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16	R5FSS1_CORE1_INTR_IN_8
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17	R5FSS1_CORE0_INTR_IN_9
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17	R5FSS1_CORE1_INTR_IN_9
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18	R5FSS1_CORE0_INTR_IN_10
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18	R5FSS1_CORE1_INTR_IN_10
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19	R5FSS1_CORE0_INTR_IN_11
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19	R5FSS1_CORE1_INTR_IN_11
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20	R5FSS1_CORE0_INTR_IN_12
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20	R5FSS1_CORE1_INTR_IN_12
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21	R5FSS1_CORE0_INTR_IN_13
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21	R5FSS1_CORE1_INTR_IN_13
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22	R5FSS1_CORE0_INTR_IN_14
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22	R5FSS1_CORE1_INTR_IN_14
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23	R5FSS1_CORE0_INTR_IN_15
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23	R5FSS1_CORE1_INTR_IN_15
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24	R5FSS1_CORE0_INTR_IN_153
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24	R5FSS1_CORE1_INTR_IN_153
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25	R5FSS1_CORE0_INTR_IN_154
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25	R5FSS1_CORE1_INTR_IN_154
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26	R5FSS1_CORE0_INTR_IN_155
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26	R5FSS1_CORE1_INTR_IN_155
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27	R5FSS1_CORE0_INTR_IN_156
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27	R5FSS1_CORE1_INTR_IN_156
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28	R5FSS1_CORE0_INTR_IN_157
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28	R5FSS1_CORE1_INTR_IN_157
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29	R5FSS1_CORE0_INTR_IN_158
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29	R5FSS1_CORE1_INTR_IN_158
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30	R5FSS1_CORE0_INTR_IN_159
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30	R5FSS1_CORE1_INTR_IN_159
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31	R5FSS1_CORE0_INTR_IN_160
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31	R5FSS1_CORE1_INTR_IN_160
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32	C7X256V0_CLEC_GIC_SPI_IN_96

Table 10-35. DMASS0_INTAGGR Out Interrupts (continued)

OUT Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32	C7X256V1_CLEC_GIC_SPI_IN_96
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33	C7X256V0_CLEC_GIC_SPI_IN_97
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33	C7X256V1_CLEC_GIC_SPI_IN_97
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34	C7X256V0_CLEC_GIC_SPI_IN_98
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34	C7X256V1_CLEC_GIC_SPI_IN_98
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35	C7X256V0_CLEC_GIC_SPI_IN_99
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35	C7X256V1_CLEC_GIC_SPI_IN_99
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36	C7X256V0_CLEC_GIC_SPI_IN_100
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36	C7X256V1_CLEC_GIC_SPI_IN_100
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37	C7X256V0_CLEC_GIC_SPI_IN_101
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37	C7X256V1_CLEC_GIC_SPI_IN_101
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38	C7X256V0_CLEC_GIC_SPI_IN_102
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38	C7X256V1_CLEC_GIC_SPI_IN_102
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39	C7X256V0_CLEC_GIC_SPI_IN_103
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39	C7X256V1_CLEC_GIC_SPI_IN_103
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40	WKUP_R5FSS0_CORE0_INTR_IN_64
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41	WKUP_R5FSS0_CORE0_INTR_IN_65
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42	WKUP_R5FSS0_CORE0_INTR_IN_66
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43	WKUP_R5FSS0_CORE0_INTR_IN_67
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44	WKUP_R5FSS0_CORE0_INTR_IN_68
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45	WKUP_R5FSS0_CORE0_INTR_IN_69
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46	WKUP_R5FSS0_CORE0_INTR_IN_70
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47	WKUP_R5FSS0_CORE0_INTR_IN_71
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48	WKUP_R5FSS0_CORE0_INTR_IN_72
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49	WKUP_R5FSS0_CORE0_INTR_IN_73
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50	WKUP_R5FSS0_CORE0_INTR_IN_74
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51	WKUP_R5FSS0_CORE0_INTR_IN_75
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52	WKUP_R5FSS0_CORE0_INTR_IN_76
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53	WKUP_R5FSS0_CORE0_INTR_IN_77
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54	WKUP_R5FSS0_CORE0_INTR_IN_78
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55	WKUP_R5FSS0_CORE0_INTR_IN_79
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56	WKUP_R5FSS0_CORE0_INTR_IN_80
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57	WKUP_R5FSS0_CORE0_INTR_IN_81
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58	WKUP_R5FSS0_CORE0_INTR_IN_82

Table 10-35. DMASS0_INTAGGR Out Interrupts (continued)

OUT Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59	WKUP_R5FSS0_CORE0_INTR_IN_83
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60	WKUP_R5FSS0_CORE0_INTR_IN_84
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61	WKUP_R5FSS0_CORE0_INTR_IN_85
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62	WKUP_R5FSS0_CORE0_INTR_IN_86
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63	WKUP_R5FSS0_CORE0_INTR_IN_87
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64	WKUP_R5FSS0_CORE0_INTR_IN_88
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65	WKUP_R5FSS0_CORE0_INTR_IN_89
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66	WKUP_R5FSS0_CORE0_INTR_IN_90
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67	WKUP_R5FSS0_CORE0_INTR_IN_91
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68	WKUP_R5FSS0_CORE0_INTR_IN_92
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69	WKUP_R5FSS0_CORE0_INTR_IN_93
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70	WKUP_R5FSS0_CORE0_INTR_IN_94
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71	WKUP_R5FSS0_CORE0_INTR_IN_95
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72	WKUP_R5FSS0_CORE0_INTR_IN_8
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73	WKUP_R5FSS0_CORE0_INTR_IN_9
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74	WKUP_R5FSS0_CORE0_INTR_IN_10
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75	WKUP_R5FSS0_CORE0_INTR_IN_11
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76	WKUP_R5FSS0_CORE0_INTR_IN_12
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77	WKUP_R5FSS0_CORE0_INTR_IN_13
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78	WKUP_R5FSS0_CORE0_INTR_IN_14
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79	WKUP_R5FSS0_CORE0_INTR_IN_15
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_84	C7X256V0_CLEC_SOC_EVENTS_IN_IN_16
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_85	C7X256V0_CLEC_SOC_EVENTS_IN_IN_17
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_86	C7X256V0_CLEC_SOC_EVENTS_IN_IN_18
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_87	C7X256V0_CLEC_SOC_EVENTS_IN_IN_19
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_88	C7X256V0_CLEC_SOC_EVENTS_IN_IN_20
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_89	C7X256V0_CLEC_SOC_EVENTS_IN_IN_21
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_90	C7X256V0_CLEC_SOC_EVENTS_IN_IN_22
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_91	C7X256V0_CLEC_SOC_EVENTS_IN_IN_23
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_92	C7X256V0_CLEC_SOC_EVENTS_IN_IN_24
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_93	C7X256V0_CLEC_SOC_EVENTS_IN_IN_25
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_94	C7X256V0_CLEC_SOC_EVENTS_IN_IN_26
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_95	C7X256V0_CLEC_SOC_EVENTS_IN_IN_27
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_96	C7X256V0_CLEC_SOC_EVENTS_IN_IN_28

Table 10-35. DMASS0_INTAGGR Out Interrupts (continued)

OUT Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_97	C7X256V0_CLEC_SOC_EVENTS_IN_IN_29
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_98	C7X256V0_CLEC_SOC_EVENTS_IN_IN_30
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_99	C7X256V0_CLEC_SOC_EVENTS_IN_IN_31
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_100	C7X256V1_CLEC_SOC_EVENTS_IN_IN_16
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_101	C7X256V1_CLEC_SOC_EVENTS_IN_IN_17
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_102	C7X256V1_CLEC_SOC_EVENTS_IN_IN_18
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_103	C7X256V1_CLEC_SOC_EVENTS_IN_IN_19
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_104	C7X256V1_CLEC_SOC_EVENTS_IN_IN_20
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_105	C7X256V1_CLEC_SOC_EVENTS_IN_IN_21
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_106	C7X256V1_CLEC_SOC_EVENTS_IN_IN_22
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_107	C7X256V1_CLEC_SOC_EVENTS_IN_IN_23
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_108	C7X256V1_CLEC_SOC_EVENTS_IN_IN_24
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_109	C7X256V1_CLEC_SOC_EVENTS_IN_IN_25
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_110	C7X256V1_CLEC_SOC_EVENTS_IN_IN_26
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_111	C7X256V1_CLEC_SOC_EVENTS_IN_IN_27
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_112	C7X256V1_CLEC_SOC_EVENTS_IN_IN_28
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_113	C7X256V1_CLEC_SOC_EVENTS_IN_IN_29
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_114	C7X256V1_CLEC_SOC_EVENTS_IN_IN_30
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_115	C7X256V1_CLEC_SOC_EVENTS_IN_IN_31
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_152	R5FSS0_CORE0_INTR_IN_64
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_152	R5FSS0_CORE1_INTR_IN_64
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_153	R5FSS0_CORE0_INTR_IN_65
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_153	R5FSS0_CORE1_INTR_IN_65
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_154	R5FSS0_CORE0_INTR_IN_66
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_154	R5FSS0_CORE1_INTR_IN_66
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_155	R5FSS0_CORE0_INTR_IN_67
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_155	R5FSS0_CORE1_INTR_IN_67
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_156	R5FSS0_CORE0_INTR_IN_68
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_156	R5FSS0_CORE1_INTR_IN_68
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_157	R5FSS0_CORE0_INTR_IN_69
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_157	R5FSS0_CORE1_INTR_IN_69
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_158	R5FSS0_CORE0_INTR_IN_70
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_158	R5FSS0_CORE1_INTR_IN_70
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_159	R5FSS0_CORE0_INTR_IN_71
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_159	R5FSS0_CORE1_INTR_IN_71
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_160	R5FSS0_CORE0_INTR_IN_72

Table 10-35. DMASS0_INTAGGR Out Interrupts (continued)

OUT Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_160	R5FSS0_CORE1_INTR_IN_72
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_161	R5FSS0_CORE0_INTR_IN_73
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_161	R5FSS0_CORE1_INTR_IN_73
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_162	R5FSS0_CORE0_INTR_IN_74
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_162	R5FSS0_CORE1_INTR_IN_74
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_163	R5FSS0_CORE0_INTR_IN_75
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_163	R5FSS0_CORE1_INTR_IN_75
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_164	R5FSS0_CORE0_INTR_IN_76
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_164	R5FSS0_CORE1_INTR_IN_76
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_165	R5FSS0_CORE0_INTR_IN_77
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_165	R5FSS0_CORE1_INTR_IN_77
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_166	R5FSS0_CORE0_INTR_IN_78
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_166	R5FSS0_CORE1_INTR_IN_78
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_167	R5FSS0_CORE0_INTR_IN_79
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_167	R5FSS0_CORE1_INTR_IN_79
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168	R5FSS0_CORE0_INTR_IN_8
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168	R5FSS0_CORE1_INTR_IN_8
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169	R5FSS0_CORE0_INTR_IN_9
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169	R5FSS0_CORE1_INTR_IN_9
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170	R5FSS0_CORE0_INTR_IN_10
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170	R5FSS0_CORE1_INTR_IN_10
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171	R5FSS0_CORE0_INTR_IN_11
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171	R5FSS0_CORE1_INTR_IN_11
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172	R5FSS0_CORE0_INTR_IN_12
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172	R5FSS0_CORE1_INTR_IN_12
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173	R5FSS0_CORE0_INTR_IN_13
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173	R5FSS0_CORE1_INTR_IN_13
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174	R5FSS0_CORE0_INTR_IN_14
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174	R5FSS0_CORE1_INTR_IN_14
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175	R5FSS0_CORE0_INTR_IN_15
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175	R5FSS0_CORE1_INTR_IN_15
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_176	R5FSS0_CORE0_INTR_IN_153
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_176	R5FSS0_CORE1_INTR_IN_153
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_177	R5FSS0_CORE0_INTR_IN_154

Table 10-35. DMASS0_INTAGGR Out Interrupts (continued)

OUT Interrupt	Connected To
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_177	R5FSS0_CORE1_INTR_IN_154
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_178	R5FSS0_CORE0_INTR_IN_155
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_178	R5FSS0_CORE1_INTR_IN_155
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_179	R5FSS0_CORE0_INTR_IN_156
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_179	R5FSS0_CORE1_INTR_IN_156
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_180	R5FSS0_CORE0_INTR_IN_157
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_180	R5FSS0_CORE1_INTR_IN_157
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_181	R5FSS0_CORE0_INTR_IN_158
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_181	R5FSS0_CORE1_INTR_IN_158
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_182	R5FSS0_CORE0_INTR_IN_159
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_182	R5FSS0_CORE1_INTR_IN_159
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_183	R5FSS0_CORE0_INTR_IN_160
DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_183	R5FSS0_CORE1_INTR_IN_160

Table 10-36. Timer Out Interrupts

Instance	OUT Interrupt	Connected To
TIMER0	TIMER0_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_152
	TIMER0_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_152
	TIMER0_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_24
	TIMER0_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_24
	TIMER0_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_24
	TIMER0_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_24
	TIMER0_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_216
	TIMER0_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_0
TIMER1	TIMER1_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_153
	TIMER1_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_153
	TIMER1_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_25
	TIMER1_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_25
	TIMER1_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_25
	TIMER1_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_25
	TIMER1_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_217
	TIMER1_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_1
TIMER10	TIMER10_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_66
	TIMER10_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_66
	TIMER10_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_266
	TIMER10_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_266
	TIMER10_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_266

Table 10-36. Timer Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	TIMER10_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_266
	TIMER10_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_226
TIMER11	TIMER11_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_67
	TIMER11_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_67
	TIMER11_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_267
	TIMER11_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_267
	TIMER11_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_267
	TIMER11_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_267
	TIMER11_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_227
TIMER12	TIMER12_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_68
	TIMER12_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_68
	TIMER12_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_268
	TIMER12_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_268
	TIMER12_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_268
	TIMER12_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_268
	TIMER12_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_228
TIMER13	TIMER13_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_69
	TIMER13_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_69
	TIMER13_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_269
	TIMER13_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_269
	TIMER13_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_269
	TIMER13_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_269
	TIMER13_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_229
TIMER14	TIMER14_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_70
	TIMER14_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_70
	TIMER14_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_270
	TIMER14_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_270
	TIMER14_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_270
	TIMER14_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_270
	TIMER14_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_230
TIMER15	TIMER15_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_71
	TIMER15_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_71
	TIMER15_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_271
	TIMER15_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_271

Table 10-36. Timer Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	TIMER15_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_271
	TIMER15_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_271
	TIMER15_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_231
TIMER2	TIMER2_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_154
	TIMER2_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_154
	TIMER2_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_26
	TIMER2_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_26
	TIMER2_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_26
	TIMER2_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_26
	TIMER2_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_218
	TIMER2_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_2
TIMER3	TIMER3_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_155
	TIMER3_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_155
	TIMER3_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_27
	TIMER3_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_27
	TIMER3_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_27
	TIMER3_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_27
	TIMER3_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_219
	TIMER3_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_3
TIMER4	TIMER4_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_156
	TIMER4_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_156
	TIMER4_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_28
	TIMER4_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_28
	TIMER4_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_28
	TIMER4_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_28
	TIMER4_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_220
	TIMER4_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_4
TIMER5	TIMER5_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_157
	TIMER5_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_157
	TIMER5_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_29
	TIMER5_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_29
	TIMER5_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_29
	TIMER5_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_29
	TIMER5_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_221

Table 10-36. Timer Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	TIMER5_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_5
TIMER6	TIMER6_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_158
	TIMER6_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_158
	TIMER6_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_22
	TIMER6_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_22
	TIMER6_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_22
	TIMER6_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_22
	TIMER6_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_222
	TIMER6_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_6
TIMER7	TIMER7_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_159
	TIMER7_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_159
	TIMER7_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_23
	TIMER7_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_23
	TIMER7_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_23
	TIMER7_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_23
	TIMER7_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_223
	TIMER7_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_7
TIMER8	TIMER8_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_64
	TIMER8_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_64
	TIMER8_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_264
	TIMER8_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_264
	TIMER8_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_264
	TIMER8_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_264
	TIMER8_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_224
	TIMER8_TIMER_PWM_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_8
TIMER9	TIMER9_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_65
	TIMER9_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_65
	TIMER9_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_265
	TIMER9_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_265
	TIMER9_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_265
	TIMER9_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_265
	TIMER9_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_225
WKUP_TIMER0	WKUP_TIMER0_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_138
	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_28
	WKUP_TIMER0_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_214
WKUP_TIMER1	WKUP_TIMER1_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_139
	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_29
	WKUP_TIMER1_TIMER_PWM_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_215

Table 10-37. ECAP Out Interrupts

Instance	OUT Interrupt	Connected To
ECAP0	ECAP0_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_145
	ECAP0_ECAP_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_145
	ECAP0_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_83
	ECAP0_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_83
	ECAP0_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_83
	ECAP0_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_83
ECAP1	ECAP1_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_146
	ECAP1_ECAP_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_146
	ECAP1_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_84
	ECAP1_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_84
	ECAP1_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_84
	ECAP1_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_84
ECAP2	ECAP2_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_147
	ECAP2_ECAP_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_147
	ECAP2_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_85
	ECAP2_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_85
	ECAP2_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_85
	ECAP2_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_85
ECAP3	ECAP3_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_148
	ECAP3_ECAP_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_148
	ECAP3_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_86
	ECAP3_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_86

Table 10-37. ECAP Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
ECAP3	ECAP3_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_86
	ECAP3_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_86
ECAP4	ECAP4_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_149
	ECAP4_ECAP_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_149
	ECAP4_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_87
	ECAP4_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_87
	ECAP4_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_87
	ECAP4_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_87
ECAP5	ECAP5_ECAP_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_150
	ECAP5_ECAP_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_150
	ECAP5_ECAP_INT_OUT_0	R5FSS0_CORE0_INTR_IN_88
	ECAP5_ECAP_INT_OUT_0	R5FSS0_CORE1_INTR_IN_88
	ECAP5_ECAP_INT_OUT_0	R5FSS1_CORE0_INTR_IN_88
	ECAP5_ECAP_INT_OUT_0	R5FSS1_CORE1_INTR_IN_88

Table 10-38. EMMC Out Interrupts

OUT Interrupt	Connected To
MMCSD0_EMMCSDSS_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_165
MMCSD0_EMMCSDSS_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_165
MMCSD0_EMMCSDSS_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_161
MMCSD0_EMMCSDSS_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_161
MMCSD0_EMMCSDSS_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_161
MMCSD0_EMMCSDSS_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_161
MMCSD0_EMMCSDSS_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_161
MMCSD0_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_54
MMCSD0_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_55
MMCSD0_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_56
MMCSD0_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_57

Table 10-39. ESM Out Interrupts

Instance	OUT Interrupt	Connected To
WKUP_ESM0	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_37
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_140
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_140

Table 10-39. ESM Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_140
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_140
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_140
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_38
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_141
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_141
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_141
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_141
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_141
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_39
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_142
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_142
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_142
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_142
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_142
ESM0	ESM0_ESM_INT_CFG_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_180
	ESM0_ESM_INT_CFG_LVL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_180
	ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_0
	ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_167
	ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_167
	ESM0_ESM_INT_HI_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_181
	ESM0_ESM_INT_HI_LVL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_181
	ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_1
	ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_168
	ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_168
	ESM0_ESM_INT_LOW_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_182
	ESM0_ESM_INT_LOW_LVL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_182
	ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_2
	ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_169
	ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_169

Table 10-40. FSS Out Interrupts

Instance	OUT Interrupt	Connected To
FSS1_FSAS_0	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_169
	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_169
	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_142
	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_181
	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_181
	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_181
	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_181
	FSS1_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_181
	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_175
	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_175
	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_180
	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_180
	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_180
	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_180
	FSS1_FSAS_0_OTFA_INTR_ERR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_180
FSS1_HYPERBUS1P0_0	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_179
	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_179
	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_179
	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_179

Table 10-40. FSS Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_179
	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_179
	FSS1_HYPERBUS1P0_0_HPB_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_179
FSS1_HYPERBUS_ECC_AGGR_0	FSS1_HYPERBUS_ECC_AGGR_0_HPB_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_143
	FSS1_HYPERBUS_ECC_AGGR_0_HPB_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_144
FSS1_MISC_0	FSS1_MISC_0_ECC_INTR_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_147
FSS1_OSPI_0	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_178
	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_178
	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_178
	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_178
	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_178
	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_178
	FSS1_OSPI_0_OSPI_LVL_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_178
FSS1_OSPI_ECC_AGGR_0	FSS1_OSPI_ECC_AGGR_0_OSPI_ECC_CORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_12
	FSS1_OSPI_ECC_AGGR_0_OSPI_ECC_UNCORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_75

Table 10-40. FSS Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
FSS0	FSS0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_145
	FSS0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_146
	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_170
	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_170
	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_141
	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_182
	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_182
	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_182
	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_182
	FSS0_FSAS_ECC_INTR_ERR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_182
	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_173
	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_173
	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_173

Table 10-40. FSS Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
FSS0	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_173
	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_173
	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_173
	FSS0_FSAS_FOTA_STAT_ERR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_173
	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_172
	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_172
	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_172
	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_172
	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_172
	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_172
	FSS0_FSAS_FOTA_STAT_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_172
	FSS0_OSPI0_ECC_CORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_11
	FSS0_OSPI0_ECC_UNCORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_74
	FSS0_OSPI0_LVL_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_171
	FSS0_OSPI0_LVL_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_171
	FSS0_OSPI0_LVL_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_171
	FSS0_OSPI0_LVL_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_171
	FSS0_OSPI0_LVL_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_171
	FSS0_OSPI0_LVL_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_171
	FSS0_OSPI0_LVL_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_171
	FSS0_OTFA_INTR_ERR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_174
	FSS0_OTFA_INTR_ERR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_174
	FSS0_OTFA_INTR_ERR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_174
	FSS0_OTFA_INTR_ERR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_174
	FSS0_OTFA_INTR_ERR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_174
	FSS0_OTFA_INTR_ERR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_174
	FSS0_OTFA_INTR_ERR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_174

Table 10-41. GPIO Out Interrupts

OUT Interrupt	Connected To
GPIO0_GPIO_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_0

Table 10-41. GPIO Out Interrupts (continued)

OUT Interrupt	Connected To
GPIO0_GPIO_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_1
GPIO0_GPIO_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_2
GPIO0_GPIO_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_3
GPIO0_GPIO_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_4
GPIO0_GPIO_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_5
GPIO0_GPIO_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_6
GPIO0_GPIO_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_7
GPIO0_GPIO_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_8
GPIO0_GPIO_OUT_9	MAIN_GPIOMUX_INTROUTER0_IN_IN_9
GPIO0_GPIO_OUT_10	MAIN_GPIOMUX_INTROUTER0_IN_IN_10
GPIO0_GPIO_OUT_11	MAIN_GPIOMUX_INTROUTER0_IN_IN_11
GPIO0_GPIO_OUT_12	MAIN_GPIOMUX_INTROUTER0_IN_IN_12
GPIO0_GPIO_OUT_13	MAIN_GPIOMUX_INTROUTER0_IN_IN_13
GPIO0_GPIO_OUT_14	MAIN_GPIOMUX_INTROUTER0_IN_IN_14
GPIO0_GPIO_OUT_15	MAIN_GPIOMUX_INTROUTER0_IN_IN_15
GPIO0_GPIO_OUT_16	MAIN_GPIOMUX_INTROUTER0_IN_IN_16
GPIO0_GPIO_OUT_17	MAIN_GPIOMUX_INTROUTER0_IN_IN_17
GPIO0_GPIO_OUT_18	MAIN_GPIOMUX_INTROUTER0_IN_IN_18
GPIO0_GPIO_OUT_19	MAIN_GPIOMUX_INTROUTER0_IN_IN_19
GPIO0_GPIO_OUT_20	MAIN_GPIOMUX_INTROUTER0_IN_IN_20
GPIO0_GPIO_OUT_21	MAIN_GPIOMUX_INTROUTER0_IN_IN_21
GPIO0_GPIO_OUT_22	MAIN_GPIOMUX_INTROUTER0_IN_IN_22
GPIO0_GPIO_OUT_23	MAIN_GPIOMUX_INTROUTER0_IN_IN_23
GPIO0_GPIO_OUT_24	MAIN_GPIOMUX_INTROUTER0_IN_IN_24
GPIO0_GPIO_OUT_25	MAIN_GPIOMUX_INTROUTER0_IN_IN_25
GPIO0_GPIO_OUT_26	MAIN_GPIOMUX_INTROUTER0_IN_IN_26
GPIO0_GPIO_OUT_27	MAIN_GPIOMUX_INTROUTER0_IN_IN_27
GPIO0_GPIO_OUT_28	MAIN_GPIOMUX_INTROUTER0_IN_IN_28
GPIO0_GPIO_OUT_29	MAIN_GPIOMUX_INTROUTER0_IN_IN_29
GPIO0_GPIO_OUT_30	MAIN_GPIOMUX_INTROUTER0_IN_IN_30
GPIO0_GPIO_OUT_31	MAIN_GPIOMUX_INTROUTER0_IN_IN_31
GPIO0_GPIO_OUT_32	MAIN_GPIOMUX_INTROUTER0_IN_IN_32

Table 10-41. GPIO Out Interrupts (continued)

OUT Interrupt	Connected To
GPIO0_GPIO_OUT_33	MAIN_GPIOMUX_INTROUTER0_IN_IN_33
GPIO0_GPIO_OUT_34	MAIN_GPIOMUX_INTROUTER0_IN_IN_34
GPIO0_GPIO_OUT_35	MAIN_GPIOMUX_INTROUTER0_IN_IN_35
GPIO0_GPIO_OUT_36	MAIN_GPIOMUX_INTROUTER0_IN_IN_36
GPIO0_GPIO_OUT_37	MAIN_GPIOMUX_INTROUTER0_IN_IN_37
GPIO0_GPIO_OUT_38	MAIN_GPIOMUX_INTROUTER0_IN_IN_38
GPIO0_GPIO_OUT_39	MAIN_GPIOMUX_INTROUTER0_IN_IN_39
GPIO0_GPIO_OUT_40	MAIN_GPIOMUX_INTROUTER0_IN_IN_40
GPIO0_GPIO_OUT_41	MAIN_GPIOMUX_INTROUTER0_IN_IN_41
GPIO0_GPIO_OUT_42	MAIN_GPIOMUX_INTROUTER0_IN_IN_42
GPIO0_GPIO_OUT_43	MAIN_GPIOMUX_INTROUTER0_IN_IN_43
GPIO0_GPIO_OUT_44	MAIN_GPIOMUX_INTROUTER0_IN_IN_44
GPIO0_GPIO_OUT_45	MAIN_GPIOMUX_INTROUTER0_IN_IN_45
GPIO0_GPIO_OUT_46	MAIN_GPIOMUX_INTROUTER0_IN_IN_46
GPIO0_GPIO_OUT_47	MAIN_GPIOMUX_INTROUTER0_IN_IN_47
GPIO0_GPIO_OUT_48	MAIN_GPIOMUX_INTROUTER0_IN_IN_48
GPIO0_GPIO_OUT_49	MAIN_GPIOMUX_INTROUTER0_IN_IN_49
GPIO0_GPIO_OUT_50	MAIN_GPIOMUX_INTROUTER0_IN_IN_50
GPIO0_GPIO_OUT_51	MAIN_GPIOMUX_INTROUTER0_IN_IN_51
GPIO0_GPIO_OUT_52	MAIN_GPIOMUX_INTROUTER0_IN_IN_52
GPIO0_GPIO_OUT_55	MAIN_GPIOMUX_INTROUTER0_IN_IN_55
GPIO0_GPIO_OUT_56	MAIN_GPIOMUX_INTROUTER0_IN_IN_56
GPIO0_GPIO_OUT_57	MAIN_GPIOMUX_INTROUTER0_IN_IN_57
GPIO0_GPIO_OUT_58	MAIN_GPIOMUX_INTROUTER0_IN_IN_58
GPIO0_GPIO_OUT_59	MAIN_GPIOMUX_INTROUTER0_IN_IN_59
GPIO0_GPIO_OUT_62	MAIN_GPIOMUX_INTROUTER0_IN_IN_62
GPIO0_GPIO_OUT_63	MAIN_GPIOMUX_INTROUTER0_IN_IN_63
GPIO0_GPIO_OUT_64	MAIN_GPIOMUX_INTROUTER0_IN_IN_64
GPIO0_GPIO_OUT_65	MAIN_GPIOMUX_INTROUTER0_IN_IN_65
GPIO0_GPIO_OUT_66	MAIN_GPIOMUX_INTROUTER0_IN_IN_66
GPIO0_GPIO_OUT_67	MAIN_GPIOMUX_INTROUTER0_IN_IN_67
GPIO0_GPIO_OUT_68	MAIN_GPIOMUX_INTROUTER0_IN_IN_68
GPIO0_GPIO_OUT_69	MAIN_GPIOMUX_INTROUTER0_IN_IN_69
GPIO0_GPIO_OUT_70	MAIN_GPIOMUX_INTROUTER0_IN_IN_70

Table 10-41. GPIO Out Interrupts (continued)

OUT Interrupt	Connected To
GPIO0_GPIO_OUT_71	MAIN_GPIOMUX_INTROUTER0_IN_IN_71
GPIO0_GPIO_OUT_72	MAIN_GPIOMUX_INTROUTER0_IN_IN_72
GPIO0_GPIO_OUT_73	MAIN_GPIOMUX_INTROUTER0_IN_IN_73
GPIO0_GPIO_OUT_74	MAIN_GPIOMUX_INTROUTER0_IN_IN_74
GPIO0_GPIO_OUT_75	MAIN_GPIOMUX_INTROUTER0_IN_IN_75
GPIO0_GPIO_OUT_76	MAIN_GPIOMUX_INTROUTER0_IN_IN_76
GPIO0_GPIO_OUT_77	MAIN_GPIOMUX_INTROUTER0_IN_IN_77
GPIO0_GPIO_OUT_78	MAIN_GPIOMUX_INTROUTER0_IN_IN_78
GPIO0_GPIO_OUT_79	MAIN_GPIOMUX_INTROUTER0_IN_IN_79
GPIO0_GPIO_OUT_80	MAIN_GPIOMUX_INTROUTER0_IN_IN_80
GPIO0_GPIO_OUT_81	MAIN_GPIOMUX_INTROUTER0_IN_IN_81
GPIO0_GPIO_OUT_82	MAIN_GPIOMUX_INTROUTER0_IN_IN_82
GPIO0_GPIO_OUT_83	MAIN_GPIOMUX_INTROUTER0_IN_IN_83
GPIO0_GPIO_OUT_84	MAIN_GPIOMUX_INTROUTER0_IN_IN_84
GPIO0_GPIO_OUT_85	MAIN_GPIOMUX_INTROUTER0_IN_IN_85
GPIO0_GPIO_OUT_86	MAIN_GPIOMUX_INTROUTER0_IN_IN_86
GPIO0_GPIO_OUT_87	MAIN_GPIOMUX_INTROUTER0_IN_IN_87
GPIO0_GPIO_OUT_88	MAIN_GPIOMUX_INTROUTER0_IN_IN_88
GPIO0_GPIO_OUT_89	MAIN_GPIOMUX_INTROUTER0_IN_IN_89
GPIO0_GPIO_OUT_90	MAIN_GPIOMUX_INTROUTER0_IN_IN_90
GPIO0_GPIO_OUT_91	MAIN_GPIOMUX_INTROUTER0_IN_IN_91
GPIO0_GPIO_OUT_92	MAIN_GPIOMUX_INTROUTER0_IN_IN_92
GPIO0_GPIO_BANK_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_192
GPIO0_GPIO_BANK_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_56
GPIO0_GPIO_BANK_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_193
GPIO0_GPIO_BANK_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_57
GPIO0_GPIO_BANK_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_194
GPIO0_GPIO_BANK_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_195
GPIO0_GPIO_BANK_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_196
GPIO0_GPIO_BANK_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_197
GPIO1_GPIO_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_96
GPIO1_GPIO_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_97
GPIO1_GPIO_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_98
GPIO1_GPIO_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_99

Table 10-41. GPIO Out Interrupts (continued)

OUT Interrupt	Connected To
GPIO1_GPIO_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_100
GPIO1_GPIO_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_101
GPIO1_GPIO_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_102
GPIO1_GPIO_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_103
GPIO1_GPIO_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_104
GPIO1_GPIO_OUT_9	MAIN_GPIOMUX_INTROUTER0_IN_IN_105
GPIO1_GPIO_OUT_10	MAIN_GPIOMUX_INTROUTER0_IN_IN_106
GPIO1_GPIO_OUT_11	MAIN_GPIOMUX_INTROUTER0_IN_IN_107
GPIO1_GPIO_OUT_12	MAIN_GPIOMUX_INTROUTER0_IN_IN_108
GPIO1_GPIO_OUT_13	MAIN_GPIOMUX_INTROUTER0_IN_IN_109
GPIO1_GPIO_OUT_14	MAIN_GPIOMUX_INTROUTER0_IN_IN_110
GPIO1_GPIO_OUT_15	MAIN_GPIOMUX_INTROUTER0_IN_IN_111
GPIO1_GPIO_OUT_16	MAIN_GPIOMUX_INTROUTER0_IN_IN_112
GPIO1_GPIO_OUT_17	MAIN_GPIOMUX_INTROUTER0_IN_IN_113
GPIO1_GPIO_OUT_18	MAIN_GPIOMUX_INTROUTER0_IN_IN_114
GPIO1_GPIO_OUT_19	MAIN_GPIOMUX_INTROUTER0_IN_IN_115
GPIO1_GPIO_OUT_20	MAIN_GPIOMUX_INTROUTER0_IN_IN_116
GPIO1_GPIO_OUT_21	MAIN_GPIOMUX_INTROUTER0_IN_IN_117
GPIO1_GPIO_OUT_22	MAIN_GPIOMUX_INTROUTER0_IN_IN_118
GPIO1_GPIO_OUT_23	MAIN_GPIOMUX_INTROUTER0_IN_IN_119
GPIO1_GPIO_OUT_24	MAIN_GPIOMUX_INTROUTER0_IN_IN_120
GPIO1_GPIO_OUT_25	MAIN_GPIOMUX_INTROUTER0_IN_IN_121
GPIO1_GPIO_OUT_26	MAIN_GPIOMUX_INTROUTER0_IN_IN_122
GPIO1_GPIO_OUT_27	MAIN_GPIOMUX_INTROUTER0_IN_IN_123
GPIO1_GPIO_OUT_28	MAIN_GPIOMUX_INTROUTER0_IN_IN_124
GPIO1_GPIO_OUT_29	MAIN_GPIOMUX_INTROUTER0_IN_IN_125
GPIO1_GPIO_OUT_30	MAIN_GPIOMUX_INTROUTER0_IN_IN_126
GPIO1_GPIO_OUT_31	MAIN_GPIOMUX_INTROUTER0_IN_IN_127
GPIO1_GPIO_OUT_32	MAIN_GPIOMUX_INTROUTER0_IN_IN_128
GPIO1_GPIO_OUT_33	MAIN_GPIOMUX_INTROUTER0_IN_IN_129
GPIO1_GPIO_OUT_34	MAIN_GPIOMUX_INTROUTER0_IN_IN_130
GPIO1_GPIO_OUT_35	MAIN_GPIOMUX_INTROUTER0_IN_IN_131
GPIO1_GPIO_OUT_36	MAIN_GPIOMUX_INTROUTER0_IN_IN_132
GPIO1_GPIO_OUT_37	MAIN_GPIOMUX_INTROUTER0_IN_IN_133

Table 10-41. GPIO Out Interrupts (continued)

OUT Interrupt	Connected To
GPIO1_GPIO_OUT_38	MAIN_GPIOMUX_INTROUTER0_IN_IN_134
GPIO1_GPIO_OUT_39	MAIN_GPIOMUX_INTROUTER0_IN_IN_135
GPIO1_GPIO_OUT_40	MAIN_GPIOMUX_INTROUTER0_IN_IN_136
GPIO1_GPIO_OUT_41	MAIN_GPIOMUX_INTROUTER0_IN_IN_137
GPIO1_GPIO_OUT_42	MAIN_GPIOMUX_INTROUTER0_IN_IN_138
GPIO1_GPIO_OUT_43	MAIN_GPIOMUX_INTROUTER0_IN_IN_139
GPIO1_GPIO_OUT_44	MAIN_GPIOMUX_INTROUTER0_IN_IN_140
GPIO1_GPIO_OUT_45	MAIN_GPIOMUX_INTROUTER0_IN_IN_141
GPIO1_GPIO_OUT_46	MAIN_GPIOMUX_INTROUTER0_IN_IN_142
GPIO1_GPIO_OUT_47	MAIN_GPIOMUX_INTROUTER0_IN_IN_143
GPIO1_GPIO_OUT_48	MAIN_GPIOMUX_INTROUTER0_IN_IN_144
GPIO1_GPIO_OUT_49	MAIN_GPIOMUX_INTROUTER0_IN_IN_145
GPIO1_GPIO_OUT_50	MAIN_GPIOMUX_INTROUTER0_IN_IN_146
GPIO1_GPIO_OUT_72	MAIN_GPIOMUX_INTROUTER0_IN_IN_168
GPIO1_GPIO_OUT_74	MAIN_GPIOMUX_INTROUTER0_IN_IN_170
GPIO1_GPIO_OUT_75	MAIN_GPIOMUX_INTROUTER0_IN_IN_171
GPIO1_GPIO_OUT_76	MAIN_GPIOMUX_INTROUTER0_IN_IN_172
GPIO1_GPIO_OUT_77	MAIN_GPIOMUX_INTROUTER0_IN_IN_173
GPIO1_GPIO_OUT_78	MAIN_GPIOMUX_INTROUTER0_IN_IN_174
GPIO1_GPIO_OUT_79	MAIN_GPIOMUX_INTROUTER0_IN_IN_175
GPIO1_GPIO_OUT_80	MAIN_GPIOMUX_INTROUTER0_IN_IN_176
GPIO1_GPIO_OUT_81	MAIN_GPIOMUX_INTROUTER0_IN_IN_177
GPIO1_GPIO_OUT_82	MAIN_GPIOMUX_INTROUTER0_IN_IN_178
GPIO1_GPIO_OUT_83	MAIN_GPIOMUX_INTROUTER0_IN_IN_179
GPIO1_GPIO_OUT_84	MAIN_GPIOMUX_INTROUTER0_IN_IN_180
GPIO1_GPIO_OUT_85	MAIN_GPIOMUX_INTROUTER0_IN_IN_181
GPIO1_GPIO_BANK_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_200
GPIO1_GPIO_BANK_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_201
GPIO1_GPIO_BANK_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_202
GPIO1_GPIO_BANK_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_203
GPIO1_GPIO_BANK_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_204
GPIO1_GPIO_BANK_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_205
MCU_GPIO0_GPIO_OUT_0	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_0
MCU_GPIO0_GPIO_OUT_1	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_1

Table 10-41. GPIO Out Interrupts (continued)

OUT Interrupt	Connected To
MCU_GPIO0_GPIO_OUT_2	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_2
MCU_GPIO0_GPIO_OUT_3	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_3
MCU_GPIO0_GPIO_OUT_4	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_4
MCU_GPIO0_GPIO_OUT_5	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_5
MCU_GPIO0_GPIO_OUT_6	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_6
MCU_GPIO0_GPIO_OUT_7	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_7
MCU_GPIO0_GPIO_OUT_8	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_8
MCU_GPIO0_GPIO_OUT_9	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_9
MCU_GPIO0_GPIO_OUT_10	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_10
MCU_GPIO0_GPIO_OUT_11	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_11
MCU_GPIO0_GPIO_OUT_12	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_12
MCU_GPIO0_GPIO_OUT_13	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_13
MCU_GPIO0_GPIO_OUT_14	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_14
MCU_GPIO0_GPIO_OUT_15	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_15
MCU_GPIO0_GPIO_OUT_16	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_16
MCU_GPIO0_GPIO_OUT_19	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_19
MCU_GPIO0_GPIO_OUT_20	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_20
MCU_GPIO0_GPIO_OUT_21	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_21
MCU_GPIO0_GPIO_OUT_22	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_22
MCU_GPIO0_GPIO_OUT_23	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_23
MCU_GPIO0_GPIO_OUT_24	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_24
MCU_GPIO0_GPIO_OUT_25	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_25
MCU_GPIO0_GPIO_BANK_OUT_0	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_30
MCU_GPIO0_GPIO_BANK_OUT_1	MCU_MCU_GPIOMUX_INTROUTER0_IN_IN_31
MCU_GPIO0_GPIO_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_18

Table 10-42. WKUP_GTC0 Out Interrupts

OUT Interrupt	Connected To
WKUP_GTC0_GTC_PUSH_EVENT_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_11

Table 10-43. WKUP_ICEMELTER0 Out Interrupts

OUT Interrupt	Connected To
WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_23

Table 10-44. ASRC Out Interrupts

OUT Interrupt	Connected To
AASRC0_ERR_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_54
AASRC0_ERR_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_54
AASRC0_ERR_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_54
AASRC0_ERR_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_54
AASRC0_ERR_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_54

Table 10-44. ASRC Out Interrupts (continued)

OUT Interrupt	Connected To
AASRC0_ERR_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_54
AASRC0_INFIFO_DMA_OUT_0	PDMA_AASRC0_6_INFIFO_EVT_IN_0
AASRC0_INFIFO_DMA_OUT_1	PDMA_AASRC0_6_INFIFO_EVT_IN_1
AASRC0_INFIFO_DMA_OUT_2	PDMA_AASRC0_6_INFIFO_EVT_IN_2
AASRC0_INFIFO_DMA_OUT_3	PDMA_AASRC0_6_INFIFO_EVT_IN_3
AASRC0_INFIFO_DMA_OUT_4	PDMA_AASRC0_6_INFIFO_EVT_IN_4
AASRC0_INFIFO_DMA_OUT_5	PDMA_AASRC0_6_INFIFO_EVT_IN_5
AASRC0_INFIFO_DMA_OUT_6	PDMA_AASRC0_6_INFIFO_EVT_IN_6
AASRC0_INFIFO_DMA_OUT_7	PDMA_AASRC0_6_INFIFO_EVT_IN_7
AASRC0_INFIFO_DMA_OUT_8	PDMA_AASRC0_6_INFIFO_EVT_IN_8
AASRC0_INFIFO_DMA_OUT_9	PDMA_AASRC0_6_INFIFO_EVT_IN_9
AASRC0_INFIFO_DMA_OUT_10	PDMA_AASRC0_6_INFIFO_EVT_IN_10
AASRC0_INFIFO_DMA_OUT_11	PDMA_AASRC0_6_INFIFO_EVT_IN_11
AASRC0_INFIFO_DMA_OUT_12	PDMA_AASRC0_6_INFIFO_EVT_IN_12
AASRC0_INFIFO_DMA_OUT_13	PDMA_AASRC0_6_INFIFO_EVT_IN_13
AASRC0_INFIFO_DMA_OUT_14	PDMA_AASRC0_6_INFIFO_EVT_IN_14
AASRC0_INFIFO_DMA_OUT_15	PDMA_AASRC0_6_INFIFO_EVT_IN_15
AASRC0_INFIFO_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_50
AASRC0_INFIFO_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_50
AASRC0_INFIFO_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_50
AASRC0_INFIFO_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_50
AASRC0_INFIFO_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_50
AASRC0_INFIFO_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_50
AASRC0_INGROUP_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_51
AASRC0_INGROUP_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_51
AASRC0_INGROUP_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_51
AASRC0_INGROUP_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_51
AASRC0_INGROUP_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_51
AASRC0_INGROUP_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_51
AASRC0_INGRP_DMA_OUT_0	PDMA_AASRC0_6_INGRP_EVT_IN_0
AASRC0_INGRP_DMA_OUT_1	PDMA_AASRC0_6_INGRP_EVT_IN_1
AASRC0_INGRP_DMA_OUT_2	PDMA_AASRC0_6_INGRP_EVT_IN_2
AASRC0_INGRP_DMA_OUT_3	PDMA_AASRC0_6_INGRP_EVT_IN_3
AASRC0_OUTFIFO_DMA_OUT_0	PDMA_AASRC0_6_OUTFIFO_EVT_IN_0

Table 10-44. ASRC Out Interrupts (continued)

OUT Interrupt	Connected To
AASRC0_OUTFIFO_DMA_OUT_1	PDMA_AASRC0_6_OUTFIFO_EVT_IN_1
AASRC0_OUTFIFO_DMA_OUT_2	PDMA_AASRC0_6_OUTFIFO_EVT_IN_2
AASRC0_OUTFIFO_DMA_OUT_3	PDMA_AASRC0_6_OUTFIFO_EVT_IN_3
AASRC0_OUTFIFO_DMA_OUT_4	PDMA_AASRC0_6_OUTFIFO_EVT_IN_4
AASRC0_OUTFIFO_DMA_OUT_5	PDMA_AASRC0_6_OUTFIFO_EVT_IN_5
AASRC0_OUTFIFO_DMA_OUT_6	PDMA_AASRC0_6_OUTFIFO_EVT_IN_6
AASRC0_OUTFIFO_DMA_OUT_7	PDMA_AASRC0_6_OUTFIFO_EVT_IN_7
AASRC0_OUTFIFO_DMA_OUT_8	PDMA_AASRC0_6_OUTFIFO_EVT_IN_8
AASRC0_OUTFIFO_DMA_OUT_9	PDMA_AASRC0_6_OUTFIFO_EVT_IN_9
AASRC0_OUTFIFO_DMA_OUT_10	PDMA_AASRC0_6_OUTFIFO_EVT_IN_10
AASRC0_OUTFIFO_DMA_OUT_11	PDMA_AASRC0_6_OUTFIFO_EVT_IN_11
AASRC0_OUTFIFO_DMA_OUT_12	PDMA_AASRC0_6_OUTFIFO_EVT_IN_12
AASRC0_OUTFIFO_DMA_OUT_13	PDMA_AASRC0_6_OUTFIFO_EVT_IN_13
AASRC0_OUTFIFO_DMA_OUT_14	PDMA_AASRC0_6_OUTFIFO_EVT_IN_14
AASRC0_OUTFIFO_DMA_OUT_15	PDMA_AASRC0_6_OUTFIFO_EVT_IN_15
AASRC0_OUTFIFO_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_52
AASRC0_OUTFIFO_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_52
AASRC0_OUTFIFO_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_52
AASRC0_OUTFIFO_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_52
AASRC0_OUTFIFO_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_52
AASRC0_OUTFIFO_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_52
AASRC0_OUTGROUP_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_53
AASRC0_OUTGROUP_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_53
AASRC0_OUTGROUP_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_53
AASRC0_OUTGROUP_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_53
AASRC0_OUTGROUP_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_53
AASRC0_OUTGROUP_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_53
AASRC0_OUTGRP_DMA_OUT_0	PDMA_AASRC0_6_OUTGRP_EVT_IN_0
AASRC0_OUTGRP_DMA_OUT_1	PDMA_AASRC0_6_OUTGRP_EVT_IN_1
AASRC0_OUTGRP_DMA_OUT_2	PDMA_AASRC0_6_OUTGRP_EVT_IN_2
AASRC0_OUTGRP_DMA_OUT_3	PDMA_AASRC0_6_OUTGRP_EVT_IN_3
AASRC1_ERR_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_59
AASRC1_ERR_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_59
AASRC1_ERR_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_59

Table 10-44. ASRC Out Interrupts (continued)

OUT Interrupt	Connected To
AASRC1_ERR_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_59
AASRC1_ERR_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_59
AASRC1_ERR_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_59
AASRC1_INFIFO_DMA_OUT_0	PDMA_AASRC1_7_INFIFO_EVT_IN_0
AASRC1_INFIFO_DMA_OUT_1	PDMA_AASRC1_7_INFIFO_EVT_IN_1
AASRC1_INFIFO_DMA_OUT_2	PDMA_AASRC1_7_INFIFO_EVT_IN_2
AASRC1_INFIFO_DMA_OUT_3	PDMA_AASRC1_7_INFIFO_EVT_IN_3
AASRC1_INFIFO_DMA_OUT_4	PDMA_AASRC1_7_INFIFO_EVT_IN_4
AASRC1_INFIFO_DMA_OUT_5	PDMA_AASRC1_7_INFIFO_EVT_IN_5
AASRC1_INFIFO_DMA_OUT_6	PDMA_AASRC1_7_INFIFO_EVT_IN_6
AASRC1_INFIFO_DMA_OUT_7	PDMA_AASRC1_7_INFIFO_EVT_IN_7
AASRC1_INFIFO_DMA_OUT_8	PDMA_AASRC1_7_INFIFO_EVT_IN_8
AASRC1_INFIFO_DMA_OUT_9	PDMA_AASRC1_7_INFIFO_EVT_IN_9
AASRC1_INFIFO_DMA_OUT_10	PDMA_AASRC1_7_INFIFO_EVT_IN_10
AASRC1_INFIFO_DMA_OUT_11	PDMA_AASRC1_7_INFIFO_EVT_IN_11
AASRC1_INFIFO_DMA_OUT_12	PDMA_AASRC1_7_INFIFO_EVT_IN_12
AASRC1_INFIFO_DMA_OUT_13	PDMA_AASRC1_7_INFIFO_EVT_IN_13
AASRC1_INFIFO_DMA_OUT_14	PDMA_AASRC1_7_INFIFO_EVT_IN_14
AASRC1_INFIFO_DMA_OUT_15	PDMA_AASRC1_7_INFIFO_EVT_IN_15
AASRC1_INFIFO_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_55
AASRC1_INFIFO_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_55
AASRC1_INFIFO_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_55
AASRC1_INFIFO_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_55
AASRC1_INFIFO_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_55
AASRC1_INFIFO_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_55
AASRC1_INGROUP_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_56
AASRC1_INGROUP_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_56
AASRC1_INGROUP_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_56
AASRC1_INGROUP_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_56
AASRC1_INGROUP_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_56
AASRC1_INGROUP_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_56
AASRC1_INGRP_DMA_OUT_0	PDMA_AASRC1_7_INGRP_EVT_IN_0
AASRC1_INGRP_DMA_OUT_1	PDMA_AASRC1_7_INGRP_EVT_IN_1
AASRC1_INGRP_DMA_OUT_2	PDMA_AASRC1_7_INGRP_EVT_IN_2

Table 10-44. ASRC Out Interrupts (continued)

OUT Interrupt	Connected To
AASRC1_INGRP_DMA_OUT_3	PDMA_AASRC1_7_INGRP_EVT_IN_3
AASRC1_OUTFIFO_DMA_OUT_0	PDMA_AASRC1_7_OUTFIFO_EVT_IN_0
AASRC1_OUTFIFO_DMA_OUT_1	PDMA_AASRC1_7_OUTFIFO_EVT_IN_1
AASRC1_OUTFIFO_DMA_OUT_2	PDMA_AASRC1_7_OUTFIFO_EVT_IN_2
AASRC1_OUTFIFO_DMA_OUT_3	PDMA_AASRC1_7_OUTFIFO_EVT_IN_3
AASRC1_OUTFIFO_DMA_OUT_4	PDMA_AASRC1_7_OUTFIFO_EVT_IN_4
AASRC1_OUTFIFO_DMA_OUT_5	PDMA_AASRC1_7_OUTFIFO_EVT_IN_5
AASRC1_OUTFIFO_DMA_OUT_6	PDMA_AASRC1_7_OUTFIFO_EVT_IN_6
AASRC1_OUTFIFO_DMA_OUT_7	PDMA_AASRC1_7_OUTFIFO_EVT_IN_7
AASRC1_OUTFIFO_DMA_OUT_8	PDMA_AASRC1_7_OUTFIFO_EVT_IN_8
AASRC1_OUTFIFO_DMA_OUT_9	PDMA_AASRC1_7_OUTFIFO_EVT_IN_9
AASRC1_OUTFIFO_DMA_OUT_10	PDMA_AASRC1_7_OUTFIFO_EVT_IN_10
AASRC1_OUTFIFO_DMA_OUT_11	PDMA_AASRC1_7_OUTFIFO_EVT_IN_11
AASRC1_OUTFIFO_DMA_OUT_12	PDMA_AASRC1_7_OUTFIFO_EVT_IN_12
AASRC1_OUTFIFO_DMA_OUT_13	PDMA_AASRC1_7_OUTFIFO_EVT_IN_13
AASRC1_OUTFIFO_DMA_OUT_14	PDMA_AASRC1_7_OUTFIFO_EVT_IN_14
AASRC1_OUTFIFO_DMA_OUT_15	PDMA_AASRC1_7_OUTFIFO_EVT_IN_15
AASRC1_OUTFIFO_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_57
AASRC1_OUTFIFO_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_57
AASRC1_OUTFIFO_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_57
AASRC1_OUTFIFO_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_57
AASRC1_OUTFIFO_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_57
AASRC1_OUTFIFO_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_57
AASRC1_OUTGROUP_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_58
AASRC1_OUTGROUP_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_58
AASRC1_OUTGROUP_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_58
AASRC1_OUTGROUP_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_58
AASRC1_OUTGROUP_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_58
AASRC1_OUTGROUP_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_58
AASRC1_OUTGRP_DMA_OUT_0	PDMA_AASRC1_7_OUTGRP_EVT_IN_0
AASRC1_OUTGRP_DMA_OUT_1	PDMA_AASRC1_7_OUTGRP_EVT_IN_1
AASRC1_OUTGRP_DMA_OUT_2	PDMA_AASRC1_7_OUTGRP_EVT_IN_2
AASRC1_OUTGRP_DMA_OUT_3	PDMA_AASRC1_7_OUTGRP_EVT_IN_3

Table 10-45. DDPA0 Out Interrupts

OUT Interrupt	Connected To
DDPA0_DDPA_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_177

Table 10-45. DDPA0 Out Interrupts (continued)

OUT Interrupt	Connected To
DDPA0_DDPA_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_177
DDPA0_DDPA_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_177
DDPA0_DDPA_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_177
DDPA0_DDPA_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_177
DDPA0_DDPA_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_177
DDPA0_DDPA_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_177

Table 10-46. EPWM Out Interrupts

Instance	OUT Interrupt	Connected To
EPWM0	EPWM0_EPWM_ETINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_229
	EPWM0_EPWM_ETINT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_229
	EPWM0_EPWM_ETINT_OUT_0	R5FSS0_CORE0_INTR_IN_3
	EPWM0_EPWM_ETINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_123
	EPWM0_EPWM_SYNCO_O_OUT_0	TIMESYNC_EVENT_INTROUTER0_IN_IN_9
	EPWM0_EPWM_SYNCOUT_OUT_0	EPWM1_EPWM_SYNCIN_IN_0
	EPWM0_EPWM_TRIPZINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_230
	EPWM0_EPWM_TRIPZINT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_230
	EPWM0_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_80
	EPWM0_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_80
	EPWM0_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_80
	EPWM0_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_80
	EPWM0_EPWM_TRIPZINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_124
EPWM1	EPWM1_EPWM_ETINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_231
	EPWM1_EPWM_ETINT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_231
	EPWM1_EPWM_ETINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_125
	EPWM1_EPWM_SYNCOUT_OUT_0	EPWM2_EPWM_SYNCIN_IN_0
	EPWM1_EPWM_TRIPZINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_233
	EPWM1_EPWM_TRIPZINT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_233
	EPWM1_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_81
	EPWM1_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_81
	EPWM1_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_81
	EPWM1_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_81

Table 10-46. EPWM Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	EPWM1_EPWM_TRIPZINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_126
EPWM2	EPWM2_EPWM_ETINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_234
	EPWM2_EPWM_ETINT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_234
	EPWM2_EPWM_ETINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_127
	EPWM2_EPWM_TRIPZINT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_235
	EPWM2_EPWM_TRIPZINT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_235
	EPWM2_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE0_INTR_IN_82
	EPWM2_EPWM_TRIPZINT_OUT_0	R5FSS0_CORE1_INTR_IN_82
	EPWM2_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE0_INTR_IN_82
	EPWM2_EPWM_TRIPZINT_OUT_0	R5FSS1_CORE1_INTR_IN_82
	EPWM2_EPWM_TRIPZINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_148

Table 10-47. PBIST Out Interrupts

Instance	OUT Interrupt	Connected To
PBIST0	PBIST0_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
	PBIST0_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST0_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST0_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_228
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_228
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_228
	PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_157
PBIST1	PBIST1_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
	PBIST1_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST1_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST1_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST1_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_243
	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_243
	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_243

Table 10-47. PBIST Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_213
PBIST2	PBIST2_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
	PBIST2_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST2_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST2_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST2_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST2_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_244
	PBIST2_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_244
	PBIST2_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_244
	PBIST2_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_214
PBIST3	PBIST3_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
	PBIST3_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST3_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST3_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST3_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST3_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_246
	PBIST3_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_246
	PBIST3_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_246
	PBIST3_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_202
PBIST4	PBIST4_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
	PBIST4_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST4_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST4_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST4_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST4_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_247
	PBIST4_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_247
	PBIST4_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_247
	PBIST4_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_203

Table 10-47. PBIST Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
PBIST5	PBIST5_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
	PBIST5_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST5_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST5_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST5_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST5_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_248
	PBIST5_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_248
	PBIST5_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_248
	PBIST5_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_204
PBIST6	PBIST6_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
	PBIST6_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST6_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST6_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST6_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST6_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_249
	PBIST6_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_249
	PBIST6_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_249
	PBIST6_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_205
PBIST7	PBIST7_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113
	PBIST7_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST7_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST7_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST7_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST7_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_250
	PBIST7_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_250
	PBIST7_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_250
	PBIST7_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_206
PBIST8	PBIST8_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_113

Table 10-47. PBIST Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	PBIST8_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_113
	PBIST8_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_113
	PBIST8_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_113
	PBIST8_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	PBIST8_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_251
	PBIST8_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_251
	PBIST8_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_251
	PBIST8_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_207
WKUP_PBIST1	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_114
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_114
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_114
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_114
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_114
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_240
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_240
	WKUP_PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_240
	WKUP_PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_159
WKUP_PBIST0	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE0_INTR_IN_114
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	R5FSS0_CORE1_INTR_IN_114
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE0_INTR_IN_114
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	R5FSS1_CORE1_INTR_IN_114
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_114
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_234
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_234
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_234
	WKUP_PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_158

Table 10-48. WKUP_VTM0 Out Interrupts

OUT Interrupt	Connected To
WKUP_VTM0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_11
WKUP_VTM0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_139

Table 10-48. WKUP_VTM0 Out Interrupts (continued)

OUT Interrupt	Connected To
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_183
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_183
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_8
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_137
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_183
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_183
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_183
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_183
WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_183
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_184
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_184
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_10
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_138
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_184
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_184
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_184
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_184
WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_184
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_185
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_185
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_9
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_136
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	R5FSS0_CORE0_INTR_IN_185
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	R5FSS0_CORE1_INTR_IN_185
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	R5FSS1_CORE0_INTR_IN_185
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	R5FSS1_CORE1_INTR_IN_185
WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_185
WKUP_VTM0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_12

Table 10-48. WKUP_VTM0 Out Interrupts (continued)

OUT Interrupt	Connected To
WKUP_VTM0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_140

Table 10-49. Mailbox Out Interrupts

Instance	OUT Interrupt	Connected To
MAILBOX0_MAILBOX_CLUSTER_0	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_240
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_240
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_2	R5FSS1_CORE0_INTR_IN_240
	MAILBOX0_MAILBOX_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_3	R5FSS1_CORE1_INTR_IN_240
MAILBOX0_MAILBOX_CLUSTER_1	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_241
	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS1_CORE0_INTR_IN_241
	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_2	C7X256V0_CLEC_SOC_EVENTS_IN_IN_6
	MAILBOX0_MAILBOX_CLUSTER_1_MAILBOX_CLUSTER_PEND_OUT_3	C7X256V1_CLEC_SOC_EVENTS_IN_IN_6
MAILBOX0_MAILBOX_CLUSTER_2	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_241
	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS1_CORE1_INTR_IN_241
	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_2	C7X256V0_CLEC_SOC_EVENTS_IN_IN_7
	MAILBOX0_MAILBOX_CLUSTER_2_MAILBOX_CLUSTER_PEND_OUT_3	C7X256V1_CLEC_SOC_EVENTS_IN_IN_7
MAILBOX0_MAILBOX_CLUSTER_3	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_242
	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_242
	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_2	C7X256V0_CLEC_SOC_EVENTS_IN_IN_8
	MAILBOX0_MAILBOX_CLUSTER_3_MAILBOX_CLUSTER_PEND_OUT_3	C7X256V1_CLEC_SOC_EVENTS_IN_IN_8
MAILBOX0_MAILBOX_CLUSTER_4	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_242
	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS1_CORE1_INTR_IN_242
	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_2	C7X256V0_CLEC_SOC_EVENTS_IN_IN_9
	MAILBOX0_MAILBOX_CLUSTER_4_MAILBOX_CLUSTER_PEND_OUT_3	C7X256V1_CLEC_SOC_EVENTS_IN_IN_9

Table 10-49. Mailbox Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
MAILBOX0_MAILBOX_CLUSTER_5	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_240
	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE0_INTR_IN_243
	MAILBOX0_MAILBOX_CLUSTER_5_MAILBOX_CLUSTER_PEND_OUT_2	R5FSS1_CORE1_INTR_IN_243
MAILBOX0_MAILBOX_CLUSTER_6	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_241
	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_1	R5FSS0_CORE1_INTR_IN_243
	MAILBOX0_MAILBOX_CLUSTER_6_MAILBOX_CLUSTER_PEND_OUT_2	R5FSS1_CORE0_INTR_IN_243
MAILBOX0_MAILBOX_CLUSTER_7	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_242
	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_1	C7X256V0_CLEC_SOC_EVENTS_IN_IN_10
	MAILBOX0_MAILBOX_CLUSTER_7_MAILBOX_CLUSTER_PEND_OUT_2	C7X256V1_CLEC_SOC_EVENTS_IN_IN_10

Table 10-50. MCAN Out Interrupts

Instance	OUT Interrupt	Connected To
MCAN0	MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_58
	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_59
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_186
	MCAN0_MCANSS_FE_OUT_0	PDMA0_MCANSS_MAIN_0_FE_IN_0
	MCAN0_MCANSS_FE_OUT_1	PDMA0_MCANSS_MAIN_0_FE_IN_1
	MCAN0_MCANSS_FE_OUT_2	PDMA0_MCANSS_MAIN_0_FE_IN_2
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_230
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_230
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_230
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_230
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_230
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE0_INTR_IN_231
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE1_INTR_IN_231
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE0_INTR_IN_231
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE1_INTR_IN_231
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_231

Table 10-50. MCAN Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCAN0_MCANSS_TX_DMA_OUT_0	PDMA0_MCANSS_MAIN_0_TX_IN_0
	MCAN0_MCANSS_TX_DMA_OUT_1	PDMA0_MCANSS_MAIN_0_TX_IN_1
	MCAN0_MCANSS_TX_DMA_OUT_2	PDMA0_MCANSS_MAIN_0_TX_IN_2
MCAN1	MCAN1_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_60
	MCAN1_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_61
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_199
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_199
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_229
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_229
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_229
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_229
	MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_229
	MCAN1_MCANSS_FE_OUT_0	PDMA0_MCANSS_MAIN_1_FE_IN_0
	MCAN1_MCANSS_FE_OUT_1	PDMA0_MCANSS_MAIN_1_FE_IN_1
	MCAN1_MCANSS_FE_OUT_2	PDMA0_MCANSS_MAIN_1_FE_IN_2
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_245
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_245
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_232
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_232
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_232
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_232
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_232
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_246
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_246
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE0_INTR_IN_233
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE1_INTR_IN_233
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE0_INTR_IN_233
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE1_INTR_IN_233
	MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_233
	MCAN1_MCANSS_TX_DMA_OUT_0	PDMA0_MCANSS_MAIN_1_TX_IN_0
	MCAN1_MCANSS_TX_DMA_OUT_1	PDMA0_MCANSS_MAIN_1_TX_IN_1
	MCAN1_MCANSS_TX_DMA_OUT_2	PDMA0_MCANSS_MAIN_1_TX_IN_2

Table 10-50. MCAN Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
MCAN2	MCAN2_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_62
	MCAN2_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_63
	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_189
	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_189
	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_187
	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_187
	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_187
	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_187
	MCAN2_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_187
	MCAN2_MCANSS_FE_OUT_0	PDMA4_MCANSS_MAIN_2_FE_IN_0
	MCAN2_MCANSS_FE_OUT_1	PDMA4_MCANSS_MAIN_2_FE_IN_1
	MCAN2_MCANSS_FE_OUT_2	PDMA4_MCANSS_MAIN_2_FE_IN_2
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_247
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_247
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_234
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_234
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_234
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_234
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_234
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_248
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_248
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE0_INTR_IN_235
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE1_INTR_IN_235
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE0_INTR_IN_235
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE1_INTR_IN_235
	MCAN2_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_235
	MCAN2_MCANSS_TX_DMA_OUT_0	PDMA4_MCANSS_MAIN_2_TX_IN_0
	MCAN2_MCANSS_TX_DMA_OUT_1	PDMA4_MCANSS_MAIN_2_TX_IN_1
	MCAN2_MCANSS_TX_DMA_OUT_2	PDMA4_MCANSS_MAIN_2_TX_IN_2

Table 10-50. MCAN Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
MCAN3	MCAN3_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_68
	MCAN3_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_69
	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_190
	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_190
	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_188
	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_188
	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_188
	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_188
	MCAN3_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_188
	MCAN3_MCANSS_FE_OUT_0	PDMA4_MCANSS_MAIN_3_FE_IN_0
	MCAN3_MCANSS_FE_OUT_1	PDMA4_MCANSS_MAIN_3_FE_IN_1
	MCAN3_MCANSS_FE_OUT_2	PDMA4_MCANSS_MAIN_3_FE_IN_2
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_249
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_249
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_236
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_236
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_236
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_236
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_236
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_250
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_250
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE0_INTR_IN_237
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE1_INTR_IN_237
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE0_INTR_IN_237
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE1_INTR_IN_237

Table 10-50. MCAN Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCAN3_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_237
	MCAN3_MCANSS_TX_DMA_OUT_0	PDMA4_MCANSS_MAIN_3_TX_IN_0
	MCAN3_MCANSS_TX_DMA_OUT_1	PDMA4_MCANSS_MAIN_3_TX_IN_1
	MCAN3_MCANSS_TX_DMA_OUT_2	PDMA4_MCANSS_MAIN_3_TX_IN_2
MCAN4	MCAN4_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_70
	MCAN4_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_71
	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_191
	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_191
	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_189
	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_189
	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_189
	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_189
	MCAN4_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_189
	MCAN4_MCANSS_FE_OUT_0	PDMA4_MCANSS_MAIN_4_FE_IN_0
	MCAN4_MCANSS_FE_OUT_1	PDMA4_MCANSS_MAIN_4_FE_IN_1
	MCAN4_MCANSS_FE_OUT_2	PDMA4_MCANSS_MAIN_4_FE_IN_2
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_251
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_251
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE0_INTR_IN_238
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS0_CORE1_INTR_IN_238
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE0_INTR_IN_238
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0	R5FSS1_CORE1_INTR_IN_238
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_238
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_252
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_252
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE0_INTR_IN_239
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS0_CORE1_INTR_IN_239
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE0_INTR_IN_239

Table 10-50. MCAN Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1	R5FSS1_CORE1_INTR_IN_239
	MCAN4_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_239
	MCAN4_MCANSS_TX_DMA_OUT_0	PDMA4_MCANSS_MAIN_4_TX_IN_0
	MCAN4_MCANSS_TX_DMA_OUT_1	PDMA4_MCANSS_MAIN_4_TX_IN_1
	MCAN4_MCANSS_TX_DMA_OUT_2	PDMA4_MCANSS_MAIN_4_TX_IN_2

Table 10-51. MCASP Out Interrupts

Instance	OUT Interrupt	Connected To
MCASP0	MCASP0_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_0_RX_IN_0
	MCASP0_REC_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_267
	MCASP0_REC_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_267
	MCASP0_REC_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_120
	MCASP0_REC_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_120
	MCASP0_REC_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_120
	MCASP0_REC_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_120
	MCASP0_XMIT_DMA_EVENT_REQ_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_1
	MCASP0_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_0_TX_IN_0
	MCASP0_XMIT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_268
	MCASP0_XMIT_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_268
	MCASP0_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_121
	MCASP0_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_121
	MCASP0_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_121
	MCASP0_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_121
MCASP1	MCASP1_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_1_RX_IN_0
	MCASP1_REC_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_269
	MCASP1_REC_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_269
	MCASP1_REC_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_122
	MCASP1_REC_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_122
	MCASP1_REC_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_122
	MCASP1_REC_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_122
	MCASP1_XMIT_DMA_EVENT_REQ_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_2
	MCASP1_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_1_TX_IN_0
	MCASP1_XMIT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_270
	MCASP1_XMIT_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_270
	MCASP1_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_123
	MCASP1_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_123
	MCASP1_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_123
	MCASP1_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_123

Table 10-51. MCASP Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
MCASP2	MCASP2_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_2_RX_IN_0
	MCASP2_REC_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_271
	MCASP2_REC_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_271
	MCASP2_REC_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_124
	MCASP2_REC_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_124
	MCASP2_REC_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_124
	MCASP2_REC_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_124
	MCASP2_XMIT_DMA_EVENT_REQ_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_3
	MCASP2_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_2_TX_IN_0
	MCASP2_XMIT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_272
	MCASP2_XMIT_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_272
	MCASP2_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_125
	MCASP2_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_125
	MCASP2_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_125
	MCASP2_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_125
MCASP3	MCASP3_REC_DMA_EVENT_REQ_OUT_0	PDMA3_MCASP_MAIN_3_RX_IN_0
	MCASP3_REC_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_273
	MCASP3_REC_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_273
	MCASP3_REC_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_126

Table 10-51. MCASP Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCASP3_REC_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_126
	MCASP3_REC_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_126
	MCASP3_REC_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_126
	MCASP3_XMIT_DMA_EVENT_REQ_OUT_0	PDMA3_MCASP_MAIN_3_TX_IN_0
	MCASP3_XMIT_DMA_EVENT_REQ_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_4
	MCASP3_XMIT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_274
	MCASP3_XMIT_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_274
	MCASP3_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_127
	MCASP3_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_127
	MCASP3_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_127
	MCASP3_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_127
MCASP4	MCASP4_REC_DMA_EVENT_REQ_OUT_0	PDMA3_MCASP_MAIN_4_RX_IN_0
	MCASP4_REC_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_275
	MCASP4_REC_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_275
	MCASP4_REC_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_130
	MCASP4_REC_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_130
	MCASP4_REC_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_130
	MCASP4_REC_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_130
	MCASP4_XMIT_DMA_EVENT_REQ_OUT_0	PDMA3_MCASP_MAIN_4_TX_IN_0
	MCASP4_XMIT_DMA_EVENT_REQ_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_5
	MCASP4_XMIT_INTR_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_276
	MCASP4_XMIT_INTR_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_276
	MCASP4_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_131
	MCASP4_XMIT_INTR_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_131
	MCASP4_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_131
	MCASP4_XMIT_INTR_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_131

Table 10-52. MCRC Out Interrupts

OUT Interrupt	Connected To
MCRC64_0_DMA_EVENT_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_28
MCRC64_0_DMA_EVENT_OUT_1	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_29
MCRC64_0_DMA_EVENT_OUT_2	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_30
MCRC64_0_DMA_EVENT_OUT_3	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_31
MCRC64_0_INT_MCRC_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_166
MCRC64_0_INT_MCRC_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_166
MCRC64_0_INT_MCRC_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_7
MCRC64_0_INT_MCRC_OUT_0	R5FSS0_CORE0_INTR_IN_119
MCRC64_0_INT_MCRC_OUT_0	R5FSS0_CORE1_INTR_IN_119
MCRC64_0_INT_MCRC_OUT_0	R5FSS1_CORE0_INTR_IN_119
MCRC64_0_INT_MCRC_OUT_0	R5FSS1_CORE1_INTR_IN_119
MCRC64_0_INT_MCRC_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_119

Table 10-53. MLB0 Out Interrupts

OUT Interrupt	Connected To
MLB0_MLBSS_ECC_CORR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_77
MLB0_MLBSS_ECC_UNCORR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_78
MLB0_MLBSS_MLB_AHB_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_61
MLB0_MLBSS_MLB_AHB_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_61
MLB0_MLBSS_MLB_AHB_INT_OUT_0	R5FSS0_CORE0_INTR_IN_61
MLB0_MLBSS_MLB_AHB_INT_OUT_0	R5FSS0_CORE1_INTR_IN_61
MLB0_MLBSS_MLB_AHB_INT_OUT_0	R5FSS1_CORE0_INTR_IN_61
MLB0_MLBSS_MLB_AHB_INT_OUT_0	R5FSS1_CORE1_INTR_IN_61
MLB0_MLBSS_MLB_AHB_INT_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_62
MLB0_MLBSS_MLB_AHB_INT_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_62
MLB0_MLBSS_MLB_AHB_INT_OUT_1	R5FSS0_CORE0_INTR_IN_62
MLB0_MLBSS_MLB_AHB_INT_OUT_1	R5FSS0_CORE1_INTR_IN_62
MLB0_MLBSS_MLB_AHB_INT_OUT_1	R5FSS1_CORE0_INTR_IN_62
MLB0_MLBSS_MLB_AHB_INT_OUT_1	R5FSS1_CORE1_INTR_IN_62
MLB0_MLBSS_MLB_INT_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_60
MLB0_MLBSS_MLB_INT_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_60
MLB0_MLBSS_MLB_INT_OUT_0	R5FSS0_CORE0_INTR_IN_60
MLB0_MLBSS_MLB_INT_OUT_0	R5FSS0_CORE1_INTR_IN_60
MLB0_MLBSS_MLB_INT_OUT_0	R5FSS1_CORE0_INTR_IN_60
MLB0_MLBSS_MLB_INT_OUT_0	R5FSS1_CORE1_INTR_IN_60

Table 10-54. I2C Out Interrupts

Instance	OUT Interrupt	Connected To
I2C0	I2C0_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_193
	I2C0_POINTRPEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_193
	I2C0_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_193
	I2C0_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_193
I2C1	I2C1_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_194
	I2C1_POINTRPEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_194
	I2C1_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_194
	I2C1_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_194
I2C2	I2C2_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_195
	I2C2_POINTRPEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_195
	I2C2_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_195
	I2C2_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_195
I2C3	I2C3_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_196
	I2C3_POINTRPEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_196
	I2C3_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_196
	I2C3_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_196
I2C4	I2C4_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_197
	I2C4_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_197
	I2C4_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_197
	I2C4_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_197
	I2C4_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_197
I2C5	I2C5_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_198
	I2C5_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_198
	I2C5_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_198
	I2C5_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_198
	I2C5_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_198

Table 10-54. I2C Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
I2C6	I2C6_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_199
	I2C6_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_199
	I2C6_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_199
	I2C6_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_199
	I2C6_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_199
WKUP_I2C0	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_143
	WKUP_I2C0_POINTRPEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_197
	WKUP_I2C0_POINTRPEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_197
	WKUP_I2C0_POINTRPEND_OUT_0	R5FSS0_CORE0_INTR_IN_190
	WKUP_I2C0_POINTRPEND_OUT_0	R5FSS0_CORE1_INTR_IN_190
	WKUP_I2C0_POINTRPEND_OUT_0	R5FSS1_CORE0_INTR_IN_190
	WKUP_I2C0_POINTRPEND_OUT_0	R5FSS1_CORE1_INTR_IN_190
	WKUP_I2C0_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_190

Table 10-55. MSRAM Out Interrupts

Instance	OUT Interrupt	Connected To
MSRAM_1MB0	MSRAM_1MB0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_184
	MSRAM_1MB0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_185
MSRAM_1MB1	MSRAM_1MB1_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_186
	MSRAM_1MB1_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_187
MSRAM_1MB2	MSRAM_1MB2_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_188
	MSRAM_1MB2_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_189
MSRAM_1MB3	MSRAM_1MB3_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_190
	MSRAM_1MB3_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_191

Table 10-55. MSRAM Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
MSRAM_1MB4	MSRAM_1MB4_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_215
	MSRAM_1MB4_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_216
MSRAM_1MB5	MSRAM_1MB5_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_217
	MSRAM_1MB5_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_218

Table 10-56. PLLFRACF2_SSMOD Out Interrupts

Instance	OUT Interrupt	Connected To
pllfracf2_ssmod_16fft0	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_54
	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_128
pllfracf2_ssmod_16fft1	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_55
	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_129
pllfracf2_ssmod_16fft14	PLLFRACF2_SSMOD_16FFT14_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_58
	PLLFRACF2_SSMOD_16FFT14_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_132
pllfracf2_ssmod_16fft15	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_59
	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_133
pllfracf2_ssmod_16fft2	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_56
	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_130
pllfracf2_ssmod_16fft4	PLLFRACF2_SSMOD_16FFT4_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_57
	PLLFRACF2_SSMOD_16FFT4_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_131
pllfracf2_ssmod_16fft7	PLLFRACF2_SSMOD_16FFT7_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_61
	PLLFRACF2_SSMOD_16FFT7_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_18
MCU_pllfracf2_ssmod_16fft0	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_63
	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_134

Table 10-57. PSRAM Out Interrupts

Instance	OUT Interrupt	Connected To
PSRAMECC0	PSRAMECC0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_29
	PSRAMECC0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_90
WKUP_psram2kx32e0	WKUP_PSRAM2KX32E0_ECC_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_44
	WKUP_PSRAM2KX32E0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_16
	WKUP_PSRAM2KX32E0_ECC_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_45
	WKUP_PSRAM2KX32E0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_17
WKUP_PSRAMECC_8K0	WKUP_PSRAMECC_8K0_ECC_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_42
	WKUP_PSRAMECC_8K0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_8
	WKUP_PSRAMECC_8K0_ECC_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_43
	WKUP_PSRAMECC_8K0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_13

Table 10-58. RL2 Out Interrupts

OUT Interrupt	Connected To
RL2_0_ERR_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_261
RL2_0_ERR_LVL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_261
RL2_0_ERR_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_90
RL2_0_ERR_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_49
RL2_0_ERR_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_90
RL2_0_ERR_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_90
RL2_0_ERR_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_90

Table 10-58. RL2 Out Interrupts (continued)

OUT Interrupt	Connected To
RL2_0_ERR_LVL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_261
RL2_0_ERR_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_90
RL2_0_ERR_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_49
RL2_0_ERR_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_90
RL2_0_ERR_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_90
RL2_0_ERR_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_90
RL2_2_ERR_LVL_OUT_0	RL2_2_ERR_LVL_OUT_0
RL2_2_ERR_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_262
RL2_2_ERR_LVL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_262
RL2_2_ERR_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_91
RL2_2_ERR_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_91
RL2_2_ERR_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_49
RL2_2_ERR_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_91
RL2_3_ERR_LVL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_263
RL2_3_ERR_LVL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_263
RL2_3_ERR_LVL_OUT_0	R5FSS0_CORE0_INTR_IN_92
RL2_3_ERR_LVL_OUT_0	R5FSS0_CORE1_INTR_IN_92
RL2_3_ERR_LVL_OUT_0	R5FSS1_CORE0_INTR_IN_92
RL2_3_ERR_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_49
RL2_3_ERR_LVL_OUT_0	R5FSS1_CORE1_INTR_IN_92

Table 10-59. WKUP_RTCSS0 Out Interrupts

OUT Interrupt	Connected To
WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_132
WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_132
WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	R5FSS0_CORE0_INTR_IN_97
WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	R5FSS0_CORE1_INTR_IN_97
WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	R5FSS1_CORE0_INTR_IN_97
WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	R5FSS1_CORE1_INTR_IN_97
WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_97

Table 10-60. RTI Out Interrupts

Instance	OUT Interrupt	Connected To
RTI4	RTI4_INTR_WWD_OUT_0	C7X256V0_CLEC_SOC_EVENTS_IN_IN_4
	RTI4_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_252
	RTI4_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_252
	RTI4_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_252
RTI5	RTI5_INTR_WWD_OUT_0	C7X256V1_CLEC_SOC_EVENTS_IN_IN_4
	RTI5_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_253

Table 10-60. RTI Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	RTI5_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_253
	RTI5_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_253
RTI0	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_224
	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_224
	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_224
	RTI0_INTR_WWD_OUT_0	R5FSS0_CORE0_INTR_IN_30
RTI1	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_225
	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_225
	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_225
	RTI1_INTR_WWD_OUT_0	R5FSS0_CORE1_INTR_IN_30
RTI2	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_241
	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_241
	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_241
	RTI2_INTR_WWD_OUT_0	R5FSS1_CORE0_INTR_IN_30
RTI3	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_242
	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_242
	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_242
	RTI3_INTR_WWD_OUT_0	R5FSS1_CORE1_INTR_IN_30
WKUP_RTI0	WKUP_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_86
	WKUP_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_86
	WKUP_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_86
	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_227
	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_227
	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_227
	WKUP_RTI0_INTR_WWD_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_30

Table 10-61. SA_UL Out Interrupts

Instance	OUT Interrupt	Connected To
SA3_SS0_DMSS_ECCAGGR_0	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_118
	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_119

Table 10-61. SA_UL Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
SA3_SS0_INTAGGR_0	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_112
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4	C7X256V1_CLEC_GIC_SPI_IN_112
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_113
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5	C7X256V1_CLEC_GIC_SPI_IN_113
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_7
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7	R5FSS0_CORE0_INTR_IN_7
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7	R5FSS0_CORE1_INTR_IN_7
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7	R5FSS1_CORE0_INTR_IN_7
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7	R5FSS1_CORE1_INTR_IN_7
SA3_SS0_SA_UL_0	SA3_SS0_SA_UL_0_SA_UL_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_120
	SA3_SS0_SA_UL_0_SA_UL_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_121
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_160
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_160
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	R5FSS0_CORE0_INTR_IN_16
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	R5FSS0_CORE1_INTR_IN_16
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	R5FSS1_CORE0_INTR_IN_16
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	R5FSS1_CORE1_INTR_IN_16
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_16
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_161
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_161
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	R5FSS0_CORE0_INTR_IN_17
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	R5FSS0_CORE1_INTR_IN_17
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	R5FSS1_CORE0_INTR_IN_17
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	R5FSS1_CORE1_INTR_IN_17
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_17

Table 10-62. Efuse Out Interrupts

OUT Interrupt	Connected To
EFUSE0_EFC_ERROR_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_131
EFUSE0_EFC_ERROR_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_131

Table 10-62. Efuse Out Interrupts (continued)

OUT Interrupt	Connected To
EFUSE0_EFC_ERROR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_25
EFUSE0_EFC_ERROR_OUT_0	R5FSS0_CORE0_INTR_IN_98
EFUSE0_EFC_ERROR_OUT_0	R5FSS0_CORE1_INTR_IN_98
EFUSE0_EFC_ERROR_OUT_0	R5FSS1_CORE0_INTR_IN_98
EFUSE0_EFC_ERROR_OUT_0	R5FSS1_CORE1_INTR_IN_98
EFUSE0_EFC_ERROR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_98

Table 10-63. Debugss Out Interrupts

OUT Interrupt	Connected To
DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_201
DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_201
DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_201
DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_201
DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_201
DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_201
DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_201
DEBUGSS0_CTM_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_202
DEBUGSS0_CTM_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_202
DEBUGSS0_CTM_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_202
DEBUGSS0_CTM_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_202
DEBUGSS0_CTM_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_202
DEBUGSS0_CTM_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_202
DEBUGSS0_CTM_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_202
DEBUGSS0_DAVDMA_LEVEL_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_27
DEBUGSS0_DAVDMA_LEVEL_OUT_0	USB0_TRACE_INEP_PKT_BUFF_AVAIL_IN_0

Table 10-64. WKUP_PSC0 Out Interrupts

OUT Interrupt	Connected To
WKUP_PSC0_PSC_ALLINT_OUT_0	R5FSS0_CORE0_INTR_IN_145
WKUP_PSC0_PSC_ALLINT_OUT_0	R5FSS0_CORE1_INTR_IN_145
WKUP_PSC0_PSC_ALLINT_OUT_0	R5FSS1_CORE0_INTR_IN_145
WKUP_PSC0_PSC_ALLINT_OUT_0	R5FSS1_CORE1_INTR_IN_145
WKUP_PSC0_PSC_ALLINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_145

Table 10-65. POK Out Interrupts

Instance	OUT Interrupt	Connected To
MCU_PRG_MCU_5POKS0	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_64

Table 10-65. POK Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_64
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_64
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT2_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT0_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT1_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT2_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_72
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_72
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_72
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_76
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_76
	MCU_PRG_MCU_5POKS0_POK_PGOOD	WKUP_ESM0_ESM_PLS_EVENT2_IN_76

Table 10-65. POK Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
MCU_PRG_MCU0	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_79

Table 10-65. POK Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT2_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT0_IN_82
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT1_IN_82
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT2_IN_82

Table 10-66. MCSPI Out Interrupts

Instance	OUT Interrupt	Connected To
MCSPI0	MCSPI0_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_0_RX_IN_0
	MCSPI0_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_0_RX_IN_1
	MCSPI0_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_0_RX_IN_2
	MCSPI0_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_0_RX_IN_3
	MCSPI0_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_0_TX_IN_0
	MCSPI0_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_0_TX_IN_1
	MCSPI0_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_0_TX_IN_2
	MCSPI0_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_0_TX_IN_3
	MCSPI0_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_204
	MCSPI0_INTR_SPI_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_204
	MCSPI0_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_204
	MCSPI0_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_204
	MCSPI0_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_204
	MCSPI0_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_204
	MCSPI0_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_204
MCSPI1	MCSPI1_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_1_RX_IN_0
	MCSPI1_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_1_RX_IN_1
	MCSPI1_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_1_RX_IN_2
	MCSPI1_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_1_RX_IN_3
	MCSPI1_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_1_TX_IN_0

Table 10-66. MCSPI Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCSPI1_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_1_TX_IN_1
	MCSPI1_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_1_TX_IN_2
	MCSPI1_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_1_TX_IN_3
	MCSPI1_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_205
	MCSPI1_INTR_SPI_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_205
	MCSPI1_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_205
	MCSPI1_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_205
MCSPI2	MCSPI2_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_2_RX_IN_0
	MCSPI2_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_2_RX_IN_1
	MCSPI2_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_2_RX_IN_2
	MCSPI2_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_2_RX_IN_3
	MCSPI2_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_2_TX_IN_0
	MCSPI2_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_2_TX_IN_1
	MCSPI2_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_2_TX_IN_2
	MCSPI2_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_2_TX_IN_3
	MCSPI2_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_206
	MCSPI2_INTR_SPI_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_206
	MCSPI2_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_206
	MCSPI2_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_206
MCSPI3	MCSPI3_DMA_READ_EVENT_OUT_0	PDMA4_SPI_MAIN_3_RX_IN_0
	MCSPI3_DMA_READ_EVENT_OUT_1	PDMA4_SPI_MAIN_3_RX_IN_1
	MCSPI3_DMA_READ_EVENT_OUT_2	PDMA4_SPI_MAIN_3_RX_IN_2
	MCSPI3_DMA_READ_EVENT_OUT_3	PDMA4_SPI_MAIN_3_RX_IN_3
	MCSPI3_DMA_WRITE_EVENT_OUT_0	PDMA4_SPI_MAIN_3_TX_IN_0

Table 10-66. MCSPI Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	MCSPI3_DMA_WRITE_EVENT_OUT_1	PDMA4_SPI_MAIN_3_TX_IN_1
	MCSPI3_DMA_WRITE_EVENT_OUT_2	PDMA4_SPI_MAIN_3_TX_IN_2
	MCSPI3_DMA_WRITE_EVENT_OUT_3	PDMA4_SPI_MAIN_3_TX_IN_3
	MCSPI3_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_207
	MCSPI3_INTR_SPI_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_207
	MCSPI3_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_207
	MCSPI3_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_207
	MCSPI3_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_207
	MCSPI3_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_207
	MCSPI3_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_207
MCSPI4	MCSPI4_DMA_READ_EVENT_OUT_0	PDMA4_SPI_MAIN_4_RX_IN_0
	MCSPI4_DMA_READ_EVENT_OUT_1	PDMA4_SPI_MAIN_4_RX_IN_1
	MCSPI4_DMA_READ_EVENT_OUT_2	PDMA4_SPI_MAIN_4_RX_IN_2
	MCSPI4_DMA_READ_EVENT_OUT_3	PDMA4_SPI_MAIN_4_RX_IN_3
	MCSPI4_DMA_WRITE_EVENT_OUT_0	PDMA4_SPI_MAIN_4_TX_IN_0
	MCSPI4_DMA_WRITE_EVENT_OUT_1	PDMA4_SPI_MAIN_4_TX_IN_1
	MCSPI4_DMA_WRITE_EVENT_OUT_2	PDMA4_SPI_MAIN_4_TX_IN_2
	MCSPI4_DMA_WRITE_EVENT_OUT_3	PDMA4_SPI_MAIN_4_TX_IN_3
	MCSPI4_INTR_SPI_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_208
	MCSPI4_INTR_SPI_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_208
	MCSPI4_INTR_SPI_OUT_0	R5FSS0_CORE0_INTR_IN_208
	MCSPI4_INTR_SPI_OUT_0	R5FSS0_CORE1_INTR_IN_208
	MCSPI4_INTR_SPI_OUT_0	R5FSS1_CORE0_INTR_IN_208
	MCSPI4_INTR_SPI_OUT_0	R5FSS1_CORE1_INTR_IN_208
	MCSPI4_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_208

Table 10-67. UART Out Interrupts

Instance	OUT Interrupt	Connected To
UART0	UART0_USART_DMA_OUT_0	PDMA1_USART_MAIN_0_TX_IN_0
	UART0_USART_DMA_OUT_1	PDMA1_USART_MAIN_0_RX_IN_0
	UART0_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_210
	UART0_USART_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_210
	UART0_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_210

Table 10-67. UART Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	UART0_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_210
	UART0_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_210
	UART0_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_210
	UART0_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_210
UART1	UART1_USART_DMA_OUT_0	PDMA1_USART_MAIN_1_TX_IN_0
	UART1_USART_DMA_OUT_1	PDMA1_USART_MAIN_1_RX_IN_0
	UART1_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_211
	UART1_USART_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_211
	UART1_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_211
	UART1_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_211
	UART1_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_211
	UART1_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_211
	UART1_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_211
UART2	UART2_USART_DMA_OUT_0	PDMA1_USART_MAIN_2_TX_IN_0
	UART2_USART_DMA_OUT_1	PDMA1_USART_MAIN_2_RX_IN_0
	UART2_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_212
	UART2_USART_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_212
	UART2_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_212
	UART2_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_212
	UART2_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_212
	UART2_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_212
	UART2_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_212
UART3	UART3_USART_DMA_OUT_0	PDMA1_USART_MAIN_3_TX_IN_0
	UART3_USART_DMA_OUT_1	PDMA1_USART_MAIN_3_RX_IN_0
	UART3_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_213
	UART3_USART_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_213
	UART3_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_213
	UART3_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_213

Table 10-67. UART Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	UART3_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_213
	UART3_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_213
	UART3_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_213
UART4	UART4_USART_DMA_OUT_0	PDMA1_USART_MAIN_4_TX_IN_0
	UART4_USART_DMA_OUT_1	PDMA1_USART_MAIN_4_RX_IN_0
	UART4_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_214
	UART4_USART_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_214
	UART4_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_214
	UART4_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_214
	UART4_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_214
	UART4_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_214
	UART4_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_214
UART5	UART5_USART_DMA_OUT_0	PDMA1_USART_MAIN_5_TX_IN_0
	UART5_USART_DMA_OUT_1	PDMA1_USART_MAIN_5_RX_IN_0
	UART5_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_215
	UART5_USART_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_215
	UART5_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_215
	UART5_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_215
	UART5_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_215
	UART5_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_215
	UART5_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_215
UART6	UART6_USART_DMA_OUT_0	PDMA1_USART_MAIN_6_TX_IN_0
	UART6_USART_DMA_OUT_1	PDMA1_USART_MAIN_6_RX_IN_0
	UART6_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_216
	UART6_USART_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_216
	UART6_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_216
	UART6_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_216
	UART6_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_216

Table 10-67. UART Out Interrupts (continued)

Instance	OUT Interrupt	Connected To
	UART6_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_216
	UART6_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_216
WKUP_UART0	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_144
	WKUP_UART0_USART_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_218
	WKUP_UART0_USART_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_218
	WKUP_UART0_USART_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_219
	WKUP_UART0_USART_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_219
	WKUP_UART0_USART_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_219
	WKUP_UART0_USART_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_219
	WKUP_UART0_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_219

Table 10-68. USB0 Out Interrupts

OUT Interrupt	Connected To
USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_35
USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_111
USB0_HOST_SYSTEM_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_32
USB0_IRQ_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_220
USB0_IRQ_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_220
USB0_IRQ_OUT_0	R5FSS0_CORE0_INTR_IN_220
USB0_IRQ_OUT_0	R5FSS0_CORE1_INTR_IN_220
USB0_IRQ_OUT_0	R5FSS1_CORE0_INTR_IN_220
USB0_IRQ_OUT_0	R5FSS1_CORE1_INTR_IN_220
USB0_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_220
USB0_IRQ_OUT_1	C7X256V0_CLEC_GIC_SPI_IN_221
USB0_IRQ_OUT_1	C7X256V1_CLEC_GIC_SPI_IN_221
USB0_IRQ_OUT_1	R5FSS0_CORE0_INTR_IN_221
USB0_IRQ_OUT_1	R5FSS0_CORE1_INTR_IN_221
USB0_IRQ_OUT_1	R5FSS1_CORE0_INTR_IN_221
USB0_IRQ_OUT_1	R5FSS1_CORE1_INTR_IN_221
USB0_IRQ_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_221
USB0_IRQ_OUT_2	C7X256V0_CLEC_GIC_SPI_IN_222
USB0_IRQ_OUT_2	C7X256V1_CLEC_GIC_SPI_IN_222
USB0_IRQ_OUT_2	R5FSS0_CORE0_INTR_IN_222
USB0_IRQ_OUT_2	R5FSS0_CORE1_INTR_IN_222

Table 10-68. USB0 Out Interrupts (continued)

OUT Interrupt	Connected To
USB0_IRQ_OUT_2	R5FSS1_CORE0_INTR_IN_222
USB0_IRQ_OUT_2	R5FSS1_CORE1_INTR_IN_222
USB0_IRQ_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_222
USB0_IRQ_OUT_3	C7X256V0_CLEC_GIC_SPI_IN_223
USB0_IRQ_OUT_3	C7X256V1_CLEC_GIC_SPI_IN_223
USB0_IRQ_OUT_3	R5FSS0_CORE0_INTR_IN_223
USB0_IRQ_OUT_3	R5FSS0_CORE1_INTR_IN_223
USB0_IRQ_OUT_3	R5FSS1_CORE0_INTR_IN_223
USB0_IRQ_OUT_3	R5FSS1_CORE1_INTR_IN_223
USB0_IRQ_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_223
USB0_IRQ_OUT_4	C7X256V0_CLEC_GIC_SPI_IN_224
USB0_IRQ_OUT_4	C7X256V1_CLEC_GIC_SPI_IN_224
USB0_IRQ_OUT_4	R5FSS0_CORE0_INTR_IN_224
USB0_IRQ_OUT_4	R5FSS0_CORE1_INTR_IN_224
USB0_IRQ_OUT_4	R5FSS1_CORE0_INTR_IN_224
USB0_IRQ_OUT_4	R5FSS1_CORE1_INTR_IN_224
USB0_IRQ_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_224
USB0_IRQ_OUT_5	C7X256V0_CLEC_GIC_SPI_IN_225
USB0_IRQ_OUT_5	C7X256V1_CLEC_GIC_SPI_IN_225
USB0_IRQ_OUT_5	R5FSS0_CORE0_INTR_IN_225
USB0_IRQ_OUT_5	R5FSS0_CORE1_INTR_IN_225
USB0_IRQ_OUT_5	R5FSS1_CORE0_INTR_IN_225
USB0_IRQ_OUT_5	R5FSS1_CORE1_INTR_IN_225
USB0_IRQ_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_225
USB0_IRQ_OUT_6	C7X256V0_CLEC_GIC_SPI_IN_226
USB0_IRQ_OUT_6	C7X256V1_CLEC_GIC_SPI_IN_226
USB0_IRQ_OUT_6	R5FSS0_CORE0_INTR_IN_226
USB0_IRQ_OUT_6	R5FSS0_CORE1_INTR_IN_226
USB0_IRQ_OUT_6	R5FSS1_CORE0_INTR_IN_226
USB0_IRQ_OUT_6	R5FSS1_CORE1_INTR_IN_226
USB0_IRQ_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_226
USB0_IRQ_OUT_7	C7X256V0_CLEC_GIC_SPI_IN_227
USB0_IRQ_OUT_7	C7X256V1_CLEC_GIC_SPI_IN_227
USB0_IRQ_OUT_7	R5FSS0_CORE0_INTR_IN_227

Table 10-68. USB0 Out Interrupts (continued)

OUT Interrupt	Connected To
USB0_IRQ_OUT_7	R5FSS0_CORE1_INTR_IN_227
USB0_IRQ_OUT_7	R5FSS1_CORE0_INTR_IN_227
USB0_IRQ_OUT_7	R5FSS1_CORE1_INTR_IN_227
USB0_IRQ_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_227
USB0_MISC_LEVEL_OUT_0	C7X256V0_CLEC_GIC_SPI_IN_228
USB0_MISC_LEVEL_OUT_0	C7X256V1_CLEC_GIC_SPI_IN_228
USB0_MISC_LEVEL_OUT_0	R5FSS0_CORE0_INTR_IN_228
USB0_MISC_LEVEL_OUT_0	R5FSS0_CORE1_INTR_IN_228
USB0_MISC_LEVEL_OUT_0	R5FSS1_CORE0_INTR_IN_228
USB0_MISC_LEVEL_OUT_0	R5FSS1_CORE1_INTR_IN_228
USB0_MISC_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_228
USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_61

11 Data Movement Architecture

This chapter describes the data movement architecture of the device.

11.1 Data Movement Architecture Overview

This chapter is a high-level summary of the data movement architecture implemented in the device.

11.1.1 Overview

The primary goal of the device Data Movement Architecture and related Subsystems is to ensure that data can be efficiently transferred from a producer to a consumer while meeting the real time requirements of the system can be met.

The Data Movement Subsystem (DMSS) aims to facilitate direct memory access (DMA) and provides a consistent Application Programming Interface (API) to the host software.

Data movement tasks are commonly offloaded from the host processor to peripheral hardware to increase system performance. Significant performance gains may result from careful design of the interface between the host software and the underlying acceleration hardware. In networking applications, packet transmission and reception are critical tasks. In general purpose compute, ping pong buffer prefetch and store are critical tasks as well as general mis-aligned block copy operations.

The design goals for the device Data Movement Architecture and are as follows:

- Minimize cost
- Minimize host overhead
- Maximize memory use efficiency
- Maximize bus burst efficiency
- Maximize symmetry between transmit/receive operations
- Maximize scalability for number of connections / buffer sizes / queue sizes / protocols supported
- Minimize protocol specific features
- Minimize complexity

11.1.1.1 Ring Accelerator (RINGACC)

The ring accelerator (RINGACC or RA) is a hardware module that is responsible for accelerating management of various types of queues in the system. The RINGACC accelerates passing of packets between a producer and consumer in normal system memory (including cached memory). The RINGACC is capable of accelerating the read/write pointer maintenance and occupancy tracking operations.

The ring accelerator operates like a bus infrastructure bridge in that it passes transactions through it between a source and destination interface. As transactions are passed, the RINGACC modifies the address, byte count, and transaction identifiers and internally updates the occupancies/pointers.

Each queue that the RINGACC provides can operate in either exposed-ring-mode or private-queue-mode.

- The exposed ring mode allows software to directly access the underlying ring structure to add or remove items from the tail or head of the ring respectively. Whenever items are added or removed from a ring, the host software is required to write to a corresponding doorbell register (RINGRT[a]_RT_DB) to increment or decrement the ring occupancy. When using the exposed ring mode, no proxy is required between the software and the RINGACC but all queue add operations require a memory fence to be performed to ensure that the data has landed in a snoopable cache before the doorbell register is written.
- The private queue mode provides an abstract view of the ring so that the host software does not need to know the actual physical address location or current read or write indexes of the ring. The private queue mode provides a memory window for each ring which when written redirects the write to the address pointed to by the write pointer and when read redirects the read to the address pointed to by the read pointer. The same address range is always used to push or pop elements from a given queue.

Rings are an implementation of a logical queue with the following limitations:

- Each ring has a finite size. When rings are used in exposed ring mode the following conditions apply:
  - A separate operation is required to write/read the contents of a ring and to update the occupancy of the ring

- It is not straightforward to allow multiple producers to write to a ring or multiple consumers to read from a ring. Additional synchronization and pointer passing is required since rings require software to manage one of the pointers for the queue.
- An exposed ring cannot be used when software or hardware needs to both read and write the same queue (such as for a DMA RX free queue where errors can have the DMA write the element back onto the same RX free queue). Since software owns one side of the pointers and hardware owns the other, they cannot be kept coherent if either side needs to update either at any time.

The RINGACC allows each ring to be configured to a different primary element size. Element sized chunks of data are placed onto and retrieved from rings when queuing or de-queueing occurs. Element sizes can be as small as 4 bytes or as large as 256 bytes.

11.1.1.2 Secure Proxy (SEC_PROXY)

A proxy provides a mechanism for software to access the RINGACC coherently when the processor does not support large bursts. The RINGACC requires a single burst for each operation so that it maintains atomicity and coherence by relying on the atomicity of the bursts on the bus interconnect fabric, since it only delivers a single burst to the RINGACC before the next. Since processors are usually limited in the size of a burst they can deliver natively, such as 32 to 128 bits, they cannot be used directly with the data access region of the RINGACC for larger element sizes. The proxy solves this gap by providing a temporary space for the software to form a larger burst of data before it is sent to the RINGACC. The proxy allows smaller processor accesses to the data and only forwards to the RINGACC when the entire data burst is complete, as directed by the software.

Each proxy hardware can support multiple threads of software (whether on the same or different processors) operating on bursts at the same time, and they do not interfere with each other, as long as each thread of software only operates on its thread in the proxy. Each proxy thread also supports access to any RINGACC queue via different offsets similar to how the RINGACC provides access to the queues via different offsets.

A special version of a proxy is the Secure Proxy that provides secured access to RINGACC queues for communication to the security initiator of the system. It provides basically the same function as a normal proxy. The data burst size is fixed for message sizes to the security initiator, so there is no support for all the element sizes of the RINGACC. The security initiator locks down the RINGACC queue to access and direction for each proxy thread so that the software cannot access anything they shouldn’t, so the software only sees a single queue (unlike the normal proxy), and any attempts to access another queue or access it in violation of how the security initiator defined and an error will be flagged. This allows for a much more controlled setup for passing messages to the security initiator.

11.1.1.3 Interrupt Aggregator (INTAGGR)

The interrupt aggregator (INTAGGR or INTA) is a hardware module which provides a persistent view of the real time status of various DMA components within the overall SoC DMA system. The main function of the module is to convert between 'global events' (assertion and de-assertion events transmitted on the event-transport-lane bus) and 'local events' (level sensitive signals on output, and level or edge sensitive signals on input).

The INTA block provides the following functions:

- Conversion of local event signal lines into global events
- Performing an 'Y-split' operation of global events
- Counting global events
- Steering and aggregation of global events into specified bit positions in one of N interrupt cause registers
- SoC interrupt-architecture-compliant set/clear and mask set/clear functionality to cover interrupt cause registers

11.1.1.4 Packet DMA (PKTDMA)

The PKTDMA module supports the transmission and reception of various packet types. The PKTDMA is architected to facilitate the segmentation and reassembly of DMA data structure compliant packets to/from smaller data blocks that are natively compatible with the specific requirements of each connected peripheral. Multiple Tx and Rx channels are provided within the DMA which allow multiple segmentation or reassembly operations to be ongoing. The DMA controller maintains state information for each of the channels which allows packet segmentation and reassembly operations to be time division multiplexed between channels in order to share the underlying DMA hardware. An internal DMA scheduler is used to control the ordering and rate at which this multiplexing occurs for Transmit operations. The ordering and rate of Receive operations is indirectly controlled by the order in which blocks are pushed into the DMA on the Rx PSI-L interface.

A block diagram of the PKTDMA Controller is shown below:

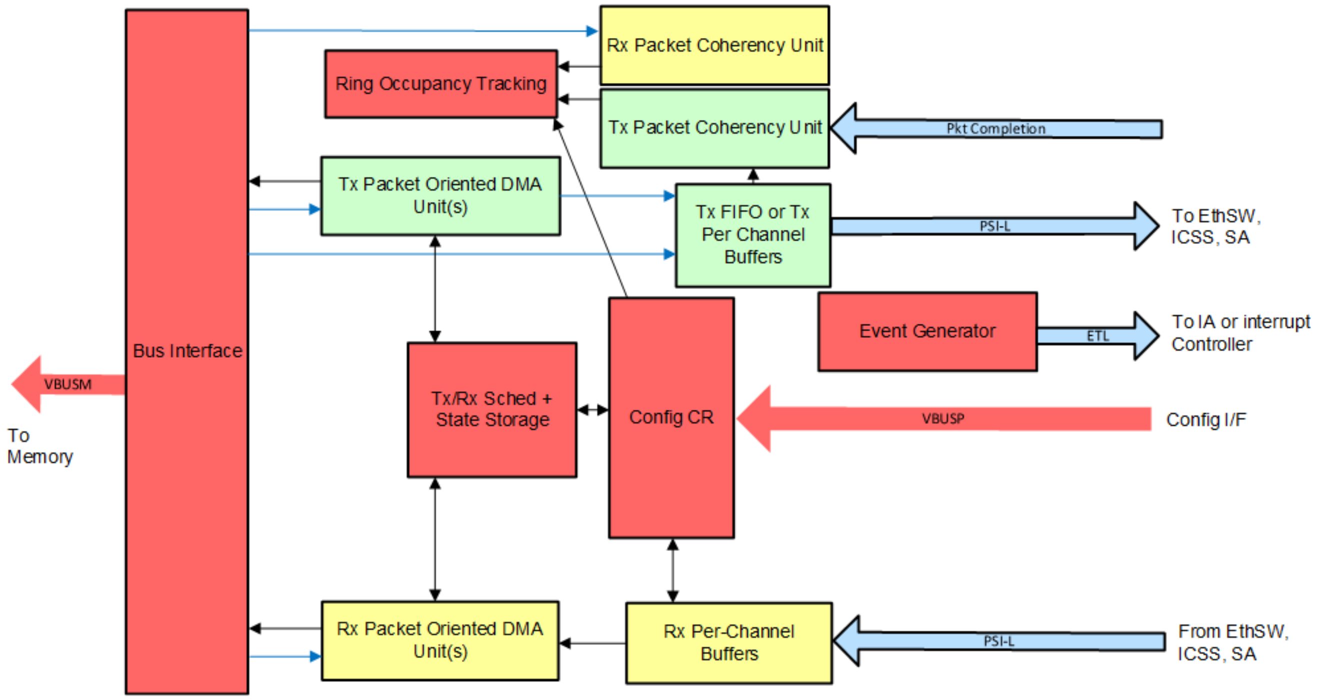


Figure 11-1. PKTDMA Block Diagram

11.1.1.4.1 PKTDMA Submodule Descriptions

11.1.1.4.1.1 Bus Interface Unit

The Bus Interface Unit is responsible for merging and buffering all of the transactions that originate from the various initiator blocks inside the DMA controller into the 4 separate VBUSM initiator interfaces. Arbitration between the blocks to a given VBUSM interface is round robin within a single priority level. A 2 word deep retiming buffer is provided on each sub interface of each provided VBUSM bus.

11.1.1.4.1.2 Config CR

The function of the Config CR is to switch transactions which arrive on the configuration interface to the various configuration targets within the DMA. The Config CR also provides a retiming buffer on the configuration bus primary interface ports.

11.1.1.4.1.3 Configuration Registers

The Configuration Registers block is responsible for monitoring the fullness level of the Tx Per Channel FIFOs, monitoring data transfer work which is pending, maintaining data movement thread state information, arbitrating which channel will be allowed to perform work next, issuing scheduler commands to the Tx PKTDMA core blocks, and writing back the updated state returned from those same DMA core blocks.

The Configuration Registers block is also responsible for providing memory mapped registers for configuration of the Rx DMA functions including the default settings for the free descriptor and destination queues. For modularity and high speed pipelining reasons, the Rx traffic is looped through the Configuration Registers block where the original stream information is merged with information from the configuration registers on its way to the Rx DMA unit module. This prevents the Rx DMA Core from having to spend cycles accessing the channel configuration information for the channel.

11.1.1.4.1.3.1 RX State Mapping

<table>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td colspan="32">sop_descriptor_ptr[35:4]</td></tr>
<tr><td colspan="32">0x80</td></tr>
<tr><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td><td>48</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr>
<tr><td colspan="12">sop_descriptor_ptr[35:4]</td><td colspan="4">sop_descriptor_asel</td><td colspan="16">curr_descriptor_ptr</td></tr>
<tr><td colspan="32">0x84</td></tr>
<tr><td>64</td><td>65</td><td>66</td><td>67</td><td>68</td><td>69</td><td>70</td><td>71</td><td>72</td><td>73</td><td>74</td><td>75</td><td>76</td><td>77</td><td>78</td><td>79</td><td>80</td><td>81</td><td>82</td><td>83</td><td>84</td><td>85</td><td>86</td><td>87</td><td>88</td><td>89</td><td>90</td><td>91</td><td>92</td><td>93</td><td>94</td><td>95</td></tr>
<tr><td colspan="28">curr_descriptor_ptr</td><td colspan="4">curr_descriptor_asel</td></tr>
<tr><td colspan="32">0x88</td></tr>
<tr><td>96</td><td>97</td><td>98</td><td>99</td><td>100</td><td>101</td><td>102</td><td>103</td><td>104</td><td>105</td><td>106</td><td>107</td><td>108</td><td>109</td><td>110</td><td>111</td><td>112</td><td>113</td><td>114</td><td>115</td><td>116</td><td>117</td><td>118</td><td>119</td><td>120</td><td>121</td><td>122</td><td>123</td><td>124</td><td>125</td><td>126</td><td>127</td></tr>
<tr><td colspan="32">curr_buffer_ptr</td></tr>
<tr><td colspan="32">0x8C</td></tr>
<tr><td>128</td><td>129</td><td>130</td><td>131</td><td>132</td><td>133</td><td>134</td><td>135</td><td>136</td><td>137</td><td>138</td><td>139</td><td>140</td><td>141</td><td>142</td><td>143</td><td>144</td><td>145</td><td>146</td><td>147</td><td>148</td><td>149</td><td>150</td><td>151</td><td>152</td><td>153</td><td>154</td><td>155</td><td>156</td><td>157</td><td>158</td><td>159</td></tr>
<tr><td colspan="16">curr_buffer_ptr</td><td colspan="4">curr_buffer_asel</td><td colspan="12">curr_buffer_length</td></tr>
<tr><td colspan="32">0x90</td></tr>
<tr><td>160</td><td>161</td><td>162</td><td>163</td><td>164</td><td>165</td><td>166</td><td>167</td><td>168</td><td>169</td><td>170</td><td>171</td><td>172</td><td>173</td><td>174</td><td>175</td><td>176</td><td>177</td><td>178</td><td>179</td><td>180</td><td>181</td><td>182</td><td>183</td><td>184</td><td>185</td><td>186</td><td>187</td><td>188</td><td>189</td><td>190</td><td>191</td></tr>
<tr><td colspan="10">curr_buffer_length</td><td colspan="22">curr_buffer_offset</td></tr>
<tr><td colspan="32">0x94</td></tr>
<tr><td>192</td><td>193</td><td>194</td><td>195</td><td>196</td><td>197</td><td>198</td><td>199</td><td>200</td><td>201</td><td>202</td><td>203</td><td>204</td><td>205</td><td>206</td><td>207</td><td>208</td><td>209</td><td>210</td><td>211</td><td>212</td><td>213</td><td>214</td><td>215</td><td>216</td><td>217</td><td>218</td><td>219</td><td>220</td><td>221</td><td>222</td><td>223</td></tr>
<tr><td>curr_buffer_eop</td><td colspan="21">pkt_length</td><td>flush</td><td colspan="6">ps_wordcnt</td><td>flowid_is_default</td><td colspan="2">drop_flush</td></tr>
<tr><td colspan="32">0x98</td></tr>
<tr><td>224</td><td>225</td><td>226</td><td>227</td><td>228</td><td>229</td><td>230</td><td>231</td><td>232</td><td>233</td><td>234</td><td>235</td><td>236</td><td>237</td><td>238</td><td>239</td><td>240</td><td>241</td><td>242</td><td>243</td><td>244</td><td>245</td><td>246</td><td>247</td><td>248</td><td>249</td><td>250</td><td>251</td><td>252</td><td>253</td><td>254</td><td>255</td></tr>
<tr><td colspan="7">ps offset</td><td colspan="4">ps_flags</td><td colspan="13">pktid_data</td><td colspan="4">orderid</td><td colspan="3">priority</td><td></td></tr>
<tr><td colspan="32">0x9C</td></tr>
</table>

Table 11-1. RX State Mapping Table

Total Bits	Bits	Register Offset	Field	Description
31 - 0	31 - 0	0x80	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
43 - 32	11 - 0	0x84	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
47 - 44	15 - 12	0x84	sop_descriptor_asel	The asel for descriptor pointer at start of packet
63 - 48	31 - 16	0x84	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
91 -64	27 - 0	0x88	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
95 - 92	31 - 28	0x88	curr_descriptor_asel	The asel of the current descriptor
127 - 96	31 - 0	0x8C	curr_buffer_ptr	The pointer for the current buffer
143 - 128	15 - 0	0x90	curr_buffer_ptr	The pointer for the current buffer
147 - 144	19 - 16	0x90	curr_buffer_asel	The asel for the current buffer
159 - 148	9 - 0	0x90	curr_buffer_length	The length of the current buffer
169 - 160	31 - 20	0x90	curr_buffer_length	The length of the current buffer
191 - 170	31 - 10	0x94	curr_buffer_offset	The offset inside the current buffer
192	0	0x98	curr_buffer_eop	The end of packet flag for the current buffer
213 - 193	21 - 1	0x98	pkt_length	The size of the packet length
214	22	0x98	flush	The packet is being flushed
220 - 215	28 - 23	0x98	ps_wordcnt	protocol specific word count
221	29	0x98	flowid_is_default	Use default flow id
223 - 222	31 - 30	0x98	drop_flush	The flush is a drop condition
230 - 224	6 - 0	0x9C	ps offset	protocol specific offset
234 - 231	10 - 7	0x9C	ps_flags	protocol specific flags
247 - 235	23 - 11	0x9C	pktid_data	The pktid number for scoreboard
251 - 248	27 - 24	0x9C	orderid	The orderid of the packet
254 - 252	30 - 28	0x9C	priority	The priority of the packet

11.1.1.4.1.3.2 TX State Mapping

<table>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td colspan="32">sop_descriptor_ptr[35:4]</td></tr>
<tr><td colspan="32">0x80</td></tr>
<tr><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td><td>48</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr>
<tr><td colspan="12">sop_descriptor_ptr[35:4]</td><td colspan="4">sop_descriptor_asel</td><td colspan="16">curr_descriptor_ptr</td></tr>
<tr><td colspan="32">0x84</td></tr>
<tr><td>64</td><td>65</td><td>66</td><td>67</td><td>68</td><td>69</td><td>70</td><td>71</td><td>72</td><td>73</td><td>74</td><td>75</td><td>76</td><td>77</td><td>78</td><td>79</td><td>80</td><td>81</td><td>82</td><td>83</td><td>84</td><td>85</td><td>86</td><td>87</td><td>88</td><td>89</td><td>90</td><td>91</td><td>92</td><td>93</td><td>94</td><td>95</td></tr>
<tr><td colspan="28">curr_descriptor_ptr</td><td colspan="4">curr_descriptor_asel</td></tr>
<tr><td colspan="32">0x88</td></tr>
<tr><td>96</td><td>97</td><td>98</td><td>99</td><td>100</td><td>101</td><td>102</td><td>103</td><td>104</td><td>105</td><td>106</td><td>107</td><td>108</td><td>109</td><td>110</td><td>111</td><td>112</td><td>113</td><td>114</td><td>115</td><td>116</td><td>117</td><td>118</td><td>119</td><td>120</td><td>121</td><td>122</td><td>123</td><td>124</td><td>125</td><td>126</td><td>127</td></tr>
<tr><td colspan="32">curr_buffer_ptr</td></tr>
<tr><td colspan="32">0x8C</td></tr>
<tr><td>128</td><td>129</td><td>130</td><td>131</td><td>132</td><td>133</td><td>134</td><td>135</td><td>136</td><td>137</td><td>138</td><td>139</td><td>140</td><td>141</td><td>142</td><td>143</td><td>144</td><td>145</td><td>146</td><td>147</td><td>148</td><td>149</td><td>150</td><td>151</td><td>152</td><td>153</td><td>154</td><td>155</td><td>156</td><td>157</td><td>158</td><td>159</td></tr>
<tr><td colspan="16">curr_buffer_ptr</td><td colspan="4">curr_buffer_asel</td><td colspan="12">curr_buffer_length</td></tr>
<tr><td colspan="32">0x90</td></tr>
<tr><td>160</td><td>161</td><td>162</td><td>163</td><td>164</td><td>165</td><td>166</td><td>167</td><td>168</td><td>169</td><td>170</td><td>171</td><td>172</td><td>173</td><td>174</td><td>175</td><td>176</td><td>177</td><td>178</td><td>179</td><td>180</td><td>181</td><td>182</td><td>183</td><td>184</td><td>185</td><td>186</td><td>187</td><td>188</td><td>189</td><td>190</td><td>191</td></tr>
<tr><td colspan="10">curr_buffer_length</td><td colspan="22">curr_buffer_offset</td></tr>
<tr><td colspan="32">0x94</td></tr>
<tr><td>192</td><td>193</td><td>194</td><td>195</td><td>196</td><td>197</td><td>198</td><td>199</td><td>200</td><td>201</td><td>202</td><td>203</td><td>204</td><td>205</td><td>206</td><td>207</td><td>208</td><td>209</td><td>210</td><td>211</td><td>212</td><td>213</td><td>214</td><td>215</td><td>216</td><td>217</td><td>218</td><td>219</td><td>220</td><td>221</td><td>222</td><td>223</td></tr>
<tr><td>curr_buffer_eop</td><td colspan="22">rem_length</td><td>info_present</td><td>truncated_non_eop</td><td colspan="7">psbytes_rem</td></tr>
<tr><td colspan="32">0x98</td></tr>
<tr><td>224</td><td>225</td><td>226</td><td>227</td><td>228</td><td>229</td><td>230</td><td>231</td><td>232</td><td>233</td><td>234</td><td>235</td><td>236</td><td>237</td><td>238</td><td>239</td><td>240</td><td>241</td><td>242</td><td>243</td><td>244</td><td>245</td><td>246</td><td>247</td><td>248</td><td>249</td><td>250</td><td>251</td><td>252</td><td>253</td><td>254</td><td>255</td></tr>
<tr><td>psbytes_rem</td><td colspan="8">psbytes_off</td><td colspan="13">wptr_data</td><td colspan="2">pktid_data</td><td colspan="4">orderid</td><td colspan="3">priority</td><td></td></tr>
<tr><td colspan="32">0x9C</td></tr>
</table>

Table 11-2. TX State Mapping Table

Total Bits	Bits	Register Offset	Field	Description
31 - 0	31 - 0	0x80	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
43 - 32	11 - 0	0x84	sop_descriptor_ptr[35:4]	The descriptor pointer at start of packet
47 - 44	15 - 12	0x84	sop_descriptor_asel	The asel for descriptor pointer at start of packet
63 - 48	31 - 16	0x84	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
91 -64	27 - 0	0x88	curr_descriptor_ptr	The pointer for the current descriptor aligned on 16 byte boundary
95 - 92	31 - 28	0x88	curr_descriptor_asel	The asel of the current descriptor
127 - 96	31 - 0	0x8C	curr_buffer_ptr	The pointer for the current buffer
143 - 128	15 - 0	0x90	curr_buffer_ptr	The pointer for the current buffer
147 - 144	19 - 16	0x90	curr_buffer_asel	The asel for the current buffer
159 - 148	9 - 0	0x90	curr_buffer_length	The length of the current buffer
169 - 160	31 - 20	0x90	curr_buffer_length	The length of the current buffer
191 - 170	31 - 10	0x94	curr_buffer_offset	The offset inside the current buffer
192	0	0x98	curr_buffer_eop	The end of packet flag for the current buffer
214 - 193	22 - 1	0x98	rem_length	The remaining length in the buffer
215	23	0x98	info_present	The packet has info present
216	24	0x98	truncated_non_eop	Eop if packet length is greater than the total buffer length
223 - 217	31 - 25	0x98	psbytes_rem	Number of protocol specific bytes remaining
224	0	0x9C	psbytes_rem	Number of protocol specific bytes remaining
232 - 225	8 - 1	0x9C	psbytes_off	The offset of the protocol specific bytes
245 - 233	21 - 9	0x9C	wptr_data	The current write pointer in the data fifo
247 - 246	23 - 22	0x9C	pktid_data	The pktid number for scoreboard
251 - 248	27 - 24	0x9C	orderid	The orderid of the packet
254 - 252	30 - 28	0x9C	priority	The priority of the packet

11.1.1.4.1.4 Tx Packet DMA Unit

The Tx Packet DMA Unit block implements all of the state machine functionality necessary to implement the KS3 DMA Host Tx protocol. The Tx Packet DMA unit initiates VBUSM transactions in order to read descriptor pointers from the memory mapped Tx ring, read descriptors from memory, and read data from buffers in memory.

11.1.1.4.1.5 Tx Packet Coherency Unit

The Tx Packet Coherency Unit is responsible for ensuring that all control structures and data have been read (and updated if applicable) by the Tx DMA unit(s) and that all previous packets on that channel/flow have also completed prior to incrementing the reverse ring occupancy for the channel/flow.

11.1.1.4.1.6 Tx Per Channel Buffers

The Tx Per Channel Buffers implement a FIFO for each Tx DMA channel that is used for buffering packet control and payload data that has been fetched by the Tx Packet DMA units. The buffers are byte oriented on write so that the data from the DMA units which may not be full words can be packed properly. The buffers are block oriented on read and each Tx (source) channel in the PKTDMA controller maps directly onto a thread in the Tx PSI interface. The Tx Per Channel Buffer block outputs queue fullness information to the Tx Scheduler block which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Tx Per Channel Buffer will initiate transfers to the target whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block will simultaneously monitor the status of all of the threads and will perform a round robin arbitration between the different threads for the use of the Transmit PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer will be included in the arbitration.

11.1.1.4.1.7 Rx Per Channel Buffers

The Rx Per Channel Buffers implement a FIFO for each Rx DMA channel that is used for buffering packet control and payload data that has been pushed into the DMA from the Rx PSI-L interface. The Rx Per Channel Buffers also includes an arbitration unit which determines which Rx DMA channel should be serviced next.

11.1.1.4.1.8 Rx Packet DMA Unit

The Rx Packet DMA Unit block implements all of the state machine functionality necessary to implement the KS3 DMA Rx protocol for Host descriptor types. The Rx Packet DMA Unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read buffer descriptor information, write descriptors to memory, and write data to buffers in memory.

11.1.1.4.1.9 Rx Packet Coherency Unit

The Rx Packet Coherency Unit is responsible for ensuring that all control structures and data have been written by the Rx DMA unit(s) and that all previous packets on that channel/flow have completed prior to incrementing the reverse ring occupancy for the channel/flow. This unit ensures that the ordering of the Packet Descriptor pointer writes to the return queue directly matches the ordering in which those packets were fetched from the Rx free queues. Writes are not considered complete by this unit until the entire write status has been returned for all outstanding transactions for a given packet ID.

11.1.1.4.1.10 Event Handler

The Event Handler block is responsible for generating channel completion and error events.

11.1.1.4.2 Channel Classes

Not all channels within the PKTDMA require the same performance capabilities. Raw bandwidth and latency tolerance requirements will vary greatly between data transfers at various points in the system. Due to area concerns, several different classes of DMA channels are provided in the PKTDMA and are described as follows:

Class Name	Description
Normal Capacity	Provides baseline amount of descriptor prefetch and Tx/Rx control and data buffering. Suitable for most peripheral transfers which are communicating with on-chip memories and DDR
High Capacity	Provides an elevated amount of descriptor prefetch and custom Tx/Rx control and data buffering. Suitable for applications which require moderate per-channel bandwidth with significantly increased latency (ex. Transferring data to/from PCIe)
Ultra-High Capacity	Provides identical descriptor and TR prefetch as High Capacity but with increased Tx data buffering to allow for more read data in flight. Suitable for applications requiring high per-channel bandwidth with significantly increased latency (ex. 16+Gbps transfers to/from PCIe).

PKTDMA instances may provide support for any or all of the above channel classes through design time configuration parameters.

11.1.1.5 Block Copy DMA (BCDMA)

The Block Copy DMA is intended to perform similar functions as an Embedded DMA (EDMA) and the UDMA-P. The BCDMA module moves data from a memory mapped source address set to a corresponding memory mapped address. The BCDMA maintains state information for each of the channels which allows data copy operations to be time division multiplexed between channels in order to share the underlying DMA hardware. An internal DMA scheduler is used to control the ordering and rate at which this multiplexing occurs.

A block diagram of the Block Copy DMA Controller is shown below:

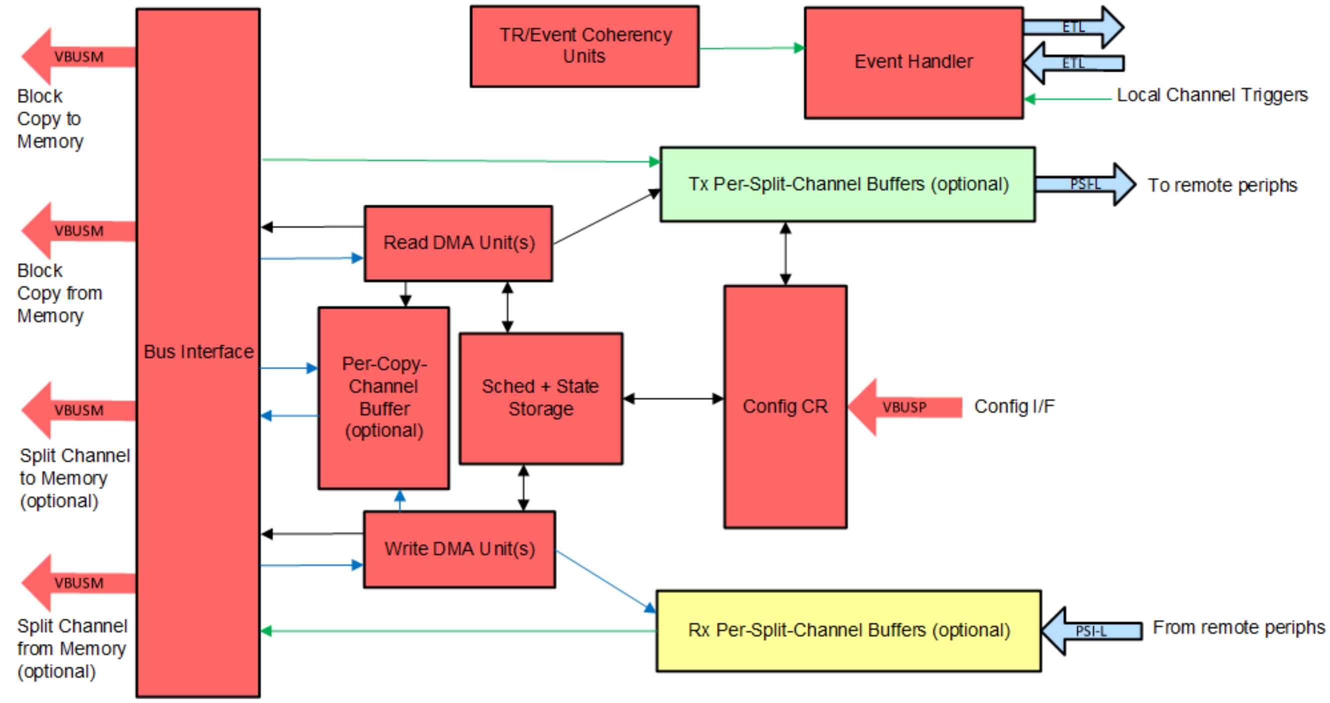


Figure 11-2. Block Copy DMA Block Diagram

11.1.1.5.1 BCDMA Submodule Descriptions

11.1.1.5.1.1 Bus Interface Unit

The Bus Interface Unit is reponsible for merging and buffering all of the transactions that originate from the various controller blocks inside the DMA controller into the 4 seperate VBUSM controller interfaces. Arbitration between the blocks to a given VBUSM interface is round robin within a single priority level. A 2 word deep retiming buffer is provided on each sub interface of each provided VBUSM bus.

11.1.1.5.1.2 Config CR

The function of the Config CR is to switch transactions which arrive on the configuration interface to the various configuration targets within the DMA. The Config CR also provides a retiming buffer on the configuration bus primary interface ports.

11.1.1.5.1.3 Configuration Registers

The Configuration Registers block is responsible for monitoring the fullness level of the Per Channel FIFOs, monitoring data transfer work which is pending, maintaining data movement thread state information, arbitrating which channel will be allowed to perform work next, issuing scheduler commands to the Read and Write DMA units, and writing back the updated state returned from those same DMA units.

The Configuration Registers block is also responsible for providing memory mapped registers for configuration of the DMA channels.

11.1.1.5.1.3.1 BCDMA Mapping Table

Table 11-3 applies to TX, RX and BC Mapping.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
reload_count				waitcomp	event_size		trigger0		trigger0_type		trigger1_type		trigger1_type		spflags				eop	eol			reload_count								
0x80																															
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
tr_dim1																															
0x84																															
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
tr_dim2																															
0x88																															
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
tr_dim3																															
0x8C																															
128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
tr_icnt0																tr_icnt1															
0x90																															
160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
tr_icnt2																tr_icnt3															
0x94																															
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
icnt1																icnt2															
0x98																															
224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
icnt3																rem_icnt0															
0x9C																															
256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
tr_addr																															
0xA0																															
288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
tr_addr				tr_asel				descriptor_ptr																							
0xA4																															
320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
descriptor_ptr												RVSD				curr_index														last_index	
0xA8																															
352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
last_index												nom_elsize			reload_index						curr_wptr										
0xAC																															
384		385		386		387		388		389		390		391		392		393		394		395		396		397		398		399	
curr_wptr				pktid				orderid								priority						trid				evtid				sot	

0xB0

Table 11-3. BCDMA Mapping Table

Total Bits	Bits	Register Offset	Field	Description
3 - 0	3 - 0	0x80	reload_count	
4	4	0x80	waitcomp	
6 - 5	6 - 5	0x80	event_size	
8 - 7	8 - 7	0x80	trigger0	
10 - 9	10 - 9	0x80	trigger0_type	
12 - 11	12 - 11	0x80	trigger1_type	
14 - 13	14 - 13	0x80	trigger1_type	
18 - 15	18 - 15	0x80	spflags	
19	19	0x80	eop	
22 - 20	22 - 20	0x80	eol	
31 - 23	31 - 23	0x80	reload_count	
63 - 32	31 - 0	0x84	tr_dim1	
95 - 64	31 - 0	0x88	tr_dim2	
127 - 96	31 - 0	0x8C	tr_dim3	
143 - 128	15 - 0	0x90	tr_icnt0	
159 - 144	31 - 16	0x90	tr_ictn1	
175 - 160	15 - 0	0x94	tr_ictn2	
191 - 176	31 - 16	0x94	tr_icnt3	
207 - 192	15 - 0	0x98	icnt1	
223 - 208	31 - 16	0x98	icnt2	
239 - 224	15 - 0	0x9C	icnt3	
255 - 240	31 - 16	0x9C	rem_icnt0	
287 - 256	31 - 0	0xA0	tr_addr	
291 - 288	3 - 0	0xA4	tr_addr	
295 - 292	7 - 4	0xA4	tr_asel	
319 - 296	31 - 8	0xA4	descriptor_ptr	
331 - 320	11 - 0	0xA8	descriptor_ptr	
349 - 336	29 - 16	0xA8	curr_index	
363 - 350	11 - 30	0xA8	last_index	
366 - 364	14 - 12	0xAC	nom_elsize	
372 - 367	20 - 15	0xAC	reload_index	
385 - 373	1 - 21	0xAC	curr_wptr	
387 - 386	3 - 2	0xB0	pktid	
391 - 388	7 - 4	0xB0	orderid	
394 - 392	10 - 8	0xB0	priority	
396 - 395	12 - 11	0xB0	trid	
398 - 397	14 - 13	0xB0	evtid	

Table 11-3. BCDMA Mapping Table (continued)

Total Bits	Bits	Register Offset	Field	Description
399	15	0xB0	sot	

11.1.1.5.1.4 Read Unit(s)

The Read Units implement all of the state machine functionality necessary to perform the read transfers defined in the SW supplied Transfer Request records. The read DMA unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read descriptors, Transfer Request records, and payload data from memory.

11.1.1.5.1.5 TR Coherency Unit

The TR Coherency Unit is responsible for ensuring that all control structures and data have been read (and updated if applicable) by the BCDMA unit(s) and all prior TRs have completed prior to incrementing the reverse ring occupancy for the flow/channel.

11.1.1.5.1.6 Per-Copy-Channel Buffers

The Per-Copy-Channel Buffers implement a FIFO for each BCDMA generic block copy channel and is used for buffering payload data that has been fetched by read DMA unit modules. The write DMA units issue write transfers from the Per Channel Buffers to specified addresses in memory. The buffers are byte oriented on both write and read so that the data from the DMA units which may not be full words can be packed and unpacked properly. This unit is optional and is only present if one or more generic block copy channels are configured in the BCDMA instance.

11.1.1.5.1.7 Tx Per-Split-Channel Buffers

The Tx Per-Split-Channel Buffers implement a FIFO for each BCDMA Tx split mode channel and is used for buffering payload data that has been fetched by read DMA unit modules. Data is transferred from the buffer to the remote peripheral via a PSI-L interface. This unit is optional and is only present if one or more Tx split mode channels are configured in the BCDMA instance.

11.1.1.5.1.8 Rx Per-Split-Channel Buffers

The Rx Per-Split-Channel Buffers implement a FIFO for each BCDMA Rx split mode channel and is used for buffering payload data that has been received from remote peripherals via a PSI-L interface. Data is read from these FIFOs and written out to memory as directed by the write DMA unit modules. This unit is optional and is only present if one or more Rx split mode channels are configured in the BCDMA instance.

11.1.1.5.1.9 Write Unit(s)

The Write Units implement all of the state machine functionality necessary to perform the write transfers defined in the SW supplied Transfer Request records. The write DMA unit initiates VBUSM transactions in order to read descriptor pointers from memory mapped rings, read descriptors and/or Transfer Request records from memory mapped rings, read descriptor and Transfer Request records, and write payload data to memory.

11.1.1.5.1.10 Event Coherency Unit

The Event Coherency Unit is responsible for ensuring that all writes have completed prior to signaling an output event for a channel/flow.

11.1.1.5.1.11 Event Handler

The Event Handler block is responsible for generating channel completion and error events and for accepting and tracking channel triggering.

11.1.1.5.2 Channel Classes

Not all channels within a DMA controller require the same performance capabilities. Raw bandwidth and latency tolerance requirements will vary greatly between data transfers at various points in the system. Due to area concerns, several different classes of DMA channels are provided in the BCDMA and are described as follows:

Class Name	Description
Normal Capacity	Provides baseline amount of descriptor and TR prefetch and Tx/Rx control and data buffering. Suitable for most peripheral transfers which are communicating with on-chip memories and DDR
High Capacity	Provides an elevated amount of descriptor and TR prefetch and custom Tx/Rx control and data buffering. Suitable for applications which require moderate per-channel bandwidth with significantly increased latency (ex. Transferring data to/from PCIe)
Ultra-High Capacity	Provides identical descriptor and TR prefetch as High Capacity but with increased Tx data buffering to allow for more read data in flight. Suitable for applications requiring high per-channel bandwidth with significantly increased latency (ex. 16+Gbps transfers to/from PCIe).

BCDMA instances may provide support for any or all of the above channel classes through design time configuration parameters.

11.1.2 Definition of Terms

Host— The host is an intelligent system resource that configures and manages each communications control module. The host is responsible for allocating memory, initializing all data structures, and responding to port interrupts.

Channel— A channel refers to the sub-division of information (flows) that is transported across a DMA engine. Each channel has associated state information. Channels are used to segregate information flows based on the protocol used, scheduling requirements (for example, CBR, VBR, ABR), or concurrency requirements (that is, blocking avoidance). Information flow within a channel is a stream of strongly ordered information.

Data Buffer— A data buffer is a single data structure that contains payload information for transmission to or reception from a channel.

Buffer Descriptor— A buffer descriptor is a single data structure that contains information about one or more data buffers.

Packet Descriptor— A packet descriptor is another name for the first buffer descriptor within a packet. Some fields within a data buffer descriptor are only valid when it is a packet descriptor including the tags, packet length, packet type, and flags. All Monolithic type descriptors are packet descriptors (and are also a Data Buffer).

Queue— A queue is a list of strongly ordered entries which is typically used to pass work between a producer and a consumer. Queue entries in most cases are references to a work payload which is being passed, but in some cases, (Transfer Request Packets for example) queue entries may actually contain data which is being transferred. Queues are used throughout DMA whenever communication is required between entities. Queues can have multiple different implementations and DMA uses two of the most common: linked lists and rings.

Linked list— A linked list is a data structure in which each entry stores not only the entry data but also a chaining pointer to the next entry in the list. The last entry in each list has its chaining pointer set to NULL (typically encoded as 0x0). The list manager maintains a pointer to the head element on the list and to the tail element on the list. Since the chaining pointer is stored with the entry data, linked lists have a length which is dynamically changeable and limited only by the ability to allocate additional entries which are to be queued/de-queued. Linked lists are present in Host Descriptors to chain multiple descriptors to form a packet.

Ring— A ring is a data structure in which a contiguous memory block defined by M N-byte entries (total size is M × N bytes) is statically allocated and sequentially written/read in order to pass data or data references. Rings are also referred to as circular buffers because when the last element in the contiguous memory array is written, the pointers wrap back to the beginning address for the ring and start the process all over again. The Ring Accelerator component uses rings in order to implement logical queues.

Free Descriptor/Buffer Queue— A free descriptor/buffer queue is a list of available descriptors with prelinked empty buffers that are to be used by the receive ports for host type descriptors. Free Descriptor/Buffer Queues are implemented by the Ring Accelerator.

Free Descriptor Queue— A free descriptor queue is a list of available descriptors that are not yet linked with buffers that are to be used by the receive ports for monolithic type descriptors. Free Descriptor Queues are implemented by the Ring Accelerator.

Packet Queue— A packet queue is a list of valid (that is, populated) packet descriptors that is used for forwarding a packet from one entity to another for any number of purposes. Packet Queues are implemented by the Ring Accelerator.

Memory— Memory is an area of data storage managed by the host. This area is visible to the port as a 64-bit addressable area.

Device Driver— A device driver is application independent software that runs on the host for purposes abstracting the low level hardware so that upper level software can use the hardware without knowing every bit field location or initialization sequence. General device driver functions include port initialization, transmit packet queuing, and receive packet processing.

SOP— Start of Packet. This refers to the descriptor/buffer that is the first buffer in a packet.

MOP— Middle of Packet. This refers to the descriptors/buffers that are neither the first or last buffers in a packet.

EOP— End of Packet. This refers to the descriptor/buffer that is the last buffer in a packet.

11.1.3 DMSS Hardware/Software Interface

The intent of the Data Movement architecture is to provide a uniform HW/SW interface which includes a rich set of mechanisms that SW can make use of to transfer data with low overhead and reasonable complexity. To this goal, the number of components which SW is required to interact with on an ongoing real time basis has been kept to a minimum and is as follows (in order of anticipated frequency of access):

- Interrupt Aggregator
- Packet DMA
- Block Copy DMA

When interrupts are used, the interrupt aggregator will provide the vast majority of interrupt sources from all DMA components in the system. Each non-exception/non-debug packet and TR completion signaling originates from the Interrupt Aggregator and the IA provides a uniform set of MMRs that can be queried to quickly determine the cause of a specific interrupt. Events from PSI-L/ETL components are all routed to the host via the Interrupt Aggregator.

Each PKTDMA and BCDMA instance includes an inbuilt ring control mechanism which is the primary means by which work is sent to or received from these DMAs. Each DMA instance also includes both static configuration type memory mapped registers and some real-time accessible memory mapped registers for monitoring and control of each individual channel.

Memory mapped data structures are used anytime information needs to be passed between components in the system. These components may be hardware or software. The following sections describe the data structures which are used within the DMSS for passing information. These data structures include data buffers, packet descriptors, buffer descriptors, queues (including transmit queues, transmit completion queues, and receive queues) and the configuration MMRs that are provided in the various components. The following sections provide a detailed description of these data structures.

11.1.3.1 Data Buffers

A data buffer is a byte aligned contiguous block of memory used to store payload data. Each buffer is described in an entry in either a packet descriptor or in a buffer descriptor. A data buffer may hold any portion of a packet and may be linked together (via descriptors) with other buffers to form packets. Data buffers may be allocated anywhere within the 64-bit memory space.

The Buffer Length field of the packet/buffer descriptor indicates the number of valid data bytes in the buffer. There may be from 1 to 4M-1 valid data bytes in each buffer.

11.1.3.2 Descriptors

Descriptors are so named because their primary function is to describe other data structures.

The PKTDMA architecture provides for 2 basic types of descriptors whose characteristics are shown in PKTDMA Descriptor Types and Attributes.

Table 11-4. PKTDMA Descriptor Types and Attributes

Descriptor Type	Includes Valid Packet Info	Provided # of Slots to Link In External Data	Provides Local Protocol Specific Storage	Provides Slot to Link Additional Descriptors Within Same Packet	Description
Host Packet Descriptor	✓	1	✓	✓	Used to describe packet and SOP buffer in applications that require Host OS compatible data structures (i.e. applications where the descriptors and buffers cannot be managed independently but must instead be pre-linked by the Host software). These applications inherently require a separate descriptor for each buffer.
Host Buffer Descriptor		1		✓	Used to describe non-SOP buffers in applications that require Host OS compatible data structures

As the above table shows, the Host Packet Descriptor provides packet level information that is useful to both the ports and the Host in order to properly process the packet. These descriptors are referred to as Packet Descriptors and will always appear as the first descriptor within a packet.

The PKTDMA allows descriptors to be allocated on 16-byte address boundaries. This is intended to allow for better memory utilization by allowing on-chip descriptors which are not a power of 2 in length to be packed into arrays with little wasted memory space.

Even though descriptors and buffers may be allocated on any 16-byte alignment, careful consideration of the alignment effects should be made based on the storage location and any cache related affects that may exist. If data structures are placed in off-chip SDRAM the burst size and alignment restrictions of the memory devices must be considered in order to avoid performance issues related to continually fetching mis-aligned blocks. In this case, the memory efficiency can be reduced to 50% because 2 memory bank lines are read for every line sized data fetch. Similarly, placing more than one descriptor or buffer object within a single cache line can cause the adjacent object to become corrupted during cache line writeback operations.

Software/application specific control information may be added to the end of any of the packet descriptor types using as many extra words as necessary but the above alignment rules still apply.

The Block Copy DMA architecture provides a single descriptor type whose characteristics are shown in Block Copy DMA Descriptor Types and Attributes.

Table 11-5. Block Copy DMA Descriptor Types and Attributes

Descriptor Type	Includes Valid Packet Info	Provided # of Slots to Link In External Data	Provides Local Protocol Specific Storage	Provides Slot to Link Additional Descriptors Within Same Packet	Description
Transfer Request Packet Descriptor		0			Used to feed transfer request sequences to the BCDMA

11.1.3.2.1 Host Packet Descriptor

Host Packet Descriptors are designed to be used when the application requires support for true, unlimited fragment count scatter/gather type operations. The Host Packet Descriptor contains the following information:

- Indicator which identifies the descriptor as a Host Packet Descriptor
- Source and Destination Tags
- Packet Type
- Packet Length
- Protocol Specific Region Size
- Protocol Specific Control / Status Bits
- Pointer to the first valid byte in the SOP data buffer
- Length of the SOP data buffer
- Pointer to the next buffer descriptor in the packet
- Software specific information

Host Packet Descriptors always contain 48 bytes of required information and may also contain optional software specific information and protocol specific information. How much optional information (and therefore the allocated size of the descriptors) is required is application dependent.

The Host Packet descriptor layout is shown below.

Table 11-6. Host Packet Descriptor Layout

Packet Info (16 bytes)
Linking Info (8 bytes)
Buffer Info (12 bytes)
Original Buffer Info (12 bytes)
Extended Packet Info Block (Optional) Includes Timestamp and Software Data (16 bytes)
Protocol Specific Data (Optional) (0 to M bytes where M is a multiple of 4)
Other SW Data (Optional and User Defined)

Host Packet Descriptors may be linked with zero or more additional Host Buffer Descriptors in a singly linked list fashion to form packets. Each Host Packet consists of a single Host Packet Descriptor followed by a chain of zero or more Host Buffer Descriptors linked together using the Next Descriptor Pointer fields in the descriptors. The last descriptor in a Host packet has a zero Next Descriptor Pointer.

The ‘Other SW Data’ portion of the descriptor exists after all of the defined words and is reserved for use by the host software to store completely private data. This region is not used in any way by HW components in a PKTDMA system and these modules will not modify any bytes within this region.

The contents of the Host Packet Descriptor words are detailed in Table 11-7 through Table 11-23

Table 11-7. Host Packet Descriptor Packet Information Word 0 (PD Word 0)

Bits	Name	Description	Rx Overwrite
31:30	2'd1	64-bit Host Packet Descriptor Type Identifier	Yes
29	Extended Packet Info Block Present	This field indicates the presence of the Extended Packet Info Block in the descriptor. 0 = EPIB is not present 1 = 16 byte EPIB is present	Yes
28	RESERVED	-	*Yes*
27:22	Protocol Specific Valid Word Count	This field indicates the valid # of 32-bit words in the protocol specific region. This is encoded in increments of 4 bytes as follows: 0 = 0 bytes 1 = 4 bytes … 16 = 64 bytes ... 32 = 128 bytes 33-63 = RESERVED	Yes
21:0	Packet Length	The length of the packet in bytes. If the Packet Length is less than the sum of the buffer lengths, then the packet data will be truncated. A Packet Length greater than the sum of the buffers is an error. The valid range for an exact packet length is 0 to 4M-1 bytes. If the packet length is set to 0, the port will not actually transmit any information.	Yes

Table 11-8. Host Packet Descriptor Packet Information Word 1 (PD Word 1)

Bits	Name	Description	Rx Overwrite
31:28	Error Flags	This field contains error flags that can be assigned based on the packet type	Yes
27:24	Protocol Specific Flags	This field contains protocol specific flags / information that can be assigned based on the packet type.	Yes
23:14	RESERVED	-	Yes

Table 11-8. Host Packet Descriptor Packet Information Word 1 (PD Word 1) (continued)

Bits	Name	Description	Rx Overwrite
13:0	Flow ID	Flow ID within which this packet is being transported. The FlowID is used by downstream blocks to make decisions about packet steering and resource allocations. FlowIDs are also used to allow specific packets to be received into specific sets of buffers.	Yes

Table 11-9. Host Packet Descriptor Packet Information Word 2 (PD Word 2)

Bits	Name	Description	Rx Overwrite
31:27	Packet Type	This field indicates the type of this packet and is encoded as follows: 0-31 = Application specific	Yes
26:16	RESERVED	-	Yes
15:0	RESERVED	-	Yes

Table 11-10. Host Packet Descriptor Packet Information Word 3 (PD Word 3)

Bits	Name	Description	Rx Overwrite
31:24	Source Tag – Hi	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L src_tag field bits 15:8.	Yes
23:16	Source Tag – Lo	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L src_tag field bits 7:0.	Yes
15:8	Dest Tag – Hi	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L dst_tag field bits 15:8.	Yes
7:0	Dest Tag – Lo	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field with the value provided in the PSI-L dst_tag field bits 7:0	Yes

Table 11-11. Host Packet Descriptor Linking Word 0 (PD Word 4)

Bits	Name	Description	Rx Overwrite
31:0	Next Descriptor Pointer LSB	The 32 LSBs of the 48-bit word aligned memory address of the next buffer descriptor in the packet. If the value of this pointer is zero then the current buffer is the last buffer in the packet. The host sets the Next Descriptor Pointer.	No

Table 11-12. Host Packet Descriptor Linking Word 1 (PD Word 5)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
19:16	Next Descriptor Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.	No
15:0	Next Descriptor Pointer MSB	The 16 MSBs of the 48-bit next descriptor pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-13. Host Packet Descriptor Buffer 0 Info Word 0 (PD Word 6)

Bits	Name	Description	Rx Overwrite
31:0	Buffer 0 Pointer LSB	The Buffer Pointer is the byte aligned memory address of the buffer associated with the buffer descriptor. This value will be written during reception. These are the 32 LSBs of the 48-bit buffer pointer. **THIS Value along with the MSB bits cannot be 0 or the buffer will be seen as a NULL PTR**	Yes

Table 11-14. Host Packet Descriptor Buffer 0 Info Word 1 (PD Word 7)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		Yes

Table 11-14. Host Packet Descriptor Buffer 0 Info Word 1 (PD Word 7) (continued)

Bits	Name	Description	Rx Overwrite
19:16	Buffer 0 Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.	Yes
15:0	Buffer 0 Pointer MSB	The 16 MSBs of the 48-bit buffer pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	Yes

Table 11-15. Host Packet Descriptor Buffer 0 Info Word 2 (PD Word 8)

Bits	Name	Description	Rx Overwrite
31:22	RESERVED	Written to 0	Yes
21:0	Buffer 0 Length	The Buffer Length field indicates how many valid data bytes are in the buffer.	Yes

Table 11-16. Host Packet Descriptor Reserved Word 0 (PD Word 9)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-17. Host Packet Descriptor Reserved Word 1 (PD Word 10)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-18. Host Packet Descriptor Reserved Word 2 (PD Word 11)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
15:0	RESERVED		No

This word is only present if the Extended Packet Info Block present bit is set in Word 0

Table 11-19. Host Packet Descriptor Extended Packet Info Block Word 0 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Timestamp Info	This field contains an application specific timestamp which can be used for traffic shaping in a QoS enabled system.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-20. Host Packet Descriptor Extended Packet Info Block Word 1 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 0	This field stores software centric information that needs to travel with the packet through the stack. This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-21. Host Packet Descriptor Extended Packet Info Block Word 2 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 1	This field stores software centric information that needs to travel with the packet through the stack. This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

This word is only present if the Extended Packet Info Block present bit is set in Word 0.

Table 11-22. Host Packet Descriptor Extended Packet Info Block Word 3 (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Software Info 2	This field stores software centric information that needs to travel with the packet through the stack. This information will be copied from the source descriptor to the destination descriptor whenever a prefetch operation is performed or when transferring through an infrastructure DMA node.	Configurable

Table 11-23. Host Packet Descriptor Protocol Specific Word N (Optional)

Bits	Name	Description	Rx Overwrite
31:0	Protocol Specific Data N	This field stores information which varies depending on the block and packet type.	Configurable

11.1.3.2.2 Host Buffer Descriptor

The Host Buffer Descriptor is identical in size and organization to a Host Packet Descriptor but does not include valid information in the packet level fields and does not include a populated region for protocol specific information. Host Buffer Descriptors are designed to be linked onto a Host Packet Descriptor or another Host Buffer Descriptor to provide support for unlimited scatter / gather type operations. Host Buffer Descriptors provide information about a single corresponding data buffer. Every Host buffer descriptor stores the following information:

- Pointer to the first valid byte in the data buffer
- Length of the data buffer
- Pointer to the next buffer descriptor in the packet

Host Buffer Descriptors always contain 48 bytes of required information. Since it is a requirement that it is possible to convert a Host descriptor between a Buffer Descriptor and a Packet Descriptor (by filling in the appropriate fields) in practice, Host Buffer Descriptors will be allocated using the same sizes as Host Packet Descriptors. The Host Buffer Descriptor layout is shown below.

Table 11-24. Host Buffer Descriptor Layout

Buffer Reclamation Info (16 bytes)
Linking Info (8 bytes)
Buffer Info (12 bytes)
Original Buffer Info (12 bytes)

A Host Packet Descriptor and zero or more Host Buffer Descriptors may be linked together using the Next Descriptor Pointer fields to form packets. The last descriptor in a packet has a zero Next Descriptor Pointer. Each Host Buffer descriptor also points to a single data buffer.

The contents of the Host Buffer Descriptor words are detailed in : Table 11-25 through Table 11-33

Table 11-25. Host Buffer Descriptor Reserved Word 0 (BD Word 0)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED	-	No

Table 11-26. Host Buffer Descriptor Reserved Word 1 (BD Word 1)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED	-	No

Table 11-27. Host Buffer Descriptor Reserved Word 2 (BD Word 2)

Bits	Name	Description	Rx Overwrite
31:16	RESERVED	-	No
15:0	RESERVED	-	No

Table 11-28. Host Buffer Descriptor Reserved Word 3 (BD Word 3)

Bits	Name	Description	Rx Overwrite
31:0	RESERVED		No

Table 11-29. Host Buffer Descriptor Linking Word 0 (BD Word 4)

Bits	Name	Description	Rx Overwrite
31:0	Next Descriptor Pointer LSB	The 32 LSBs of the 48-bit word aligned memory address of the next buffer descriptor in the packet. If the value of this pointer is zero then the current buffer is the last buffer in the packet. The host sets the Next Descriptor Pointer.	No

Table 11-30. Host Buffer Descriptor Linking Word 1 (BD Word 5)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No
19:16	Next Descriptor Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.	No
15:0	Next Descriptor Pointer MSB	The 16 MSBs of the 48-bit next descriptor pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-31. Host Buffer Descriptor Buffer N Info Word 1 (BD Word 6)

Bits	Name	Description	Rx Overwrite
31:0	Buffer 0 Pointer LSB	The Buffer Pointer is the byte aligned memory address of the buffer associated with the buffer descriptor. This value will be written during reception. These are the 32 LSBs of the 48-bit buffer pointer.	No

Table 11-32. Host Buffer Descriptor Buffer N Info Word 1 (BD Word 7)

Bits	Name	Description	Rx Overwrite
31:20	RESERVED		No

Table 11-32. Host Buffer Descriptor Buffer N Info Word 1 (BD Word 7) (continued)

Bits	Name	Description	Rx Overwrite
19:16	Buffer 0 Pointer Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.	No
15:0	Buffer 0 Pointer MSB	The MSBs of the 48-bit buffer pointer. If a specific SoC uses less than 48 bits of address reach the width of this field may be reduced.	No

Table 11-33. Host Buffer Descriptor Buffer N Info Word 2 (BD Word 8)

Bits	Name	Description	Rx Overwrite
31:22	RESERVED		No
21:0	Buffer N Length	The Buffer Length field indicates how many valid data bytes are in the buffer. Unused or protocol specific bytes at the beginning of the buffer are not counted in the Buffer Length field. This value will be overwritten during reception.	No

11.1.3.2.3 Transfer Request Descriptor

The Transfer Request Descriptor contains the following information:

- Indicator which identifies the descriptor as a TR Descriptor
- Set of one or more Transfer Request Records
- Set of one or more Transfer Response Records

Transfer Request Packet Descriptors always contain 16 bytes of required information and a variable number of Transfer Request / Transfer Response Records (request and response counts match).

The Transfer Request descriptor layout is shown below.

Table 11-34. Transfer Request Packet Descriptor Layout

Packet Info Given via Transfer Request Packet Descriptor Word 0-3 (16 bytes)
Null (0-102 bytes to bring start of TR request array into natural alignment for memory fetch efficiency)
Array of Transfer Request Records
Array of Transfer Response Records

Table 11-35. Transfer Request Packet Descriptor Word 0

Bits	Name	Description	Rx Overwrite
31:30	2’d3	TR Packet Descriptor type.	No
29	RESERVED		No
28:20	Reload Count	Specifies what to do when the last entry is processed in this packet. This field specifies how many times to return to the Reload Index upon reaching the Last Entry. When an internal count is incremented to this value and the TR indicated by the Last Entry has been processed, this packet will be considered complete and the descriptor will be placed back on the return queue specified in Word 2. A value of 0x1FF indicates that a perpetual loop is desired. In this case, the loop count is considered infinite and the internal count will not be incremented. A teardown operation on the channel will cause the loop to be broken at the nearest iteration boundary.	No
19:14	Reload Index	Specifies the value to set the current processing index to when the last entry is processed and the Reload Enable is set to 1. This is basically an absolute index to jump to on the 2**nd** and following passes through the TR packet.	No
13:0	Last Entry	Specifies the index of the last valid entry in this packet	No

Table 11-36. Transfer Request Packet Descriptor Word 1

Bits	Name	Description	Rx Overwrite
31:28	RESERVED	-	No
27	RESERVED		No

Table 11-36. Transfer Request Packet Descriptor Word 1 (continued)

Bits	Name	Description	Rx Overwrite
26:24	Transfer Request Nominal Element Size	Specifies the stride between TR entries. The value in this field must be set large enough that any TR in the buffer will fit within the given dimension. TRs are expected to be placed on boundaries as given in this dimension. This field is also used to calculate the location where the Transfer Responses will be written back. This field is encoded as follows: 0 = 16-byte Transfer Request record size 1 = 32-byte Transfer Request record size 2 = 64-byte Transfer Request record size 3 = 128-byte Transfer Request record size 4-7 = RESERVED	No
23:14	RESERVED	-	No
13:0	RESERVED	-	No

Table 11-37. Transfer Request Packet Descriptor Word 2

Bits	Name	Description	Rx Overwrite
31:17	RESERVED		Yes
16	RESERVED	-	Yes
15:0	RESERVED	-	Yes

Table 11-38. Transfer Request Packet Descriptor Word 3

Bits	Name	Description	Rx Overwrite
31:24	RESERVED	-	No
15:0	RESERVED	-	No

Table 11-39. Transfer Request Packet Descriptor Payload Words 0-N

Bits	Name	Description	Rx Overwrite
31:0	Transfer Control Record Array	Transfer Control Records. This is an array of records which encapsulate the Transfer Request and Transfer Response messages which are used by the BCDMA	Yes (partial)

11.1.3.3 Transfer Request Record

11.1.3.3.1 Overview

This section describes the standard transfer request (TR) format to initiate a DMA transfer. The TRs can support both half and full duplex with multiple dimensions. Each TR will also generate a TR response. A TR can be sent to the BCDMA either through a TR descriptor using a pass-by-reference ring or as a Direct TR submission using a pass-by-value ring.

Table 11-40. Terms and Definitions

Term	Definition
TR	A transfer request to move data.
CR	A cache operation request. A request to send messages to a specified cache controller to prepare the cache for a future operation.

11.1.3.3.2 Addressing Algorithm

For a basic TR request the same algorithm is used. The innermost loop always consumes physically contiguous elements from memory. Its implicit dimension is 1 byte. The pointer itself moves from fetch to fetch on the maximum byte alignments specified for the BCDMA, in increasing order. In each level outside the inner loop, the loop moves the pointer to a new location based on the size of that loop level’s dimension.

11.1.3.3.2.1 Linear Addressing (Forward)

The following code illustrates the basic algorithm for a 4-level loop nest block move. This model assumes that it transfers data 1 byte at a time and the input and output block are the same size in all dimensions.

```
// sptr is a byte pointer.
// dptr is a byte pointer.
// Source address is indirect
if (TR_ISA) {
    sptr = *sptr;
}
// Destination address is indirect
if (TR_IDA) {
    dptr = *dptr;
}
// TR_TRIGX can be selected to come from Global events, Local event, or none.
// Check for trigger of TYPE0
if (TR_TRIG0_TYPE == TYPE0) while(!TR_TRIG0);
if (TR_TRIG1_TYPE == TYPE0) while(!TR_TRIG1);
for (i3 = 0; i3 < ICNT3; i3++)
{
    sptr3 = sptr; // save current position before entering next level
    dptr3 = dptr; // save current position before entering next level
    // Check for trigger of TYPE1
    if (TR_TRIG0_TYPE == TYPE1) while(!TR_TRIG0);
    if (TR_TRIG1_TYPE == TYPE1) while(!TR_TRIG1);
    for (i2 = 0; i2 < ICNT2; i2++) {
        sptr2 = sptr; // save current position before entering next level
        dptr2 = dptr; // save current position before entering next level
        // Check for trigger of TYPE2
        if (TR_TRIG0_TYPE == TYPE2) while(!TR_TRIG0);
        if (TR_TRIG1_TYPE == TYPE2) while(!TR_TRIG1);
        for (i1 = 0; i1 < ICNT1; i1++) {
            sptr1 = sptr; // save current position before entering next level
            dptr1 = dptr; // save current position before entering next level
            // Check for trigger of TYPE3
            if(TR_TRIG0_TYPE == TYPE3) while(!TR_TRIG0);
            if(TR_TRIG1_TYPE == TYPE3) while(!TR_TRIG1);
            for (i0 = 0; i0 < ICNT0; i0++) {
                // BCDMA can combine these in optimized burst aligned accesses.
                *dptr = *sptr;
                sptr = sptr++;
                dptr = dptr++;
            }
        // Update based on saved pointer for this level
        sptr = sptr1 + SDIM1;
        dptr = dptr1 + DDIM1;
        }
    // Update based on saved pointer for this level
    sptr = sptr2 + SDIM2;
    dptr = dptr1 + DDIM2;
    }
```

This form of addressing allows programs to specify regular paths through memory in a small number of parameters. Additionally, it allows for various stall points through the loop to allow for hardware or software induced pausing of the transfer. The following section defines these parameters in detail.

11.1.3.3.3 Transfer Request Formats

The BCDMA defines a four-level loop nest for addressing elements within the TR, using the algorithms described in the Addressing algorithm. Most of the fields in the TR template map directly to the parameters in those algorithms.

Table 11-41. Transfer Request Fields

Field Name	Description	Size
FLAGS	TR flags that specify type of TR and how the TR should be handled. It also supports the TR triggering and output events.	32 bits
ICNT0	Total loop iteration count for level 0 (innermost)	16 bits
ICNT1	Total loop iteration count for level 1	16 bits
ADDR	Starting address for the source data or destination data if it is a half-duplex write.	64 bits
DIM1	Signed dimension for loop level 1 for the source data	32 bits
ICNT2	Total loop iteration count for level 2	16 bits
ICNT3	Total loop iteration count for level 3 (outermost)	16 bits
DIM2	Signed dimension for loop level 2	32 bits
DIM3	Signed dimension for loop level 3	32 bits
DDIM1	Signed dimension for loop level 1 for the destination data	32 bits
DADDR	Starting address for the destination of the data	64 bits
DDIM2	Signed dimension for loop level 2 for the destination data	32 bits
DDIM3	Signed dimension for loop level 3 for the destination data	32 bits
DICNT0	Total loop iteration count for level 0 (innermost) used for destination	16 bits
DICNT1	Total loop iteration count for level 1 used for destination	16 bits
DICNT2	Total loop iteration count for level 2used for destination	16 bits
DICNT3	Total loop iteration count for level 3 used for destination	16 bits

The TR assumes all iteration counts as unsigned integers, and all dimensions as signed integers representing byte offsets.

The template above fully specifies the type of elements, length, and dimensions of the transfer.

Since all transfers will not require all the fields the TRs have the type field which allow the number of words required to be sent for the TR to be reduced.

11.1.3.3.4 Flags Field Definition

The next diagram expands the 32-bit FLAGS field. The numbers above each field here indicate bit numbers within the field.

Table 11-42. Transfer Request Template FLAGS Field

31			24	23				16
CONFIGURATION SPECIFIC FLAGS				Reserved				
15			8	7	5	4	3	0
TRIGGER_SIZE1	TRIGGER1	TRIGGER_SIZE0	TRIGGER0	EVENT_SIZE	WAIT	STATIC	TYPE	

The flags field fills in the remaining details about the stream, as follows:

Table 11-43. FLAGS Field Descriptions

Bit	Field	Description
0-3	**TYPE**	The TYPE of TR that is being sent 0: One dimensional data move 1: Two dimensional data move 2: Three dimensional data move 3: Four dimensional data move 4: Four dimensional data move with data formatting 5: Four dimensional Cache Warm 6-7: Reserved 8: Four Dimensional Block Move 9: Four Dimensional Block Move with Repacking 10: Two Dimensional Block Move 11: Two Dimensional Block Move with Repacking 12-14: Reserved 15 Four Dimensional Block Move with Repacking and Indirection
4	Reserved	Reserved for Future use.
5	**WAIT**	This field is only valid on Type 15 TRs. This field indicates whether or not this TR should ensure it completes before allowing the next TR to start on this channel. The encoding is as follows: 0 = Allow next TR to start immediately 1 = Wait for this TR to complete before allowing next TR to start When set, the next TR will not be considered triggered (regardless of any other trigger conditions) until all write status responses for the current TR have landed.

Table 11-43. FLAGS Field Descriptions (continued)

Bit	Field	Description
6-7	**EVENT_SIZE**	This is how often the TR will generate an output event. 0: Event is only generated with the TR is complete 1: Event is generated when the second inner most loop (ICNT1) is decremented by 1. 2: Event is generated when the third inner most loop (ICNT2) is decremented by 1. 3: Event is generated when the outer most loop (ICNT3) is decremented by 1.
8-9	**TRIGGER0**	This is one of two selectable triggers. The receipt of this trigger will enable the TR to be active for enough data transfer as specified by the TRIGGER0_TYPE Field. 0: No Trigger 1: Global Trigger 0 for the channel 2: Global Trigger 1 for the channel 3: Local Event for the channel
10-11	**TRIGGER0_TYPE**	This is the type of data transfer that will be enabled by receiving a trigger. 0: The second inner most loop (ICNT1) will be decremented by 1. 1: The third inner most loop (ICNT2) will be decremented by 1. 2: The outer most loop (ICNT3) will be decremented by 1. 3: The entire TR will be allowed to complete.
12-13	**TRIGGER1**	This is one of two selectable triggers. The receipt of this trigger will enable the TR to be active for enough data transfer as specified by the TRIGGER1_TYPE Field. 0: No Trigger 1: Global Trigger 0 for the channel 2: Global Trigger 1 for the channel 3: Local Event for the channel This field is reserved for a Direct TR.
14-15	**TRIGGER1_TYPE**	This is the type of data transfer that will be enabled by receiving a trigger. 0: The second inner most loop (ICNT1) will be decremented by 1. 1: The third inner most loop (ICNT2) will be decremented by 1. 2: The outer most loop (ICNT3) will be decremented by 1. 3: The entire TR will be allowed to complete.
16-23	Reserved	Reserved for Future use.

Table 11-43. FLAGS Field Descriptions (continued)

Bit	Field	Description
24-31	**Configuration Specific Flags**	These are flag bits that can be specified by the specific BCDMA configuration. These bits will remain undefined in the global TR format to allow for customization requirements that might be required in the specific BCDMA implementation.

The following sections expand on each of these fields.

11.1.3.3.4.1 Type: TR Type Field

The TR Type field gives the size of the TR and which fields are expected in the TR. Based on the type the number of words required to be sent to complete the TR can be decreased. The tables below show the minimum size for each TR as well if any fields will be treated as reserved.

Table 11-44. Transfer Request Minimum Size Type 0 One Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0	ADDR		RESERVED/NOT REQUIRED											

Table 11-45. Transfer Request Minimum Size Type 1 Two Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/1	ADDR		DIM1	RESERVED/NOT REQUIRED										

Table 11-46. Transfer Request Minimum Size Type 2 Three Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/1	ADDR		DIM1	ICNT2	DIM2	RESERVED/NOT REQUIRED								

Table 11-47. Transfer Request Minimum Size Type 3 Four Dimensional Transfer

word 0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/1	ADDR		DIM1	ICNT2/3	DIM2	DIM3	RESERVED/NOT REQUIRED							

Table 11-48. Transfer Request Minimum Size Type 15 Four Dimensional Block Copy with Repacking and Indirection Support

w0	word 1	word 2	word 3	word 4	word 5	word 6	word 7	word 8	word 9	word 10	word 11	word 12	word 13	word 14	word 15
FLAGS	ICNT0/1	ADDR		DIM1	ICNT2/3	DIM2	DIM3	RESERVED	DDIM1	DADDR		DDIM2	DDIM3	DICNT 0/1	DICNT 2/3

11.1.3.3.4.2 EVENT_SIZE: Event Generation Definition

The BCDMA allows for an event to be generated at specified intervals for each TR. As the TR passes through the various loops in the addressing algorithm it will generate an event that then can be routed to other event receivers, such as other channels or interrupts to processors.

Table 11-49. Event Size Encoding

Value	Event Type	When it Fires
0	Completion Event	When the TR is complete and all status for the TR has been received.
1	ICNT1 Decrement	Type 0: When the last data transaction is sent for the TR. Type 1-11: When ICNT1 is decremented
2	ICNT2 Decrement	Type 0 – 1,10-11: When the last transaction is sent for the TR. All Other Types: When ICNT2 is decremented
3	ICNT3 Decrement	Type 0 – 2,10-11: When the last transaction is sent for the TR. All Other Types: When ICNT3 is decremented

11.1.3.3.4.3 TRIGGER_INFO: TR Triggers

The TR allows for two different triggers to be set to allow for the data transfer to be prevented or halted through the process of transferring the data. The triggers are specified by selecting a type of trigger and the size of the transfer that can be allowed for the receipt of a given trigger. The triggers themselves in the BCDMA are collected on a per channel basis and for each of three sources. Anytime the trigger event is received the internal counter is incremented. The trigger event will not be cleared until the specified block has started its transfer and it will **only** clear the triggers that are active.

CAUTION

This does allow for one TR in the channel to use global event 0 and the next TR to use global event 1. If while the first TR is running global event 0 can increment and will decrement each time the TR reaches the specified level. At the same time global event 1 will be incremented whenever it is received but it will not decrement until the next TR runs. If the global event 1 counter reaches overflows then an error event will NOT be generated but the event will be lost.

11.1.3.3.4.4 TRIGGERX_TYPE: Trigger Type

The trigger type sets the value of TR_TRIGX as shown in the addressing algorithm description. The TR_TRIGX value allows for the temporary halting of the TR until the expected event has been received. After the given loop has been entered the selected trigger will be decremented.

11.1.3.3.4.5 TRIGGERX: Trigger Selection

The TR is able to select up to 2 of 3 trigger sources for a given TR. The events can come from the dedicated local event on the BCDMA itself or from two assigned global events that come from the PSI-L interface on the BCDMA. The trigger counters are always enabled so that events can be received prior to the TR getting loaded. The trigger counters are only decremented when the trigger is active and the TR has scheduled the first transfer of the transaction.

11.1.3.3.4.6 Configuration Specific Flags Definition

The configuration specific flags are specific to a given TR type. If a TR type does not require additional flags the field should be filled with 0’s. Currently only Types 0-4 and Type 15 support the following configuration specific flags:

Bit	Field	Description
0	**ISA**	Indirect Source Address 0: Source address in TR is a directly usable pointer to the data 1: Source address in TR is a pointer to a 64-bit location that contains the actual pointer to the data
1	**IDA**	Indirect Destination Address 0: Destination address in TR is a directly usable pointer to the data 1: Destination address in TR is a pointer to a 64-bit location that contains the actual pointer to the data
2	**SUPR_EVT**	Suppress Event Output: 0 = Output events will be generated according to FLAGS.EVENT_SIZE field 1 = No output events will be generated for the duration of this TR execution This field is only valid on split and type 15 TRs (Type 0-3,15)
3	**Reserved**	Reserved for Future use.

Bit	Field	Description
6:4	**EOL**	This field is only valid on split TRs (Type 0-3). On source (Read) split TRs, this field specifies whether or not the EOL delimiters should be produced on the Tx PSI-L bus. The encodings of this field for source split TRs is as follows: 0 = SOL/EOL match SOP/EOP 1 = SOL/EOL boundaries are each ICNT0 bytes 2 = SOL/EOL boundaries are each ICNT0*ICNT1 bytes 3 = SOL/EOL boundaries are each ICNT0*ICNT1*ICNT2 bytes 4 = SOL/EOL boundaries are each ICNT0*ICNT1*ICNT2*ICNT3 bytes On destination (Write) split TRs, this field specifies how to handle EOL delimiters when they are encountered on the Rx (write) side of a TR. EOL delimiters can be produced from the Tx (read) side of a block copy operation or from a remotely paired peripheral when operating in split TR mode. The encodings of this field are as follows: 0: Ignore EOL 1: Line length is icnt0 bytes. Clear any remaining ICNT0 bytes and increment ICNT1 by 1 2: Line length is icnt0*icnt1 bytes. Clear any remaining ICNT0/1 bytes and increment ICNT2 by 1 3: Line length is icnt0*icnt1*icnt2 bytes. Clear any remaining ICNT0/1/2 bytes and increment ICNT3 by 1 4: Line length is icnt0*icnt1*icnt2*icnt3 bytes. Move on to next TR 5-7: RESERVED
7	**EOP**	This TR should generate an EOP on the streaming interface for any downstream packet oriented consumers to denote that a ‘packet’ of data is complete 0: No EOP flag will accompany the last PSI-L data phase associated with transfers from this TR 1: On egress the DMA will set the EOP flag coincident with transferring the last of the data for this TR. If the TR data does not complete an entire PSI-L data phase then the remaining bytes in the data phase will be skipped and the internal FIFO pointer will be updated to begin packing new data on a new data phase boundary.

11.1.3.3.5 TR Address and Size Attributes

The fields described below all describe the data transfer that needs to be made as described in the Linear Memory Addressing Block Move Algorithm.

11.1.3.3.5.1 ICNT0

The ICNT0 is the number of elements to transfer in the inner loop of the TR. If the TR type does not contain a FMTFLAGS field then this count is assumed to be the number of bytes to transfer. If the FMTFLAGS field is included in the types then the number of bytes to be transferred will be ICNT0 times the Element size rounded up to the nearest byte.

11.1.3.3.5.2 ICNT1

The ICNT1 field is the loop count for the second innermost loop count as defined in the Addressing algorithm.

11.1.3.3.5.3 ADDR

The address location is the initial address that will be accessed at the start of the transfer. All of the dimensions will also be based off of this value. This address can either physical or virtual based upon settings in the DMA channel Configuration register.

While the ADDR field is 64 bits wide, the usable extent of the address is up to 48 bits of absolute offset plus a 4-bit address space selector which indicates 1 of 16 different orthogonal address spaces that the pointer is referencing within. The format of the ADDR field is given as follows:

Bits	Subfield	Description
63:52	Reserved	Reserved
51:48	Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other ‘tiles’ on large devices.
47:0	Address	The 48-bit source or source starting address for the transfer. This address is assumed to be a physical address. The actual width implemented for the address field on any given DMA instance may be adjusted to the needs of each specific KSLC SoC. 48 bits is just the maximum size which is envisioned to be supported. Some systems may have address widths as low as 32 or 36 bits. The HW implementation may choose to provide address width configurability in order to reduce costs.

11.1.3.3.5.4 DIM1

This is the offset of the address from the initial address for the first access of the second loop. This will be added to the address from the loop before. This is a signed value so that the address can be both above and below the initial address.

11.1.3.3.5.5 ICNT2

This is the count for the third innermost loop in the addressing algorithm.

11.1.3.3.5.6 ICNT3

This is the count for the outermost loop in the addressing.

11.1.3.3.5.7 DIM2

This is the offset of the address from the initial address to the next address in the third innermost loop. This is a signed value so that the address can be both above and below the previous address.

11.1.3.3.5.8 DIM3

This is the offset of the address from the initial address to the next address in the outermost loop. This is a signed value so that the address can be both above and below the previous address.

11.1.3.3.5.9 DDIM1

This is the offset of the destination address from the initial destination address for the first access of the second loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.10 DADDR

The destination address location is the initial destination address that will be accessed at the start of the transfer. All of the dimensions will also be based off of this value. This address can either physical or virtual based upon settings in the DMA channel Configuration register

While the DADDR field is 64 bits wide, the usable extent of the address on a KSLC system is up to 48 bits of absolute offset plus a 4 bit address space selector which indicates 1 of 16 different orthogonal address spaces that the pointer is referencing within. The format of the DADDR field is given as follows:

Bits	Subfield	Description
63:52	Reserved	Reserved
51:48	Address Space Select	Effectively bits 51:48 of the address. The value given in this field will be output by the DMA initiators on the casel pin which is used by the infrastructure as an identifier for which address space this particular memory region is located within. Address space 0 is the default unified address space for a given device. Address spaces 1-15 are used for alternate address maps which may be external to the device (PCIe/Hyperlink) or in other 'tiles' on large devices.
47:0	Address	The 48-bit starting destination address for the transfer. This address is assumed to be a physical address. The actual width implemented for the address field on any given DMA instance may be adjusted to the needs of each specific KSLC SoC. 48 bits is just the maximum size which is envisioned to be supported. Some systems may have address widths as low as 32 or 36 bits. The HW implementation may choose to provide address width configurability in order to reduce costs.

11.1.3.3.5.11 DDIM2

This is the offset of the destination address from the initial destination address for the first access of the third loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.12 DDIM3

This is the offset of the destination address from the initial destination address for the first access of the outer loop. This will be added to the destination address from the loop before. This is a signed value so that the destination address can be both above and below the initial destination address.

11.1.3.3.5.13 DICNT0

This is the number of elements to use in the destination if the TR is repacking the data. This number reflects the number of elements to be transferred.

11.1.3.3.5.14 DICNT1

This is the number of times to execute the second loop to use in the destination transfer.

11.1.3.3.5.15 DICNT2

This is the number of times to execute the third loop to use in the destination transfer.

11.1.3.3.5.16 DICNT3

This is the number of times to execute the fourth loop to use in the destination transfer. The value of DICNT0 x DICNT1 x DICNT2 x DICNT3 must equal ICNT0 x ICNT1 x ICNT2 x ICNT3. If any of the values are zero they are NOT included in the multiplication.

11.1.3.4 Transfer Response Record

Upon completing a TR, the BCDMA will send back a TR Response. The BCDMA TR response format is a single 32 bit word as shown in the Table 11-51 below.

Table 11-50. Transfer Request Response Template STATUS FLAGS Field

31	24	23			16
CONFIGURATION SPECIFIC STATUS		RESERVED			
15	8	7	7 4	3	0
RESERVED		STATUS_INFO		STATUS_TYPE	

Table 11-51. STATUS FLAGS Field Descriptions

Bit	Field	Description
3:0	**STATUS_TYPE**	The completion status of the TR.
7:4	**STATUS_INFO**	Information that is unique based on the STATUS_TYPE returned
15:8	**Reserved**	Reserved for Future use
23:16	**Reserved**	Reserved for Future use
31:24	**Configuration Specific Flags**	These are flag bits that can be specified by the specific BCDMA configuration. These bits will remain undefined in the global TR format to allow for customization requirements that might be required in the specific BCDMA implementation. For BCDMA channels which are capable of interfacing to endpoint peripherals (or via a PDMA) the format of these flags are as follows: 31:28 error_flags – the error_flags field as is provided across PSI-L 27:24 ps_flags – the ps_flags field as is provided across PSI-L

11.1.3.4.1 STATUS Field Definition

The Status field is made up of two sub-fields STATUS_TYPE and STATUS_INFO. A value of 0 means it completed as requested any other value means an error has occurred. The Table below states the legal STATUS_TYPEs and the use of the STATUS_INFO in each case.

11.1.3.4.1.1 STATUS_TYPE Definitions

The STATUS_TYPE field is used to determine what type of status is being returned. Depending on the type of Status it might additionally have information in the STATUS_INFO to give more details about the specific reason why the status was returned.

Table 11-52. STATUS_TYPE Encoded Values

Value	Error Type	Completion	STATUS INFO Definition
0	None	Complete	None
1	Transfer Error	None to Partial	CBA Non-Complete Status Received
2	Aborted Error	None to Partial	None
3	Submission Error	None	Submission Error Type
4	Unsupported Feature	None	Feature Type
5	Transfer Exception	Partial	Exception Type
6	Teardown Flush	None	None
7-15	Reserved	Unknown	Reserved

11.1.3.4.1.1.1 Transfer Error

A transfer error occurs anytime that one of the CBA transactions performed by the BCDMA returns a status other than complete. The BCDMA may continue the transfer or may abort the transfer and return back to an IDLE state. Once the transfer is finished (aborted or complete) the BCDMA will send back the TR Response with the STATUS TYPE of Transfer Error. The STATUS INFO will contain the 3 bit CBA Status field the upper bit specifies if it was a read status (1) or a write status (0).

11.1.3.4.1.1.2 Aborted Error

An aborted error occurs if the PSI-L interface asserts the drop signal prior to the completion of the TR. The BCDMA will return back to an IDLE state and send back the TR Response with the STATUS TYPE. If the BCDMA receives a transfer error after receiving the abort the transfer error should be reported instead of the abort error.

11.1.3.4.1.1.3 Submission Error

A submission error is returned for a TR that is received that cannot be run. The STATUS_INFO field specifies the type of submission errors.

Table 11-53. Submission Error STATUS_INFO Encodings

Value	Submission Error Type
0	ICNT0 was 0
1	Channel FIFO was full when TR received
2	Channel is not owned by the submitter. Either CC submitting to Direct or Direct submitting to a CC channel
3	Reserved
4	Reserved
5	Bad descriptor type
6-15	Reserved

11.1.3.4.1.1.4 Unsupported Feature

An unsupported feature error is returned for a TR that is received that cannot be run because it specifies a feature that is optional and not supported by the BCDMA that received the TR. The STATUS INFO specifies the feature that was not supported. If it specifies multiple features that were not supported the BCDMA implementation can determine which type it wants to return.

Table 11-54. Unsupported Feature STATUS_INFO Encodings

Value	Submission Error Type
0	TR Type not supported
1	STATIC not supported
2	EOL not supported
3	CONFIGURATION SPECIFIC not supported
4	AMODE not supported
5	ELTYPE not supported
6	DFMT not supported
7	SECTR not supported
8	AMODE SPECIFIC Field not supported
9-15	Reserved

11.1.3.4.1.1.5 Transfer Exception

A transfer exception is returned for a TR that completed but experienced a known exception during reception. The STATUS_INFO field specifies the type of transfer exception that was encountered.

Table 11-55. Transfer Exception STATUS_INFO Encodings

Value	Transfer Exception Type
0	EOP on incoming data stream was encountered prematurely (short packet)
1	EOP on incoming data stream was encountered late (long packet)
2-15	Reserved

11.1.3.4.1.1.6 Teardown Flush

Split mode BCDMA Rx channels (write channels) can respond with a teardown flush in the case that they have received a teardown message, all data has been transferred , and TRs have been prefetched (in anticipation of more data being received). In this case, the BCDMA will simply return the prefetched TR to the completion queue with the status type set to teardown flush.

11.1.3.5 Channels

Each DMA controller instance contains one or more channels. A channel represents a single thread of strongly ordered operations whose purpose is to move data from one interface to another. Operations between channels are orthogonal and have no assumption of ordering but operations within a channel must be completed in order. The DMA controller uses time division multiplexing to allow work from channels to momentarily use shared data transfer units and data paths.

11.1.3.6 Flows

Each DMA channel will provide one or more flows which allow communication with one or more SW hosts. Each flow contains a single queue pair implemented within a shared circular buffer (ring) in memory. One queue provides uni-directional communication from SW to the DMA while the other queue provides uni-directional communication from the DMA back to SW. Flows are intended to allow traffic which is produced or consumed by a different Host SW process or traffic which is on different priorities to share a single physical DMA channel. A DMA channel will perform time division multiplexing between flows on specific work boundaries. Once a channel is in work on a specific flow, that entire unit of work will be completed before allowing work from a different flow to begin.

11.1.3.7 Queues

Queues are used to hold either values or references that need to be passed between SW and HW components in the system. Queues are implemented in the PKTDMA and BCDMA modules using memory mapped rings. Each ring is comprised of a single contiguous memory block which contains an array of elements. Each element is 8 bytes. The size of the ring is selectable from 1 entry up to 64K entries with single entry granularity. Each ring is used to implement a forward and a reverse queue which share the same data elements but which have independent pointers and occupancies. The forward queue is used to pass work from SW to HW and the reverse queue is used to pass completed work back from HW to SW. A doorbell MMR is provided per ring to allow SW to add elements to the forward queue. A separate doorbell MMR is provided per ring to allow SW to acknowledge the popping of elements from the reverse queue. An occupancy MMR is provided for the reverse queue so that SW can know how many entries are currently completed. Entries are returned on the reverse queue in the exact same order and in the exact same index as the work was provided on the forward queue and because of this, the DMA controllers do not actually modify the ring entry for completion operations (the only exception being for acknowledgement of a teardown operation). Completion is indicated by incrementing of the reverse occupancy only.

11.1.3.7.1 Queue Types

11.1.3.7.1.1 Transmit Queues

Tx channels use packet queues referred to as “transmit queues” to store the packets that are waiting to be transmitted. Tx Queues only pass a pointer to a descriptor. For the PKTDMA, Tx Queues contain pointers to Host descriptors. For the BCDMA, pass Tx Queues contain a pointer to a TR packet descriptor. Transmit Queues are implemented as the forward queue on the shared ring structure for a Tx flow.

11.1.3.7.1.2 Transmit Completion Queues

Tx channels also use packet queues referred to as “transmit completion queues” to return packets to the host after they are transmitted. A Tx Completion Queue is provided for each Tx Queue. The DMA controllers do not actually write anything back to completion queues (except for a teardown acknowledgement) but instead just increment the reverse occupancy. Transmit completion queues are implemented as the reverse queue on the shared ring structure for a Tx flow.

11.1.3.7.1.3 Free Descriptor / Buffer Queues

Free descriptor/buffer queues pass an empty list of pre-chained descriptors, each pointing to a single buffer, from SW to the DMA to use for receiving incoming packets. Free Descriptor/Buffer Queues are implemented as the forward queue on the shared ring structure for an Rx flow.

11.1.3.7.1.4 Receive Queues

Rx queues pass a packet which has been received from the DMA back to the SW. Receive queues are implemented as the reverse queue on the shared ring structure for an Rx flow.

11.1.3.7.1.5 Ring Based Queues Implementation

Work packets which are stored in a queue are shown in the following diagram:

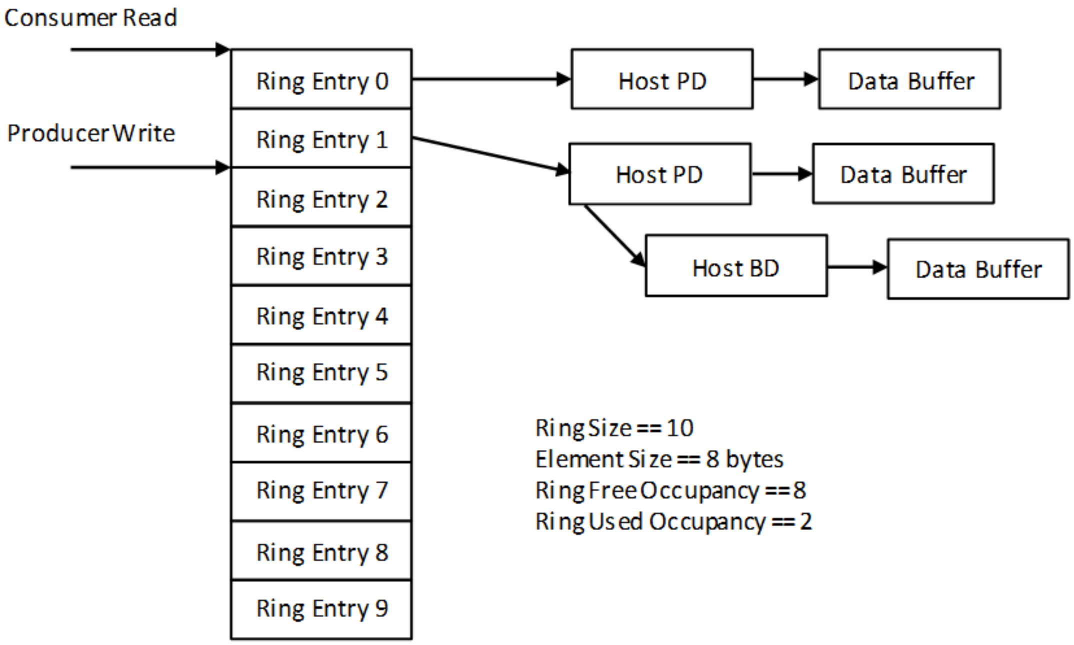


Figure 11-3. Ring Based Queue Structure

11.1.4 Operational Description

11.1.4.1 Resource Allocation

Rings, memory, interrupts, DMA channels, and flow table entries are shared resources within the data movement architecture and their ownership and use must be managed in order to provide stable, safe, and secure operation. The DMSS provides channelized firewalls which can be used to protect arrayed resources (like rings, channel control MMRs, etc.) from unwanted/unauthorized use as well as restricted access to the firewall configurations themselves. It is outside the scope of this document to define how the resource management system functions but it is assumed that all of these resources are isolate-able and secure-able.

11.1.4.2 PKTDMA/BCDMA - Ring Operation

11.1.4.2.1 Queue Initialization

The base address and size for each ring must be initialized via the provided MMRs prior to using the ring. Ring initialization is typically done only on channel / flow setup as once initialized the rings can be used indefinitely.

11.1.4.2.2 Queueing Entries

Entries can only be queued by SW onto the forward queue of a ring. To queue an entry the producer will write the entry contents (typically a pointer to the Packet Descriptor or a TR) to the memory location pointed to by the current write pointer and will decrement its internally maintained free entry occupancy. After the producer has confirmed that the data has actually landed it memory, it will then write to the forward doorbell register (RINGRT[a]_RT_FDB) for the ring to increment the pending forward occupancy count for the ring.

More than one entry can be queued with a single doorbell write as the entry count in the doorbell write indicates how many entries have been queued.

11.1.4.2.3 De-queueing Entries

Entries can only be de-queued by SW from the reverse queue of a ring. The consumer (entity which is going to de-queue an entry from the ring) maintains a current read pointer for each ring it controls. To de-queue an entry the consumer will read the occupancy from the reverse occupancy register (RINGRT[a]_RT_ROCC) and will then read the entry contents from the memory location pointed to by the current read pointer. The consumer will then write a decrement value to the reverse doorbell register (RINGRT[a]_RT_ROCC) for the ring to decrement the waiting occupancy count for the reverse queue within the ring and will increment its internally maintained free entry occupancy for the ring.

11.1.4.3 PKTDMA/BCDMA - Output Event Generation

Each channel and flow within a DMA has the ability to generate specific types of events which can be routed to the IA in the system and from there re-routed to any event consumer. Events are output from the DMA controllers using a simple integer encoding. Up to 4 events can be generated from any given channel but only event types which have functional value are supported on each specific type of channel. The DMA channel event types are listed as follows:

Table 11-56. Per-Channel/Flow Event Support and Encoding

Name	Description	Per	BCDMA BC	BCDMA Tx	BCDMA Rx	PKTDMA Tx	PKTDMA Rx
Ring Entry Zero/Non-zero	Asserts an up event anytime the ring transitions to a non-zero occupancy / teardown state. Asserts a down event anytime the ring transitions to a zero occupancy / teardown state.	Flow	X	X	X	X	X
Channel Error	Asserts an up event anytime an error occurs on the channel. Asserts a down event when the channel error bit is cleared.	Channel	First flow in channel only	First flow in channel only	First flow in channel only	First flow in channel only	First flow in channel only
Rx Starvation	Asserts an up event when starvation occurs on a flow. Asserts a down event when entries are added to the ring for that flow.	Flow					First flow in channel only

Table 11-56. Per-Channel/Flow Event Support and Encoding (continued)

Name	Description	Per	BCDMA BC	BCDMA Tx	BCDMA Rx	PKTDMA Tx	PKTDMA Rx
RX Flow FW Error	Asserts an up event when a flow id arrives on the RX interface that is not between the flowid_start and flowid end values for the channel. Asserts a down event when the RX Flow ID Firewall Status Register pend bit is cleared	Pktdma					X
Data Events	Asserts an up event when the selected loop counter has decremented. If the suppress event bit is not set in the TR	Channel	X	X	X		

Each BCDMA/PKTDMA instance will provide an event transport-lane (ETL) interface to pass outgoing events. The index field on this ETL will be calculated based on the event type and channel or flow offset. Each PKTDMA or BCDMA instance is configured with base values to which a channel or flow index is added for each type of event which can be generated. These base index values are listed in the specification for that specific instantiation of each DMA and are named as follows:

Table 11-57. BCDMA/PKTDMA Event Base Index Parameters

DMA	Event Base Parameter Name	Function	Offset
PKTDMA	tcomp_evtbase	Base index for Tx flow reverse ring completion events	Tx flow number
	rcomp_evtbase	Base index for Rx flow reverse ring completion events	Rx flow number
	terr_evtbase	Base index for Tx channel error events	Tx channel number
	rerr_evtbase	Base index for Rx channel error events	Rx channel number
	rstarve_evtbase	Base index for Rx flow starvation events	Rx flow number
	rflowfw_evtbase	Base index for Rx Flow Firewall event	None

Table 11-57. BCDMA/PKTDMA Event Base Index Parameters (continued)

DMA	Event Base Parameter Name	Function	Offset
BCDMA	tcomp_evtbase	Base index for split Tx flow reverse ring completion events	Tx flow number
	rcomp_evtbase	Base index for split Rx flow reverse ring completion events	Rx flow number
	bcomp_evtbase	Base index for normal Block Copy flow reverse ring completion events	BC flow number
	terr_evtbase	Base index for split Tx channel error events	Tx channel number
	rerr_evtbase	Base index for split Rx channel error events	Rx channel number
	berr_evtbase	Base index for normal Block Copy channel error events	BC channel number
	tdcomp_evtbase	Base index for Tx channel TR data completion events	Tx channel number
	rdcomp_evtbase	Base index for Rx channel TR data completion events	Tx channel number
	bdcomp_evtbase	Base index for Block Copy channel TR data completion events	BC channel number

Example:

The producer event map is set up so that the Tx flows from a PKTDMA instance are to start at 64 and proceed upward from there. The tcomp_evtbase for that PKTDMA instance is set to 64. In this configuration, the reverse ring entry completion event for flow 0 will produce an event on index 64, flow 1 will produce an event on index 65, etc. The terr_evtbase for the same PKTDMA instance is set to 128. In this configuration, error events for channel 2 would produce events with an index of 130.

11.1.4.4 PKTDMA - Transmit Channel Setup

This section describes the setup procedure for Tx channels within the PKTDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel’s Tx Port DMA State. The host initializes the channel Tx Port DMA State by configuring all of the Tx flow entries for the channel and then writing to the Tx Channel Configuration Register A (TCHAN[a]_TCFG). The Host may choose to write the enable bit in the Tx Channel Configuration Register A (TCHAN[a]_TCFG) at the same time or after it has written all of the channel parameters but note that every write to the Tx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a Transmit channel has been set up, packets can be added to the Queues for the channel to begin the transmit operation. The following sections describe how the transmit operations are performed for the various descriptor types.

11.1.4.5 PKTDMA - Transmit Channel Pause

Setting the tx_pause bit in the Tx Channel N Real-time Control Register (<TCHANRT[a]_TRT_CTL > [29] TX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potential underrun/overrun conditions from a downstream data sink or upstream data source.

11.1.4.6 PKTDMA - Transmit Channel Teardown

This section describes the teardown procedure for internal Tx channels within the PKTDMA. A Tx channel teardown is initiated by the host by writing the tx_teardown bit in the Tx Channel N Real-time Control Register (<TCHANRT[a]_TRT_CTL > [30] TX_TEARDOWN).

Once the host has written the tx_teardown bit, the PKTDMA will do the following:

1. Stops performing any additional descriptor fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/TR fetch has already been performed.
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.
4. Clears the channel enable in the Tx Channel N Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
7. If the current Tx reverse ring occupancy is 0, issues an Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current TX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
9. The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not.

The Host can determine that a teardown is complete by using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.7 PKTDMA - Transmit Operation

After a channel has been set up it can begin to be used to transmit packets. Packet transmission involves the following steps:

1. The Host is made aware of one or more chunks of data in memory that need to be transmitted as a packet. This may involve directly sourcing data from the Host or it may involve data which has been forwarded from another data source in the system.
2. The Host allocates and populates a host packet descriptor. The host will initialize the following fields within the packet descriptor:
   a. Descriptor Type (set to Host).
   b. Packet Length indicating the total number of bytes that are to be read from all of the buffers for this packet.
   c. Source Tag.
   d. Destination Tag.
   e. Packet Type.
   f. Any protocol specific flags for the given packet type.
   g. Buffer Pointer with the byte aligned address of the first chunk of buffer data.
   h. Buffer Length with the number of bytes in the first chunk of buffer data.
   i. The Next Descriptor Pointer with the 16-byte aligned address of the next descriptor in this packet. If this is the last chunk of data in the packet, this field must be set to zero.
   j. Any protocol specific descriptor sections that are required for the given packet type or system configuration.
3. The Host allocates and populates host buffer descriptors as necessary to point to any remaining chunks of data that belong to this packet. The host will initialize the following fields within the host buffer descriptor:

  a. Buffer Pointer with the byte aligned address of the given chunk of buffer data.
  b. Buffer Length with the number of bytes in the given chunk of buffer data.
  c. The Next Descriptor Pointer with the 16-byte aligned address of the next descriptor in this packet. If this is the last chunk of data in the packet, this field must be set to zero.

4. The Host writes queues the packet onto one of the Transmit Queues for the desired DMA channel. Channels may provide more than one Tx Queue (if more than 1 flow is provided) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller / scheduler implementation.
5. The PKTDMA internally generates a level sensitive status signal for the queue which indicates if any packets are currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
6. The PKTDMA Tx engine is eventually brought into context for the corresponding channel and begins to process the packet.
7. The PKTDMA reads the packet descriptor pointer from the memory mapped ring for that channel/flow.
8. The PKTDMA reads the packet descriptor from memory.
9. The PKTDMA empties each buffer in sequence by transmitting the contents in one or more block data moves. The size of these blocks is application specific. The PKTDMA module specification is intended to document the block size used by a given implementation. As each buffer is emptied, the PKTDMA will read the next buffer descriptor to obtain the pointer and size of the data buffer as well as the pointer to the next descriptor in the chain.
10. When all data for the packet has been transmitted as specified in the packet size field, the DMA will increment the occupancy of the reverse queue (Tx Completion Queue).
11. After the occupancy is incremented, the PKTDMA will indicate the status of the Tx Completion Queue by sending an up event.
12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_STATUS_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the PKTDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.
15. The PKTDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS) and potentially de-assert the interrupt line.

11.1.4.8 PKTDMA - Receive Free Descriptor / Buffer Queue Setup

The Host is ultimately responsible for providing all of the free descriptors and buffers that the port uses as it receives packets. Each entry on the Rx Free Descriptor/Buffer Queue consists of one or more descriptors chained together with each descriptor also pointing to a single contiguous buffer. Each entry on the Rx Free Descriptor/Buffer queue is intended to receive one packet of data. All chaining of descriptors within a packet is performed prior to placing the Rx resources onto the free queues.

Before the Host adds each Rx buffer descriptor chain to the queue, it must first initialize the Rx buffer descriptor values as follows:

- Write the Buffer Pointer with the byte aligned address of the buffer data
- Write the Buffer Size
- Write the next descriptor pointer to the next descriptor in the chain (non-eop) or to 0x0 (eop)

All other fields in the Descriptor do not need to be initialized as they will be overwritten by the Port on reception.

11.1.4.9 PKTDMA - Receive Channel Setup

After a reset or a previous teardown operation but before receiving packets on a channel the host must initialize the channel's Rx Port DMA State. The host initializes the channel Rx Port DMA State by writing to the Rx Channel Configuration Registers. The Host may choose to write the enable bit in the Rx Global Channel Configuration Register (<RCHANRT[a]_RRT_CTL> [31] RX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Rx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

11.1.4.10 PKTDMA - Receive Channel Teardown

An Rx channel teardown is intended to be initiated at the data source (the source thread). Initiation is commanded by the host by writing the teardown bit in the PSI-L source thread register 0x408 . This will cause the source of the data to gracefully terminate any packet that is in flight and send a PSI-L data phase with the tdown signal asserted. When the PKTDMA receives a data phase with the tdown attribute asserted it will immediately set the internal rx_teardown bit in the Rx Channel N Real-time Control Register (<RCHANRT[a]_RRT_CTL> [30] RX_TEARDOWN).

Once a teardown has been initiated, the PKTDMA will do the following:

1. Completes any packets normally which may be pending in the ingress port buffers (what the port considers as pending packets is application specific).
2. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL> [31] RX_ENABLE)**>**.
3. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
4. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register to indicate that a teardown has completed (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE).
5. If the current Rx reverse ring occupancy is 0, issues an Rx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
6. If the current RX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not. The normally intended method of issuing a teardown on a packet mode channel is to initiate the teardown at the remote PSI-L data source and allow it to flow into the PKTDMA. If that is not possible, the host may write the rx_teardown bit directly to a 1.

The Host determines that a teardown is complete by using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.11 PKTDMA - Receive Channel Pause

Setting the rx_pause bit in the Rx Channel N Control Register (<RCHANRT[a]_TRT_CTL> [29] RX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potential underrun/overrun conditions from a downstream data sink or upstream data source.

11.1.4.12 PKTDMA - Receive Operation

When packet reception begins on a given channel, the port will begin by fetching the descriptor and buffer from the ring for the channel / flow. If the SOP Buffer Offset in the Rx Flow Table entry is nonzero, then the port will begin writing data after the offset number of bytes in the SOP buffer. The port will then continue filling that buffer and will fill additional descriptors + buffers as needed using the pre-linked buffers in the packet.

A detailed summary is as follows:

1. Host allocates, populates, and places pointers to free descriptor/buffer structures onto Rx Free Descriptor/ Buffer Queues
2. PKTDMA fetches packet descriptor pointer from forward queue of ring for specified channel.
3. PKTDMA reads the packet descriptor to obtain the packet info, buffer pointer, buffer size, and next descriptor pointer.
4. PKTDMA fills the buffer with received data

If packet is not complete and the rx_chan_type field in the Rx Channel Configuration Register (<RCHAN[a]_RCFG> [19:16] RX_CHAN_TYPE) is set to 2 (Normal Rx Host Mode). The machine will proceed to step 5 and will repeat steps 5-6 until all packet data is received at which point the Rx engine proceeds to step 8. If the rx_desc_type is set to 3 (Single Buffer Packet Host Mode) the Rx engine will proceed directly to step 7 regardless of whether or not an end of packet terminator has been reached on the incoming data stream. The current packet will be completed following the sequence through step 12 and a new packet will be started back at step 1.

5. PKTDMA fetches next buffer descriptor using next descriptor pointer obtained from previous descriptor.

6. PKTDMA fills the buffer with received data.

The PKTDMA performs the following operations when the entire packet has been received:

7. PKTDMA writes the packet descriptor to memory. This includes the following fields:

a. Descriptor Type (set to Host)

b. Packet Length indicating the total number of bytes that are to be read from all of the buffers for this packet.

c. Source Tag

d. Destination Tag

e. Packet Type

f. Any protocol specific flags for the given packet type

g. Any protocol specific words that are required for the given packet type

h. Extended Packet Information (optional)

8. PKTDMA increments the occupancy of the reverse queue for the channel / flow.

9. Once the occupancy is incremented it will send an up event to the Interrupt Aggregator

10. The Interrupt Aggregator upon receiving the up event will set the appropriate bit in the Interrupt Status Register (VINT[a]_STATUS_SET) indicated by the interrupt mapping table which will cause an interrupt to be asserted to the Host

11.The Host will pop the packet pointer from the Rx Queue by reading the ring contents and then pushing a decrement to the reverse occupancy for the ring.

12. If the pop causes the queue to become empty, the PKTDMA will send a down event to the Interrupt Aggregator thus causing the associated bit to be cleared and also potentially clearing the interrupt to the Host.

11.1.4.13 BCDMA - Block Copy Channel Setup

This section describes the setup procedure for channels within the BCDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel's Port DMA State. The host initializes the channel Port DMA State by initializing all of the channel flow entries and then writing to the Block Copy Channel Configuration Register A (BCHANRT[a]_TRT_CTL). The Host may choose to write the enable bit in the Block Copy Channel Configuration Register A (<BCHANRT[a]_TRT_CTL> [31] TX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a channel has been set up, packets can be added to the Queues for the channel to begin the copy operation.

For general purpose block copy channels, only the Block Copy DMA configuration, flow, and real-time registers will be present. For split mode channels, separate Tx and Rx configuration, flow, and real-time registers are provided. In all cases, configuration of all fields must be completed before a channel is enabled.

11.1.4.14 BCDMA - Block Copy Channel Pause

Setting the pause bit in the Channel N Control Register (<BCHANRT[a]_TRT_CTL> [29] TX_PAUSE]) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.15 BCDMA - Block Copy Channel Teardown

This section describes the teardown procedure for generic block copy channels within the BCDMA. A channel teardown is initiated by the host by writing the teardown bit in the Channel N Real-time Control Register (<BCHANRT[a]_TRT_CTL> [30] TX_TEARDOWN). When the host initiates teardown, it can choose to perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the forced_teardown bit in the Channel N Real-time Control Register (<BCHANRT[a]_TRT_CTL> [28] TX_FORCED_TEARDOWN).

If the forced_teardown bit is clear, a normal teardown has been initiated. In this case, the BCDMA will do the following:

1. Stops performing any additional fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/data fetch has already been performed
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.
4. Clears the channel enable in the Channel N Global Configuration Register (<BCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the BC Flow Reverse Ring Occupancy register to indicate that a teardown has completed.
7. If the current BC reverse ring occupancy is 0, issues an BC reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current BC Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
9. If the forced_teardown bit is set, a destructive teardown has been initiated. In this case, the BCDMA will do the following:
    a. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
    b. Completes any packets which have been fetched with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation).
    c. Clears the channel enable in the Channel Global Configuration Register.
    d. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
    e. Sets bit 31 of the BC Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
    f. If the current BC reverse ring occupancy is 0, issues an BC reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

    The host may issue a teardown on any channel at any time, regardless of whether the channel is actively transferring data or not.

    The Host determines that a teardown using either of the following methods:

    a. Periodically polling the teardown and enable bits for the channel
    b. Waiting for an interrupt and observing the teardown complete bit is set in the channel’s default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

    Note that the teardown message will actually be written to the next available location in the ring following the last completed packet.

11.1.4.16 BCDMA - Block Copy Operation (TR Packet)

Packet transmission in TR Packet mode involves the following steps:

1. The Host allocates and populates a type 15 TR packet descriptor. The host will initialize the following fields within the packet descriptor:
    a. Descriptor Type (set to TR)
    b. Reload Enable to 1 if looping is required, otherwise 0
    c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
    d. Last Entry to TR count minus 1
    e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
    f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Block Copy Queues for the desired BCDMA channel. Channels may provide more than one Queue (1 queue per provided flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller/scheduler implementation.
3. The BCDMA internally provides a level sensitive status signal for the queue which indicates if any work is currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
4. The DMA controller is eventually brought into context for the corresponding read channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller sequentially empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves. As a TR is read from the descriptor, it is stored in the internal state of the DMA channel until it is completed.
8. All of the data transfers specified in a TR will be completed as a series of reads followed later on by a set of corresponding writes (which may or may not be the same size based on the parameters in the block copy TR).
9. The BCDMA will wait until write status returns for the final write operation that was initiated for each TR. When the final write status is returned within each TR, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.
10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the BCDMA will increment the reverse occupancy for the channel/flow.
11. After the occupancy is incremented, the BCDMA will indicate the status of the Tx Completion Queue by sending an up event.
12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_STATUS_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the BCDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.
15. The BCDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS) and potentially de-assert the interrupt line

11.1.4.17 BCDMA - Block Copy Error/Exception Handling

There are 3 specific errors which may be encountered during generic block copy operation and which are trapped by the BCDMA. The following table lists the errors and how the BCDMA will process them:

Table 11-58. BCDMA Generic Block Copy Mode Error / Exception Handling

Condition	Pauses Channel	Error Flag Set in Channel	Data Transfer	TR Flush	Outputs Transfer Events
TR null icnt0	Selectable(1)	Yes	No	Just that TR	No

Table 11-58. BCDMA Generic Block Copy Mode Error / Exception Handling (continued)

Condition	Pauses Channel	Error Flag Set in Channel	Data Transfer	TR Flush	Outputs Transfer Events
Unsupported TR Type	Selectable[1]	Yes	No	Just that TR	No
Bus Errors	Selectable[1]	Yes	Yes	No	Yes

(1) If pause_on_error bit is set in channel configuration

11.1.4.17.1 Null Icnt0 Error

The icnt0 parameter in a TR is never allowed to be 0 as this would cause zero byte count transactions to be issued on the bus and is unproductive wrt completion of any useful work. The Block Copy engine in the BCDMA will trap any TR for which the icnt0 is zero and will immediately return a transfer response with the TR icnt0 error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.17.2 Unsupported TR Type

If a TR is provided to a channel which is of a type which is not supported by the channel, the Block Copy engine in the BCDMA will trap that TR and immediately return a transfer response with the Unsupported TR error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.17.3 Bus Errors

If a bus error is encountered during transmit the BCDMA will log the error by asserting the tx_error bit for the channel (and optionally sending an error event if enabled) but the DMA will continue to attempt to complete the transfer using the returned (and potentially incorrect) data.

11.1.4.18 BCDMA - Split Transmit Channel Setup

This section describes the setup procedure for split Tx channels within the BCDMA. After a reset or a previous teardown operation but before queuing packets to a channel the host must initialize the channel's Tx Port DMA State. The host initializes the channel Tx Port DMA State by configuring all of the Tx flow entries for the channel and then writing to the Tx Channel Configuration Register A (TCHANRT[a]_TRT_CTL). The Host may choose to write the enable bit in the Tx Channel Configuration Register A (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Tx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

After a Transmit channel has been set up, packets can be added to the Queues for the channel to begin the transmit operation. The following sections describe how the transmit operations are performed for the various descriptor types.

11.1.4.19 BCDMA - Split Transmit Operation Pause

Setting the pause bit in the Channel N Control Register (<TCHANRT[a]_TRT_CTL> [29] TX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.20 BCDMA - Split Transmit Channel Teardown

This section describes the teardown procedure for split mode Tx channels within the BCDMA. A Tx channel teardown is initiated by the host by writing the tx_teardown bit in the Tx Channel N Real-time Control Register (<TCHANRT[a]_TRT_CTL> [30] TX_TEARDOWN). When the host initiates teardown, it can choose to perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the tx_forced_teardown bit in the Tx Channel N Real-time Control Register (<TCHANRT[a]_TRT_CTL> [28] TX_FORCED_TEARDOWN) .

If the tx_forced_teardown bit is clear, a normal teardown has been initiated. In this case, the DMA will do the following:

1. Stops performing any additional descriptor fetches for the channel.
2. Completes any packets normally for which a pointer/descriptor/TR fetch has already been performed
3. Sets the tdown bit on the EOP data phase of the last packet to be sent (if any traffic was pending when teardown was initiated) or sends a zero byte packet with the tdown, sop, and eop bits asserted. This signals the destination thread that all of the data has been sent.
4. Clears the channel enable in the Tx Channel N Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
5. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
6. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
7. If the current Tx reverse ring occupancy is 0, issues a Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
8. If the current TX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
9. If the tx_forced_teardown bit is set (only valid on BCDMA), a destructive teardown has been initiated. In this case, the BCDMA will do the following:

1. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
2. Completes any packets which have been prefetched with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation).
3. Clears the channel enable in the Tx Channel Global Configuration Register (<TCHANRT[a]_TRT_CTL> [31] TX_ENABLE).
4. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
5. Sets bit 31 of the Tx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
6. If the current Tx reverse ring occupancy is 0, issues a Tx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not.

The Host determines that a teardown using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel's default flow (first flow in channel) reverse occupancy register (RINGRT[a]_RT_ROCC) for the channel.

11.1.4.21 BCDMA - Split Transmit Operation (TR Packet)

Packet transmission in TR Packet mode involves the following steps:

1. The Host allocates and populates a TR packet descriptor. The host will initialize the following fields within the packet descriptor:
    a. Descriptor Type (set to TR)
    b. Reload Enable to 1 if looping is required, otherwise 0
    c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
    d. Last Entry to TR count minus 1
    e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
    f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Transmit Queues for the desired BCDMA channel. Channels may provide more than one Queue (1 queue per provided flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller/ scheduler implementation.
3. The BCDMA internally provides a level sensitive status signal for the queue which indicates if any work is currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.

4. The DMA controller is eventually brought into context for the corresponding read channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller sequentially empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves. As a TR is read from the descriptor, it is stored in the internal state of the DMA channel until it is completed.
8. All of the data transfers specified in a TR will be completed as a series of reads.
9. The BCDMA will wait until data returns for each read operation that has been initiated. When the final read operation is returned within each TR, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.
10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the BCDMA will increment the reverse occupancy for the channel / flow.
11. After the occupancy is incremented, the BCDMA will indicate the status of the Tx Completion Queue by sending an up event.
12. The Interrupt Aggregator receives the up event and sets the corresponding bit in the interrupt status register (VINT[a]_ENABLE_SET) as programmed in the interrupt mapping registers. This in turn causes an interrupt to the Host to be generated.
13. The Host responds to the status change from the BCDMA (via the Interrupt Aggregator) and performs garbage collection as necessary for the packet.
14. During garbage collection the Host will write to the reverse queue Doorbell register (RINGRT[a]_RT_RDB) for the channel/flow to acknowledge the popping of those completed packets. The doorbell writes eventually cause the queue to become empty.
15. The BCDMA will send a down event to the Interrupt Aggregator which will clear the corresponding bit in the Interrupt Status Register (VINT[a]_STATUS) and potentially de-assert the interrupt line.

11.1.4.22 BCDMA - Split Transmit Error / Exception Handling

There are 3 specific errors which may be encountered during Tx split operation and which are trapped by the BCDMA. The following table lists the errors and how the BCDMA will process them:

Table 11-59. BCDMA Tx Error / Exception Handling

Condition	Pauses Channel	Error Flag Set in Channel	Data Transfer	TR Flush	Outputs Transfer Events
TR null icnt0	Selectable(1)	Yes	No	Just that TR	No
Unsupported TR Type	Selectable(1)	Yes	No	Just that TR	No
Bus Errors	Selectable(1)	Yes	Yes	No	Yes

(1) If pause_on_error bit is set in channel configuration

11.1.4.22.1 Null Icnt0 Error

The icnt0 parameter in a TR is never allowed to be 0 as this would cause zero byte count transactions to be issued on the bus and is unproductive wrt completion of any useful work. The Block Copy engine in the BCDMA will trap any TR for which the icnt0 is zero and will immediately return a transfer response with the TR icnt0 error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.22.2 Unsupported TR Type

If a TR is provided to a channel which is of a type which is not supported by the channel, the Block Copy engine in the BCDMA will trap that TR and immediately return a transfer response with the Unsupported TR error conditions set without performing any data transfer and without outputting any events (including end of TR event).

11.1.4.22.3 Bus Errors

If a bus error is encountered during transmit the BCDMA will log the error by asserting the tx_error bit for the channel (and optionally sending an error event if enabled) but the DMA will continue to attempt to complete the transfer using the returned (and potentially incorrect) data.

11.1.4.23 BCDMA - Split Receive Channel Setup

After a reset or a previous teardown operation but before receiving packets on a channel the host must initialize the channel's Rx Port DMA State. The host initializes the channel Rx Port DMA State by writing to the Rx Channel Configuration Registers. The Host may choose to write the enable bit in the Rx Global Channel Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE) at the same time or after it has written all of the channel parameters but note that every write to the Rx Channel Configuration Registers will overwrite the channel state for all bytes that are enabled for the write transaction.

11.1.4.24 BCDMA - Split Receive Channel Pause

Setting the pause bit in the Channel N Control Register (<RCHANRT[a]_RRT_CTL > [29] RX_PAUSE) will suspend the channel from arbitration resulting in a halting of the flow of data. Clearing this bit will cause the channel to be added back into the arbitration list. Pausing a channel has no other destructive side effects (other than potentially overflowing trigger events.

11.1.4.25 BCDMA - Split Receive Channel Teardown

An Rx channel teardown is intended to be initiated at the data source (the source thread). Initiation is commanded by the host by writing the teardown bit in the PSI-L source thread register 0x408 . This will cause the source of the data to gracefully terminate any packet that is in flight and send a PSI-L data phase with the tdown signal asserted. When the BCDMA receives a data phase with the tdown attribute asserted it will immediately set the internal rx_teardown bit in the Rx Channel N Real-time Control Register (<RCHANRT[a]_RRT_CTL > [30] RX_TEARDOWN).

Upon seeing the rx_teardown bit asserted the port can perform either a graceful (no data loss) or forced teardown of the channel depending on the setting of the rx_forced_teardown bit in the Rx Channel N Real-time Control Register (<RCHANRT[a]_RRT_CTL > [28] RX_FORCED_TEARDOWN).

If the rx_forced_teardown bit is clear, a normal teardown has been initiated. In this case, the BCDMA will do the following:

1. Stops performing any additional prefetches for the channel (TR mode channels)
2. Completes any packets normally which may be pending in the ingress port buffers (what the port considers as pending packets is application specific).
3. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE).
4. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
5. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
6. If the current Rx reverse ring occupancy is 0, issues an Rx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.
7. If the current RX Reverse ring occupancy is not 0 then a write to the doorbell with a negative value of the current occupancy will clear any remaining work but the forward ring pointer will remain the same. If the ring pointer needs to be reset then perform a write to any of the ring configuration registers.
8. If the rx_forced_teardown bit is set, a destructive teardown has been initiated. In this case, the BCDMA will do the following:

    a. Suspends any triggers to allow the channel to operate even if the trigger source is no longer functioning.
    b. Completes any packets which may be pending in the ingress port buffers with or without transferring any data or generating events (the implementation has the option of doing whichever is simplest for that implementation) . Packets will be drained from the Rx FIFO either using 'null' write transfers or real transfers and the Packet Descriptors will be returned with an accurate accounting of actual bytes transferred.
    c. Clears the channel enable in the Rx Channel Global Configuration Register (<RCHANRT[a]_RRT_CTL > [31] RX_ENABLE).

  d. Resets the channel state (including scoreboards, FIFOs, counters, statistics, etc.) to their after reset values.
  e. Sets bit 31 of the Rx Flow Reverse Ring Occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) to indicate that a teardown has completed.
  f. If the current Rx reverse ring occupancy is 0, issues an Rx reverse ring completion up event which is then routed to an IA and can be further routed to any event consumer.

The host may issue a teardown on any channel at any time, regardless of whether the channel is actively receiving a packet or not. The normally intended method of issuing a teardown on a packet mode channel is to initiate the teardown at the remote PSI-L data source and allow it to flow into the BCDMA. If that is not possible, the host may write the rx_teardown bit directly to a 1.

The Host determines that a teardown using either of the following methods:

1. Periodically polling the teardown and enable bits for the channel
2. Waiting for an interrupt and observing the teardown complete bit is set in the channel’s default flow (first flow in channel) reverse occupancy register (<RINGRT[a]_RT_ROCC> [31] TDOWN_COMPLETE) for the channel.

11.1.4.26 BCDMA - Split Receive Operation (TR Packet)

Packet reception in TR Packet mode involves the following steps:

1. The Host allocates and populates a TR packet descriptor. The host will initialize the following fields within the packet descriptor:
   a. Descriptor Type (set to TR)
   b. Reload Enable to 1 if looping is required, otherwise 0
   c. Reload Index to an appropriate offset if Reload Enable set, otherwise 0
   d. Last Entry to TR count minus 1
   e. TR Nominal Element Size to a value that is as large as required for any given TR in the buffer
   f. A set of one or more valid Transfer Request records whose quantity matches the last index specified previously.
2. The Host queues the packet onto one of the Rx TR Queues for the desired BCDMA channel. Channels may provide more than one Rx TR Queue (one per flow) and may provide a particular prioritization policy between the queues. This behavior is application specific and is controlled by the DMA controller / scheduler implementation.
3. The Ring Accelerator provides a level sensitive status signal for the queue which indicates if any packets are currently pending. This level sensitive status line is sent to the hardware block which is responsible for scheduling DMA operations.
4. The DMA controller is eventually brought into context for the corresponding channel and begins to process the packet.
5. The DMA controller reads the packet descriptor pointer from the ring in memory.
6. The DMA controller reads the packet descriptor from memory
7. The DMA controller empties the data region in the descriptor by reading the contents in one or more nominal TR sized block data moves.
8. All of the data transfers specified in a TR will be completed as a series of writes and a Transfer Response will be returned indicating the completion and status of the transfer.
9. The BCDMA will wait until Transfer Responses have been returned for each Transfer Request that it issued. As each Transfer Response is returned, the BCDMA will write the response into the TR buffer in the Transfer Response records array. Each response is written into an array index which directly matches the index of the request record to which is corresponds.
10. When all Transfer Requests in the packet have been processed and all Transfer Responses have been written back and confirmed to have landed in memory, the DMSS will write the pointer to the packet descriptor to the queue specified in the return queue number fields of the packet descriptor.
11. After the Packet Descriptor pointer has been written, the Ring Accelerator indicates the status of the Rx Completion Queues to other ports / processors / prefetcher blocks using events sent to the Interrupt Aggregator. These events are then converted into standard interrupts.

11.1.4.27 BCDMA - Split Receive Error / Exception Handling

Several types of errors/exceptions may be encountered during reception of split Rx data. The following table outlines the various errors and exceptions that can occur:

Table 11-60. Rx Error / Exception Handling

Condition	Channel Type	Severity	Pauses Channel	Error Flag Set	Data Transfer	Data Flush	TR Flush	Event Output
Descriptor Starvation	All Packet	Exception	No	No	Option	Option	-	No
Protocol Errors	All Packet	Info	No	No	Normal	No	-	No
Drop	Host – normal	Exception	No	No	Partial(1)	Until EOP	-	No
EOP Asserted Late (Long Packet)	BCDMA – single ended	Exception	No	No	Partial	Excess	No	Yes
TR null icnt0	All BCDMA	Error	Selectable(1)	Yes	No	No	Just that TR	No
Unsupported TR Type	All BCDMA	Error	Selectable(1)	Yes	No	No	Just that TR	No

(1) Data will not be transferred after drop is detected. All data after that point is guaranteed to be flushed and some data prior to the exact data phase on PSI-L where drop was asserted may also be flushed since data is constantly accumulated so it can be transferred in chunks.

11.1.4.27.1 PKTDMA Exception Conditions

There are a few cases which can occur when processing incoming packets which are not considered errors but which will require handling in order to avoid locking up the PKTDMA engines.

Packet mode channel exceptions include:

- Descriptor Starvation
- Protocol Errors
- Dropped Packets
- Long Packets

11.1.4.27.1.1 Descriptor Starvation

Descriptor starvation occurs when the Port needs to fetch a free descriptor from the RX ring and none are available. When the port detects that descriptor starvation has occurred it will react based on the value of the rx_error_handling bit which was programmed into the Rx Flow N Configuration Register A (<RFLOW[a]_RFA> [28] RX_ERROR_HANDLING).

If the rx_error_handling bit is cleared:

- The Port will increment an internal per-channel starvation counter and will then flush the packet.

If the rx_error_handling bit is set:

- The Port will assert a RX descriptor starvation event (which may cause an interrupt to the Host) and will then wait for the doorbell for the selected flow to be written with a positive value. Note that the intention is that the port will wait for an entry to be added to the ring. It is assumed that when in this mode, if data loss is not desired that the host will guarantee that a chain of buffers will be provided that can receive the entire packet.

11.1.4.27.1.2 Protocol Errors

Protocol errors occur when the port logic detects that the received packet did not pass protocol specific criteria that was checked during reception of the packet. Examples of protocol errors include packet length errors, CRC errors, or alignment errors.

When protocol errors are detected, the port may choose whether or not it will drop the packet. The mechanism that is used to determine which packets to drop and which to forward is application specific. If the port determines that it needs to forward the packet to the Host, it will set the Packet Error bit in the Descriptor indicating that this is a packet which experienced a protocol related error. The type of protocol related error is generally indicated in either the Protocol Specific bits in the Host descriptor or in the Protocol Specific bytes region. The packet length information and certain portions of the Protocol Specific region may not be correct for packets which encounter errors.

11.1.4.27.1.3 Dropped Packets

Packets can be dropped within an Rx Port for any number for reasons which with the exception of the starvation case which was covered above are application specific.

When a Port determines that it needs to drop a packet after reception of the packet has begun, it must flush the remainder of the packet, increment the dropped packets statistic, and rewind any fetched descriptor/buffer chain so that the it can be use the same descriptor/buffer chain on the next packet.

11.1.4.27.1.4 Long Packet

For Rx channels which are not configured in single buffer mode, if the host provides a buffer chain whose total length is insufficient to receive the entire packet, whatever portion of the packet which has not been received will be flushed until an end of packet indicator is received on the PSI-L interface. This behavior will occur regardless of which error handling mode has been selected for the channel.

11.1.4.27.2 BCDMA Exception Conditions

Since the TR mode engine performs transfer sequencing using a count based mechanism it is susceptible to becoming out of synchronization if the source of the data and the destination for the data do not exactly match in their expectations for how much data will be transferred. The following sections outline these scenarios.

TR mode channel exceptions include:

- Reception of EOL delimiter
- Short Packets
- Long Packets
- Descriptor Starvation

11.1.4.27.2.1 Reception of EOL Delimiter

If an end of line delimiter is received by the Rx (write) side of the BCDMA the EOL_ADV field in the TR application specific flags field is used to advance the appropriate indices of the TR to the next level. Each EOL that is received will cause the TR to advance to the next specified loop iteration breaking as many intermediate loops as are required.

11.1.4.27.2.2 EOP Asserted Prematurely (Short Packet)

Split TR mode channels can experience an incoming packet whose length is shorter than what was expected based on one or more TRs which form the control description for the expected packet. If an EOP is received for a TR and the TR has not been completely executed, the port is required to receive as much data as is actually provided in the incoming data placing it in accordance with the instructions in the TR and the to continue executing any remaining TR(s) such that the required events are produced to keep downstream consumers in sync. In this case, no data will be transferred to the buffers described by the TR beyond what was provided in the incoming packet.

11.1.4.27.2.3 EOP Asserted Late (Long Packets)

Split TR mode channels can experience an incoming packet whose length is longer than what was expected based on one or more TRs which form the control description for the expected packet. If a TR completes and is marked as EOP but the incoming packet is not finished, then the port must throw away any additional received data until the incoming packet reaches an EOP condition. At this point, reception will start with a new TR and a new incoming packet.

11.1.4.27.2.4 Descriptor Starvation

Descriptor starvation occurs when the Port receives enough data for a burst but the ring for the channel is currently empty. This causes push back on the receive port and can cause lost data.

The Port will assert a starvation bit in the RX Receive Channel Status register (RCHANRT[a]_RRT_STATUS[1-0]). When the doorbell register (RINGRT[a]_RT_DB) is written to populate the ring the starvation bit will clear. Note that the intention is that the port will wait for an entry to be added to the ring. It is assumed that if data loss is not desired that the host will guarantee that a descriptor is present.

11.2 Data Movement Subsystem (DMSS)

This chapter describes the Data Movement Subsystem (DMSS) module in the device.

11.2.1 Data Movement Subsystem (DMSS)

This chapter describes the features and functions of the Data Movement Subsystem (DMSS) hardware modules in the device.

11.2.1.1 DMSS Overview

The DMSS module provides data movement (DMA) and bridges between the CBA switched interconnect and the packet streaming fabric (network on chip) on the device.

The Data Movement Subsystem (DMSS) consists of DMA/Queue Management components and Peripherals:

- Packet DMA
- Block Copy DMA
- Ring Accelerator
- Packet Streaming Interface (PSILSS)
- Infrastructure components such as CBASS, secure proxy, and an interrupt aggregator

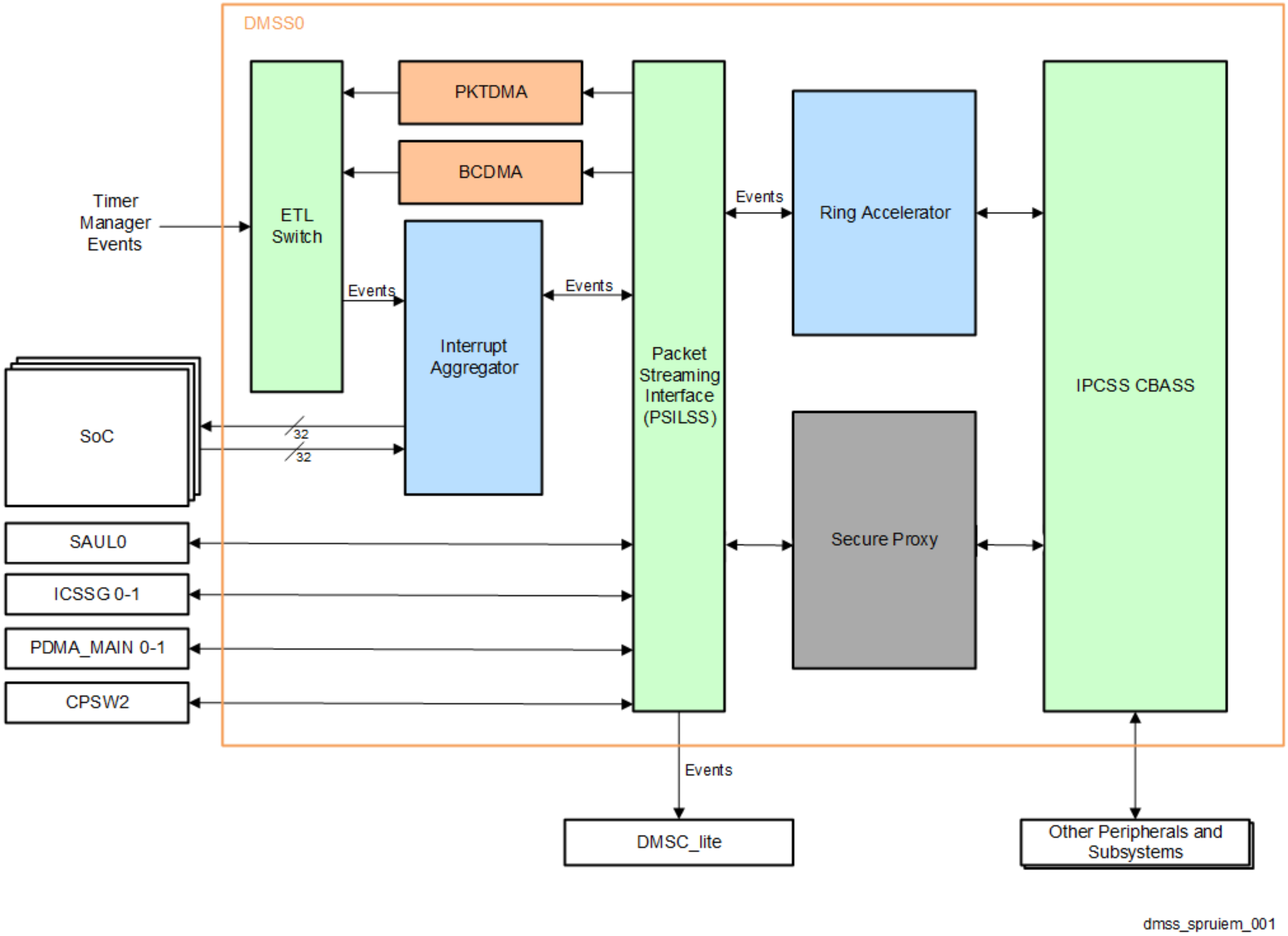


Figure 11-4. DMSS Top-Level Block Diagram

Table 11-61. DMSS Allocation Within Device Domain

Module Instance	Domain
	MAIN
DMSS0	✓(DMSS)

Note

Some features may not be available. See *Module Integration* for more information.

11.2.1.2 DMSS Functional Description

See *Data Movement Architecture*, for the TI Data Movement Architecture (DMA) specification.

See the following sections for the respective module description:

- PKTDMA - Section 11.1.1.4
- BCDMA - Section 11.1.1.5
- Ring Accelerator:
  - See Section 11.1.1.1 for a summary overview of the Ring accelerator.
  - SeeSection 11.2.2 for a full chapter breakdown of the Ring accelerator.
  - See Section 11.2.2.1 for a block diagram overview.
  - See Section 11.2.2.1.1 for a list of features.
  - See Section 11.2.2.2 for a functional description of the Ring Accelerator.
- Infrastructure Components:
  - CBASS
  - Secure Proxy:
    - See Section 11.1.1.2 for a summary overview of the Secure Proxy.
    - See Section 11.2.3 for a full chapter breakdown of the Secure Proxy.
    - SeeSection 11.2.3.1.1 for a list of features.
    - See Section 11.2.3.2 for a functional description of the Secure Proxy.
  - Interrupt Aggregator
    - See Section 11.1.1.3 for a summary overview of the Interrupt Aggregator.
    - See Section 11.2.4 for a full chapter breakdown of the Interrupt Aggregator.
    - SeeSection 11.2.4.1.1 for a list of features.
    - See Section 11.2.4.2 for a functional description of the Interrupt Aggregator.

11.2.1.3 DMSS Interrupt Configuration

This section describes the actions needed to configure interrupts within the DMSS.

Table 11-62. DMSS Parameters

Parameter	Value DMSS	Description
RA_RING_CNT	20	Number of total rings supported (specific to each ring accelerator)
IA_SEVI	1536	Interrupt Aggregator Source Event Input (SEVI) count (specific to each interrupt aggregator)
IS_VINTR	184	Interrupt Aggregator Virtual Interrupt (VINTR) count (specific to each interrupt aggregator)
EO	See *Global Event Map* in Module Integration	Event offset

DMSS Software Variables lists software-configurable variables used in the examples and descriptions.

Table 11-63. DMSS Software Variables

Variable	Valid Range	Description
R#	0 to RA_RING_CNT-1	Ring number
E#	0 to (destination module specific)	Event number
GE#	= EO + E#	Global event number

Table 11-63. DMSS Software Variables (continued)

Variable	Valid Range	Description
SB#	0 to IA_SEVI-1	Interrupt aggregator status bit number
VI#	0 to IA_VINTR-1	Virtual interrupt number

11.2.1.3.1 DMSS Event and Interrupt Flow

DMSS Interrupt Flow illustrates the event and interrupt flow within the DMSS and output interrupts to a CPU.

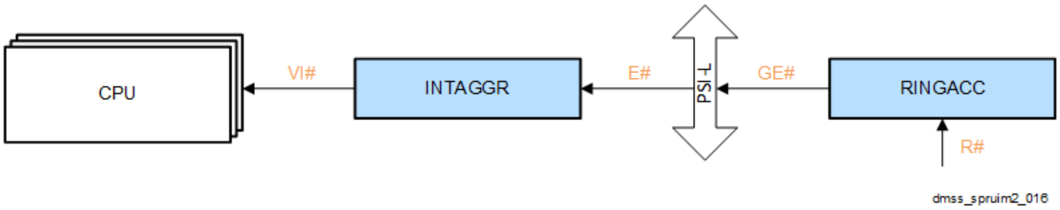


Figure 11-5. DMSS Interrupt Flow

11.2.1.3.1.1 DMSS Interrupt Description

This section describes the interrupt-related information that flows within DMSS and how this information is configured or generated.

1. **Ring Number (R#):**
   - Data is read from and written to a specific Ring Accelerator ring using direct ring-mode, or secure proxy access
   - The Ring Accelerator has specific ring number ranges for specific purposes. The R# must match the intended purpose of the ring (see Table 10-578, RINGACC Ring Mapping)
2. **Global Event and Event Numbers (GE# and E#):**
   - GE# = EO + E#
   - EO determines the destination module for the event. The PSILSS will route the GE# to the destination module per the DMSS event mapping, removing EO in the process. The destination module sees only E#. See *Global Event Map* in *Module Integration* for details.
   - For the INTAGGR module, E# ranges from 0 to (IA_SEVI - 1)
3. **Virtual Interrupt (VI#)**
   - The INTAGGR maps E# (via software configuration) to any SB#
   - ranges from 0 to (IA_SEVI - 1)
   - Each VI# (0 – (IA_VINTR-1)) is driven by a group of 64 contiguous SB# numbers (VI# driven by SB#'s VI#×64 – (VI#×64)+63)

11.2.1.3.1.2 DMSS Event Description

1. Interrupt aggregator includes two orthogonal functions:
   a. Event mapping block which converts local/umapped events to global events, and sends those events out.
   b. Aggregating global events and convert them into interrupt outputs.

2. L2G Block: This block converts the event/interrupt from SoC level into global events. L2G block takes wired signal from SoC (interrupt signal or DMA signal) converted into local events. Those local events are sent to ETL and sent to event mapping logic inside interrupt aggregator to convert them into global event. And then those global events are sent out again.
3. PSIL and ETL: PSIL is a streaming protocol which carries both data information and event information. ETL is the PSIL portion which only carries event. PSIL data is transported independently. When you see PSIL, it must include ETL.
4. Local events and unmapped events are in the same category. All those unmapped/local events are routed to the mapping block inside Interrupt aggregator to be converted into global events

5. Other than L2G block, Currently there are only three components generating unmapped events: BCDMA, PktDMA and timer manager. All those unmapped events are routed to the event mapping block inside interrupt aggregator first. All the other components produce global events.
6. After the local/unmapped events are mapped to global events in interrupt aggregator, those global events are sent out by interrupt aggregator and can be transported to different locations (for example, BCDMA to trigger BCDMA or pktDMA or going back to interrupt aggregator's aggregating global events into interrupts.

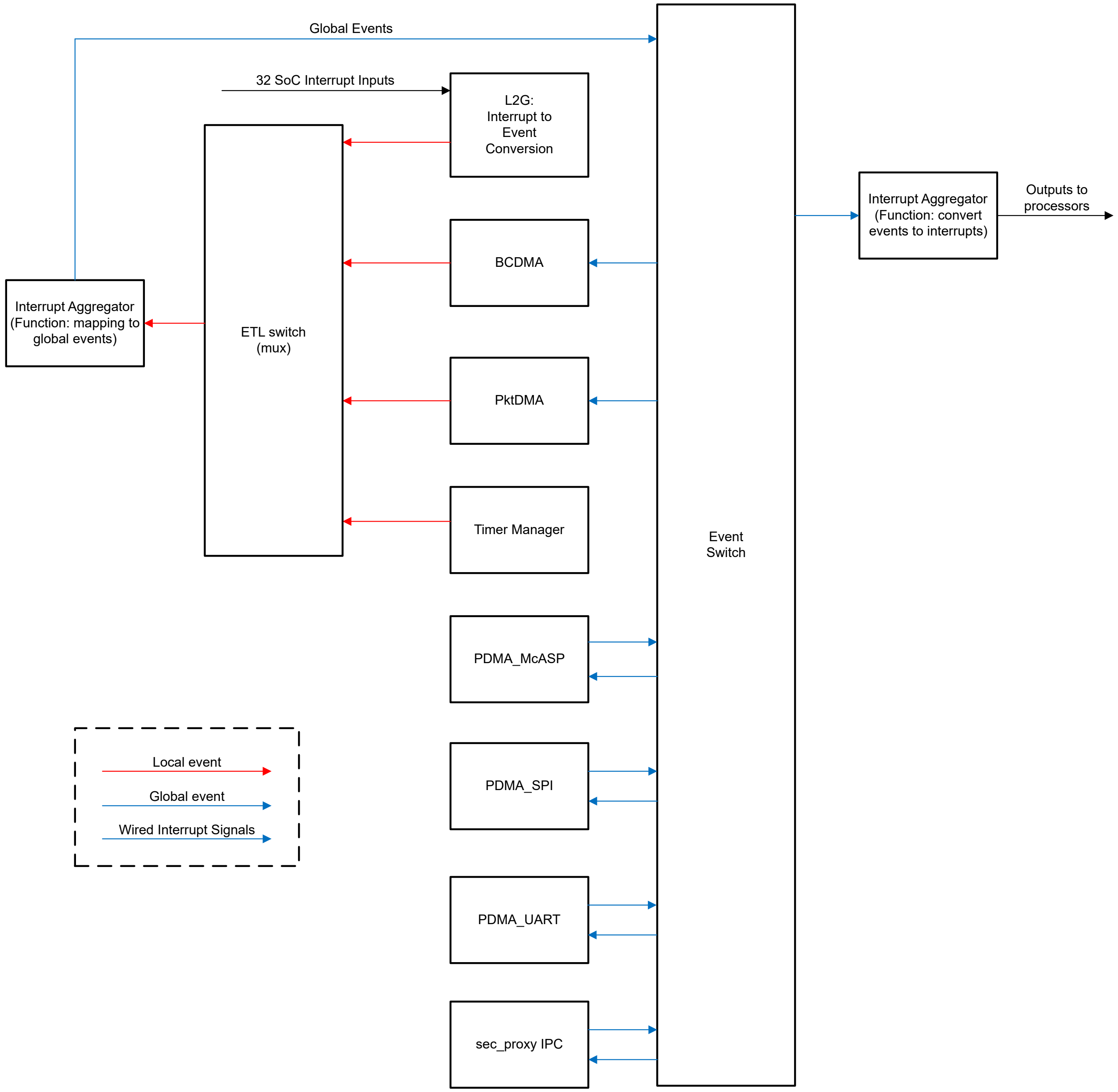


Figure 11-6. DMSS Event Flow

11.2.2 Ring Accelerator (RINGACC)

This chapter describes the RINGACC module, part of the DMSS.

Note

Not all of the RINGACC Functions specified in the document are supported in the device. Updates will be included in the next revision to reflect only supported modes of operation.

11.2.2.1 RINGACC Overview

The Ring Accelerator (RINGACC or RA) provides hardware acceleration to enable straightforward passing of work between a producer and a consumer.

Table 11-64. RINGACC Allocation Within Device Domain

Module Instance	Domain
	MAIN
DMSS0_RINGACC0	✓(DMSS)

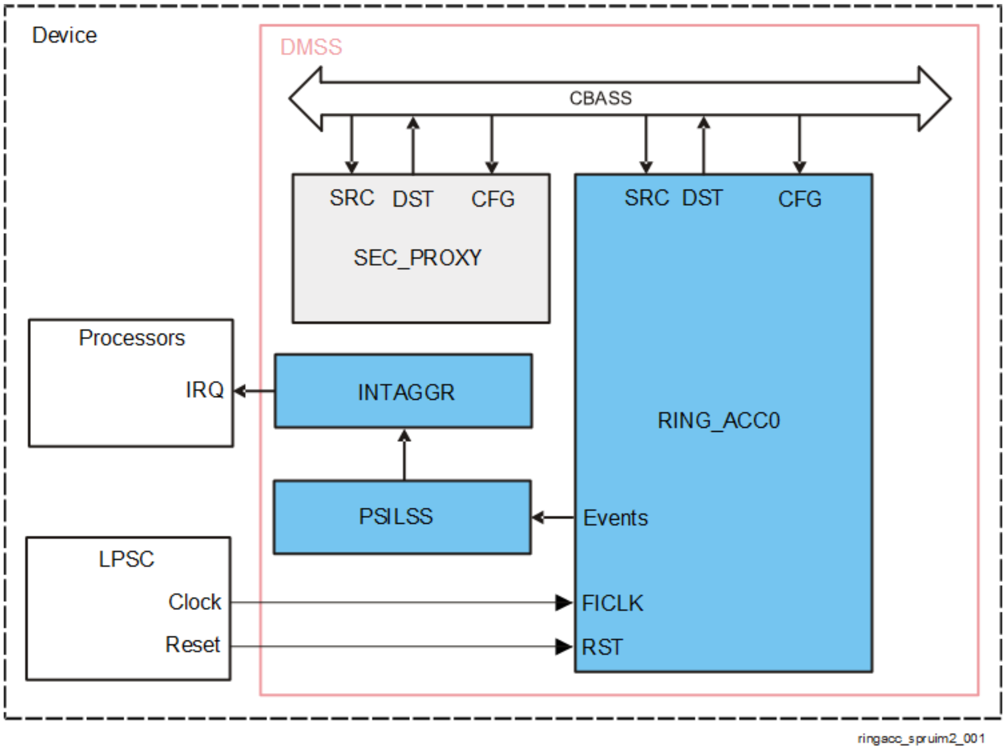


Figure 11-7. RINGACC Overview

11.2.2.1.1 RINGACC Features

- Ring Accelerator implementation
  - Supports up to 32 independent memory mapped ring structure
  - Supports various modes for each ring based on usage and compatibility
  - Provides single word deep shared incoming Transfer Response FIFO
  - Optionally supports dynamic clock gating
  - Provides bit wide source VBUSM read/write target interface for accesses from DMA controller entities
    - Provides 2 word deep command FIFO
    - Provides 2 word deep write data FIFO
    - Provides 2 word deep read data FIFO
    - Provides 2 word deep write status FIFO

- Provides bit wide destination VBUSM read/write initiator interface for accesses to ring structures in memory
- Supports up to 16 outstanding writes
- Supports up to 16 outstanding reads
- Provides 2 word deep command FIFO
- Provides 2 word deep write data FIFO
- Provides 2 word deep read data FIFO
- Provides 2 word deep write status FIFO
- Source interface provides an array of 32x512-byte long address windows (four for each ring) which are packed into a single contiguous address range.
  - Read and write addresses which target a specific window are mangled to redirect the read or write transaction to an effective address calculated from the base address for the ring plus current ring offset.
  - Each read or write access presented on VBUSM target interface is modified and bridged onto the VBUSM initiator interface.

Note

Some features may not be available. See *Module Integration* for more information.

11.2.2.1.2 RINGACC Parameters

Table 11-65 shows the RINGACC configuration parameters in this SoC

Table 11-65. RINGACC Configuration Parameters

Module Instance	Parameters			
	Ring Count	Number of Monitors	mem_dpwdth	FIFO Endpoint Address
DMSS0_RINGACC0	20	0	64	0x400000

11.2.2.2 RINGACC Functional Description

The Ring Accelerator (RINGACC) converts constant-address read and write accesses to equivalent read or write accesses to a circular data structure in memory. The RINGACC eliminates the need for each DMA controller which needs to access ring elements from having to know the current state of the ring (base address, current offset). The DMA controller performs a read or write access to a specific address range (which maps to the source interface on the RINGACC) and the RINGACC replaces the address for the transaction with a new address which corresponds to the head or tail element of the ring (head for reads, tail for writes). Since the RINGACC maintains the state, multiple DMA controllers or channels are allowed to coherently share the same rings as applicable. The RINGACC serves a very similar function to the Queue Manager in the earlier SoCs. The RINGACC uses less memory and is able to place data which is destined towards software into cached memory directly.

11.2.2.2.1 Block Diagram

Ring Accelerator Block-Diagram shows ring accelerator's main internal components.

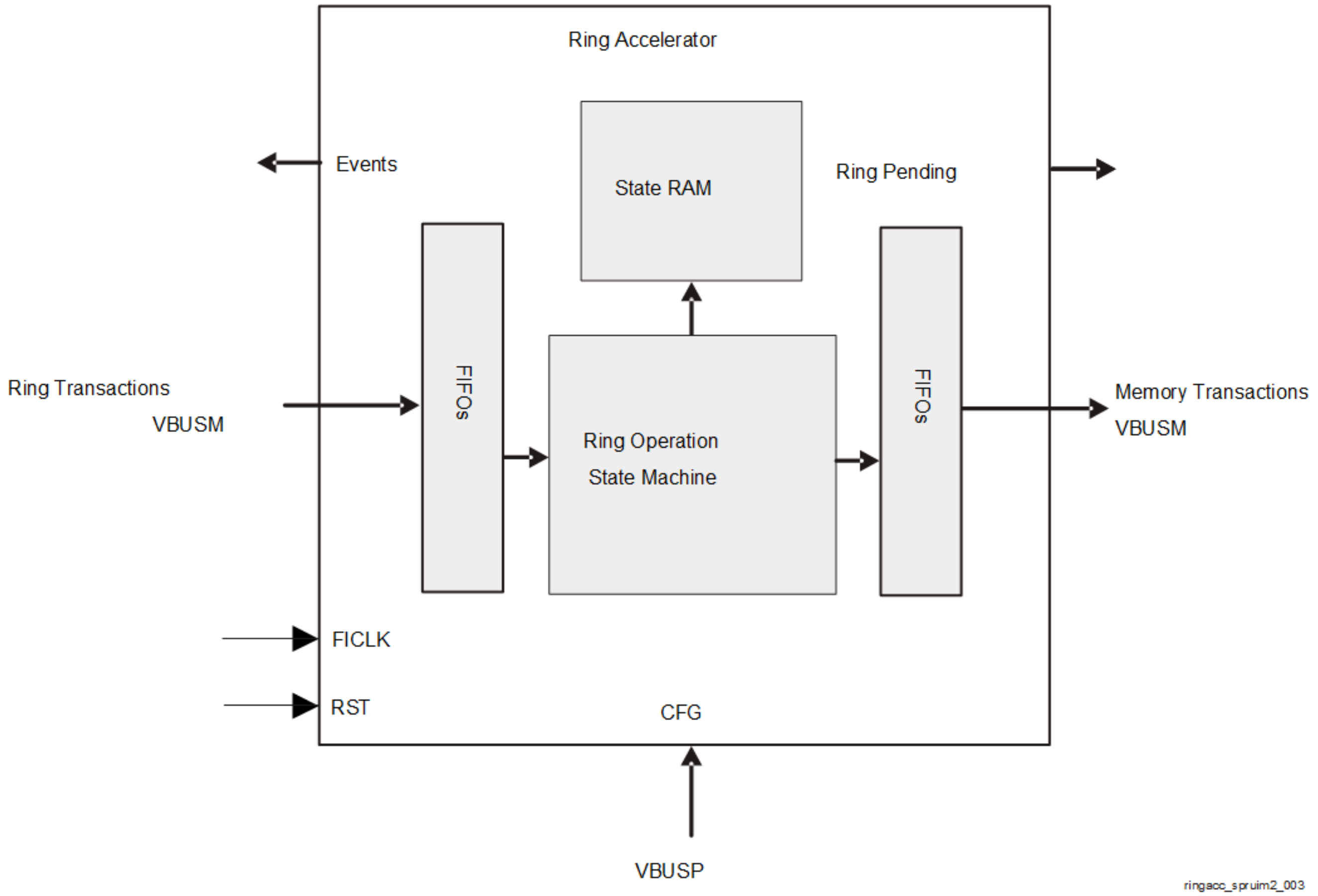


Figure 11-8. Ring Accelerator Block-Diagram

11.2.2.2.1.1 Configuration Registers

The Configuration Registers block is responsible for providing memory mapped registers for configuration of the RINGACC functions. The configuration registers are divided into:

- Static configuration fields , which are typically initialized and then left at specified values for long time periods (or until a reset occurs)
- Real-time (RT) registers , which are modified frequently during runtime. Configuration registers are listed and described in *RINGACC Registers*.

11.2.2.2.1.2 Source Command FIFO

The Source Command FIFO buffers VBUSM command phases which are accepted from the VBUSM source interface.

11.2.2.2.1.3 Source Write Data FIFO

The Source Write Data FIFO buffers VBUSM write data phases which are accepted from the VBUSM source interface.

11.2.2.2.1.4 Source Read Data FIFO

The Source Read Data FIFO buffers VBUSM read data phases which have been returned from the VBUSM destination interface (via the main state machine) and which are to be output on the VBUSM source interface.

11.2.2.2.1.5 Source Write Status FIFO

The Source Write Status FIFO buffers VBUSM write status data phases which have been returned from the VBUSM destination interface and which are to be output on the VBUSM source interface.

11.2.2.2.1.6 Main State Machine

The Main State Machine (MSM) block implements all of the control logic which is necessary to accept a command from the source interface, perform a lookup into the ring state RAM, determine the effective address for the destination interface transaction, modify the address (and byte count for reads) for the transaction, and place that modified transaction into the outgoing destination FIFOs. The MSM block is also responsible for updating the ring index and occupancy values and for producing output status to indicate changes to the ring state. The MSM also modifies the ring state whenever the read data or write status for a previous ring transaction return and forwards those responses back to the originating initiator.

11.2.2.2.1.7 Destination Command FIFO

The Destination Command FIFO stores VBUSM transaction commands which are output from the MSM as modified versions of transactions that were popped from the Source Command FIFO. The Destination command FIFO allocates a new command ID for each read or write command that is pushed to the FIFO. Read IDs are allocated from a scoreboard maintained in the Destination Read Data FIFO. Write IDs are allocated from a scoreboard maintained in the Destination Write Status FIFO. When a new command is allocated, the Destination Command FIFO also pushes the original cid and crouteid values from the source side transaction into a scoreboard in either the Destination Read Data or Destination Write Status FIFOs depending on the applicable transaction direction. The read interface of the Destination Command FIFO directly drives commands onto the destination VBUSM command interface.

11.2.2.2.1.8 Destination Write Data FIFO

The Destination Write Data FIFO stores write data phases for write commands that are passing through the RINGACC towards memory. The write interface of the Destination Write Data FIFO is directly connected to the read interface of the Source Write Data FIFO and the read interface directly drives write data onto the destination VBUSM write data interface.

11.2.2.2.1.9 Destination Read Data FIFO

The Destination Read Data FIFO provides a read command translation scoreboard and also stores read data phases that are passing through the RINGACC towards the originating DMA controller. The write interface of the Destination Read Data FIFO is directly connected to the destination VBUSM read data interface. As read data passes through the Destination Read Data FIFO, the *rid* and *rrouteid* are changed back to their original values using information which was stored in read command translation scoreboard.

11.2.2.2.1.10 Destination Write Status FIFO

The Destination Write Status FIFO provides a write command translation scoreboard and also stores write status phases that are passing through the RINGACC towards the originating DMA controller. The write interface of the Destination Writes Status FIFO is directly connected to the destination VBUSM write status interface. As write status words pass through the Destination Write Status FIFO, the *sid* and *srouteid* are changed back to their original values using information which was stored in the write command translation scoreboard.

11.2.2.2.2 RINGACC Functional Operation

11.2.2.2.2.1 Queue Modes

Each ring or queue can be in one of four modes that determines how it must be accessed and the compatibility it has with hardware and software.

11.2.2.2.2.1.1 Ring Mode

Ring mode is used when software owns one side of the ring, and hardware or another software owns the other side. This mode allows the software that owns a side of the ring to control that side including accessing the memory directly rather than going through hardware, and software updates the hardware on any changes through the Doorbell registers. These doorbell accesses indicate when software has pushed or popped entries, allowing the entity on the other side of the ring to know when there are elements ready. The ring mode has limitations that the exposed side of the ring is completely under software control, and any atomicity needed must also be performed by software, which is why the exposed side of a ring is usually owned by a single thread of software. This limitation also means that any hardware configuration that would normally access the same ring for both pushes and pops cannot use ring mode as hardware cannot access the exposed side of the ring, such as free queues that are normally read by hardware but could also be pushed by hardware on an error.

When software is popping from the ring, it must guarantee that it never pops more elements through the Doorbell register (RINGRT[a]_RT_DB) than what is valid in the Ring Occupancy (RINGRT[a]_RT_OCC) register, which holds how many elements are ready for software consumption. There could be some elements which have data written to memory but have not received status back from memory and those are not considered ready to pop yet as the ring status has not fully updated. Therefore, just reading from memory to determine the number of elements to pop is not sufficient. If software attempts to pop more than the RINGRT[a]_RT_OCC register value, then the occupancies could go negative resulting in missed down events and spurious interrupts. An optimization for software is to read the RINGRT[a]_RT_OCC register less frequently and keep a local copy which guarantees the maximum number of allowed pops. When the software copy of RINGRT[a]_RT_OCC reaches 0, or periodically, the software can read the register to refresh the value. This must reduce the frequency of register reads instead of reading the register for every software pop.

11.2.2.2.2.1.2 Messaging Mode

Messaging mode requires that all accesses to the queue must go through RINGACC so that all accesses to the memory are controlled and ordered. RINGACC then controls the entire state of the queue, and software has no directly control, such as through doorbells and cannot access the storage memory directly. This is particularly useful when more than one software or hardware entity can be the producer and/or consumer at the same time. Software must access the data through bus accesses to the RINGACC. As with the earlier example, if there are free queues that need the hardware to both push and pop, then they must be configured as at least messaging mode (or a later mode) and not ring mode.

11.2.2.2.2.1.3 Credentials Mode

Credentials mode adds per element credentials storage to messaging mode. This allows multiple producers with their own credentials to have those credentials stored with the element. This allows the consumer to inherit the credentials of each element rather than a single set for the entire queue, such as for DMA TR credential inheritance. This mode requires each operation to use two elements of storage since the credentials are stored in the second element, so the element count must be scaled appropriately. The credentials field is located in the same location as all modes, the word just before the first word of the message.

11.2.2.2.2.1.4 Peek Support

All modes except ring mode allow the peek operations so that software can view the next element without actually popping it from the queue. This is done by reading from a different offset from the normal pop operation. All the same fields are read but the element is not actually popped off of the queue. This is useful for algorithms that need to know about the overall queue and head element to make decisions but have not yet decided to pop from the queue.

11.2.2.2.2.1.5 Index Register Operation

In ring mode, the Index (RINGRT[a]_RT_INDX) register follows the software control of the ring through the doorbell registers, while the hardware index (RINGRT[a]_RT_HWINDX) register follows the hardware access of the ring through bus transactions. It works for a ring in either direction as the doorbell register (RINGRT[a]_RT_DB) update indicates whether elements were produced or consumed. But in the other queue modes, there is no simple manner to determine which index is for software or hardware since they both use bus transactions which the module cannot differentiate. So for these other queue modes, the index register is always the read index, and the hardware index register is the write index.

11.2.2.2.2.2 VBUSM Target Ring Operations

Each ring contains four memory spaces on the VBUSM target bus for access, each of which is 512 bytes long, with a total of 4 kB per ring. Each ring space starts immediately after the preceding ring. The allocation per ring is as in Table 11-66.

Table 11-66. Ring Memory Partition

Offset	Operation	Supported Ring Modes
0x0 - 0x1FF	Reads pop from head. Writes push to head.	Read supported in all modes, write supported in all modes except Ring mode
0x200 - 0x3FF	Writes push to tail. Reads pop from tail.	Write supported in all modes, read supported in all modes except Ring mode
0x400 - 0x5FF	Reads peek from head. Writes ignored.	All modes except for Ring mode.
0x600 - 0x7FF	Reads peek from tail. Writes ignored.	All modes except for Ring mode.
0x800 - 0xFFF	Reserved	Reserved

Within each 512-byte (0x200) space, the message data is right justified so that the last byte is always the 511-th byte. The element size of the ring defines which words are valid. The word just before the first valid message word is the credentials field. Access must not be made before the credentials register (CRED[a]_CRED).

11.2.2.2.2.3 VBUSM Initiator Interface Command ID Selection

The RINGACC keeps a transaction command scoreboard for reads and writes. Each scoreboard tracks which command indexes are currently outstanding from the RINGACC and which are free to use. When a read or write is requested by the Main State Machine, the scoreboard corresponding to the specified direction (read/write) is queried starting at index 0 and extending up to the maximum index for that scoreboard. The lowest index that is found and which is not currently allocated is selected and is directly used as the command ID (*cid*) for the outgoing transaction on the destination interface. 15 is the maximum index value for each scoreboard. Entries are freed for re-use in a write scoreboard when write status responses are received which account for all of the outstanding write data. Entries are freed for re-use in the read scoreboard only when all data has been returned for the read.

11.2.2.2.2.4 Ring Push Operation (VBUSM Write to Source Interface)

The following sequence will occur for each VBUSM write which is sent to the source interface:

1. RINGACC extracts ring number from incoming write transaction address
2. RINGACC looks up ring state using *ring number*
3. RINGACC calculates effective write address using *ring base* + *ring_index*
4. RINGACC re-evaluates pending bit for ring
5. RINGACC increments HW index and HW occupancy for ring
6. RINGACC allocates *cid* from scoreboard and places original *crouteid, cid, and ring number* into scoreboard
7. RINGACC pushes altered *caddress, cid* and unaltered remainder of command attributes to output FIFO (note *routeid* is not included)

At a later time when write status returns:

1. RINGACC recovers original *cid, crouteid,* and *ring number* from scoreboard
2. RINGACC increments SW index and occupancy for ring

3. RINGACC pushes restored *srouteid, sid*, and unaltered write status to output write status FIFO

11.2.2.2.2.5 Ring Pop Operation (VBUSM Read from Source Interface)

The following sequence will occur for each VBUSM read which is sent to the source interface:

1. RINGACC extracts ring number from incoming read transaction address
2. RINGACC looks up ring state using *ring number*
3. RINGACC calculates effective read address using *ring base* + *ring_index*
4. RINGACC increments HW index and decrements HW occupancy for ring
5. RINGACC re-evaluates pending bit for ring
6. RINGACC munges *cid* to add indicator in 4 MSBs to reconstitute *routeid* for returning read data
7. RINGACC pushes altered *caddress, cid* and unaltered remainder of command attributes to output FIFO (note routeid is not included)

At a later time when read data returns:

1. RINGACC recovers original *cid, crouteid*, and *ring number* from scoreboard
2. RINGACC increments SW index and decrements SW occupancy for ring
3. RINGACC pushes restored *rrouteid, rid,* and unaltered read data, status, and other control signals to output read FIFO

11.2.2.2.2.6 Host Doorbell Access

The following sequence will occur for each VBUSP write to the doorbell register (RINGRT[a]_RT_DB) for a ring:

1. RINGACC extracts ring number from config address
2. RINGACC looks up ring state using ring number
3. RINGACC adds doorbell ring value to both HW and SW occupancies for ring
4. RINGACC re-evaluates pending bit for ring

11.2.2.2.2.7 Queue Push Operation (VBUSM Write to Source Interface)

The following sequence will occur for each VBUSM write which is sent to the source interface:

1. RINGACC extracts ring number from incoming write transaction address
2. RINGACC looks up ring state using *ring number*
3. RINGACC calculates effective write address using *ring base* + *ring_index*
4. RINGACC re-evaluates pending bit for ring
5. RINGACC increments WR index and RD and WR occupancy for ring
6. RINGACC allocates *cid* from scoreboard and places original *crouteid, cid*, and *ring number* into scoreboard
7. RINGACC pushes altered *caddress, cid* and unaltered remainder of command attributes to output FIFO (note routeid is not included)

At a later time when write status returns:

1. RINGACC recovers original *cid, crouteid*, and ring number from scoreboard
2. RA pushes restored srouteid, sid, and unaltered write status to output write status FIFO

11.2.2.2.2.8 Queue Pop Operation (VBUSM Read from Source Interface)

The following sequence will occur for each VBUSM read which is sent to the source interface:

- RINGACC extracts ring # from incoming read transaction address
- RINGACC looks up ring state using *ring number*
- RINGACC calculates effective read address using *ring base* + *ring_index*
- RINGACC increments RD index and decrements RD and WR occupancy for ring
- RINGACC re-evaluates pending bit for ring
- RINGACC munges cid to add indicator in 4 MSBs to reconstitute routeid for returning read data
- RINGACC pushes altered *caddress, cid* and unaltered remainder of command attributes to output FIFO (note routeid is not included)

1. At a later time when read data returns:

- RINGACC recovers original *cid, crouteid*, and *ring number* from scoreboard
- RINGACC pushes restored *rrouteid, rid*, and unaltered read data, status, and other control signals to output read FIFO

11.2.2.2.2.9 Mismatched Element Size Handling

When less data is written than defined by the element size for the ring for RING or MESSAGE modes, only the written data is stored in the memory and any remaining bytes maintain their old values. The index and occ are still incremented normally, and any special fields that are unwritten are assumed to be 0 (such as the length for QM mode rings).

Writing less data for CREDENTIALS mode is illegal, as those types need the full data to append the additional words to the correct offsets in memory.

When more data is written than defined by the element size for the ring, it will be an error and the write will be ignored and no index or occ increments occur. The only exception is for writes to an 8 byte element size ring, where the additional fields up to another 8 bytes are allowed but not written (for old Queue Manager compatibility).

When less data is read than defined by the element size for the ring, only the read data is fetched from memory, and any remaining bytes are lost. The index and occ are still incremented normally.

When more data is read than defined by the element size for the ring, it will be an error and the read will not affect the ring, the read data will be 0s, and no index or occ decrements occur. Access beyond the credentials word should not be attempted and can result in unpredictable behavior.

All accesses must be for multiples of 32 bit words, and partial bytes are not supported for all ring modes.

11.2.2.2.3 Events

The module outputs events about queue levels that can be used by an external module for statistics or interrupts.

Each queue has:

- an up event when the queue goes from 0 elements to 1 or more elements
- and a down event when the queue goes from 1 or more elements to 0 elements. The event number is programmable per queue in the RING[a]_EVT register. This event occurs when the state machine updates the final occupancy for the queue. In ring mode this is when the response from the memory access returns, while in other queue modes this is when the operation is processed.

An event number programmed to 0xFFFF indicates to not produce an event for that ring when an event is not necessary. The register event number fields reset to 0xFFFF, so they must be programmed to a valid value before events will be generated. This applies to the monitor event number fields as well.

11.2.2.2.4 Bus Error Handling

If a bus error is detected on a response to a ring memory transaction, an error event is triggered to alert software. Since the ring contents may be corrupted as the push or pop was not completed correctly, software should consider resetting the ring and any software or hardware elements using the ring. A log register (RINGACC_ERROR_LOG) captures the ring that had the error and whether it was from a push or pop, and an error up event is sent to the programmed event number. After an error is logged, another will not be captured until the first is read out. When read, if an error is pending an error down event is sent to clear any interrupt, and then the next bus error log can be captured. A read of the RINGACC_ERROR_LOG register when there is no error log pending will not produce any down events. The event that is triggered is also programmable. Only legal push and pop operations will capture this error, and not for any peek, emudbg read, flush command, or any operations that is illegal and causes the resulting memory access to be flushed.

11.2.2.2.5 Monitors

Monitors can be configured that allow various functions to be tracked of programmed queues. Each monitor is programmed to monitor a particular queue, the function to provide, and the data source to operate on. The supported functions are: to check the queue against programmed thresholds, to keep track of watermarks of the queue, to keep track of starvation occurrences (a read of an empty queue), or statistics capture. The supported data sources are: the queue element count, the head element size value, or the accumulated size value. Each monitor can also be programmed to produce an event should it have a triggering condition.

11.2.2.2.5.1 Threshold Monitor

A threshold monitor uses a programmed low threshold value and a programmed high threshold value to track the data source in the queue and cause an interrupt or status when a threshold is broken, either below the low value or above the high value. This is useful for software to replenish empty buffers when a queue has too few, or for a queue to accumulate enough elements so that software must start processing them, or for debug. The threshold being broken will cause the up or down event.

11.2.2.2.5.2 Watermark Monitor

A watermark monitor tracks the low and high values of the data source since the last read of the monitor. After initial setup or clearing, the watermark values will load the current value of the data source as the low and high. Then for successive operations if the resulting data source of the queue is below the low watermark, or above the high watermark, the associated watermark will be updated. When the monitor value registers are read, the value is cleared and starts tracking again using the current data source value. This can be useful for tracking low and high values of queue element counts or sizes for data tracking, debug or future optimizations, such as allocating items to a queue or buffer sizes based on counts.

11.2.2.2.5.3 Starvation Monitor

A starvation monitor tracks the number of starvation events (a read to an empty queue) that occurred on the queue. The data source is ignored, and the starvation count is always incremented whenever there is a read to the queue and the queue is empty. The count is cleared when the monitor value is read. This can be useful to trigger if any starvation event occurs, or to track how many of these events occur in a timeframe, and can be used for future optimizations or debug.

11.2.2.2.5.4 Statistics Monitor

The statistics monitor can track some simple statistics on the queue operations. The data source is ignored. The first value is the count of the number of writes to the queue, and the second value is the count of the number of reads from the queue. The counts are cleared when the monitor values are read. This can be useful to track the activity on a queue, and can be used for future optimizations or debug.

11.2.2.2.5.5 Overflow

RINGACC provides an overflow function where a push to a full ring will result in a push to a special overflow ring, rather than just losing the pushed data. The overflow ring is defined through RINGACC_OVERFLOW register, and that ring must be defined with a large enough element size to cover the element size of any other ring, as well as enough elements to hold enough overflow data (as an overflow to the overflow ring will be lost). When there is a push to a full ring, there will be two elements written to the overflow ring, first the push data, and then the ring number that was full. A supervisor entity can own the overflow ring and perform what actions are needed from the overflow data. The size of the overflow ring must be an even number since two elements will be pushed for each overflow event. The overflow ring must be configured in ring or message modes.

An overflow queue value of 0xFFFF will disable the overflow function and will not record queue overflows. (SR2.0)

11.2.2.2.5.6 Ring Update Port

To enhance performance for DMAs, the RINGACC provides a bus that indicates when ring updates occur, allowing the DMA to track their own rings and detect updates before the responses arrive. The bus will go valid whenever there is an update to the state of a ring, which can be from a push, pop, or doorbell write. It will not go valid for a peek, an emudbg pop, or a push to a full ring, as those do not update the ring state. When the bus is valid, the other signals are valid and indicate whether the operation was a push or a pop, whether the resulting state of the ring is empty, the ring number, and the number of elements updated to the ring (the push determines whether it is subtracted or added to the current count). One special case is a pop from an empty ring, which indicates an update but the element count is 0 since no items were actually popped, but a DMA using the cnt to add or subtract must handle this correctly by default. The bus will go valid once the operation command has been completed, and not after the response has been received, even for ring mode rings, allowing the DMA to see the update as soon as it is known by the RINGACC even before it is known to software.

11.2.2.2.5.7 Tracing

This module provides a trace output of all operations so that the traffic can be viewed at a later time. The trace uses a simple write-only 32-bit VBUSP bus, with a defined packet header. The msgtype field defines the type of operation, and the message data is simply the data involved in the operation. It is likely the trace output will be read slower than new operations could provide data, so there will be a trace buffer able to hold two complete messages plus trace headers. If a new operation starts while the trace buffer does not have enough space, then that trace message will not be sent. And RINGACC_TRACE_CTL register controls whether to enable the trace output, whether to trace a single queue or all queues, and whether to include the message data in the trace output.

Table 11-67 shows the trace message for a push.

Table 11-67. Trace Message for a Push

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware
1	15:9	0x1	Msgtype for push
1	8:0	0x009	Standard Trace Header
2	31	push_to_head	Push to head flag, 0 = to tail, 1 = to head
2	30:16	0x0	Unused
2	15:0	queue	Queue for push
3-N	31:0	message data	Optional message data for push, length dependent on message size

Table 11-68 shows the trace message for a pop.

Table 11-68. Trace Message for a Pop

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware
1	15:9	0x2	Msgtype for pop
1	8:0	0x009	Standard Trace Header
2	31	empty	empty pop, 0 = valid message, 1 = empty
2	30:16	0x0	unused
2	15:0	queue	queue for pop
3-N	31:0	message data	Optional message Data for pop, length dependent on message size

Table 11-69 shows the trace message for a peek

Table 11-69. Trace Message for a Peek

Word	Bits	Data	Comment
1	31:16	0x0	Time to be replaced by trace hardware
1	15:9	0x3	Msgtype for peek
1	8:0	0x009	Standard Trace Header
2	31	empty	empty peek, 0 = valid message, 1 = empty
2	30:16	0x0	unused
2	15:0	queue	queue for peek
3-N	31:0	message data	Optional message Data for peek, length dependent on message size

11.2.3 Secure Proxy (SEC_PROXY)

This chapter describes the Secure Proxy (SEC_PROXY) module in the DMSS.

11.2.3.1 Secure Proxy Overview

The Secure Proxy module provides proxy buffers for hosts that need to create large data bursts but can only perform small accesses.

11.2.3.1.1 Secure Proxy Features

Secure Proxy supports the following features:

- Provides proxy function to store large data bursts that a host can only access in smaller amounts
- Supports a configurable number of threads, where each has their own independent proxy function
- Keeps the large data burst coherent until the complete data has been accessed
- Allows for interleaved access between multiple hosts or tasks using multiple proxy threads
- Supports a configurable target resource. The target has a configurable number of channels, size of each channel and base address
- Supports a programmable fixed queue for each proxy thread
- Supports multiple producers all writing to the same queue
- Supports a max message count for outbound proxy threads limiting the number of messages a thread can produce
- Supports programmable thresholds for when to generate events
- Optionally supports dynamic clock gating

Table 11-70. Secure Proxy Allocation Within Device Domain

Module Instance	**Domain**
	MAIN
DMSS0_SEC_PROXY0	✓(DMSS)

11.2.3.1.2 Secure Proxy Parameters

Secure Proxy Configuration Parameters shows the Secure Proxy configuration parameters set during SoC design.

Table 11-71. Secure Proxy Configuration Parameters

Module Instance	**Parameters**				
	Proxies(1)	**Message Size**(2)	**Target**	**Channels**(3)	**Sizes**(4)
DMSS0_SEC_PROXY0	76	64	DMSS0_RINGACC	20	4096

(1) Number of proxy threads supported. Can be read off from the SEC_PROXY_CONFIG read-only register
(2) Number of bytes for message. Can be read off from the SEC_PROXY_CONFIG read-only register
(3) Number of channels for the target
(4) Number of bytes per channel supported for the target

Note

Some features may not be available. See *Module Integration* for more information.

11.2.3.2 Secure Proxy Functional Description

This module provides proxy functions for hosts that need to create large data bursts but can only perform small accesses. Examples of this need are:

- large messages (for power control, security control, or IPC)
- data descriptors that are more than a pointer
- DMA Transfer Requests (TR)

All of these require larger data sets, from 12 to 128 bytes, and the storage hardware requires the entire data on the bus in a single burst. Unfortunately, many CPUs cannot produce bursts to device memory, such as registers, and the largest CPU access is typically 8 bytes. So the proxy provides the ability to access the hardware with a single burst, and at the same time allows the CPU to access the same data in smaller accesses. The proxy itself does not contain the resources, but will front other hardware that do contain the resources. The proxy will access this other hardware with the entire data in a single burst, once the host has completed the data.

Secure Proxy Block Diagram describes Secure Proxy major building block

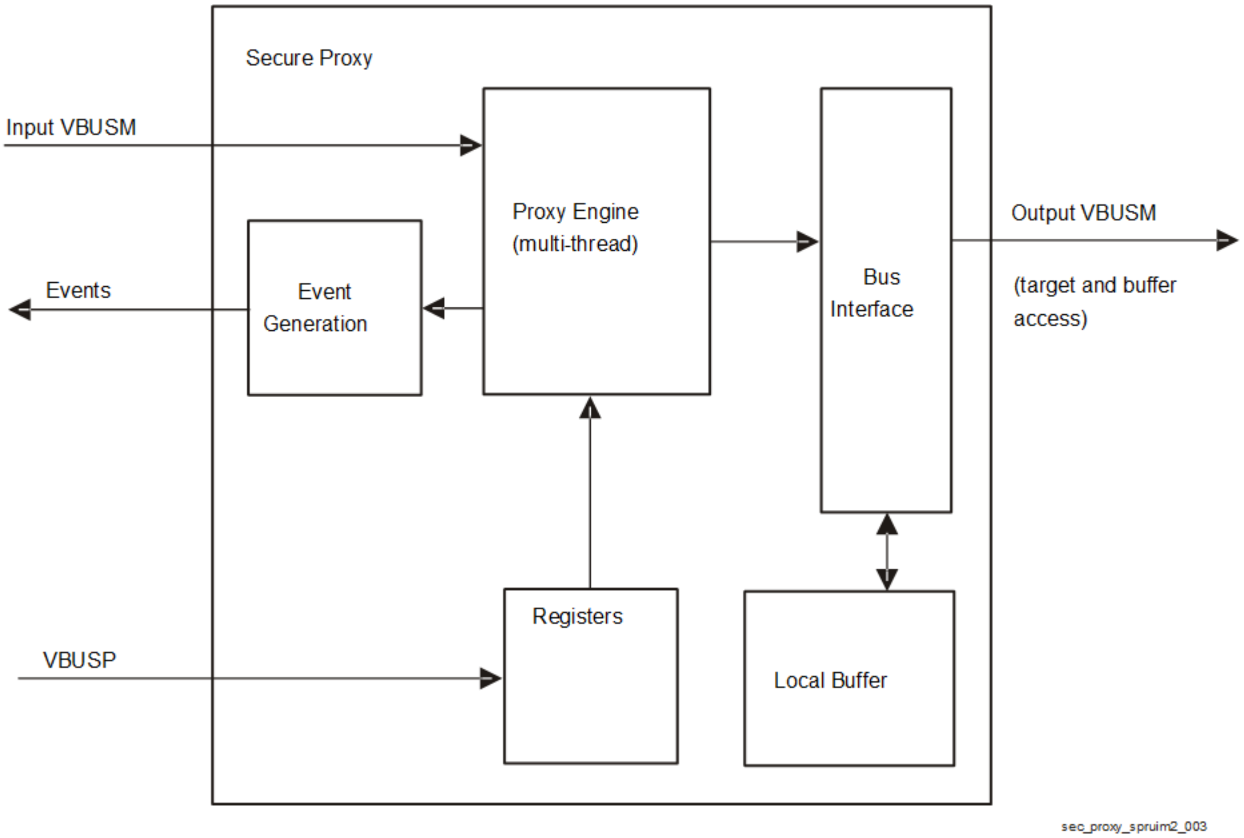


Figure 11-9. Secure Proxy Block Diagram

11.2.3.2.1 Targets

11.2.3.2.1.1 Ring Accelerator

The RINGACC provides four distinct offsets to use per ring/queue shown in RINGACC Offset per Ring/Queue, totaling 4 KB space per ring/queue.

Secure Proxy always writes to tail, which is the offsets from 0x200 to 0x3FF. Secure Proxy always reads from the head, which is the offsets from 0x000 to 0x1FF. The latter two offsets in RINGACC are not used by this proxy. And if the proxy message size is less than 512 bytes, then it always accesses the upper bytes of those regions, so that the message always ends on the last byte of each region, byte 511.

Table 11-72. RINGACC Offsets per Ring/Queue

Offset	Operation
0x0 - 0x1FF	Reads pop from head. Writes push to head.
0x200 - 0x3FF	Writes push to tail. Reads pop from tail.
0x400 - 0x5FF	Reads peek from head. Writes ignored.
0x600 - 0x7FF	Reads peek from tail. Writes ignored.
0x800 - 0xFFF	Reserved.

This means that target writes will use the following calculation:

target base address + (queue × 4KB) + 0x400 - msg_size (17), and burst until offset 0x3FF.

And target reads will use the following calculation:

target base address + (queue × 4KB) + 0x200 - msg_size (18), and burst until offset 0x1FF.

11.2.3.2.2 Buffers

The proxy does not store all the buffers internally. It is programmed with a buffer base address (SEC_PROXY_BUFFER_L, SEC_PROXY_BUFFER_H), and all accesses to the buffer are made through the output VBUSM port using that base. The external buffer must be enough to store one msg_size per proxy thread. The proxy only includes a small temporary buffer to save one entire message when accessing the target. Otherwise all host accesses are made to the external buffer. This buffer storage must be considered private for the proxy hardware, so any other access can cause unpredictable results.

11.2.3.2.2.1 Proxy Credits

To support outbound proxy limits, the proxy will use internal credits for tracking resource usage. SEC_PROXY_THREAD[a]_CTL register sets the max credits each outbound proxy thread contains. When a proxy thread sends a message, the current credit count (SEC_PROXY_THREAD[a]_STATUS) decrements by 1. If the current credit count is 0, then the proxy thread is not allowed to send any more messages, and they just remain inside the proxy (so that the host can come back later when a credit has become available and quickly send the same message). When a message that was send by this proxy thread is read by an inbound proxy thread then the credit is returned to this proxy thread and the current credit count increments by 1.

For inbound proxy threads, the credits are used to track pending messages. When an outbound proxy thread sends a message that is read by this proxy thread, then the current credit count of this proxy thread is incremented by 1. A current credit count that is non zero indicates a message is pending and can be read. When the proxy thread completes the read of a message the current credit count is decremented by 1. If the current credit count is zero, then the proxy thread will read an empty message where all the data is 0s. The credit count saturates at 255, so if there can be more messages in the system for that proxy thread than 255 then multiple proxy threads should be used, or the count can become mismatched after a saturate.

11.2.3.2.2.2 Proxy Private Word

To support tracking of credits from each proxy thread, the proxy will extract the first word from the total message size for private tracking usage. This will include saving the proxy thread ID used within the proxy. This is necessary so that when a proxy reads a new message from the target it can inspect this word and return the credit to the source proxy thread. This allows the outbound proxy threads to have a set number of message credits, which decrement when a new message is written, and increment when a message from that proxy thread is read, thus keeping the credits in the system coherent. Any data written to this first word of the message will be ignored, so software should not write to the first word of messages through the proxy. Consumer software can use the first word to identify the source proxy thread of the message (SEC_PROXY_DATA_j).

11.2.3.2.2.3 Completion Byte

The proxy completes a message when the completion byte is accessed. This completion byte is the final byte in the full size of the message. This byte can be written by any size access, whether byte, 32-bit, or 64-bit word. The write of a message is not complete until this final byte of the message is written, and only then will the message be sent to the target. The read of a message is not complete until this final byte of the message is read by the host, and only then will reading a new message be allowed. Even if the final byte of the message is not needed, it must be accessed to complete the message inside the proxy hardware.

11.2.3.2.3 Proxy Thread Sizes

There are a configurable number of proxy threads in the module. Each thread has its own address space to the module and determining which proxy thread is being accessed is simply based on the address bits above the final size of each proxy thread space. Since each proxy thread will be programmed to a single resource, the only space requirement is that for using 4 KB to match typically used MMU page sizes. Only the first N bytes, matching the target channel size, is usable.

11.2.3.2.4 Proxy Thread Interleaving

Each proxy thread must have a single owner, as each proxy thread only has a single buffer to work on the current data. If there are multiple owners in the system, they must each use their own proxy thread. Then they will have their own buffer and each can access a different resource at the same time. Each proxy thread is completely independent and kept coherent regardless of accesses to other proxy threads or regardless of the order of accesses. So the proxy support interleaving of multiple hosts' accesses.

11.2.3.2.5 Proxy States

Each proxy thread uses a simple state machine to track the currently usage by that host. This state machine is used to track when a proxy thread is in use or not, but also for error detection. The proxy thread always starts in idle state, when there is no currently activity. There is a write state for when the proxy thread has been written and contains data that has yet to be written to a resource. There is a read state for when the proxy thread has read data from a resource and that entire data has not been fully read by the host. When a proxy thread access completes, final write or final read, then the state will go back to idle. The following sections show the utilization of these states.

11.2.3.2.6 Proxy Host Access

A proxy thread begins in an idle state, where there is no data in the buffer. In this state the proxy thread will accept an access to the resource.

11.2.3.2.6.1 Proxy Host Writes

The first write to an idle proxy thread puts the proxy thread into write mode for the selected channel. Further legal writes are stored in the buffer for the enabled bytes and offset within the buffer. A write to a previously written location will overwrite the previous data. The buffer is not cleared initially, so if a byte is not written, the message will include previous buffer data. When there is a legal write to the last byte of the resource, then the entire data is written by the proxy to the target and channel as a single write burst. The proxy will wait for the write status from the target write before it sends the write status for this final byte host write. This allows the host to use the write status to guarantee the entire write data from the proxy has landed at the target. The proxy thread is then put back into idle state. A write completion when there are no credits available results in the message not being written to the resource and the proxy thread remains in write mode (so that the message can be quickly completed when a credit becomes available).

11.2.3.2.6.2 Proxy Host Reads

When in idle state, the first read to the proxy thread will put the proxy into read state, and the proxy will read the target and channel requested in a single burst of the target's channel size. When the data is returned it is stored in the buffer and the accessed part is returned to the host. Further legal reads are allowed and return the accessed data in the buffer. When there is a legal read to the last byte of the resource, the accessed data is returned, and the proxy thread is put back into idle state. If an initial read is made and there are no pending messages, the proxy thread will return an empty message, where the data is all 0s.

11.2.3.2.6.3 Buffer Accesses

Each read or write will actually trigger a read or write to the external buffer space allocated for that proxy thread, where the real message data is stored. In addition, when a write message completes, the external buffer will be read for the entire message for that proxy thread so that it can then be written to the target. Similarly, after a read causes a read from the target to get a new message, the entire message is written to the external buffer to store the message to the buffer.

11.2.3.2.6.4 Target Access

After the write has completed and the external buffer read for the entire message, the entire message is then written to the target as a single burst. Similarly, for a read that needs a new message, the target is read for a full message as a single burst.

11.2.3.2.6.5 Error State

If an error is detected in a proxy thread, the proxy will put that proxy thread into error state, and the current buffer will be lost. A status bit will be set that indicates the proxy thread is in error. All accesses to that proxy thread will be ignored until the status bit is cleared. Once cleared the proxy thread is put back into idle state. Errors are an access to an offset beyond the length of the message, or a mismatch in the direction of access against what was programmed such as reading an outbound thread or writing an inbound thread.

11.2.3.2.7 Permission Inheritance

The proxy will automatically inherit the permissions from the access and pass these to the target upon the target burst access. The exact transactions that are inherited from are the final byte write or the first read, and these exact permissions are used on the output bus transaction that accesses the target.

11.2.3.2.8 Resource Association

Each proxy thread has a register (SEC_PROXY_THREAD[a]_CTL) to define the resource within the target that the proxy thread is mapped to. The host has no ability to access any other resource in the target. This allows the setup of the proxy to determine the resources that all the hosts use.

11.2.3.2.9 Direction

Each proxy thread has a register (SEC_PROXY_THREAD[a]_CTL) to define the direction for access. It can either be an outbound proxy thread for writing messages to resources. Or it can be an inbound proxy thread for reading messages from resources. The host must match the direction programmed or it will result in a proxy thread error.

11.2.3.2.10 Threshold Events

Each proxy thread can produce events based on the state of the resource it uses. For outbound proxy threads, a threshold can be set so that an event is produced when there are now at least N messages available to write. For inbound proxy threads, a threshold can be set so that an event is produced when there are now at least N messages available to read. These threshold values are programmed in SEC_PROXY_EVT_MAP_j, allowing the host to determine how often it gets events. Programming the count values while the threshold is set to 0 will not trigger events, but if the threshold is not 0 then programming the counts will trigger events based on whether the threshold is reached or not. No event is generated if the event is programmed to 0xFFFF.

11.2.3.2.11 Error Events

Each proxy thread can produce an event when it has detected an error. This error occurs when the host violates the programmed setup of the proxy thread or accesses beyond the message size. There is a separate status bit per proxy thread for these errors. No event is generated if the event is programmed to 0xFFFF.

11.2.3.2.12 Bus Error and Credits

If a target read for a message returns a bus error, this indicates the read was bad and the data is corrupt and usually 0s. Because the private word in contained in the message, if the private word is corrupted then the source proxy thread is not valid and the credit return will not be correct. Since the data is usually 0, this means the credit would be returned to proxy thread 0 incorrectly most of the time. And the credit will be lost for the actual source proxy thread of the message that was not read correctly. The hardware has no way to correct for this, as the message from the target is corrupt so it does not know the correct owner of the credit. If software detects that a read message is corrupt, it can attempt to correct the situation by resetting the affected proxy threads using that queue, to restore their credit counts back to the default. Software may also want to reset proxy thread 0 since it may be getting extra credits.

11.2.3.2.13 Debug

When the transaction has the emudbg set for a read, all side effects will not occur. This means that the read will not cause a target read since that would affect the target, and instead current buffer will be read even if the previous message has completed.

11.2.4 Interrupt Aggregator (INTAGGR)

This chapter describes the INTAGGR module, part of DMSS

11.2.4.1 INTAGGR Overview

The Interrupt Aggregator (INTAGGR or INTA) provides a centralized machine which handles the termination of system events to that they can be coherently processed by the host(s) in the system. The main function of the module is to convert between 'global events' (assertion and de-assertion events transmitted on the event-transport-lane (ETL) bus) and 'local events' (level sensitive signals on output, and level or edge sensitive signals on input).

Table 11-73. INTAGGR Allocation Within Device Domain

Module Instance	Parameters
	MAIN
DMSS0_INTAGGR0	✓(DMSS)

11.2.4.1.1 INTAGGR Features

The DMSS0_INTAGGR0 supports the following features:

- 64-bit VBUSP target using 64-bit registers
- Provides a set of TI Interrupt Architecture compliant interrupt status and mask register sets which are used to pass specific event status to one or more Host blocks.
  - Maps a collection of DMA Messaged Events which are input through an Event Transport Lane into specific bit locations in one or more interrupt cause registers
  - Mapping is performed based on a programmable table which provides a single location for each ordinal input event number (0 through sevt_cnt-1)
    - Table specifies a specific bit in a specific cause register that the event should set or clear depending on the type of event (up vs down)
    - Tracks a single 'event up' / 'event down' condition. There is no event counting. (The 'cnt' field of the ETL is ignored.)
  - Tracked status interrupts are presented to the user through a standard interrupt register interface.
    - Provides separate 'enable set' and 'enable clear' registers.
    - Provides both masked and unmasked interrupt status.
    - Interrupt status bits can be manually cleared using 'write 1 to clear'.
- Provides an optional set of Unmapped Event (UNMAP) which can take an 'unmapped' event from the ingress ETL and generate a Global event on the egress Event Transport Lane (ETL) interface.
  - Each ingress event can generate an egress Global event on the egress ETL, controllable through a mapping register.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.
- Provides an optional set of Global Event Input (GEVI) counters which can count events which were delivered via an ingress Event Transport Lane (ETL).
  - Each counted event provides an MMR by which the count can be read and an MMR by which a specified amount can be decremented by the host.
  - Each counted event generates an egress Global event on a zero to non-zero and non-zero to zero transition, controllable through a mapping register.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.
- Provides an optional set of Global Event Input (GEVI) 'Multicast' registers which can take a Global event from an ingress ETL and generate two egress Global events on the egress ETL interface.
  - Each mapping register has the option of alternatively directly setting an interrupt status bit.
- Provides an optional set of Local Event Input (LEVI) to Global event registers which can be used to convert pulsed discrete interrupt inputs or clock synchronous rising edge events into Global events on an egress ETL.

  - Each ingress event index provides a configurable 'pulse' or 'rising edge' bit, plus the configurable index of the generated Global event.
- Supports dynamic clock gating via

Note

Some features may not be available. See *Module Integration* for more information.

11.2.4.1.2 INTAGGR Parameters

Interrupt Aggregators Parameters shows the Interrupt Aggregator 0, parameters set during design time.

Table 11-74. Interrupt Aggregators Parameters

Module Instance	Parameters				
	VINTR[1]	SEVI[2]	GEVI[3]	LEVI[4]	MEVI[5]
DMSS0_INTAGGR0	184	1536	256	32	128

(1) VINTR – Number of Virtual Interrupt outputs. These are connected to the interrupt router inputs. Value can be read from INTAGGR_INTCAP register.

(2) SEVI – Number of Main (Steerable) Events. Value can be read from INTAGGR_INTCAP register.

(3) GEVI – Number of Countable Events. Value can be read from INTAGGR_AUXCAP register.

(4) LEVI – Number of Local Event inputs. Value can be read from INTAGGR_AUXCAP register.

(5) MEVI – Number of Multicast Events. Value can be read from INTAGGR_AUXCAP register.

11.2.4.2 INTAGGR Functional Description

The Interrupt Aggregator (INTAGGR) provides a centralized machine which handles the termination of system events to that they can be coherently processed by the Host(s) in the system. Both the signaling and content of TI system events are incompatible with standard interrupt controllers. The INTAGGR provides mechanisms which convert the TI proprietary system events to standard level sensitive pending bits which can be used by all downstream interrupt infrastructure. Events can be presented to the INTAGGR in two different forms:

- Events may be active high pulses, or clock synchronous rising edges, which are input on separate orthogonal pins. These are called 'Local Events'.
  - Local event signals that are used in pulse counting mode must be sourced by the same clock as the interrupt aggregator.
  - Local event signals that are used in edge counting mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the interrupt aggregator clock, and they must remain high for at least 1 'slow' clock cycle.
- Events may be messages which are input in time division multiplexed sequential order from an Event Transport Lane. These are called 'Global Events'.

In both cases, these events need to be conditioned to transition them from a transient indicator that something occurred to a persistent and reliable indication of the current state of the system. The IA is architected to perform this conversion in an efficient and cost effective manner.

11.2.4.2.1 Submodule Descriptions

11.2.4.2.1.1 Status/Mask Registers

The Status and Mask Registers block is responsible for providing persistent storage for the interrupt status and mask bits and for formatting those in a way that is compliant to the TI Interrupt Architecture requirements. These requirements include the ability to set and clear bits orthogonally and to provide a masked version of the status register that corresponds to the supplied bit mask for each register.

11.2.4.2.1.2 Interrupt Mapping Block

The Interrupt Mapping Block accepts ordinally numbered events (0-N) and converts those ordinal event numbers into a status register number and bit number pair that is then used to manipulate the specified bit in the Status Registers block.

11.2.4.2.1.3 Global Event Input (GEVI) Counters

The GEVI Counters block is responsible for accepting an Event Transport Lane events and summing the total message counts for each received event index. The module creates global egress events for zero to non-zero count up' events and non-zero to zero 'count down' events. The egress global event index is configured via GEVI[a]_MCMAP register, so count status egress events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

11.2.4.2.1.4 Local Event Input (LEVI) to Global Event Conversion

The Local to Global event block is responsible for accepting an array of input pins and independently counting the number of cycles for which those pins are asserted high, or by counting individual clock synchronous rising edge events. The counting mode is configurable on a 'per pin' basis. The events are converted to egress Global events on an egress ETL. Global events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

11.2.4.2.1.5 Global Event Multicast

The Global event multicast block takes an ingress global event from an ingress ETL, and maps it into two egress Global events on two egress ETL interfaces. Global events can optionally be fed back into the INT_AGGR, via the ETL switch fabric.

11.2.4.2.2 General Functionality

11.2.4.2.2.1 Event to Interrupt Bit Steering

Each time an event message is received on the Main Event Transport Lane interface, the interrupt mapping block performs a direct lookup into an SRAM using the event number as the address. The SRAM stores a corresponding interrupt status (INTR_STATUSM) register and bit number within that register (VINT[a]_STATUS_MSKD) which are to be manipulated anytime a message is received indicating something occurred on that specific event. When an up event is received, the specified bit in the [a] Status register will be set. When a down event is received, that same bit will be cleared. This block is what allows flexible aggregation of various system events into an array of bits in the interrupt status registers. It is intended that this mapping is essentially static - set up when a resource is allocated and left untouched until the resource is no longer needed. Note that the 'cnt' field of the ETL is ignored and no interrupt counting is performed here. When 'UpDn=1', the interrupt flag bit is set, and when 'UpDn=0', the flag bit is cleared.

11.2.4.2.2.2 Interrupt Status

The event messages which are generated from the event to interrupt bit steering logic are input to the Interrupt Status registers. Each time an event is received, the interrupt status registers machine will assert or de-assert the specified bit in the specified register. The assertion and de-assertion in the interrupt status register is unaffected by the interrupt enable state. When an up event is received, the corresponding bit is set and when a down event is received, the corresponding bit is cleared. Some sources of input events will not include the ability to send a down event. In these cases, the interrupt router provides the ability to clear the status bits through the Interrupt Source Clear register (VINT[a]_STATUS). The host will write a one to the specific bit in the register which is to be cleared and the interrupt status machine will clear the bit internally. It is not intended that the Host directly clear bits which are automatically cleared via down events from the source itself.

11.2.4.2.2.3 Interrupt Masked Status

Interrupt enable bits are used in conjunction with the interrupt status bits to create the interrupt masked status register values. The interrupt masked status register (VINT[a]_STATUS_MSKD) contains the value of the interrupt status ANDed with the value of the interrupt enable register (VINT[a]_ENABLE_SET). Each time a new event message is received from the event to interrupt bit steering logic or the interrupt enable register is modified, the interrupt masked status register is re-evaluated.

11.2.4.2.2.4 Enabling/Disabling Individual Interrupt Source Bits

Separate (VINT[a]_ENABLE_SET and VINT[a]_ENABLE_CLR) registers are provided to allow individual enable bits to be enabled or disabled without the need for a read-modify-write operation. When the VINT[a]_ENABLE_SET register is written, all bits within written bytes which are 1 will cause corresponding bits in the internal enable register to be set. When the VINT[a]_ENABLE_CLEAR register is written, all bits within written bytes which are 1 will cause corresponding bits in the internal enable register to be cleared.

11.2.4.2.2.5 Global Event Counting

When enabled, the INTAGGR will provide a set of counters which will track how many outstanding messages have been observed for each ingress event index from the ingress Counted Global Event Transport Lane (ETL) interface. For each message received where the 'UpDn' flag is set, the corresponding counter will be incremented by value of the 'cnt' field of ingress message. Events where the 'UpDn' flag is cleared are ignored. The counter is made visible to software in the GEVI[a]_COUNT register. When software has read the count, it can acknowledge that count has been seen and processed by writing back an integer value specifying the amount by which the counter should be decremented, and the counter will subtract that value from the current count (which may have updated since it was read). The count will saturate at a value of 0xFFFFFFFF. Writing a count 'ack' value higher than the one read is not supported and will produce non-deterministic results.

When a count transitions from zero to a non-zero value, a Global Up 'UpDn=1' event is sent out an egress ETL interface. When a count transitions from a non-zero value to zero, a down 'UpDn=0' event will be sent. The index of the Global event is mappable on a 'per-counter' basis, using the GEVI[a]_MAP register. The event may be mapped such that it then re-enters INTAGGR's 'Event to Interrupt Bit Steering Block' to generate an interrupt to the host. The event routing is handled by an external event switch fabric. Note that writing a new egress event index via the GEVI[a]_MAP register does not alter the stored event count for the ingress event register index.

11.2.4.2.2.6 Local Event to Global Event Conversion

When enabled, the INTAGGR will provide a set of Local to Global event conversion registers. Local events may be discrete clock synchronous pulses or clock synchronous rising edges. The counting mode is configurable on a 'per pin' basis. In pulsed mode, the module will track how many outstanding clock cycle long pulses have been observed on each of the provided levi interface pins. For each cycle in which a LEVI input pending bit is asserted the corresponding counter will be incremented by 1. In 'rising edge' mode, the number of rising edge transitions on the pin is counted.

The module will generate egress Global events on its egress ETL, with a different global index configured for each ingress LEVI pin. The LEVI pins numbers (1-N) are converted to arbitrary global event indices via the global event mapping LEVI[a]_MAP registers. The egress Global events can themselves be mapped to re-enter the INTAGGR's Global Event Counting block, so that the counts can then be made visible to software in the GEVI count registers as described in Section 10.2.7.3.1.3. The event routing is handled by an external event switch fabric.

11.2.4.2.2.7 Global Event Multicast

In DMSS0_INTAGGR0, the INTAGGR will provide a set of Global event multicast (GEVI[a]_MCMAP) registers. These registers allow an ingress Global event on its ingress ETL interface to be mapped into two egress Global events on two separate egress ETL interfaces. A set of registers map the ingress Global event index (1-N) into two arbitrary egress event indices.

11.2.5 Packet Streaming Interface Link (PSI-L)

This section describes the Packet Streaming Interface Link (PSI-L) for the device.

11.2.5.1 PSI-L Overview

PSI-L is a packet based protocol used to transfer data between several device modules. Each transaction is routed based on thread ID value instead of physical address. All PSI-L interfaces are point to point direct connections to DMSS0. All switching functions among the PSI-L based interfaces are done inside DMSS0.

The PSI-L also has an event interface referred to as ETL, which is purely used to transfer event information.

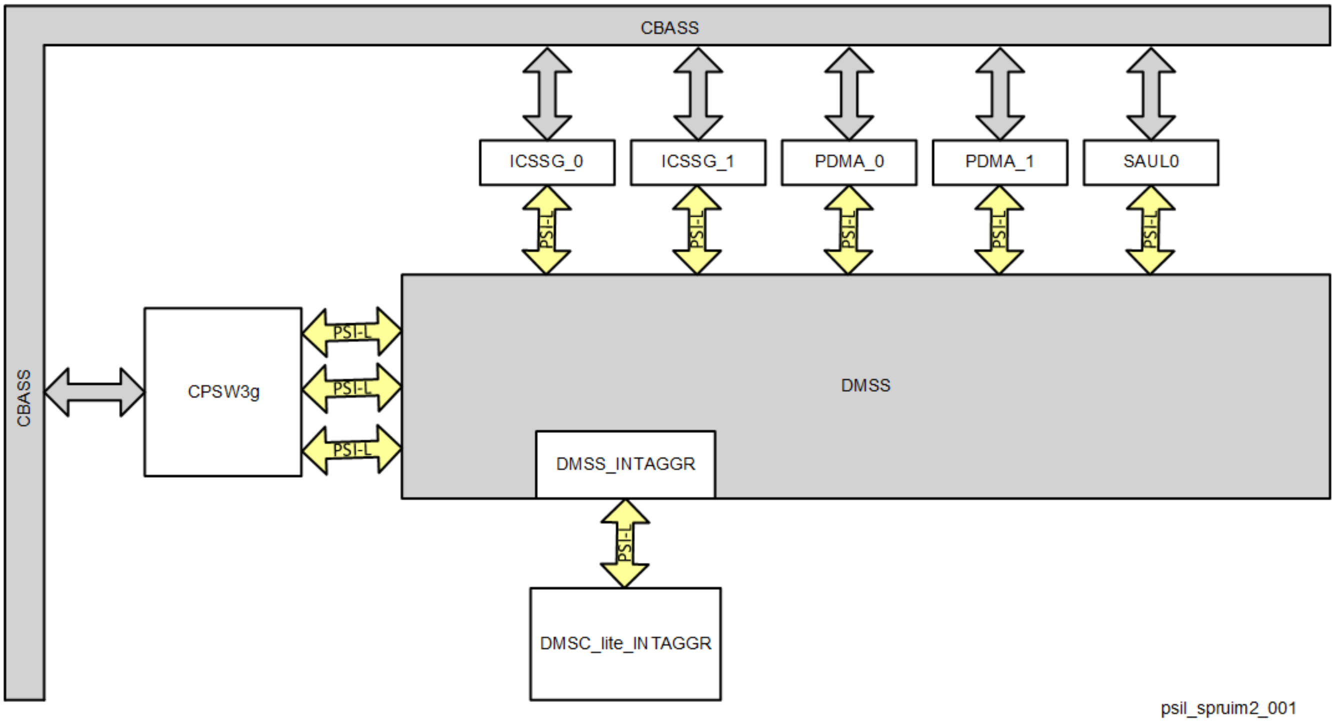


Figure 11-10. PSI-L Overview

11.2.5.2 PSI-L Functional Description

11.2.5.2.1 PSI-L Introduction

The PSI-L is used to transfer words of packet data and control information between two peer entities via direct connection. There are credits used for flow control to guarantee that blocking does not occur between threads. Multiple packet transfers can be ongoing simultaneously across a PSI-L interface each on a separate logical thread but all sharing a single data path through time division multiplexing. Each packet which is transferred is accompanied by a destination thread ID which indicates the logical destination thread to which the packet is being sent.

There is low level hardware handshake between PSI-L initiator and target used for transferring data. As it is blocking by nature, a higher level protocol is also used in which credits are maintained for each thread connection. Moments of non-readiness are allowed on the interface but there is no possibility that one thread can block another for an indefinite time since a thread must have credit for the destination before it is allowed to use the interface.

PSI-L Connection illustrates the point to point PSI-L connection.

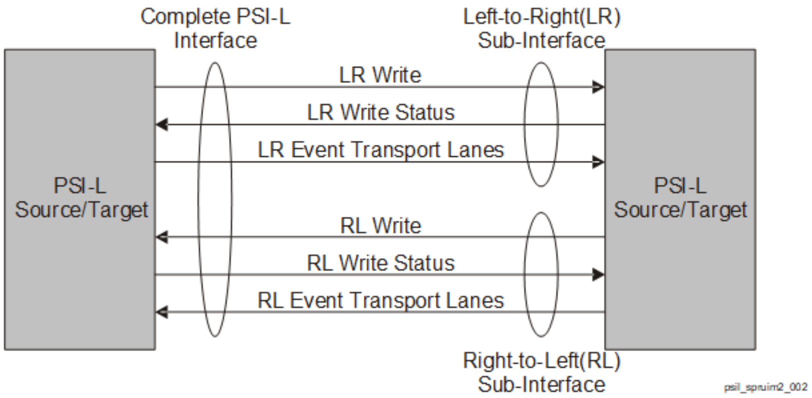


Figure 11-11. PSI-L Connection

PSI-L is intended to be a versatile interface which can carry various types of communications. The following table describes several types of threads which have been defined.

Table 11-75. Types of PSI-L Threads

Type	Description	Example Endpoints
Queue Management (QM) Messaging	Provides transport for queue push, pop, and divert messages to support distributed queue based work passing	Centralized queue manager or message manager and distributed DMA clients
Direct IO	Allows for tunneling CBASS compatible bus transactions through a PSI interconnect	Module which has no CBASS initiator to a remote proxy block
DMA Control Transport	Provides transport for DMA transfer descriptions from a source thread to a destination thread	DMA channel controller to DMA transfer controller
DMA Data Transport	Provides transport for packed data from a source thread to a destination thread	Packet oriented module like networking adapters to or from centralized DMA

Each thread on PSI-L is established between a single thread initiator and a single thread target using a connection oriented transfer mechanism. A thread initiator and a thread target are "paired" to create a logical connection between them referred to as a thread. Pairing is accomplished using a Pair Configuration Message which is valid in all thread types. Pairing can only occur between a thread initiator and a thread target of the same type.

11.2.5.2.2 PSI-L Operation

The PSI-L allows multiple independent streams of packet data (threads) to share a single interface using data phase granularity time division multiplexing. This time division multiplexing is accomplished by dividing each stream into single data transfers. In this way a stream is comprised of a sequence of strongly ordered data transfers but packet transfers between different streams are allowed to be interleaved. Each data phase is qualified with a type identifier which indicates whether the data is packet info, direct IO write or read info, timestamp, software info, control data, payload data, or status.

11.2.5.2.3 Event Transport

PSI-L provides a mechanism by which events can be transported within one or more optional subinterfaces on a link. These sub-interfaces are referred to as event transport lanes (ETLs) and are independent of any PSI-L packet or message transfers which may be ongoing on the other interfaces within the PSI-L. A maximum of one event can be transferred on each event transport lane in each clock cycle. The event transport protocol is a simple request-ready type of hardware handshake.

11.2.5.2.4 Threads

A thread is a complete flow-controlled stream of communication. The PSI-L thread space is divided into a 32K contiguous region representing all of the source threads (0x0000 - 0x7FFF) and a 32K contiguous region representing all of the destination threads (0x8000 - 0x8FFF).

Source threads are responsible for sending request transactions, accepting response transactions, and sending data transfer transactions. Destination threads are responsible for accepting request transactions, sending response transactions, and accepting data transfer transactions. A given thread generally performs only a single class of transactions (see PSI-L Defined Threads). Both source and destination threads may act as initiators for transfers on one of the PSI-L write sub-interfaces but in this case source threads are actually initiating data transfers while destination threads are only responding to a previous request issued by a source request. Source threads only transfer to destination threads and destination threads only transfer to source threads. Transfers between same thread types do not occur.

The following types of message transfers always originate from source threads and terminate in destination threads:

- Configuration write message
- Configuration read message
- QM push message
- QM pop message
- QM divert message
- Direct read operation message
- Direct write operation message
- DMA transfer request message
- DMA data message

The following types of message transfers always originate in destination threads and terminate in source threads:

- Configuration write response message
- Configuration read response message
- QM push response message
- QM pop response message
- QM divert response message
- DMA transfer response message

11.2.5.2.5 Arbitration Protocol

On each cycle, an arbiter built into the initiator side of each interface decides on which thread to transfer data in the next clock cycle. Both forward (from source threads) and reverse (from destination threads) direction transfers can occur across the same physical interface so the arbiter must ensure that sustained blocking of any thread can occur.

The decision about which thread to allow using the interface is based on the following factors:

1. Whether data is ready at the source to be sent
2. Whether credit exists for the thread such that it is guaranteed there is a place for the data to land in the destination endpoint. For reverse direction transfers (response messages), it is assumed that credit always exists.
3. The relative priority of the traffic that the thread is carrying for the given packet duration
4. Whether the transfer is for a forward or reverse direction thread (requests versus responses).

No thread can be considered for inclusion in arbitration unless both data is available and credit exists in the destination endpoint. For each thread which can be considered in the current arbitration cycle, the arbiter should then pick the thread with the highest priority. Reverse transfers should be considered higher priority than forward transfers.

11.2.5.2.6 Thread Configuration

Each source thread has programmable registers for configuring the pairing with a corresponding destination thread and for enabling data flow. Each destination thread has programmable registers for reporting the buffering capability of the thread and for enabling data flow. These registers are accessed using configuration read and write messages from a configuration host.

Each configuration write message sent from a configuration host is acknowledged with a configuration write response message from the addressed endpoint. Each configuration read message sent from a configuration host is acknowledged with a configuration read response message from the addressed endpoint.

11.2.5.2.6.1 Thread Pairing

Depending on the type of traffic that each source thread carries it may or may not have a fixed pairing with a destination thread.

11.2.5.2.6.1.1 Configuration Transaction Pairing

Configuration write and read transactions are only initiated by a special module called configuration proxy (PSILCFG_PROXY). Each configuration proxy in the system uses a single source thread which can initiate configuration write and read transactions to the configuration registers of every other source and destination thread in the PSI-L system. The PSILCFG_PROXY registers are described in *DMASS_PSILCFG_0 Registers*, located in *DMA Controller Registers*.

Each source thread routes to a single target thread and this pairing is specified by programming a required pairing register set for each thread. A source has no ability to change what target thread it talks to. If a source must be able to talk to different targets (or target threads), then it can either have multiple threads or a streaming switch that can be programmed to route the transfers appropriately based on specific packet fields.

11.2.5.2.6.2 Configuration Registers Region

The configuration registers region contains static configuration information including the settings for linking a thread source to a thread destination. These registers are described in *DMA Controller Registers*. The thread ID mapping is shown in *PSI-L System Thread Map*, located in *Module Integration*.

11.3 Peripheral DMA (PDMA)

This chapter describes the PDMA architecture in the device.

11.3.1 PDMA Controller

11.3.1.1 PDMA Overview

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers (MMRs) accessed via a standard non-coherent bus fabric. The PDMA module is located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured transfer request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer DMSS destination channel which then performs the movement of the data into memory. Likewise, a remote DMSS source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (DMSS + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

The PDMA is linked to the DMSS through a direct PSI-L connection. For more details, refer to *Packet Streaming Interface Link (PSI-L)*.

11.3.1.1.1 PDMA Features

11.3.1.1.1.1 PDMA - SPI Features

The PDMA0 and PDMA4- SPI module supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit(s)
  - Each unit supports write bursts up to 64 bytes (on selected channel types)
  - Write Unit 0
    - Provides a 32-bit wide VBUSP write-only initiator interface for peripheral accesses
- Provides 1 memory read access unit(s)
  - Supports 1 outstanding read per interface (VBUSP)
  - Supports read burst up to 64 bytes (on selected channel types)
  - Read Unit 0
    - Provides a 32-bit wide VBUSP read-only initiator interface for peripheral accesses
- Supports up to 15 simultaneous destination (Tx) channels
- Supports negative credit monitoring on Tx channels
- Supports up to 15 simultaneous source (Rx) channels
- Supports Static Transfer Requests Only
- Supports X-Y, MCAN, and AASRC transfer modes (as per configuration)
- Provides per-channel buffering:
  - Provides 8 128-bit word deep data FIFO for each destination channel
  - Provides 8 128-bit word deep data FIFO for each source channel
- Provides 128-bit wide PSI-L compliant data interface to and from DMSS endpoints and remote peripherals

11.3.1.1.1.2 PDMA1 - UART Features

The PDMA1 - UART module supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)

- Provides 1 memory write access unit(s)
  - Each unit supports write bursts up to 64 bytes (on selected channel types)
  - Write Unit 0
    - Provides a 32-bit wide VBUSP write-only initiator interface for peripheral accesses
- Provides 1 memory read access unit(s)
  - Supports 1 outstanding read per interface (VBUSP)
  - Supports read burst up to 64 bytes (on selected channel types)
  - Read Unit 0
    - Provides a 32-bit wide VBUSP read-only initiator interface for peripheral accesses
- Supports up to 7 simultaneous destination (Tx) channels
- Supports negative credit monitoring on Tx channels
- Supports up to 7 simultaneous source (Rx) channels
- Supports Static Transfer Requests Only
- Supports X-Y, MCAN, and AASRC transter modes (as per configuration)
- Provides per-channel buffering:
  - Provides 8 128-bit word deep data FIFO for each destination channel
  - Provides 8 128-bit word deep data FIFO for each source channel
- Provides 128-bit wide PSI-L compliant data interface to and from DMSS endpoints and remote peripherals

11.3.1.1.1.3 PDMA - McASP Features

The PDMA2 and PDMA3 - McASP module supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit(s)
  - Each unit supports write bursts up to 64 bytes (X-Y FIFO transfer mode only)
  - Write Unit 0
    - Provides a 32-bit wide VBUSP write-only initiator interface for peripheral accesses
- Provides 1 memory read access unit(s)
  - Supports 1 outstanding read per interface (VBUSP)
  - Supports read burst up to 64 bytes (X-Y FIFO transfer mode only)
  - Read Unit 0
    - Provides a 32-bit wide VBUSP read-only initiator interface for peripheral accesses
- Supports up to 2 simultaneous destination (Tx) channels
- Supports up to 2 simultaneous source (Rx) channels
- Supports Static Transfer Requests Only
- Supports X-Y, MCAN, and AASRC transter modes (as per configuration)
- Provides per-channel buffering:
  - Provides 8 128-bit word deep data FIFO for each destination channel
  - Provides 8 128-bit word deep data FIFO for each source channel
- Provides 128-bit wide PSI-L compliant data interface to and from DMSS endpoints and remote peripherals

11.3.1.1.1.4 PDMA - ADC Features

The PDMA5 - ADC module supports the following features:

- Implements CPPI 5.0 compliant Third Party Unified Transfer Controller
- Provides 0 memory write access unit(s)
  - Each unit supports write bursts up to 64 bytes (on selected channel types)
  - Provides 1 memory read access unit(s)
  - Supports 1 outstanding read per interface (VBUSP).
  - Supports read burst up to 64 bytes (on selected channel types)
  - Read Unit 0:
    - Provides a 32 bit wide VBUSP read only master interface for peripheral accesses.
- Supports up to 0 simultaneous destination (Tx) channels
  - Supports negative credit monitoring on Tx channels
  - Supports up to 2 simultaneous source (Rx) channels
  - Supports Static Transfer Requests Only

  - Supports X-Y, MCAN, and AASRC transfer modes (as per configuration)
  - Provides per-channel buffering:
    - Provides 8 128-bit word deep data FIFO for each destination channel
    - Provides 8 128-bit word deep data FIFO for each source channel
  - Provides 128 bit wide PSI-L compliant data interface to remote paired DMA and remote peripherals
  - Provides 128 bit wide PSI-L compliant data interface from remote paired DMA and remote peripherals

The module **does not** support the following:

- Dynamic Transfer Request
- Cross Channel Triggering

11.3.1.1.1.5 PDMA - ASRC Features

- Implements CPPI 5.0 compliant Third Party Unified Transfer Controller
- Provides 1 memory write access unit(s)
  - Each unit supports write bursts up to 64 bytes (on selected channel types)
  - Write Unit 0:
    - Provides a 32 bit wide VBUSP write only master interface for peripheral accesses.
  - Provides 1 memory read access unit(s)
  - Supports 1 outstanding read per interface (VBUSP).
  - Supports read burst up to 64 bytes (on selected channel types)
  - Read Unit 0:
    - Provides a 32 bit wide VBUSP read only master interface for peripheral accesses.

  Supports up to 8 simultaneous destination (Tx) channels
- Supports negative credit monitoring on Tx channels
- Supports up to 8 simultaneous source (Rx) channels
- Supports Static Transfer Requests Only
- Supports X-Y, MCAN, and AASRC transfer modes (as per configuration)
- Provides per-channel buffering:
  - Provides 8 128-bit word deep data FIFO for each destination channel
  - Provides 8 128-bit word deep data FIFO for each source channel
- Provides 128 bit wide PSI-L compliant data interface to remote paired DMA and remote peripherals
- Provides 128 bit wide PSI-L compliant data interface from remote paired DMA and remote peripherals

The module **does not** support the following:

- Dynamic Transfer Request
- Cross Channel Triggering

Note

Some features may not be available. See *Module Integration* for more information.

11.3.1.2 Functional Description - SPI

11.3.1.2.1 Compliance to Standards

The PDMA complies fully to all standards listed in the previous section.

11.3.1.2.2 Functional Operation

The Peripheral DMA is a simple, low cost implementation of the CPPI 5.0 Unified Transfer Controller. The PDMA module is required to be located close to one or more peripherals (both peripherals and PDMA direct connected to the SCR) which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only the static Transfer Request subset of UTC features which are useful for peripheral type transactions. Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs time division multiplexing between channels in order to share the underlying DMA hardware. A scheduler is provided to control the ordering and rate at which this multiplexing occurs. A block diagram of the PDMA Controller is shown below.

11.3.1.2.2.1 Submodule Descriptions

11.3.1.2.2.1.1 Scheduler

The Scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low level read or write operation.

11.3.1.2.2.1.2 Tx Per Channel Buffers

The Tx Per Channel Buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx Per Channel Buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.2.2.1.3 Tx DMA Unit

The Tx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming dma event and then writes data from the Tx Per Channel Data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.2.2.1.4 Rx Per Channel Buffers

Rx Per Channel Buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte oriented on write so that the data from the Rx DMA units which may not be full words can be packed properly. The buffers are word oriented on read in accordance with the transport mechanism outlined in the PSI-L Interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface. The Rx Per Channel Buffer block outputs queue fullness information to the scheduler block which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Rx Per Channel Buffer will initiate transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block will simultaneously monitor the status of all of the threads and will perform a round robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer will be included in the arbitration.

11.3.1.2.2.1.5 Rx DMA Unit

The Rx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx Per Channel Data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.2.2.2 General Functionality (Applicable to All Functions/Modes)

11.3.1.2.2.2.1 Operational States

At any given time, the PDMA can be in one of three different states, as shown in Table 11-76.

Table 11-76. Operational States

Operational State	Description
Init	This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the init state, the DMA will de-assert all ready signals on all applicable target interfaces and will de-assert all request signals on all applicable controller interfaces. The PDMA will automatically transition out of the init state into the idle state when all of the RAM initialization has been completed.

Table 11-76. Operational States (continued)

Operational State	Description
Idle	Once the PDMA leaves the Init state, it enters the Idle state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The Idle state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. For clock stop purposes, the module will only report idle if all DMA channels are disabled using the enable bit in PSIL register 2 for each channel.
Active	The PDMA enters the active state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent) the PDMA transitions to the Idle state.

11.3.1.2.2.2.2 Clock Stop

The clock stop interface is a request/acknowledge interface used to coordinate the handshaking of properly stopping the main clock to the IP. Before attempting to perform a clock stop operation, software is required to teardown all active channels (via UDMAP 'real time' registers in the UDMAP, or PSIL register 0x408 in PSIL based peripherals), and after this is complete, also clear the global enable bit for all channels (via PSIL register 0x2 in both the UDMAP and PSIL based peripherals). Attempting a clock stop on the IP without first performing the channel teardowns or clearing of global enable bits will result in IP specific behavior that may be UNDEFINED.

The PDMA will not drive clock stop IDLE or clock stop ACK while the global enable (PSIL register 0x2) is set for any channel.

11.3.1.2.2.2.3 Emulation Control

The emulation control input (susp_emususp) and the per channel emulation control 'free' bit allow DMA operation to be suspended on a per channel basis. When the emulation suspend state is entered, the DMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. Emulation control is implemented for compatibility with other peripherals. Each source and destination channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is controlled via the 'free' bit in the channel Enable Register. Note the real time emulation suspend request signal is not supported.

11.3.1.2.2.2.4 Dynamic Clock Gating

The PDMA includes up to two mid level clock gates using ksdw_pm_clkgate(). One is on the main clock of the PDMA while the other is on the interal ecc_aggr (when RAM is used). These clock gates turn off the clock to their corresponding IP under idle conditions, and then turn the clock back on when work is to be done. Detecting work is done via internal state, or activity on the PSIL or DMA triggers. The DMA triggers are thus always monitored, even when the clocking to the rest of the IP is disabled.

The dynamic clock gating can be disabled through an external port called pwr_disable_nogate. No additional signaling is needed to support the dynamic clock gate, although the PDMA supports the 'early wake' pins on PSIL and VBUSP.

11.3.1.2.2.3 Events and Flow Control

The following sections describe the simplified mechanism that is provided on the Peripheral DMA for triggering.

11.3.1.2.2.3.1 Channel Triggering

Channels must be triggered in order for them to perform work. A local event input bus is provided on the peripheral DMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, etc.). The event inputs for XY mode are triggered either via pulse, or by a clock synchronous rising edge. The counting mode is a design time configuration parameter. In MCAN mode, the inputs are expected to be single cycle pulses, synchronous with the PDMA clock.

- Event signals that are used in pulse mode must be sourced by the same clock as the PDMA.
- Event signals that are used in edge mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the PDMA clock, and they must remain high for at least 1 'slow' clock cycle.

The PDMA provides a 2 bit counter per event input to accommodate startup latency in the channel. (In AASRC mode, the signals are not counted, but latched whenever asserted.)

11.3.1.2.2.3.2 Completion Events

All transfers on PDMA are split TR in that they have a UDMA-P half and a (static) PDMA half. Completion events are designed to be triggered from the UDMA-P half of the split TR.

11.3.1.2.2.3.3 Channel Types

Each channel in the Peripheral DMA is configured at design time to be either standard X-Y FIFO mode or MCAN channel. The channel type is configured at design time, and can not be changed by software.

11.3.1.2.2.3.3.1 X-Y FIFO Mode

Most peripherals which are serviced by the Peripheral DMA follow the pattern of transferring X bytes from a fixed, non-changing address in a loop Y times for each triggering event that is received. The X parameter is typically 1-16 bytes and the Y parameter can be any integer up to 2048. If a peripheral can be serviced by this basic functionality then it is recommended to use this mode for the peripheral.

11.3.1.2.2.3.3.2 MCAN Mode

The MCANSS subsystem was found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the DMA will start out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, MCAN packet fragmentation requirement to place an 8 byte header on each 64 byte chunk that is transmitted and to remove the header from each 64 byte chunk (other than the first block) that is received.

11.3.1.2.2.3.3.3 AASRC Mode

The AASRC mode of the PDMA is similar to the X-Y mode in that X specifies the sample width, any Y specifies the number of FIFO samples to transfer per DMA request, but in addition to this, a programmable FIFO list is supplied that allows a single PDMA channel to transfer data to multiple FIFOs. The FIFO list specifies which FIFOS to access, and in which order to access them. Both AASRC 'stream' and 'group' modes are supported in terms of DMA signalling and the FIFO memory map. When in AASRC mode, the entire PDMA operates exclusively in this mode. AASRC channels to not share the same PDMA as do XY and MCAN channels.

The following addition details apply to the PDMA in AASRC mode:

Main Features:

- Up to 16 independent RX channels and 16 TX channels
  - Each channel represents a different data stream to either the UDMA-P-P or a McASP PDMA
- Each channel can be configured to read or write any of the AASRC FIFOs in any order
- Packing support for 1, 2, 3, and 4 byte samples
  - Can directly talk to a McASP using any McASP data format
  - Packing sample size is fixed for a given channel
- Supports both Group and Stream AASRC signaling and FIFO memory maps
  - There is a single stream/group mode setting for each PDMA channel

Additional details:

- Each channel has a 'mask' of which DMA requests must fire to activate the channel
  - In stream mode, the mask specifies the all the FIFO DMA requests that must fire
  - In group mode, the mask specifies the one group DMA request that must fire
- Each channel specifies an ordered list of how FIFOs should be accessed
  - All channels use a common list, specifying a range of entry indices within that list. This allows each channel to use a varying number of list elements.
  - The order list can be processed multiple times per DMA request. The number of samples to be transferred per request must match the configured threshold for the DMA request in the AASRC.
- All FIFOs are specified by index only

  - In the TX ordering table, the indices are assumed to be TX FIFOs
  - In the RX ordering table, the indices are assumed to be RX FIFOs
  - If a DMA channel is in 'Group Mode', the PDMA assumes the indices referenced by that channel represent Group Mode FIFOs; otherwise, it assumes Stream Mode FIFOs.
- The PDMA has configured base addressed and inter-FIFO spans such that is can always convert from a FIFO index to the proper Stream or Group mode FIFO address.

11.3.1.2.2.4 Transmit Operation

11.3.1.2.2.4.1 Destination (Tx) Channel Allocation

A total of 17 destination channels are provided within the DMA for concurrent transfers from Tx per channel buffers to the various attached peripherals. Each Tx channel requires a single PSI-L thread. The Tx channels are allocated as in the following table.

Table 11-77. Tx Channel Allocation

Tx DMA Channel	Function	Channel Type	Trigger Mode	Data FIFO Address	Strobe MMR Address	Control FIFO Address
8000	SPI 3 Tx Ch 0	XY	edge	000020130138	000000000000	000000000000
8001	SPI 3 Tx Ch 1	XY	edge	00002013014C	000000000000	000000000000
8002	SPI 3 Tx Ch 2	XY	edge	000020130160	000000000000	000000000000
8003	SPI 3 Tx Ch 3	XY	edge	000020130174	000000000000	000000000000
8004	SPI 4 Tx Ch 0	XY	edge	000020140138	000000000000	000000000000
8005	SPI 4 Tx Ch 1	XY	edge	00002014014C	000000000000	000000000000
8006	SPI 4 Tx Ch 2	XY	edge	000020140160	000000000000	000000000000
8007	SPI 4 Tx Ch 3	XY	edge	000020140174	000000000000	000000000000
8008	MCAN 2 Tx Ch 0	MCAN	pulse	000020728000	0000207210D0	000000000000
8009	MCAN 2 Tx Ch 1	MCAN	pulse	000020728048	0000207210D0	000000000000
800a	MCAN 2 Tx Ch 2	MCAN	pulse	000020728090	0000207210D0	000000000000
800b	MCAN 3 Tx Ch 0	MCAN	pulse	000020738000	0000207310D0	000000000000
800c	MCAN 3 Tx Ch 1	MCAN	pulse	000020738048	0000207310D0	000000000000
800d	MCAN 3 Tx Ch 2	MCAN	pulse	000002708090	0000207310D0	000000000000
800e	MCAN 4 Tx Ch 0	MCAN	pulse	000020748000	0000207410D0	000000000000
800f	MCAN 4 Tx Ch 1	MCAN	pulse	000020748048	0000207410D0	000000000000
8010	MCAN 4 Tx Ch 2	MCAN	pulse	000020748090	0000207410D0	000000000000

11.3.1.2.2.4.2 Destination (Tx) Channel Out of Band Signals

The following table shows how PSIL signals are handled for destination channels.

Table 11-78. Tx Channel Out of Band Signals

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sop	ignored	ignored
eop	ignored	closes current MCAN packet
sol	ignored	ignored
eol	ignored	ignored
drop	ignored	ignored
pkt_error	ignored	ignored
tdown	reflect in status, teardown when data marker reached	reflect in status, teardown when data marker reached

11.3.1.2.2.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will need to first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.2.2.4.3.1 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host will pair each destination PDMA channel with (typically) a corresponding source channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the UDMA-P will send all their data to the destination channel in the PDMA and the destination channel in the PDMA will never see any data other than data from the source channel in the UDMA-P.

11.3.1.2.2.4.3.2 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies somewhat.

11.3.1.2.2.4.3.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
Z	0x401	23:0	Not used

11.3.1.2.2.4.3.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information.
Acc32	0x400	30	Not used
X	0x400	26:24	Not used

Param	PSIL Addr	Field	Description
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8 byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
Z	0x401	23:0	Not used

11.3.1.2.2.4.3.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer to each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
Z	0x401	23:0	Not used

11.3.1.2.2.4.3.3 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled in order to accept data. Threads are enabled or disabled by setting or clearing the enable bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.2.2.4.4 Data Transfer

Packet transmission is accomplished within the PDMA by unpacking and moving data from the Tx Per Channel FIFOs which were filled via the Transmit PSI-L Interface to specified memory mapped address ranges via the VBUSP controller interfaces. On the Tx side of the PDMA, these transfers are always writes. Each write transfer which is performed by the Tx DMA Unit is to a destination address that is hardcoded in the channel at design time and of a size as specified in the static Transfer Request.

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during transmit is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.2.2.4.4.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter writes of 'X' parameter bytes to the data_address specified in the tchan_info parameter for the channel. Each write that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The write transfers that are performed will be accomplished as quickly as possible given availability of data in the Tx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.2.2.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.2.2.4.4.2 MCAN Mode Channel

The PDMA channel will remain idle until data is received from the UDMA-P over the PSIL interface. At this time, the PDMA will immediately start copying packet bytes into the MCAN TX buffer corresponding the PDMA/MCAN channel. The number of bytes copied is smaller of the remaining bytes in the packet, or the value of the 'Y' parameter. Once a TX buffer has been filled, the PDMA will transfer ownership of the buffer to MCAN by performing an MCAN register write. The PDMA will then wait to regain ownership of the TX buffer by waiting for the corresponding MCAN TX event. At this time, the PDMA will continue with refilling the TX buffer for the next packet fragment. On subsequent fills (until the end of packet is reached), the PDMA will skip over the 8 byte MCAN header, leaving the original contents from the initial fragment copy in place.

11.3.1.2.2.4.4.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.2.2.4.4.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's TxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the TxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it will start reading FIFO index values from the TxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs written for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width written to the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The write transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.2.2.4.5 Transmit PSI-L Interface Transactions

The PDMA will accept data across the Tx PSI-L Interface in accordance with the physical handshaking protocol as defined in the PSI-L Interface specification. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_i_link	This signal is asserted high to indicate the PSI-L link is valid.
strm_i_ready	This signal is asserted high anytime there is space in the PSI-L ingress fifo.
strm_i_sreq	This signal is asserted high anytime there is credit return data waiting in the PSI-L status fifo.
strm_i_sthreadid	This is set to the local destination thread that is returning credit.
strm_i_sccnt	This is set to the number of credits being returned, or 0 on a TX teardown acknowledgement.

11.3.1.2.2.4.6 Tx Pause

The Host initiates a channel pause by setting the pause bit in the RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.2.2.4.7 Tx Teardown

The Host initiates a channel teardown by setting the tdown bit in the UDMA-P channel that is paired with the PDMA. The UDMA-P communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous UDMA-P data for the channel has been flushed. At this time, the teardown state will be reflected in the PSI-L RT Enable register of the PDMA. Note that a non-synchronized teardown can also be initiated by directly clearing the enable bit in the PSI-L RT Enable register of the PDMA.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel will be cleared in the PSI-L RT enable register, but the teardown bit will remain high. A teardown completion indication is sent back across the status pins of the PSI-L in the form of a credit response with sccnt=0. Upon completion, no further packet processing will occur until the Host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the UDMA-P transmission stops on a data boundary that is not compatible with the static TR configuration, the flush bit in the RT enable register can be set to guarantee that all data can be properly flushed from the internal pipe.

11.3.1.2.2.4.8 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L Enable register. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.2.2.4.9 Tx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as in the following table.

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.

Name	PSIL Addr	Field	Description
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Flush	0x403	30	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
Pause	0x403	29	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.
Data	0x403	28	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
XData	0x403	27	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.

11.3.1.2.2.5 Receive Operation

11.3.1.2.2.5.1 Source (Rx) Channel Allocation

A total of 17 source channels are provided within the DMA for concurrent transfers from the various attached peripherals into the Rx per channel buffers and on to the PSI-L Rx Interface. Each Rx channel requires a single PSI-L thread. The Rx channels are allocated as in *Rx Channel Allocation.*

Table 11-79. Rx Channel Allocation

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
0	SPI 3 Rx Ch 0	XY	edge	00002013013C	000000000000	000000000000
1	SPI 3 Rx Ch 1	XY	edge	000020130150	000000000000	000000000000
2	SPI 3 Rx Ch 2	XY	edge	000020130164	000000000000	000000000000
3	SPI 3 Rx Ch 3	XY	edge	000020130178	000000000000	000000000000
4	SPI 4 Rx Ch 0	XY	edge	00002014013C	000000000000	000000000000
5	SPI 4 Rx Ch 1	XY	edge	000020140150	000000000000	000000000000
6	SPI 4 Rx Ch 2	XY	edge	000020140164	000000000000	000000000000
7	SPI 4 Rx Ch 3	XY	edge	000020140178	000000000000	000000000000
8	MCAN 2 Rx Ch 0	XY	pulse	000020728900	000020721098	000000000000
9	MCAN 2 Rx Ch 1	XY	pulse	000020728990	000020721098	000000000000
10	MCAN 2 Rx Ch 2	XY	pulse	000020728A20	000020721098	000000000000
11	MCAN 3 Rx Ch 0	XY	pulse	000020738900	000020731098	000000000000
12	MCAN 3 Rx Ch 1	XY	pulse	000020738990	000020731098	000000000000
13	MCAN 3 Rx Ch 2	XY	pulse	000020738A20	000020731098	000000000000
14	MCAN 4 Rx Ch 0	XY	pulse	000020748900	000020741098	000000000000
15	MCAN 4 Rx Ch 1	XY	pulse	000020748990	000020741098	000000000000
16	MCAN 4 Rx Ch 2	XY	pulse	000020748A20	000020741098	000000000000

11.3.1.2.2.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will need to first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.2.2.5.2.1 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host will pair each source PDMA channel with (typically) a corresponding destination channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA will send all their data to the source channel in the UDMA-P and the destination channel in the UDMA-P will never see any data other than data from the source channel in the PDMA.

11.3.1.2.2.5.2.2 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.2.2.5.2.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.2.2.5.2.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information.
Acc32	0x400	30	Not used
X	0x400	26:24	Not used

Param	PSIL Addr	Field	Description
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an 'EOP' indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8 byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

11.3.1.2.2.5.2.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each read which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full DMA request operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.2.2.5.2.3 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.2.2.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.2.2.5.3.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the Rx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.2.2.5.3.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.2.2.5.3.2 MCAN Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA will start copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN will skip the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0

CAN FE2	CAN FE1	CAN FE0	Description
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example the following two filter entries will setup a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0:

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.2.2.5.3.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.2.2.5.3.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it will start reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.2.2.5.4 Receive PSI-L Interface Transactions

When an entire word has been packed into the Rx Per Channel Buffer for a given channel, a one word data phase transfer will be initiated for that channel/thread on the Rx PSI-L interface and the data will be popped from the Rx Per Channel FIFO. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_o_req	This signal is asserted when the PDMA determines that there is at least 1 word of data in it's TP-CC output FIFO
strm_o_sthread_id	Set equal to the TP-CC DMA channel number which is on the interface for this cycle

Pin	Output Value / Source From PDMA
strm_o_dthread_id	Set equal to the target thread ID value given in the PSI-L pairing configuration registers for this DMA channel
strm_o_data_type	Will be set to the proper PSI-L data type. The PDMA can send config response, PSI info word 0, and PSI data word.
strm_o_wnum	Set equal to the packing lane for the current word within a contiguous transfer. This value will start at 0 for each new TR and will increment for each subsequent data phase in the TR.
strm_o_lastw	This signal will be asserted coincident with eop.
strm_o_xcnt	The xcnt will be equal to the data path width in bytes.
strm_o_worden	The worden will be modulated to indicate which 32-bit words are valid within each control type data phase.
strm_o_data	The data will be packed/left justified to comply to the big endian data ordering as required in the PSI-L I/F specification.
strm_o_sop	This signal is asserted for 1 data phase at the beginning of each new TR or data transfer packet.
strm_o_eop	This signal is asserted for 1 data phase at the end of each TR or data transfer packet.
strm_o_sol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the start of a new set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_eol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the end of a set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_priv	Set to zero.
strm_o_privid	Set to zero.
strm_o_virtid	Set to zero.
strm_o_secure	Set to zero.
strm_o_interest	Set to zero.
strm_o_sready	Always asserted as the PDMA is always able to accept credit returns.

11.3.1.2.2.5.5 Rx Pause

The Host initiates a channel pause by setting the pause bit in RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.2.2.5.6 Rx Teardown

The Host initiates a RX channel teardown by setting the tdown bit in the RT enable register for the target RX channel. The PDMA communicates the teardown state to the UDMA-P through the PSI-L data channel, to ensure that the teardown is not seen by the UDMA-P until all the previous PDMA data for the channel has been flushed.

The PDMA will not stop reading peripheral data until it reaches a FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. It will always attempt to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA will then clear the enable bit in the pairing register, however the teardown bit will remain set. No further packet processing will occur until the Host re-configures the channel. The teardown process will propagate to the UDMA-P and its final status can be checked there.

11.3.1.2.2.5.7 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L enable register. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.2.2.5.8 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as follows.

Name	PSIL Addr	Field	Description
Z*	0x402	31:16	This field holds the lower 12 bits of the current Z count for legacy pursposes. See register 0x40F below for the full width version of Z.
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Tdown	0x403	30	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
Pause	0x403	29	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is un-paused or disabled.
Space	0x403	28	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
XSpace	0x403	27	When set, there is a enough internal FIFO space available to start servicing a peripheral DMA event.
Buffer	0x403	26	This is the current RX buffer (0/1) for the current MCAN receive operation.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.
Z	0x40F	31:0	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

11.3.1.3 Functional Description - UART

11.3.1.3.1 Compliance to Standards

The PDMA complies fully to all standards listed in the previous section.

11.3.1.3.2 Functional Operation

The Peripheral DMA is a simple, low cost implementation of the CPPI 5.0 Unified Transfer Controller. The PDMA module is required to be located close to one or more peripherals (both peripherals and PDMA direct connected to the SCR) which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only the static Transfer Request subset of UTC features which are useful for peripheral type transactions. Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs time division multiplexing between channels in order to share the underlying DMA hardware. A scheduler is provided to control the ordering and rate at which this multiplexing occurs. A block diagram of the PDMA Controller is shown below.

11.3.1.3.2.1 Submodule Descriptions

11.3.1.3.2.1.1 Scheduler

The Scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low level read or write operation.

11.3.1.3.2.1.2 Tx Per Channel Buffers

The Tx Per Channel Buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx Per Channel Buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.3.2.1.3 Tx DMA Unit

The Tx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming dma event and then writes data from the Tx Per Channel Data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.3.2.1.4 Rx Per Channel Buffers

Rx Per Channel Buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte oriented on write so that the data from the Rx DMA units which may not be full words can be packed properly. The buffers are word oriented on read in accordance with the transport mechanism outlined in the PSI-L Interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface. The Rx Per Channel Buffer block outputs queue fullness information to the scheduler block which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Rx Per Channel Buffer will initiate transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block will simultaneously monitor the status of all of the threads and will perform a round robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer will be included in the arbitration.

11.3.1.3.2.1.5 Rx DMA Unit

The Rx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx Per Channel Data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.3.2.2 General Functionality (Applicable to All Functions/Modes)

11.3.1.3.2.2.1 Operational States

At any given time, the PDMA can be in one of three different states, as shown in Table 11-80.

Table 11-80. Operational States

Operational State	Description
Init	This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the init state, the DMA will de-assert all ready signals on all applicable target interfaces and will de-assert all request signals on all applicable controller interfaces. The PDMA will automatically transition out of the init state into the idle state when all of the RAM initialization has been completed.
Idle	Once the PDMA leaves the Init state, it enters the Idle state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The Idle state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. For clock stop purposes, the module will only report idle if all DMA channels are disabled using the enable bit in PSIL register 2 for each channel.
Active	The PDMA enters the active state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent) the PDMA transitions to the Idle state.

11.3.1.3.2.2.2 Clock Stop

The clock stop interface is a request/acknowledge interface used to coordinate the handshaking of properly stopping the main clock to the IP. Before attempting to perform a clock stop operation, software is required to teardown all active channels (via UDMAP 'real time' registers in the UDMAP, or PSIL register 0x408 in PSIL based peripherals), and after this is complete, also clear the global enable bit for all channels (via PSIL register 0x2 in both the UDMAP and PSIL based peripherals). Attempting a clock stop on the IP without first performing the channel teardowns or clearing of global enable bits will result in IP specific behavior that may be UNDEFINED.

The PDMA will not drive clock stop IDLE or clock stop ACK while the global enable (PSIL register 0x2) is set for any channel.

11.3.1.3.2.2.3 Emulation Control

The emulation control input (susp_emususp) and the per channel emulation control 'free' bit allow DMA operation to be suspended on a per channel basis. When the emulation suspend state is entered, the DMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. Emulation control is implemented for compatibility with other peripherals. Each source and destination channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is controlled via the 'free' bit in the channel Enable Register. Note the real time emulation suspend request signal is not supported.

11.3.1.3.2.2.4 Dynamic Clock Gating

The PDMA includes up to two mid level clock gates using ksdw_pm_clkgate(). One is on the main clock of the PDMA while the other is on the interal ecc_aggr (when RAM is used). These clock gates turn off the clock to their corresponding IP under idle conditions, and then turn the clock back on when work is to be done. Detecting work is done via internal state, or activity on the PSIL or DMA triggers. The DMA triggers are thus always monitored, even when the clocking to the rest of the IP is disabled.

The dynamic clock gating can be disabled through an external port called pwr_disable_nogate. No additional signaling is needed to support the dynamic clock gate, although the PDMA supports the 'early wake' pins on PSIL and VBUSP.

11.3.1.3.2.3 Events and Flow Control

The following sections describe the simplified mechanism that is provided on the Peripheral DMA for triggering.

11.3.1.3.2.3.1 Channel Triggering

Channels must be triggered in order for them to perform work. A local event input bus is provided on the peripheral DMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, etc.). The event inputs for XY mode are triggered either via pulse, or by a clock synchronous rising edge. The counting mode is a design time configuration parameter. In MCAN mode, the inputs are expected to be single cycle pulses, synchronous with the PDMA clock.

- Event signals that are used in pulse mode must be sourced by the same clock as the PDMA.
- Event signals that are used in edge mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the PDMA clock, and they must remain high for at least 1 'slow' clock cycle.

The PDMA provides a 2 bit counter per event input to accommodate startup latency in the channel. (In AASRC mode, the signals are not counted, but latched whenever asserted.)

11.3.1.3.2.3.2 Completion Events

All transfers on PDMA are split TR in that they have a UDMA-P half and a (static) PDMA half. Completion events are designed to be triggered from the UDMA-P half of the split TR.

11.3.1.3.2.3.3 Channel Types

Each channel in the Peripheral DMA is configured at design time to be either standard X-Y FIFO mode or MCAN channel. The channel type is configured at design time, and can not be changed by software.

11.3.1.3.2.3.3.1 X-Y FIFO Mode

Most peripherals which are serviced by the Peripheral DMA follow the pattern of transferring X bytes from a fixed, non-changing address in a loop Y times for each triggering event that is received. The X parameter is typically 1-16 bytes and the Y parameter can be any integer up to 2048. If a peripheral can be serviced by this basic functionality then it is recommended to use this mode for the peripheral.

11.3.1.3.2.3.3.2 MCAN Mode

The MCANSS subsystem was found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the DMA will start out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, MCAN packet fragmentation requirement to place an 8 byte header on each 64 byte chunk that is transmitted and to remove the header from each 64 byte chunk (other than the first block) that is received.

11.3.1.3.2.3.3.3 AASRC Mode

The AASRC mode of the PDMA is similar to the X-Y mode in that X specifies the sample width, any Y specifies the number of FIFO samples to transfer per DMA request, but in addition to this, a programmable FIFO list is supplied that allows a single PDMA channel to transfer data to multiple FIFOs. The FIFO list specifies which FIFOS to access, and in which order to access them. Both AASRC 'stream' and 'group' modes are supported in terms of DMA signalling and the FIFO memory map. When in AASRC mode, the entire PDMA operates exclusively in this mode. AASRC channels to not share the same PDMA as do XY and MCAN channels.

The following addition details apply to the PDMA in AASRC mode:

Main Features:

- Up to 16 independent RX channels and 16 TX channels
  - Each channel represents a different data stream to either the UDMA-P-P or a McASP PDMA
- Each channel can be configured to read or write any of the AASRC FIFOs in any order
- Packing support for 1, 2, 3, and 4 byte samples
  - Can directly talk to a McASP using any McASP data format
  - Packing sample size is fixed for a given channel
- Supports both Group and Stream AASRC signaling and FIFO memory maps
  - There is a single stream/group mode setting for each PDMA channel

Additional details:

- Each channel has a 'mask' of which DMA requests must fire to activate the channel
  - In stream mode, the mask specifies the all the FIFO DMA requests that must fire
  - In group mode, the mask specifies the one group DMA request that must fire
- Each channel specifies an ordered list of how FIFOs should be accessed

  - All channels use a common list, specifying a range of entry indices within that list. This allows each channel to use a varying number of list elements.
  - The order list can be processed multiple times per DMA request. The number of samples to be transferred per request must match the configured threshold for the DMA request in the AASRC.
- All FIFOs are specified by index only
  - In the TX ordering table, the indices are assumed to be TX FIFOs
  - In the RX ordering table, the indices are assumed to be RX FIFOs
  - If a DMA channel is in 'Group Mode', the PDMA assumes the indices referenced by that channel represent Group Mode FIFOs; otherwise, it assumes Stream Mode FIFOs.
- The PDMA has configured base addressed and inter-FIFO spans such that is can always convert from a FIFO index to the proper Stream or Group mode FIFO address.

11.3.1.3.2.4 Transmit Operation

11.3.1.3.2.4.1 Destination (Tx) Channel Allocation

A total of 7 destination channels are provided within the DMA for concurrent transfers from Tx per channel buffers to the various attached peripherals. Each Tx channel requires a single PSI-L thread. The Tx channels are allocated as shown in Table 11-81.

Table 11-81. Tx Channel Allocation

Tx DMA Channel	Function	Channel Type	Trigger Mode	Data FIFO Address	Strobe MMR Address	Control FIFO Address
8000	USART 0 Tx Ch 0	XY	edge	000002800000	000000000000	000000000000
8001	USART 1 Tx Ch 0	XY	edge	000002810000	000000000000	000000000000
8002	USART 2 Tx Ch 0	XY	edge	000002820000	000000000000	000000000000
8003	USART 3 Tx Ch 0	XY	edge	000002830000	000000000000	000000000000
8004	USART 4 Tx Ch 0	XY	edge	000002840000	000000000000	000000000000
8005	USART 5 Tx Ch 0	XY	edge	000002850000	000000000000	000000000000
8006	USART 6 Tx Ch 0	XY	edge	000002860000	000000000000	000000000000

11.3.1.3.2.4.2 Destination (Tx) Channel Out of Band Signals

The following table shows how PSIL signals are handled for destination channels.

Table 11-82. Tx Channel Out of Band Signals

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sop	ignored	ignored
eop	ignored	closes current MCAN packet
sol	ignored	ignored
eol	ignored	ignored
drop	ignored	ignored
pkt_error	ignored	ignored
tdown	reflect in status, teardown when data marker reached	reflect in status, teardown when data marker reached

11.3.1.3.2.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will need to first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.3.2.4.3.1 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host will pair each destination PDMA channel with (typically) a corresponding source channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the UDMA-P will send all their data to the destination channel in the PDMA and the destination channel in the PDMA will never see any data other than data from the source channel in the UDMA-P.

11.3.1.3.2.4.3.2 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.3.2.4.3.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
Z	0x401	23:0	Not used

11.3.1.3.2.4.3.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information.
Acc32	0x400	30	Not used
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8 byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
Z	0x401	23:0	Not used

11.3.1.3.2.4.3.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used

Param	PSIL Addr	Field	Description
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer to each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
Z	0x401	23:0	Not used

11.3.1.3.2.4.3.2.4 AASRC TxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this TX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each TX FIFO. The flags corresponding to all TX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.3.2.4.3.2.5 AASRC TxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	TX FIFO Index for slot 7
27:24	Entry6	6	TX FIFO Index for slot 6
23:20	Entry5	5	TX FIFO Index for slot 5
19:16	Entry4	4	TX FIFO Index for slot 4
15:12	Entry3	3	TX FIFO Index for slot 3
11:8	Entry2	2	TX FIFO Index for slot 2
7:4	Entry1	1	TX FIFO Index for slot 1
3:0	Entry0	0	TX FIFO Index for slot 0

11.3.1.3.2.4.3.2.6 AASRC TxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	TX FIFO Index for slot 15
27:24	Entry14	14	TX FIFO Index for slot 14
23:20	Entry13	13	TX FIFO Index for slot 13
19:16	Entry12	12	TX FIFO Index for slot 12
15:12	Entry11	11	TX FIFO Index for slot 11
11:8	Entry10	10	TX FIFO Index for slot 10
7:4	Entry9	9	TX FIFO Index for slot 9
3:0	Entry8	8	TX FIFO Index for slot 8

11.3.1.3.2.4.3.3 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled in order to accept data. Threads are enabled or disabled by setting or clearing the enable bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.3.2.4.4 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.3.2.4.4.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the Rx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.3.2.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.3.2.4.4.2 MCAN Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA will start copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN will skip the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example the following two filter entries will setup a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0:

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.3.2.4.4.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.3.2.4.4.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it will start reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.3.2.4.5 Transmit PSI-L Interface Transactions

The PDMA will accept data across the Tx PSI-L Interface in accordance with the physical handshaking protocol as defined in the PSI-L Interface specification. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_i_link	This signal is asserted high to indicate the PSI-L link is valid.
strm_i_ready	This signal is asserted high anytime there is space in the PSI-L ingress fifo.
strm_i_sreq	This signal is asserted high anytime there is credit return data waiting in the PSI-L status fifo.
strm_i_sthreadid	This is set to the local destination thread that is returning credit.
strm_i_sccnt	This is set to the number of credits being returned, or 0 on a TX teardown acknowledgement.

11.3.1.3.2.4.6 Tx Pause

The Host initiates a channel pause by setting the pause bit in the RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.3.2.4.7 Tx Teardown

The Host initiates a channel teardown by setting the tdown bit in the UDMA-P channel that is paired with the PDMA. The UDMA-P communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous UDMA-P data for the channel has been flushed. At this time, the teardown state will be reflected in the PSI-L RT Enable register of the PDMA. Note that a non-synchronized teardown can also be initiated by directly clearing the enable bit in the PSI-L RT Enable register of the PDMA.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel will be cleared in the PSI-L RT enable register, but the teardown bit will remain high. A teardown completion indication is sent back across the status pins of the PSI-L in the form of a credit response with sccnt=0. Upon completion, no further packet processing will occur until the Host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the UDMA-P transmission stops on a data boundary that is not compatible with the static TR configuration, the flush bit in the RT enable register can be set to guarantee that all data can be properly flushed from the internal pipe.

11.3.1.3.2.4.8 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L Enable register. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.3.2.4.9 Tx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as in the following table.

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Flush	0x403	30	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
Pause	0x403	29	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.
Data	0x403	28	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
XData	0x403	27	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.

11.3.1.3.2.5 Receive Operation

11.3.1.3.2.5.1 Source (Rx) Channel Allocation

A total of 7 source channels are provided within the DMA for concurrent transfers from the various attached peripherals into the Rx per channel buffers and on to the PSI-L Rx Interface. Each Rx channel requires a single PSI-L thread. The Rx channels are allocated as shown in Table 11-83.

Table 11-83. Rx Channel Allocation

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
0	USART 0 Rx Ch 0	XY	edge	000002800000	000000000000	000000000000
1	USART 1 Rx Ch 0	XY	edge	000002810000	000000000000	000000000000
2	USART 2 Rx Ch 0	XY	edge	000002820000	000000000000	000000000000
3	USART 3 Rx Ch 0	XY	edge	000002830000	000000000000	000000000000
4	USART 4 Rx Ch 0	XY	edge	000002840000	000000000000	000000000000
5	USART 5 Rx Ch 0	XY	edge	000002850000	000000000000	000000000000

Table 11-83. Rx Channel Allocation (continued)

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
6	USART 6 Rx Ch 0	XY	edge	000002860000	000000000000	000000000000

11.3.1.3.2.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will need to first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.3.2.5.2.1 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host will pair each source PDMA channel with (typically) a corresponding destination channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA will send all their data to the source channel in the UDMA-P and the destination channel in the UDMA-P will never see any data other than data from the source channel in the PDMA.

11.3.1.3.2.5.2.2 Static Transfer Request Setup

After reset, all channels in the PDMA will be idle and waiting for work to be assigned to them. In order to initiate PDMA operation, the Host will send configuration transactions across PSI-L and will set up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.3.2.5.2.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.3.2.5.2.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information.
Acc32	0x400	30	Not used
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an 'EOP' indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8 byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

11.3.1.3.2.5.2.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each read which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.

Param	PSIL Addr	Field	Description
Z	0x401	23:0	FIFO count. This field specifies how many full DMA request operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.3.2.5.2.2.4 AASRC RxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this RX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each RX FIFO. The flags corresponding to all RX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.3.2.5.2.2.5 AASRC RxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. RX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all RX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	RX FIFO Index for slot 7
27:24	Entry6	6	RX FIFO Index for slot 6
23:20	Entry5	5	RX FIFO Index for slot 5
19:16	Entry4	4	RX FIFO Index for slot 4

Bits	Field	Reset	Description
15:12	Entry3	3	RX FIFO Index for slot 3
11:8	Entry2	2	RX FIFO Index for slot 2
7:4	Entry1	1	RX FIFO Index for slot 1
3:0	Entry0	0	RX FIFO Index for slot 0

11.3.1.3.2.5.2.2.6 AASRC RxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. RX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all RX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	RX FIFO Index for slot 15
27:24	Entry14	14	RX FIFO Index for slot 14
23:20	Entry13	13	RX FIFO Index for slot 13
19:16	Entry12	12	RX FIFO Index for slot 12
15:12	Entry11	11	RX FIFO Index for slot 11
11:8	Entry10	10	RX FIFO Index for slot 10
7:4	Entry9	9	RX FIFO Index for slot 9
3:0	Entry8	8	RX FIFO Index for slot 8

11.3.1.3.2.5.2.3 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.3.2.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.3.2.5.3.1 X-Y FIFO Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA will sequentially issue a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs will be a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the Rx channelized FIFO and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.3.2.5.3.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts will be sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA will 'gap' the byte enables on writes as needed

11.3.1.3.2.5.3.2 MCAN Mode Channel

The PDMA channel will remain idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA will start copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN will skip the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example the following two filter entries will setup a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0:

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.3.2.5.3.2.1 MCAN Burst Mode

Since MCAN buffers are stored in linear memory, the burst mode for MCAN is a simple linear burst across the transfer window. The max burst size is set to the 72 byte size of the MCAN buffer. This will allow a full MCAN packet to be read out as a single burst.

11.3.1.3.2.5.3.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel will remain idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it will start reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed the channel will return to an idle state and wait until it is triggered again. The read transfers that are performed will be accomplished as quickly as possible given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.3.2.5.4 Receive PSI-L Interface Transactions

When an entire word has been packed into the Rx Per Channel Buffer for a given channel, a one word data phase transfer will be initiated for that channel/thread on the Rx PSI-L interface and the data will be popped from the Rx Per Channel FIFO. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_o_req	This signal is asserted when the PDMA determines that there is at least 1 word of data in it's TP-CC output FIFO
strm_o_sthread_id	Set equal to the TP-CC DMA channel number which is on the interface for this cycle
strm_o_dthread_id	Set equal to the target thread ID value given in the PSI-L pairing configuration registers for this DMA channel
strm_o_data_type	Will be set to the proper PSI-L data type. The PDMA can send config response, PSI info word 0, and PSI data word.
strm_o_wnum	Set equal to the packing lane for the current word within a contiguous transfer. This value will start at 0 for each new TR and will increment for each subsequent data phase in the TR.
strm_o_lastw	This signal will be asserted coincident with eop.
strm_o_xcnt	The xcnt will be equal to the data path width in bytes.
strm_o_worden	The worden will be modulated to indicate which 32-bit words are valid within each control type data phase.
strm_o_data	The data will be packed/left justified to comply to the big endian data ordering as required in the PSI-L I/F specification.
strm_o_sop	This signal is asserted for 1 data phase at the beginning of each new TR or data transfer packet.
strm_o_eop	This signal is asserted for 1 data phase at the end of each TR or data transfer packet.
strm_o_sol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the start of a new set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_eol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the end of a set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_priv	Set to zero.
strm_o_privid	Set to zero.
strm_o_virtid	Set to zero.
strm_o_secure	Set to zero.
strm_o_interest	Set to zero.

Pin	Output Value / Source From PDMA
strm_o_sready	Always asserted as the PDMA is always able to accept credit returns.

11.3.1.3.2.5.5 Rx Pause

The Host initiates a channel pause by setting the pause bit in RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.3.2.5.6 Rx Teardown

The Host initiates a RX channel teardown by setting the tdown bit in the RT enable register for the target RX channel. The PDMA communicates the teardown state to the UDMA-P through the PSI-L data channel, to ensure that the teardown is not seen by the UDMA-P until all the previous PDMA data for the channel has been flushed.

The PDMA will not stop reading peripheral data until it reaches a FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. It will always attempt to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA will then clear the enable bit in the pairing register, however the teardown bit will remain set. No further packet processing will occur until the Host re-configures the channel. The teardown process will propagate to the UDMA-P and its final status can be checked there.

11.3.1.3.2.5.7 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L enable register. This will cause a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.3.2.5.8 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as follows.

Name	PSIL Addr	Field	Description
Z*	0x402	31:16	This field holds the lower 12 bits of the current Z count for legacy pursposes. See register 0x40F below for the full width version of Z.
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Tdown	0x403	30	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
Pause	0x403	29	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is un-paused or disabled.
Space	0x403	28	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
XSpace	0x403	27	When set, there is a enough internal FIFO space available to start servicing a peripheral DMA event.
Buffer	0x403	26	This is the current RX buffer (0/1) for the current MCAN receive operation.

Name	PSIL Addr	Field	Description
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.
Z	0x40F	31:0	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

11.3.1.4 Functional Description - McASP

11.3.1.4.1 Compliance to Standards

The PDMA complies fully to all standards listed in the previous section.

11.3.1.4.2 Functional Operation

The Peripheral DMA is a simple, low cost implementation of the CPPI 5.0 Unified Transfer Controller. The PDMA module is required to be located close to one or more peripherals (both peripherals and PDMA direct connected to the SCR) which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only the static Transfer Request subset of UTC features which are useful for peripheral type transactions. Multiple source and destination channels are provided within the PDMA, which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs time division multiplexing between channels to share the underlying DMA hardware. A scheduler is provided to control the ordering and rate at which this multiplexing occurs. A block diagram of the PDMA Controller is shown below:

11.3.1.4.2.1 Submodule Descriptions

11.3.1.4.2.1.1 Scheduler

The Scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low level read or write operation.

11.3.1.4.2.1.2 Tx Per Channel Buffers

The Tx Per Channel Buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx Per Channel Buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.4.2.1.3 Tx DMA Unit

The Tx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming dma event and then writes data from the Tx Per Channel Data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.4.2.1.4 Rx Per Channel Buffers

Rx Per Channel Buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte oriented on write so that the data from the Rx DMA units which may not be full words can be packed properly. The buffers are word oriented on read in accordance with the transport mechanism outlined in the PSI-L Interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface. The Rx Per Channel Buffer block outputs queue fullness information to the scheduler block, which it then uses to determine when it should initiate

DMA opportunities to backfill the buffers. The Rx Per Channel Buffer initiates transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block simultaneously monitors the status of all of the threads and performs a round robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer is included in the arbitration.

11.3.1.4.2.1.5 Rx DMA Unit

The Rx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx Per Channel Data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.4.2.2 General Functionality (Applicable to All Functions/Modes)

11.3.1.4.2.2.1 Operational States

At any given time, the PDMA can be in one of three different states, as shown in Table 11-84.

Table 11-84. PDMA Operational States

Operational State	Description
Init	This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the init state, the DMA will de-assert all ready signals on all applicable target interfaces and will de-assert all request signals on all applicable controller interfaces. The PDMA will automatically transition out of the init state into the idle state when all of the RAM initialization has been completed.
Idle	Once the PDMA leaves the Init state, it enters the Idle state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The Idle state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. For clock stop purposes, the module will only report idle if all DMA channels are disabled using the enable bit in PSIL register 2 for each channel.
Active	The PDMA enters the active state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent) the PDMA transitions to the Idle state.

11.3.1.4.2.2.2 Clock Stop

The clock stop interface is used to instruct the PDMA to stop issuing commands on its external interfaces. Note that the PDMA will report a clock stop idle if all its DMA channels have been previously disabled by software using the enable bit in PSIL register 2 for each channel.

11.3.1.4.2.2.3 Emulation Control

The emulation control input (susp_emususp) and the per channel emulation control 'free' bit allow DMA operation to be suspended on a per channel basis. When the emulation suspend state is entered, the DMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. Emulation control is implemented for compatibility with other peripherals. Each source and destination channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is controlled via the 'free' bit in the channel Enable Register. Note the real time emulation suspend request signal is not supported.

11.3.1.4.2.3 Events and Flow Control

The following sections describe the simplified mechanism provided on the Peripheral DMA for triggering.

11.3.1.4.2.3.1 Channel Triggering

Channels must be triggered for them to perform work. A local event input bus is provided on the peripheral DMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, and so forth). The event inputs for XY mode are triggered either via pulse, or by a clock synchronous rising edge. The counting mode is a design time configuration parameter. In MCAN mode, the inputs are expected to be single cycle pulses, synchronous with the PDMA clock.

- Event signals that are used in pulse mode must be sourced by the same clock as the PDMA.
- Event signals that are used in edge mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the PDMA clock, and they must remain high for at least 1 'slow' clock cycle.

The PDMA provides a 2-bit counter per event input to accommodate startup latency in the channel. (In AASRC mode, the signals are not counted, but latched whenever asserted.)

11.3.1.4.2.3.2 Completion Events

All transfers on PDMA are split TR in that they have a UDMA-P half and a (static) PDMA half. Completion events are designed to be triggered from the UDMA-P half of the split TR.

11.3.1.4.2.3.3 Channel Types

Each channel in the Peripheral DMA is configured at design time to be either standard X-Y FIFO mode or MCAN channel. The channel type is configured at design time, and can not be changed by software.

11.3.1.4.2.3.3.1 X-Y FIFO Mode

Most peripherals which are serviced by the Peripheral DMA follow the pattern of transferring X bytes from a fixed, non-changing address in a loop Y times for each triggering event that is received. The X parameter is typically 1-16 bytes and the Y parameter can be any integer up to 2048. If a peripheral can be serviced by this basic functionality then it is recommended to use this mode for the peripheral.

11.3.1.4.2.3.3.2 MCAN Mode

The MCANSS subsystem was found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the DMA starts out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, MCAN packet fragmentation requirement to place an 8-byte header on each 64-byte chunk that is transmitted and to remove the header from each 64-byte chunk (other than the first block) that is received.

11.3.1.4.2.3.3.3 AASRC Mode

The AASRC mode of the PDMA is similar to the X-Y mode in that X specifies the sample width, any Y specifies the number of FIFO samples to transfer per DMA request, but in addition to this, a programmable FIFO list is supplied that allows a single PDMA channel to transfer data to multiple FIFOs. The FIFO list specifies which FIFOS to access, and in which order to access them. Both AASRC 'stream' and 'group' modes are supported in terms of DMA signalling and the FIFO memory map. When in AASRC mode, the entire PDMA operates exclusively in this mode. AASRC channels to not share the same PDMA as do XY and MCAN channels.

The following additional details apply to the PDMA in AASRC mode.

Main Features:

- Up to 16 independent RX channels and 16 TX channels
  - Each channel represents a different data stream to either the UDMA-P-P or a McASP PDMA
- Each channel can be configured to read or write any of the AASRC FIFOs in any order
- Packing support for 1, 2, 3, and 4 byte samples
  - Can directly talk to a McASP using any McASP data format
  - Packing sample size is fixed for a given channel
- Supports both Group and Stream AASRC signaling and FIFO memory maps
  - There is a single stream/group mode setting for each PDMA channel

Additional details:

- Each channel has a 'mask' of which DMA requests must fire to activate the channel
  - In stream mode, the mask specifies the all the FIFO DMA requests that must fire
  - In group mode, the mask specifies the one group DMA request that must fire
- Each channel specifies an ordered list of how FIFOs should be accessed

  - All channels use a common list, specifying a range of entry indices within that list. This lets each channel use a varying number of list elements.
  - The order list can be processed multiple times per DMA request. The number of samples to be transferred per request must match the configured threshold for the DMA request in the AASRC.
- All FIFOs are specified by index only
  - In the TX ordering table, the indices are assumed to be TX FIFOs
  - In the RX ordering table, the indices are assumed to be RX FIFOs
  - If a DMA channel is in 'Group Mode', the PDMA assumes the indices referenced by that channel represent Group Mode FIFOs; otherwise, it assumes Stream Mode FIFOs.
- The PDMA has configured base addressed and inter-FIFO spans such that is can always convert from a FIFO index to the proper Stream or Group mode FIFO address

11.3.1.4.2.4 Transmit Operation

11.3.1.4.2.4.1 Destination (Tx) Channel Allocation

A total of 2 destination channels are provided within the DMA for concurrent transfers from Tx per channel buffers to the various attached peripherals. Each Tx channel requires a single PSI-L thread. The Tx channels are allocated as follows:

Tx DMA Channel	Function	Channel Type	Trigger Mode	Data FIFO Address	Strobe MMR Address	Control FIFO Address
8000	McASP 3 Tx Ch 0	XY	edge	000002B38000	000000000000	000000000000
8001	McASP 4 Tx Ch 0	XY	edge	000002B48000	000000000000	000000000000

11.3.1.4.2.4.2 Destination (Tx) Channel Out of Band Signals

The following table shows how PSIL signals are handled for destination channels.

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sop	ignored	ignored
eop	ignored	closes current MCAN packet
sol	ignored	ignored
eol	ignored	ignored
drop	ignored	ignored
pkt_error	ignored	ignored
tdown	reflect in status, teardown when data marker reached	reflect in status, teardown when data marker reached

11.3.1.4.2.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA is idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host must first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.4.2.4.3.1 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host pairs each destination PDMA channel with (typically) a corresponding source channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread, and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the UDMA-P send all their data to the destination channel in the PDMA, and the destination channel in the PDMA never sees any data other than data from the source channel in the UDMA-P.

11.3.1.4.2.4.3.2 Static Transfer Request Setup

After reset, all channels in the PDMA are idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host sends configuration transactions across PSI-L and sets up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies somewhat.

11.3.1.4.2.4.3.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
Z	0x401	23:0	Not used

11.3.1.4.2.4.3.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8 byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
Z	0x401	23:0	Not used

11.3.1.4.2.4.3.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED

Param	PSIL Addr	Field	Description
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer to each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
Z	0x401	23:0	Not used

11.3.1.4.2.4.3.3 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled to accept data. Threads are enabled or disabled by setting or clearing the enable bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.4.2.4.4 Data Transfer

Packet transmission is accomplished within the PDMA by unpacking and moving data from the Tx Per Channel FIFOs which were filled via the Transmit PSI-L Interface to specified memory mapped address ranges via the VBUSP controller interfaces. On the Tx side of the PDMA, these transfers are always writes. Each write transfer which is performed by the Tx DMA Unit is to a destination address that is hardcoded in the channel at design time and of a size as specified in the static Transfer Request.

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during transmit is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.4.2.4.4.1 X-Y FIFO Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA sequentially issues a total of 'Y' parameter writes of 'X' parameter bytes to the data_address specified in the tchan_info parameter for the channel. Each write that the DMA performs is a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The write transfers that are performed are accomplished as quickly as possible given availability of data in the Tx channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.4.2.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address increments throughout the burst
- Bursts are sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA 'gaps' the byte enables on writes as needed

11.3.1.4.2.4.4.2 MCAN Mode Channel

The PDMA channel remains idle until data is received from the UDMA-P over the PSIL interface. At this time, the PDMA immediately starts copying packet bytes into the MCAN TX buffer corresponding the PDMA/MCAN channel. The number of bytes copied is smaller of the remaining bytes in the packet, or the value of the 'Y' parameter. Once a TX buffer has been filled, the PDMA transfers ownership of the buffer to MCAN by performing an MCAN register write. The PDMA then waits to regain ownership of the TX buffer by waiting for the corresponding MCAN TX event. At this time, the PDMA continues with refilling the TX buffer for the next packet fragment. On subsequent fills (until the end of packet is reached), the PDMA skips over the 8 byte MCAN header, leaving the original contents from the initial fragment copy in place.

11.3.1.4.2.4.4.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's TxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel remains idle until a pulse is detected on ALL associated input DMA request event pins required by the TxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it starts reading FIFO index values from the TxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs written for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width written to the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The write transfers that are performed are accomplished as quickly as possible, given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.4.2.4.5 Transmit PSI-L Interface Transactions

The PDMA accepts data across the Tx PSI-L Interface in accordance with the physical handshaking protocol, as defined in the PSI-L Interface specification. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_i_link	This signal is asserted high to indicate the PSI-L link is valid.
strm_i_ready	This signal is asserted high anytime there is space in the PSI-L ingress fifo.
strm_i_sreq	This signal is asserted high anytime there is credit return data waiting in the PSI-L status fifo.
strm_i_sthreadid	This is set to the local destination thread that is returning credit.
strm_i_sccnt	This is set to the number of credits being returned, or 0 on a TX teardown acknowledgement.

11.3.1.4.2.4.6 Tx Pause

The Host initiates a channel pause by setting the pause bit in the RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.4.2.4.7 Tx Teardown

The Host initiates a channel teardown by setting the tdown bit in the UDMA-P channel paired with the PDMA. The UDMA-P communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous UDMA-P data for the channel has been flushed. At this time, the teardown state is reflected in the PSI-L RT Enable register of the PDMA. Note that a non-synchronized teardown can also be initiated by directly clearing the enable bit in the PSI-L RT Enable register of the PDMA.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel is cleared in the PSI-L RT enable register, but the teardown bit remains high. A teardown completion indication is sent back across the status pins of the PSI-L in the form of a credit response with sccnt=0. Upon completion, no further packet processing occurs until the Host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the UDMA-P transmission stops on a data boundary that is not compatible with the static TR configuration, the flush bit in the RT enable register can be set to ensure that all data can be properly flushed from the internal pipe.

11.3.1.4.2.4.8 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L Enable register. This causes a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.4.2.4.9 Tx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as in Table 11-85.

Table 11-85. Tx Debug/State Register

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Flush	0x403	30	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
Pause	0x403	29	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.
Data	0x403	28	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
XData	0x403	27	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.

11.3.1.4.2.5 Receive Operation

11.3.1.4.2.5.1 Source (Rx) Channel Allocation

A total of 2 source channels are provided within the DMA for concurrent transfers from the various attached peripherals into the Rx per channel buffers and on to the PSI-L Rx Interface. Each Rx channel requires a single PSI-L thread. The Rx channels are allocated as follows.

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
0	McASP 3 Rx Ch 0	XY	edge	000002B38000	000000000000	000000000000

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
1	McASP 4 Rx Ch 0	XY	edge	000002B48000	000000000000	000000000000

11.3.1.4.2.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host must first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.4.2.5.2.1 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host pairs each source PDMA channel with (typically) a corresponding destination channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread, and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA send all their data to the source channel in the UDMA-P, and the destination channel in the UDMA-P never sees any data other than data from the source channel in the PDMA.

11.3.1.4.2.5.2.2 Static Transfer Request Setup

After reset, all channels in the PDMA are idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host sends configuration transactions across PSI-L and sets up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.4.2.5.2.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.4.2.5.2.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Not used

Param	PSIL Addr	Field	Description
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an 'EOP' indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8 byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

11.3.1.4.2.5.2.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each read which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full DMA request operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.4.2.5.2.3 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.4.2.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the

Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what happens for the different channel types.

11.3.1.4.2.5.3.1 X-Y FIFO Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA sequentially issues a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs is a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The read transfers that are performed are accomplished as quickly as possible given availability of data in the Rx channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.4.2.5.3.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. For example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts are sub-divided to fit into a 64-byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA 'gaps' the byte enables on writes as needed

11.3.1.4.2.5.3.2 MCAN Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA starts copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN skips the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example, the following two filter entries set up a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0.

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.4.2.5.3.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel remains idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it starts reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The read transfers that are performed are accomplished as quickly as possible given availability of data in the TX channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.4.2.5.4 Receive PSI-L Interface Transactions

When an entire word has been packed into the Rx Per Channel Buffer for a given channel, a one word data phase transfer is initiated for that channel/thread on the Rx PSI-L interface, and the data is popped from the Rx Per Channel FIFO. The value sources for the output pins on the PSI-L interface are described in Table 11-86.

Table 11-86. PSI-L Interface Output Pins

Pin	Output Value / Source From PDMA
strm_o_req	This signal is asserted when the PDMA determines that there is at least 1 word of data in it's TP-CC output FIFO
strm_o_sthread_id	Set equal to the TP-CC DMA channel number which is on the interface for this cycle
strm_o_dthread_id	Set equal to the target thread ID value given in the PSI-L pairing configuration registers for this DMA channel
strm_o_data_type	Will be set to the proper PSI-L data type. The PDMA can send config response, PSI info word 0, and PSI data word.
strm_o_wnum	Set equal to the packing lane for the current word within a contiguous transfer. This value will start at 0 for each new TR and will increment for each subsequent data phase in the TR.
strm_o_lastw	This signal will be asserted coincident with eop.
strm_o_xcnt	The xcnt will be equal to the data path width in bytes.
strm_o_worden	The worden will be modulated to indicate which 32-bit words are valid within each control type data phase.
strm_o_data	The data will be packed/left justified to comply to the big endian data ordering as required in the PSI-L I/F specification.
strm_o_sop	This signal is asserted for 1 data phase at the beginning of each new TR or data transfer packet.

Table 11-86. PSI-L Interface Output Pins (continued)

Pin	Output Value / Source From PDMA
strm_o_eop	This signal is asserted for 1 data phase at the end of each TR or data transfer packet.
strm_o_sol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the start of a new set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_eol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the end of a set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_priv	Set to zero.
strm_o_privid	Set to zero.
strm_o_virtid	Set to zero.
strm_o_secure	Set to zero.
strm_o_interest	Set to zero.
strm_o_sready	Always asserted as the PDMA is always able to accept credit returns.

11.3.1.4.2.5.5 Rx Pause

The Host initiates a channel pause by setting the pause bit in RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.4.2.5.6 Rx Teardown

The Host initiates a RX channel teardown by setting the tdown bit in the RT enable register for the target RX channel. The PDMA communicates the teardown state to the UDMA-P through the PSI-L data channel, to ensure that the teardown is not seen by the UDMA-P until all the previous PDMA data for the channel has been flushed.

The PDMA does not stop reading peripheral data until it reaches a FIFO boundary, as configured through the 'X' and 'Y' parameters in the static TR. It always attempts to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA then clears the enable bit in the pairing register; however, the teardown bit remains set. No further packet processing occurs until the Host re-configures the channel. The teardown process propagates to the UDMA-P and its final status can be checked there.

11.3.1.4.2.5.7 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L enable register. This causes a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.4.2.5.8 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as in Table 11-87.

Table 11-87. Rx Debug/State Register

Name	PSIL Addr	Field	Description
Z*	0x402	31:16	This field holds the lower 12 bits of the current Z count for legacy pursposes. See register 0x40F below for the full width version of Z.
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.

Table 11-87. Rx Debug/State Register (continued)

Name	PSIL Addr	Field	Description
Tdown	0x403	30	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
Pause	0x403	29	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is un-paused or disabled.
Space	0x403	28	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
XSpace	0x403	27	When set, there is a enough internal FIFO space available to start servicing a peripheral DMA event.
Buffer	0x403	26	This is the current RX buffer (0/1) for the current MCAN receive operation.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.
Z	0x40F	31:0	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

11.3.1.5 Functional Description - ADC

11.3.1.5.1 Compliance to Standards

The PDMA complies fully to all standards listed in the previous section.

11.3.1.5.2 Functional Operation

The Peripheral DMA is a simple, low cost implementation of the CPPI 5.0 Unified Transfer Controller. The PDMA module is required to be located close to one or more peripherals (both peripherals and PDMA direct connected to the SCR) which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only the static Transfer Request subset of UTC features which are useful for peripheral type transactions. Multiple source and destination channels are provided within the PDMA, which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs time division multiplexing between channels to share the underlying DMA hardware. A scheduler is provided to control the ordering and rate at which this multiplexing occurs. A block diagram of the PDMA Controller is shown below:

11.3.1.5.2.1 Submodule Descriptions

11.3.1.5.2.1.1 Scheduler

The Scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low level read or write operation.

11.3.1.5.2.1.2 Tx Per Channel Buffers

The Tx Per Channel Buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx Per Channel Buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.5.2.1.3 Tx DMA Unit

The Tx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming dma event and then writes data from the Tx Per Channel Data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.5.2.1.4 Rx Per Channel Buffers

Rx Per Channel Buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte oriented on write so that the data from the Rx DMA units which may not be full words can be packed properly. The buffers are word oriented on read in accordance with the transport mechanism outlined in the PSI-L Interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface. The Rx Per Channel Buffer block outputs queue fullness information to the scheduler block, which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Rx Per Channel Buffer initiates transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block simultaneously monitors the status of all of the threads and performs a round robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer is included in the arbitration.

11.3.1.5.2.1.5 Rx DMA Unit

The Rx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx Per Channel Data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.5.2.2 General Functionality (Applicable to All Functions/Modes)

11.3.1.5.2.2.1 Operational States

At any given time, the PDMA can be in one of three different states, as shown in Table 11-88.

Table 11-88. PDMA Operational States

Operational State	Description
Init	This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the init state, the DMA will de-assert all ready signals on all applicable target interfaces and will de-assert all request signals on all applicable controller interfaces. The PDMA will automatically transition out of the init state into the idle state when all of the RAM initialization has been completed.
Idle	Once the PDMA leaves the Init state, it enters the Idle state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The Idle state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. For clock stop purposes, the module will only report idle if all DMA channels are disabled using the enable bit in PSIL register 2 for each channel.
Active	The PDMA enters the active state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent) the PDMA transitions to the Idle state.

11.3.1.5.2.2.2 Clock Stop

The clock stop interface is used to instruct the PDMA to stop issuing commands on its external interfaces. Note that the PDMA will report a clock stop idle if all its DMA channels have been previously disabled by software using the enable bit in PSIL register 2 for each channel.

11.3.1.5.2.2.3 Emulation Control

The emulation control input (susp_emususp) and the per channel emulation control 'free' bit allow DMA operation to be suspended on a per channel basis. When the emulation suspend state is entered, the DMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. Emulation control is implemented for compatibility with other peripherals. Each source and destination channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is controlled via the 'free' bit in the channel Enable Register. Note the real time emulation suspend request signal is not supported.

11.3.1.5.2.3 Events and Flow Control

The following sections describe the simplified mechanism provided on the Peripheral DMA for triggering.

11.3.1.5.2.3.1 Channel Triggering

Channels must be triggered for them to perform work. A local event input bus is provided on the peripheral DMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, and so forth). The event inputs for XY mode are triggered either via pulse, or by a clock synchronous rising edge. The counting mode is a design time configuration parameter. In MCAN mode, the inputs are expected to be single cycle pulses, synchronous with the PDMA clock.

- Event signals that are used in pulse mode must be sourced by the same clock as the PDMA.
- Event signals that are used in edge mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the PDMA clock, and they must remain high for at least 1 'slow' clock cycle.

The PDMA provides a 2-bit counter per event input to accommodate startup latency in the channel. (In AASRC mode, the signals are not counted, but latched whenever asserted.)

11.3.1.5.2.3.2 Completion Events

All transfers on PDMA are split TR in that they have a UDMA-P half and a (static) PDMA half. Completion events are designed to be triggered from the UDMA-P half of the split TR.

11.3.1.5.2.3.3 Channel Types

Each channel in the Peripheral DMA is configured at design time to be either standard X-Y FIFO mode or MCAN channel. The channel type is configured at design time, and can not be changed by software.

11.3.1.5.2.3.3.1 X-Y FIFO Mode

Most peripherals which are serviced by the Peripheral DMA follow the pattern of transferring X bytes from a fixed, non-changing address in a loop Y times for each triggering event that is received. The X parameter is typically 1-16 bytes and the Y parameter can be any integer up to 2048. If a peripheral can be serviced by this basic functionality then it is recommended to use this mode for the peripheral.

11.3.1.5.2.3.3.2 MCAN Mode

The MCANSS subsystem was found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the DMA starts out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, MCAN packet fragmentation requirement to place an 8-byte header on each 64-byte chunk that is transmitted and to remove the header from each 64-byte chunk (other than the first block) that is received.

11.3.1.5.2.3.3.3 AASRC Mode

The AASRC mode of the PDMA is similar to the X-Y mode in that X specifies the sample width, any Y specifies the number of FIFO samples to transfer per DMA request, but in addition to this, a programmable FIFO list is supplied that allows a single PDMA channel to transfer data to multiple FIFOs. The FIFO list specifies which FIFOS to access, and in which order to access them. Both AASRC 'stream' and 'group' modes are supported in terms of DMA signalling and the FIFO memory map. When in AASRC mode, the entire PDMA operates exclusively in this mode. AASRC channels to not share the same PDMA as do XY and MCAN channels.

The following additional details apply to the PDMA in AASRC mode.

Main Features:

- Up to 16 independent RX channels and 16 TX channels
  - Each channel represents a different data stream to either the UDMA-P-P or a McASP PDMA
- Each channel can be configured to read or write any of the AASRC FIFOs in any order
- Packing support for 1, 2, 3, and 4 byte samples
  - Can directly talk to a McASP using any McASP data format
  - Packing sample size is fixed for a given channel
- Supports both Group and Stream AASRC signaling and FIFO memory maps
  - There is a single stream/group mode setting for each PDMA channel

Additional details:

- Each channel has a 'mask' of which DMA requests must fire to activate the channel
  - In stream mode, the mask specifies the all the FIFO DMA requests that must fire
  - In group mode, the mask specifies the one group DMA request that must fire
- Each channel specifies an ordered list of how FIFOs should be accessed
  - All channels use a common list, specifying a range of entry indices within that list. This lets each channel use a varying number of list elements.
  - The order list can be processed multiple times per DMA request. The number of samples to be transferred per request must match the configured threshold for the DMA request in the AASRC.
- All FIFOs are specified by index only
  - In the TX ordering table, the indices are assumed to be TX FIFOs
  - In the RX ordering table, the indices are assumed to be RX FIFOs
  - If a DMA channel is in 'Group Mode', the PDMA assumes the indices referenced by that channel represent Group Mode FIFOs; otherwise, it assumes Stream Mode FIFOs.
- The PDMA has configured base addressed and inter-FIFO spans such that is can always convert from a FIFO index to the proper Stream or Group mode FIFO address

11.3.1.5.2.4 Transmit Operation

11.3.1.5.2.4.1 Destination (Tx) Channel Allocation

A total of 0 destination channels are provided within the DMA for concurrent transfers from Tx per channel buffers to the various attached peripherals. Each Tx channel requires a single PSI-L thread. The Tx channels are allocated as follows:

11.3.1.5.2.4.2 Destination (Tx) Channel Out of Band Signals

The following table shows how PSIL signals are handled for destination channels.

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sop	ignored	ignored
eop	ignored	closes current MCAN packet
sol	ignored	ignored
eol	ignored	ignored
drop	ignored	ignored
pkt_error	ignored	ignored
tdown	reflect in status, teardown when data marker reached	reflect in status, teardown when data marker reached

11.3.1.5.2.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA is idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host must first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.5.2.4.3.1 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host pairs each destination PDMA channel with (typically) a corresponding source channel in the UDMA-P. The PDMA thread is configured to point to the

UDMA-P thread, and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the UDMA-P send all their data to the destination channel in the PDMA, and the destination channel in the PDMA never sees any data other than data from the source channel in the UDMA-P.

11.3.1.5.2.4.3.2 Static Transfer Request Setup

After reset, all channels in the PDMA are idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host sends configuration transactions across PSI-L and sets up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies somewhat.

11.3.1.5.2.4.3.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
Z	0x401	23:0	Not used

11.3.1.5.2.4.3.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8 byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
Z	0x401	23:0	Not used

11.3.1.5.2.4.3.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.

Param	PSIL Addr	Field	Description
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer to each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
Z	0x401	23:0	Not used

11.3.1.5.2.4.3.2.4 AASRC TxFifoConfig (PSIL Address 0x405)

This register describes the FIFO list to be processed for this TX channel.

Bits	Field	Reset	Description
31	GroupMode	0x0	When set, the channel is in 'Group Mode'. It will look for Group Mode DMA requests, and access the Group Mode FIFOs. When clear, the channel is 'Stream Mode'. It will look for Stream FIFO DMA requests, and access the Stream Mode FIFOs.
30	DmaReqReset	0x0	When set, resets any latched DMA request using the DmaReqMask. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
23:20	LastSlot	0x0	This is the index (0-15) of the last slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19:16	FirstSlot	0x0	This is the index (0-15) of the first slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
15:0	DmaReqMask	0x0	This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate. In Steam Mode, these 16 flags correspond to the 16 DMA requests for each TX FIFO. The flags corresponding to all TX FIFOs involved with the channel should be set to 1. In Group Mode, these flags indicate which Group Mode DMA requests must fire. In this case, only bits 3:0 are relevant and only one bit should be set to 1 as a DMA channel only services a single group.

11.3.1.5.2.4.3.2.5 AASRC TxOrderTable0 (PSIL Address 0x406)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry7	7	TX FIFO Index for slot 7
27:24	Entry6	6	TX FIFO Index for slot 6
23:20	Entry5	5	TX FIFO Index for slot 5
19:16	Entry4	4	TX FIFO Index for slot 4

Bits	Field	Reset	Description
15:12	Entry3	3	TX FIFO Index for slot 3
11:8	Entry2	2	TX FIFO Index for slot 2
7:4	Entry1	1	TX FIFO Index for slot 1
3:0	Entry0	0	TX FIFO Index for slot 0

11.3.1.5.2.4.3.2.6 AASRC TxOrderTable1 (PSIL Address 0x407)

This table is filled with FIFO index values. TX channels reference a starting and ending 'slot' in this table for each transfer. The actual FIFO accessed by the DMA for each slot is determined by the FIFO index stored in this table. Note: This is a single register that is shared by all TX threads.

Bits	Field	Reset	Description
31:28	Entry15	15	TX FIFO Index for slot 15
27:24	Entry14	14	TX FIFO Index for slot 14
23:20	Entry13	13	TX FIFO Index for slot 13
19:16	Entry12	12	TX FIFO Index for slot 12
15:12	Entry11	11	TX FIFO Index for slot 11
11:8	Entry10	10	TX FIFO Index for slot 10
7:4	Entry9	9	TX FIFO Index for slot 9
3:0	Entry8	8	TX FIFO Index for slot 8

11.3.1.5.2.4.3.3 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled to accept data. Threads are enabled or disabled by setting or clearing the enable bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.5.2.4.4 Data Transfer

Packet transmission is accomplished within the PDMA by unpacking and moving data from the Tx Per Channel FIFOs which were filled via the Transmit PSI-L Interface to specified memory mapped address ranges via the VBUSP controller interfaces. On the Tx side of the PDMA, these transfers are always writes. Each write transfer which is performed by the Tx DMA Unit is to a destination address that is hardcoded in the channel at design time and of a size as specified in the static Transfer Request.

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during transmit is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.5.2.4.4.1 X-Y FIFO Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA sequentially issues a total of 'Y' parameter writes of 'X' parameter bytes to the data_address specified in the tchan_info parameter for the channel. Each write that the DMA performs is a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The write transfers that are performed are accomplished as quickly as possible given availability of data in the Tx channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.5.2.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address increments throughout the burst
- Bursts are sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA 'gaps' the byte enables on writes as needed

11.3.1.5.2.4.4.2 MCAN Mode Channel

The PDMA channel remains idle until data is received from the UDMA-P over the PSIL interface. At this time, the PDMA immediately starts copying packet bytes into the MCAN TX buffer corresponding the PDMA/MCAN channel. The number of bytes copied is smaller of the remaining bytes in the packet, or the value of the 'Y' parameter. Once a TX buffer has been filled, the PDMA transfers ownership of the buffer to MCAN by performing an MCAN register write. The PDMA then waits to regain ownership of the TX buffer by waiting for the corresponding MCAN TX event. At this time, the PDMA continues with refilling the TX buffer for the next packet fragment. On subsequent fills (until the end of packet is reached), the PDMA skips over the 8 byte MCAN header, leaving the original contents from the initial fragment copy in place.

11.3.1.5.2.4.4.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's TxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel remains idle until a pulse is detected on ALL associated input DMA request event pins required by the TxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it starts reading FIFO index values from the TxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs written for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width written to the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The write transfers that are performed are accomplished as quickly as possible, given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.5.2.4.5 Transmit PSI-L Interface Transactions

The PDMA accepts data across the Tx PSI-L Interface in accordance with the physical handshaking protocol, as defined in the PSI-L Interface specification. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_i_link	This signal is asserted high to indicate the PSI-L link is valid.
strm_i_ready	This signal is asserted high anytime there is space in the PSI-L ingress fifo.
strm_i_sreq	This signal is asserted high anytime there is credit return data waiting in the PSI-L status fifo.
strm_i_sthreadid	This is set to the local destination thread that is returning credit.

Pin	Output Value / Source From PDMA
strm_i_sccnt	This is set to the number of credits being returned, or 0 on a TX teardown acknowledgement.

11.3.1.5.2.4.6 Tx Pause

The Host initiates a channel pause by setting the pause bit in the RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.5.2.4.7 Tx Teardown

The Host initiates a channel teardown by setting the tdown bit in the UDMA-P channel paired with the PDMA. The UDMA-P communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous UDMA-P data for the channel has been flushed. At this time, the teardown state is reflected in the PSI-L RT Enable register of the PDMA. Note that a non-synchronized teardown can also be initiated by directly clearing the enable bit in the PSI-L RT Enable register of the PDMA.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel is cleared in the PSI-L RT enable register, but the teardown bit remains high. A teardown completion indication is sent back across the status pins of the PSI-L in the form of a credit response with sccnt=0. Upon completion, no further packet processing occurs until the Host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the UDMA-P transmission stops on a data boundary that is not compatible with the static TR configuration, the flush bit in the RT enable register can be set to ensure that all data can be properly flushed from the internal pipe.

11.3.1.5.2.4.8 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L Enable register. This causes a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.5.2.4.9 Tx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as in Table 11-89.

Table 11-89. Tx Debug/State Register

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Flush	0x403	30	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
Pause	0x403	29	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.
Data	0x403	28	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
XData	0x403	27	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.

11.3.1.5.2.5 Receive Operation

11.3.1.5.2.5.1 Source (Rx) Channel Allocation

A total of 2 source channels are provided within the DMA for concurrent transfers from the various attached peripherals into the Rx per channel buffers and on to the PSI-L Rx Interface. Each Rx channel requires a single PSI-L thread. The Rx channels are allocated as follows.

Rx DMA Channel	Function	Channel Type	Trigger Type	Data FIFO Address	Strobe MMR Address	Control FIFO Address
0	ADC0 Rx Ch 0	XY	edge	000020608100	000000000000	000000000000
1	ADC1 Rx Ch 0	XY	edge	000020608200	000000000000	000000000000

11.3.1.5.2.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host must first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.5.2.5.2.1 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host pairs each source PDMA channel with (typically) a corresponding destination channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread, and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA send all their data to the source channel in the UDMA-P, and the destination channel in the UDMA-P never sees any data other than data from the source channel in the PDMA.

11.3.1.5.2.5.2.2 Static Transfer Request Setup

After reset, all channels in the PDMA are idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host sends configuration transactions across PSI-L and sets up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.5.2.5.2.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.5.2.5.2.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an 'EOP' indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8 byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

11.3.1.5.2.5.2.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each read which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full DMA request operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.5.2.5.2.3 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.5.2.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what happens for the different channel types.

11.3.1.5.2.5.3.1 X-Y FIFO Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA sequentially issues a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs is a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The read transfers that are performed are accomplished as quickly as possible given availability of data in the Rx channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.5.2.5.3.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. For example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts are sub-divided to fit into a 64-byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA 'gaps' the byte enables on writes as needed

11.3.1.5.2.5.3.2 MCAN Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA starts copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN skips the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example, the following two filter entries set up a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0.

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.5.2.5.3.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel remains idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it starts reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The read transfers that are performed are accomplished as quickly as possible given availability of data in the TX channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.5.2.5.4 Receive PSI-L Interface Transactions

When an entire word has been packed into the Rx Per Channel Buffer for a given channel, a one word data phase transfer is initiated for that channel/thread on the Rx PSI-L interface, and the data is popped from the Rx Per Channel FIFO. The value sources for the output pins on the PSI-L interface are described in Table 11-90.

Table 11-90. PSI-L Interface Output Pins

Pin	Output Value / Source From PDMA
strm_o_req	This signal is asserted when the PDMA determines that there is at least 1 word of data in it's TP-CC output FIFO
strm_o_sthread_id	Set equal to the TP-CC DMA channel number which is on the interface for this cycle
strm_o_dthread_id	Set equal to the target thread ID value given in the PSI-L pairing configuration registers for this DMA channel

Table 11-90. PSI-L Interface Output Pins (continued)

Pin	Output Value / Source From PDMA
strm_o_data_type	Will be set to the proper PSI-L data type. The PDMA can send config response, PSI info word 0, and PSI data word.
strm_o_wnum	Set equal to the packing lane for the current word within a contiguous transfer. This value will start at 0 for each new TR and will increment for each subsequent data phase in the TR.
strm_o_lastw	This signal will be asserted coincident with eop.
strm_o_xcnt	The xcnt will be equal to the data path width in bytes.
strm_o_worden	The worden will be modulated to indicate which 32-bit words are valid within each control type data phase.
strm_o_data	The data will be packed/left justified to comply to the big endian data ordering as required in the PSI-L I/F specification.
strm_o_sop	This signal is asserted for 1 data phase at the beginning of each new TR or data transfer packet.
strm_o_eop	This signal is asserted for 1 data phase at the end of each TR or data transfer packet.
strm_o_sol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the start of a new set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_eol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the end of a set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_priv	Set to zero.
strm_o_privid	Set to zero.
strm_o_virtid	Set to zero.
strm_o_secure	Set to zero.
strm_o_interest	Set to zero.
strm_o_sready	Always asserted as the PDMA is always able to accept credit returns.

11.3.1.5.2.5.5 Rx Pause

The Host initiates a channel pause by setting the pause bit in RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.5.2.5.6 Rx Teardown

The Host initiates a RX channel teardown by setting the tdown bit in the RT enable register for the target RX channel. The PDMA communicates the teardown state to the UDMA-P through the PSI-L data channel, to ensure that the teardown is not seen by the UDMA-P until all the previous PDMA data for the channel has been flushed.

The PDMA does not stop reading peripheral data until it reaches a FIFO boundary, as configured through the 'X' and 'Y' parameters in the static TR. It always attempts to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA then clears the enable bit in the pairing register; however, the teardown bit remains set. No further packet processing occurs until the Host re-configures the channel. The teardown process propagates to the UDMA-P and its final status can be checked there.

11.3.1.5.2.5.7 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L enable register. This causes a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.5.2.5.8 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as in Table 11-91.

Table 11-91. Rx Debug/State Register

Name	PSIL Addr	Field	Description
Z*	0x402	31:16	This field holds the lower 12 bits of the current Z count for legacy pursposes. See register 0x40F below for the full width version of Z.
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Tdown	0x403	30	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
Pause	0x403	29	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is un-paused or disabled.
Space	0x403	28	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
XSpace	0x403	27	When set, there is a enough internal FIFO space available to start servicing a peripheral DMA event.
Buffer	0x403	26	This is the current RX buffer (0/1) for the current MCAN receive operation.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.
Z	0x40F	31:0	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

11.3.1.6 Functional Description - ASRC

11.3.1.6.1 Compliance to Standards

The PDMA complies fully to all standards listed in the previous section.

11.3.1.6.2 Functional Operation

The Peripheral DMA is a simple, low cost implementation of the CPPI 5.0 Unified Transfer Controller. The PDMA module is required to be located close to one or more peripherals (both peripherals and PDMA direct connected to the SCR) which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only the static Transfer Request subset of UTC features which are useful for peripheral type transactions. Multiple source and destination channels are provided within the PDMA, which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs time division multiplexing between channels to share the underlying DMA hardware. A scheduler is provided to control the ordering and rate at which this multiplexing occurs. A block diagram of the PDMA Controller is shown below:

11.3.1.6.2.1 Submodule Descriptions

11.3.1.6.2.1.1 Scheduler

The Scheduler block is responsible for monitoring the fullness level of the various FIFOs, monitoring input DMA triggering events, maintaining channel state information, and issuing credits to the Tx and Rx DMA units when it is time to perform each low level read or write operation.

11.3.1.6.2.1.2 Tx Per Channel Buffers

The Tx Per Channel Buffers implement channelized FIFOs for each DMA channel. A single logical data FIFO is provided for each destination DMA channel that is used for buffering payload data that has been pushed into the PDMA from the Tx PSI-L interface. The Tx Per Channel Buffers are always written with full Tx PSI-L wide words (except for EOL/EOP data phases) but are read on byte granularity from the Tx DMA units.

11.3.1.6.2.1.3 Tx DMA Unit

The Tx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC destination channels. The Tx DMA unit waits until it is triggered by an incoming dma event and then writes data from the Tx Per Channel Data FIFO associated with the channel to an external memory mapped target via a VBUSP controller interface. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.6.2.1.4 Rx Per Channel Buffers

Rx Per Channel Buffers implement a logical FIFO for each source DMA channel that is used for buffering payload data that has been fetched by the Rx DMA units. The buffers are byte oriented on write so that the data from the Rx DMA units which may not be full words can be packed properly. The buffers are word oriented on read in accordance with the transport mechanism outlined in the PSI-L Interface specification. Each channel in the Rx DMA controller maps directly onto a thread in the Rx PSI-L interface. The Rx Per Channel Buffer block outputs queue fullness information to the scheduler block, which it then uses to determine when it should initiate DMA opportunities to backfill the buffers. The Rx Per Channel Buffer initiates transfers to the remote paired thread whenever any data is available in each channel buffer and credits are available in the corresponding thread. The block simultaneously monitors the status of all of the threads and performs a round robin arbitration between the different threads for the use of the Rx PSI-L interface. Each thread for which the target is indicating it can accept data and which currently has data available in the channel buffer is included in the arbitration.

11.3.1.6.2.1.5 Rx DMA Unit

The Rx DMA Unit block implements all of the state machine functionality necessary to implement static TR type UTC source channels. The Rx DMA unit waits until it is triggered by an incoming DMA event and then reads data from an external memory mapped source via a VBUSP controller read interface into the Rx Per Channel Data FIFO associated with the channel. The number and width of the writes that are performed is in accordance with the parameters which were programmed via PSI-L into the static TR for the channel.

11.3.1.6.2.2 General Functionality (Applicable to All Functions/Modes)

11.3.1.6.2.2.1 Operational States

At any given time, the PDMA can be in one of three different states, as shown in Table 11-92.

Table 11-92. PDMA Operational States

Operational State	Description
Init	This is the initial state of the machine during and immediately after reset. During this state, all of the RAMs inside the PDMA will be initialized to known values including the ECC redundant parity bits. While in the init state, the DMA will de-assert all ready signals on all applicable target interfaces and will de-assert all request signals on all applicable controller interfaces. The PDMA will automatically transition out of the init state into the idle state when all of the RAM initialization has been completed.
Idle	Once the PDMA leaves the Init state, it enters the Idle state whenever no outstanding transactions are pending on any of the PDMA interfaces (controller or target). The Idle state is generally a transient state and is used by the PDMA to determine when it is appropriate to allow the SoC power management complex to turn off the clock. For clock stop purposes, the module will only report idle if all DMA channels are disabled using the enable bit in PSIL register 2 for each channel.

Table 11-92. PDMA Operational States (continued)

Operational State	Description
Active	The PDMA enters the active state as soon as it issues a transaction or receives a transaction on any interface that uses a split protocol (expects a later response for a request). When all transactions have been accounted for (responses have all been either received or sent) the PDMA transitions to the Idle state.

11.3.1.6.2.2.2 Clock Stop

The clock stop interface is used to instruct the PDMA to stop issuing commands on its external interfaces. Note that the PDMA will report a clock stop idle if all its DMA channels have been previously disabled by software using the enable bit in PSIL register 2 for each channel.

11.3.1.6.2.2.3 Emulation Control

The emulation control input (susp_emususp) and the per channel emulation control 'free' bit allow DMA operation to be suspended on a per channel basis. When the emulation suspend state is entered, the DMA will stop processing receive and transmit TRs for each channel at the next TR boundary. Any TR currently in reception or transmission will be halted at its next FIFO boundary as configured through the 'X' and 'Y' parameters in the static TR. Emulation control is implemented for compatibility with other peripherals. Each source and destination channel can be configured to either honor the suspend signal, or to 'free run' without regard to suspend. This is controlled via the 'free' bit in the channel Enable Register. Note the real time emulation suspend request signal is not supported.

11.3.1.6.2.3 Events and Flow Control

The following sections describe the simplified mechanism provided on the Peripheral DMA for triggering.

11.3.1.6.2.3.1 Channel Triggering

Channels must be triggered for them to perform work. A local event input bus is provided on the peripheral DMA and each bit in the input bus corresponds to the trigger for the channel with the same channel index as the bit index in the bus (bit 0 triggers channel 0, bit 1 triggers channel 1, and so forth). The event inputs for XY mode are triggered either via pulse, or by a clock synchronous rising edge. The counting mode is a design time configuration parameter. In MCAN mode, the inputs are expected to be single cycle pulses, synchronous with the PDMA clock.

- Event signals that are used in pulse mode must be sourced by the same clock as the PDMA.
- Event signals that are used in edge mode must be sourced by pseudo-synchronous sources (and be a slower clock multiple) to the PDMA clock, and they must remain high for at least 1 'slow' clock cycle.

The PDMA provides a 2-bit counter per event input to accommodate startup latency in the channel. (In AASRC mode, the signals are not counted, but latched whenever asserted.)

11.3.1.6.2.3.2 Completion Events

All transfers on PDMA are split TR in that they have a UDMA-P half and a (static) PDMA half. Completion events are designed to be triggered from the UDMA-P half of the split TR.

11.3.1.6.2.3.3 Channel Types

Each channel in the Peripheral DMA is configured at design time to be either standard X-Y FIFO mode or MCAN channel. The channel type is configured at design time, and can not be changed by software.

11.3.1.6.2.3.3.1 X-Y FIFO Mode

Most peripherals which are serviced by the Peripheral DMA follow the pattern of transferring X bytes from a fixed, non-changing address in a loop Y times for each triggering event that is received. The X parameter is typically 1-16 bytes and the Y parameter can be any integer up to 2048. If a peripheral can be serviced by this basic functionality then it is recommended to use this mode for the peripheral.

11.3.1.6.2.3.3.2 MCAN Mode

The MCANSS subsystem was found to require a few minor differences than standard X-Y mode. First, buffer ownership on transmit is different in that the DMA starts out owning the TX buffer space (instead of waiting for an initial DMA event from the MCAN). There is also a requirement to perform a write of a fixed value to a fixed address after each DMA event is serviced to pass ownership of a buffer back to the MCAN. Finally, MCAN packet fragmentation requirement to place an 8-byte header on each 64-byte chunk that is transmitted and to remove the header from each 64-byte chunk (other than the first block) that is received.

11.3.1.6.2.3.3.3 AASRC Mode

The AASRC mode of the PDMA is similar to the X-Y mode in that X specifies the sample width, any Y specifies the number of FIFO samples to transfer per DMA request, but in addition to this, a programmable FIFO list is supplied that allows a single PDMA channel to transfer data to multiple FIFOs. The FIFO list specifies which FIFOS to access, and in which order to access them. Both AASRC 'stream' and 'group' modes are supported in terms of DMA signalling and the FIFO memory map. When in AASRC mode, the entire PDMA operates exclusively in this mode. AASRC channels to not share the same PDMA as do XY and MCAN channels.

The following additional details apply to the PDMA in AASRC mode.

Main Features:

- Up to 16 independent RX channels and 16 TX channels
  - Each channel represents a different data stream to either the UDMA-P-P or a McASP PDMA
- Each channel can be configured to read or write any of the AASRC FIFOs in any order
- Packing support for 1, 2, 3, and 4 byte samples
  - Can directly talk to a McASP using any McASP data format
  - Packing sample size is fixed for a given channel
- Supports both Group and Stream AASRC signaling and FIFO memory maps
  - There is a single stream/group mode setting for each PDMA channel

Additional details:

- Each channel has a 'mask' of which DMA requests must fire to activate the channel
  - In stream mode, the mask specifies the all the FIFO DMA requests that must fire
  - In group mode, the mask specifies the one group DMA request that must fire
- Each channel specifies an ordered list of how FIFOs should be accessed
  - All channels use a common list, specifying a range of entry indices within that list. This lets each channel use a varying number of list elements.
  - The order list can be processed multiple times per DMA request. The number of samples to be transferred per request must match the configured threshold for the DMA request in the AASRC.
- All FIFOs are specified by index only
  - In the TX ordering table, the indices are assumed to be TX FIFOs
  - In the RX ordering table, the indices are assumed to be RX FIFOs
  - If a DMA channel is in 'Group Mode', the PDMA assumes the indices referenced by that channel represent Group Mode FIFOs; otherwise, it assumes Stream Mode FIFOs.
- The PDMA has configured base addressed and inter-FIFO spans such that is can always convert from a FIFO index to the proper Stream or Group mode FIFO address

11.3.1.6.2.4 Transmit Operation

11.3.1.6.2.4.1 Destination (Tx) Channel Allocation

A total of 8 destination channels are provided within the DMA for concurrent transfers from Tx per channel buffers to the various attached peripherals. Each Tx channel requires a single PSI-L thread. The Tx channels are allocated as follows:

Tx DMA Channel	Function	Channel Type	Trigger Mode	Stream FIFO Address	Group FIFO Address
8000	ASRC0 Tx Ch 0	ASRC	pulse	000002D20000	000002D10000
	ASRC1 Tx Ch 0	ASRC	pulse	000002D60000	000002D50000
8001	ASRC0 Tx Ch 1	ASRC	pulse	000002D20000	000002D10000
	ASRC1 Tx Ch 1	ASRC	pulse	000002D60000	000002D50000

Tx DMA Channel	Function	Channel Type	Trigger Mode	Stream FIFO Address	Group FIFO Address
8002	ASRC0 Tx Ch 2	ASRC	pulse	000002D20000	000002D10000
	ASRC1 Tx Ch 2	ASRC	pulse	000002D60000	000002D50000
8003	ASRC0 Tx Ch 3	ASRC	pulse	000002D20000	000002D10000
	ASRC1 Tx Ch 3	ASRC	pulse	000002D60000	000002D50000
8004	ASRC0 Tx Ch 4	ASRC	pulse	000002D20000	000002D10000
	ASRC1 Tx Ch 4	ASRC	pulse	000002D60000	000002D50000
8005	ASRC0 Tx Ch 5	ASRC	pulse	000002D20000	000002D10000
	ASRC1 Tx Ch 5	ASRC	pulse	000002D60000	000002D50000
8006	ASRC0 Tx Ch 6	ASRC	pulse	000002D20000	000002D10000
	ASRC1 Tx Ch 6	ASRC	pulse	000002D60000	000002D50000
8007	ASRC0 Tx Ch 7	ASRC	pulse	000002D20000	000002D10000
	ASRC1 Tx Ch 7	ASRC	pulse	000002D60000	000002D50000

11.3.1.6.2.4.2 Destination (Tx) Channel Out of Band Signals

The following table shows how PSIL signals are handled for destination channels.

PSI-L Signal	XY/AASRC Mode	MCAN Mode
sop	ignored	ignored
eop	ignored	closes current MCAN packet
sol	ignored	ignored
eol	ignored	ignored
drop	ignored	ignored
pkt_error	ignored	ignored
tdown	reflect in status, teardown when data marker reached	reflect in status, teardown when data marker reached

11.3.1.6.2.4.3 Destination Channel Initialization

After reset, all threads/channels in the PDMA is idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host must first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.6.2.4.3.1 PSI-L Destination Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host pairs each destination PDMA channel with (typically) a corresponding source channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread, and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the UDMA-P send all their data to the destination channel in the PDMA, and the destination channel in the PDMA never sees any data other than data from the source channel in the UDMA-P.

11.3.1.6.2.4.3.2 Static Transfer Request Setup

After reset, all channels in the PDMA are idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host sends configuration transactions across PSI-L and sets up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies somewhat.

11.3.1.6.2.4.3.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.

Param	PSIL Addr	Field	Description
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
Z	0x401	23:0	Not used

11.3.1.6.2.4.3.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8 byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
Z	0x401	23:0	Not used

11.3.1.6.2.4.3.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information:

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer to each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
Z	0x401	23:0	Not used

11.3.1.6.2.4.3.3 PSI-L Destination Thread Enables

PSI-L destination threads must first be enabled to accept data. Threads are enabled or disabled by setting or clearing the enable bit in the PSI-L pairing registers for the thread. When a thread is disabled, it must drop any data phases which are sent but properly return the credits for the data phases which are dropped.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of write transactions.

11.3.1.6.2.4.4 Data Transfer

Packet transmission is accomplished within the PDMA by unpacking and moving data from the Tx Per Channel FIFOs which were filled via the Transmit PSI-L Interface to specified memory mapped address ranges via the VBUSP controller interfaces. On the Tx side of the PDMA, these transfers are always writes. Each write transfer which is performed by the Tx DMA Unit is to a destination address that is hardcoded in the channel at design time and of a size as specified in the static Transfer Request.

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during transmit is dependent on the channel type. The following sections describe what will happen for the different channel types.

11.3.1.6.2.4.4.1 X-Y FIFO Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA sequentially issues a total of 'Y' parameter writes of 'X' parameter bytes to the data_address specified in the tchan_info parameter for the channel. Each write that the DMA performs is a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The write transfers that are performed are accomplished as quickly as possible given availability of data in the Tx channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.6.2.4.4.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. So for example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address increments throughout the burst
- Bursts are sub-divided to fit into a 64 byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA 'gaps' the byte enables on writes as needed

11.3.1.6.2.4.4.2 MCAN Mode Channel

The PDMA channel remains idle until data is received from the UDMA-P over the PSIL interface. At this time, the PDMA immediately starts copying packet bytes into the MCAN TX buffer corresponding the PDMA/MCAN channel. The number of bytes copied is smaller of the remaining bytes in the packet, or the value of the 'Y' parameter. Once a TX buffer has been filled, the PDMA transfers ownership of the buffer to MCAN by performing an MCAN register write. The PDMA then waits to regain ownership of the TX buffer by waiting for the corresponding MCAN TX event. At this time, the PDMA continues with refilling the TX buffer for the next packet fragment. On subsequent fills (until the end of packet is reached), the PDMA skips over the 8 byte MCAN header, leaving the original contents from the initial fragment copy in place.

11.3.1.6.2.4.4.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's TxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel remains idle until a pulse is detected on ALL associated input DMA request event pins required by the TxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it starts reading FIFO index values from the TxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs written for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width written to the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The write transfers that are performed are accomplished as quickly as possible, given availability of data in the TX channelized FIFO and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.6.2.4.5 Transmit PSI-L Interface Transactions

The PDMA accepts data across the Tx PSI-L Interface in accordance with the physical handshaking protocol, as defined in the PSI-L Interface specification. The value sources for the output pins on the PSI-L interface are described in the following table.

Pin	Output Value / Source From PDMA
strm_i_link	This signal is asserted high to indicate the PSI-L link is valid.
strm_i_ready	This signal is asserted high anytime there is space in the PSI-L ingress fifo.
strm_i_sreq	This signal is asserted high anytime there is credit return data waiting in the PSI-L status fifo.
strm_i_sthreadid	This is set to the local destination thread that is returning credit.
strm_i_sccnt	This is set to the number of credits being returned, or 0 on a TX teardown acknowledgement.

11.3.1.6.2.4.6 Tx Pause

The Host initiates a channel pause by setting the pause bit in the RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.6.2.4.7 Tx Teardown

The Host initiates a channel teardown by setting the tdown bit in the UDMA-P channel paired with the PDMA. The UDMA-P communicates the teardown state through the PSI-L data channel, to ensure that the teardown is not seen by the PDMA until all the previous UDMA-P data for the channel has been flushed. At this time, the teardown state is reflected in the PSI-L RT Enable register of the PDMA. Note that a non-synchronized teardown can also be initiated by directly clearing the enable bit in the PSI-L RT Enable register of the PDMA.

Once all data has been flushed from the PDMA to the peripheral, the enable state of the PDMA channel is cleared in the PSI-L RT enable register, but the teardown bit remains high. A teardown completion indication is sent back across the status pins of the PSI-L in the form of a credit response with sccnt=0. Upon completion, no further packet processing occurs until the Host re-configures the channel. If the channel fails to teardown because the peripheral has stopped responding, or if the UDMA-P transmission stops on a data boundary that is not compatible with the static TR configuration, the flush bit in the RT enable register can be set to ensure that all data can be properly flushed from the internal pipe.

11.3.1.6.2.4.8 Tx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully, even with flush enabled. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L Enable register. This causes a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.6.2.4.9 Tx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For transmit, they are defined as in Table 11-93.

Table 11-93. Tx Debug/State Register

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Flush	0x403	30	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
Pause	0x403	29	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.
Data	0x403	28	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
XData	0x403	27	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.

11.3.1.6.2.5 Receive Operation

11.3.1.6.2.5.1 Source (Rx) Channel Allocation

A total of 8 source channels are provided within the DMA for concurrent transfers from the various attached peripherals into the Rx per channel buffers and on to the PSI-L Rx Interface. Each Rx channel requires a single PSI-L thread. The Rx channels are allocated as follows.

Rx DMA Channel	Function	Channel Type	Trigger Type	Stream FIFO Address	Group FIFO Address
0	ASRC0 Rx Ch 0	ASRC	pulse	000002D21000	000002D10080
	ASRC1 Rx Ch 0	ASRC	pulse	000002D61000	000002D50080
1	ASRC0 Rx Ch 1	ASRC	pulse	000002D21000	000002D10080
	ASRC1 Rx Ch 1	ASRC	pulse	000002D61000	000002D50080
2	ASRC0 Rx Ch 2	ASRC	pulse	000002D21000	000002D10080
	ASRC1 Rx Ch 2	ASRC	pulse	000002D61000	000002D50080
3	ASRC0 Rx Ch 3	ASRC	pulse	000002D21000	000002D10080
	ASRC1 Rx Ch 3	ASRC	pulse	000002D61000	000002D50080
4	ASRC0 Rx Ch 4	ASRC	pulse	000002D21000	000002D10080
	ASRC1 Rx Ch 4	ASRC	pulse	000002D61000	000002D50080
5	ASRC0 Rx Ch 5	ASRC	pulse	000002D21000	000002D10080
	ASRC1 Rx Ch 5	ASRC	pulse	000002D61000	000002D50080

Rx DMA Channel	Function	Channel Type	Trigger Type	Stream FIFO Address	Group FIFO Address
6	ASRC0 Rx Ch 6	ASRC	pulse	000002D21000	000002D10080
	ASRC1 Rx Ch 6	ASRC	pulse	000002D61000	000002D50080
7	ASRC0 Rx Ch 7	ASRC	pulse	000002D21000	000002D10080
	ASRC1 Rx Ch 7	ASRC	pulse	000002D61000	000002D50080

11.3.1.6.2.5.2 Source Channel Initialization

After reset, all threads/channels in the PDMA will be idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host must first pair the channel with a remote data source (normally a UDMA-P channel), set up the static TR for the channel, and enable the thread.

11.3.1.6.2.5.2.1 PSI-L Source Thread Pairing

After reset, all threads on PSI-L are uninitialized and unpaired. The Host pairs each source PDMA channel with (typically) a corresponding destination channel in the UDMA-P. The PDMA thread is configured to point to the UDMA-P thread, and the UDMA-P thread is configured to point to the PDMA thread. Once paired, the source channels in the PDMA send all their data to the source channel in the UDMA-P, and the destination channel in the UDMA-P never sees any data other than data from the source channel in the PDMA.

11.3.1.6.2.5.2.2 Static Transfer Request Setup

After reset, all channels in the PDMA are idle and waiting for work to be assigned to them. To initiate PDMA operation, the Host sends configuration transactions across PSI-L and sets up the static TR for each destination channel. The format of the TR is identical for each DMA mode, consisting of an X, Y, and Z parameter, but the field interpretation varies.

11.3.1.6.2.5.2.2.1 X-Y FIFO Mode Static TR

In X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	When set, enables VBUSP burst mode on this channel. See the XY burst description for more information.
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, 4 = 64 bits, and 5-7 = RESERVED
Y	0x400	11:0	Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.6.2.5.2.2.2 MCAN Mode Static TR

In MCAN mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used

Param	PSIL Addr	Field	Description
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Not used
Y	0x400	11:0	Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an 'EOP' indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8 byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.

11.3.1.6.2.5.2.2.3 AASRC Mode Static TR

AASRC mode is similar to X-Y FIFO mode, the static TR consists of the following information.

Param	PSIL Addr	Field	Description
Burst	0x400	31	Not used
Acc32	0x400	30	When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
X	0x400	26:24	Element size. This field specifies how much data is transferred in each read which is performed by the DMA. This field is encoded as follows: 0 = 8 bits, 1 = 16 bits, 2 = 24 bits, 3 = 32 bits, and 4-7 = RESERVED
Y	0x400	11:0	FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.
EOL	0x401	31	EOL Mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
Z	0x401	23:0	FIFO count. This field specifies how many full DMA request operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an 'EOP' indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.

11.3.1.6.2.5.2.3 PSI-L Source Thread Enables

PSI-L source threads must be enabled in order to process peripheral DMA requests and send data. When disabled, DMA requests are ignored.

Once a thread is paired, the TR has been set up and the enable is asserted, the channel is armed and ready to be triggered to perform the specified set of read transactions.

11.3.1.6.2.5.3 Data Transfer

Packet reception is accomplished within the PDMA by moving data from structures that are located in memory accessible via the VBUSP Memory Interface(s) onto the Receive PSI-L Interface. On the Rx side of the PDMA, these transfers are always reads. Data is read from an attached memory mapped space and packed into the Rx Per Channel Buffer for that channel. At a later time, the data is moved from the Rx Per Channel FIFO to a remote peer DMA entity via the Rx PSI-L interface

The sequences of logical transactions that are performed by the PDMA on the Memory I/F during receive is dependent on the channel type. The following sections describe what happens for the different channel types.

11.3.1.6.2.5.3.1 X-Y FIFO Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. Once the pulse is detected, the DMA sequentially issues a total of 'Y' parameter reads of 'X' parameter bytes from the data_address specified in the tchan_info parameter for the channel. Each read that the DMA performs is a single 'X' element in size (no large bursts). Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The read transfers that are performed are accomplished as quickly as possible given availability of data in the Rx channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same read unit.

11.3.1.6.2.5.3.1.1 X-Y FIFO Burst Mode

The burst mode for XY is designed to allow the PDMA to burst across a FIFO region, while extracting out the 'sample size' from each data phase. For example, it can read a "burst" of multiple 32-bit words from a McASP, and grab only 24-bits from each data phase.

It uses the same registers as standard XY mode, where X is the encoded sample size, and Y is the number of samples to read/write per DMA request. Setting bit 31 of the XY register enables burst.

The following are the rules for enabling burst mode. Incompatible peripherals do not need to enable burst, or can enable it on RX without enabling it on TX.

- The VBUSP address will increment throughout the burst
- Bursts are sub-divided to fit into a 64-byte transfer window
- One sample is transferred for every bus data phase
  - Cannot burst one byte samples from a 16-bit peripheral on a 32-bit bus
  - Cannot burst 64-bit samples on a 32-bit bus (configure for 2 32-bit samples instead)
- PDMA 'gaps' the byte enables on writes as needed

11.3.1.6.2.5.3.2 MCAN Mode Channel

The PDMA channel remains idle until a pulse is detected on the associated input DMA request event pin. The DMA event pins are mapped from the CAN filter event bits. The event bits determine the channel and one of two CAN buffers to use for the RX operation. This allows the RX buffers on the CAN to be configured in a ping/pong fashion, preventing the loss of CAN packet data. When an event is received, the PDMA starts copying bytes out of the corresponding CAN buffer. The number of bytes copied is equal to the value of the 'Y' parameter in the channel configuration. Once all data has been copied from the buffer, the PDMA transfers ownership of the buffer back to the CAN by writing a CAN register. It then waits for another RX DMA event. The PDMA can copy multiple CAN RX buffers to the same CPPI packet. It will not close out the CPPI packet until it has copied out a number of RX buffers equal to the 'Z' parameter in the channel configuration. On subsequent RX buffer copies, the MCAN skips the first 8 bytes of the RX buffer, which is the MCAN packet header.

The mapping of MCAN filter events to MCAN channels and buffer is important for properly configuring the DMA. The mapping is defined as follows.

CAN FE2	CAN FE1	CAN FE0	Description
0	0	0	Not used
0	0	1	Not used
0	1	0	PDMA CAN channel offset 0, RX buffer 0
0	1	1	PDMA CAN channel offset 0, RX buffer 1
1	0	0	PDMA CAN channel offset 1, RX buffer 2

CAN FE2	CAN FE1	CAN FE0	Description
1	0	1	PDMA CAN channel offset 1, RX buffer 3
1	1	0	PDMA CAN channel offset 2, RX buffer 4
1	1	1	PDMA CAN channel offset 2, RX buffer 5

By using two filter entries in the CAN, software can setup a ping/pong buffer for a particular RX packet ID. For example, the following two filter entries set up a ping/pong using RX buffers 0 and 1 for packet ID 5 on CAN RX channel 0.

Filter Entry	Packet Match ID	Filter Event Bits
0	5	0x2
1	5	0x3

11.3.1.6.2.5.3.3 AASRC Channel

The AASRC channel is controlled primarily via the channel's RxFifoConfig register. This register holds 3 basic pieces of information:

- Whether the channel uses AASRC Stream Mode or Group Mode
- The slot range in the order table used (from designated first slot to designated last slot)
- The AASRC DMA request event(s) that must fire before the channel becomes active

The channel remains idle until a pulse is detected on ALL associated input DMA request event pins required by the RxFifoConfig setting. The pulses for the individual events are latched and held by the PDMA until they all arrive.

Once the channel activates, it starts reading FIFO index values from the RxOrderTable, starting at the configured 'First Slot' and ending with the 'Last Slot'. The actual FIFO indices used are obtained from the ordering table. For example, say FirstSlot=3 and LastSlot=5. If the first 6 slots of the ordering table were: 0, 2, 4, 6, 8, 10, the FIFOs read for the event would be 6, 8, and 10, because 'slot 3' of the table contains 6, and it would proceed through 'slot 5' of the table which contains 10.

The X and Y registers are still used as they are in a normal X-Y mode. When accessing each FIFO, the setting of X determines the sample byte width read from the FIFO. The value of 'Y' determines how many times the entire FIFO list is processed for each activation of the channel.

Once the total specified number of transactions has been completed, the channel returns to an idle state and waits until it is triggered again. The read transfers that are performed are accomplished as quickly as possible given availability of data in the TX channelized FIFO, and given the arbitration that may occur as a result of other channels also using the same write unit.

11.3.1.6.2.5.4 Receive PSI-L Interface Transactions

When an entire word has been packed into the Rx Per Channel Buffer for a given channel, a one word data phase transfer is initiated for that channel/thread on the Rx PSI-L interface, and the data is popped from the Rx Per Channel FIFO. The value sources for the output pins on the PSI-L interface are described in Table 11-94.

Table 11-94. PSI-L Interface Output Pins

Pin	Output Value / Source From PDMA
strm_o_req	This signal is asserted when the PDMA determines that there is at least 1 word of data in it's TP-CC output FIFO
strm_o_sthread_id	Set equal to the TP-CC DMA channel number which is on the interface for this cycle
strm_o_dthread_id	Set equal to the target thread ID value given in the PSI-L pairing configuration registers for this DMA channel
strm_o_data_type	Will be set to the proper PSI-L data type. The PDMA can send config response, PSI info word 0, and PSI data word.
strm_o_wnum	Set equal to the packing lane for the current word within a contiguous transfer. This value will start at 0 for each new TR and will increment for each subsequent data phase in the TR.
strm_o_lastw	This signal will be asserted coincident with eop.
strm_o_xcnt	The xcnt will be equal to the data path width in bytes.

Table 11-94. PSI-L Interface Output Pins (continued)

Pin	Output Value / Source From PDMA
strm_o_worden	The worden will be modulated to indicate which 32-bit words are valid within each control type data phase.
strm_o_data	The data will be packed/left justified to comply to the big endian data ordering as required in the PSI-L I/F specification.
strm_o_sop	This signal is asserted for 1 data phase at the beginning of each new TR or data transfer packet.
strm_o_eop	This signal is asserted for 1 data phase at the end of each TR or data transfer packet.
strm_o_sol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the start of a new set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_eol	This signal is set to zero unless the EOL bit is set in PSI-L register 0x401, in which case, it is set for 1 data phase at the end of a set of transactions designated by the count set in the Z field of PSI-L register 0x401.
strm_o_priv	Set to zero.
strm_o_privid	Set to zero.
strm_o_virtid	Set to zero.
strm_o_secure	Set to zero.
strm_o_interest	Set to zero.
strm_o_sready	Always asserted as the PDMA is always able to accept credit returns.

11.3.1.6.2.5.5 Rx Pause

The Host initiates a channel pause by setting the pause bit in RT enable register. The paused channel can be resumed by clearing the register bit.

11.3.1.6.2.5.6 Rx Teardown

The Host initiates a RX channel teardown by setting the tdown bit in the RT enable register for the target RX channel. The PDMA communicates the teardown state to the UDMA-P through the PSI-L data channel, to ensure that the teardown is not seen by the UDMA-P until all the previous PDMA data for the channel has been flushed.

The PDMA does not stop reading peripheral data until it reaches a FIFO boundary, as configured through the 'X' and 'Y' parameters in the static TR. It always attempts to complete the 'Y' count for the current event being processed. Upon reaching a stopping point, the PDMA then clears the enable bit in the pairing register; however, the teardown bit remains set. No further packet processing occurs until the Host re-configures the channel. The teardown process propagates to the UDMA-P and its final status can be checked there.

11.3.1.6.2.5.7 Rx Channel Reset

In the unlikely event that channel synchronization is corrupted, a channel may fail to teardown gracefully. If this occurs, the channel may be reset by clearing the enable bit in the PSI-L enable register. This causes a local reset of the entire channel, including TR and pairing registers. Note that it does not reset the UDMA-P peer. Resetting the UDMA-P peer is also required before re-initializing and re-pairing the channel.

11.3.1.6.2.5.8 Rx Debug/State Register

The debug/state registers are supplied to give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations. The registers appear on the PSI-L bus, near the static TR registers. For receive, they are defined as in Table 11-95.

Table 11-95. Rx Debug/State Register

Name	PSIL Addr	Field	Description
Z*	0x402	31:16	This field holds the lower 12 bits of the current Z count for legacy purposes. See register 0x40F below for the full width version of Z.

Table 11-95. Rx Debug/State Register (continued)

Name	PSIL Addr	Field	Description
Y	0x402	15:0	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.
InEvent	0x403	31	When set, the PDMA is in the middle of processing a FIFO event.
Tdown	0x403	30	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
Pause	0x403	29	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is un-paused or disabled.
Space	0x403	28	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
XSpace	0x403	27	When set, there is a enough internal FIFO space available to start servicing a peripheral DMA event.
Buffer	0x403	26	This is the current RX buffer (0/1) for the current MCAN receive operation.
State	0x403	23:20	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
EventCnt	0x403	19:16	This field holds the number of backlogged DMA events yet to be serviced.
Z	0x40F	31:0	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

12 Peripherals

Note

This chapter can refer to an MCU domain or IPs with a "MCU_" substring. These don't apply to the device. Please refer to *Domain Partition* for more details.

12.1 Audio Peripherals

12.1.1 Audio Sample Rate Converter (ASRC)

This section describes the asynchronous Audio Sample Rate Converter (ASRC) in the device.

12.1.1.1 ASRC Overview

The reception of many different audio sources and the transmission of these to different audio zones, may require different audio clocks. The asynchronous Audio Sample Rate Converter (ASRC) module takes samples from one clock zone and moves them to another, while maintaining a high signal to noise ratio to ensure that the output quality is sufficient to meet the requirements for various high-end algorithms.

ASRC Overview Diagram is a simplified overview diagram of the ASRC module implementation within the device.

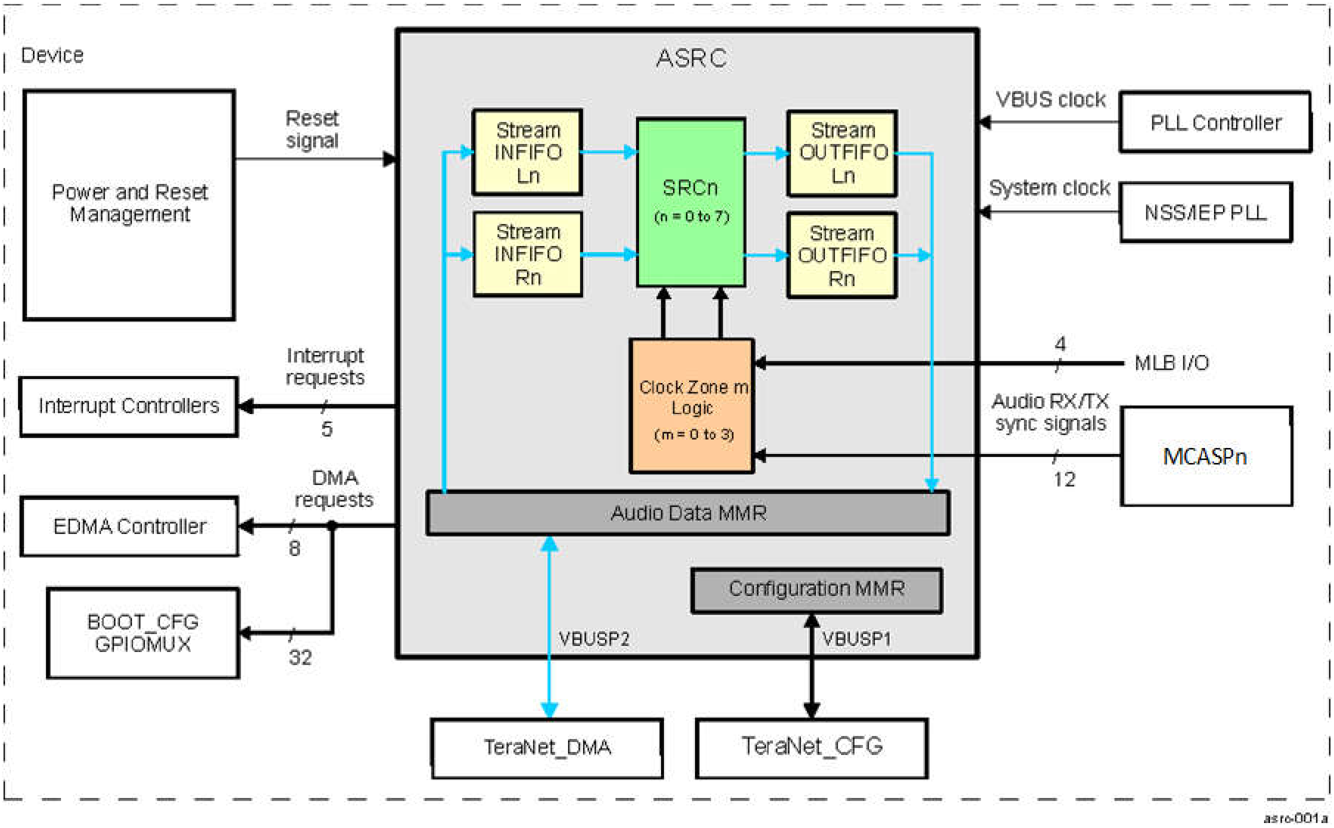


Figure 12-1. ASRC Overview Diagram

The ASRC module supports the following main features:

- High performance Asynchronous Sample Rate Converter with 140dB Signal-to-Noise (SNR)
- Up to 8 input and output stereo streams (16 audio channels)
- 4 input and output clock zones
- Support for input and output audio sample rates from 8 kHz to 216 kHz
- Automatically sensing/detection of input sample frequencies
- Attenuation of sampling clock jitter
- 16-, 18-, 20-, 24-bit data input/output
- Input/output sampling ratios from 16:1 to 1:16
- 128-sample input and 32-sample output FIFO for each channel with independently configurable thresholds
- Group mode, where multiple ASRC blocks use the same timing loop for input or output
- Linear phase FIR filter
- Controllable soft mute
- De-Emphasis supported for 48, 44.1 and 32 kHz sample rates
- Separate DMA events for input and output, for each channel and group

- Interrupts for input, output, and error for channels and groups of channels
- Independent clock generator for each input and output clock zone
- Channels belonging in an input/output clock zone may be configured and managed as a group or as individual streams

The ASRC module has the following main constrains:

- The ASRC output rate divided by input rate must be between 1/16 and 16
- Sample rate must be between 8 and 216 kHz

Note

ASRC is also known as AASRC

12.1.1.2 ASRC Functional Description

12.1.1.2.1 ASRC Block Diagram and Implementation

The Asynchronous Audio Sample Rate Converter (ASRC) allows the movement of up to 8 audio stereo streams (16 audio channels) from one audio zone to another audio zone via 8 two-channel sample rate converters.

Each sample rate converter performs a digital audio sample rate conversion between input and output clock zone sample rates. The input and output clock zones can be individually selected for each sample rate converter in stream mode configuration. In group mode configuration, the sample rate converters that make up each group share the same input and output clock zone specifications. Each input and output channel is buffered by a 32-sample FIFO. The FIFO threshold values are programmed to a value between 1 and 16 samples.

The ASRC converts audio data between 4 input and 4 output clock zones. The clock zones provide a sample rate (Fs) input into clock rate estimators on the receive side and transmit side. Each ASRC receive and transmit clock zone input can come from one of 8 possible sources as shown in *ASRC Block Diagram*. The input clocks and output clocks can have any frequency that is within the constraints specified in *ASRC Overview* and are completely asynchronous to each other.

The ASRC works by interpolating the input audio signals that are in the sequential domain of the source audio input clock. The input audio signal is interpolated up to 16x the input rate, then resampled at 16x the output rate, and then downsampled to the desired output clock frequency.

ASRC Block Diagram shows a simplified block diagram of ASRC module.

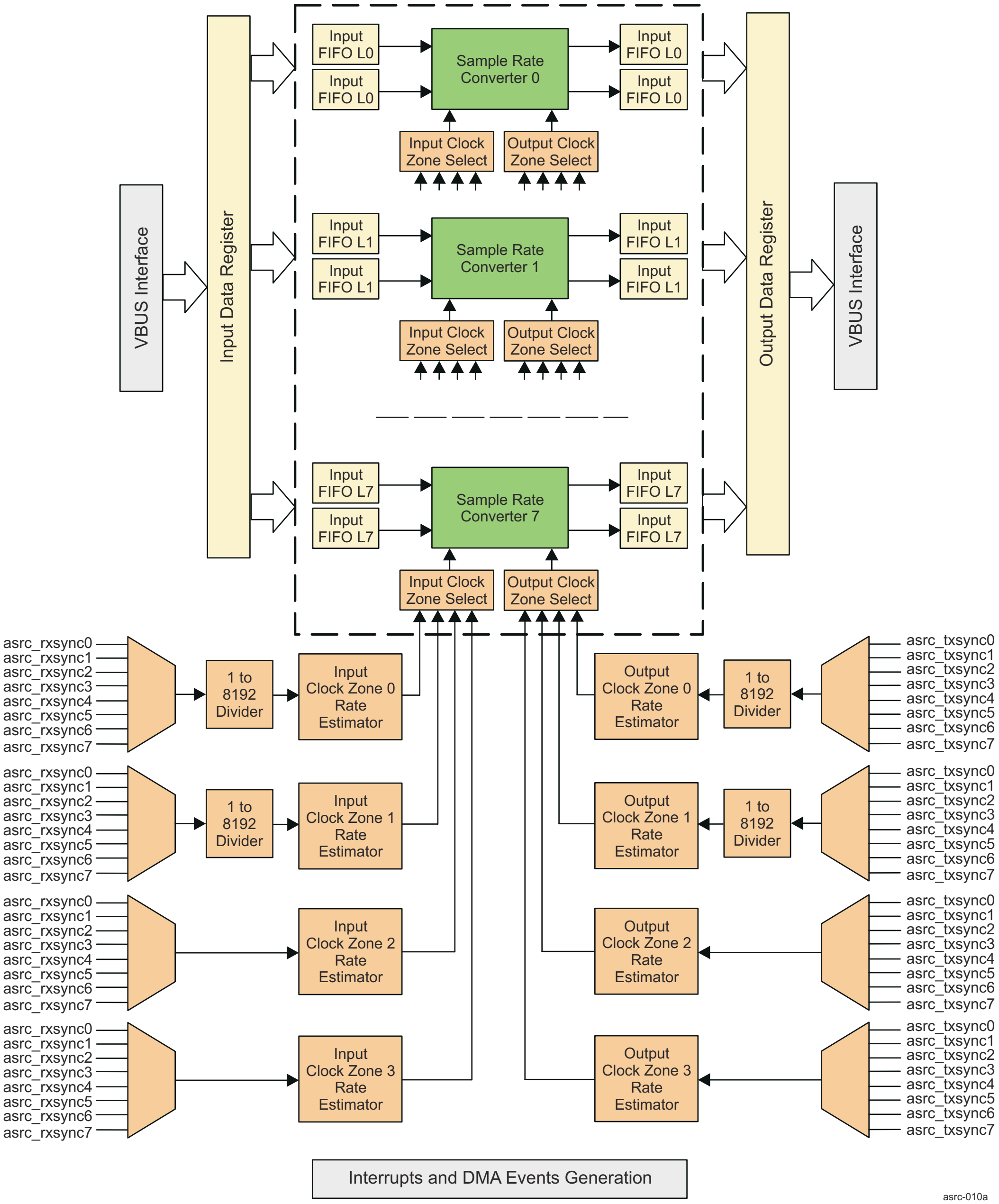


Figure 12-2. ASRC Block Diagram

The ASRC can handle multiple channels and switch between each channel as samples become available. The ASRC external interface is VBUS interface. One VBUS Interface is provided for configuration and status registers and another VBUS interface is dedicated for writing and reading audio samples. The ASRC also generate events when a configurable amount of output samples are ready. The ASRC implemets sample packer modules for processing the different streams as data becomes available.

The ASRC is a loosely coupled coprocessor to the main SoC DSP. Data is moved into the ASRC by device EDMA controller and an event is generated when another block of samples is completed for a given audio stream. In order to minimize the number of EDMA channels and events required, the ASRC also supports group events which are generated only when all of the selected Left and Right channels meet a pre-defined FIFO threshold. This permits a single EDMA transfer to perform the input and a single EDMA transfer to perform the output of all of the channels in the group.

As an alternative to EDMA moderated data input and output ASRC data transfers, the ASRC also supports input FIFO and output FIFO interrupts to permit a device processor to control the data transfers. The ASRC generates an error interrupt when a FIFO overflow and underflow error condition occurs.

The ASRC supports two modes of transferring data into the ASRC data inputs and from the ASRC data outputs:

- Group Mode, which enables all of the streams that are part of an input or output clock zone to be transferred using a single EDMA (each group is controlled by separate EDMA. Group mode is well suited for handing stereo or multichannel data from a single source.
- Stream Mode, which enables each stream to be transferred using a separate EDMA (each individual stream can be controlled by a separate EDMA). Stream mode is well suited for handing data from two or more isolated sources.

12.1.1.2.2 ASRC Data Rate and Traffic Behavior

The ASRC traffic and transaction behavior is a function of the input and output sample rates. The rate of the transactions is 4 bytes per sample. For example, if the input rate is 48 kHz, then the input data rate will be 192 KB/s. The traffic is bursty based upon the threshold size set in the ASRC_SRCFFCTRL_0 register.

The following must be considered:

- Output rate / Input rate ratio must be between 1/16 and 16
- Sample rate must be less than or equal to 216 kHz

12.1.1.2.3 ASRC Data Interface and Formats

Note

The only internal data format is of a 28-bit sample. Externally, the only format supported is a packed 24-bit samples into a 32-bit word, as described in this section.

Data is written to the ASCR and read from the ASRC using the VBUS interface. This interface has separate data register memory regions for Stream and Group input / output. Each region is used as based upon the mode (Group or Stream) that has been selected for each sample rate converter.

The ASRC data format is little endian, with up to 24-bit samples of data packed into 32-bit word.

ASRC supports 16-/18-/20-/24-bit audio data. ASRC understands audio data in the format dictated by *ASRC Data Packing at the SRC Interface*, which holds true for both input and output channels.

Table 12-1. ASRC Data Packing at the SRC Interface

Sample Width	[31:24]	[23:8]	[7:6]	[5:4]	[3:0]
24-bit	8’h00	AudioData[23:0]			
20-bit	8’h00	AudioData[19:0]			4’h0
18-bit	8’h00	AudioData[17:0]		6’h00	
16-bit	8’h00	AudioData[15:0]	8’h00		

ASRC also supports automatic HW audio data alignment. Audio data alignment is active by default, but can be disabled via ASRC_SYSCONFIG[1] DATA_FORMAT_DISABLE register bit.

If auto data alignment feature is disabled, then data format for the audio samples at the VBUS interface can be seen in *ASRC Data Packing at the VBUS at the Interface When Auto Alignments is Disable*d. For input audio samples packed into 32-bit VBUS packet, the most significant 8 bits [31:24] are always ignored by the ASRC internal engine. For output audio samples packed into 32-bit VBUS packet, the most significant 8 bits are always padded with 0’s.

Table 12-2. ASRC Data Packing at the VBUS Interface When Auto Alignment is Disabled

Sample Width	[31:24]	[23:8]	[7:6]	[5:4]	[3:0]
24-bit	8’h00	AudioData[23:0]			
20-bit	8’h00	AudioData[19:0]			4’h0
18-bit	8’h00	AudioData[17:0]		6’h00	

Table 12-2. ASRC Data Packing at the VBUS Interface When Auto Alignment is Disabled (continued)

Sample Width	[31:24]	[23:8]	[7:6]	[5:4]	[3:0]
16-bit	8’h00	AudioData[15:0]	8’h00		

In case of automatic HW alignment is being used (this feature is selected by default), input audio samples packed into 32-bit VBUS packet must be LSB aligned. Input data format for the audio samples at the VBUS interface can be seen in *ASRC Input Data Packing at the VBUS Interface When Auto Alignment is Enabled*.

Table 12-3. ASRC Input Data Packing at the VBUS Interface When Auto Alignment is Enabled

Sample Width	[31:24]	[23:20]	[19:18]	[17:16]	[15:0]
24-bit	xx	AudioData[23:0]			
20-bit	xx		AudioData[19:0]		
18-bit	xx			AudioData[17:0]	
16-bit	xx				AudioData[15:0]

In case of automatic HW alignment is being used, output audio samples will be packed into 32-bit VBUS packet. Audio data will be LSB aligned, little endian and sign extended 2’s complement. Output data format for the audio samples at the VBUS interface can be seen in *ASRC Output Data Packing at the VBUS Interface When Auto Alignment is Enabled*.

Table 12-4. ASRC Output Data Packing at the VBUS Interface When Auto Alignment is Enabled

Sample Width	[31:24]	[23:20]	[19:18]	[17:16]	[15:0]
24-bit	sign extend	AudioData[23:0]			
20-bit	sign extend		AudioData[19:0]		
18-bit	sign extend			AudioData[17:0]	
16-bit	sign extend				AudioData[15:0]

12.1.1.2.4 ASRC Clock Configuration

The ASRC_SYS_CLK is used for all filter processing in the module..

The ASRC_VBUS_CLK is used for VBUS interfaces.

There are four dividers present to divide the input audio sample rate clocks (ASRC_RXSYNC0-7 and ASRC_TXSYNC0-7). Two dividers are used for RX side and other two dividers are used for the TX side. The RX side dividers are working on the muxed ASRC_RXSYNC0-7 clocks. The TX side dividers are working on the muxed ASRC_TXSYNC0-7 clocks. The dividers are used for Clock Zone 0 and Clock Zone 1 only, on both RX and TX sides, and are controlled via ASRC_ICKDIV register (for RX side) and ASRC_OCKDIV register (for TX side).

The muxing of ASRC_RXSYNC0-7 clocks is controlled by [3-0] INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT bit-field within ASRC_ICKZCTRL_0 to ASRC_ICKZCTRL_3 registers. The muxing of ASRC_TXSYNC0-7 clocks is controlled by [3-0] OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT bit-field within ASRC_OCKZCNT_0 to ASRC_OCKZCNT_3 registers.

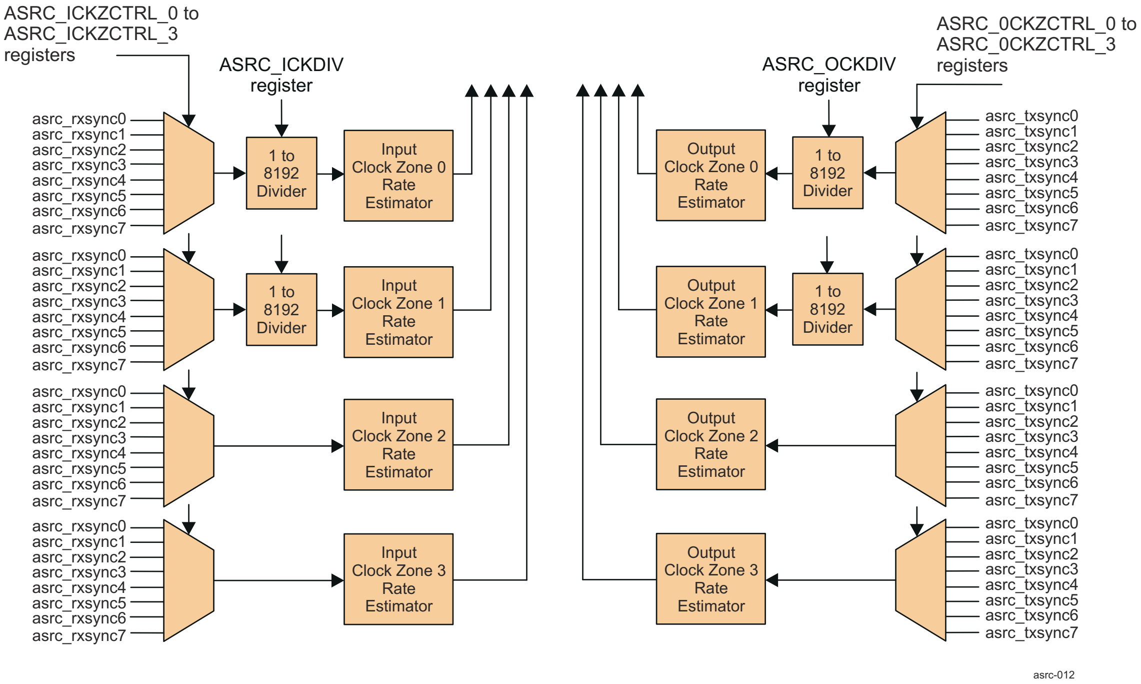


Figure 12-3. ASRC Input and Output Clock Zone Controls

12.1.1.2.4.1 ASRC RXSYNC and TXSYNC

The Input side Audio Sample Clock can be selected through the mux select bits described in Table 12-5. The Output Side Audio Sample Clock can be selected through the mux bits described in Table 12-6.

Table 12-5. ARSC_RXSYNC[0:4]_SEL_SYNC_SEL

Mux Select (ASRC[0:1]_RXSYNC[0:4]_SEL_SYNC_SEL)	SYNC Source
0	MCASP0_AFSR Pin Input
1	MCASP1_AFSR Pin Input
2	MCASP2_AFSR Pin Input
3	MCASP3_AFSR Pin Input
4	MCASP4_AFSR Pin Input
8	MCASP0 AFSX Pin Input
9	MCASP1 AFSX Pin Input
10	MCASP2 AFSX Pin Input
11	MCASP3 AFSX Pin Input
12	MCASP4 AFSX Pin Input
16	AUDIO_EXT_REFCLK0_IN
17	AUDIO_EXT_REFCLK1_IN
18	AUDIO_EXT_REFCLK2_IN
20	ADC0_CLK
21	MLB_IO_CLK
22	DIV_PLL4_HSDIV3_CLKOUT
24	MCU_EXT_REFCLK0
25	EXT_REFCLK1
26	CPSW_3GUSS_CPTS_GENF0
27	CPSW_3GUSS_CPTS_GENF1

Table 12-6. ASRC_TXSYNC[0:4]_SEL_SYNC_SEL

Mux Select (ASRC[0:1]_TXSYNC[0:4]_SEL_SYNC_SEL)	SYNC Source
0	MCASP0_AFSR Pin Input
1	MCASP1_AFSR Pin Input
2	MCASP2_AFSR Pin Input
3	MCASP3_AFSR Pin Input
4	MCASP4_AFSR Pin Input
8	MCASP0 AFSX Pin Input
9	MCASP1 AFSX Pin Input
10	MCASP2 AFSX Pin Input
11	MCASP3 AFSX Pin Input
12	MCASP4 AFSX Pin Input
16	AUDIO_EXT_REFCLK0_IN
17	AUDIO_EXT_REFCLK1_IN
18	AUDIO_EXT_REFCLK2_IN
20	ADC0_CLK
21	MLB_IO_CLK
22	DIV_PLL4_HSDIV3_CLKOUT
24	MCU_EXT_REFCLK0
25	EXT_REFCLK1
26	CPSW_3GUSS_CPTS_GENF0
27	CPSW_3GUSS_CPTS_GENF1

12.1.1.2.5 ASRC Reset Configuration

The ASRC module is based on a single asynchronous reset that is synchronized to ASRC_SYS_CLK, ASRC_VBUS_CLK, and divider clocks (muxed version of TX and RX SYNC signals). The reset impacts configuration and processing information.

Additionally, each processing path enters a reset state when it is disabled, until the path is enabled with a new stream. This reset clears the data path and all memories associated with the path, when the new stream is started.

12.1.1.2.6 ASRC Power Management

Power management is accomplished using a standard clock stop protocol interface. When ASRC module is instructed to disable clocks for the internal clock domain, the internal clock network is shut down. This applies to the ASRC_SYS_CLK and ASRC_VBUS_CLK

Before a clock stop request is asserted at ASRC input, SW needs to confirm that ASRC is fully idle. HW will not check internal states to verify ASRC is idle. HW does check that no VBUSP transactions are ongoing before acknowledging the clock stop request.

12.1.1.2.7 ASRC Interrupts and Data Transfer Model

The ASRC can generate interrupt signals whenever interrupt condition is satisfied. These signals are exported on ASRC module boundary and can be used to trigger DMA transactions. There is a dedicated interrupt signal for audio samples write and for audio samples read, respectively.

All channels share common interrupt signals at the ASRC module boundary: infifo_intr and outfifo_intr, for write and read respectively. All groups also share common interrupt signals at the ASRC module boundary: ingrp_intr and outgrp_intr, for write and read respectively.

- In group mode, where more than one channels are part of one particular group, ingrp_intr and outgrp_intr need to be used, and infifo_intr and outfifo_intr need to be disabled accordingly.
- In stream mode, where a channel is working independently, infifo_intr and outfifo_intr need to be used.

For more details on interrupt descriptions, refer to *ASRC Interrupts*. Software is aware of the configuration of each channel, whether it is a part of stream mode or group mode, and corresponding interrupts need to be disabled. If a channel is part of any group, then infifo_intr and outfifo_intr for that particular channel need to be disabled.

Table 12-7. ASRC Interrupts

Interrupt Event Name	Status Register	Set Register	Clear Register	Description
INFIFO_INTR	ASRC_IFIRQENSTS	ASRC_IFIRQENSET	ASRC_IFIRQENCLR	Interrupt indicating that one of the input FIFOs has enough space below the configured threshold.
OUTFIFO_INTR	SRC_OFIRQENSTS	ASRC_OFIRQENSET	ASRC_OFIRQENCLR	Interrupt indicating that one of output FIFOs has enough data above the configured threshold.
INGROUP_INTR	ASRC_IGIRQENSTS	ASRC_IGIRQENSET	ASRC_IGIRQENCLR	Interrupt indicating that the one of the configured Group interrupts has all of the configured Input FIFOs below their respective threshold.
OUTGROUP_INTR	ASRC_OGIRQENSTS	ASRC_OGIRQENSET	ASRC_OGIRQENCLR	Interrupt indicating that one of the configured Group interrupts has all of the configured Output FIFOs above their respective threshold.
ERROR_INTR	ASRC_ERIRQENSTS	ASRC_ERIRQENSET	ASRC_ERIRQENCLR	Interrupt indicating one of the streams has received an error condition, FIFO overflow or underflow

12.1.1.2.7.1 Input FIFO Interrupts

Each channel has a dedicated input FIFO that is filled when an VBUS write (by a processor, EDMA, or DMA) occurs to that particular channel data register. The ASRC keeps tracks of the number of writes to the input FIFO and the number of reads that are sent into the processing path. The infifo interrupt will fire whenever the Input FIFO for the channel is below the threshold set in the ASRC_SRCFFCTRL_0[7:0] INFIFO_THRESHOLD register field. The interrupt will not be active until channel is enabled. Status for each FIFO can be checked in the ASRC_IFIRQENSTS status register. Once an INFIFO interrupt is fired, next interrupt will be generated only after INFIFO_THRESHOLD number of Audio RX Sync pulses has occured for that particular channel.

When the CPU is used to transfer data to ASRC, whenever an infifo_intr is triggered, SW needs to read the ASRC_IFIRQENSTS status register in order to determine which channels need to be serviced. Based on interrupt status register, software can trigger DMA to initiate transactions to channels. Data transfer will be in the same manner as described in *ASRC Stream Mode Audio Data Write for Channel N* with DMA triggered by software instead of infifo_evt event. After servicing the channel, SW needs to clear the interrupt for that particular channel.

12.1.1.2.7.2 Output FIFO Interrupts

Each channel has a dedicated output FIFO that is filled when the data path writes a sample to the output FIFO. The ASRC keeps tracks of the number of writes to the output FIFO and the number of reads that occur from the VBUS (by a processor, EDMA, or DMA). The outfifo interrupt will fire whenever the amount of available data matches the threshold set in the ASRC_SRCFFCTRL_0[23:16] OUTFIFO_THRESHOLD register field. Status for each FIFO can be checked in the ASRC_OFIRQENSTS status register. Once an OUTFIFO interrupt is fired, next interrupt will be generated only after OUTFIFO_THRESHOLD number of Audio RX Sync pulses has occured for that particular channel.

When the CPU is used to transfer data from ASRC, whenever an outfifo_intr is triggered, SW needs to read the ASRC_OFIRQENSTS status register and needs to determine which channel needs to be serviced. Based on interrupt status register software can trigger DMA to initiate transactions to channels. Data transfer will be in the same manner as described in *ASRC Stream Mode Audio Data Read for Channel N* with DMA triggered by software instead of outfifo_evt event. After servicing the channel SW needs to clear the interrupt for that particular channel.

12.1.1.2.7.3 Group Interrupts

The group interrupt is used to allow multiple stream DMA events to be tied together. That is, multiple channel inputs and outputs to be managed using a single DMA. A group is configured by writing to either the ASRC_IGRPSEL_0 to ASRC_IGRPSEL_3 registers for input groups, or the ASRC_OGRPSEL_0 to ASRC_OGRPSEL_3 registers for output groups. In the ASRC_IGRPSEL and ASRC_OGRPSEL registers there is a bit field for each channel. The group is determined by all the channels that have a 1 in them. When all of the selected streams in the input or output group are above the threshold, the corresponding group interrupt will fire. Once an ingrp_intr interrupt is fired, next interrupt will be generated only after INFIFO_THRESHOLD number of Audio RX Sync pulses has occured for all the channels of that group. Once an outgrp_intr interrupt is fired, next interrupt will be generated only after OUTFIFO_THRESHOLD number of Audio RX Sync pulses has occured for all the channels of that group.

When the CPU is used to transfer data to ASRC, whenever an ingrp_intr is triggered, SW needs to read the ASRC_IGIRQENSTS status register and needs to determine which group channels needs to be serviced. Based on interrupt status register, software can trigger DMA to initiate transactions to channels of that particular group. Data transfer will be in the same manner as described in *ASRC Group Mode Audio Data Write for Channels of Group N* with DMA triggered by software instead of ingrp_evt event. After servicing the channel, SW needs to clear the interrupt for that particular group.

When the CPU is used to transfer data from ASRC, whenever there is outgrp_intr is triggered, SW needs to read the ASRC_OGIRQENSTS status register and needs to determine which group channels needs to be serviced. Based on interrupt status register, software can trigger DMA to initiate transactions to channels of that particular group. Data transfer will be in the same manner as described in *ASRC Group Mode Audio Data Read from Channels of Group N* with DMA triggered by software instead of outgrp_evt event. After servicing the channel, SW needs to clear the interrupt for that particular group.

12.1.1.2.7.4 Error Interrupts

The error interrupt is used to signal a FIFO error condition. Below is a list of events that will cause the error interrupt to fire:

- Input FIFO overflow / underflow
- Output FIFO overflow / underflow

Overflow and underflow status for each SRC channel can be read through the ASRC_SRCFFCTRL_0 register. Clearing ERROR_INTR also clears the overflow/underflow status for that channel.

12.1.1.2.8 ASRC DMA Events and Data Transfer Model

The ASRC can be configured to generate individual EDMA events to initiate EDMA transfers for fillimg the input FIFOs in each operating mode, Group or Stream. Similarly, the ASRC is able to generate individual EDMA events to initiate EDMA transfers to empty the output FIFOs for each operating mode. Each event is triggered when the specific Group or Stream mode FIFO threshold condition has been met. The event generation is enabled on a group and stream basis. There are 4 group input events and 4 group output events. There are 16 stream input events and 8 stream output events (one for each input and output channel). The group and stream mode events are enabled when setting up the Stream or Group ASRC configuration

ASRC has individual event signals that generate pulse on ASRC external ports to trigger a DMA transaction. There are dedicated DMA events for audio samples write and read, respectively. Each channel/stream and each group has separate DMA event at the ASRC module boundary. The total number of events is determined by the number of channels and the number of groups. These events can be used to transfer the fixed block of data to ASRC.

- In group mode, where more than one channels are part of one particular group, ingrp_evt and outgrp_evt for that group need to be used, and infifo_evt and outfifo_evt need to be ignored.
- In stream mode, where channel is working independently, infifo_evt and outfifo_evt for that channel need to be used.

ASRC DMA Events describes the DMA events, and provides mapping to ASRC boundary signals covered in *ASRC Hardware Requests*.

Table 12-8. ASRC DMA Events

DMA Event	Mapped to ASRC Boundary Signal	Number of Events	Description
infifo_evt[15:0]	ASRC_STREAM_IN[15:0]	16	The event will send out a pulse when the threshold for the input FIFO has fallen below the configured level. Once an INFIFO event is fired, next event will be generated only after ASRC_SRCFFCTRL_0[7:0] INFIFO_THRESHOLD number of Audio RX Sync pulses for that particular channel.
outfifo_evt[15:0]	ASRC_STREAM_OUT[15:0]	16	The event will send out a pulse when the threshold for the output FIFO has reached the configured level. Once an OUTFIFO event is fired, next event will be generated only after ASRC_SRCFFCTRL_0[23:16] OUTFIFO_THRESHOLD number of Audio RX Sync pulses for that particular channel.
ingrp_evt[3:0]	ASRC_GROUP_IN[3:0]	4	The event will send out a pulse when all input FIFOs in the configured group has fallen below their configured level. Once an INGROUP event is fired, next event will be generated only after INFIFO_THRESHOLD number of Audio RX Sync pulses for all the channels of that group.
outgrp_evt[3:0]	ASRC_GROUP_OUT[3:0]	4	The event will send out a pulse when all output FIFOs in the configured group has reached their configured level. Once an OUTGROUP event is fired, next event will be generated only after OUTFIFO_THRESHOLD number of Audio RX Sync pulses for all the channels of that group.

12.1.1.2.8.1 Stream Mode DMA Events

In stream mode, data transfer for channel number N is shown in A*SRC Stream Mode Audio Data Write for Channel N* and *ASRC Stream Mode AUdio Data Read for Channel N*.

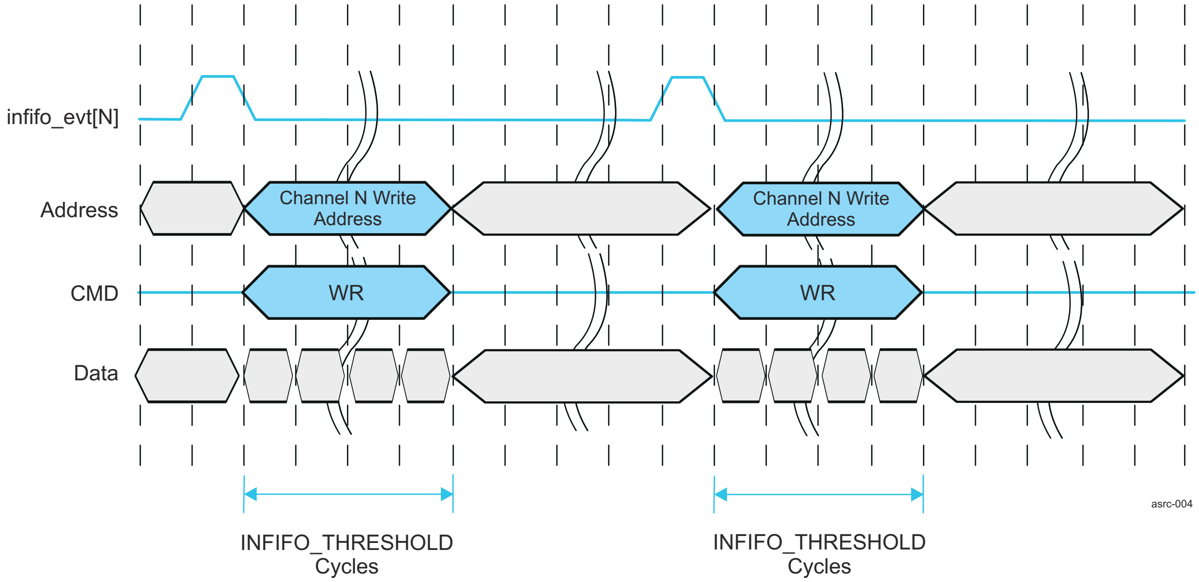


Figure 12-4. ASRC Stream Mode Audio Data Write for Channel N

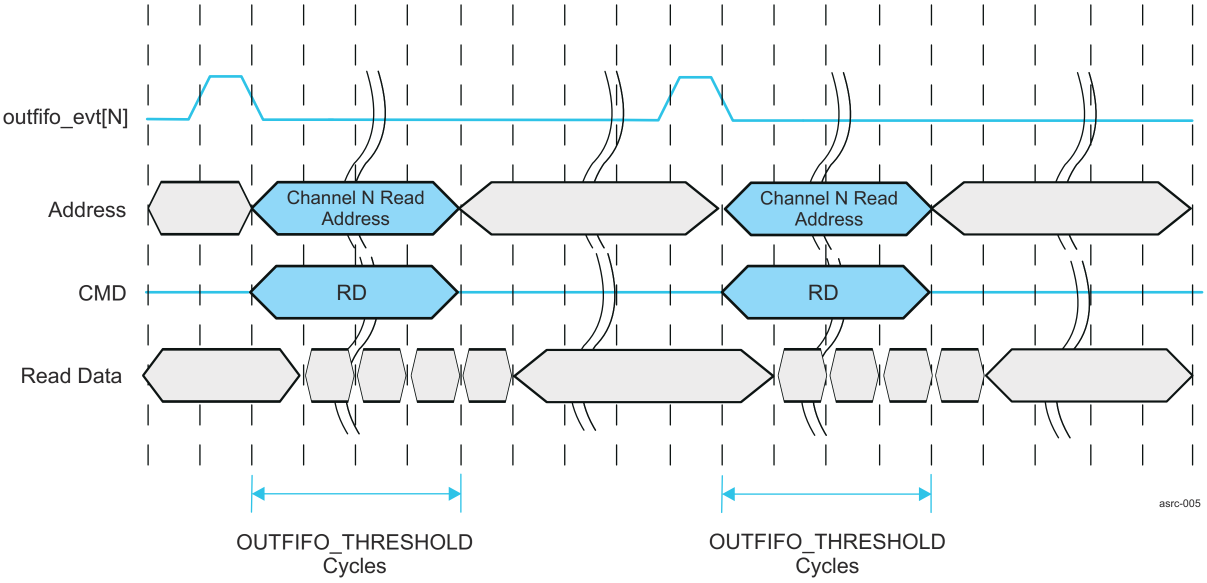


Figure 12-5. ASRC Stream Mode Audio Data Read for Channel N

It is not required for the device EDMA to service an event in one cycle, as it may be busy with other transfers also. If EDMA channel is shared between more than one channels, then it can queue the events and service whenever it has the resources available.

For each infifo_evt[N], that is infifo event for channel N, ASRC ensures that there is space available for at least INFIFO_THRESHOLD number of samples in the INFIFO of that channel. This INFIFO_THRESHOLD value can be set in ASRC_SRCFFCTRL_0[7:0] INFIFO_THRESHOLD register bitfield of that channel.

For each outfifo_evt[N], that is outfifo event for channel N, ASRC ensures that there is at least OUTFIFO_THRESHOLD number of samples available in OUTFIFO of that channel. This OUTFIFO_THRESHOLD value can be set in ASRC_SRCFFCTRL_0[23:16] OUTFIFO_THRESHOLD register bitfield of that channel.

12.1.1.2.8.2 Group Mode DMA Events

In group mode data transfer for all the channels of group number N is shown in *ASRC Group Mode Audio Data Write for Channels of Group N* and *ASRC Group Mode Audio Data Read from Channels of Group N*.

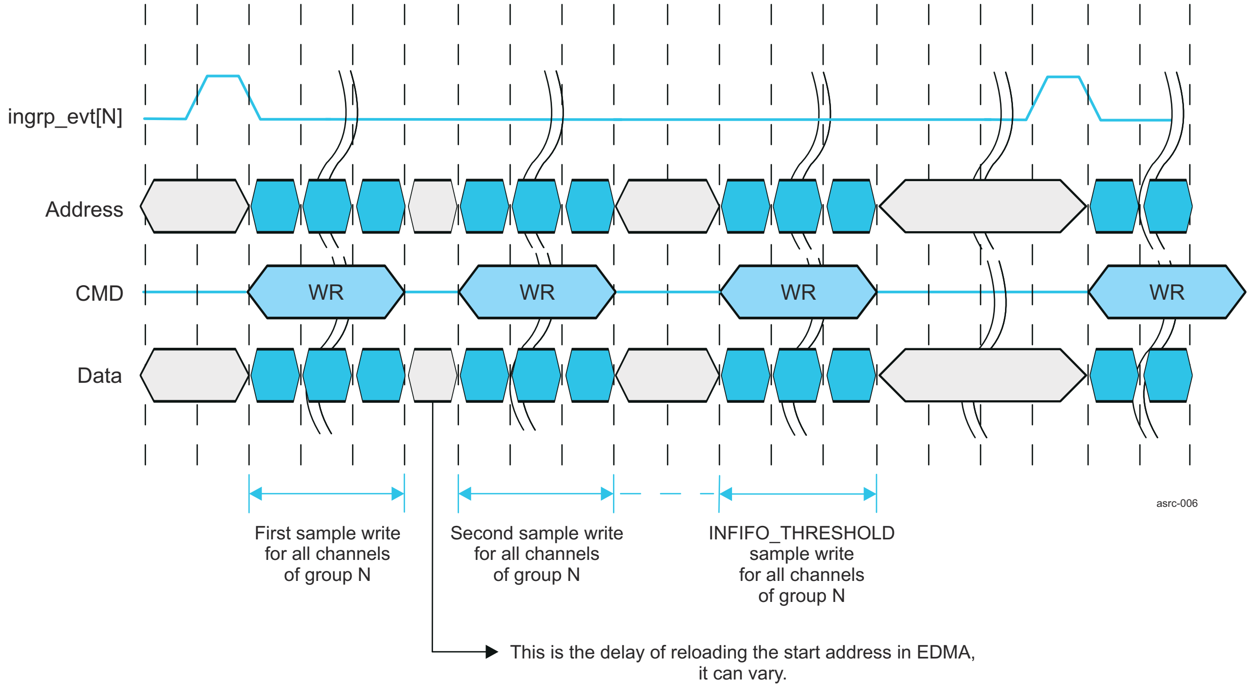


Figure 12-6. ASRC Group Mode Audio Data Write for Channels of Group N

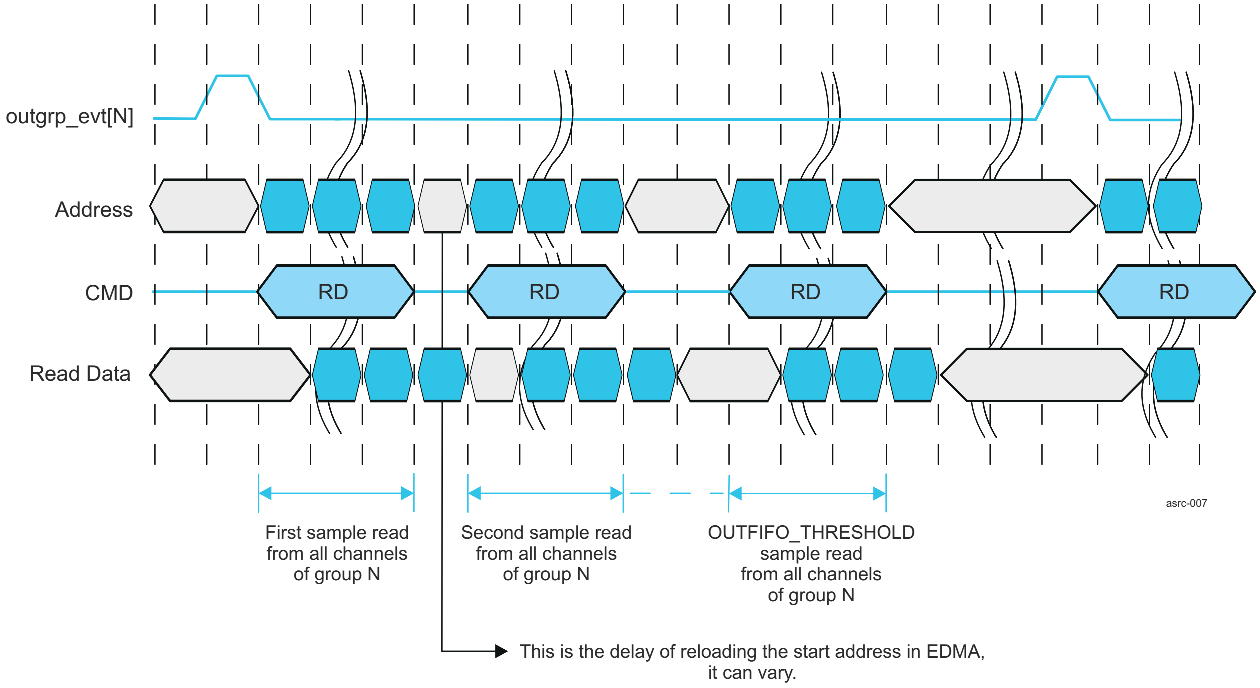


Figure 12-7. ASRC Group Mode Audio Data Read from Channels of Group N

It is not required for the device EDMA to service an event in one cycle as it may be busy with other transfers also. If EDMA channel is shared between more than one channels or groups, then it can queue the events and service whenever it has the resources available.

For each ingrp_evt[N], that is infifo event for group N, ASRC ensures that there is space available for at least INFIFO_THRESHOLD number of samples in the INFIFO of all the channels of that group. This INFIFO_THRESHOLD value can be set in ASRC_GFFCTRL_0[7:0] INFIFO_THRESHOLD register bitfield of that particular group. In this mode one sample is written in each of the channels of that group. The EDMA will update the adress to follow the channel number sequence of that group. This step is repeated

INFIFO_THRESHOLD number of times to fill in INFIFO_THRESHOLD number of samples in each channel of that particular group.

For each outgrp_evt[N], that is outfifo event for group N, ASRC ensures that there is at least OUTFIFO_THRESHOLD number of samples available in OUTFIFO of all the channels of that group. This OUTFIFO_THRESHOLD value can be set in ASRC_GFFCTRL_0[23:16] OUTFIFO_THRESHOLD register bitfield of that particular group. In this mode one sample is read from all the channels of that group. The EDMA will update the address to follow the channel number sequence of that group. This step is repeated OUTFIFO_THRESHOLD number of times to drain OUTFIFO_THRESHOLD number of samples from each channel of that particular group.

12.1.1.2.9 ASRC Group Mode Configuration

Note

Interleaving of audio data must be handled outside the ASRC module.

The ASRC supports 4 input and 4 output groups that can be configured. Each group can be composed of 1 to 16 channels. A stereo pair can only be assigned to one group. In group mode, a single INFIFO interrupt/event is triggered based upon status of Input FIFO status of all channels of the group. Similarly, a single OUTFIFO interrupt/event is triggered based upon status of Output FIFO status of all channels of the group. Each group can be controlled by separate EDMA.

ASRC Group Mode Example shows and an example for group mode where all four input channels of SRC0 and SRC1 are part of input Clock Zone 1 and all four output channels are part of output Clock Zone 2.

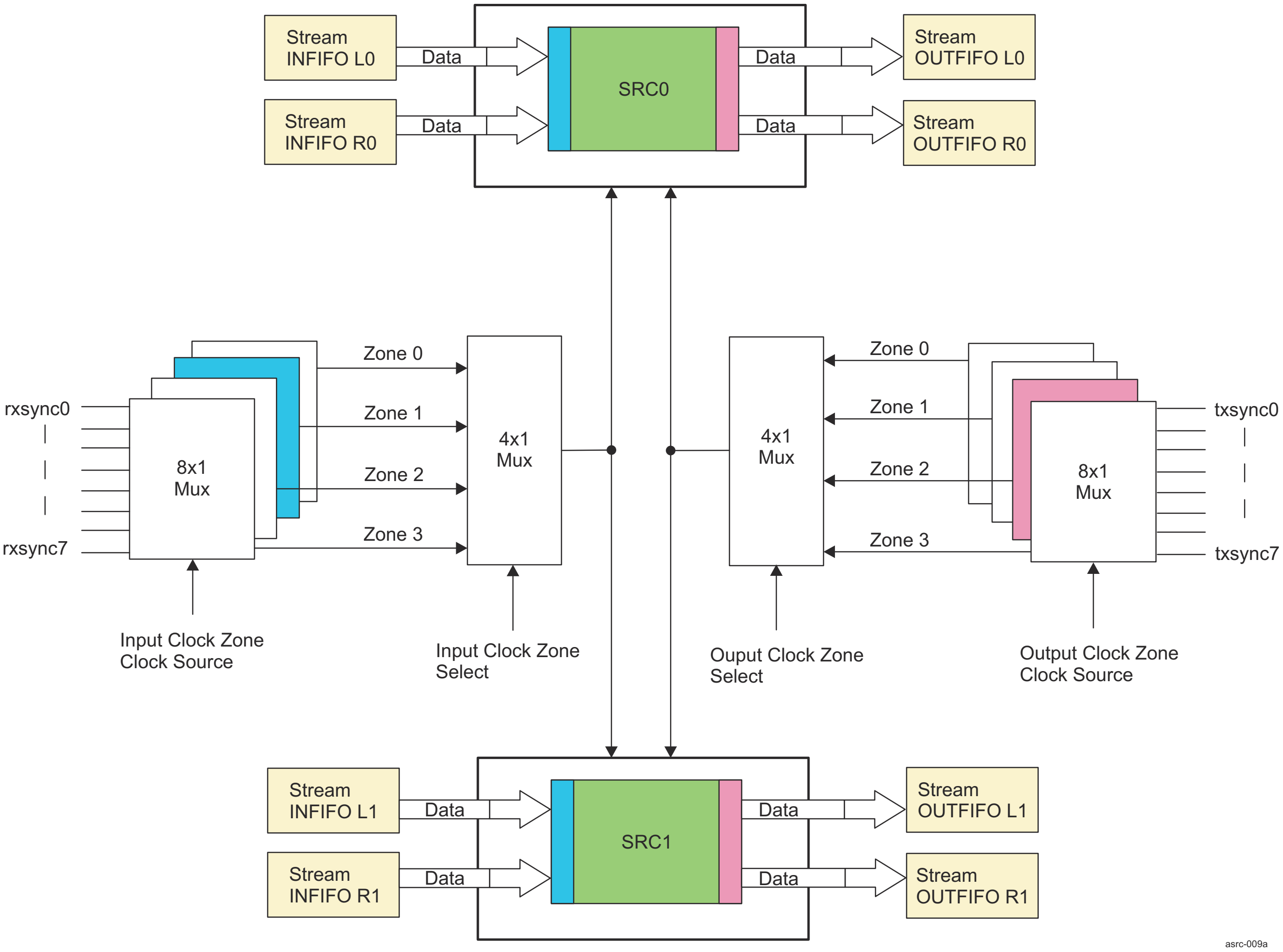


Figure 12-8. ASRC Group Mode Example

The basic functionality of the ASRC follows the steps below for setting up a single group. For more details on programming model, refer to *Group Mode Configuration Sequence*.

- Configure the Input and Output Clock Zone inputs to use one of the 8 possible input and output clock sources.
- Set the input and output channels.
- Configure INFIFO threshold and OUTFIFO threshold values.
- Configure Input and Output Word Length.
- Configure other conversion settings like de-emphasis, group delay, direct down conversion, output dither enable, and mute.
- Enable the conversion by enabling events or interrupts.

At this point, the ASRC automation starts. The ASRC clock zone input and output rate estimators will start estimation of the input and output sample rates. Once the estimation has settled, the ASRC will initiate input and output event or interrupt generation based upon the input and output FIFO status.

12.1.1.2.9.1 Group Mode Configuration Sequence

1. Configure Clock Zones:
   a. Program Input Clock Zone Clock Source and Loop Setup:
      - ASRC_ICKZCTRL_0[3-0] INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT register bitfield
      - ASRC_ICKZCTRL_0[16-9] LOOP_SETUP register bitfield
   b. Program Output Clock Zone Clock Source and Loop Setup
      - ASRC_OCKZCTRL_0[3-0] OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT register bitfield
      - ASRC_OCKZCTRL_0[16-9] LOOP_SETUP register bitfield
2. Program Clock Zone 0 divider and Clock Zone 1 divider values (optional step, required if ASRC module dividers are being used):
   - ASRC_ICKDIV[13-0] CLOCK_ZONE0_DIVIDE
   - ASRC_ICKDIV[29-16] CLOCK_ZONE1_DIVIDE
   - ASRC_OCKDIV[13-0] CLOCK_ZONE0_DIVIDE
   - ASRC_OCKDIV[29-16] CLOCK_ZONE1_DIVIDE
3. Program Clock Zone 0 divider enable and Clock Zone 1 divider enable (optional step, required if ASRC module dividers are being used):
   - ASRC_ICKDIV[14] CLOCK_ZONE0_DIVIDE_EN
   - ASRC_ICKDIV[30] CLOCK_ZONE1_DIVIDE_EN
   - ASRC_OCKDIV[14] CLOCK_ZONE0_DIVIDE_EN
   - ASRC_OCKDIV[30] CLOCK_ZONE1_DIVIDE_EN
4. Program Input Group and Output Group Select Registers (select channels):
   - ASRC_IGRPSEL_0 to ASRC_IGRPSEL_3[...] CHANNEL_#_GROUP_ENABLE
   - ASRC_OGRPSEL_0 to ASRC_OGRPSEL_3[...] CHANNEL_#_GROUP_ENABLE
5. Program INFIFO threshold and OUTFIFO threshold values:
   - ASRC_GFFCTRL_0[7-0] INFIFO_THRESHOLD
   - ASRC_GFFCTRL_0[23-16] OUTFIFO_THRESHOLD
6. Program Output Word Length, Group Delay, De-emphasis Mode, Attenuation, Direct Down Sample, Mute, Dither Enable, Output Clock Zone Select and Input Clock Zone Select:
   - ASRC_GSRCCTRL_0[29-28] OUTPUT_WORD_LENGTH
   - ASRC_GSRCCTRL_0[27-26] GROUP_DELAY
   - ASRC_GSRCCTRL_0[25-24] DE_EMPHASIS_MODE
   - ASRC_GSRCCTRL_0[23-16] ATTENUATION
   - ASRC_GSRCCTRL_0[10] DIRECT_DOWN_SAMPLE
   - ASRC_GSRCCTRL_0[9] MUTE
   - ASRC_GSRCCTRL_0[8] DITHER_ENABLE
   - ASRC_GSRCCTRL_0[7-6] INPUT_WORD_LENGTH
   - ASRC_GSRCCTRL_0[5-3] OUTPUT_CLOCK_ZONE_SELECT
   - ASRC_GSRCCTRL_0[2-0] INPUT_CLOCK_ZONE_SELECT
7. Program Data Alignment Disable:

  - ASRC_SYSCONFIG[1] DATA_FORMAT_DISABLE
8. Program Channel Enable (channel enable will be effective, only if that particular channel is the part of a that particular group):
   - ASRC_GSRCCTRL_0[31-30] CHANNEL_ENABLE
9. Program DMA transfers:
   - Once the INGROUP_EVT event is triggered, a maximum block of ASRC_GFFCTRL_0[7-0] INFIFO_THRESHOLD audio samples can be written to the data register of each channel of that group. Once the OUTGROUP_EVT event is triggered, ASRC_GFFCTRL_0[23-16] OUTFIFO_THRESHOLD samples can be read from OUTPUT FIFO DATA registers (ASRC_GOFDATAL_0 and ASRC_GOFDATAR_0) of channel in the group. Events will not be triggered until Input Clock Recovery Loop and Output Clock Recovery Loop are settled. For this SW must check the status of bit [8] SETTLE in ASRC_ICKZCTRL_0 and ASRC_OCKZCTRL_0 registers, respectively.

12.1.1.2.10 ASRC Stream Mode Configuration

Note

Interleaving of audio data must be handled outside the ASRC module.

In stream mode each stereo stream / channel can be controlled by a separate EDMA. Both channels of one SRC must be in same clock zone. User can process the audio samples by putting the sample in appropriate channel data register. In stream mode the individual channel FIFO interrupt / interrupts are not consolidated. In stream mode, a stereo pair is individually assigned to an input and output clock zone. A stereo pair is assigned even if only one channel is active. A stereo pair can only be part of one clock zone.

ASRC Stream Mode Example shows and an example for stream mode where the two input channels of SRC0 (which are part of input Clock Zone 0) are moved to output Clock Zone 1.

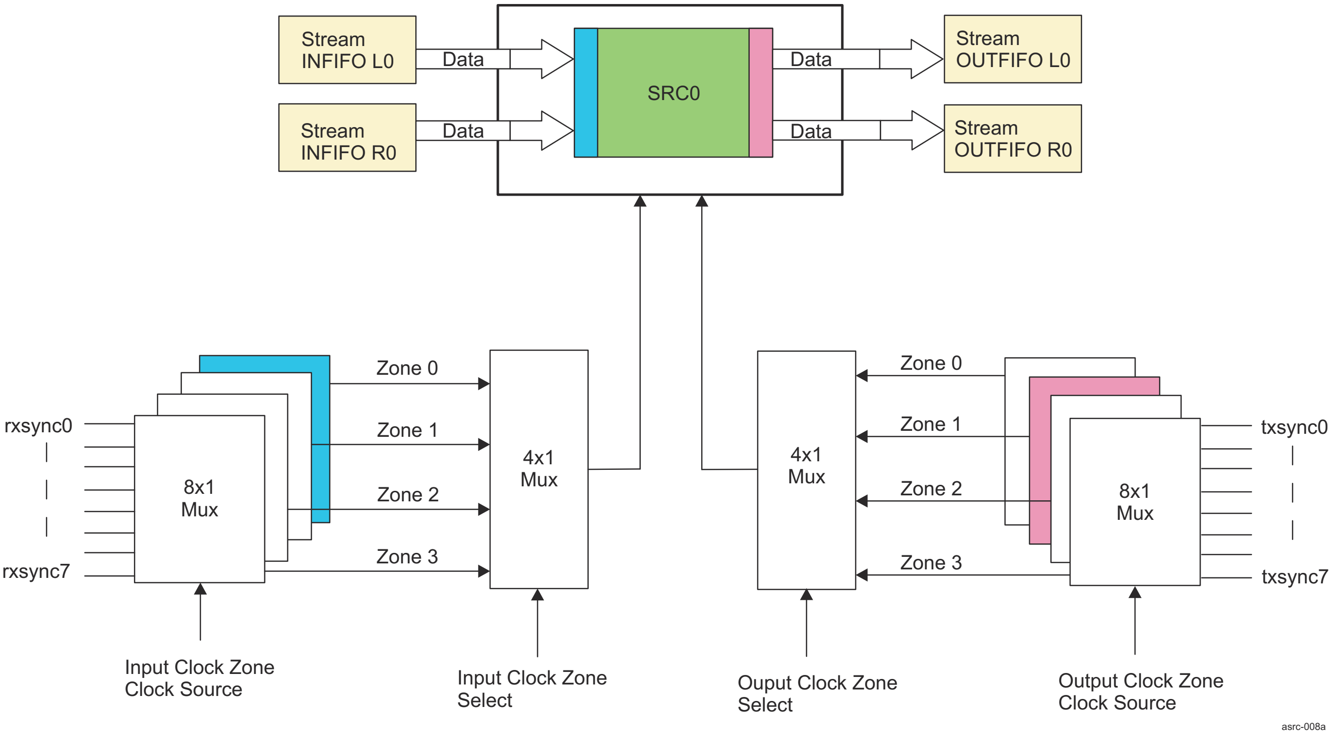


Figure 12-9. ASRC Stream Mode Example

The basic functionality of the ASRC in stream mode follows the steps below for setting up a single channel. For more details on programming model, refer to *Stream Mode Configuration Sequence*.

- Configure the Input and Output Clock Zone inputs to use one of the 8 possible input and output clock sources.

- Set the input and output channels.
- Configure INFIFO threshold and OUTFIFO threshold values.
- Configure Input and Output Word Length.
- Configure other conversion settings like de-emphasis, group delay, direct down conversion, output dither enable, and mute.
- Enable the conversion by enabling events or interrupts.

At this point, the ASRC automation starts. The ASRC clock zone input and output rate estimators will start estimation of the input and output sample rates. Once the estimation has settled, the ASRC will initiate input and output event or interrupt generation based upon the input and output FIFO status.

12.1.1.2.10.1 Stream Mode Configuration Sequence

1. Configure Clock Zones:
   a. Program Input Clock Zone Clock Source and Loop Setup:
      - ASRC_ICKZCTRL_0[3-0] INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT register bitfield
      - ASRC_ICKZCTRL_0[16-9] LOOP_SETUP register bitfield
   b. Program Output Clock Zone Clock Source and Loop Setup
      - ASRC_OCKZCTRL_0[3-0] OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT register bitfield
      - ASRC_OCKZCTRL_0[16-9] LOOP_SETUP register bitfield
2. Program Clock Zone 0 divider and Clock Zone 1 divider values (optional step, required if ASRC module dividers are being used):
   - ASRC_ICKDIV[13-0] CLOCK_ZONE0_DIVIDE
   - ASRC_ICKDIV[29-16] CLOCK_ZONE1_DIVIDE
   - ASRC_OCKDIV[13-0] CLOCK_ZONE0_DIVIDE
   - ASRC_OCKDIV[29-16] CLOCK_ZONE1_DIVIDE
3. Program Clock Zone 0 divider enable and Clock Zone 1 divider enable (optional step, required if ASRC module dividers are being used):
   - ASRC_ICKDIV[14] CLOCK_ZONE0_DIVIDE_EN
   - ASRC_ICKDIV[30] CLOCK_ZONE1_DIVIDE_EN
   - ASRC_OCKDIV[14] CLOCK_ZONE0_DIVIDE_EN
   - ASRC_OCKDIV[30] CLOCK_ZONE1_DIVIDE_EN
4. Program INFIFO threshold and OUTFIFO threshold values:
   - ASRC_SRCFFCTRL_0[7-0] INFIFO_THRESHOLD
   - ASRC_SRCFFCTRL_0[23-16] OUTFIFO_THRESHOLD
5. Program Output Word Length, Group Delay, De-emphasis Mode, Attenuation, Direct Down Sample, Mute, Dither Enable, Output Clock Zone Select and Input Clock Zone Select:
   - ASRC_SRCCTRL_0[29-28] OUTPUT_WORD_LENGTH
   - ASRC_SRCCTRL_0[27-26] GROUP_DELAY
   - ASRC_SRCCTRL_0[25-24] DE_EMPHASIS_MODE
   - ASRC_SRCCTRL_0[23-16] ATTENUATION
   - ASRC_SRCCTRL_0[10] DIRECT_DOWN_SAMPLE
   - ASRC_SRCCTRL_0[9] MUTE
   - ASRC_SRCCTRL_0[8] DITHER_ENABLE
   - ASRC_SRCCTRL_0[7-6] INPUT_WORD_LENGTH
   - ASRC_SRCCTRL_0[5-3] OUTPUT_CLOCK_ZONE_SELECT
   - ASRC_SRCCTRL_0[2-0] INPUT_CLOCK_ZONE_SELECT
6. Program Data Alignment Disable (optional step, if desired):
   - ASRC_SYSCONFIG[1] DATA_FORMAT_DISABLE
7. Program Channel Enable:
   - ASRC_SRCCTRL_0[31-30] CHANNEL_ENABLE
8. Program DMA transfers:
   - Once the INFIFO_EVT event is triggered, a maximum block of ASRC_SRCFFCTRL_0[7-0] INFIFO_THRESHOLD audio samples can be written to the data register. If OUTFIFO_EVT event is triggered, then ASRC_SRCFFCTRL_0[23-16] OUTFIFO_THRESHOLD samples can be read from output data register. Events will not be triggered until Input Clock Recovery Loop and Output Clock Recovery

Loop are settled. For this SW must check the status of [8] SETTLE bit in ASRC_ICKZCTRL_0 and ASRC_OCKZCTRL_0 registers, respectively.

The typical time that for an ASRC clock rate estimator to settle is proportionate to the clock rate that is input to the rate estimator. The typical setting time in ms is approximately 8850 / sample rate in kHz. A 192 kHz clock will typically settle in 46 ms.

12.1.1.2.11 ASRC Programming Ranges and Restrictions

The following programming ranges and restrictions are valid:

- The programmed values of [7-0] INFIFO_THRESHOLD and [23-16] OUTFIFO_THRESHOLD register bitfields should be within 1-32 range. This applies to ASRC_SRCFFCTRL_0 and ASRC_GFFCTRL_0 registers.
- Only the following settings for [16-9] LOOP_SETUP bit-field are allowed: 8’h00, 8’h40, 8’h80, 8’hC0. This applies to SRC_ICKZCTRL_0 and ASRC_OCKZCTRL_0 registers.
- ASRC_IGRPSEL_0 to ASRC_IGRPSEL_3 and ASRC_OGRPSEL_0 to ASRC_OGRPSEL_3 registers should have same channels enabled for group number 0 to 3.

12.1.1.2.12 ASRC Registers Shadowing

ASRC module has no shadowing of registers. A stream must be disabled and a new stream enabled to change an active stream.

12.1.2 Multichannel Audio Serial Port (MCASP)

This section describes the Multichannel Audio Serial Port (MCASP).

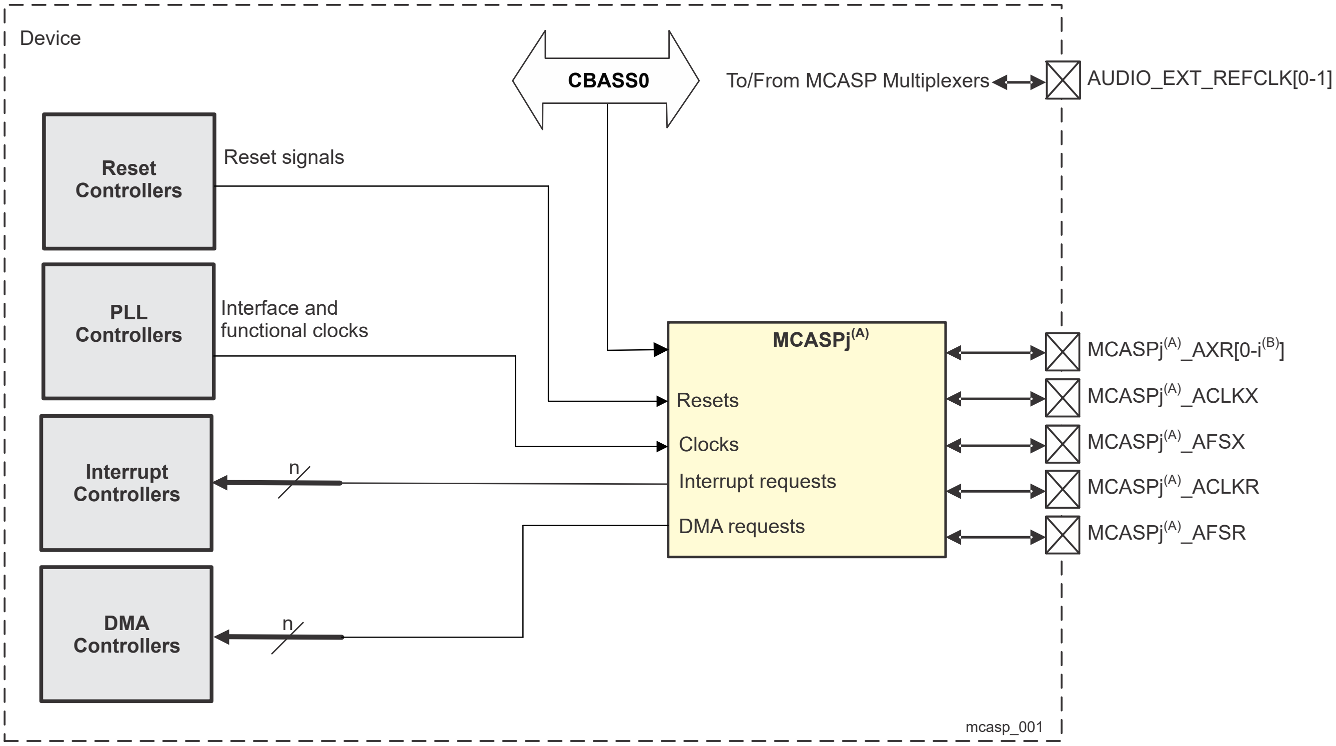
12.1.2.1 MCASP Overview

This section introduces the Multichannel Audio Serial Port (MCASP) module and describes its main functions and connections in the device.

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

Figure 12-10 shows the MCASP modules overview.



A. j represents a valid instance of MCASP in a domain

B. i represents the maximum number of MCASPj_AXR signals - 1.

Figure 12-10. MCASP Modules Overview

12.1.2.1.1 MCASP Features

Each MCASP module includes the following main features:

- Independent serializer for each AXRx channel of each MCASP module
- Clock stop request/acknowledge protocol
- A single 32-bit buffer per serializer for transmit and receive operations
- Interconnect interface port for CBASS0
- Two independent clock generator modules for transmit and receive (clocking flexibility allows the MCASP to receive and transmit at different rates. For example, the MCASP can receive data at 48 kHz, but output up-sampled data at 96 kHz or 192 kHz)

- Each MCASP module functional clock can be generated:
  - Internally (controller mode)
  - Supplied over MCASP serial interface (target mode)
  - Has a controllable functional clock divide ratio
- Independent transmit and receive modules, each includes:
  - Programmable clock and frame sync generator
  - TDM streams from 2 to 32, and 384 time slots
  - Support for time slot sizes of 8, 12, 16, 20, 24, 28, and 32 bits
  - Data formatter for bit manipulation
- Glueless connection to audio Analog-to-Digital Converters (ADC), Digital-to-Analog Converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components
- Wide variety of I2S and similar bit-stream format
- Integrated digital audio interface transmitter (DIT):
  - S/PDIF, IEC60958-1, AES-3 formats
  - Enhanced channel status/user data RAM
- 384-slot TDM with external digital audio interface receiver (DIR) device
  - For DIR reception, an external DIR receiver integrated circuit should be used with I2S output format and connected to the MCASP receive section
- Support for 2 × DMA requests (one per direction):
  - 1 level-sensitive transmit direct memory access (DMA) request common for all of the MCASP serializers
  - 1 level-sensitive receive direct memory access (DMA) request common for all of the MCASP serializers
  - All transmit DMA requests are mapped to the device DMA controllers
- One transmit interrupt request common for all serializers
- One receive interrupt request common for all serializers
- Each of the Rx and Tx interrupts is propagated to different host processors via the device Interrupts

Note

Because a serializer receive and transmit channels data is shared on the same MCASP data pin, user can choose to have either Tx or Rx function from a serializer, not both at the same time.

Note

Some features may not be available. See *Module Integration* for more information.

12.1.2.1.2 Unsupported Features

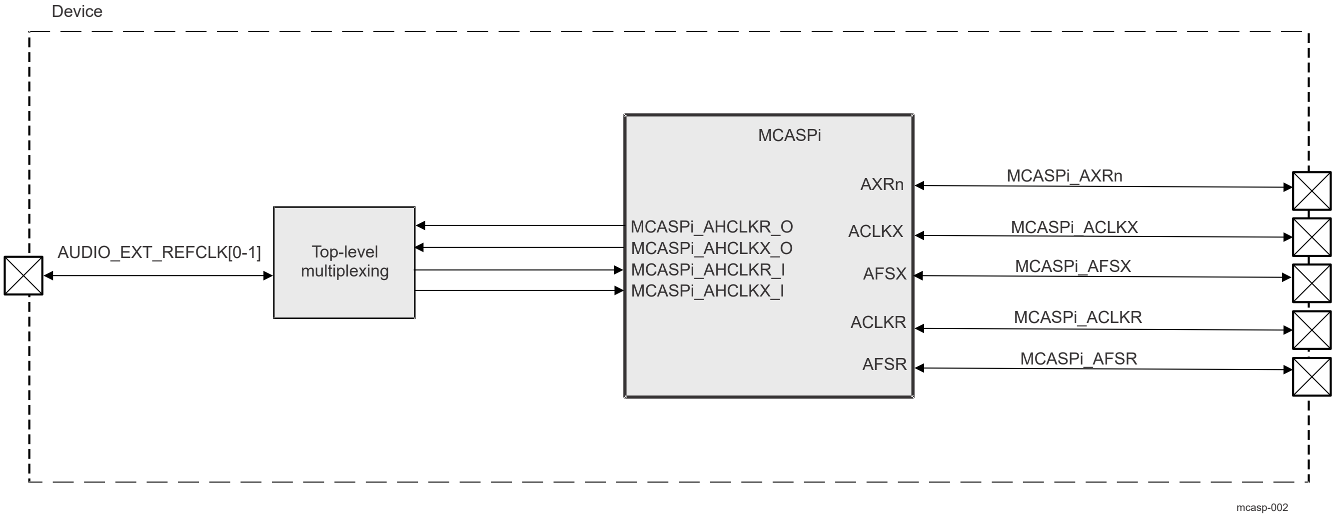
See the *Module Integration* section for information about unsupported features.

12.1.2.2 MCASP Environment

This section describes the MCASP application fields from an environment point of view (external connections). This section also lists the possible interfaces and describes the protocol and data format used in each case.

12.1.2.2.1 MCASP Signals

Figure 12-11 shows all of the MCASP interface signals.



Note

i represents a MCASP instance. See the device datasheet for available domains and MCASP instances.

n represents a AXR signal from a MCASP instance. See the device datasheet for available domains and MCASP instances.

Figure 12-11. MCASP Interface Signals

Table 12-9 describes the MCASP I/O signals.

Table 12-9. MCASP I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
		MCASPi[3] module		
AXR0	MCASPi[3]_AXR0	I/O	Audio transmit/receive data - channel 0	HiZ
AXR1	MCASPi[3]_AXR1	I/O	Audio transmit/receive data - channel 1	HiZ
AXR2	MCASPi[3]_AXR2	I/O	Audio transmit/receive data - channel 2	HiZ
AXR3	MCASPi[3]_AXR3	I/O	Audio transmit/receive data - channel 3	HiZ
AXR4	MCASPi[3]_AXR4	I/O	Audio transmit/receive data - channel 4	HiZ
AXR5	MCASPi[3]_AXR5	I/O	Audio transmit/receive data - channel 5	HiZ
AXR6	MCASPi[3]_AXR6	I/O	Audio transmit/receive data - channel 6	HiZ
AXR7	MCASPi[3]_AXR7	I/O	Audio transmit/receive data - channel 7	HiZ
AXR8	MCASPi[3]_AXR8	I/O	Audio transmit/receive data - channel 8	HiZ
AXR9	MCASPi[3]_AXR9	I/O	Audio transmit/receive data - channel 9	HiZ
AXR10	MCASPi[3]_AXR10	I/O	Audio transmit/receive data - channel 10	HiZ
AXR11	MCASPi[3]_AXR11	I/O	Audio transmit/receive data - channel 11	HiZ
AXR12	MCASPi[3]_AXR12	I/O	Audio transmit/receive data - channel 12	HiZ
AXR13	MCASPi[3]_AXR13	I/O	Audio transmit/receive data - channel 13	HiZ
AXR14	MCASPi[3]_AXR14	I/O	Audio transmit/receive data - channel 14	HiZ

Table 12-9. MCASP I/O Signals (continued)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
AXR15	MCASPi[3]_AXR15	I/O	Audio transmit/receive data - channel 15	HiZ
ACLKX	MCASPi[3]_ACLKX	I/O	Transmit bit clock	HiZ
AFSX	MCASPi[3]_AFSX	I/O	Transmit frame synchronization	HiZ
ACLKR	MCASPi[3]_ACLKR	I/O	Receive bit clock	HiZ
AFSR	MCASPi[3]_AFSR	I/O	Receive frame synchronization	HiZ
MCASPi[3]_AHCLKX_I/O	AUDIO_EXT_REFCLK[0-1]	I/O	Transmit high-frequency controller clock. See *Module Integration*	HiZ
MCASPi[3]_AHCLKR_I/O	AUDIO_EXT_REFCLK[0-1]	I/O	Receive high-frequency controller clock. See *Module Integration*	HiZ

(1) I = Input; O = Output; I/O = Bidirectional
(2) HiZ = High Impedance
(3) i represents a MCASP instance. See the device datasheet for available domains and MCASP instances.

Note

MCASPi_AHCLKR_I/O and MCASPi_AHCLKX_I/O signals are multiplexed to AUDIO_EXT_REFCLK[0-1] device pins.

Note

For MCASPi_ACLKR_I/O, MCASPi_ACLKX_I/O, MCASPi_AHCLKR_I/O and MCASPi_AHCLKX_I/O signals to work properly, the RXACTIVE bit of the appropriate PADCFG_CTRL_MMR_CFG0_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

Note

A serializer AXR data pin is shared between the transmit and receive logic of that serializer. The direction of data is determined in the *MCASP_PDIR* register and the function (Tx or Rx) is selected in the corresponding serializer control register MCASP_SRCTLn (n = 0 to 15).

12.1.2.2.2 MCASP Protocols and Data Formats

12.1.2.2.2.1 Protocols Supported

The MCASP supports a wide variety of protocols:

- Transmit section supports:
  - Wide variety of I2S and similar bit-stream formats
  - TDM streams from 2 to 32 time slots
  - S/PDIF, IEC60958-1, AES-3 formats
- Receive section supports:
  - Wide variety of I2S and similar bit-stream formats
  - TDM streams from 2 to 32 time slots
  - TDM stream of 384 time slots specifically designed for easy interface to external digital interface receiver (DIR) device transmitting DIR frames to MCASP using the I2S protocol (one time slot for each DIR subframe)

The transmit and receive sections of the module may be individually programmed to support the following options on the basic serial protocol:

- Programmable clock and frame sync polarity (rising or falling edge): ACLKR/X, AFSR/X and AHCLKR/X_I/O
- Slot length (number of bits per time slot): 2, 4, 8, 12, 16, 20, 24, 28, 32 bits supported
- Word length (bits per word): 2, 4, 8, 12, 16, 20, 24, 28, 32 bits; always less than or equal to the time slot length
- First-bit data delay: 0, 1, 2 bit clocks
- Left/right alignment of word inside slot
- Bit order: MSB first or LSB first
- Bit mask/pad/rotate function
  - Automatically aligns data internally in either Q31 or integer formats
  - Automatically masks nonsignificant bits (sets to 0, 1, or extends value of another bit)

Note

In I2S mode, the transmit and receive sections can support simultaneous transfers on up to all serial data pins operating as 192 kHz stereo channels.

In DIT mode for MCASP, additional features of the transmitters are:

- Transmit-only mode 384 time slots (subframe) per frame
- Biphase encoded 3.3 V Output
- Channel status RAM (384 bits)
- User data RAM (384 bits)
- Support for consumer and professional applications
- Separate valid bit (V) for subframe A, B
- Stereo Support Only (Mono means send data 2 × via software)

In DIT mode, the transmitter can support a 192 kHz frame rate (stereo) on up to all serial data pins simultaneously (note that the internal bit clock for DIT runs two times faster than the equivalent bit clock for I2S mode, due to the need to generate Biphase Mark Encoded Data).

Note

The MCASP does NOT natively support DIR-mode reception (this is, receiving in the S/PDIF format). To allow this, the MCASP can use a DIR-input to I2S-output converter implemented by an external device (this is, external DIR component). To facilitate reception in this case, the TDM mode of MCASP receivers logic is extended to support a non-standard 384-slot TDM stream.

Note

An external transceiver must be connected to the MCASP port in the device to translate the electrical signals delivered by the MCASP (1.2 V or 1.8 V LVCMOS levels) to the electrical levels of the S/PDIF standard.

12.1.2.2.2.2 Definition of Terms

The serial bitstream transmitted or received by a MCASP serializer is a long sequence of 1s and 0s on an audio transmit/receive pins AXRn. However, the sequence has a hierarchical organization that can be described in terms of frames of data, slots, words, and bits.

A basic synchronous serial interface consists of three important components: clock, frame sync, and data. Figure 12-12 shows two of the three basic components: the clock signal (ACLKX/ACLKR) and the data signals AXRn. Figure 12-12 does not specify whether the clock is for transmit (ACLKX) or receive (ACLKR) because the definitions of terms apply to both receive and transmit interfaces. In operation, each transmitter and receiver uses the signals ACLKX and ACLKR as serial clock, respectively. Optionally, a receiver can use ACLKX as the serial clock when a transmitter and receiver (not from the same serializer) of the MCASP are configured to operate synchronously.

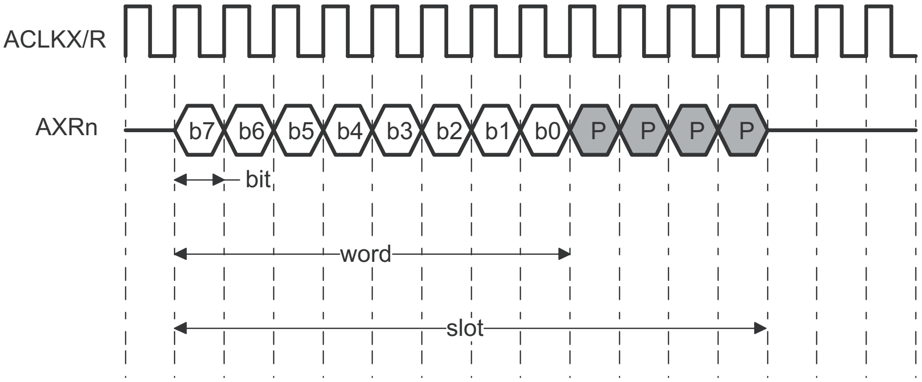
- Bit:

  A bit is the smallest entity in the serial data stream. The beginning and end of each bit is marked by an edge of the serial clock. The duration of a bit is a serial clock period. A '1' is represented by a logic high on AXRn pins for the entire duration of the bit. A 0 is represented by a logic low on an AXRn pin for the entire duration of the bit.
- Word:

  A word is a group of bits that make up the data being transferred between the MCASP and the external device. Figure 12-12 shows an 8-bit word.
- Slot:

  A slot consists of the bits that make up the word and can consist of additional bits used to pad the word to a convenient number of bits for the interface between the MCASP and the external device. In Figure 12-12, the audio data consists of only 8 bits of useful data (8-bit word), but it is padded with four 0s (12-bit slot) to satisfy the desired protocol in interfacing to an external device. Within a slot, the bits can be shifted out of the MCASP on an AXRn pin with either MSB or LSB first.

  When the word size is smaller than the slot size, the word can be aligned to the left of the slot (beginning) or to the right of the slot (end). The additional bits in the slot not belonging to the word can be padded with 0, 1, or with one of the bits (typically, the MSB or LSB) from the data word, this is, left-aligned words within a slot are terminated with padding bits and right-aligned words within a slot are preceded by padding bits to fit in the slot size. Figure 12-13 shows these options.



(1) b7:b0 - bits. Bits b7 to b0 form a word.

(2) P - pad bits. Bits b7 to b0, together with the 4 pad bits, form a slot.

(3) In this example, the data is transmitted MSB first, left-aligned.

mcasp-003

Figure 12-12. Definition of Bit, Word, and Slot

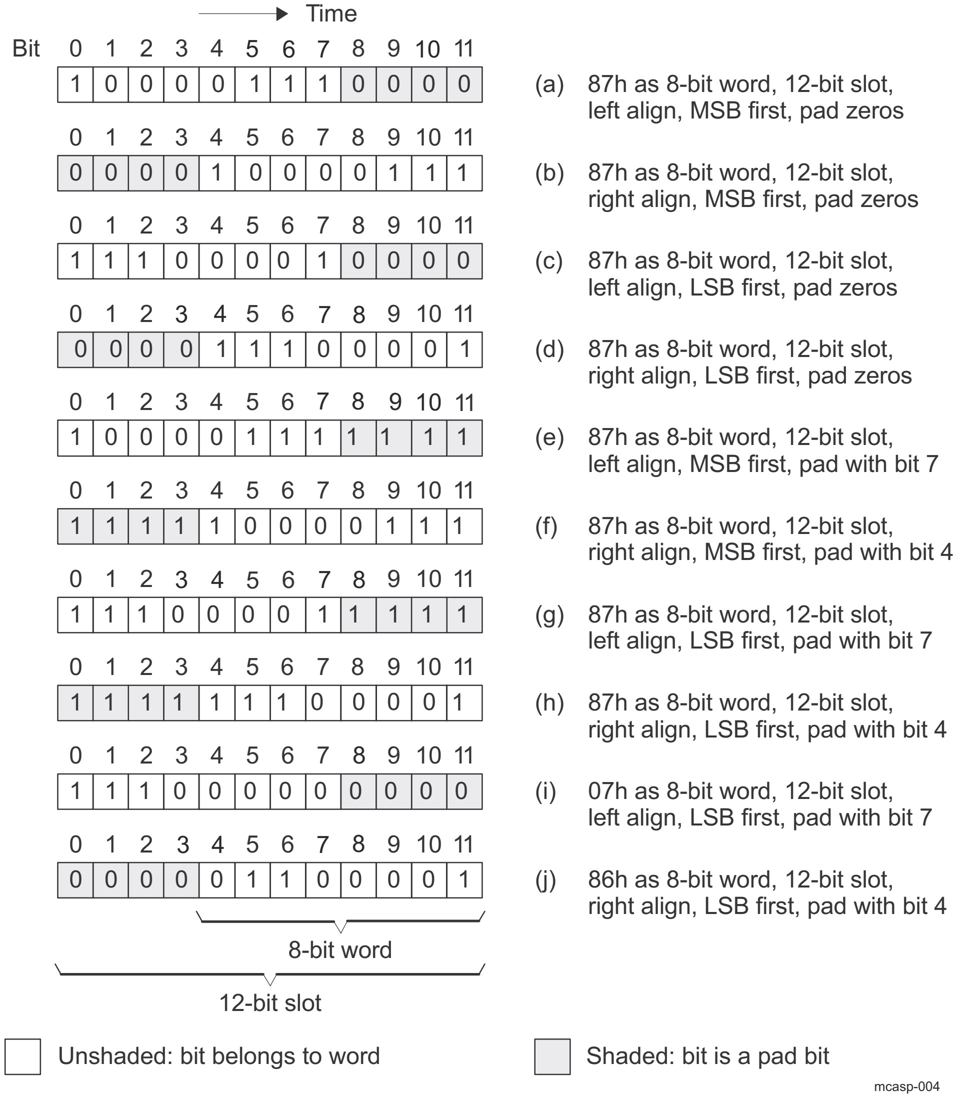


Figure 12-13. Bit Order and Word Alignment Within a Slot Examples

- Frame

  The third basic element of a synchronous serial interface is the frame synchronization signal, also referred to as frame sync in this chapter. A frame contains one or multiple slots, as determined by the desired protocol. Figure 12-14 shows an example frame of data and the frame definitions. In operation, the transmitter uses AFSX, and the receiver - AFSR signal. Figure 12-14 does NOT specify whether the frame sync (FS) is for transmit (AFSX) or receive (AFSR) because the definitions of terms apply to both receive and transmit interfaces. In operation, each transmitter/receiver uses AFSX/AFSR as a frame synchronization signal, respectively. Optionally, the receiver can use AFSX as the frame sync when the transmitter and receiver of the MCASP are configured to operate synchronously. This example shows two slots in a frame (I2S format) and a frame-sync (FS) duration of a slot length.

  This section shows only the generic definition of the frame sync. For more information about the frame-sync formats required for the transfer modes and protocols (TDM-mode and DIT-mode supported formats), see Section 12.1.2.2.2.3, *TDM Format* and Section 12.1.2.2.2.5, *S/PDIF-Coding Format*.

Note

All of the MCASP serializers share the same, device pad accessible, clock and frame signals, as follows:

– AHCLKX_I/O, ACLKX and AFSX for the transmitting section
– AHCLKR_I/O, ACLKR and AFSR for the receiving section

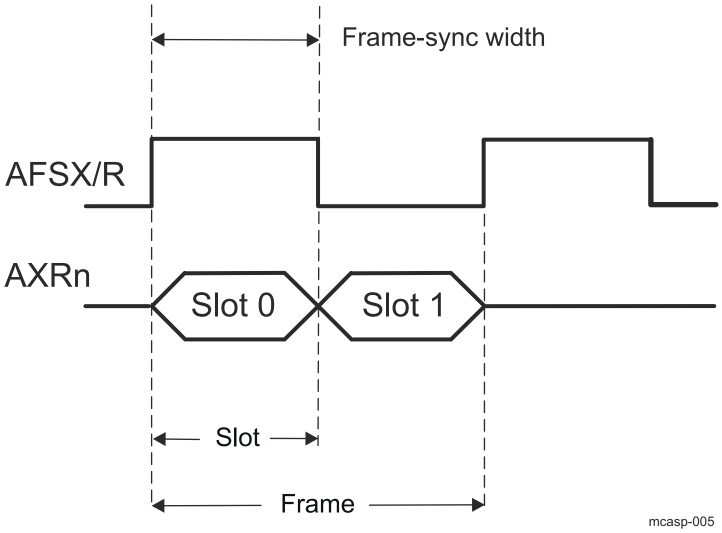


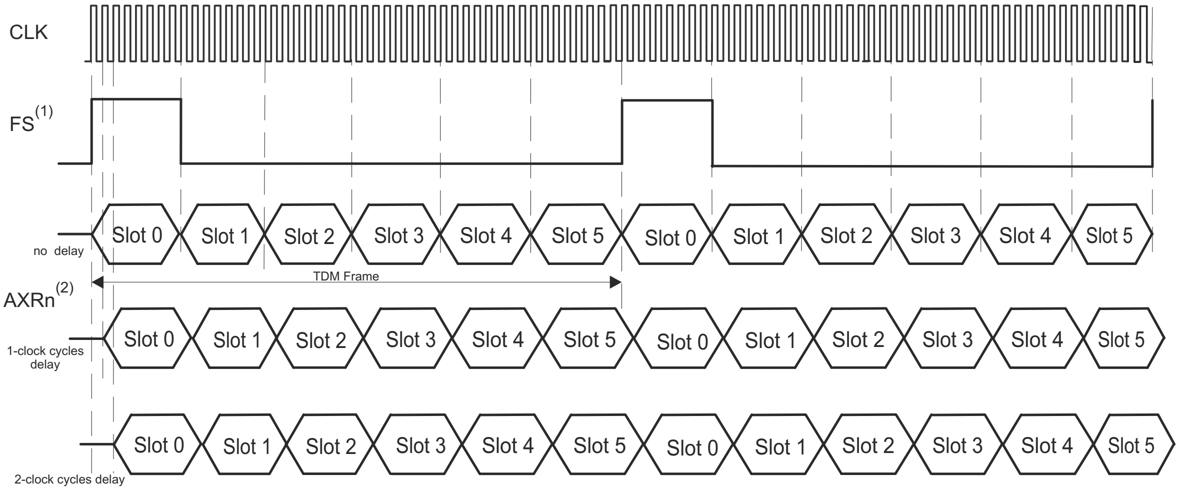
Figure 12-14. Definition of Frame and Frame-Sync Width

The following terms are used throughout this chapter:

- TDM: Time-division multiplexed. See Section 12.1.2.2.2.3, *TDM Format* for details on the TDM protocol.
- I2S: Inter-Integrated Sound protocol, commonly used on audio interfaces. The MCASP supports the I2S protocol as part of the TDM mode (when configured as a 2-slot frame).
- DIT: Digital audio interface transmit. The MCASP supports transmitting in S/PDIF format on each AXRn data pin.
- DIR: Digital audio interface receive. The MCASP does NOT natively support receiving in S/PDIF format on AXRn data pins and requires an external DIR-to-TDM or DIR-to-I2S converter chip for a DIR-frame reception.
- Slot or time slot: For DIT/DIR format, a MCASP time slot corresponds to a DIT/DIR subframe.

12.1.2.2.2.3 TDM Format

The TDM format is used to transfer data between the host CPU and one or more analog-to-digital converter (ADC), digital-to-analog converter (DAC), or S/PDIF receiver (DIR) devices. An example for a 6-slot (channel) TDM transmission on one MCASP data pin - AXRn is illustrated on Figure 12-15.



(1) - Frame sync duration of 1 slot - length is shown. A single bit - duration of FS is also supported

(2) - Slot 0 of AXRn stream is being offset with 0-, 1-, and 2- clock cycle delay from the frame sync, respectively.

mcasp-006

Figure 12-15. TDM Format - 6 channel example

The TDM format uses three signals in a basic synchronous serial interface: data (AXRn), clock (CLK) and frame sync (FS). The data signal present on AXRn pin is fully synchronous to the serial clock (ACLKX or ACLKR). The data bits are grouped into words and slots (see also Section 12.1.2.2.2.2), the latter being also refered to as the "time-slots" or "channels" in TDM terminology. A frame consists of multiple time-slots. Each TDM frame is marked by the frame sync signal (AFSX or AFSR). The TDM transfer is continuous and periodic, with no delays between slots.

Within a certain frame, the last bit of slot N is followed immediately on the next serial clock with the first bit of the next slot N+1. On the boundary between two adjacent TDM-frames, the last bit of the last slot from the frame M, is followed immediately on the next clock cycle with the first bit of the first slot from the next frame M+1. For MCASP, there is an option to offset the first bit of the first slot with a 0-,1- or 2-cycle delay from the frame sync signal.

The frame sync - AFSX/AFSR only marks the beginning of slot 0 and start of a new frame. Since it does not determine the boundaries of a slot, there is a requirement for a connected transmitter and receiver to agree on the number of transferred bits per slot.

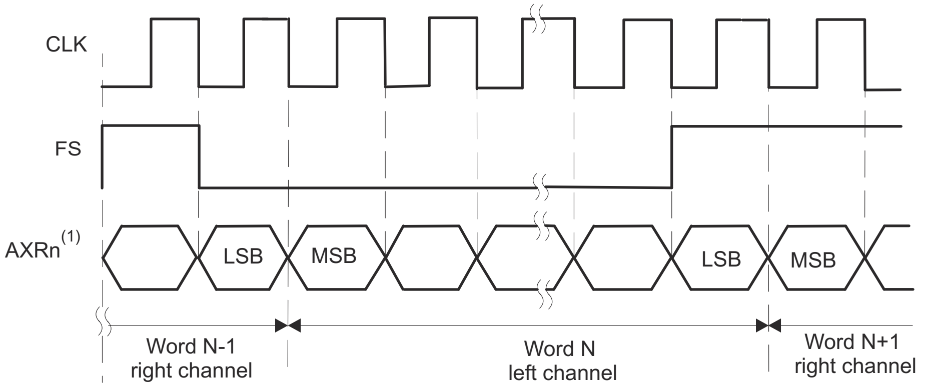
In a typical audio system involving MCASP module, a single TDM data frame is transferred during each sample period Ts of a data converter. The user has following choices to implement multiple channels:

- Use more data slots (on a price of higher speed serial clock) per frame transmitted/received on just one of the available MCASP data pins AXRn.
- Use less number of slots per TDM frame (requires a slower serial clock), making them available on several of the MCASP pins AXRn.

12.1.2.2.2.4 I2S Format

The TDM transfer mode of the MCASP supports the I2S format when frame is configured to have 2 slots. The I2S format is specifically designed to transfer a stereo channel (left and right) over a single data pin AXRn. The "Slots" are also commonly referred to as "channels". The frame width duration in the I2S format equals size of a slot. The frame signal is also referred to as "word select" in the I2S format.

The I2S protocol is illustrated on Figure 12-16.



(1) - The example shows I2S data MSB-first transmission with 1-clock cycle delay between FS and data MSB

mcasp-007

Figure 12-16. I2S Format Overview

12.1.2.2.2.5 S/PDIF Coding Format

The MCASP transmitter supports the S/PDIF format with 3.3 V biphase-mark encoded output. The S/PDIF format is supported by the DIT- transfer mode of the MCASP. This section briefly discusses the S/PDIF coding format.

Note

The DIR- reception of S/PDIF format frames is NOT natively supported from the device MCASP. For this purpose, an external DIR-to-TDM transfer mode adapter can be used between the remote device S/PDIF transmitter output and the MCASP TDM-only compatible receiver input.

12.1.2.2.2.5.1 Biphase-Mark Code

In S/PDIF format, the digital signal is coded using the biphase-mark code (BMC). For each serializer transmitter n, the clock, frame, and data are embedded in only one signal - the data signal AXRn. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin. These two logical states form a cell. The duration of the cell, which equals the duration of the data bit, is called a time interval. A logical 1 is represented by two transitions of the signal within a time interval, which corresponds to a cell with logical states 01 or 10. A logical 0 is represented by one transition within a time interval, which corresponds to a cell with logical states 00 or 11. In addition, the logical level at the start of a cell is inverted from the level at the end of the previous cell. Figure 12-17 and Table 12-10 show how data is encoded to the BMC format.

As shown in Figure 12-17, the clock frequency is twice the unencoded data bit rate. In addition, the clock is always programmed to 128 × f_S, where f_S is the sample rate (see Section 12.1.2.2.2.5.3, *Frame Format*, for details on how this clock rate is derived based on the S/PDIF format). The device receiving in S/PDIF format can recover the clock and frame information from the BMC signal.

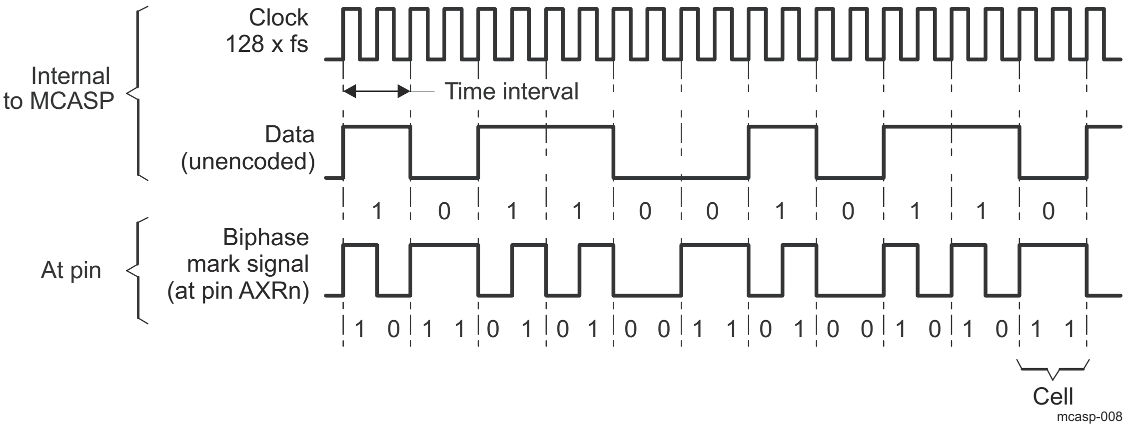


Figure 12-17. Biphase-Mark Code

Table 12-10. Biphase-Mark Encoder

Data (Unencoded)	Previous State at Pin AXRn	BMC-Encoded Cell Output at Pin AXRn
0	0	11
0	1	00
1	0	10
1	1	01

12.1.2.2.2.5.2 S/PDIF Subframe Format

Every audio sample transmitted in a subframe consists of 32 S/PDIF time intervals (or cells), numbered 0 to 31. Figure 12-18 shows a subframe.

- Time intervals 0–3 carry one of the three permitted preambles to signify the type of audio sample in the current subframe. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0 or 1 logical states in a row. See Table 12-11.
- Time intervals 4–27 carry the audio sample word in linear 2s-complement representation. The MSB is carried by time interval 27. When a 24-bit coding range is used, the LSB is in time interval 4. When a 20-bit coding range is used, time intervals 8-27 carry the audio sample word with the LSB in time interval 8. Time intervals 4–7 may be used for other applications and are designated auxiliary sample bits.
- If the source provides fewer bits than the interface allows (20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field can carry any other information.
- Time interval 28 carries the validity bit (V) associated with the main data field in the subframe.
- Time interval 29 carries the user data channel (U) associated with the main data field in the subframe.
- Time interval 30 carries the channel status information (C) associated with the main data field in the subframe. The channel status indicates if the data in the subframe is digital audio or some other type of data.
- Time interval 31 carries a parity bit (P) such that time intervals 4–31 carry an even number of 1s and an even number of 0s (even parity). As listed in Table 12-11, the preambles (time intervals 0–3) are also defined with even parity.

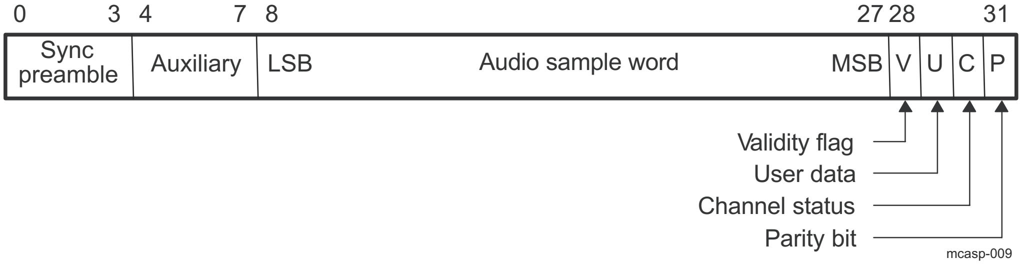


Figure 12-18. S/PDIF Subframe Format

As listed in Table 12-11, the MCASP DIT generates only one polarity of preambles, and it assumes the previous logical state is 0. This is because the MCASP assures an even-polarity encoding scheme when transmitting in DIT mode. If an underrun condition occurs, the DIT resynchronizes to the correct logic level on the AXRn pin before continuing with the next transmission.

Table 12-11. Preamble Codes

Preamble Code(1)	Previous Logical State	Logical States on pin AXRn(2)	Description
B (or Z)	0	1110 1000	Start of a block and subframe 1
M (or X)	0	1110 0010	Subframe 1
W (or Y)	0	1110 0100	Subframe 2

(1) Historically, preamble codes are referred to as B, M, and W. For use in professional applications, preambles are referred to as Z, X, and Y, respectively.
(2) The preamble is not BMC-encoded. Each logical state is synchronized to the serial clock. These eight logical states make up time slots (cells) 0 to 3 in the S/PDIF stream.

12.1.2.2.2.5.3 Frame Format

An S/PDIF frame is composed of two subframes (see Figure 12-19). For linear coded audio applications, the rate of frame transmission normally corresponds exactly to the source sampling frequency f_S. The S/PDIF format clock rate is therefore 128 × f_S (128 = 32 cells per subframe × 2 clocks per cell × 2 subframes per sample). For example, for an S/PDIF stream at a 192-kHz sampling frequency, the serial clock is 128 × 192 kHz = 24.58 MHZ.

In 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive subframes. Both subframes contain valid data (cell 28 validity bits for A- and B- channels, both set to '0'). The first subframe (left or A channel in stereophonic operation and primary channel in monophonic operation) normally starts with preamble M. However, the preamble of the first subframe changes to preamble B once every 192 frames to identify the start of the block structure used to organize the channel status information. The second subframe (right or B channel in stereophonic operation and secondary channel in monophonic operation) always starts with preamble W.

In single-channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried in the first subframe and may be duplicated in the second subframe. If the second subframe is not carrying duplicate data, cell 28 (validity bit) is set to logical 1.

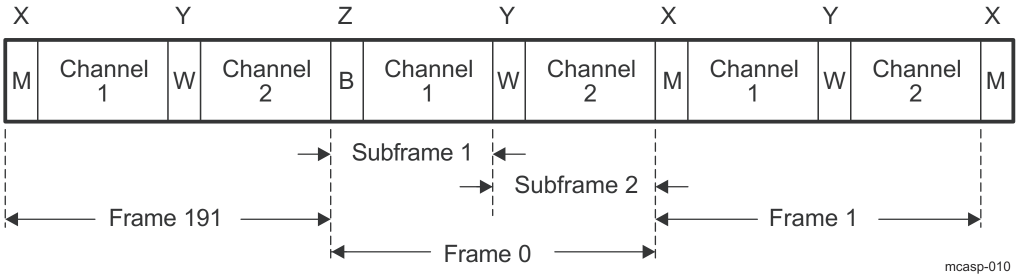


Figure 12-19. S/PDIF Frame Format

12.1.2.3 Integration

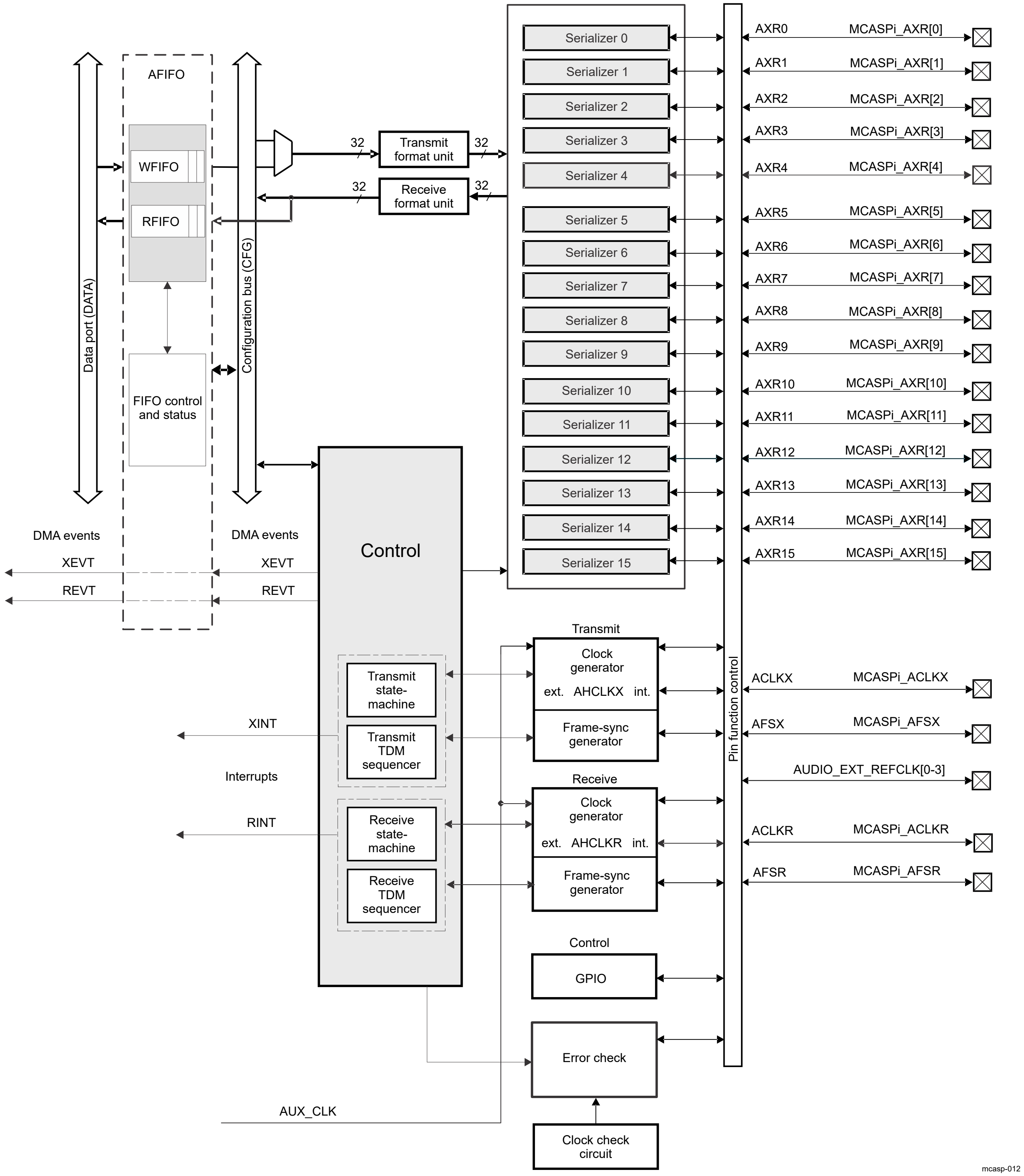
See the *Module Integration* section for information about clocks, resets and hardware requests.

12.1.2.4 MCASP Functional Description

In the text throughout this section a single instance of MCASP is described assuming that all modules are functionally identical. For module availability and integration differences, see Section 12.1.2.2, *MCASP Environment*, and *Module Integration*.

12.1.2.4.1 MCASP Block Diagram

Figure 12-20 shows the major blocks of the MCASP module.



A. i represents a valid instance of MCASP in a domain. See the device datasheet for valid instances.

B. All signals might not be valid for an instance. See the device datasheet for specifics.

Figure 12-20. MCASP Module Block Diagram

Note

The internal and external clocks mentioned in this section are with respect to clock and frame-sync generator modules.

12.1.2.4.2 MCASP Clock and Frame-Sync Configurations

There are three scenarios to provide clock source signals for the Tx part and four scenarios for the Rx part of the MCASP serializers. The first three scenarios are identical between the Tx and Rx part of the MCASP. They feature an asynchronous operation between receiver and transmitter channels using independent Tx/Rx bit rate clock sources (either internal or external).

In the first scenario, the transmit - XCLK and receive - RCLK serial clocks (clock at the bit rate) are generated internally by passing through a couple of clock dividers off the internal functional clock source (AUXCLK). In this case, the bit rate clock is generated internally and is driven out on the pin ACLKX for the Tx part and pin ACLKR for the Rx part, respectively. An internally generated high-frequency clock can be optionally driven out onto the AHCLKX pin for the Tx part to serve as a reference clock for other components in the system.

In the second scenario, an external for the device clock, is passed on the ACLKX (for the TX part) and ACLKR (for the RX part) pins which are configured as inputs. In this case the Rx- /Tx- high-speed clock logic is bypassed for the XCLK/RCLK generation.

In the third (mixed) scenario, an externally driven (controller) high-frequency clock is applied on the AHCLKX (for the TX part) pin, which is configured as input. In this case the AHCLKX clock frequency can be divided down via programming the ACLKX associated divider to produce the necessary bit rate clock. The high-speed clock divider can NOT be used.

In the fourth clock generation scenario the bit rate clock for MCASP receivers - RCLK is derived from the bit rate clock of the MCASP transmitters - XCLK for a synchronous operation between transmitters and receivers. Hence, the whole receiver clock generator logic is bypassed.

A typical role of the MCASP frame sync signal is to carry the left/right clock (LRCLK) signal when transmitting and receiving stereo data.

For an asynchronous operation, the AFSX (Tx part) and AFSR (Rx part) frame synchronization signals can be sourced internally or delivered externally independently for the Tx and Rx channels. During synchronous operation the receive frame sync - AFSR signal is derived from the transmit frame sync - AFSX signal. A synchronous and asynchronous mode applies to bit rate clock and frame sync signals at the same time.

12.1.2.4.2.1 MCASP Transmit Clock

The transmit high-speed and transmit clock configuration is controlled by the following registers:

- *MCASP_ACLKXCTL*
- *MCASP_AHCLKXCTL*

In case, the transmit bit clock, ACLKX, is generated internally, the *MCASP_ACLKXCTL*[5] CLKXM bit must be set to 1. Thus, the clock is divided down by a programmable bit clock divider (the *MCASP_ACLKXCTL*[4-0] CLKXDIV bit field) from the source signal.

If the transmit high-frequency controller clock, AHCLKX, is also sourced internally (that is first scenario described in Section 12.1.2.4.2, the *MCASP_AHCLKXCTL*[15] HCLKXM bit must be set to 1. Thus, the clock is divided down by a programmable high-clock divider (the *MCASP_AHCLKXCTL*[11-0] HCLKXDIV bit field) from the MCASP internal clock source AUXCLK.

Internally, the MCASP always shifts transmit data at the rising edge of the internal transmit clock - XCLK, (see Figure 12-21). The CLKXP mux determines if ACLKX needs to be inverted to become XCLK. If *MCASP_ACLKXCTL*[7] CLKXP = 0, the CLKXP mux directly passes ACLKX signal to XCLK. As a result, the MCASP shifts transmit data at the rising edge of ACLKX. If *MCASP_ACLKXCTL*[7] CLKXP = 1, the CLKX mux passes the inverted version of ACLKX to XCLK. As a result, the MCASP shifts transmit data at the falling edge of ACLKX.

It can be seen in Figure 12-21 that XCLK is propagated to the Rx clock logic, to allow an internally synchronous operation between MCASP transmitters and receivers. This is used for example in the MCASP loopback mode.

Note

The polarity of ACLKX can be controlled in the *MCASP_ACLKXCTL*[7] CLKXP bit, regardless of ACLKX signal being internally or externally sourced.

In addition, there is an option to invert polarity of the AHCLKX controller high speed clock via writing the *MCASP_AHCLKXCTL*[14] HCLKXP bit.

Note

In a similar way, the polarity of AHCLKX clock can be controlled in the *MCASP_AHCLKXCTL*[14] HCLKXP bit, regardless of the AHCLKX signal being internally or externally sourced.

Figure 12-21 presents the block diagram of the transmit clock generator.

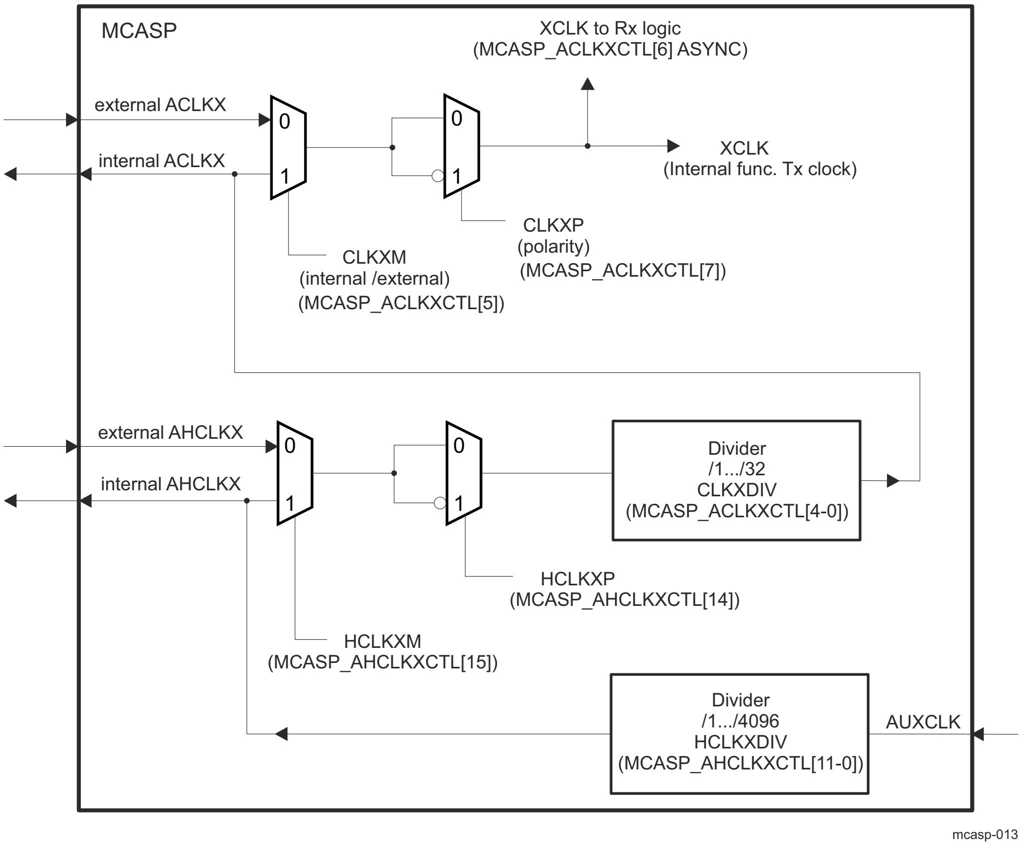


Figure 12-21. Transmit Clock Generator Block Diagram

Note

In this device:

- ACLKX is mapped on the device ball ACLKX
- internal AHCLKX is mapped on the device balls AUDIO_EXT_REFCLK[0-1]
- external AHCLKX is mapped on MCASPi_AHCLKX clock from the Device Configuration

For more information about MCASP integration, see Section 12.1.2.2, *MCASP Environment*, and *Module Integration*.

12.1.2.4.2.2 MCASP Receive Clock

The MCASP receive clock generator is built on a very similar to the transmit clock generator (but independent) circuit.

The receive clock configuration is controlled by the following registers:

- *MCASP_ACLKRCTL*
- *MCASP_AHCLKRCTL*

In case, the receive bit clock, ACLKR, is generated internally (but asynchronously to XCLK), the *MCASP_ACLKRCTL*[5] CLKRM bit must be set to 1. Thus, the clock is divided down by a programmable bit clock divider (the *MCASP_ACLKRCTL*[4-0] CLKRDIV bit field) from the source signal.

If the receive high-frequency controller clock, AHCLKR, is also sourced internally (that is, first scenario described in Section 12.1.2.4.2) and the *MCASP_AHCLKRCTL*[15] HCLKRM bit must be set to 1. Thus, the clock is divided down by a programmable high-clock divider (the *MCASP_AHCLKRCTL*[11-0] HCLKRDIV bit field) from the MCASP internal clock source AUXCLK.

Note

The polarity of ACLKR can be controlled in the *MCASP_ACLKRCTL*[7] CLKRP bit, regardless of ACLKR signal being internally or externally sourced.

In a similar way, the polarity of AHCLKR clock can be controlled in the *MCASP_AHCLKRCTL*[14] HCLKRP bit, regardless of the AHCLKR signal being internally or externally sourced.

There is an option for the MCASP receiver to be configured to operate synchronously to the ACLKX and AFSX signals. The XCLK output of the Tx Clock generator (see Figure 12-21 and Figure 12-22) becomes source of the receive clock (RCLK output), when the *MCASP_ACLKRCTL*[6] ASYNC bit in the transmit clock control register is set to '0b0'. For more information, refer to Section 12.1.2.4.2.4.

Figure 12-22 presents the block diagram of the receive clock generator.

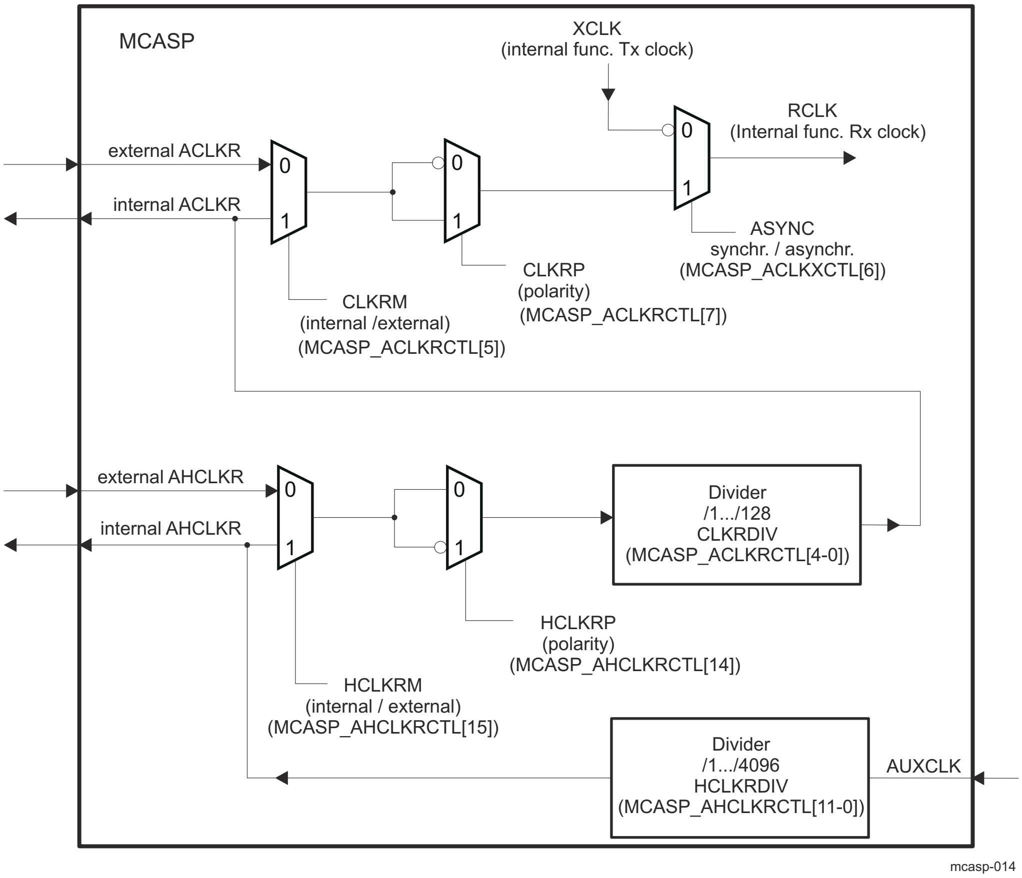


Figure 12-22. Receive Clock Generator Block Diagram

Note

In this device:

- ACLKR is mapped on the device ball ACLKR
- internal AHCLKX is mapped on the device balls AUDIO_EXT_REFCLK[0-1]
- external AHCLKR is mapped on Device Configuration MCASPi_AHCLKR from Device Configuration

For more information about MCASP integration, see Section 12.1.2.2, *MCASP Environment*, and , *Module Integration*.

12.1.2.4.2.3 Frame-Sync Generator

There are two different modes for frame sync: burst and TDM. The MCASP frame sync generator logic is illustrated in Figure 12-23.The I/O buffers are not part of the MCASP module, and are not shown in the figure.

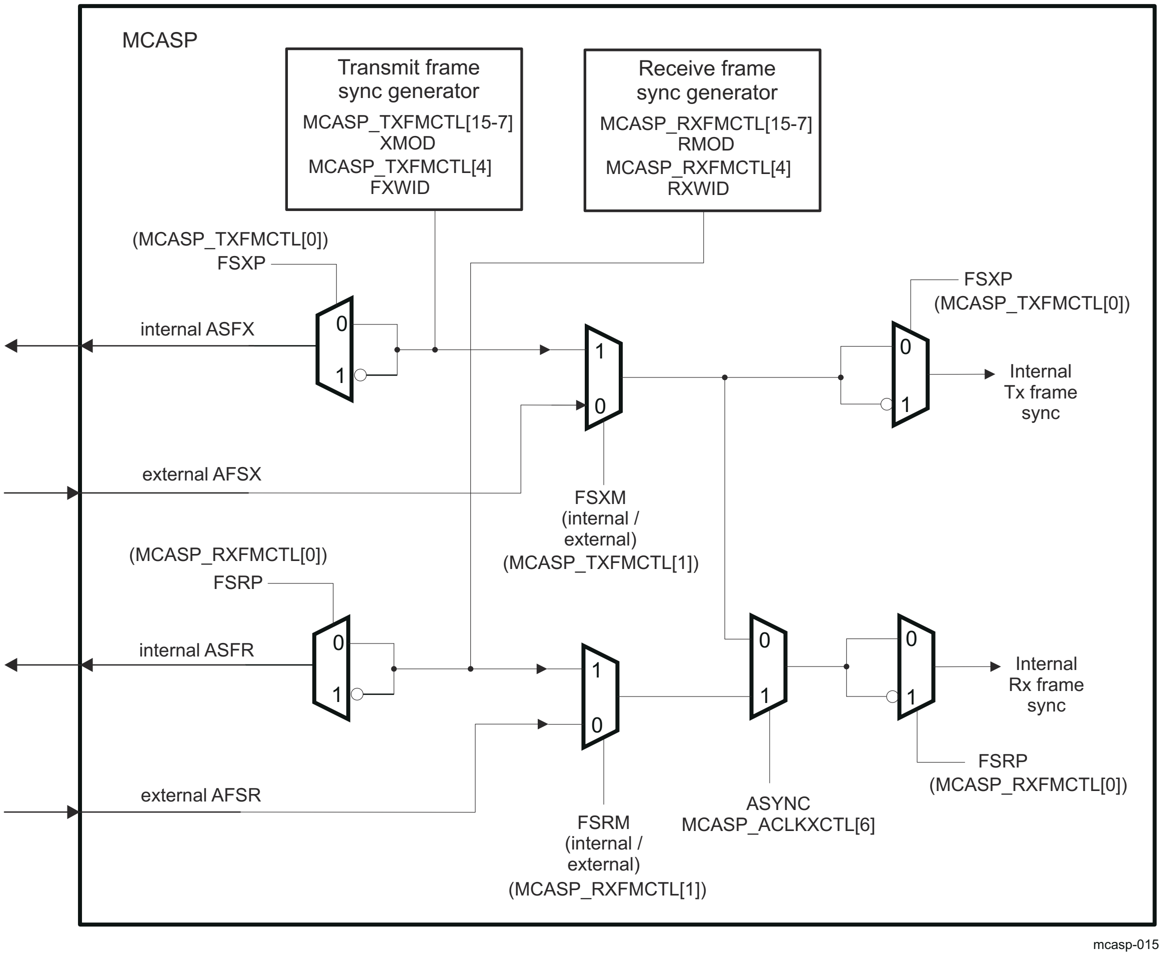


Figure 12-23. Frame Sync Generator Block Diagram

Note

For more on MCASP integration, see Section 12.1.2.2, *MCASP Environment*, and *Module Integration*.

For the transmit logic, following frame-sync generator configurations can be selected:

- Internally/externally generated frame-sync via configuring MCASP_AFSXCTL[1] FSXM bit
- Frame-sync polarity: Rising edge or falling edge via configuring MCASP_AFSXCTL[0] FSXP bit
- Frame-sync width: "single bit" or "single word" via configuring MCASP_AFSXCTL[4] FXWID bit
- Frame sync mode - the appropriate frame sync generation pattern for the selected transfer mode is defined in the MCASP_AFSXCTL[15-7] XMOD bit field, as follows:
  - For DIT mode (384 slots) - MCASP_AFSXCTL[15-7] XMOD = 0x180
  - For I2S mode (2 TDM slots) - MCASP_AFSXCTL[15-7] XMOD = 0x2
  - For TDM mode (from 3 to 32 TDM slots) - MCASP_AFSXCTL[15-7] XMOD bit field set in range 0x3 - 0x20
- Bit delay: 0, 1, or 2 cycles before the first data bit. This delay is defined in MCASP_XFMT[17-16] XDATDLY bit field

For the receive logic, following frame-sync generator configurations can be selected:

- Internally/externally generated frame-sync via configuring MCASP_AFSRCTL[1] FSRM bit
- Frame-sync polarity: Rising edge or falling edge via configuring MCASP_AFSRCTL[0] FSRP bit
- Frame-sync width: "single bit" or "single word" via configuring MCASP_AFSRCTL[4] FRWID bit
- Frame sync mode - the appropriate frame sync generation pattern for the selected transfer mode is defined in the MCASP_AFSRCTL[15-7] RMOD bit field, as follows:
  - For I2S mode (2 TDM slots) - MCASP_AFSRCTL[15-7] RMOD = 0x2

  - For TDM mode (from 3 to 32 TDM slots) - MCASP_AFSRCTL[15-7] RMOD set in range 0x3 - 0x20
  - For the special 384-slot TDM mode - MCASP_AFSRCTL[15-7] RMOD = 0x180
- Bit delay: 0, 1, or 2 cycles before the first data bit. This delay is defined in the MCASP_RFMT[17-16] RDATDLY bit field
- Selecting the source (AFSX or AFSR) of receiver internal frame synchronization. This is done in the same bit - *MCASP_ACLKXCTL*[6] ASYNC, used to define the receiver internal clock source. For more details, refer to Section 12.1.2.4.2.4, *Synchronous and Asynchronous Transmit and Receive Operations*.

Regardless of the AFSX/AFSR being internally generated or externally sourced, the polarity of AFSX/AFSR is determined by FSXP/FSRP, respectively, to be either rising or falling edge. If FSXP/FSRP = 0, the frame sync polarity is rising edge. If FSXP/FSRP = 1, the frame sync polarity is falling edge.

Note

Certain restrictions apply to the receive and transmit logic settings, when the *MCASP_ACLKXCTL*[6] ASYNC bit is set to 0b0. They are described in Section 12.1.2.4.2.4.

12.1.2.4.2.4 Synchronous and Asynchronous Transmit and Receive Operations

Synchronous Transmit and Receive Operations -

When the *MCASP_ACLKXCTL*[6] ASYNC bit is written to 0b0, the transmit and receive sections operate synchronously to the transmit section clock and transmit frame sync signals.

Though Rx section may have a different data format, it has to be configured to have the same slot size than the transmit section one. As shown on the Figure 12-22, with the ASYNC bit set to 0b0, the RCLK becomes an inverted version of the transmit clock generator XCLK output.

When the *MCASP_ACLKXCTL*[6] ASYNC = 0b0, both Rx and Tx sections use the same clock and frame sync signals. For this reason, they must be aligned on the following settings:

- MCASP_DITCTL[0] DITEN = 0 (that is, transmission in TDM mode is enabled)
- The total number of bits per frame must be the same (that is, RSSZ * RMOD product value must equal XSSZ * XMOD product value)
- The settings in the *MCASP_ACLKRCTL* register are NOT considered
- FSXM must match FSRM
- FXWID must match FRWID

For all other settings, the transmit and receive sections may be programmed independently.

Asynchronous Transmit and Receive Operations -

When the *MCASP_ACLKXCTL*[6] ASYNC = 0b1, Tx and Rx operate independently from each other with separate clock and frame sync signals.

Note

Synchronous transmit and receive operations are allowed only in the MCASP TDM (I2S) mode (this is, when MCASP_DITCTL[0] DITEN = 0b0).

12.1.2.4.3 MCASP Serializers

The MCASP serializers shift serial data in (Rx) and out (Tx) of the MCASP. A given serializer n consists of a shift register (XRSRn) with a single-entry data buffer XRBUFn used either for transmitting (write accessible in the MCASP_XBUFn register) or for receiving (read accessible in the MCASP_RBUFn register) data. In addition, each serializer has a dedicated control register (MCASP_SRCTLn) and a serial bidirectional data pin - AXRn. The register MCASP_SRCTLn allows n-th serializer to be configured as a transmitter, receiver, or as inactive. There are transmit and receive data formatting units to support data alignment options of the MCASP which are shared between all Tx and Rx serializers, respectively.

A given serializer XRSRn shifter configured as a receiver in the MCASP_SRCTLn register, shifts in data through MCASP corresponding device level bidirectional data pad AXRn. A given serializer XRSRn shifter configured as a transmitter in the MCASP_SRCTLn register, shifts out data on MCASP corresponding device level bidirectional data pad AXRn (n = 0 to 15).

The serializer is clocked from the transmit section clock (ACLKX signal) if configured to transmit or clocked from the receive section clock (ACLKR signal) if configured to receive. A serializer configured to transmit and receive operates in lockstep, which means that for MCASP there are at most a couple of zones, one for transmit and one for receive.

Figure 12-24 shows the serializer block diagram.

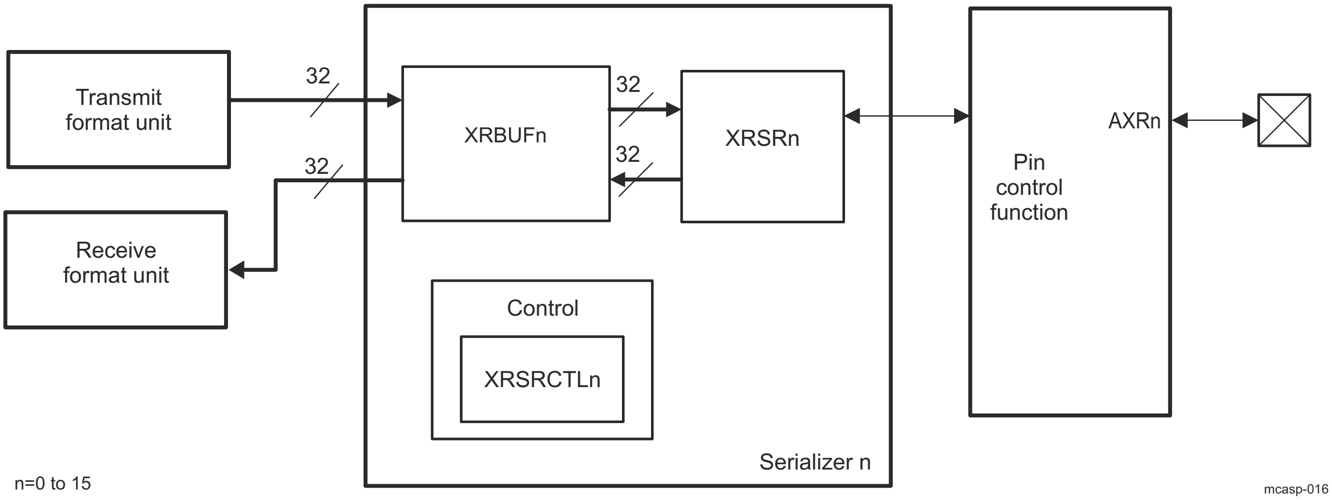


Figure 12-24. Individual Serializer and Connections Within MCASP

Transmission on the n-th serializer is performed as follows:

The MCASP is serviced by writing data into the MCASP_XBUFn register, which is an alias of the serializer data buffer - XRBUFn for transmit function. The data automatically passes through the transmit format unit before reaching the XRBUFn register in the serializer. The data is then copied from the XRBUFn to XRSRn and shifted out from AXRn synchronously to the serial clock.

Reception from the n-th serializer is performed as follows:

The data is shifted into the MCASP XRSRn serializer register through the AXRn pin, bit by bit. Once the entire slot becomes available within the XRSRn shift register, the data is copied into the serializer data buffer - XRBUFn, and can be accessed in the MCASP_RBUFn register, which is an alias of the serializer data buffer - XRBUFn for receive function. When software reads the data from this register, the MCASP passes the data through the receive format unit, hence it returns the formatted data.

Serializer controls:

A serializer n is configured as inactive via setting MCASP_SRCTLn[1-0] SRMOD bit field to 0x0.

For a transmitting serializer, the MCASP_SRCTLn[3-2] DISMOD bitfield, defines the AXRn pin output state, during inactive slots (HIGH, LOW or Hi-Z).

Transmit function for the n-th serializer is selected via setting MCASP_SRCTLn[1-0] SRMOD bit field to 0x1.

Receive function for the n-th serializer is selected via setting MCASP_SRCTLn[1-0] SRMOD bit field to 0x2 (n = 0 to 15).

In the DIT-transmission mode (that is S/PDIF format data transmission): in addition to the data, the serializer shifts out other DIT-specific information accordingly (preamble, user data, etc.). For more information, see Section 12.1.2.2.2.5, *S/PDIF Coding Format*.

12.1.2.4.4 MCASP Format Units

The MCASP has one transmit data formatting unit and one receive data formatting unit, shared between the device MCASP serializers. These units automatically remap the data bits within the transmitted or received words between a natural format for the device processors (for example, a Q31 representation) and the required format for the external serial device (for example I2S format). During the remapping process, the format unit can also mask off certain bits.

Since all transmitters share the same data formatting unit, the MCASP only supports one transmit format at a time. For example, the MCASP does NOT transmit in "I2S format" on serializer 0, while transmitting "Left Justified" on serializer 1. Likewise, the receiver section of the MCASP only supports one data format at a time, and this format applies to all receiving serializers.

Note

The MCASP can transmit in one format while receiving in a completely different format.

The bit mask and pad stage of each of Tx and Rx format units includes a full 32-bit mask register, allowing selected individual bits to either pass through the stage unchanged, or be masked off. The bit mask and pad then pad the value of the masked off bits by inserting either a 0, a 1, or one of the original 32 bits as the pad value. The last option allows for sign-extension when the sign bit is selected to pad the remaining bits. The rotate right stage performs bitwise rotation by a multiple of 4 bits (between 0 and 28 bits), programmable by the MCASP_RFMT/MCASP_XFMT register. Note that this is a rotation process, not a shifting process, so bit 0 gets shifted back into bit 31 during the rotation. The bit order - reversal stage either passes all 32 bits directly through, or swaps them. This allows for either MSB or LSB first data formats. If bit order reversal is not enabled, then the MCASP will naturally transmit and receive in an LSB first order. Finally, note that the RDATDLY/XDATDLY bits in the MCASP_RFMT/MCASP_XFMT also determine the data format. For example, the difference between I2S format and left-justified is determined by the delay between the frame sync edge and the first data bit of a given time slot. For I2S format, RDATDLY/XDATDLY should be set to a 1-bit delay, whereas for left-justified format, it should be set to a 0-bit delay. The combination of all the options in the MCASP_RFMT/MCASP_XFMT register means that the MCASP supports a wide variety of data formats, both on the serial data lines, and in the device CPU data representation.

12.1.2.4.4.1 Transmit Format Unit

The MCASP transmit formatting unit consists of three stages :

- Bit mask (masks off bits)
- Rotate right (aligns data within word)
- Bit reversal (selects between MSB-first or LSB-first)

Figure 12-25 shows the transmit formatting unit.

The MCASP transmitter supports serial formats of:

- Slot (or Time slot) size = 8, 12, 16, 20, 24, 28, 32 bits
- Word size ≤ Slot size
- Alignment: when more bits/slot than bits/words, then:
  - Left aligned = word shifted first, remaining bits are pad
  - Right aligned = pad bits are shifted first, word occupies the last bits in slot
- Order of bits shifted out:
  - MSB: most-significant bit of word is shifted out first, last bit is LSB
  - LSB: least-significant bit of word is shifted out last, last bit is MSB

Hardware support for these serial formats comes from the programmable options in the bitstream format register - MCASP_XFMT:

- XRVRS: bit reverse (1) or no bit reverse (0)
- XROT: rotate right by 0, 4, 8, 12, 16, 20, 24, or 28 bits
- XSSZ: transmit slot size of 8, 12, 16, 20, 24, 28, or 32 bits

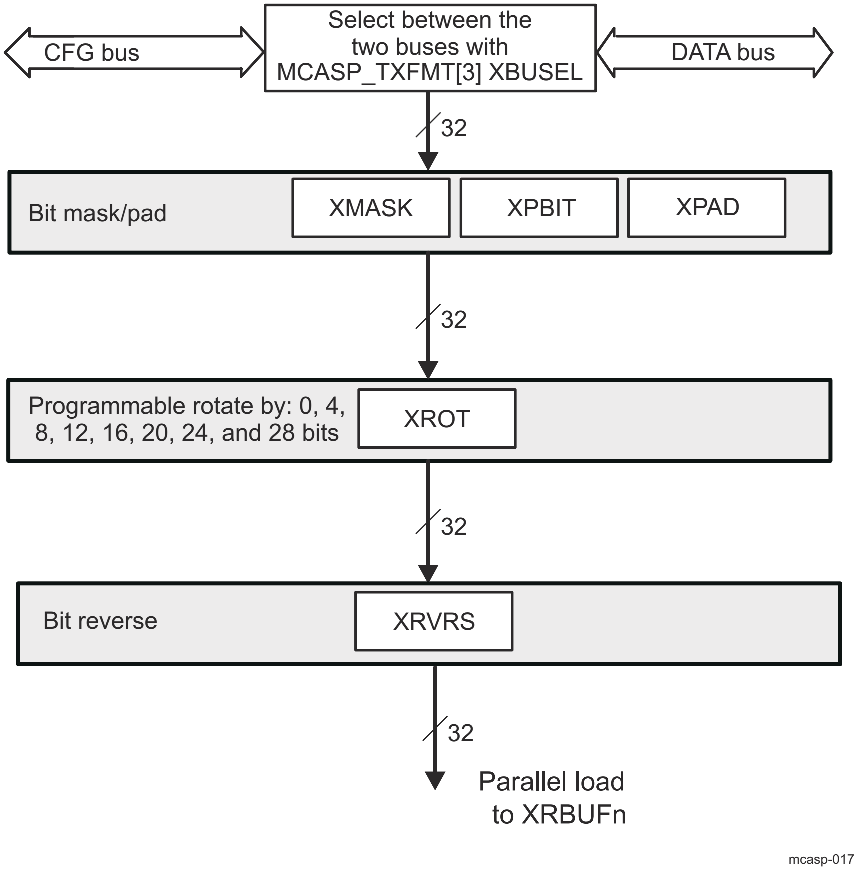


Figure 12-25. Transmit Format Unit

As shown in Figure 12-25, the data to the transmit format unit can come from the configuration port (CFG) or the data port (DATA). The selection is made through the MCASP_XFMT[3] XBUSEL bit. According to port type selected, data transfer has different behaviour. For more details, refer to the Section 12.1.2.4.10.1.3, *Transfers Through the DATA Port*, and Section 12.1.2.4.10.1.4, *Transfers Through the Configuration (CFG) Bus*.

In the transmit format unit (TFU), the input data bits are first masked-off with the MCASP_XMASK[31-0] XMASK contents. The masked data is then right-rotated to the MCASP_XFMT[2-0] XROT bit field positions, to produce the output word for a TDM- or DIT- transmission.

The bit mask stage includes a full 32-bit mask register, allowing selected individual bits to pass through the stage unchanged or be masked off.

12.1.2.4.4.1.1 TDM Mode Transmission Data Alignment Settings

The TDM-mode transmission settings are relevant for I2S-protocol and protocols using more than 2 TDM-slots.

XSSZ should always be programmed to match the slot size of the serial stream.

Note

Note that, TDM word size is not directly programmed into the MCASP, but rather is used to determine the rotation needed in the XROT field.

The Table 12-12 show the XRVRS and XROT fields for each serial format and for both integer and Q31 fractional internal representations.

The Table 12-12 assumes that all slot size (SLOT in Table 12-12) and word size (WORD in Table 12-12) options are multiples of 4, since the transmit rotate right unit only supports rotation by multiples of 4. However, the bit mask/pad unit does allow for any number of significant digits. For example, a Q31 number may have 19 significant digits (word) and be transmitted in a 24-bit slot; this would be formatted as a word size of 20 bits and a slot size of 24 bits. However, it is possible to set the bit mask unit to only pass the 19 most-significant digits (program the mask value to FFFF E000h). The digits that are not significant can be set to a selected pad value, which can be any one of the significant digits, a fixed value of 0, or a fixed value of 1.

The transmit bit mask/pad unit operates on data as an initial step of the transmit format unit, and the data is aligned in the same representation as it is written to the transmitter (typically Q31 or integer).

Table 12-12. MCASP TFU TDM Mode Settings

Bit Stream Order	Bit Stream Alignment	Internal Numeric Representation	MCASP_XFMT bits	
			XROT[1]	XRVRS
MSB first[2]	Left aligned	Q31 fraction	0	1
MSB first	Right aligned	Q31 fraction	SLOT - WORD	1
LSB first	Left aligned	Q31 fraction	32 - WORD	0
LSB first	Right aligned	Q31 fraction	32 - SLOT	0
MSB first[2]	Left aligned	Integer	WORD	1
MSB first	Right aligned	Integer	SLOT	1
LSB first	Left aligned	Integer	0	0
LSB first	Right aligned	Integer	(32 - (SLOT - WORD)) % 32	0

(1) WORD = Word size rounded up to the nearest multiple of 4; SLOT = slot size; % = modulo operator
(2) To transmit in I2S format, select MSB first, left aligned, and also select XDATDLY = 01 (1 bit delay)

12.1.2.4.4.1.2 DIT Mode Transmission Data Alignment Settings

In case of a DIT-mode (S/PDIF protocol) transmission, while left-aligned Q31 data should be right-rotated to a multiple by 4 positions, no right-rotation is required for a right-aligned Q31 data. Because this is a rotation process, not a shifting process, bit 0 gets shifted back into bit 31 during the process.

The MCASP_XFMT[17-16] XDATDLY bit field must be set to a 0-bit delay (0x0 value).

For left-aligned Q31 data, the following transmit format unit settings process the data into right-aligned data, ready for transmission:

- MCASP_XFMT[2-0] XROT =
  - 0x2 (rotate right by 8 bits) - for a 24-bit output audio data
  - 0x3 (rotate right by 12 bits) - for a 20-bit output audio data
  - 0x4 (rotate right by 16 bits) - for a 16-bit output audio data
- MCASP_XFMT[15] XRVRS = 0x0 – Bit reversal is not enabled; the MCASP naturally transmits and receives in a LSB-first order.
- MCASP_XMASK[32] XMASK = 0xFFFFFF00 – 0xFFFF0000
- MCASP_XFMT[14-13] XPAD = 0x0 (Pad extra bits with 0s.)

For right-aligned data, the following transmit format unit settings process the data into right-aligned audio data ready for transmission:

- MCASP_XFMT[2-0] XROT = 0x0 (rotate right by 0 bits regardless of the audio word length)
- MCASP_XFMT[15] XRVRS = 0x0 – Bit reversal is not enabled; the MCASP naturally transmits and receives in a LSB-first order.
- MCASP_XMASK[32] XMASK = 0x00FFFFFF – 0x0000FFFF
- MCASP_XFMT[14-13] XPAD = 0x0 (Pad extra bits with 0s.)

The example settings provided in Table 12-13 should be applied to MCASP in cases of DIT-transmitting a Q31 data as a 24-bit, 20-bit and 16-bit left- or right- aligned audio word, respectively. Note that the listed settings let the MCASP TFU preserve the most significant bits and cut only the LSBs of the original Q31 CPU data:

Table 12-13. MCASP TFU DIT-Mode Example Settings

Output Audio Word Alignment	Audio Word Length	Right-rotation (multiple of 4-bit positions)	XMASK	XROT
LEFT	16	16	0xFFFF0000	0x4
LEFT	20	12	0xFFFFF000	0x3

Table 12-13. MCASP TFU DIT-Mode Example Settings (continued)

Output Audio Word Alignment	Audio Word Length	Right-rotation (multiple of 4-bit positions)	XMASK	XROT
LEFT	24	8	0xFFFFFF00	0x2
RIGHT	16	0	0x0000FFFF	0x0
RIGHT	20	0	0x000FFFFF	0x0
RIGHT	24	0	0x00FFFFFF	0x0

Assuming that a Q31 data word 0xFA5AFxxx (where x-marked nibbles of the data are applied as padding bits of the word) is generated on the MCASP CFG (peripheral) port. To transmit a left-aligned 20-bit version of same word, preserving the MSBs, according to the Table 12-13, the user must set XMASK = 0xFFFFF000, and to select a right-rotation to 12 positions (XROT = 0x3).

- After applying 0-s (XPAD = 0) as masking-off bits at the first TFU stage, word is transformed to the word 0xFA5AF000.
- After a rotation by 12 positions to the right is performed in TFU, the 20-bit output word obtained is: 0x000FA5AF. Thus the word gets ready for transmission being mapped with its LS-bit as bit 8 and its MS-bit as bit 27 within a S/PDIF bitstream. This word is shifted in a LSB-to-MSB order (XRVRS = 0x0) out of the XRSR register during a DIT-transmission.

Assuming that a right-aligned Q31 data word - 0x yyyyE4B4 is generated by software on the MCASP CFG (peripheral) port (with the presumption that y-marked nibbles of the input data are applied as padding bits). To transmit a right-aligned 16-bit version of same word, preserving the MSBs, according to the table MCASP TFU Example Settings, user is supposed to set XMASK = 0x0000FFFF, and to select right-rotation to 0 positions (XROT = 0x0).

- After masking-off with 0s at first TFU stage, word is transformed to 0x0000E4B4.
- Since no rotation is applied, the 16-bit output word obtained is actually the one obtained in the masking stage – 0x0000E4B4.

The above examples use internal representation in integer and Q31 notation, but other fractional notations are also possible.

12.1.2.4.4.2 Receive Format Unit

The MCASP receive formatting unit consists of three stages:

- Bit mask (masks off bits)
- Rotate right (aligns data within word)
- Bit reversal (selects between MSB first or LSB first)

Figure 12-26 shows the receive format unit (RFU).

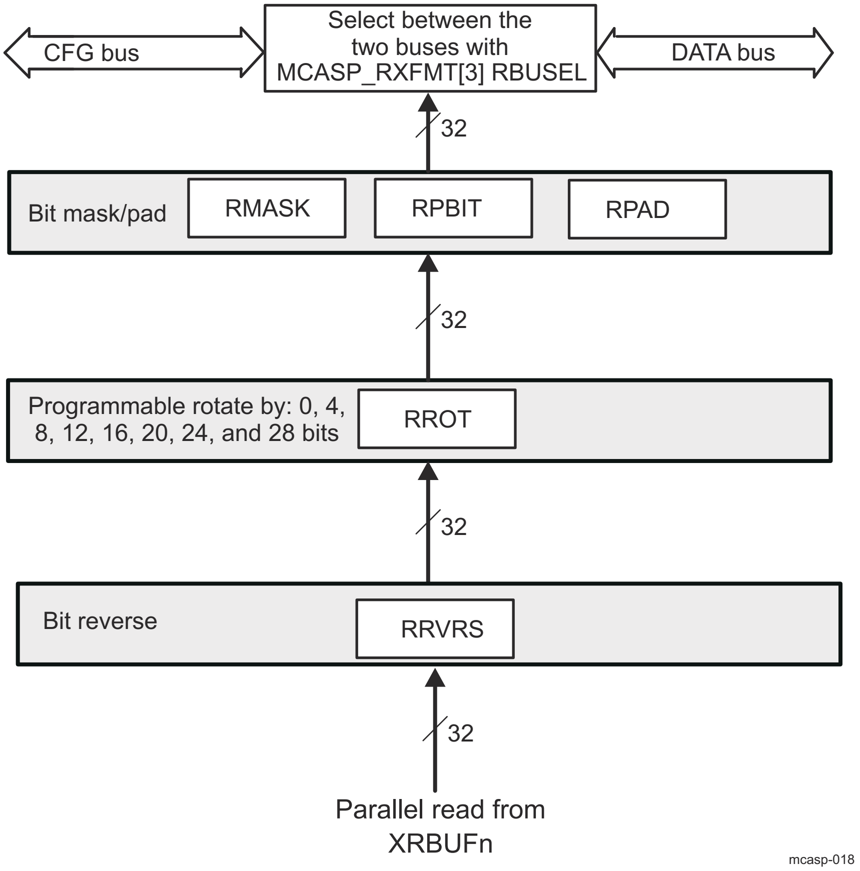


Figure 12-26. Receive Format Unit

The MCASP receiver supports serial formats of:

- Slot or time slot size = 8, 12, 16, 20, 24, 28, 32 bits
- Word size ≤ Slot size
- Alignment when more bits are available per slot than bits per word within the slot, then:
  - Left aligned = word shifted first, remaining bits are pad
  - Right aligned = pad bits are shifted first, word occupies the last bits in slot
- Order of bits shifted out:
  - MSB: most-significant bit of word is shifted out first, last bit is LSB
  - LSB: least-significant bit of word is shifted out last, last bit is MSB

Hardware support for these serial formats comes from the programmable options in the receive bitstream format register - MCASP_RFMT:

- RRVRS: bit reverse (1) or no bit reverse (0)
- RROT: rotate right by 0, 4, 8, 12, 16, 20, 24, or 28 bits
- RSSZ: receive slot size of 8, 12, 16, 20, 24, 28, or 32 bits

As shown on Figure 12-26, the data processed in the RFU can be output to host CPU through the configuration port (CFG) or the data port (DATA). The selection is made through the MCASP_RFMT[3] RBUSEL bit. According to port type selected, data transfer has different behaviour. For more details, refer to the Section 12.1.2.4.10.1.3, *Transfers Through the DATA Port*, and Section 12.1.2.4.10.1.4, *Transfers Through the Configuration (CFG) Bus*.

12.1.2.4.4.2.1 TDM Mode Reception Data Alignment Settings

RSSZ should always be programmed to match the slot size of the serial stream.

Note

Note that the word size is not directly programmed into the MCASP, but rather is used to determine the rotation needed in the RROT field.

Table 12-14 shows the RRVRS and RROT fields for each serial format and for both integer and Q31 fractional internal representations.

Table 12-14. MCASP RFU Settings

Bit Stream Order	Bit Stream Alignment	Internal Numeric Representation	MCASP_RFMT bits	
			RROT[1]	RRVRS
MSB first[2]	Left aligned	Q31 fraction	SLOT	1
MSB first	Right aligned	Q31 fraction	WORD	1
LSB first	Left aligned	Q31 fraction	(32 - (SLOT - WORD)) % 32	0
LSB first	Right aligned	Q31 fraction	0	0
MSB first[2]	Left aligned	Integer	SLOT - WORD	1
MSB first	Right aligned	Integer	0	1
LSB first	Left aligned	Integer	32 - SLOT	0
LSB first	Right aligned	Integer	32 - WORD	0

(1) WORD = Word size rounded up to the nearest multiple of 4; SLOT = slot size; % = modulo operator
(2) To receive in I2S format, select MSB first, left aligned, and also select RDATDLY = 01 (1 bit delay)

The Table 12-14 assumes that all slot size and word size options are multiples of 4; since the receive rotate right unit only supports rotation by multiples of 4. However, the bit mask/pad unit does allow for any number of significant digits. For example, a Q31 number may have 19 significant digits (word) and be received in a 24-bit slot; this would be formatted as a word size of 20 bits and a slot size of 24 bits. However, it is possible to set the bit mask unit to only pass the 19 most-significant digits (program the mask value to FFFF E000h). The digits that are not significant can be set to a selected pad value, which can be any one of the significant digits, a fixed value of 0, or a fixed value of 1. The receive bit mask/pad unit operates on data as the final step of the receive format unit (see Figure 12-26), and the data is aligned in the same representation as it is read from the receiver (typically Q31 or integer).

12.1.2.4.5 MCASP State-Machines

The receive and transmit sections have independent state machines.

Each state-machine controls the interactions between the various units in the MCASP Rx and Tx sections, respectively. In addition, each state-machine keeps track of error conditions and serial port status. No serial transfers can occur until the RX/TX state-machine is released from reset.

The transmit state-machine is controlled by the transmit bitstream format register (MCASP_XFMT) and it reports the MCASP status and error conditions in the transmitter status register (MCASP_XSTAT).

Similarly, the receive state-machine is controlled by the receive bitstream format register (MCASP_RFMT) and it reports the MCASP status and error conditions in the receiver status register (MCASP_RSTAT).

12.1.2.4.6 MCASP TDM Sequencers

There are separate TDM sequencers for the transmit section and the receive section. Each TDM sequencer keeps track of the slot count. In addition, the TDM sequencer checks the bits of the MCASP_RTDM/MCASP_XTDM register and determines if the MCASP should receive/transmit in that time slot.

There are two possibilities for a slot: The MCASP either performs Rx/Tx operations during the time slot (transmit/receive bit is active), or the MCASP skips Rx/Tx operations during the time slot (transmit/receive bit is inactive). In the latter case, no transfers between the XRBUF and XRSR registers in the serializer would occur during that time slot.

In addition, during time of inactive slots, the serializers programmed as transmitters place their data output pins - AXRn in a predetermined state - logic low, high, or high impedance (tri-stated) as programmed in each serializer control MCASP_SRCTLn[3-2] DISMOD register. Refer also to Section 12.1.2.4.9.2.1, *TDM Time Slots Generation and Processing*, for details on how DMA event or interrupt generations are handled during inactive time slots in TDM mode.

In case of a DIT-transmission (S/PDIF transfers): the time division multiplexing (TDM) sequencer is used to count the 384 subframes (slots) in the DIT block. If currently transmitting slot 1, slot 2 (next value of the TDM slot counter) should be used during the encode phase to select the appropriate C, V, and U bit, because the data encoded and written to a MCASP_XBUFn register during the current time slot (slot 1) is actually shifted out on the next time slot (n = 0 to 15).

The transmit TDM sequencer is controlled by the MCASP_XTDM register and reports the current transmit slot to the MCASP_XTDMSLOT[9-0] XSLOTCNT bit field.

12.1.2.4.7 MCASP Software Reset

The MCASP can be put into reset through the global transmit and receive control register (*MCASP_GBLCTL*). A valid serial clock must be supplied to the MCASP to assert the software reset bits in the *MCASP_GBLCTL* register.

12.1.2.4.8 MCASP Power Management

Table 12-15 describes power-management features available to the MCASP.

Table 12-15. Local Power-Management Features

Feature	Registers	Description
Target clock stop modes	*MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE	Force-clock stop, no-clock stop, and smart-clock stop modes are available.

CAUTION

No wakeup schema is supported for the MCASP. To ensure a correct behavior after enabling MCASP at device Device Configuration level, the user software is strongly recommended to choose *No Idle* mode, setting *MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE bit field to 0x1. Before disabling MCASP at device Device Configuration level, user software is strongly recommended to choose a *Smart-Idle* mode, setting *MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE bit field to 0x2.

12.1.2.4.9 MCASP Transfer Modes

12.1.2.4.9.1 Burst Transfer Mode

The MCASP supports a burst transfer mode, which is useful for nonaudio data such as passing control information between two processors. Burst transfer mode uses a synchronous serial format similar to the TDM mode. The frame sync generation is not periodic or time-driven as in TDM mode, but data driven, and the frame sync is generated for each data word transferred.

When operating in burst frame sync mode (see Figure 12-27), as specified for transmit (MCASP_AFSXCTL[15-7] = 0) and receive (MCASP_AFSRCTL[15-7] RMOD = 0), one slot is shifted for each active edge of the frame sync signal that is recognized. Additional clocks after the slot and before the next frame sync edge are ignored.

In burst frame sync mode, the frame sync delay may be specified as 0, 1, or 2 serial clock cycles. This is the delay between the frame sync active edge and the start of the slot. The frame sync signal lasts for a single bit clock duration (MCASP_AFSRCTL[4] FRWID = 0, MCASP_AFSXCTL[4] FXWID = 0).

For transmit, when generating the transmit frame sync internally, the frame sync begins when the previous transmission has completed and when all the XBUFn (for every serializer set to operate as a transmitter) has been updated with new data.

For receive, when generating the receive frame sync internally, frame sync begins when the previous transmission has completed and when all the RBUFn (for every serializer set to operate as a receiver) has been read.

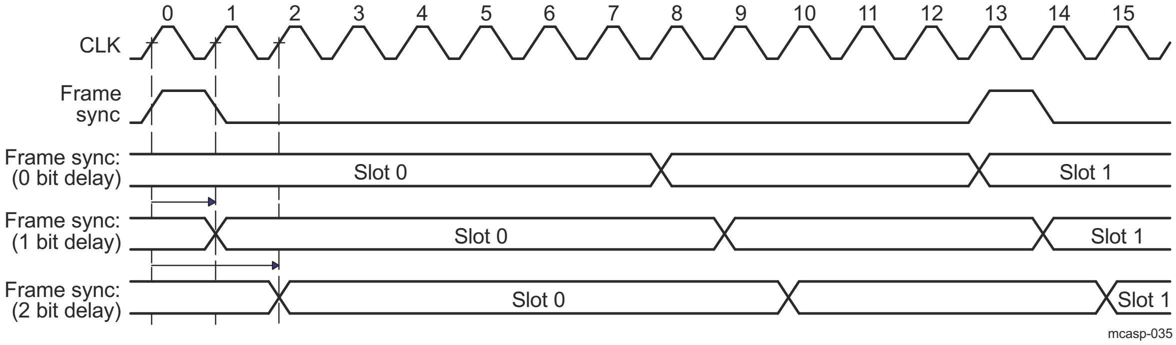


Figure 12-27. Burst Frame Sync Mode

The control registers must be configured as follows for the burst transfer mode. The burst mode specific bit fields are in bold face:

- *MCASP_PFUNC*: The clock, frame, data pins must be configured for MCASP function.
- *MCASP_PDIR*: The clock, frame, data pins must be configured to the direction desired.
- *MCASP_PDOUT*, *MCASP_PDIN*, *MCASP_PDCLR*: Not applicable. Leave at default.
- *MCASP_GBLCTL*: Follow the initialization sequence in Section 12.1.2.5.1.2, *MCASP Global Initialization*, to configure this register.
- *MCASP_AMUTE*: Not applicable. Leave at default.
- MCASP_DLBCTL: If loopback mode is desired, configure this register according to Section 12.1.2.4.14, *MCASP Loopback Modes*, otherwise leave this register at default.
- MCASP_DITCTL: DITEN must be left at default 0 to select non-DIT mode. Leave the register at default.
- MCASP_RMASK/MCASP_XMASK: Mask desired bits according to Section 12.1.2.4.4, *MCASP Format Units*.
- MCASP_RFMT/MCASP_XFMT: Program all fields according to data format desired. See Section 12.1.2.4.4, *MCASP Format Units*.
- MCASP_RFMT/MCASP_XFMT: Clear RMOD/XMOD bits to 0 to indicate burst mode. Clear FRWID/FXWID bits to 0 for single bit frame sync duration. Configure other fields as desired.
- *MCASP_ACLKRCTL/MCASP_ACLKXCTL*: Program all fields according to bit clock desired. See Section 12.1.2.4.2, *MCASP Clock and Frame-Sync Configurations*.
- *MCASP_AHCLKRCTL/MCASP_AHCLKXCTL*: Program all fields according to high-frequency clock desired. See Section 12.1.2.4.2, *MCASP Clock and Frame-Sync Configurations*.
- MCASP_RTDM/MCASP_XTDM: Program RTDMS0/XTDMS0 to 1 to indicate one active slot only. Leave other fields at default.
- MCASP_RINTCTL/MCASP_XINTCTL: Program all fields according to interrupts desired.
- MCASP_RCLKCHK/MCASP_XCLKCHK: Not applicable. Leave at default.
- MCASP_SRCTLn: Program SRMOD to inactive/transmitter/receiver as desired. DISMOD is not applicable and should be left at default (n = 0 to 15).
- MCASP_DITCSRAi, MCASP_DITCSRBi, MCASP_DITUDRAi, MCASP_DITUDRBi: Not applicable. Leave at default (i = 0 to 5).

12.1.2.4.9.2 Time-Division Multiplexed (TDM) Transfer Mode

The MCASP time-division multiplexed (TDM) transfer mode supports the TDM format discussed in Section 12.1.2.2.2.3, *TDM Format*.

Transmitting data in the TDM transfer mode requires a minimum set of pins:

- ACLKX - transmit bit clock
- AFSX - transmit frame sync (or commonly called left/right clock)
- One or more serial data pins, AXRn, whose serializers are configured to transmit

For more details on MCASP transmitting serializers clock and frame sync options, refer to the Section 12.1.2.4.2.1, *Transmit Clock*, and Section 12.1.2.4.2.3, *Frame-Sync Generator*.

Similarly, to receive data in the TDM transfer mode requires a minimum set of pins:

- ACLKR - receive bit clock

- AFSR - receive frame sync (or commonly called left/right clock)
- One or more serial data pins, AXRn, whose serializers are configured to receive

For more details on MCASP receiving serializers clock and frame sync options, refer to Section 12.1.2.4.2.2, *Receive Clock*, and Section 12.1.2.4.2.3, *Frame-Sync Generator*.

The control registers must be configured as follows for the TDM mode. The TDM mode specific bit fields are highlighted in bold:

- *MCASP_PFUNC*: The clock, frame, data pins must be configured for MCASP function.
- *MCASP_PDIR*: The clock, frame, data pins must be configured to the direction desired.
- *MCASP_PDOUT*, *MCASP_PDIN*, *MCASP_PDCLR*: Not applicable. Leave at default.
- *MCASP_GBLCTL*: Follow the initialization sequence is described in the Section 12.1.2.5.2, *MCASP Operational Modes Configuration*.
- *MCASP_AMUTE*: Leave this register at default state.
- MCASP_DLBCTL: If loopback mode is desired, configure this register according to Section 12.1.2.4.14, otherwise leave this register at default.
- MCASP_DITCTL: DITEN must be left at default 0 to select TDM mode (transmitters only).
- MCASP_RMASK/MCASP_XMASK: Mask desired bits according to Section 12.1.2.4.4, *MCASP Format Units*.
- MCASP_RFMT/MCASP_XFMT: Program all fields according to data format desired. See the Section 12.1.2.4.4, *MCASP Format Units*.
- MCASP_AFSRCTL/MCASP_AFSXCTL: Set RMOD/XMOD bits to (0x2 - 0x20) for Rx/Tx (2- 32 slots) TDM mode. In addition, set RMOD to 0x180 if 384-slot TDM stream has to be received by MCASP. Configure other fields as desired.
- *MCASP_ACLKRCTL/MCASP_ACLKXCTL*: Program all fields according to bit clock desired. For more inforamtion, refer to Section 12.1.2.4.2, *MCASP Clock and Frame-Sync Configurations*.
- *MCASP_AHCLKRCTL/MCASP_AHCLKXCTL*: Program all fields according to high-frequency clock desired. For more details, refer to Section 12.1.2.4.2, *MCASP Clock and Frame-Sync Configurations*.
- MCASP_RTDM/MCASP_XTDM: Program all fields according to the time slot characteristics desired.
- MCASP_XINTCTL: Program all fields according to transmit interrupts desired.
- MCASP_RCLKCHK/MCASP_XCLKCHK: Program all fields according to clock checking desired.
- MCASP_SRCTLn: Program all fields according to serializer operation desired (n = 0 to 15).

Note

The MCASP_DITCSRAi, MCASP_DITCSRBi, MCASP_DITUDRAi, MCASP_DITUDRBi (i = 0 to 5) settings are NOT applicable in TDM transfer modes. They have to be kept at their default values.

12.1.2.4.9.2.1 TDM Time Slots Generation and Processing

TDM mode on the MCASP can extend to support multiprocessor applications, with up to 32 time slots per frame. For each of the time slots, the MCASP may be configured to participate or to be inactive by configuring MCASP_XTDM and/or MCASP_RTDM registers.

The TDM sequencer (separate ones for transmit and receive) functions in this mode. The TDM sequencer counts the slots beginning with the frame sync. For each slot, the TDM sequencer checks the respective bit in either MCASP_XTDM or MCASP_RTDM register to determine if the MCASP transmits/receives in that time slot.

Note

If a MCASP_XTDM/MCASP_RTDM bit defines an active slot (number of slot matches the bit position), the MCASP functions normally during that time slot; otherwise, the MCASP is inactive during that time slot; no update to the buffer occurs, and no event is generated. MCASP (transmit only) data pins are automatically set to a high-impedance state, 0, or 1 during that slot, as determined by bitfield MCASP_SRCTLn[3-2] DISMOD (n = 0 to 15).

Figure 12-28 shows when the transmit DMA event - XINT is generated. See Section 12.1.2.4.10.1, *Data Ready Status and Event/Interrupt Generation* for details on data ready and the initialization period indication. The transmit DMA event for an active time slot (slot N) is generated during the previous time slot (slot N - 1), regardless of the previous time slot (slot N - 1) being active or inactive.

During an active transmit time slot (slot N), if the next time slot (slot N + 1) is configured to be active, the copy from XRBUFn to XRSRn generates the DMA event for time slot N + 1. If the next time slot (slot N + 1) is configured to be inactive, then the DMA event will be delayed to time slot M - 1. In this case, slot M is the next active time slot. The DMA event for time slot M is generated during the first bit time of slot M - 1.

The receive DMA event is generated after data is received in the buffer (looks back in time). If a time slot is disabled, then no data is copied to the buffer for that time slot and no DMA event is generated.

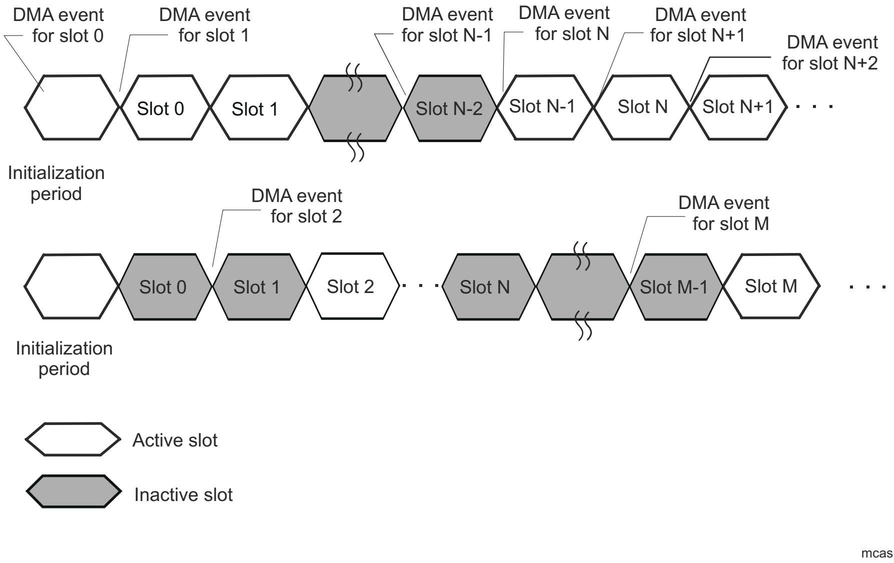


Figure 12-28. Transmit DMA Event (XINT) Generation in TDM Time Slots

12.1.2.4.9.2.2 Special 384-Slot TDM Mode for Connection to External DIR

The MCASP receiver also supports a 384 time slot TDM mode (DIR mode), to support S/PDIF receiver ICs whose natural block (block corresponds to MCASP frame) size is 384 samples. The receive TDM time slot register (MCASP_RTDM) should be programmed to all 1s during reception of a DIR block. Other TDM functionalities (for example, inactive slots) are not supported (only the slot counter counts the 384 subframes in a block). To receive data in DIR mode, the following pins are typically needed:

- ACLKR - receive bit clock
- AFSR - receive frame sync (or commonly called left/right clock)
- In this mode, AFSR should be connected to a DIR which outputs a start of block signal, instead of LRCLK
- One or more serial data pins, AXRn, whose serializers have been configured to receive
- For this special DIR mode, the control registers can be configured just as for TDM mode, except set MCASP_AFSRCTL[15-7] RMOD bit field to 384 (0x180) to receive 384 time slots

12.1.2.4.9.3 DIT Transfer Mode

The DIT transfer mode of the MCASP also supports transmission of audio data in S/PDIF, AES-3, and IEC-60958 formats. These formats are designed to carry audio data between different systems through an optical or coaxial cable. The DIT mode applies only to a serializer configured as transmitter, not as receiver. For a description of the S/PDIF format, see Section 12.1.2.2.2.5, *S/PDIF Coding Format*.

12.1.2.4.9.3.1 Transmit DIT Encoding

When the MCASP operates in DIT mode, the data transmitted is output as a biphase-mark encoded bitstream, with preamble, channel status, user data, validity, and parity automatically stuffed into the bitstream by the MCASP. The MCASP includes separate validity bits for even/odd subframes and two 384-bit RAM modules to hold channel status and user data bits.

Note

The transmit TDM time slot register (MCASP_XTDM) should be programmed to all 1s during DIT mode. TDM functionality is not supported in DIT mode, except that the TDM slot counter counts the DIT subframes.

To transmit data in DIT mode, the following pins are typically required:

- AHCLKX – transmit high-frequency controller clock (The internal clock source can be used instead.)
- One serial data pin (AXRn) of a serializer n configured to transmit.

For DIT Mode Transmission Data Alignment Settings see Section 12.1.2.4.4.1.2, *DIT Mode Transmission Data Alignment Settings*.

If the MCASP is configured to transmit in the DIT mode on more than one serial data pin, the bit streams on all pins will be synchronized. In addition, although they will carry unique audio data, they will carry the same channel status, user data, and validity information.

The actual 24-bit audio data must always be in bit positions 23–0 after passing through the first three stages of the transmit format unit.

12.1.2.4.9.3.2 Transmit DIT Clock and Frame-Sync Generation

The DIT transmitter works only in the following configuration:

- In the transmit frame control register (MCASP_AFSXCTL):
  - Internally generated transmit frame sync, FSXM = 1
  - Rising-edge frame sync, FSXP = 0
  - Bit-width frame sync, FXWID = 0
  - 384-slot TDM, XMOD = 1 1000 0000b
- In the transmit clock control register (*MCASP_ACLKXCTL*), ASYNC = 1
- In the transmit bitstream format register (MCASP_XFMT), XSSZ = 1111 (32-bit slot size)

All combinations of AHCLKX and ACLKX are supported.

The following summarizes the register configurations required for DIT mode. DIT mode-specific bit fields are in bold face:

- *MCASP_PFUNC*: The data pin - AXRn must be configured for MCASP function. If AHCLKX is used, it must also be configured for MCASP function. Other pins can be configured to function as GPIOs, if desired.
- *MCASP_PDIR*: The data pin must be configured as output. If internal clock source AUXCLK is used as the reference clock, it may be output as the AHCLKX device level signal by configuring AHCLKX pin as an output.
- *MCASP_GBLCTL*: Global initialization
- *MCASP_AMUTE*: Leave this register at default state.
- MCASP_DITCTL: The DITEN bit must be set to 0b1 to enable DIT mode. Configure other bits as desired.
- MCASP_XMASK: Mask the desired bits, depending upon left-aligned or right-aligned internal data.
- MCASP_XFMT: XDATDLY = 0. XRVRS = 0. XPAD = 0. XSSZ = Fh (32-bit slot). XBUSEL = configured as desired. The XROT bit is configured, as described in the Section 12.1.2.4.4.1.2 .
- MCASP_AFSXCTL: Configure the bits according to former discussions.
- *MCASP_ACLKXCTL*: ASYNC = 1. Program the CLKXDIV bits to obtain the bit clock rate desired. CLKXM = 1.
- *MCASP_AHCLKXCTL*: Program the HCLKXDIV bits to obtain the high-frequency bit clock rate desired.
- MCASP_XTDM: Set to FFFF FFFFh for all active slots for DIT transfers.
- MCASP_XINTCTL: Program all fields according to the interrupts desired.
- MCASP_XCLKCHK: Program all fields according to the clock checking desired.
- MCASP_SRCTLn: Set SRMOD = 1 (transmitter) for the DIT pins (n = 0 to 15).
- MCASP_DITCSRAi and MCASP_DITCSRBi: Program the channel status bits as desired (i = 0 to 5).
- MCASP_DITUDRAi and MCASP_DITUDRBi: Program the user data bits as desired (i = 0 to 5).

Note

In DIT mode, the transmitter can support a 192 kHz frame rate (stereo) on up to 2 serial data pins simultaneously (note that the internal bit clock for DIT runs two times faster than the equivalent bit clock for TDM (I2S) mode, due to the need to generate Biphase Mark Encoded Data - see Section 12.1.2.2.2.5.1, *Biphase-Mark Code*).

12.1.2.4.9.3.3 DIT Channel Status and User Data Register Files

The channel status registers (MCASP_DITCSRAi and MCASP_DITCSRBi) and user data registers (MCASP_DITUDRAi and MCASP_DITUDRBi) are not double-buffered. Typically, programmers use one of the synchronizing interrupts, such as the last slot, to create an event at a safe time so the register may be updated. In addition, the software reads the transmit TDM slot counter to determine which word of the register is being used (i = 0 to 5).

It is a software requirement to avoid writing to the word of user data and channel status that are being used to encode the current time slot; otherwise, it is undetermined whether old or new data is used to encode the bitstream.

The DIT subframe format is defined in Section 12.1.2.2.2.5.2, *S/PDIF Subframe Format*. The channel status information (C) and user data (U) are defined in the following DIT control registers:

- *MCASP_DITCSRA0* to *MCASP_DITCSRA5*: The 192 bits in these six registers contain the channel status information for the left channel within each frame.
- *MCASP_DITCSRA0* to *MCASP_DITCSRA5*: The 192 bits in these six registers contain the channel status information for the right channel within each frame.
- *MCASP_DITCSRA0* to *MCASP_DITCSRA5*: The 192 bits in these six registers contain the user data information for the left channel within each frame.
- *MCASP_DITCSRA0* to *MCASP_DITCSRA5*: The 192 bits in these six registers contain the user data information for the right channel within each frame.
- The S/PDIF block format is shown in Figure 12-19. There are 192 frames within a block (frame 0 to frame 191). There are two subframes within each frame (subframes 1 and 2 for the left and right channels, respectively).

The channel status and user data information sent on each subframe is summarized in Table 12-16.

Table 12-16. Channel Status and User Data for Each DIT Block

Frame	Subframe	Preamble	Channel Status Defined in:	User Data Defined in:
Defined by DITCSRA0, DITCSRB0, DITUDRA0, DITUDRB0				
0	1 (L)	B	DITCSRA0[0]	DITUDRA0[0]
0	2 (R)	W	DITCSRB0[0]	DITUDRB0[0]
1	1 (L)	M	DITCSRA0[1]	DITUDRA0[1]
1	2 (R)	W	DITCSRB0[1]	DITUDRB0[1]
2	1 (L)	M	DITCSRA0[2]	DITUDRA0[2]
2	2 (R)	W	DITCSRB0[2]	DITUDRB0[2]
…	…	…	…	…
31	1 (L)	M	DITCSRA0[31]	DITUDRA0[31]
31	2 (R)	W	DITCSRB0[31]	DITUDRB0[31]
Defined by DITCSRA1, DITCSRB1, DITUDRA1, DITUDRB1				
32	1 (L)	M	DITCSRA1[0]	DITUDRA1[0]
32	2 (R)	W	DITCSRB1[0]	DITUDRB1[0]
…	…	…	…	…
63	1 (L)	M	DITCSRA1[31]	DITUDRA1[31]
63	2 (R)	W	DITCSRB1[31]	DITUDRB1[31]
Defined by DITCSRA2, DITCSRB2, DITUDRA2, DITUDRB2				
64	1 (L)	M	DITCSRA2[0]	DITUDRA2[0]
64	2 (R)	W	DITCSRB2[0]	DITUDRB2[0]

Table 12-16. Channel Status and User Data for Each DIT Block (continued)

Frame	Subframe	Preamble	Channel Status Defined in:	User Data Defined in:
…	…	…	…	…
95	1 (L)	M	DITCSRA2[31]	DITUDRA2[31]
95	2 (R)	W	DITCSRB2[31]	DITUDRB2[31]
Defined by DITCSRA3, DITCSRB3, DITUDRA3, DITUDRB3				
96	1 (L)	M	DITCSRA3[0]	DITUDRA3[0]
96	2 (R)	W	DITCSRB3[0]	DITUDRB3[0]
…	…	…	…	…
127	1 (L)	M	DITCSRA3[31]	DITUDRA3[31]
127	2 (R)	W	DITCSRB3[31]	DITUDRB3[31]
Defined by DITCSRA4, DITCSRB4, DITUDRA4, DITUDRB4				
128	1 (L)	M	DITCSRA4[0]	DITUDRA4[0]
128	2 (R)	W	DITCSRB4[0]	DITUDRB4[0]
…	…	…	…	…
159	1 (L)	M	DITCSRA4[31]	DITUDRA4[31]
159	2 (R)	W	DITCSRB4[31]	DITUDRB4[31]
Defined by DITCSRA5, DITCSRB5, DITUDRA5, DITUDRB5				
160	1 (L)	M	DITCSRA5[0]	DITUDRA5[0]
160	2 (R)	W	DITCSRB5[0]	DITUDRB5[0]
…	…	…	…	…
191	1 (L)	M	DITCSRA5[31]	DITUDRA5[31]
191	2 (R)	W	DITCSRB5[31]	DITUDRB5[31]

12.1.2.4.10 MCASP Data Transmission and Reception

The MCASP is serviced by writing data to the MCASP_XBUFn registers for transmit operations, and by reading data from the MCASP_RBUFn registers for receive operations. The MCASP sets status flags and notifies the software whenever data is ready to be serviced. The Section 12.1.2.4.10.1, *Data Ready Status and Event/ Interrupt Generation*, discusses data-ready status in details (n = 0 to 15).

The MCASP transmit/receive XRBUFn buffer can be accessed through one of the two peripheral ports of the device:

- DATA port: This port is dedicated to DMA initiated data transfers on the device for MCASP transmit (Tx) purposes.
- Configuration bus (CFG): The configuration bus- CFG port is used for peripheral configuration control and receive/transmit data transfers initiated by the host CPU in the device.

Section 12.1.2.4.10.1.3, *Transfers Through the Data Port (DATA)*, and Section 12.1.2.4.10.1.4, *Transfers Through the Configuration Bus (CFG),* discuss how to perform transfers through the data port (DATA) and the configuration port (CFG), respectively.

A device CPU and DMA usages are discussed in Section 12.1.2.4.10.1.5, *Using the device CPUs for MCASP Servicing*, and Section 12.1.2.4.10.1.6, *Using the DMA for MCASP Servicing*, respectively.

MCASP DATA port allows DMAs to access the MCASP transmit buffer more efficiently on the CBASS0, using burst transfers. The physical addresses to access these registers are listed in *DMA Registers*.

12.1.2.4.10.1 Data Ready Status and Event/Interrupt Generation

12.1.2.4.10.1.1 Transmit Data Ready

The transmit data ready flag - XDATA in the MCASP_XSTAT register reflects the data ready status of XRBUFn buffers for all of the active slot transmitting serializers. The XDATA flag is set whenever data is transferred from a transmitting serializer buffer - XRBUFn to its corresponding XRSRn shift register. Thus, the XDATA bit indicates the global event that some of the serializers data buffer - XRBUFn is emptied and ready to accept new data from the host (CPU or DMA). The transmit data ready event is individually indicated per serializer in its corresponding control register MCASP_SRCTLn[4] XRDY status bit. When this bit is set to 0b1, it notifies to host that this serializer Tx buffer must be serviced (written). When MCASP_XBUFn is written to by the host, the MCASP_SRCTLn[4] XRDY is deasserted to 0b0. As XDATA global flag is an OR-event of all active serializers XRDY flags, it indicates to software the moment, when write service operation has to be initiated by the MCASP host (XDATA=0b1). The XRDY flags have to be sequentially scanned by user software to determine which serializer MCASP_XBUFn register has to be currently written. Once all requested MCASP_XBUFn are written, the serializers control XRDY flags are cleared to 0b0. As a consequence, XDATA flag is deasserted to 0b0, to indicate to SW that write operation is completed for all serializers.

The global XDATA flag can be cleared when the MCASP_XSTAT[5] XDATA bit is written to 0b1, or once MCASP_XBUFn registers of all the serializers, that have previously raised their XRDY flags, are written with corresponding active slot data by the host.

Whenever XDATA is set, the XINT event is automatically generated on MCASP[0-2]_XMIT_DMA_EVT line (if enabled in the *MCASP_XEVTCTL* register) to notify the DMA of the MCASP_XBUFn empty status. An interrupt - MCASP[0-2]_XMIT_INTR_PEND can be also generated if the XDATA interrupt is enabled in the MCASP_XINTCTL register (for details, see Section 12.1.2.4.12.1, *Transmit Data Ready Interrupt*).

For DMA requests, the MCASP does not require that MCASP_XSTAT register be read between DMA events. This means that, even if MCASP_XSTAT register already has the XDATA flag set to 1 from a previous request, the next transfer triggers another DMA request.

Because the serializer acts in lockstep, only one DMA event is generated to indicate that the transmit serializer is ready to be written to with new data.

Figure 12-29 shows the timing details of when XINT is generated at the MCASP boundary. In this example, as soon as the last bit (A0) of word A is transmitted, the MCASP sets the XDATA flag and generates an XINT event. However, it takes up to five MCASP interface clocks (XINT latency) before XINT is active at the MCASP boundary. Upon XINT, the CPU can begin servicing the MCASP by writing word C into the MCASP_XBUFn (service time). The CPU must write word C into the MCASP_XBUFn within the setup time required by the MCASP (setup time) (n = 0 to 15).

The maximum service time (see Figure 12-29) can be calculated as:

Service Time = Time Slot – XINT Latency –Setup Time

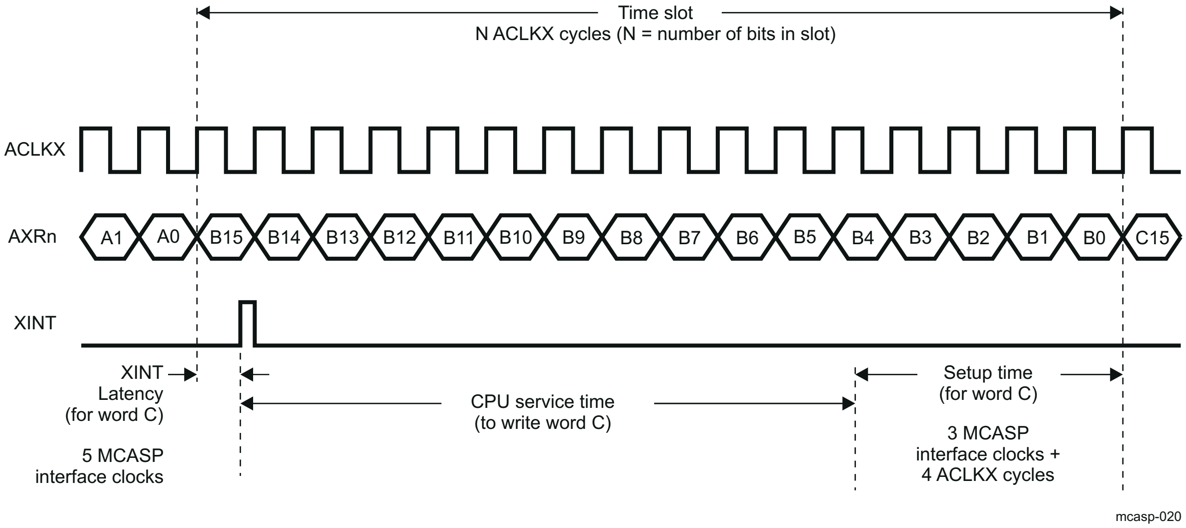


Figure 12-29. Service Time Upon Transmit DMA Event (XINT)

12.1.2.4.10.1.2 Receive Data Ready

Similarly, the receive data ready flag - RDATA in the MCASP_RSTAT register reflects the data ready status of XRBUFn buffers for all of the active slot receiving serializers. The RDATA flag is set whenever data is transferred from a receiving serializer shift register XRSRn to its corresponding XRBUFn data buffer. Thus, the RDATA bit indicates the global event that some of the receivers data buffer - RXBUFn already contains received data (this is, a buffer is full) and is ready to transfer it to the host. The receive data ready event is individually indicated per serializer in its corresponding control register MCASP_SRCTLn [5] RRDY status bit. When this bit is set to 0b1, it notifies to host that this serializer Rx buffer must be serviced (read). When MCASP_RBUFn register is read from the host, the MCASP_SRCTLn [5] RRDY bit is deasserted to 0b0. As RDATA global flag is an OR-event of all active serializers RRDY flags, it indicates to software the moment, when read service operation has to be initiated by the MCASP host (RDATA = 0b1). The RRDY flags have to be sequentially scanned by user software to determine which serializer MCASP_RBUFn register has to be currently read. Once all requested MCASP_RBUFn registers are read, the serializers control RRDY flags are cleared to 0b0. As a consequence, RDATA flag is deasserted to 0b0, to indicate to SW that read operation is completed for all serializers.

The global RDATA flag can be cleared when the MCASP_RSTAT[5] RDATA bit is written to 0b1, or once MCASP_RBUFn registers of all the serializers, that have previously raised their RRDY flags, are read by the host.

Whenever RDATA flag is set, the RINT event is automatically generated on MCASP[0-2]_REC_DMA_EVT line (if enabled in the MCASP_PIDTCTL register) to notify the DMA of the MCASP_RBUFn full status. An interrupt - MCASP[0-2]_REC_INTR_PEND can be also generated if the RDATA interrupt is enabled in the MCASP_RINTCTL register (for details, see Section 12.1.2.4.12.1, *Receive Data Ready Interrupt*).

Figure 12-30 shows the timing details of when RINT event is generated at the MCASP boundary. In this example, as soon as the last bit (bit A0) of Word A is received, the MCASP sets the RDATA flag and generates an RINT event. However, it takes up to five MCASP interface clocks (RINT Latency) before RINT is active at the MCASP boundary. Upon RINT, the CPU can begin servicing the MCASP by reading Word A from the MCASP_RBUFn (service time). The CPU must read Word A from the MCASP_RBUFn register no later than the setup time required by the MCASP (Setup Time) (n = 0 to 15).

The maximum service time (see Figure 12-30) can be calculated as:
Service Time = Time Slot - RINT Latency - Setup Time

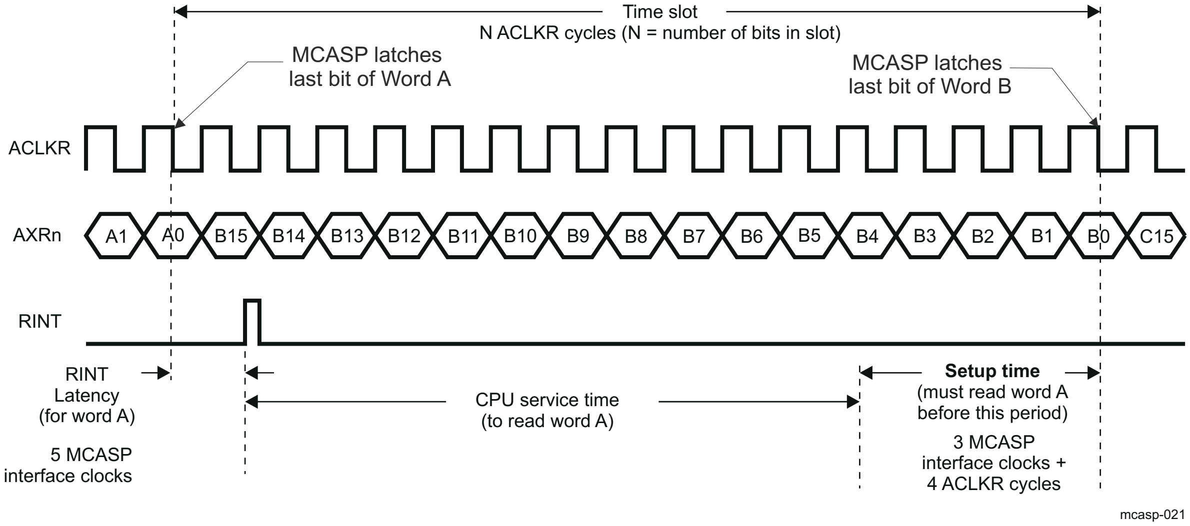


Figure 12-30. CPU Service Time Upon Receive Event (RINT)

12.1.2.4.10.1.3 Transfers Through the Data Port (DATA)

CAUTION

To perform internal transfers through the DATA port, clear the XBUSEL/RBUSEL bit to 0b0 in the MCASP_XFMT/MCASP_RFMT register, respectively. Failure to do so may result in software malfunction.

In a typical MCASP transfer scenario, the DMA Controller write accesses the XRBUFn transmit buffer through the MCASP data port (DATA) on CBASS0 Interconect. CPU hosts can access both XRBUFn transmit and receive data buffers on their corresponding DATA port address via DATA port corresponding address. To perform transfers through the DATA port, simply have the DMA Controller write the MCASP Tx buffer through Interconect DATA port location. Refer to *DMA Registers*. Although the transfer is passed through an integrated AFIFO transmit/receive buffer, the host (DMA or CPU) must follow the described below procedure to access the data buffers of each serializer, regardless the AFIFO is enabled or disabled. The AFIFO operation is described in Section 12.1.2.4.11.

For accesses through the DATA port, the DMA/CPU services all the serializers through accessing only a single address. In addition, as can be seen in *DMA Registers*, the same physical DATA port address is used regardless of a read or write access is performed. The MCASP automatically cycles through the active slot transmitting/receiving serializers, internally generating the appropriate offsets.

Note

DATA port allows the DMA/CPU to automatically access only the data buffers. There is no way for DMA/CPU to access the MCASP configuration registers addressing their corresponding MCASP DATA port.

For transmit operations through the DATA port, the host must always write to the same transmit buffer DATA port address (which is same than the receive buffer DATA port adress) to service all of the active slot transmitting serializers. Regardless of MCASP serializer 0 being configured inactive or active, the user software must always configure the destination address to match the DATA port location of TXBUF buffer (See *DMA Registers*).

In addition, the DMA/CPU must write the buffers of all transmitting serializers in incremental (although not necessarily consecutive) order. For example, if only serializers 1 and 3 are set up as active transmitters, to the same transmit buffer DATA port address twice - first data for serializer 1 and second data for serializer 3 upon each transmit data ready event. This exact servicing order must be followed so that data appears in the appropriate serializers.

Note

For write transfers through MCASP DATA port it is preferable to use DMA on corresponding Interconect. This is because DMAs initiated traffic gets better advantage of the burst transfers supported by DATA port.

For receive operations through the DATA port, the DMA/CPU must always read from the same receive buffer DATA port address (which is same than the transmit buffer DATA port adress) to service all of the active slot receiving serializers. Regardless of MCASP serializer 0 being configured inactive or active, the user software must always configure the DMA/CPU source address to match the DATA port location of RXBUF buffer (See *DMA Registers*).

In addition, reads from the receive buffer for all active slot receiving serializers through the Rx DATA port return data in incremental (although not necessarily consecutive) order. For example, if serializers 0, 1 and 3 are set up as active receivers, the CPU should read from the same receive buffer DATA port address three times to obtain data for serializers 0,1 and 3 in this exact order, upon each receive data ready event.

Note

To service a serializer for a transmit or receive operation through the MCASP DATA port, the initiator always writes (preferably DMA) and reads from the same address (refer to *DMA Registers*), respectively.

Note

When transmitting through the DATA port, the DMA/CPU must write data (at the same address) to each serializer configured as *active* (active slot selected in MCASP_XTDM) and *transmit* (Tx enabled in MCASP_SRCTLn) within each time slot. Failure to do so results in a buffer underrun condition (see Section 12.1.2.4.15.1, *Buffer Underrun Error - Transmitter*). Similarly, when DMA/CPU receives, data must be read from each serializer configured as *active* (active slot selected in MCASP_RTDM) and *receive* (Rx enabled in MCASP_SRCTLn) within each time slot. Failure to do results in a buffer overrun condition (see Section 12.1.2.4.15.2, *Buffer Overrun Error - Receiver*) (n = 0 to 15).

12.1.2.4.10.1.4 Transfers Through the Configuration Bus (CFG)

CAUTION

To perform internal transfers through the configuration bus, set the XBUSEL/RBUSEL bit to 1 in the MCASP_XFMT/MCASP_RFMT registers, respectively. Failure to do so may result in software malfunction.

Note

MCASP[0-2] whose data ports are accessible directly via CBASS0 do not support FIFO/constant addressing modes. Incrementing transfers must be used instead.

In this method, the CPU accesses the XRBUFn transmit or receive buffer through corresponding configuration bus (CFG) address.

The exact XRBUFn transmit/receive buffer physical address for any particular serializer is determined by adding the transmit/receive buffer alias register offset for that particular serializer to the base address of MCASP CFG port actual for CBASS0 accesses. The XRBUFn buffer of the n-th serializer configured as a transmitter is aliased - MCASP_XBUFn in the CFG port address space. For example, the XRBUF2 transmit buffer is mapped as the MCASP_XBUF2 register. Similarly, the XRBUFn buffer of the n-th serializer configured as a receiver is aliased - MCASP_RBUFn in the CFG port address space. For example, the XRBUF3 receive buffer is mapped as the MCASP_RBUF3 register.

Accessing the XRBUF through the DATA port (see Section 12.1.2.4.10.1.3) is different than CFG port accesses because the DATA port access demands the same physical address, regardless of transfer direction or current channel index , while accessing through the peripheral configuration port - CFG, the CPU must provide the exact MCASP_XBUFn or MCASP_RBUFn address upon accessing n-th serializer TX or RX buffer, respectively. For more details about MCASP_XBUFn and MCASP_RBUFn addresses corresponding to MCASP CFG port, see *CFG Registers* (n = 0 to 15).

12.1.2.4.10.1.5 Using a Device CPU for MCASP Servicing

The device CPUs can be used to service the MCASP transmit channels through interrupts (upon MCASP[0-2]_XMIT_INTR_PEND and MCASP[0-2]_REC_INTR_PEND interrupts). Because these interrupt events are connected to device COMPUTE_CLUSTER0, PRUSS, MAIN2MCU_LVL_INTRTR0, R5FSS0/1_INTRTR0, C66SS0/1_INTRTR0, R5FSS0/1 modules, they could be software mapped to input interrupt lines of any device CPU. Another way to service the transmit and receive channels, a polling of the XDATA bit in the MCASP_XSTAT register and RDATA bit in the MCASP_RSTAT register can be performed by device CPUs, respectively. As discussed in Section 12.1.2.4.10.1.3, *Transfers Through the Data Port (DATA)*, and Section 12.1.2.4.10.1.4, *Transfers Through the Configuration Bus (CFG)*, the device CPUs can access MCASP XRBUF serializer buffer through their corresponding DATA and CFG port locations.

To use the device CPUs to service the MCASP through interrupts, the XDATA/RDATA bit must be enabled in the respective MCASP_XINTCTL/MCASP_RINTCTL registers, to generate interrupts MCASP[0-2]_XMIT_INTR_PEND/MCASP[0-2]_REC_INTR_PEND to the device CPUs upon data ready

12.1.2.4.10.1.6 Using the DMA for MCASP Servicing

Note

The associated static Transfer Request (TR) operations of PDMA0, located in front of MCASP, must be configured to match the MCASP configuration. For more information, refer to chapter *DMA Controllers*.

The typical scenario is to use the DMA to service the MCASP transmit and receive logic through the DATA port. The transfer passes through integrated AFIFO transmit/receive buffer. If AFIFO is enabled, DMA requests are collected and fed to a device DMA controller (see Figure 12-20). The data transfer is managed by the AFIFO according to generated transmit and receive events in the MCASP and data is fed to transmit buffers and fetched from receive buffers as described in Section 12.1.2.4.11, *MCASP Audio FIFO (AFIFO)*. The generation of transmit and receive request is described below. After generation of transmit/receive DMA events from MCASP module, these events are collected in AFIFO and on specific AFIFO conditions described in Section 12.1.2.4.11, *MCASP Audio FIFO (AFIFO)* the requests (transmit or receive) are forwarded to a DMA controller via MCASP[0-2]_XMIT_DMA_EVT and MCASP[0-2]_REC_DMA_EVT outputs. If the AFIFO is disabled (default state) it is transperrant for the MCASP module and all request are directly sent to the DMA controller.

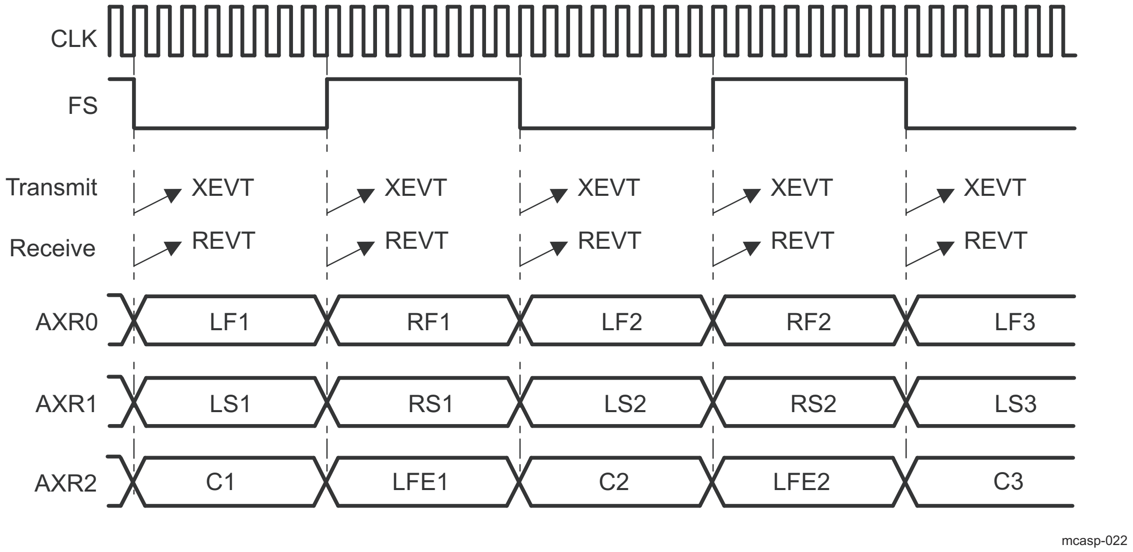


Figure 12-31. DMA Transmit and Receive Event in an Audio Example – One Event

In transmit mode, the DMA event - XINT (MCASP[0-2]_XMIT_DMA_EVT output), which is triggered upon each XDATA transition from 0 to 1, is used to service the MCASP TXBUFn transmit buffers. In receive mode, the DMA event RINT (MCASP[0-2]_REC_DMA_EVT output) which is triggered upon each RDATA transition from 0 to 1, is used to service the MCASP RXBUFn receive buffers.

Figure 12-31 is an example of an audio system with six audio channels (LF, RF, LS, RS, C and LFE) transmitted or received through the MCASP signals - AXR0, AXR1 and AXR2. It shows the points at which events XINT/RINT are triggered.

In Figure 12-31, a Tx DMA event XINT is triggered on each time slot. In the example, XINT is triggered for each of the transmit audio channel time slot (time slot for channels LF, LS, and C; and time slot for channels RF, RS, LFE). Transmit DMA events are generated automatically upon transmit data ready, provided that DMA TX requests generation is enabled in the *MCASP_XEVTCTL* register. Similarly, Rx DMA event RINT is triggered for each of the receive audio channel time slot. Receive DMA events are generated automatically upon receive data ready, provided that DMA RX requests generation is enabled in the MCASP_PIDTCTL register.

12.1.2.4.11 MCASP Audio FIFO (AFIFO)

The AFIFO contains two FIFOs: one Read FIFO (RFIFO), and one Write FIFO (WFIFO). The RFIFO and the WFIFO are the same size: 64 32-bit Words. To ensure backward compatibility with existing software, both the

Read and Write FIFOs are disabled by default. See Figure 12-32 for a high-level block diagram of the AFIFO. The AFIFO may be enabled/disabled and configured via the MCASP_WFIFOCTL and MCASP_RFIFOCTL registers. Note that if the Read or Write FIFO is to be enabled, it must be enabled prior to initializing the receive/transmit section of the MCASP.

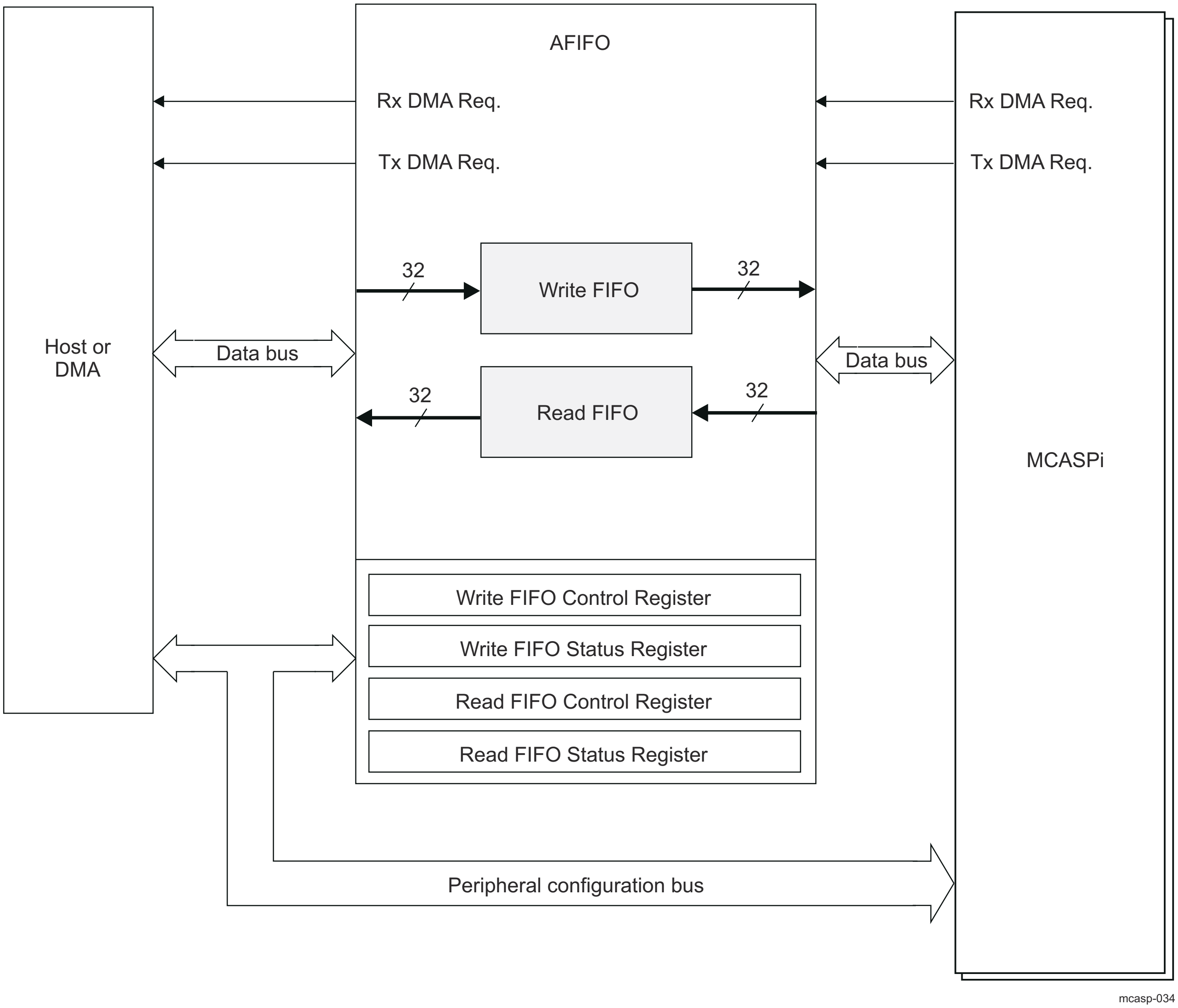


Figure 12-32. MCASP Audio FIFO (AFIFO) Block Diagram

12.1.2.4.11.1 AFIFO Data Transmission

When the Write FIFO is disabled, transmit DMA requests pass through directly from the MCASP to the host/DMA controller. Whether the WFIFO is enabled or disabled, the MCASP generates transmit DMA requests as needed; the AFIFO is “invisible” to the MCASP. When the Write FIFO is enabled, transmit DMA requests from the MCASP are sent to the AFIFO, which in turn generates transmit DMA requests to the host/DMA controller. If the Write FIFO is enabled, upon a transmit DMA request from the MCASP, the WFIFO writes WNUMDMA 32-bit words to the MCASP if and when there are at least WNUMDMA words in the Write FIFO. If there are not, the WFIFO waits until this condition has been satisfied. At that point, it writes WNUMDMA words to the MCASP (see description for the MCASP_WFIFOCTL[7-0] WNUMDMA). If the host CPU writes to the Write FIFO, independent of a transmit DMA request, the WFIFO will accept host writes until full. After this point, excess data will be discarded. Note that when the WFIFO is first enabled, it will immediately issue a transmit DMA request to the host. This is because it begins in an empty state, and is therefore ready to accept data.

12.1.2.4.11.1.1 Transmit DMA Event Pacer

The AFIFO may be configured to delay making a transmit DMA request to the host until the Write FIFO has enough space for a specified number of words. In this situation, the number of transmit DMA requests to the host or DMA controller is reduced. If the Write FIFO has space to accept WNUMEVT 32-bit words, it generates a transmit DMA request to the host and then waits for a response. Once WNUMEVT words have been written to the FIFO, it checks again to see if there is space for WNUMEVT 32-bit words. If there is space, it generates another transmit DMA request to the host, and so on. In this fashion, the Write FIFO will attempt to stay filled. Note that if transmit DMA event pacing is desired, MCASP_WFIFOCTL[15-8] WNUMEVT bit field should be set to a non-zero integer multiple of the value in MCASP_WFIFOCTL[7-0] WNUMDMA bit field. If transmit DMA event pacing is not desired, then the value in MCASP_WFIFOCTL[15-8] WNUMEVT bit field should be set equal to the value in MCASP_WFIFOCTL[7-0] WNUMDMA bit field.

12.1.2.4.11.2 AFIFO Data Reception

When the Read FIFO is disabled, receive DMA requests pass through directly from MCASP to the host/DMA controller. Whether the RFIFO is enabled or disabled, the MCASP generates receive DMA requests as needed; the AFIFO is “invisible” to the MCASP. When the Read FIFO is enabled, receive DMA requests from the MCASP are sent to the AFIFO, which in turn generates receive DMA requests to the host/DMA controller. If the Read FIFO is enabled and the MCASP makes a receive DMA request, the RFIFO reads RNUMDMA 32-bit words from the MCASP, if and when the RFIFO has space for RNUMDMA words. If it does not, the RFIFO waits until this condition has been satisfied; at that point, it reads RNUMDMA words from the MCASP (see description for theMCASP_RFIFOCTL[7-0] RNUMDMA). If the host CPU reads the Read FIFO, independent of a receive DMA request, and the RFIFO at that time contains less than RNUMEVT words, those words will be read correctly, emptying the FIFO.

12.1.2.4.11.2.1 Receive DMA Event Pacer

The AFIFO may be configured to delay making a receive DMA request to the host until the Read FIFO contains a specified number of words. In this situation, the number of receive DMA requests to the host or DMA controller is reduced. If the Read FIFO contains at least RNUMEVT 32-bit words, it generates a receive DMA request to the host and then waits for a response. Once RNUMEVT 32-bit words have been read from the RFIFO, the RFIFO checks again to see if it contains at least another RNUMEVT words. If it does, it generates another receive DMA request to the host, and so on. In this fashion, the Read FIFO will attempt to stay empty. Note that if receive DMA event pacing is desired, MCASP_RFIFOCTL[15-8] RNUMEVT bit field should be set to a non-zero integer multiple of the value in MCASP_RFIFOCTL[7-0] RNUMDMA bit field. If receive DMA event pacing is not desired, then the value in MCASP_RFIFOCTL[15-8] RNUMEVT bit field should be set equal to the value in MCASP_RFIFOCTL[7-0] RNUMDMA bit field.

12.1.2.4.11.3 Arbitration Between Transmit and Receive DMA Requests

If both the WFIFO and the RFIFO are enabled and a transmit DMA request and receive DMA request occur simultaneously, priority is given to the transmit DMA request. Once a transfer is in progress, it is allowed to complete. If only the WFIFO is enabled and a transmit DMA request and receive DMA request occur simultaneously, priority is given to the transmit DMA request. Once a transfer is in progress, it is allowed to complete. If only the RFIFO is enabled and a transmit DMA request and receive DMA request occur simultaneously, priority is given to the receive DMA request. Once a transfer is in progress, it is allowed to complete.

12.1.2.4.12 MCASP Events and Interrupt Requests

Table 12-17 lists all the transmit event flags. Table 12-18 lists all the Receive event flags. Source of each of these TX/RX events can be a TX/RX channel from any MCASP serializer configured as transmitter or receiver respectively.

Table 12-17. TX Events

Event Mask[1]	Event Flag	Map to [1]	Description
MCASP_XINTCTL[0] XUNDRN	MCASP_XSTAT[0] XUNDRN	MCASP[0-2]_XMIT_INTR_PEND	Transmit buffer underrun
MCASP_XINTCTL[1] XSYNCERR	MCASP_XSTAT[1] XSYNCERR	MCASP[0-2]_XMIT_INTR_PEND	Unexpected transmit frame sync

Table 12-17. TX Events (continued)

Event Mask[1]	Event Flag	Map to [1]	Description
MCASP_XINTCTL[2] XCKFAIL	MCASP_XSTAT[2] XCKFAIL	MCASP[0-2]_XMIT_INTR_PEND	Transmit clock failure
MCASP_XINTCTL[3] XDMAERR	MCASP_XSTAT[7] XDMAERR	MCASP[0-2]_XMIT_INTR_PEND	DATA port transmit error
MCASP_XINTCTL[4] XLAST	MCASP_XSTAT[4] XLAST	MCASP[0-2]_XMIT_INTR_PEND	Transmit last slot interrupt
MCASP_XINTCTL[5] XDATA	MCASP_XSTAT[5] XDATA	MCASP[0-2]_XMIT_INTR_PEND	Transmit data-ready interrupt
MCASP_XINTCTL[7] XSTAFRM	MCASP_XSTAT[6] XSTAFRM	MCASP[0-2]_XMIT_INTR_PEND	Transmit start of frame interrupt
n.a.	MCASP_XSTAT[8] XERR	n.a.	OR-event of all Tx-error events: (XDMAERR | XCKFAIL | XUNDRN | XSYNCERR). It is cleared ONLY when all error flags are cleared
n.a.	MCASP_XSTAT[3] XTDMSLOT	n.a.	Qualifies the current TDM slot as an odd or an even slot.

(1) Every MCASP module generates separate interrupt event.

Table 12-18. RX Events

Event Mask[1]	Event Flag	Map to[1]	Description
MCASP_RINTCTL[0] ROVRN	MCASP_RSTAT[0] ROVRN	MCASP[0-2]_REC_INTR_PEND	Receive buffer overrun
MCASP_RINTCTL[1] RSYNCERR	MCASP_RSTAT[1] RSYNCERR	MCASP[0-2]_REC_INTR_PEND	Unexpected receive frame sync
MCASP_RINTCTL[2] RCKFAIL	MCASP_RSTAT[2] RCKFAIL	MCASP[0-2]_REC_INTR_PEND	Receive clock failure
MCASP_RINTCTL[3] RDMAERR	MCASP_RSTAT[7] RDMAERR	MCASP[0-2]_REC_INTR_PEND	DATA port receive error
MCASP_RINTCTL[4] RLAST	MCASP_RSTAT[4] RLAST	MCASP[0-2]_REC_INTR_PEND	Receive last slot
MCASP_RINTCTL[5] RDATA	MCASP_RSTAT[5] RDATA	MCASP[0-2]_REC_INTR_PEND	Receive data-ready
MCASP_RINTCTL[7] RSTAFRM	MCASP_RSTAT[6] RSTAFRM	MCASP[0-2]_REC_INTR_PEND	Receive start of frame
n.a.	MCASP_RSTAT[8] RERR	n.a.	OR-event of all Rx-error events: (RDMAERR | RCKFAIL | ROVRN | RSYNCERR). RERR event is cleared once all error flags are cleared.
n.a.	MCASP_RSTAT[3] RTDMSLOT	n.a.	Qualifies the current TDM slot as an odd or an even slot.

(1) Every MCASP module generates separate interrupt event.

Software has to read the MCASP_XSTAT/MCASP_RSTAT register to determine which event occurs at a global level for MCASP Tx/Rx logic. In addition user software has to scan the XRDY/RRDY read-only flags in the MCASP_SRCTLn registers to determine which active serializer is the actual source of the event.

A Tx interrupt line (MCASP[0-2]_XMIT_INTR_PEND) is asserted (active high) when one of the MCASP_XSTAT notified events occurs, provided that it is enabled in its corresponding MCASP_XINTCTL bit. Similarly, a Rx interrupt line (MCASP[0-2]_REC_INTR_PEND) is asserted (active high) when one of MCASP_RSTAT notified events occurs, provided that it is enabled in its corresponding MCASP_RINTCTL bit. See also Section 12.1.2.4.12.4, *Multiple Interrupts* and the Section 12.1.2.4.10.1, *Data Ready Status and Event/Interrupt Generation* (n = 0 to 15).

12.1.2.4.12.1 Transmit Data Ready Event and Interrupt

The transmit data-ready interrupt (XDATA) is generated if the MCASP_XSTAT[5] XDATA bit is 1 and MCASP_XINTCTL[5] XDATA bit is enabled. The Section 12.1.2.4.10.1, *Data Ready Status and Event/Interrupt Generation*, provides details on when XDATA is set in the MCASP_XSTAT register.

A transmit-start-of-frame interrupt (XSTAFRM) is triggered by the recognition of a transmit frame sync.

A transmit-last-slot interrupt (XLAST) is a qualified version of the data-ready interrupt (XDATA). It has the same behavior than the data-ready interrupt, but is further qualified by having the data requested belonging to the last slot (the slot that just ended is the next-to-last TDM slot, the current slot is the last slot).

12.1.2.4.12.2 Receive Data Ready Event and Interrupt

The receive data-ready interrupt (RDATA) is generated if the MCASP_RSTAT[5] RDATA bit is 1 and MCASP_RINTCTL[5] RDATA bit is enabled. The Section 12.1.2.4.10.1, *Data Ready Status and Event/Interrupt Generation*, provides details on when the MCASP_RSTAT[5] RDATA bit is set.

A receiver start of frame (RSTAFRM) interrupt is triggered by the recognition of a receiver frame sync.

A receiver last slot (RLAST) interrupt is a qualified version of the data ready interrupt (RDATA). It has the same behavior as the data ready interrupt, but is further qualified by having the data in the buffer come from the last TDM time slot (the slot that just ended was last TDM slot).

12.1.2.4.12.3 Error Interrupt

Upon detection, the following error conditions generate interrupt flags:

In the transmit status register (MCASP_XSTAT):

- Transmit underrun (XUNDRN)
- Unexpected transmit frame sync (XSYNCERR)
- Transmit clock failure (XCKFAIL)
- Transmit DATA port error (XDMAERR)

Each interrupt source also has a corresponding enable bit in the transmit interrupt control register (MCASP_XINTCTL). If the enable bit is set, an interrupt is requested when the interrupt flag is set in MCASP_XSTAT. If the enable bit is not set, no interrupt request is generated. However, the interrupt flag may be polled.

In the receive status register (MCASP_RSTAT) :

- Receiver overrun (ROVRN)
- Unexpected receive frame sync (RSYNCERR)
- Receive clock failure (RCKFAIL)
- Receive DATA port error (RDMAERR)

Each interrupt source also has a corresponding enable bit in the receive interrupt control register (MCASP_RINTCTL). If the enable bit is set, an interrupt is requested when the interrupt flag is set in MCASP_RSTAT. If the enable bit is not set, no interrupt request is generated. However, the interrupt flag may be polled.

12.1.2.4.12.4 Multiple Interrupts

This only applies to interrupts and not to DMA requests. The following terms are defined:

- **Active Interrupt Request:** a flag in MCASP_XSTAT is set and the interrupt is enabled in MCASP_XINTCTL.
- **Outstanding Interrupt Request:** An interrupt request has been issued on one of the MCASP transmit interrupt port, but that request has not yet been serviced.
- **Serviced:** The CPUs write to MCASP_XSTAT to clear one or more of the active interrupt request flags.

The first interrupt request to become active for the serializer with the interrupt flag set in MCASP_XSTAT/ MCASP_RSTAT and the interrupt enabled in MCASP_XINTCTL/MCASP_RINTCTL generates a request on the MCASP transmit or receive interrupt port.

If more than one interrupt request becomes active in the same cycle, a single interrupt request is generated on the MCASP transmit or receive interrupt port. Subsequent interrupt requests that become active while the first interrupt request is outstanding do not immediately generate a new request pulse on the MCASP transmit or receive interrupt port.

The interrupt is serviced with the CPU writing to MCASP_XSTAT/MCASP_RSTAT. If any interrupt requests are active after the write, a new request is generated on the MCASP transmit or receive interrupt port.

One outstanding interrupt request is allowed on each port, so a transmit and a receive interrupt request may both be outstanding at the same time.

12.1.2.4.13 MCASP DMA Requests

The MCASP can generate one DMA request to the DMA controller to transmit (MCASP[0-2]_XMIT_DMA_EVT) or receive (MCASP[0-2]_REC_DMA_EVT) data. A DMA request to transmit data is generated if the *MCASP_XEVTCTL*[0] XDATDMA bit is cleared. A DMA request to receive data is generated if the MCASP_PIDTCTL[0] RDATDMA bit is cleared.

12.1.2.4.14 MCASP Loopback Modes

The MCASP features a digital loopback mode (DLB) that allows loopback test transfers in TDM mode between MCASP transmitters and receivers within the same device. In loopback mode, the output of a transmit serializer is connected internally to the input of a receive serializer. Therefore, a receiver data can be checked against a transmitter data to ensure that the MCASP settings are correct. Digital loopback mode applies to TDM mode only (2 to 32 slots in a frame). It does not apply to DIT mode (XMOD = 0x180) or burst mode (XMOD = 0).

Figure 12-33 shows the basic logical connection of the serializers in loopback mode.

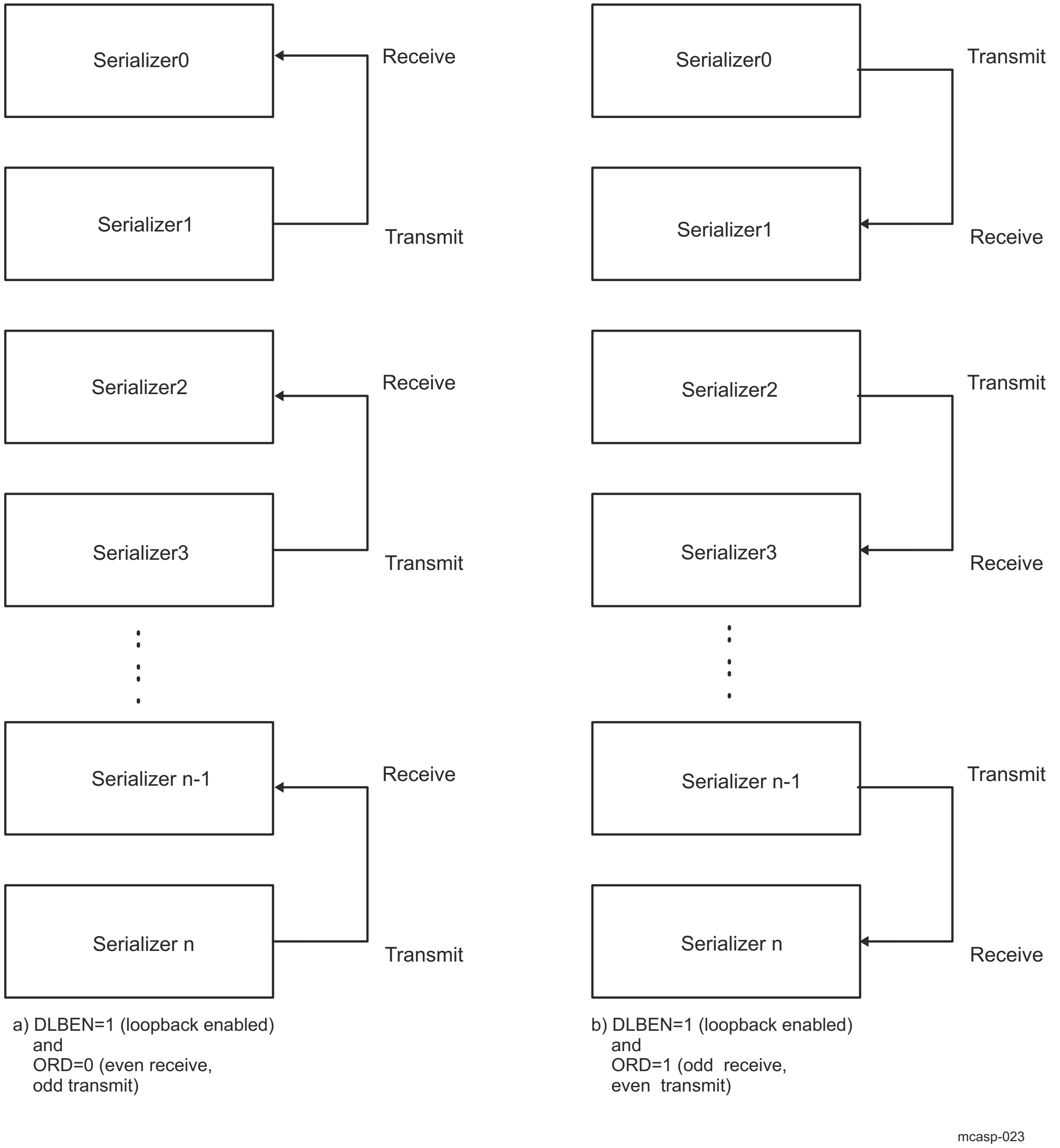


Figure 12-33. MCASP Serializers Operation in Loopback Mode

Two types of loopback connections are possible, selected by the ORD bit in the digital loopback control register - MCASP_DLBCTL as follows:

- ORD = 0: Outputs of odd serializers are connected to inputs of even serializers. If this mode is selected, the odd serializers must be configured as transmitters and even serializers as receivers.
- ORD = 1: Outputs of even serializers are connected to inputs of odd serializers. If this mode is selected, the even serializers must be configured as transmitters and odd serializers as receivers.

User can choose in software (the MCASP_DLBCTL[4] IOLBEN bit) between a MCASP module internal loopback and a device I/O level loopback.

When a **MCASP internal loopback** is selected (MCASP_DLBCTL[4] IOLBEN = 0b0), it is NOT necessary to configure *MCASP_PFUNC* and *MCASP_PDIR* registers for MCASP pin settings. Nevertheless, data can be optionally made externally visible at the I/O pin of the transmit serializer, if the pin is configured as a MCASP output pin by setting the corresponding *MCASP_PFUNC* bit to 0 (this is, to function as MCASP, not GPIO) and *MCASP_PDIR* bit to 1 (output).

When a **device I/O level loopback** is selected (MCASP_DLBCTL[4] IOLBEN = 0b1), the *MCASP_PFUNC* and *MCASP_PDIR* registers must be configured with the appropriate settings for all AXRn pins, according to ORD bit configuration.

In case of device I/O loopback, the connectivity is externally applied between device pads (this is, reaching device I/O buffers).

When in loopback mode, the transmit clock and frame sync are used by both the transmit and receive sections of the MCASP. The transmit and receive sections operate synchronously. This is achieved by setting the MCASP_DLBCTL[3-2] MODE bit field to 0x1 and the *MCASP_ACLKXCTL*[6] ASYNC bit to 0b0.

12.1.2.4.14.1 Loopback Mode Configurations

This is a summary of the settings required for digital loopback mode for TDM format :

- The MCASP_DLBCTL[0] DLBEN bit must be set to 0b1 to enable a loopback mode. It must be kept at 0b0 during normal MCASP operation.
- The MCASP_DLBCTL[4] IOLBEN bit must be set to select between internal (MCASP local) loopback mode or device I/O level loopback mode.
- The MCASP_DLBCTL[3-2] MODE bit field must be set to 0x1 for both the transmit and receive sections to use the transmit clock and frame sync generator.
- The MCASP_DLBCTL[1] ORD bit must be programmed appropriately to select odd or even serializers to be transmitters or receivers.
- The corresponding serializers must be configured accordingly.
- The *MCASP_ACLKXCTL*[6] ASYNC bit must be cleared to 0b0 to ensure synchronous transmit and receive operations.
- The MCASP_AFSRCTL[15-7] RMOD bit field and MCASP_AFSXCTL[15-7] XMOD bit field must be set within range (0x2 - 0x20) to indicate TDM mode.

Note

Loopback mode does not apply to DIT or burst mode, because MCASP receivers do NOT natively support DIR - reception.

12.1.2.4.15 MCASP Error Reporting

The MCASP includes error-checking capability for the serial protocol and data underrun. In addition, the MCASP includes a timer that continually measures the high-frequency controller clock every 32 AHCLKX clock cycles. The value of the timer can be read to get a measurement of the clock frequency and has a minimum and maximum range setting that can set an error flag if the controller clock goes out of a specified range.

When one or more errors (software selectable) are detected, an interrupt can be generated if desired, based on one or more error sources.

12.1.2.4.15.1 Buffer Underrun Error -Transmitter

A buffer underrun occurs when a serializer is instructed by the transmit state-machine to transfer data from XRBUFn buffer to XRSRn shift register, but the corresponding (MCASP_XBUFn) register has not yet been written with new data since the last time the transfer occurred. When this occurs, the transmit state-machine sets the XUNDRN flag.

An underrun is checked only once per time slot. The MCASP_XSTAT[0] XUNDRN flag is set when an underrun condition occurs. Once set, the XUNDRN flag remains set until the host explicitly writes 1 to the XUNDRN bit to clear it (n = 0 to 15).

In DIT mode, a pair of BMC zeros is shifted out when an underrun occurs (four bit times at 128 bfs). By shifting out a pair of zeros, a clock can be recovered on the receiver. To recover, reset the MCASP and restart with the proper initialization.

In TDM mode, during an underrun case, a long stream of zeros are shifted out causing the DACs to mute. To recover, reset the MCASP and start again with the proper initialization.

12.1.2.4.15.2 Buffer Overrun Error-Receiver

A buffer overrun occurs when a serializer is instructed to transfer data from XRSRn shift register to XRBUFn receiver buffer, but the corresponding MCASP_RBUFn register has not yet been read since the last time the transfer occured. When this occurs, the receiver state machine sets the overrun flag - ROVRN. However, the individual serializer writes over the data in the XRBUFn buffer register (destroying the previous sample) and continues shifting (n = 0 to 15).

An overrun is checked only once per time slot. The MCASP_RSTAT[0] ROVRN flag is set when an overrun condition occurs. It is possible that an overrun occurs on one time slot but then the host catches up and does not cause an overrun on the following time slots. However, once the ROVRN flag is set, it remains set until the host explicitly writes a 1 to the ROVRN bit to clear the ROVRN bit.

12.1.2.4.15.3 DATA Port Error - Transmitter

A transmit DATA port error, as indicated by the MCASP_XSTAT[7] XDMAERR bit, occurs when the DMA or device CPU writes more words to the DATA port of the MCASP than it should.

The MCASP_XSTAT[7] XDMAERR = 0b1 indicates that the DMA or device CPU wrote too many words to the MCASP DATA port for a given transmit DMA event. Writing too few words results in a transmit underrun error setting the MCASP_XSTAT[0] XUNDRN bit.

While XDMAERR occurs infrequently, an occurrence indicates a serious loss of synchronization between the MCASP and the DMA or device CPU. The MCASP transmitter and the DMA must be reinitialized to resynchronize them.

12.1.2.4.15.4 DATA Port Error - Receiver

A receive DATA port error, as indicated by the MCASP_RSTAT[7] RDMAERR bit, occurs when the DMA or device CPU reads more words from the DATA port of the MCASP than it should.

The MCASP_RSTAT[7] RDMAERR bit indicates that the DMA or device CPU read too many words from the MCASP DATA port for a given receive RINT event. Reading too few words results in a receiver overrun error setting the MCASP_RSTAT[0] ROVRN bit.

While RDMAERR occurs infrequently, an occurrence indicates a serious loss of synchronization between the MCASP and the DMA or device CPU. The MCASP receiver and the DMA must be reinitialized to resynchronize them.

12.1.2.4.15.5 Unexpected Frame Sync Error

An unexpected frame sync occurs in when:

- in burst mode and TDM mode, the next active edge of the frame sync occurs early such that the current slot will not be completed by the time the next slot is scheduled to begin.
- in TDM mode, an unexpected frame sync occurs also if the frame sync does NOT occur exactly during the correct bit clock (not a cycle earlier or later) and before slot 0.

When an unexpected frame sync occurs, there are two possible actions depending upon when the unexpected frame sync occurs:

1. **Early:** An early unexpected frame sync occurs when the MCASP is in the process of completing the current frame and a new frame sync is detected (not including overlap that occurs due to a 1 or 2 bit frame sync delay). When an early unexpected frame sync occurs:
    - Error event flag is set (XSYNCERR, if an unexpected transmit frame sync occurs; RSYNCERR, if an unexpected receive frame sync occurs).
    - Current frame is not resynchronized. The number of bits in the current frame is completed. The next frame sync, which occurs after the current frame is completed, will be resynchronized.
2. **Late:** A late unexpected frame sync occurs when there is a gap or delay between the last bit of the previous frame and the first bit of the next frame. When a late unexpected frame sync occurs (as soon as the gap is detected):

- Error event flag is set (XSYNCERR, if an unexpected transmit frame sync occurs; RSYNCERR, if an unexpected receive frame sync occurs).
- Resynchronization occurs upon the arrival of the next frame sync.

Late frame sync is detected the same way in burst mode and TDM mode. However, in burst mode, late frame sync is not meaningful and its interrupt enable should not be set.

12.1.2.4.15.6 Clock Failure Detection

12.1.2.4.15.6.1 Clock Failure Check Startup

It is initially expected of the clock failure circuits to generate an error until at least one measurement is taken. Therefore, the clock failure interrupts, clock switch, and mute functions should not be enabled immediately, but only after a specific startup procedure.

To start the transmit clock failure check procedure:

1. Configure the transmit clock failure detect logic (XMIN, XMAX, XPS) in the transmit clock check control register (MCASP_XCLKCHK).
2. Clear the transmit clock failure flag (XCKFAIL) in the transmit status register (MCASP_XSTAT).
3. Wait until the first measurement is taken (> 32 AHCLKX clock periods).
4. Verify that no clock failure is detected.
5. Repeat Step 2 through Step 4 until the clock is running and is no longer issuing clock failure errors.
6. After the transmit clock is measured and falls within the acceptable range, the following can be enabled:
    a. The transmit clock failure interrupt enable bit (XCKFAIL) in the transmitter interrupt control register (MCASP_XINTCTL)

To start the receive clock failure check procedure:

1. Configure receive clock failure detect logic (RMIN, RMAX, RPS) in the receive clock check control register (MCASP_RCLKCHK).
2. Clear receive clock failure flag (RCKFAIL) in the receive status register (MCASP_RSTAT).
3. Wait until first measurement is taken (> 32 AHCLKR clock periods).
4. Verify no clock failure is detected.
5. Repeat steps 2–4 until clock is running and is no longer issuing clock failure errors.
6. After the receive clock is measured and falls within the acceptable range, the following may be enabled:
    a. the receive clock failure (RCKFAIL) interrupt enable bit in the receive interrupt control register (MCASP_RINTCTL)

12.1.2.4.15.6.2 Transmit Clock Failure Check and Recovery

The transmit clock failure check circuit (see Figure 12-34) works off the internal MCASP interface clock and the external high-frequency serial clock (AHCLKX). It continually counts the number of interface clocks for every 32 high-rate serial clock (AHCLKX) periods, and stores the count in XCNT of the transmit clock check control register (MCASP_XCLKCHK) every 32 high-rate serial clock cycles.

The logic compares the count against a user-defined minimum allowable boundary (XMIN), and automatically flags an interrupt (the MCASP_XSTAT[2] XCKFAIL bit) when an out-of-range condition occurs. An out-of-range minimum condition occurs when the count is less than XMIN. The logic continually compares the current count (from the running interface clock counter) to the maximum allowable boundary (XMAX). This is so that if the external clock completely stops, the counter value is not copied to XCNT. An out-of-range maximum condition occurs when the count is greater than XMAX. The XMIN and XMAX fields are 8-bit unsigned values, and the comparison is performed using unsigned arithmetic.

An out-of-range count may indicate that an unstable clock was detected or that the audio source has changed and a new sample rate is being used.

For the transmit clock failure check circuit to operate correctly, the high-frequency serial clock divider must be taken out of reset.

If a clock failure is detected, the MCASP_XSTAT[2] XCKFAIL transmit clock failure flag is set. This causes an interrupt if the MCASP_XINTCTL[2] XCKFAIL transmit clock failure interrupt enable bit is set.

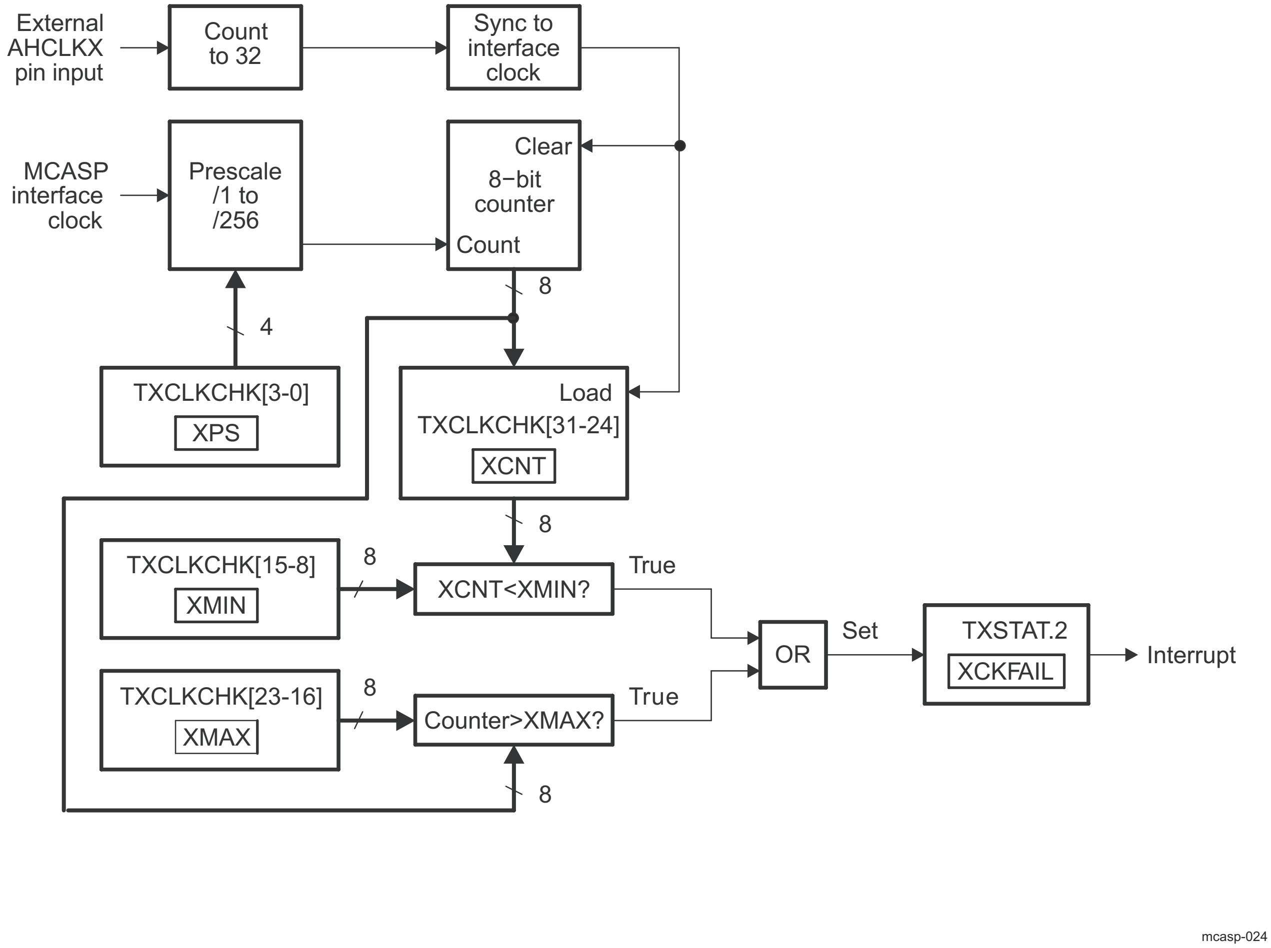


Figure 12-34. Transmit Clock Failure Detection Circuit Block Diagram

12.1.2.4.15.6.3 Receive Clock Failure Check and Recovery

The receive clock failure check circuit (see Figure 12-35) works off both the internal MCASP interface clock and the external high-frequency serial clock (AHCLKR). It continually counts the number of interface clocks for every 32 high rate serial clock (AHCLKR) periods, and stores the count in RCNT of the receive clock check control register (MCASP_RCLKCHK) every 32 high rate serial clock cycles.

The logic compares the count against a user-defined minimum allowable boundary (RMIN) and automatically flags an event (the MCASP_RSTAT[2] RCKFAIL bit) when an out-of-range condition occurs. An out-of-range minimum condition occurs when the count is smaller than RMIN. The logic continually compares the current count (from the running interface clock counter) against the maximum allowable boundary (RMAX). This is in case the external clock completely stops, so that the counter value is not copied to RCNT. An out-of-range maximum condition occurs when the count is greater than RMAX. Note that the RMIN and RMAX fields are 8-bit unsigned values, and the comparison is performed using unsigned arithmetic.

An out-of-range count may indicate either that an unstable clock was detected or that the audio source has changed and a new sample rate is being used.

In order for the receive clock failure check circuit to operate correctly, the high-frequency serial clock divider must be taken out of reset.

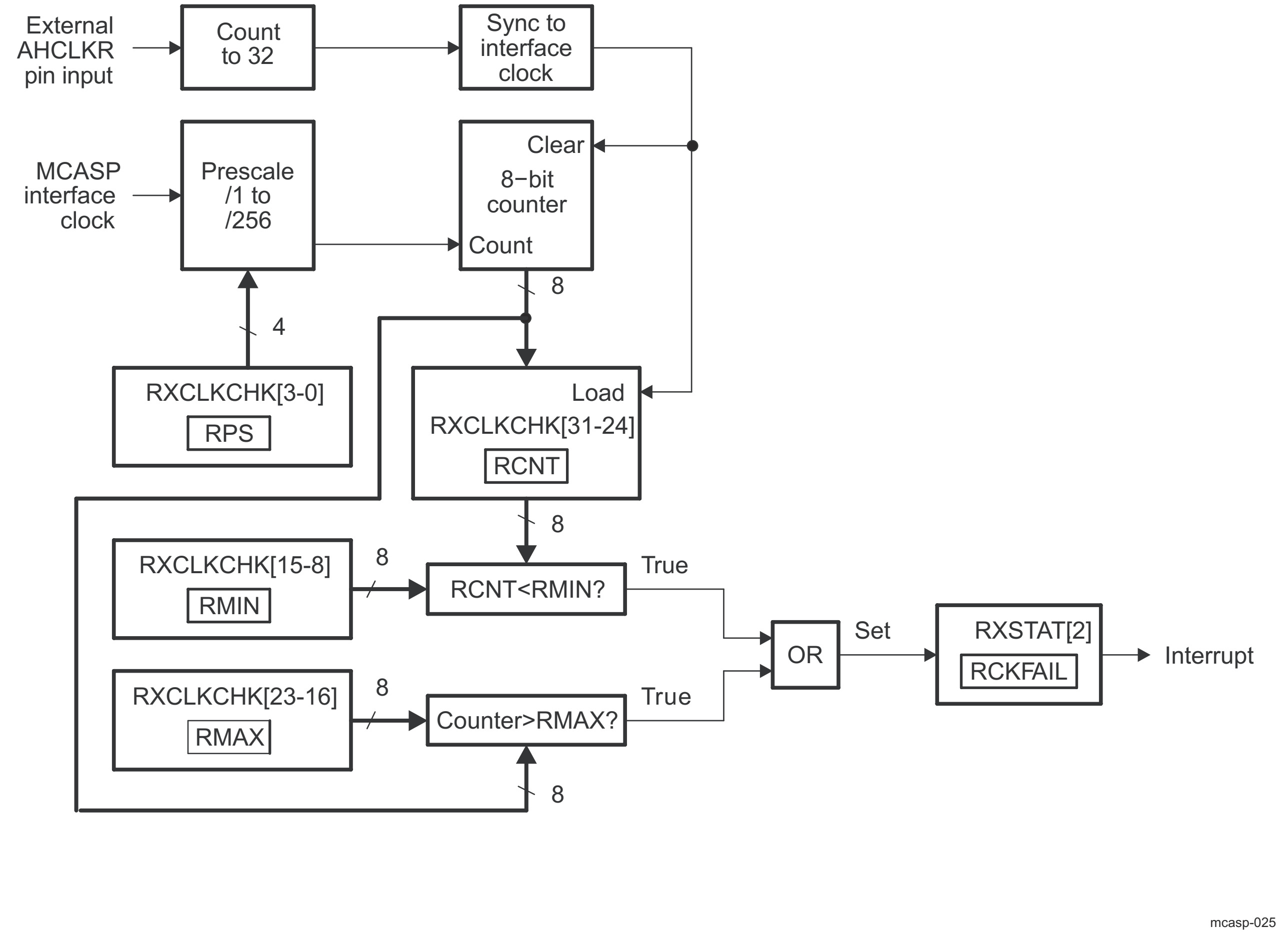


Figure 12-35. Receive Clock Failure Detection Circuit Block Diagram

12.1.2.5 MCASP Programming Guide

This section describes the low-level hardware programming sequences for the configuration and use of the MCASP module.

12.1.2.5.1 MCASP Global Initialization

12.1.2.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the MCASP module is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MCASP (for more information, see *Module Integration*, and *MCASP Environment*).

Table 12-19 describes the global initialization of surrounding modules.

Table 12-19. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC3	Module reset must be enabled. For more information about the module configuration, see *Reset*.
PLLCTRL0	PLLCTRL0 configuration must be done to enable the clocks to the MCASP modules, see *Clocking*.
PLL4	PLL4 configuration must be done to enable the clocks to the MCASP modules, see *Clocking*.
PLL2	PLL2 configuration must be done to enable the clocks to the MCASP modules, see *Clocking*.
ATL	ATL configuration must be done to enable the clocks to the MCASP modules, see *Audio Tracking Logic (ATL)*.
COMPUTE_CLUSTER0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling COMPUTE_CLUSTER0 interrupts, see *Interrupts*.
MAIN2MCU_LVL_INTRTR0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MAIN2MCU_LVL_INTRTR0 interrupts, see *Interrupts*.
R5FSS0_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS0_CORE0/1 interrupts, see *Interrupts*.
PDMA0_MCASP_G0	PDMA0_MCASP_G0 controllers configuration must be done to enable the module PDMA0_MCASP_G0 channel request, see *PDMA Controller*.
Interconnects	For information about the CBASS0 interconnects configuration, see *System Interconnect*.

Note

NAVSS configuration (UMDA channel set-up) must be done in order to move data from/to MCASP via the PDMA Controller. For more information, see *Navigator Subsystem (NAVSS)*.

Note

The COMPUTE_CLUSTER0, MAIN2MCU_LVL_INTRTR0, R5FSS0_CORE0/1, and the PDMA0_MCASP_G0 configurations are required when the interrupt and DMA-based communication modes are used. Further initialization of the selected interrupt and DMA controllers of the host CPU must be done for full functionality of the MCASP DMA and interrupt lines.

12.1.2.5.1.2 MCASP Global Initialization

12.1.2.5.1.2.1 Main Sequence – MCASP Global Initialization for DIT-Transmission

The procedure in Table 12-20 initializes the MCASP serializers transmitters to operate in DIT-mode (S/PDIF-transmission protocol) after a power-on reset (POR).

CAUTION

Before performing MCASP global initialization, If external clock ACLKR is used, it must be running already for proper synchronization of the *MCASP_GBLCTL* register.

Table 12-20. MCASP Transmitters Global Initialization for DIT-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP components.	*MCASP_GBLCTL*[12-8]	0x00
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	*MCASP_GBLCTL*[12-8]	=0x00
3. Configure the local power management.	*MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE	0x1
4. Configure the transmit format unit.	See Section 12.1.2.5.1.2.1.1.	
5. Configure the transmit frame sync generator.	See Section 12.1.2.5.1.2.1.2.	
6. Configure the transmit clock generator.	See Section 12.1.2.5.1.2.1.3.	
7. Configure the TDM sequencer—set all slots active.	MCASP_XTDM[31-0] XTDMS	0xFFFF FFFF
8. Configure the desired n-th serializer (n=0 to 3) for transmit mode operation.[3]	MCASP_SRCTLn [1-0] SRMOD; n = 0 to 15	0x1
9. Configure the MCASP pins functionality.	See Section 12.1.2.5.1.2.1.4.	
10. Enable the MCASP DIT - transmission mode.	MCASP_DITCTL[0] DITEN	0x1[2]
11. Configure DIT-specific subframe fields.	See Table 12-25.	
12. Release from reset state the divider that outputs the AHCLKX clock.[1]	*MCASP_GBLCTL*[9] XHCLKRST	0x1
13. Poll the bit to ensure that it is successfully latched in the register.	*MCASP_GBLCTL*[9] XHCLKRST	=0x1
14. Release from reset state the divider that outputs the ACLKX clock.[1]	*MCASP_GBLCTL*[8] XCLKRST	0x1
15. Poll the bit to ensure that it is successfully latched in the register.	*MCASP_GBLCTL*[8] XCLKRST	=0x1

(1) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the *MCASP_AHCLKXCTL* and *MCASP_ACLKXCTL* registers are ignored; hence, the transmission clock does not stop during the reset state of the dividers.
(2) This globally configures all active transmitters to operate in DIT-mode.
(3) For an unused serializer n, write MCASP_SRCTLn [1-0] SRMOD = 0x0 to disable it (n = 0 to 15).

12.1.2.5.1.2.1.1 Subsequence – Transmit Format Unit Configuration for DIT-Transmission

The procedure in Table 12-21 configures the transmit frame format unit of the MCASP module for a DIT-transmission.

Note

- The first transmit data bit always has a 0-bit delay.
- The bitstream is always transmitted in least-significant-bit (LSB)-first order.
- Pad value for extra bits in a certain slot is always 0.

Table 12-21. Transmit Format Unit Configuration for DIT-Transmission

Step	Register/Bit Field/Programming Model	Value
Configure the slot size to 32 bits.	MCASP_XFMT[7-4] XSSZ	0xF
IF: the data to transmit is left- aligned	Software test condition	
Set data mask in the range 0xFFFF FF00 – 0xFFFF 0000.	MCASP_XMASK[31-0] XMASK	0x-[1]
Rotate data right by a multiple-of-4- bit positions.	MCASP_XFMT[2-0] XROT	0x-[1]
ELSE		
Set data mask in the range 0x00FF FFFF– 0x0000 FFFF.	MCASP_XMASK[31-0] XMASK	0x-[1]
Rotate data right by 0-bit positions.	MCASP_XFMT[2-0] XROT	0x0
ENDIF		

Table 12-21. Transmit Format Unit Configuration for DIT-Transmission (continued)

Step	Register/Bit Field/Programming Model	Value
Select to write data to active serializers transmit buffers using peripheral (CFG) or DATA port	MCASP_XFMT[3] XBUSEL	0x-

(1) Refer to Section 12.1.2.4.4.1, *Transmit Fromat Unit* and Section 12.1.2.4.4.1.2, *DIT-Mode Transmission Data Alignment Settings*.

12.1.2.5.1.2.1.2 Subsequence – Transmit Frame Synchronization Generator Configuration for DIT-Transmission

The procedure in Table 12-22 configures the transmit frame synchronization generator of the MCASP module.

Note

The frame synchronization signal is always rising-edge active and always has a single-bit width.

Table 12-22. Transmit Frame-Synchronization Generator Configuration for DIT-Transmission

Step	Register/Bit Field/Programming Model	Value
Select 384-slot size block.	MCASP_AFSXCTL[15-7] XMOD	0x180
Select internally-generated transmit frame sync.	MCASP_AFSXCTL[1] FSXM	0x1

12.1.2.5.1.2.1.3 Subsequence – Transmit Clock Generator Configuration for DIT-Transmission

Note

By default, the ACLKX and AHCLKX clocks are generated only from the MCASP internal clock source.

The procedure in Table 12-23 configures the transmit clock generator of the MCASP module.

Table 12-23. Transmit Clock Generator Configuration in DIT-Mode

Step	Register/Bit Field/Programming Model	Value
Set the divisor for the internally generated high frequency clock– AHCLKX.	*MCASP_AHCLKXCTL*[11-0] HCLKXDIV	0x-
Set he divisor for the internally generated transmission clock– ACLKX.	*MCASP_ACLKXCTL*[4-0] CLKXDIV	0x-
Configure the transmit clock failure detect logic.	See Section 12.1.2.4.15.6.1, *Clock Failure Check Startup*.	

12.1.2.5.1.2.1.4 Subsequence - MCASP Pins Functional Configuration

The procedure in Table 12-24 configures the MCASP pins for MCASP functionality.

Table 12-24. MCASP Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	*MCASP_PFUNC*[31-0]	0x0
Configure the MCASP pins as outputs: AFSX AHCLKX ACLKX Desired i-th MCASP data pin AXRi is configured as an output for DIT-transmission.	*MCASP_PDIR*[28] AFSX; *MCASP_PDIR*[27] AHCLKX; *MCASP_PDIR*[26] ACLKX; *MCASP_PDIR*[i] AXRi	0x1 0x1 0x1 0x1

12.1.2.5.1.2.1.5 Subsequence – DIT-specific Subframe Fields Configuration

The procedure in Table 12-25 configures the DIT-specific subframe fields as part of the S/PDIF format data.

Table 12-25. DIT-Specific Subframe Fields Configuration

Step	Register/Bit Field/Programming Model	Value
Configure the valid bit value for odd time slots.	MCASP_DITCTL[3] VB	0x-
Configure the valid bit value for even time slots.	MCASP_DITCTL[2] VA	0x-

Table 12-25. DIT-Specific Subframe Fields Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Configure the user data bit for each subframe A and B in a 384-slot S/PDIF block.	MCASP_DITUDRAi[31-0] DITUDRAi, where i = 0 to 5 MCASP_DITUDRBi[31-0] DITUDRBi, where i = 0 to 5	0x- 0x-
Configure the channel status bit for each subframe A and B in a 384-slot S/PDIF block.	MCASP_DITCSRAi[31-0], where i = 0 to 5 MCASP_DITCSRBi[31-0], where i = 0 to 5	0x- 0x-

12.1.2.5.1.2.2 Main Sequence – MCASP Global Initialization for TDM-Reception

The procedure in Table 12-26 initializes a MCASP serializer n receiver(s) to operate in TDM-mode (the only mode supported by MCASP receivers) after a power-on reset (POR). This is used for I2S (2-slot TDM) and other TDM-based audio protocols reception.

CAUTION

Before performing MCASP global initialization, If external clock ACLKR is used, it must be running already for proper synchronization of the *MCASP_GBLCTL* register.

Note

The MCASP receivers support only TDM-frames (including 384-TDM frames) reception. DIT-frames reception (this is, S/PDIF stream) can be implemented indirectly via an external DIR-chip converter with DIT-input and TDM (I2S)-compatible output connected to device MCASP receiver input (TDM-only compatible).

Table 12-26. MCASP Receivers Global Initialization for TDM-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP receive components.	*MCASP_GBLCTL*[4-0]	0x00
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	*MCASP_GBLCTL*[4-0]	=0x00
3. Configure the local power management.	*MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE	0x1
4. Configure the receive format unit.	See Section 12.1.2.5.1.2.2.1.	
5. Configure the receive frame sync generator.	See Section 12.1.2.5.1.2.2.2.	
6. Configure the receive clock generator.	See Section 12.1.2.5.1.2.2.3.	
7. Program all bits - RTDMSk (where k = 0 to 31) according to the time slot characteristics desired (positions of active versus inactive slots within a frame).	MCASP_RTDM[k] RTDMSk , where k = 0 to 31	0x-
8. Configure the desired n-th serializer for receive mode operation.[4]	MCASP_SRCTLn [1-0] SRMOD; n = 0 to 15	0x2
9. Configure the MCASP pins functionality.	See Section 12.1.2.5.1.2.2.4.	
10. Optional: Configure a MCASP Rx channel for a loopback operation (TDM mode only) in MCASP_DLBCTL [31-0].	See Section 12.1.2.4.14.1, *Loopback Mode Configurations*.	0x-[5]
11. Release from reset state the divider that outputs the AHCLKR clock.[1] See also[2].	*MCASP_GBLCTL*[1] RHCLKRST	0x1
12. Poll the bit to ensure that it is successfully latched in the register. See also[2].	*MCASP_GBLCTL*[1] RHCLKRST	=0x1
13. Release from reset state the divider that outputs the ACLKR clock. [1] See also[3].	*MCASP_GBLCTL*[0] RCLKRST	0x1

Table 12-26. MCASP Receivers Global Initialization for TDM-Mode Operation (continued)

Step	Register/Bit Field/Programming Model	Value
14. Poll the bit to ensure that it is successfully latched in the register. See also(3).	*MCASP_GBLCTL*[0] RCLKRST	=0x1

(1) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the *MCASP_AHCLKRCTL* and *MCASP_ACLKRCTL* registers are ignored; hence, the reception clock does not stop during the reset state of the dividers.
(2) This step is necessary even if external high-frequency serial clocks are used.
(3) This step can be skipped if external serial clocks are used and they are running.
(4) For an unused serializer n, write MCASP_SRCTLn [1-0] SRMOD = 0x0 to disable it (n = 0 to 15).
(5) In this case the receiver clock and frame sync are derived from the MCASP transmitter logic, so *MCASP_ACLKXCTL*[6] ASYNC must be set to 0b0. Neither MCASP internal receiver clock and frame sync generators, nor external clock and frame sync source are used.

12.1.2.5.1.2.2.1 Subsequence – Receive Format Unit Configuration in TDM Mode

The procedure in Table 12-27 configures the receive frame format unit of the MCASP module for TDM slots reception.

Table 12-27. Receive Format Unit Configuration for TDM-Reception

Step	Register/Bit Field/Programming Model	Value
Configure the desired TDM-slot size	MCASP_RFMT[7-4] RSSZ	0x-(1)
Set data mask out value (0x0000 0000 - 0xFFFF FFFF).	MCASP_RMASK[31-0] RMASK	0x-(2)
Select a padding value for masked-out bits.	MCASP_RFMT[14-13] RPAD	0x-
Specify position (0x0-0x1F) of the bit in corresponding register MCASP_RBUFn which value to be used as a pad value in case MCASP_RFMT[14-13] RPAD = 0x2. (n = 0 to 15)	MCASP_RFMT[12-8] RPBIT	0x-
Rotate data right by a multiple of 4- bit positions.	MCASP_RFMT[2-0] RROT	0x-(3)
Received stream bit order (LSB- or MSB-first). Must be set to 0x1 for an I2S stream reception (MSB-first).	MCASP_RFMT[15] RRVRS	0x-(3)
Specify a delay between frame sync and first bit of data in number of bits. Must be set to 0x1 for an I2S stream reception.	MCASP_RFMT[17-16] RDATDLY	0x-
Select to read data from active serializers receive buffers using peripheral (CFG) or DATA port	MCASP_RFMT[3] RBUSEL	0x-

(1) Refer to Section 12.1.2.4.4.2, *Receive Format Unit*, regarding options for received TDM-slot sizes.
(2) For more details on Rx masking value, refer to Section 12.1.2.4.4.2.1, *TDM - Mode Reception Data Alignment Settings*
(3) For more details on rotation and received TDM stream bit order, refer to Section 12.1.2.4.4.2.1, *TDM - Mode Reception Data Alignment Settings* and Table 12-14, *MCASP RFU Settings*.

12.1.2.5.1.2.2.2 Subsequence – Receive Frame Synchronization Generator Configuration in TDM Mode

The procedure in Table 12-28 configures the transmit frame synchronization generator of the MCASP module.

Note

The same bit - *MCASP_ACLKXCTL*[6] ASYNC which is used to determine if MCASP receivers and transmitters work synchronously on the same clock, is also used to define if receiver frame sync is derived from the transmit frame sync generator, or generated independently in the receiver (either inernally or externally sourced). Hence, the settings in below table Table 12-28 have no effect, if *MCASP_ACLKXCTL*[6] ASYNC = 0.

Table 12-28. Receive Frame-Synchronization Generator Configuration for TDM-Reception

Step	Register/Bit Field/Programming Model	Value
Select number of TDM slots per frame. Must be set to 0x2, in case of an I2S-reception. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3.	MCASP_AFSRCTL[15-7] RMOD	0x-(1)

Table 12-28. Receive Frame-Synchronization Generator Configuration for TDM-Reception (continued)

Step	Register/Bit Field/Programming Model	Value
Choose the receive frame sync width -single bit/single word. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3.	MCASP_AFSRCTL[4] FRWID	0x-
Select start of received frame sync polarity - rising / falling edge. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3.	MCASP_AFSRCTL[0] FSRP	0x-
IFreceive frame sync - FS is internally generated	Software test condition	
Select internally- generated receive frame sync. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3.	MCASP_AFSRCTL[1] FSRM	0b1
If MCASP receiver is required to output internally generated frame, AFSR pin must be set as an output in step 9 of the sequence documented in the Table 12-26. This must not be done in current step because the frame control register - MCASP_AFSXCTL must be appropriately configured prior to AFSR pin outputting a frame to an external device.	*MCASP_PDIR*[31] AFSR	0b1
ELSE		
Select externally- generated receive frame sync. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3.	MCASP_AFSRCTL[1] FSRM	0b0
Setup the AFSR pin as input (device level: MCASPi_AFSR)	*MCASP_PDIR*[31] AFSR	0b0
ENDIF		
To generate MCASP receive frame sync in receiver logic, select an asynchronous frame sync.	*MCASP_ACLKXCTL*[6] ASYNC	0b1

(1) Must be set to 0x180 in case of 384-TDM slot frame reception from a DIR component I2S-output. For more details on TDM-frame settings, refer to *Module Integration*.

12.1.2.5.1.2.2.3 Subsequence – Receive Clock Generator Configuration

The procedure in Table 12-29 configures the receive clock generator of the MCASP module.

Note

The settings in below table Table 12-29 have no effect, if *MCASP_ACLKXCTL*[6] ASYNC = 0 (this is, receive clock is sourced from the inverted version of the transmit clock). For example, such is the case when MCASP loopback mode is used.

Table 12-29. Receive Clock Generator Configuration

Step	Register/Bit Field/Programming Model	Value
To use the MCASP receive clock generator, select an asynchronous receiver clock schema (ASYNC = 1). Otherwise an inverted version of transmit clock XCLK is used (receiver synchronized with transmitter).	*MCASP_ACLKXCTL*[6] ASYNC	0b1
IF receive clock - RCLK is internally generated	Software test condition	
The high-speed receive clock - AHCLKR is internally generated based on AUXCLK		
Select an internally-generated high-frequency clock.	*MCASP_AHCLKXCTL*[15] HCLKRM	0b1
Select the internal high-speed clock source polarity: non-inverted or inverted.	*MCASP_AHCLKXCTL*[14] HCLKRP	0x-
Set the divisor for the internally generated high-frequency clock – AHCLKR in range (1 - 4096).	*MCASP_AHCLKXCTL*[11-0] HCLKRDIV	0x-
Select an internally-generated receive clock.	*MCASP_ACLKXCTL*[5] CLKRM	0b1

Table 12-29. Receive Clock Generator Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Receiver samples on rising/falling edge. Select Rx sampling on the rising edge if transmitter shifts out on falling edge, and vice versa.	*MCASP_ACLKXCTL*[7] CLKRP	0x-
Set the divisor for the internally generated receive clock– ACLKR in range (1 - 32).	*MCASP_ACLKXCTL*[4-0] CLKRDIV	0x-
Optional: If MCASP receiver is required to output internally generated clock, ACLKR pin must be set as an output in step 9 of the sequence documented in the Table 12-26. This must not be done in current step because the clock control register - *MCASP_ACLKRCTL* must be appropriately configured prior to ACLKR pin outputting a receive clock to an external device.	*MCASP_PDIR*[29] ACLKR	0b1
ELSE		
Select an externally-generated receive clock. Note that in this case the AHCLKR signal path and the CLKRDIV divider are NOT used.	*MCASP_ACLKXCTL*[5] CLKRM	0b0
Receiver samples on rising/falling edge. Select Rx sampling on the rising edge if transmitter shifts out on falling edge, and vice versa.	*MCASP_ACLKXCTL*[7] CLKRP	0x-
Setup an input direction for the ACLKR pin	*MCASP_PDIR*[29] ACLKR	0b0
ENDIF		
Configure the transmit clock failure detect logic.	See Section 12.1.2.4.15.6.1, *Clock Failure Check Startup.*	

12.1.2.5.1.2.2.4 Subsequence—MCASP Receiver Pins Functional Configuration

The procedure in Table 12-30 configures the MCASP pins for MCASP functionality.

Table 12-30. MCASP Receiver Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	*MCASP_PFUNC*[31-0]	0x0
Configure the MCASP pins direction: AFSR ACLKR Desired n-th MCASP data pin AXRn is configured as an input for receiving.	 *MCASP_PDIR*[31] AFSR; *MCASP_PDIR*[29] ACLKR; *MCASP_PDIR*[n] AXRn;	 0x-[1] 0x-[2] 0x0

(1) See Table 12-28.
(2) For more details on MCASP clock configurations, refer to Table 12-29.

12.1.2.5.1.2.3 Main Sequence – MCASP Global Initialization for TDM -Transmission

The procedure in Table 12-31 initializes a MCASP serializer n transmitter(s) to operate in TDM-mode after a power-on reset (POR). This is used for I2S (2-slot TDM) and other TDM-based audio protocols transmission.

> **CAUTION**
>
> Before performing MCASP global initialization, If external clock ACLKR is used, it must be running already for proper synchronization of the *MCASP_GBLCTL* register.

Table 12-31. MCASP Transmitters Global Initialization for TDM-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP transmit components.	*MCASP_GBLCTL*[12-8]	0x00
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	*MCASP_GBLCTL*[12-8]	=0x00
3. Configure the local power management.	*MCASP_PWRIDLESYSCONFIG*[1-0] IDLE_MODE	0x1

Table 12-31. MCASP Transmitters Global Initialization for TDM-Mode Operation (continued)

Step	Register/Bit Field/Programming Model	Value
4. Configure the transmit format unit.	See Section 12.1.2.5.1.2.3.1.	
5. Configure the transmit frame sync generator.	See Section 12.1.2.5.1.2.3.2.	
6. Configure the transmit clock generator.	See Section 12.1.2.5.1.2.3.3.	
7. Program all bits - XTDMSk, where k = 0 to 31, according to the time slot characteristics desired (positions of active versus inactive slots within a frame).	MCASP_XTDM[k] XTDMSk, where k = 0 to 31(4)	0x-
8. Configure the desired n-th serializer for transmit mode operation.(3)	MCASP_SRCTLn[1-0] SRMOD; n = 0 to 15	0x1
9. Setup all active transmitters to operate in TDM mode.	MCASP_DITCTL[0] DITEN	0x0(2)
10. Configure the MCASP pins functionality.	See Section 12.1.2.5.1.2.3.4.	
11. Optional: Configure a MCASP Tx channel for loopback operation (TDM mode only) in MCASP_DLBCTL [31-0].	See Section 12.1.2.4.14.1, *Loopback Mode Configurations*.	0x-
12. Release from reset state the divider that outputs the AHCLKR clock. See(1)	*MCASP_GBLCTL*[9] XHCLKRST	0x1
13. Poll the bit to ensure that it is successfully latched in the register.	*MCASP_GBLCTL*[9] XHCLKRST	=0x1
14. Release from reset state the divider that outputs the ACLKR clock. See(1)	*MCASP_GBLCTL*[8] XCLKRST	0x1
15. Poll the bit to ensure that it is successfully latched in the register.	*MCASP_GBLCTL*[8] XCLKRST	=0x1

(1) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the *MCASP_AHCLKXCTL* and *MCASP_ACLKXCTL* registers are ignored; hence, the transmission clock does not stop during the reset state of the dividers.
(2) All active transmit channels operate either in TDM mode or in DIT mode depending on DITEN value. There is no option to choose Tx Mode between DIT and TDM separately per serializer transmitter.
(3) For an unused serializer n, write MCASP_SRCTLn [1-0] SRMOD = 0x0 to disable it (n = 0 to 15).
(4) Appropriately program in the MCASP_SRCTLn[3-2] DISMOD bit field, the desired level (high-impedance state, 0, or 1) at AXRn output, during time of inactive slots. Note, that this setting does NOT apply when all slots are programmed to be active within a frame (in particular DIT-mode) (n = 0 to 15).

12.1.2.5.1.2.3.1 Subsequence – Transmit Format Unit Configuration in TDM Mode

The procedure in Table 12-32 configures the transmit frame format unit of the MCASP module for TDM slots transmission.

Table 12-32. Transmit Format Unit Configuration for TDM-Transmission

Step	Register/Bit Field/Programming Model	Value
Configure the desired TDM-slot size	MCASP_XFMT[7-4] XSSZ	0x-(1)
Set data mask out value (0x0000 0000 - 0xFFFF FFFF).	MCASP_XMASK[31-0] XMASK	0x-(2)
Select a padding value for masked-out bits.	MCASP_XFMT[14-13] XPAD	0x-
Specify position (0x0-0x1F) of the bit in corresponding register MCASP_XBUFn which value to be used as a pad value in case MCASP_XFMT[14-13] XPAD = 0x2 (n = 0 to 15).	MCASP_XFMT[12-8] XPBIT	0x-
Rotate data right by a multiple of 4- bit positions.	MCASP_XFMT[2-0] XROT	0x-(3)
transmitted stream bit order (LSB- or MSB-first). Must be set to 0x1 for an I2S stream transmission (MSB-first).	MCASP_XFMT[15] XRVRS	0x-(3)
Specify a delay between frame sync and first bit of data in number of bits. Must be set to 0x1 for an I2S stream transmission.	MCASP_XFMT[17-16] XDATDLY	0x-
Select to write data to active serializers transmit buffers using peripheral (CFG) or DATA port	MCASP_XFMT[3] XBUSEL	0x-

(1) Refer to Section 12.1.2.4.4.1, *Transmit Format Unit* , regarding options for transmitted TDM-slot sizes.
(2) For more details on Tx masking value, refer to Section 12.1.2.4.4.1.1, *TDM - Mode Transmission Data Alignment Settings*

(3) For more details on rotation and transmitd TDM stream bit order, refer to Section 12.1.2.4.4.1.1, *TDM - Mode Transmission Data Alignment Settings* and Table 12-12, *MCASP TFU TDM Mode Settings*.

12.1.2.5.1.2.3.2 Subsequence – Transmit Frame Synchronization Generator Configuration in TDM Mode

The procedure in Table 12-33 configures the transmit frame synchronization generator of the MCASP module.

Table 12-33. Transmit Frame-Synchronization Generator Configuration for TDM-Transmission

Step	Register/Bit Field/Programming Model	Value
Select number of TDM slots per frame (2 - 32). Must be set to 0x2, in case of an I2S-transmission. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3, *Frame-Sync Generator*.	MCASP_AFSXCTL[15-7] XMOD	0x-
Choose the transmit frame sync width -single bit/single word. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3, *Frame-Sync Generator*.	MCASP_AFSXCTL[4] FXWID	0x-
Select start of transmit frame sync polarity - rising / falling edge. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3, *Frame-Sync Generator*.	MCASP_AFSXCTL[0] FSXP	0x-
IF transmit frame sync - FS is internally generated	Software test condition	
Select internally- generated transmit frame sync. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3, *Frame-Sync Generator*.	MCASP_AFSXCTL[1] FSXM	0b1
If MCASP transmitter is required to output internally generated frame, AFSX pin must be set as an output in step 10 of the sequence documented in the Table 12-31. This must NOT be done in current step because the frame control register - MCASP_AFSXCTL must be appropriately configured prior to AFSX pin outputting a frame sync to an external device.	*MCASP_PDIR*[28] AFSX	0b1
ELSE		
Select externally- generated transmit frame sync. For more details on frame-sync generator, refer to Section 12.1.2.4.2.3, *Frame-Sync Generator*.	MCASP_AFSXCTL[1] FSXM	0b0
Setup the AFSX pin as input	*MCASP_PDIR*[28] AFSX	0b0

12.1.2.5.1.2.3.3 Subsequence – Transmit Clock Generator Configuration for TDM Cases

The procedure in Table 12-34 configures the transmit clock generator of the MCASP module.

Table 12-34. Transmit Clock Generator Configuration for TDM Cases

Step	Register/Bit Field/Programming Model	Value
IF transmit clock - XCLK is internally generated	Software test condition	
IF high-speed transmit clock - AHCLKX is internally generated based on AUXCLK	Software test condition	
Select an internally-generated high-frequency clock.	*MCASP_AHCLKXCTL*[15] HCLKXM	0b1
Select the high-frequency clock source polarity: non-inverted or inverted.	*MCASP_AHCLKXCTL*[14] HCLKXP	0x-
Set the divisor for the internally generated high-frequency clock – AHCLKX in range (1 - 4096).	*MCASP_AHCLKXCTL*[11-0] HCLKXDIV	0x-
Optional: If MCASP transmitter is required to output internally generated high-frequency clock, AHCLKX pin must be set as an output in step 10 of the sequence documented in the Table 12-31. This must NOT be done in current step because the clock control register - *MCASP_AHCLKXCTL* must be appropriately configured prior to AHCLKX pin outputting a high-speed clock to an external device.	*MCASP_PDIR*[27] AHCLKX	0b1
ELSE		

Table 12-34. Transmit Clock Generator Configuration for TDM Cases (continued)

Step	Register/Bit Field/Programming Model	Value
Select an externally-generated high frequency clock (HCLKXDIV divider can not be used).	*MCASP_AHCLKXCTL*[15] HCLKXM	0b0
Select the high-speed transmit clock source polarity: non-inverted or inverted.	*MCASP_AHCLKXCTL*[14] HCLKXP	0x-
Setup an input directon for the AHCLKX pin	*MCASP_PDIR*[27] AHCLKX	0b0
ENDIF		
Select an internally-generated transmit clock.	*MCASP_ACLKXCTL*[5] CLKXM	0b1
Transmitter samples on rising/falling edge. Select Tx shifting out data on the rising edge if receiver samples on falling edge, and vice versa.	*MCASP_ACLKXCTL*[7] CLKXP	0x-
Set the divisor for the internally generated transmit clock– ACLKX in range (1 - 32).	*MCASP_ACLKXCTL*[4-0] CLKXDIV	0x-
Optional: If MCASP transmitter is required to output internally generated clock, ACLKX pin) must be set as an output in step 10 of the sequence documented in the Table 12-31. This must NOT be done in current step because the clock control register - *MCASP_ACLKXCTL* must be appropriately configured prior to ACLKX pin outputting a transmit clock to an external device.	*MCASP_PDIR*[26] ACLKX	0b1
ELSE		
Select an externally-generated transmit clock. Note that in this case the AHCLKX signal path and the CLKXDIV divider are NOT used.	*MCASP_ACLKXCTL*[5] CLKXM	0b0
Transmitter samples on rising/falling edge. Select Tx shifting out data on the rising edge if receiver samples on falling edge, and vice versa.	*MCASP_ACLKXCTL*[7] CLKXP	0x-
Setup an input directon for the ACLKX pin	*MCASP_PDIR*[26] ACLKX	0b0
ENDIF		
Configure the transmit clock failure detect logic.	See Section 12.1.2.4.15.6.1, *Clock Failure Check Startup*.	

12.1.2.5.1.2.3.4 Subsequence—MCASP Transmit Pins Functional Configuration

The procedure in Table 12-35 configures the MCASP pins for MCASP functionality.

Table 12-35. MCASP Transmit Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	*MCASP_PFUNC*[31-0]	0x0
Configure the MCASP pins direction: AFSX AHCLKX ACLKX Desired n-th MCASP data pin AXRn is configured as an ouput for transmission.	*MCASP_PDIR*[28] AFSR; *MCASP_PDIR*[27] AHCLKR; *MCASP_PDIR*[26] ACLKR; *MCASP_PDIR*[n] AXRn	0x-(1) 0x-(2) 0x-(2) 0x1

(1) See Table 12-33.

12.1.2.5.2 MCASP Operational Modes Configuration

12.1.2.5.2.1 MCASP Transmission Modes

12.1.2.5.2.1.1 Main Sequence – MCASP DIT- /TDM- Polling Transmission Method

Figure 12-36 shows the MCASP DIT-/TDM- polling method.

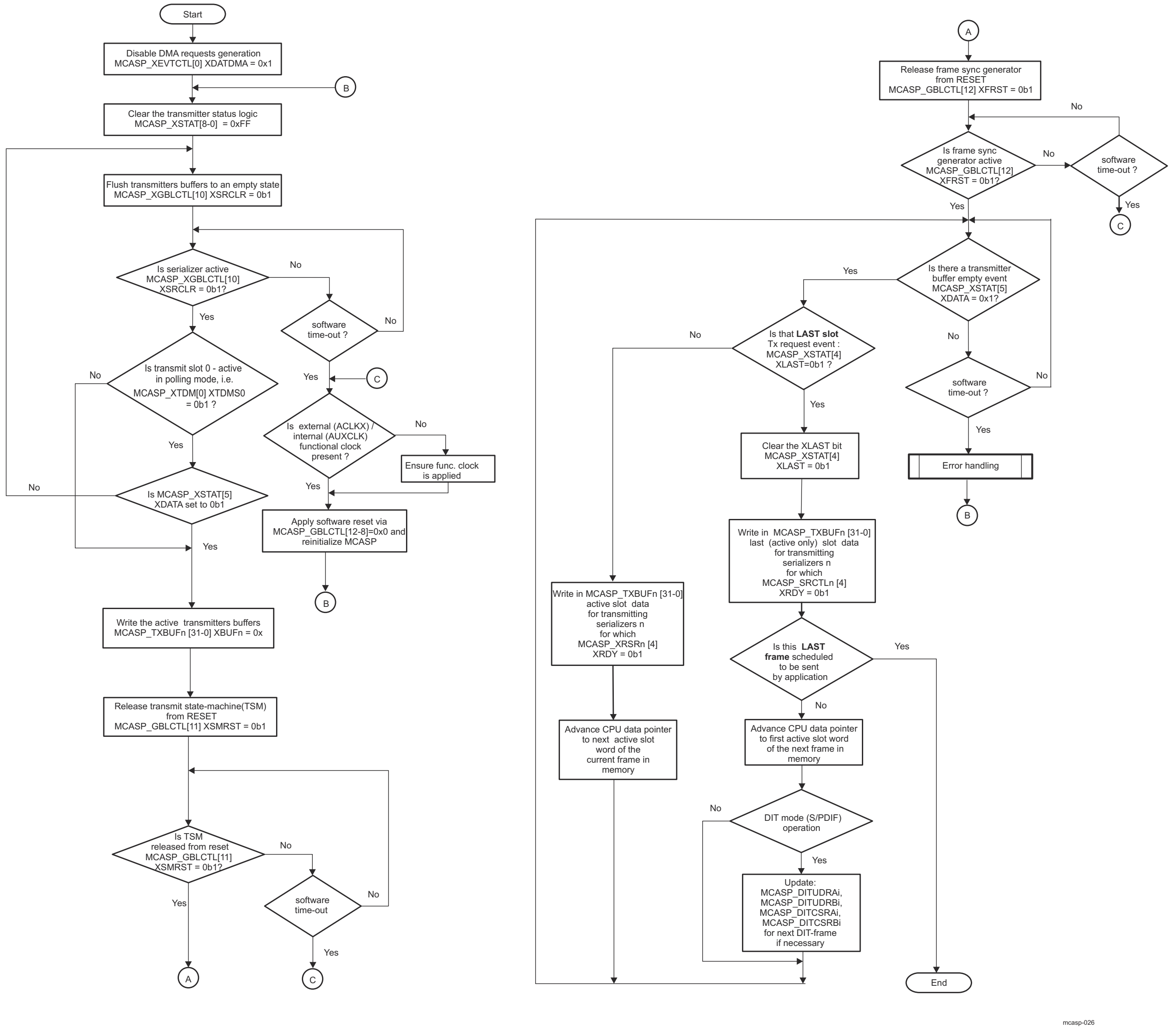


Figure 12-36. MCASP DIT- /TDM- Transmission Polling Method

These registers are for MCASP DIT-/TDM- transmission polling method: *MCASP_XEVTCTL*, MCASP_XSTAT, *MCASP_GBLCTL*, MCASP_XTDM, MCASP_XBUFn, MCASP_SRCTLn, MCASP_DITUDRAi, MCASP_DITUDRBi, MCASP_DITCSRAi, MCASP_DITCSRBi (n = 0 to 15 and i = 0 to 5).

Table 12-36 summarizes the subprocess call for the DIT-/TDM- transmission polling mode.

Table 12-36. Subprocess Call Summary for Main Sequence – MCASP DIT-/TDM- Transmission Polling Method

Subprocess Name	Cross-Reference
Error handling	Figure 12-42

12.1.2.5.2.1.2 Main Sequence – MCASP DIT- /TDM - Interrupt Transmission Method

Figure 12-37 shows the initial setup for interrupt-based transmission.

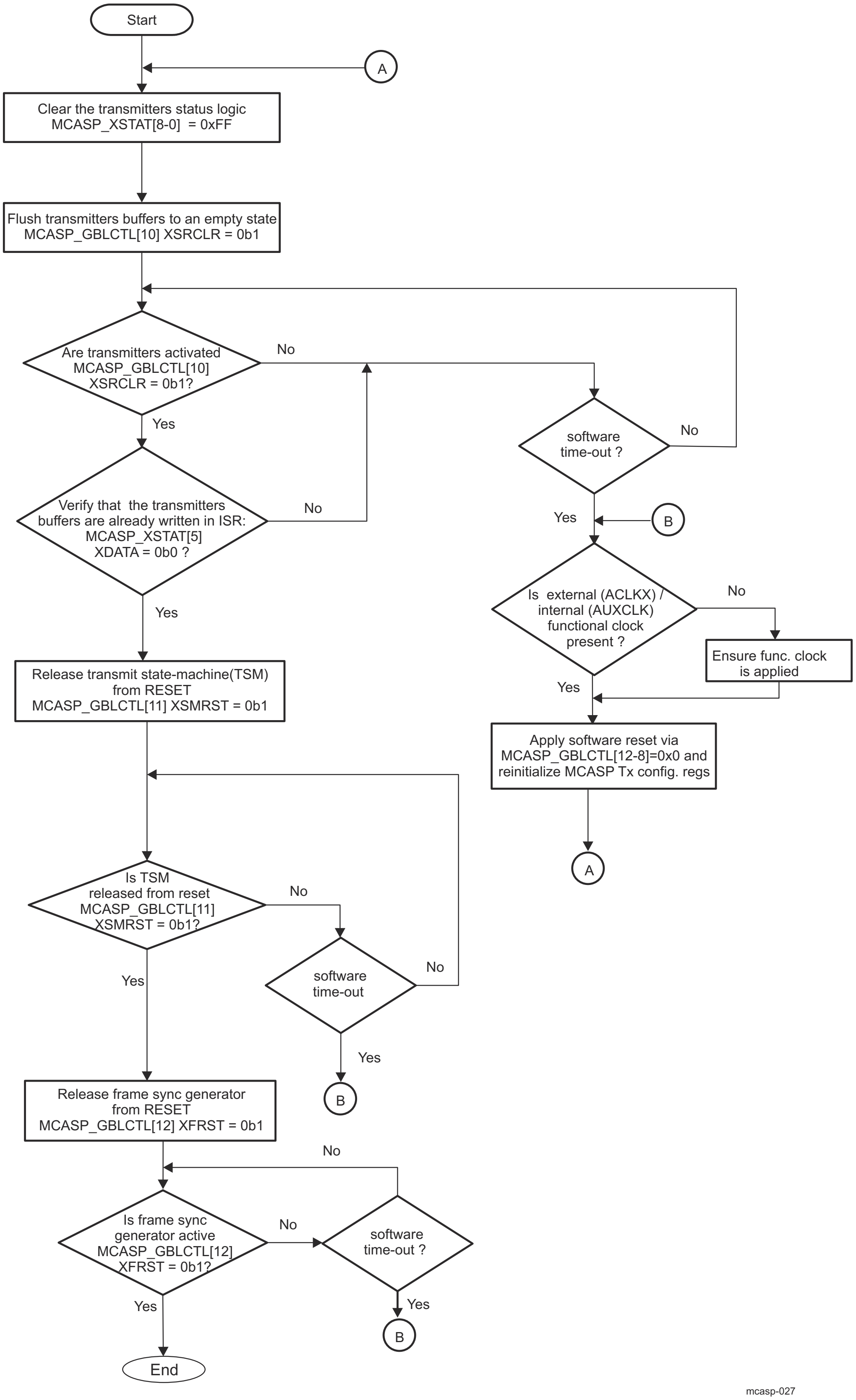


Figure 12-37. Subsequence – DIT-/TDM- Transmission Startup Procedure

Table 12-37 shows the configuration of the MCASP using an interrupt method for DIT-/TDM- transmission.

Table 12-37. MCASP DIT-/TDM- Interrupt Transmission Model

Step	Register/Bit Field/Programming Model	Value
Disable Tx DMA requests generation.	*MCASP_XEVTCTL*[0] XDATDMA	0x1
Enable the data ready event transmit interrupt.	MCASP_XINTCTL[5] XDATA	0x1
Optional: Enable the transmit error event interrupts.	MCASP_XINTCTL[2] XCKFAIL MCASP_XINTCTL[1] XSYNCERR MCASP_XINTCTL[0] XUNDRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt (useful for DIT user data/ channel status next S/PDIF frame info update).	MCASP_XINTCTL[7] XSTAFRM MCASP_XINTCTL[4] XLAST	0x1 0x1
IFwrite transfer is through the MCASP DATA port (MCASP_XFMT[3] XBUSEL is set to 0b0).	Software test condition (setting is done in step4 of the *MCASP Transmitters Global Initialization* - see Table 12-20)	
Enable the DATA port error based interrupt.	MCASP_XINTCTL[3] XDMAERR	0x1
ELSE		
Disable the DATA port error based interrupt.	MCASP_XINTCTL[3] XDMAERR	0x0
ENDIF		
DIT/TDM - Transmission Startup Procedure	See Figure 12-37.	

These registers are for MCASP DIT-/TDM- transmission startup procedure: *MCASP_GBLCTL*, *MCASP_XSTAT*.

12.1.2.5.2.1.3 Main Sequence –MCASP DIT- /TDM - Mode DMA Transmission Method

Table 12-38 shows the configuration of the ↓ using the DMA method for transmission. Possible interrupt error event servicing is also considered. shows the initial setup for DMA - based transmission.

> **Note**
>
> Because of the DATA port burst access capability with the DMA method, it is strongly recommended that DMA transfers are initiated through the MCASP DATA port.

Table 12-38. MCASP DMA Transmission Model with Interrupt Events Servicing

Step	Register/Bit Field/Programming Model	Value
Recommended: Select DATA port to access the transmit buffers.	MCASP_XFMT[3] XBUSEL	0x0
Enable the Tx DMA requests generation.	*MCASP_XEVTCTL*[0] XDATDMA	0x0
Enable the Tx DMA error event, because of MCASP DATA port usage.	MCASP_XINTCTL[3] XDMAERR	0x1
Optional: Enable the transmit error event interrupts.	MCASP_XINTCTL[2] XCKFAIL MCASP_XINTCTL[1] XSYNCERR MCASP_XINTCTL[0] XUNDRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt.	MCASP_XINTCTL[7] XSTAFRM MCASP_XINTCTL[4] XLAST	0x1 0x1
Disable the data ready event transmit interrupt, as DMA is used to service this request.	MCASP_XINTCTL[5] XDATA	0x0
DMA startup transmission procedure. This procedure is identical than the one shown in Figure 12-37. The only difference is that DMA automatically services all the XINT events raised by the MCASP, and no CPU data processing intervention is required. The CPU is involved only in error handling shown in Figure 12-40.	See Figure 12-37.	

12.1.2.5.2.2 MCASP Reception Modes

12.1.2.5.2.2.1 Main Sequence – MCASP Polling Reception Method

Figure 12-38 shows the MCASP polling reception method.

Note

The MCASP polling reception model considers thedevice CPUs as the accessor of audio data from the MCASP receive buffers.

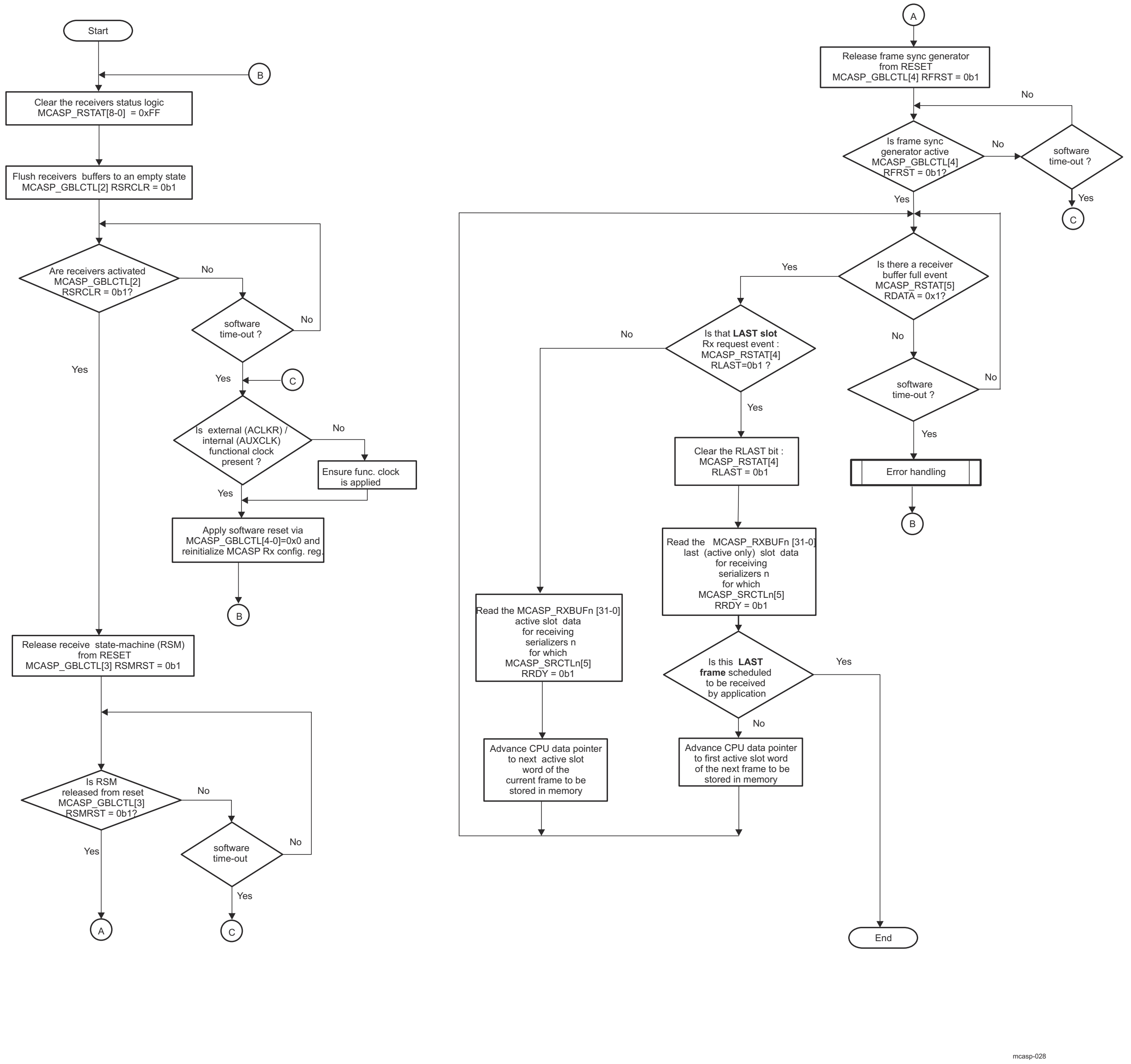


Figure 12-38. MCASP Polling Reception Method

These registers are for MCASP reception polling method: MCASP_RSTAT, MCASP_XGBLCTL, MCASP_RBUFn, MCASP_SRCTLn (n = 0 to 15).

Table 12-39 summarizes the subprocess call for the polling mode.

Table 12-39. Subprocess Call Summary for Main Sequence – MCASP Reception Polling Method

Subprocess Name	Cross-Reference
Error handling	Figure 12-43

12.1.2.5.2.2.2 Main Sequence – MCASP TDM - Interrupt Reception Method

Figure 12-39 shows the initial setup for interrupt-based reception.

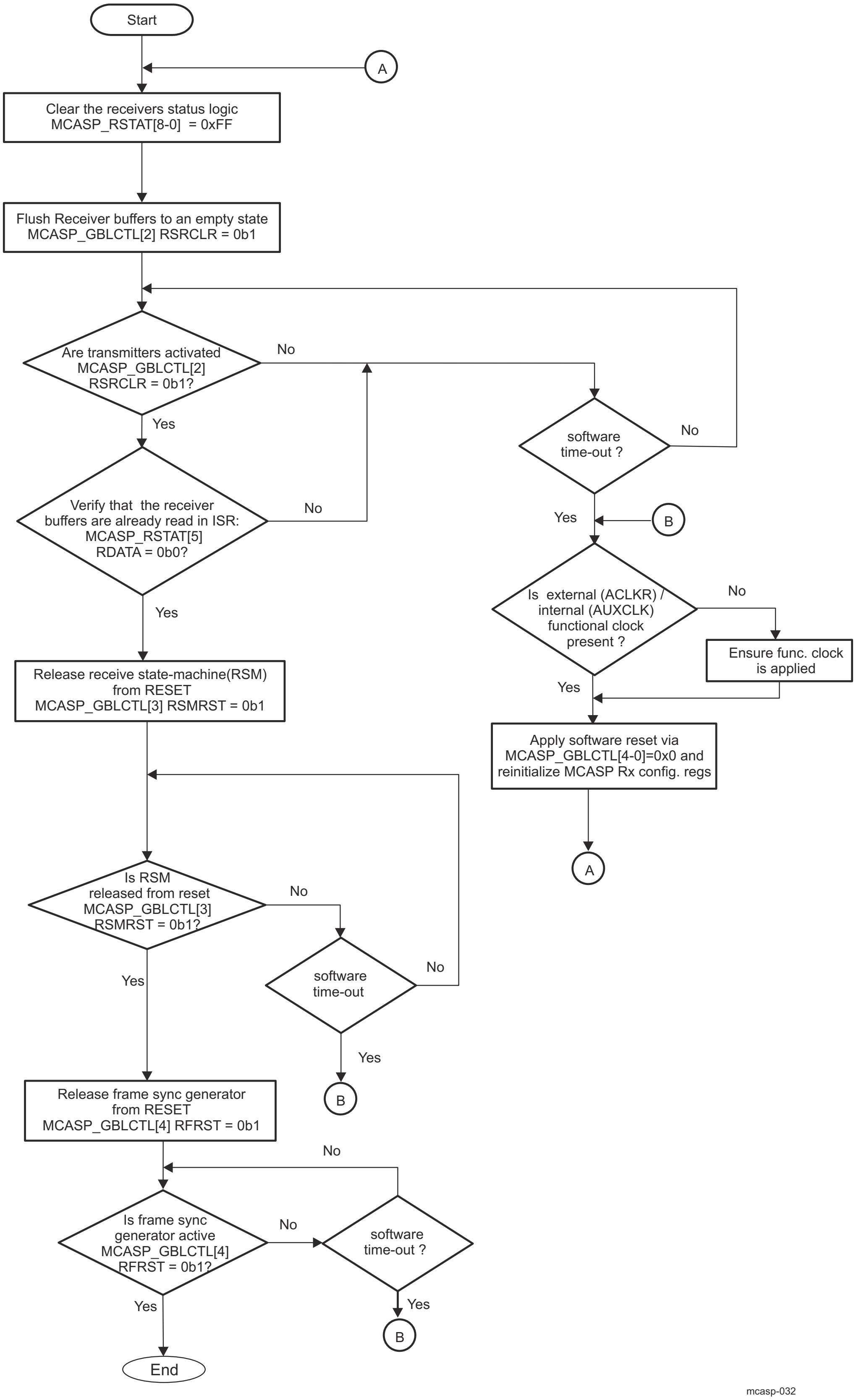


Figure 12-39. Subsequence – TDM - Reception Startup Procedure

Table 12-40 shows the configuration of the MCASP using an interrupt method for TDM- reception.

Table 12-40. MCASP TDM- Interrupt Reception Model

Step	Register/Bit Field/Programming Model	Value
Disable Rx DMA requests generation.	MCASP_PIDTCTL[0] RDATDMA	0x1
Enable the data ready event receive interrupt.	MCASP_RINTCTL[5] RDATA	0x1
Optional: Enable the receive error event interrupts.	MCASP_RINTCTL[2] RCKFAIL MCASP_RINTCTL[1] RSYNCERR MCASP_RINTCTL[0] ROVRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt	MCASP_RINTCTL[7] RSTAFRM MCASP_RINTCTL[4] RLAST	0x1 0x1
IF read transfer is through the MCASP DATA port (MCASP_RFMT[3] RBUSEL is set to 0b0).	Software test condition (setting is done in step4 of the *MCASP Receivers Global Initialization for TDM-Mode Operation* - see Table 12-26)	
Enable the DATA port error based interrupt.	MCASP_RINTCTL[3] RDMAERR	0x1
ELSE		
Disable the DATA port error based interrupt.	MCASP_RINTCTL[3] RDMAERR	0x0
ENDIF		
TDM - Transmission Startup Procedure	See Figure 12-39.	

These registers are for MCASP TDM- interrupt reception model: MCASP_XGBLCTL, MCASP_RSTAT.

12.1.2.5.2.2.3 Main Sequence – MCASP TDM - Mode DMA Reception Method

Table 12-41 shows the configuration of the MCASP using the DMA method for reception. Possible interrupt error event servicing is also considered. shows the initial setup for DMA - based transmission.

Note

Because of the DATA port burst access capability with the DMA method, it is strongly recommended that DMA transfers are initiated through the MCASP DATA port.

Table 12-41. MCASP DMA Reception Model with Interrupt Events Servicing

Step	Register/Bit Field/Programming Model	Value
Recommended: Select DATA port to access the transmit buffers.	MCASP_RFMT[3] RBUSEL	0x0
Enable the Rx DMA requests generation.	MCASP_PIDTCTL[0] RDATDMA	0x0
Enable the Rx DMA error event, because of MCASP DATA port usage.	MCASP_RINTCTL[3] RDMAERR	0x1
Optional: Enable the receive error event interrupts.	MCASP_RINTCTL[2] RCKFAIL MCASP_RINTCTL[1] RSYNCERR MCASP_RINTCTL[0] ROVRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt.	MCASP_RINTCTL[7] RSTAFRM MCASP_RINTCTL[4] RLAST	0x1 0x1
Disable the data ready event receive interrupt, as DMA is used to service this request.	MCASP_RINTCTL[5] RDATA	0x0
DMA startup reception procedure. This procedure is identical than the one shown in Figure 12-39. The only difference is that DMA automatically services all the RINT events raised by the MCASP, and no CPU data processing intervention is required. The CPU is involved only in error handling shown in Figure 12-41.	See Figure 12-39.	

12.1.2.5.2.3 MCASP Event Servicing

12.1.2.5.2.3.1 MCASP DIT-/TDM- Transmit Interrupt Events Servicing

Figure 12-40 shows the flow of DIT-/TDM- mode transmit interrupt events servicing for the MCASP module.

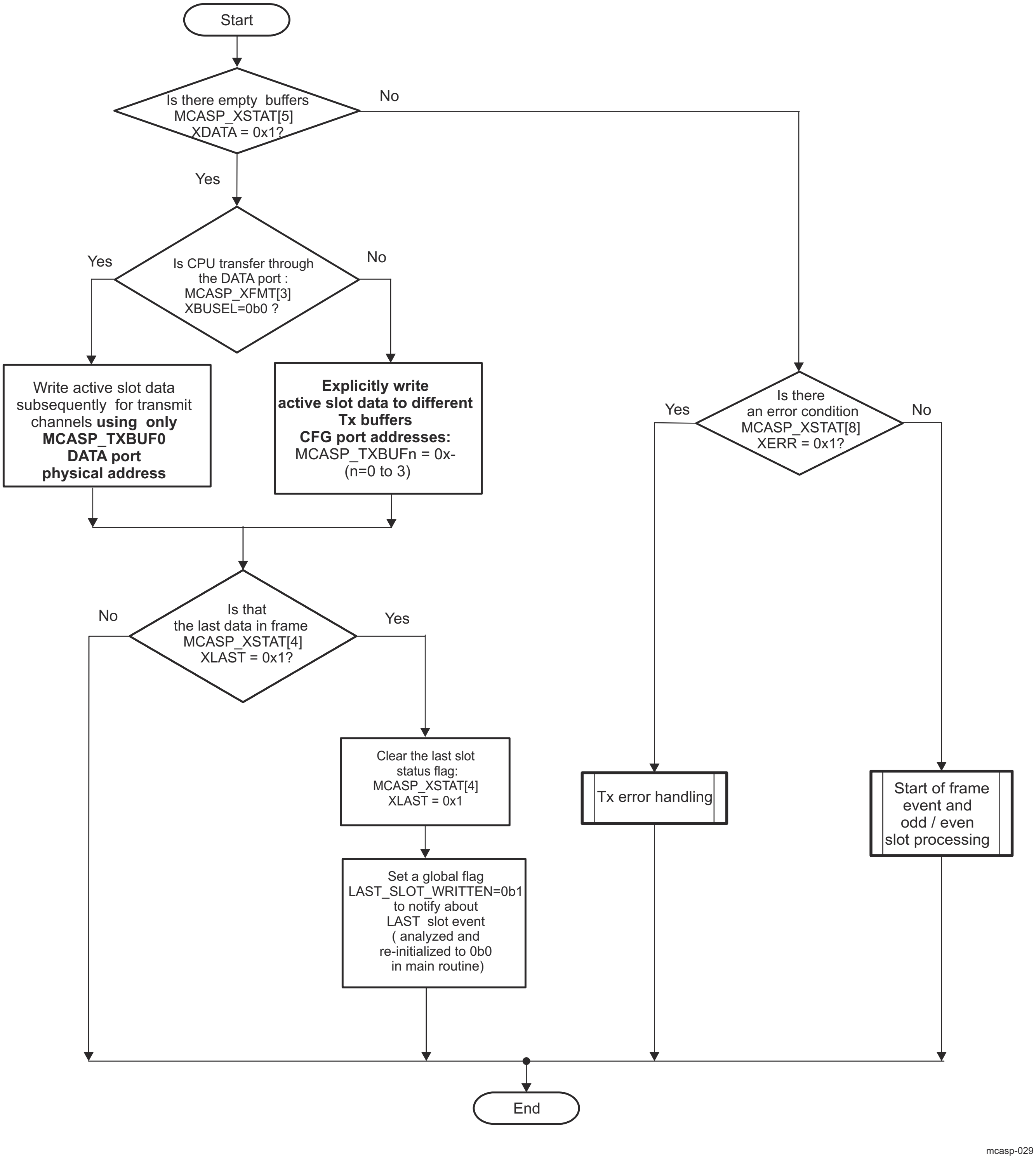


Figure 12-40. MCASP Transmit Interrupt Events Servicing

12.1.2.5.2.3.2 MCASP TDM- Receive Interrupt Events Servicing

Figure 12-41 shows the flow of DIT-/TDM- mode transmit interrupt events servicing for the MCASP module.

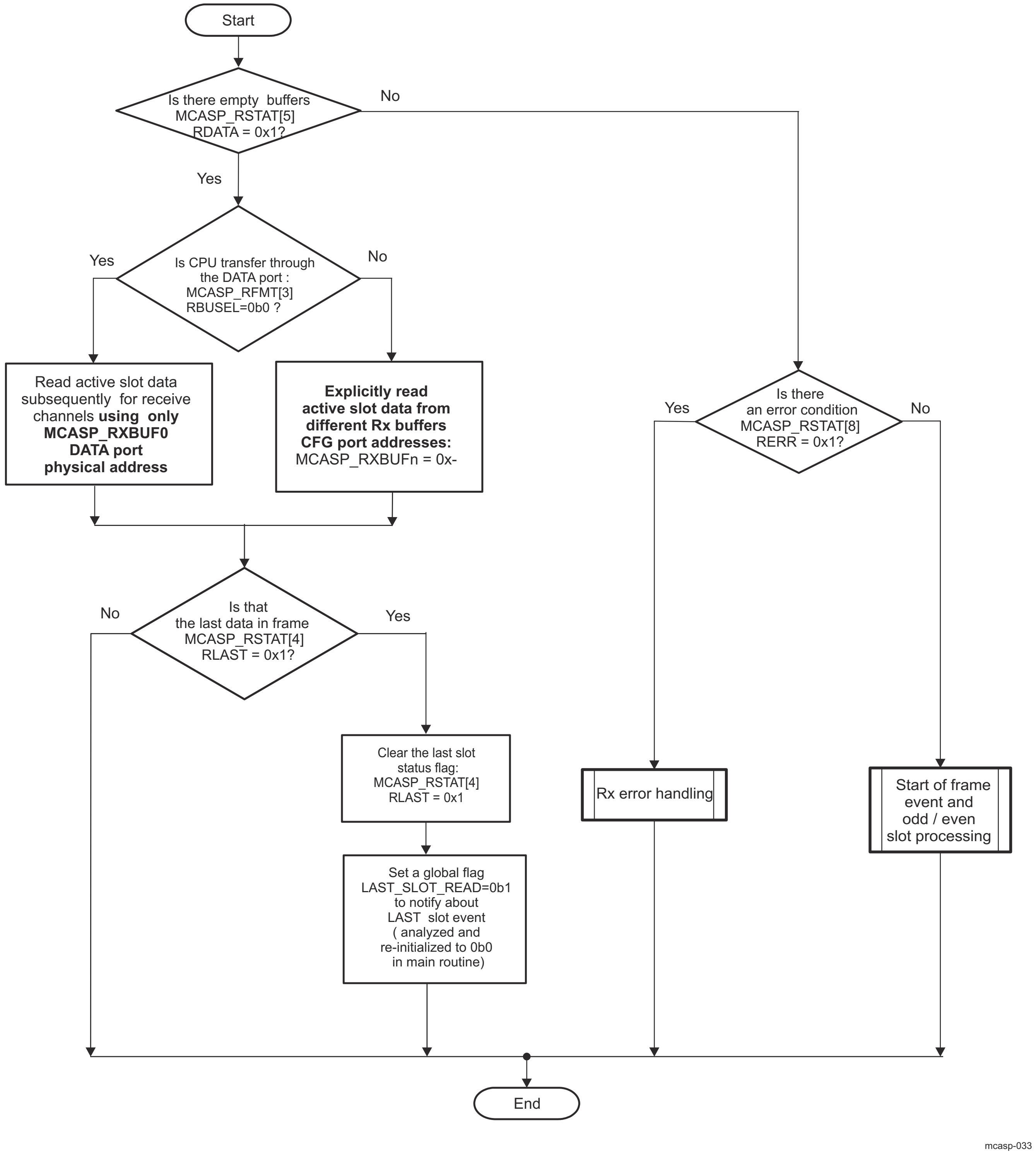


Figure 12-41. MCASP Receive Interrupt Events Servicing

These registers are for MCASP receive interrupt events servicing: MCASP_RSTAT, MCASP_RBUFn, MCASP_RFMT (n = 0 to 15).

Table 12-42 lists the subprocess call summary for receive interrupt events servicing.

Table 12-42. Subprocess Call Summary for Receive Interrupt Events Servicing

Subprocess Name	Cross-Reference
MCASP receive error handling	Figure 12-43

Table 12-42. Subprocess Call Summary for Receive Interrupt Events Servicing (continued)

Subprocess Name	Cross-Reference
Start of frame handling	Section 12.1.2.4.12.2, *Receive Data Ready Event and Interrupt*

12.1.2.5.2.3.3 Subsequence – MCASP DIT-/TDM -Modes Transmit Error Handling

Figure 12-42 shows the transmit error handling schema for the MCASP, which can be implemented as part of the Tx interrupt service routine or as part of the Tx polling sequence.

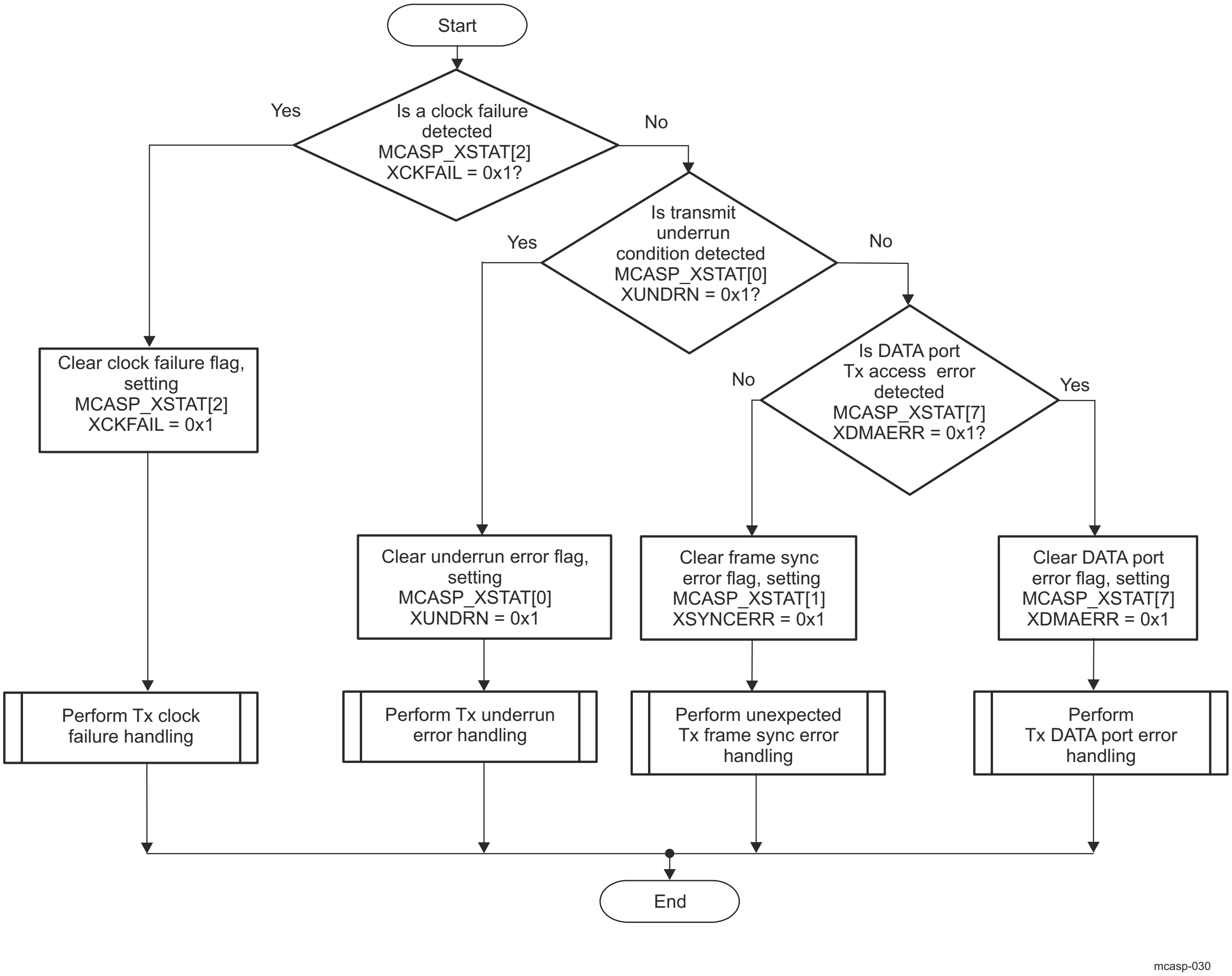


Figure 12-42. MCASP Transmit Error Handling

Note

- For more information about transmit clock failure handling, see Section 12.1.2.4.15.6.2, *Transmit Clock Failure Check and Recovery*.
- For more information about transmit buffer underrun handling, see Section 12.1.2.4.15.1, *Buffer Underrun Error -Transmitter*.
- For more information about DATA port Tx error handling, see Section 12.1.2.4.15.3, *DATA Port Error - Transmitter*.
- For more information about unexpected Tx frame sync error handling, see Section 12.1.2.4.15.5, *Unexpected Frame Sync Error*.

12.1.2.5.2.3.4 Subsequence – MCASP Receive Error Handling

Figure 12-43 shows the receive error handling schema for the MCASP, which can ONLY be implemented as part of the Rx polling sequence.

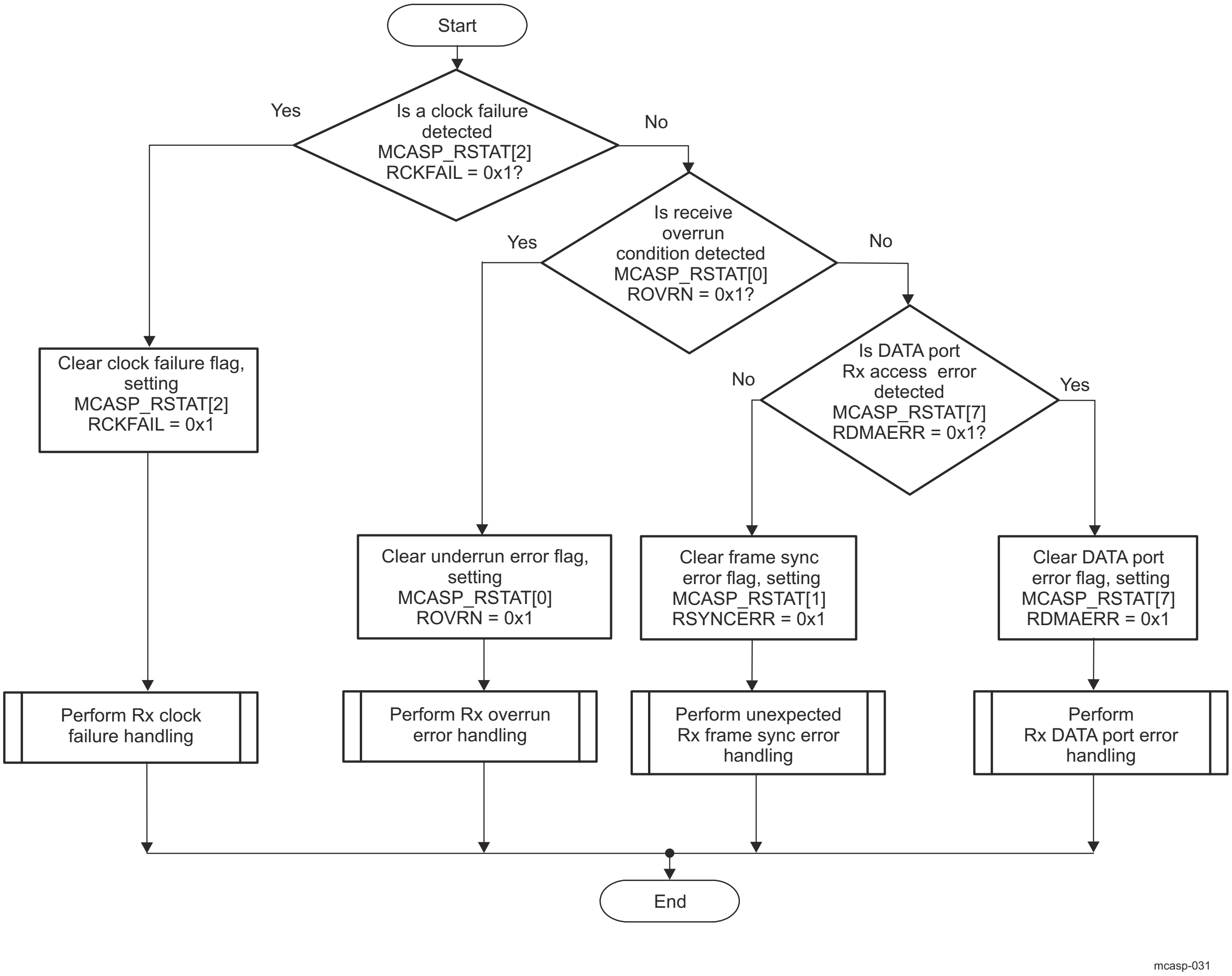


Figure 12-43. MCASP Receive Error Handling

This register is for MCASP receive error handling: MCASP_RSTAT.

Note

- For more information about receive clock failure handling, see Section 12.1.2.4.15.6.3, *Receive Clock Failure Check and Recovery*.
- For more information about receive buffer overrun handling, see Section 12.1.2.4.15.2, *Buffer Overrun Error - Receiver*.
- For more information about DATA port Rx error handling, see Section 12.1.2.4.15.4, *DATA Port Error - Receiver*.
- For more information about unexpected Rx frame sync error handling, see Section 12.1.2.4.15.5, *Unexpected Frame Sync Error*.

12.1.3 Audio Tracking Logic (ATL)

This chapter describes the integration of the Audio Tracking Logic (ATL) subsystem in the device.

12.1.3.1 ATL Overview

The Audio Tracking Logic (ATL) is used by HD Radio™ applications to synchronize the digital audio output to the baseband clock. This same IP can also be used generically to track errors between two reference signals (such as frame syncs) and generate a modulated clock output (using software-controlled cycle stealing) which averages to some desired frequency. This process can be used as a hardware assist for asynchronous sample rate conversion algorithms.

12.1.3.1.1 ATL Features Overview

The ATL module supports the following features:

- One ATL module, containing four ATL instances, for HD Radio support and asynchronous sample rate conversion assistance
- Each instance tracks the time error between two syncs (local audio word select [AWS] and baseband word select [BWS])
- Each instance selects between 28 mux choices for BWS and 30 mux choices for AWS.
- Each instance generates modulated ATCLK clock signals with software-initiated pulse stealing. The intention is to use these clocks to derive audio output bit clock on MCASP
- Selection between ATL_VCLK clock or functional ATL_PCLK to run error counting timers and to derive modulated ATCLK clock outputs.
- Clock and reset management: Receives clock and reset signals from the device PSC module. The ATL module receives hardware reset.
- Power management: The ATL belongs to the PD0 power domain.
- Local software reset

Unsupported Features:

- See the Module Integration section of this document for a list of module features not supported by the integration on this Device.

12.1.3.1.2 ATL Ports

Table 12-43. ATL Clocks and Resets

Clocks	
Module Clock Input	**Description**
ATL_VCLK	ATL interface clock
ATL_PCLK	ATL functional clock.
Resets	
Module Reset Input	**Description**
ATL_RST	ATL reset

12.1.3.2 ATL Functional Description

This section is a functional description of the ATL module.

12.1.3.2.1 ATL Block Diagram

The tracking mechanism is capable of handling all input (baseband) and output (audio) sampling rates used by HD Radio. The ATL works on a single-clock domain and is insensitive to a particular choice of the master clock frequency as long as it is divisible by the desired audio frequency.

The ATL consists of two circuits: Measurement Circuit and Adjustment Circuit.

The main interface includes two registers:

- Read register in the measurement circuit, baseband sample registers (four compare clear registers ATL0_BBSR, ATL1_BBSR, ATL2_BBSR, and ATL3_BBSR).
- Write register in the adjustment circuit, parts-per-million register (four compare clear registers ATL0_PPMR, ATL1_PPMR, ATL2_PPMR, and ATL3_PPMR).

The measurement circuit includes an 8-bit rolling counter, a 16-bit rolling counter, and the 16-bit sample count register. The 8-bit counter counts audio clock cycles. The 16-bit counter counts the number of baseband samples received by the modem. When the 8-bit counter rolls over, the content of the 16-bit counter is strobed into the sample count from four compare clear registers (ATL0_BBSR, ATL1_BBSR, ATL2_BBSR, and ATL3_BBSR). The HD Radio library uses this content to determine the relative frequency offset between the audio clock and baseband sampling clock.

The adjusting circuit produces a timing signal at the top of the audio clock tree, which is used by dividers that make the audio timing signals including DAC oversampling clock, bit clock, and word select. The output is occasionally adjusted by altering the divide count by one “tick” of the master clock. It includes a 20-bit accumulator circuit with a 9-bit PPM from four compare clear registers (ATL0_PPMR, ATL1_PPMR, ATL2_PPMR, and ATL3_PPMR) and an adjustable clock divider from four compare clear registers (ATL0_ATLCR, ATL1_ATLCR, ATL2_ATLCR, and ATL3_ATLCR). The content of the four compare clear registers (ATL0_PPMR, ATL1_PPMR, ATL2_PPMR, and ATL3_PPMR) is subtracted from the accumulator every master clock (ATL_PCLK) cycle. On underflow, the audio clock divider adds or subtracts one master clock (ATL_PCLK) period from the nominal periods of the audio clocks. The rate of adjustments in PPM (parts-per-220) is exactly the value written to PPM from four compare clear registers (ATL0_PPMR, ATL1_PPMR, ATL2_PPMR, and ATL3_PPMR). The MSB or PPM from four compare clear registers (ATL0_PPMR, ATL1_PPMR, ATL2_PPMR, and ATL3_PPMR) of the PPM register determines whether the audio clock period is shortened or lengthened.

Figure 12-44 shows the ATL top-level block diagram.

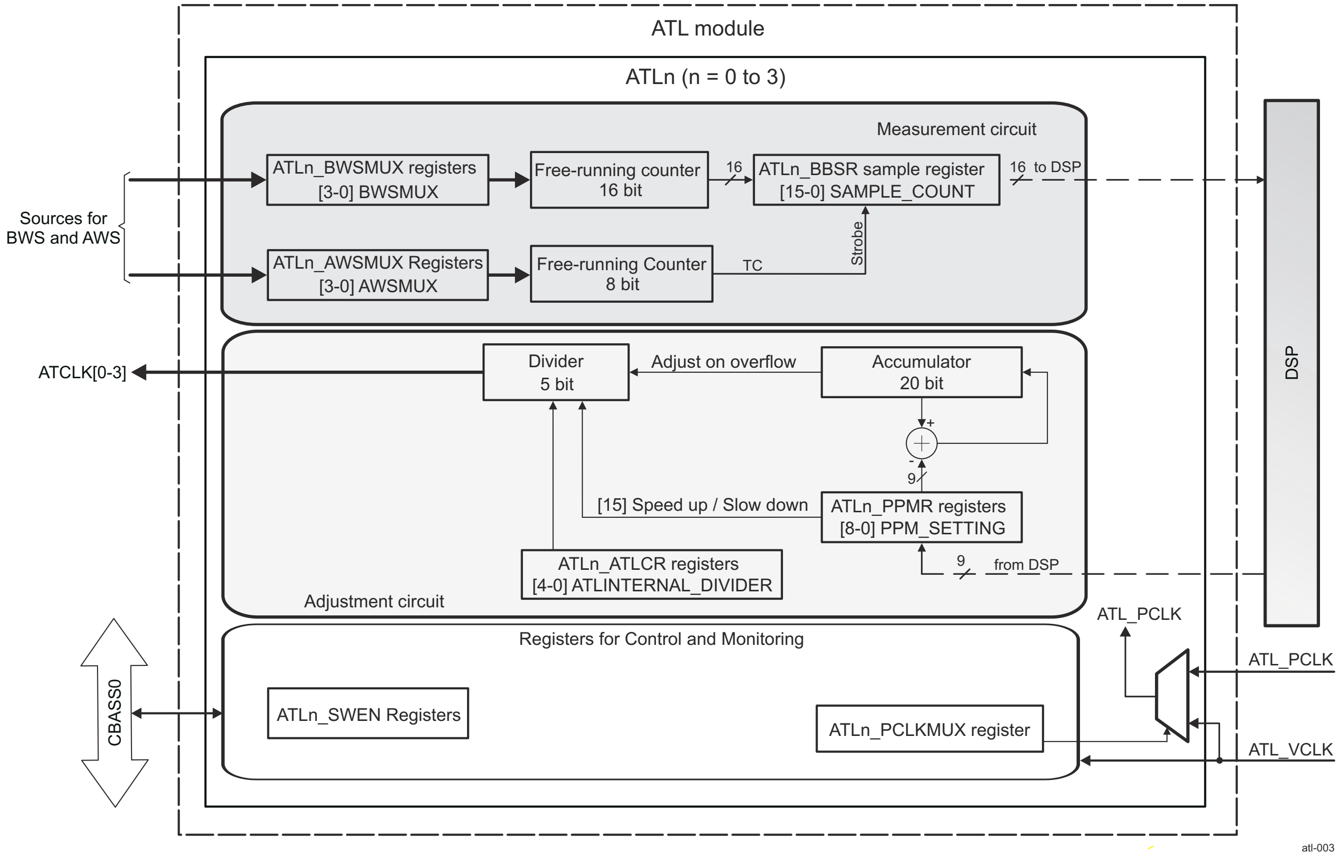


Figure 12-44. ATL Block Diagram

12.1.3.2.2 ATL Source Signal Control

The sources for BWS and AWS inputs are defined by internal muxing from multiple reference signals.

BWS and AWS are logic inputs, not clocks, to the ATL module. ATL performs an edge detection on these signals. To minimize jitter in HD Radio clocking implementation, ATL_PCLK must be higher than 100 MHz. When ATL is used for HD Radio applications, the measuring circuit is connected to the word select signal from Audio IIS output (AWS) and Baseband IIS input (BWS). The (ATL0_BWSMUX, ATL1_BWSMUX, ATL2_BWSMUX, and ATL3_BWSMUX) and (ATL0_AWSMUX, ATL1_AWSMUX, ATL2_AWSMUX, and ATL3_AWSMUX) registers select which inputs are used as the ATL BWS and AWS inputs.

12.1.3.2.3 ATL Clock and Reset Configuration

The ATL module is clocked by a functional clock (ATL_PCLK) and one interface clock (ATL_VCLK).

- The functional clock is used to generate control signals depending on the internal configuration of the module. The ATL_PCLK selection register mux for one of four compare clear registers (ATL0_PCLKMUX, ATL1_PCLKMUX, ATL2_PCLKMUX, and ATL3_PCLKMUX) chooses the functional clock for ATL_PCLK input to run error counting timers and to derive modulated ATCLK clock outputs.
- ATL0_VCLK is used to trigger access to the ATL configuration interface through the CBASS0 Interconnect.
- A software reset register is provided to hold the four ATL modules in reset while the AWS/BWS and ATL0_PCLK mux selections are set and while the system-level clocking is configured. Software is required to release the module from reset. Software must enable the bit [0] for one of four compare clear registers (ATL0_SWEN, ATL1_SWEN, ATL2_SWEN, and ATL3_SWEN) to enable the ATL. Each ATL in the device must be independently enabled.

12.1.4 Media Local Bus Subsystem (MLBSS)

This chapter describes the function, operation, and configuration of the Media Local Bus Subsystem (MLBSS) in the device.

12.1.4.1 MLBSS Overview

The MLBSS provides a MediaLB/MediaLB+ controller and an interface to other MediaLB/MediaLB+ devices. The MediaLB/MediaLB+ interface allows also connection to a MOST (Media Oriented Systems Transport) network controller.

Figure 12-45 shows the MLBSS overview.

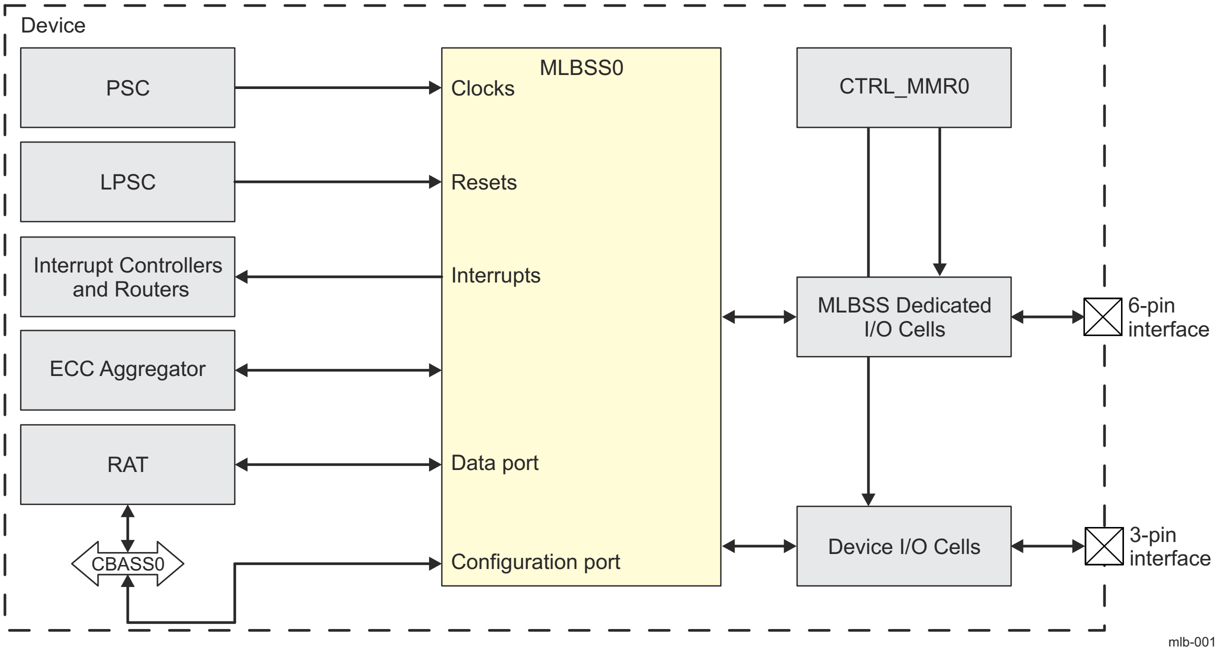


Figure 12-45. MLBSS Overview

12.1.4.1.1 MLBSS Features

The MLBSS supports the following features:

- 3-pin MediaLB 3.3V LVCMOS I/Os compliant to MediaLB Physical Layer and Link Layer Specification v4.2
- 6-pin MediaLB+ low-voltage differential signaling (LVDS) I/Os (3 differential pairs) compliant to MediaLB Physical Layer and Link Layer Specification v4.2
- MediaLB core functionality compliant to MediaLB Physical Layer and Link Layer Specification v4.2
- Supports 256/512/1024Fs in 3-pin mode
- Supports 2048Fs in 6-pin mode using a 1:1 recovered-to-external clock ratio
- Supports 3072/4096Fs in 6-pin mode using a 2:1 recovered-to-external clock ratio
- Supports all types of transfers (synchronous stream data, asynchronous packet data, control message data, and isochronous data) over 64 logical channels
- Supports single 32-bit slave interface for configuration
- Supports single 32-bit master interface with burst capability for DMA transfers into system memory. The maximum burst size is 32 Bytes
- RAT module on the master interface to translate the 32-bit address into a 40-bit system address
- ECC aggregator to protect internal memories
- Has 16 KB buffer for all types of transfers in the subsystem
- Dedicated register for controlling the MLBSS priority on the system interconnect

12.1.4.1.2 MLBSS Not Supported Features

The MLBSS does not support the following:

- 5-pin mode
- Intelligent hardware-controlled power down. It is software responsibility to put the MLB core into idle state (see Section 12.1.4.4.3) before the system stops the MLBSS clocks.

12.1.4.2 MLBSS Environment

This section describes the MLBSS external connections (environment).

Figure 12-46 shows the MLBSS associated signals available on device pads.

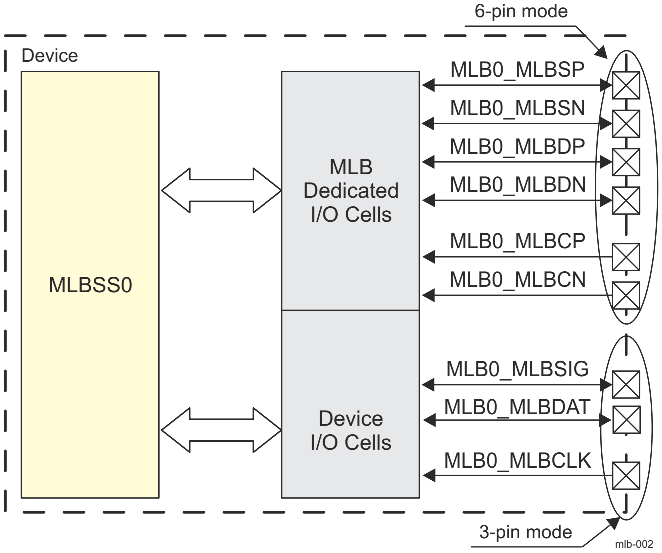


Figure 12-46. MLBSS Subsystem Environment

Table 12-44 describes the MLBSS I/O signals used in both 3-pin and 6-pin modes.

Table 12-44. MLBSS Subsystem I/O Description

Device Level Signal	I/O(1)	Description
	6-pin mode	
MLB0_MLBSP	I/O	Differential pair signal line
MLB0_MLBSN	I/O	
MLB0_MLBDP	I/O	Differential pair data line
MLB0_MLBDN	I/O	
MLB0_MLBCP	I	Differential pair clock line
MLB0_MLBCN	I	
	3-pin mode	
MLB0_MLBSIG	I/O	Single ended signal line
MLB0_MLBDAT	I/O	Single ended data line
MLB0_MLBCLK	I	Single ended clock line

(1) I = Input; O = Output; I/O = Bidirectional

Note

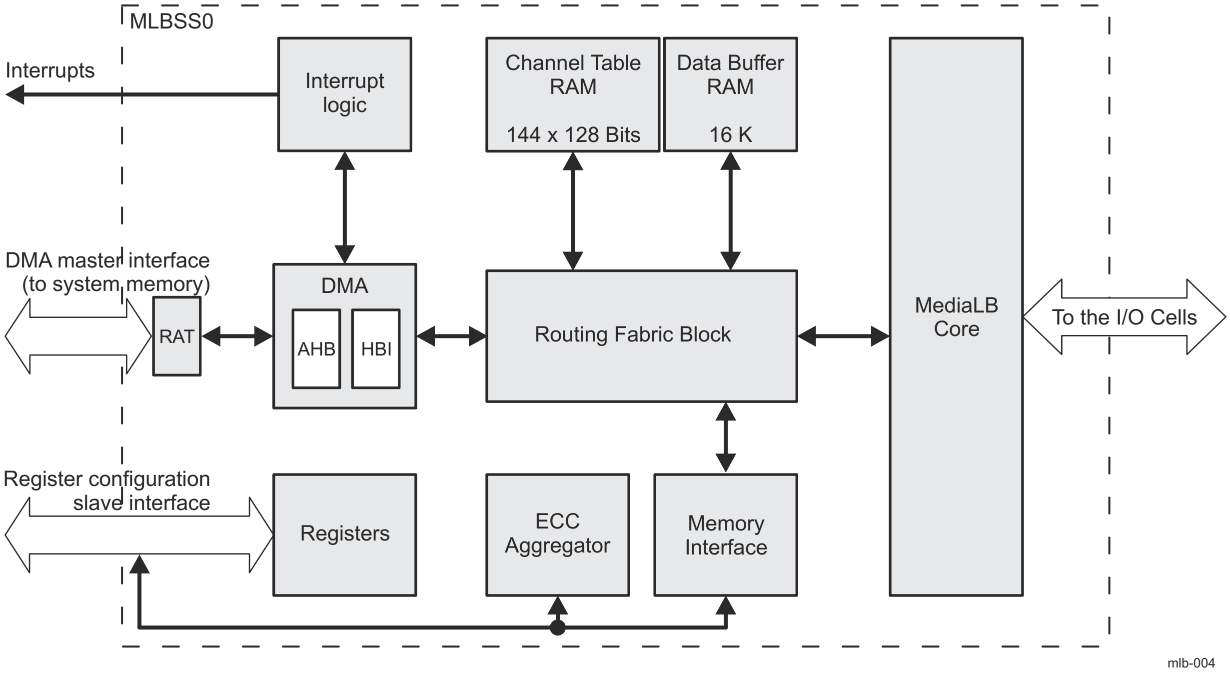
For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.1.4.3 MLBSS Functional Description

12.1.4.3.1 MLBSS Block Diagram

Figure 12-47 shows the MLBSS block diagram. It includes the following functional blocks:

- MediaLB core – Implements the physical and link layer requirements of either a 3-pin or the 6-pin interface. Serial-to-parallel/parallel-to-serial are also implemented along with MediaLB frame synchronization.
- Routing fabric block – Manages the flow of data between the MediaLB core and the DMA block, implementing bus arbiter and muxing logic to the channel table RAM and the data buffer RAM.
- Channel table RAM (CTR) – Used for storing channel descriptors for managing accesses to dynamic buffers in the data buffer RAM.
- Data buffer RAM (DBR) – Provides dynamic circular buffering between the transmit and receive devices.
- Memory interface – Implements a bridge between the configuration TeraNet_CFG slave interface and the channel table RAM or data buffer RAM interfaces.
- DMA – Implements a bus bridge between the DMA master and the routing fabric block.
- Registers – Used for configuration.
- Interrupt logic.
- RAT – The MLBSS natively supports 32-bit addressing. As the SoC has 40-bit address bus a RAT module is put on the MLBSS master interface to translate the 32-bit addresses into 40-bit system addresses. For information about the RAT module functionality, see *Region-based Address Translation (RAT) Module*.
- ECC Aggregator – Performs single error correction and double error detection over the DBR. For information about the ECC aggregator functionality, see *ECC Aggregator*.



AHB - Advanced High-performance Bus

HBI - Host Bus Interface

Figure 12-47. MLBSS Structural Overview

12.1.4.3.1.1 MediaLB Core Block

Although the MediaLB block supports both a MediaLB 3-pin and 6-pin interface, only one of these interfaces is active at any given time. The selection is done through the MLB_MLBC0[5] MLBPEN bit. *MLBSS Subsystem I/O Description* describes the signals associated with 3-pin and 6-pin modes. Both MediaLB interfaces provide real-time access to all network data types including streaming, packet, control, and isochronous data.

The MediaLB 3-pin interface supports the MediaLB protocol for single-ended 3-pin mode with a maximum data rate of 1024Fs.

The MediaLB 6-pin interface supports the MediaLB protocol for high-speed differential 6-pin mode, with a maximum data rate of 4096Fs.

There is a set of physical channels implemented for exchanging data over the MediaLB 3-pin or 6-pin interface. These physical channels (called quadlets) are 4-byte wide and can also be grouped together to form logical channels. These logical channels are referenced using channel addresses, and define a uni-directional path between a specific MediaLB device transmitting data and another specific MediaLB device receiving data. In other words, the logical channel is a group of multiple quadlets, which selects a unique pair of MediaLB devices with a unique channel address. The logical channels, configured by the system software can be of any combination of channel types (synchronous, asynchronous, control, or isochronous) and direction (transmit/receive).

The MediaLB channel addresses are mapped to the logical channels as shown in Table 12-45.

Table 12-45. MediaLB Channel Address to Logical Channel Mapping

MediaLB Channel Address	Logical Channel Number
02h	1
04h	2
06h	3
…	…
007Ch	62
007Eh	63
01FEh	0 (1)

(1) The logical channel 0 is the system channel and is reserved.

Thus, 64 logical channels can be supported and one of them is the system channel which is reserved.

Note

The MediaLB channel address should always be an even number.

12.1.4.3.1.2 Routing Fabric Block

The routing fabric block manages the flow of data between the MediaLB core and the DMA block. Bus multiplexers and a bus arbiter are implemented in the routing fabric block for accessing the channel table RAM and data buffer RAM. Each DMA controller in the routing fabric uses channel descriptors to manage access to dynamic buffers in the data buffer RAM. These channel descriptors are stored in the channel table RAM.

12.1.4.3.1.3 Data Buffer RAM

The data buffer RAM is 8-bit × 16k entries deep and provides dynamic circular buffering between the transmit and receive devices. The size and location of each data buffer is defined by software in the channel descriptor table, which is located in the channel table RAM.

The DMA controllers in the routing fabric are responsible for ensuring that the circular buffers do not overflow or underflow. Each channel type (that is, synchronous, isochronous, asynchronous and control) has full and empty detection.

12.1.4.3.1.4 Channel Table RAM

The channel table RAM is 128-bit × 144-entry (max). It allows system software to dynamically configure channel routing and allocate data buffers in the data buffer RAM.

The channel table RAM is logically divided into three subtables:

- Channel descriptor table
- DMA descriptor table
- Channel allocation table

The details of the channel descriptor table and channel allocation table are described in Table 12-46.

The details of the DMA descriptor table are described in Table 12-56.

Table 12-46. Channel Table RAM Address Mapping

<table>
<tr><th>Label</th><th>Address</th><th colspan="2">Bits 127-96</th><th colspan="2">Bits 95-64</th><th colspan="2">Bits 63-32</th><th colspan="2">Bits 31-0</th></tr>
<tr><td colspan="10">Channel Descriptor Table (CDT):</td></tr>
<tr><td rowspan="7">Channel descriptor table</td><td>00h</td><td colspan="8">CDT0[127-0], CL = 0</td></tr>
<tr><td>01h</td><td colspan="8">CDT1[127-0], CL = 1</td></tr>
<tr><td>02h</td><td colspan="8">CDT2[127-0], CL = 2</td></tr>
<tr><td>…</td><td colspan="8">…</td></tr>
<tr><td>3Dh</td><td colspan="8">CDT61[127-0], CL = 61</td></tr>
<tr><td>3Eh</td><td colspan="8">CDT62[127-0], CL = 62</td></tr>
<tr><td>3Fh</td><td colspan="8">CDT63[127-0], CL = 63</td></tr>
<tr><td colspan="10">DMA Descriptor Table (DDT):</td></tr>
<tr><td rowspan="7">DMA descriptor table</td><td>40h</td><td colspan="8">DDT0[127-0], CAT64</td></tr>
<tr><td>41h</td><td colspan="8">DDT1[127-0], CAT65</td></tr>
<tr><td>42h</td><td colspan="8">DDT2[127-0], CAT66</td></tr>
<tr><td>…</td><td colspan="8">…</td></tr>
<tr><td>7Dh</td><td colspan="8">DDT61[127-0], CAT125</td></tr>
<tr><td>7Eh</td><td colspan="8">DDT62[127-0], CAT126</td></tr>
<tr><td>7Fh</td><td colspan="8">DDT63[127-0], CAT127</td></tr>
<tr><td colspan="10">Channel Allocation Table (CAT):</td></tr>
<tr><td rowspan="3">Channel allocation table for MediaLB</td><td>80h</td><td>CAT7</td><td>CAT6</td><td>CAT5</td><td>CAT4</td><td>CAT3</td><td>CAT2</td><td>CAT1</td><td>CAT0</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>87h</td><td>CAT63</td><td>CAT62</td><td>CAT61</td><td>CAT60</td><td>CAT59</td><td>CAT58</td><td>CAT57</td><td>CAT56</td></tr>
<tr><td rowspan="3">Channel allocation table for DMA</td><td>88h</td><td>CAT71</td><td>CAT70</td><td>CAT69</td><td>CAT68</td><td>CAT67</td><td>CAT66</td><td>CAT65</td><td>CAT64</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>8Fh</td><td>CAT127</td><td>CAT126</td><td>CAT125</td><td>CAT124</td><td>CAT123</td><td>CAT122</td><td>CAT121</td><td>CAT120</td></tr>
</table>

Note

A fixed relationship between DMA descriptor table entries and DMA channel allocation table entries exists. When using DMA channel 0 (CAT64) software should program DDT0. When using DMA channel 1 (CAT65) software should program DDT1, in case of CAT66 DDT2 should be programmed and so on. In case of CAT127 software should program DDT63.

The following base addresses are valid:

- Channel descriptor table has base address 00h
- DMA descriptor table has base address 40h
- Channel allocation table for MediaLB has base address 80h
- Channel allocation table for DMA has base address 88h

12.1.4.3.1.4.1 Channel Allocation Table

The channel allocation table comprises 16 entries of the channel table RAM. Each entry is 16-bit. The first entry starts at address 80h and the sixteenth entry at address 8Fh. Each 16-bit channel allocation table entry represents a logical connection to or from a transmit/receive device (that is, MediaLB or DMA channel). All entries are indexed according to a fixed physical address assigned to every Rx/Tx channel. This is shown in Table 12-47. The value stored in a channel allocation table entry includes a 6-bit connection label (CL[5-0]), which provides a pointer to the channel descriptor table. To complete a logical channel and form a routing connection, system software must assign the same connection label to both the Rx and Tx channels.

Table 12-47. Channel Allocation Table Entry Map

Peripheral	Number of Tx Channels Allowed	Number of Rx Channels Allowed	Channel Allocation Table Start Index	Channel Allocation Table End Index	Entries
MediaLB	0 to 64	64 - (Number of Tx channels)	0	63	64
DMA	0 to 64	64 - (Number of Tx channels)	64	127	64

The format of a full channel allocation table entry is shown in Table 12-48. All reserved bits should be written to zero.

Table 12-48. Format Of Channel Allocation Table Entry

Channel Type	15	14	13	12	11	10 8	7 6	5 0
Isochronous	Reserved	FCE	Reserved	RNW	CE	CT[2-0] = 3	Reserved	CL[5-0]
Asynchronous	Reserved		MT	RNW	CE	CT[2-0] = 2	Reserved	CL[5-0]
Control	Reserved		MT	RNW	CE	CT[2-0] = 1	Reserved	CL[5-0]
Synchronous	Reserved	MFE	MT	RNW	CE	CT[2-0] = 0	Reserved	CL[5-0]

The field descriptions of a channel allocation table entry are shown in Table 12-49.

Table 12-49. Field Descriptions Of Channel Allocation Table Entry

Field	Description
CL[5-0]	Connection Label (offset into channel descriptor table)
CT[2-0]	Channel type
	111 = Reserved
	110 = Reserved
	101 = Reserved
	100 = Reserved
	011 = Isochronous
	010 = Asynchronous
	001 = Control
	000 = Synchronous
CE	Channel enable
	0 = Disabled
	1= Enabled
RNW	Read, not Write (1)
	1 = Read
	0 = Write
MT	Mute Bit (2)
	1= Enabled
	0 = Disabled
FCE	Flow control enable (3)
	1 = Enabled
	0 = Disabled
MFE	Multi-frame per sub-buffer enable (4)
	1 = Enabled
	0 = Disabled
Reserved	Reserved. Software writes zeros to all reserved bits when the entry is initialized. The reserved bits are read-only after initialization.

(1) For a Tx channel (from the host to the MediaLB interface):

- DMA channel allocation table entry: RNW = 0 (write)
- MediaLB channel allocation table entry: RNW = 1 (read)

For a Rx channel (data from MediaLB to host):

- DMA channel allocation table entry: RNW = 1 (read)
- MediaLB channel allocation table entry: RNW = 0 (write)

(2) When set for synchronous channels, the MT bit forces Rx channels to write zeros into the channel data buffer, and Tx channels to output zeros on the physical interface. When set for asynchronous and control channels, the MT bit causes DMA to halt at a packet boundary. Not valid for isochronous channels.

(3) The FCE bit is used by MediaLB isochronous Rx channels only.

(4) The MFE bit is used by MediaLB synchronous channels only.

12.1.4.3.1.4.1.1 Channel Setup

Data direction in the MLBSS is in reference to the DBR; therefore, the data direction of DMA entries corresponding to the same channel is reversed for the CAT DMA and the CAT MLB.

- For a Tx channel (from Device master to the MediaLB interface):
  - CAT DMA entry: RNW = 0 (write)
  - CAT MLB entry: RNW = 1 (read)
- Conversely, for a Rx channel (data from MediaLB to Device master):
  - CAT DMA entry: RNW = 1 (read)
  - CAT MLB entry: RNW = 0 (write)

Figure 12-48 illustrates the directional relationship in the MLBSS.

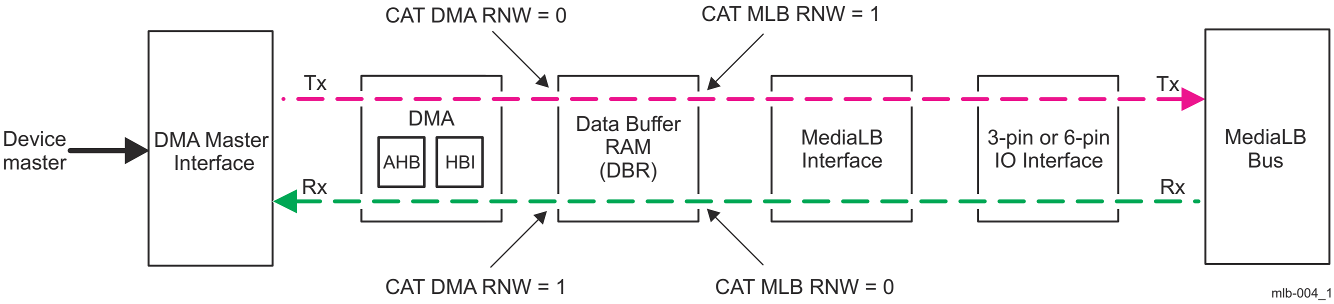


Figure 12-48. MLBSS DBR Directional Relationship

12.1.4.3.1.4.2 Channel Descriptor Table

The channel descriptor table comprises 64 channel table RAM entries. Each entry is 128-bit. The first entry starts at address 00h and the 64th entry at address 3Fh. Each 128-bit entry of the channel descriptor table is referenced by a connection label and contains information about data buffer in the data buffer RAM (that is, buffer size, or address pointers). The format of each channel descriptor table entry depends on the channel type (synchronous, isochronous, asynchronous, or control).

Software must write all reserved channel descriptor bits to ’0’ when the entry is initialized.

Synchronous Channel Descriptor Table

The MLBSS provides two modes of operation (standard and multi-frame per sub-buffer) to provide flexibility for implementing synchronous channels.

Channels set up for standard mode require less buffer space. For channels configured for standard mode, the host controller must transfer one full frame of streaming data in/out of the data buffer of each streaming channel.

Channels set up for multiple-frames per sub-buffer mode require more buffer space. For channels configured for multiple-frames per sub-buffer mode, the host controller must transfer N full frames of streaming data in/out of the data buffer of each streaming channel.

To set up a channel in multi-frame per sub-buffer mode:

- Program the MLB_MLBC0[17-15] FCNT bit field to select the number of frames per sub-buffer
- Program the channel allocation table to enable multi-frame sub-buffering (MFE = 1) for each particular channel
- Set the buffer depth (BD[11-0]) in the channel descriptor table
- Repeat for additional synchronous channels

A sample synchronous data buffer is shown in Figure 12-49. Each data buffer contains four sub-buffers and each sub-buffer contains space for 1 to 64 frames of data, determined by MLB_MLBC0[17-15] FCNT bit field.

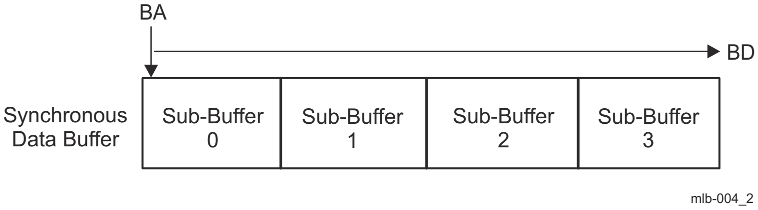


Figure 12-49. Synchronous Data Buffer Structure

The format of a synchronous channel descriptor table entry is shown in Table 12-50. All reserved bits should be written to zero.

Table 12-50. Format Of Synchronous Channel Descriptor Table Entry

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WSBC[1-0]		Reserved													
16	RSBC[1-0]		Reserved													
32	Reserved															
48	Reserved															
64	WSTS[3-0]				WPTR[11-0]											
80	RSTS[3-0]				RPTR[11-0]											
96	Reserved				BD[11-0]											
112	Reserved		BA[13-0]													

The field descriptions of a synchronous channel descriptor table entry are shown in Table 12-51.

Table 12-51. Field Descriptions Of Synchronous Channel Descriptor Table Entry

Field	Description	Details	Accessibility (1)
BA	Buffer base address	BA can start at any byte in the 16k data buffer RAM	r, w
BD	Buffer depth	1. BD = size of buffer in bytes - 1 2. Buffer end address = BA + BD 3. BD = 4 × m × bpf - 1, where: m = frames per sub-buffer (for MFE = 0, m = 1) bpf = bytes per frame	r, w
RPTR	Read pointer	1. Software initializes to zero, hardware updates 2. Counts the read address offset within a buffer 3. DMA read address = BA + RPTR	r, w, u
WPTR	Write pointer	1. Software initializes to zero, hardware updates 2. Counts the write address offset within a buffer 3. DMA write address = BA + WPTR	r, w, u
RSBC	Read sub-buffer counter	1. Software initializes to zero, hardware updates 2. Counts the read sub-buffer offset 3. DMA uses for pointer management	r, w, u
WSBC	Write sub-buffer counter	1. Software initializes to zero, hardware updates 2. Counts the write sub-buffer offset 3. DMA uses for pointer management	r, w, u

Table 12-51. Field Descriptions Of Synchronous Channel Descriptor Table Entry (continued)

Field	Description	Details	Accessibility [1]
RSTS	Read status	1. Software initializes to zero, hardware updates 2. RSTS states: (Only for DMA associated with MLBSS) xxx0 = normal operation (no mute) xxx1 = normal operation (mute) xx0x = idle	r, w, u
WSTS	Write status	1. Software initializes to zero, hardware updates 2. WSTS states: (Only for DMA associated with MLBSS) xxx0 = normal operation (no mute) xxx1 = normal operation (mute) xx0x = idle 1xxx = command protocol error	r, w, u
Reserved	Reserved	Software writes a zero to all Reserved bits when the entry is initialized. The Reserved bits are Read-only after initialization.	r, w, u

(1)
- r - software readable
- w - software writable
- u - updated periodically by hardware

Isochronous Channel Descriptor Table

The format of an isochronous channel descriptor table entry is shown in Table 12-52. All reserved bits should be written to zero.

Table 12-52. Format Of Isochronous Channel Descriptor Table Entry

<table>
<tr><th>Bit Offset</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td colspan="16">Reserved</td></tr>
<tr><td>16</td><td colspan="16">Reserved</td></tr>
<tr><td>32</td><td colspan="7">Reserved</td><td colspan="9">BS[8-0]</td></tr>
<tr><td>48</td><td colspan="16">Reserved</td></tr>
<tr><td>64</td><td colspan="3">WSTS[2-0]</td><td colspan="13">WPTR[12-0]</td></tr>
<tr><td>80</td><td colspan="3">RSTS[2-0]</td><td colspan="13">RPTR[12-0]</td></tr>
<tr><td>96</td><td colspan="3">Reserved</td><td colspan="13">BD[12-0]</td></tr>
<tr><td>112</td><td>BF</td><td>Reserved</td><td colspan="14">BA[13-0]</td></tr>
</table>

The field descriptions of an isochronous channel descriptor table entry are shown in Table 12-53.

Table 12-53. Field Descriptions Of Isochronous Channel Descriptor Table Entry

Field	Description	Details	Accessibility [1]
BA	Buffer Base Address	BA can start at any byte in the 16k data buffer RAM	r, w
BD	Buffer Depth	1. BD = size of buffer in bytes - 1 2. Buffer end address = BA + BD 3. Isochronous buffers must be large enough to hold at least 3 blocks (packets) of data 4. Buffer depth must be a integer multiple of blocks	r, w

Table 12-53. Field Descriptions Of Isochronous Channel Descriptor Table Entry (continued)

Field	Description	Details	Accessibility (1)
BF	Buffer Full	1. Software initializes to zero, hardware updates 2. DMA write hardware sets BF when the buffer is full 3. DMA read hardware clears BF when the buffer is empty 4. BF is valid only when the buffer is full or empty, otherwise ignore	r, w, u
BS	Block Size	1. BS defines when to begin the DMA to the data buffer 2. BS = buffer block size in bytes - 1 3. For Rx channels, the DMA writes start when the number of empty bytes (SPACE) in the data buffer >= the block size 4. For Tx channels, the DMA reads start when the number of valid bytes (VALID) in the data buffer >= the block size	r, w, u
RPTR	Read Pointer	1. Software initializes to zero, hardware updates 2. Counts the read address offset within a buffer 3. DMA read address = BA + RPTR	r, w, u
WPTR	Write Pointer	1. Software initializes to zero, hardware updates 2. Counts the write address offset within a buffer 3. DMA write address = BA + WPTR	r, w, u
RSTS	Read status	1. Software initializes to zero, hardware updates 2. RSTS Status states (Only for DMA associated with MLBSS) xx1 = active xx0 = idle	r, w, u
WSTS	Write status	1. Software initializes to zero, hardware updates 2. WSTS states: (Only for DMA associated with MLBSS) xx1 = active xx= idle x1x = command protocol error 1xx = buffer overflow (FCE = 0 only)	r, w, u
Reserved	Reserved	Software writes a zero to all reserved bits when the entry is initialized. The reserved bits are read-only after initialization.	r, w, u

(1)
- r - software readable
- w - software writable
- u - updated periodically by hardware

Asynchronous and Control Channel Description Table

The format of an asynchronous and control channel descriptor table entry is shown in Table 12-54. All reserved bits should be written to zero.

Table 12-54. Format Of Asynchronous and Control Channel Descriptor Table Entry

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WPC[4-0]					Reserved										
16	RPC[4-0]					Reserved										
32	Reserved	WPC[7-5]			Reserved											

Table 12-54. Format Of Asynchronous and Control Channel Descriptor Table Entry (continued)

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
48	Reserved	RPC[7-5]			Reserved											
64	WSTS[3-0]				WPTR[11-0]											
80	RSTS[3-0]				RPTR[11-0]											
96	RSTS[4]	WSTS[4]	Reserved		BD[11-0]											
112	Reserved		BA[13-0]													

The field descriptions of an asynchronous and control channel descriptor table entry are shown in Table 12-55.

Table 12-55. Field Descriptions Of Asynchronous And Control Channel Descriptor Table Entry

Field	Description	Details	Accessibility [2]
BA	Buffer Base Address	BA can start at any byte in the 16k data buffer RAM	r, w
BD	Buffer Depth	1. BD = size of buffer in bytes - 1 2. Buffer end address = BA + BD 3. BD >= max packet length - 1	r, w
RPC	Read Packet Count	1. Software initializes to zero, hardware updates 2. Used in conjunction with WPC, RPTR and WPTR to determine if the buffer is empty or full	r, w, u
WPC	Write Packet Count	1. Software initializes to zero, hardware updates 2. Used in conjunction with RPC, RPTR and WPTR to determine if the buffer is empty or full	r, w, u
RPTR	Read Pointer	1. Software initializes to zero, hardware updates 2. Counts the read address offset within a buffer 3. DMA read address = BA + RPTR	r, w, u
WPTR	Write Pointer	1. Software initializes to zero, hardware updates 2. Counts the write address offset within a buffer 3. DMA write address = BA + WPTR	r, w, u
RSTS	Read status	1. Software initializes to zero, hardware updates 2. Status states:[1] x0x00 = idle xx1xx = ReceiverProtocolError response received from Rx device 1xxxx = ReceiverBreak response received from Rx device	r, w, u
WSTS	Write status	1. Software initializes to zero, hardware updates 2. Status states:[1] x0x00 = idle xx1xx = command protocol error detected 1xxxx = AsyncBreak/ControlBreak command received from Tx device	r, w, u
Reserved	Reserved	Software writes a zero to all reserved bits when the entry is initialized. The Reserved bits are read-only after initialization.	r, w, u

(1) Only valid for DMA pointers associated with the MediaLB core. Not valid for DMA block related pointers.

(2)
- r - software readable
- w - software writable
- u - updated periodically by hardware

12.1.4.3.1.5 DMA Block

The DMA block manages data exchange between the local channel data buffers which reside in the MLBSS and a memory buffer residing in the system memory. To support system memory buffering, a ping-pong memory structure is implemented on a per channel basis using 128-bit descriptors for DMA descriptor table entries. 64 DMA descriptor table entries are directly mapped to the 64 DMA physical channels.

Each logical channel is assigned a separate 128-bit descriptor, defining data buffers in the system memory which are used by the DMA interface for this logical channel. The descriptors are stored at fixed addresses in the channel table RAM.

The description of the DMA descriptor table fields is shown in Table 12-56.

Table 12-56. Field Descriptions Of DMA Descriptor Table

Field	Numbers of bits	Description	Accessibilty (1)
CE	1	Channel enable: 0 = Disabled 1 = Enabled	r, w, u
LE	1	Endianess Enable: 0 = Big endian 1 = Little Endian	r, w
PG	1	Page pointer. Software initializes to zero, hardware writes thereafter. 0 = Ping buffer 1 = Pong buffer	r, w, u
RDY1	1	Buffer ready bit for ping buffer page: 0 = Not ready 1 = Ready	r, w
RDY2	1	Buffer ready bit for pong buffer page: 0 = Not ready 1 = Ready	r, w
DNE1	1	Buffer done bit for ping buffer page: 0 = Not done 1 = Done	r, u, c0
DNE2	1	Buffer done bit for pong buffer page: 0 = Not done 1 = Done	r, u, c0
ERR1	1	DMA error response detected for ping buffer page: 0 = No error 1 = Error	r, u, c0
ERR2	1	DMA error response detected for pong buffer page: 0 = No error 1 = Error	r, u, c0
PS1	1	Packet start bit for ping buffer page: 0 = No packet start 1 = Packet start Reserved for synchronous and isochronous channels.	r, w, u (both Tx and Rx)
PS2	1	Packet start bit for pong buffer page: 0 = No packet start 1 = Packet start Reserved for synchronous and isochronous channels.	r, w, u (both Tx and Rx)

Table 12-56. Field Descriptions Of DMA Descriptor Table (continued)

Field	Numbers of bits	Description	Accessibilty (1)
MEP1	1	Most ethernet packet (MEP) indicator for ping buffer page: 0 = No MEP 1 = MEP MEP1 only valid for the first page of a segmented buffer. Reserved for control, synchronous and isochronous channels	r, w, u (both Tx and Rx)
MEP2	1	Most ethernet packet (MEP) indicator for pong buffer page: 0 = No MEP 1 = MEP MEP2 only valid for the first page of a segmented buffer. Reserved for control, synchronous and isochronous channels	r, w, u (both Tx and Rx)
BD1(2)	11 to 13	Buffer depth for ping buffer page: 11 or 12-bits for asynchronous and control channels. 13-bits for synchronous and isochronous channels.	r, w
BD2(2)	11 to 13	Buffer depth for pong buffer page: 11 or 12-bits for asynchronous and control channels. 13-bits for synchronous and isochronous channels.	r, w
BA1	32	Buffer base address for ping buffer page	r, w
BA2	32	Buffer base address for pong buffer page	r, w
Reserved	varies	Software writes a zero to all Reserved bits when the entry is initialized. The Reserved bits are Read-only after initialization.	r, w, u

(1)
- r - software readable
- w - software writable
- u - updated periodically by hardware
- c0 - software writes '0' to clear

(2) The buffer depth (BD1 and BD2) for synchronous channels must consider if multi-frame per sub-buffer mode (the MFE bit in the Channel Allocation Table) is enabled.

Data exchange across the DMA interface can be configured as little endian (LE = 1h) or big endian (LE = 0h). Figure 12-50 provides an overview of the endian options, chosen by the LE bit.

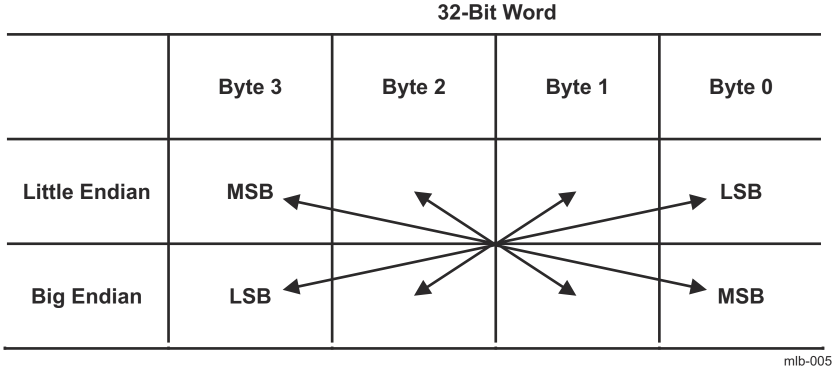


Figure 12-50. DMA Descriptor Table Endian Options

Figure 12-51 shows an example of ping-pong system memory structure. This system memory structure is similar for all channel types and shows the relationship between the BA1, BA2, BD1, BD2 and PG descriptor fields.

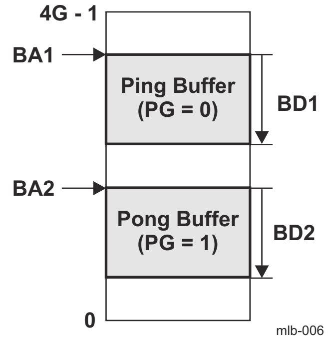


Figure 12-51. Ping-Pong System Memory Structure

Each DMA descriptor table entry (also referred to as a channel descriptor) holds a 32-bit BAn (n = 1 and 2) field which defines the start of each ping or pong buffer within system memory. The BDi (i = 1 and 2) field is used to indicate the size for the respective ping or pong page. The maximum size is 2k-entries for asynchronous and control channels, and 8k-entries for isochronous and synchronous channels.

12.1.4.3.1.5.1 Synchronous Channel Descriptor

The synchronous buffering scheme allows each ping or pong buffer to contain a single frame or a multiple number of frames. For this reason, the synchronous buffer depth (BDi) must be defined in terms of an integer number (n), frames per sub-buffer (m) and bytes per frame (bpf) of data (that is, BDi = n × m × bpf - 1).

Table 12-57 shows the format for a synchronous DMA descriptor table entry. For more details about the field descriptions see Table 12-56. Each synchronous channel buffer can be up to 8k-bytes deep.

Note

In synchronous transmit mode software should take care that the pong DDT is configured before ping DMA completion and ping DDT is configured before pong DMA completion. For more information about ping and pong DMA configuration see Table 12-68 and Table 12-69, respectively.

Table 12-57. Format Of Synchronous DMA Descriptor Table Entry

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CE	LE	PG	Reserved												
16	Reserved															
32	RDY1	DNE1	ERR1	BD1[12-0]												
48	RDY2	DNE2	ERR2	BD2[12-0]												
64	BA1[15-0]															
80	BA1[31-16]															
96	BA2[15-0]															
112	BA2[31-16]															

12.1.4.3.1.5.2 Isochronous Channel Descriptors

The isochronous buffering scheme allows each ping or pong buffer to contain a single block or a multiple number of blocks. For this reason, the isochronous buffer depth (BDi) must be defined in terms of an integer number (n) and block size (BS) (that is, BDi = n × (BS + 1) - 1).

Table 12-58 shows the format for an isochronous DMA descriptor table entry. For more details about the field descriptions see Table 12-56. Each isochronous channel buffer can be up to 8k-bytes deep.

Table 12-58. Format Of Isochronous DMA Descriptor Table Entry

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CE	LE	PG	Reserved												

Table 12-58. Format Of Isochronous DMA Descriptor Table Entry (continued)

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16	Reserved															
32	RDY1	DNE1	ERR1	BD1[12-0]												
48	RDY2	DNE2	ERR2	BD2[12-0]												
64	BA1[15-0]															
80	BA1[31-16]															
96	BA2[15-0]															
112	BA2[31-16]															

12.1.4.3.1.5.3 Asynchronous and Control Channel Descriptors

Every asynchronous and control designates the first two bytes of each packet as the packet length. Each packet must be no more than 2048 bytes (packet length ≤ 2048).

Software must set the buffer ready bit (RDYn) for each buffer as it programs the DMA. As hardware processes each buffer, it sets the done bit (DNEn) and generates an interrupt. When hardware finishes the buffer processing, it can begin processing another buffer if RDYn is set. The application is responsible for setting up and configuring the channel buffer descriptor prior to every DMA access on the channel.

Two-packet modes are supported by hardware for programming the DMA. These are single-packet mode and multiple-packet mode.

12.1.4.3.1.5.3.1 Single-Packet Mode

The single-packet mode asynchronous and control buffering scheme supports a maximum of one packet per buffer (that is, ping or pong). Both non-segmented and segmented data packets are allowed while using single-packet mode. Non-segmented packets are exchanged when only one buffer (that is ping or pong) is needed for packet transfer. Segmented packets are exchanged when a single packet is too long for one buffer and the packet must span multiple buffers. Figure 12-52 shows the memory space usage for both non-segmented and segmented asynchronous or control packets along with the packet start bit (PSn).

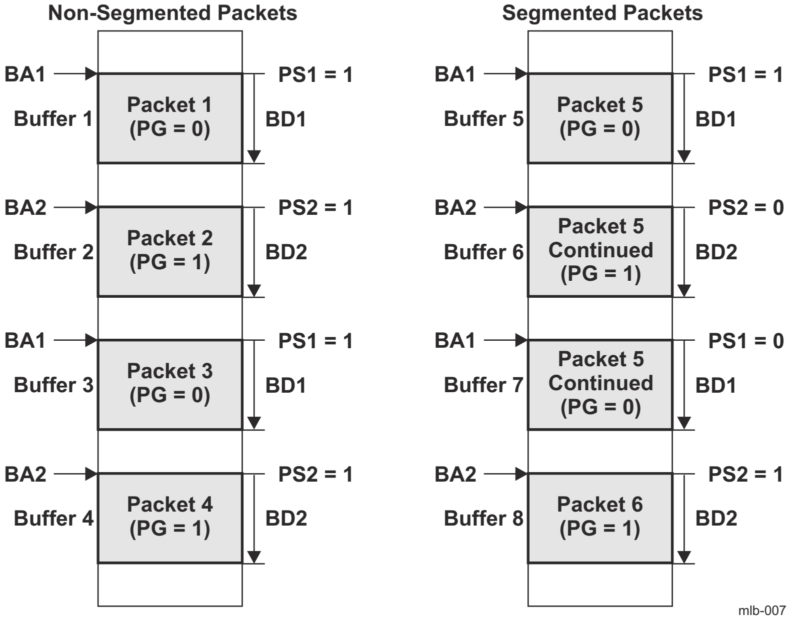


Figure 12-52. Single-Packet Mode Memory Space

While using single-packet mode, buffer done (DNEn) is set in hardware when a packet is done or the buffer is full.

Table 12-59 shows the format for single-packet mode asynchronous and control DMA descriptor table entries. For more details about the field descriptions see Table 12-56.

Table 12-59. Format Of Single-Packet Asynchronous and Control DMA Descriptor Table Entry

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CE	LE	PG	Reserved												
16	Reserved															
32	RDY1	DNE1	ERR1	PS1	MEP1	BD1[10-0]										
48	RDY2	DNE2	ERR2	PS2	MEP2	BD2[10-0]										
64	BA1[15-0]															
80	BA1[31-16]															
96	BA2[15-0]															
112	BA2[31-16]															

12.1.4.3.1.5.3.2 Multiple-Packet Mode

The multiple-packet mode asynchronous and control buffering scheme supports more than one packet per system memory buffer, as shown in Figure 12-53. The multiple-packet mode reduces the interrupt rate for packet channels at the cost of increasing buffering and latency.

For Tx packet channels in multiple-packet mode, software sets the packet start bit (PSn) for every buffer. Setting PSn informs hardware that the first two bytes of the buffer contains the port message length (PML) of the first packet. After the first packet, hardware keeps track of where packets start and end within the current buffer. Software should not write to PSn while the buffer is active (RDYn = 1 and DNEn = 0). For Tx packet channels, the buffer is done (DNEn = 1) when the last byte of the last packet in the buffer is read from system memory. Software should set the buffer depth to contain the exact number of complete packets for that buffer. Segmented buffers are not supported for Tx packet channels in multiple-packet mode.

For Rx packet channels in multiple-packet mode, PSn has no meaning and should be ignored. Software is responsible for keeping track of where each packet starts and ends within the multiple-packet buffer via the packet PML. The buffer done bit (DNEn) is set in hardware for Rx channels when a buffer is full (see Buffer 1 in Figure 12-53) or if a packet ends exactly 1-byte before the end of the buffer (see Buffer 2 in Figure 12-53). Multiple-packet mode also supports segmented Rx packets spanning two or more buffers (see Buffers 3 – 6 in Figure 12-53).

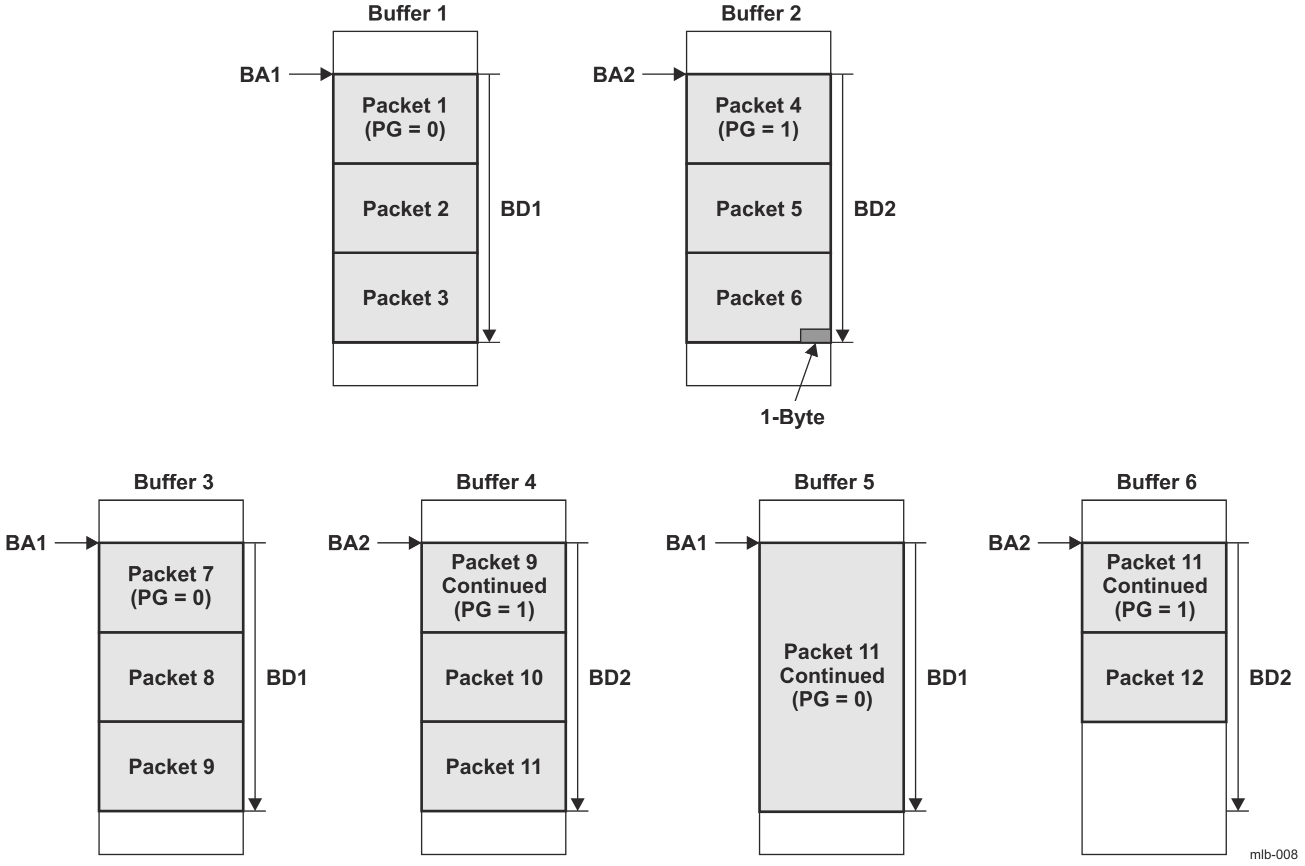


Figure 12-53. Multi-Packet Mode System Memory

Table 12-60. Format Of Multiple-Packet Asynchronous And Control DMA Descriptor Table Entry

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CE	LE	PG	Reserved												
16	Reserved															
32	RDY1	DNE1	ERR1	PS1 (1)	BD1[11-0]											
48	RDY2	DNE2	ERR2	PS2 (1)	BD2[11-0]											
64	BA1[15-0]															
80	BA1[31-16]															
96	BA2[15-0]															
112	BA2[31-16]															

(1) PS1 and PS2 have no meaning and should be ignored in Rx mode.

12.1.4.3.2 MLBSS Software and Data Flow

Figure 12-54 shows an overview of the MLBSS software and data flow when transmitting.

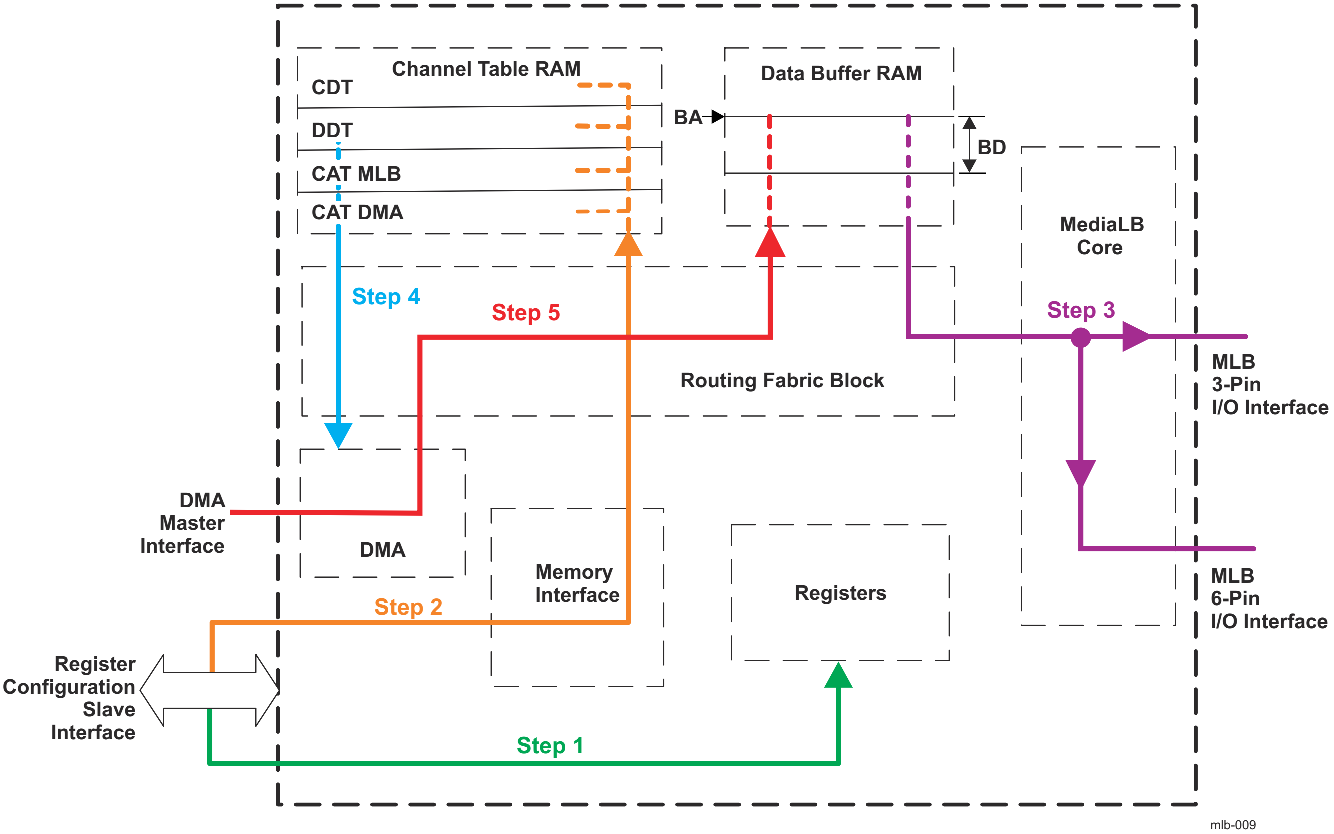


Figure 12-54. MLBSS Software and Data Tx Flow Overview

The MLBSS data Tx flow is defined in the following way:

1. Hardware is configured (see Table 12-62).
2. Channel table RAM is cleared and configured (see Table 12-63).
3. Data Tx begins through MediaLB 3-pin or 6-pin interface after MLBSS is synchronized to the incoming MLB framesync.
4. DMA reads from channel table RAM.
5. Data Tx is done through the DMA master interface.

Figure 12-55 shows an overview of the MLBSS software and data flow when receiving.

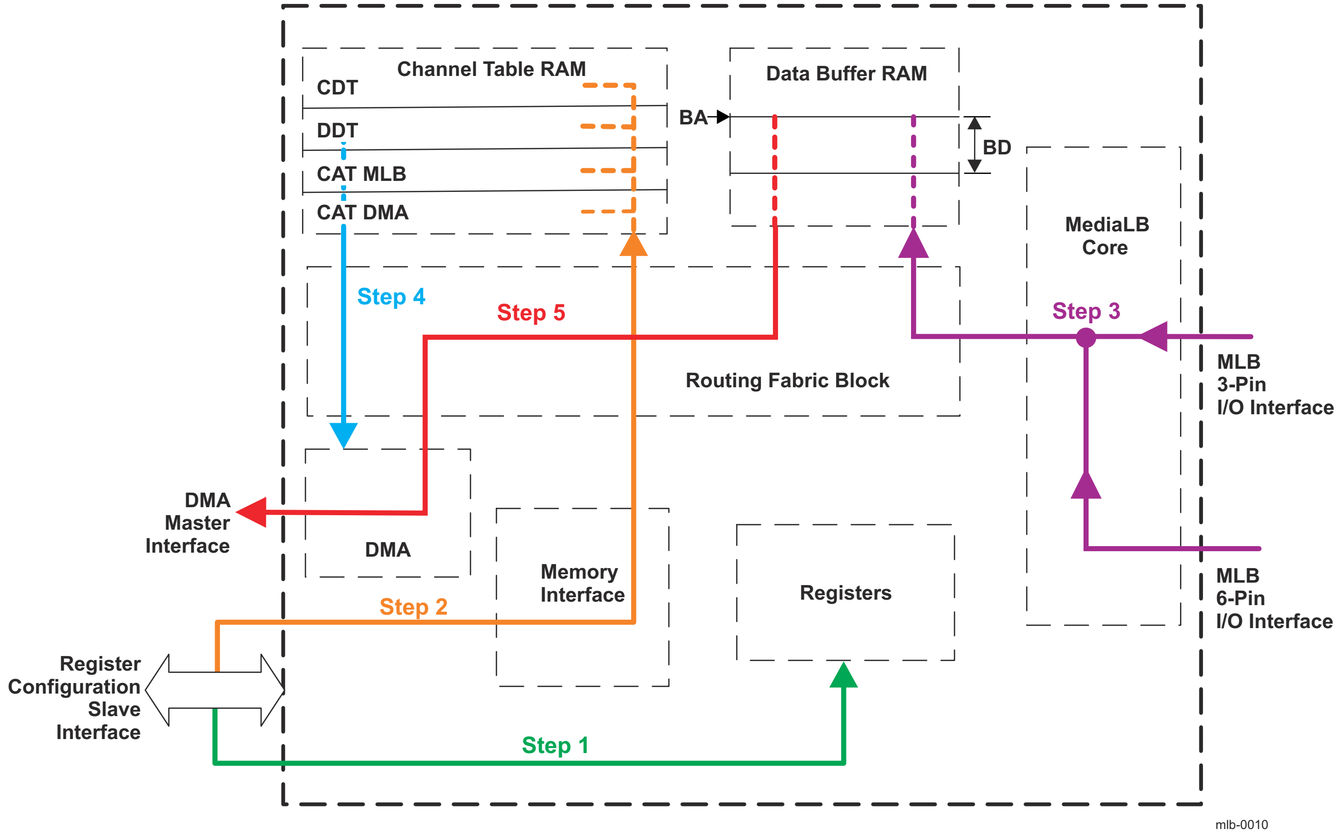


Figure 12-55. MLBSS Software and Data Rx Flow Overview

The MLBSS data Rx flow is defined in the following way:

1. Hardware is configured (see Table 12-62).
2. Channel table RAM is cleared and configured (see Table 12-63).
3. Data Rx begins through MediaLB 3-pin or 6-pin interface after MLBSS is synchronized to the incoming MLB framesync.
4. DMA reads from channel table RAM.
5. Data Rx is done through the DMA master interface.

Steps 1 and 2 from Figure 12-54 and Figure 12-55 are done by software. For more information see Section 12.1.4.4.1.1.1, *Channel Initialization*.

Steps 3-5 from Figure 12-54 and Figure 12-55 are handled by MLBSS internal hardware.

The top-level software tasks that the application must perform, can be placed in two categories:

- Channel initialization
- Channel servicing

For more information about channel initialization, see Section 12.1.4.4.1.1.1, *Channel Initialization*.

For more information about channel servicing, see Section 12.1.4.4.2.1, *Channel Servicing*.

12.1.4.3.2.1 Data Flow For Receive Channels

The data flow for receive channels is as follows:

1. After MLBSS is configured (see Section 12.1.4.4.1.1.1) and MediaLB has synchronized to the incoming MediaLB framesync (MLB_MLBC0[7] MLBLK = 1h) MLB_MLBC0, serial data is received either through the MLB0_MLBDP and MLB0_MLBDN pads or through the MLB0_MLBDAT pad, depending on the pin mode (6-pin or 3-pin) selected.
2. The MLBSS logic writes incoming data to the appropriate buffer in the data buffer RAM. The data buffer RAM address to which data is written is the BA field of the channel descriptor table entry. The channel

descriptor table entry is specified by the CL field of the MediaLB channel allocation table entry for the channel. The MediaLB channel allocation table entry equals (1/2)*ChannelAddr.

3. The DMA access for a particular DMA channel (DMA channel allocation table entry) is started when there is sufficient data for the DMA channel in the data buffer RAM to write into system memory and the system memory buffer (ping or pong depending on the PG bit in DMA descriptor table entry) is marked as ready. Note that presence of a frame for synchronous/isochronous traffic (multiple frames in multi frame mode) or a packet for control/asynchronous traffic (multiple packets in multi packet mode) is deemed sufficient data to mark a DMA channel as ready.
4. The DMA hardware reads from the data buffer RAM memory address specified by the BA field of the channel descriptor table entry and writes to the system memory address specified in the DMA descriptor table. The CL field in the DMA channel allocation table entry is used to determine the appropriate channel descriptor table entry. Note that CL field of DMA channel allocation table and MLBSS channel allocation table entries must be the same, thus providing the common data buffer RAM address for MLBSS core to write into DMA and the DMA to read from the MLBSS core. Further, each DMA channel allocation table entry corresponds to a DMA descriptor table entry as per the following mapping:
   - Address of DMA descriptor table entry = 40h + Index of DMA channel allocation table entry.

12.1.4.3.2.2 Data Flow for Transmit Channels

The data flow for transmit channels is as follows:

1. The DMA access for a particular DMA channel (DMA channel allocation table entry) is started when data buffer RAM has sufficient buffer space and the system memory buffer (ping or pong depending on the PG bit in DMA descriptor table entry) is marked as ready for a particular DMA channel allocation table entry. Each DMA channel allocation table entry corresponds to a DMA descriptor table entry as per the following mapping:
   - Address of DMA descriptor table entry = 40h + Index of DMA channel allocation table entry.
2. The DMA reads from the system memory address specified in the DMA descriptor table and writes to the data buffer RAM memory address specified by the BA field of the channel descriptor table entry. The CL field in the DMA channel allocation table entry is used to determine the appropriate channel descriptor table entry. Note that CL field of DMA channel allocation table and MLBSS channel allocation table entries must be the same, thus providing the common data buffer RAM address for DMA to write into MLBSS core and the MLBSS core to read from the DMA.
3. Once the MLBSS is synchronized to the incoming MediaLB framesync (MLB_MLBC0[7] MLBLK = 1h) MLB_MLBC0 and a MediaLB channel address is received, the MediaLB core refers to the specific MediaLB channel allocation table entry and reads data from the data buffer RAM buffer. The data buffer RAM address from which data is read is the BA field of the channel descriptor table entry. The channel descriptor table entry is specified by the CL field of the MLBSS channel allocation table entry for the channel. The MediaLB channel allocation table entry equals (1/2)*ChannelAddr.
4. This data is serialized and transmitted through the MediaLB 3-pin or 6-pin interface.

12.1.4.3.3 MLBSS Priority On The System Interconnect

There is a register used for controlling the priority of the MLBSS on the system interconnect. This is done through the MLBSS_DMA_CTRL MLBSS_DMA_CTRL[2-0] PRIORITY bit field. Setting this bit field to 0h means that the MLBSS traffic has highest priority over the other initiator traffics. A value of 7h is for lowest priority.

12.1.4.4 MLBSS Programming Guide

This section describes the programming sequences for the configuration and use of the MLBSS.

12.1.4.4.1 Global Initialization

12.1.4.4.1.1 MLBSS Global Initialization

12.1.4.4.1.1.1 Channel Initialization

A channel initialization must be performed in order to ensure proper operation. Table 12-61 shows the sequence.

Table 12-61. Channel Initialization Steps

Step	Crossreference
Configuring the hardware	Table 12-62
Programming the routing fabric block	Table 12-63
Programming the DMA block	Table 12-67
Synchronizing and unmuting the synchronous channel	Table 12-70

Configuring The Hardware

To configure the MediaLB interface, the steps shown in Table 12-62 should be followed.

Table 12-62. Configuring The Hardware

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Clear channel table RAM, to ensure that no stray interrupts are generated	-	0h
Clear the interrupt status bits for logical channels 0 to 63	MLB_ACSR0 and MLB_ACSR1	FFFF FFFFh
Mask all interrupts for DMA channels (from 0 to 63)	MLB_ACMR0 and MLB_ACMR1	0000 0000h
Select 3-pin or 6-pin MediaLB operation	MLB_MLBC0[5] MLBPEN	0h for 3-pin 1h for 6-pin
Select MediaLB clock speed	MLB_MLBC0[4-2] MLBCLK	-h
Enable the MediaLB	MLB_MLBC0[0] MLBEN	1h
Activate (unmask) all channels	MLB_HCMR0 and MLB_HCMR1	FFFF FFFFh
Enable the HBI block	MLB_HCTL[15] EN	1h
Set the DMA channel mask bits according to all active DMA channels	MLB_HCMR0 and MLB_HCMR1	-h
Select DMA Mode 1 to be used	MLB_ACTL[2] DMA_MODE	1h
Select software to clear the interrupts	MLB_ACTL[0] SCE	1h
Enable MLBSS interrupts, if required	MLB_MIEN	-h

Programming The Routing Fabric Block

The channel allocation table and channel descriptor table reside in the channel table RAM and are programmed indirectly through the memory interface block. The steps to be followed are shown in Table 12-63.

Table 12-63. Programming The Routing Fabric Block

Step	Register/ Bit Field/ Programming Model/ Comments	Value
1. Initialize all bits of the channel allocation table	-	0h
2. Select a connection label	CL	N = 0h to 3Fh
3. Program the channel descriptor table for channel N	Use the memory interface registers to do a write to the channel descriptor table. See Table 12-64.	Mask to be used: FFFF FFFFh
4. Program the channel allocation table for inbound data buffer RAM access	Write to the data buffer RAM. See Table 12-65.	-

Table 12-63. Programming The Routing Fabric Block (continued)

Step	Register/ Bit Field/ Programming Model/ Comments	Value
5. Program the channel allocation table for outbound data buffer RAM access	Read from the data buffer RAM. See Table 12-66.	-
6. Repeat steps 2-5 to initialize all logical channels	-	-

Table 12-64. Subsequence - Program The Channel Descriptor Table

Step	Register/ Bit Field/ Programming Model/ Comments	Value
1. Set the 14-bit base address	BA	-h
2. Set the 12-bit or 13-bit buffer depth	BD (set this according to the BA so that it doesn't overflow the buffer)	BD = buffer depth in bytes - 1
IF: Synchronous channels		
Set the 12-bit or 13-bit buffer depth	BD	(BD + 1) = 4 × frames per sub-buffer (m) × bytes per frame (bpf)
ENDIF		
IF: Isochronous channels		
Set the 12-bit or 13-bit buffer depth	BD	(BD + 1) mod (BS + 1) = 0
ENDIF		
IF: Asynchronous channels		
Set the 12-bit or 13-bit buffer depth	BD	(BD + 1) >= max packet length (1024 for a MOST Data Packet (MDP))
ENDIF		
IF: Control channels		
Set the 12-bit or 13-bit buffer depth	BD	(BD + 1) >= max packet length (64)
ENDIF		
3. For isochronous channels, configure the block size	BS	BS = block size in bytes - 1
4. Write to all other bits of the channel descriptor table		0h

Table 12-65. Subsequence - Write To The Data Buffer RAM

Step	Register/ Bit Field/ Programming Model/ Comments	Value
For Tx channels the DMA block does the inbound data buffer RAM access	A Tx channel is from MLBSS to external host	-
For Rx channels MediaLB does the inbound data buffer RAM access	An Rx channel is from external host to MLBSS	-
Set the channel direction	RNW	0h
Set the channel type	CT[2-0]	0h: synchronous 1h: control 2h: asynchronous 3h: isochronous
Set the connection label	CL[5-0]	CL[5-0] = N
IF: CT[2-0] = 0h (synchronous)		
Set the mute bit.	MT (the mute bit is set to avoid any flow of the garbage data that will be there in the data buffer prior to any transfer)	1h
ENDIF		
Set the channel enable bit	CE	1h
Clear all other bits of the channel allocation table	-	0h

Table 12-66. Subsequence - Read From The Data Buffer RAM

Step	Register/ Bit Field/ Programming Model/ Comments	Value
For Tx channels MediaLB does the outbound data buffer RAM access	A Tx channel is from MLBSS to external host	-
For Rx channels the DMA block does the outbound data buffer RAM access	An Rx channel is from external host to MLBSS	-
Set the channel direction	RNW	1h
Set the channel type	CT[2-0]	0h: synchronous 1h: control 2h: asynchronous 3h: isochronous
Set the connection label	CL[5-0]	CL[5-0] = N
IF: CT[2-0] = 000 (synchronous),		
Set the mute bit.	MT	1h
ENDIF		
Set the channel enable bit	CE	1h
Clear all other bits of the channel allocation table	-	0h

Programming The DMA Block

The DMA descriptor table resides in the channel table RAM and is programmed through TeraNet_CFG slave interface using the registers of the memory interface block. The steps to be followed are shown in Table 12-67.

Table 12-67. Programming The DMA Block

Step (1)	Register/ Bit Field/ Programming Model/ Comments	Value
1. Initialize all bits of the DMA descriptor table	-	0h
2. Select a connection label	CL (Note that the CL number chosen in this step should be equal to the CL number chosen in step 2 of Table 12-63)	N = 0h to 3Fh
3. Program the DMA block ping page for channel N (2)	See Table 12-68	-
4. Program the DMA block pong page for channel N	See Table 12-69	-
5. Select big or little endian	LE	-h
6. Select the active page	PG (Program this bit only once in the beginning of the configuration. It shouldn't be touched by the software after that. The hardware updates this bit as the transactions happen)	-h
7. Set the channel enable bit for all active logical channels	CE	1h
8. Repeat steps 2-7 for all active logical channels	-	-

(1) **Tip:** In order to program the MLBSS and DMA channel allocation table entries with respect to corresponding MLBSS and DMA channel address, the following steps are recommended:

- Given the MLBSS channel address is X (1-63), the MLBSS channel allocation table entry to be programmed should be X/2.
- Given the DMA channel address is X (0-63), the DMA channel allocation table entry to be programmed is X.

(2) For programming the 128-bit DMA descriptor table entry,

- IF: The DMA descriptor table is initialized with zeros and the PG bit is intended to be set to 0h, the following mask should only be used: MLB_MDWE0 = 000C 0000h
- ELSE: The following steps should be performed:
  - The mask to be used: = 000E 0000h.
  - Program the DMA descriptor table and the PG bit.

- Change the MLB_MDWE0 mask value to 000C 0000h after the first configuration has been done to prevent any further writes by host to the PG bit during ongoing MLBSS transactions.
- Write the FFFF FFFFh mask to the MLB_MDWE1, MLB_MDWE2 and MLB_MDWE3 registers

Table 12-68. Subsequence - Program The DMA Block Ping Page

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Set the 32-bit base address	BA1	-h
Set the 11-bit buffer depth	BD1	BD1 = buffer depth in bytes - 1
IF: Synchronous channels		
Set the 11-bit buffer depth	BD1	(BD1+ 1) = n × frames per sub-buffer (m) × bytes-per-frame (bpf)
ENDIF		
IF: Isochronous channels		
Set the 11-bit buffer depth	BD1	(BD1 + 1) mod (BS + 1) = 0
ENDIF		
IF: Asynchronous and control Rx channels		
Set the 11-bit buffer depth	BD1	5 <= (BD1 + 1) <= 4096 (1)
ENDIF		
IF: Asynchronous and control Tx channels		
Set the 11-bit buffer depth	BD1	5 <= (BD1 + 1) <= 4096 (1)
Set the packet start bit if the page contains the start of the packet	PS1	1h
ENDIF		
Clear the page done bit	DNE1	0h
Clear the error bit	ERR1	0h
Set the page ready bit	RDY1	1h

(1) 4096 is the max packet length.

Table 12-69. Subsequence - Program The DMA Block Pong Page

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Set the 32-bit base address	BA2	-h
Set the 11-bit buffer depth	BD2	BD2 = buffer depth in bytes - 1
IF: Synchronous channels		
Set the 11-bit buffer depth	BD2	(BD2+ 1) = n × frames per sub-buffer (m) × bytes-per-frame (bpf)
ENDIF		
IF: Isochronous channels		
Set the 11-bit buffer depth	BD2	(BD2 + 1) mod (BS + 1) = 0
ENDIF		
IF: Asynchronous and control Rx channels		
Set the 11-bit buffer depth	BD2	5 <= (BD2 + 1) <= 4096 (1)
ENDIF		
IF: Asynchronous and control Tx channels		
Set the 11-bit buffer depth	BD2	5 <= (BD2 + 1) <= 4096 (1)
Set the packet start bit if the page contains the start of the packet	PS2	1h
ENDIF		
Clear the page done bit	DNE2	0h
Clear the error bit	ERR2	0h

Table 12-69. Subsequence - Program The DMA Block Pong Page (continued)

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Set the page ready	RDY2	1h

(1) 4096 is the max packet length.

Synchronizing And Unmuting The Synchronous Channel

The steps to be followed are shown in Table 12-70

Table 12-70. Synchronizing And Unmuting The Synchronous Channel

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Check that MediaLB clock is running	MLB_MLBC1[7] CLKMERR	0h
IF: The MediaLB clock is not toggling at the pads	MLB_MLBC1[7] CLKMERR	1h
Clear the register bit	MLB_MLBC1[7] CLKMERR	
Wait one MLBSS_PCLK or MLBSS I/O clock cycle		
Check that MediaLB clock is running	MLB_MLBC1[7] CLKMERR	0h
ENDIF		
Poll for MediaLB lock	MLB_MLBC0[7] MLBLK	1h
Wait four frames	-	-
Unmute the synchronous channel/ channels	MT	0h

12.1.4.4.2 MLBSS Operational Modes Configuration

12.1.4.4.2.1 Channel Servicing

After initialization, each channel requires periodic servicing. Table 12-71 shows the steps which can be performed concurrently and in any order.

Table 12-71. Channel Servicing Steps

Step	Crossreference
Servicing the DMA Interrupts	Table 12-72
Servicing MLBSS Interrupts	Table 12-74
Polling for MediaLB System Commands	Table 12-75

Servicing the DMA Interrupts

The steps to be followed are shown in Table 12-72

Table 12-72. Servicing the DMA Interrupts

Step	Register/ Bit Field/ Programming Model/ Comments	Value
1. Enable (unmask) the interrupts from all active DMA channels	MLB_ACMR0 and MLB_ACMR1	1h for each bit associated with an active DMA channel
2. Select the status clear method	MLB_ACTL[0] SCE	-h
3. Select one (MLB0_MLBSS_MLB_AHB_INT_0 only) or two (MLB0_MLBSS_MLB_AHB_INT_0 and MLB0_MLBSS_MLB_AHB_INT_1) interrupt signals	MLB_ACTL[1] SMX	-h
4. Wait for an interrupt from MLB0_MLBSS_MLB_AHB_INT_0 and/or MLB0_MLBSS_MLB_AHB_INT_1 line	-	-
5. Determine which channel or channels are causing an interrupt	Read the MLB_ACSR0 and MLB_ACSR1 registers	-h

Table 12-72. Servicing the DMA Interrupts (continued)

Step	Register/ Bit Field/ Programming Model/ Comments	Value
6. IF: MLB_ACTL[0] SCE = 1h (software clears the interrupts)		
Write the results of step 5 back to the MLB_ACSR0 and MLB_ACSR1 registers to clear the interrupt	MLB_ACSR0 and MLB_ACSR1	MLB_ACSR0 and MLB_ACSR1
ENDIF		
7. Select a logical channel (N = 0-63) with an interrupt to service	-	-
8. Read the DMA descriptor table entry for channel N	See Table 12-73	-
9. Reprogram the expired or broken DMA page/pages via steps 3 and 4 of Table 12-67	-	-
10. Repeat steps 6-9 for all channels with pending interrupts	-	-
11. Repeat steps 4-10 while there are active channels	-	-

Note

The MLB_ACSR0, MLB_ACSR1, MLB_ACMR0 and MLB_ACMR1 register bits correspond to the DMA channel address for a particular logical channel. This should not be confused with the MLB channel address.

Channels that receive a DMA error response are disabled (CE = 0) by hardware.

Table 12-73. Subsequence - Reading The DMA Descriptor Table Entry

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Determine the active page (ping or pong)	Use the PG bit	-h
Determine which page/pages are done	Use the DNE1 and DNE2 bits	1h
Determine which channels encountered a DMA error	Use the ERR1 and ERR2 bits	1h
Determine which asynchronous and control Rx channel pages contain a packet start	Use the PS1 and PS2 bits	1h

Servicing MLBSS Interrupts

To service the MLBSS interrupts, the steps desctibed in Table 12-74 should be followed.

Table 12-74. Servicing MLBSS Interrupts

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Clear the appropriate MediaLB channel status bits	MLB_MS0 and MLB_MS1 registers	0h
Enable protocol error interrupts for all active MediaLB channels	MLB_MIEN[28] CTX_PE MLB_MIEN[25] CRX_PE MLB_MIEN[21] ATX_PE MLB_MIEN[18] ARX_PE MLB_MIEN[16] SYNC_PE MLB_MIEN[0] ISOC_PE	1h 1h 1h 1h 1h 1h
Wait for an interrupt on the MLB0_MLBSS_MLB_INT_0 line		

Table 12-74. Servicing MLBSS Interrupts (continued)

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Determine which channel/channels are causing the interrupt	Read the MLB_MS0 and MLB_MS1 registers	1h
Determine the interrupt type	Read the RSTS and WSTS bits of the appropriate channel descriptor tables	-h
IF: Synchronous channels		
Clear WSTS errors to resume channel operation	WSTS[3]	0h
ENDIF		
IF: Isochronous channels		
Clear WSTS errors to resume channel operation	WSTS[2-1]	0h
ENDIF		
IF: Asynchronous and control channels		
Clear RSTS and WSTS errors to resume channel operation	RSTS[4], WSTS[4], RSTS[2] and WSTS[2]	0h
ENDIF		

Polling For MediaLB System Commands

The MediaLB core supports the MediaLB system commands (MlbScan, MlbReset, MOST_Unlock). The MLB_MSS register is used to detect a system command received from the MediaLB controller. The MLBSS automatically sends the appropriate system response to the MediaLB Controller. Software should follow the procedure shown in Table 12-75.

Table 12-75. Polling For MediaLB System Commands

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Poll periodically for a system command received from the MediaLB controller	MLB_MSS	-h
Clear the appropriate bits in MLB_MSS register after the application finishes the servicing	MLB_MSS	0h
IF: Software system command is detected	MLB_MSS[4] SWSYSCMD	1h
Read the MLB_MSD register to receive the system data sent from MediaLB Controller	MLB_MSD	-h
ENDIF		

12.1.4.4.2.2 Channel Table RAM Access

The memory interface block allows a direct software access to the channel table RAM. Any write to the MLB_MADR register triggers a single read or write cycle. Reading from the MLB_MADR register does not initiate a read or write access.

Table 12-76 shows a direct write to the channel table RAM.

Table 12-76. Direct Channel Table RAM Writes

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Load the 128-bit data entry	MLB_MDAT0, MLB_MDAT1, MLB_MDAT2 and MLB_MDAT3 registers	-h
Enable writing data	MLB_MDWE0, MLB_MDWE1, MLB_MDWE2 and MLB_MDWE3 registers	1h
Write the 8-bit channel table RAM target address	MLB_MADR[7-0] ADDR_7_0	-h

Table 12-76. Direct Channel Table RAM Writes (continued)

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Initiate a write cycle	MLB_MADR[31] WNR	1h
Determine when the transfer is complete	Poll the MLB_MCTL[0] XCMP	1h

Table 12-77 shows a direct read from the channel table RAM.

Table 12-77. Direct Channel Table RAM Reads

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Write the 8-bit channel table RAM target address	MLB_MADR[7-0] ADDR_7_0	-h
Initiate a read cycle	MLB_MADR[31] WNR	0h
Determine when the transfer is complete	Poll the MLB_MCTL[0] XCMP	1h
Read the 128-bit data entry	MLB_MDAT0, MLB_MDAT1, MLB_MDAT2 and MLB_MDAT3 registers	-h

12.1.4.4.3 MLBSS Standby Mode

Table 12-78 shows the software procedure to put MLBSS into standby mode.

Table 12-78. Putting MLBSS Into Standby Mode

Step	Register/ Bit Field/ Programming Model/ Comments	Value
Ensure that there are no more transfers pending on both ends - system memory and MediaLB	No more data has to be transmitted from system memory to MediaLB and no more data has to be transmitted from MediaLB to system memory	-
Check if on system memory side all DMA transfers (receiving from MediaLB and transmitting to MediaLB) are completed	Read the DNE1 and DNE2 bits in the associated DDT channel descriptor of all enabled channels(1)	1h
Ensure that no more valid data is received or transmitted on MediaLB.	This means that all expected packets/messages have been transferred out of the MLBSS internal data buffer. For asynchronous and isochronous control this can be confirmed by reading the write (WSTS) and read status (RSTS) of the CDT which indicates if a channel is active or idle. For synchronous control this check is not possible, since MediaLB channels always have some data to transmit or receive on an enabled MediaLB channel, no matter if this data is valid from a system software standpoint.	-
Disable MediaLB	MLB_MLBC0[0] MLBEN	0h
Disable HBI	MLB_HCTL[15] EN	0h
Disable DDT and CDT channels	Clear the associated channel enable bits in the CAT, DDT and CDT	0h
Stop the MLBSS clocks	At this point no data transfers can occur in the MLBSS and the clocks MLBSS_SCLK, MLBSS_HCLK and MLBSS_PCLK can be stopped	-

(1) The channel status interrupts in the MLB_ACSR0 and MLB_ACSR1 registers are active for the done channels (DNE1 = 1h and DNE2 = 1h). If this status is reached, the channels should not be set ready for transfer again through the RDY1 and RDY2 bits in DDT.

12.2 General Connectivity Peripherals

This section describes the general connectivity peripherals in the device.

12.2.1 General-Purpose Interface (GPIO)

This chapter describes the General-Purpose Input/Output (GPIO) for the device.

12.2.1.1 GPIO Overview

The General-Purpose Input/Output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

The device has one or more instances of GPIO modules. The GPIO pins are grouped into banks (16 pins per bank and 9 banks per module), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Not all GPIO pins are pinned out. See General Purpose Input/Output (GPIO) in the Module Integration section for more information.

Figure 12-56 presents the GPIO modules overview.

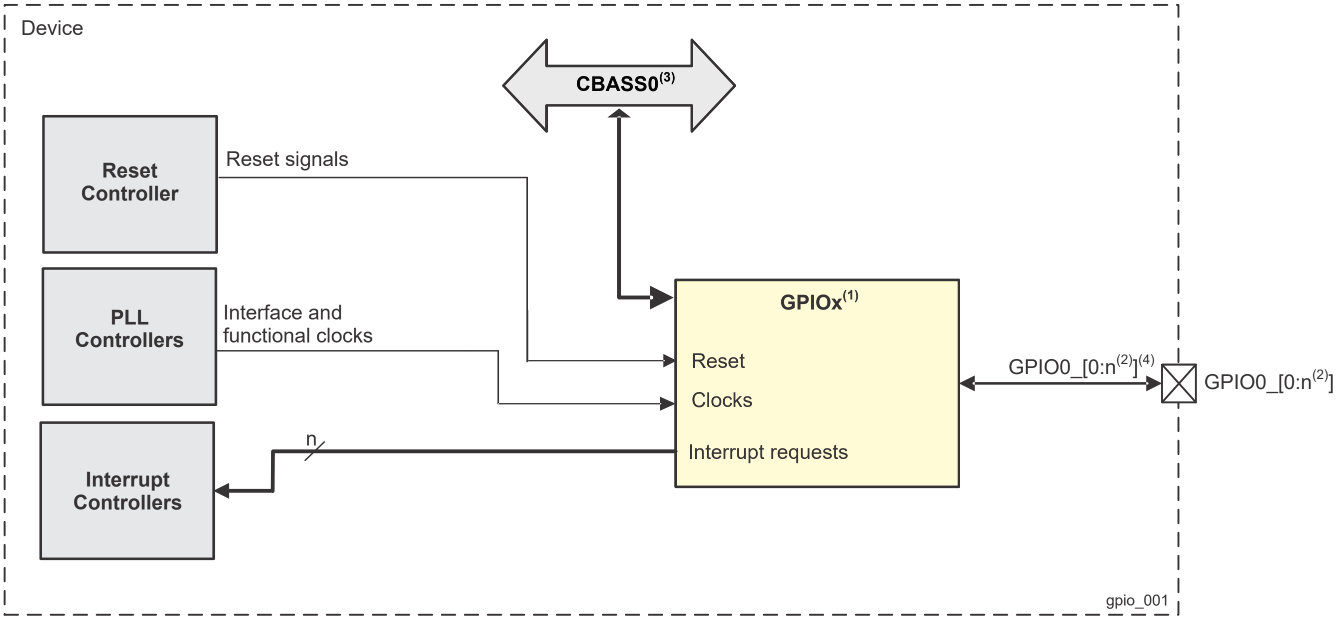


Figure 12-56. GPIO Modules Overview

A. (1): x represents a valid instance of GPIO in a domain.
B. (2): n represents the maximum number of GPIO signals -1.
C. (3): CBASS0 represents the connectivity in the domain of the IP.
D. (4): Some GPIO signals may be uni-directional. Consult the device datasheet for specifics.

12.2.1.1.1 GPIO Features

Each channel in the GPIO modules has the following features:

- Supports 9 banks of 16 GPIO signals
- Supports up to 9 banks of interrupt capable GPIOs
- Interrupts:
  - Can enable interrupts for each bank of 16 GPIO signals
  - Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO signal
- Set/clear functionality:

  - Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to another process during GPIO programming).
- Separate Input/Output registers:
  - If preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s) in addition to set/clear.
  - Output register, when read in, reflects output drive status. This, in addition to the input register reflecting pin status, allows wired logic be implemented.

12.2.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.2.1.2 GPIO Environment

This section describes the GPIO external connections (environment).

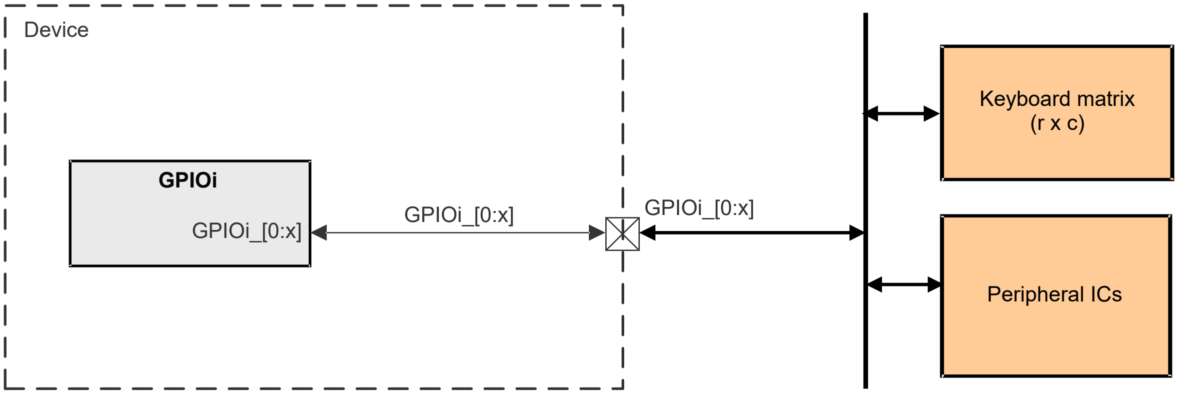
The general-purpose interface combines three GPIO modules for a flexible, user-programmable, general-purpose input/output (I/O) controller. The general-purpose interface implements functions that are not implemented with the dedicated controllers in the device and require simple input and/or output software-controlled signals. The GPIO allows a variety of custom connections and expands the I/O capabilities of the system to the real world.

The general-purpose interface can physically connect the device to a keyboard matrix and peripheral integrated circuits (ICs).

Figure 12-57 shows a typical application using the general-purpose interface.

12.2.1.2.1 GPIO Interface Signals

Figure 12-57 shows all of the GPIO interface signals.



Note

i represents a GPIO instance. See the device datasheet for available domains and GPIO instances.

Note

See Module Integration section for signal specifics in GPIO.

Figure 12-57. GPIO Interface Signals and Typical Application

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

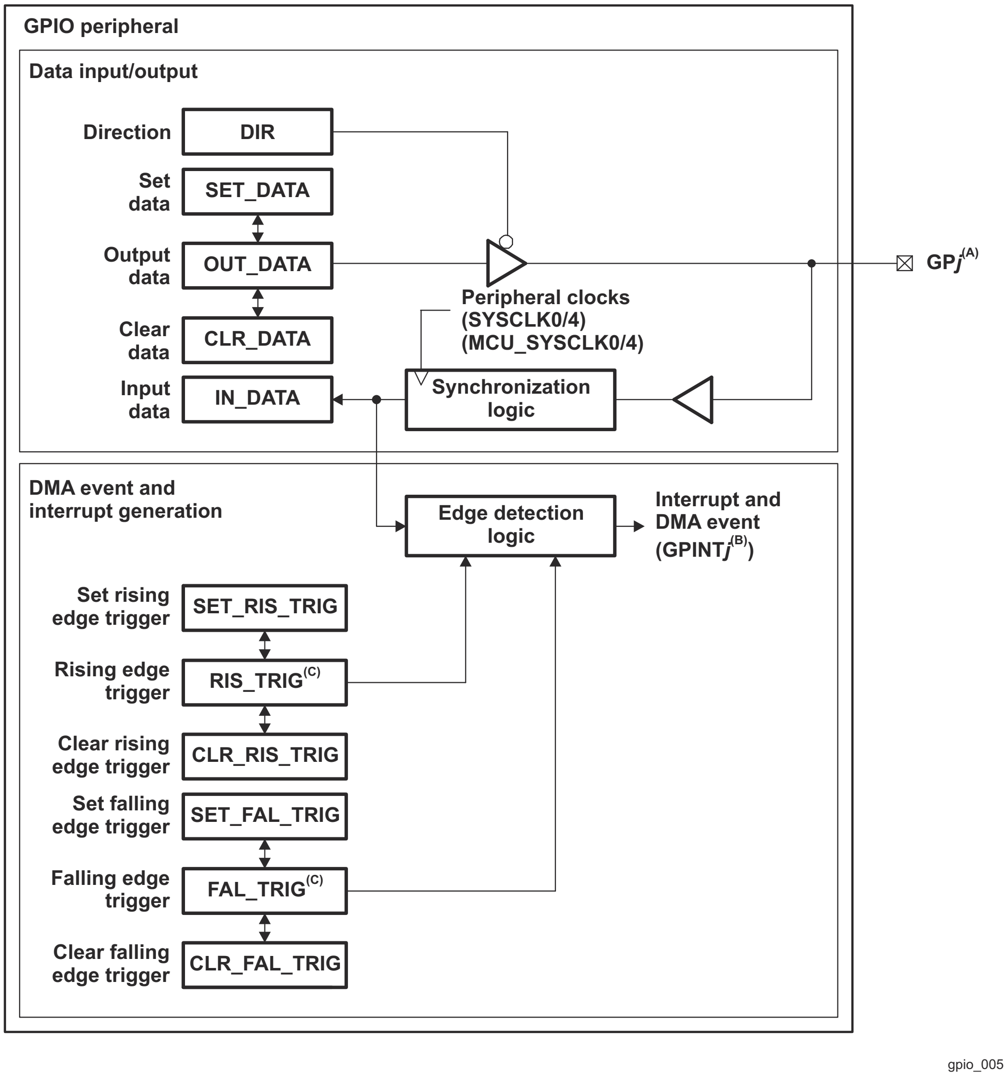
12.2.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.2.1.4 GPIO Functional Description

12.2.1.4.1 GPIO Block Diagram

Figure 12-58 shows the general-purpose interface block diagram.



A. Some of the GPj pins are muxed with other device signals. For details, see the device-specific Datasheet.

B. All GPINTj can be used as host CPU interrupts and synchronization events to the DMA.

C. The RIS_TRIG and FAL_TRIG registers are internal to the GPIO module and are not visible to the host CPU.

Figure 12-58. GPIO Block Diagram

12.2.1.4.2 GPIO Function

Each GPIO pin (GPj) can be independently configured as either an input or an output using the GPIO direction registers. The GPIO direction register (DIR) specifies the direction of each GPIO signal. Logic 0 indicates the GPIO pin is configured as output, and logic 1 indicates input.

When configured as output, writing a 0x1 to a bit in the set data register drives the corresponding GPj to a logic-high state. Writing a 0x1 to a bit in the clear data register drives the corresponding GPj to a logic-low state. The output state of each GPj can also be directly controlled by writing to the output data register.

For example, to set GP8 to a logic-high state, the software can perform one of the following:

- Write 100h to the GPIO0_SET_DATA01 register.
- Write 0h to the GPIO_DIR01 register to configure as output pin.

- Read in GPIO_OUT_DATA01 register, change bit 8 to 0x1, and write the new value back to GPIO_OUT_DATA01.

To set GP8 to a logic-low state, the software can perform one of the following:

- Write 100h to the GPIO_CLR_DATA01 register.
- Write 0h to the GPIO_DIR01 register to configure as output pin.
- Read in GPIO_OUT_DATA01 register, change bit 8 to 0x0, and write the new value back to GPIO_OUT_DATA01.

Note that writing a 0x0 to bits in the set data and clear data registers does not affect the GPIO pin state.

Also, for GPIO pins configured as input, writing to the set data, clear data, or output data registers does not affect the pin state.

For a GPIO pin configured as input, reading the input data register (IN_DATA) will return the pin state. Reading the SET_DATA register or the CLR_DATA data register will return the value in OUT_DATA, not the actual pin state. The pin state is available by reading the input data register. Note that when the direction is configured as input, the output state is determined by software’s programming set/clear/output registers, and may not agree with the pin state, which is driven by an external device.

12.2.1.4.3 Interrupt and Event Generation

Each GPIO pin (GPj) can be configured to generate a host CPU interrupt (GPINTj) or a synchronization event to the DMA (GPINTj). Configuration is on per-bank basis. Each bit of the BINT_EN parameter dictates YES/NO option for each bank. Bit 0 controls bank 0, bit 1 controls bank 1, and so on.

The interrupt and DMA event can be generated on the rising-edge, falling-edge, or on both edges of the GPIO signal. The edge detection logic is synchronized to the GPIO peripheral clock.

The direction of the GPIO pin does not need to be input when using the pin to generate the interrupt or DMA event. When the GPIO pin is configured as input, transitions on the pin trigger interrupts or DMA events. When the GPIO pin is configured as output, software can toggle the GPIO output register to change the pin state and in turn trigger the interrupt or DMA event.

Note that the direction of the pin need not be input for interrupt generation to work. When the GPINT pin is configured as input, transitions on the pin trigger interrupts. When the GPINT pin is configured as output, firmware can toggle the GPIO output register to change the pin state, and in turn trigger interrupts.

Each interrupt output of GPINT signal are available at the module boundary. Each group of 16 GPINT signals also has their masked interrupt outputs ORed together to generate a per bank interrupt, available at the module boundary. The idea is to either connect individual interrupts or per bank interrupts to the system interrupt controller.

12.2.1.4.3.1 Interrupt Enable (per Bank)

The GPIO_BINTEN register provides interrupt enable/disable feature for each bank of 16 GPINT signals.

12.2.1.4.3.2 Trigger Configuration (per Bit)

Two internal registers, RIS_TRIG and FAL_TRIG, specify which edge of the GPj signal generates an interrupt or DMA event. Each bit in these two registers corresponds to a GPj pin. Table 12-79 describes the host CPU interrupt and DMA event generation of GPj pin based on the bit settings of the RIS_TRIG and FAL_TRIG registers.

Table 12-79. GPIO Interrupt and DMA Event Configuration Options

Clarifying configuration of GPIO interrupt generation RIS_TRIG Bit n	FAL_TRIG Bit n	Host CPU Interrupt and DMA Event Generation
0	0	GPINTj interrupt and DMA event is disabled
0	1	GPINTj interrupt and DMA event is triggered on falling edge of GPj signal
1	0	GPINTj interrupt and DMA event is triggered on rising edge of GPj signal

Table 12-79. GPIO Interrupt and DMA Event Configuration Options (continued)

Clarifying configuration of GPIO interrupt generation RIS_TRIG Bit n	FAL_TRIG Bit n	Host CPU Interrupt and DMA Event Generation
1	1	GPINTj interrupt and DMA event is triggered on both rising and falling edge of GPj signal

The RIS_TRIG and FAL_TRIG registers are not directly accessible or visible to the host CPU. These registers are accessed indirectly through four registers: SET_RIS_TRIG, CLR_RIS_TRIG, SET_FAL_TRIG, and CLR_FAL_TRIG. Writing 1 to a bit on the SET_RIS_TRIG register sets the corresponding bit on the RIS_TRIG register. Writing 1 to a bit of the CLR_RIS_TRIG register clears the corresponding bit on the RIS_TRIG register. Writing to the SET_FAL_TRIG and CLR_FAL_TRIG registers works the same way on the FAL_TRIG register.

Reading the SET_RIS_TRIG or CLR_RIS_TRIG register returns the value of the RIS_TRIG register. Reading from the SET_FAL_TRIG and CLR_FAL_TRIG register returns the value of the FAL_TRIG register.

To use the GPIO pins as sources for host CPU interrupts and DMA events, the associated bank interrupt enable register bit in GPIO_BINTEN must also be set to 1. For example, to enable GPIO0_19 (which is in bank 1), GPIO_BINTEN[1] = 1 should be set to enable interrupts for bank 1.

12.2.1.4.3.3 Interrupt Status and Clear (per Bit)

The INTSTAT registers provide interrupt status upon reading, and interrupt clear feature upon writing 1 to the corresponding bit position(s). Upon receiving an interrupt, the ISR can examine the interrupt status and clear the processed interrupts.

Note

The GPIO module generates an interrupt pulse on the individual GPINT interrupt in response to each occurrence of the specified edge condition. Therefore, for GPINT signals having their interrupts routed directly to the interrupt controller, it is not necessary to clear the status bits in this module. The interrupt status and clear register is a facility for the per-bank interrupt connection.

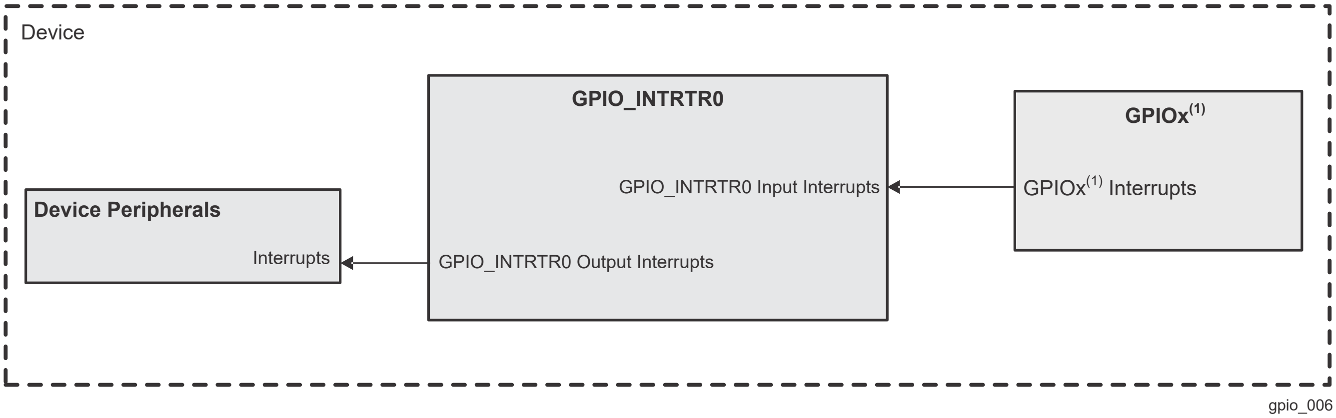
12.2.1.4.4 GPIO Interrupt Connectivity

Because this device muxes GPIO signals with other functional signals, the availability of any particular GPIO and hence the usability of its associated interrupt will change based on the use case pin muxing. The large number of possible GPIO interrupt sources makes it impractical to route all interrupt events to each processing element. Since most applications do not typically require a large number of GPIO interrupts, the interrupt uncertainty is resolved by mapping all GPIO interrupts to a series of event muxes implemented using Interrupt Router (IntRouter) modules. These muxes allow any one of the available GPIO interrupts to be selected and passed on as an event to the various processor interrupt controllers and DMA controllers. Event selection is controlled through associated registers within each IntRouter.

The GPIO bank interrupts already represent a consolidation of the 16 GPIO interrupts associated with each bank and are routed directly to various interrupt controllers rather than through the GPIO IntRouters.

One of the GPIO pins has a potential use case as an Arm reset input and should therefore be routed as highest priority interrupt in the GIC and mapped to nFIQ in software.

Figure 12-59 shows the GPIO Interrupt Routers connectivity. Refer to *Interrupt Routers*, for more details on the GPIO Interrupt Routers connectivity.



A. (1): x represents a valid instance of GPIO in a domain.

Figure 12-59. GPIO Interrupt Router Connectivity

12.2.1.4.5 Emulation Halt Operation

The GPIO peripheral is not affected by emulation halts.

12.2.1.5 GPIO Programming Guide

12.2.1.5.1 GPIO Low-Level Programming Models

12.2.1.5.1.1 Global Initialization

12.2.1.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the general-purpose interface module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the environment and integration of the general-purpose interface. For more information, see *GPIO Environment* and *Module Integration*.

Table 12-80. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
LPSC0	Module reset must be enabled. For more information about the module configuration, see *Reset*.
PLLCTRL0	Interface and functional clocks must be enabled. For more information about the module configuration, see *Clocking*.
MCU_PLLCTRL0	Interface and functional clocks must be enabled. For more information about the module configuration, see *Clocking*.
GPIOMUX_INTRTR0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling GPIOMUX_INTRTR0 interrupts, see *Interrupts*.
MCU_GPIOMUX_INTRTR0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MCU_GPIOMUX_INTRTR0 interrupts, see *Interrupts*.
Interconnects	For information about the MCU_CBASS0, and CBASS0 interconnects configuration, see *System Interconnect*.

12.2.1.5.1.1.2 GPIO Module Global Initialization

This procedure initializes the general-purpose Interface module after a power-on reset (POR) or software reset.

Table 12-81. GPIO Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure GPIO channels as input or output of the corresponding bank	DIR	-h
Interrupt requests configuration		
Configure detection events	SET_RIS_TRIG and/or SET_FAL_TRIG	-h
Clear interrupt status	INTSTAT	FFFFh
Enable interrupts for desired banks [0:8]	GPIO_BINTEN[8-0]	-h

12.2.1.5.1.2 GPIO Operational Modes Configuration

12.2.1.5.1.2.1 GPIO Read Input Register

Table 12-82. GPIO Read Input Register

Step	Register/Bit Field/Programming Model	Value
Read interrupt status of the corresponding bank	INTSTAT	-h
Read input register value	IN_DATA	-h
Clear interrupt status	INTSTAT	FFFF FFFFh

12.2.1.5.1.2.2 GPIO Set Bit Function

Table 12-83. GPIO Set Bit Function

Step	Register/Bit Field/Programming Model	Value
Write 1h to set desired bit(s) in SET_DATA register.	SET_DATA	-h

12.2.1.5.1.2.3 GPIO Clear Bit Function

Table 12-84. GPIO Clear Bit Function

Step	Register/Bit Field/Programming Model	Value
Write 1h to clear desired bit(s) in CLR_DATA register.	CLR_DATA	-h

12.2.2 Inter-Integrated Circuit (I2C) Interface

This section describes the Inter-Integrated Circuit (I2C) module in the device.

12.2.2.1 I2C Overview

The device contains multicontroller Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm and any I^2C-bus-compatible device that connects via the I^2C serial bus. External components attached to the I^2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I^2C interface.

Each multicontroller I^2C module can be configured to act like a target or controller I^2C-compatible device.

I^2C instances may be implemented with dedicated, I^2C compliant, open-drain I/O buffers, or with standard LVCMOS I/O buffers. The I^2C instances associated with open-drain I/O buffers can support Hs-mode (up to 3.4 Mbps when the I/O buffers are operating at 1.8 V but limited to 400 kbps when the I/O buffers are operating at 3.3 V).

The I^2C instances associated with standard LVCMOS I/O buffers can support Fast-mode (up to 400 kbps). The LVCMOS I/O buffers being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.

Refer to the device specific datasheet for details on which instances support which buffer type.

For the specific I/O timing characteristics of the different I^2C instances, see the device-specific Datasheet.

I2C Modules Overview shows the I2C modules overview.

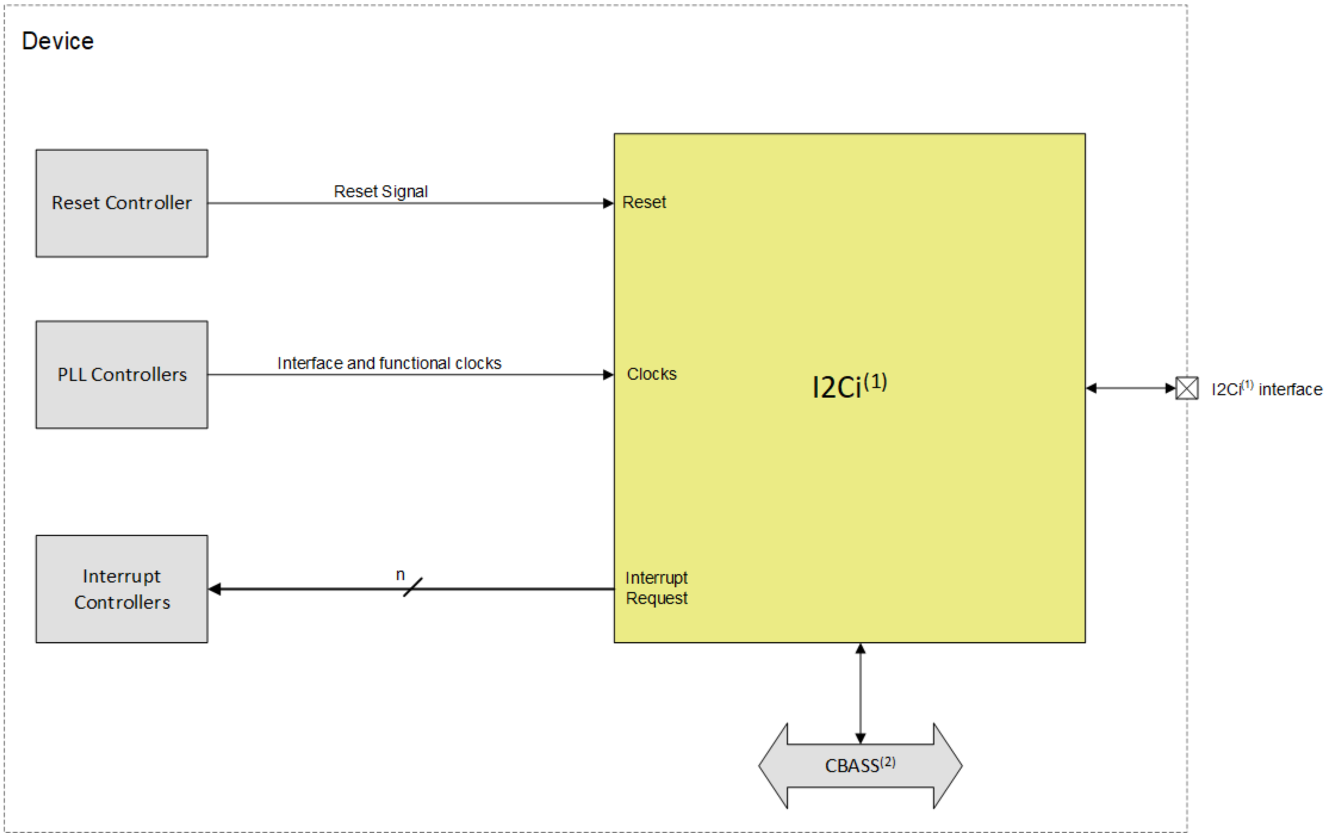


Figure 12-60. I2C Module Overview

Note

(1): i = 0 to (number of instances - 1) in the Domain

Note

(2): If MCU Domain is applicable, MCU_I2C instances are connected to MCU_CBASS

12.2.2.1.1 I2C Features

Each multicontroller I2C module has the following features:

- Compliant with Philips I^2C-bus specification version 2.1
- Supports a standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Supports HS mode (up to 3.4 Mbps) only for instances with true open drain buffer and in 1.8 V mode
- 7-bit and 10-bit device addressing modes
- General call
- Start/Restart/Stop
- Multicontroller transmitter/target receiver mode
- Multicontroller receiver/target transmitter mode
- Combined controller transmit/receive and receive/transmit mode
- Built-in FIFO for buffered read
- Module enable/disable capability
- Programmable multitarget channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Low power consumption
- Support Auto Idle mechanism
- Support Idle Request/Idle Acknowledge handshake mechanism
- Support for asynchronous wakeup mechanism
- Wide interrupt capability

12.2.2.1.2 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.2.2.1.3 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.2.2.2 I2C Environment

This section describes the I2C external connections (environment).

12.2.2.2.1 I2C Typical Application

Figure 12-61 shows the multicontroller I2C and their related connections with I^{2}C-compliant devices.

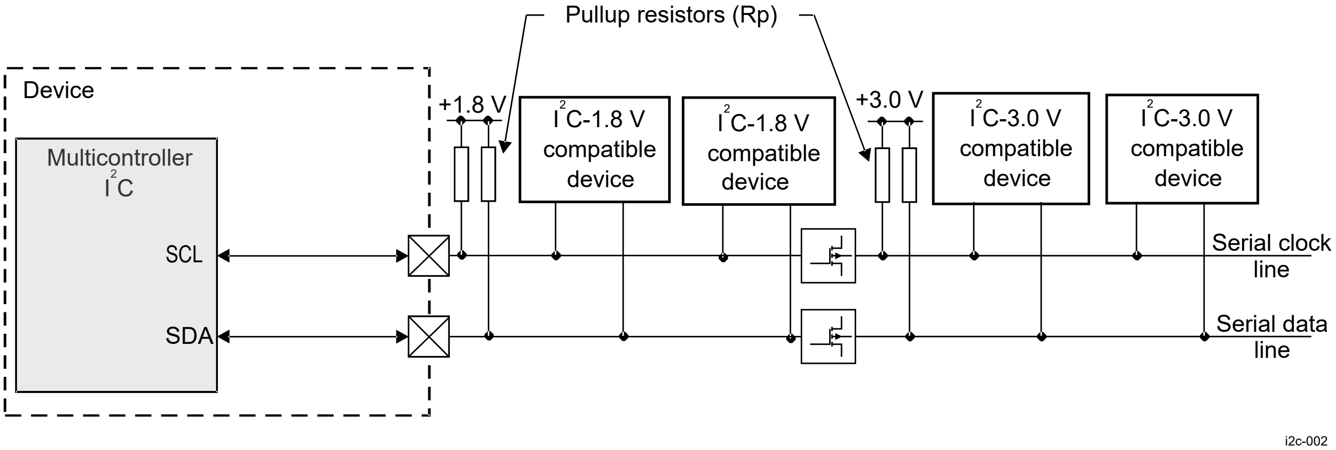
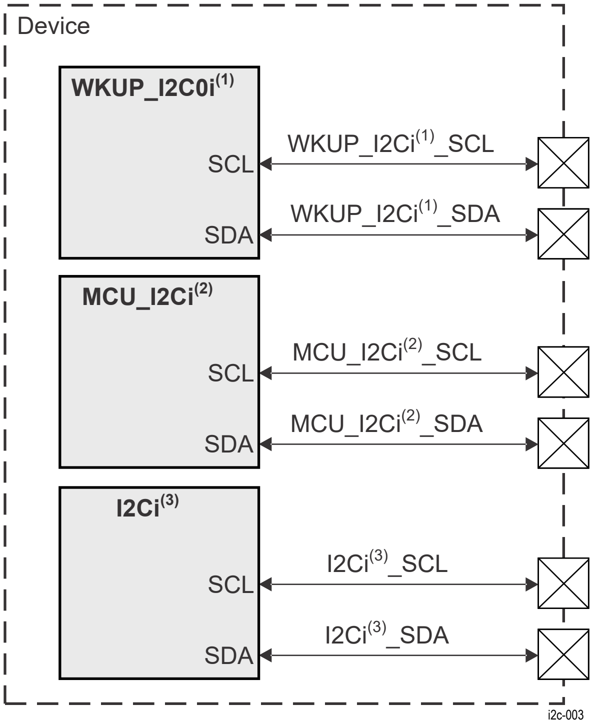


Figure 12-61. I2C and Typical Connections to I2C Devices

12.2.2.2.1.1 I2C Pins for Typical Connections in I2C Mode

Figure 12-62 shows the multicontroller I2C pins used for typical connections with I^{2}C devices.



1. i = 0 to (number of devices - 1) in WKUP Domain, if applicable
2. i = 0 to (number of devices - 1) in MCU Domain, if applicable
3. i = 0 to (number of devices - 1) in MAIN Domain, if applicable

Figure 12-62. I2C Interface Signals

12.2.2.2.1.2 I2C Interface Typical Connections

Table 12-85 describes the I2C I/O signals.

Table 12-85. I2C I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value
			WKUP_I2Ci(2)	
SCL	WKUP_I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	WKUP_I2Ci(2)_SDA	I/O	I^2C serial data line.	1
			MCU_I2Ci(2)	
SCL	MCU_I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	MCU_I2Ci(2)_SDA	I/O	I^2C serial data line.	1
			I2Ci(2)	
SCL	I2Ci(2)_SCL	I/O	I^2C serial clock line.	1
SDA	I2Ci(2)_SDA	I/O	I^2C serial data line.	1

(1) I = Input; O = Output; I/O = Bidirectional
(2) i represents an I2C instance. See the device datasheet for available domains and I2C instances.

12.2.2.2.1.3

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.2.2.2 I2C Typical Connection Protocol and Data Format

12.2.2.2.2.1 I2C Serial Data Format

The I2C controller operates in 8-bit word data format (byte write access supported for the last access). Each byte transmitted or received on the serial data line is 8 bits long. The number of bytes that can be transmitted or received is not restricted. The data is transferred with the most-significant bit (MSB) first. In receiver mode, each byte is followed by an acknowledge bit from the I2C module.

Figure 12-63 shows a typical I^2C communication format.

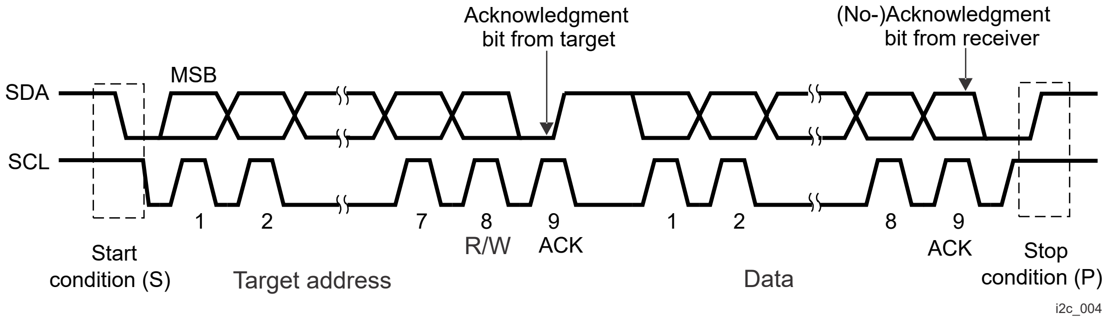


Figure 12-63. I2C Data Transfer

12.2.2.2.2.2 I2C Data Validity

The data on the serial data line (SDA) must be stable during the high period of the serial clock line. The high and low states of the data line can change only when the clock signal on the serial clock line (SCL) is low.

Figure 12-64 is an example of data validity requirements.

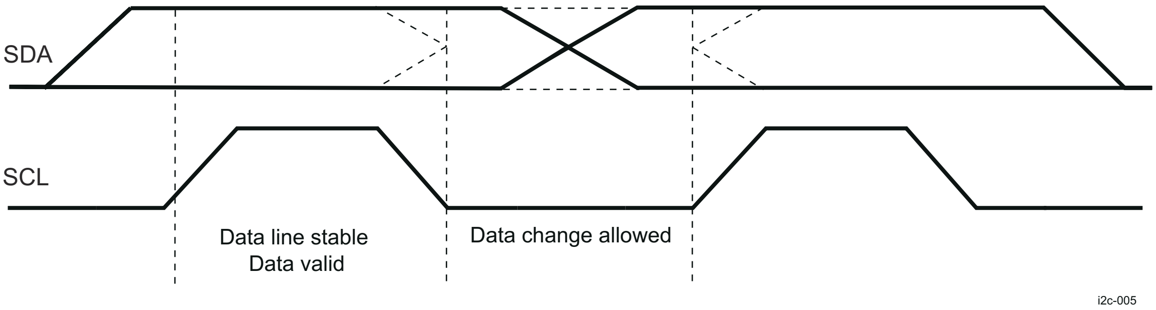


Figure 12-64. I2C Bit Transfer on the I2C Bus

12.2.2.2.2.3 I2C Start and Stop Conditions

The I2C module generates start (S) and stop (P) conditions when it is configured as a controller.

- An S condition is a high-to-low transition on the serial data line while serial clock line is high.
- A P condition is a low-to-high transition on the serial data line while serial clock line is high.

The bus is considered busy after the S condition (the I2C_IRQSTATUS_RAW [12] BB bit is 1 to indicate that the bus is busy) and free after the P condition (the I2C_IRQSTATUS_RAW [12] BB bit is 0 to indicate that the bus is free).

Figure 12-65 shows the waveforms that occur during an S and a P condition.

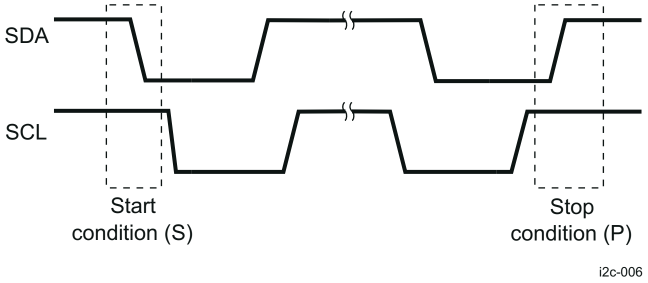


Figure 12-65. I2C S and P Condition Events

Note

I2C controller does not support messages non-compliant with I^{2}C standard. Void messages are non-standard I^{2}C messages and will lockup the controller. A void message is a START condition followed by a STOP condition, in other words, while the bus is free the SDA line is pulled low (START) and then released (STOP). This would result in a timeout (software) of the next controller transfer which would never complete. A soft reset of the controller is recommended for recovery.

12.2.2.2.2.4 I2C Addressing

The I2C module supports two data formats in fast/standard (F/S) and HS modes:

- 7-bit/10-bit addressing format
- 7-bit/10-bit addressing format with repeated start (Sr) condition

12.2.2.2.2.4.1 Data Transfer Formats in F/S Mode

Figure 12-66 shows the I2C data transfer formats in F/S mode.

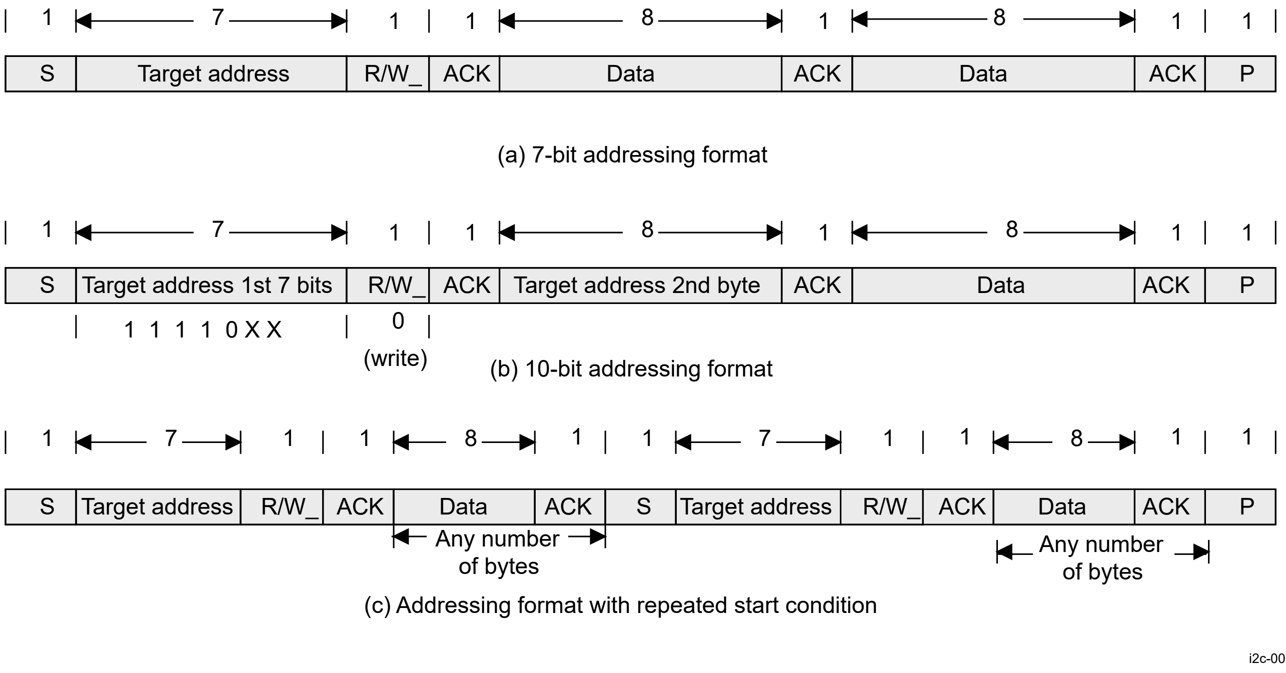


Figure 12-66. I2C Data Transfer Formats in F/S Mode

The first word after an S condition consists of 8 bits. In acknowledge mode, an extra dedicated acknowledgment bit is inserted after each byte.

In addressing formats with 7-bit addresses, the first byte is composed of 7 MSB target address bits and 1 least-significant bit (LSB) R/W_ bit.

The LSB R/W_ bit of the address byte indicates the transmission direction of the data bytes that follow it. If R/W_ is 0, the controller writes data to the selected target; if it is 1, the controller reads data from the target.

In addressing formats with 10-bit addresses, the structure of the first byte is 11110XXY, where XX is the two MSBs of the 10-bit addresses, and Y is the R/W_ bit. If the R/W_ bit is 0, the next byte contains the last 8 bits of the target address. If the R/W_ bit is 1, the next byte contains data transmitted from the target to the controller.

12.2.2.2.2.4.2 Data Transfer Format in HS Mode

Figure 12-67 shows the I2C data transfer format in HS mode.

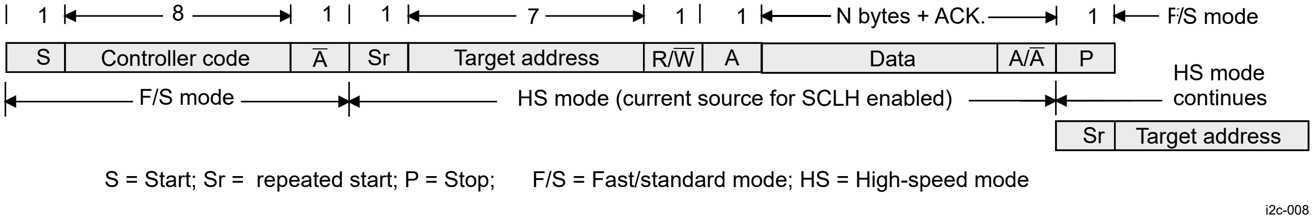


Figure 12-67. HS I2C Data Transfer in HS Mode

Each multicontroller I2C can also operate in HS mode. In this case, after the S condition, the module, which is in F/S mode, writes the controller code address (0x00001XXX, where XXX is the variable portion of the controller code) on the bus. No device connected on the same bus acknowledges this address. The module switches the clock to the HS clock and after an Sr condition, and sends the target address and the data, as shown in Figure 12-67.

12.2.2.2.2.5 I2C Controller Transmitter

In controller transmitter mode, data assembled in one of the previously described data formats is shifted out on the serial data line SDA in sync with the self-generated clock pulses on the serial clock line SCL. The clock pulses are inhibited and SCL is held low when the intervention of the processor is required (XUDF) after a byte is transmitted.

12.2.2.2.2.6 I2C Controller Receiver

Controller receiver mode can be entered only from controller transmitter mode. With any of the address formats (a), (b), or (c) (see Figure 12-66), if R/W_ is high, the module enters controller receiver mode after the target address byte and bit R/W_ are transmitted. Serial data bits received on bus line SDA are shifted in synchronization with the self-generated clock pulses on SCL.

12.2.2.2.2.7 I2C Target Transmitter

Target transmitter mode can be entered only from target receiver mode. With any of the address formats (a), (b), or (c) (see Figure 12-66), the target transmitter is entered if the target address byte is the same as its own address and bit R/W_ is transmitted, if R/W_ is high. The target transmitter shifts the serial data out on the data line SDA in sync with the clock pulses that are generated by the controller device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (XUDF).

12.2.2.2.2.8 I2C Target Receiver

In this mode, serial data bits received on the bus line SDA are shifted-in in sync with the clock pulses on SCL that are generated by the controller device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (ROVR) after a byte is received.

12.2.2.2.2.9 I2C Bus Arbitration

If two or more controller transmitters start a transmission on the same bus almost simultaneously, an arbitration procedure is invoked. The arbitration procedure uses the data presented on the serial bus by the competing transmitters. When a transmitter senses that a high signal it has presented on the bus has been overruled by a low signal, it switches to the target receiver mode, sets the arbitration lost (I2C_IRQSTATUS_RAW[0] AL) flag, and generates the arbitration lost interrupt. I2C Arbitration Between Controller Transmitters shows the arbitration procedure between two devices. The arbitration procedure gives priority to the device that transmits the serial data stream with the lowest binary value. If two or more devices send identical first bytes, arbitration continues on the subsequent bytes.

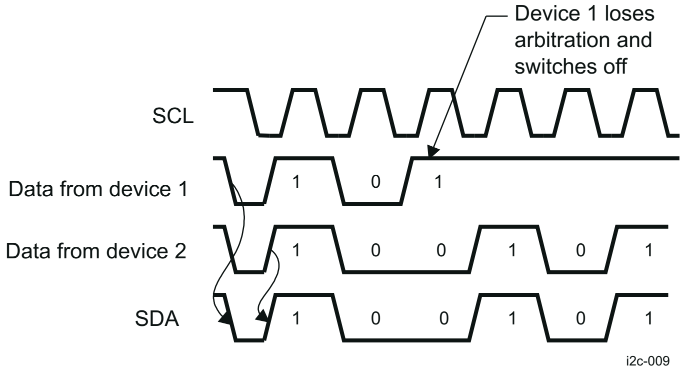


Figure 12-68. I2C Arbitration Between Controller Transmitters

12.2.2.2.2.10 I2C Clock Generation and Synchronization

Under normal conditions, only one controller device generates the clock signal - SCL. However, there are two or more controller devices during the arbitration procedure, and the clock must be synchronized so that the data output can be compared. The wired-AND property of the clock line means that a device that first generates a low period of the clock line overrules the other devices. At this high/low transition, the clock generators of the other devices are forced to start generation of their own low period. The clock line is then held low by the device with the longest low period, while the other devices that finish their low periods must wait for the clock line to be released before starting their high periods. A synchronized signal on the clock line is thus obtained, where the slowest device determines the length of the low period and the fastest device determines the length of the high period. If a device pulls down the clock line for a longer time, the result is that all clock generators must enter the

WAIT-state. In this way a target can slow down a fast controller and the slow device can create enough time to store a received byte or prepare a byte to be transmitted (clock stretching).

Note

In case the SCL or SDA lines are stuck low, a bus clearing operation is supported:

- If the clock line (SCL) is stuck low, the preferential procedure is to reset the bus using the hardware reset signal if the I^2C devices have hardware reset inputs. If the I^2C devices do not have hardware reset inputs, cycle power to the devices to activate the mandatory internal power-on reset (POR) circuit.
- If the data line (SDA) is stuck low, the controller should send nine clock pulses. The device that held the bus low should release it sometime within those nine clocks. If not, then use the hardware reset or cycle power to clear the bus.

Figure 12-69 shows clock synchronization.

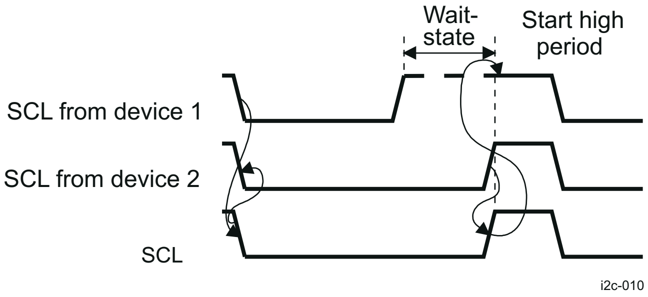


Figure 12-69. I2C Clock Generators Synchronization

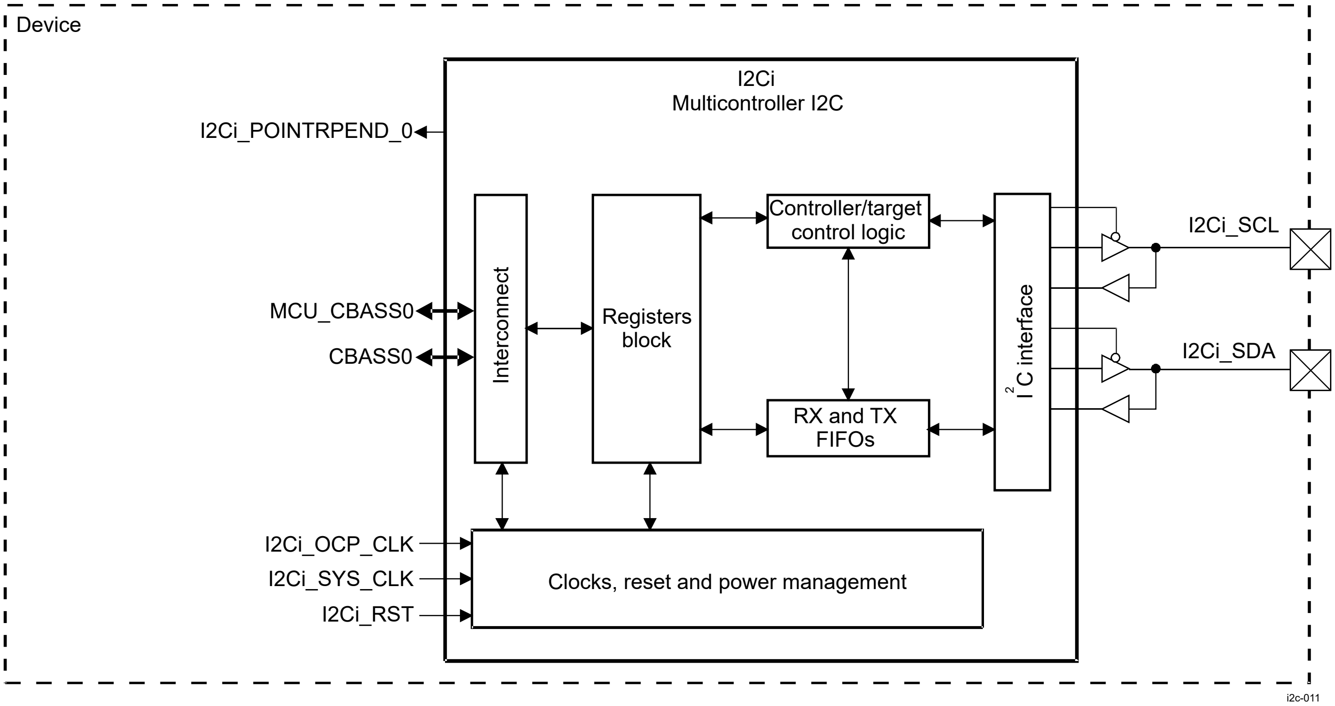
12.2.2.3 I2C Functional Description

12.2.2.3.1 I2C Block Diagram

Note

DMA mode and SCCB Protocol are not supported on this family of devices.

Figure 12-70 presents the multicontroller I2C block diagram.



A. i = 0 to number of devices in MCU domain -1, if applicable.

B. i = 0 to number of devices in MAIN domain -1, if applicable.

Figure 12-70. I2C Block Diagram

The ten multicontroller I2C can be configured in F/S I^{2}C mode or HS I^{2}C mode. The operation mode is selected by configuring the I2C_CON[13-12] OPMODE bit field.

Table 12-86 lists the available operation modes.

Table 12-86. I^{2}C Operation Mode Selection

Operation Mode	Value of I2C_CON[13-12] OPMODE
F/S I^{2}C	0x0
HS I^{2}C	0x1
SCCB	0x2
Reserved (not used)	0x3

12.2.2.3.2 I2C Clocks

12.2.2.3.2.1 I2C Clocking

Each multicontroller I2C uses the SYS_CLK functional clock in the Device Configuration section. The internal sampling clock INTERNAL_CLK is generated by dividing the functional clock by the I2C_PSC[7-0] PSC bit field value + 1 in F/S mode, or in the first phase of HS mode; or by directly using the functional clock in the second phase of HS mode (prescaler is bypassed).

The low time of the SCLL signal is determined by the I2C_SCLL[7-0] SCLL bit field in F/S mode and in the first phase of HS mode; or by the I2C_SCLL[15-8] HSSCLL bit field in the second phase of HS mode.

The high time of the SCLH signal is determined by the I2C_SCLH[7-0] SCLH bit field in F/S mode and in the first phase of HS mode; or by the I2C_SCLH[15-8] HSSCLH bit field in the second phase of HS mode.

Table 12-87 lists the t_{LOW} and t_{high} values in controller mode only (in target mode, the I2C controller does not generate the I^2C clock).

Table 12-87. I^2C t_{LOW} and t_{high}Values of the I^2C Clock

Mode	Clock	t_{LOW}	t_{high}
F/S or HS first phase	INTERNAL_CLK = SYS_CLK / (I2C_PSC[7-0] PSC bit field + 1)	(I2C_SCLL[7-0] SCLL bit field value + 7) × INTERNAL_CLK period	(I2C_SCLH[7-0] SCLH bit field value + 5) × I2Ci_INTERNAL_CLK period
HS second phase	SYS_CLK	(I2C_SCLL[15-8] HSSCLL bit field value + 7) × SYS_CLK period	(I2C_SCLL[15-8] HSSCLH bit field value + 5) × I2Ci_SYS_CLK period

Note

i = 0 to number of devices in MCU domain -1, if applicable.

Note

i = 0 to number of devices in MAIN domain -1, if applicable.

Note

For HS mode, the I2C_SCLL[15-8] HSSCLL and I2C_SCLL[7-0] SCLL bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

For HS mode, the I2C_SCLH[15-8] HSSCLH and I2C_SCLH[7-0] SCLH bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

Note

The equations in Table 12-87 give the SCLL timing values for SCLL/SCLH/HSSCLL/HSSCLH at I2C controller outputs. Actual t_{low} and thigh periods may vary depending on the board (the load capacitance on the SCLL signal). If necessary, any adjustments to the SCLL/SCLH/HSSCLL/HSSCLH values must be determined by measurements of actual SCL signal on the board.

CAUTION

During active mode (the I2C_CON[15] I2C_EN bit is set to 1), make no changes to the I2C_SCLL and I2C_SCLH registers. Changes may result in unpredictable behavior.

Table 12-88 lists the register values for obtaining the maximum I^2C bit rates and the maximum period of the filtered spikes in F/S mode and HS mode.

Table 12-88. I2C Register Values for Maximum I2C Bit Rates in I2C F/S, I2C HS Modes (1)

	I^2C Mode for			Description
	Standard Mode	**Fast Mode**	**High-Speed Mode(2)**	
SYS_CLK frequency (MHz)	96			
OCP_CLK frequency (MHz)	133			
I2C_PSC[7-0] PSC	**23**	**9**	**1**	Prescaler value for F/S and HS modes
INTERNAL_CLK frequency (MHz)	4	9.6	96	
I2C_SCLL[7-0] SCLL	**13**	**7**	**115**	Value for F/S mode and first phase of HS mode

Table 12-88. I2C Register Values for Maximum I2C Bit Rates in I2C F/S, I2C HS Modes (1) (continued)

	I^{2}C Mode for			Description
I2C_SCLH[7-0] SCLH	**15**	**5**	**113**	Value for F/S mode and first phase of HS mode
Maximum bit rate (Mbps)	0.1	0.4	0.4	F/S mode and first phase in HS mode maximum bit rate
Maximum filter period (ns)	250	104.2	10	
I2C_SCLL[15-8] HSSCLL			**12**	Values for second phase of HS mode
I2C_SCLH[15-8] HSSCLH			**5**	Values for second phase of HS mode
HS mode maximum bit rate (Mbps)			3.31	HS mode maximum bit rate
Maximum filter period (ns)			10	

(1) Programmable fields are in bold.
(2) HS mode is not supported on this family of devices.

Note

This table presents informative values only for the configuration parameters and the I^{2}C bus performance obtained according to these values. The delays added by the analog pads are not considered in these figures.

Note

For MCU_I2C[0-1]

For I2C[0-3]

I2Ci_INTERNAL_CLK freq = I2Ci_SYS_CLK / (PSC +1)

F/S filter period = 1 / I2Ci_INTERNAL_CLK

HS filter period = 1 / I2Ci_SYS_CLK freq

HS bit rate = I2Ci_SYS_CLK freq / (HSSCLL+ 7 + HSSCLH + 5)

FS bit rate = I2Ci_INTERNAL_CLK / (SCLL+ 7 + SCLH + 5)

12.2.2.3.2.2 I2C Automatic Blocking of the I2C Clock Feature

This feature offers the possibility for the LH to command the blocking of the I^{2}C clock after the target addressing phase, when the I2C controller is addressed by an external controller device using a certain Own Address.

The release of the I^{2}C clock can be performed independently for each Own Address (I2C_OA, and I2C_OAx registers, where x = 1, 2, 3) by deasserting the corresponding bit in the I2C_SBLOCK register.

12.2.2.3.3 I2C Software Reset

Each multicontroller I2C supports the software reset by accessing the I2C_SYSC[1] SRST bit (1: reset; 0: normal mode).

The software reset status can be checked by accessing the I2C_SYSS[0] RDONE bit (1: reset is done; 0: reset is ongoing).

To do a software reset, the following steps must be done:

1. Ensure that the module is disabled (clear the I2C_CON[15] I2C_EN bit to 0).
2. Set the I2C_SYSC[1] SRST bit to 1.
3. Enable the module by setting I2C_CON[15] I2C_EN bit to 1.
4. Check the I2C_SYSS[0] RDONE bit until it is set to 1 to indicate the software reset is complete.

Note

The I2C_CON[15] I2C_EN bit can hold the functional clock domain of the multicontroller I2C in reset after the device reset has been released. When the system bus reset is removed, this bit remains cleared. The functional part of the I2C controller is held in reset state while this bit is 0, and all configuration registers can be accessed.

The I2C_CON[15] I2C_EN bit must be set to 1 to enable the functional part of the I2C controller.

The I2C_SYSS[0] RDONE bit is asserted only after the module is enabled by setting the I2C_CON[15] I2C_EN bit to 1.

12.2.2.3.4 I2C Power Management

Table 12-89 describes power-management features available for the multicontroller I2C.

Note

For information about source clock gating, see *Power* in the *Device Configuration*.

Note

Some of the I2C features described in this section may not be supported on this family of devices. See the *Module Integration* section for more information about unsupported features..

Table 12-89. I2C Local Power-Management Features

Feature	Registers	Description
Clock auto gating	I2C_SYSC[0] AUTOIDLE	This bit allows a local power optimization inside the module.
Target idle modes	I2C_SYSC[4-3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Clock activity	I2C_SYSC[9-8] CLOCKACTIVITY	For configuration details, see Table 12-90.
Global wake-up enable	I2C_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.

Table 12-90. I2C Clock Activity Settings

I2C_SYSC[9-8] CLOCKACTIVITY	Clock State When Module is in IDLE State		Features Available/Unavailable When Module is in IDLE State
	OCP_CLK	SYS_CLK	
00	OFF	OFF	Both clocks are disabled.
10	OFF	ON	Interface clock is disabled; Functional clock is enabled
01	ON	OFF	Functional clock is disabled; Interface clock is enabled
11	ON	ON	Both clocks are enabled.

12.2.2.3.5 I2C Interrupt Requests

The I2C controller must allocate a minimum of five registers for interrupts.

- Interrupt Raw Status (I2C_IRQSTATUS_RAW)
- Interrupt Enabled Status (I2C_IRQSTATUS)
- Interrupt Enable Set (I2C_IRQENABLE_SET)
- Interrupt enable Clear (I2C_IRQENABLE_CLR)
- End of interrupt (I2C_EOI)

End of Interrupt (I2C_EOI) is used by software to trigger an interrupt service completion.

Table 12-91 lists the event flags, and their mask, that can cause module interrupts.

Table 12-91. I2C Events

Event Flag	Event Unmask	Event Mask	Description
I2C_IRQSTATUS[0] AL	I2C_IRQENABLE_SET[0] AL_IE	I2C_IRQENABLE_CLR[0] AL_IE	Arbitration lost. This bit is automatically set by the hardware when it loses the arbitration in controller transmit mode, an interrupt is signaled to the host.
I2C_IRQSTATUS[1] NACK	I2C_IRQENABLE_SET[1] NACK_IE	I2C_IRQENABLE_CLR[1] NACK_IE	No acknowledgement. Bit is set when No Acknowledge is received, an interrupt is signaled to the host.
I2C_IRQSTATUS[2] ARDY	I2C_IRQENABLE_SET[2] ARDY_IE	I2C_IRQENABLE_CLR[2] ARDY_IE	Register access ready. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to the host.
I2C_IRQSTATUS[3] RRDY	I2C_IRQENABLE_SET[3] RRDY_IE	I2C_IRQENABLE_CLR[3] RRDY_IE	Receive data ready. Set to 1 by core when in receiver mode, a new data can be read. An interrupt is signaled to the host.
I2C_IRQSTATUS[4] XRDY	I2C_IRQENABLE_SET[4] XRDY_IE	I2C_IRQENABLE_CLR[4] XRDY_IE	Transmit data ready. Set to 1 by core when transmitter is ready for new data. An interrupt is signaled to the host.
I2C_IRQSTATUS[5] GC	I2C_IRQENABLE_SET[5] GC_IE	I2C_IRQENABLE_CLR[5] GC_IE	General call. Set to 1 by core when General Call address was detected. An interrupt is signaled to the host.
I2C_IRQSTATUS[6] STC	I2C_IRQENABLE_SET[6] STC_IE	I2C_IRQENABLE_CLR[6] STC_IE	Start condition detected. An interrupt is signaled to the host.
I2C_IRQSTATUS[7] AERR	I2C_IRQENABLE_SET[7] AERR_IE	I2C_IRQENABLE_CLR[7] AERR_IE	Bus Access Error. An interrupt is signaled to the host.
I2C_IRQSTATUS[8] BF	I2C_IRQENABLE_SET[8] BF_IE	I2C_IRQENABLE_CLR[8] BF_IE	Bus free. An interrupt is signaled to the host.
I2C_IRQSTATUS[9] AAS	I2C_IRQENABLE_SET[9] AAS_IE	I2C_IRQENABLE_CLR[9] AAS_IE	Address recognized as target. An interrupt is signaled to the host.
I2C_IRQSTATUS[10] XUDF	I2C_IRQENABLE_SET[10] XUDF_IE	I2C_IRQENABLE_CLR[10] XUDF_IE	Transmit underflow. An interrupt is signaled to the host.
I2C_IRQSTATUS[11] ROVR	I2C_IRQENABLE_SET[11] ROVR_IE	I2C_IRQENABLE_CLR[11] ROVR_IE	Receive overrun. An interrupt is signaled to the host.
I2C_IRQSTATUS[12] BB	N/A	N/A	Bus busy indicator
I2C_IRQSTATUS[13] RDR	I2C_IRQENABLE_SET[13] RDR_IE	I2C_IRQENABLE_CLR[13] RDR_IE	Receive draining. An interrupt is signaled to the host.
I2C_IRQSTATUS[14] XDR	I2C_IRQENABLE_SET[14] XDR_IE	I2C_IRQENABLE_CLR[14] XDR_IE	Transmit draining. An interrupt is signaled to the host.

12.2.2.3.6 I2C Programmable Multitarget Channel Feature

This feature allows each multicontroller I2C to be addressed using four separate Own Addresses configured in the I2C_OA and I2C_OAx registers (where x = 1, 2, 3). An additional register (I2C_ACTOA) is used to indicate to the LH which address is used by the external controller to communicate with the I2C controller.

Each Own Address can be independently configured in 7-bit or 10-bit mode by setting the corresponding bit (I2C_CON[7] XOA0, I2C_CON[6] XOA1, I2C_CON[5] XOA2, or I2C_CON[4] XOA3).

12.2.2.3.7 I2C FIFO Management

The depth of the RX and TX FIFOs can be checked by reading the I2C_BUFSTAT[15-14] FIFODEPTH bit field (0x0: 8 bytes, 0x1: 16 bytes, 0x2: 32 bytes, and 0x3: 64 bytes).

12.2.2.3.7.1 I2C FIFO Interrupt Mode

In FIFO interrupt mode (relevant interrupts enabled by the I2C_IRQENABLE_SET register), an interrupt signal informs the processor of the receiver and transmitter status. These interrupts are raised when the RX/TX FIFO thresholds (defined by the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX FIFO or the I2C_BUF[5-0] TXTRSH bit field value + 1 for the TX FIFO) are reached; the interrupt signals instruct the LH to transfer data to the destination (from the I2C controller in receive mode and/or from any source to the I2C controller FIFO in transmit mode).

Figure 12-71 and Figure 12-72 show receive and transmit operations, respectively, from a FIFO management point of view.

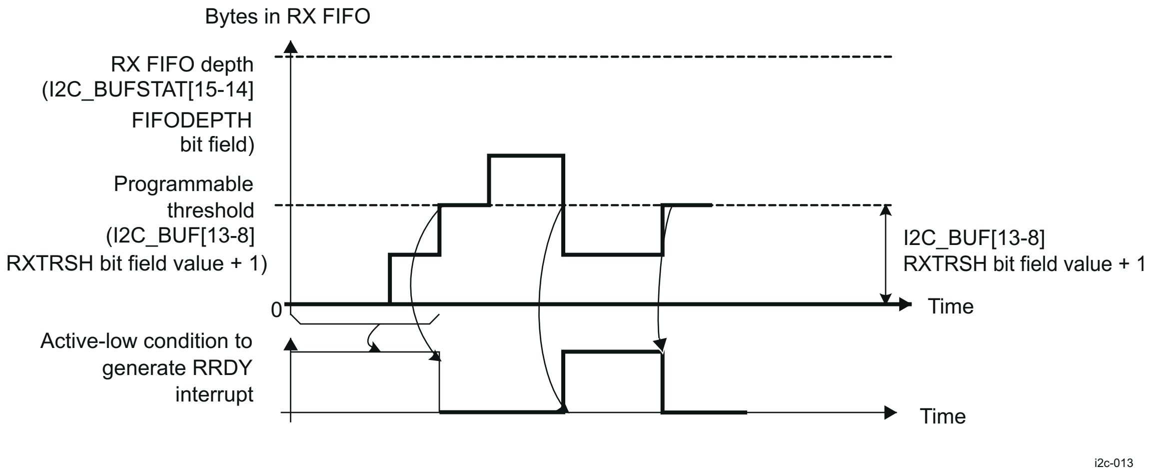


Figure 12-71. I2C Receive FIFO Interrupt Request Generation

In Figure 12-71 , the RRDY interrupt condition shows that the condition for generating an RRDY interrupt is achieved. The interrupt request is generated when this signal is active, and it can be cleared only by the LH by writing 1 in the corresponding bit. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In receive mode, an RRDY interrupt is generated as soon as the FIFO reaches its receive threshold (I2C_BUF[13-8] RXTRSH bit field value + 1). The interrupt can be deasserted only when the LH has handled enough bytes to make the number of bytes in the RX FIFO lower than the programmed threshold. For each interrupt, the LH can be configured to read a number of bytes equal to the value of the RX FIFO threshold.

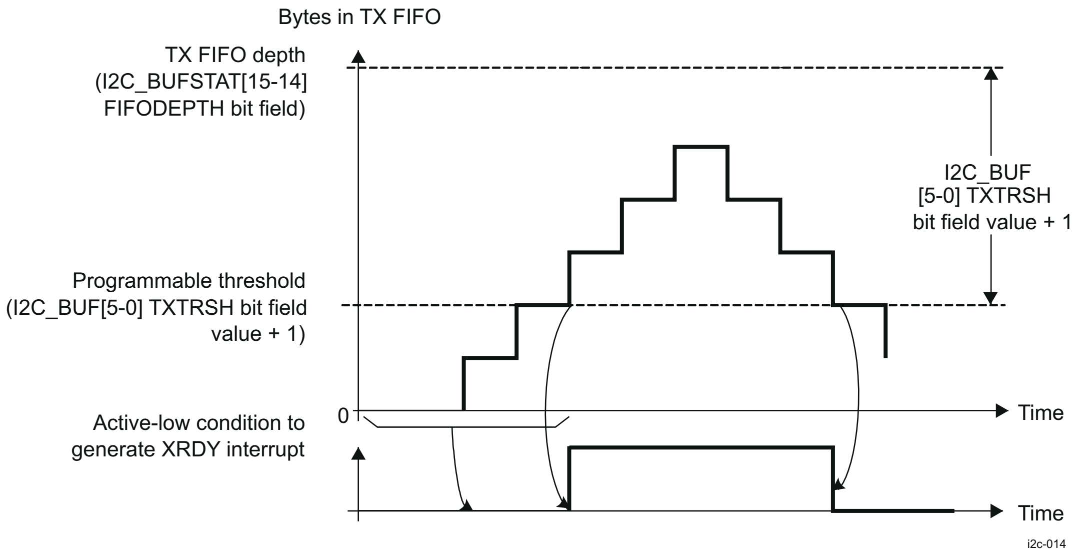


Figure 12-72. I2C Transmit FIFO Interrupt Request Generation

In Figure 12-72 , the XRDY interrupt condition shows that the condition for generating an XRDY interrupt is achieved. The interrupt request is generated when TX FIFO is empty or when the TX FIFO threshold is not reached, and the LH can clear the XRDY status bit by setting the I2C_IRQENABLE_CLR[4] XRDY_IE bit to

1 after transmitting the configured number of bytes. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In interrupt mode, the module offers two options for the LH application to handle the interrupts:

- When detecting an interrupt request (XRDY or RRDY type), the LH can write/read 1 data byte to/from the TX/RX FIFO and then clear the interrupt. The module reasserts the interrupt until the interrupt condition is not met.
- When detecting an interrupt request (XRDY or RRDY type), the LH can be programmed to write/read the amount of data bytes specified by the corresponding FIFO threshold (I2C_BUF[5-0] TXTRSH + 1 or I2C_BUF[5-0] RXTRSH + 1). In this case, the interrupt condition is cleared and the next interrupt is asserted again when the XRDY or RRDY condition is met again.

If the second-interrupt-serving approach is used, an additional mechanism (draining feature) is implemented for cases where the transfer length is not a multiple of the FIFO threshold value (see Section 12.2.2.3.7.3, *Draining Feature [I2C Mode Only]*).

Note

In target transmit mode (the I2C_CON[10] MST bit is cleared and the I2C_CON[9] TRX bit is set to 1), the draining feature must not be used, because the transfer length is not known at configuration time, and the external controller can end the transfer at any point by not acknowledging 1 data byte. If the draining feature is used in target transmit mode, data can remain in the TX FIFO without being transmitted over the I^2C bus. In this case, the TX FIFO must be cleared by setting the I2C_BUF[6] TXFIFO_CLR bit.

12.2.2.3.7.2 I2C FIFO Polling Mode

In FIFO polling mode (the I2C_IRQENABLE_SET[4] XRDY_IE and I2C_IRQENABLE_SET[3] RRDY_IE bits are disabled), the status of the module (receiver or transmitter) can be checked by polling the I2C_IRQSTATUS_RAW[4] XRDY and the I2C_IRQSTATUS_RAW[3] RRDY bits (the I2C_IRQSTATUS_RAW[13] RDR and I2C_IRQSTATUS_RAW[14] XDR bits can also be polled if the draining feature is enabled). The I2C_IRQSTATUS_RAW[4] XRDY and I2C_IRQSTATUS_RAW[3] RRDY bits accurately reflect the interrupt conditions described in the discussion of FIFO interrupt mode.

12.2.2.3.7.3 I2C Draining Feature

Note

DMA mode and SCCB Protocol are not supported on this family of devices.

The draining feature is implemented to handle the end of a transfer whose length is not a multiple of the FIFO threshold values (the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX threshold and the I2C_BUF[5-0] TXTRSH field value + 1 for the TX threshold). It can also transfer the remaining number of bytes (because the threshold is not reached).

This feature prevents the LH or the DMA controller from trying more FIFO accesses than necessary (for example, to generate at the end of a transfer a DMA RX request having fewer bytes in the FIFO than the configured DMA transfer length). Otherwise, an AERR interrupt is generated by the I2C_IRQSTATUS_RAW[7] AERR bit.

The draining mechanism generates an interrupt using the I2C_IRQSTATUS_RAW[13] RDR or I2C_IRQSTATUS_RAW[14] XDR bit at the end of the transfer, informing the LH that it must check the amount of data left to be transferred (the I2C_BUFSTAT[13-8] RXSTAT or I2C_BUFSTAT[5-0] TXSTAT bit fields) and enable the draining feature of the DMA controller by reconfiguring the DMA transfer length according to this value (when the DMA mode is enabled) or perform only the required number of data accesses (when the DMA mode is disabled).

In receive mode (controller or target), if the RX FIFO threshold (the I2C_BUF[13-8] RXTRSH bit field value + 1) is not reached, but the transfer ends on the I^2C bus and data remains in the RX FIFO (less than the threshold), the receive draining interrupt (the I2C_IRQSTATUS_RAW[13] RDR bit) is asserted to inform the LH that it can read the amount of data in the RX FIFO (the I2C_BUFSTAT[13-8] RXSTAT bit field). The LH performs a number of data read accesses equal to the I2C_BUFSTAT[13-8] RXSTAT bit field (interrupt or polling mode), or reconfigures the DMA controller with the required value to drain the FIFO.

In controller transmit mode, if the TX FIFO threshold (the I2C_BUF[5-0] TXTRSH bit field value + 1) is not reached, but the amount of data remaining to be written in the TX FIFO is less than the threshold, the transmit draining interrupt (the I2C_IRQSTATUS_RAW[14] XDR bit) is asserted to inform the LH that it can read the amount of data remaining to be written in the TX FIFO (the I2C_BUFSTAT[5-0] TXSTAT bit field). The LH must write the required number of data bytes specified by the I2C_BUFSTAT[5-0] TXSTAT bit field value or reconfigure the DMA controller with the value required to transfer the last bytes to the FIFO.

In controller mode, the LH can alternately not check the values of the I2C_BUFSTAT[5-0] TXSTAT and I2C_BUFSTAT[13-8] RXSTAT bit fields, because it can obtain this information internally (by computing the I2C_CNT[15-0] DATACOUNT bit field value modulo I2C_BUF[13-8] RXTRSH or I2C_BUF[5-0] TXTRSH).

By default, the draining feature is disabled; it can be enabled using the I2C_IRQENABLE_SET[14] XDR_IE or I2C_IRQENABLE_SET[13] RDR_IE bits (default disabled) only for transfers with lengths not equal to the threshold values (I2C_BUF[5-0] TXTRSH bit field value + 1 for the TX threshold or the I2C_BUF[13-8] RXTRSH bit field value + 1 for the RX threshold).

12.2.2.3.8 I2C Noise Filter

The noise filter is used to suppress any noise that is 50 ns or less in case of F/S operation modes, and any noise that is 10 ns or less in case of HS mode operation. The noise filter is always one period of the INTERNAL_CLK clock. This way, for HS mode operation (prescaler bypassed), the filter suppresses spikes of less than 10.4 ns.

For standard mode (for example, the I2C_PSC[7-0] PSC bit field = 4), the maximum width of suppressed spikes is 46.1 ns.

To ensure correct filtering, the prescaler must be programmed accordingly by the I2C*i*.I2C_PSC[7-0] PSC bit field.

12.2.2.3.9 I2C System Test Mode

A system test mode is available for multicontroller I2C module testing. This mode is enabled by setting the I2C_SYSTEST[15] ST_EN bit to 1. When this bit is cleared to 0, the I2C controller is configured in normal operation mode.

In system test mode, the I2C_SYSTEST[13-12] TMODE bit field selects the type of test. Table 12-92 lists the tests available for the multicontroller HS I2C.

Table 12-92. I2C List of Tests

I2C_SYSTEST[13-12] TMODE	Test	Description
00	Functional mode	Normal operation mode
01	Reserved (not used)	
10	Test of SCL serial clock line	The SCL line is driven with a permanent clock as if controlled with the parameters set in the I2C_PSC, I2C_SCLL, and I2C_SCLH registers.
11	Loop-back mode + SCL/SDA I/O	In controll transmit mode only, data transmitted out of the I2C_DATA register (write action) is received in the same I2C_DATA register through an internal path through the FIFO buffers. The interrupt request is normally generated if it is enabled. Moreover, the SCL and SDA are controlled with the I2C_SYSTEST[3-0] bits.

Note

When the I2C_SYSTEST[13-12] TMODE bit field is set to 11, the I2C controller must be configured in I^{2}C F/S (I2C_CON[13-12] OPMODE set to 00) or I^{2}C HS mode (I2C_CON[13-12] OPMODE set to 01).

Note

In normal operation mode (the I2C_SYSTEST[15] ST_EN bit cleared to 0), the I2C_SYSTEST[3-0] bits that control the SCL, SDA lines in system test mode are read-only bits.

In system test mode (the I2C_SYSTEST[15] ST_EN bit set to 1), the I2C_IRQSTATUS_RAW[4] XRDY, I2C_IRQSTATUS_RAW[3] RRDY, I2C_IRQSTATUS_RAW[10] XUDF, I2C_IRQSTATUS_RAW[11] ROVR, I2C_IRQSTATUS_RAW[2] ARDY and I2C_IRQSTATUS_RAW[1] NACK status bits can be set to 1 when the I2C_SYSTEST[11] SSB bit is set to 1. Clearing the I2C_SYSTEST[11] SSB bit to 0 does not clear the I2C_IRQSTATUS_RAW bits to 0. The I2C_IRQSTATUS_RAW bit field can be cleared to 0 only by writing 1 in the corresponding bits.

12.2.2.4 I2C Programming Guide

12.2.2.4.1 I2C Low-Level Programming Models

12.2.2.4.1.1 I2C Programming Model

This section describes the programming model of the multicontroller I2C configured in I^{2}C mode.

12.2.2.4.1.1.1 Main Program

12.2.2.4.1.1.1.1 Configure the Module Before Enabling the I2C Controller

Before enabling the I2C controller, perform the following steps:

1. Enable the functional and interface clocks (see *Module Integration* for details).
2. Program the prescaler to obtain an approximately 12-MHz internal sampling clock by programming the corresponding value in the I2C_PSC[7-0] PSC bit field. This value depends on the frequency of the functional clock (SYS_CLK).
3. Program the I2C_SCLL[7-0] SCLL and I2C_SCLH[7-0] SCLH bit fields to obtain a bit rate of 100 kbps or 400 kbps. These values depend on the internal sampling clock frequency (see Table 12-87).
4. (Optional) Program the I2C_SCLL[15-8] HSSCLL and I2C_SCLH[15-8] HSSCLH bit fields to obtain a bit rate of 400 kbps or 3.4 Mbps (for the second phase of HS mode). These values depend on the internal sampling clock frequency (see Table 12-87).
5. Configure the Own Address of the I2C controller by storing it in the I2C_OA register. Up to four Own Addresses can be programmed in the I2C_OA and I2C_OAx registers (where x = 1, 2, 3) for each I2C controller.

Note

For a 10-bit address, set the corresponding expand Own Address bit in the I2C_CON register.

6. Set the TX threshold (in transmitter mode) and the RX threshold (in receiver mode) by setting the I2C_BUF[5-0] TXTRSH bit field to (TX threshold – 1) and the I2C_BUF[13-8] RXTRSH bit field to (RX threshold – 1), where the TX and RX thresholds are greater than or equal to 1.
7. Take the I2C controller out of reset by setting the I2C_CON[15] I2C_EN bit to 1.

12.2.2.4.1.1.1.2 Initialize the I2C Controller

To initialize the I2C controller, perform the following steps:

1. Configure the I2C_CON register:
    - For controller or target mode, set the I2C_CON[10] MST bit (0: target; 1: controller).
    - For transmitter or receiver mode, set the I2C_CON[9] TRX bit (0: receiver; 1: transmitter).
2. If using an interrupt to transmit and receive data, set the corresponding bit in the I2C_IRQENABLE_SET register to 1 (the I2C_IRQENABLE_SET[4] XRDY_IE bit for the transmit interrupt, the I2C_IRQENABLE_SET[3] RRDY bit for the receive interrupt).

12.2.2.4.1.1.1.3 Configure Target Address and the Data Control Register

In controller mode, configure the target address register by programming the I2C_SA[9-0] SA bit field and the number of data bytes (I^{2}C data payload) associated with the transfer by programming the I2C_CNT[15-0] DCOUNT bit field.

Note

For a 10-bit address, set the I2C_CON[8] XSA bit to 1.

12.2.2.4.1.1.1.4 Initiate a Transfer

Poll the I2C_IRQSTATUS_RAW[12] BB bit. If it is cleared to 0 (bus not busy), configure the I2C_CON[0] STT and I2C_CON[1] STP bits. To initiate a transfer, the I2C_CON[0] STT bit must be set to 1, and it is not mandatory to set the I2C_CON[1] STP bit to 1.

12.2.2.4.1.1.1.5 Receive Data

Poll the I2C_IRQSTATUS_RAW[3] RRDY bit, or use the RRDY interrupt (the I2C_IRQENABLE_SET[3] RRDY_IE bit must be set to 1) to read the receive data in the I2C_DATA register.

If the transfer length does not equal the RX FIFO threshold (the I2C_BUF[13-8] RTRSH bit field + 1), use the draining feature (enable the RDR interrupt by setting the I2C_IRQENABLE_SET[13] RDR_IE bit to 1).

Note

In receive mode only, the I2C_IRQSTATUS_RAW[11] ROVR (receive overrun) bit indicates whether the receiver has experienced overrun. An overrun condition occurs when the shift register and the RX FIFO are full. An overrun condition does not result in data loss; the I2C controller simply holds SCL to low to prevent other bytes from being received.

The I2C_IRQSTATUS_RAW[7] AERR bit is set to 1 when a read access is performed in the I2C_DATA register while the RX FIFO is empty. The corresponding interrupt can be enabled by setting the I2C_IRQENABLE_SET[7] AERR_IE bit to 1.

12.2.2.4.1.1.1.6 Transmit Data

Poll the I2C_IRQSTATUS_RAW[4] XRDY bit, or use the XRDY interrupt (the I2C_IRQENABLE_SET[4] XRDY_IE bit must be set to 1) to write data to the I2C_DATA register.

If the transfer length does not equal the TX FIFO threshold (the I2C_BUF[5-0] TXTRSH bit field + 1), use the draining feature (enable the XDR interrupt by setting the I2C_IRQENABLE_SET[14] XDR_IE bit to 1).

Note

In transmit mode only, the I2C_IRQSTATUS_RAW[10] XUDF bit indicates whether the transmitter has experienced underflow.

In controller transmit mode, underflow occurs when the shift register and the TX FIFO are empty and there are still some bytes to transmit (the value of the I2C_CNT[15-0] DCOUNT bit field is not 0).

In target transmit mode, underflow occurs when the shift register and the TX FIFO are empty and the external I^{2}C controller device still requests data bytes to be read.

The I2C_IRQSTATUS_RAW[7] AERR bit is set to 1 when a write access is performed in the I2C_DATA register while the TX FIFO is full. The corresponding interrupt can be enabled by setting the I2C_IRQENABLE_SET[7] AERR_IE bit to 1.

12.2.2.4.1.1.2 Interrupt Subroutine Sequence

1. Test for arbitration lost (the I2C_IRQSTATUS_RAW[0] AL bit) and resolve accordingly.
2. Test for no acknowledgment (the I2C_IRQSTATUS_RAW[1] NACK bit) and resolve accordingly.
3. Test for register access ready (the I2C_IRQSTATUS_RAW[2] ARDY bit) and resolve accordingly.
4. Test for receive data ready (the I2C_IRQSTATUS_RAW[3] RRDY bit) and resolve accordingly.
5. Test for transmit data ready (the I2C_IRQSTATUS_RAW[4] XRDY bit) and resolve accordingly.
6. Test for general call (the I2C_IRQSTATUS_RAW[5] GC bit) and resolve accordingly.
7. Test for start (S) condition (the I2C_IRQSTATUS_RAW[6] STC bit) and resolve accordingly. For this test, the functional clock must be inactive.
8. Test for access error (the I2C_IRQSTATUS_RAW[7] AERR bit) and resolve accordingly.
9. Test for bus free (the I2C_IRQSTATUS_RAW[8] BF bit) and resolve accordingly.

12.2.2.4.1.1.3 Programming Flow-Diagrams

Figure 12-73 through Figure 12-79 are procedure flow charts for programming the F/S and HS I^{2}C modes.

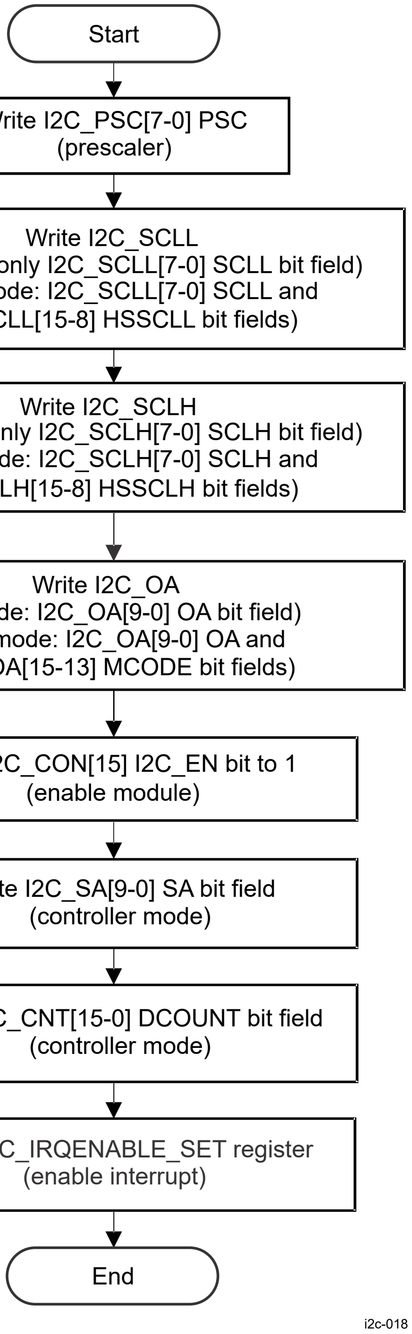
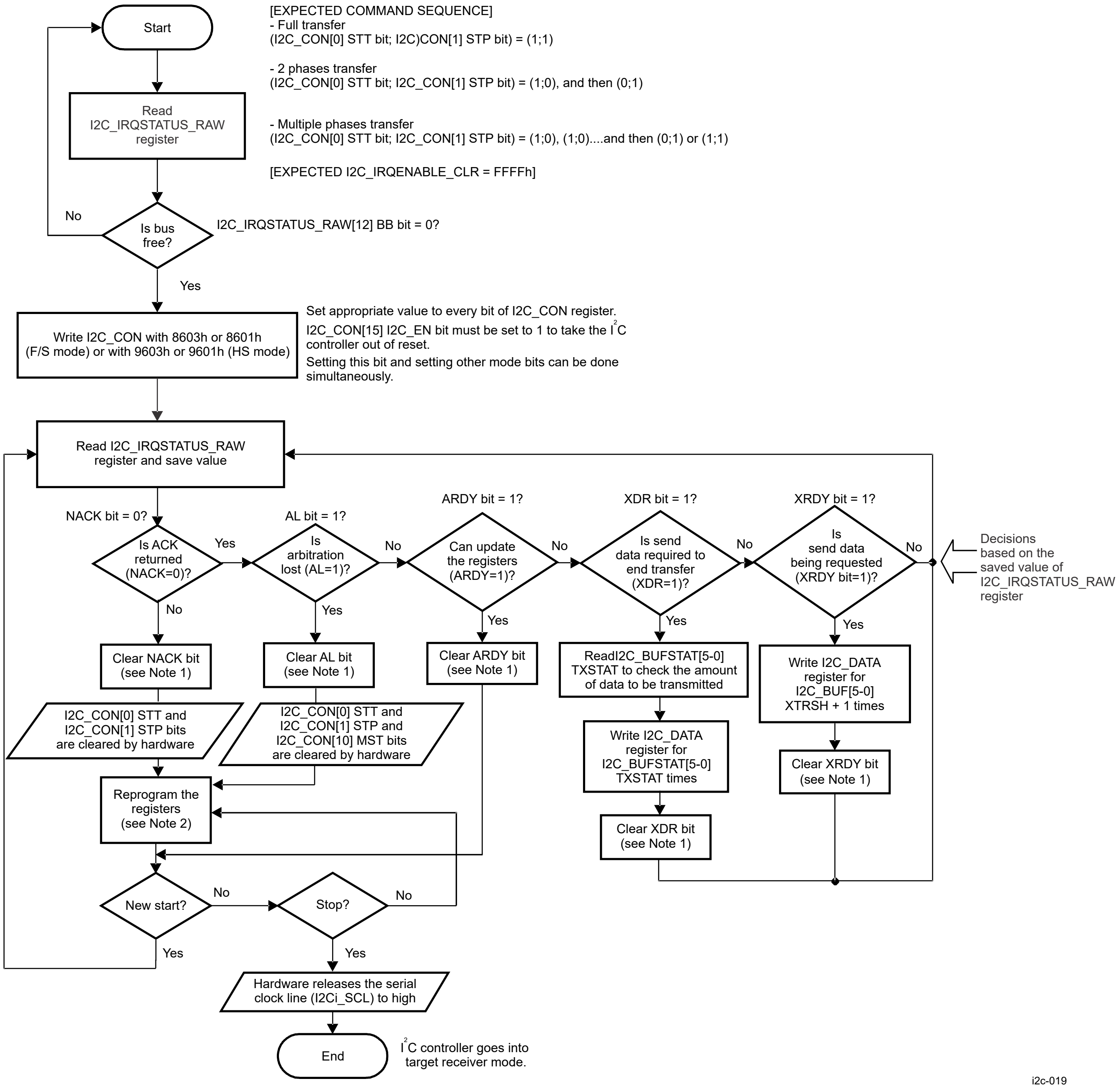


Figure 12-73. I2C Setup Procedure



A. The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

B. Reprogram the registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

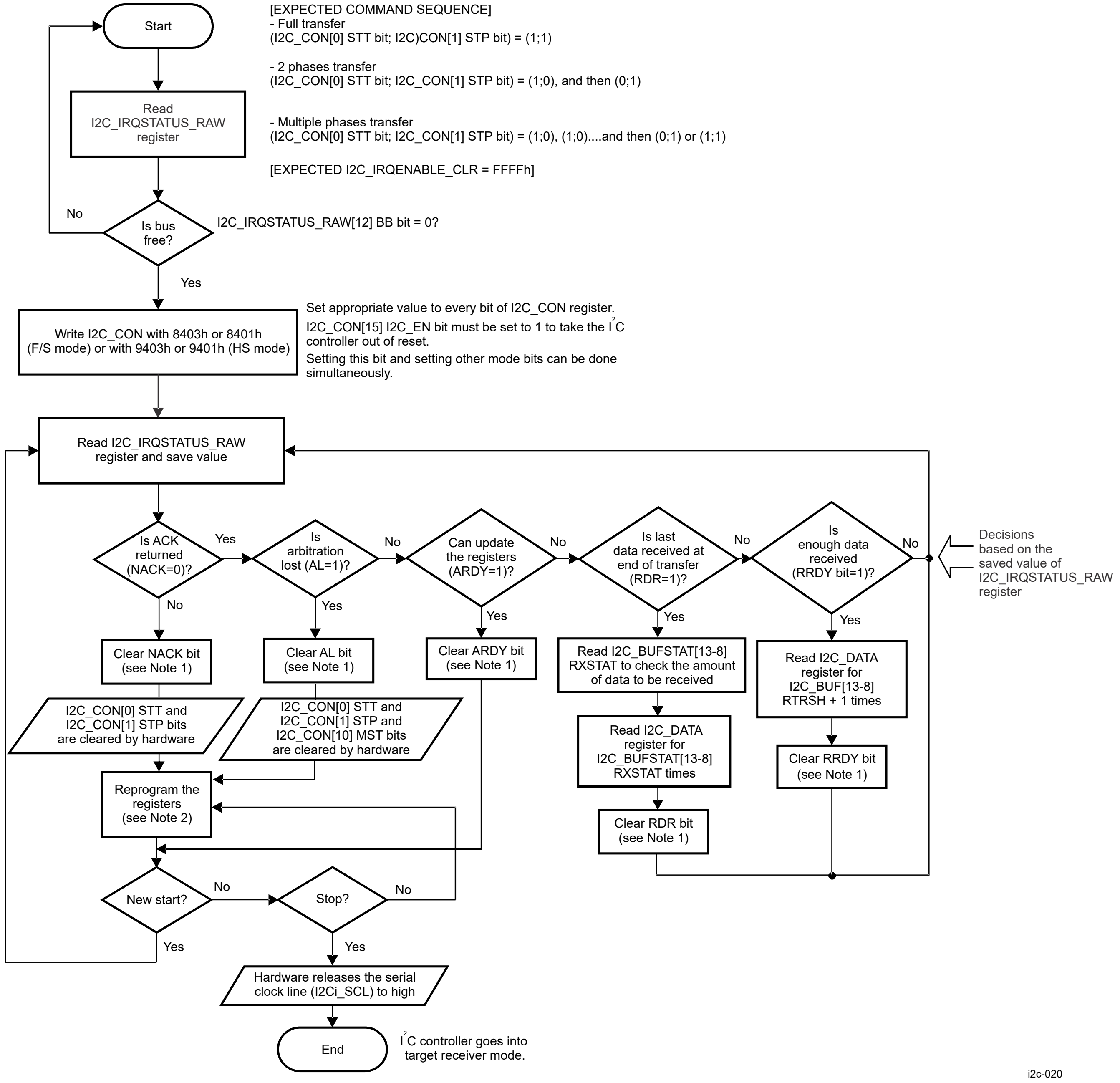
Figure 12-74. I2C Controller Transmitter Mode, Polling Method, in F/S and HS Modes

Note

The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

Note

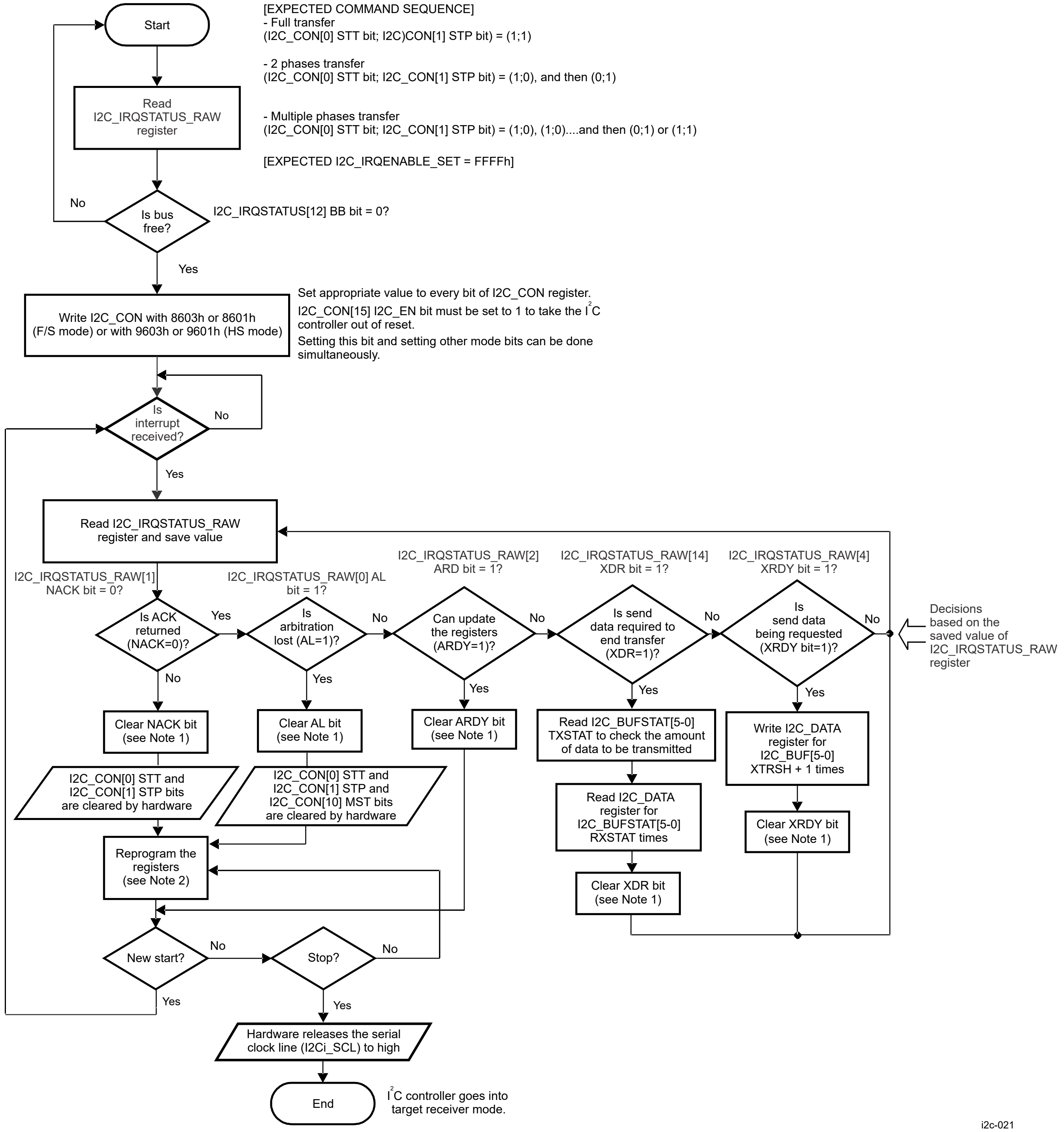
In HS mode, the Sr condition and clock frequency switching are automatically generated by the multicontroller I2C.



A. The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

B. Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

Figure 12-75. I2C Controller Receiver Mode, Polling Method, in F/S and HS Modes



A. The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

B. Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

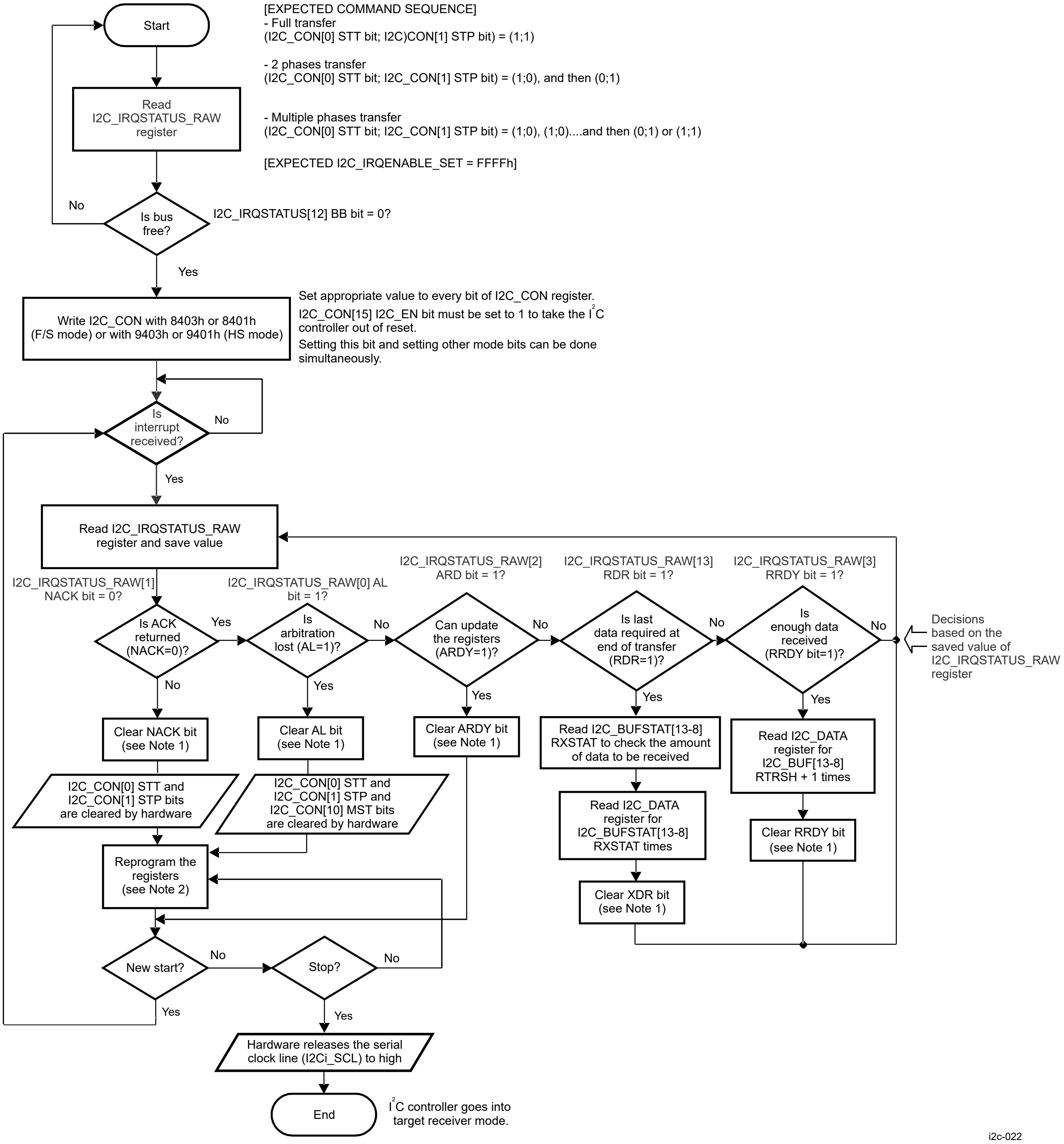
Figure 12-76. I2C Controller Transmitter Mode, Interrupt Method, in F/S and HS Modes

Note

The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

Note

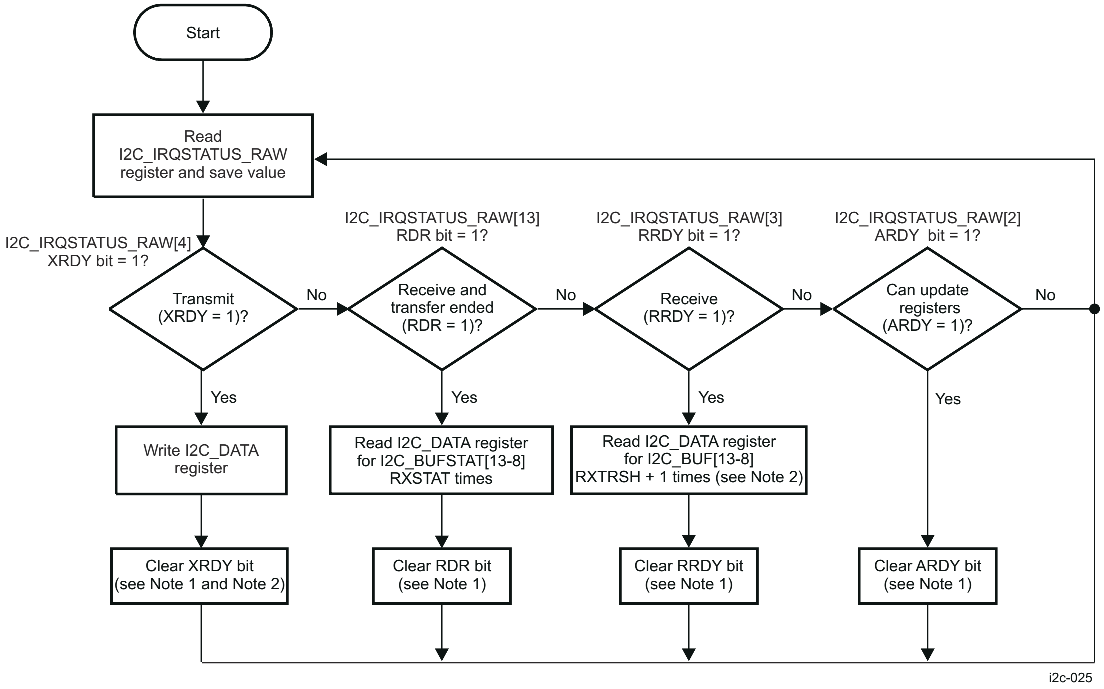
In HS mode, the Sr condition and clock frequency switching are automatically generated by the multicontroller I2C.



A. The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

B. Reprogram registers means: I2C_CON[11] STB and/or I2C_CON[10] MST bit and/or I2C_SA[9-0] SA register and/or I2C_CNT[15-0] DCOUNT register and/or I2C_CON[0] STT bit and/or I2C_CON[1] STP bit.

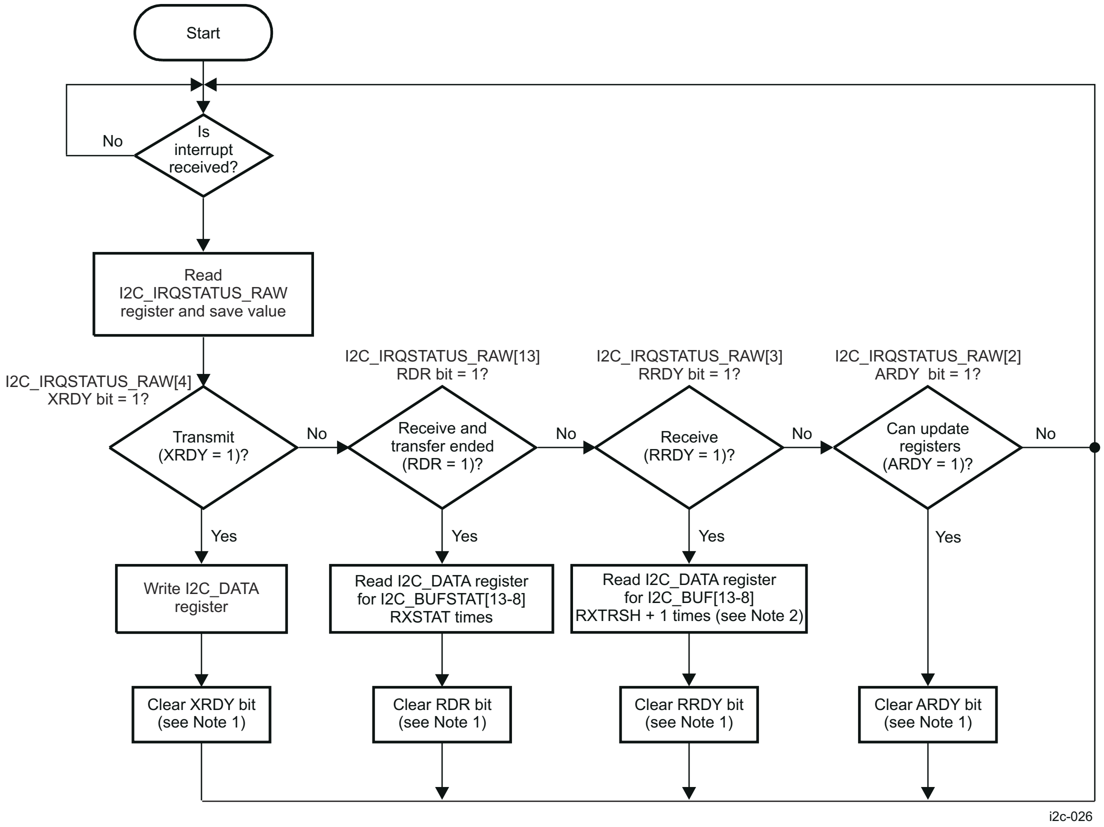
Figure 12-77. I2C Controller Receiver Mode, Interrupt Method, in F/S and HS Modes



A. The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

B. In target transmitter mode, the amount of data requested by the external controller I^{2}C device is unknown; thus, the I2C_BUF[5-0] XTRSH bit field must be configured to 0x0 (TX threshold = 1).

Figure 12-78. I2C Target Transmitter/Receiver Mode, Polling



A. The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2C_IRQSTATUS register.

B. In target transmitter mode, the amount of data requested by the external controller I^2C device is unknown; thus, the I2C_BUF[5-0] XTRSH bit field must be configured to 0x0 (TX threshold = 1).

Figure 12-79. I2C Target Transmitter/Receiver Mode, Interrupt

12.2.3 Multichannel Serial Peripheral Interface (MCSPI)

This section describes the Multichannel Serial Peripheral Interface (MCSPI) modules for the device.

12.2.3.1 MCSPI Overview

The MCSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

Figure 12-80 shows the MCSPI overview.

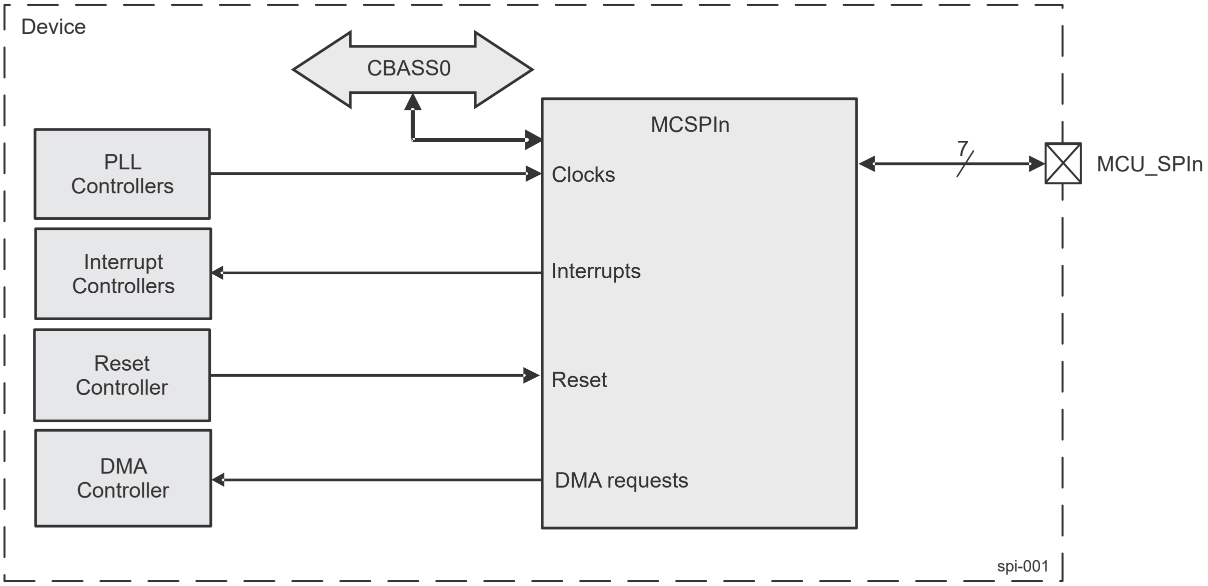


Figure 12-80. MCSPI Overview

n represents a valid instance of MCSPI in a domain.

12.2.3.1.1 MCSPI Features

The MCSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of MCSPI word lengths, ranging from 4 to 32 bits
- Up to four controller channels, or single channel in peripheral mode
- Controller multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - MCSPI configuration per channel. This means, clock definition, polarity enabling and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for MCSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.

12.2.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

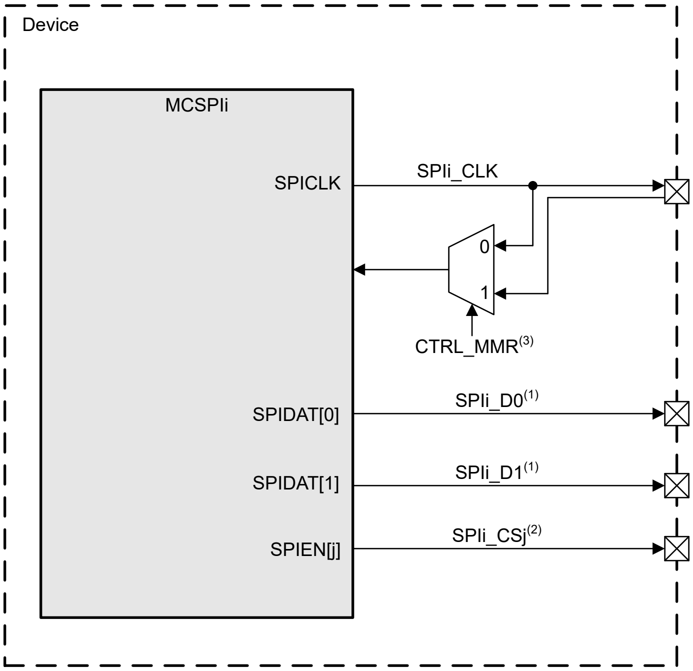
Some features may not be available. See *Module Integration* for more information.

12.2.3.2 MCSPI Environment

This section describes the MCSPI external connections (environment).

12.2.3.2.1 Basic MCSPI Pins for Controller Mode

Figure 12-81 shows all of the MCSPI interface signals in controller mode.



A. Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

B. j = 0 to 3

Note

i represents a MCSPI instance. See the device datasheet for available domains and MCSPI instances.

Figure 12-81. MCSPI Interface Signals in Controller Mode

Table 12-93 describes the MCSPI I/O signals in controller mode.

Table 12-93. MCSPI I/O Signals (Controller Mode)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
			MCU_MCSPIi(5)	
SPICLK	MCU_SPIi(5)_CLK	O	MCSPI Serial clock output for controller mode.	HiZ
SPIDAT[0]	MCU_SPIi(5)_D0	O(3)	MCSPI Data I/O for controller mode.	HiZ
SPIDAT[1]	MCU_SPIi(5)_D1	I(4)	MCSPI Data I/O for controller mode.	HiZ
SPIEN_[n]	MCU_SPIi(5)_CSi	O	MCSPI Chip-select i output for controller mode	HiZ
			MCSPIi(5)	
SPICLK	SPIi(5)_CLK	O	MCSPI Serial clock output for controller mode.	HiZ
SPIDAT[0]	SPIi(5)_D0	O(3)	MCSPI Data I/O for controller mode.	HiZ
SPIDAT[1]	SPIi(5)_D1	I(4)	MCSPI Data I/O for controller mode.	HiZ
SPIEN_[n]	SPIi(5)_CSi	O	MCSPI Chip-select i output for controller mode	HiZ

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH(i)CONF[18] IS and MCSPI_CH(i)CONF[16] DPE0.

(4) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH(i)CONF[18] IS and MCSPI_CH(i)CONF[17] DPE1.

(5) i represents a MCSPI instance. See the device datasheet for available domains and MCSPI instances.

Note

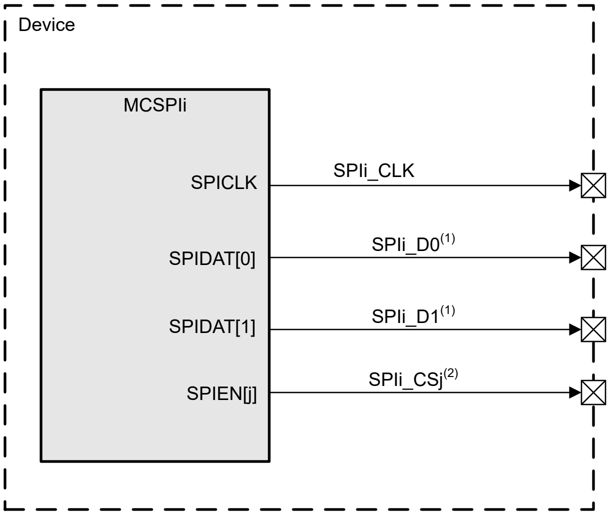
For SPIi(5)_CLK and MCU_SPIi(5)_CLK signals to work properly, the RXACTIVE bit of the appropriate MCU_PADCFG_CTRL_MMR_CFG0_PADCONFIGx/ MAIN_CTRL_MMR_CFG0_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.3.2.2 Basic MCSPI Pins for Peripheral Mode

Figure 12-82 shows all of the MCSPI interface signals in peripheral mode.



A. Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

B. j = 0 to 3

Note

i represents a MCSPI instance. See the device datasheet for available domains and MCSPI instances.

Figure 12-82. MCSPI Interface Signals in Peripheral Mode

Table 12-94 describes the MCSPI I/O signals in peripheral mode.

Table 12-94. MCSPI I/O Signals (Peripheral Mode)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(1)
			MCU_MCSPI[1-0]	
SPICLK	MCU_SPIi(5)_CLK	I	MCSPI serial clock input for peripheral mode.	HiZ
SPIDAT[0]	MCU_SPIi(5)_D0	I(2)	MCSPI Data I/O for peripheral mode.	HiZ
SPIDAT[1]	MCU_SPIi(5)_D1	O(3)	MCSPI Data I/O for peripheral mode.	HiZ
SPIEN_[n]	MCU_SPIi(5)_CSi	I(4)	MCSPI chip-select i input for peripheral mode.	HiZ
			MCSPI[4-0]	
SPICLK	SPIi(5)_CLK	I	MCSPI serial clock input for peripheral mode.	HiZ
SPIDAT[0]	SPIi(5)_D0	I(2)	MCSPI Data I/O for peripheral mode.	HiZ

Table 12-94. MCSPI I/O Signals (Peripheral Mode) (continued)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[1]
SPIDAT[1]	SPIi[5]_D1	O[3]	MCSPI Data I/O for peripheral mode.	HiZ
SPIEN_[n]	SPIi[5]_CSi	I[4]	MCSPI chip-select i input for peripheral mode.	HiZ

(1) HiZ = High Impedance

(2) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH(i)CONF[18] IS and MCSPI_CH(i)CONF[16] DPE0.

(3) Example configuration only. Can be configured either as input or as output depending on MCSPI_CH(i)CONF[18] IS and MCSPI_CH(i)CONF[17] DPE1.

(4) The chip-select input in peripheral mode can be selected through the MCSPI_CH(i)CONF[22-21] SPIENSLV bit field.

(5) i represents a MCSPI instance. See the device datasheet for available domains and MCSPI instances.

Note

For SPI[4-0]_CLK and MCU_SPI[1-0]_CLK signals to work properly, the RXACTIVE bit of the appropriate CTRLMMR_MCU_PADCONFIGx/ CTRLMMR_PADCONFIGy registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.3.2.3 MCSPI Protocol and Data Format

The synchronous MCSPI protocol allows a controller device to initiate serial data transfers to a peripheral device. A peripheral select line (SPIEN_[n]) allows selection of an individual peripheral MCSPI device. Peripheral devices that are not selected do not interfere with MCSPI bus activities.

MCSPI offers the flexibility to modify the following parameters to adapt to the device features:

- Word length

  MCSPI supports any MCSPI word ranging from 4 bits to 32 bits long (the MCSPI_CH(i)CONF[11-7] WL bit field).

  MCSPI word length can be changed between transmissions to allow the controller device to communicate with peripheral devices that have different requirements.
- MCSPI enable (SPIEN_[n], for channel i)

  The polarity of the MCSPI enable signals is programmable (the MCSPI_CH(i)CONF[6] EPOL bit). SPIEN_[n] signals can be active high or low.

  Assertion of the SPIEN_[n] signals is programmable and can be done manually or automatically. The manual assertion mode is available in single controller mode only. SPIEN_[n] can be kept active between words with the MCSPI_CH(i)CONF[20] FORCE bit.

  Two consecutive words for two different peripheral devices can go along with active SPIEN_[n] signals with different polarity.
- Programmable start-bit

  In start-bit mode a start-bit is added before the MCSPI word length to indicate how the next MCSPI word must be handled. The start-bit is enabled by setting the MCSPI_CH(i)CONF[23] SBE bit to 1. The MCSPI_CH(i)CONF[24] SBPOL bit defines the polarity of the start-bit.
- Programmable MCSPI clock
  - Bit rate

    In controller mode, the baud rate of the MCSPI serial clock is programmable using the 50-MHz reference clock (from the device clock management module). Table 12-95 lists the SPICLK bit rates obtained for data transfer when programming the clock divider (the MCSPI_CH(i)CONF[5-2] CLKD bit field).

Table 12-95. MCSPI Controller Clock Rates

Divider	Clock Rate
1	50 MHz(1)
2	25 MHz(1)
4	12.5 MHz
8	6.25 MHz
16	3.125 MHz
32	1.5625 MHz
64	781.25 kHz
128	390.625 kHz
256	~195 kHz
512	~97.7 kHz
1024	~48.8 kHz
2048	~24.4 kHz
4096	~12.2 kHz

(1) These frequencies are not necessarily supported by all MCSPI modules. For more information, see the *Timing Requirements*

and Switching Characteristics chapter in the device-specific Datasheet.

– Polarity and phase

The polarity (the MCSPI_CH(i)CONF[1] POL bit) and the phase (the MCSPI_CH(i)CONF[0] PHA bit) of the MCSPI serial clock (SPICLK) are configurable to offer four combinations. Software selects the right combination, depending on the device. See Table 12-96 and Figure 12-83.

Data transfer is not required to update polarity, but it is configuration specific.

- In multi-controller mode POL/PHA is only updated to a channel's settings when a transaction is necessary on that channel.
- In single-controller mode POL/PHA is only updated on CS assertion (assuming channel already enabled), which is now SW-controlled using the FORCE bitfield.

Table 12-96. Phase and Polarity Combinations

Polarity (POL)	Phase (PHA)	MCSPI Mode	Description
0	0	Mode 0	SPICLK is inactive low and sampling occurs at the rising edge.
0	1	Mode 1	SPICLK is inactive low and sampling occurs at the falling edge.
1	0	Mode 2	SPICLK is inactive high and sampling occurs at the falling edge.
1	1	Mode 3	SPICLK is inactive high and sampling occurs at the rising edge.

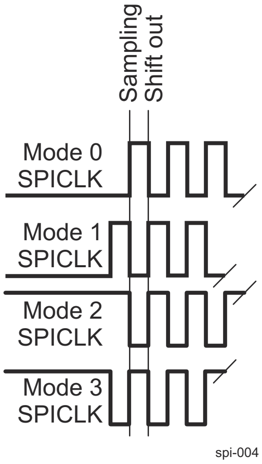


Figure 12-83. Phase and Polarity Combinations

12.2.3.2.3.1 Transfer Format

In controller and peripheral modes, the MCSPI drives the data lines when SPIEN_[n] is asserted.

Each word is transmitted starting with the most-significant bit (MSB).

This section explains the two cases of data transmission determined by the clock phase (PHA) and the type of data transmission using a start-bit (SBE) called the start-bit mode:

- Transmission in mode 0 and mode 2 (PHA = 0)

  When PHA = 0, the first bit of the MCSPI word to transmit (on the controller or the peripheral data output pin) is valid one-half cycle of SPICLK after the assertion of SPIEN_[n].

  Therefore, the first edge of the SPICLK line is used by the controller to sample the first data bit sent by the peripheral. On the same edge, the first data bit sent by the controller is sampled by the peripheral.

  On the next SPICLK edge, the received data bit is shifted into the receive shift register and a new data bit is transmitted on the serial data line.

  This process continues for a number of pulses on the SPICLK line defined by the MCSPI word length programmed in the controller device, with data being latched on odd-numbered edges and shifted on even-numbered edges, see Figure 12-84.

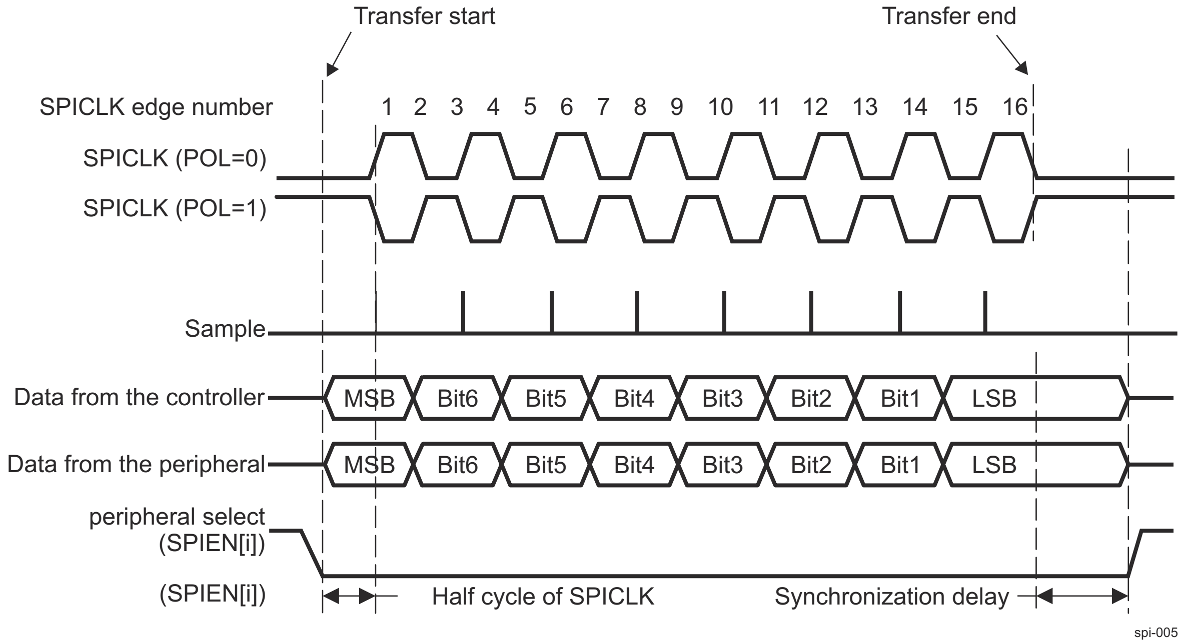


Figure 12-84. Full-Duplex Transfer Format With PHA = 0

- Transmission in mode 1 and mode 3 (PHA = 1)

  When PHA = 1, the first bit of the MCSPI word to transmit (on the controller or the peripheral data output pin) is valid on the following SPICLK edge (one-half cycle later). This is the sampling edge for the controller and peripheral. A synchronization delay is added between the activation of SPIEN_[n] and the first SPICLK edge.

  The received data bit is shifted into the shift register on the third SPICLK edge.

  This process continues for a number of pulses on the SPICLK line defined by the MCSPI word length programmed in the controller device, with data being latched on even-numbered edges and shifted on odd-numbered edges.

Note

The minimum synchronization delay is one cycle of SPICLK, if the frequency of SPICLK equals the frequency of MCSPI_FCLK (MCSPI functional clock) in controller mode. The minimum synchronization delay is one-half cycle of SPICLK, if the frequency of SPICLK is lower than the frequency of MCSPI_FCLK in the controller and peripheral modes.

- Transmission with a start-bit (SBE = 1)

  When the MCSPI_CH(i)CONF[23] SBE bit is set to 1, a start-bit is added before the MSB to indicate whether the next MCSPI word must be handled as a command or as data.

  Figure 12-85 shows an example of a data transfer with an extra start-bit.

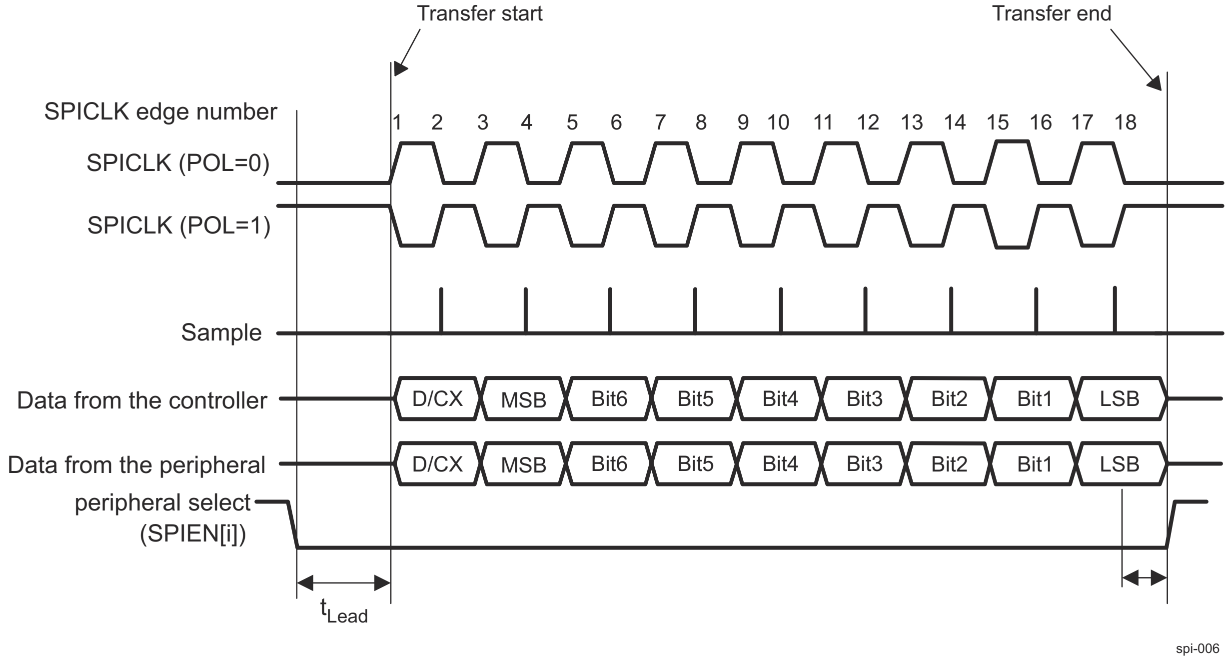
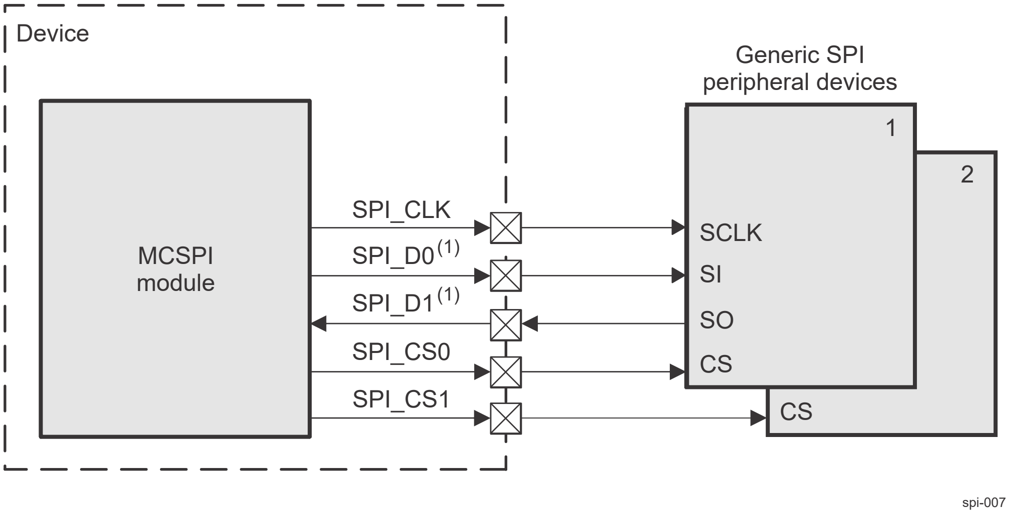


Figure 12-85. Extended MCSPI Transfer With a Start-Bit (SBE = 1)

12.2.3.2.4 MCSPI in Controller Mode

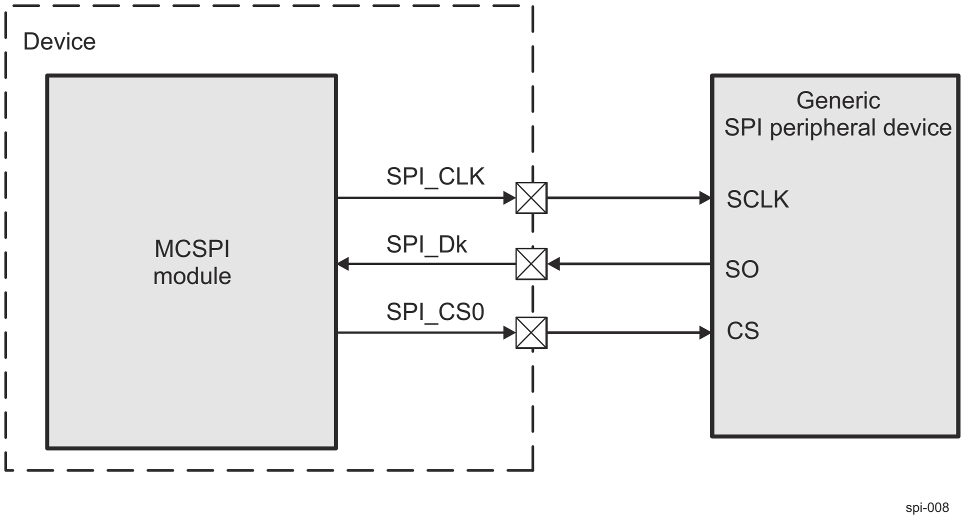
Figure 12-86 shows a case in controller mode (full-duplex) where the MCSPI module is connected with two peripheral devices.



A. Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-86. MCSPI Controller Mode (Full Duplex)

Figure 12-87 shows the controller single mode, which can also be configured in receive-only mode.



k = 0 or 1 depending on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

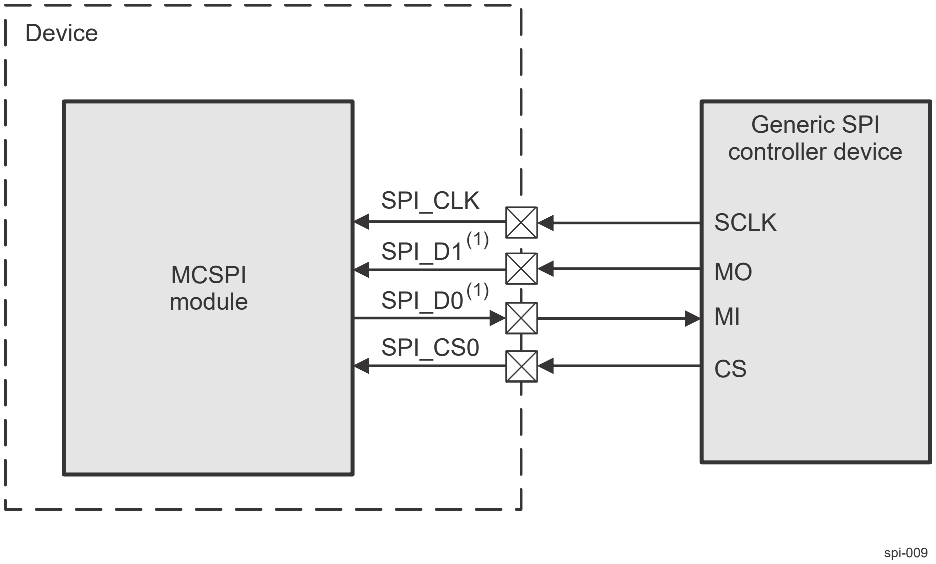
Figure 12-87. MCSPI Controller Single Mode (Receive Only)

12.2.3.2.5 MCSPI in Peripheral Mode

Figure 12-88 shows a case in peripheral mode (full-duplex).

Note

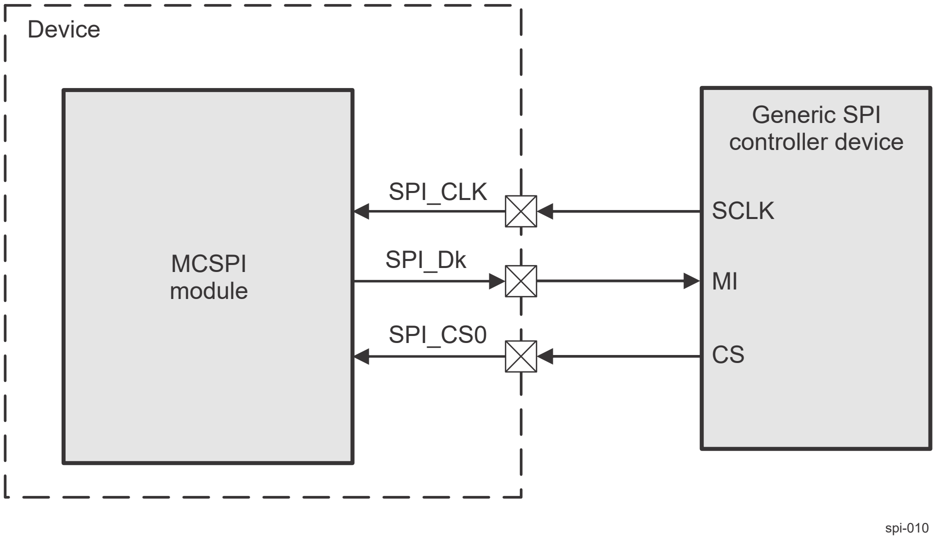
Only channel 0 can be configured as peripheral, but the chip-enable signal can be connected to any SPIEN_[n] pin and then rerouted internally to channel 0 (the MCSPI_CH0CONF[22-21] SPIENSLV bit field). For more information, see Section 12.2.3.4.4, *MCSPI Peripheral Mode*.



A. Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-88. MCSPI Peripheral Mode (Full Duplex)

Figure 12-89 shows the peripheral single mode, which can also be configured in transmit-only mode.



k = 0 or 1 depending on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-89. MCSPI Peripheral Single Mode (Transmit Only)

12.2.3.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.2.3.4 MCSPI Functional Description

12.2.3.4.1 MCSPI Block Diagram

Figure 12-90 shows the MCSPI module.

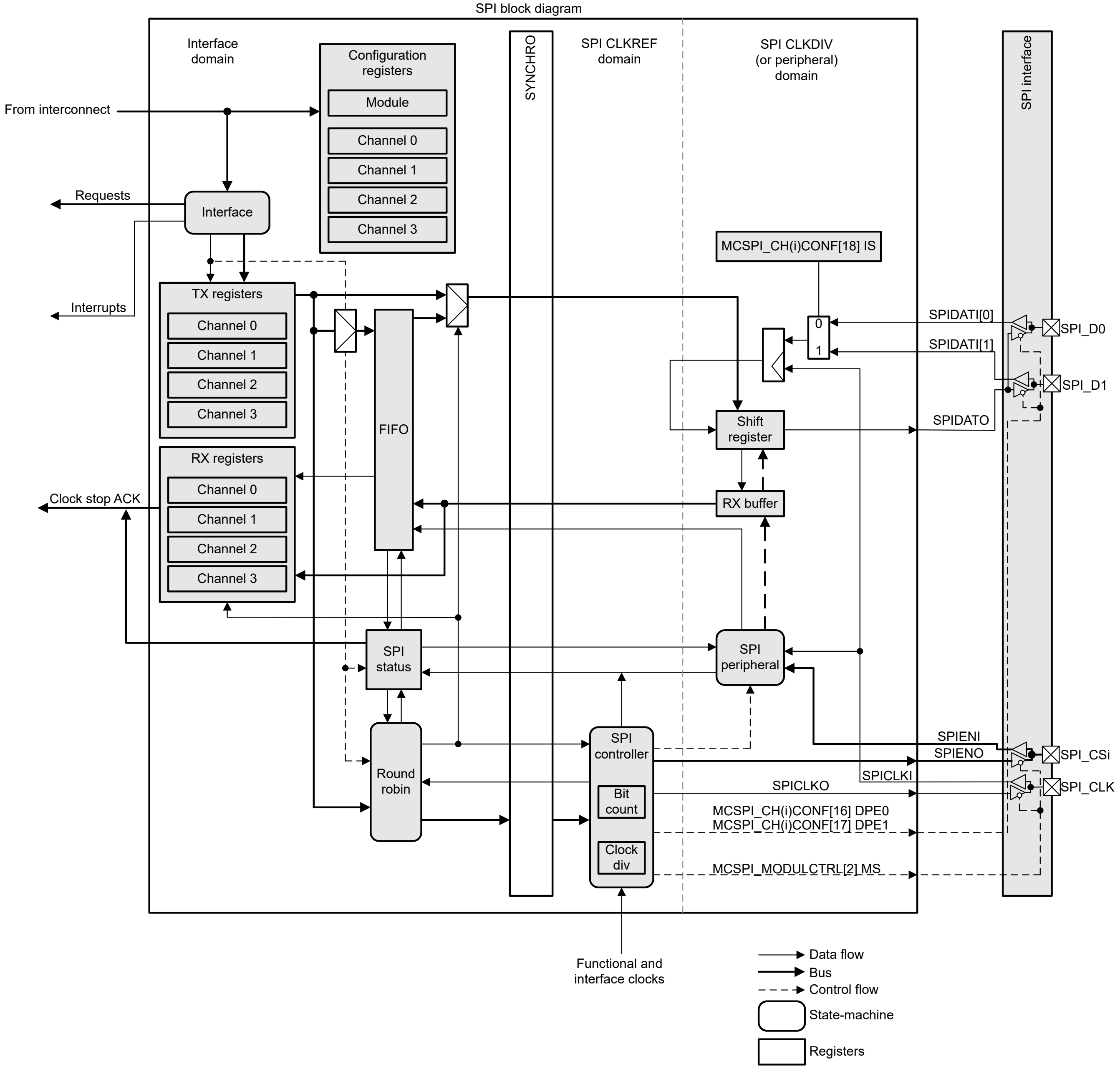


Figure 12-90. MCSPI Block Diagram

12.2.3.4.2 MCSPI Reset

The MCSPI module can be reset either by hardware or by software reset. All configuration registers and all state machines are reset by the hardware reset signal (MCSPI_RST). MCSPI can be reset by software through the MCSPI_SYSCONFIG[1] SOFTRESET bit. This bit has the same impact on the module as the hardware reset signal. The only exception is that the MCSPI_SYSCONFIG register is not affected by that software reset.

12.2.3.4.3 MCSPI Controller Mode

12.2.3.4.3.1 Controller Mode Features

The MCSPI controller mode supports multichannel communication with up to four independent MCSPI communication channel contexts. The MCSPI initiates a data transfer on the data lines (SPIDAT[0] and SPIDAT[1]) and generates clock (SPICLK) and control (SPIEN_[n]) signals.

Connected to multiple external devices, the MCSPI exchanges data with one MCSPI device at a time through two main modes (available in peripheral mode):

- Two-data-pins interface mode (transmit-and-receive mode for full-duplex transmission)
- Single-data-pin interface mode (recommended for half-duplex transmission)

Note

There is a fixed chip select line allocation in multichannel controller mode. Channel i is mapped to SPIEN_[n].

Two DMA request events (read and write) allow synchronized accesses of the DMA controller with the activity of MCSPI.

Three interrupt events can be used for data transmission and reception in controller mode (for more information about interrupts, see Section 12.2.3.4.7.1, *Interrupt Events in Controller Mode*).

12.2.3.4.3.2 Controller Transmit-and-Receive Mode (Full Duplex)

In full-duplex transmission, data is transmitted (shifted out serially on SPIDAT[0]) and received (shifted in serially on SPIDAT[1]) simultaneously on separate data lines.

The controller transmit-and-receive mode is programmable per channel (the MCSPI_CH(i)CONF[13-12] TRM bit field).

Channel access to the shift registers for transmission/reception is based on the MCSPI_TXi transmitter register state, the MCSPI_RXi receiver register state, and round-robin arbitration.

Channels that meet the following rules are included in the round-robin list of active channels scheduled for transmission and/or reception. The arbiter skips channels that do not meet the rules and searches in the rotation for the next enabled channel.

- Rule 1: Only enabled channels (the MCSPI_CH(i)CTRL[0] EN bit) can be scheduled for transmission and/or reception.
- Rule 2: If its MCSPI_TXi transmitter register is not empty (the MCSPI_CH(i)STAT[1] TXS bit), an enabled channel can be scheduled when the shift register is assigned. If the MCSPI_TXi register is empty when the shift register is assigned, the TXx_UNDERFLOW event is activated, and the next enabled channel with new data to transmit is scheduled (see also transmit-only mode).
- Rule 3: An enabled channel can be scheduled if its receive register is not full (the MCSPI_CH(i)STAT[0] RXS bit) when the shift register is assigned (see also receive-only mode). Therefore, the MCSPI_RXi register cannot be overwritten. The MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set to this mode.

When MCSPI word transfer completes (the MCSPI_CH(i)STAT[2] EOT bit is set), the updated MCSPI_TXi register of the next scheduled channel is loaded into the shift register. The serialization (transmit-and-receive) starts depending on the channel communication configuration. When serialization completes, the received data transfers to the channel receive register.

The serial clock (SPICLK) synchronizes shifting and sampling of the information on the two serial data lines (SPIDAT[0] and SPIDAT[1]). Each time a bit transfers out from the controller, 1 bit transfers in from the peripheral.

Figure 12-91 shows an example of a full-duplex system with a controller device on the left and a peripheral device on the right. After eight cycles of the serial clock SPICLK, WordA transfers from the controller to the peripheral. At the same time, WordB transfers from the peripheral to the controller.

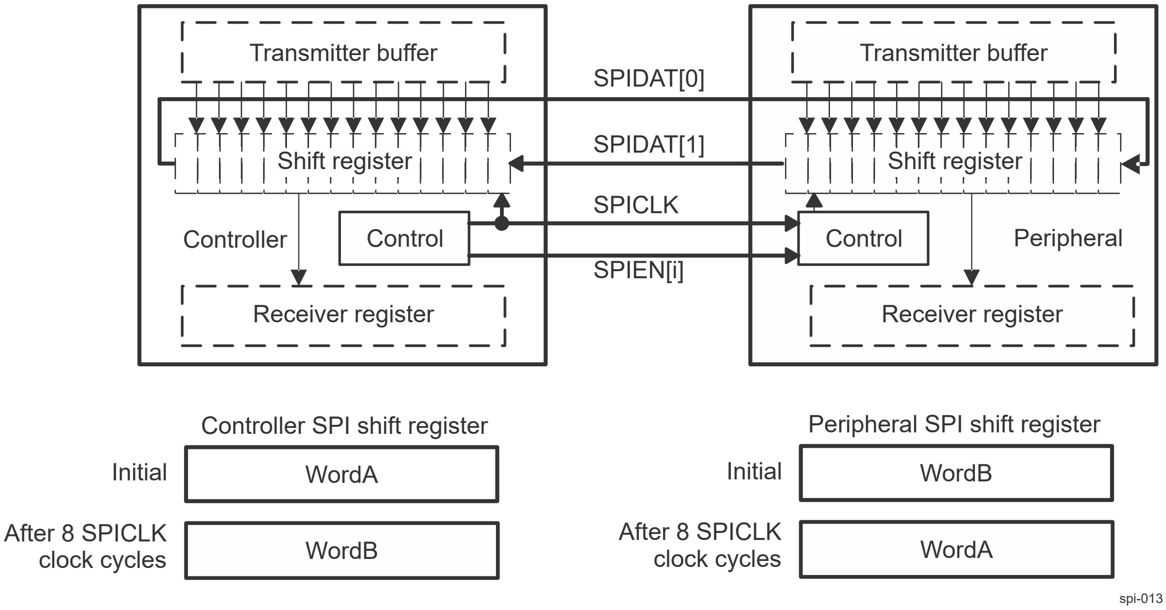


Figure 12-91. MCSPI Full-Duplex Transmission (Example)

12.2.3.4.3.3 Controller Transmit-Only Mode (Half Duplex)

The controller transmit-only mode prevents the processor from reading the MCSPI_RXi register (minimizing data movement) when only transmission is meaningful.

The controller transmit-only mode is programmable per channel (the MCSPI_CH(i)CONF[13-12] TRM bit field). Transmission starts only after data is loaded into the MCSPI_TXi register.

Rule 1 and Rule 2, defined in Section 12.2.3.4.3.2, apply in this mode.

Rule 3, defined in Section 12.2.3.4.3.2, does not apply.

In controller transmit-only mode, the MCSPI_RXi register state FULL does not prevent transmission and the MCSPI_RXi register is always overwritten with the new MCSPI word. This event is not significant when only transmission is meaningful. Thus, the RX0_OVERFLOW bit in the MCSPI_IRQSTATUS register is never set in this mode.

The hardware automatically disables the RX_FULL interrupt and the DMA read requests.

The transfer status is given by the MCSPI_CH(i)STAT[2] EOT bit.

12.2.3.4.3.4 Controller Receive-Only Mode (Half Duplex)

The controller receive mode prevents the processor from refilling the MCSPI_TXi register (minimizing data movement) when only reception is meaningful.

The controller receive mode is programmable per channel (the MCSPI_CH(i)CONF[13-12] TRM bit field).

The controller receive-only mode enables channel scheduling only on the empty state of the MCSPI_RXi register.

Rule 1 and Rule 3, defined in Section 12.2.3.4.3.2, apply in this mode.

Rule 2, defined in Section 12.2.3.4.3.2, does not apply.

In the controller receive-only mode, software must write dummy data to the MCSPI_TXi register. Only one dummy write is enough to receive any number of words from the peripheral. Software must ensure that the MCSPI_TXi register is always full (the TXi_EMPTY bits of MCSPI_IRQSTATUS) when receiving. The content of the MCSPI_TXi register is always loaded into the shift register when the shift register is assigned. After writing the dummy data to the MCSPI_TXi register, the TXi_EMPTY and TXi_UNDERFLOW bits in the MCSPI_IRQSTATUS register are never set in receive-only mode.

The MCSPI_CH(i)STAT[2] EOT bit gives the status of serialization. The RXi_FULL bits of the MCSPI_IRQSTATUS register are set when received data is loaded from the shift register to the corresponding MCSPI_RXi register. The MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

12.2.3.4.3.5 Single-Channel Controller Mode

When the MCSPI is configured as a controller device with a single enabled channel (MCSPI_MODULCTRL[2] MS = 0 and MCSPI_MODULCTRL[0] SINGLE = 1), the assertion of the SPIEN_[n] signal is optional depending on device connected to the controller. In 3-pin mode (MCSPI_MODULCTRL[1] PIN34 = 1) the controller starts transmitting data when a write to the MCSPI_TXi register or the FIFO is performed. In 4-pin mode (MCSPI_MODULCTRL[1] PIN34 = 0) the assertion and de-assertion of SPIEN_[n] is controlled by software using the MCSPI_CH(i)CONF[20] FORCE bit.

12.2.3.4.3.5.1 Programming Tips When Switching to Another Channel

When a single channel is enabled and data transfer is ongoing:

- Wait for the MCSPI word transfer to complete (wait until the MCSPI_CH(i)STAT[2] EOT bit is set to 1) before disabling the current channel and enabling a different channel.
- Disable the current channel, and then enable the other channel.

12.2.3.4.3.5.2 Force SPIEN_[n] Mode

Continuous transfers are allowed manually by keeping the SPIEN_[n] signal active for successive MCSPI words transfer. Several sequences (configuration/enable/disable of the channel) can be run without deactivating the SPIEN_[n] line. This mode is supported by all channels and any controller sequence can be used (transmit-receive, transmit-only, receive-only).

Keeping the SPIEN_[n] active mode is supported when:

- A single channel is used (with the MCSPI_MODULCTRL[0] SINGLE bit set to 1).
- Transfer parameters are loaded in the configuration register of the appropriate channel (MCSPI_CH(i)CONF).

  The state of the SPIEN_[n] signal is programmable:
  - Writing 1 to the MCSPI_CH(i)CONF[20] FORCE bit drives the SPIEN_[n] line high when the MCSPI_CH(i)CONF[6] EPOL bit is set to 0. SPIEN_[n] is driven low when the MCSPI_CH(i)CONF[6] EPOL bit is set to 1.
  - Writing 0 to the MCSPI_CH(i)CONF[20] FORCE bit drives the SPIEN_[n] line low when the MCSPI_CH(i)CONF[6] EPOL bit is set to 0. SPIEN_[n] is driven high when the MCSPI_CH(i)CONF[6] EPOL bit is set to 1.
- A single channel is enabled (the MCSPI_CH(i)CTRL[0] EN bit is set to 1). The first enabled channel activates the SPIEN_[n] line.

When the channel is enabled, the SPIEN_[n] signal activates with the programmed polarity. As in the multichannel controller mode, the transfer start depends on the status of the MCSPI_TXi register (the MCSPI_CH(i)STAT[1] TXS bit), the status of the MCSPI_RXi register (the MCSPI_CH(i)STAT[1] RXS bit), and the defined mode (the MCSPI_CH(i)CONF[13-12] TRM bit field) of the channel enabled.

The MCSPI_CH(i)STAT[2] EOT bit gives the transfer status of each MCSPI word. The RXx_FULL bit in the MCSPI_IRQSTATUS register is set when received data is loaded from the shift register to the MCSPI_RXi register.

A change in the configuration parameters is propagated directly on the MCSPI interface. If the SPIEN_[n] signal is activated, ensure that the configuration is changed only between MCSPI words to avoid corrupting the current transfer.

Note

To avoid data corruption, SPIEN_[n] polarity and SPICLK phase and SPICLK polarity must not be modified when the SPIEN_[n] signal is activated.

A delay between MCSPI words that requires the connected MCSPI peripheral device to switch from one configuration to another (for instance, from transmit-only to receive-only) must be handled by software.

At the end of the last MCSPI word, the channel must be deactivated (the MCSPI_CH(i)CTRL[0] EN bit set to 0) and SPIEN_[n] can be forced to its INACTIVE state using the MCSPI_CH(i)CONF[20] FORCE bit.

Figure 12-92 and Figure 12-93 show successive transfers with SPIEN_[n] maintained active low with a different configuration for each MCSPI word in single-data-pin and dual-data-pin interface modes, respectively.

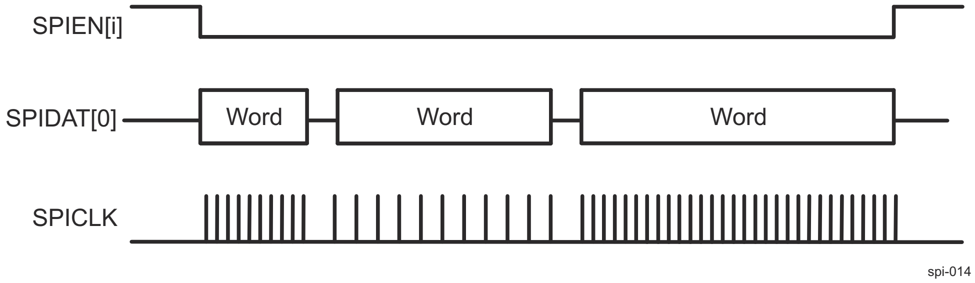


Figure 12-92. Continuous Transfers With SPIEN_[n] Maintained Active (Single-Data-Pin Interface Mode)

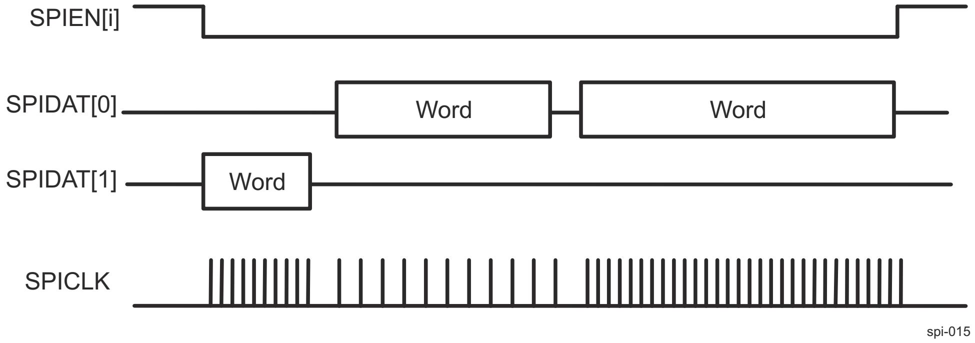


Figure 12-93. Continuous Transfers With SPIEN_[n] Maintained Active (Dual-Data-Pin Interface Mode)

Note

The SPIEN_[n] signal can be maintained active via software using the MCSPI_CH(i)CONF[20] FORCE bit only when the MCSPI_MODULCTRL[0] SINGLE bit is set to 0x1.

12.2.3.4.3.5.3 Turbo Mode

Turbo mode improves the throughput of the MCSPI interface when a single channel is enabled by allowing transfers until the shift register and the MCSPI_RXi register are full. Turbo mode is time saving when a transfer exceeds two words. This mode is programmable per channel (through the MCSPI_CH(i)CONF[9] TURBO bit).

When several channels are enabled, the TURBO bit has no effect and the channel access to the shift registers remains as previously described.

In turbo mode, Rule 1 and Rule 2 apply, but Rule 3 does not (see Section 12.2.3.4.3.2, *Controller Transmit-and-Receive Mode (Full Duplex)*). An enabled channel can be scheduled if its receive register is full (the MCSPI_CH(i)STAT[0] RXS bit) when the shift-register is assigned until the shift register is full.

The MCSPI_RXi register cannot be overwritten in turbo mode. Consequently, the MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

12.2.3.4.3.6 Start-Bit Mode

In start-bit mode, an extended bit is added before the MCSPI word to indicate whether the next MCSPI word must be handled as a command or as data. This feature is available only in controller mode. Start-bit mode cannot be used at the same time as turbo mode and/or force SPIEN_[n] mode. In this case, only one channel can be used; round-robin arbitration is not possible.

This mode is programmable per channel by setting the MCSPI_CH(i)CONF[23] SBE bit to 1. The polarity of the extended bit is programmable per channel. When the MCSPI_CH(i)CONF[24] SBPOL bit is set to 0, the MCSPI word must be handled as a command. When the MCSPI_CH(i)CONF[24] SBPOL bit is set to 1, the MCSPI word must be handled as data. Moreover, start-bit polarity can be changed dynamically during start-bit transfer without disabling the channel for reconfiguration; in this case, users must configure the MCSPI_CH(i)CONF[24] SBPOL bit before writing the MCSPI word to be transmitted to the TX register.

12.2.3.4.3.7 Chip-Select Timing Control

The chip-select (CS) timing control is available only in controller mode with automatic CS generation (the MCSPI_MODULCTRL[0] SINGLE bit set to 0) to add a programmable delay between CS assertion and first clock edge, or CS removal and last clock edge. This option is available only in 4-pin mode when MCSPI_MODULCTRL[1] PIN34 set to 0.

This mode is programmable per channel through the MCSPI_CH(i)CONF[26-25] TCS0 bit field.

Figure 12-94 shows the CS SPIEN timing controls.

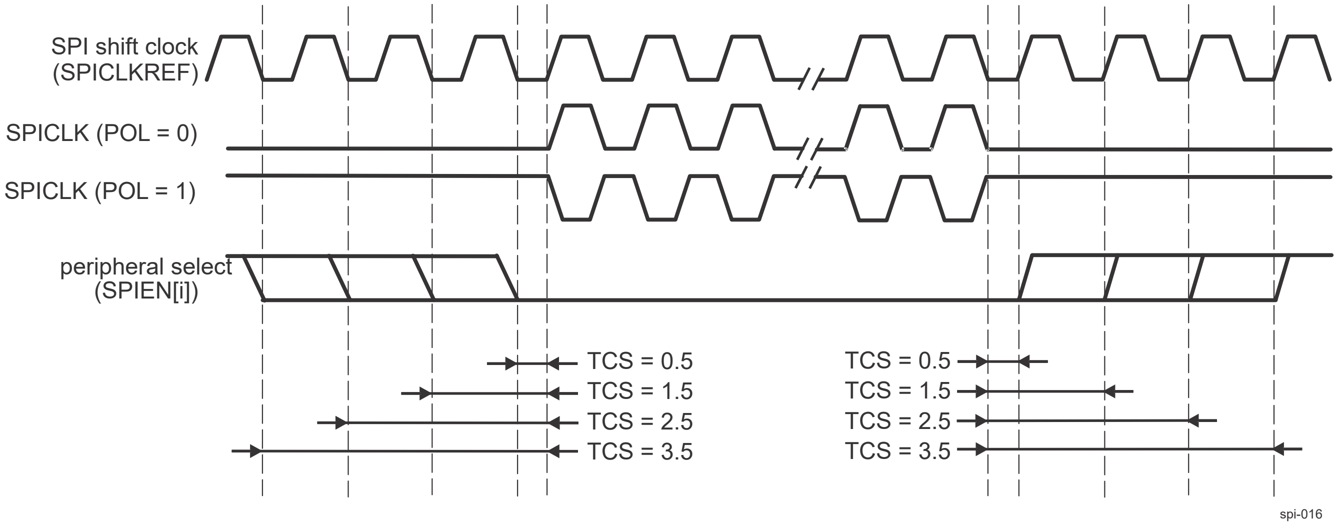


Figure 12-94. CS SPIEN Timing Controls

Note

Because of the design implementation for transfers using a clock divider ratio set to 1 (clock bypassed), a half cycle must be added to the value between CS assertion and the first clock edge with PHA = 1 or between CS removal and the last clock edge with PHA = 0.

12.2.3.4.3.8 Programmable MCSPI Clock (SPICLK)

In controller mode, the baud rate of the MCSPI serial clock is programmable.

An internal reference clock, SPICLKREF, is used as input of a programmable divider (the MCSPI_CH(i)CONF[5-2] CLKD bit field) to generate the bit rate of the serial output clock SPICLK. Table 12-97 summarizes the supported divisor values.

Table 12-97. MCSPI Controller Clock Rates

Divider	Clock Rate
1	50 MHz(1)
2	25 MHz(1)
4	12.5 MHz
8	6.25 MHz
16	3.125 MHz
32	1.5625 MHz

Table 12-97. MCSPI Controller Clock Rates (continued)

Divider	Clock Rate
64	781.25 kHz
128	~390 kHz
256	~195 kHz
512	~97.7 kHz
1024	~48.8 kHz
2048	~24.4 kHz
4096	~12.2 kHz
8192 and higher: Division not supported	–

(1) These frequencies are not necessarily supported by all MCSPI modules. For more information, see the *Timing Requirements and Switching Characteristics* chapter in the device-specific Datasheet.

12.2.3.4.3.8.1 Clock Ratio Granularity

By default, the clock division ratio is defined by the MCSPI_CH(i)CONF[5-2] CLKD bit field with power-of-2 granularity leading to a clock division in the range 1 to 4096; in this case, the duty cycle is always 50 percent. With the MCSPI_CH(i)CONF[29] CLKG bit, clock division granularity can be changed to one clock cycle; in that case the MCSPI_CH(i)CTRL[15-8] EXTCLK bit field is concatenated with the MCSPI_CH(i)CONF[5-2] CLKD bit field to give a 12-bit-wide division ratio in the range 1 to 4096.

When granularity is one clock cycle (the CLKG bit set to 1), for the odd value of the clock ratio, the clock high level lasts one clock cycle more than the low level, depending on the MCSPI_CH(i)CONF[1] POL and MCSPI_CH(i)CONF[0] PHA bits (see Table 12-98).

Table 12-98. CLKSPIO High/Low Time Computation

Clock Ratio F_{RATIO}	CLKSPIO High Time	CLKSPIO Low Time
1	T_{HIGH_REF}	T_{LOW_REF}
Even >= 2	T_ref * (F_{RATIO}/2)	T_ref * (F_{RATIO}/2)
Odd >= (POL = PHA)	T_ref * (F_{RATIO}– 1)/2	T_ref * (F_{RATIO} + 1)/2
Odd >= (POL =! PHA)	T_ref * (F_{RATIO}+ 1)/2	T_ref * (F_{RATIO} – 1)/2

Note

F_{RATIO} = SPICLK frequency (F_{OUT}) division ratio
T_{HIGH} = SPICLK high time period
T_{LOW} = SPICLK low time period
T_ref = MCSPI_FCLK period
T_{HIGH_REF} = MCSPI_FCLK high time period
T_{LOW_REF} = MCSPI_FCLK low time period

If the CLKG bit is set to 1; F_{RATIO} = EXTCLK concatenated with CLKD + 1.

For odd ratio values, the duty cycle is calculated as follows:

Duty_cycle = $(1 – 1/F_{RATIO})/2$

Table 12-99 shows examples of clock granularity with a clock source frequency of 50 MHz.

Table 12-99. Clock Granularity Examples

EXTCLK	CLKD	CLKG	F_{RATIO}	PHA	POL	T_{HIGH} (ns)	T_{LOW} (ns)	T_{PERIOD} (ns)	Duty Cycle	F_{OUT} (MHz)
X	0	0	1	X	X	10.0	10.0	20.0	50–50	50
X	1	0	2	X	X	20.0	20.0	40.0	50–50	25
X	2	0	4	X	X	40.0	40.0	80.0	50–50	12.5
X	3	0	8	X	X	80.0	80.0	160.0	50–50	6.2
0	0	1	1	X	X	10.0	10.0	20.0	50–50	50
0	1	1	2	X	X	20.0	20.0	40.0	50–50	25
0	2	1	3	1	0	40.0	20.0	60.0	66–33	16.6
0	2	1	3	1	1	20.0	40.0	60.0	33–66	16.6
0	3	1	4	X	X	40.0	40.0	80.0	50–50	12.5
5	0	1	81	1	0	820.0	800.0	1620.0	50.6–49.4	0.617
5	7	1	88	X	X	880.0	880.0	1760.0	50–50	0.568

12.2.3.4.4 MCSPI Peripheral Mode

To select the MCSPI peripheral mode, set the MCSPI_MODULCTRL[2] MS bit.

A MCSPI peripheral device can be connected to up to four external MCSPI controller devices but handles transactions with one MCSPI controller device at a time.

In peripheral mode, the MCSPI initiates data transfer on the data lines (SPIDAT[0] and SPIDAT[1]) when it is selected by an active control signal (SPIEN_[n]) and receives an MCSPI clock (SPICLK) from the external MCSPI controller device. Only channel 0 can be configured as a peripheral but through the MCSPI_CH0CONF_0[22-21] SPIENSLV bit field any of the SPIEN_[n] signals can be used to select the MCSPI module. In peripheral mode and when the MCSPI_MODULCTRL[1] PIN34 is set to 0x0 (default behaviour), the MCSPI uses the edge of SPIEN_[n] to detect word length. For this reason, SPIEN_[n] must become inactive between each word.

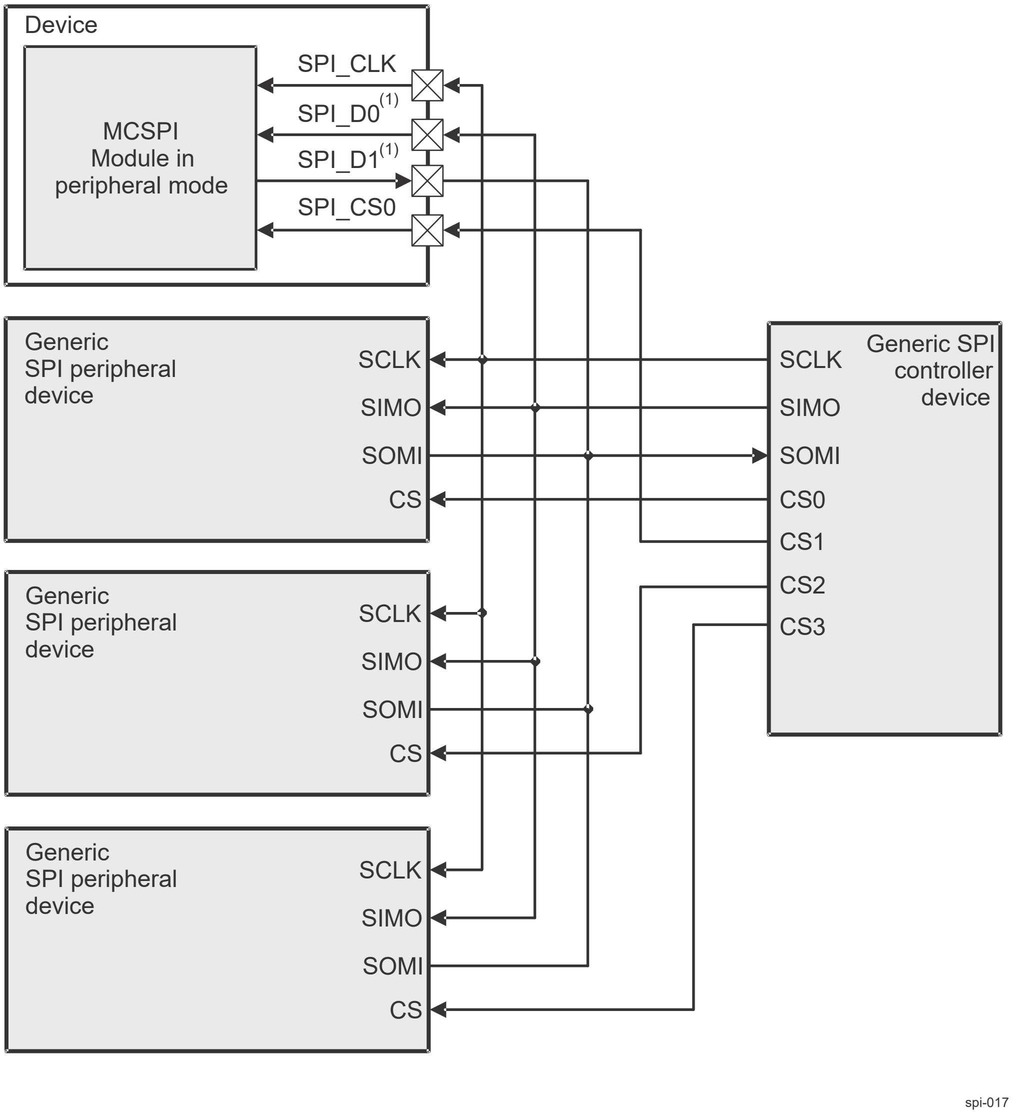
When the MCSPI_MODULCTRL[1] PIN34 is set to 0x0, the MCSPI does not support SPIEN_[n] active between MCSPI words. In this case, the MCSPI uses the edge to detect word length.

When the MCSPI_MODULCTRL[1] PIN34 is set to 0x1, a multiword transfer can be performed without needing the external MCSPI controller to deactivate SPIEN_[n] between each word as in this case the MCSPI module works in 3-pin peripheral mode and SPIEN_[n] is not needed.

12.2.3.4.4.1 Dedicated Resources

Only channel 0 can be enabled in peripheral mode.

Figure 12-95 shows an example of four peripherals wired on a single controller device.



A. Direction depends on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-95. Example of MCSPI Peripheral With One Controller and Multiple Peripheral Devices on Channel 0

Channel 0 in peripheral mode has the following resources:

- Its own channel enable, programmable with the MCSPI_CH0CTRL[0] EN bit. This channel must be enabled before transmission and reception.
- For this mode, the peripheral-select signal can be detected on any of the SPIEN_[n] ports. This is programmable with the MCSPI_CH0CONF[22-21] SPIENSLV bit field.
- Its own transmitter register, MCSPI_TX0, on top of the common transmit shift register. If the MCSPI_TX0 register is empty, the MCSPI_CH0STAT[1] TXS bit is set. If MCSPI is selected by an external controller (the active signal on the SPIEN_[n] port assigned to channel 0), the MCSPI_TX0 register content of channel 0 is always loaded into the shift register, whether its content is updated or not. The MCSPI_TX0 register must be loaded before MCSPI is selected by a controller.
- Its own receiver register, MCSPI_RX0, on top of the common receive shift register. If the MCSPI_RX0 register is full, the MCSPI_CH0STAT[0] RXS bit is set.

Note

The MCSPI_TXi and MCSPI_RXi registers are not used. Reading from or writing to a channel register other than channel 0 has no effect.

- Its own communication configuration with the following parameters through the MCSPI_CH0CONF:
  - Transmit and receive modes, programmable with the TRM field
  - Interface mode (two data pins or single data pin) and data pins assignment, both programmable with the IS and DPE bits. (The MCSPI modules are in peripheral mode after reset and must be properly configured for the modules to act in controller mode.)
  - MCSPI word length, programmable with the WL bit
  - SPIEN_[n] polarity, programmable with the EPOL bit
  - SPICLK polarity, programmable with the POL bit
  - SPICLK phase, programmable with the PHA bit

  The SPICLK frequency of a transfer is controlled by the external MCSPI controller connected to the MCSPI peripheral device. The MCSPI_CH0CONF[5-2] CLKD bit field is not used in peripheral mode.

Note

The configuration of the channel can be loaded in the MCSPI_CH0CONF only when the channel is disabled.

- Two DMA request events, read and write, synchronize read/write accesses of the DMA controller with the activity of MCSPI. DMA requests are asserted using the MCSPI_CH0CONF[15] DMAR bit for reading and the MCSPI_CH0CONF[14] DMAW bit for writing.
- Four interrupt events (see Section 12.2.3.4.7.2, *Interrupt Events in Peripheral Mode*).

12.2.3.4.4.2 Peripheral Transmit-and-Receive Mode

The peripheral receive mode is programmable (set the MCSPI_CH0CONF[13-12] TRM bit field to 0x0).

In peripheral transmit-and-receive mode, the MCSPI_TX0 register must be loaded before MCSPI is selected by an external MCSPI controller device.

After a channel is enabled, transmission and reception proceed with interrupt and DMA request events.

The MCSPI_TX0 register content is always loaded in the shift register whether it is updated or not. The event TX0_UNDERFLOW is activated accordingly and does not prevent transmission.

When the MCSPI word transfer completes (the MCSPI_CH0STAT[2] EOT bit is set to 1), the received data is transferred to the channel receive register.

To use MCSPI as a peripheral transmit-only device, the RX0_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the state of the MCSPI_RX0 register (see Section 12.2.3.4.7.2, *Interrupt Events in Peripheral Mode*).

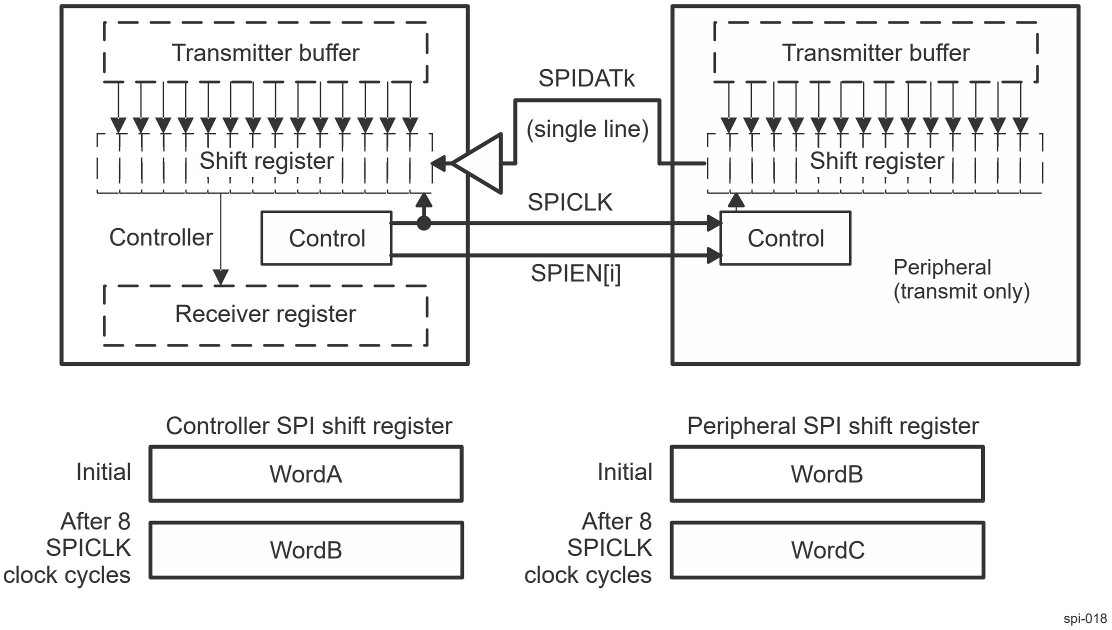
12.2.3.4.4.3 Peripheral Transmit-Only Mode

The peripheral transmit-only mode is programmable (set the MCSPI_CH0CONF[13-12] TRM bit field to 0x2) and avoids the requirement for the processor to read the MCSPI_RX0 register (minimizing data movement) only when transmission is meaningful.

To use the MCSPI as a peripheral transmit-only device, the RX0_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the state of the MCSPI_RX0 register.

When the MCSPI word transfer completes, the MCSPI_CH0STAT[2] EOT bit is set.

Figure 12-96 shows a half-duplex system with a controller device on the left and a transmit-only peripheral device on the right. Each time a bit transfers out from the peripheral, 1 bit transfers in the controller. After eight cycles of the serial clock SPICLK, WordB transfers from the peripheral to the controller.



k = 0 or 1 depending on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-96. MCSPI Half-Duplex Transmission (Transmit-Only Peripheral)

12.2.3.4.4.4 Peripheral Receive-Only Mode

The peripheral receive mode is programmable (set the MCSPI_CH0CONF[13-12] TRM bit field to 0x1).

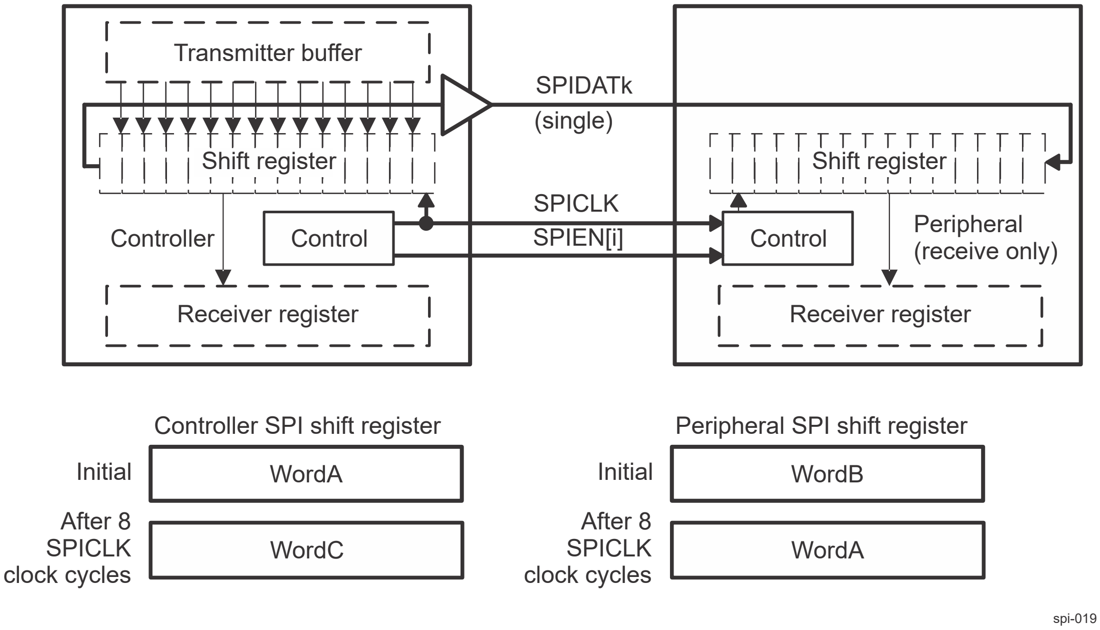
In receive-only mode, the MCSPI_TX0 register must be loaded before the MCSPI is selected by an external MCSPI controller device. The MCSPI_TX0 register content is always loaded into the shift register whether it is updated or not. The TX0_UNDERFLOW event is activated accordingly and does not prevent transmission.

When the MCSPI word transfer completes (the MCSPI_CH0STAT[2] EOT bit is set to 1), the received data is transferred to the channel receive register.

To use the MCSPI as a peripheral receive-only device, the TX0_EMPTY and TX0_UNDERFLOW interrupts and the DMA write requests must be disabled due to the state of the MCSPI_TX0 register.

For a full-duplex transmission, the serial clock (SPICLK) synchronizes shifting and sampling of the information on the single serial data line. For full duplex, two data lines are required. If SPICLK synchronizes on a single serial data line, the data line should be half-duplex.

Figure 12-97 shows a half-duplex system with a controller device on the left and a receive-only peripheral device on the right. Each time a bit transfers out from the controller, 1 bit transfers in from the peripheral. After eight cycles of the serial clock SPICLK, WordA transfers from the controller to the peripheral.



k = 0 or 1 depending on MCSPI_CH(i)CONF[16] DPE0, MCSPI_CH(i)CONF[17] DPE1 and MCSPI_CH(i)CONF[18] IS bits

Figure 12-97. MCSPI Half-Duplex Transmission (Receive-Only Peripheral)

12.2.3.4.5 MCSPI 3-Pin or 4-Pin Mode

Depending on targeted application the MCSPI interface can be configured to use 3 or 4 pins through the MCSPI_MODULCTRL[1] PIN34 bit. If this bit is set to 0, MCSPI is in 4-pin mode using the SPICLK, SPIDAT[0], SPIDAT[1] and SPIEN_[n] signals. If PIN34 is set to 1 the controller is in 3-pin mode and SPIEN_[n] is not used. In this mode all options related to chip select management are useless (EPOL, FORCE and TCS0 bits of MCSPI_CH(i)CONF). 3-pin and 4-pin operation applies to both controller and peripheral modes.

12.2.3.4.6 MCSPI FIFO Buffer Management

The MCSPI controller has a built-in 64-byte buffer to unload the DMA or interrupt handler and improve data throughput.

This buffer can be used by only one channel at a time and is selected by setting the MCSPI_CH(i)CONF[28] FFER or MCSPI_CH(i)CONF[27] FFEW bit to 1. If several channels are selected and several FIFO enable bit fields are set to 1, the controller forces the buffer not to be used; the driver must set only one FIFO enable bit field.

The buffer can be used in the following modes:

- Controller or peripheral mode
- Transmit-only, receive-only, or transmit-and-receive mode
- Single channel or turbo mode, or normal round-robin mode. In round-robin mode the buffer is used by only one channel.

Every word length (MCSPI_CH(i)CONF[11-7] WL) is supported.

In transmit-and-receive mode, the buffer can be used in transmit (see Figure 12-98) or receive (see Figure 12-99) directions, or in both directions. If only one direction is chosen in transmit-and-receive mode, the full buffer is used for this direction. In both directions, the buffer is split into two halves, one for each direction (see Figure 12-100).

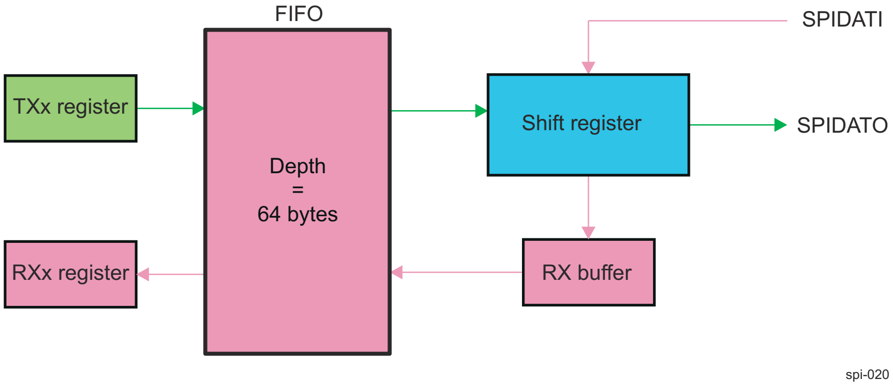


Figure 12-98. Buffer Used in Transmit Direction Only

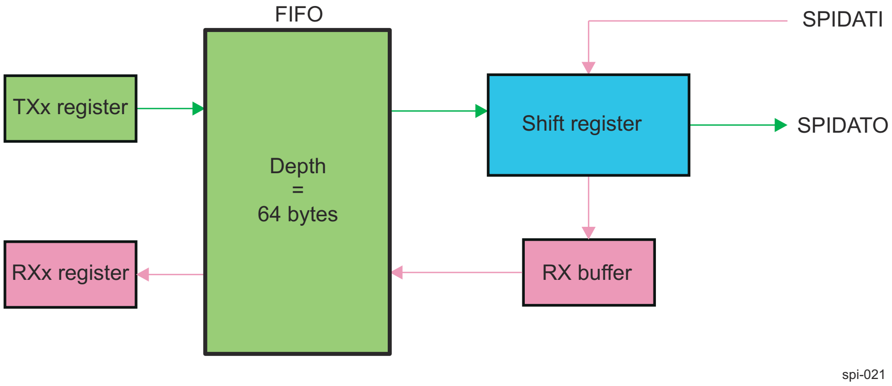


Figure 12-99. Buffer Used in Receive Direction Only

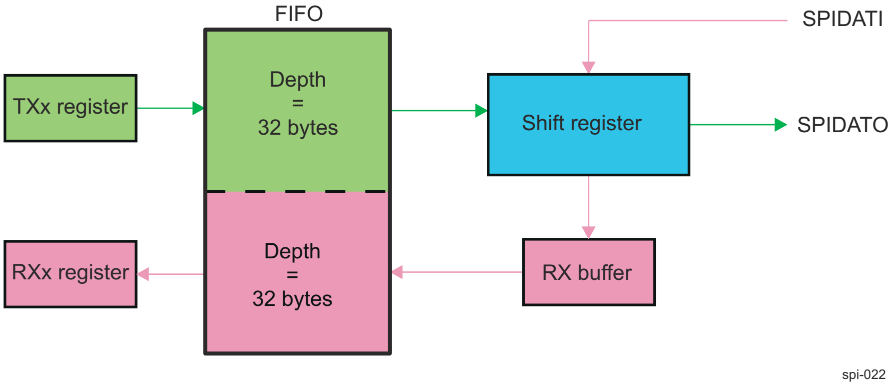


Figure 12-100. Buffer Used for Transmit and Receive Directions

Two levels (MCSPI_XFERLEVEL[5-0] AEL and MCSPI_XFERLEVEL[13-8] AFL) rule the buffer management. The granularity of these levels is 1 byte; it is not aligned with the MCSPI word length. The driver must set these values as a multiple of the MCSPI word length defined in WL. Table 12-100 lists the number of bytes written in the FIFO, depending on the word length.

Table 12-100. FIFO Writes, Word Length Relationship

	MCSPI Word Length (WL)		
	3 ≤ WL≤ 7	**8 ≤ WL ≤ 15**	**16 ≤ WL ≤ 31**
Number of bytes written in the FIFO	1 byte	2 bytes	4 bytes

The FIFO buffer pointers are reset when the corresponding channel is enabled or the FIFO configuration changes.

12.2.3.4.6.1 Buffer Almost Full

The MCSPI_XFERLEVEL[15-8] AFL bit field is needed when the buffer is used to receive an MCSPI word from a peripheral (the MCSPI_CH(i)CONF[28] FFER bit must be set to 1). It defines the almost-full buffer status. See Figure 12-101.

When the FIFO pointer reaches this level, an interrupt or a DMA request is sent to the processor to enable the system to read AFL + 1 bytes from the receive register.

Note

AFL + 1 must correspond to a multiple value of the MCSPI_CH(i)CONF[11-7] WL bit field.

When DMA is used, the request is de-asserted after the first receive register read.

No new request is asserted again as long as the system has not performed the correct number of read accesses.

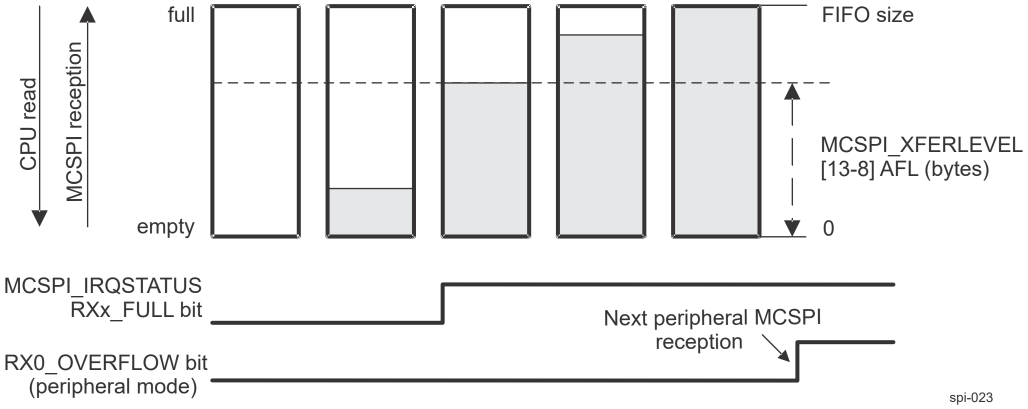


Figure 12-101. Buffer Almost Full Level (AFL)

Note

The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the request is asserted on the same conditions as the MCSPI_IRQSTATUS RXi_FULL flag.

12.2.3.4.6.2 Buffer Almost Empty

The MCSPI_XFERLEVEL[7-0] AEL bit field is needed when the buffer is used to transmit an MCSPI word to a peripheral (the MCSPI_CH(i)CONF[27] FFEW bit must be set to 1). It defines the almost-empty buffer status. See Figure 12-102.

When the FIFO pointer does not reach this level, an interrupt or a DMA request is sent to the processor to enable the system to write AEL + 1 bytes to the transmit register.

Note

AEL + 1 must correspond to a multiple value of the MCSPI_CH(i)CONF[11-7] WL bit field.

When DMA is used, the request is de-asserted after the first transmit register write.

No new request is asserted again as long as the system has not performed the correct number of write accesses.

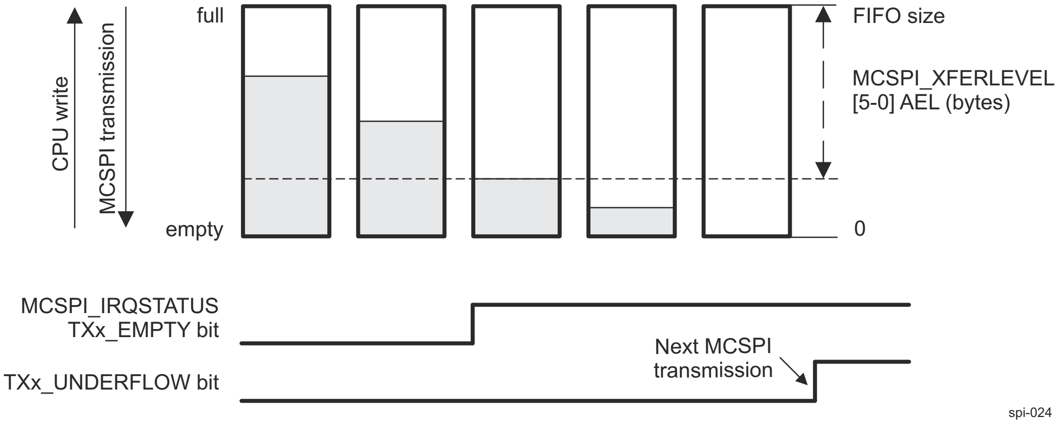


Figure 12-102. Buffer Almost Empty Level (AEL)

Note

The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the request is asserted on the same conditions as the MCSPI_IRQSTATUS TXi_EMPTY flag.

12.2.3.4.6.3 End of Transfer Management

When the FIFO buffer is enabled for a channel, the user must previously configure in the MCSPI_XFERLEVEL register the AEL and AFL levels and especially the MCSPI_XFERLEVEL[31-16] WCNT bit field to define the number of MCSPI words to be transferred using the FIFO before enabling the channel.

This counter lets the controller stop the transfer correctly after a defined number of MCSPI word transfers. If WNCT is set to 0x0000, the counter is not used and the user must stop the transfer manually by disabling the channel; in this case, the user does not know how many MCSPI transfers have been done. For received words, software must poll the MCSPI_CH(i)STAT[5] RXFFE bit and read the MCSPI_RXi receive register to empty the FIFO buffer.

When the end-of-word count interrupt is generated (the MCSPI_IRQSTATUS[17] EOW bit is set), the user can disable the channel and poll the MCSPI_CH(i)STAT[5] RXFFE bit to know the last MCSPI words in the FIFO buffer and read them.

No new request is asserted as long as the system has not performed the correct number of write accesses.

12.2.3.4.6.4 Multiple MCSPI Word Access

The processor has the ability to perform multiple MCSPI word access to the receive or transmit registers within a single 32-bit interface access by setting the MCSPI_MODULCTRL[7] MOA to 1 under specific conditions:

- The channel selected has the FIFO enable.
- Only FIFO sense enabled support the kind of access.
- MCSPI_MODULCTRL[7] MOA is set to 1.
- Only 32-bit interface access and data width can be performed to receive or transmit registers, for other kind of access the processor must de-assert MCSPI_MODULCTRL[7] MOA bit.
- The level MCSPI_XFERLEVEL[7-0] AEL and MCSPI_XFERLEVEL[15-8] AFL must be 32-bit aligned, it means that AEL[0] = AEL[1] = 1 or AFL[0] = AFL[1] = 1.
- If MCSPI_XFERLEVEL[31-16] WCNT is used it must be configured according to MCSPI word length.
- The word length of MCSPI words allows to perform multiple MCSPI access, that means that MCSPI_CH(i)CONF[11-7] WL is <16.

The number of MCSPI word access depends on MCSPI word length:

- 3 ≤ WL ≤ 7, MCSPI word length smaller or equal to byte length, 4 MCSPI words accessed per 32-bit interface read/write. If word count is used (MCSPI_XFERLEVEL[31-16] WCNT), set the bit field to WCNT[0] = WCNT[1] = 0.

- 8 ≤ WL ≤ 15, MCSPI word length greater than byte or equal to 16-bit length, 2 MCSPI words accessed per 32-bit interface read/write. If word count is used (MCSPI_XFERLEVEL[31-16] WCNT]), set the bit field to WCNT[0] = 0.
- 16 ≤ WL Multiple MCSPI word access is not applicable.

12.2.3.4.6.5 First MCSPI Word Delay

Figure 12-103 shows the MCSPI controller ability to delay the first MCSPI word transfer to give time for system to complete some parallel processes or fill the FIFO in order to improve transfer bandwidth. This delay is applied only on first MCSPI word after MCSPI channel enabled and first write in transmit register. It is based on output clock frequency.

This option is meaningful in controller mode and single channel mode asserted through MCSPI_MODULCTRL[0] SINGLE.

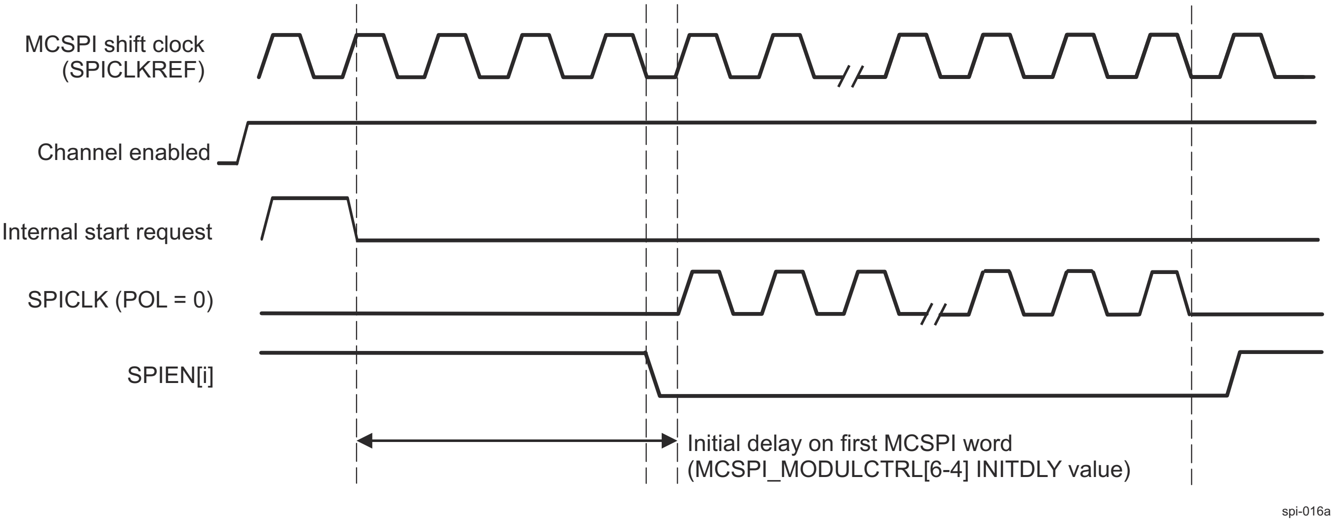


Figure 12-103. Controller Single Channel Initial Delay

Few delay values are available: No delay, 4/8/16/32 MCSPI cycles.

Its accuracy is half cycle in clock bypass mode and depends on clock polarity and phase.

12.2.3.4.7 MCSPI Interrupts

Each channel can issue interrupt events.

Each interrupt event has status bits in the MCSPI_IRQSTATUS register (RXi_FULL, TXi_UNDERFLOW, TXi_EMPTY, etc.) (where x = 0, 3) that indicate whether service is required. Each status bit has an interrupt enable bit (a mask) in the MCSPI_IRQENABLE register (RXi_FULL_ENABLE, TXi_UNDERFLOW_ENABLE, TXi_EMPTY_ENABLE, etc.).

When an interrupt occurs and a mask is later applied on it, the interrupt line is not asserted again, even if the interrupt source is not serviced.

The MCSPI supports interrupt-driven and polling operations.

12.2.3.4.7.1 Interrupt Events in Controller Mode

In controller mode, the interrupt events related to the state of the MCSPI_TXi register are TXi_EMPTY and TXi_UNDERFLOW. The interrupt event related to the state of the MCSPI_RXi register is RXi_FULL.

12.2.3.4.7.1.1 TXx_EMPTY

The TXx_EMPTY event is activated when a channel is enabled and its MCSPI_TXi register is empty (transient event). Enabling a channel automatically triggers this event, except in controller receive-only mode (see Section 12.2.3.4.3.4, *Controller Receive-Only Mode*). When the FIFO buffer is enabled (the MCSPI_CH(i)CONF[27]

FFEW bit is set to 1), the MCSPI_IRQSTATUS TXi_EMPTY bit is set as soon as there is enough space in the buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5-0] AEL bit field.

The MCSPI_TXi register must be loaded with data to remove the source of the interrupt; the MCSPI_IRQSTATUS TXi_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXi_EMPTY event is asserted as long as the processor has not performed the number of writes into the MCSPI_TXi register defined by the MCSPI_XFERLEVEL[5-0] AEL bit field. The processor must perform the correct number of writes.

12.2.3.4.7.1.2 TXx_UNDERFLOW

The event TXx_UNDERFLOW is activated when the channel is enabled and if the MCSPI_TXi register or the FIFO is empty (not updated with new data) when an external controller device starts a data transfer with the MCSPI (transmit and receive).

The TXi_UNDERFLOW is a harmless warning in controller mode.

To avoid having a TXi_UNDERFLOW event at the beginning of a transmission, the TXi_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TXi register, because the channel is enabled. To avoid having a TXx_UNDERFLOW event, the MCSPI_TXi register must seldom be loaded.

The MCSPI_IRQSTATUS TXi_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.1.3 RXx_ FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RXi register becomes filled (transient event). When the FIFO buffer is enabled (the MCSPI_CH(i)CONF[28] FFER bit is set to 1), RXi_ FULL is asserted as soon as the number of bytes held in the FIFO to be read reaches the MCSPI_XFERLEVEL[13-8] AFL threshold.

The MCSPI_RXi register must be read to remove the source of the interrupt; the MCSPI_IRQSTATUS RXi_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXi_FULL event is asserted as long as the processor has not performed AFL + 1 reads into MCSPI_RXi. The processor must perform the correct number of reads.

12.2.3.4.7.1.4 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31-16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the MCSPI transfer is halted on the channel using the FIFO buffer as soon as MCSPI_XFERLEVEL[31-16] WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.2 Interrupt Events in Peripheral Mode

In peripheral mode, the interrupt events related to the state of the MCSPI_TXi register are TX0_EMPTY and TX0_UNDERFLOW. The interrupt events related to the state of the MCSPI_RXi are RX0_FULL and RX0_OVERFLOW (channels 1, 2, and 3 do not have a receiver overflow status bit). See the MCSPI_IRQSTATUS register.

12.2.3.4.7.2.1 TXx_EMPTY

The TXi_EMPTY event is activated when a channel is enabled and its MCSPI_TXi register is empty. Enabling the channel automatically raises this event. If the FIFO buffer is enabled (the MCSPI_CH(i)CONF[27] FFEW bit is set to 1), the TXx_EMPTY event is asserted as soon as there is enough space in buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5-0] AEL bit field.

The MCSPI_TXi register must be loaded with data to remove the source of the interrupt; the MCSPI_IRQSTATUS TXi_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXi_EMPTY event is asserted as long as the processor has not performed the number of writes into the MCSPI_TXi register defined by MCSPI_XFERLEVEL[5-0] AEL bit field. The processor must perform the correct number of writes.

12.2.3.4.7.2.2 TXx_UNDERFLOW

The TXx_UNDERFLOW event is activated when a channel is enabled and if the MCSPI_TXi register is empty (not updated with new data) when an external controller device starts a data transfer with the MCSPI (transmit and receive).

When FIFO is enabled, the data emitted while the underflow event is raised is not the last data written in the FIFO but the next data in the FIFO (an old transmitted value or a dummy data in the FIFO has been reset).

TXx_UNDERFLOW indicates an error (data loss) in peripheral mode.

To avoid having a TXi_UNDERFLOW event at the beginning of a transmission, the TXi_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TXi register because the channel is enabled.

The MCSPI_IRQSTATUS TXx_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.2.3 RXx_FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RXi register is being filled (transient event). When the FIFO buffer is enabled (the MCSPI_CH(i)CONF[28] FFER bit is set to 1), RXi_FULL is asserted as soon as the number of bytes held in the buffer to read defined by the MCSPI_XFERLEVEL[13-8] AFL bit field.

The MCSPI_RXi register must be read to remove the source of the interrupt; the MCSPI_IRQSTATUS RXi_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXi_FULL event is asserted as long as the processor has not performed AFL + 1 reads into MCSPI_RXi. The processor must perform the correct number of reads.

12.2.3.4.7.2.4 RX0_OVERFLOW

The RX0_OVERFLOW event is activated in peripheral mode in transmit-and-receive mode or receive-only mode when a channel is enabled and the MCSPI_RXi register or FIFO is full when a h MCSPI word is received. The MCSPI_RXi register is always overwritten with the new MCSPI word. If the FIFO is enabled, data within the FIFO are overwritten; it must be considered as corrupted. The RX0_OVERFLOW event should not appear in peripheral mode using the FIFO.

The RX0_OVERFLOW event indicates an error (data loss) in peripheral mode.

The MCSPI_IRQSTATUS[3] RX0_OVERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.2.5 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31-16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the MCSPI transfer is halted on the channel using the FIFO buffer as soon as WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

12.2.3.4.7.3 Interrupt-Driven Operation

An interrupt enable bit in the MCSPI_IRQENABLE register can be set to enable each event to generate interrupt requests when the corresponding event occurs. Status bits are automatically set by hardware logic conditions.

When an event occurs (the single interrupt line is asserted), the processor must:

1. Read the MCSPI_IRQSTATUS register to identify which event occurred.
2. Read the MCSPI_RXi register that corresponds to the event to remove the source of an RXi_FULL event or write into the MCSPI_TXi register that corresponds to the event to remove the source of a TXi_EMPTY event. No action is required to remove the source of the TXi_ UNDERFLOW and RX0_OVERFLOW events.
3. Set the corresponding bit of the MCSPI_IRQSTATUS register to 1 to clear an interrupt status and then release the interrupt line.

The interrupt status bit must always be reset after channel enabling and before events are enabled as interrupt sources.

12.2.3.4.7.4 Polling

When the interrupt capability of an event is disabled in the MCSPI_IRQENABLE register, the interrupt line is not asserted, but the status bits in the MCSPI_IRQSTATUS register can be polled by software to detect when the corresponding event occurs.

Once the expected event occurs:

- RXx_FULL: To remove the source of the event, the processor must read the corresponding MCSPI_RXi register.
- TXx_EMPTY: To remove the source of the event, the processor must write into the corresponding MCSPI_TXi register.
- TXx_UNDERFLOW and RX0_OVERFLOW: No action is required to remove the source of the event.

To clear an interrupt, set the corresponding status bit of the MCSPI_IRQSTATUS register to 1. This does not affect the interrupt line state.

12.2.3.4.8 MCSPI DMA Requests

Each MCSPI channel, if enabled, can issue DMA requests. There are two DMA request lines per MCSPI channel (one for read and one for write).

The DMA read request line is asserted when the MCSPI channel is enabled and new data is available in the receive register of the MCSPI channel. A DMA read request can be individually masked with the MCSPI_CH(i)CONF[15] DMAR bit. The DMA read request line is de-asserted when reading of the MCSPI_RXi register of the MCSPI channel completes.

The DMA write request line is asserted when the MCSPI channel is enabled and the MCSPI_TXi register of the MCSPI channel is empty. A DMA write request can be individually masked with the MCSPI_CH(i)CONF[14] DMAW bit. The DMA write request line is de-asserted when loading of the MCSPI_TXi register of the channel completes.

12.2.3.4.9 MCSPI Power Saving Management

Power consumption can be optimized by switching off internal clocks (interface and functional clock) when there is no activity.

12.2.3.4.9.1 Normal Mode

In normal mode, internal MCSPI module clocks are automatically switched off (autogated) when there is no activity in peripheral or controller mode.

Autogating of the module interface clock and functional clock occurs when the following conditions are met:

- The MCSPI_SYSCONFIG[0] AUTOIDLE bit is set.
- In controller mode, there is no data to transmit or receive in all channels.

- In peripheral mode, the MCSPI is not selected by the external controller and there are no register accesses.

Autogating of the module interface clock and functional clock stops when the following conditions are met:

- In controller mode, an internal access occurs.
- In peripheral mode, an internal access occurs or the MCSPI is selected by the external controller.

12.2.3.4.9.2 Idle Mode

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

At the power management level, when all conditions to shut off the MCSPI_FCLK or MCSPI_ICLK clocks are met, the corresponding LPSC asserts a clock stop request to the MCSPI. Although this procedure is completely hardware-oriented and out of software control, the method in which the MCSPI module acknowledges the clock stop request can be configured through the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field.

The settings of the SIDLEMODE bit field and the related acknowledgement modes are:

- Force-idle mode (the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field is set to 0x0): The MCSPI module acknowledges unconditionally the clock stop request, regardless of its internal operations. This mode must be used carefully in this case because it does not prevent the loss of data when the clock is switched off.
- No-idle mode (the SIDLEMODE bit field is set to 0x1): The MCSPI never acknowledges the clock stop request and is safe from a module point of view because it ensures that the clocks remain active. However, it is not efficient to save power because it does not allow shut off of MCSPI_FCLK and MCSPI_ICLK.
- Smart-idle mode (the SIDLEMODE bit field is set to 0x2): The MCSPI acknowledges the clock stop request, depending on its internal activity. MCSPI acknowledges the shut off of MCSPI_FCLK and MCSPI_ICLK only when all pending transactions, IRQs, or DMA requests are treated. This is the best approach for efficient system power management.

When configured in smart-idle mode, the MCSPI also offers an additional feature to control gating of MCSPI_FCLK or MCSPI_ICLK. The MCSPI_SYSCONFIG[9-8] CLOCKACTIVITY bit field determines which clock shuts down (MCSPI_FCLK, MCSPI_ICLK, neither clock, or both clocks).

The setting of the CLOCKACTIVITY bit field is used internally to the MCSPI to determine on which part of the module the conditions to acknowledge the clock stop request are tested. For example, if MCSPI_FCLK is not shut off on clock stop request, the MCSPI considers only MCSPI_ICLK and the associated pending activities before acknowledging the request.

Some MCSPI features are associated with MCSPI_ICLK and others with MCSPI_FCLK. Using the CLOCKACTIVITY bit field with the smart-idle mode ensures that the features associated with the clock that remains active are always enabled, even if MCSPI acknowledges the clock stop request.

12.2.3.4.9.2.1 Force-Idle Mode

Force-idle mode is enabled and exited as follows:

- Force-idle mode is enabled when the MCSPI_SYSCONFIG[4-3] SIDLEMODE bit field is set to 0x0.
  - In force-idle mode, the MCSPI responds unconditionally to the clock stop request by de-asserting unconditionally the interrupt and DMA request lines, if asserted.
  - The transition from normal mode to idle mode does not affect the interrupt event bits of the MCSPI_IRQSTATUS register.
  - In force-idle mode, because the module must be disabled, the interrupt and DMA request lines are likely de-asserted. The interface clock and MCSPI clock provided to the MCSPI can be switched off.
  - A clock stop request during an MCSPI data transfer can lead to an unexpected and unpredictable result. Software must avoid such a request.

12.2.3.5 MCSPI Programming Guide

This section describes the low-level hardware programming sequences for the configuration and use of the MCSPI module.

12.2.3.5.1 MCSPI Global Initialization

12.2.3.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the MCSPI module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MCSPI. For further information, see *MCSPI Integration* and *MCSPI Environment*.

Table 12-101 lists the information on the global initialization of the surrounding modules.

Table 12-101. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
COMPUTE_CLUSTER0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling COMPUTE_CLUSTER0 interrupts and if this applicable, see *Interrupts*.
MCU_M4FSS0_CORE0	Device INTCs must be configured to enable the interrupt request generation. For information about enabling MCU_M4FSS0_CORE0 interrupts and if this is applicable, see *Interrupts*.
R5FSS0/1_CORE0/1	Device INTCs must be configured to enable the interrupt request generation. For information about enabling R5FSS0/1_CORE0/1 interrupts and if this is applicable, see *Interrupts*.
PRUSS	Device INTCs must be configured to enable the interrupt request generation. For information about enabling PRUSS interrupts and if this is applicable, see *Interrupts*.
PDMA0 and PDMA1	Device INTCs must be configured to enable the interrupt request generation.
MCU_PLLCTRL0 and PLLCTRL0	PLL controller's configuration must be done to enable the module clocks. For more information, see *Clocking*.

12.2.3.5.1.2 MCSPI Global Initialization

12.2.3.5.1.2.1 Main Sequence – MCSPI Global Initialization

The procedure in Table 12-102 can be used to initialize MCSPI when performing software reset.

Table 12-102. MCSPI Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	MCSPI_SYSCONFIG[1] SOFTRESET	1
Wait until reset is finished?	MCSPI_SYSSTATUS[0] RESETDONE	=1
Configure static settings (such as SPI controller or peripheral) as required.	MCSPI_MODULCTRL[8-0]	0x-
Write MCSPI_SYSCONFIG	MCSPI_SYSCONFIG	0x-

12.2.3.5.2 MCSPI Operational Mode Configuration

12.2.3.5.2.1 MCSPI Operational Modes

The selection of the working mode is done with the MCSPI_CH(i)CONF register.

Table 12-103. MCSPI Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set receive mode for the channel.	MCSPI_CH(i)CONF[13-12] TRM	0x1
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CH(i)CONF	0x-
Reset the status bits.	MCSPI_IRQSTATUS	0x0

Table 12-104. MCSPI Transmit Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit mode for the channel.	MCSPI_CH(i)CONF[13-12] TRM	0x2
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CH(i)CONF	0x-

Table 12-104. MCSPI Transmit Mode Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Reset the status bits.	MCSPI_IRQSTATUS	0x0

Table 12-105. MCSPI Transmit-and-Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit and receive mode for the channel.	MCSPI_CH(i)CONF[13-12] TRM	0x0
Configure SPI clock polarity/phase, clock divider, word length, and others for the channel.	MCSPI_CH(i)CONF	0x-
Reset the status bits.	MCSPI_IRQSTATUS	0x0

12.2.3.5.2.1.1 Common Transfer Sequence

MCSPI module allows the transfer of one or several words, according to different modes:

- CONTROLLER Normal, CONTROLLER Turbo, PERIPHERAL
- TRANSMIT–RECEIVE, TRANSMIT-ONLY, RECEIVE-ONLY
- Write and Read requests: Interrupts, DMA
- SPIEN_[n] lines assertion/deassertion: automatic, manual

For all these sequences, the host process contains the main process and the interrupt routines.

The interrupt routines are called on the interrupt signals or by an internal call if the module is used in polling mode.

Table 12-106 represents the main sequence which is common to all transfers.

In multi-channel controller mode, the sequences of different channels can be run simultaneously.

Table 12-106. Common Transfer Sequence (Main Process)

Step	Register/Bit Field/Programming Model	Value
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
Write MCSPI_IRQENABLE to enable interrupts	MCSPI_IRQENABLE	0x-
Write MCSPI_CH(i)CONF to configure the channel	MCSPI_CH(i)CONF	0x-
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait for the first write request (TX empty or DMA write)		
Write the transmitter register with data	MCSPI_TXi	0x-
Wait for the host event for end of transfer		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.2.1.2 End of Transfer Sequences

The end of transfer depends on the transfer mode. Table 12-107 summarizes the type of end of transfer per transfer mode and gives a reference to the appropriate section for details.

Table 12-107. End of Transfer Sequences

		TRANSMIT-AND-RECEIVE		TRANSMIT-ONLY		RECEIVE-ONLY	
		INTERRUPT	**DMA**	**INTERRUPT**	**DMA**	**INTERRUPT**	**DMA**
CONTROLLER Normal	End of transfer sequence	See Section 12.2.3.5.2.1.3		See Section 12.2.3.5.2.1.4.1	See Section 12.2.3.5.2.1.4.2	See Section 12.2.3.5.2.1.5.1	See Section 12.2.3.5.2.1.5.2
	Minimum number of word	1	1	1	1	1	2
	DMA transfer size		N		N		N-1

Table 12-107. End of Transfer Sequences (continued)

		TRANSMIT-AND-RECEIVE		TRANSMIT-ONLY		RECEIVE-ONLY	
		INTERRUPT	**DMA**	**INTERRUPT**	**DMA**	**INTERRUPT**	**DMA**
CONTROLLER Turbo	End of transfer sequence	See Section 12.2.3.5.2.1.3		See Section 12.2.3.5.2.1.4.1	See Section 12.2.3.5.2.1.4.2	See Section 12.2.3.5.2.1.6.1	See Section 12.2.3.5.2.1.6.2
	Minimum number of word	1	1	1	1	2	3
	DMA transfer size		N		N		N-2
PERIPHERAL	End of transfer sequence	See Section 12.2.3.5.2.1.3		See Section 12.2.3.5.2.1.4.1	See Section 12.2.3.5.2.1.4.2	See Section 12.2.3.5.2.1.7	
	Minimum number of word	1	1	1	1	1	1
	DMA transfer size		N		N	N	N

The transfer to execute has a size of N words.

The different sequences can be merged in one process to manage transfers of several types. The end of transfer sequences are described from the start of the channel.

In these sequences, some soft variables are used:

- write_count = 0
- read_count = 0
- channel_enable = FALSE
- last_transfer = FALSE
- last_request = FALSE

They are initialized before starting the channel.

12.2.3.5.2.1.3 Transmit-and-Receive (Controller and Peripheral)

If the requests are configured in DMA, write_count and read_count are assigned with ‘N’ when the DMA handlers have completed their ‘N’ CBASS0 accesses.

Table 12-108. Transmit-and-Receive (Controller and Peripheral) (Main Process)

Step	**Register/Bit Field/Programming Model**	**Value**
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait for write_count = N **AND** read_count = N		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

Table 12-109. Transmit-and-Receive (Controller and Peripheral) (Interrupt Routine)

Step	**Register/Bit Field/Programming Model**	**Value**
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXi_EMPTY		
Write the transmitter register with data	MCSPI_TXi	0x-
Increment write_count +1		
IF: RXi_FULL		
Read the receiver register	MCSPI_RXi	
Increment read_count +1		
ENDIF		

12.2.3.5.2.1.4 Transmit-Only (Controller and Peripheral)

12.2.3.5.2.1.4.1 Based on Interrupt Requests

Table 12-110. Transmit-Only With Interrupts (Controller and Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until last transfer = TRUE		
Wait for end of transfer	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

Table 12-111. Transmit-Only With Interrupts (Controller and Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXx_EMPTY **AND** write_count < N		
Write the transmitter register with data	MCSPI_TXi	0x-
Increment write_count +1		
ELSEIF: write_count ≥ N		
last_transfer = TRUE		
ENDIF		

12.2.3.5.2.1.4.2 Based on DMA Write Requests

When the DMA handler has completed its ‘N’ CBASS0 accesses, write_count is assigned with ‘N’.

Table 12-112. Transmit-Only With DMA (Controller and Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until write_count = N		
Disable DMA write request	MCSPI_CH(i)CONF[14] DMAW	0
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

Table 12-113. Transmit-Only With DMA (Controller and Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: TXi_EMPTY **AND** write_count = N		
last_transfer = TRUE		
ENDIF		

12.2.3.5.2.1.5 Controller Normal Receive-Only

12.2.3.5.2.1.5.1 Based on Interrupt Requests

Table 12-114. Receive-Only With Interrupt (Controller Normal) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until last_request = TRUE		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		

Table 12-115. Receive-Only With Interrupt (Controller Normal) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL **AND** read_count = N - 1		
last_request = TRUE		
ELSEIF: read_count ≠ N - 1		
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		
ENDIF		

12.2.3.5.2.1.5.2 Based on DMA Read Requests

When the DMA handler has completed its ‘N-1’ CBASS0 accesses, read_count is assigned with ‘N-1’.

Table 12-116. Receive-Only With DMA (Controller Normal) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until read_count = N - 1		
Disable DMA read request	MCSPI_CH(i)CONF[15] DMAR	0
Wait until last_transfer = TRUE		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		

Table 12-117. Receive-Only With DMA (Controller Normal) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL **AND** read_count = N		
last_transfer = TRUE		
ENDIF		

12.2.3.5.2.1.6 Controller Turbo Receive-Only

12.2.3.5.2.1.6.1 Based on Interrupt Requests

Table 12-118. Receive-Only With Interrupt (Controller Turbo) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until channel_enable = TRUE		
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0
Wait until channel_enable = FALSE		

Table 12-119. Receive-Only With Interrupt (Controller Turbo) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL		
IF: read_count = N - 2		
last_transfer = TRUE		

Table 12-119. Receive-Only With Interrupt (Controller Turbo) (Interrupt Routine) (continued)

Step	Register/Bit Field/Programming Model	Value
Wait until channel_enable = FALSE		
ENDIF		
IF: read_count < N		
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		
ENDIF		
ENDIF		

12.2.3.5.2.1.6.2 Based on DMA Read Requests

When the DMA handler has completed its 'N-2' CBASS0 accesses read_count is assigned with 'N-2'.

Table 12-120. Receive-Only With DMA (Controller Turbo) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until channel_enable = TRUE		
Wait until read_count = TRUE		
Disable DMA read request	MCSPI_CH(i)CONF[15] DMAR	0
Wait until last_transfer = TRUE		
Wait for end of transfer	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0
Wait until channel_enable = FALSE		

Table 12-121. Receive-Only With DMA (Controller Turbo) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL		
IF: read_count = N - 2		
last_transfer = TRUE		
Wait until channel_enable = FALSE		
ENDIF		
IF: read_count < N		
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		
ENDIF		
ENDIF		

12.2.3.5.2.1.7 Peripheral Receive-Only

If the requests are configured in DMA, read_count is assigned with 'N' when the DMA handler has completed its 'N' CBASS0 accesses.

Table 12-122. Receive-Only (Peripheral) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
Wait until read_count = N		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

Table 12-123. Receive-Only (Peripheral) (Interrupt Routine)

Step	Register/Bit Field/Programming Model	Value
Read MCSPI_IRQSTATUS	MCSPI_IRQSTATUS	0x-
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS[channel i bits]	0b1111
IF: RXi_FULL		
Read the receiver register	MCSPI_RXi	0x-
Increment read_count +1		
ENDIF		

12.2.3.5.2.1.8 Transfer Procedures With FIFO

These flows describe the transfer with FIFO.

The MCSPI module allows the transfer of one or several words, according to different modes:

- CONTROLLER Normal, CONTROLLER Turbo, PERIPHERAL
- TRANSMIT–RECEIVE, TRANSMIT-ONLY, RECEIVE-ONLY
- Write and Read requests: IRQ, DMA

For all these flows, the host process contains the main process and the interrupt routine. This routine is called on the IRQ signals or by an internal call if the module is used in polling mode.

For more information, see Section 12.2.3.4.6, *MCSPI FIFO Buffer Management*.

Table 12-124. FIFO Mode Common Sequence (Controller) (Main Process)

Step	Register/Bit Field/Programming Model	Value
Write MCSPI_IRQSTATUS to reset channel status bits	MCSPI_IRQSTATUS	1
Write MCSPI_IRQENABLE to enable interrupts	MCSPI_IRQENABLE	1
Write MCSPI_CH(i)CONF to configure the channel	MCSPI_CH(i)CONF	0x-
Write MCSPI_XFERLEVEL	MCSPI_XFERLEVEL	0x-
Start the channel	MCSPI_CH(i)CTRL[0] EN	1
IF: Receive only		
Wait for the write request (TX empty or DMA write)		
Write for the transmitter register with data	MCSPI_TXi	0x-
ENDIF		
Wait for the host event for end of transfer		
Stop the channel	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.2.1.8.1 Common Transfer Sequence in FIFO Mode

This flow describes the host sequence for a transfer of any type defined in Section 12.2.3.5.2.1.8, *Transfer Procedures With FIFO*.

In multi-channel, only one channel can use the FIFO.

Before enabling the FIFO for a channel (MCSPI_CH(i)CONF[28] FFER and MCSPI_CH(i)CONF[27] FFEW bits), the host must check that the FIFO is not enabled for another channel, even if these channels are not used.

In transmit-and-receive mode, the FIFO can be enabled for write or read request only, without FIFO for the other request.

In Peripheral mode, the channel 0 only can be activated. The correct SPIEN line is chosen in MCSPI_CH0CONF[22-21] SPIENSLV bits.

The MCSPI module can start the transfer only when the first write request has been released by writing the MCSPI_TXi register, even in receive-only mode (only one write request occurs in this case).

12.2.3.5.2.1.8.2 End of Transfer Sequences in FIFO Mode

Table 12-125 summarizes the type of end of transfer per transfer mode and gives a reference to the appropriate section for details.

Table 12-125. End of Transfer Sequences in FIFO Mode

Word count	TRANSMIT AND RECEIVE	TRANSMIT-ONLY	RECEIVE-ONLY
Yes	See Figure 12-104	See Figure 12-106	See Figure 12-107
No	See Figure 12-105	See Figure 12-106	See Figure 12-108

The end of transfer sequences are described from the start of the channel.

In these sequences, some soft variables are used:

- write_count = N
- read_count = N
- last_request = FALSE

They are initialized before starting the channel.

12.2.3.5.2.1.8.3 Transmit-and-Receive With Word Count

Figure 12-104 shows the flow of a transfer in transmit-and-receive mode, with word count.

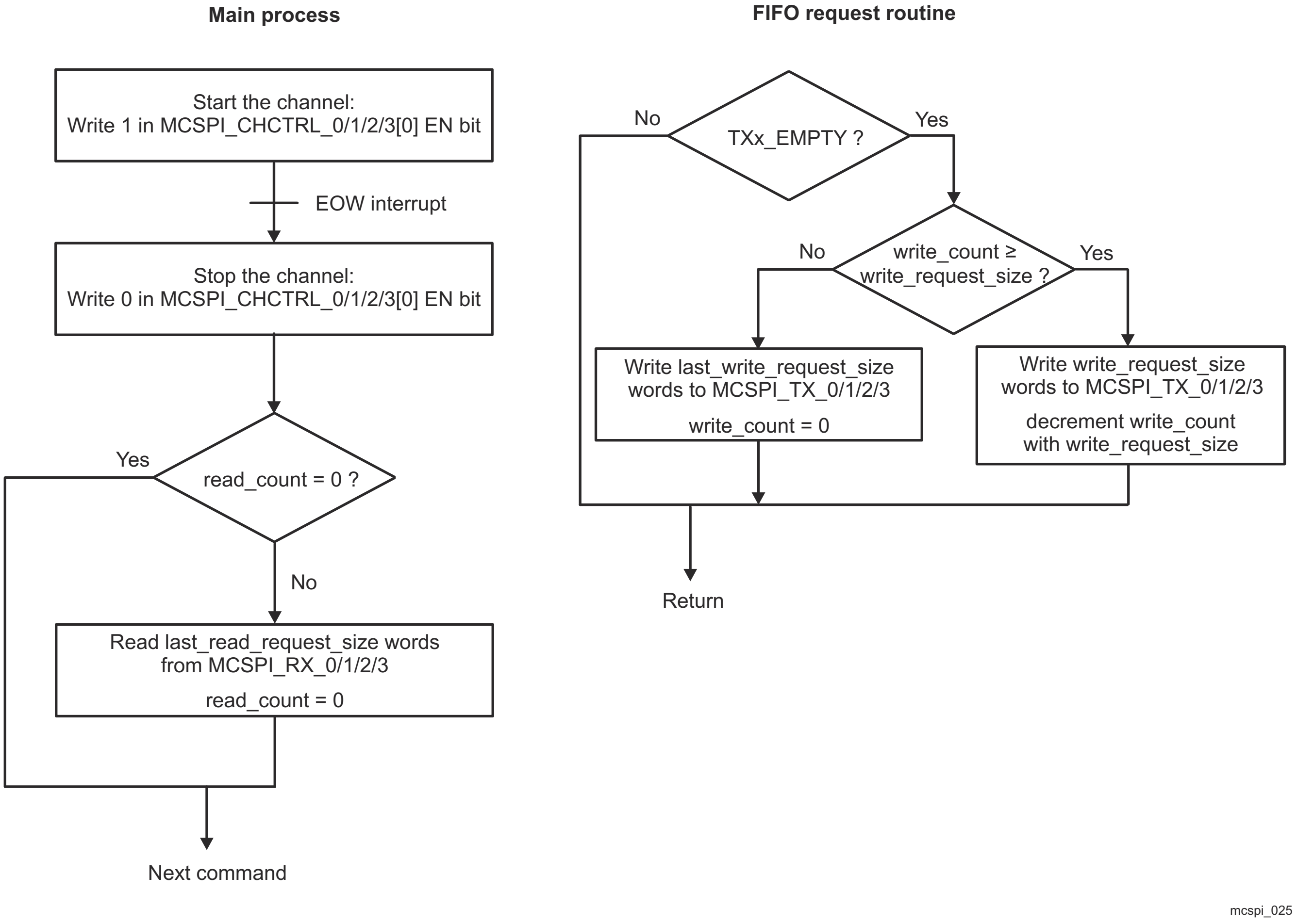


Figure 12-104. FIFO Mode Transmit-and-Receive With Word Count (Controller)

12.2.3.5.2.1.8.4 Transmit-and-Receive Without Word Count

Figure 12-105 shows the flow of a transfer in transmit-and-receive mode, without word count.

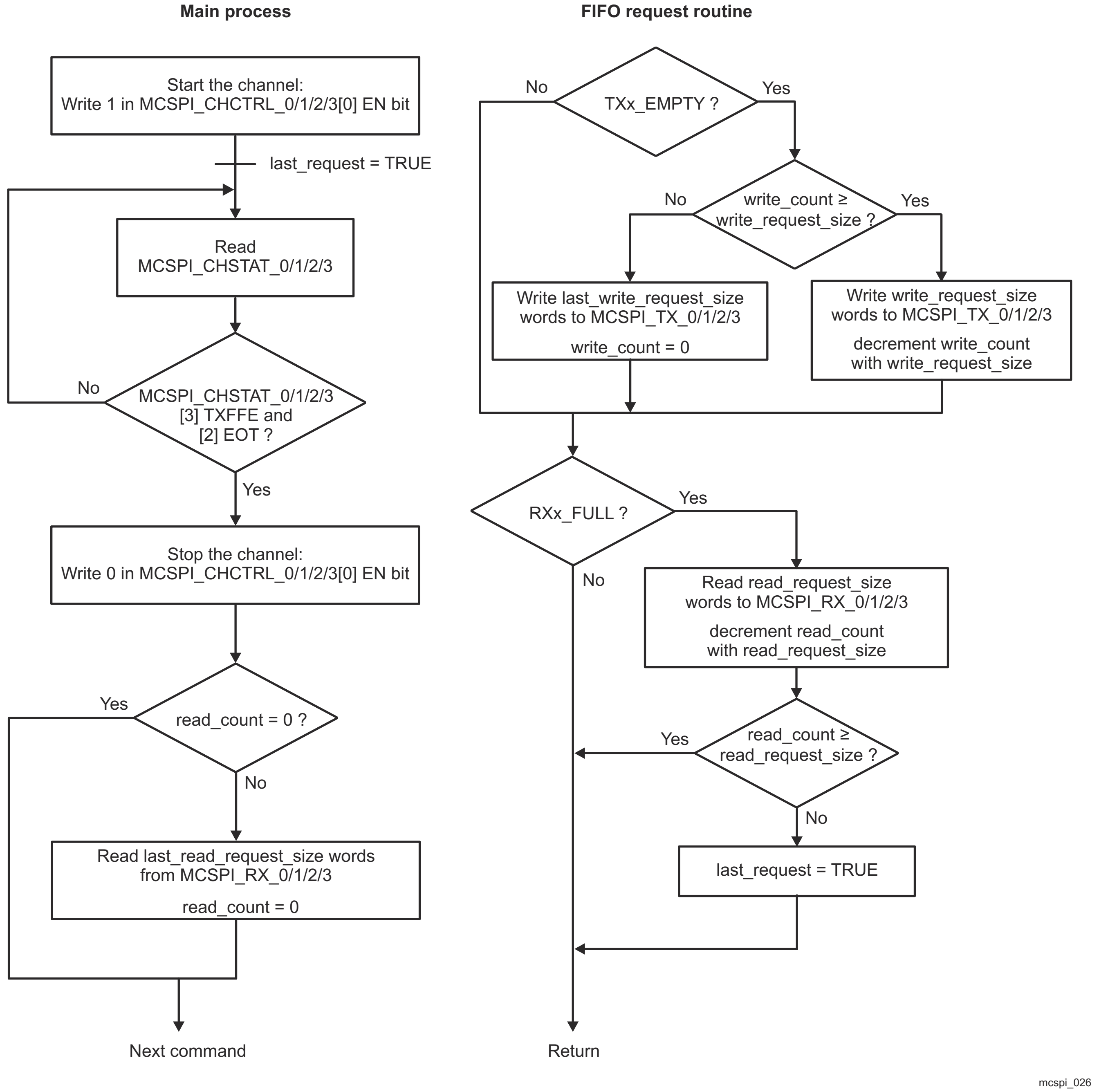


Figure 12-105. FIFO Mode Transmit-and-Receive Without Word Count (Controller)

12.2.3.5.2.1.8.5 Transmit-Only

Figure 12-106 shows the flow of a transfer in transmit-only mode, with or without word count. The difference between word count enabled or not is just on the condition after starting the channel:

- word count enable: wait for EOW interrupt
- word count disable: wait for write_count = 0

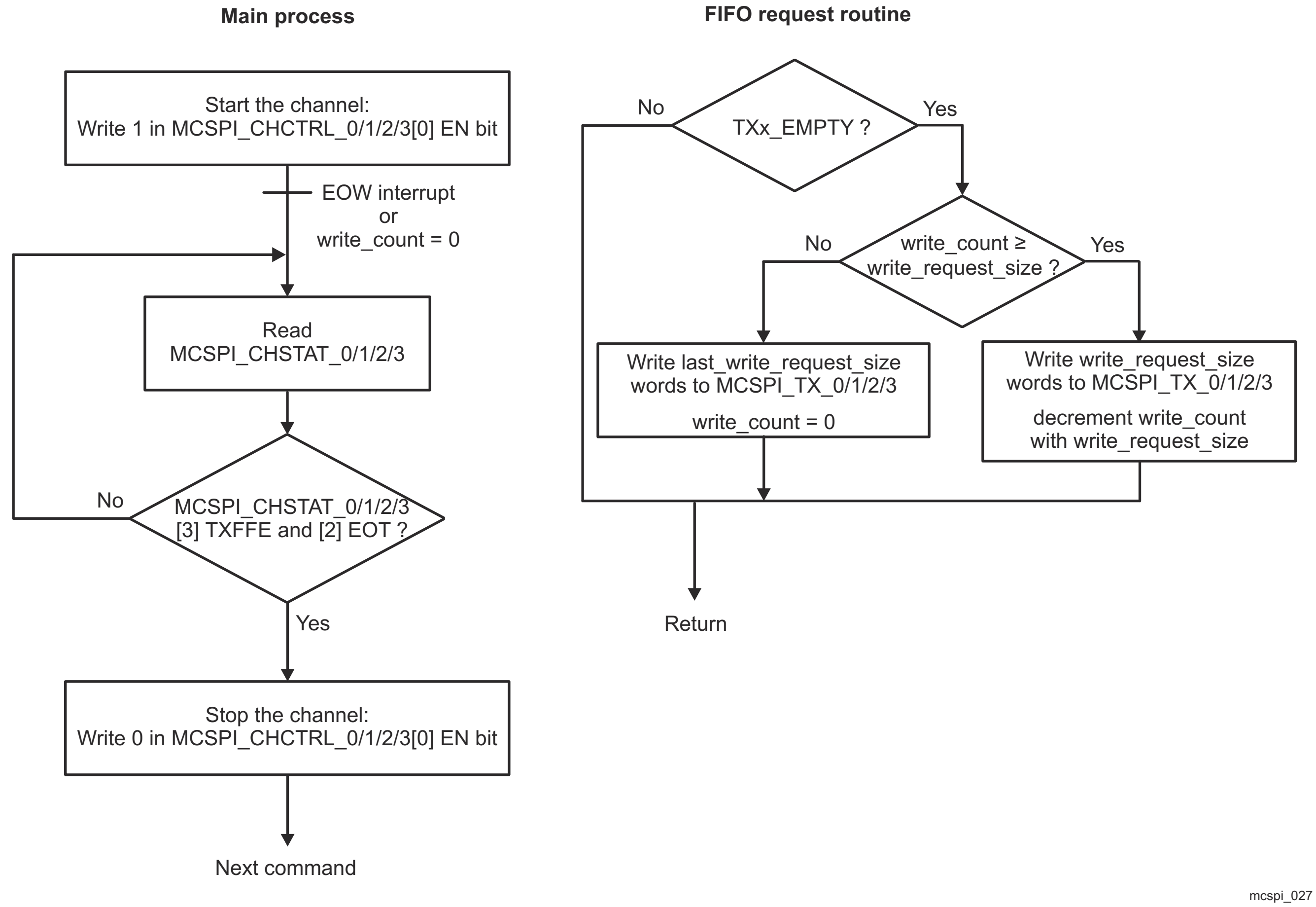


Figure 12-106. FIFO Mode Transmit-Only (Controller)

12.2.3.5.2.1.8.6 Receive-Only With Word Count

Figure 12-107 shows the flow of a transfer in receive-only mode, with word count.

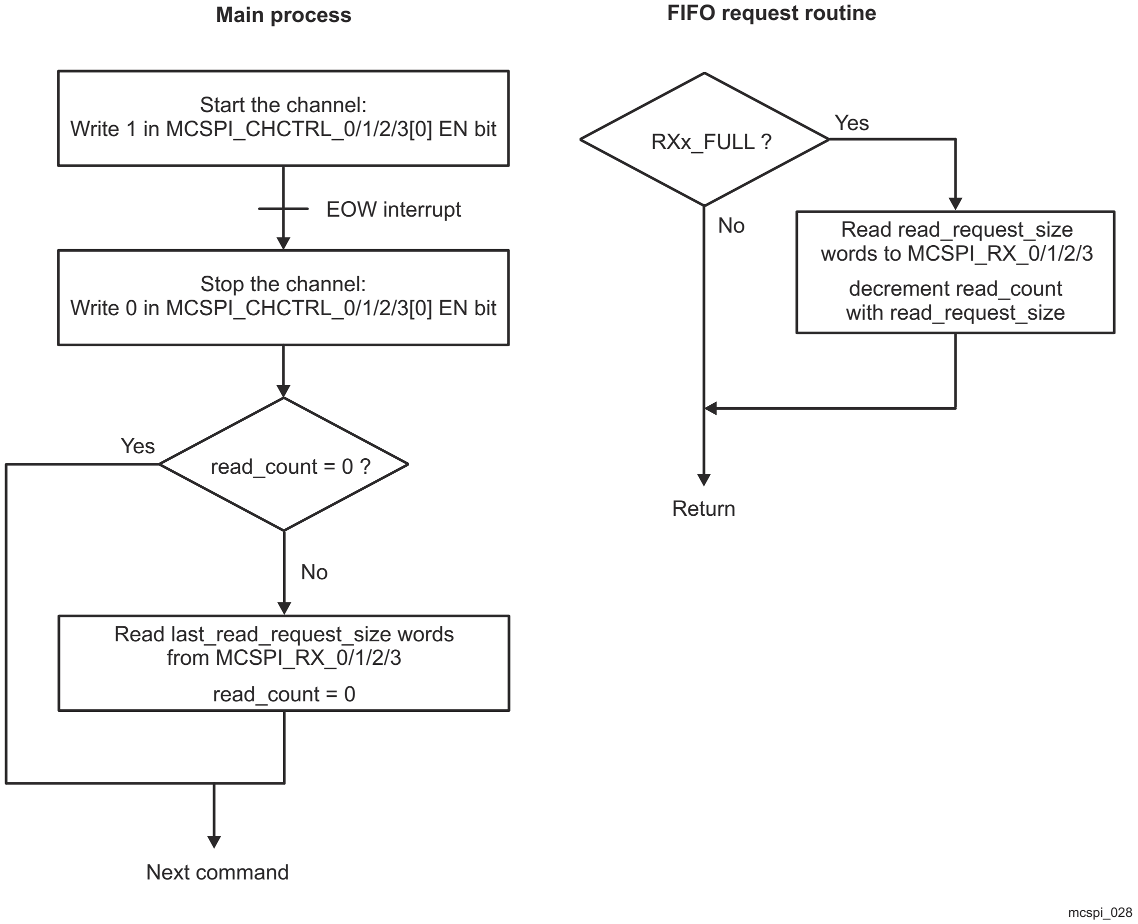


Figure 12-107. FIFO Mode Receive-Only With Word Count (Controller)

12.2.3.5.2.1.8.7 Receive-Only Without Word Count

Figure 12-108 shows the flow of a transfer in receive-only mode, with word count.

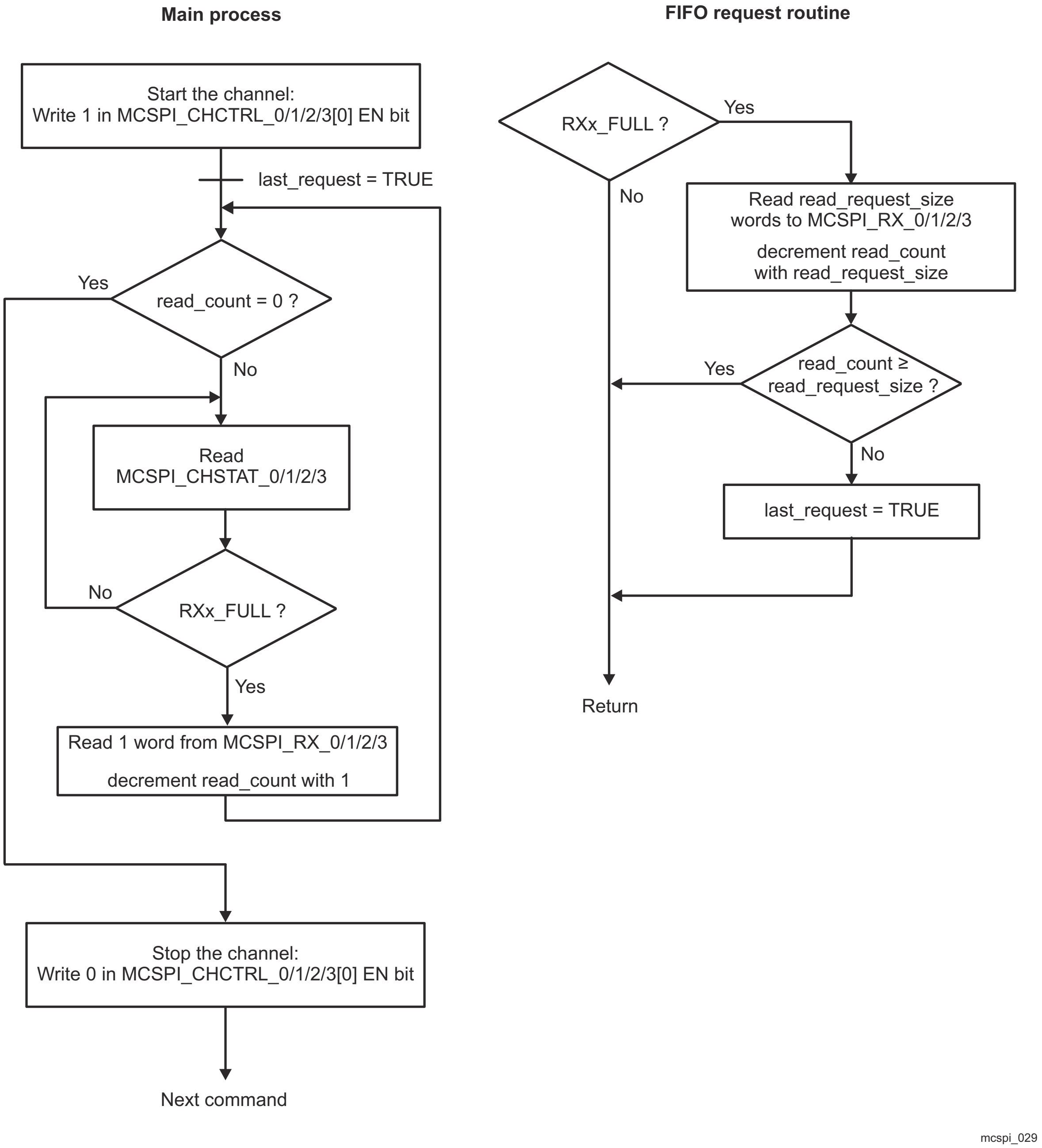


Figure 12-108. FIFO Mode Receive-Only Without Word Count (Controller)

12.2.3.5.2.1.9 Common Transfer Procedures Without FIFO – Polling Method

12.2.3.5.2.1.9.1 Receive-Only Procedure – Polling Method

Table 12-126 lists the receive-only procedure using the polling method.

Table 12-126. Receive-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-103.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Wait for end-of-transfer.	MCSPI_CH(i)STAT[2] EOT	=1
Read the receiver register.	MCSPI_RXi	0x-
Stop the channel if no more data is expected.	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.2.1.9.2 Receive-Only Procedure – Interrupt Method

Table 12-127 lists the receive-only procedure using the interrupt method.

Table 12-127. Receive-Only Procedure – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-103.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Enable the interrupt for the receiver register.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	1
Wait for interrupt.		
Read the status register.	MCSPI_IRQSTATUS[2] RX_FULL	1
Disable the interrupt if no more data is expected.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0
Stop the channel if no more data is expected.	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register.	MCSPI_RXi	0x-

12.2.3.5.2.1.9.3 Transmit-Only Procedure – Polling Method

Table 12-128 lists the transmit-only procedure using the polling method.

Table 12-128. Transmit-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-104.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Write the transmitter register with data.	MCSPI_TXi	0x-
Wait until end of transfer?	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel.	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.2.1.9.4 Transmit-and-Receive Procedure – Polling Method

Table 12-129 lists the transmit-and-receive procedure using the polling method.

Table 12-129. Transmit-and-Receive Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-105.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Write the transmitter register with data.	MCSPI_TXi	0x-
Wait until transmit/receive word?	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel.	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register.	MCSPI_RXi	0x-

12.2.3.5.3 Common Transfer Procedures Without FIFO – Polling Method

12.2.3.5.3.1 Receive-Only Procedure – Polling Method

Table 12-130 lists the receive-only procedure using the polling method.

Table 12-130. Receive-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-103.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Wait for end-of-transfer.	MCSPI_CH(i)STAT[2] EOT	=1
Read the receiver register.	MCSPI_RXi	0x-
Stop the channel if no more data is expected.	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.3.2 Receive-Only Procedure – Interrupt Method

Table 12-131 lists the receive-only procedure using the interrupt method.

Table 12-131. Receive-Only Procedure – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-103.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Enable the interrupt for the receiver register.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	1
Wait for interrupt.		
Read the status register.	MCSPI_IRQSTATUS[2] RX_FULL	1
Disable the interrupt if no more data is expected.	MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0
Stop the channel if no more data is expected.	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register.	MCSPI_RXi	0x-

12.2.3.5.3.3 Transmit-Only Procedure – Polling Method

Table 12-132 lists the transmit-only procedure using the polling method.

Table 12-132. Transmit-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-104.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Write the transmitter register with data.	MCSPI_TXi	0x-
Wait until end of transfer?	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel.	MCSPI_CH(i)CTRL[0] EN	0

12.2.3.5.3.4 Transmit-and-Receive Procedure – Polling Method

Table 12-133 lists the transmit-and-receive procedure using the polling method.

Table 12-133. Transmit-and-Receive Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 12-105.	
Start the channel.	MCSPI_CH(i)CTRL[0] EN	1
Write the transmitter register with data.	MCSPI_TXi	0x-
Wait until transmit/receive word?	MCSPI_CH(i)STAT[2] EOT	=1
Stop the channel.	MCSPI_CH(i)CTRL[0] EN	0
Read the receiver register.	MCSPI_RXi	0x-

12.2.4 Universal Asynchronous Receiver/Transmitter (UART)

This chapter describes the function, operation, and configuration of the Universal Asynchronous Receiver/ Transmitter (UART)/RS-485/Infrared Data Association (IrDA)/Consumer Infrared (CIR) module in the device.

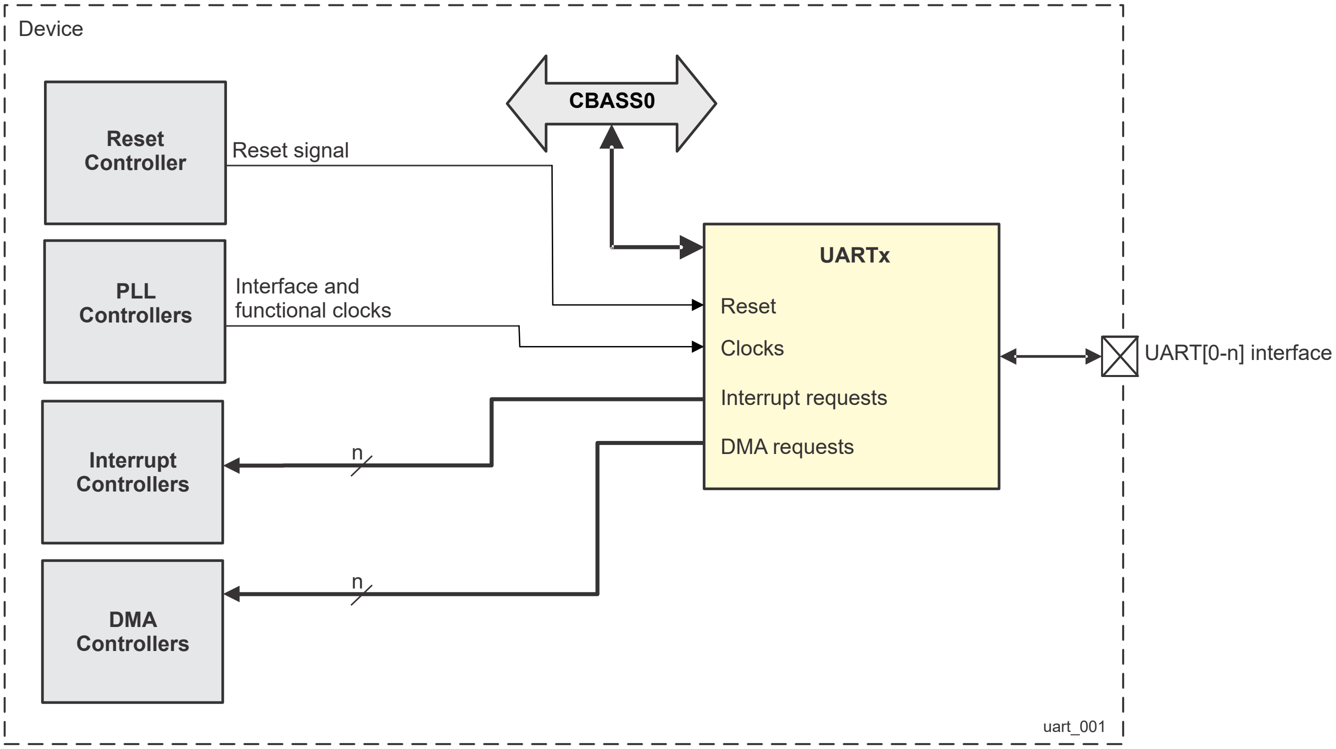
Note

UART and USART acronyms are used interchangeably in this section.

12.2.4.1 UART Overview

The UART is a peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

Figure 12-109 shows the UART modules overview.



A. x represents a valid instance of UART in a domain. See the device datasheet for specifics.

B. n represents the maximum number of available UART signals -1.

Figure 12-109. UART Modules Overview

12.2.4.1.1 UART Features

The UART includes the following features:

- 16C750-compatible
- RS-485 external transceiver auto flow control support
- 64-byte FIFO buffer for receiver and 64-byte FIFO buffer for transmitter
- Programmable interrupt trigger levels for FIFOs
- Programmable sleep mode
- The 48 MHz functional clock is default option and allows baud rates up to 3.6 Mbps
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Optional multi-drop transmission
- Configurable time-guard feature

- Configurable data format:
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- False start bit detection
- Line break generation and detection
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities
- Modem control functions (CTS, RTS)
- UART0 module in MAIN domain has extended modem control signals (DCD, RI, DTR, DSR)

12.2.4.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.2.4.1.3 IrDA Features

The IrDA includes the following features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications:
  - Slow infrared (SIR 115.2 KBAUD), medium infrared (MIR 0.576 MBAUD) and fast infrared (FIR 4.0 MBAUD) operations (very fast infrared (VFIR) is not supported)
  - Frame formatting: addition of variable beginning-of-frame (xBOF) characters and end-of-frame (EOF) characters
  - Uplink/downlink cyclic redundancy check (CRC) generation/detection
  - Asynchronous transparency (automatic insertion of break character)
  - Eight-entry status FIFO (with selectable trigger levels) to monitor frame length and frame errors
  - Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection
- IrDA mode when 48 MHz function clock is used

12.2.4.1.4 CIR Features

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on a user-definable frame structure and packet content.

The CIR includes the following features to provide CIR support for remote-control applications:

- Transmit and receive mode
- Free data format (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency
- 1/2, 5/12, 1/3, or 1/4 carrier duty cycle
- CIR mode when 48 MHz function clock is used

12.2.4.2 UART Environment

The , modules are hereinafter referred to as UART module.

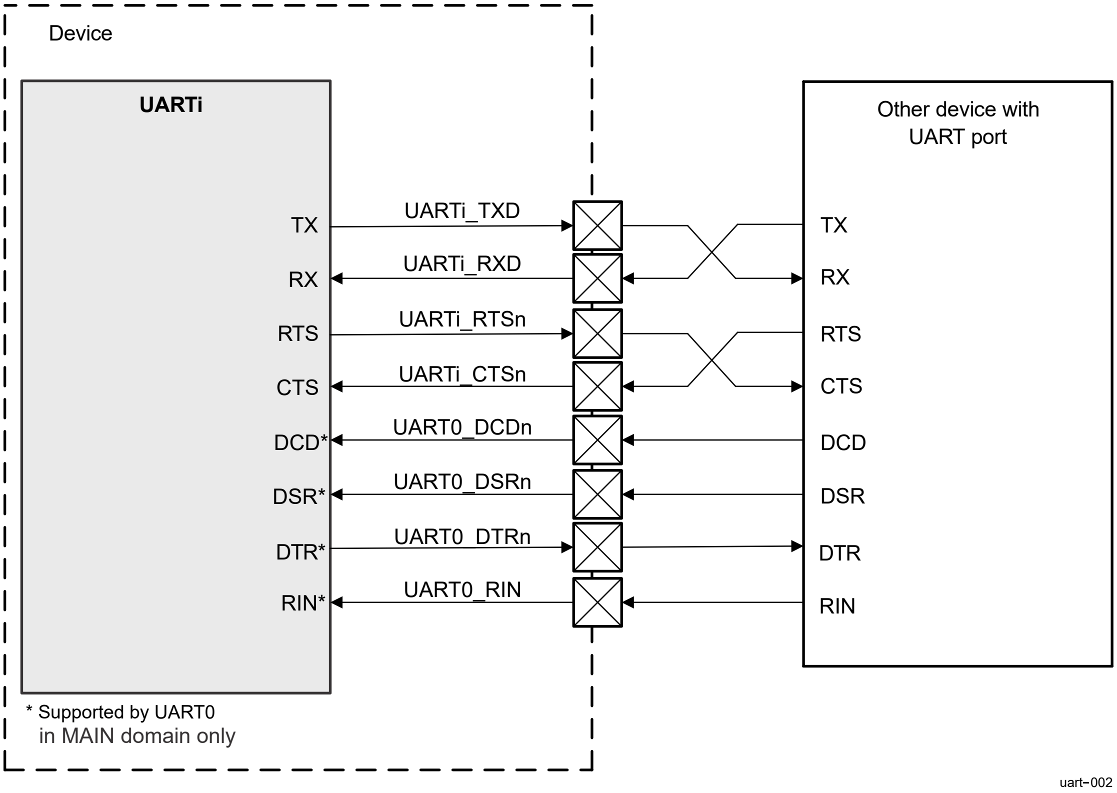
This section describes the UART/RS-485/IrDA/CIR external connections (environment).

- The UART interface is described in Section 12.2.4.2.1, *UART Functional Interfaces*.
- The RS-485 interface is described in Section 12.2.4.2.2, *RS-485 Functional Interfaces*.
- The IrDA interface is described in Section 12.2.4.2.3, *IrDA Functional Interfaces*.
- The CIR interface is described in Section 12.2.4.2.4, *CIR Functional Interfaces*.

12.2.4.2.1 UART Functional Interfaces

12.2.4.2.1.1 System Using UART Communication With Hardware Handshake

Each UART instance can be easily connected to the UART port of an external IC (see Figure 12-110).



A. i represents a valid instance of UART in a domain. See the device datasheet for valid domains and instances.

Figure 12-110. UART Mode Interface Signals

12.2.4.2.1.2 UART Interface Description

Table 12-134 lists the UART interface input/output (I/O) signals.

Table 12-134. UART I/O Signals

Module Pin Name	Device Level Signal Name	I/O[1]	Description	Module Pin Reset Value[2]
WKUP_UARTi[10]				
RX	WKUP_UARTi[10]_RXD	I	Serial data input	HiZ
TX	WKUP_UARTi[10]_TXD	O	Serial data output[3]	1
CTS	WKUP_UARTi[10]_CTSn	I	Clear to send[4]	HiZ
RTS	WKUP_UARTi[10]_RTSn	O	Request to send[5]	1
MCU_UARTi[10]				
RX	MCU_UARTi[10]_RXD	I	Serial data input	HiZ
TX	MCU_UARTi[10]_TXD	O	Serial data output[3]	1
CTS	MCU_UARTi[10]_CTSn	I	Clear to send[4]	HiZ
RTS	MCU_UARTi[10]_RTSn	O	Request to send[5]	1
UARTi[10] Modem Signals				
RX	UARTi[10]_RX	I	Serial data input	HiZ
TX	UARTi[10]_TX	O	Serial data output[3]	1
CTS	UARTi[10]_CTSn	I	Clear to send[4]	HiZ
RTS	UARTi[10]_RTSn	O	Request to send[5]	1
DCD	UARTi[10]_DCDn	I	Data Carrier Detect[6]	HiZ
DSR	UARTi[10]_DSRn	I	Data Set Ready[7]	HiZ
DTR	UARTi[10]_DTRn	O	Data Terminal Ready[8]	1
RIN	UARTi[10]_RIN	I	Ring Indicator[9]	HiZ

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) Because this pin is active high in IrDA mode and the output is muxed, this pin is set to low on reset (when the UART_MDR1[2-0] bit field is set to 0x7) and takes the defined inactive level of that signal corresponding to when and how the UART_MDR1 register is programmed; that is, the output is 1 (inactive for UART modem modes) and 0 (inactive for IrDA modes).

(4) Active-low modem status signal. Reading the UART_MSR[4] NCTS_STS bit checks the condition of CTS. Reading the UART_MSR[0] CTS_STS bit checks a change of state of CTS since the last read of the modem status register. The auto-CTS mode uses CTS to control the transmitter.

(5) When active (low), the module is ready to receive data. Setting the UART_MCR[1] RTS bit activates RTS signal, which becomes inactive as the result of a module reset, loopback mode, or clearing the UART_MCR[1] RTS bit. In auto-RTS mode, RTS signal becomes inactive as a result of the receiver threshold logic.

(6) Active-low modem status signal. The condition of DCD can be checked by reading the UART_MSR[7] NCD_STS bit. Any change in its state can be detected by reading the UART_MSR[3] DCD_STS bit.

(7) Active-low modem status signal. Reading the UART_MSR[5] NDSR_STS bit checks the condition of DSR. Reading the UART_MSR[1] DSR_STS bit checks a change of state of DSR since the last read of the UART_MSR register.

(8) When active (low), this signal informs the modem that the module is ready to communicate. It is activated by setting the UART_MCR[0] DTR bit.

(9) Active-low modem status signal. The condition of RIN can be checked by reading the UART_MSR[6] NRI_STS bit. Any change in its state can be detected by reading the UART_MSR[2] RI_STS bit.

(10) i represents a UART instance. See the device datasheet for available domains and UART instances.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.4.2.1.3 UART Protocol and Data Format

The UART device operates in three modes:

- UART 16× (<= 230.4 kbps)
- UART 16× with autobauding (>= 1200 bps and <= 115.2 kbps)
- UART 13× (>= 460.8 kbps)

CAUTION

To be used as a UART, the operating mode must be programmed appropriately in the UART_MDR1[2-0] MODE_SELECT bit field to select UART, IrDA, or CIR mode, and the UART_MDR3[4] DIR_EN bit field to select RS-485 mode.

The UART uses a wired interface for serial communication with a remote device.

The UART is functionally compatible with the TL16C750 UART and earlier designs such as the TL16C550.

Figure 12-111 shows the UART frame data format.

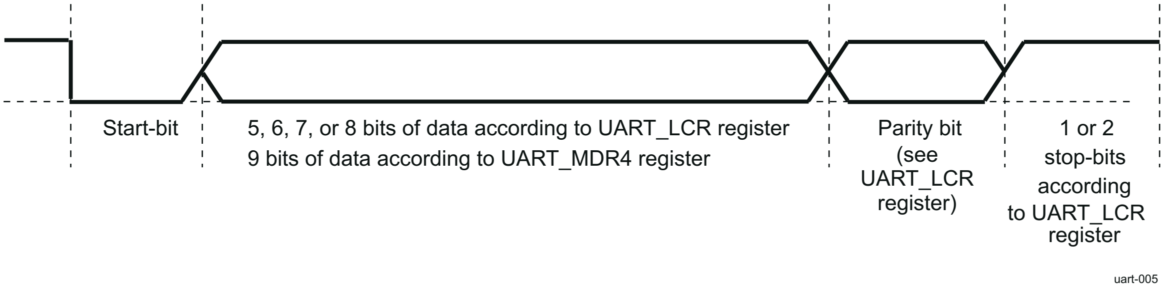
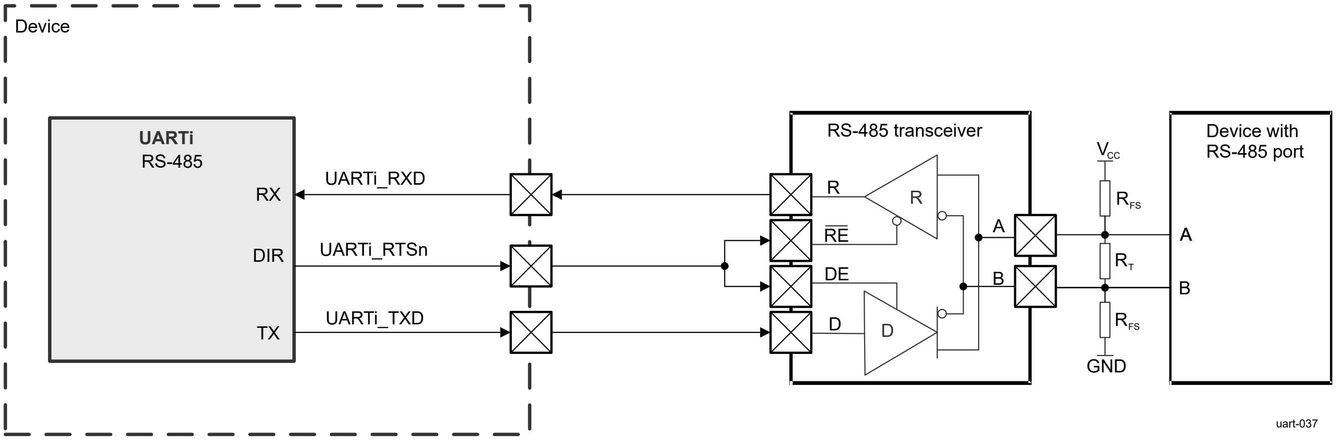


Figure 12-111. UART Frame Data Format

12.2.4.2.2 RS-485 Functional Interfaces

12.2.4.2.2.1 System Using RS-485 Communication

The RS-485 network physical layer consists of two-wire differential bus, usually twisted pair. External RS-485 transceiver IC is needed to access a RS-485 bus by the RS-485 mode. Figure 12-112 shows an example connection of an UART instance in RS-485 mode.



A. i represents a valid instance of UART in a domain. See the device data sheet for valid domains and instances.

Figure 12-112. RS-485 Mode Interface Signals

12.2.4.2.2.2 RS-485 Interface Description

Table 12-135 lists the RS-485 interface input/output (I/O) signals.

Table 12-135. UART I/O Signals (RS-485 Mode)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
			WKUP_UARTi(3)	
RX	WKUP_UARTi(3)_RXD	I	Serial data input	HiZ
TX	WKUP_UARTi(3)_TXD	O	Serial data output	1
DIR	WKUP_UARTi(3)_RTSn	O	RS-485 Direction	1

Table 12-135. UART I/O Signals (RS-485 Mode) (continued)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
			MCU_UARTi(3)	
RX	MCU_UARTi(3)_RXD	I	Serial data input	HiZ
TX	MCU_UARTi(3)_TXD	O	Serial data output	1
DIR	MCU_UARTi(3)_RTSn	O	RS-485 Direction	1
			UARTi(3)	
RX	UARTi(3)_RXD	I	Serial data input	HiZ
TX	UARTi(3)_TXD	O	Serial data output	1
DIR	UARTi(3)_RTSn	O	RS-485 Direction	1

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) i represents a valid UART instance. See the device datasheet for available domains and UART instances.

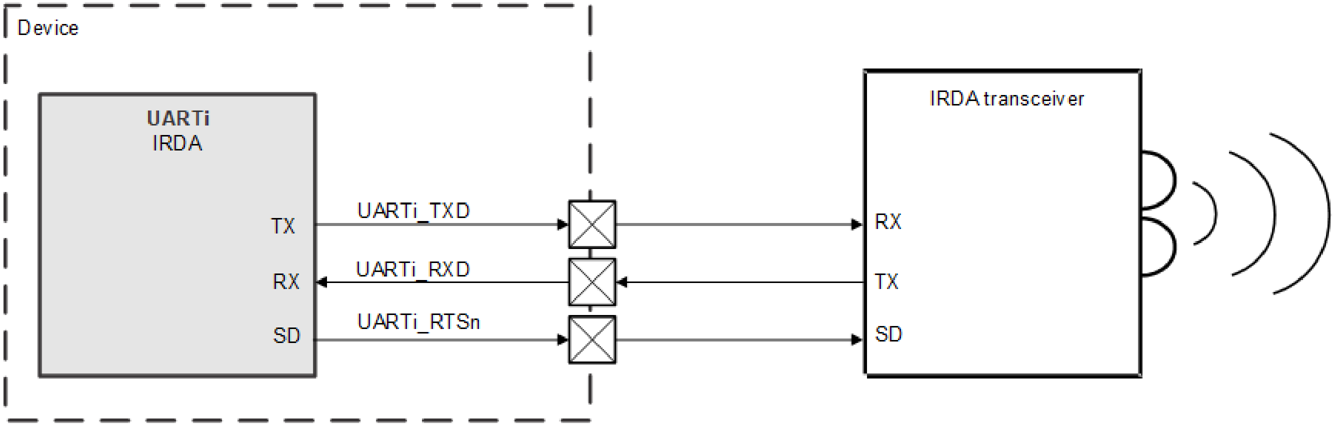
Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.4.2.3 IrDA Functional Interfaces

12.2.4.2.3.1 System Using IrDA Communication Protocol

Figure 12-113 shows an example connection of an UART instance to an external infrared transceiver in the IrDA modes (FIR, SIR, and MIR).



A. i represents a valid instance of UART in a domain. See the device data sheet for valid domains and instances.

Figure 12-113. IrDA Mode Interface Signals

12.2.4.2.3.2 IrDA Interface Description

Table 12-136 lists the IrDA interface I/O signals.

Table 12-136. UART I/O Signals (IrDA Mode)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
RX		I	Serial data input	HiZ
TX		O	Serial data output in IrDA modes (SIR, MIR, and FIR).(3)	0
SD		O	SD mode is used to configure the transceivers.(4)	1
RX		I	Serial data input	HiZ
TX		O	Serial data output in IrDA modes (SIR, MIR, and FIR).(3)	0
SD		O	SD mode is used to configure the transceivers.(4)	1

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) In other modes, this pin is set to the reset value (inactive state).
(4) The SD pinout (see UART_ACREG[6] SD_MOD bit).

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.4.2.3.3 IrDA Protocol and Data Format

12.2.4.2.3.3.1 SIR Mode

In SIR mode, data is transferred between the Host CPU and peripheral devices at speeds of up to 115.2 baud. A SIR transmit frame begins with start flags (a single 0xC0, a multiple 0xC0, or a single 0xC0 preceded by a number of 0xFF flags), followed by frame data and a CRC-16, and ends with a stop flag (0xC1).

The bit format for a single word uses 1 start-bit, 8 data bits, and 1 stop-bit, and is unaffected by the use and settings of the UART_LCR register.

The UART_BLR[6] XBOF_TYPE bit selects whether the 0xC0 or 0xFF start patterns are used when multiple start flags are required.

The SIR transmit state-machine attaches start flags, CRC-16, and stop flags, and checks the outgoing data to establish whether data transparency is required.

The SIR transparency is carried out if the outgoing data between the start and stop flags contains 0xC0, 0xC1, or 0x7D. If one of these start flags is about to be transmitted, the SIR state-machine sends an escape character (0x7D), inverts the fifth bit of the real data to be sent, and then sends this data immediately after the 0x7D character.

The SIR receive state-machine recovers the receive clock, removes the start flags and any transparency from the incoming data, and determines the frame boundary with reception of the stop flag. The SIR state-machine also checks for errors such as a frame abort (0x7D character followed immediately by a 0xC1 stop flag without transparency), a CRC error, or a frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to find possible errors of the received frame.

Note

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. See the description of the UART_ACREG[5] DIS_IR_RX bit. This applies to all three modes: SIR, MIR, and FIR.

Infrared output in SIR mode can be 1.6-μs or 3/16 encoding, selected by the UART_ACREG[7] PULSE_TYPE bit. In 1.6-μs encoding, the infrared pulse width is 1.6 μs; and in 3/16th encoding, the infrared pulse width is 3/16th of a bit duration (1/baud rate).

For back-to-back frames, the transmitting device must send at least two start flags at the start of each frame.

Note

Reception supports variable-length stop-bits.

12.2.4.2.3.3.1.1 Frame Format

Figure 12-114 shows the IrDA SIR frame format.

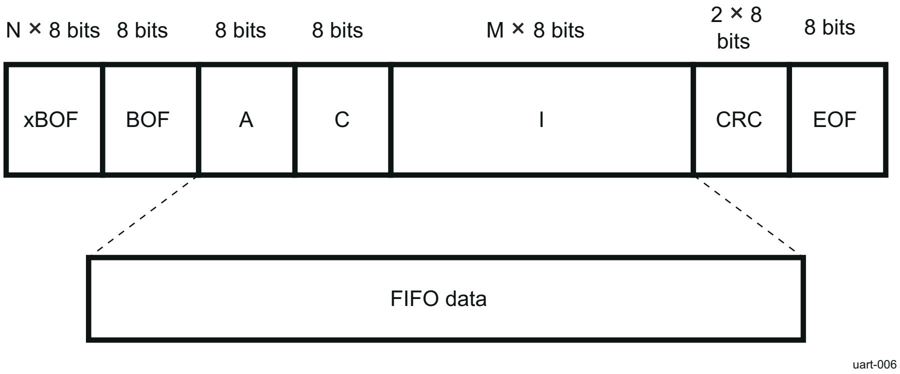


Figure 12-114. IrDA SIR Frame Format

The CRC is applied on the address (A), control (C), and information (I) bytes.

Note

The two words of CRC are written to the FIFO in reception.

12.2.4.2.3.3.1.2 Asynchronous Transparency

Before transmitting a byte, the UART IrDA controller examines each byte of the payload and the CRC field (between BOF and EOF). For each byte equal to 0xC0 (BOF), 0xC1 (EOF), or 0x7D (control escape), the controller performs certain tasks:

- In transmission:
  - Inserts a control escape (CE) byte preceding the byte
  - Complements bit 5 of the byte (that is, exclusive ORs the byte with 0x20)

  The byte sent for the CRC computation is the initial byte written in the TX FIFO (before the XOR with 0x20).
- In reception:

  For the A, C, I, and CRC fields:
  - Compares the byte with the CE byte; if they are not equal, sends the byte to the CRC detector and stores it in the RX FIFO.
  - If the byte is equal to the CE byte, discards the CE byte
  - Complements bit 5 of the byte following the CE
  - Sends the complemented byte to the CRC detector and stores it in the RX FIFO

12.2.4.2.3.3.1.3 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

When a 0x7D character that is followed immediately by a 0xC1 character is received without transparency, the receiver treats the frame as an aborted frame.

12.2.4.2.3.3.1.4 Pulse Shaping

The SIR mode supports the 3/16 and the 1.6-µs pulse duration methods. The UART_ACREG[7] PULSE_TYPE bit selects the pulse-width method in transmit mode.

12.2.4.2.3.3.1.5 Encoder

Serial data from the transmit state-machine are encoded to transmit data to the optoelectronics. While the TX FIFO output is high, the TX line is always low, and the counter used to form a pulse on TX is cleared continuously.

After the TX FIFO output resets to 0, TX rises on the falling edge of the seventh 16XCLK. On the falling edge of the tenth 16XCLK pulse, TX falls, creating a 3-clock-wide pulse. While the TX FIFO output stays low, a pulse is transmitted during the seventh clock to the tenth clock of each 16-clock bit cycle.

Figure 12-115 shows the IrDA SIR encoding mechanism.

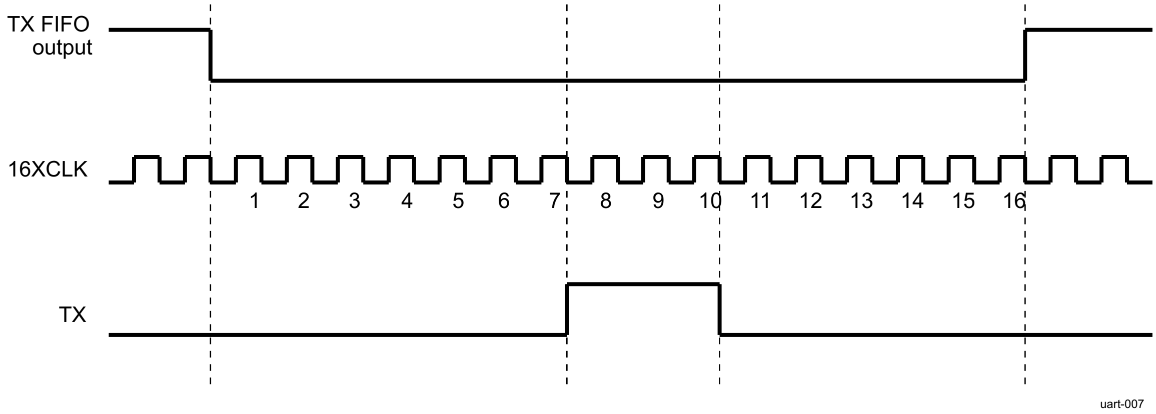


Figure 12-115. IrDA SIR Encoding Mechanism

12.2.4.2.3.3.1.6 Decoder

After reset, the RX FIFO input is high and the 4-bit counter is cleared. When a rising edge is detected on RX, the RX FIFO input falls on the next rising edge of 16XCLK with sufficient setup time. The RX FIFO input stays low for 16 cycles (16XCLK) and then returns to high as required by the IrDA specification. As long as no pulses (rising edges) are detected on the RX, the RX FIFO input remains high.

Figure 12-116 shows the IrDA SIR decoding mechanism.

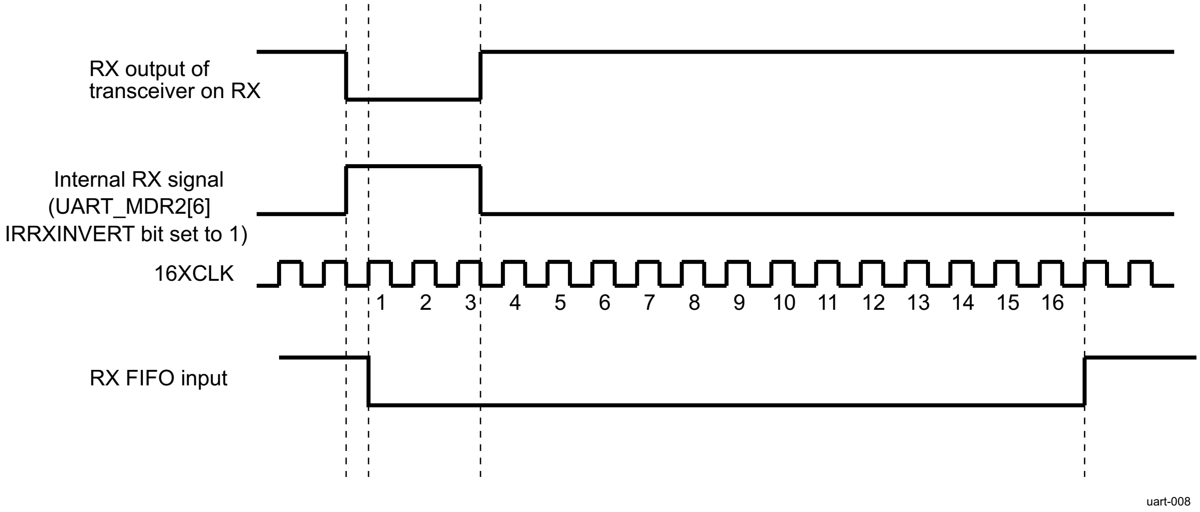


Figure 12-116. IrDA SIR Decoding Mechanism

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. The operation of the RX input can be disabled using the UART_ACREG[5] DIS_IR_RX bit. The UART_MDR2[6] IRRXINVERT bit can invert the signal from the transceiver (RX) pin to the IR RX logic in the UART. This inversion is performed by default.

12.2.4.2.3.3.1.7 IR Address Checking

In all IR modes, when address checking is enabled by setting the UART_EFR[1-0] bit field (see Table 12-137), only frames intended for the device are written to the RX FIFO. This is to avoid receiving frames not meant for this device in a multipoint infrared environment. To program two frame addresses that the UARTi receives in IrDA mode, use the UART_XON1_ADDR1[7-0] and UART_XON2_ADDR2[7-0] bit fields.

Table 12-137. UART_EFR[1-0] IR Address Checking Options

UART_EFR[1]	UART_EFR[0]	IR Address Checking
0	0	All address-checking operations disabled
0	1	Only address 1 checking enabled
1	0	Only address 2 checking enabled
1	1	All address-checking operations enabled

12.2.4.2.3.3.2 SIR Free-Format Mode

To allow complete software flexibility when transmitting and receiving infrared data packets, the SIR free-format (FF) mode is a subfunction of the existing SIR mode. In FF mode, all frames going to and from the FIFO buffers are untouched with respect to appending and removing control characters and CRC values.

The FF mode corresponds to a UART mode with a pulse modulation of 3/16 of baud rate pulse width.

For example, a normal SIR packet has BOF control and CRC error-checking data appended (transmitting) or removed (receiving) from the data going to and from the FIFOs.

Figure 12-117 shows SIR FF mode.

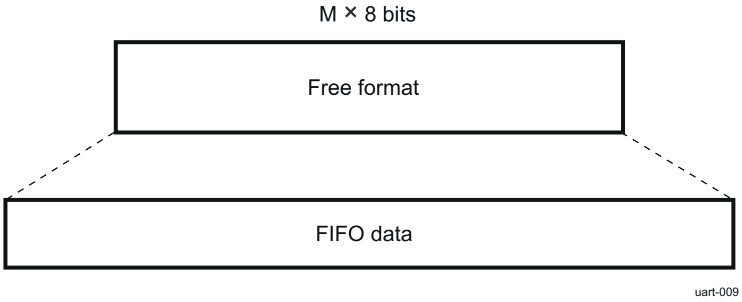


Figure 12-117. SIR FF Mode

In SIR FF mode, the Host CPU software must construct (that is, encode and decode) the entire FIFO data packet.

12.2.4.2.3.3.3 MIR Mode

In MIR mode, data is transferred between the Host CPU and the peripheral devices at 0.576 Mbps or 1.152 Mbps. A MIR transmit frame starts with at least two start flags, followed by a frame data and a CRC-16, and ends with a stop flag (see Figure 12-118).

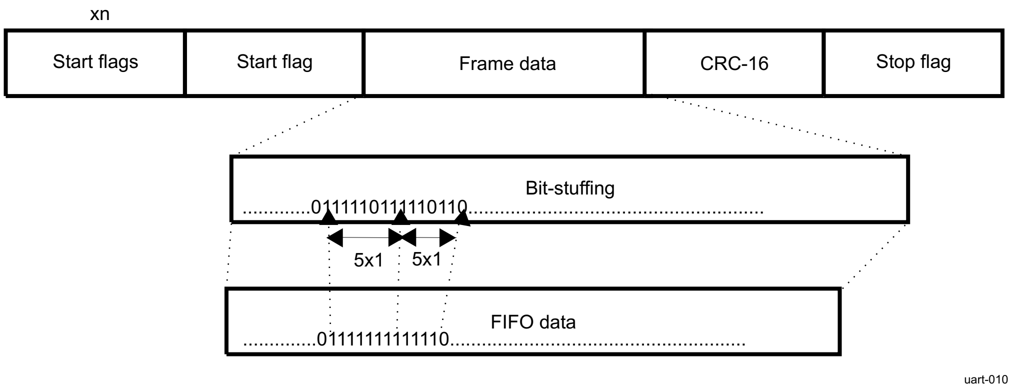


Figure 12-118. MIR Transmit Frame Format

On transmit, the MIR state-machine attaches start flags, a CRC-16, and stop flags, as in SIR mode. All fields are transmitted least-significant bit (LSB) of each byte first.

In MIR mode:

- The state-machine looks for consecutive 1s in the frame data and automatically inserts 0 after five consecutive 1s (this is called bit-stuffing).
- 0x7E is used for start and stop flags (unambiguously, not data, because of bit-stuffing).
- An abort sequence requires a minimum of seven consecutive 1s (unambiguously, not data, because of bit-stuffing).
- Back-to-back frames are allowed with three or more stop flags between them. If two consecutive frames are not back to back, the gap between the last stop flag of the first frame and the start flag of the second frame must be separated by at least seven bit durations.

On receive, the MIR receive state-machine recovers the receive clock, removes the start flags, destuffs the incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as frame abort, CRC error, and frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

12.2.4.2.3.3.3.1 MIR Encoder/Decoder

To meet the MIR baud rate tolerance of 0.1 percent with a 48-MHz clock input, a 42-41-42 encoding/decoding adjustment is performed. The reference start point is the first start flag, and the 42-41-42 cyclic pattern is repeated until the stop flag is sent or detected.

The jitter created this way is within MIR tolerances. The pulse width is not exactly 1/4, but it is within the tolerances defined by IrDA specifications.

Figure 12-119 shows the MIR baud rate adjustment mechanism.

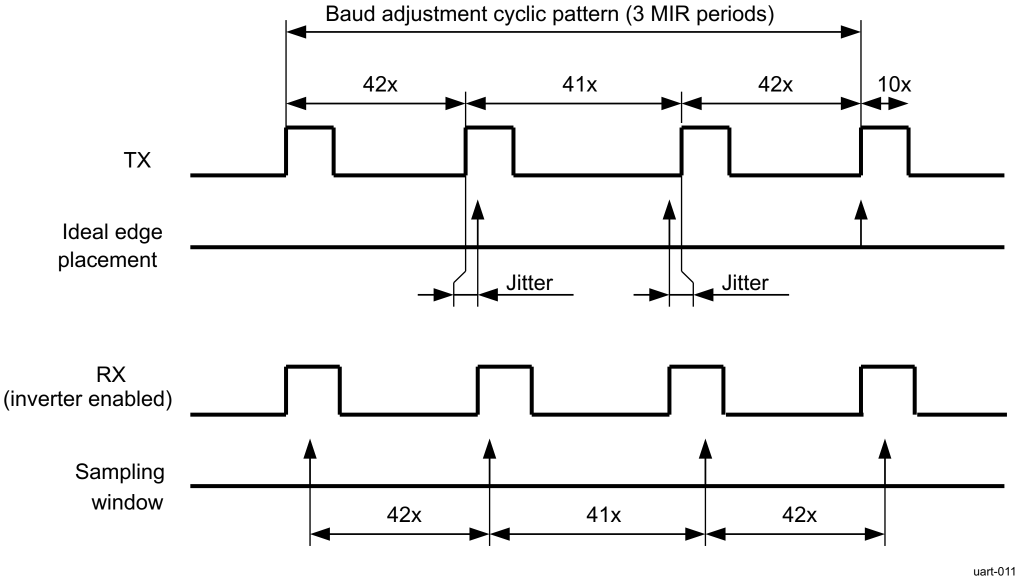


Figure 12-119. MIR Baud Rate Adjustment Mechanism

12.2.4.2.3.3.3.2 SIP Generation

In the MIR and FIR operation modes, the transmitter must send a serial infrared interaction pulse (SIP) at least once every 500 ms. The SIP informs slow devices (operating in SIR mode) that the medium is occupied.

Figure 12-120 shows the SIP.

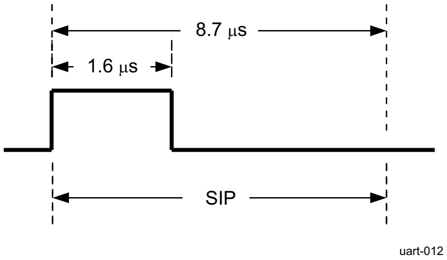


Figure 12-120. SIP

12.2.4.2.3.3.4 FIR Mode

In FIR mode, data is transferred between the Host CPU and the peripheral devices at 4 Mbps. A FIR transmit frame starts with a preamble that is followed by a start flag, frame data, CRC-32, and ends with a stop flag.

Figure 12-121 shows the FIR transmit frame format.

Figure 12-121. FIR Transmit Frame Format

Preamble (16x)	Start flag	Frame data	CRC-32	Stop flag

On transmit, the FIR transmit state-machine attaches the preamble, start flag, CRC-32, and stop flag. An abort sequence requires at least two transmissions of 0000. Back-to-back frames are allowed, but each frame must be complete.

The state-machine also encodes the transmit data into 4-PPM format (see Table 12-138) and generates the SIP (see Section 12.2.4.2.3.3.3.2, *SIP Generation*).

Table 12-138. 4-PPM Format

Data Bit Pair (Bin)	4-PPM Data Symbol (Bin)
00	1000
01	0100

Table 12-138. 4-PPM Format (continued)

Data Bit Pair (Bin)	4-PPM Data Symbol (Bin)
10	0010
11	0001

The four symbols described in Table 12-138 are the legal, encoded data symbols. All other combinations are illegal for encoding data. Some of these illegal symbols are used in the definition of the preamble, start flag, and stop flag because they are unambiguously not data (see Table 12-139).

Table 12-139. FIR Preamble, Start Flag, and Stop Flag

Frame Part	Transmitted Frame (Bin)
Preamble	1000 0000 1010 1000 (16 repeated transmissions)
Start flag	0000 1100 0000 1100 0110 0000 0110 0000
Stop flag	0000 1100 0000 1100 0000 0110 0000 0110

All fields are transmitted LSBs of each byte first (see Table 12-140).

Table 12-140. FIR Data Byte Transmission Order Example

Data Byte (Hex)	Data Byte Pair (Bin)	4-PPM Data Symbol (Bin)	Transmission Order
0x0B	00	1000	4
	00	1000	3
	10	0010	2
	11	0001	1

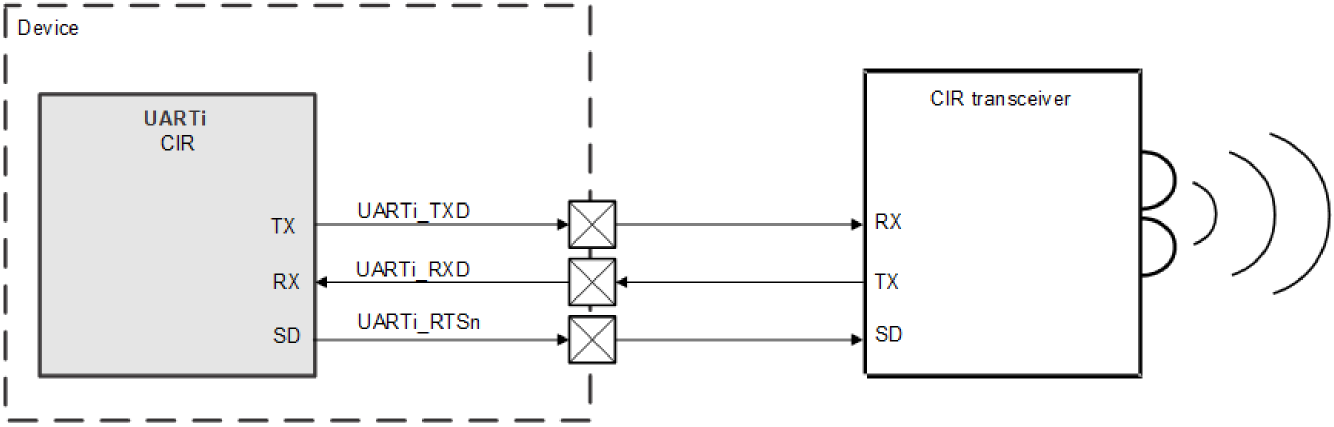
On receive, the FIR receive state-machine recovers the receive clock, removes the preamble and the start flag, decodes the 4-PPM incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as illegal symbol, CRC error, and frame-length error. At the end of a frame reception, the Host CPU reads the line status register (UART_LSR_IRDA) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

12.2.4.2.4 CIR Functional Interfaces

12.2.4.2.4.1 System Using CIR Communication Protocol With Remote Control

All UART modules can be connected to an external infrared transceiver in CIR mode. Figure 12-122 shows an example connection of a UART instance in CIR mode.



A. i represents a valid instance of UART in a domain. See the device data sheet for valid domains.

Figure 12-122. CIR Mode Interface Signals

12.2.4.2.4.2 CIR Interface Description

Table 12-141 lists the CIR interface I/O signals.

Table 12-141. UART I/O Signals (CIR Mode)

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
RX		I	Serial data input	HiZ
TX		O	Serial data output in CIR mode. [3]	0
SD		O	SD mode is used to configure the transceivers.[4]	1
			UART[0-9]	
RX		I	Serial data input	HiZ
TX		O	Serial data output in CIR mode. [3]	0
SD		O	SD mode is used to configure the transceivers.[4]	1

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) In other modes, this pin is set to the reset value (inactive state).
(4) The SD pinout is an inverted value of the UART_ACREG[6] SD_MOD bit.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.2.4.2.4.3 CIR Protocol and Data Format

In CIR mode, the infrared operation functions as a programmable (universal) remote control.

The CIR mode uses a variable PWM technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on user-defined frame structure and packet content.

12.2.4.2.4.3.1 Carrier Modulation

Each modulated pulse that constitutes a digit is a train of on/off pulses (see Figure 12-123).

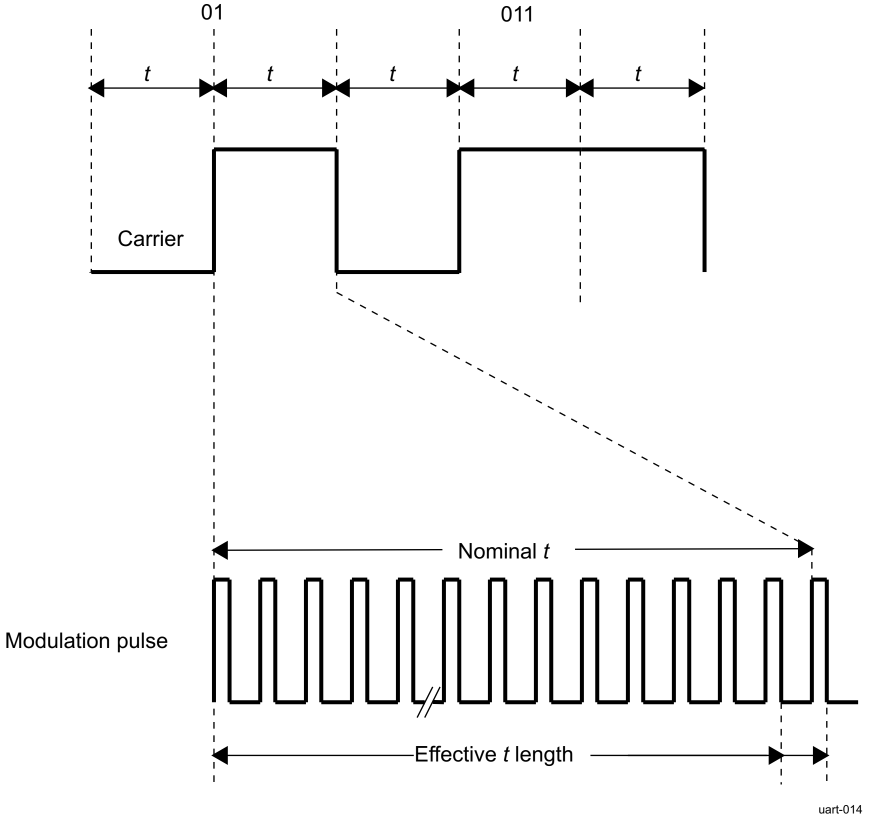


Figure 12-123. CIR Pulse Modulation

12.2.4.2.4.3.2 Pulse Duty Cycle

The programmer can choose one of four duty cycles for modulation pulses by setting the appropriate value in the UART_MDR2[5-4] CIR_PULSE_MODE bit field (1/4, 1/3, 5/12, or 1/2).

Figure 12-124 shows the CIR modulation duty cycles.

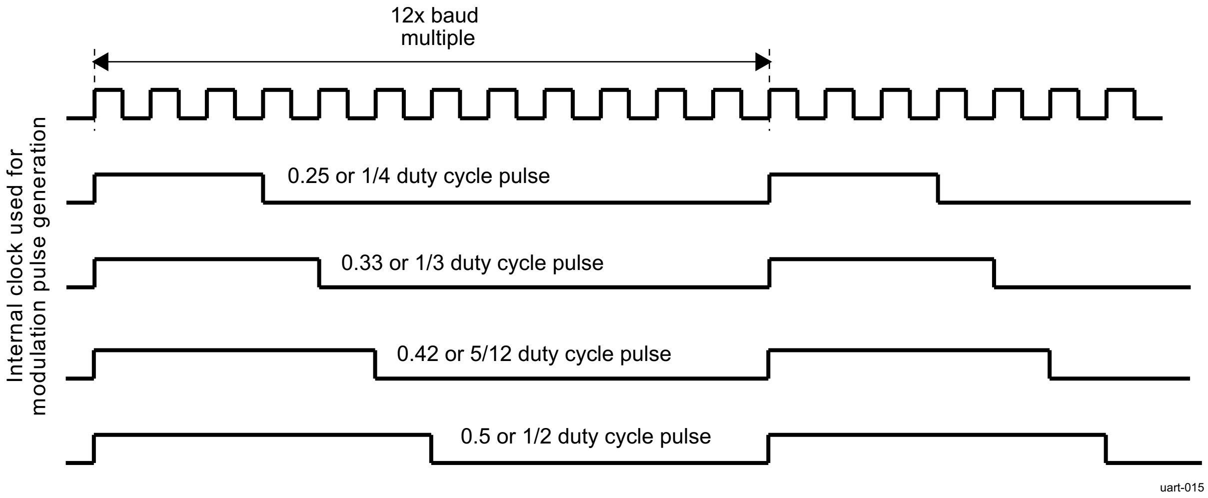


Figure 12-124. CIR Modulation Duty Cycle

The transmission logic ensures that all pulses are transmitted completely (no cutoff during transmission). While transmitting continuous bytes back-to-back, no delay is inserted between 2 transmitted bytes. Thus, software must handle the delay between consecutively transmitted bytes if the receiving end requires it.

12.2.4.2.4.3.3 Consumer IR Encoding/Decoding

There are two methods of encoding for remote-control applications:

- Pulse duration encoding (time-extended bit forms): A variable pulse distance, or duration, in which the difference between logic 1 and logic 0 is the length of the pulse width
- Biphase encoding: The encoding of logic 0 and logic 1 is in the change of signal level from 1 to 0 or 0 to 1, respectively.

Japanese manufacturers favor pulse duration encoding; European manufacturers favor biphase encoding.

CIR mode uses a completely flexible free-format encoding in which 1 is transmitted from the TX FIFO as a modulated pulse with duration *t*.

Similarly, 0 is transmitted as a blank duration T. The Host CPU constructs and deciphers the protocol of the data. For example, the RC-5 protocol using Manchester encoding can be emulated as using a 01 pair for 1 and a 10 pair for 0 (see Figure 12-125).

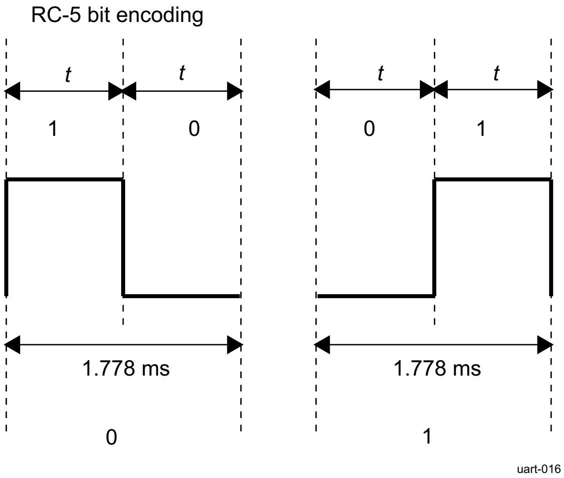


Figure 12-125. UART RC-5 Bit Encoding

Because CIR mode logic does not impose a fixed format for infrared packets of data, the Host CPU software can define the format using simple data structures that are then modulated into an industry standard, such as RC-5 or SIRC. To send a sequence of 0101 in RC-5, the Host CPU software must write an 8-bit binary character of 10011001 to the data FIFO of the UART.

For SIRC, the modulation length (multiples of *t*) is used to distinguish between 1 and 0. The subsequent SIRC digits show the difference in encoding between this and, for example, RC-5. The pulse width is extended for one digit.

Figure 12-126 shows SIRC bit encoding.

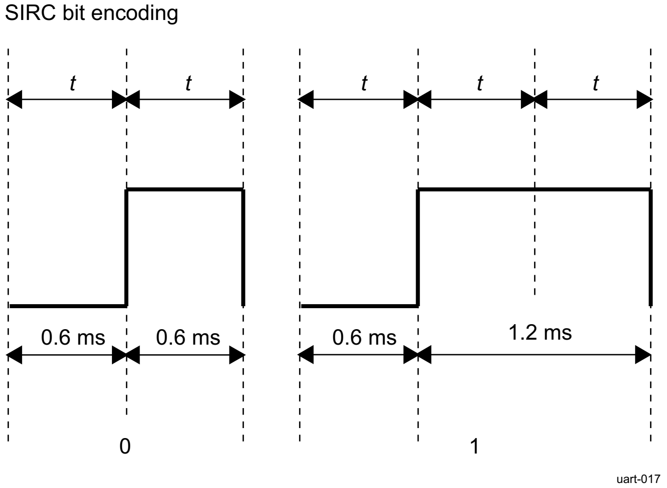


Figure 12-126. UART SIRC Bit Encoding

To construct comprehensive packets constituting remote-control commands, the Host CPU software must combine a number of 8-bit data characters in a sequence that follows one of the universally accepted formats.

Figure 12-127 shows a standard RC-5 frame as detected by UART in CIR mode (the SIRC format follows this). Each field in RC-5 can be considered as two *t* pulses (digital bits) from the TX FIFO.

S1	S2	T	A4	A3	A2	A1	A0	C5	C4	C3	C2	C1	C0

uart-018

Figure 12-127. UART RC-5 Standard Packet Format

Where:

S1, S2:	Start-bits (always 1)
T:	Toggle bit
A4..A0:	Address (or system) bits
C5..C0:	Command bits

The toggle bit T changes when a new command is transmitted to detect when the same key is pressed twice (effectively receiving the same data from the host consecutively). A brief delay in the transmission of the same command is detected by the use of the toggle bit because a code is sent while the Host CPU transmits characters to the UART for transmission. The address bits define the machine or device for which the infrared transmission is intended, and the command defines the operation.

To accommodate an extended RC-5 format, the S2 bit is replaced by an additional command bit (C6) that lets the command range increase to 7 bits. This format is known as the extended RC-5 format.

The SIRC encoding uses the duration of modulation for mark and space; therefore, the duration of data bits in the standard frame length varies.

Figure 12-128 shows the packet format and bit encoding. As Figure 12-129 shows, 1 start-bit of 2.4 ms and control codes are followed by data that constitute the entire frame.

S	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4

uart-019

Figure 12-128. UART SIRC Packet Format

Note

The encoding must take a standard duration, but the contents of the data can vary. This implies that the control software for sending and receiving data packets must exercise a scheme of interpacket delay, where successive packets can be sent only after a real-time delay expires.

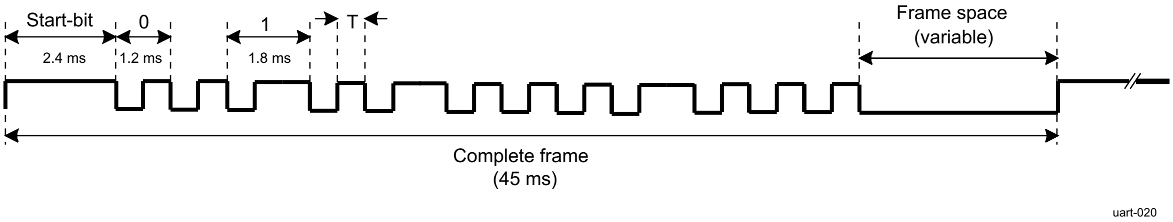


Figure 12-129. UART SIRC Bit Transmission Example

Note

This document does not describe all encoding methods and techniques; the previous information discusses the considerations required to employ different encoding methods for different industry-standard protocols. See industry-standard documentation for specific methods of encoding and protocol use.

12.2.4.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.2.4.4 UART Functional Description

12.2.4.4.1 UART Block Diagram

The UART module can be divided into three main blocks:

- FIFO management
- Mode selection
- Protocol formatting

FIFO management is common to all functions and enables the transmission and reception of data from the host processor point of view.

There are two modes:

- Function mode: Routes the data to the chosen function (UART, RS-485, IrDA, or CIR) and enables the mechanism corresponding to the chosen function.
- Register mode: Enables conditional access to registers.

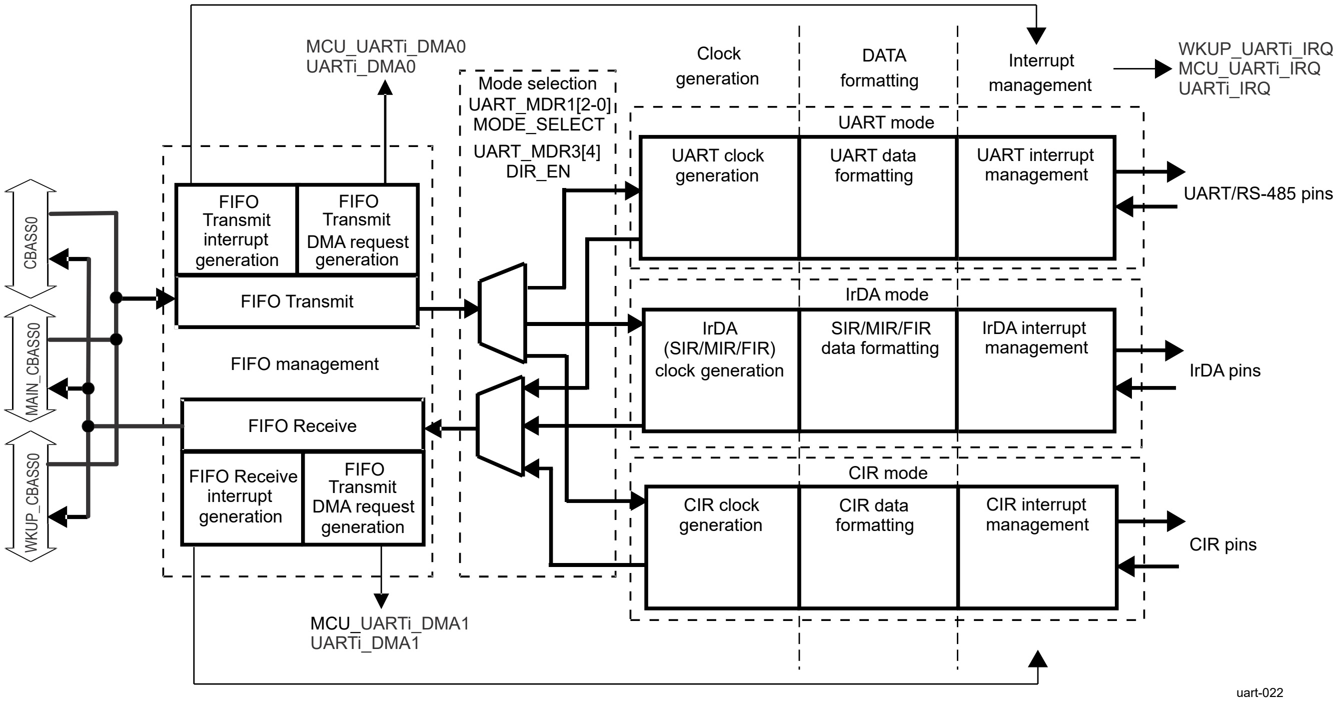
For more information about mode configuration, see Section 12.2.4.4.7, *Mode Selection*.

Protocol formatting has three subcategories:

- Clock generation: The 48-MHz input clock generates all necessary clocks.
- Data formatting: Each function uses its own state-machine that is responsible for the transition between FIFO data and frame data associated with it.
- Interrupt management: Different interrupt types are generated depending on the chosen function. In each mode, when an interrupt is generated, the UART_IIR_UART register indicates the interrupt type.
  - UART mode interrupts: Seven interrupts prioritized in six different levels
  - IrDA mode interrupts: Eight interrupts. The interrupt line is activated when any interrupt is generated (there is no priority).
  - CIR mode interrupts: A subset of existing IrDA mode interrupts is used.

In parallel with these functional blocks, a power-saving strategy exists for each function.

Figure 12-130 is the UART block diagram.



A. i represents a valid instance of UART in a domain. See the device datasheet for valid domains and instances.

Figure 12-130. UART Functional Block Diagram

12.2.4.4.2 UART Clock Configuration

Each UART uses a 48-MHz functional clock for its logic and to generate external interface signals. Each UART uses an interface clock for register accesses.

12.2.4.4.3 UART Software Reset

The UART_SYSC[1] SOFTRESET bit controls the software reset; setting this bit to 1 triggers a software reset functionally equivalent to hardware reset.

12.2.4.4.3.1 Independent TX/RX

The receiver and transmitter are enabled by default after reset. Software can choose to disable, re-enable or to reset either the RX or the TX side independently of the other through the UART_ECR register.

12.2.4.4.4 UART Power Management

12.2.4.4.4.1 UART Mode Power Management

12.2.4.4.4.1.1 Module Power Saving

In UART modes, sleep mode is enabled by setting the UART_IER_UART[4] SLEEP_MODE bit to 1 (when the UART_EFR[4] ENHANCED_EN bit is set to 1).

Sleep mode is entered when all of the following conditions exist:

- The serial data input line, RX, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.
- The only pending interrupts are THR interrupts.

Sleep mode is a good way to lower UART power consumption, but this state can be achieved only when the UART is set to modem mode. Therefore, even if the UART has no key role functionally, it must be initialized in a functional mode to take advantage of sleep mode.

In sleep mode, the module clock and baud rate clock are stopped internally. Because most registers are clocked by these clocks, this greatly reduces power consumption. The module wakes up when a change is detected on the RX line, when data is written to the TX FIFO, and when there is a change in the state of the modem input pins.

An interrupt can be generated on a wake-up event by setting the UART_SCR[4] RX_CTS_WU_EN bit to 1. To understand how to manage the interrupt, see Section 12.2.4.4.5.1.2, *Wake-Up Interrupt*.

Note

There must be no writing to the divisor latches, UART_DLL and UART_DLH, to set the baud clock (BCLK) while in sleep mode. It is advisable to disable sleep mode using the UART_IER_UART[4] SLEEP_MODE bit before writing to the UART_DLL or UART_DLH register.

12.2.4.4.4.1.2 System Power Saving

Sleep and auto-idle modes are embedded power-saving features. Power-reduction techniques can be applied at the system level by shutting down certain internal clock and power domains of the device.

The UART supports an idle req/idle ack handshaking protocol used at the system level to shut down the UART clocks in a clean and controlled manner and to switch the UART from interrupt-generation mode to wake-up generation mode for unmasked events (see the UART_SYSC[2] ENAWAKEUP bit and the UART_WER register).

For more information, see *Power* in the *Device Configuration*.

12.2.4.4.4.2 IrDA Mode Power Management

12.2.4.4.4.2.1 Module Power Saving

In IrDA modes, sleep mode is enabled by setting the UART_MDR1[3] IR_SLEEP bit to 1.

Sleep mode is entered when all of the following conditions exist:

- The serial data input line, RXD, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.
- No interrupts are pending except THR interrupts.

The module wakes up when a change is detected on the RXD line or when data is written to the TX FIFO.

12.2.4.4.4.2.2 System Power Saving

System power saving for the IrDA mode has the same function as for the UART mode (see Section 12.2.4.4.4.1.2, *System Power Saving*).

12.2.4.4.4.3 CIR Mode Power Management

12.2.4.4.4.3.1 Module Power Saving

Module power saving for the CIR mode has the same function as for the IrDA mode (see Section 12.2.4.4.4.2.1, *Module Power Saving*).

12.2.4.4.4.3.2 System Power Saving

System power saving for the CIR mode has the same function as for the UART mode (see Section 12.2.4.4.4.1.2, *System Power Saving*).

12.2.4.4.4.4 Local Power Management

Table 12-142 describes power-management features available for the UART.

Note

For information about source clock gating and the sleep/wake-up transitions description, see *Power* in the *Device Configuration*.

Table 12-142. UART Local Power-Management Features

Feature	Registers	Description
Clock autogating	UART_SYSC[0] AUTOIDLE	This bit allows local power optimization in the module by gating the clock on interface activity or gating the UARTi_FCLK clock on internal activity.
Peripheral idle modes	UART_SYSC[4-3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Clock activity	N/A	Feature not available
Controller standby modes	N/A	Feature not available
Global wake-up enable	UART_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.
Wake-Up sources enable	N/A	Feature not available

12.2.4.4.5 UART Interrupt Requests

12.2.4.4.5.1 UART Mode Interrupt Management

12.2.4.4.5.1.1 UART Interrupts

The UART mode includes seven possible interrupts prioritized to six levels.

When an interrupt is generated, the interrupt identification register (UART_IIR_UART) sets the UART_IIR_UART[0] IT_PENDING bit to 0 to indicate that an interrupt is pending, and indicates the type of interrupt through the UART_IIR_UART[5-1] bit field. Table 12-143 summarizes the interrupt control functions.

Table 12-143. UART Mode Interrupts

IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
000001	N/A	No Interrupt	N/A	N/A
000110	1	Receiver line status	OE, FE, PE, or BI errors occur in characters in the RX FIFO.	FE, PE, BI: Read the UART_RHR register. OE: Read the UART_LSR_UART register.
001100	2	RX time-out	Stale data in RX FIFO	Read the UART_RHR register.

Table 12-143. UART Mode Interrupts (continued)

IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
000100	2	RHR interrupt	DRDY (data ready) (FIFO disabled) RX FIFO above trigger level (FIFO enabled)	Read the UART_RHR register until the interrupt condition disappears
000010	3	THR interrupt	TFE (THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR until the interrupt condition disappears
000000	4	Modem status	See the UART_MSR register.	Read the MSR register
010000	5	XOFF interrupt/ special character interrupt	Receive XOFF characters/special character	Receive XON character(s), if XOFF interrupt/read of the UART_IIR_UART register, if special character interrupt
100000	6	CTS, RTS	RTS pin or CTS pin change state from active (low) to inactive (high)	Read the UART_IIR_UART register

For the receiver-line status interrupt, the UART_LSR_UART[7] RX_FIFO_STS bit generates the interrupt.

For the XOFF interrupt, if an XOFF flow character detection caused the interrupt, the interrupt is cleared by an XON flow character detection. If special character detection caused the interrupt, the interrupt is cleared by a read of the UART_IIR_UART register.

12.2.4.4.5.1.2 Wake-Up Interrupt

Wake-up interrupt is a special interrupt that works differently from other interrupts. This interrupt is enabled when the UART_SCR[4] RX_CTS_WU_EN bit is set to 1. The UART_IIR_UART register is not modified when this occurs; the UART_SSR[1] RX_CTS_WU_STS bit must be checked to detect a wake-up event.

When a wake-up interrupt occurs, it can be cleared only by resetting the UART_SCR[4] RX_CTS_WU_EN bit. This bit must be reenabled (set to 1) after the current wake-up interrupt event is processed to detect the next incoming wake-up event.

12.2.4.4.5.2 IrDA Mode Interrupt Management

12.2.4.4.5.2.1 IrDA Interrupts

The IrDA function generates interrupts. All interrupts can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART_IER_IRDA). The interrupt status of the device can be checked by reading the interrupt identification register (UART_IIR_IRDA).

The UART, IrDA, and CIR modes have different interrupts in the UART module and, therefore, different UART_IER_IRDA and UART_IIR_IRDA mappings, depending on the selected mode.

The IrDA modes have eight possible interrupts (see Table 12-144). The interrupt line is activated when any interrupt is generated (there is no priority).

Table 12-144. IrDA Mode Interrupts

IIR_IRDA Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	RHR interrupt	DRDY (data ready) (FIFO disabled) RX FIFO above trigger level (FIFO enabled)	Read the UART_RHR register until the interrupt condition disappears.
1	THR interrupt	TFE (UART_THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR until the interrupt condition disappears.
2	Last byte in RX FIFO	Last byte of frame in RX FIFO is available to be read at the UART_RHR port.	Read the UART_RHR register.
3	RX overrun	Write to the UART_RHR register when the RX FIFO is full.	Read UART_RESUME register.
4	Status FIFO interrupt	Status FIFO triggers level reached.	Read STATUS FIFO.
5	TX status	UART_THR empty before EOF sent. Last bit of transmission of the IrDA frame occurred, but with an underrun error OR Transmission of the last bit of the IrDA frame completed successfully.	Read the UART_RESUME register OR Read the UART_IIR_IRDA register.

Table 12-144. IrDA Mode Interrupts (continued)

IIR_IRDA Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
6	Receiver line status interrupt	CRC, ABORT, or frame-length error is written into the STATUS FIFO.	Read the STATUS FIFO (read until empty - maximum of eight reads required).
7	Received EOF	Received end-of-frame	Read the UART_IIR_IRDA register.

12.2.4.4.5.2.2 Wake-Up Interrupts

The wake-up interrupt for IrDA mode has the same function as that for UART mode (see Section 12.2.4.4.5.1.2, *Wake-Up Interrupt*).

12.2.4.4.5.3 CIR Mode Interrupt Management

12.2.4.4.5.3.1 CIR Interrupts

The CIR function generates interrupts that can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART_IER_CIR). The interrupt status of the device can be checked by reading the interrupt identification register (UART_IIR_CIR).

The UART, IrDA, and CIR modes have different interrupts in the UART module and, therefore, different UART_IER_CIR and UART_IIR_CIR mappings, depending on the selected mode.

Table 12-145 lists the interrupt modes to be maintained. In CIR mode, the sole purpose of the UART_IIR_CIR[5] TX_STATUS_IT bit is to indicate that the last bit of infrared data was passed to the TX pin.

Table 12-145. CIR Mode Interrupts

IIR_CIR Bit Number	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
1	THR interrupt	TFE (THR empty) (FIFO disabled) TX FIFO below trigger level (FIFO enabled)	Write to the UART_THR register until the interrupt condition disappears
2	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
3	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
4	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
5	TX status	Transmission of the last bit of the frame is complete successfully	Read the UART_IIR_CIR register
6	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
7	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode

12.2.4.4.5.3.2 Wake-Up Interrupts

The wake-up interrupt for CIR mode has the same function as that for UART mode (see Section 12.2.4.4.5.1.2, *Wake-Up Interrupt*).

12.2.4.4.6 UART FIFO Management

The FIFO is accessed by reading and writing the UART_RHR and UART_THR registers. Parameters are controlled using the FIFO control register (UART_FCR) and supplementary control register (UART_SCR). Reading the UART_SSR[0] TX_FIFO_FULL bit at 1 means the FIFO is full.

The UART_TLR register controls the FIFO trigger level, which enables DMA and interrupt generation. After reset, transmit (TX) and receive (RX) FIFOs are disabled; thus, the trigger level is the default value of 1 byte. Figure 12-131 shows the FIFO management registers.

Note

Data in the UART_RHR register is not overwritten when an overflow occurs.

Note

The UART_SFLSR, UART_SFREGL, and UART_SFREGH status registers are used in IrDA mode only. For information about their use, see Section 12.2.4.4.8.3.3, *IrDA Data Formatting*.

Note

Bits UART_FCR[2] TX_FIFO_CLEAR and UART_FCR[1] RX_FIFO_CLEAR are automatically cleared by hardware after 4 × + 5 × UARTi_FCLK clock cycles. This delay is needed to finish the resetting of the corresponding FIFO and DMA control registers.

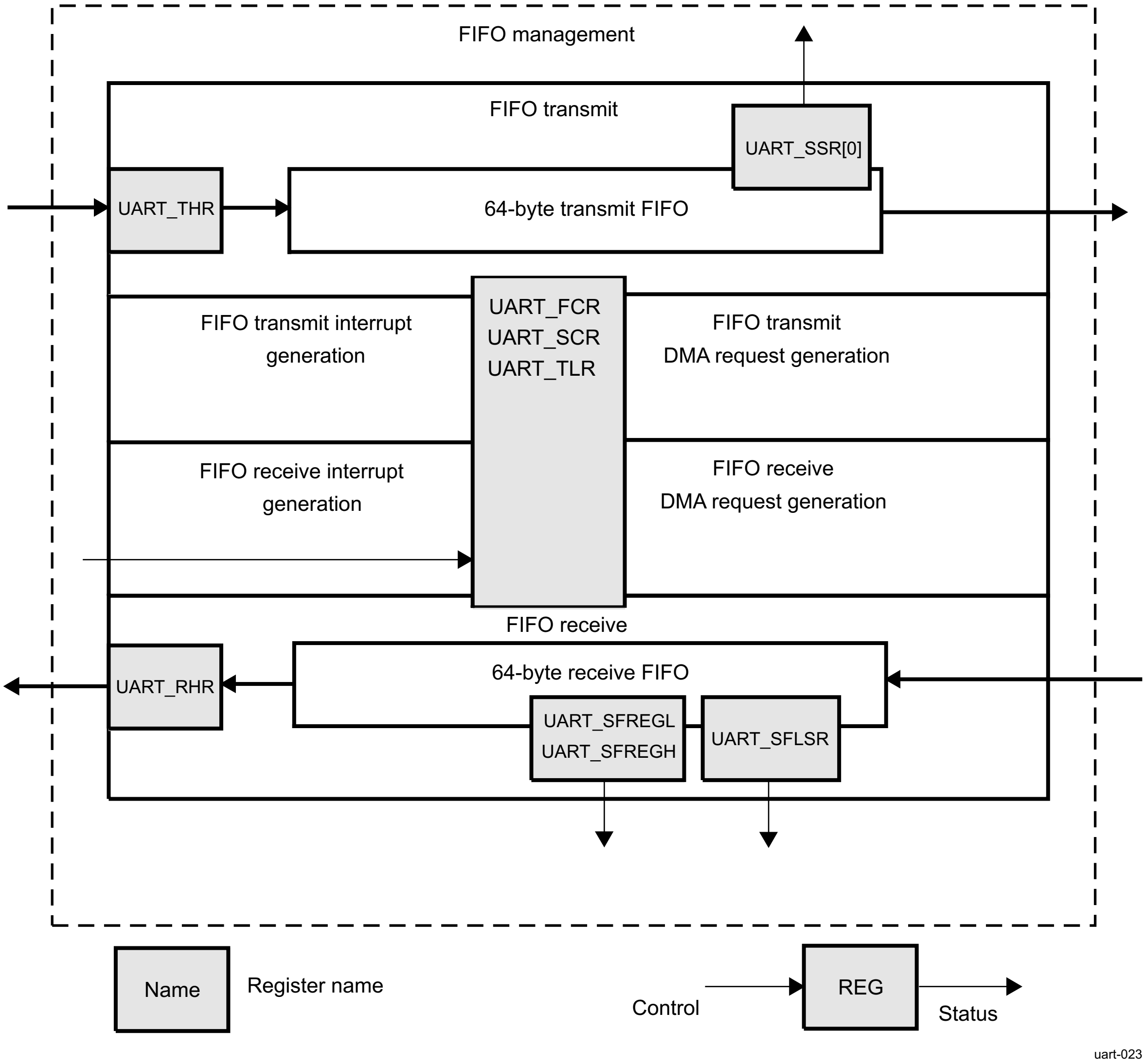


Figure 12-131. UART FIFO Management Registers

12.2.4.4.6.1 FIFO Trigger

12.2.4.4.6.1.1 Transmit FIFO Trigger

Table 12-146 lists the TX FIFO trigger level settings.

Table 12-146. UART TX FIFO Trigger Level Setting Summary

SCR[6]	TLR[3:0]	TX FIFO Trigger Level
0	= 0x0	Defined by the UART_FCR[5-4] TX_FIFO_TRIG bit field (8,16, 32, or 56 spaces)
0	!= 0x0	Defined by the UART_TLR[3-0] TX_FIFO_TRIG_DMA bit field (from 4 to 60 spaces with a granularity of 4 spaces)
1	Value	Defined by the concatenated value of TX_FIFO_TRIG_DMA and TX_FIFO_TRIG (from 1 to 63 spaces with a granularity of 1 space)

Table 12-146. UART TX FIFO Trigger Level Setting Summary (continued)

SCR[6]	TLR[3:0]	TX FIFO Trigger Level
		Note: The combination of TX_FIFO_TRIG_DMA = 0x0 and TX_FIFO_TRIG = 0x0 (all zeros) is not supported (minimum of 1 space required). All zeros result in unpredictable behavior.

12.2.4.4.6.1.2 Receive FIFO Trigger

Table 12-147 lists the RX FIFO trigger-level settings.

Table 12-147. UART RX FIFO Trigger-Level Setting Summary

SCR[7]	TLR[7:4]	RX FIFO Trigger Level
0	= 0x0	Defined by the UART_FCR[7-6] RX_FIFO_TRIG bit field (8,16, 56, or 60 characters)
0	!= 0x0	Defined by the UART_TLR[7-4] RX_FIFO_TRIG_DMA bit field (from 4 to 60 characters with a granularity of 4 characters)
1	Value	Defined by the concatenated value of RX_FIFO_TRIG_DMA and RX_FIFO_TRIG (from 1 to 63 characters with a granularity of 1 character) **Note:** The combination of RX_FIFO_TRIG_DMA = 0x0 and RX_FIFO_TRIG = 0x0 (all zeros) is not supported (minimum of 1 character required). All zeros result in unpredictable behavior.

The receive threshold is programmed using the UART_TCR[7-4] RX_FIFO_TRIG_START and UART_TCR[3-0] RX_FIFO_TRIG_HALT bit fields:

- Trigger levels from 0 to 60 bytes are available with a granularity of 4 (trigger level = 4 × [4-bit register value]).
- To ensure correct device operation, ensure that RX_FIFO_TRIG_HALT > RX_FIFO_TRIG when auto-RTS is enabled.

  Delay = [4 + 16 × (1 + CHAR_LENGTH + Parity + Stop – 0.5)] × Baud_rate + 4 × FCLK

  Note

  The RTS signal is deasserted after the UART module receives the data over RX_FIFO_TRIG_HALT. Delay means how long the UART module takes to deassert the RTS signal after reaching RX_FIFO_TRIG_HALT.

- In FIFO interrupt mode with flow control, ensure that the trigger level to HALT transmission is greater than or equal to the RX FIFO trigger level (the UART_TCR[7-4] RX_FIFO_TRIG_START bit field or the UART_FCR[7-6] RX_FIFO_TRIG bit field); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist, because a DMA request is sent when a byte is received.

12.2.4.4.6.2 FIFO Interrupt Mode

In FIFO interrupt mode (the FIFO control register UART_FCR[0] FIFO_EN bit is set to 1 and relevant interrupts are enabled by the UART_IER_UART register), an interrupt signal informs the processor of the status of the receiver and transmitter. These interrupts are raised when the RX/TX FIFO threshold (the UART_TLR[7-4] RX_FIFO_TRIG_DMA and UART_TLR[3-0] TX_FIFO_TRIG_DMA bit fields or the UART_FCR[7-6] RX_FIFO_TRIG and UART_FCR[5-4] TX_FIFO_TRIG bit fields, respectively) is reached.

The interrupt signals instruct the Host CPU to transfer data to the destination (from the UART in receive mode and/or from any source to the UART FIFO in transmit mode).

When UART flow control is enabled with interrupt capabilities, the UART flow control FIFO threshold (the UART_TCR[3-0] RX_FIFO_TRIG_HALT bit field) must be greater than or equal to the RX FIFO threshold.

Figure 12-132 shows the generation of the RX FIFO interrupt request.

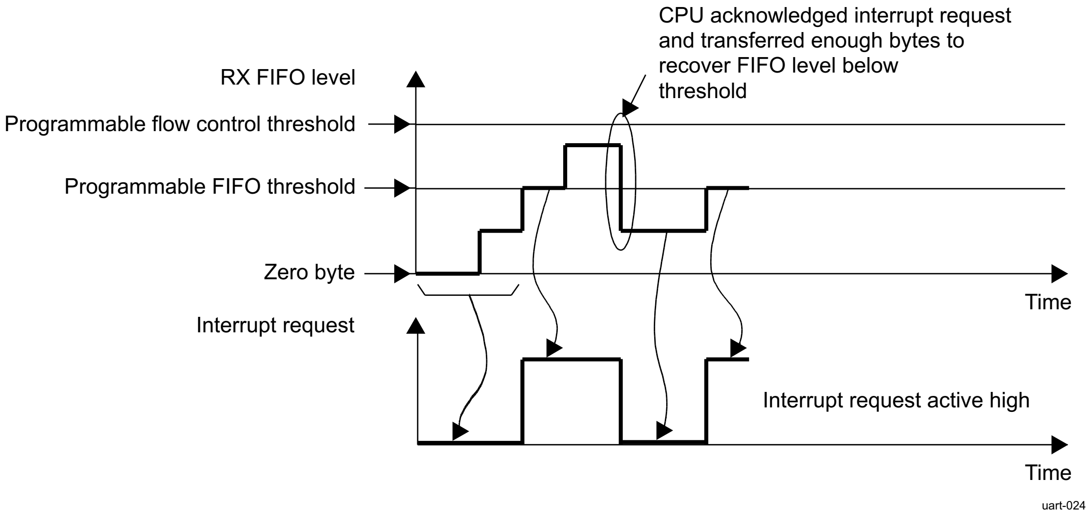


Figure 12-132. UART RX FIFO Interrupt Request Generation

In receive mode, no interrupt is generated until the RX FIFO reaches its threshold. Once low, the interrupt can be deasserted only when the Host CPU has handled enough bytes to put the FIFO level below threshold. The flow control threshold is set at a higher value than the FIFO threshold.

Figure 12-133 shows the generation of the TX FIFO interrupt request.

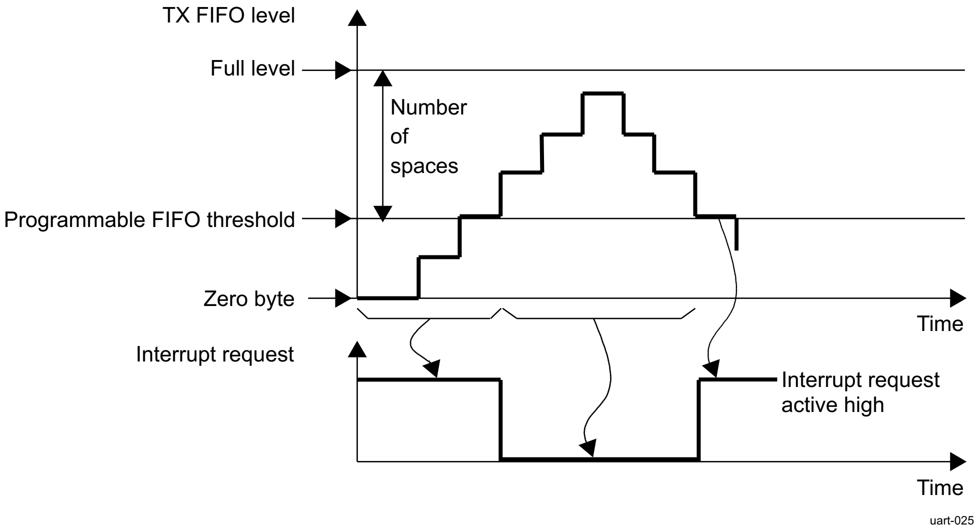


Figure 12-133. UART TX FIFO Interrupt Request Generation

In transmit mode, an interrupt request is automatically asserted when the TX FIFO is empty. This request is deasserted when the TX FIFO crosses the threshold level. The interrupt line is deasserted until a sufficient number of elements is transmitted to go below the TX FIFO threshold.

12.2.4.4.6.3 FIFO Polled Mode Operation

In FIFO polled mode (the UART_FCR[0] FIFO_EN bit is set to 0 and the relevant interrupts are disabled by the UART_IER_UART register), the status of the receiver and transmitter can be checked by polling the line status register (UART_LSR_UART).

This mode is an alternative to the FIFO interrupt mode of operation in which the status of the receiver and transmitter is automatically determined by sending interrupts to the Host CPU.

12.2.4.4.6.4 FIFO DMA Mode Operation

Although the DMA operation includes four modes (DMA modes 0 through 3), the information in *UART Hardware Requests*, assumes that mode 1 is used. (Mode 2 and mode 3 are legacy modes that use only one DMA request for each module.)

In mode 2, the remaining DMA request is used for RX. In mode 3, the remaining DMA request is used for TX.

DMA requests in mode 2 and mode 3 use the signals (where i = 0 to).

signals are not used by the module in mode 2 and mode 3:

The DMA mode and signals usage can be selected as follows:

- When the UART_SCR[0] DMA_MODE_CTL bit is set to 0, setting the UART_FCR[3] DMA_MODE bit to 0 enables DMA mode 0. Setting the UART_FCR[3] DMA_MODE bit to 1 enables DMA mode 1.
- When the UART_SCR[0] DMA_MODE_CTL bit is set to 1, the UART_SCR[2-1] DMA_MODE_2 bit field determines DMA mode 0 to mode 3 based on the supplementary control register (UART_SCR) description.

For example:

- If no DMA operation is desired, set the UART_SCR[0] DMA_MODE_CTL bit to 1 and the UART_SCR[2-1] DMA_MODE_2 bit field to 0x0. (The DMA_MODE bit is discarded.)
- If DMA mode 1 is desired, set the UART_SCR[0] DMA_MODE_CTL bit to 0 and the UART_FCR[3] DMA_MODE bit to 1, or set the UART_SCR[0] DMA_MODE_CTL bit to 1 and the UART_SCR[2-1] DMA_MODE_2 bit field to 01. (The UART_FCR[3] DMA_MODE bit is discarded.)

If the FIFOs are disabled (the UART_FCR[0] FIFO_EN bit is set to 0), the DMA occurs in single-character transfers.

When DMA mode 0 is programmed, the signals associated with DMA operation are not active.

Depending on UART_MDR3[2] SET_DMA_TX_THRESHOLD, the threshold can be programmed different ways:

- SET_TX_DMA_THRESHOLD = 1:

  The threshold value will be the value of the UART_TX_DMA_THRESHOLD register. If SET_TX_DMA_THRESHOLD + TX trigger spaces 64, then the default method of threshold is used: threshold value = TX FIFO size.
- SET_TX_DMA_THRESHOLD = 0:

  The threshold value = TX FIFO size TX trigger space. The TX DMA line is asserted if the TX FIFO level is lower then the threshold. It remains asserted until TX trigger spaces number of bytes are written into the FIFO. The DMA line is then deasserted and the FIFO level is compared with the threshold value.

12.2.4.4.6.4.1 DMA sequence to disable TX DMA

In order to disable TX DMA if it is not needed anymore (e.g. all transfers are done and UART idle mode is desired), the following sequence must be use

1. DMA mode 1 is set (both TX/RX DMA) by registers UART_SCR[0] DMA_MODE_CTL = 0 and UART_FCR[3] DMA_MODE = 1:
   a. Set the UART_SCR[2-1] DMA_MODE_2 bit fields to 01 (DMA mode 1)
   b. Set the UART_SCR[0] DMA_MODE_CTL bit to1 (this setting of UART_SCR[0] DMA_MODE-CTL will ignores UART_FCR[3] DMA_MODE_CTL bit)

   Note

   It is strongly suggested to do steps ‘a’ and ‘b’ in two separate write in order to avoid malfunction of the device.

   ---

   c. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

Note

There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

   d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
   e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
   f. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
   g. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.

2. DMA mode 1 is set (both TX/RX DMA) by registers UART_FCR[3] DMA_MODE = 0 and UART_SCR[0] DMA_MODE_CTL = 1, UART_SCR[2-1] DMA_MODE_2 = 01. It is almost the same as above, but steps ‘a’, and ‘b’ can be skipped:
   a. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

Note

There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

   b. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
   c. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
   d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
   e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.

3. DMA mode 3 is set (TX DMA only) by registers UART_FCR[3] DMA_MODE = 0 and UART_SCR[0] DMA_MODE_CTL = 1, UART_SCR[2-1] DMA_MODE_2 = 11. It is the same as above:
   a. Set the UART_FCR[3] DMA_MODE bit to 0. It is not necessary but suggested to avoid restore of DMA mode 1 during accidental reset of UART_SCR[0] DMA_MODE_CTL bit. Be sure that all data was read out from RX FIFO and if it possible disable the RX side. In UART mode the RTS/CTS or XOFF/XON protocol can be used. In IrDA modes RX can be forcibly disabled by setting UART_ACREG[5] DIS_IR_RX bit

Note

There can be RX DATA loss during the next steps if all DATA was not read out or there was an ongoing reception!

   b. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO).
   c. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 10 (DMA mode 2, RX only).
   d. Set the UART_FCR[2-1] DMA_MODE bit field to 11 (clear TX and RX FIFO and the DMA request again).
   e. Set the UART_SCR[2-1] DMA_MODE_2 bit field to 00 (no DMA) or keep 10 if RX DMA is needed.

12.2.4.4.6.4.2 DMA Transfers (DMA Mode 1, 2, or 3)

Figure 12-134 through Figure 12-137 show the supported DMA operations.

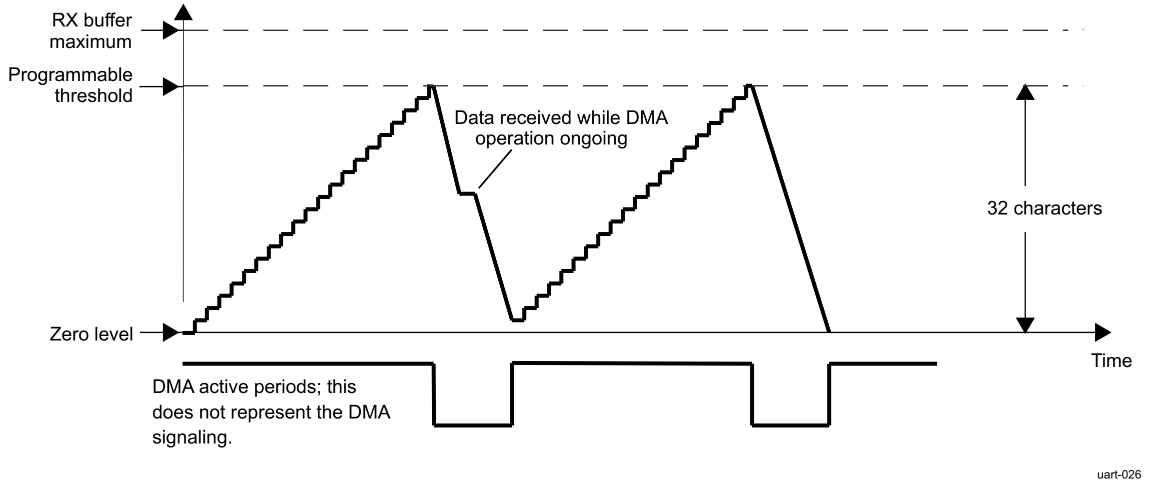


Figure 12-134. UART Receive FIFO DMA Request Generation (32 Characters)

In receive mode, a DMA request is generated when the RX FIFO reaches its threshold level defined in the trigger level register (UART_TLR). This request is deasserted when the number of bytes defined by the threshold level is read by the device DMA controllers.

In transmit mode, a DMA request is automatically asserted when the TX FIFO is empty. This request is deasserted when the number of bytes defined by the number of spaces in the UART_TLR register is written by the device DMA controllers. If an insufficient number of characters is written, the DMA request stays active.

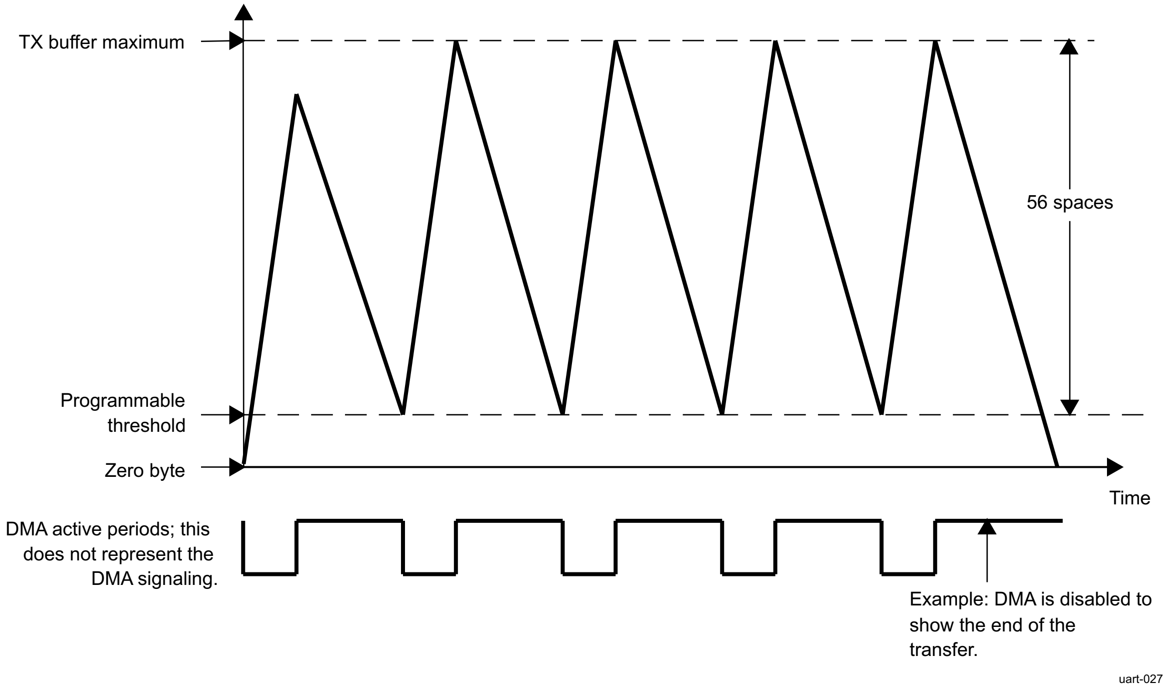


Figure 12-135. UART Transmit FIFO DMA Request Generation (56 Spaces)

The DMA request is again asserted if the FIFO can receive the number of bytes defined by the UART_TLR register.

The threshold can be programmed in a number of ways. Figure 12-135 shows a DMA transfer operating with a space setting of 56 that can arise from using the auto settings in the UART_FCR[5-4] TX_FIFO_TRIG bit field or the UART_TLR[3-0] TX_FIFO_TRIG_DMA bit field concatenated with the TX_FIFO_TRIG bit field.

The setting of 56 spaces in the UART module must correlate with the settings of the device DMA controllers, so that the buffer does not overflow (program the DMA request size of the LH controller to equal the number of spaces in the UART module).

Figure 12-136 shows an example with eight spaces to show the buffer level crossing the space threshold. The LH DMA controller settings must correspond to those of the UART module.

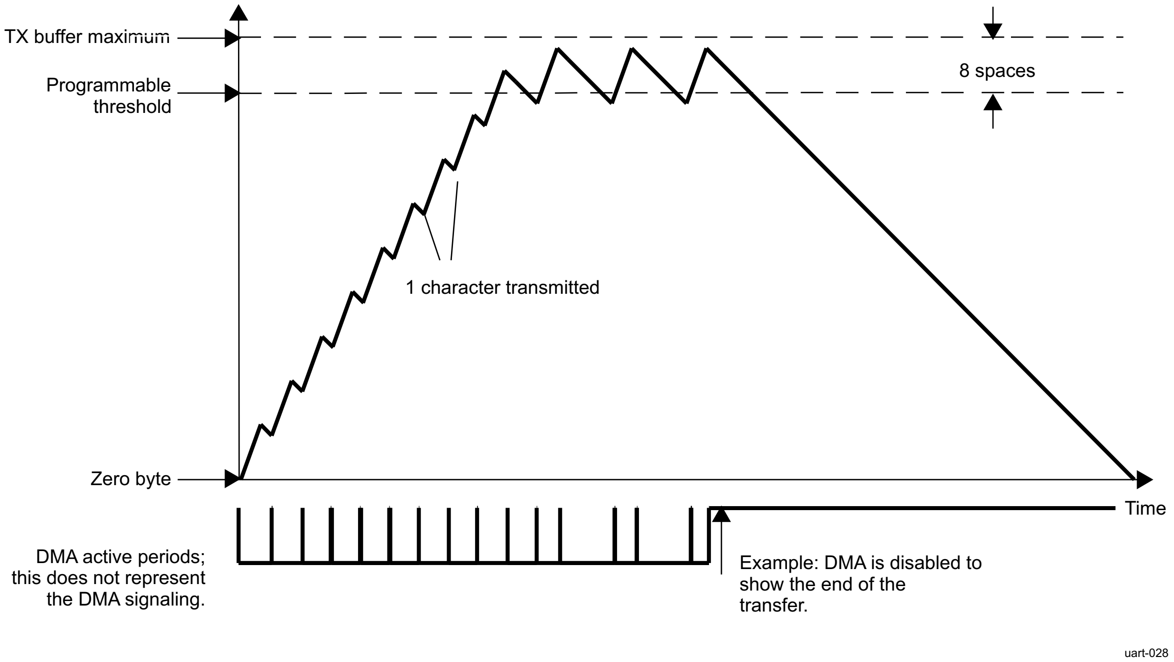


Figure 12-136. UART Transmit FIFO DMA Request Generation (8 Spaces)

The next example shows the setting of one space that uses the DMA for each transfer of one character to the transmit buffer (see Figure 12-137). The buffer is filled faster than the baud rate at which data is transmitted to the TX pin. Eventually, the buffer is completely full and the DMA operations stop transferring data to the transmit buffer.

On two occasions, the buffer holds the maximum amount of data words; shortly after this, the DMA is disabled to show the slower transmission of the data words to the TX pin. Eventually, the buffer is emptied at the rate specified by the baud rate settings of the UART_DLL and UART_DLH registers.

The DMA settings must correspond to the system LH DMA controller settings to ensure correct operation of this logic.

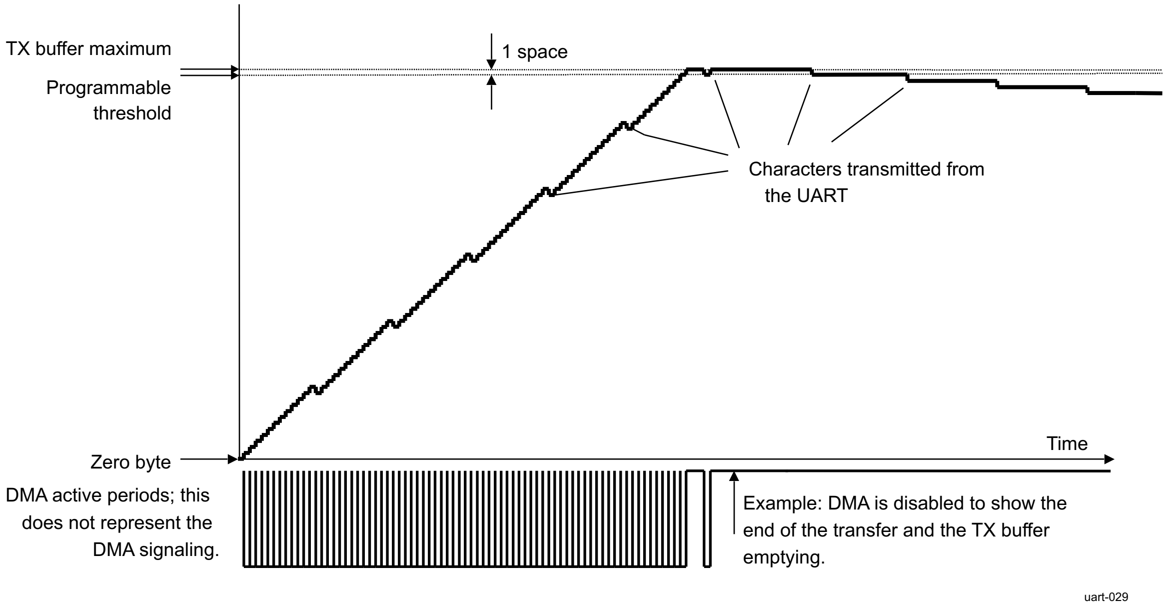


Figure 12-137. UART Transmit FIFO DMA Request Generation (1 Space)

The final example illustrates the setting of eight spaces but setting the TX DMA threshold directly by setting UART_MDR3[1] NONDEFAULT_FREQ bit and UART_TX_DMA_THRESHOLD register (see Figure 12-138). In the example, the UART_TX_DMA_THRESHOLD[5-0] TX_DMA_THRESHOLD = 3 and the trigger level is 8. The buffer is filled at a faster rate than the BAUD rate transmits data to the TX pin. The buffer is filled with 8 bytes and the DMA operations stop transferring data to the transmit buffer. When the buffer is emptied to the threshold level by transmission, the DMA operation activates again to fill the buffer with 8 bytes.

Eventually, the buffer will be emptied at the rate specified by the BAUD Rate settings of the UART_DLL and UART_DLH registers.

If the selected threshold level + trigger level exceeds max buffer size, then the original TX DMA threshold method is used to prevent TX overrun, regardless of the UART_MDR3[1] NONDEFAULT_FREQ value.

The DMA settings should correspond to the system Local Host DMA controller settings in order to ensure the correct operation of this logic.

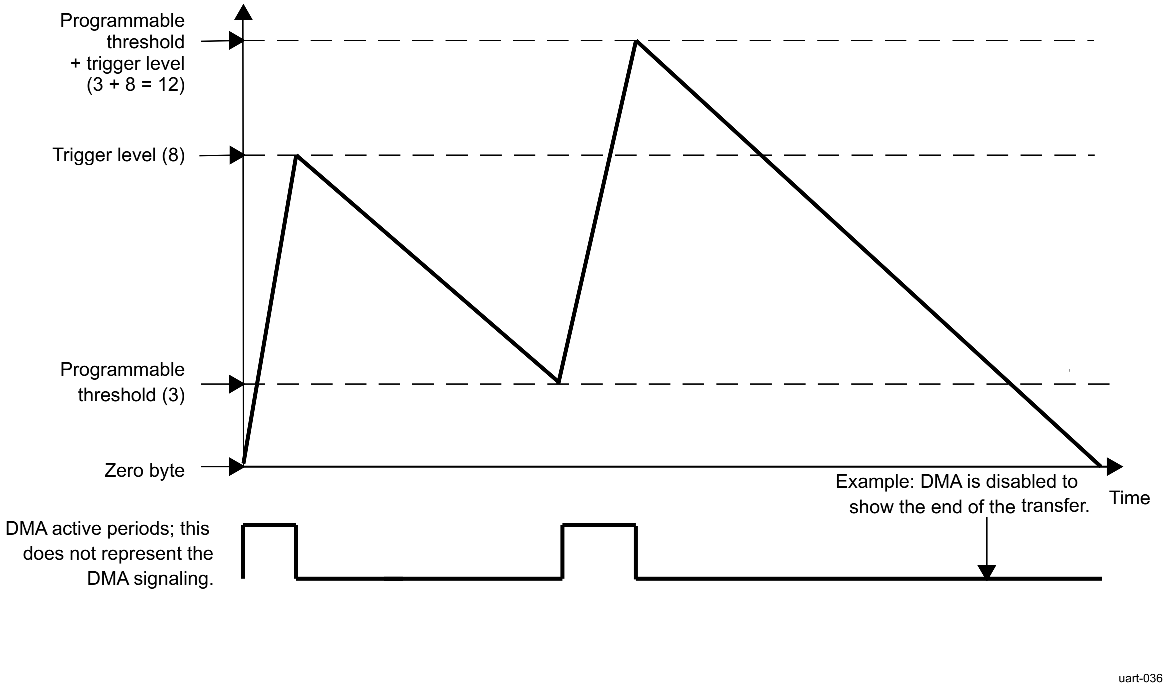


Figure 12-138. UART Transmit FIFO DMA Request Generation Using Direct TX DMA Threshold Programming. (Threshold = 3; Spaces = 8)

12.2.4.4.6.4.3 DMA Transmission

Figure 12-139 shows DMA transmission.

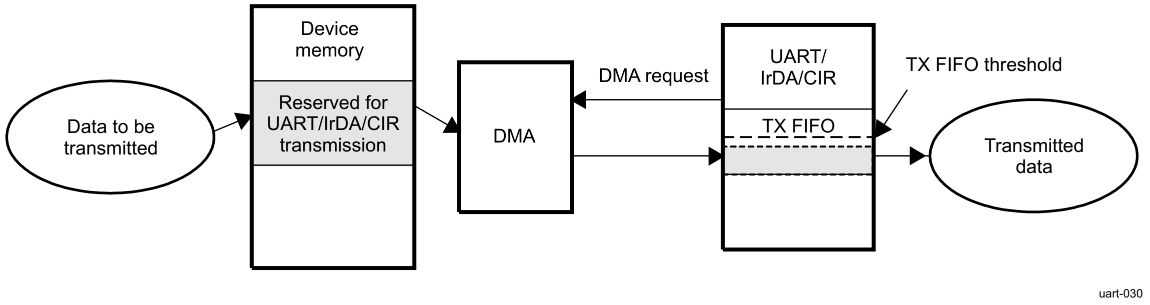


Figure 12-139. DMA Transmission

1. Data to be transmitted are put in the device memory reserved for UART transmission by the DMA:
    a. Until the TX FIFO trigger level is not reached, a DMA request is generated
    b. An element (1 byte) is transferred from the SDRAM to the TX FIFO at each DMA request (DMA element synchronization).
2. Data in the TX FIFO are automatically transmitted.
3. The end of the transmission is signaled by the UART_THR empty (TX FIFO empty).

Note

In IrDA mode, the transmission does not end immediately after the TX FIFO empties, at which point the last data byte, the CRC field, and the stop flag still must be transmitted; thus, the end of transmission occurs a few milliseconds after the UART_THR register empties.

12.2.4.4.6.4.4 DMA Reception

Figure 12-140 shows DMA reception.

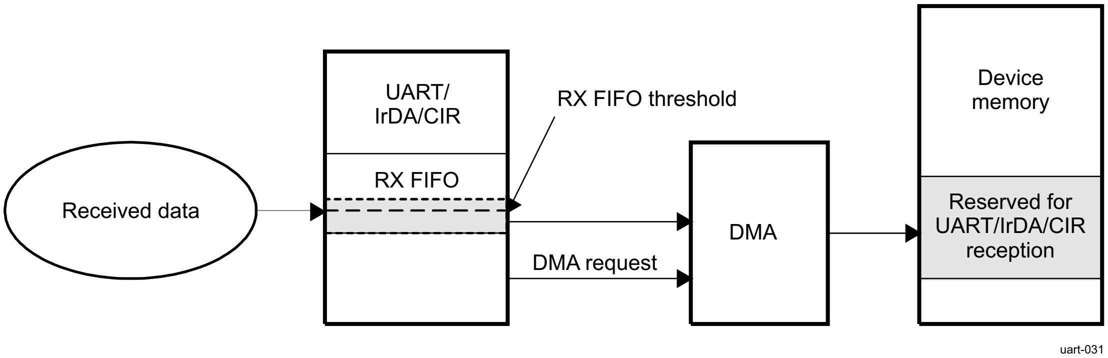


Figure 12-140. DMA Reception

1. Enable the reception.
2. Received data are put in the RX FIFO.
3. Data are transferred from the RX FIFO to the device memory by the DMA:
    a. At each received byte, the RX FIFO trigger level (one character) is reached and a DMA request is generated.
    b. An element (1 byte) is transferred from the RX FIFO to the SDRAM at each DMA request (DMA element synchronization).
4. The end of the reception is signaled by the EOF interrupt.

12.2.4.4.7 UART Mode Selection

12.2.4.4.7.1 Register Access Modes

12.2.4.4.7.1.1 Operational Mode and Configuration Modes

Register access depends on the register access mode, although register access modes are not correlated to functional mode selection. Three different modes are available:

- Operational mode
- Configuration mode A
- Configuration mode B

Operational mode is the selected mode when the function is active; serial data transfer can be performed in this mode.

Configuration mode A and configuration mode B are used during module initialization steps. These modes enable access to configuration registers, which are hidden in the operational mode. The modes are used when the module is inactive (no serial data transfer processed) and only for initialization or reconfiguration of the module.

The value of the UART_LCR register determines the register access mode (see Table 12-148).

Table 12-148. UART Register Access Mode Programming (Using UART_LCR)

Mode	Condition
Configuration mode A	UART_LCR[7] = 0x1 and UART_LCR[7-0] != 0xBF
Configuration mode B	UART_LCR[7] = 0x1 and UART_LCR[7-0] = 0xBF
Operational mode	UART_LCR[7] = 0x0

12.2.4.4.7.1.2 Register Access Submode

In each access register mode (operational mode or configuration mode A/B), some register accesses are conditional on the programming of a submode (MSR_SPR, TCR_TLR, and XOFF). These registers are identified in Table 12-171, *UART Load FIFO Triggers Defined by the Concatenated Value*.

Table 12-149 through Table 12-151 summarize the register access submodes.

Table 12-149. UART Subconfiguration Mode A Summary

Mode	Condition
MSR_SPR	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

Table 12-150. UART Subconfiguration Mode B Summary

Mode	Condition
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1
XOFF	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)

Table 12-151. UART Suboperational Mode Summary

Mode	Condition
MSR_SPR	UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

12.2.4.4.7.1.3 Registers Available for the Register Access Modes

Table 12-152 lists the names of the register bits in each access register mode. Gray shading indicates that the register does not depend on the register access mode (available in all modes).

Table 12-152. UART Register Access Mode Overview

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART	UART_IER_UART
0x008	UART_IIR_UART	UART_FCR	UART_EFR	UART_EFR	UART_IIR_UART	UART_FCR
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR_UART	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART	–
0x018	UART_MSR / UART_TCR	UART_TCR	UART_TCR / UART_XOFF1	UART_TCR / UART_XOFF1	UART_MSR / UART_TCR	UART_TCR
0x01C	UART_SPR / UART_TLR	UART_SPR / UART_TLR	UART_TLR / UART_XOFF2	UART_TLR / UART_XOFF2	UART_SPR / UART_TLR	UART_SPR / UART_TLR
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	UART_UASR	–	UART_UASR	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS

Table 12-152. UART Register Access Mode Overview (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

12.2.4.4.7.2 UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection

To select a mode, set the UART_MDR1[2:0] MODE_SELECT bit field (see Table 12-153).

Table 12-153. UART Mode Selection

Value	Mode
0x0:	UART 16× mode
0x1:	SIR mode
0x2:	UART 16× auto-baud
0x3:	UART 13× mode
0x4:	MIR mode
0x5:	FIR mode
0x6:	CIR mode

MODE_SELECT is effective when the module is in operational mode (see Section 12.2.4.4.7.1, *Register Access Modes*).

To select a RS-485 mode, set the UART_MDR3[4] DIR_EN bit field to 0x1.

12.2.4.4.7.2.1 Registers Available for the UART Function

Only the registers listed in Table 12-154 are used for the UART function.

Table 12-154. UART Mode Register Overview

Address Offset	Registers(1) (2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (UART)	UART_IER_UART (UART)
0x008	UART_IIR_UART	UART_FCR	UART_EFR [4]	UART_EFR [4]	UART_IIR_UART (UART)	UART_FCR (UART)
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR_UART (UART)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART (UART)	–
0x018	UART_MSR/ UART_TCR	UART_TCR	UART_XOFF1/ UART_TCR	UART_XOFF1/ UART_TCR	UART_MSR/ UART_TCR	UART_TCR
0x01C	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR	UART_TLR/ UART_XOFF2	UART_TLR/ UART_XOFF2	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR
0x020	UART_MDR1	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]	UART_MDR1 [2-0]

Table 12-154. UART Mode Register Overview (continued)

Address Offset	Registers(1) (2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	–	–	–	–	–	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	UART_UASR	–	UART_UASR	–	–	–
0x03C	–	–	–	–	–	–
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	–	–
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	–	–	–	–	–	–
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in *UART Registers*).
(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

12.2.4.4.7.2.2 Registers Available for the IrDA Function

Only the registers listed in Table 12-155 are used for the IrDA function.

Table 12-155. IrDA Mode Register Overview

Address Offset	Registers(1) (2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (IrDA)	UART_IER_UART (IrDA)
0x008	UART_IIR_UART	UART_FCR	UART_EFR [4]	UART_EFR [4]	UART_IIR_UART (IrDA)	UART_FCR (IrDA)
0x00C	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]
0x010	–	–	UART_XON1_ADDR1	UART_XON1_ADDR1	–	–
0x014	UART_LSR_UART (IrDA)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR_UART (IrDA)	–
0x018	UART_MSR/ UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/ UART_TCR	UART_TCR

Table 12-155. IrDA Mode Register Overview (continued)

Address Offset	Registers(1) (2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x01C	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR	UART_TLR	UART_TLR	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	–	–	–	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]
0x060	–	–	–	–	–	–
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(IrDA) notation indicates that the register exists for other functions (UART or CIR), but fields have different meanings for other functions (described separately in *UART Registers*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the IrDA function.

12.2.4.4.7.2.3 Registers Available for the CIR Function

Only the registers listed in Table 12-156 are used for the CIR function.

Table 12-156. CIR Mode Register Overview

Address Offset	Registers(1) (2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	–	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER_UART (CIR)	UART_IER_UART (CIR)
0x008	UART_IIR_UART	UART_FCR	UART_EFR	UART_EFR	UART_IIR_UART (CIR)	UART_FCR (CIR)
0x00C	UART_LCR	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]	UART_LCR [7]
0x010	–	–	–	–	–	–
0x014	UART_LSR_UART (CIR)	–	–	–	UART_LSR_UART (CIR)	–

Table 12-156. CIR Mode Register Overview (continued)

Address Offset	Registers(1) (2)					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x018	UART_MSR/ UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/ UART_TCR	UART_TCR
0x01C	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR	UART_TLR	UART_TLR	UART_TLR/ UART_SPR	UART_TLR/ UART_SPR
0x020	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]	UART_MDR1 [3-0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	UART_RESUME	–	UART_RESUME	–	UART_RESUME	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	–	–	–	–	–	–
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]	UART_WER [6-4]
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

(1) REGISTER_NAME(CIR) notation indicates that the register exists for other functions (IrDA or UART), but fields have different meanings for other functions (described separately in *UART Registers*).
(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the CIR function.

12.2.4.4.8 UART Protocol Formatting

12.2.4.4.8.1 UART Mode

12.2.4.4.8.1.1 UART Clock Generation: Baud Rate Generation

The UART function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 12-141 shows the baud rate generator and associated controls.

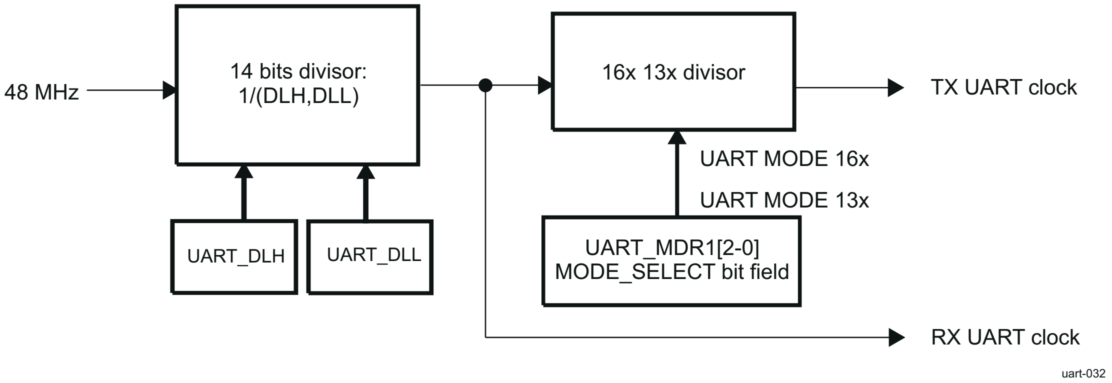


Figure 12-141. UART Baud Rate Generation

CAUTION

Before initializing or modifying clock parameter controls (UART_DLH, UART_DLL), UART_MDR1[2-0] MODE_SELECT = DISABLE must be set to 0x7. Failure to observe this rule can result in unpredictable module behavior.

12.2.4.4.8.1.2 Choosing the Appropriate Divisor Value

Two divisor values are:

- UART 16× mode: Divisor value = Operating frequency / (16× baud rate)
- UART 13× mode: Divisor value = Operating frequency / (13× baud rate)

Table 12-157 describes the UART baud rate settings.

Table 12-157. UART Baud Rate Settings (48MHz, 160MHz, 192MHz Clock)

Baud Rate	Baud Multiple	Source Clock(MHz)	DLH, DLL (Decimal)	DLH, DLL (Hex)	Actual Baud Rate	Error (%)
0.3kbps	16x	48	10000	0x27, 0x10	0.3kbps	0
0.6kbps	16x	48	5000	0x13, 0x88	0.6kbps	0
1.2kbps	16x	48	2500	0x09, 0xC4	1.2kbps	0
2.4kbps	16x	48	1250	0x04, 0xE2	2.4kbps	0
4.8kbps	16x	48	625	0x02, 0x71	4.8kbps	0
9.6kbps	16x	48	312	0x01, 0x38	9.615385kbps	-0.16
9.6kbps	16x	192	1250	0x04, 0xE2	9.6kbps	0
14.4kbps	16x	48	208	0x00, 0xD0	14.42308kbps	-0.16
19.2kbps	16x	192	625	0x02, 0x71	19.2kbps	0
28.8kbps	16x	48	104	0x00, 0x68	28.84615kbps	-0.16
38.4kbps	16x	48	78	0x00, 0x4E	38.46154kbps	-0.16
57.6kbps	16x	48	52	0x00, 0x34	57.69231kbps	-0.16
115.2kbps	16x	48	26	0x00, 0x1A	115.3846kbps	-0.16
230.4kbps	16x	48	13	0x00, 0x0D	230.7692kbps	-0.16
460.8kbps	13x	48	8	0x00, 0x08	461.5385kbps	-0.16
921.6kbps	13x	48	4	0x00, 0x04	923.0769kbps	-0.16
1.843Mbps	13x	48	2	0x00, 0x02	1.846154Mbps	-0.17
2.5Mbps	16x	160	4	0x00, 0x04	2.5Mbps	0
3.0Mbps	16x	48	1	0x00, 0x01	3.0Mbps	0
3.6884Mbps	13x	48	1	0x00, 0x01	3.692308Mbps	-0.11
4Mbps	16x	192	3	0x00, 0x03	4Mbps	0
5Mbps	16x	160	2	0x00, 0x02	5Mbps	0
10Mbps	16x	160	1	0x00, 0x01	10Mbps	0

Table 12-157. UART Baud Rate Settings (48MHz, 160MHz, 192MHz Clock) (continued)

Baud Rate	Baud Multiple	Source Clock(MHz)	DLH, DLL (Decimal)	DLH, DLL (Hex)	Actual Baud Rate	Error (%)
12Mbps	16x	192	1	0x00, 0x01	12Mbps	0

12.2.4.4.8.1.3 UART Data Formatting

The UART can use hardware flow control to manage transmission and reception. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the RTS output and CTS input signals.

The UART is enhanced with the autobauding function. In control mode, autobauding lets the speed, the number of bits per character, and the parity selected be set automatically.

12.2.4.4.8.1.3.1 Frame Formatting

When autobauding is not used, frame format attributes must be defined in the UART_LCR register.

Character length is specified using the UART_LCR[1-0] CHAR_LENGTH bit field.

The number of stop-bits is specified using the UART_LCR[2] NB_STOP bit.

The parity bit is programmed using the UART_LCR[5-3] PARITY_EN, UART_LCR[5-3] PARITY_TYPE_1, and UART_LCR[5-3] PARITY_TYPE_2 bit fields (see Table 12-158).

Table 12-158. UART Parity Bit Encoding

PARITY_EN	PARITY_TYPE_1	PARITY_TYPE_2	Parity
0	N/A	N/A	No parity
1	0	0	Odd parity
1	1	0	Even parity
1	0	1	Forced 1
1	1	1	Forced 0

12.2.4.4.8.1.3.2 Hardware Flow Control

Hardware flow control is composed of auto-CTS and auto-RTS. Auto-CTS and auto-RTS can be enabled and disabled independently by programming the UART_EFR[7] AUTO_CTS_EN and UART_EFR[6] AUTO_RTS_EN bit fields, respectively.

With auto-CTS, CTS signal must be active before the module can transmit data.

Auto-RTS activates the RTS output only when there is enough room in the RX FIFO to receive data. It deactivates the RTS output when the RX FIFO is sufficiently full. The HALT and RESTORE trigger levels in the UART_TCR register determine the levels at which RTS is activated and deactivated.

If auto-CTS and auto-RTS are enabled, data transmission does not occur unless the RX FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If auto-CTS and auto-RTS are not enabled, overrun errors occur if the transmit data rate exceeds the RX FIFO latency.

- Auto-RTS:

  Auto-RTS data flow control originates in the receiver block. The RX FIFO trigger levels used in auto-RTS are stored in the UART_TCR register. RTS is active if the RX FIFO level is below the HALT trigger level in the UART_TCR[3-0] RX_FIFO_TRIG_HALT bit field. When the RX FIFO HALT trigger level is reached, RTS is deasserted. The sending device (for example, another UART) can send an additional byte after the trigger level is reached because it may not recognize the deassertion of RTS until it begins sending the additional byte.

  RTS is automatically reasserted when the RX FIFO reaches the RESUME trigger level programmed by the UART_TCR[7-4] RX_FIFO_TRIG_START bit field. This reassertion requests the sending device to resume transmission.

  In this case, RTS is an active-low signal.
- Auto-CTS:

The transmitter circuitry checks CTS before sending the next data byte. When CTS is active, the transmitter sends the next byte. To stop the transmitter from sending the next byte, CTS must be deasserted before the middle of the last stop-bit currently sent.

The auto-CTS function reduces interrupts to the host system. When auto-CTS flow control is enabled, the CTS state changes do not have to trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO, and a receiver overrun error can result.

In this case, CTS is an active-low signal.

12.2.4.4.8.1.3.3 Software Flow Control

Software flow control is enabled through the enhanced feature register (UART_EFR) and the modem control register (UART_MCR). Different combinations of software flow control can be enabled by setting different combinations of the UART_EFR[3-0] bit field (see Table 12-159).

Two other enhanced features relate to software flow control:

- XON-any function (UART_MCR[5] XON_EN): Operation resumes after receiving any character after the XOFF character is recognized. If special character detect is enabled and special character is received after XOFF1, it does not resume transmission. The special character is stored in the RX FIFO.

Note

The XON-any character is written into the RX FIFO even if it is a software flow character.

- Special character (UART_EFR[5] SPECIAL_CHAR_DETEC T): Incoming data is compared to XOFF2. When the special character is detected, the XOFF interrupt (UART_IIR_UART) is set, but it does not halt transmission. The XOFF interrupt is cleared by a read of UART_IIR_UART. The special character is transferred to the RX FIFO. Special character does not work with XON2, XOFF2, or sequential XOFFs.

Table 12-159. UART_EFR[3:0] Software Flow Control Options

Bit 3	Bit 2	Bit 1	Bit 0	TX, RX Software Flow Controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit XON1, XOFF1
0	1	X	X	Transmit XON2, XOFF2
1	1	X	X	Transmit XON1, XON2: XOFF1, XOFF2(1)
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares XON1, XOFF1
X	X	0	1	Receiver compares XON2, XOFF2
X	X	1	1	Receiver compares XON1, XON2: XOFF1, XOFF2(1)

(1) In these cases, the XON1 and XON2 characters or the XOFF1 and XOFF2 characters must be transmitted/received sequentially with XON1/XOFF1 followed by XON2/XOFF2.
XON1 is defined in the UART_XON1_ADDR1[7-0] XON_WORD1 bit field. XON2 is defined in the UART_XON2_ADDR2[7-0] XON_WORD2 bit field.
XOFF1 is defined in the UART_XOFF1[7-0] XOFF_WORD1 bit field. XOFF2 is defined in the UART_XOFF2[7-0] XOFF_WORD2 bit field.

12.2.4.4.8.1.3.3.1 Receive (RX)

When software flow control operation is enabled, the UART compares incoming data with XOFF1/2 programmed characters (in certain cases, XOFF1 and XOFF2 must be received sequentially). When the correct XOFF characters are received, transmission stops after transmission of the current character completes. Detection of XOFF also sets the UART_IIR_UART[4] bit (if enabled by UART_IER_UART[5]) and causes the interrupt line to go low.

To resume transmission, an XON1/2 character must be received (in certain cases, XON1 and XON2 must be received sequentially). When the correct XON characters are received, the UART_IIR_UART[4] bit is cleared and the XOFF interrupt disappears.

Note

When a parity, framing, or break error occurs while receiving a software flow control character, this character is treated as normal data and is written to the RX FIFO.

When XON-any and special character detect are disabled and software flow control is enabled, no valid XON or XOFF characters are written to the RX FIFO. For example, when UART_EFR[1-0] = 0x2, if XON1 and XOFF1 characters are received, they are not written to the RX FIFO.

When pairs of software flow characters are programmed to be received sequentially (UART_EFR[1-0] = 0x3), the software flow characters are not written to the RX FIFO if they are received sequentially. However, received XON1/XOFF1 characters must be written to the RX FIFO if the subsequent character is not XON2/XOFF2.

12.2.4.4.8.1.3.3.2 Transmit (TX)

Two XOFF1 characters are transmitted when the RX FIFO passes the trigger level programmed by UART_TCR[3-0] RX_FIFO_TRIG_HALT. As soon as the RX FIFO reaches the trigger level programmed by UART_TCR[7-4] RX_FIFO_TRIG_START, two XON1 characters are sent, so the data transfer recovers.

Note

If software flow control is disabled after an XOFF character is sent, the module transmits XON characters automatically to enable normal transmission.

The transmission of XOFF(s)/XON(s) follows the same protocol as transmission of an ordinary byte from the TX FIFO. This means that even if the word length is 5, 6, or 7 characters, the 5, 6, or 7 LSBs of XOFF1/2 and XON1/2 are transmitted. The 5, 6, or 7 bits of a character are seldom transmitted, but this function is included to maintain compatibility with earlier designs.

It is assumed that software flow control and hardware flow control are never enabled simultaneously.

12.2.4.4.8.1.3.4 Autobauding Modes

In autobauding mode, the UART can extract transfer characteristics (speed, length, and parity) from an "at" (AT) command (ASCII code). These characteristics are used to receive data after an AT and to send data.

The following AT commands are valid:

AT	DATA	<CR>
at	DATA	<CR>
A/		
a/		

A line break during the acquisition of the sequence AT is not recognized, and an echo function is not implemented in hardware.

A/ and a/ are not used to extract characteristics, but they must be recognized because of their special meaning. A/ or a/ is used to instruct the software to repeat the last received AT command; therefore, an a/ always follows an AT, and transfer characteristics are not expected to change between an AT and an a/.

When a valid AT is received, AT and all subsequent data, including the final <CR> (0x0D), are saved to the RX FIFO. The autobaud state-machine waits for the next valid AT command. If an a/ (A/) is received, the a/ (A/) is saved in the RX FIFO and the state-machine waits for the next valid AT command.

On the first successful detection of the baud rate, the UART activates an interrupt to signify that the AT (upper or lower case) sequence is detected. The UART_UASR register reflects the correct settings for the baud rate detected. Interrupt activity can continue in this fashion when a subsequent character is received. Therefore, it is recommended that the software enable the RHR interrupt when using the autobaud mode.

The following settings are detected in autobaud mode with a module clock of 48 MHz:

- Speed:

  - 115.2K baud
  - 57.6K baud
  - 38.4K baud
  - 28.8K baud
  - 19.2K baud
  - 14.4K baud
  - 9.6K baud
  - 4.8K baud
  - 2.4K baud
  - 1.2K baud
- Length: 7 or 8 bits
- Parity: Odd, even, or space

Note

The combination of 7-bit character plus space parity is not supported.

Autobauding mode is selected when the UART_MDR1[2-0] MODE_SELECT bit field is set to 0x2. In UART autobauding mode, UART_DLL, UART_DLH, and UART_LCR[5-0] bit field settings are not used; instead, the UART_UASR register is updated with the configuration detected by the autobauding logic.

UASR Autobauding Status Register Use

This register is used to set up transmission according to the characteristics of the previous reception instead of the UART_LCR, UART_DLL, and UART_DLH registers when the UART is in autobauding mode.

To reset the autobauding hardware (to start a new AT detection) or to set the UART in standard mode (no autobaud), the UART_MDR1[2-0] MODE_SELECT bit field must be set to reset state (0x7) and then to the UART in autobauding mode (0x2) or to the UART in standard mode (0x0).

Use limitation:

- Only 7- and 8-bit characters (5- and 6-bit not supported)
- 7-bit character with space parity not supported
- Baud rate between 1200 and 115.2 bps (10 possibilities)

12.2.4.4.8.1.3.5 Error Detection

When the UART_LSR_UART register is read, the UART_LSR_UART[4:2] bit field reflects the error bits (BI: break condition, FE: framing error, PE: parity error) of the character at the top of the RX FIFO (the next character to be read). Therefore, reading the UART_LSR_UART register and then reading the UART_RHR register identifies errors in a character.

Reading the UART_RHR register updates the BI, FE, and PE bits (see Table 12-143 for the UART mode interrupts).

The UART_LSR_UART[7] RX_FIFO_STS bit is set when there is an error in the RX FIFO and is cleared only when no errors remain in the RX FIFO.

Note

Reading the UART_LSR_UART register does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the UART_RHR register.

Reading the UART_LSR_UART register clears the OE bit if it is set (see Table 12-143 for the UART mode interrupts).

12.2.4.4.8.1.3.6 Overrun During Receive

Overrun during receive occurs if the RX state-machine tries to write data into the RX FIFO when it is already full. When overrun occurs, the device interrupts the Host CPU with the UART_IIR_UART[5-1] IT_TYPE bit field set to 0x3 (receiver line status error) and discards the remaining portion of the frame.

Overrun also causes an internal flag to be set, which disables further reception. Before the next frame can be received, the Host CPU must:

- Reset the RX FIFO.
- Read the UART_RESUME register, which clears the internal flag.

12.2.4.4.8.1.3.7 Time-Out and Break Conditions

12.2.4.4.8.1.3.7.1 Time-Out Counter

An RX idle condition is detected when the receiver line (RX) is high for a time that equals 4x the programmed word length + 12 bits or manually configured amount of baud clocks, if a value other zero is set in the timeout register. RX is sampled midway through each bit.

For sleep mode, the counter is reset when there is activity on RX.

There are two modes of operation:

- In default operation on the UART_EFR2[6] TIMEOUT_BEHAVE is set to 0. For the time-out interrupt, the counter counts only when there is data in the RX FIFO, and the count is reset when there is activity on RX or when the UART_RHR register is read.
- Optionally, for choose to enable the timeout counter even if no character has been received by setting UART_EFR2[6] TIMEOUT_BEHAVE bit. This will generate periodic interrupts if the RX line remains idle. In this mode the counter will auto-reset when a timeout has been reached. Reading the UART_IIR_UART will clear the interrupt, but not the counter.

12.2.4.4.8.1.3.7.2 Break Condition

When a break condition occurs, TX is pulled low. A break condition is activated by setting the UART_LCR[6] BREAK_EN bit. The break condition is not aligned on word stream (a break condition can occur in the middle of a character). The only way to send a break condition on a full character is:

1. Reset the TX FIFO (if enabled).
2. Wait for the transmit shift register to empty (the UART_LSR_UART[6] TX_SR_E bit is set to 1).
3. Take a guard time according to stop-bit definition.
4. Set the BREAK_EN bit to 1.

The break condition is asserted while the BREAK_EN bit is set to 1.

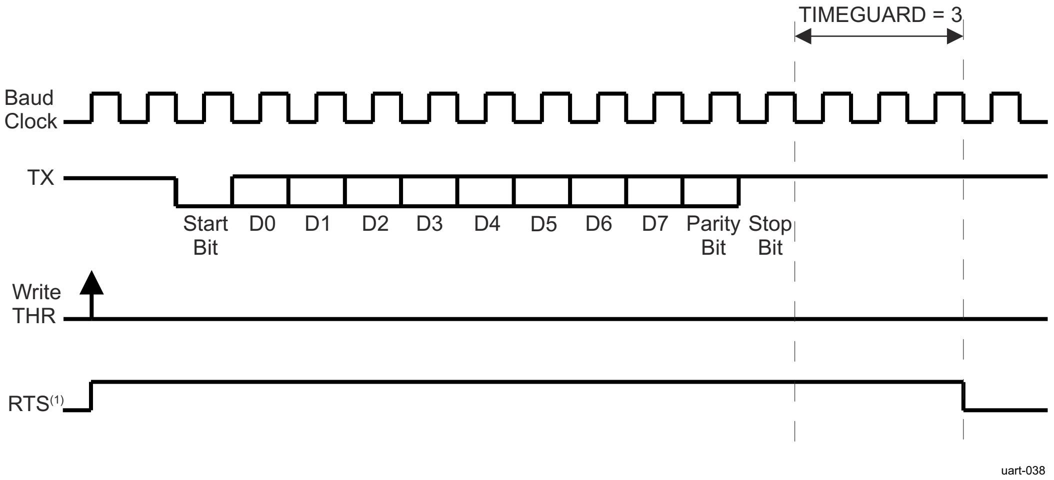
The time-out counter and break condition apply only to UART modem operation and not to IrDA/CIR mode operation.

12.2.4.4.8.2 RS-485 Mode

12.2.4.4.8.2.1 RS-485 External Transceiver Direction Control

The UART_MDR3[4] DIR_EN bit enables hardware control over an external transceiver to support RS-485. The direction signal comes across the DIR port. The direction polarity is controlled by the UART_MDR3[3] DIR_POL bit. The direction is determined by the hardware monitoring the TX FIFO and the TX shift register. When both are empty the transceiver is set to RX. There is a guard band delay counter of 3 bit clock cycles after the TX shift register is going empty to allow time for the stop bit to transition through the transceiver before a direction change to receive might be applied.

Figure 12-142 shows the direction control.



(1) Assumes DIR_POL = 1

Figure 12-142. RS-485 External Transceiver Direction Control

12.2.4.4.8.3 IrDA Mode

12.2.4.4.8.3.1 IrDA Clock Generation: Baud Generator

The IrDA function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 12-143 shows the baud rate generator and associated controls.

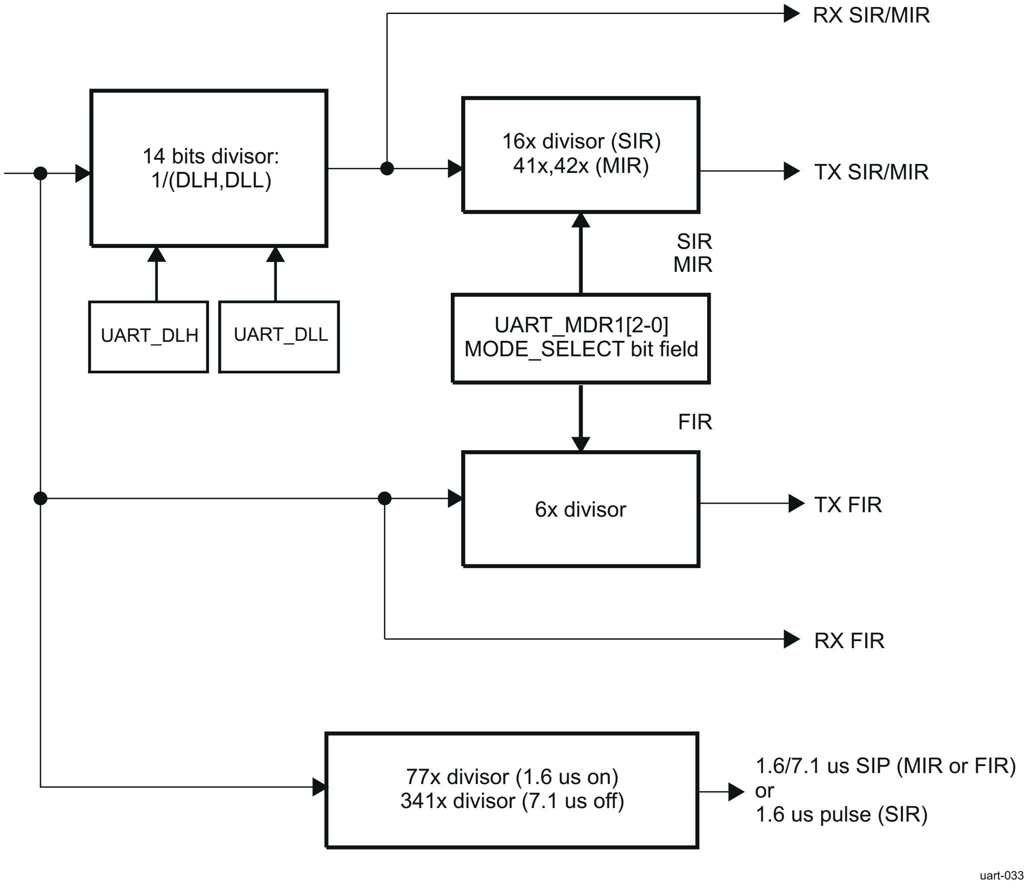


Figure 12-143. IrDA Baud Rate Generator

CAUTION

Before initializing or modifying clock parameter controls (UART_DLH, UART_DLL), MODE_SELECT=DISABLE (UART_MDR1[2-0] MODE_SELECT) must be set to 0x7). Failure to observe this rule can result in unpredictable module behavior.

12.2.4.4.8.3.2 Choosing the Appropriate Divisor Value

Three divisor values are:

- SIR mode: Divisor value = Operating frequency/(16× baud rate)
- MIR mode: Divisor value = Operating frequency/(41×/42× baud rate)
- FIR mode: Divisor value = None

Table 12-160 lists the IrDA baud rate settings.

Table 12-160. IrDA Baud Rate Settings

Baud Rate	IR Mode	Baud Multiple	Encoding	DLH, DLL (Decimal)	Actual Baud Rate	Error (%)	Source Jitter (%)	Pulse Duration
2.4 kbps	SIR	16x	3/16	1250	2.4 kbps	0	0	78.1 µs
9.6 kbps	SIR	16x	3/16	312	9.6153 kbps	+0.16	0	19.5 µs
19.2 kbps	SIR	16x	3/16	156	19.231 kbps	+0.16	0	9.75 µs
38.4 kbps	SIR	16x	3/16	78	38.462 kbps	+0.16	0	4.87 µs
57.6 kbps	SIR	16x	3/16	52	57.692 kbps	+0.16	0	3.25 µs
115.2 kbps	SIR	16x	3/16	26	115.38 kbps	+0.16	0	1.62 µs
0.576 Mbps	MIR	41×/42×	1/4	2	0.5756 Mbps(1)	0	+1.63/-0.80	416 ns
1.152 Mbps	MIR	41×/42×	1/4	1	1.1511 Mbps(1)	0	+1.63/-0.80	208 ns
4 Mbps	FIR	6×	4 PPM	–	4 Mbps	0	0	125 ns

(1) Average value

Note

Baud rate error and source jitter table values do not include 48-MHz reference clock error and jitter.

12.2.4.4.8.3.3 IrDA Data Formatting

The methods described in this section apply to all IrDA modes (SIR, MIR, and FIR).

12.2.4.4.8.3.3.1 IR RX Polarity Control

The UART_MDR2[6] IRRXINVERT bit provides the flexibility to invert the RX pin in the UART to ensure that the protocol at the output of the transceiver has the same polarity at module level. By default, the RX pin is inverted because most transceivers invert the IR receive pin.

12.2.4.4.8.3.3.2 IrDA Reception Control

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

Operation of the RX input can be disabled by the UART_ACREG[5] DIS_IR_RX bit.

12.2.4.4.8.3.3.3 IR Address Checking

In all IR modes, when address checking is enabled, only frames intended for the device are written to the RX FIFO. This restriction avoids receiving frames not meant for this device in a multipoint infrared environment. It is possible to program two frame addresses that the UART IrDA receives, with the UART_XON1_ADDR1[7-0] XON_WORD1 and UART_XON2_ADDR2[7-0] XON_WORD2 bit fields.

Setting the UART_EFR[0] bit to 1 selects address1 checking. Setting the UART_EFR[1] bit to 1 selects address2 checking. Setting the UART_EFR[1-0] bit field to 0 disables all address checking operations. If both bits are set, the incoming frame is checked for private and public addresses.

If address checking is disabled, all received frames write to the RX FIFO.

12.2.4.4.8.3.3.4 Frame Closing

A transmission frame can be terminated in two ways:

- Frame-length method: Set the UART_MDR1[7] FRAME_END_MODE bit to 0. The Host CPU writes the value of the frame length to the UART_TXFLH and UART_TXFLL registers. The device automatically attaches end flags to the frame when the number of bytes transmitted equals the value of the frame length.
- Set-EOT bit method: Set the UART_MDR1[7] FRAME_END_MODE bit to 1. The Host CPU writes 1 to the UART_ACREG[0] EOT bit just before it writes the last byte to the TX FIFO. When the Host CPU writes the last byte to the TX FIFO, the device internally sets the tag bit for that character in the TX FIFO. As the TX state-machine reads data from the TX FIFO, it uses this tag-bit information to attach end flags and correctly terminate the frame.

12.2.4.4.8.3.3.5 Store and Controlled Transmission

In store and controlled transmission (SCT) mode, the Host CPU starts writing data to the TX FIFO. Then, after writing a part of a frame (for a bigger frame) or an entire frame (a small frame; that is, a supervisory frame), the Host CPU writes 1 to the UART_ACREG[2] SCTX_EN bit (deferred TX start) to start transmission.

SCT mode is enabled by setting the UART_MDR1[5] SCT bit to 1. This transmission method differs from normal mode, in which data transmission starts immediately after data is written to the TX FIFO. SCT mode is useful for sending short frames without TX underrun.

12.2.4.4.8.3.3.6 Error Detection

When the UART_LSR_UART register is read, the UART_LSR_UART[4-2] bit field reflects the error bits [FL, CRC, ABORT] of the frame at the top of the STATUS FIFO (the next frame status to be read).

The error is triggered by an interrupt (for IrDA mode interrupts, see Table 12-144). The STATUS FIFO must be read until empty (a maximum of eight reads is required).

12.2.4.4.8.3.3.7 Underrun During Transmission

Underrun during transmission occurs when the TX FIFO is empty before the end of the frame is transmitted. When underrun occurs, the device closes the frame with end flags but attaches an incorrect CRC value. The receiving device detects a CRC error and discards the frame; it can then ask for a retransmission.

Underrun also causes an internal flag to be set, which disables additional transmissions. Before the next frame can be transmitted, the Host CPU must:

- Reset the TX FIFO.
- Read the UART_RESUME register, which clears the internal flag.

This function can be disabled by the UART_ACREG[4] DIS_TX_UNDERRUN bit, compensated by the extension of the stop-bit in transmission if the TX FIFO is empty.

12.2.4.4.8.3.3.8 Overrun During Receive

Overrun during receive for the IrDA mode has the same function as that for the UART mode (see Section 12.2.4.4.8.1.3.6, *Overrun During Receive*).

12.2.4.4.8.3.3.9 Status FIFO

In IrDA modes, a status FIFO records the received frame status. When a complete frame is received, the length of the frame and the error bits associated with the frame are written to the status FIFO.

Reading the UART_SFREGH[3-0] MSB and UART_SFREGL[3-0] (LSB) bit fields obtains the frame length. The frame error status is read in the UART_SFLSR register. Reading the UART_SFLSR register increments the status FIFO read pointer. Because the status FIFO is eight entries deep, it can hold the status of eight frames.

The Host CPU uses the frame-length information to locate the frame boundary in the received frame data. The Host CPU can screen bad frames using the error status information and can later request the sender to resend only the bad frames.

This status FIFO can be used effectively in DMA mode because the Host CPU must be interrupted only when the programmed status FIFO trigger level is reached, not each time a frame is received.

12.2.4.4.8.3.3.10 Multi-drop Parity Mode with Address Match

Multi-drop mode is enabled in the UART_EFR2 register.

Address matching mode is only available with 8 bit character length setting. UART_LCR[1-0] CHAR_LENGTH bit fields should always be set to 0x11 (8 bits) prior to enabling the feature.

This mode allows the transmitter to send data on a line where multiple receivers are connected, when supported. In this mode, a set parity bit is used to mark an address, and a parity of 0 denotes data.

This setting affects how the parity is generated. Writing a 0x1 into the UART_ECR[0] A_MULTIDROP bit will set the parity bit for the next byte to be sent, which will then be considered an address, for sending a data frame, the UART_ECR[0] A_MULTIDROP bit has to be cleared.

On reception if the feature is enabled by setting the UART_EFR2[2] MULTIDROP bit to 0x1 incoming frames with parity set to 0x1 are treated as address frames and with parity set to 0x0 as data frames. The receiver will drop all data frames until a matching address frame was found.

The matching address is determined by the values set in UART_MAR, UART_MMR and UART_MBR registers and the value set in UART_EFR2[7] BROADCAST bit.

Table 12-161 summarizes the operation of address matching based on the mentioned values.

Table 12-161. Details of address matching

Received frame	Received parity	Frame type	UART_MAR	UART_MMR	UART_MBR	UART_EFR2[7] BROADCAST	Operation of receiver	Address matching
0xXX(2)	0	DATA	X(1)	X(1)	0xXX(2)	X(1)	Drops data until matching address found	N/A
0xXX(2)	1	ADDRESS	0xXX(2)	0x00	0xXX(2)	0	Matches any address	Yes
0xEF	1	ADDRESS	0xXX(2)	0xXX(2)	0xEF	1	Matches broadcast address	Yes
0x1A	1	ADDRESS	0x1A	0xFF	0xXX(2)	0	Single address match	Yes
0xF5	1	ADDRESS	0xF3	0xF9	0xXX(2)	0	Group address match	Yes

(1) X indicates a do not care bit value
(2) 0xXX indicates a do not care 8 bit hexadecimal value

The possible values for matching address can be calculated in the following way:

- Single and Group addresses can be formed by masking the UART_MAR registers value with the value set in the UART_MMR register, bits set to 0x0 in the UART_MMR register result in do not care values.
- Broadcast addresses can be set in the UART_MBR register if broadcast address is enabled in the UART_EFR2[7] BROADCAST bit, the module will match on received address frames containing the broadcast address.
- For more details, see example below:
  - UART_MAR: 0xF3, UART_MMR: 0xF9, UART_MBR: 0xFF
  - Single and Group addresses: 0xF1, 0xF3, 0xF5, 0xF7
  - Broadcast addresses: 0xFF

If an address match occurred the matching address value can be obtained from the UART_RHR register in the following way:

- If the FIFO is disabled or the threshold is set to 0x1, the matching address can be directly read from UART_RHR as the FIFO will not be overwritten.
- If the FIFO is enabled or the threshold is greater than 0x1, the matching address will be the latest frame in the FIFO with a parity error bit set.

For received data, the parity error bit in the UART_LSR_UART register is set when a bit with a parity of 0x1 is received indicating an address frame and the received address matches based on the values of UART_MAR, UART_MMR, UART_MBR and UART_EFR2[2] MULTIDROP bit.

In Multi-drop mode no parity is used, as the parity bit is used to differentiate address and data frames. The parity error bit is used for indicating an address match.

For enabling the interrupt generation for address matching UART_IER_UART[2] LINE_STS_IT bit has to be set to 0x1.

An interrupt for the matching address can be identified by reading the UART_IIR_UART[5-1] IT_TYPE bit fields, a value of 0x00011 indicates a receiver line status error. After the UART_LSR_UART[2] RX_PE bit has to be read, a value of 0x1 indicates that an address match occurred. The reception of a frame is indicated with a value of 0x1 in the UART_LSR_UART[0] RX_FIFO_E bit as the matching value is written into the FIFO regardless of the frame type (data or address). UART_LSR_UART[7] RX_FIFO_STS bit will also be set to 0x1 as the parity error bit is used to indicate a matching address.

Note that the operation of the UART_LSR_UART[2] RX_PE bit depends on the value set in UART_EFR2[2] MULTIDROP bit. If UART_EFR2[2] MULTIDROP bit is set to 0x0, UART_LSR_UART[2] RX_PE bit is used to indicate a received parity error. If UART_EFR2[2] MULTIDROP bit is set to 0x1, the receiver is in Multi-drop Address Match mode, thus the value in UART_LSR_UART[2] RX_PE bit is used to indicate an address match.

The interrupt is cleared the same way in both operation modes: reading the UART_LSR_UART register updates the values.

12.2.4.4.8.3.3.11 Time-guard

The time-guard feature enables the UART interface to operate with slow remote devices.

When set, it will insert a number of idle states between transmitting two characters, the length of which can be set in the UART_TIMEGUARD register. The value in the register defines the number of baud clocks of idle period to insert.

This idle state essentially acts like a long stop bit.

12.2.4.4.8.3.4 SIR Mode Data Formatting

This section provides specific instructions for SIR mode programming.

12.2.4.4.8.3.4.1 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

A transmission frame can be aborted by setting the UART_ACREG[1] ABORT_EN bit to 1. When this bit is set to 1, 0x7D and 0xC1 are transmitted and the frame is not terminated with CRC or stop flags.

When a 0x7D character followed immediately by a 0xC1 character is received without transparency, the receiver treats a frame as an aborted frame.

CAUTION

When the TX FIFO is not empty and the UART_MDR1[5] SCT bit is set to 1, the UART IrDA starts a new transfer with data of a previous frame when the aborted frame is sent. Therefore, the TX FIFO must be reset before sending an aborted frame.

12.2.4.4.8.3.4.2 Pulse Shaping

SIR mode supports the 3/16 or the 1.6-μs pulse duration methods. The UART_ACREG[7] PULSE_TYPE bit selects the pulse width method in the transmit mode.

12.2.4.4.8.3.4.3 SIR Free Format Programming

The SIR FF mode is selected by setting the module in the UART mode (UART_MDR1[2-0] MODE_SELECT = 0x0) and the UART_MDR2[3] PULSE bit to 1 to allow pulse shaping.

Because the bit format stays the same, some UART mode configuration registers must be set at specific values:

- UART_LCR[1-0] CHAR_LENGTH bit field = 0x3 (8 data bits)
- UART_LCR[2] NB_STOP bit = 0x0 (1 stop-bit)
- UART_LCR[3] PARITY_EN bit = 0x0 (no parity)

The UART mode interrupts are used for the SIR FF mode, but many are not relevant (XOFF, RTS, CTS, modem status register, etc.).

12.2.4.4.8.3.5 MIR and FIR Mode Data Formatting

This section describes common instructions for FIR and MIR mode programming.

At the end of a frame reception, the CPU reads the line status register (UART_LSR_UART) to detect errors in the received frame.

When the UART_MDR1[6] SIP_MODE bit is set to 1, the TX state-machine always sends one SIP at the end of a transmission frame. However, when the SIP_MODE bit is set to 0, SIP transmission depends on the UART_ACREG[3] SEND_SIP bit.

The CPU can set the SEND_SIP bit at least once every 500 ms. The advantage of this approach over the default approach is that the TX state-machine does not have to send the SIP at the end of each frame, thus reducing the overhead required.

12.2.4.4.8.4 CIR Mode

12.2.4.4.8.4.1 CIR Mode Clock Generation

Depending on the encoding method (variable pulse distance/biphase), the Host CPU must develop a data structure that combines 1 and 0 with a *t* period to encode the complete frame to transmit. This can then be transmitted to the infrared output with a modulation method, as shown in Figure 12-144.

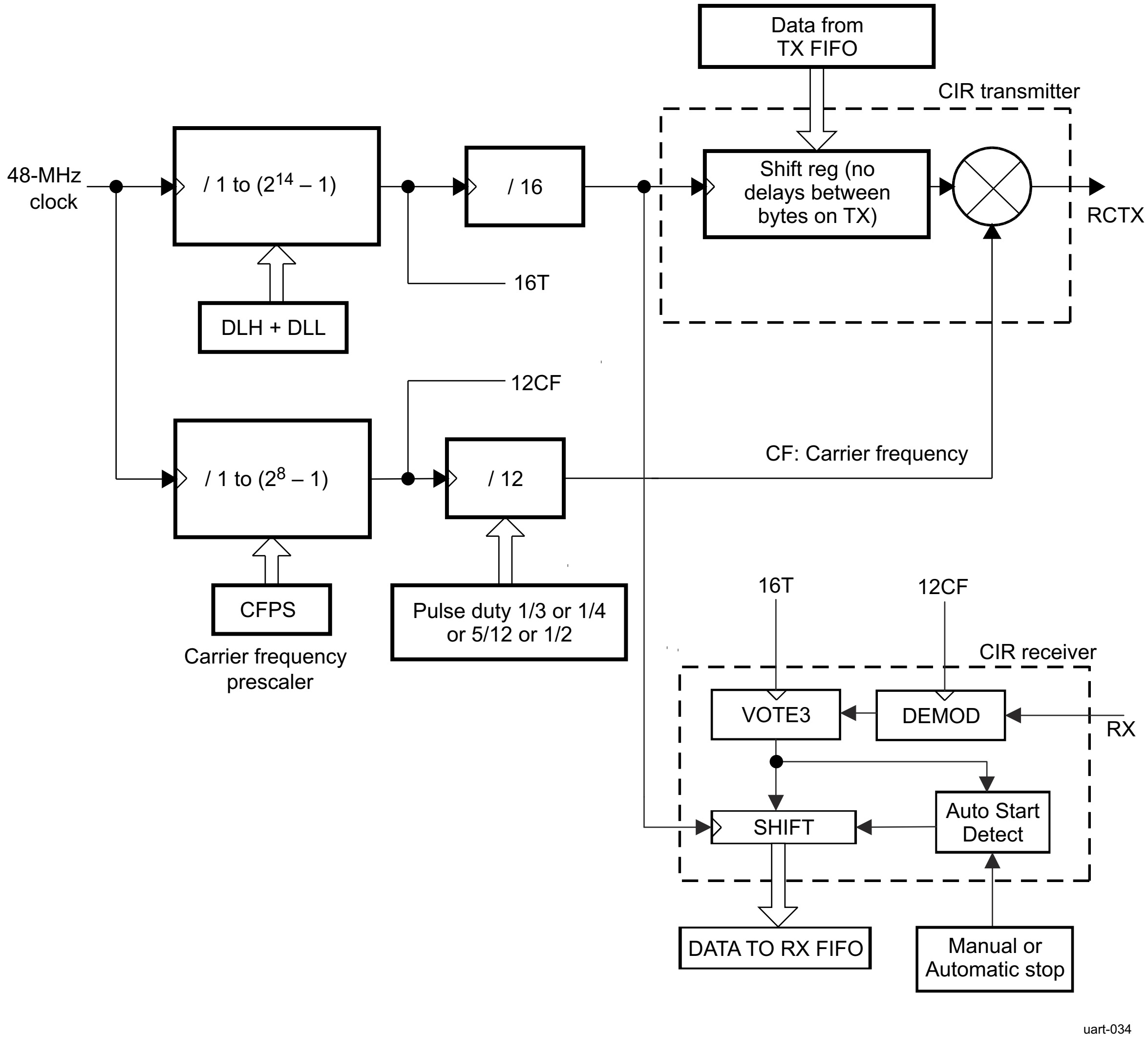


Figure 12-144. CIR Mode Block Components

Based on the requested modulation frequency, the UART_CFPS register must be set with the correct dividing value to provide an accurate pulse frequency:

Dividing value = (FCLK / 12) / MODfreq

Where:

FCLK = System clock frequency (48 MHz)

12 = Real value of baud multiple

MODfreq = Effective frequency of the modulation (MHz)

Example: For a targeted modulation frequency of 36 kHz, the value of CFPS must be set to 0x7 (decimal), which provides a modulation frequency of 36.04 kHz.

Note

The UART_CFPS register starts with a reset value of 105 (decimal), which translates to a frequency of 38.1 kHz.

The duty cycle of these pulses is user-defined by the pulse duty register bits in the UART_MDR2 register. Table 12-162 shows the duty cycle.

Table 12-162. CIR Duty Cycle

UART_MDR2[5-4] CIR_PULSE_MODE	Duty Cycle (High-Level)
00	1/4
01	1/3
10	5/12
11	1/2

12.2.4.4.8.4.2 CIR Data Formatting

The methods described in this section apply to all CIR modes.

12.2.4.4.8.4.2.1 IR RX Polarity Control

The IR RX polarity control for CIR mode has the same function as that for IrDA mode (see Section 12.2.4.4.8.3.3.1, *IR RX Polarity Control*).

12.2.4.4.8.4.2.2 CIR Transmission

In transmission, the Host CPU software must exercise an element of real-time control to transmit data packets, each of which must be emitted at a constant delay from the start-bits of each individual packet. Thus, when sending a series of packets, the packet-to-packet delay must respect a specific delay. Two methods can be used to control this delay:

- Filling the TX FIFO with a number of zero bits that are transmitted with a *t* period
- Using an external system timer to control the delay between each start-of-frame or between the end of a frame and the start of the next one. This can be performed by:
  - Controlling the start of the frame using the UART_MDR1[5] SCT bit and the UART_ACREG[2] SCTX_EN bit, depending on the timer status
  - Using the UART_IIR_UART[5] TX_STATUS_IT interrupt bit to preload the next frame in the TX FIFO and to control the start of the timer (in case of control delay between the end of a frame and the start of the next frame)

12.2.4.4.8.4.2.3 CIR Reception

In reception, there are 2 ways to stop it

- The Host CPU can disable the reception by setting the UART_ACREG[5] DIS_IR_RX bit to 1. When it considers that the reception is finished because a large number of 0 has been received. To receive a new frame, the UART_ACREG[5] DIS_IR_RX bit must be set to 0.
- Using a specific mechanism, depending on the value set in the BOF length register (UART_EBLR), allows stopping automatically the reception. If the value set in the UART_EBLR register is different than 0, this features is enabled and count a number of bit received at 0. When the counter achieved the value defined in the UART_EBLR register, the reception is automatically stop and UART_IIR_CIR[2] RX_STOP_IT bit is set. When a 1 is detected on the RX pin, the reception is automatically enabled.

There is a limitation when receiving data in UART CIR mode. The IrDA transceivers on the market have a common characteristic that shrinks the hold time of the received modulation pulse. The UART filtering schema on receiving is based on the same encoding mechanism used in transmission.

For the following scenario:

- shift register period: 0.9us
- modulation frequency: 36kHz
- duty cycle: 1/4 of a modulation frequency period

So the data sent in those conditions would look like 7us pulses within 28us period. The UART expects to receive similar incoming data on receive, but available transceiver timing characteristics typically send 2us modulated pulses. Those will be filtered out and RX FIFO will not receive any data.

This does not affect UART CIR mode in transmission.

Note

The CIR RX demodulation can be bypassed by setting the UART_MDR3[0] DISABLE_CIR_RX_DEMOD bit.

12.2.4.5 UART Programming Guide

This section describes the procedure for operating the UART with FIFO and DMA or interrupts. This three-part procedure ensures the quick start of the UART. It does not cover every UART feature.

The first programming model covers software reset of the UART. The second programming model describes FIFO and DMA configuration. The last programming model describes protocol, baud rate, and interrupt configuration.

Note

Each programming model can be used independently of the other two; for instance, reconfiguring the FIFOs and DMA settings only.

Each programming model can be executed starting from any UART register access mode (register modes, submodes, and other register dependencies). However, if the UART register access mode is known before executing the programming model, some steps that enable or restore register access are optional. For more information, see Section 12.2.4.4.7.1, *Register Access Modes*.

12.2.4.5.1 UART Global Initialization

12.2.4.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the UART module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the UART.

For more information, see , *UART Integration*.

12.2.4.5.1.2 UART Module Global Initialization

The procedure in Table 12-163 can be used to initialize UART when performing software reset.

Table 12-163. UART Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	UART_SYSC[1] SOFTRESET	1
Wait until reset is finished.	UART_SYSS[0] RESETDONE	=1

12.2.4.5.2 UART Mode selection

Table 12-164 describes how to set different register access mode.

Table 12-164. UART Configure Register Access Mode

Step	Register/Bit Field/Programming Model	Value
Set the register access mode A	UART_LCR[7] DIV_EN	1
	UART_LCR[7-0]	≠0xBF
Set the register access mode B	UART_LCR[7-0]	0xBF
Set the operational mode	UART_LCR[7] DIV_EN	0

12.2.4.5.3 UART Submode selection

This section describes how to set different register access submode.

Table 12-165. UART Configure Register Access Submode TCR_TLR

Step	Register/Bit Field/Programming Model	Value
Configure the submode TCR_TLR		
Configure mode B	see Table 12-164	
Enable writing to register bits UART_MCR[7-5]	UART_EFR[4] ENHANCED_EN	1
Configure mode A	see Table 12-164	0x1
Set the submode TCR_TLR	UART_MCR[6] TCR_TLR	1

Table 12-166. UART Configure Register Access Submode MSR_SPR

Step	Register/Bit Field/Programming Model	Value
First option: configure the submode MSR_SPR		
Configure mode B	see Table 12-164	
Set the submode MSR_SPR	UART_EFR[4] ENHANCED_EN	0
Second option: configure the submode MSR_SPR		
Configure mode B	see Table 12-164	
Enable writing to register bits UART_MCR[7-5]	UART_EFR[4] ENHANCED_EN	1
Set the submode MSR_SPR	UART_MCR[6] TCR_TLR	0

Table 12-167. UART Configure Register Access Submode XOFF

Step	Register/Bit Field/Programming Model	Value
Configure of the XOFF		
Configure B	see Table 12-164	
Set the submode XOFF	UART_EFR[4] ENHANCED_EN	0

12.2.4.5.4 UART Load FIFO trigger and DMA mode settings

12.2.4.5.4.1 DMA mode Settings

To enable and configure program the DMA mode, perform the following steps:

Table 12-168. DMA Mode Settings

Step	Register/Bit Field/Programming Model	Value
Set the option of DMA mode configuration	UART_SCR[0] DMA_MODE_CTL	-
IF Configure DMA mode 0 and 1	UART_SCR[0] DMA_MODE_CTL	=0
Select the DMA mode, for more information see Section 12.2.4.4.6.4	UART_FCR[3] DMA_MODE	-
IF Configure DMA mode from 0 to 3	UART_SCR[0] DMA_MODE_CTL	=1
Select the DMA mode, for more information see Section 12.2.4.4.6.4	UART_SCR[2-1] DMA_MODE_2	-

12.2.4.5.4.2 FIFO Trigger Settings

In this section is described configuration and settings of FIFO trigger level, which enable DMA and interrupt generation.

Table 12-169. Load FIFO Triggers Defined by the FCR

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-165	0x-
Set the desire RX FIFO trigger level	UART_FCR[5-4] TX_FIFO_TRIG	0x-
Set the desire TX FIFO trigger level	UART_FCR[7-6] RX_FIFO_TRIG	0x-

Table 12-170. Load FIFO Triggers Defined by the TLR

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-165	0x-
Set the desire RX FIFO trigger level	UART_TLR[7-4] RX_FIFO_TRIG_DMA	0x-
Set the desire TX FIFO trigger level	UART_TLR[3-0] TX_FIFO_TRIG_DMA	0x-

Table 12-171. Load FIFO Triggers Defined by the Concatenated Value

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-165	0x-
Set the register bit	UART_SCR[7] RX_TRIG_GRANU1	1
Set the desire RX FIFO trigger level	UART_TLR[7-4] RX_FIFO_TRIG_DMA UART_FCR[7-6] RX_FIFO_TRIG	0x-

Table 12-171. Load FIFO Triggers Defined by the Concatenated Value (continued)

Step	Register/Bit Field/Programming Model	Value
Set the register bit	UART_SCR[6] TX_TRIG_GRANU1	1
Set the desire TX FIFO trigger level	UART_TLR[3-0] TX_FIFO_TRIG_DMA UART_FCR[5-4] TX_FIFO_TRIG	0x-

12.2.4.5.5 UART Protocol, Baud rate and interrupt settings

12.2.4.5.5.1 Baud rate settings

Table 12-172. UART Baud Rate Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Switch to register configuration mode B	see Table 12-164	
Enable access to UART_IER_UART[7-4]	UART_EFR[4] ENHANCED_EN	1
Switch register operational mode	see Table 12-164	
Disable sleep mode	UART_IER_UART[4] SLEEP_MODE	0
Switch to register configuration mode A or B	see Table 12-164	
Set the appropriate divisor value	UART_DLL[7-0] CLOCK_LSB UART_DLH[5-0] CLOCK_MSB	0x-

12.2.4.5.5.2 Interrupt settings

Table 12-173. UART Interrupt Settings

Step	Register/Bit Field/Programming Model	Value
Switch to register configuration mode B	see Table 12-164	0x7
Enable access to UART_IER_UART[7-4]	UART_EFR[4] ENHANCED_EN	1
Switch register operational mode	see Table 12-164	
Set the desired interrupt configuration (0: Disable the interrupt; 1: Enable the interrupt)	UART_IER_UART[7] CTS_IT UART_IER_UART[6] RTS_IT UART_IER_UART[5] XOFF_IT UART_IER_UART[4] SLEEP_MODE UART_IER_UART[3] MODEM_STS_IT UART_IER_UART[2] LINE_STS_IT UART_IER_UART[1] THR_IT UART_IER_UART[0] RHR_IT	0x-

12.2.4.5.5.3 Protocol settings

Load the desired protocol formatting (parity, stop-bit, character length) and switch to register operational mode.

Table 12-174. UART Protocol Settings

Step	Register/Bit Field/Programming Model	Value
Load desired protocol formatting, see Section 12.2.4.4.8.1.3.1 , *Frame Formatting*	UART_LCR[5] PARITY_TYPE_2 UART_LCR[4] PARITY_TYPE_1 UART_LCR[3] PARITY_EN UART_LCR[2] NB_STOP UART_LCR[1-0] PARITY_LENGTH	0x-
Switch to register operational mode	UART_LCR[7] DIV_EN UART_LCR[6] BREAK_EN	0

12.2.4.5.5.4 UART/RS-485/IrDA(SIR/MIR/FIR)/CIR

Table 12-175. UART Mode Selection

Step	Register/Bit Field/Programming Model	Value
Load the desired UART/IrDA (SIR, MIR, FIR)/CIR modes, see Section 12.2.4.4.7.2, *UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection*	UART_MDR1[2-0] MODE_SELECT	0x-
Load the desire RS-485 mode, see Section 12.2.4.4.7.2, *UART/RS-485/IrDA (SIR, MIR, FIR)/CIR Mode Selection*	UART_MDR3[4] DIR_EN	0x1

12.2.4.5.5.5 UART Multi-drop Parity Address Match Mode Configuration

Table 12-176. UART Multi-drop Parity Address Match Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Disable receive mode	UART_ECR[3] RX_EN	0
Enable Multi-drop parity Address match mode	UART_EFR2[2] MULTIDROP	1
Set the matching device address	UART_MAR[7-0] ADDRESS	0x-
Set the address match masking	UART_MMR[7-0] MASK	0x-
Set the broadcast address match	UART_MBR[7-0] BROADCAST_ADDRESS	0x-
Enable broadcast address matching if needed	UART_EFR2[7] BROADCAST	1
Enable receive mode	UART_ECR[3] RX_EN	1

12.2.4.5.6 UART Hardware and Software Flow Control Configuration

This section describes the programming steps to enable and configure hardware and software flow control. Hardware and software flow control cannot be used at the same time.

12.2.4.5.6.1 Hardware Flow Control Configuration

Table 12-177. UART Hardware Flow Control Configuration

Step	Register/Bit Field/Programming Model	Value
Configure register submode TCR_TLR	see Table 12-165	0x7
Load the start and halt trigger value.	UART_TCR[7-4] AUTO_RTS_START UART_TCR[3-0] AUTO_RTS_HALT	0x-
Enable or disable receive and transmit hardware flow control mode.	UART_EFR[7] AUTO_CTS_EN UART_EFR[6] AUTO_RTS_EN	0x-

12.2.4.5.6.2 Software Flow Control Configuration

Table 12-178. UART Software Flow Control Configuration

Step	Register/Bit Field/Programming Model	Value
Set the register access submode XOFF	see Table 12-167	
Load the software control characters	UART_XON1_ADDR1[7-0] XON_WORD1 UART_XON2_ADDR2[7-0] XON_WORD2 UART_XOFF1[7-0] XOFF_WORD1 UART_XOFF2[7-0] XOFF_WORD2	0x-
Set the register access submode TCR_TLR	see Table 12-165	
Enable or disable XON any function (0: Disable; 1: Enable).	UART_MCR[5] XON_EN	--
Load start and halt trigger value for software flow control	UART_TCR[7-4] AUTO_RTS_START UART_TCR[3-0] AUTO_RTS_HALT	0x-
Enable or disable special character function (0: Disable; 1: Enable)	UART_EFR[5] SPEC_CHAR	0x-
Set the software flow control mode	UART_EFR[3-0] SW_FLOW_CONTROL	0x-

12.2.4.5.7 IrDA Programming Model

12.2.4.5.7.1 SIR mode

12.2.4.5.7.1.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with parity forced to 1, baud rate = 115.2 kbps, FIFOs disabled, 2 stop-bits, and 8-bit word length:

Table 12-179. SIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate(115.2 Kbps)	UART_DLL[7-0] CLOCK_LSB	0x1A
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.2.4.5.7.1.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 6-byte frame with no parity, baud rate = 115.2 kbps, FIFOs disabled, 3/16 encoding, 2 stop-bits, and 7-bit word length:

Table 12-180. SIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (115.2 Kbps)	UART_DLL[7-0] CLOCK_LSB	0x1A
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force output DTR to active	UART_MCR[0] DTR	1
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	0x1
Set transmit frame length to 6 bytes	UART_TXFLL[7-0] TXFLL	0x06
Set the seven starts of frame transmission	UART_EBLR[7-0] EBLR	0x08
Set SIR pulse width to be 1.6 μs	UART_ACREG[7] PULSE_TYPE	1

12.2.4.5.7.2 MIR mode

12.2.4.5.7.2.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled.

Table 12-181. MIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (1.152 bps)	UART_DLL[7-0] CLOCK_LSB	0x01
	UART_DLH[5-0] CLOCK_MSB	0x00
Set MIR mode	UART_MDR1[2-0] MODE_SELECT	0x4
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force outputs DTR and RTS to active	UART_MCR[1-0]	0x3

Table 12-181. MIR Mode Receive Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.2.4.5.7.2.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 60-byte frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled.

Table 12-182. MIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Load the baud rate (115.2 kbps)	UART_DLL[7-0] CLOCK_LSB	0x01
	UART_DLH[5-0] CLOCK_MSB	0x00
Set SIR mode	UART_MDR1[2-0] MODE_SELECT	0x4
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Force output DTR to active	UART_MCR[0] DTR	1
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	0x1
Set transmit frame length to 60 bytes	UART_TXFLL[7-0] TXFLL	0x3C
Set the eight additional starts of frame transmission	UART_EBLR[7-0] EBLR	0x08
SIP is sent at the end of transmission	UART_ACREG[3] SEND_SIP	1

12.2.4.5.7.3 FIR mode

12.2.4.5.7.3.1 Receive

The following programming model explains how to program the module to receive the IrDA frame with no parity, baud rate = 4 Mbps, FIFOs enabled, 8-bit word length.

Table 12-183. FIR Mode Receive Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80
Enable access to change UART_FCR[0]	UART_DLL[7-0] CLOCK_LSB	0x0
	UART_DLH[7-0] CLOCK_MSB	
FIFO clear and enable	UART_FCR[2-0]	0x7
Set the FIFO trigger level	see Section 12.2.4.5.4, *Load FIFO trigger and DMA mode settings*	
Set FIR mode	UART_MDR1[2-0] MODE_SELECT	0x5
Set frame length	UART_RXFLL[7-0] RXFLL	0xA
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Enable the UART_RHR interrupt	UART_IER_IRDA[0] RHR_IT	1

12.2.4.5.7.3.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 4-byte frame with no parity, baud rate = 4 Mbps, FIFOs enabled, and 8-bit word length.

Table 12-184. FIR Mode Transmit Settings

Step	Register/Bit Field/Programming Model	Value
Disable UART mode	UART_MDR1[2-0] MODE_SELECT	0x7
Grant access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x80

Table 12-184. FIR Mode Transmit Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Enable access to change UART_FCR[0]	UART_DLL[7-0] CLOCK_LSB UART_DLH[5-0] CLOCK_MSB	0x0
FIFO clear and enable	UART_FCR[2-0]	0x7
Set the FIFO trigger level	see Section 12.2.4.5.4, *Load FIFO trigger and DMA mode settings*	
Set FIR mode	UART_MDR1[2-0] MODE_SELECT	0x1
Disable access to the UART_DLL and UART_DLH registers	UART_LCR[7-0]	0x00
Set FIR mode and enable auto-SIP mode	UART_MDR1[7-0]	0x45
Set frame length	UART_TXFLL[7-0] TXFLL UART_TXFLH[7-0] TXFLH	0x4 0x0
Force output DTR to active	UART_MCR[0] DTR	1
Enable the UART_THR interrupt	UART_IER_IRDA[1] THR_IT	1
Set the eight additional starts of frame transmission	UART_EBLR[7-0] EBLR	0x08
SIP is sent at the end of transmission	UART_ACREG[3] SEND_SIP	1

12.3 High-Speed Serial Interfaces

This section describes the high speed serial interfaces in the devices.

12.3.1 Gigabit Ethernet Switch (CPSW3G)

This chapter describes the Gigabit Ethernet Switch (CPSW3G) subsystem in the device.

12.3.1.1 CPSW0 Overview

The 3-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch.

Figure 12-145 shows the CPSW0 module overview.

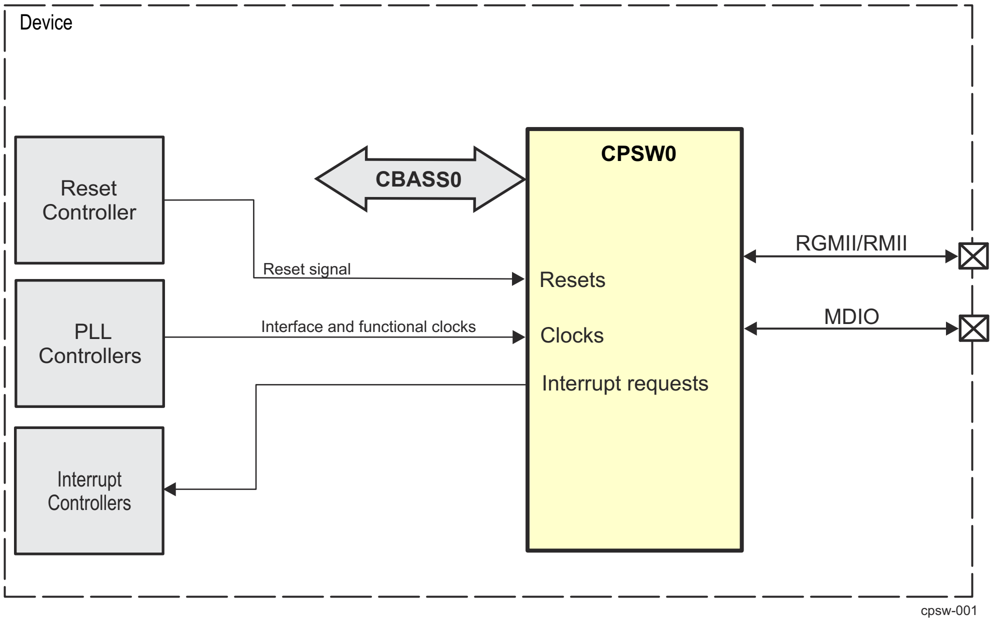


Figure 12-145. CPSW0 Overview

12.3.1.1.1 CPSW0 Features

The 3-port CPSW0 subsystem provides the following features:

- Two Ethernet ports (port 1 and 2) with selectable RGMII and RMII interfaces and an internal Communications Port Programming Interface (CPPI) port (port 0)
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Cut through switch support
- Eight priority level Quality Of Service (QOS) support (802.1p)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
  - Timestamp module capable of time stamping external timesync events like Pulse-Per-Second and also generating Pulse-Per-Second outputs
  - CPTS module that supports time stamping for IEEE1588 with support for 4 hardware push events and generation of compare output pulses
- DSCP Priority Mapping (IPv4 and IPv6)
- Energy Efficient Ethernet (EEE) support (802.3az)
- Flow Control Support (802.3x)
- Wire rate switching (802.1d)
- Non-Blocking switch fabric
- Time Sensitive Network Support
  - IEEE P802.3br Interspersing Express Traffic
  - IEEE 802.1Qbv Enhancements for Scheduled Traffic
- Address Lookup Engine (ALE)
  - 512 ALE table entries
  - Configurable number of addresses plus VLANs

  - Wire rate lookup
  - Host controlled time-based aging and/or auto-aging
  - Spanning tree support
  - L2 address lock and L2 filtering support
  - MAC authentication (802.1x)
  - Receive-based or destination-based Multicast and Broadcast rate limits
  - MAC address blocking
  - Source port locking
  - OUI (Vendor ID) host accept/deny feature
  - Configurable number of classifier/policers (32)
  - VLAN support
    - 802.1Q compliant
      - Auto add port VLAN for untagged frames on ingress
      - Auto VLAN removal on egress and auto pad to minimum frame size
- EtherStats and 802.3Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)
- Ethernet Mac transmit to Ethernet Mac receive Loopback mode (digital loopback) supported
- CPSGMII Loopback Modes (transmit to receive)
- Maximum frame size of 2024 bytes
- Management Data Input/Output (MDIO) module for PHY Management with Clause 45 support
- Programmable interrupt control with selected interrupt pacing
- Host port CPPI Streaming Packet Interface (CPPI_GCLK)
- Digital loopback and FIFO loopback modes supported
- Emulation support
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps modes only.
- RAM Error Detection and Correction (SECDED)

12.3.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.3.1.1.3 CPSW Terminology

Terminology:

AVB	Audio Video Bridging
AVBTP	Audio Video Bridging Trasport Protocol
BCCA	Best Controller Clock Algorithm
CFI	Canonical Format Indicator
CPPI	Communications Port Programming Interface
CPSW	Common Platform Switch
DLR	Device Level Ring
DSCP	Differentiated Services Code Point
EEE	Energy Efficient Ethernet
EMAC	Ethernet Media Access Control
EOP	End of Packet
EOQ	End of Queue
IPG	Inter-Packet Gap
LPI	Low Power Indicator
MDIO	Management Data Input/Output
MOF	Middle of Frame
OUI	Organizationally Unique Identifier
PFC	Priority based Flow Control
PTP	Precision Time Protocol
RMON	Remote Monitoring
RTCP	RTP Control Protocol
RTP	Real-time Transport Protocol
SCR	Switched Central Resource
SRP	Stream Reservation Protocol
TOS	Type of Service
VLAN	Virtual Local Area Network

12.3.1.2 CPSW0 Environment

This section describes the CPSW0 external connections (environment).

12.3.1.2.1 CPSW0 RMII Interface

Figure 12-146 shows a device with integrated EMAC and MDIO interfaced via a RMII connection in a typical system. The individual CPSW0 and MDIO signals for the RMII interface are summarized in Table 12-185.

The CPSW0 module integrated in the device supports internal and external clock sources in RMII mode. Figure 12-146 shows the internal clock source for RMII_MHZ_50_CLK clock. It is 50 MHz clock source that is provided on the CLKOUT0 device pin. This clock has to be routed on the PCB to the RMII_REF_CLK device pin and the external PHY, RMII clock input.

For more information, refer to either the IEEE 802.3 standard or ISO/IEC 8802-3:2000(E).

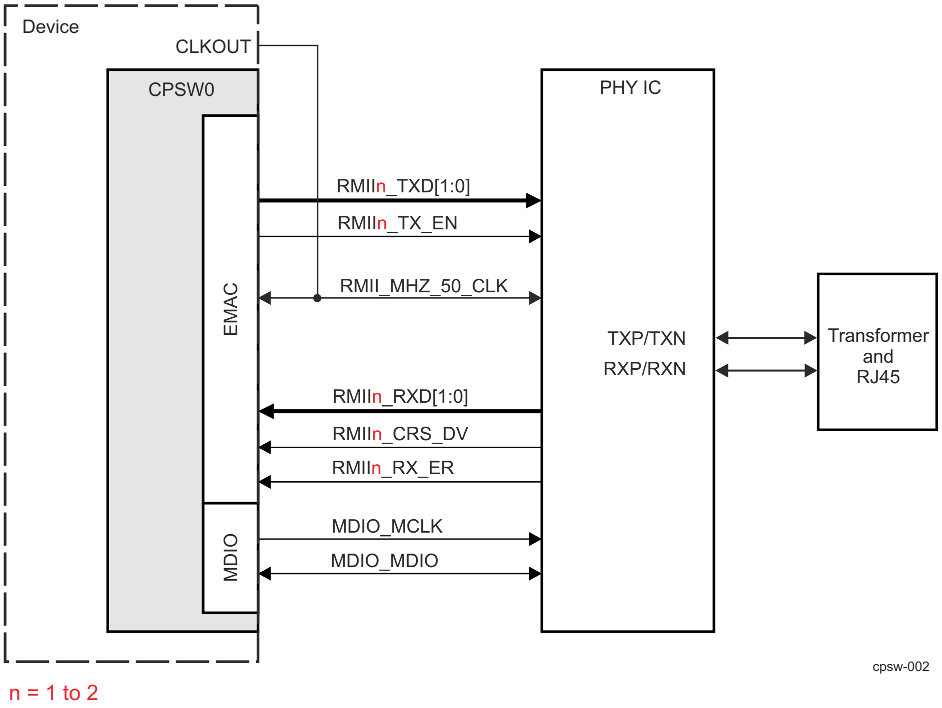
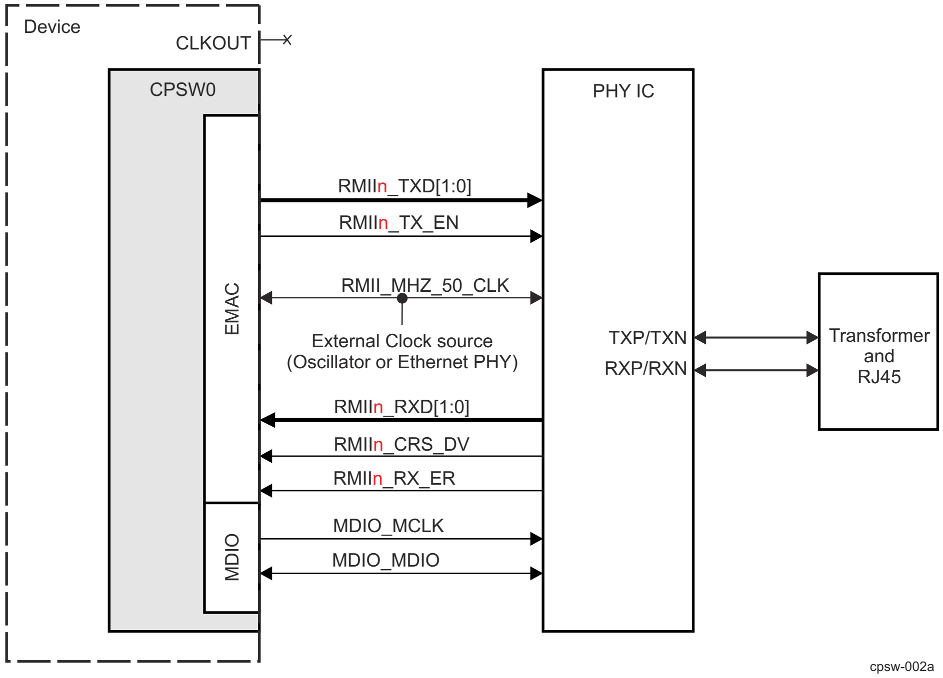


Figure 12-146. RMII Interface Typical Application (Internal Clock Source)

Figure 12-147 shows the external clock source for RMII_MHZ_50_CLK clock. In this case a 50 MHz clock is available on the PCB and it can be sourced from an oscillator or from the Ethernet PHY. This externally generated clock should be routed to both RMII_REF_CLK device pin and the external PHY, RMII clock input.



n = 1 to 2

Figure 12-147. RMII Interface Typical Application (External Clock Source)

Table 12-185. RMII I/O Description

Signal[2]	Device Pin(s)	I/O[1]	Description
RMIIn_TXD[1:0]	RMIIn_TXD[1:0]	O	Transmit data. The transmit data pins are a collection of 2 bits of data. TXD0 is the least-significant bit (LSB). The signals are synchronized by RMII_MHZ_50_CLK and valid only when RMIIn_TX_EN is asserted.
RMIIn_TX_EN	RMIIn_TX_EN	O	RMII transmit enable. The transmit enable signal indicates that the RMIIn_TXD[1:0] pins are generating data for use by the PHY. RMIIn_TX_EN is synchronous to RMII_MHZ_50_CLK.
RMII_MHZ_50_CLK	RMII_REF_CLK	I	RMII 50MHz reference clock. The reference clock is used to synchronize all RMII signals. RMII_MHZ_50_CLK must be continuous and fixed at 50 MHz.
RMIIn_RXD[1:0]	RMIIn_RXD[1:0]	I	Receive data. The receive data pins are a collection of 2 bits of data. RXD0 is the least-significant bit (LSB). The signals are synchronized by RMII_MHZ_50_CLK and valid only when RMIIn_CRS_DV is asserted and RMIIn_RX_ER is de-asserted.
RMIIn_CRS_DV	RMIIn_CRS_DV	I	Carrier sense/receive data valid. Multiplexed signal between carrier sense and receive data valid.
RMIIn_RX_ER	RMIIn_RX_ER	I	Receive error. The receive error signal is asserted to indicate that an error was detected in the received frame.
MDIO_MCLK	MDIO0_MDC	O	Management data clock (MDIO_MCLK). The MDIO data clock is sourced by the MDIO module on the system. It is used to synchronize MDIO data access operations done on the MDIO0_MDIO data pin.
MDIO_MDIO	MDIO0_MDIO	I/O	MDIO data pin drives PHY management data into and out of the PHY by way of an access frame consisting of start of frame, read/write indication, PHY address, register address, and data bit cycles. The MDIO0_MDIO pin acts as an output for all but the data bit cycles at which time it is an input for read operations.

(1) I = Input; O = Output
(2) n 1 to 2

12.3.1.2.2 CPSW0 RGMII Interface

Figure 12-148 shows a device with integrated EMAC and MDIO interfaced via a RGMII connection in a typical system. The individual CPSW0 and MDIO signals for the RGMII interface are summarized in Table 12-186.

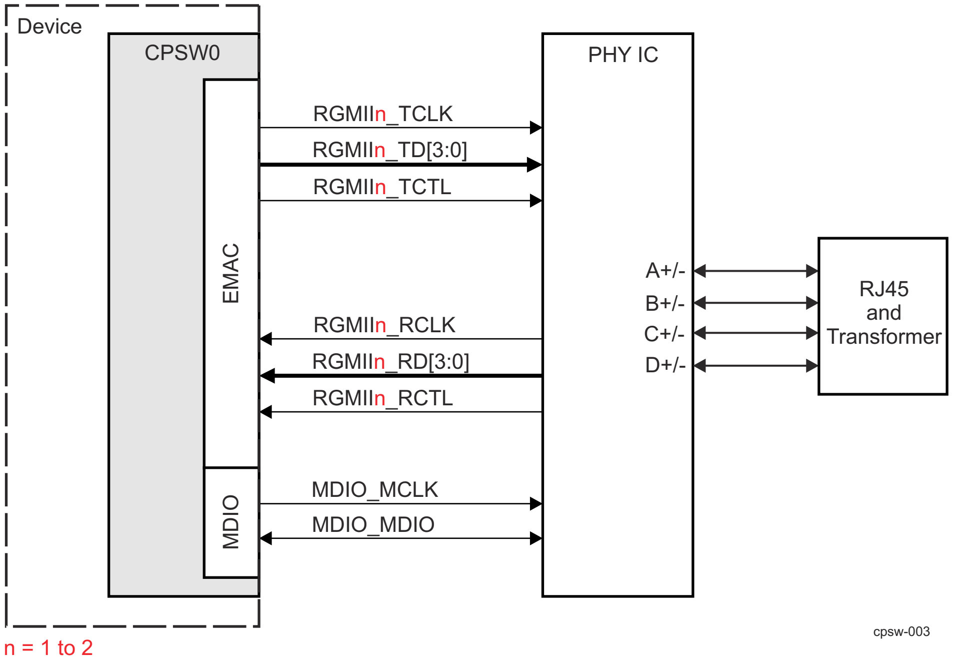


Figure 12-148. RGMII Interface Typical Application

Table 12-186. RGMII I/O Description

Signal[2]	Device Pin(s)	I/O[1]	Description
RGMIIn_TD[3:0]	RGMIIn_TD[3:0]	O	The transmit data pins are a collection of 4 bits of data. TD0 is the least-significant bit (LSB). The signals are valid only when RGMIIn_TCTL is asserted.
RGMIIn_TCTL	RGMIIn_TX_CTL	O	Transmit Control/enable. The transmit enable signal indicates that the TD pins are generating data for use by the PHY.
RGMIIn_TCLK	RGMIIn_TXC	O	The transmit reference clock. The clock is 2.5 MHz at 10 Mbps operation, 25 MHz at 100 Mbps operation, and 125 MHz at 1000 Mbps of operation.
RGMIIn_RD[3:0]	RGMIIn_RD[3:0]	I	The receive data pins are a collection of 4 bits of data. RD0 is the least-significant bit (LSB). The signals are valid only when RGMIIn_RX_CTL is asserted
RGMIIn_RCTL	RGMIIn_RX_CTL	I	The receive data valid/control signal indicates that the RD pins are nibble data for use by the EMAC.
RGMIIn_RCLK	RGMIIn_RXC	I	The receive clock is a continuous clock that provides the timing reference for receive operations. The clock is generated by the PHY and is 2.5 MHz at 10 Mbps operation, 25 MHz at 100 Mbps operation, 125 MHz at 1000 Mbps of operation.
MDIO_MCLK	MDIO0_MDC	O	Management data clock (MDIO_MCLK). The MDIO data clock is sourced by the MDIO module on the system. It is used to synchronize MDIO data access operations done on the MDIO0_MDIO pin.
MDIO_MDIO	MDIO0_MDIO	I/O	The MDIO0_MDIO pin drives PHY management data into and out of the PHY by way of an access frame consisting of start of frame, read/write indication, PHY address, register address, and data bit cycles. The MDIO0_MDIO pin acts as an output for all but the data bit cycles at which time it is an input for read operations.

(1) I = Input; O = Output
(2) n 1 to 2

Note

The Control Module registers assign the specific function to the device pads. For more information on Control Module settings, see *Pad Configuration Registers* in *Control Module (CTRL_MMR)* and the device-specific Datasheet.

12.3.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.3.1.4 CPSW0 Functional Description

The three-port switch Ethernet subsystem module (CPSW) is compliant to the IEEE Std 802.3 Specification. CPSW top level functional block diagram is shown in *CPSW Top Level Block Diagram*.

12.3.1.4.1 Functional Block Diagram

The three-port Ethernet subsystem consists of:

- CPSW_3G
- One RGMIIn (where n = 1 to 2) interface module
- One RMIIn (where n = 1 to 2) interface module
- One Host Port 0 CPPI Packet Streaming Interface
- CPSW subsystem control registers (REG)
- One MDIO interface module
- One Interrupt Controller module

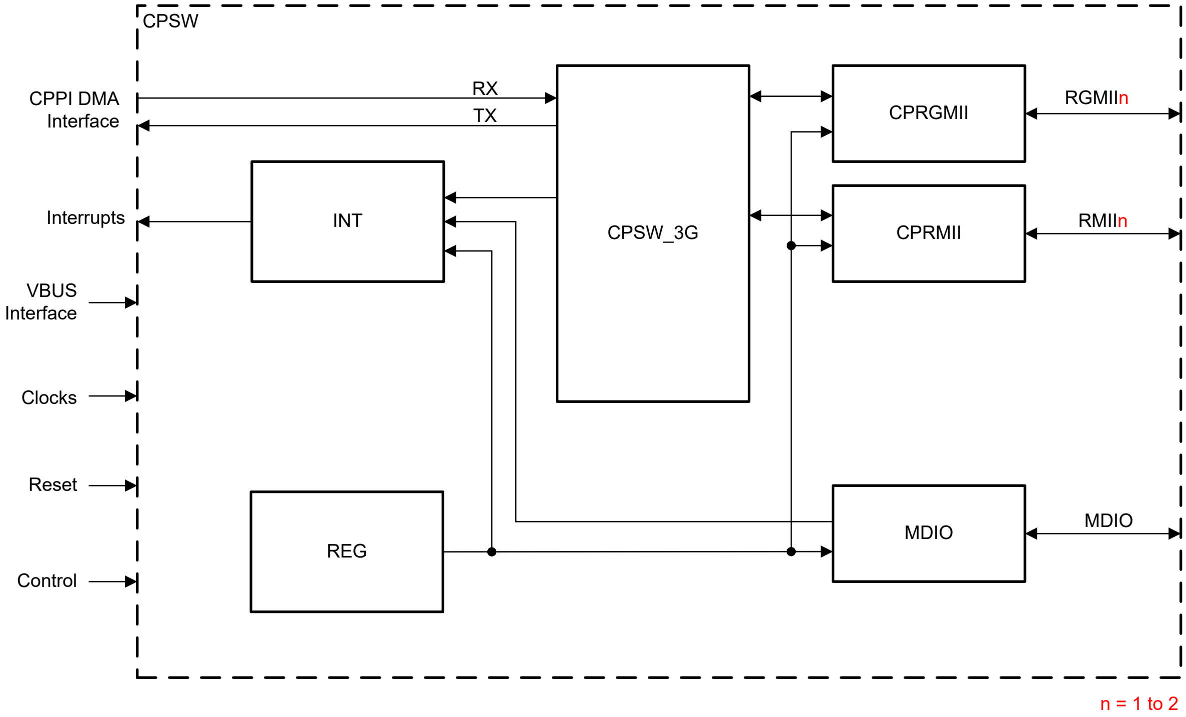


Figure 12-149. CPSW Top Level Block Diagram

12.3.1.4.2 CPSW Ports

The Ethernet Subsystem has three ports. Port 0 is the Host port (internal to the Subsystem). Port 1 and 2 are the external ports connected to RGMII and RMII interfaces as per the interface selected.

Naming conventions followed in this chapter:

- Port0 is referred to the CPPI Host Port
- Port1 and 2 are referred to the interfaces RGMII/RMII

12.3.1.4.2.1 Interface Mode Selection

The three-port switch (CPSW) Ethernet Subsystem has one 10/100/1000 Ethernet port with selectable RMII and RGMII interfaces.

The interface modes for all 2 Ethernet ports are selected by configuring the Ethernet interface mode selection bitfield (PORT_MODE_SEL) in the ENET1_CTRL and ENET2_CTRL registers.

See the device-specific Datasheet for configuring the pin mux mode as per the interface selected.

12.3.1.4.3 Clocking

12.3.1.4.3.1 Subsystem Clocking

CPSW clocking summary is shown in *CPSW Integration*.

12.3.1.4.3.2 Interface Clocking

Data is transmitted and received with respect to the reference clocks of the interface pins.

12.3.1.4.3.2.1 RGMII Interface Clocking

RGMII_RXC, RGMII_TXC frequencies are:

- 2.5 MHz at 10 Mbps
- 25 MHz at 100 Mbps
- 125 MHz at 1000 Mbps

12.3.1.4.3.2.2 RMII Interface Clocking

RMII interface clock RMII_50MHZ_CLK frequency is:

- 50 MHz at 10 Mbps
- 50 MHz at 100 Mbps

For more details on RMII clocking, please see *CPSW0 Integration*

CLKOUT_CTRL bits are used to enable and select the clock source for CLKOUT device pin.

12.3.1.4.3.2.3 MDIO Clocking

The MDIO clock is based on a divide-down of the interface (CPPI_ICLK) clock. The application software or driver must control the divide-down value.

See the CPSW3_MDIO_CONTROL_REG register for configuring the Clock Divider ([15-0]CLKDIV) value.

12.3.1.4.4 Software IDLE

The submodule software idle register bits enable CPSW operation to be completely or partially suspended by software control. There are two CPSW submodules that contain software idle register bits. Each of the two submodules may be individually commanded to enter the idle state. The idle state is entered at packet boundaries, and no further packet operations will occur on an idled submodule until the idle command is removed. The CPSW module enters the idle state when all two submodules are commanded to enter and have entered the idle state. Idle status is determined by reading or polling the two submodule idle bits. The CPSW_3G is in the idle state when all two submodules are in the idle state. The CPSW3_CPSW_NU_SOFT_IDLE_REG[0] SOFT_IDLE bit may be set if desired after the submodules are in the idle state. The SOFT_IDLE bit causes packets to not be transferred from one FIFO to another FIFO internal to the switch.

12.3.1.4.5 Interrupt Functionality

CPSW Ethernet Subsystem has six interrupt outputs:

- Cn_FH_PEND_INTR - FHost (from host to Ethernet) level interrupt
- Cn_TH_PEND_INTR - THost (from Ethernet to host) level interrupt
- Cn_TH_THRESH_PEND_INTR - THost (from Ethernet to host) non-paced level interrupt
- Cn_MISC_PEND_INTR - Miscellaneous non-paced pending interrupt
- ECC_SEC_PEND_INTR: ECC SEC pending interrupt - from CPSW ECC module. This interrupt is also included in the C0_MISC_PEND_INTR if enabled or can be used separately if desired.
- ECC_DED_PEND_INTR: ECC DED pending interrupt - from CPSW ECC module. This interrupt is also included in the C0_MISC_PEND_INTR if enabled or can be used separately.

Note

n = 0 to $num_cores-1

12.3.1.4.5.1 EVNT_PEND Interrupt

See Section 12.3.1.4.7, *Common Platform Time Sync (CPTS)* for more details on this interrupt.

12.3.1.4.5.2 Statistics Interrupt (STAT_PEND0)

The statistics level interrupt (STAT_PEND0) will be asserted, if enabled when any statistics value is greater than or equal to 8000 0000h. The statistics interrupt is cleared by writing to decrement any statistics values greater than 8000 0000h (such that their new values are less than 8000 0000h). The statistics are mapped into internal memory space and are 32-bits wide. The raw and masked statistics interrupt status may be read by reading the CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG and CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG registers, respectively.

The statistics interrupt is enabled by setting to 1h the TS_PEND_EN bit in the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG register.

12.3.1.4.5.3 ECC DED Level Interrupt (ECC_DED_INT)

Level interrupt (ECC_DED_INT) indicating an ECC double error has been detected.

12.3.1.4.5.4 ECC SEC Level Interrupt (ECC_SEC_INT)

Level interrupt (ECC_SEC_INT) indicating an ECC single error has been detected and corrected.

12.3.1.4.5.5 MDIO Interrupts

Normal Mode: (CPSW3_MDIO_POLL_REG[30] STATECHANGEMODE = 0h)

MDIO_LINKINT event is set if there is a change in the link state of the PHY corresponding to the address in the PHYADR_MON field of the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k register and the corresponding LINKINT_ENABLE bit is set. The MDIO_LINKINT event is also captured in the MDIO CPSW3_MDIO_LINK_INT_MASKED_REG register. When the GO bit in the CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register transitions from 1 to 0, indicating the completion of a user access, and the corresponding USERINTMASKSET bit in the CPSW3_MDIO_USER_INT_MASK_SET_REG register is set, the MDIO_USERINT signal is asserted. The MDIO_USERINT event is also captured in the CPSW3_MDIO_USER_INT_MASKED_REG register.

State Change Mode: (CPSW3_MDIO_POLL_REG[30] STATECHANGEMODE = 1h)

In State Change Mode, the MDIO will assert MDIO_LINKINT[0] when any bit in the MDIO CPSW3_MDIO_ALIVE_REG or CPSW3_MDIO_LINK_REG registers changes due to MDIO operations. The MDIO_LINKINT event is also captured in the CPSW3_MDIO_LINK_INT_MASKED_REG register. MDIO_LINKINT[1] output is unused in State Change Mode. The CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k registers are unused in state change mode.

Manual Mode: (CPSW3_MDIO_POLL_REG[31] MANUALMODE = 1h)

Manual Mode allows software to directly control the MDIO serial clock output (CPSW3_MDIO_MANUAL_IF_REG[2] MDIO_MDCLK_O) and the MDIO serial data output enable (CPSW3_MDIO_MANUAL_IF_REG[1] MDIO_OE). Manual Interface Mode is enabled when the MANUALMODE bit is set in the CPSW3_MDIO_POLL_REG register. Manual Mode is intended to be used by software for slow speed general purpose IO operations and not for MDIO PHY operations.

12.3.1.4.6 CPSW_3G

The CPSW_3G RMII/ RGMII interface is compliant to the IEEE Std 802.3 Specification.

The CPSW_3G contains two Ethernet port interfaces (Ethernet port 1 and 2), one CPPI packet streaming interface host port (port 0), Common Platform Time Sync (CPTS), ALE Engine and Statistics (STATS). A top-level block diagram of the CPSW_3G is shown in Figure 12-150.

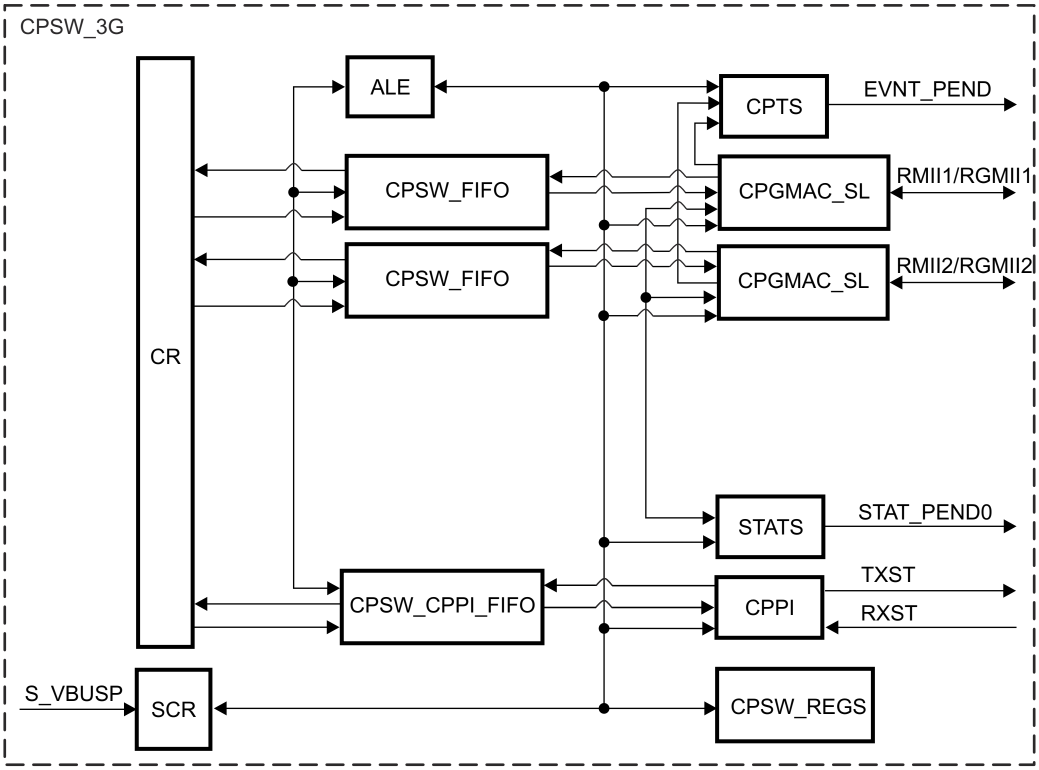


Figure 12-150. CPSW_3G Block Diagram

12.3.1.4.6.1 Address Lookup Engine (ALE)

The Address Lookup Engine (ALE) is a sub-block of the CPSW Switch and it processes all received packets and determines to which port(s) the packet should be forwarded. The ALE uses the incoming packet received port number, destination address, source address, length/type, and VLAN information to determine how the packet should be forwarded. The ALE outputs the port mask to the switch fabric that indicates the port(s) the packet should be forwarded to. The ALE is enabled when the ENABLE_ALE bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register is set. All packets are dropped when the ENABLE bit is cleared to 0.

12.3.1.4.6.1.1 Error Handling

In normal operation, the Ethernet port modules are configured to issue an abort, instead of an end of packet, at the end of a packet that contains an error (runt, frag, oversize, jabber, crc, alignment, code etc.) or at the end of a MAC control packet. However, when the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG configuration bit(s) RX_CEF_EN, RX_CSF_EN, or RX_CMF_EN are set, error frames, short frames or MAC control frames have a normal end of packet instead of an abort at the end of the packet. When the ALE receives a packet that contains errors (due to a set header error bit), or a MAC control frame and does not receive an abort, the packet will be forwarded only to the host port (port 0). Packets with errors that are forwarded to the host have no VLAN untagging or drop due to rate limiting. No ALE learning occurs on packets with errors or mac control frames. Learning is based on source address and lookup is based on destination address. Directed packets from the host are not learned, updated, or touched.

12.3.1.4.6.1.2 Bypass Operations

The ALE may be configured to operate in bypass mode by setting the ENABLE_BYPASS bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register. When in bypass mode, all Ethernet port received packets are forwarded only to the host port (port 0). In bypass mode, the ALE processes host port transmit packets the same as in normal mode. In general, packets would be directed by the host in bypass mode.

12.3.1.4.6.1.3 OUI Deny or Accept

The ALE may be configured to operate in OUI deny mode by setting the ENABLE_OUI_DENY bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register. When in OUI deny mode, a packet with a non-matching OUI source address will be dropped unless the destination address matches a multicast table entry with the SUPER bit set. When ENABLE_OUI_DENY bit is cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory address table entry. Broadcast packets will be dropped unless the broadcast address is entered into the table with the SUPER bit set. Unicast packets will be dropped unless the unicast address is in the table with BLOCK and SECURE both set (supervisory unicast packet).

12.3.1.4.6.1.4 Statistics Counting

ALE sends many statistics along with the frame routing so the CPSW can count them on a per port basis. There are many reasons to drop frames the below drop events are individually counted in CPSW per port statistics counters.

Table 12-187. Learned Address Control Bits

Abbreviation	Description
vddc	Dual VLAN or Double VLAN drop counter.
frdc	IPv4 fragmented drop counter.
nldc	IPv4 Protocol or IPv6 Next Header drops due to next header limit drop counter.
etdc	Ether Type field is <= 1500 and the frame size is too small drop counter.
smdc	The Source Address has bit 40 set drop counter.
badc	The Source or Destination Address blocked drop counter.
svdc	The Source Address is locked to a different port drop counter.
des	The Source and Destination are equal and the Source Address is not in the table drop counter.
adc	The Source Address is not in the table in authentication mode drop counter.
vicdc	The VLAN ingress check failed drop counter.
rldc	Rate Limit Drop Counter.
over	Lookup Overflow, the rate of the ALE clock is not sufficient to handle the incoming frame rate (Should never happen).
drop	Packet is dropped and not forwarded.

12.3.1.4.6.1.5 Automotive Security Features

The ALE has many automotive security features that most enterprise switches do not require.

- VLANs can be configured to not allow fragmented IPv4 frames. That is a VLAN can be configured to not allow fragmented IPv4 traffic.
- VLANs can be configured to only allow up to four different IPv4 Protocols or IPv6. Next Header values, for example a VLAN can be configured to only allow TCP traffic in both IPv4 and IPv6 packets.
- Drop invalid Source Addresses, that is drop Source Addresses with bit 40 set (Multicast/Broadcast indicator on Destination Addresses)
- IEEE802.3 Length Check, drop frames that the IEEE802.3 Length is not contained within the frame. (Ether Types 0-1500)
- Any Source Address can be secured to a port dropping any attempts from other ports to masquerade as a service.
- Any source or destination address can be blocked.
- Per Port or Per VLAN ingress checking, dropping traffic from non-member ports.

- Classification, Policing on L2 and L3 information.

12.3.1.4.6.1.6 CPSW Switching Solutions

The host port can operate in many different modes as well depending on the functionality of the host. It is important to understand the modes and configure them properly.

The ALE Table is designed to maximize the modes without compromise of the system functionality as well.

12.3.1.4.6.1.6.1 Basics of 3-port Switch Type

The 3-port switch has a host port, and that port can operate in two fundamental modes. Bridge mode allows the host to extent the switched domain to another network like Wi-Fi or another multi-port switch. In this case the host must be able to see unknown unicast addresses so they can be broadcast to the other network. In Port mode the host need not see any unknown unicast traffic. The CPSW3_CPSW_NU_ALE_ALE_CONTROL[8] EN_HOST_UNI_FLOOD bit determines the host mode for unknown unicast traffic. This bit should only be set if the user is bridging two or more networks together.

The 3-port switch can operate like a two-port switch using the ALE table just for the host info, the only adder is now other VLANs need to be supported for transit traffic between the external ports. This can easily be done using the default VLAN rules so no ALE table entries are used.

The 3-port switch can also operate in a fully authenticated environment where all network nodes are registered via the 802.1x based protocols. In this case the ALE table is filled with network node addresses that have been authenticated

12.3.1.4.6.1.7 VLAN Routing and OAM Operations

12.3.1.4.6.1.7.1 InterVLAN Routing

The CPSW module supports wire rate InterVLAN routing for a small number of routes, that is the host will setup an ALE classifier with and associated egress operation that will cause the CPSW to perform particular egress operations. The ALE can optionally check time to live validity as well.

The ALE uses the classifier along with an egress opcode, destination port mask and TTL check field to tell the CPSW to manipulate the packet on the egress. The CPSW will use the opcode along with a per port operation table to process the packet. By setting up the CPSW egress operation table you can replace the DA, SA and VLAN along with optionally updating the time to live IP header field. This allows the CPSW to perform the routing function for a small set of routes without getting the local host/CPU involved.

The Egress opcode will only be use for a classifier match and the packet would normally be sent only to the host. That is the host would have routed the packet but the CPSW has been configured to do the work instead. In the event that the time-to-live check feature is enabled and the time-to-live is either 0 or 1, the packet will not get the egress opcode and instead be sent to the host as if the route is not setup. This allows the host to deal with invalid TTL fields.

12.3.1.4.6.1.7.2 OAM Operations

The ALE supports OAM loopback on ports so that a remote link can be tested. That is a port placed in OAM loopback will echo packets received on a port back to the port with an egress op of 0xFF which will swap the SA and DA on egress in the CPSW.

Any supervisory packet will not be affected, so the spanning tree and other bridging functions are not affected.

Packets will only be echoed if the port is in OAM loopback mode, the received packet in not a supervisor packet. The port is in a forwarding state and the packet received DA!=SA and there are no errors in the packet.

When a port is in OAM loopback the port will not egress traffic from other ports, no address for loop backed traffic will be learned if enabled. Any packet received on the OAM loopback port with an error will be process as if the port is not in OAM. That is if the host has enabled copy errored frames the errored frames will be sent to the host instead.

12.3.1.4.6.1.8 Supervisory packets

Multicast supervisory packets are designated by the SUPER bit in the table entry. Unicast supervisory packets are indicated when BLOCK and SECURE are both set. Supervisory packets are not dropped due to rate limiting, OUI, or VLAN processing. The purpose of supervisory packets is to allow packets that would be otherwise blocked to be forwaded for special purposes.

12.3.1.4.6.1.9 Address Table Entry

The ALE table contains multiple table entry types. Each table entry represents a free entry, an address, a VLAN, an address/VLAN pair, or an OUI address. Software should ensure that there are not double address entries in the table. The double entry used would be indeterminate. Reserved table bits must be written with zeroes.

Source Address learning occurs for packets with a unicast, multicast or broadcast destination address and a unicast or multicast (including broadcast) source address. Multicast source addresses have the group bit (bit 40) cleared before ALE processing begins, changing the multicast source address to a unicast source address. A multicast address of all ones is the broadcast address which may be added to the table. A learned unicast source address is added to the table with the following control bits:

Table 12-188. Learned Address Control Bits

Bit(s)	Value
Ageable	1
Touch	1
BLOCK	0
SECURE	0

If a received packet has a source address that is equal to the destination address then the following occurs:

- The address is learned if the address is not found in the table.
- The address is updated if the address is found.
- The packet is dropped.

Table Entry Type

00 - Free Entry

01 - Address Entry : unicast or multicast determined by destination **address bit 40.**

10 - VLAN entry

11 - VLAN Address Entry : unicast or multicast determined by **address bit 40.**

12.3.1.4.6.1.9.1 Multicast Address Table Entry

Table 12-189. Multicast Address Table Entry Bit Values

70:68	67:66	65	64	63:62	61:60	59:48	47:0
Reserved	PORT_MASK	SUPER	Reserved	MCAST_FWD_STATE	ENTRY_TYPE (01)	Reserved	MULTICAST_ADDRESS

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Port Mask(1:0) (PORT_MASK)

This 2-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Multicast Forward State (MCAST_FWD_STATE)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state in order to forward the packet. If the transmit PORT_MASK has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

00 - Forwarding

01 - Blocking/Forwarding/Learning

10 - Forwarding/Learning

11 - Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.3.1.4.6.1.9.2 OUI Unicast Address Table Entry

Table 12-190. OUI Unicast Address Table Entry Bit Values

70:64	63:62	61:60	59:48	47:24	23:0
Reserved	UNICAST_TYPE (10)	ENTRY_TYPE (01)	Reserved	UNICAST_OUI	Reserved

Unicast Type (UNICAST_TYPE)

This field indicates the type of unicast address the table entry contains.

00 - Unicast address that is not ageable.

01 - Ageable unicast address that has not been touched.

10 - OUI address - lower 24-bits are don't cares (not ageable).

11 - Ageable unicast address that has been touched.

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (UNICAST_OUI)

For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup.

12.3.1.4.6.1.9.3 Unicast Address Table Entry (Bit 40 == 0)

Table 12-191. Unicast Address Table Entry Bit Values

70:69	68	67:66	65	64	63	62	61:60	59:48	47:0
RESERVED	TRUNK	PORT_NUMBER	BLOCK	SECURE	TOUCH	AGEABLE	ENTRY_TYPE (3h)	RESERVED	UNICAST_ADDRESS

Trunk Indicator (TRUNK)

0h = The port bits in the entry are the port number

1h = The port bits in the entry are the trunk numbe

Port Number (PORT_NUMBER)

This field indicates the port number (not port mask) that the packet with a unicast destination address may be forwarded to. Packets with unicast destination addresses are forwarded only to a single port (but not the receiving port).]

Block (BLOCK)

The block bit indicates that a packet with a matching source or destination address should be dropped (block the address).

0h = Address is not blocked.

1h = Drop a packet with a matching source or destination address (secure must be zero)

If block and secure are both set, then they no longer mean block and secure. When both are set, the block and secure bits indicate that the packet is a unicast supervisory (super) packet and they determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state.

Secure (SECURE)

This bit indicates that a packet with a matching source address should be dropped if the received port number is not equal to the table entry PORT_NUMBER.

0h = Received port number is a don't care.

1h = Drop the packet if the received port is not the secure port for the source address and do not update the address (block must be zero)

Touch Indicator (TOUCH)

Only valid when AGEABLE it a 1h.

0h = Ageable unicast address has not been touched

1h = Ageable unicast address that has been touched

Ageable (AGEABLE)

This bit indicates that the address is ageable.

0h = Unicast address that is not ageable

1h = Unicast address that is ageable

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (UNICAST_ADDRESS)

This is the 48-bit packet MAC address. All 48-bits are used in the lookup.

12.3.1.4.6.1.9.4 Multicast Address Table Entry (Bit 40==1)

Table 12-192. Multicast Address Table Entry Bit Values

70:69	68:66	65	64	63:62	61:60	59:48	47:0
RESERVED	PORT_MASK	SUPER	IGNMBITS	FWDSTLVL	ENTRY_TYPE (1h)	RESERVED	MULTICAST_ADDRESS

Port Mask(2:0) (PORT_MASK)

This 3-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Forward State Level (FWDSTLVL)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s).

A transmit port must be in the Forwarding state in order to forward the packet. If the transmit port_mask has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

0h = Forwarding

1h = Blocking/Forwarding/Learning

2h = Forwarding/Learning

3h = Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

01: Address entry. Unicast or multicast determined by address bit 40.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.3.1.4.6.1.9.5 VLAN/Unicast Address Table Entry (Bit 40 == 0)

Table 12-193. Unicast Address Table Entry Bit Values

70:69	68	67:66	65	64	63	62	61:60	59:48	47:0
RESERVED	TRUNK	PORT_NUMBER	BLOCK	SECURE	TOUCH	AGEABLE	ENTRY_TYPE (3h)	VLAN_ID	UNICAST_ADDRESS

Trunk Indicator (TRUNK)

0h = The port bits in the entry are the port number

1h = The port bits in the entry are the trunk number

Port Number (PORT_NUMBER)

This field indicates the port number (not port mask) that the packet with a unicast destination address may be forwarded to. Packets with unicast destination addresses are forwarded only to a single port (but not the receiving port).]

Block (BLOCK)

The block bit indicates that a packet with a matching source or destination address should be dropped (block the address).

0h = Address is not blocked.

1h = Drop a packet with a matching source or destination address (secure must be zero)

If block and secure are both set, then they no longer mean block and secure. When both are set, the block and secure bits indicate that the packet is a unicast supervisory (super) packet and they determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/ Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state.

Secure (SECURE)

This bit indicates that a packet with a matching source address should be dropped if the received port number is not equal to the table entry PORT_NUMBER.

0h = Received port number is a don't care.

1h = Drop the packet if the received port is not the secure port for the source address and do not update the address (block must be zero)

Touch Indicator (TOUCH)

Only valid when AGEABLE is a 1h.

0h = Ageable unicast address has not been touched

1h = Ageable unicast address that has been touched

Ageable (AGEABLE)

This bit indicates that the address is ageable.

0h = Unicast address that is not ageable

1h = Unicast address that is ageable

Table Entry Type (ENTRY_TYPE)

Address entry. Unicast or multicast determined by address bit 40.

3h: VLAN address entry. Unicast or multicast determined by address bit 40.

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

Packet Address (UNICAST_ADDRESS)

This is the 48-bit packet MAC address. All 48-bits are used in the lookup.

12.3.1.4.6.1.9.6 VLAN/Multicast Address Table Entry (Bit 40==1)

Table 12-194. VLAN/Multicast Address Table Entry Bit Values

70:69	68:66	65	64	63:62	61:60	59:48	47:0
RESERVED	PORT_MASK	SUPER	IGNMBITS	FWDSTLVL	ENTRY_TYPE (11)	VLAN_ID	MULTICAST_ADDRESS

Port Mask(2:0) (PORT_MASK)

This 3-bit field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).

Supervisory Packet (SUPER)

When set, this field indicates that the packet with a matching multicast destination address is a supervisory packet.

0: Non-supervisory packet

1: Supervisory packet

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Forward State Level (FWDSTLVL)

Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s).

A transmit port must be in the Forwarding state in order to forward the packet. If the transmit port_mask has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision.

0h = Forwarding

1h = Blocking/Forwarding/Learning

2h = Forwarding/Learning

3h = Forwarding

The forward state test returns a true value if both the RX and TX ports are in the required state.

Table Entry Type (ENTRY_TYPE)

Address entry type. Unicast or multicast determined by address bit 40.

11: VLAN address entry. Unicast or multicast determined by address bit 40.

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

Packet Address (MULTICAST_ADDRESS)

This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.

12.3.1.4.6.1.9.7 Inner VLAN Table Entry

Table 12-195. Inner VLAN Table Entry

70:69	68:66	65	64:62	61:60	59:48	47	46:39	38:36
RESERVED	NO_LEARN_MASK	VLAN_FORCE_INGRESS_CHECK	0h	ENTRY_TYPE (1h)	VLAN_ID	NOFRAG	RESERVED	REG_MCAST_FLOOD_INDEX

35:27	26:24	23	22:15	14:12	11:3	2:0
RESERVED	FORCE_UNTAGGED_EGRESS	LMTNXTHDR	RESERVED	UREGMSK	RESERVED	VLAN_MEMBER_LIST

No Learn Mask (NO_LEARN_MASK)

When a bit is set in this mask, a packet with an unknown source address received on the associated port will not be learned (i.e. When a VLAN packet is received and the source address is not in the table, the source address will not be added to the table).

VLAN Force Ingress Check (VLAN_FORCE_INGRESS_CHECK)

If the receive port is not a member of this VLAN then the packet is dropped. This is similar to the Iy_REG_Py_VID_INGRESS_CHECK bit in the CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register except this check is for this VLAN only (not all VLANs).

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

(NOFRAG)

VLAN No IPv4 Fragmented frames Control - Causes IPv4 fragmented IP frames to be dropped.

Registered Multicast Flood Index (REG_MCAST_FLOOD_INDEX)

This field indicates which port(s) are the registered multicast flood mask.

Force Untagged Packet Egress (FORCE_UNTAGGED_EGRESS)

This field causes the packet VLAN tag to be removed on egress for the specified port(s) (except on port 0).

VLAN Limit Next Header Control (LMTNXTHDR)

This bit causes frames to be dropped if the Protocol/Nxt Header does not match the CPSW3_CPSW_NU_ALE_ALE_NXT_HDR register values.

VLAN Unregister Multicast Mask (UREGMSK)

This field indicates which port(s) are the unregistered multicast flood mask.

VLAN Member List (VLAN_MEMBER_LIST)

This field indicates which port(s) are members of the associated VLAN. One bit per port.

12.3.1.4.6.1.9.8 Outer VLAN Table Entry

Table 12-196. Outer VLAN Table Entry

70:69	68:66	65	64:62	61:60	59:48	47	46:39	38:36
RESERVED	NO_LEARN_MASK	VLAN_FORCE_INGRESS_CHECK	2h	ENTRY_TYPE (2h)	VLAN_ID	NOFRAG	RESERVED	REG_MCAST_FLOOD_INDEX

35:27	26:24	23	22:15	14:12	11:3	2:0
RESERVED	FORCE_UNTAGGED_EGRESS	LMTNXTHDR	RESERVED	UREGMSK	RESERVED	VLAN_MEMBER_LIST

No Learn Mask (NO_LEARN_MASK)

When a bit is set in this mask, a packet with an unknown source address received on the associated port will not be learned (i.e. When a VLAN packet is received and the source address is not in the table, the source address will not be added to the table).

VLAN Force Ingress Check (VLAN_FORCE_INGRESS_CHECK)

If the receive port is not a member of this VLAN then the packet is dropped. This is similar to the Iy_REG_Py_VID_INGRESS_CHECK bit in the CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register except this check is for this VLAN only (not all VLANs).

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

VLAN ID (VLAN_ID)

The unique identifier for VLAN identification. This is the 12-bit VLAN ID.

(NOFRAG)

VLAN No IPv4 Fragmented frames Control - Causes IPv4 fragmented IP frames to be dropped.

Registered Multicast Flood Index (REG_MCAST_FLOOD_INDEX)

Index into CPSW_ALE_MSK_MUX0 to CPSW_Ix_ALE_MSK_MUXx register array that is used to create the registered multicast flood mask.

Force Untagged Packet Egress (FORCE_UNTAGGED_EGRESS)

This field causes the packet VLAN tag to be removed on egress for the specified port(s) (except on port 0).

VLAN Limit Next Header Control (LMTNXTHDR)

This bit causes frames to be dropped if the Protocol/Nxt Header does not match the CPSW3_CPSW_NU_ALE_ALE_NXT_HDR register values.

VLAN Unregister Multicast Mask (UREGMSK)

This field indicates which port(s) are the unregistered multicast flood mask.

VLAN Member List (VLAN_MEMBER_LIST)

This field indicates which port(s) are members of the associated VLAN. One bit per port.

12.3.1.4.6.1.9.9 EtherType Table Entry

Table 12-197. EtherType Table Entry

70:65	64:62	61:60	59:16	15:0
RESERVED	4h	ENTRY_TYPE (2h)	RESERVED	ETHERTYPE

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

Ether Type (ETHERTYPE)

16-bits Ether Type field.

12.3.1.4.6.1.9.10 IPv4 Table Entry

Table 12-198. IPv4 Table Entry

70	69:65	64:62	61:60	59:32	31:0
RESERVED	IGNMBITS	6h	ENTRY_TYPE (2h)	RESERVED	IPV4ADR

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv4 Address (IPV4ADR)

32-bit IPv4 Address. Any ignored bits must be zero value in the table entry.

12.3.1.4.6.1.9.11 IPv6 Table Entry High

Table 12-199. IPv6 Table Entry High

70:64	63	62	61:60	59:0
IGNMBITS	RESERVED	(1h)	ENTRY_TYPE (2h)	IPV6ADR[127:68]

Ignore Multicast Bits (IGNMBITS)

Indication that the Multicast Address has ignored bits.

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv6 Address - upper 64 bits (IPV6ADR[127:68])

This address is plit into three fields in the IPv6 High and IPv6 Low table entry. Any ignored bits must be zero in the table entry(s).

12.3.1.4.6.1.9.12 IPv6 Table Entry Low

Table 12-200. IPv6 Table Entry Low

70:63	62	61:60	59:0
IPV6ADR[67:60]	1h	ENTRY_TYPE (2h)	IPV6ADR[59:0]

Table Entry Type (ENTRY_TYPE)

2h: VLAN entry

IPv6 Address - upper 8 bits (IPV6ADR[67:60])

IPv6 Address - upper 60 bits (IPV6ADR[59:0])

This address is plit into three fields in the IPv6 High and IPv6 Low table entry. Any ignored bits must be zero in the table entry(s).

Note: IPV6 table address entries operate differently than all other table entry types. IPV6 table entries have a high entry concatenated with a low entry. The high entry must have an entry_pointer value of the low entry_pointer plus 0x40. Bit six of the entry_pointer must be set for the high entry and must be zero for the low entry.

12.3.1.4.6.1.10 Multicast Address

Multicast addresses are addresses with bit 40 set. Only destination addresses can be Multicast addresses. The group bit (bit 40) of the source address is reserved in the IEEE tandard.

A multicast address of all ones is the broadcast address which can be added to the lookup table if forwading of broadcast packets need be modified.

12.3.1.4.6.1.10.1 Multicast Ranges

Added IgnMbits to indicate at least one bit of the multicast address is ignored. Up to 10 bits of the multicast address can be ignored to provide the ability to create multiple multicast address ranges.

```
if ((IgnMbits)&(MultiCastAddress[0] ==0x000)) { MultiCastAddress[0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[1:0]==0x001)) { MultiCastAddress[1:0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[2:0]==0x003)) { MultiCastAddress[2:0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[3:0]==0x007)) { MultiCastAddress[3:0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[4:0]==0x00F)) { MultiCastAddress[4:0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[5:0]==0x01F)) { MultiCastAddress[5:0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[6:0]==0x03F)) { MultiCastAddress[6:0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[7:0]==0x07F)) { MultiCastAddress[7:0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[8:0]==0x0FF)) { MultiCastAddress[8:0] is ignored in compare}
if ((IgnMbits)&(MultiCastAddress[9:0]==0x1FF)) { MultiCastAddress[9:0] is ignored in compare}
```

Below is 'C' code to modify ALE MultiCastAddress and IgnMbits when iNumOfBitsToIgnore is greater than zero. Where fGenMask(iOffset,iBitsToMask) creates a Mask for the value provided. For example fGenMast(0,5) will return 0x1F.

```
if(iNumOfBitsToIgnore)
{
int iIgnClrMsk,iIgnSetMsk;
iIgnClrMsk=fGenMask(0, iNumOfBitsToIgnore);
iIgnSetMsk=fGenMask(0, iNumOfBitsToIgnore -1);
MultiCastAddress &= ~iIgnClrMsk;
MultiCastAddress |= iIgnSetMsk;
IgnMbits = 1;
}
```

else

{

IgnMbits = 0;

}

Multicast Addresses or Ranges can overlap, in the event of an overlap; the higher ALE index will be used.

12.3.1.4.6.1.11 Aging and Auto Aging

The ALE supports software control or automatic aging of agable addresses.

Any time an agable address is seen as a source address entering from a port the source address entry will be marked as touched.

If the aging timer expires or the software sets the [29] AGE_OUT_NOW bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL, the aging process will be started.

The aging process will read each ALE entry and for all entries that are an address with or without VLAN that is also agable, the touch check process will be done.

The touch check process will test the TOUCH bit and if clear, the entry will be marked as free, else the TOUCH bit will be cleared.

What this means is that if the aging interval was programmed as one second, any unused entry could stay in the ALE table for 1.000001 to 1.999999 seconds

12.3.1.4.6.1.12 ALE Policing and Classification

The ALE has a number of configurable classifier engines (policers) that can be used for classification. Classification is a subset of the policing function and uses a policer without the color marking or rate limiting functions. A policer is a hardware engine that is used for policing. The POLCNTDIV8 field in the CPSW3_CPSW_NU_ALE_ALE_STATUS register indicates the number of policers available to be used for classification. Each policer can be enabled to match on one or more of any of the below packet fields for classification. All but Port and Priority are index references to the ALE table entries.

- Port Number
- Priority extracted from VLAN, mapped from DSCP if enabled, or Default Port Priority
- Organization Network Unique identifier - ONU
- Destination Address - DA
- Source Address - SA
- Outer VLANID -S-VLANID
- Inner VLANID -C-VLANID
- Ether Type
- IP Source Address - IPSA with full CIDR masking for IPv4 and IPv6
- IP Destination Address - IPSA with full CIDR masking for IPv4 and IPv6
- Support Host Thread/Flow ID mapping based on any packet classification above

12.3.1.4.6.1.12.1 ALE Policing

The policing function on each policer engine is implemented as dual-counter three-color marking engine as described in the IETF RFC2698. The first counter is the Committed Information Rate (CIR) counter and the second counter is the Peak Information Rate (PIR) counter. The policing function can use either or both counters. Based on the counter values the packet color is determined. The color is used to determine whether the packet is dropped or forwarded. The ALE has a local feature that can drop packets regardless of queue state.

The policing rates are determined by the below equations:

CIR policing rate in Mbit/s = ((ALE frequency in Mhz) * CPSW3_CPSW_NU_ALE_POLICECFG7[31-0] CIR_IDLE_INC_VAL) / 32768

PIR policing rate in Mbit/s = ((ALE frequency in Mhz) * CPSW3_CPSW_NU_ALE_POLICECFG6[31-0] PIR_IDLE_INC_VAL) / 32768

Each policer has 10 different match operations (see Section 12.3.1.4.6.1.12). Since multiple policing entries can be hit on a single packet this provides the ability to create precise traffic stream control.

Packets are colored at ALE lookup time. Packets can be colored RED, YELLOW, or GREEN. If multiple policers are configured for a packet stream then the packet color is merged from all matching (hit) policers. If any policer is RED then the packet is marked RED. Else if any policer is YELLOW then the packet is marked YELLOW. Otherwise the packet is marked GREEN.

The Policing engine supports several modes such that packets that don't hit a policing/classifier match can be treated as RED, YELLOW, GREEN or policer 0 color. Using policer 0 allows for a system to regulate unregulated traffic.

12.3.1.4.6.1.12.2 Classifier to Host Thread Mapping

The ALE module allows Host Thread mapping based on any packet classification. That is the ALE can generate a thread ID used by the host based on ALE classifier matches.

When enabled the highest classifier match can map to a particular thread ID value.

The ALE also supports an optional default Thread ID value in the event that no classifier match.

Each Thread ID, including the default thread ID, has an enable functionality such that, if no classifier matches occur the default value is used, if the default is not enabled, the switch will use the {port,priority} value instead. If multiple classifier matches occur, the highest matching entry with a thread enable bit set will be used.

Three registers are used for ALE classification thread mapping configuration (CPSW3_CPSW_NU_ALE_THREADMAPDEF, CPSW3_CPSW_NU_ALE_THREADMAPCTL and CPSW3_CPSW_NU_ALE_THREADMAPVAL). The three thread mapping registers are used independently and are separate from the other ALE policing registers. The CPSW3_CPSW_NU_ALE_THREADMAPCTL register allows the CPSW3_CPSW_NU_ALE_THREADMAPVAL register contents to be written to the selected classifier. There is a CPSW3_CPSW_NU_ALE_THREADMAPDEF register that is used for all classifiers. The thread mapping registers can be written or changed at any time but any packets that are already processed will not have their thread altered.

12.3.1.4.6.1.12.3 ALE Classification

When the policers are configured as classifiers, the color marking and policing functions of the policing/classifier engines are not used. One or multiple classifiers can be configured to match on a single packet. For example, a classifier can be enabled to match on priority while another classifier could match IP address.

12.3.1.4.6.1.12.3.1 Classifier to CPPI Transmit Flow ID Mapping

The ALE can generate a 6-bit transmit CPPI Flow ID based on classifier matches that can be used instead of the switch default transmit Flow ID mapping. The switch default flow ID is the remapped received packet priority (0 to 7). Thread and flow ID are used interchangeably for this since there is a single hardware thread (TXST_THREAD_MREADY) but there are 6-bits of FLOW_ID in the transmit CPPI INFO word 0. When enabled, the highest classifier match can map to a particular 6-bit flow ID value that is associated with the classifier. The ALE also supports an optional ALE default thread/flow ID value in the event that no classifiers match. Each thread/flow ID, including the ALE default thread/flow ID, has an enable such that the ALE default thread/Flow ID is used if enabled and if no matches occur (instead of the remapped received packet priority). If the ALE default is not enabled and no matches occur then the switch default value will be used. If multiple classifier matches occur, the highest match with a thread enable bit set will be used. The resultant flow ID has the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG register value added to it to determine the actual value in the INFO 0 Flow ID field.

Three registers are used for ALE classification thread/flow ID mapping configuration (CPSW3_CPSW_NU_ALE_THREADMAPDEF, CPSW3_CPSW_NU_ALE_THREADMAPCTL and CPSW3_CPSW_NU_ALE_THREADMAPVAL). The three thread mapping registers are used independently and are separate from the other ALE policing registers. The CPSW3_CPSW_NU_ALE_THREADMAPCTL register allows the CPSW3_CPSW_NU_ALE_THREADMAPVAL register contents to be written to the selected classifier.

There is a single CPSW3_CPSW_NU_ALE_THREADMAPDEF that is used for all classifiers. The thread mapping registers can be written or changed at any time but any packets that are already processed will not have their thread altered.

12.3.1.4.6.1.13 Mirroring

The ALE supports three mirroring modes: destination port, source port and or table entry.

Destination port mirroring allows packets from any ingress port or trunk which ends up switching to a particular egress destination port or trunk to be mirrored to yet another egress destination port or trunk. For example any traffic from any port that is switched to port 'A' can be also mirrored to port 'B'. (MIRROR_DP=A, MIRROR_DEN=1h, MIRROR_TOP=B in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register).

Source port mirroring allows packets received on any enabled ingress source port or trunk to be switched to the mirror egress port as well as the actual egress destination ports. For example traffic received on ingress port 'A' can be switched to egress port 'B' as well as the intended egress destination port.(Iy_REG_Py_MIRROR_SP=1h in the CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register, MIRROR_SEN=1h, MIRROR_TOP=B in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register).

Table entry mirroring allows for any MAC Address, MAC Address with VLAN, ONU Address or VLAN entry that matches on ingress to be switched to the egress destination as well as the actual egress destination. For example all traffic for VLAN ID of 35 can be mirrored to port 'B'. That is any traffic switched on VLAN ID of 35 will be mirrored. ({VLAN ID of 35 in ALE Table entry index=C}, MIRROR_MIDX=C, MIRROR_MEN=1h, MIRROR_TOP=B)

In the event that mirrored packets are mirrored to or from a port that is also the mirror port the packet will not be duplicated or marked as a mirror packet since the packet has already been on the port as ingress or egress. The packet sent to the mirror port may have modified VLAN info based on the port and VLAN lookup table entries. The mirror port need not be a member of the VLAN ID it is mirroring, the ALE will forward traffic to the mirror port after ingress and egress filters are applied.

The switch may decide to drop any mirror traffic based on switch buffer thresholds as to prevent required traffic from becoming congested.

Port mirroring is controlled by register fields in CPSW3_CPSW_NU_ALE_ALE_CONTROL, CPSW3_CPSW_NU_ALE_ALE_CTRL2 and the port control registers.

- MIRROR_DP - The destination port that will have its traffic mirrored (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_TOP - The port to which mirrored traffic is sent (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_MEN - The enable for mirroring traffic that matches a supported lookup table entry (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_DEN - The Enable for destination port mirroring (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_SEN - The Enable for source port mirroring (CPSW3_CPSW_NU_ALE_ALE_CONTROL register).
- MIRROR_MIDX - The index of a lookup table entry that will be mirrored CPSW3_CPSW_NU_ALE_ALE_CTRL2 register).
- Iy_REG_Py_MIRROR_SP - The enable for the Source port to be mirrored. Although multiple source ports can be mirrored concurrently, a mirror traffic bandwidth issue may occur on the mirror egress port (CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register).

12.3.1.4.6.1.14 Trunking

The ALE supports port trunking of any port in any of four trunk groups. That is, four trunk groups can be supported with up to eight ports in each trunk group. There are no port adjacency rules for trunk groups. When ports are a member of a trunk group, addresses added and used in the lookup table will refer to the trunk group rather than port as indicated in the lookup table entries. If ports are removed from a trunk group, the ALE will redistribute the traffic based on the crc polynomial of enabled fields and the remaining ports within the trunk group. A trunk group may contain only one port. Packet priority, DA, SA, C-VLAN ID, IPv4SA, IPv4DA, IPv6SA, and/or IPv6DA can be used in the hash to generate destination port within the trunk group. If all hash enables are disabled, the packet can be directed to a particular port within the trunk group which allows for testing paths etc. A host directed frame is directed to the directed port regardless of trunk group settings.

Trunking is controlled through fields in the CPSW3_CPSW_NU_ALE_ALE_CTRL2 register and in each ALE CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0 register:

- TRK_EN_DST - Enable destination address hashing for trunk port calculation.
- TRK_EN_SRC - Enable source address hashing for trunk port calculation.
- TRK_EN_PRI - Enable priority hashing for trunk port calculation.
- TRK_EN_IVLAN - Enable inner C-VLAN ID hashing for trunk port calculation.
- TRK_EN_SIP - Enable source IP address hashing for trunk port calculation.
- TRK_EN_DIP - Enable destination IP address hashing for trunk port calculation.
- TRK_BASE - Hashing formula starting value and test port offset.
- Iy_REG_Py_TRUNKEN - Enable this port as a trunk group
- Iy_REG_Py_TRUNKNUM - Trunk group number defines this port as a member of a particular trunk group.

12.3.1.4.6.1.15 DSCP

The ALE can map DSCP field to priority prior to classification matching. When enabled the DSCP is mapped via 64 priority entries such that any DSCP value can be mapped to any of the eight priorities. When a packet is received without a VLAN priority this remapped priority can be used instead of the default Port VLAN priority field. See CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_y and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_DSCP_MAP_REG registers in the Register Manual section for DSCP mapping.

12.3.1.4.6.1.16 Packet Forwarding Processes

There are four processes that an incoming received packet may go through to determine packet forwarding. The processes are *Ingress Filtering*, *VLAN_Aware Lookup*, and *Egress.*

Packet processing begins in the Ingress Filtering process. Each port has an associated packet forwarding state that can be one of four values (Disabled, Blocked, Learning, or Forwarding). The default state for all ports is Disabled. The host sets the packet forwarding state for each port.

In the packet ingress process (receive packet process), there is a forward state test for unicast destination addresses and a forward state test for multicast addresses. The multicast forward state test indicates the port states required for the receiving port in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state for the packet to be forwarded for transmission. The MCAST_FWD_STATE indicates the required port state for the receiving port as indicated in the preceding table. The unicast forward state test indicates the port state required for the receiving port in order to forward the unicast packet. The transmit port must be in the Forwarding state in order to forward the packet. The BLOCK and SECURE bits determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state. The transmit port must be in the Forwarding state regardless. The forward state test used in the ingress process is determined by the destination address packet type (multicast/unicast).

In general, packets received with errors are dropped by the address lookup engine without learning, updating, or touching the address. The error condition and the abort are indicated by the Ethernet port to the ALE. Packets with errors may be passed to the host (not aborted) by a Ethernet port port, if the port has the RX_CMF_EN, RX_CEF_EN, or RX_CSF_EN bit(s) set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG registers. Error packets that are passed to the host by the Ethernet port are considered to be bypass packets by the ALE and are sent only to the host. Error packets do not learn, update, or touch addresses regardless of whether they are aborted or sent to the host. Packets with long or short errors received by the host are dropped. Packets with errors received by the host are forwarded as normal.

The following control bits are in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG registers:

- [22] RX_CEF_EN - enables frames that are fragments, long, jabber, CRC, code, and alignment errors to be forwarded

- [23] RX_CSF_EN - enables short frames to be forwarded
- [24] RX_CMF_EN - enables MAC control frames to be forwarded.

12.3.1.4.6.1.16.1 Ingress Filtering Process

Condition and action
If ((ALE BYPASS) and (host port is not the receive port)) then use host portmask and go to Egress process
if (directed packet) then use directed port number and go to Egress process
If (Rx Iy_REG_Py_PORTSTATE is Disabled) then discard the packet
if ((ALE BYPASS or error packet) and (host port is not the receive port)) then use host portmask and go to Egress process
if (((BLOCK) and (unicast source address found)) or ((BLOCK) and (unicast destination address found))) then discard the packet
if ((ENABLE_RATE_LIMIT) and (rate limit exceeded) and (not BCAST_MCAST_CTL) then if (((Multicast/Broadcast destination address found) and (not SUPER)) or (Multicast/Broadcast destination address not found)) then discard the packet
if ((not forward state test valid) and (destination address found)) then discard the packet to any port not meeting the requirements • Unicast destination addresses use the unicast forward state test and multicast destination addresses use the multicast forward state test.
if ((destination address not found) and ((not transmit port forwarding) or (not receive port forwarding))) then discard the packet to any ports not meeting the above requirements
if (source address found) and (secure) and (not block) and (receive port number != port_number)) then discard the packet
if ((not super) and (drop_untagged) and ((non-tagged packet) or ((priority tagged) and not(en_vid0_mode)) then discard the packet

If (VLAN_Unaware)
CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG = “000000”
CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST = “111111”
CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST = “111111”
UVLAN_MEMBER_LIST = “111111”
else if (VLAN not found)
CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG = CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG
CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST = CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST
CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST = CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST
CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER = CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER
else
CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG = found CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG
CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST = found CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST
CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST = found CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST
UVLAN_MEMBER_LIST = found UVLAN_MEMBER_LIST

if ((not SUPER) and (Iy_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member)) then discard the packet

if ((ENABLE_AUTH_MODE) and (source address not found) and not(destination address found and (SUPER))) then discard the packet
if (destination address equals source address) then discard the packet
if (VLAN_AWARE) goto VLAN_Aware_Lookup process else goto VLAN_Unaware_Lookup process

12.3.1.4.6.1.16.2 VLAN_Aware Lookup Process

Condition and action
if ((unicast packet) and (destination address found with or without VLAN) and (not SUPER) then portmask is the logical "AND" of the PORT_NUMBER and UVLAN_MEMBER_LIST less the host port and goto Egress process
if ((unicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical “AND” of the PORT_NUMBER and the UVLAN_MEMBER_LIST and goto Egress process
if ((unicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_NUMBER and goto Egress process
if (Unicast packet) # destination address not found then portmask is VLAN member LIST less host port and goto Egress process
if ((Multicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical “AND” of CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST and found destination address/VLAN portmask (PORT_MASK) and UVLAN_MEMBER_LIST and goto Egress process
if ((Multicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_MASK and goto Egress process
if (Multicast packet) # destination address not found then portmask is the logical “AND” of CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST and UVLAN_MEMBER_LIST then goto Egress process
if (Broadcast packet) then use found UVLAN_MEMBER_LIST and goto Egress process

Note

The UVLAN_MEMBER_LIST, UVLAN_UNREG_MCAST_FLOOD_MASK, UVLAN_REG_MCAST_FLOOD_MASK and UVLAN_FORCE_UNTAGGED_EGRESS are set in the Section 12.3.1.4.6.1.16.1 *Ingress Filtering Process*, based on VLAN_Unaware, Unknown_VLAN rules and VLAN table entries.

12.3.1.4.6.1.16.3 Egress Process

Condition and action
Clear Rx port from portmask (don’t send packet to Rx port).
Clear disabled ports from portmask.
if ((ENABLE_OUI_DENY) and (OUI source address not found) and (not ALE BYPASS) and (not error packet) and ((not mcast destination address) and (SUPER))) then Clear host port from portmask

if ((not ENABLE_OUI_DENY) and (OUI source address found) and (not ALE BYPASS) and (not error packet) and not ((mcast destination address) and (SUPER))) then Clear host port from portmask
if ((ENABLE_RATE_LIMIT) and (BCAST_MCAST_CTL)) then if (not SUPER) and (rate limit exceeded on any tx port) then clear rate limited tx port from portmask If address not found then SUPER cannot be set.
If portmask is zero then discard packet
Send packet to portmask ports.

12.3.1.4.6.1.16.4 Learning/Updating/Touching Processes

The learning, updating, and touching processes are applied to each receive packet that is not aborted. The processes are concurrent with the packet forwarding process. In addition to the following, a packet must be received without error in order to learn/update/touch an address.

12.3.1.4.6.1.16.4.1 Learning Process

The learning process is applied to each receive packet that is not aborted. The learning process is a concurrent process with the packet forwarding process.

Condition and action
If (directed) then do not learn, update, or set touched else continue
If (not (Learning or Forwarding) or (ENABLE_AUTH_MODE) or (packet error) or (Iy_REG_Py_NO_LEARN)) then do not learn address
if ((Non-tagged packet) and (Iy_REG_Py_DROP_UN_TAGGED)) then do not learn address
if ((VLAN_AWARE) and (VLAN not found) and (unknown UVLAN_MEMBER_LIST = “000”)) then do not learn address
if ((Iy_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member) and (VLAN found)) then do not learn address
if ((source address found) and (receive port_number != PORT_NUMBER) and (SECURE or BLOCK)) then do not update address else continue
if ((source address found) and (receive port number != PORT_NUMBER)) then update address else continue
if ((source address not found) and (VLAN_AWARE) and not (LEARN_NO_VLANID)) then learn address with VLAN
if ((source address not found) and ((not VLAN_AWARE) or (VLAN_AWARE and LEARN_NO_VLANID))) then learn address without VLAN

12.3.1.4.6.1.16.4.2 Updating Process

Condition and action
if (dlr_unicast) then do not update address
If (not(Learning or Forwarding) or (ENABLE_AUTH_MODE) or (packet error) or (Iy_REG_Py_NO_SA_UPDATE)) then do not update address
if ((Non-tagged packet) and (Iy_REG_Py_DROP_UN_TAGGED)) then do not update address
if ((VLAN_AWARE) and (VLAN not found) and (unknown UVLAN_MEMBER_LIST = “000”)) then do not update address

```
if ((ly_REG_Py_VID_INGRESS_CHECK) and (Rx port is not VLAN member) and (VLAN found))
then do not update address
```

```
if ((source address found) and (receive port number != PORT_NUMBER) and (SECURE or BLOCK))
then do not update address
```

```
if ((source address found) and (receive port number != PORT_NUMBER))
then update address
```

12.3.1.4.6.1.16.4.3 Touching Process

```
if ((source address found) and (ageable) and (not touched))
then set touched
```

12.3.1.4.6.1.17 VLAN Aware Mode

The CPSW is in VLAN aware mode when the VLAN_AWARE bit is set in the CPSW3_CONTROL_REG register.

In VLAN aware mode, transmitted packet data is changed depending on the packet type (PKT_TYPE), packet priority (PKT_PRI), and VLAN information.

The VLAN_LTYPE_SEL value is selected by the S_CN_SWITCH bit in the CPSW3_CONTROL_REG register and is either the VLAN_LTYPE_INNER (8100h default) or VLAN_LTYPE_OUTER (88A8h default) value.

12.3.1.4.6.1.18 VLAN Unaware Mode

An egress port is operating in the VLAN unaware mode when the VLAN_AWARE bit in the CPSW3_CONTROL_REG register is cleared to 0h. In VLAN unaware mode, transmit (egress) packets are not modified on egress.

12.3.1.4.6.2 Packet Priority Handling

Packets are received on three ports, two Ethernet port and one CPPI host port. Received packets have a received packet priority (0 to 7, with 7 being the highest priority).

The received packet priority is determined as follows:

1. If the first packet LTYPE = VLAN_LTYPE_SEL then the received packet priority is the packet priority (VLAN tagged and priority tagged packets).
2. Else if the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG, then the received packet priority is the 6-bit TOS field in byte 15 (upper 6 bits) mapped through the port’s DSCP priority mapping registers (IPv4 packet).
3. Else if the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG, then the received packet priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port’s DSCP priority mapping registers (IPv6 packet).
4. Else the received packet priority is the source (ingress) port priority.

The received packet priority is mapped through the receive ports associated packet-priority-to-header-packet-priority-mapping register (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG) to obtain the header packet priority. The header packet priority is the hardware switch priority. The header packet priority is also used as the actual transmit packet priority if the VLAN information is to be sent on egress.

The header packet priority is mapped at each destination FIFO through the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TX_PRI_MAP_REG register (header priority to switch priority mapping register) to obtain the hardware switch priority (hardware queue 0 through 7).

12.3.1.4.6.2.1 Priority Mapping and Transmit VLAN Priority

There are three priorities that are used inside the Gigabit Ethernet Switch: **packet priority**, **header packet priority**, and **switch priority**. The **header packet priority** is used as the outgoing VLAN priority if the packet is egressing from the switch with a VLAN tag. The **switch priority** determines which of the 8 FIFO priority queues the packet uses during egress.

Figure 12-151 below, as well as the corresponding explanation that follows, explains each of the priorities, how they are determined, and how they are used. A number in parentheses in the figure indicates a process (Ethernet port ingress, host port egress, etc.). Each bullet in the text following the diagram explains one of the 5 processes pointed out in the figure.

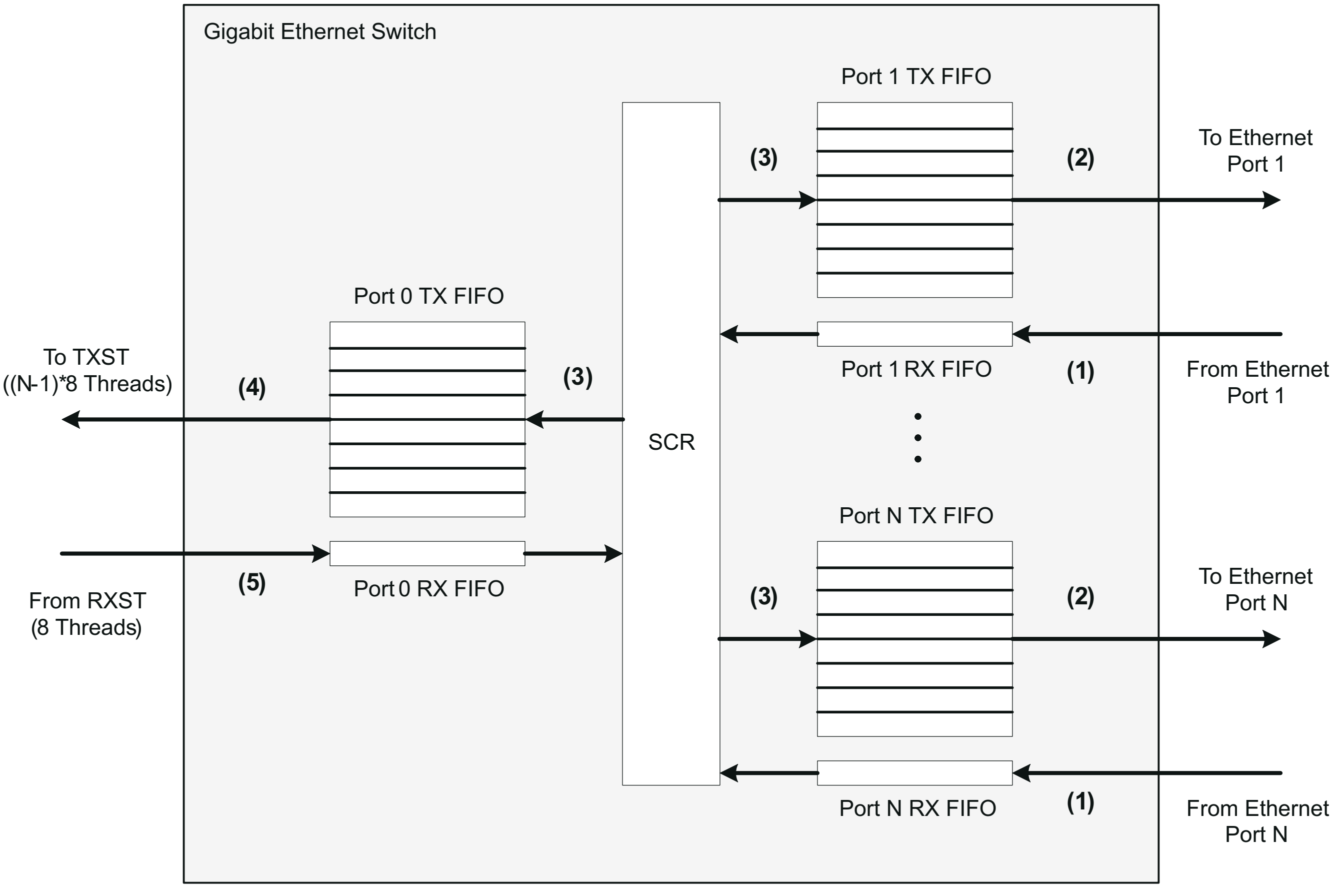


Figure 12-151. Gigabit Ethernet Switch Priority Mapping and Transmit VLAN Processing

From Figure 12-151 above:

- (1) is the ingress process that occurs at the external Ethernet ports
  - The incoming packet is assigned a **packet priority** based on either its VLAN priority, IPv4 or IPv6 DSCP value, or the ingress port's priority. This **packet priority** is then mapped to a **header packet priority** using the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register where N is the port where the packet entered the switch. This process is explained in further detail in Section 12.3.1.4.6.2.
- (2) is the egress process that occurs at the external Ethernet ports
  - If the switch is in VLAN Aware mode then the VLAN header may be added, replaced, or removed during the egress process. If the VLAN header is to be added or replaced, the VLAN priority will come from the **header packet priority** that was determined in process (1) or (5). Transmit VLAN processing is the same for both the host port and the external Ethernet ports and is described in Section 12.3.1.4.6.4.1.
- (3) is the process by which it is decided which priority TX queue to place the packet on in the Port N TX FIFO during egress
  - Each Port's TX FIFO has 8 queues that each correspond to a priority that is used when determining which packet will egress from the switch next at that port. The **header packet priority** (Ethernet port ingress, process (1)) or the receive packet thread (host port 0 ingress, process (5)) gets mapped through the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register (where N is the egress port number) to determine the **switch priority** of the packet. The **switch priority** determines which TX FIFO queue to place the packet in. The FIFO architecture is described in Section 12.3.1.4.6.10.5. The header packet priority to switch priority mapping is discussed in Section 12.3.1.4.6.2.
- (4) is the egress process that occurs at Host Port 0 toward the transmit streaming interface (TXST)
  - The TXST has 8 egress threads for each external Ethernet port (32 threads in a 5-port switch and 64 threads in a 9-port switch). The TX thread that is selected for a packet is determined by the Ethernet port of ingress and the **switch priority** of the packet that was determined in process (3).
  - If the switch is in VLAN Aware mode then the VLAN header may be added, replaced, or removed during the egress process. If the VLAN header is to be added or replaced, the VLAN priority will come from the **header packet priority** that was determined in process (1). Transmit VLAN processing is the same for both the host port and the external Ethernet ports and is described in Section 12.3.1.4.6.4.1.
- (5) is the ingress process that occurs at Host Port 0
  - The incoming packet is assigned a **packet priority** based on either its VLAN priority, IPv4 or IPv6 DSCP value, or the host port's priority. This packet priority is then mapped to a **header packet priority** using the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register.
  - Host port 0 also has a received packet thread. The receive packet thread is based on either the packet's VLAN priority, IPv4 or IPv6 DSCP value, or the streaming interface (RXST) thread that the packet entered host port 0 on.

12.3.1.4.6.3 CPPI Port Ingress

Packets received on the CPPI host port have a received packet priority (0 to 7 with 7 being the highest priority).

The received packet priority is determined as follows:

1. If the first packet LTYPE = VLAN_LTYPE_SEL then the received packet priority is the packet priority (VLAN tagged and priority tagged packets).
2. Else if the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG register, then the received packet priority is the 6-bit TOS field in byte 15 (upper 6 bits) mapped through the port's DSCP priority mapping registers (IPv4 packet).
3. Else if the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG register, then the received packet priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port's DSCP priority mapping registers (IPv6 packet).
4. Else the received packet priority is the source (ingress) port priority

The CPPI Port (port 0) also has a received packet thread. The received packet thread is determined exactly as the received packet priority except for untagged packets. For untagged packets, the received packet thread is the packet streaming interface thread that the packet was received on (instead of the port VLAN priority or DSCP priority). The received packet thread is the hardware switch priority. The received packet thread only determines which hardware switch priority the packet should be sent to, the egress VLAN rules are identical to packets that were received on Ethernet ports (as determined by the header packet priority).

For CPPI ingress packets, the destination port hardware switch priority is the below selected value remapped through CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG:

1. If the ingress packet is priority tagged or vlan tagged:
   - If RX_REMAP_VLAN in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is clear then the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_VLAN in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is set then the the destination hardware switch priority is the packet priority value. Port transmit remapping (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
2. Else if the ingress packet has the first packet LTYPE = 0x0800 and byte 14 (following the LTYPE) is equal to 0x4X, and DSCP_IPV4_EN is set in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register:
   - If RX_REMAP_DSCP_V4 bit in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is clear then the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_DSCP_V4 bit in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is set then the destination hardware switch priority is the 6-bit TOS field in byte 15 (upper 6-bits) mapped through the port's DSCP priority mapping registers (IPV4 packet). Port 1 transmit remapping (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
3. Else if the ingress packet has the first packet LTYPE = 0x86DD and the most significant nibble of byte 14 (following the LTYPE) is equal to 0x6, and DSCP_IPV6_EN is set in P0_CONTROL_REG register:
   - If RX_REMAP_DSCP_V6 bit in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is clear then the destination hardware switch priority is the CPPI receive thread number.
   - If RX_REMAP_DSCP_V6 bit in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register is set then the destination hardware switch priority is the 6-bit priority (in the 6-bits following the upper nibble 0x6) mapped through the port's DSCP priority mapping registers (IPV6 packet). Port 1 transmit remapping (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TX_PRI_MAP_REG should remain the default value) is not compatible with this bit being set, but remapping can be configured on port 0 receive.
4. Else the ingress packet is non-tagged and the destination hardware switch priority is the CPPI receive thread number.

12.3.1.4.6.4 Packet CRC Handling

The P0_TX_CRC_REMOVE bit in the CPSW3_CONTROL_REG register determines if host port egress packets have CRC included or not. If P0_TX_CRC_REMOVE is set to 1h then all packets that are transmitted from port 0 do not contain CRC. If P0_TX_CRC_REMOVE bit is cleared to 0h then all packets that are transmitted from port 0 contain CRC. The CRC type, if present, is determined by the CRC_TYPE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. If the CRC_TYPE bit is cleared to 0h then the CRC present in each packet after host port egress is Ethernet CRC. If the CRC_TYPE bit is set to 1h then the CRC present in each packet after host port egress is Castagnoli CRC.

Note

The CRC type present in the packet after host port egress is determined solely by the CRC_TYPE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register regardless of the CRC type present in the packet during Ethernet port ingress.

12.3.1.4.6.4.1 Transmit VLAN Processing

Transmit packets are NOT modified during switch egress when the VLAN_AWARE bit in the CPSW3_CONTROL_REG register is cleared to 0h. This means that the switch is not in VLAN-aware mode.

The next three sections cover transmit processing when the switch is in VLAN-aware mode for different packet types. The Gigagibit Ethernet switch is in VLAN-aware mode when the VLAN_AWARE bit is set in the CPSW3_CONTROL_REG register. While in VLAN-aware mode, VLAN is added, removed, or replaced according to the type of packet as well as the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header as explained below.

12.3.1.4.6.4.1.1 Untagged Packets (No VLAN or Priority Tag Header)

Untagged packets are all packets that are not a VLAN packet or a priority tagged packet. According to the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header the packet may exit the switch with a VLAN tag inserted or the packet may leave the switch unchanged. The two cases are discussed below.

- Insert VLAN Case:

  Untagged input packets have the header packet VLAN inserted when the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the transmit packet header is de-asserted. For untagged packets, the VLAN EtherType = 0x8100 is inserted after the source address followed by the two byte header packet VLAN. The header packet VLAN is composed of the header packet priority along with the PORT_CFI and and PORT_VID values from the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_PORT_VLAN_REG register (where N is the port that the untagged packet entered the switch) through. The packet length/type field is output four bytes later than it is input and is not removed or replaced. If the CRC is present in the packet data (PASS_CRC is asserted), then the packet CRC is replaced with a hardware generated CRC.

- No Change Case:

  Untagged input packets are output unchanged when the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS transmit packet header bit is asserted.

12.3.1.4.6.4.1.2 Priority Tagged Packets (VLAN VID == 0 && EN_VID0_MODE ==0h)

Priority tagged packets are packets that contain a VLAN header with VID = 0. According to the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header, priority tagged packets may exit the switch with their VLAN ID and priority replaced or they may have their priority tag completely removed. The two cases are discussed below.

Note

In order for a priority tagged packet to fall into this category the ENABLE_VID0_MODE bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register must also be set to 0h. If the ENABLE_VID0_MODE bit in the CPSW3_CPSW_NU_ALE_ALE_CONTROL register is set to 1h, then packets with a VLAN VID of 0 will fall into the VLAN Tagged Packets category in Section 12.3.1.4.6.4.1.3 below.

- Replace Priority and VLAN ID Case:

  Priority tagged input packets have the packet VLAN ID and the packet priority replaced with the header packet VLAN ID and the header packet priority when the transmit packet header CPSW_FORCE_UNTAGGED_EGRESS_REG[1-0] MASK bit is de-asserted. The header packet VLAN ID comes from the PORT_VID bits in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_PORT_VLAN_REG register (where N is the port where the packet entered the switch). The header packet priority is based on the packet priority to header packet priority mapping in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register (where N is the port where the packet entered the switch).

- Remove VLAN Header Case:

  Priority tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is asserted. The 0x8100 EtherType is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the PASS_CRC input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority-tagged packets use all four input CRC bytes as pad, input 65-byte priority-tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the PASS_CRC input bit is not asserted - input 64-67 byte (on the wire) priority-tagged packets go out as 60-63 byte packets. The output CRC is replaced with a generated CRC when the VLAN is removed.

12.3.1.4.6.4.1.3 VLAN Tagged Packets (VLAN VID != 0 || (EN_VID0_MODE ==1h && VLAN VID ==0))

VLAN tagged packets are packets that contain a VLAN header specifying the VLAN the packet belongs to (VID), the packet priority (PRI), and the drop eligibility indicator (CFI). According to the CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit in the packet header, VLAN tagged packets may exit the switch with their VLAN priority replaced or they may have their VLAN header completely removed. The two cases are discussed below.

- Replace Priority Case:

  VLAN tagged input packets are output with the packet priority replaced with the header packet priority when the transmit packet header CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is deasserted. The header packet priority is based on the packet priority to header packet priority mapping in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_PRI_MAP_REG register (where N is the port where the packet entered the switch). If the CRC is present in the packet data (PASS_CRC is asserted), then the packet CRC is replaced with a generated CRC.

- Remove VLAN Header Case:

  VLAN tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG[1-0] UVLAN_FORCE_UNTAGGED_EGRESS bit is asserted. The 0x8100 EtherType is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the PASS_CRC input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority tagged packets use all four input CRC bytes as pad, input 65-byte priority tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the PASS_CRC input bit is not asserted - input 64-67 byte (on the wire) priority tagged packets go out as 60-63 byte packets. The output CRC is replaced with a generated CRC when the VLAN is removed.

12.3.1.4.6.4.2 Ethernet Port Ingress Packet CRC

All Ethernet ports check the ingress packet CRC in all modes/speeds. The receive port can check either Ethernet CRC or Castagnoli CRC as determined by the CRC_TYPE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register.

12.3.1.4.6.4.3 Ethernet Port Egress Packet CRC

Ethernet ports transmit each egress packet with the CRC selected by the CRC_TYPE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register, regardless of the type of CRC that the packet had on ingress to the switch. At the egress port after passing through the switch, the packet CRC is checked for correctness and if the CRC is correct then the packet is output with the generated selected output CRC. If the packet CRC is incorrect, due either to a bit flip in a memory or an error CRC passed in on host ingress, then the generated egress CRC type is used with at least a single byte of the CRC inverted to indicate the error. If the packet length including CRC is divisible by 4 then all 4 CRC bytes will be inverted on error. If there are three bytes remainder after dividing the packet length by 4 then three bytes will be inverted (and so on down to one byte remainder).

12.3.1.4.6.4.4 CPPI Port Ingress Packet CRC

CPPI port ingress packets can be passed in with or without a CRC. The host port is Ethernet CRC only. CPPI ingress packets are not checked for CRC correctness on CPPI ingress, however they are checked for correctness on Ethernet egress and are output with a CRC error if they came in with a CRC error. If a CPPI ingress packet does not have the INFO0 PASSED_CRC bit set then a CRC will be generated for the packet on

CPPI ingress. If the PASSED_CRC bit is set then the packet is received and forwarded unchanged. The CRC type is input in the INFO0 word CRC_TYPE bit and must be Ethernet CRC.

12.3.1.4.6.4.5 CPPI Port Egress Packet CRC

The P0_TX_CRC_REMOVE bit in the CPSW3_CONTROL_REG register determines if CPPI egress packet have an Ethernet CRC included or not.

12.3.1.4.6.5 FIFO Memory Control

Each of the two CPSW_3G ports has an identical associated FIFO. Each FIFO contains a single logical receive queue and eight logical transmit queues (priority 0 through 7 with 7 the highest priority). Each FIFO memory contains 20,480 bytes (20k) total organized as 2560 by 64-bit words contained in a single memory instance. The FIFO memory is used for the associated port transmit and receive queues. The TX_MAX_BLKS field in the FIFOs associated CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG register determines the maximum number of 1k FIFO memory blocks to be allocated to the eight logical transmit queues (transmit total). The RX_MAX_BLKS field in the FIFO's associated CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG register determines the maximum number of 1k memory blocks to be allocated to the logical receive queue. The TX_MAX_BLKS value plus the RX_MAX_BLKS value must sum to 20 (the total number of blocks in the FIFO). If the sum were less than 20, then some memory blocks would be unused. The default is 17 (decimal) transmit blocks and three receive blocks. The FIFOs follow the naming convention of the Ethernet ports. Host Port is Port0 and External Ports is Port1.

Each transmit FIFO contains a configurable number of blocks (20 max) that are either 1k or 4k byte blocks that can be allocated to any priority.

12.3.1.4.6.6 FIFO Transmit Queue Control

There are eight transmit queues in the Ethernet port transmit FIFO. Software has some flexibility in determining how packets are loaded into the queues and on how packet priorities are selected for transmission (how packets are removed and transmitted from queues).

12.3.1.4.6.6.1 CPPI Port Receive Rate Limiting

Port 0 receive operations can be configured to rate limit the host ingress data for each receive thread (priority). CPPI Receive has 8 threads for QOS. There is a committed information rate (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y, where y = 0 to 7) and an excess information rate for each thread (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_y, where y = 0 to 7). Rate limiting is enabled for a thread when the committed information rate for the thread is non-zero. The excess information rate for a priority is enabled when the excess information rate for the priority is non-zero. The committed information rate must be non-zero if the excess information rate is configured to be non-zero. That is, there must be a configured non-zero committed information rate for there to be a configured non-zero excess information rate. Bulk traffic on other non-rate limited priorities does not impact the committed information traffic on a priority. However, bulk traffic on other non-rate limited threads does impact the excess information rates. No bulk thread will be enabled to send unless there are CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_PRI_CTL_REG[15-12] TX_HOST_BLKS_REM number of unused blocks remaining in each of the Ethernet port transmit FIFOs. The “blocks remaining check” ensures that bulk traffic from the host will not block rate-limited traffic from the host. Rate limited channels must be the highest priority channels. For example, if two rate limited channels are required then threads 7 and 6 should be configured for committed information (and excess information if desired). When any channels are configured to be rate-limited, the priority type must be fixed for receive. Round-robin priority type is not allowed when rate-limiting is configured for any thread. The configured transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is configured to receive is controlled by the below equation. If the configured excess information rate is zero, then only the committed information rate is transferred:

Priority Transfer rate [Mbit/s] = ((((Frequency in MHZ) * CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y) / 32768) + (((Frequency in MHZ) * CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_y) / 32768))

Where the *frequency* is the CPPI_ICLK frequency (in MHz) and priority 0 to 7.

For example, 10Mbps on priority 7 would give the below:

10Mbps = ~ ((350 * 936) / 32768), at 350Mhz and CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y[27-0] PRI_CIR value = 936 (no excess information rate)

12.3.1.4.6.6.2 Ethernet Port Transmit Rate Limiting

Ethernet port transmit operations can be configured to rate limit egress data for each egress priority. There is a committed information rate (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y, where y = 0 to 7) and an excess information rate for each priority (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_y, where y = 0 to 7). Rate limiting is enabled for a priority when the committed information rate for the priority is non-zero. The excess information rate for a priority is enabled when the excess information rate for the priority is non-zero. The committed information rate must be non-zero if the excess information rate is configured to be non-zero. That is, there must be a configured non-zero committed information rate for there to be a configured non-zero excess information rate. Bulk traffic on other non-rate limited priorities does not impact the committed information traffic on a priority. However, bulk traffic on other non-rate limited threads does impact the excess information rates. Rate limited channels must be the highest priority channels. For example, if two rate limited channels are required then priorities 7 and 6 should be configured for committed information (and excess information if desired). The configured transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is configured to send is controlled by the below equation. If the excess information rate is disabled then the committed information rate only is transferred:

Priority Transfer rate [Mbit/s] = ((((Frequency in MHZ) * CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_y) / 32768) + (((Frequency in MHZ) * CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_y) / 32768))

Where the *frequency* is the CPPI_ICLK frequency (in MHz) and priority 0 to 7.

12.3.1.4.6.7 Interspersed Express Traffic (IET – P802.3br/D2.0)

When IET is enabled through CPSW3_CONTROL_REG[17] IET_ENABLE = 1h and configured, IET allows premptable traffic on selected transmit priorities to be prempted by express traffic on selected express priorities. Received traffic is separated onto express and prempt receive queues. When IET is disabled (IET_ENABLE = 0h), all Ethernet traffic is express traffic and switch operation is as if IET does not exist. Traffic is only intended to be moved to the prempt queue after premption is verified and enabled.

12.3.1.4.6.7.1 IET Configuration

1. Using the prempt receive queue requires more blocks to be allocate to the ports receive FIFO. Write a value of decimal 7 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG[7-0] RX_MAX_BLKS bit field, and a value of decimal 13 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG [15-8] TX_MAX_BLKS register for every port to be enabled for IET.
2. Write the [23-0]MAC_VERIFY_CNT bit field in the Ethernet port CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_VERIFY_REG register to set the verify/response timeout count. The default is 10ms for Gigabit mode. For other time values or link speeds the verify count should be updated. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[2] MAC_DISABLEVERIFY bit is to be set (this is forced mode) then this step is unneeded.
3. The receive FIFO block allocation is insufficient if CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP[31-0] COUNT is nonzero, indicating that receive packets are being dropped due to FIFO block allocation.
4. Write the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG register in the Ethernet port as below:
   - Set the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CONTROL_REG[16] IET_PORT_EN bit. The port will not actually be enabled until bit IET_ENABLE is set in the CSL_CPSW3_CONTROL_REG.

  - The CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[0] MAC_PENABLE bit can be set as desired. No effect will occur until IET_ENABLE is set. This bit enables premptable packets to be prempted by express traffic but does not preclude packets from being sent to the prempt queue.
  - If verify/response is desired then CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[3] MAC_LINKFAIL should be cleared by software to enable verify and response packets. Otherwise, MAC_DISABLEVERIFY bit should be set for forced mode. Verification and response will occur immediately after clearing this bit.
  - Configure the remaining CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG register bits as desired.
5. Set the IET_ENABLE bit in the CSL_CPSW3_CONTROL_REG register to enable IET operations.
6. After preemption has been verified, the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[23-16] MAC_PREMPT field is written to configure the FIFO priorities to be sent to the prempt queue (the other priorities with cleared bits go to the express queue). The hardware switch for each queue from express to prempt happens only when there are no packets queued on the priority.

12.3.1.4.6.8 Enhanced Scheduled Traffic (EST – P802.1Qbv/D2.2)

12.3.1.4.6.8.1 Enhanced Scheduled Traffic Overview

- When enabled and configured, EST allows express queue traffic to be scheduled (placed) on the wire at specific repeatable time intervals.
- EST operates on a repeating time interval generated by the CPTS EST function generator. For example, a 125us repeating time interval can be configured.
- Each Ethernet port has 128 EST fetch commands maximum in the global EST fetch RAM.
- Each 22-bit fetch command consists of a 14-bit fetch count (14 MSB’s) and an 8-bit priority fetch allow (8 LSB’s) that will be applied for the fetch count time in wireside clocks.
- The configured port fetch commands are executed in sequence, beginning at port address zero each time through the time interval beginning at cycle start.
- EST allows non-scheduled express and prempt queue traffic to be cleared from the wire to ensure that the scheduled traffic is transmitted at the proper time (zero allow).
- EST can be used with or without premption. The CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG[23-16] MAC_PREMPT value determines whether the priority is enabled on the express or prempt queue. Whether a priority is on the express or prempt queue only effects the wire clear time from an EST operation perspective.
- Software should not move priorities to the prempt queue unless preemption is configured, enabled, and verified allowing preemption to occur.
- Express packet time stamp events can be enabled to assist software in configuring and timing EST operations.

12.3.1.4.6.8.2 Enhanced Scheduled Traffic Fetch RAM

- The EST fetch RAM is read/writable in the CPSW configuration address space.
- The Ethernet transmit port has 128 locations in the global EST fetch RAM.
  - Ethernet port 1 has EST fetch RAM addresses 0x000-0x07F.
- **One buffer operation:** When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[0] EST_ONEBUF is set to 1h, the 128 port locations operate as one buffer. The EST_BUFACT bit in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_FIFO_STATUS_REG register is the upper address bit of the port’s fetch RAM address indicating whether operation is currently in the upper or lower 64 locations of the port’s fetch RAM.
- **Two buffer operation:** When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[0] EST_ONEBUF is cleared there are two 64-location buffers with CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[1] EST_BUFSEL selecting the buffer to be used. When the buffer is switched by changing the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[1] EST_BUFSEL value, the actual switch occurs on cycle start. The actual buffer being used is indicated by the EST_BUFACT bit in

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_FIFO_STATUS_REG. Software should avoid writing the switched out buffer fetch RAM locations until it detects that the actual switch has occurred.

- The first address location in the port's fetch RAM space (location zero) is read at the beginning of each EST time interval (cycle start). Addresses are then read in ascending order for the duration of the interval. The port address zero is then read again at the beginning of the next cycle repeating the time interval packet operations.

12.3.1.4.6.8.3 Enhanced Scheduled Traffic Time Interval

- Each Ethernet port has an Enhanced Scheduled Traffic Function (ESTF) generator in the CPTS submodule.
- The EST function generator generates the EST time interval as a configured number of CPTS reference clocks (CPTS_RFT_CLK).
- The EST function generator rising edge is the cycle start time and the cycle repeats (cycle start occurs) after every time interval.
- The first fetch allowed value is at the port base address zero in the EST fetch RAM and is actually applied 16 wireside clocks after cycle start. The 16 clock cycle delay allows the first fetch value time to be fetched from the EST fetch RAM (prefetch time at cycle start).
- Each successive fetch allow is applied for the associated fetch count thereafter. The minimum non-zero fetch count is 16. The minimum value of 16 guarantees that the next fetch value has time to be fetched before the current fetch count is over. There are 64 maximum fetch values when CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[0] EST_ONEBUF = 0h, and 128 maximum fetch values when CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[0] EST_ONEBUF = 1h.
- The next cycle start then causes the fetch to once again start at the port address zero.

12.3.1.4.6.8.4 Enhanced Scheduled Traffic Fetch Values

- The 22-bit fetch value is made up of the 14-bit fetch count and the 8-bit fetch allow.
- The fetch time indicates the number of wireside clocks that the fetch allow will be active.
- The fetch count is in Ethernet wireside clocks which is bytes in Gigabit mode (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[7] GIG = 1h) and nibbles in 10/100Mbps mode.
- When a fetch allow bit is set, the corresponding priority is enabled to begin packet transmission on an allowed priority subject to rate limiting. The actual packet transmission on the wire may carry over into the next fetch count and is the reason for the wire clear time in the fetch zero allow.
- When a fetch allow bit is cleared, the corresponding priority is not enabled to transmit for the fetch count time.
- A non-zero fetch allow value with a non-zero fetch count causes the fetch allow value to be applied for the fetch count number of wireside clocks.
- A zero fetch count causes the associated fetch allow to be held for the duration of the cycle (until the next cycle start).
- A zero fetch allow with a non-zero fetch count is intended to clear the wire for a scheduled (timed) express packet in the next fetch. A zero fetch allow indicates that no packet can be started for transmission for the associated fetch count. The associated fetch count must be sufficient to guarantee that the wire is cleared given that a packet on an allowed priority in the previous fetch could have been started on the previous clock and that there is hardware latency in the clear time. The timed packet should be sent on a priority that is enabled in the next fetch but disabled in the current zero allow fetch. The fetch allow previous to a zero allow should have only prempt priorities enabled or only express priorities enabled but not both.
- The number of clocks required to clear the wire varies depending Ethernet wire speed and on whether express or prempt priorities were allowed in the previous fetch command.

12.3.1.4.6.8.5 Enhanced Scheduled Traffic Packet Fill

Packet fill can (should) be configured and enabled to occur in the fetch count time associated with a fetched zero allow that preceeds a timed express packet. The intention with fill is that a smaller packet on a non-timed priority might be able to be inserted on the wire during the wire clear time which would increase wire utilization. Fill must be configured to ensure that any fill packet does not conflict with the timed express packet allowed in the next fetch. Incorrect configuration might push out in time any express timed packet which indicates that the fill margin needs to be increased.

Fill Comfiguration:

- The **pn_est_fill_margin** value in **Enet_Pn_EST_Control** should be written with a 0x100 value.
- The **pn_est_prempt_comp** value in **Enet_Pn_EST_Control** should be written with a 0x12 value (if IET is to be configured and enabled). This value times eight is the number of wireside clocks required to clear prempt packets off the wire at the end of a zero allow.
- The **pn_est_fill_en** bit in **Enet_Pn_EST_Control** should be set.

12.3.1.4.6.8.6 Enhanced Scheduled Traffic Time Stamp

The EST can be configured to generate CPTS timestamp events for selected express traffic. The EST timestamp events use the CPTS host event type (CPSW3_CPSW_NU_CPTS_EVENT_1_REG[23-20] EVENT_TYPE = 7 decimal. The EST timestamps will not override host sent timestamps for packets that were sent from the host with an enabled host timestamp.

- EST Events (host events) contain the below information:
  - Time Stamp of the selected express packet.
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[28-24] PORT_NUMBER indicates the transmit port number.
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[23-20] EVENT_TYPE is decimal 7 (host event).
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[23-20] MESSAGE_TYPE indicates the packet transmit hardware switch priority.
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[15-0] SEQUENCE_ID upper nibble indicates the packet receive port number.
  - The event CPSW3_CPSW_NU_CPTS_EVENT_1_REG[15-0] SEQUENCE_ID lower byte indicates the sequence number of the express packet in numerical order. The first event is event one, the second is event two and so on. The sequence ID rolls over to zero after 0xFF (8-bits).
  - The event domain is the value from the CPSW3_CPSW_NU_EST_TS_DOMAIN_REG[7-0] EST_TS_DOMAIN register.
- When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[2] EST_TS_EN is set, timestamp events will be generated on selected express traffic.
- When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[3] EST_TS_FIRST is also set, events will be generated only on the first express packet in each time interval. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is also set then the event will only be on the first CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[7-5] EST_TS_PRI express packet in the time interval. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is clear then the event will be generated on the first express packet in the time interval on any priority.
- When CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[3] EST_TS_FIRST is clear, events will be generated on every express packet. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is set then the event will be generated on every CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[7-5] EST_TS_PRI express packet. If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is clear then event will be generated on every express packet on any priority.

12.3.1.4.6.8.7 Enhanced Scheduled Traffic Packets Per Priority

The number of packets allowed in a transmit FIFO priority can be selected by writing a non-zero value to CPSW_P0_RX_PKTS_PRI_REG register (packet priority 0 to 7). Then port 0 receive gap should then be enabled by setting the corresponding priority through CPSW_P0_RX_GAP_REG[7-0] RX_GAP_EN bit field. The receive gap allows a packet to land in the transmit FIFO before another packet is allowed in which guarantees that only the selected number (max) of packets is allowed in on the specified priority. If the receive gap is not enabled, then there might be one or two more packets allowed in on the priority/thread than the packets per priority value has selected (through CPSW_P0_RX_PKTS_PRI_REG register).

12.3.1.4.6.9 Audio Video Bridging

Audio Video Bridging is an ongoing project of IEEE 802.1 concerned with enabling low-latency streaming of time-sensitive audiovisual data over networks. Devices are designated as talkers (transmitters), bridges, or listeners (receivers). It is suggested that the maximum latency could be 2 ms over 7 hops for Class A devices and 20 ms over 7 hops for Class B devices. A hop is essentially a single local area network stage in the journey of a packet. Every time a bridge is encountered between one network section and another a hop is involved. One of the performance goals is that AVB streams will not use more than 75 percent of a link's bandwidth, leaving the remaining capacity for non-AVB streams.

The goal of developing AVB is simply--extend Ethernet's data-networking capabilities to the realm of reliable real-time audio/video networking.

An "Audio Video Bridging" network is one that implements a set of protocols being developed by the IEEE 802.1 Audio/Video Bridging Task Group. There are four primary differences between the proposed Audio Video Bridging architecture and existing 802 architectures (from now on the term "AVB" will be used instead of "Audio Video Bridging"):

1. Precise synchronization - IEEE 802.1AS: "*Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks.* "a.k.a Precision Time Protocol (PTP).
2. Traffic shaping for media streams - IEEE 802.1Qav: "*Virtual Bridged Local Area Networks:* Forwarding and Queuing for Time-Sensitive Streams."
3. Admission controls - IEEE 802.1Qat: "*Virtual Bridged Local Area Networks - Amendment 9:* Stream Reservation Protocol (SRP)."
4. Identification of non-participating devices - IEEE 802.1BA: "Audio/Video Bridging (AVB) Systems"

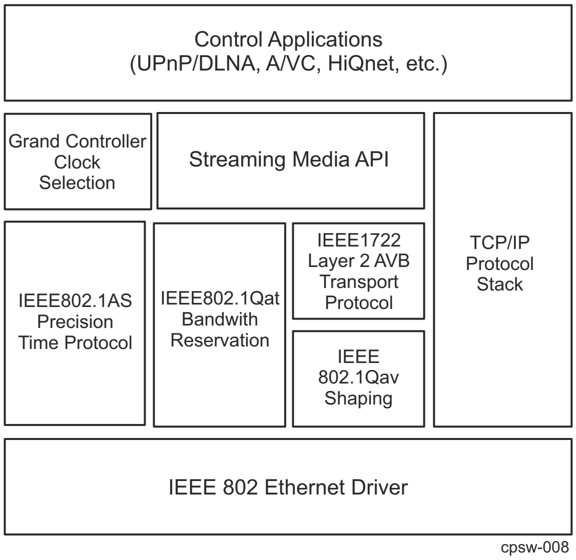


Figure 12-152. The Network Static with AVB

The following sections describe the media transport protocols that work within the AVB framework.

12.3.1.4.6.9.1 IEEE 802.1AS: Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks (Precision Time Protocol (PTP))

The protocol defined by 802.1AS automatically selects a device to be the controller clock, and then distributes this clock throughout the bridged LAN / IP subnet to all other network devices using link-specific transmit/receive time-stamping. However, we only use a two-step solution only on transmit. That is, we do not modify a packet with the timestamp on the way out. The timestamp packet is sent out and then a separate message with the timestamp is sent by the host afterward. Receive can be one or two step.

Note

The 802.1AS-distributed clock is not used as a media clock. Rather, the shared 802.1AS clock reference is used to regenerate the media clock at the listener/renderer. Such a reference removes the need to force the latency of the network to be constant, or compute long running averages in order to estimate the actual media rate of the transmitter in the presence of substantial network jitter. IEEE 802.1AS is based on the ratified IEEE 1588 standard.

Based on IEEE 1588:2002,A PTP devices exchange standard Ethernet messages that synchronize network nodes to a common time reference by defining clock controller selection and negotiation algorithms, link delay measurement and compensation, and clock rate matching and adjustment mechanisms.

Designed as a simplified profile of IEEE 1588, a primary difference between 1588 and IEEE 802.1AS is that PTP is a layer 2-in other words, a non-IP routable protocol. Like IEEE 1588, PTP defines an automatic method for negotiating the network clock controller, the Best Controller Clock Algorithm (BCCA). PTP nodes can be assigned one of eight priority levels, presumably based on clock quality. BCCA defines the underlying negotiation and signaling mechanism whose purpose is to identify the AVB LAN Grandcontroller. Once a Grandcontroller has been selected, synchronization automatically begins.

At the core of 802.1AS synchronization is time-stamping. In short, during PTP message ingress/egress from the 802.1AS-capable MAC, the PTP Ether type triggers the sampling of the value of a local real-time counter (RTC). Target nodes compare the value of their RTC against the PTP Grandcontroller and, by use of link delay measurement and compensation techniques, match their RTC value to the time of the AVB LAN PTP domain. After network time throughout the AVB LAN has converged, periodic SYNC and FOLLOW_UP messages provide the information that enables the PTP rate matching adjustment algorithms. The result is all PTP nodes are then synchronized to the same "Wall Clock" time. PTP assures 1-μs accuracy over seven network hops.

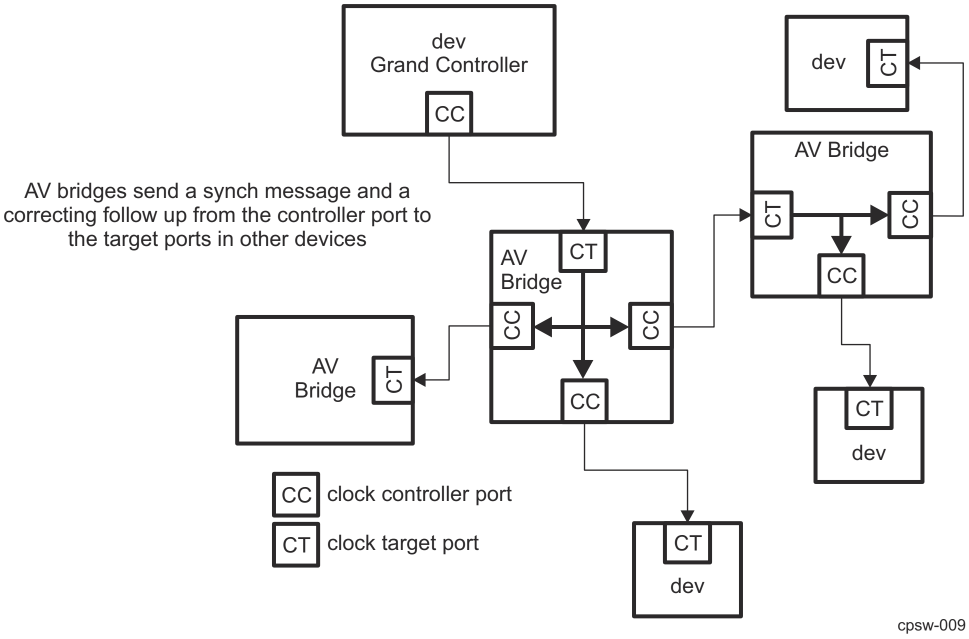


Figure 12-153. AVB Network & PTP Clock Entities

The media transport protocols that work within the AVB framework are:

12.3.1.4.6.9.1.1 IEEE 1722: "Layer 2 Transport Protocol for Time-Sensitive Streams"

AVBTP or 1722 sits above the IEEE 802.1 AVB plumbing and below the application layer. It acts as the conduit between an Ethernet MAC and a streaming application. AVBTP abstracts the underlying network transmission channel to enable the virtual connection of distributed audio and video CODECs over reliable Ethernet networks. A complete AVBTP Ethernet packet is shown in Figure 12-154 and illustrates how IEC 61883-6 AM824 uncompressed audio samples are encapsulated in an Ethernet frame.

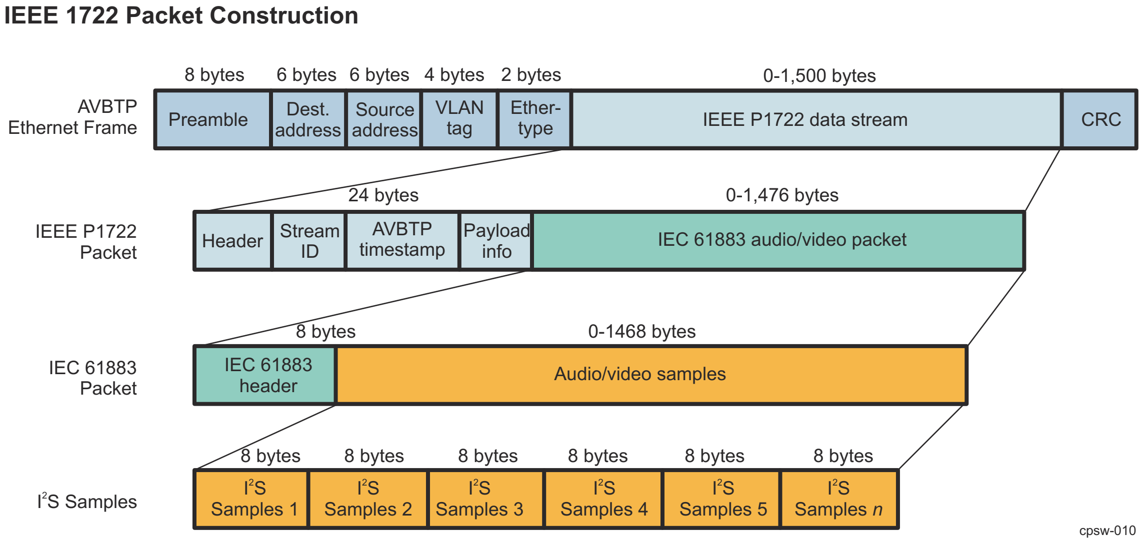


Figure 12-154. IEEE 1722 Packets

1722 or AVBTP Presentation Time and Synchronization:

Synchronization in an AVB network starts with the Precision Time Protocol but ends with synchronized media clocks. PTP is responsible for synchronizing all nodes in an AVB network to identical wall clock time; not for synchronizing media clocks. In other words, PTP does not actually transport synchronized media clocks but instead provides a low-level building block crucial for managing a distributed media synchronization system.

A crucial benefit of this approach is coexistence of multiple, independent media clock domains on an AVB network. Unrelated audio and video streams can simultaneously exist in the same LAN.

12.3.1.4.6.9.1.1.1 Cross-timestamping and Presentation Timestamps

AVBTP assumes that AVB node media clocks are clocked by free-running oscillators. It is also assumed that the node's internal concept of wall clock time has been synchronized to the PTP Grandcontroller. AVBTP media clock sources embed "AVBTP Presentation Timestamps" in AVBTP streaming packets. Figure 12-155 illustrates the relationship between PTP network time and AVBTP Presentation Timestamps.

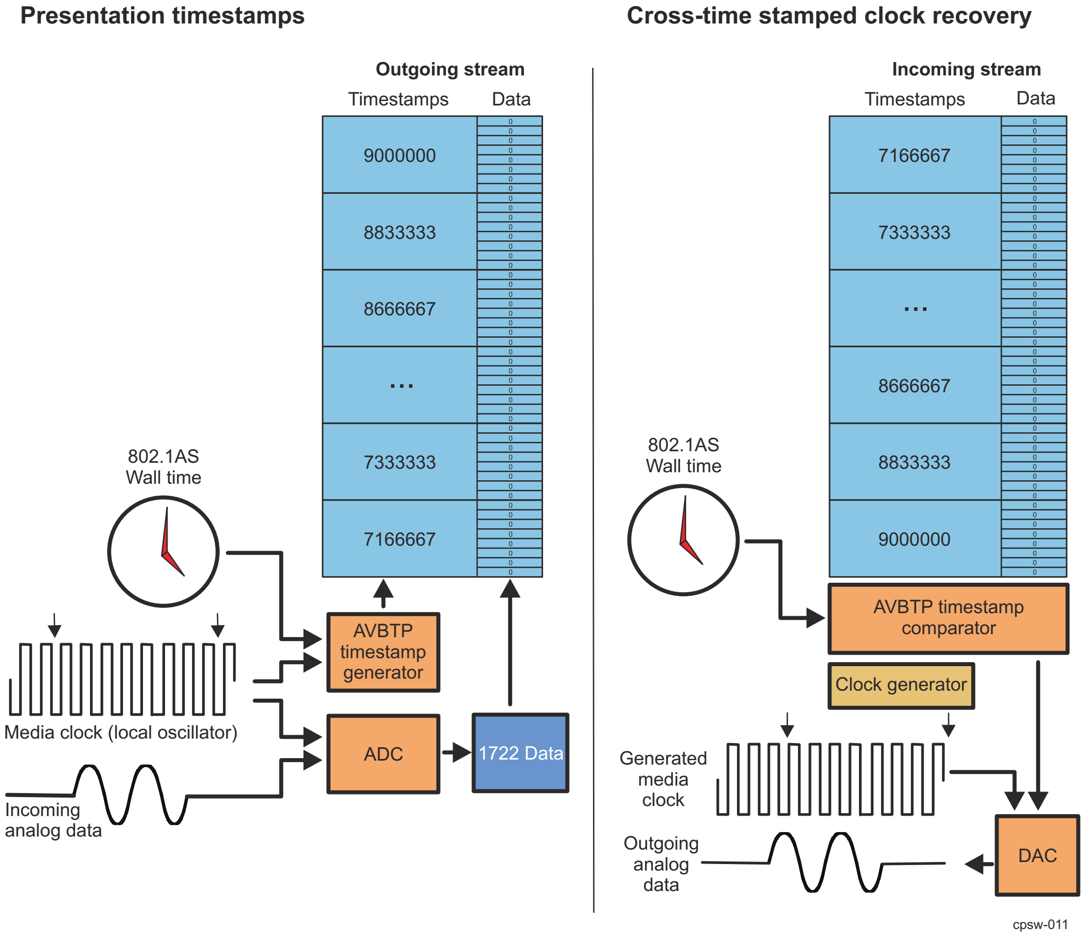


Figure 12-155. Cross Time Stamping and Presentation Timestamps

12.3.1.4.6.9.1.2 IEEE 1733: Extends RTCP for RTP Streaming over AVB-supported Networks

This standard specifies the protocol, data encapsulations, connection management and presentation time procedures used to ensure interoperability between audio and video based end stations that use standard networking services provided by all IEEE 802 networks meeting QoS requirements for time-sensitive applications by leveraging the Real-time Transport Protocol (RTP) family of protocols and IEEE 802.1 Audio/Video Bridging (AVB) protocols.

12.3.1.4.6.9.2 IEEE 802.1Qav: "Virtual Bridged Local Area Networks: Forwarding and Queuing for Time-Sensitive Streams"

This standard allows bridges to provide guarantees for time-sensitive (that is, bounded latency and delivery variation), loss-sensitive real-time audio video (AV) data transmission (AV traffic). It specifies per priority ingress metering, priority regeneration, and timing-aware queue draining algorithms. This standard uses the timing derived from IEEE 802.1AS. Virtual Local Area Network (VLAN) tag encoded priority values are allocated, in aggregate, to segregate frames among controlled and non-controlled queues, allowing simultaneous support of both AV traffic and other bridged traffic over and between wired and wireless Local Area Networks (LANs).

Such a guarantee in bandwidth is provided by two functional entities:

- A registration protocol, which registers the service and its maximum network utilization with a device or switch (IEEE 802.1Qat: "Virtual Bridged Local Area Networks - Amendment 9: Stream Reservation Protocol (SRP)")
- A hardware bandwidth management service.
  - Receive policing
  - Transmit rate control.

End Station Behavior

In order for an end station to successfully participate in the transmission and reception of time-sensitive streams, it is necessary for their behavior to be compatible with the operation of the forwarding and queuing mechanisms employed in bridges.

The requirements for end stations that participate as "talkers" i.e., sources of time-sensitive streams are different from the requirements that apply to "listeners", the destination station(s) for the streams.

Talker Behavior

In order for Talker-originated data streams to make use of the credit-based shaper behavior in Bridges, it is a requirement for a Talker to use the priorities that the Bridges in the network recognize as being associated with SR classes exclusively for transmitting stream data.

It is also necessary for the Talker and the Bridges in the path to the Listener(s), to have a common view of the bandwidth required in order to transmit the Talker's streams, and for that bandwidth to be reserved along the path to the Listener(s). This latter requirement can be met by means of stream reservation mechanisms, such as defined in SRP, or by other management means.

End stations that are Talkers shall exhibit transmission behavior for frames that are part of "time-sensitive streams" that is consistent with the operation of the credit-based shaper algorithm, both in terms of the way they transmit frames that are part of an individual data stream, and in terms of the way they transmit stream data frames from a Port.

In effect, the queuing model for a Talker Port (and a Listener port), and for given priorities, can be considered to look like Figure 12-156.

Listener Behavior

The primary requirement for a listener station is that it is capable of buffering the amount of data that could be transmitted for a stream during a time period equivalent to the accumulated maximum jitter that could be experienced by stream data frames in transmission between Talker and Listener.

From the point of view of the specification of the forwarding and queuing requirements for time-sensitive streams, it is assumed that the listener will assess the buffering required for a stream as part of the stream bandwidth reservation mechanisms employed by the implementation.

The credit-based shaper's operation details are beyond the scope of this document.

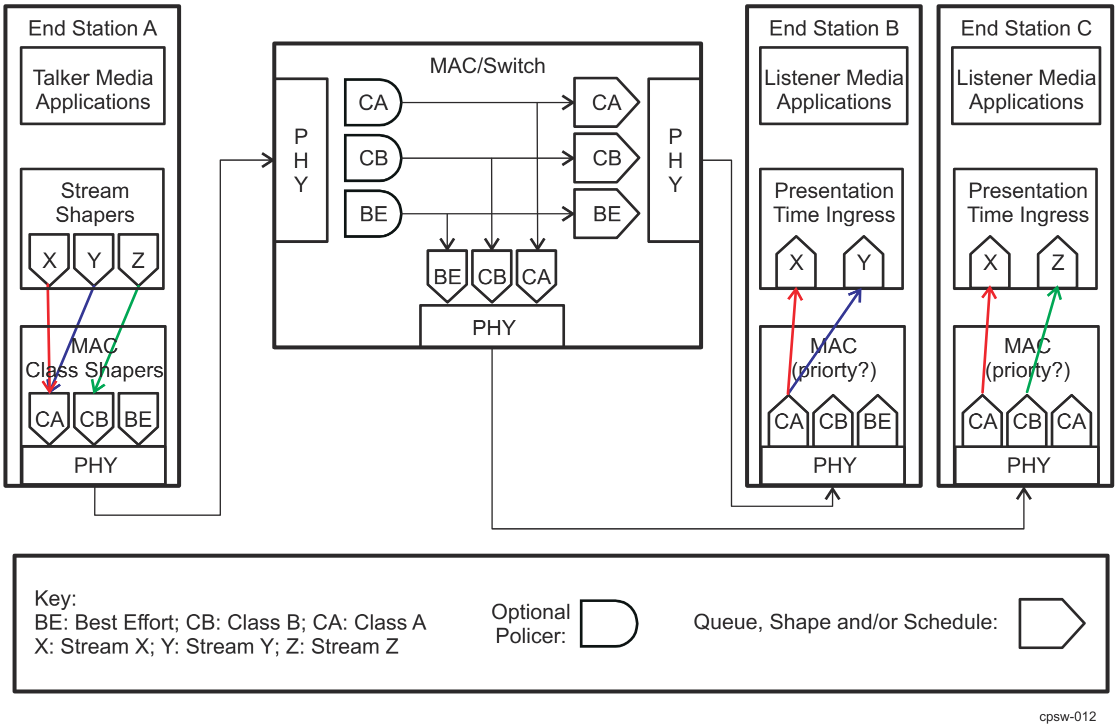


Figure 12-156. AV Stream Queuing/Policing

12.3.1.4.6.9.2.1 Configuring the Device for 802.1Qav Operation

There is no dedicated register-set to be configured for the time-sensitive stream handling. The list of functional features of CPSW_3G that will have to be configured are:

- DESCRIPTORS and CHANNEL CONFIGURATIONS:
  - CPPI TX and RX descriptors
  - VLAN and Priority tags

Table 12-201. Example of TX Configuration

TX DMA CHANNEL	Packet Priority	Switch Queue Priority
7	7	3
6	5	2
5	3	1
4	1	0

Table 12-202. Example of RX Configuration

RX DMA CHANNEL	Packet Priority	Switch Queue Priority
0	7	0
0	5	0
0	3	0
0	1	0

- ALE Configuration:
  - ALE in VLAN-ware mode, Non-ALE in bypass mode.

12.3.1.4.6.10 Ethernet MAC Sliver

The Ethernet port peripheral is compliant to the IEEE Std 802.3 Specification. Half-duplex mode is supported in 10/100 Mbps mode, but not in 1000 Mbps (gigabit) mode.

Features:

- Synchronous 10/100/1000 Mbit operation
- RMII/RGMII Interface
- Hardware Error handling including CRC
- Full-Duplex Gigabit operation (half-duplex gigabit is not supported)
- EtherStats and 802.3Stats RMON statistics gathering support for external statistics collection module
- Transmit CRC generation selectable on a per channel basis
- Emulation Support
- VLAN Aware Mode Support
- Hardware flow control
- Programmable Inter Packet Gap (IPG).

12.3.1.4.6.10.1 Ethernet MAC Sliver Overview

12.3.1.4.6.10.1.1 CRC Insertion

The MAC generates and appends a 32-bit Ethernet CRC onto the transmitted data, if the transmit packet header PASS_CRC bit is 0h. For the Ethernet port generated CRC case, a CRC at the end of the input packet data is not allowed.

If the header word PASS_CRC bit is set, then the last four bytes of the TX data are transmitted as the frame CRC. The four CRC data bytes should be the last four bytes of the frame and should be included in the packet byte count value. The MAC performs no error checking on the outgoing CRC when the PASS_CRC bit is set.

12.3.1.4.6.10.1.2 MTXER

The MTXER signal is only used for EEE. If an underflow condition occurs on a transmitted frame, the frame CRC will be inverted to indicate the error to the network. Underflow is a hardware error.

12.3.1.4.6.10.1.3 Adaptive Performance Optimization (APO)

The Ethernet MAC port incorporates Adaptive Performance Optimization (APO) logic that may be enabled by setting the TX_PACE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. Transmission pacing to enhance performance is enabled when set. Adaptive performance pacing introduces delays into the normal transmission of frames, delaying transmission attempts between stations, reducing the probability of collisions occurring during heavy traffic (as indicated by frame deferrals and collisions) thereby increasing the chance of successful transmission.

When a frame is deferred, suffers a single collision, multiple collisions or excessive collisions, the pacing counter is loaded with an initial value of 31. When a frame is transmitted successfully (without experiencing a deferral, single collision, multiple collision or excessive collision) the pacing counter is decremented by one, down to zero.

With pacing enabled, a new frame is permitted to immediately (after one IPG) attempt transmission only if the pacing counter is zero. If the pacing counter is non zero, the frame is delayed by the pacing delay, a delay of approximately four inter-packet gap delays. APO only affects the IPG preceding the first attempt at transmitting a frame. It does not affect the back-off algorithm for re-transmitted frames.

12.3.1.4.6.10.1.4 Inter-Packet-Gap Enforcement

The measurement reference for the IPG of 96-bit times is changed depending on frame traffic conditions. If a frame is successfully transmitted without collision, and MCRS is de-asserted within approximately 48-bit times of MTXEN being de-asserted, then 96-bit times is measured from MTXEN. If the frame suffered a collision, or if MCRS is not de-asserted until more than approximately 48-bit times after MTXEN is de-asserted, then 96-bit times (approximately, but not less) is measured from MCRS.

The Ethernet port transmit inter-packet gap (IPG) may be shortened by eight bit times when short gap is enabled and triggered. Setting the [10] TX_SHORT_GAP_ENABLE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register enables the gap to be shortened when triggered. The condition is triggered when the ports associated transmit packet FIFO has a user defined number of FIFO blocks used. The associated transmit FIFO blocks used value determines if the gap is shortened, and so on. The CPSW3_CPSW_NU_GAP_THRESH_REG register value determines the short gap threshold. If the FIFO blocks used is greater than or equal to the GAP_THRESH value then short gap is triggered.

12.3.1.4.6.10.1.5 Back Off

The Gigabit Ethernet Mac Sliver implements the 802.3 binary exponential back-off algorithm.

12.3.1.4.6.10.1.6 Programmable Transmit Inter-Packet Gap

The transmit inter-packet gap (IPG) is programmable through the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. The default value is decimal 12. The transmit IPG may be increased to the maximum value of 1FFh. Increasing the IPG is not compatible with transmit pacing. The short gap feature will override the increased gap value, so the short gap feature may not be compatible with an increased IPG.

12.3.1.4.6.10.1.7 Speed, Duplex and Pause Frame Support Negotiation

The Ethernet port can operate in half duplex or full duplex in 10/100 Mbit modes, and can operate in full duplex only in 1000 Mbit mode. Pause frame support is included in 10/100/1000 Mbit modes as configured by the host.

12.3.1.4.6.10.2 RMII Interface

The CPRMII peripheral is compliant to the RMII specification document.

12.3.1.4.6.10.2.1 Features

- Source Synchronous 10/100 Mbit operation
- Full and Half Duplex support

12.3.1.4.6.10.2.2 RMII Receive (RX)

The CPRMII receive (RX) interface converts the input data from the external RMII PHY (or switch) into the required MII (CPGMAC) signals. The carrier sense and collision signals are determined from the RMII input data stream and transmit inputs as defined in the RMII specification.

An asserted RMII_RXER on any di-bit in the received packet will cause an MII_RXER assertion to the CPGMAC during the packet. In 10Mbps mode, the error is not required to be duplicated on 10 successive clocks. Any di-bit which has an asserted RMII_RXER during any of the 10 replications of the data will cause the error to be propagated.

Any received packet that ends with an improper nibble boundary aligned RMII_CRS_DV toggle will issue an MII_RXER during the packet to the CPGMAC. Also, a change in speed or duplex mode during packet operations will cause packet corruption.

The CPRMII can accept receive packets with shortened preambles, but 0x55 followed by a 0x5D is the shortest preamble that will be recognized (1 preamble byte with the start of frame byte). At least one byte of preamble with the start of frame indicator is required to begin a packet. An asserted RMII_CRS_DV without at least a single correct preamble byte followed by the start of frame indicator will be ignored.

12.3.1.4.6.10.2.3 RMII Transmit (TX)

The CPRMII transmit (TX) interface converts the CPGMAC MII input data into the RMII transmit format. The data is then output to the external RMII PHY.

The CPGMAC does not source the transmit error (MII_TXERR) signal. Any transmit frame from the CPGMAC with an error (underrun) will be indicated as an error by an error CRC. Transmit error is assumed to be de-asserted at all times and is not an input into the CPRMII module. Zeroes are output on RMII_TXD[1:0] for each clock that RMII_TXEN is de-asserted.

12.3.1.4.6.10.3 RGMII Interface

The CPRGMII peripheral is compliant to the RGMII specification document.

12.3.1.4.6.10.3.1 Features

- Supports 1000/100/10 Mbps speed
- Full and Half Duplex support (CPGMAC supports only Full duplex in Gigabit mode).
- MII mode support
- Energy Efficient Ethernet Support

12.3.1.4.6.10.3.2 RGMII Receive (RX)

The CPRGMII receive (RX) interface converts the source synchronous DDR input data from the external RGMII PHY into the required G/MII (CPGMAC) signals.

12.3.1.4.6.10.3.3 In-Band Mode of Operation

The CPRGMII is operating in the in-band mode of operation when the RGMII_RX_INBAND input is asserted. RGMII_RX_INPUT is asserted by configuring the CTL_EN bit to 1h of the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. The link status, duplexity, and speed are determined from the RGMII input data stream RXD[3:0] when RX_CTL is deasserted, as defined in the RGMII specification. The PHY might need to be configured beforehand to output in-band data. The in-band data is indicated as shown in Table 12-203.

Table 12-203. In-Band Data

RXD3	RXD[2:1]		RXD0
Duplex status: 0h: half-duplex 1h: full-duplex	Link Speed: 0h: 10-Mbps mode 1h: 100-Mbps mode 2h: 1000-Mbps mode 3h: Reserved	RXC_CLK Speed: 2.5 MHz 25 MHz 125 MHz Reserved	Link Status: 0h: Link is down 1h: Link is up

12.3.1.4.6.10.3.4 Forced Mode of Operation

The CPRGMII is operating in the forced mode of operation when the RGMII_RX_INBAND input is deasserted by setting to 0h bit CTL_EN of the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register. In the forced mode of operation, the in-band data is ignored if present.
The link status is forced high, and the duplexity and speed are determined from the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[0] FULLDUPLEX and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[7] GIG bits. If bit [7] GIG = 1h, then CPRGMII is operating in Gigabit mode. If bit [7] GIG is cleared (0h), then CPRGMII is operating in 100 Mbps mode.

12.3.1.4.6.10.3.5 RGMII Transmit (TX)

The CPRGMII transmit (TX) interface converts the CPGMAC G/MII input data into the DDR RGMII format. The DDR data is then output to the external PHY.

The CPGMAC does not source the transmit error (TXERR) signal. Any transmit frame from the CPGMAC with an error (underrun) will be indicated as an error by an error CRC. Transmit error is assumed to be deasserted at all times and is not an input into the CPRGMII module.

In 10/100 Mbps mode, the TXD[7:0] data bus uses only the lower nibble. The CPRGMII will output the lower nibble twice in 10/100 Mbps mode to avoid unnecessary signal switching.

Packets will be precluded from transmission through the CPRGMII module for 4096 transmit clocks after the rising edge of RGMII_LINK. Packet transmission will begin on the first TX_CTL rising edge after the 4096 transmit clock count has expired.

12.3.1.4.6.10.4 Frame Classification

Received frames are proper (good) frames if they are between 64 and CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN in length (inclusive) and contain no errors (code/align/CRC).

Received frames are long frames if their frame count exceeds the value in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG/ CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG register. The register reset (default) value is 1518 (decimal). Long received frames are either oversized or jabber frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment errors are jabber frames.

Received frames are short frames if their frame count is less than 64 bytes. Short frames that contain no errors are undersized frames. Short frames with CRC, code, or alignment errors are fragment frames. If RX_CSF_EN bit in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG is set to 1h, undersized frames from 33 to 63 bytes will be forwarded only to the host on a best effort basis (meaning that the ALE may or may not be able to keep up with the packet rate and the short packet may be dropped due to bandwidth limitations). If RX_CSF_EN and RX_CEF_EN in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG are set, fragment frames from 33 to 63 bytes will also be forwarded only to the host on a best effort basis. Ethernet port received frames shorter than 33 bytes are dropped in all cases.

A received long packet will always contain RX_MAXLEN number of bytes transferred to memory (if CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[22]RX_CEF_EN = 1h). An example with RX_MAXLEN = 1518 is:

- If the frame length is 1518, then the packet is not a long packet and there will be 1518 bytes transferred to memory.
- If the frame length is 1519, there will be 1518 bytes transferred to memory. The last three bytes will be the first three CRC bytes.
- If the frame length is 1520, there will be 1518 bytes transferred to memory. The last two bytes will be the first two CRC bytes.
- If the frame length is 1521, there will be 1518 bytes transferred to memory. The last byte will be the first CRC byte.

If the frame length is 1522, there will be 1518 bytes transferred to memory. The last byte will be the last data byte.

12.3.1.4.6.10.5 Receive FIFO Architecture

This section describes the architecture of the Ethernet port's receive FIFOs. Internal to the Gigabit Ethernet switch, all Ethernet ports have an identical associated packet FIFO. Each transmit packet FIFO contains eight logical transmit queues (priority 0 through 7 with 7 the highest priority). Each transmit FIFO memory contains 81,920 bytes total organized as 2560 by 256-bit words. Each FIFO also contains a single memory for the receive queue. Each receive FIFO memory contains a total of 32768 bytes total organized as 1024 by 256-bit words.

12.3.1.4.6.11 Embedded Memories

Table 12-204. Embedded Memories

Memory Type Description	Number of Instances	
Single-port 3072-word × 64 RAM	1	(Combined FIFO RAM)
Single-port 128-word × 28-bit RAM	1	1 (EST)

12.3.1.4.6.12 Memory Error Detection and Correction

The CPSW_3G error detection and correction logic uses the ECC Aggregator Module.

The CPSW3_ECC_ECC_VECTOR register is used to select which ECC RAM's status and control registers are currently being read or written as shown in Table 12-205. The CPSW FIFO RAMs implement ECC only on packet headers. The packet data is protected by Ethernet CRC. The ALE and EST RAMs have complete ECC as normal.

Table 12-205. ECC RAM to CPSW RAM Mapping

ECC RAM Number	CPSW RAM
0	ALE RAM
1	Port 0 FIFO RAM

12.3.1.4.6.12.1 Packet Header ECC

Only packet headers bits are protected by ECC in the FIFO RAMs. The ECC_ERR_CTRL1[31-0] ECC_ROW bit is used to activate a row address where force single-bit error or force double-bit error needs to be applied. ECC_ERR_CTRL2 [15-0] ECC_BIT1 is implemented to determine which bit of the header is flipped for an SEC error when the ECC_CRC_MODE bit is cleared in the CPSW3_CONTROL_REG register. The ECC status registers return the RAM row address where the single or double-bit error has occured (ECC_ERR_STAT2[31-0] ECC_ROW) along with the bit position in the RAM data that is in error (ECC_ERR_STAT1[31-16] ECC_BIT1 value). Forcing double-bit errors in testing can cause indeterminate operation if multiple used packet header bits are flipped given that only single-bit errors are fixed by the ECC logic. Header bits 207 down to 200 are not currently used in the CPSW and may be used to test double bit errors without the possibility of requiring a reset for the switch to recover from the double bit error. No header bits are flipped when ECC_CRC_MODE is set to 1h. Either the RX_ECC_ERR_EN (enable receive ECC error operations) or the TX_ECC_ERR_EN (enable transmit ECC error operations) bits must be set in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register to test ECC header errors.

The header ECC code is stored in bits 255 down to 208. If any bit is flipped in the ECC code, the flipped bit will be corrected, but the index of the flipped bit will be reported as bit zero. This implies that when the aggregator reports that there is a SEC on bit 0, it can mean two things: either SEC on data bit 0 or SEC somewhere inside the ECC code. Any packet header with ECC error issues a pulse interrupt (ECC_PULSE_INTR) as does an ALE RAM ECC error.

12.3.1.4.6.12.2 Packet Protect CRC

Each packet received without error is passed through the CPSW_3G memories with a generated Ethernet protect CRC. The protect CRC is checked on egress for correctness and removed. If the CRC is correct (no RAM bit errors), then the packet is output with the selected port CRC type. If a protect CRC error is detected on host egress then the TXST_DROP signal will be asserted so that the packet is dropped to the host. If a protect CRC error is detected on Ethernet egress then the egress CRC will be generated on the packet and at least one byte of the CRC will be inverted on output. CRC memory protect errors do not assert the ECC_PULSE_INTR signal. CRC memory protect errors are counted in the associated port statistics registers and issue an interrupt on STAT_PEND_INTR if any CRC memory protect error occurs (and the statistics for that port are enabled). When the ECC_CRC_MODE bit in the CSL_CPSW3_CONTROL_REG register is set, the ECC_ERR_CTRL2 [15-0] ECC_BIT1 bit field will flip the associated column bit in any FIFO memory read operation, inducing a CRC protect error when the protect CRC is checked. No header bits are flipped when ECC_CRC_MODE is set. Either the RX_ECC_ERR_EN or the TX_ECC_ERR_EN bits must be set in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register to test packet CRC errors.

12.3.1.4.6.12.3 Aggregator RAM Control

The ECC logic for each FIFO RAM (receive and transmit) is divided into eight separate ECC encoders/decoders that encode/decode 26-bits of data each. Each of the 8 encoders (0 to 7) generates 6-bits of ECC code (48 code bits total), and each of the eight decoders (0 to 7) checks 6-bits of ECC code across the 26-bits of data (208 data bits total). The 48-bits of ECC code are passed through the RAM in the upper 48 unused bits in the header word. The header data bits and ECC code bits are shown in Table 12-206. The [15-0] ECC_BIT1 value returned on error is a 16-bit value that is the concatenation of 5 bits of zero, 3 bits of the encoder/decoder number (0 to 7), 3 bits of zero, and 5 bits of index into the indicated 26-bit encoder/decoder.

For example, an ECC_BIT1 value of 0x0308 is bit 8 of encoder/decoder 3, which is header bit 86 (that is, (26×3) + 8).

Table 12-206. ECC Submodule Header Data Bit to Encoder/Decoder Mapping

Header Data Bits	Encoder/Decoder
25:0	Encoder/Decoder 0 Data
51:26	Encoder/Decoder 1 Data
77:52	Encoder/Decoder 2 Data
103:52	Encoder/Decoder 3 Data
129:104	Encoder/Decoder 4 Data
155:130	Encoder/Decoder 5 Data
181:156	Encoder/Decoder 6 Data
207:182	Encoder/Decoder 7 Data
213:208	Encoder/Decoder 0 ECC
219:214	Encoder/Decoder 1 ECC
225:220	Encoder/Decoder 2 ECC
231:226	Encoder/Decoder 3 ECC
237:232	Encoder/Decoder 4 ECC
243:238	Encoder/Decoder 5 ECC
249:244	Encoder/Decoder 6 ECC
255:250	Encoder/Decoder 7 ECC

12.3.1.4.6.13 Ethernet Port Flow Control

The Ethernet port have flow control available for transmit and receive. Transmit flow control stops the Ethernet port from transmitting packets to the wire (switch egress) in response to a received pause frame. Transmit flow control does not depend on FIFO usage.

The Ethernet port have flow control available for receive operations (packet ingress). Ethernet port receive flow control is initiated when enabled and triggered. Packets received on an Ethernet port can be sent to the CPPI port. The destination port can trigger the receive Ethernet port flow control. An Ethernet destination port triggers another Ethernet receive flow control when the destination port is full.

When a packet is received on an Ethernet port interface with enabled flow control the below occurs:

- The packet will be sent to all ports that currently have room to take the entire packet.
- The packet will be retried until successful to all ports that indicate they don't have room for the packet.

The flow control trigger to the Ethernet port will be asserted until the packet has been sent, and there is room in the logical receive FIFO for packet runout from another flow control trigger (RX_BLK_CNT = 0h). Ethernet port receive flow control is disabled by default on reset. Ethernet port receive flow control requires that the RX_FLOW_EN bit in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG be set to 1h. When receive flow control is enabled on a port, the port's associated FIFO block allocation must be adjusted. The port RX allocation must increase from the default three blocks to accommodate the flow control runout. A corresponding decrease in the TX block allocation is required. If a sending port ignores a pause frame then packets may overrun on receive (and be dropped) but will not be dropped on transmit.

12.3.1.4.6.13.1 Ethernet Receive Flow Control

For every Ethernet port to be configured for fullduplex receive flow control, write a value of decimal 7 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG[7-0] RX_MAX_BLKS bit field, and a value of decimal 13 to the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAX_BLKS_REG[15-8] TX_MAX_BLKS register. This re-allocation allows for flow control runout on the receive FIFO at the expense of FIFO memory on the Ethernet transmit side. 10/100Mbps half-duplex collision based receive flow control does not need this re-allocation. Receive flow control is enabled by the RX_FLOW_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register.

12.3.1.4.6.13.1.1 Collision Based Receive Buffer Flow Control

Collision-based receive buffer flow control provides a means of preventing frame reception when the port is operating in half-duplex mode (FULLDUPLEX is cleared in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG). When receive flow control is enabled and triggered, the port will generate collisions for received frames. The jam sequence transmitted will be the twelve byte sequence C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3 (hex). The jam sequence will begin no later than approximately as the source address starts to be received. Note that these forced collisions will not be limited to a maximum of 16 consecutive collisions, and are independent of the normal back-off algorithm. Receive flow control does not depend on the value of the incoming frame destination address. A collision will be generated for any incoming packet, regardless of the destination address.

12.3.1.4.6.13.1.2 IEEE 802.3X Based Receive Flow Control

IEEE 802.3x based receive flow control provides a means of preventing frame reception when the port is operating in full-duplex mode (FULLDUPLEX bit is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register). When receive flow control is enabled and triggered, the port will transmit a pause frame to request that the sending station stop transmitting for the period indicated within the transmitted pause frame.

The Ethernet port will transmit a pause frame to the reserved multicast address at the first available opportunity (immediately if currently idle, or following the completion of the frame currently being transmitted). The pause frame will contain the maximum possible value for the pause time (FFFFh). The MAC will count the receive pause frame time (decrements FF00h down to 0) and retransmit an outgoing pause frame if the count reaches zero. When the flow control request is removed, the MAC will transmit a pause frame with a zero pause time to cancel the pause request.

Note that transmitted pause frames are only a request to the other end station to stop transmitting. Frames that are received during the pause interval will be received normally (provided the RX FIFO is not full at which time the receive FIFO will overrun and CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP[31-0] COUNT value will increment).

Pause frames will be transmitted if enabled and triggered regardless of whether or not the port is observing the pause time period from an incoming pause frame.

The Ethernet port will transmit pause frames as described below:

- The 48-bit reserved multicast destination address 01.80.C2.00.00.01.
- The 48-bit source address - from SL_SA[47-0] input.
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit pause time value FF.FF. A pause-quantum is 512 bit-times. Pause frames sent to cancel a pause request will have a pause time value of 00.00.
- Zero padding to 64-byte data length (The Ethernet port will transmit only 64 byte pause frames).
- The 32-bit frame-check sequence (CRC word).

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

If CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[3] RX_FLOW_EN is cleared to 0h while the pause time is nonzero, then the pause time will be cleared to 0h and a 0 count pause frame will be sent.

12.3.1.4.6.13.2 Flow Control Trigger

Receive flow control is triggered (when enabled), when the number of words in the receive FIFO is greater than or equal to the value writen in the CPSW_PN_RX_FLOW_THRESH_REG[8-0] COUNT bit field. The flow control packet runout is then contained in the remainder of the receive FIFO.

12.3.1.4.6.13.3 Ethernet Transmit Flow Control

Incoming pause frames are acted upon, when enabled, to prevent the Ethernet port from transmitting any further frames. Incoming pause frames are only acted upon when the [0] FULLDUPLEX and [4] TX_FLOW_EN bits in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register are set. Pause frames are not acted upon in half-duplex mode. Pause frame action will be taken if enabled, but normally the frame will be filtered and not transferred to memory. MAC control frames will be transferred to memory if the [24] RX_CMF_EN (RX Copy MAC Control Frames Enable) bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register is set. The [4] TX_FLOW_EN and [0] FULLDUPLEX bits effect whether or not MAC control frames are acted upon, but they have no effect upon whether or not MAC control frames are transferred to memory or filtered.

Pause frames are a subset of MAC Control Frames with an opcode field = 0001h. Incoming pause frames will only be acted upon by the port if:

- [4] TX_FLOW_EN is set in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register, and
- the RX maximum frame length is 64 bytes inclusive (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG[13-0] RX_MAXLEN), and
- the frame contains no CRC error or align/code errors.

The pause time value from valid frames will be extracted from the two bytes following the opcode. The pause time will be loaded into the port's transmit pause timer and the transmit pause time period will begin.

If a valid pause frame is received during the transmit pause time period of a previous transmit pause frame then:

- if the destination address is not equal to the reserved multicast address or any enabled or disabled unicast address, then the transmit pause timer will immediately expire, or
- if the new pause time value is zero then the transmit pause timer will immediately expire, else the port transmit pause timer will immediately be set to the new pause frame pause time value. (Any remaining pause time from the previous pause frame will be discarded).

If [4] TX_FLOW_EN in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register is cleared, then the pause-timer will immediately expire.

The port will not start the transmission of a new data frame any sooner than 512-bit times after a pause frame with a non-zero pause time has finished being received (MRXDV going inactive). No transmission will begin until the pause timer has expired (the port may transmit pause frames in order to initiate outgoing flow control). Any frame already in transmission when a pause frame is received will be completed and unaffected.

Incoming pause frames consist of the below:

- A 48-bit destination address equal to:
  - The reserved multicast destination address 01.80.C2.00.00.01, or the Ethernet port SL_SA [47:0] input.
- The 48-bit source address of the transmitting device.
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_TX_PAUSETIMER_REG[15-0] TX_PAUSETIMER. A pause-quantum is 512 bit-times.
- Padding to 64-byte data length.
- The 32-bit frame-check sequence (CRC word).

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

The padding is required to make up the frame to a minimum of 64 Bytes. The standard allows pause frames longer than 64 Bytes to be discarded or interpreted as valid pause frames. The Ethernet port will recognize any pause frame between 64 Bytes and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes in length.

12.3.1.4.6.14 Energy Efficient Ethernet Support (802.3az)

Energy Efficient Ethernet (EEE) allows the LPSC to turn off the module clock during inactive periods as determined by network and host traffic. The module can then be awakened by host queued transmit packet(s) or by a port's external Ethernet PHY. The module EEE clock stop interface is used by the external controller to control module EEE operations. EEE operations are configured as shown below:

1. The 12-bit EEE clock pre-scale value is written to the CPSW3_CPSW_NU_EEE_PRESCALE_REG register. The pre-scaler is used to clock all EEE-related counters
2. The port Idle to LPI count values (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IDLE2LPI_REG[23-0] COUNT) are written with the desired values
3. The port LPI to Wake count values (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_LPI2WAKE_REG[23-0] COUNT) are written with the desired values
4. The [0] EEE_EN bit is set in the switch CSL_CPSW3_CPSW_NU_CONTROL_REG register

EEE operation can begin after configuration. The host allows (through LPSC) the CPSW to enter a low power state by asserting the EEE_CLKSTOP_REQ signal. There are no requirements on host queues or traffic in order for the host to assert or de-assert EEE_CLKSTOP_REQ to the CPSW.

Each Ethernet port has a transmit and a receive LPI (low power indicate) state. The PHY indicates LPI by asserting MRXER with a MRXD[7:0] value of 0x01 while MRXDV is deasserted (inter-packet gap). The Ethernet transmit port indicates LPI after the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IDLE2LPI_REG value has been counted (the transmit port has gone idle for the configured amount of time). If another packet is received for transmit during the count then the count is restarted. When the transmit port has been idle for the Idle to LPI time, the transmit port enters the LPI state and indicates LPI to the associated PHY. The LPI is indicated to the external PHY by an asserted MTXER with a MTXD[7:0] while MTXEN is deasserted (inter-packet gap). The CPPI (port 0) LPI state includes transmit and receive. The CPPI LPI state is entered when the CPPI transmit and receive have both been idle for the Idle to LPI time (CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG). The Idle to LPI time value for all ports must be large relative to the switch latency to ensure that the count is not able to complete between successive packets.

Note

External PHY signaling has the following conditions:

- RGMII is a DDR interface. TXEN and TXER are the sampled values of TX_CTL at the rising and the falling TXC edges, respectively. RXDV and RXER are the sampled values of RX_CTL at the rising and the falling RXC clock edges, respectively
- In RMII mode, EEE is not supported.

When all transmit and receive ports are in the LPI state (CPSW LPI state), the EEE_CLKSTOP_ACK signal is asserted, and the LPSC is allowed to stop the module clock. When EEE_CLKSTOP_ACK is asserted, the clock may be turned on and off as desired by the host. The host is allowed to restart the clock, perform target read/write operations to the CPSW memory address space, and then turn off the clock again while EEE_CLKSTOP_ACK is asserted.

The software can remove and disable from re-entering the CPSW LPI state by restarting the module clock and then de-asserting EEE_CLKSTOP_REQ. There must be at least one rising edge of the clock before EEE_CLKSTOP_REQ is de-asserted. The module EEE_CLKSTOP_ACK output signal will be deasserted on the clock after the de-assertion of EEE_CLKSTOP_REQ. The host may queue CPPI receive packets at any time without regard to the CPSW module LPI state. The Host must deassert EEE_CLKSTOP_REQ on wakeup for a minimum of two clock periods. If EEE_CLKSTOP_REQ is deasserted for less than 5 clock periods for a wakeup event from the host to a particular Ethernet port (or visa versa), then the wakeup event will not cause the other Ethernet port port to awaken.

The external Ethernet PHY's can also wakeup the LPSC by removing the Ethernet receive LPI indication. If the CPSW module is in Idle state with EEE_CLKSTOP_ACK asserted and the receive LPI indication is removed, the EEE_CLKSTOP_WAKEUP signal will be asynchronously asserted. On wakeup, the LPSC restarts the clock and de-assert the EEE_CLKSTOP_REQ signal. The EEE_CLKSTOP_WAKEUP signal will be synchronously deasserted with EEE_CLKSTOP_ACK. Upon the deassertion of EEE_CLKSTOP_REQ, the Ethernet ports will count the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_LPI2WAKE_REG time for each port at which time the port is available for transmit.

12.3.1.4.6.15 Ethernet Switch Latency

When CPSW is configured as a store and forward switch, the switch latency is defined as the amount of time between the end of packet reception of the received packet to the start of the output packet transmit.

The store and forward latency is shown in Table 12-207:

Table 12-207. Switch Latency

Mode	Latency
Gig (1000)	880 ns
100	1.3 µs
10	6.5 µs

12.3.1.4.6.16 MAC Emulation Control

The emulation control input (EMUSUSP) and submodule emulation control registers allow CPSW operation to be completely or partially suspended. Each Ethernet port has associated emulation control registers (CPSW3_CPSW_NU_EM_CONTROL_REG and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_EMCONTROL_REG). The submodule emulation control registers must be accessed to facilitate CPSW emulation control. The CPSW module enters the emulation suspend state if all three submodules are configured for emulation suspend and the emulation suspend input is asserted. A partial emulation suspend state is entered if one or two submodules is configured for emulation suspend and the emulation suspend input is asserted. Emulation suspend occurs at packet boundaries. The emulation control feature is implemented for compatibility with other peripherals.

Ethernet port Emulation Control

The emulation control input (TBEMUSUP) and register bits (SOFT and FREE bits in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_EMCONTROL_REG register) allow Ethernet port operation to be suspended. When the emulation suspend state is entered, the Ethernet port will stop processing receive and transmit frames at the next frame boundary. Any frame currently in reception or transmission will be completed normally without suspension. For receive, frames that are detected by the Ethernet port after the suspend state is entered are ignored.

Table 12-208 shows the operations of the emulation control input and register bits.

Table 12-208. Emulation Control Input

EMUSUSP	SOFT	FREE	Description
0	X	X	Normal Operation
1	0	0	Normal Operation
1	1	0	Emulation Suspend
1	X	1	Normal Operation

12.3.1.4.6.17 MAC Command IDLE

The CMD_IDLE bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register allows MAC operation to be suspended. When the idle state is commanded, the MAC will stop processing receive and transmit frames at the next frame boundary. Any frame currently in reception or transmission will be completed normally without suspension. For transmission, any complete or partial frame in the TX cell FIFO will be transmitted. For receive, frames that are detected by the MAC after the suspend state is entered are ignored. No statistics will be kept for ignored frames. Commanded idle is similar in operation to emulation control and clock stop.

12.3.1.4.6.18 CPSW Network Statistics

The CPSW has a set of statistics that record events associated with frame traffic on selected switch ports. The statistics values are cleared to zero 38 clocks after the rising edge of CPSW0_RST. When one ore more port enable (Pn_STAT_EN) bits in the CPSW3_CPSW_NU_STAT_PORT_EN_REG register are set, all statistics registers are write to decrement. The value written will be subtracted from the register value with the result being stored in the register. If a value greater than the statistics value is written, then zero will be written to the register (writing 0xFFFF FFFF clears a statistics location). When all port enable bits are cleared to zero, all statistics registers are read/write (normal write direct, so writing 0x0000 0000 clears a statistics location). All write accesses must be 32-bit accesses.

The statistics interrupt (STAT_PEND0) will be issued if enabled when any statistics value is greater than or equal to 0x8000 0000. The statistics interrupt is removed by writing to decrement any statistics value greater than 0x8000 0000. The statistics are mapped into internal memory space and are 32-bits wide. All statistics rollover from 0xFFFF FFFF to 0x0000 0000.

Table 12-209 and Table 12-210 summarize network statistics.

12.3.1.4.6.18.1 Rx-only Statistics Descriptions

12.3.1.4.6.18.1.1 Good Rx Frames (Offset = 3A000h)

All ports

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.2 Broadcast Rx Frames (Offset = 3A004h)

All ports

The total number of good broadcast frames received on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for address FF.FF.FF.FF.FF.FF
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.3 Multicast Rx Frames (Offset = 3A008h)

All ports

The total number of good multicast frames received on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than FF.FF.FF.FF.FF.FF
- Had a length of 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.4 Pause Rx Frames (Offset = 3A00Ch)

Ethernet port N where N = 1 to 2

The total number of IEEE 802.3X pause frames received by the port (whether acted upon or not). Such a frame:

- Contained any unicast, broadcast, or multicast address
- Contained the length/type field value 88.08 (hex) and the opcode 0x0001
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error
- Pause-frames had been enabled on the port (TX_FLOW_EN = 1h).

The port could have been in either half or full-duplex mode.

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.5 Rx CRC Errors (Offset = 3A010h)

All ports

The total number of frames received on the port that experienced a CRC error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no code/align error
- Had a CRC error

Overruns have no effect upon this statistic.

A CRC error is defined to be:

- A frame containing an even number of nibbles, and
- Failing the Frame Check Sequence test.

12.3.1.4.6.18.1.6 Rx Align/Code Errors (Offset = 3A014h)

Ethernet port N where N = 1 to 2

The total number of frames received on the port that experienced an alignment error or code error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had either an alignment error, or a code error.

Overruns have no effect upon this statistic.

An alignment error is defined to be:

- A frame containing an odd number of nibbles
- Failing the Frame Check Sequence test if the final nibble is ignored

A code error is defined to be a frame which has been discarded because the port’s MRXER pin driven with a one for at least one bit-time’s duration at any point during the frame’s reception.

Note

RFC 1757 etherStatsCRCAlignErrors Ref. 1.5 can be calculated by summing Rx Align/Code Errors and Rx CRC errors.

12.3.1.4.6.18.1.7 Oversize Rx Frames (Offset = 3A018h)

All ports

The total number of oversized frames received on the port. An oversized frame is defined to be:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than RX_MAXLEN in bytes
- Had no CRC error, alignment error, or code error.

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.8 Rx Jabbers (Offset = 3A01Ch)

All ports

The total number of jabber frames received on the port. A jabber frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than RX_MAXLEN in bytes
- Had no CRC error, alignment error or code error

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.9 Undersize (Short) Rx Frames (Offset = 3A020h)

All ports

The total number of undersized frames received on the port. An undersized frame is defined to be:

- Was any data frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was less than 64 bytes
- Had no CRC error, alignment error, or code error

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.10 Rx Fragments (Offset = 3A024h)

Ethernet port N where N = 1 to 2

The total number of frame fragments received on the port. A frame fragment is defined to be:

- Any data frame (address matching does not matter)
- Less than 64 bytes long
- Having a CRC error, an alignment error, or a code error
- Not the result of a collision caused by half-duplex, collision-based flow control

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.11 RX IPG Error (Offset = 3A05Ch)

The total number of 10G frames received on a port that had a correct preamble but did not have at least five bytes of IDLE preceding the frame. This does not indicate if the frame with the IPG error was kept or ignored.

12.3.1.4.6.18.1.12 ALE Drop (Offset = 3A028h)

All ports

The total number of frames received on a port such that the destination address was not equal to the source address and the packet was not destined to the port it was received on, but the frame was not forwarded to any port (the PORT_MASK was zero).

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the destination address was not equal to the source address
- the packet was not destined for the port it was receive on
- had a zero PORT_MASK

12.3.1.4.6.18.1.13 ALE Overrun Drop (Offset = 3A02Ch)

All ports (non cut-thru mode)

The total number of frames received on a port that were dropped (zero PORT_MASK) due to exceeding the maximum ALE lookup rate (Port 0 should not have ALE Overrun Drops because the ingress rate is controlled to prevent it). This statistic should be zero and when non-zero indicates a system clock issue or indicates that short packets were sent with RX_CSF_EN at a rate that exceeded the maximum lookup rate.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- The port has no receive priorities enabled for cut-thru, and
- the maximum ALE lookup rate was exceeded so the lookup was aborted and the packet was dropped.

Ethernet Ports (cut-thru mode)

The total number of received frames on a port that were dropped due to packet errors. This statistic does not count error frames that are sent to the host with a set CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[22] RX_CEF_EN or CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG[24] RX_CMF_EN.

- was any data or MAC control frame, and
- the port has at least one receive priority enabled for cut thru, and
- the received packet was long, mac_control, code, align, crc error, and
- was dropped on receive (not transferred to the host due to error enable bits).

12.3.1.4.6.18.1.14 Rx Octets (Offset = 3A030h)

All ports

The total number of bytes in all good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the Section 12.3.1.4.6.18.1.6, *Rx Align/Code Errors* and Section 12.3.1.4.6.18.1.5, *Rx CRC errors* statistic descriptions for definitions of alignment, code and CRC errors.

Overruns have no effect upon this statistic.

12.3.1.4.6.18.1.15 Rx Bottom of FIFO Drop (Offset = 3A084h)

Ethernet port N where N = 1 to 2

The total number of frames received on a port that overran the port's receive FIFO and were dropped (bottom of receive FIFO). Port 0 (CPPI receive port) should not drop packets on receive because port 0 receive flow control should be enabled. The Ethernet ports will only drop packets in the receive FIFO when receive flow control is enabled and the sending port ignores sent pause frame and then overruns the receive FIFO. An overrun frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- Was dropped on port 0 due to a lack of memory space in the receive FIFO.

Note

This statistic should be zero if proper flow control is being followed.

Host port 0

This statistic also counts frames dropped on port 0 that were 17 to 63 bytes (only for port 0). For Ethernet ports, the drop count for frames shorter than 33 bytes is included in the undersized or fragment count. Port 0 simply gives an indication that a packet was dropped. No other statistics are counted for frames shorter than 33 bytes.

12.3.1.4.6.18.1.16 Portmask Drop (Offset = 3A088h)

All ports

The total number of frames received on a port that were dropped by the ALE (the ALE did not forward the packet to any port). Port mask drop frame is defined to be:

- Any data or MAC control frame
- Any length greater than 32 bytes
- Was dropped by the ALE due to PORT_MASK=0 (was not sent to any destination port)
- Was not a long or error packet with the port in cut-thru mode
- The frame could have been dropped due to error or other counted reason, so it could be counted elsewhere also.

Note

This statistic does not count in the overall total as it includes every packet received greater than 32 bytes that had a zero PORT_MASK.

12.3.1.4.6.18.1.17 Rx Top of FIFO Drop (Offset = 3A08Ch)

All ports

The total number of frames received on a port that had a start-of-frame (SOF) overrun on any destination port egress (when attempting to load the packet from the top of the ingress port receive FIFO into any other port’s transmit FIFO). If a multicast/broadcast packet is dropped by multiple destination ports then this statistic will increment by the number of ports that dropped the packet. Rx Top Of FIFO Drop is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error or code error
- had a SOF of frame overrun on another port egress.

12.3.1.4.6.18.1.18 ALE Rate Limit Drop (Offset = 3A090h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to receive rate limiting on this port or due to transmit rate limiting on any destination port (not sent to all expected destination ports if transmit rate limiting).

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the receive rate was exceeded and the packet was dropped, or the transmit rate was exceeded to any destination port and the packet was dropped to one or more expected destination ports (indicates that the destinations were reduced due to rate limiting).

12.3.1.4.6.18.1.19 ALE VLAN Ingress Check Drop (Offset = 3A094h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to VLAN ingress check failure.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the VLAN ID ingress check failed (the receive port was not in the group)
- The address lookup did not return a match with the SUPER bit set.

12.3.1.4.6.18.1.19.1 ALE DA=SA Drop (Offset = 3A098h)

All ports

The total number of frames received on a port that were dropped (zero PORT_MASK) due to destination address equal to source address.

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error
- the destination address was equal to the source address
- the source address was not an entry in the table.

12.3.1.4.6.18.1.19.2 Block Address Drop (Offset = 3A09Ch)

The total number of frames received on a port that were dropped (zero PORT_MASK) due to the destination or source address being blocked.

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error, and
- the source or destination address matched a table entry with the block bit set.

12.3.1.4.6.18.1.19.3 ALE Secure Drop (Offset = 3A0A0h)

The total number of frames received on a port that were dropped (zero port_mask) due to a secure violation (the source address is owned by a different receive port).

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error, and
- the source address is an entry in the table with the SECURE bit set and a port number for a different receive port.

12.3.1.4.6.18.1.19.4 ALE Authentication Drop (Offset = 3A0A4h)

The total number of frames received on a port that were dropped (zero port_mask) due to authentication failure.

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)
- had no CRC error, alignment error, or code error, and
- CPSW3_CPSW_NU_ALE_ALE_CONTROL[1] ENABLE_AUTH_MODE is set to 1h, and
- the source address is not equal to the destination address, and
- the source address is not a table entry, and
- the destination address is not a table entry with the SUPER bit set.

12.3.1.4.6.18.1.19.5 ALE Unknown Unicast (Offset = 3A0A8h)

All ports

The total number of frames received on a port that had a unicast destination address with an unknown source address.

- was any data frame with a unicast destination address
- the source address was not a table entry
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

Note: The ALE Unknown Unicast Bytecount statistic is the number of bytes contained in the ALE Unknown Unicast frames.

12.3.1.4.6.18.1.19.6 ALE Unknown Unicast Bytecount (Offset = 3A0ACh)

The total number of bytes received on a port that had a unicast destination address with an unknown source address.

12.3.1.4.6.18.1.19.7 ALE Unknown Multicast (Offset = 3A0B0h)

The total number of frames received on a port that had a multicast destination address with an unknown source address. The frame is defined to be:

- was any data frame with a unicast destination address
- the source address was not a table entry, and
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error or code error

Note: The ALE Unknown Multicast Bytecount statistic is the number of bytes contained in the ALE Unknown Multicast frames.

12.3.1.4.6.18.1.19.8 ALE Unknown Multicast Bytecount (Offset = 3A0B4h)

The total number of bytes received on a port that had a multicast destination address with an unknown source address.

12.3.1.4.6.18.1.19.9 ALE Unknown Broadcast (Offset = 3A0B8h)

The total number of frames received on a port that had a broadcast destination address with an unknown source address. The frame is defined to be:

- was any data frame with a unicast destination address
- the source address was not a table entry, and
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error or code error

Note: The ALE Unknown Broadcast Bytecount statistic is the number of bytes contained in the ALE Unknown Broadcast frames.

12.3.1.4.6.18.1.19.10 ALE Unknown Broadcast Bytecount (Offset = 3A0BCh)

The total number of bytes received on a port that had a broadcast destination address with an unknown source address.

12.3.1.4.6.18.1.19.11 ALE Policer/Classifier Match (Offset = 3A0C0h)

All ports

The total number of frames received on a port that matched a policer. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.3.1.4.6.18.2 ALE Policer Match Red (Offset = 3A0C4h)

The total number of frames received on a port that had matched a policer and the condition was red. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.3.1.4.6.18.3 ALE Policer Match Yellow (Offset = 3A0C8h)

The total number of frames received on a port that had matched a policer and the condition was red. The frame is defined to be:

- was any data frame
- matched a condition on a policer,
- was of length 64 to RX_MAXLEN bytes inclusive
- had no CRC error, alignment error, or code error

12.3.1.4.6.18.4 IET Receive Assembly Error (Offset = 3A140h)

The total number of premptable received frames with IET assembly errors.

- any frame received
- was any size, and
- was a non-initial fragment that mismatched the frame count or fragment count (went to the assembly error state in the IET receive state machine)

12.3.1.4.6.18.5 IET Receive Assembly OK (Offset = 3A144h)

The total number of correctly received and re-assembled premptable frames.

- any premptable frame received
- was any size, and
- was correctly received and re-assembled without error

12.3.1.4.6.18.6 IET Receive SMD Error (Offset = 3A148h)

The total number of received frames rejected due to an unknown SMD value or received frames rejected with an SMD-C when no frame is in progress.

- any frame received
- was any size, and
- was rejected because of an unknown SMD value or SMD-C with no frame in progress.

Note: If IET_ENABLE is not set, this statistic counts any received frame with any non express SMD.

12.3.1.4.6.18.7 IET Receive Merge Fragment Count (Offset = 3A14Ch)

The total number of received non-initial fragments that did not have an assembly error. The IET stat CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_k is derived by adding the Receive Assembly Error count to this value.

- any frame received
- was any size, and
- was a non-initial fragment that did not contain an assembly error

12.3.1.4.6.18.8 Rx Cut Thru with No Delay

The total number of frames received on the port and subsequently sent cut-thru to all internal destination port FIFOs with no delay. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port to all destination ports without delay.

12.3.1.4.6.18.9 Rx Cut Thru with Delay

The total number of frames received on the port and subsequently sent cut-thru to all destination ports with some amount of delay. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port to all destination ports with some amount of delay.

12.3.1.4.6.18.10 Rx Cut Thru Store-and-Forward

The total number of frames received on the port were attempted to be sent cut-thru to all destination ports but were held off due to configuration or traffic conditions. Such a frame:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was attempted to be sent cut-thru by the receive port to all destination ports but was sent store-and-forward.

12.3.1.4.6.18.11 Tx-only Statistics Descriptions

The maximum and minimum transmit frame size is software controllable.

12.3.1.4.6.18.11.1 Good Tx Frames (Offset = 3A034h)

All ports

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

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Note

A nonzero CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_k value should be subtracted from this value to obtain the actual good frames value (the good frames statistic also increments on a transmitted CRC error).

12.3.1.4.6.18.11.2 Broadcast Tx Frames (Offset = 3A038h)

All ports

The total number of good broadcast frames transmitted on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address FF.FF.FF.FF.FF.FF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

12.3.1.4.6.18.11.3 Multicast Tx Frames (Offset = 3A03Ch)

All ports

The total number of good multicast frames transmitted on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than FF.FF.FF.FF.FF.FF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

12.3.1.4.6.18.11.4 Pause Tx Frames (Offset = 3A040h)

Ethernet port N where N = 1 to 2

This statistic indicates the number of IEEE 802.3X pause frames transmitted by the port.

Pause frames cannot contain a CRC error because they are created in the transmitting MAC, so these error conditions have no effect upon the statistic. Pause frames sent by software will not be included in this count.

Since pause frames are only transmitted in full duplex, carrier loss and collisions have no effect upon this statistic.

Transmitted pause frames are always 64-byte multicast frames so will appear in the *Tx Multicast Frames* and *64octet Frames* statistics.

12.3.1.4.6.18.11.5 Deferred Tx Frames (Offset = 3A044h)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that first experienced deferment. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced no collisions before being successfully transmitted
- Found the medium busy when transmission was first attempted, so had to wait.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.6 Collisions (Offset = 3A048h)

Ethernet port N where N = 1 to 2

This statistic records the total number of times that the port experienced a collision. Collisions occur under two circumstances.

1. When a transmit data or MAC control frame:
   - Was destined for any unicast, broadcast or multicast address
   - Was any size
   - Had no carrier loss and no underrun
   - Experienced a collision. A jam sequence is sent for every non-late collision, so this statistic will increment on each occasion if a frame experiences multiple collisions (and increments on late collisions)

   CRC errors have no effect upon this statistic.
2. When the port is in half-duplex mode, flow control is active, and a frame reception begins.

12.3.1.4.6.18.11.7 Single Collision Tx Frames (Offset = 3A04Ch)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that experienced exactly one collision. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced one collision before successful transmission. The collision was not late.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.8 Multiple Collision Tx Frames (Offset = 3A050h)

Ethernet port N where N = 1 to 2

The total number of frames transmitted on the port that experienced multiple collisions. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 2 to 15 collisions before being successfully transmitted. None of the collisions were late.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.9 Excessive Collisions (Offset = 3A054h)

Ethernet port N where N = 1 to 2

The total number of frames for which transmission was abandoned due to excessive collisions. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 16 collisions before abandoning all attempts at transmitting the frame. None of the collisions were late.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.10 Late Collisions (Offset = 3A058h)

Ethernet port N where N = 1 to 2

The total number of frames on the port for which transmission was abandoned because they experienced a late collision. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Experienced a collision later than 512 bit-times into the transmission. There may have been up to 15 previous (non-late) collisions which had previously required the transmission to be re-attempted. The *Late Collisions* statistic dominates over the single-, multiple- , and excessive- collision statistics. If a late collision occurs, the frame will not be counted in any of these other three statistics.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.11 Carrier Sense Errors (Offset = 3A060h)

Ethernet port N where N = 1 to 2

The total number of frames on the port that experienced carrier loss. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- The carrier sense condition was lost or never asserted when transmitting the frame (the frame is not retransmitted). This is a transmit only statistic. Carrier Sense is a don’t care for received frames. Transmit frames with carrier sense errors are sent until completion and are not aborted.

CRC errors have no effect upon this statistic.

12.3.1.4.6.18.11.12 Tx Octets (Offset = 3A064h)

All ports

The total number of bytes in all good frames transmitted on the port. A good frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Was any size
- Had no late or excessive collisions, no carrier loss and no underrun.

12.3.1.4.6.18.11.13 Transmit Priority 0-7 (Offset = 3A180h to 3A1A8h)

The total number of frames transmitted on the port from transmit FIFO priority 0-7. Collision retries do not affect this statistic. Pause frames do not affect this statistic.

- Any frame transmitted from priority 0-7, and
- Was less than or equal to CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG to CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG
- Collision retries are not counted in this statistic.
- Pause frames are not counted in this statistic.
- Carrier sense errors do not affect this statistic.

Note: The Transmit Priority 0-7 Bytecount statistic is the number of bytes contained in the frames of the Transmit Priority 0-7 statistic.

12.3.1.4.6.18.11.14 Transmit Priority 0-7 Drop (Offset = 3A1C0h to 3A1E8)

The total number of transmit frames on the port that overran the transmit FIFO priority 0-7 and were dropped. This count includes frames dropped due to CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG to CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG.

- Any frame destined to be transmitted from priority 0-7, and
- Was any size, and
- Was dropped due to priority 0-7 FIFO overrun (Start of packet overrun).
- Was dropped due to frame size larger than CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG to CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG.

Note: The Transmit Priority 0-7 Drop Bytecount statistic is the number of bytes contained in the frames of the Transmit Priority 0-7 Drop statistic.

12.3.1.4.6.18.11.15 Tx Memory Protect Errors (Offset = 3A17Ch)

All ports

The total number of transmit frames on the port that had a memory protect CRC error on egress:

- Any frame destined to be transmitted,
- Was any size
- Had a memory protect CRC error on egress.

Note

1. Frames to the host with memory protect errors are dropped via TXST_DROP. Ethernet frames will have at least one byte of the generated port type CRC inverted on egress.
2. This statistic is 8-bits wide only and will not rollover but will limit at 0xFF.
3. A non-zero value in this statistic will issue a STAT_PEND0 interrupt for the associated port.

12.3.1.4.6.18.11.16 IET Transmit Merge Hold Count (Offset = 3A150h)

The total number of premptable frames that were prempted and reassembled by the assertion of MAC_HOLD in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_IET_CONTROL_REG register or were prempted by Enhanced Scheduled Traffic (EST). The IET statistic can be derived and maintained by software.

- Any frame destined to be transmitted on the premptable port, and
- was any size, and
- was prempted by the assertion of MAC_HOLD.
- was prempted by Enhanced Scheduled Traffic (EST).

12.3.1.4.6.18.11.17 IET Transmit Merge Fragment Count (Offset = 3A14Ch)

The total number of non-initial premptable transmit fragments on premptable transmit.

- Any frame destined to be transmitted on the premptable port, and
- Was any size, and
- was a non-initial fragment.

12.3.1.4.6.18.11.18 Tx CRC Errors

The total number of frames transmitted on the port with a CRC error. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size, and
- was sent cut-thru by the receive port and was received with a CRC error, or
- was a transmitted frame that also had a memory protect error (counted also in CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_k).

Note

For port0 this statistics location (CPSW_STAT0_TXDROP) counts the number of drops to the host due to a memory protect error, or due to a cut-thru packet having an error on reception but was forwarded with the error. The Ethernet port receive error could be long, CRC, jabber, or code. For Ethernet ports, the receive error could be the same but the packet is transmitted with at least one byte of the actual outgoing packet CRC inverted to indicate the error.

Note

A nonzero CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_k value should be subtracted from the CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_k value to obtain the actual good frames value (the good frames statistic also increments on a transmitted CRC error).

12.3.1.4.6.18.11.19 Tx Cut Thru

The total number of cut-thru frames transmitted on the port with or without delay. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port.
- was transmitted cut-thru with or without delay.

12.3.1.4.6.18.11.20 Tx Cut Thru Store-and-Forward

The total number of cut-thru frames transmitted store and forward. Such a frame:

- was any data frame destined for any unicast, broadcast or multicast address, and
- was any size greater than or equal to 128 bytes, and
- was sent cut-thru by the receive port.
- was transmitted store-and-forward due to traffic congestion.

12.3.1.4.6.18.12 Rx- and Tx (Shared) Statistics Descriptions

12.3.1.4.6.18.12.1 Rx + Tx 64 Octet Frames (Offset = 3A068h)

All ports

The total number of 64-byte frames received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was exactly 64 bytes long. (If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic).

CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.2 Rx + Tx 65–127 Octet Frames (Offset = 3A06Ch)

All ports

The total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 65 to 127 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.3 Rx + Tx 128–255 Octet Frames (Offset = 3A070h)

All ports

The total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 128 to 255 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.4 Rx + Tx 256–511 Octet Frames (Offset = 3A074h)

All ports

The total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 256 to 511 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.5 Rx + Tx 512–1023 Octet Frames (Offset = 3A078h)

All ports

The total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 512 to 1023 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.6 Rx + Tx 1024_Up Octet Frames (Offset = 3A07Ch)

All ports

The total number of frames of size 1024 to RX_MAXLEN bytes for receive or 1024 up for transmit on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 1024 to RX_MAXLEN bytes long on receive, or any size on transmit

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

12.3.1.4.6.18.12.7 Net Octets (Offset = 3A080h)

All ports

The total number of bytes of frame data received and transmitted on the port. Each frame counted:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address (address match does not matter)
- Any length (including less than 64 bytes and greater than RX_MAXLEN bytes)

Also counted in this statistic is:

- Every byte transmitted before a carrier-loss was experienced
- Every byte transmitted before each collision was experienced, (that is, multiple retries are counted each time)
- Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting)

Error conditions such as alignment errors, CRC errors, code errors, overruns and underruns do not affect the recording of bytes by this statistic.

The objective of this statistic is to give a reasonable indication of Ethernet utilization.

12.3.1.4.6.18.13

Table 12-209. Rx Statistics Summary

Rx Statistic	Frame/Oct	Rx/Rx+Tx	Frame Type					Frame Size (bytes)								Event				
			MAC control		Data[5]															
			Pause frame	Non-pause[4]	Multicast	Broadcast	Unicast	<64	64	65-127	128-255	256-511	512-1023	1024-rx_max len	>rx_max len	Flow Coll.[8]	CRC Error	Align/Code	Overrun	Addr. Disc.
Good Rx Frames	F	Rx	(y|[1]	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-[2]	n	n	-	n
Broadcast Rx Frames	F	Rx	(%|[6]	%|	n	y)	n	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	n
Multicast Rx Frames	F	Rx	(%|	%|	y)	n	n	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	n
Pause Rx Frames	F	Rx	y	n	n	n	n	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	-
Rx CRC Errors	F	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	y	n	-	n
Rx Align/Code Errors	F	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	-	y	-	n
Oversized Rx Frames	F	Rx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	n	y	-	n	n	-	n
Rx Jabbers	F	Rx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	n	y	-	(y|	y)	-	n
Undersized Rx Frames	F	Rx	n	n	(y|	y|	y)	y	n	n	n	n	n	n	n	-	n	n	-	n
Rx Fragments	F	Rx	n	n	(y|	y|	y)	y^[7]	n	n	n	n	n	n	n	-	(y|	y)	-	-
Rx Overruns[9]	F	Rx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y|	y)	-	-	-	y	n
64octet Frames	F	Rx+Tx[3]	(y|	y|	y|	y|	y)	n	y	n	n	n	n	n	n	-	-	-	-	n
65-127octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	y	n	n	n	n	n	-	-	-	-	n
128-255octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	y	n	n	n	n	-	-	-	-	n
256-511octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	y	n	n	n	-	-	-	-	n
512-1023octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	y	n	n	-	-	-	-	n
1024-UPoctet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	n	y	n	-	-	-	-	n
Rx Octets	O	Rx	(y|	y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	n	-	n	n	-	n
Net Octets	O	Rx+Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y|	y|	y)	-	-	-	-

(1) "AND" is assumed horizontally across the table between all conditions which form the statistic (marked y or n) except where (y|y), meaning "OR" is indicated. Parentheses are significant.
(2) "-" indicates conditions which are ignored in the formations of the statistic.
(3) Statistics marked "Rx+Tx" are formed by summing the Rx and Tx statistics, each of which is formed independently.
(4) The non-pause column refers to all MAC control frames (for example, frames with length/type=88.08) with opcodes other than 0x0001. The pauseframe column refers to MAC frames with the opcode=0x0001.
(5) The multicast, broadcast and unicast columns in the table refer to non-MAC Control/non-pause frames (i.e. data frames).
(6) "%" If either a MAC control frame or pause frame has a multicast or broadcast destination address then the appropriate statistics will be updated.
(7) "y^" Frame fragments are not counted if less than 8 bytes.
(8) Flow coll. are half-duplex collisions forced by the MAC to achieve flow-control. A collision will be forced during the first 8 bytes so should not show in frame fragments. Some of the '-'s in this column might in reality be 'n's.
(9) The rx_overruns stat is for RX_MOF_OVERRUNS and RX_SOF_OVERRUNS added together.

Table 12-210. Tx Statistics Summary

Tx Statistic(9)	Frame/ Oct	Tx/ Rx +Tx	Frame Type					Frame Size (bytes)							Event									
			MAC control(4)		Data											Collision Type								
			Pause-MAC	Any-CPU	Multicast	Broadcast	Unicast	64	65-127	128-255	256-511	512-1023	1024-1535	>1535	CRC Error	Flow(8)	1	2-15	16	Late	No Carrier	Queued	Deferred	Underrun
Good Tx Frames	F	Tx	(y|(1)	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-(2)	-	-	-	n	n	n	-	-	n
Broadcast Tx Frames	F	Tx	n	(%|(5)	n	y)	n	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Multicast Tx Frames	F	Tx	(y|	%|	y)	n	n	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Pause Tx Frames	F	Tx	y	n	n	n	n	y	n	n	n	n	n	n	-	-	-	-	-	-	-	-	-	-
Collisions	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	(+(6)	+	+	+	+)	n	-	-	-
Single Collision Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	y	n	n	n	n	-	-	-
Multiple Collision Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	y	n	n	n	-	-	-
Excessive Collisions	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	n	y	n	n	-	-	-
Late Collisions	F	Tx	n	(y|	y|	y|	y)	n	(y|	y|	y|	y|	y|	y)	-	-	-	-	-	y	-	-	-	-
Deferred Tx Frames	F	Tx	n	(y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	n	n	n	n	n	-	y	n
Carrier Sense Errors	F	Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	-	-	y	-	-	-
64octet Frames	F	Rx+Tx(3)	(y|	y|	y|	y|	y)	y	n	n	n	n	n	n	-	-	-	-	n	n	n	-	-	-
65-127octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	y	n	n	n	n	n	-	-	-	-	n	n	n	-	-	-
128-255octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	y	n	n	n	n	-	-	-	-	n	n	n	-	-	-
256-511octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	y	n	n	n	-	-	-	-	n	n	n	-	-	-
512-1023octet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	y	n	n	-	-	-	-	n	n	n	-	-	-
1024-UPoctet Frames	F	Rx+Tx	(y|	y|	y|	y|	y)	n	n	n	n	n	y	y	-	-	-	-	n	n	n	-	-	-
Tx Octets	O	Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	-	-	n	n	n	-	-	n
Net Octets	O	Rx+Tx	(y|	y|	y|	y|	y)	(y|	y|	y|	y|	y|	y|	y)	-	-	$(7)	$	$	$	$	-	-	-

(1) "AND" is assumed horizontally across the table between all conditions which form the statistic (marked y or n) except where (y|y), meaning “OR” is indicated. Parentheses are significant.
(2) “-“ indicates conditions which are ignored in the formations of the statistic.
(3) Statistics marked “Rx+Tx” are formed by summing the Rx and Tx statistics, each of which is formed independently.
(4) Pause (MAC) frames are issued in the MAC as perfect (no CRC error) 64 byte frames in full duplex only, so they cannot collide.
(5) “%” If a CPU sourced MAC control frame has a multicast or broadcast destination address then the appropriate statistics will be updated.
(6) “+” indicates collisions which are “summed” (i.e. every collision is counted in the Collisions statistic). Jam sequences used for halfduplex flow control are also counted.

(7) “$” Every byte written on the wire during each retry attempt is also counted in addition to frames which experience no collisions or carrier loss.

(8) The flow collision type is for half-duplex collisions forced by the MAC to achieve flow control. Some of the ‘-‘s in this column might in reality be ‘n’s. To prevent double-counting, Net Octets are unaffected by the jam sequence – the ‘received’ bytes, however, are counted. (See Table 12-209.)

(9) When the transmit Tx FIFO is drained due to the MAC being disabled or link being lost, then the frames being purged will not appear in the Tx statistics.

12.3.1.4.7 Common Platform Time Sync (CPTS)

The Common Platform Time Sync (CPTS) module is used to facilitate host control of time sync operations. It enables compliance with the IEEE 1588-2008 standard for a precision clock synchronization protocol.

Main features of CPTS module are:

- Supports the selection of multiple external clock sources
- Software control of time sync events via interrupt or polling
- Supports up to 8 hardware timestamp push inputs
- Supports timestamp counter compare output (CPTS_COMP)
- Supports timestamp counter bit output (CPTS_SYNC)
- Supports a configurable number of timestamp Generator bit outputs (CPTS_GENFn).
- Supports Ethernet Enhanced Scheduled Traffic Operations (CPTS_ESTFn).
- 32-bit and 64-bit timestamp modes with PPM and nudge adjustment.

12.3.1.4.7.1 CPSW0 CPTS Integration

This section describes CPTS module integration in the CPSW0 module, including information about clocks, resets, and hardware requests.

Figure 12-157 shows CPTS integration in the device CPSW0 module.

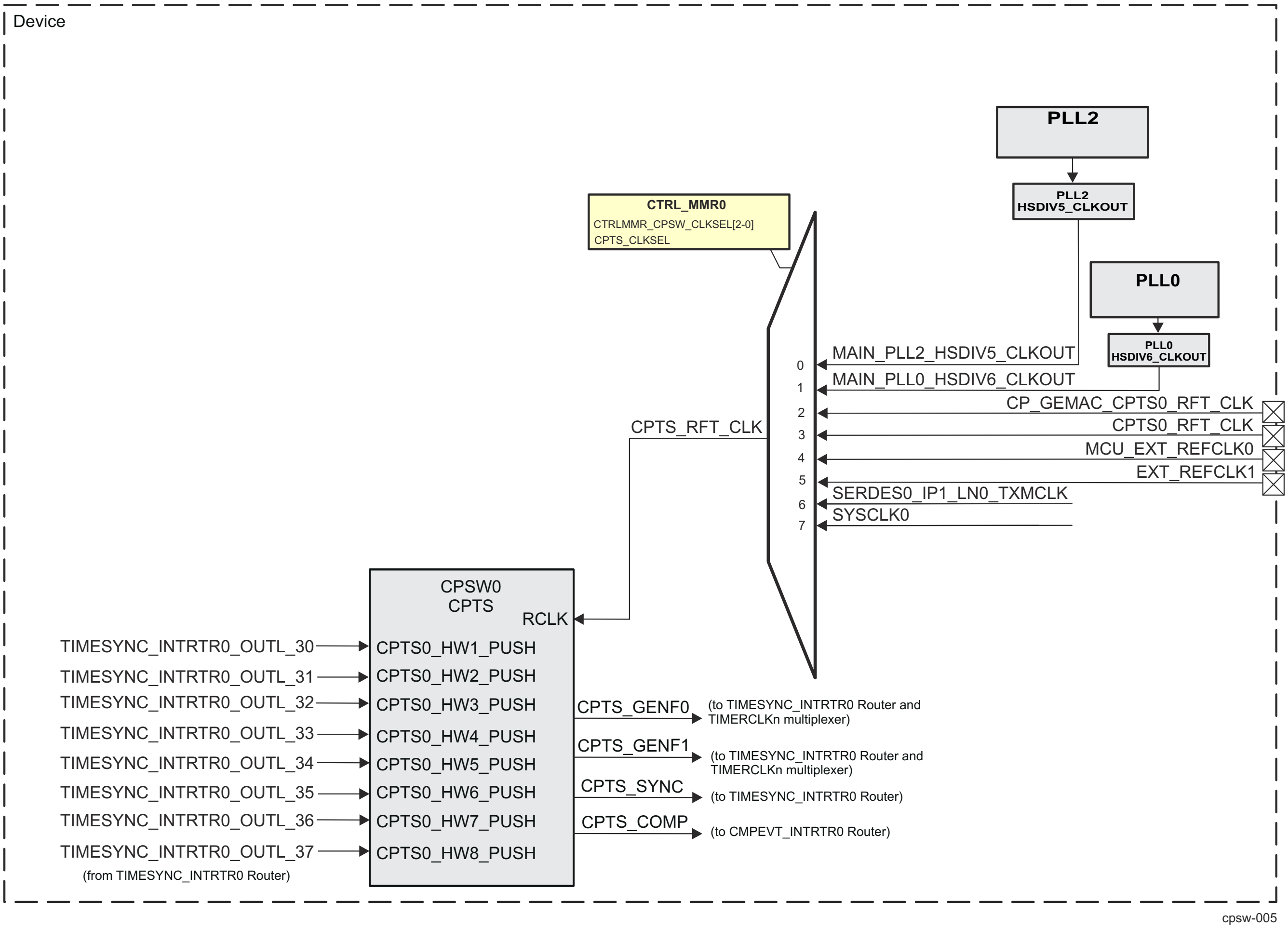


Figure 12-157. CPSW0 CPTS Integration

CPTS IEEE 1588 clock (RCLK) is selected through the CPTS_CLKSEL bit.

Note

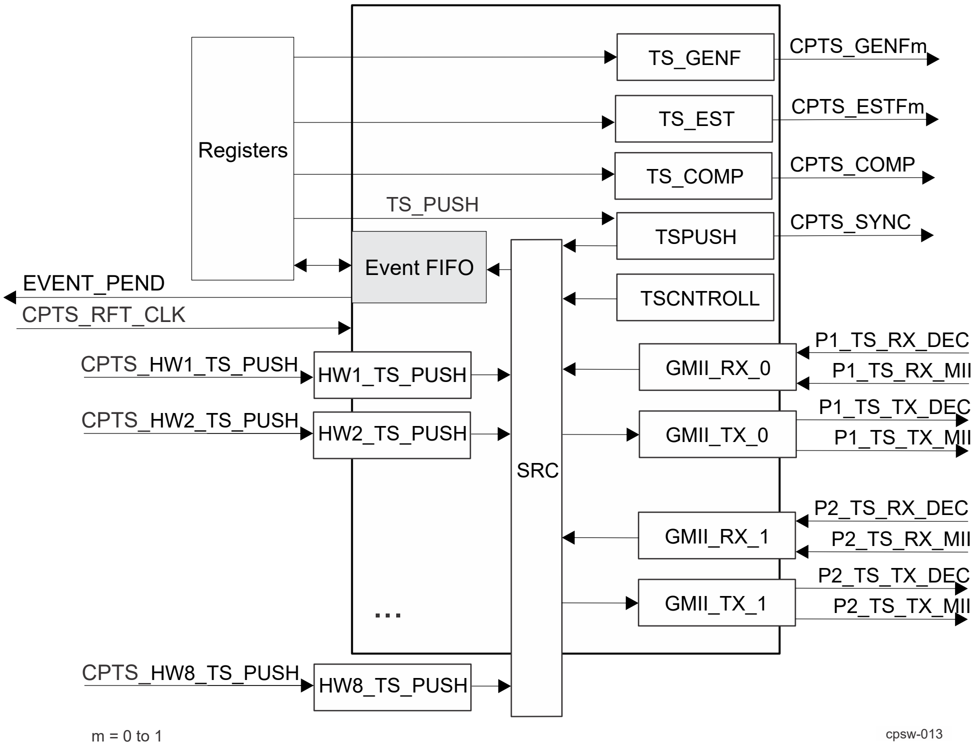
For more information about CPTS clocks and resets, see *CPWS0 Clocks* in *CPSW0 Integration*.

12.3.1.4.7.2 CPTS Architecture

Figure 12-158 shows the architecture of the CPTS module inside the CPSW Ethernet Subsystem. Time stamp values for every packet transmitted or received on external port of the CPSW are recorded. At the same time, each packet is decoded to determine if it is a valid time sync event. If so, an event is loaded into the Event FIFO for processing containing the recorded time stamp value when the packet was transmitted or received.

In addition, both hardware (HWn_TS_PUSH) and software (TS_PUSH) can be used to read the current time stamp value though the Event FIFO. The reference clock used for the time stamp (CPTS_RFT_CLK) can be derived from several sources.

Figure 12-158. CPTS Block Diagram



Note

See Section 12.3.1.4.7.1, *CPSW0 CPTS Integration* for CPTS integration in the device CPSW0 module.

12.3.1.4.7.3 CPTS Initialization

The CPTS module should be configured as follows:

1. Reset the CPTS module.
2. Write the CPTS_CLKSEL value with the desired reference clock selection. This value is allowed to be written only when the CPTS_EN bit in the CPSW3_CPSW_NU_CPTS_CONTROL_REG register is cleared to zero.
3. Set the CPTS_EN bit in the CPSW3_CPSW_NU_CPTS_CONTROL_REG register.
4. If using interrupts and not polling, enable the interrupt by setting the TS_PEND_EN bit in the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG register.

12.3.1.4.7.4 32-bit Time Stamp Value

The time stamp value is a 32-bit value that increments on each CPTS_RFT_CLK rising edge when CPTS_EN bit is set to 1h. When CPTS_EN bit is cleared to 0h, the time stamp value is reset to 0h.

If more than 32-bits of time stamp are required by the application, the host software must maintain the necessary number of upper bits. The upper time stamp value should be incremented by the host when the rollover event is detected.

For test purposes, the time stamp can be written via the time stamp load function (CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG / CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG and CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG registers).

12.3.1.4.7.5 64-bit Time Stamp Value

The time stamp value is a 64-bit value that increments on each CPTS_RFT_CLK rising edge when CPTS_EN bit is set to 1h. When CPTS_EN bit is cleared to 0h, the time stamp value is reset to 0h.

64-bit mode is selected when CPSW3_CPSW_NU_CPTS_CONTROL_REG[5] MODE bit set to 1h.

For test purposes, the time stamp value can be written via the time stamp load function (CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG, CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG, and CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG registers). The CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG feature is included to allow 1ns timestamp operations with an CPTS_RFT_CLK rate less than 1Ghz. Table 12-211 shows the CPTS_RFT_CLK and CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG values for 1ns operations.

Table 12-211. ADD_VAL feature

CPTS_RFT_CLK (MHz)	CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL
1 GHz	0
500 MHz	1
333.33 MHz	2
250 MHz	3
200 MHz	4
166.66 MHz	5
142.85714 MHz	6
125 MHz	7

12.3.1.4.7.6 64-Bit Timestamp Nudge

The 64-bit TIME_STAMP value can be adjusted by writing the CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG[7-0] TS_NUDGE_VAL bit field value which is a two's complement value. A value of FFh will subtract 1 clock cycle from the next incremented 64-bit time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG[31-0] TIME_STAMP and CPSW3_CPSW_NU_CPTS_EVENT_3_REG[31-0] TIME_STAMP value). A nudge value of 1h will add 1 clock cycle to the next incremented TIME_STAMP[63-0] value. For example, if the current TIME_STAMP value is F06h, and CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL = 3h, the next incremented timestamp value would be F0Ah without a nudge and F0Ah +/- [7-0] TS_NUDGE_VAL with a nudge. The [7-0] TS_NUDGE_VAL value is cleared to zero when the nudge has occurred.

12.3.1.4.7.7 64-bit Timestamp PPM

The 64-bit TIME_STAMP can be adjusted by parts per million or by parts per hour. Writing a non-zero value to the CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL (Time stamp PPM Low value) and CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL (Time stamp PPM High value) enables PPM operations. The adjustment is up or down depending on the [7] TS_PPM_DIR bit in the CPSW3_CPSW_NU_CPTS_CONTROL_REG register. The TIME_STAMP value is increased by the PPM value when [7] TS_PPM_DIR bit is cleared. The TIME_STAMP value is decreased by the PPM value when [7] TS_PPM_DIR bit is set.

Parts Per Million example:
To adjust for 100 parts per million the configured value for TS_PPM[41-0] (through CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL) is:
1,000,000/100 = 10,000(decimal)

Parts Per Hour example:
To adjust for 1 part per hour at 1 GHz CPTS_RFT_CLK the configured value for TS_PPM[41-0] (through CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL) is:
(1,000,0000,000Hz/1pph) * (3600 seconds/hour) = 34630B8A000 (hex)

12.3.1.4.7.8 Event FIFO

All time sync events are pushed onto the Event FIFO. There are 32 locations in the event FIFO with no overrun indication supported. Software must service the event FIFO in a timely manner to prevent FIFO overrun.

12.3.1.4.7.9 Timestamp Compare Output

CPTS features one Time Stamp Compare (CPTS_COMP) output. The CPTS_COMP function is a software oriented feature that is intended to be replaced going forward by the hardware oriented GENF function. CPTS_COMP is not compatible with timepstamp PPM or a non-zero CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL value.

12.3.1.4.7.9.1 Non-Toggle Mode: 32-bit

The CPTS_COMP output is asserted for CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH periods when the CPSW3_CPSW_NU_CPTS_EVENT_0_REG[31-0] TIME_STAMP value (lowe 32-bits) compares with the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL and the length value is non-zero. The CPTS_COMP rising edge occurs three CPTS_RFT_CLK clock periods after the values compare. A timestamp compare event is pushed into the event FIFO when CPTS_COMP is asserted. The polarity of the CPTS_COMP output is determined by the CPSW3_CPSW_NU_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit. The output is asserted low when the polarity bit is 0h.

12.3.1.4.7.9.2 Non-Toggle Mode: 64-bit

64-bit mode operation is identical to 32-bit mode except that all 64-bits of the TIME_STAMP are used (CPSW3_CPSW_NU_CPTS_EVENT_0_REG and CPSW3_CPSW_NU_CPTS_EVENT_3_REG). In 32-bit mode only the lower 32-bits (CPSW3_CPSW_NU_CPTS_EVENT_0_REG) are used.

12.3.1.4.7.9.3 Toggle Mode: 32-bit

The CPTS_COMP output is asserted (CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH) for CPTS_RFT_CLK clock periods when the TIME_STAMP[31:0] value compares with the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG and the length value is non-zero. The CPTS_COMP toggles thereafter on CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_LENGTH for CPTS_RFT_CLK periods. The length high or low can be adjusted by writing the CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE bit field value which is a two's complement value. A value of FFh will subtract one CPTS_RFT_CLK period from the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_LENGTH value. A value of 0x01h will add one CPTS_RFT_CLK period to the CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH value. Only a single high or low time is adjusted (nudged) and the CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE value is cleared to zero when the nudge has occurred. The CPTS_COMP output is asserted low when the CPSW3_CPSW_NU_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit is 0h. No compare events and no CPTS_EVNT interrupts are generated in toggle mode. The CPSW3_CPSW_NU_CPTS_CONTROL_REG[6] TS_COMP_TOG bit must be set for toggle mode (value 1h). Note this bit must be set before writing a non-zero value to CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG register.

12.3.1.4.7.9.4 Toggle Mode: 64-bit

64-bit mode operation is identical to 32-bit mode except that all 64-bits of the TIMESTAMP are used (CPSW3_CPSW_NU_CPTS_EVENT_0_REG and CPSW3_CPSW_NU_CPTS_EVENT_3_REG). In 32-bit mode only the lower 32-bits (CPSW3_CPSW_NU_CPTS_EVENT_0_REG) are used.

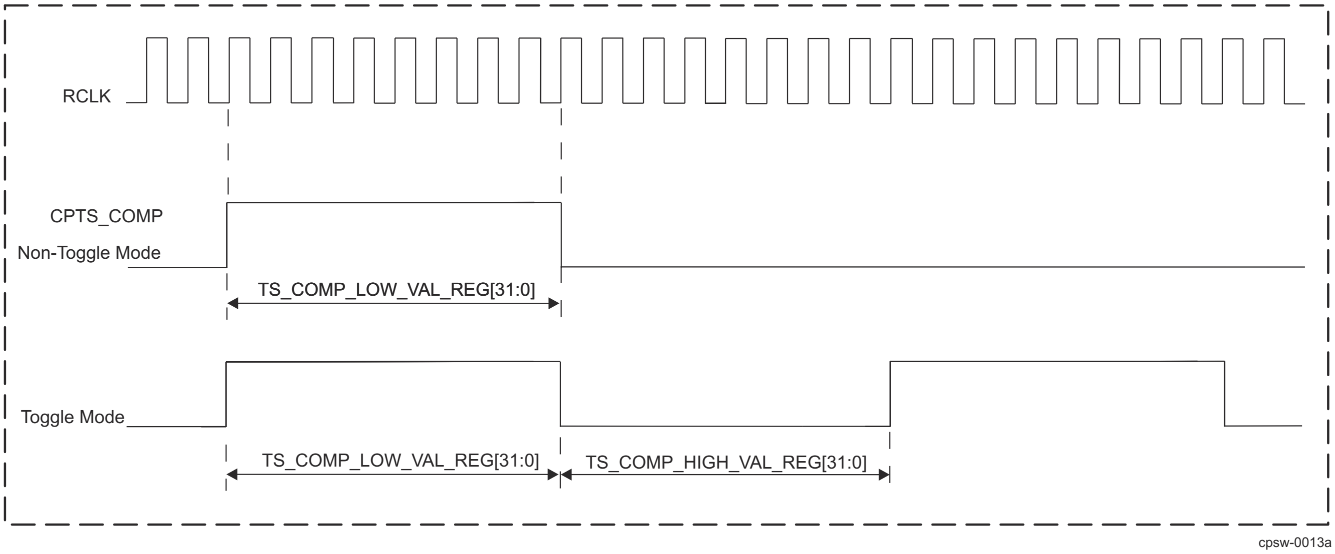


Figure 12-159. CPTS_COMP Output in Toggle and Non-Toggle Mode

12.3.1.4.7.10 Timestamp Sync Output

The CPTS_SYNC output is a selected bit of the [31-0]TIME_STAMP counter value. One of bits 17-31 can be selected in CPSW3_CPSW_NU_CPTS_CONTROL_REG[31-28] TS_SYNC_SEL. The CPTS_SYNC output is disabled when CPSW3_CPSW_NU_CPTS_CONTROL_REG[31-28] TS_SYNC_SEL is zero.

If the selected counter bit is 1 at the time when TS_SYNC_SEL value is written then a rising edge will not occur on the CPTS_SYNC output. A rising edge will occur on the CPTS_SYNC output upon the next transition to 1 of the selected counter bit. The TS_SYNC_SEL value must be written to zero before changing to a different non-zero value. No events are generated due to the CPTS_SYNC operation. The CPTS_SYNC output is two CPTS_RFT_CLK periods after the actual count value.

12.3.1.4.7.11 Timestamp GENFn Output

The CPTS_GENFn outputs have a programmable cycle (frequency) with a PPM feature and software nudge feature. The CPTS_GENFn output cycle is CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods (which is different than CPTS_COMP operation). Figure 12-160 represents the CPTS_GENFn output signal.

The CPTS_GENFn output cycle is CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods beginning when the 64-bit TIME_STAMP value compares with the 64-bit GENFn_COMP value (CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_L and CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_L registers) and the length value is non-zero. The CPTS_GENFn output cycle repeats thereafter every CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] CPTS_RFT_CLK periods. The upper 32-bit word should be written first for 64-bit values. The length should be zero while the comparison value and other configuration parameters are being configured. The length should be written non-zero to enable operations last. The first cycle after comparison is active high when the CPSW3_CPSW_NU_CPTS_CONTROL_REG[2] TS_COMP_POLARITY bit is low. No compare events and no CPTS_EVNT interrupts are generated.

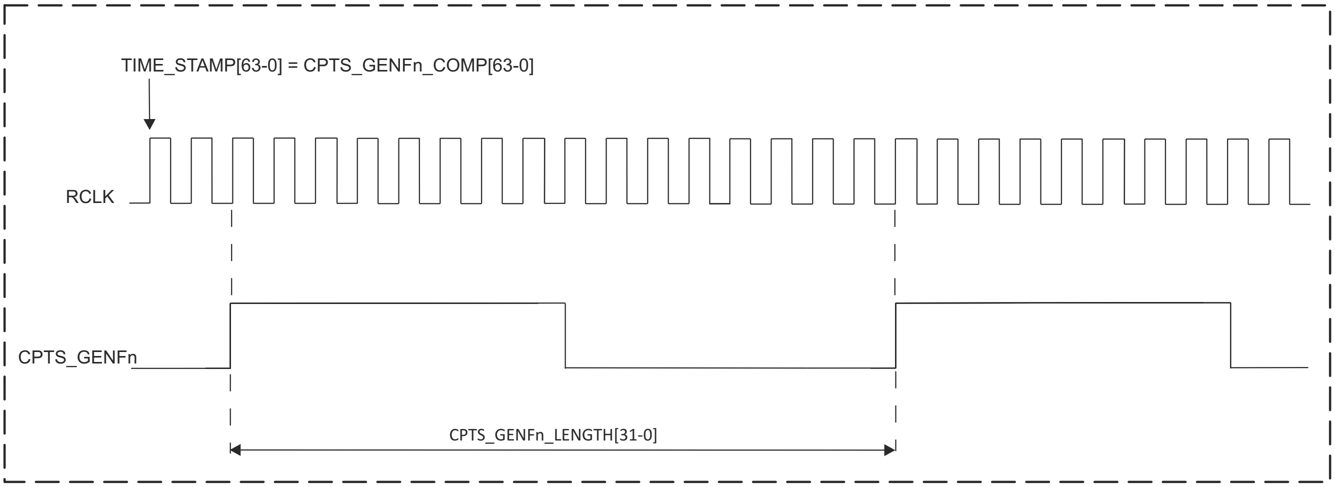


Figure 12-160. CPTS_GENFn Output Signal Diagram

12.3.1.4.7.11.1 GENFn Nudge

The cycle length can be adjusted by writing the CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE register value which is a two's complement value. A value of FFh will subtract 1 CPTS_RFT_CLK from theCPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] value. A value of 1h will add 1 CPTS_RFT_CLK to theCPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_L[31-0] value. The CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE value is cleared to zero when the nudge has occurred.

12.3.1.4.7.11.2 GENFn PPM

The CPTS_GENFn output cycle can be adjusted by parts per million or by parts per hour. Writing a non-zero value to CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_L/ CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_L enables PPM operations. The PPM counter continually loads and decrements to zero and then loads again. A single CPTS_RFT_CLK adjustment is made when the PPM counter decrements to zero. The adjustment is up or down depending on the CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG[0] PPM_DIR bit. When PPM_DIR bit is set a single CPTS_RFT_CLK time is subtracted from the generate function counter which has the effect of increasing the generate function frequency by the PPM amount. When PPM_DIR bit is cleared a single CPTS_RFT_CLK time is added to the generate function counter which has the effect of decreasing the generate function frequency by the PPM amount.

Parts Per Million example:
To adjust for 100 parts per million the configured value for GENF_PPM[41-0] (through CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_L and CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_L) is:
1,000,000/100 = 10,000(decimal)

Parts Per Hour example:
To adjust for 1 part per hour at 1 GHz CPTS_RFT_CLK the configured value for GENF_PPM[41-0] (through CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_L and CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_L) is:
(1,000,0000,000Hz/1pph) * (3600 seconds/hour) = 34630B8A000 (hex)

12.3.1.4.7.12 Timestamp ESTFn

Each Ethernet port has a dedicated ESTFn generator which operates identically to the GENFn function.

12.3.1.4.7.13 Time Sync Events

Time Sync events are 96-bit values that are pushed onto the event FIFO and read by software in 32-bit reads. Four 32-bit registers, CPSW3_CPSW_NU_CPTS_EVENT_0_REG through

CPSW3_CPSW_NU_CPTS_EVENT_3_REG hold the data of a time sync event. There are eight types of sync events:

- Time Stamp Push Event
- Time Stamp Counter Rollover Event (32-bit mode only)
- Time Stamp Counter Half-rollover Event (32-bit mode only)
- Hardware Time Stamp Push Event
- Ethernet Receive Event
- Ethernet Transmit Event
- Time Stamp Compare Event
- Host Transmit Event

12.3.1.4.7.13.1 Time Stamp Push Event

Software can obtain the current time stamp value (at the time of the write) by initiating a time stamp push event. The push event is initiated by setting the [0]TS_PUSH bit of the CPSW3_CPSW_NU_CPTS_TS_PUSH_REG register. The time stamp value is returned in the event, along with a time stamp push event code. The upper 32-bits (CPSW3_CPSW_NU_CPTS_EVENT_3_REG register) of the timestamp are zero in 32-bit mode.

12.3.1.4.7.13.2 Time Stamp Counter Rollover Event (32-bit mode only)

The CPTS module contains a 32-bit time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG). The counter upper bits are maintained by host software. The rollover event indicates to software that the time stamp counter has rolled over from 0xFFFF FFFF to 0x0000 0000 and the software-maintained upper count value should be incremented. This event occurs only in 32-bit mode.

12.3.1.4.7.13.3 Time Stamp Counter Half-rollover Event (32-bit mode only)

The CPTS includes a time stamp counter half-rollover event. The half-rollover event indicates to software that the time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG[31-0] TIME_STAMP) has incremented from 0x7FFF FFFF to 0x8000 0000. The half-rollover event is included to enable software to correct a misaligned event condition. This event occurs only in 32-bit mode.

The half-rollover event is included to enable software to determine the correct time for each event that contains a valid time stamp value, such as an Ethernet event. If an Ethernet event occurs around a counter rollover (full rollover), the rollover event could possibly be loaded into the event FIFO before the Ethernet event, even though the Ethernet event time was actually taken before the rollover. Figure 12-161 shows a misalignment condition. This misaligned event condition arises because an Ethernet event time stamp occurs at the beginning of a packet and time passes before the packet is determined to be a valid synchronization packet. The misaligned event condition occurs if the rollover occurs in the middle, after the packet time stamp has been taken, but before the packet has been determined to be a valid time sync packet.

Host software must detect and correct for misaligned event conditions. For every event time stamp after a rollover and before a half-rollover, software must examine the time stamp most significant bit. If bit 31 of the time stamp value is low (0x0000 0000 through 0x7FFF FFFF), then the event time stamp was taken after the rollover and no correction is required. If the value is high (0x8000 0000 through 0xFFFF FFFF), the time stamp value was taken before the rollover and a misalignment is detected. The misaligned case indicates to software that it must subtract one from the upper count value stored in software to calculate the correct time for the misaligned event. The misaligned event occurs only on the rollover boundary and not on the half-rollover boundary. Software only needs to check for misalignment from a rollover event to a half-rollover event.

When a rollover occurs, software increments the software time stamp upper value. The misaligned case indicates to software that the misaligned event time stamp has a valid upper value that is pre-increment, so one must be subtracted from the upper value to allow software to calculate the correct time for the misaligned event.

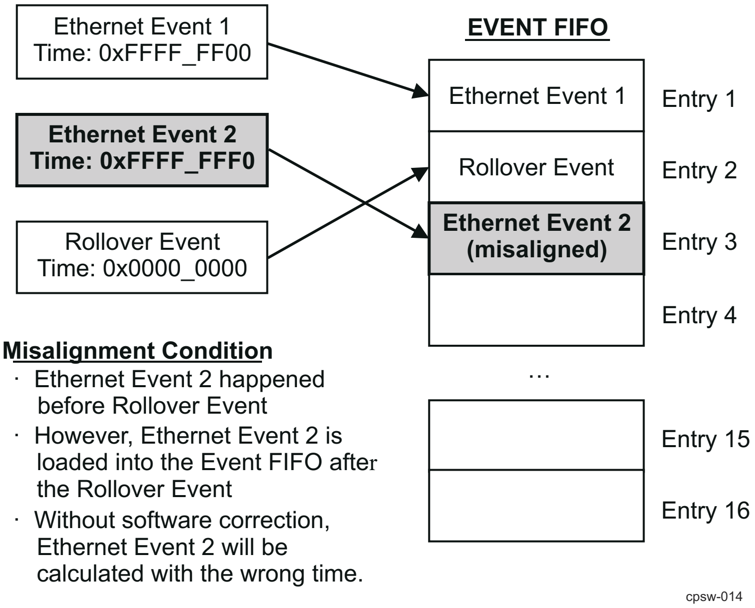


Figure 12-161. Event FIFO Misalignment Condition

12.3.1.4.7.13.4 Hardware Time Stamp Push Event

There are four hardware time stamp inputs (CPTS_HW[1:4]_TS_PUSH events) that can cause hardware time stamp push events to be loaded into the Event FIFO. Each time stamp input is mapped in the device as shown in *CPTS Integration*. The event is loaded into the event FIFO on the rising edge of the timer, and the PORT_NUMBER field in the CPSW3_CPSW_NU_CPTS_EVENT_1_REG register indicates the hardware push input that caused the event (encoded).

The hardware time stamp inputs are asynchronous and are low frequency signals. The CPTS logic synchronizes and performs a rising edge detect on the incoming asynchronous input.

Each hardware time stamp input must be asserted for at least 10 periods of the selected CPTS_RFT_CLK clock. Each input can be enabled or disabled by setting the respective bits in the CPSW3_CPSW_NU_CPTS_CONTROL_REG register.

Hardware time stamps are intended to be an extremely low frequency signals, such that the event FIFO does not overrun. Software must keep up with the event FIFO and ensure that there is no overrun, or events will be lost.

12.3.1.4.7.13.5 Ethernet Port Events

Packets transmitted or received on each Ethernet port can generate Ethernet Transmit Events or Ethernet Receive Events, respectively. The CPTS hardware will decode each packet to determine if it is a valid CPTS time sync event.

According to the IEEE 802.3 Ethernet standard, each Ethernet frame contains a 2-octet EtherType field to indicate which protocol is encapsulated in the PayLoad field, as shown in Figure 12-162. For standard time sync packets, this will contain the EtherType for the Precision Time Protocol (IEEE 1588), which is defined as 0x88F7. The CPTS hardware will compare this field to the TS_LTYPE1 field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG or the TS_LTYPE2 field in CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register (depending on which enable bit was set) , which should also be programmed to 88F7h.

When a virtual LAN is used, an additional 4-octet 802.1Q tag is inserted in the Ethernet frame before the EtherType field, as shown in Figure 12-162. To indicate to the CPTS hardware that a virtual LAN is in use, the TS_TX_VLAN_LTYPE1_EN (or TS_TX_VLAN_LTYPE2_EN) enable bit must be set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register. The EtherType for the 802.1Q tag is defined as 0x8100, and the CPTS hardware will compare this value to the TS_VLAN_LTYPE1 (or TS_VLAN_LTYPE2 depending on which enable bit was set) field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register, which should also be programmed to 0x8100.

When two stacked VLANs are used, two additional 4-octet 801.Q tags are inserted in the Ethernet frame before the EtherType field, as shown in Figure 12-162. In this case, both TS_VLAN_LTYPE1 and TS_VLAN_LTYPE2 must be enabled. The outer tag must match the value of the TS_VLAN_LTYPE1 field, and the inner tag must match the value of the TS_VLAN_LTYPE2 field.

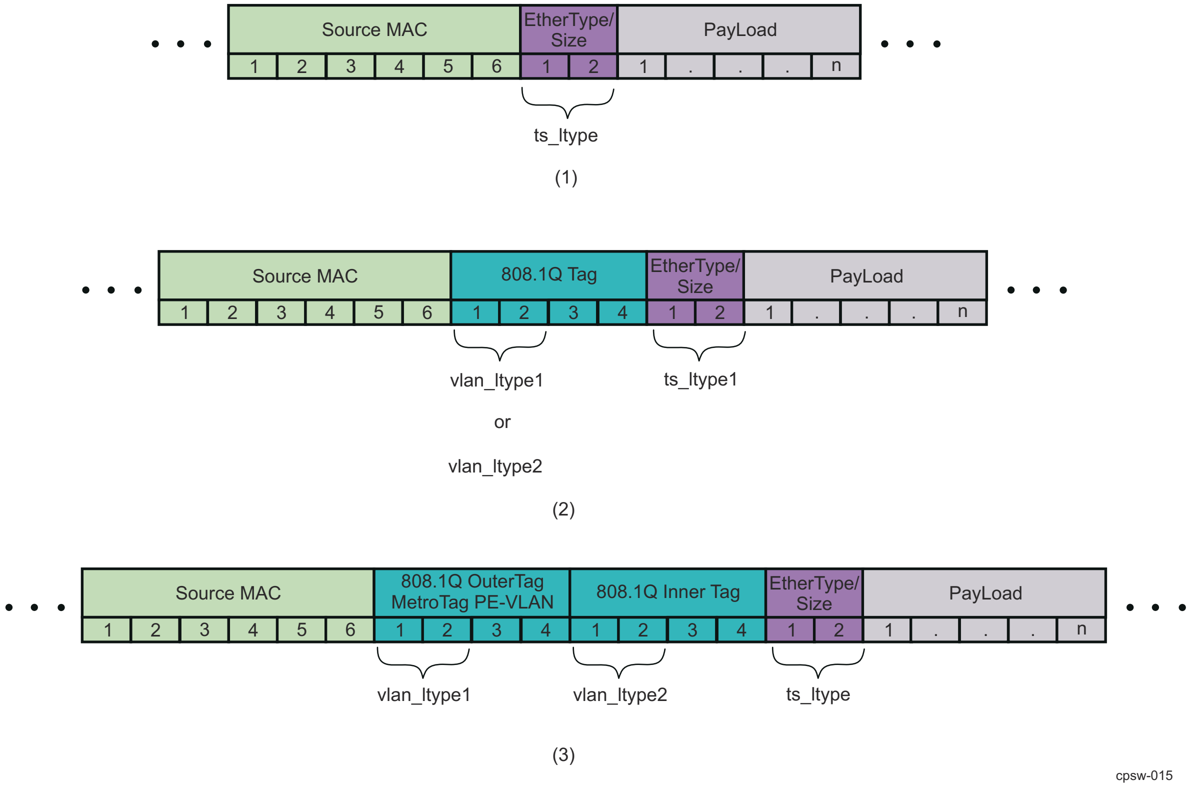


Figure 12-162. Partial Ethernet-II Frames Showing Register Mapping of EtherTypes for a Simple Frame (1), a Single 1Q Tag Added (2), and Two 1Q Tags Added (3)

12.3.1.4.7.13.5.1 Ethernet Port Receive Event

This section describes Ethernet port receive events. Ethernet port generates time synchronization events for valid received time sync packets. For every packet received on the Ethernet port, a timestamp will be captured by the receive module inside the CPTS for the corresponding port. The time stamp will be captured by the receive module regardless of whether or not the packet is a time synchronization packet to make sure that the time stamp is captured as soon as possible. The packet is sampled on both the rising and falling edges of the CPTS_RFT_CLK, and the time stamp will be captured once the start of frame delimiter for the receive packet is detected.

After the time stamp has been captured, the receive interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The CPSW decoder determines if the packet is a valid Ethernet receive time synchronization event. The receive interface for the port will use the following criteria to determine if the packet is a valid Annex D, Annex E, or Annex F time synchronization Ethernet receive event:

Annex D (IPv4)

1. Receive annex D time sync is enabled (TS_RX_ANNEX_D_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true.
    a. The first packet LTYPE matches 0x0800

  b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
  c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
  d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches 0x0800

3. Byte 14 (the byte after the LTYPE) contains 0x45 (IPv4).

Note

The byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes.

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4. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)
5. Byte 22 contains 0x01 (HOP Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 22 contains any value if CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG is set to 1h. Byte 22 is the TTL/HOP field.
6. Byte 23 contains 0x11 (Next Header UDP Fixed).
7. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h and Bytes 30 through 33 contain:
   a. Decimal 224.0.1.129 and the TS_129 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 224.0.1.130 and the TS_130 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   c. Decimal 224.0.1.131 and the TS_131 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   d. Decimal 224.0.1.132 and the TS_132 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   e. Decimal 224.0.0.107 and the TS_107 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set

   -OR-

   The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set and Bytes 30 through 33 contain any values.
8. Bytes 36 and 37 contain:
   a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set -OR-
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set.

9. The PTP message begins in byte 42.
10. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.

11. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

Annex E (IPv6)

1. Receive annex E time sync is enabled (TS_RX_ANNEX_E_EN bit is set in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true.
    a. The first packet LTYPE matches 0x86dd.
    b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
    c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
    d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches 0x86dd
3. Byte 14 (the byte after the LTYPE) contains 0x6X (IPv6).
4. Byte 20 contains 0x11 (UDP Fixed Next Header).
5. Byte 21 contains 0x01 (Hop Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 21 contains any value if TS_TTL_NONZERO is set to 1h. Byte 21 is the TTL/HOP field.
6. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0 and Bytes 38 through 53 contain:
    a. FF0M:0:0:0:0:0:0:0181 and the TS_129 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    b. FF0M:0:0:0:0:0:0:0182 and the TS_130 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    c. FF0M:0:0:0:0:0:0:0183 and the TS_131 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    d. FF0M:0:0:0:0:0:0:0184 and the TS_132 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
    e. FF0M:0:0:0:0:0:0:006B and the TS_107 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set

    Note

    All values above are 16-bit hex numbers where M is enabled in the TS_MCAST_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register.

    -OR-

    The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set to 1h and Bytes 38 through 53 contain any value.
7. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):

   a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register is set.

8. The PTP message begins in byte 62.
9. The packet message type is enabled in the MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register.
10. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

Annex F (IEEE 802.3)

1. Receive Annex F time sync is enabled (TS_RX_ANNEX_F_EN is set in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true:
   a. The first packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG/ CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.
   b. The first packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
   c. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
   e. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register.
   f. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
   g. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register.
   h. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_RX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register

3. The PTP message begins in the byte after the LTYPE.
4. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
5. The packet was received without error (not long/short/mac_ctl/CRC/code/align).

If all of the criteria described above are met for either Annex D, Annex E, or Annex F, and the packet is determined to be a valid time synchronization packet, then the RX interface will push an Ethernet receive event into the event FIFO.

12.3.1.4.7.13.5.2 Ethernet Port Transmit Event

This section describes Ethernet port transmit events. For every packet transmitted on the Ethernet ports, the port transmit interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The CPTS transmit interface for the port will use to the following criteria to determine if the packet is a valid time synchronization Ethernet transmit event. The CPSW decoder determines if the packet is a valid ethernet receive time synchronization event. To be a valid Ethernet transmit time synchronization event, the conditions listed below must be true for either Annex D, Annex E, or Annex F:

Annex D (IPv4)

1. Transmit time sync is enabled (TS_TX_ANNEX_D_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x0800
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x0800
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the

CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches 0x0800

3. Byte 14 (the byte after the LTYPE) contains 0x45 (IPv4).

Note

The byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes.

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4. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)
5. Byte 22 contains 0x01 (HOP Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 22 contains any value if TS_TTL_NONZERO is set to 1h. Byte 22 is the TTL/HOP field.
6. Byte 23 contains 0x11 (Next Header UDP Fixed).
7. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h and Bytes 30 through 33 contain:
   a. Decimal 224.0.1.129 and the TS_129 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 224.0.1.130 and the TS_130 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   c. Decimal 224.0.1.131 and the TS_131 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   d. Decimal 224.0.1.132 and the TS_132 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   e. Decimal 224.0.0.107 and the TS_107 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   f. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set and Bytes 30 through 33 contain any values.
8. Bytes 36 and 37 contain:
   a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set.
9. The PTP message begins in byte 42.
10. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
11. The packet was sent by host port 0.

Annex E (IPv6)

1. Transmit annex E time sync is enabled (TS_TX_ANNEX_E_EN bit is set in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches 0x86dd.
   b. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
   c. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches 0x86dd
   d. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG

register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches 0x86dd

3. Byte 14 (the byte after the LTYPE) contains 0x6X (IPv6).
4. Byte 20 contains 0x11 (UDP Fixed Next Header).
5. Byte 21 contains 0x01 (Hop Limit = 1) if the TS_TTL_NONZERO bit in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0h, or byte 21 contains any value if TS_TTL_NONZERO is set to 1h. Byte 21 is the TTL/HOP field..
6. The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is cleared to 0 and Bytes 38 through 53 contain:
   a. FF0M:0:0:0:0:0:0:0181 and the TS_129 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. FF0M:0:0:0:0:0:0:0182 and the TS_130 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   c. FF0M:0:0:0:0:0:0:0183 and the TS_131 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   d. FF0M:0:0:0:0:0:0:0184 and the TS_132 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   e. FF0M:0:0:0:0:0:0:006B and the TS_107 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set

   Note

   All values above are 16-bit hex numbers where M is enabled in the TS_MCAST_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL2_REG register.

   -OR-

   The TS_UNI_EN bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set to 1h and Bytes 38 through 53 contain any value.
7. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):
   a. Decimal 0x01 and 0x3F respectively and the TS_319 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set, or
   b. Decimal 0x01 and 0x40 respectively and the TS_320 bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register is set.
8. The PTP message begins in byte 62.
9. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
10. The packet was sent by host port 0.

Annex F (IEEE 802.3)

1. Transmit time sync is enabled (TS_TX_ANNEX_F_EN is set in the switch CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register).
2. One of the sequences below is true:
   a. The first packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.
   b. The first packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.

   c. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register.
   d. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_SEQ_LTYPE_REG register.
   e. The first packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register.
   f. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
   g. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register.
   h. The first packet LTYPE matches TS_VLAN_LTYPE1 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE1_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the second packet LTYPE matches TS_VLAN_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_VLAN_LTYPE_REG register and TS_TX_VLAN_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register and the third packet LTYPE matches TS_LTYPE2 in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_LTYPE2_REG register and TS_LTYPE2_EN is set in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register

3. The packet message type is enabled in the TS_MSG_TYPE_EN field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_TS_CTL_REG register.
4. The packet was sent by host port 0.

If all of the criteria described above are met, and the packet is determined to be a valid time synchronization packet, then the time stamp for the transmit event will not be generated until the start of frame delimiter of the packet is actually transmitted. The start of frame delimiter will be sampled on every rising and falling edge of the

CPTS_RFT_CLK. Once the packet is transmitted, then the TX interface will push an Ethernet transmit event into the event FIFO.

12.3.1.4.7.13.5.3 Time Sync Message Types

Table 12-212. Values of Message Type Field

Message Type	Value (hex)
Sync	0
Delay_Req	1
Pdelay_Req	2
Pdelay_Resp	3
Reserved	4:7
Follow_Up	8
Delay_Resp	9
Pdelay_Resp_Follow_Up	A
Announce	B
Signaling	C
Management	D
Reserved	E:F

Once a transmitted or received packet is determined to be a valid time sync packet, the Ethernet Transmit Event or Ethernet Receive Event is loaded onto the Event FIFO.

The CPSW3_CPSW_NU_CPTS_EVENT_1_REG register contains the Message Type and Sequence ID values from the original time sync packet. The CPSW3_CPSW_NU_CPTS_EVENT_0_REG (and CPSW3_CPSW_NU_CPTS_EVENT_3_REG) register contains the time stamp value when the packet arrived at the corresponding port.

12.3.1.4.7.14 Timestamp Compare Event

Note

Timestamp compare events are generated for non-toggle mode only.

The CPTS can generate an event for a time stamp comparison in 32-bit or 64-bit mode.

12.3.1.4.7.14.1 32-Bit Mode

The CPTS_COMP output is also asserted when the event is generated. The event is generated when the 32-bit time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG) compares with the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG register and the CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG value is non-zero. The CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG value should be written by software after the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG register is written and should be zero when the comparison value is written.

12.3.1.4.7.14.2 64-Bit Mode

The CPTS_COMP output is also asserted when the event is generated. The event is generated when the 64-bit time stamp value (CPSW3_CPSW_NU_CPTS_EVENT_0_REG and CPSW3_CPSW_NU_CPTS_EVENT_3_REG) compares with the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG and CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG registers and the CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG value is non-zero. The CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG value should be written by software after the CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG register is written and should be zero when the comparison value is written.

12.3.1.4.7.15 Host Transmit Event

The host can send a packet to be transmitted on an Ethernet port that will generate a time synchronization event. The host sets the TSTAMP_EN bit and sends the DOMAIN, MESSAGE_TYPE, and SEQUENCE_ID in the additional control information that resides in the protocol specific section of the descriptor that is transmitted to the CPSW_3G. An event is then generated and placed on the event FIFO once the packet is transmitted. Host events allow the user to timestamp exactly when a software generated packet exits the device.

12.3.1.4.7.16 CPTS Interrupt Handling

When an event is push onto the Event FIFO, an interrupt can be generated to indicate to software that a time sync event occurred. The following steps should be taken to process time sync events using interrupts:

1. Enable the TS_PEND interrupt by setting the TS_PEND_EN bit of the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG register.
2. Upon interrupt, read the CPSW3_CPSW_NU_CPTS_EVENT_0_REG through CPSW3_CPSW_NU_CPTS_EVENT_3_REG registers values.
3. Set the CPSW3_CPSW_NU_CPTS_EVENT_POP_REG[0] EVENT_POP bit to 1h to pop the previously read value off of the event FIFO.
4. Process the interrupt as required by the application software.

Software has the option of processing more than a single event from the event FIFO in the interrupt service routine in the following way:

1. Enable the TS_PEND interrupt by setting the TS_PEND_EN bit of the CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG
2. Upon interrupt, enter the CPTS service routine.
3. Read the CPSW3_CPSW_NU_CPTS_EVENT_0_REG through CPSW3_CPSW_NU_CPTS_EVENT_3_REG registers values.
4. Set the CPSW3_CPSW_NU_CPTS_EVENT_POP_REG[0] EVENT_POP bit to 1h to pop the previously read value off of the event FIFO.
5. Wait for an amount of time greater than four CPTS_RFT_CLK periods plus four CPPI_ICLK periods.
6. Read the TS_PEND_RAW bit in the CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG register to determine if another valid event is in the event FIFO. If bit TS_PEND_RAW is asserted, go to step 3. If bit TS_PEND_RAW is not asserted proceed with step 7.
7. Process the interrupt(s) as required by the application software.

Software also has the option of disabling the interrupt and polling the TS_PEND_RAW bit of the CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG register to determine if a valid event is on the event FIFO.

12.3.1.4.8 CPPI Streaming Packet Interface

The receive streaming interface on port 0 of the CPSW is responsible for receiving packet for Ethernet egress data from the packet streaming switch in the . The CPPI receive port is equivalent to an Ethernet port with the difference being that the data is provided to the CPSW in the 128-bit streaming interface data format instead RGMII data format.

In addition to the packet data, the receive streaming interface also can provide additional control information that resides in the information words of the descriptor that was transmitted to the CPSW.

The tables below show the information that may be passed along with which descriptor information word to put it in.

12.3.1.4.8.1 Port 0 CPPI Transmit Packet Streaming Interface (CPSW_3G Egress)

The CPSW_3G has a single transmit packet streaming interface. All Ethernet packet data destined for the host (Port 0) is transferred on the transmit packet streaming interface. The transmit packet streaming interface is equivalent to an Ethernet MAC output with the difference being that 128-bit streaming interface data is output. Egress packet data is packed on the 128-bit data bus with all words having 16-bytes except possibly the last packet data word which is the word previous to the EOP word. INFO Word 0–3 is transferred on SOP. The EOP word contains the packet status 0–3 (data type 24) which includes the timestamp and checksum data.

Packets are not dropped on the transmit streaming interface due to pushback, but packets may be dropped in the associated priority FIFO.

INFO Word 0–3 and Status Data Word 0–3 (on EOP) are the only non-payload data word types that are transferred. Long packets are truncated at the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN byte value of the ingress port (only the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_RX_MAXLEN_REG_k number of bytes are kept if long packets are transferred due to CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k register copy error frames set - RX_CEF_EN). MAC control frames are only transferred if the receiving Ethernet port has the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k[24] RX_CMF_EN bit set.

The error encoding on the TXST_PKT_ERR[3:0] output is shown in Table 12-213:

Table 12-213. Error Encoding on the TXST_PKT_ERR[3:0] Output

TXST_PKT_ERR[3:0]	Description
0000	No Error
0001	CRC Error
0010	Code or alignment error
0011	Short (no code/align/crc error)
0100	FragCRC (short with crc error)
0101	Frag Code/Align (short with code/align error)
0110	Long
0111	Jabber CRC (long with crc error)
1000	Jabber Code/Align (long with code/align error)
1001	Mac ontrol packet (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k[24] RX_CMF_EN set on ingress Ethernet port)
1010	Mac control CRC
1011	Mac control Code/Align
1100	Mac control short/frag (short MAC control frame with CRC/Code/Align)
1101	Mac control long/jabber (long MAC control frame with CRC/Code/Align)
1110	Reserved
1111	Reserved

The CPPI Port 0 transmit packet streaming interface has a single output thread. If a packet transmission has begun then the entire packet will be transmitted before the next packet is sent (packet data from multiple packets are not interleaved on the transmit streaming interface). The default egress flow is the port number minus 1, concatenated with the 3-bit Port 0 transmit FIFO hardware switch priority. For example, a packet that was received on port 4 with a Port 0 transmit FIFO hardware switch priority of 5 would be sent on flow 29 (decimal) or flow 0b0011101 (binary). Priority remapping on ingress and Port 0 transmit egress effects the output flow.

INFO Words are a contiguous block of four 32-bit data words aligned on a 32-bit word boundary.

Figure 12-163. TX INFO Word 0 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PKT_TYPE					RESERVED			PASS_CRC	CRC_TYPE	RESERVED					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FLOW_ID							

Bit	Field	Description
31-27	PKT_TYPE	Always set to 0b00111. Host PD (Packet Descriptor) Word 2. Packet Type: bits[31-27].

Bit	Field	Description
26-24	RESERVED	Reserved.
23	PASS_CRC	This bit is cleared to zero (no CRC passed) when the P0_TX_CRC_REMOVE bit in the CPSW3_CONTROL_REG register is set (and the egress packet has no errors). When the remove bit is cleared to zero then this bit is cleared and no CRC is passed with the output packet. The packet length includes the CRC if it is present.
22	CRC_TYPE	The packet CRC type. The type of CRC passed is determined by CRC_TYPE field in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k register (not by the type of CRC the packet had on Ethernet port ingress). Host PD Word 1. Protocol Specific Flags: bits[27-24]. 0h: Ethernet CRC 1h: Castagnoli CRC
21-8	RESERVED	Reserved.
7-0	FLOW_ID	This is the packet output transmit streaming interface flow. The default flow ID can be overridden by ALE classification (Thread mapping). The switch default flow is the 3-bit “From Port” value concatenated with the 3-bit “Switch Priority” {From_Port[2:0], Switch_Priority[2:0]} as shown below: Host PD (Packet Descriptor) Word 1. Flow ID: bits[13-0]. 0h: The packet was received on Ethernet port 1 Switch Priority – The actual hardware switch priority that the packet was stored in on the CPPI transmit FIFO.

Figure 12-164. TX INFO Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x4 (fixed_ps_size)												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		PKT_LENGTH													

Bit	Field	Description
31-20	FIXED_PS_SIZE	Fixed packet size: 0x4
19-14	RESERVED	Reserved.
13-0 (Host PD (Packet Descriptor) Word 1. Packet Length: bits[21-0])	PKT_LENGTH	Specifies the number of bytes in the entire packet. Offset bytes are not included. Valid only on SOP. The packet length must be greater than zero. The packet data will be truncated to the packet length if the packet length is shorter than the sum of the packet buffer descriptor buffer lengths. A host error occurs if the packet length is greater than the sum of the packet buffer descriptor buffer lengths.

Figure 12-165. TX INFO Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xFFFF															

Figure 12-166. TX INFO Word 3 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SRC_ID							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															

Bit	Field	Description
31-24	RESERVED	Reserved.
23-16	SRC_ID	The packet SRC_ID value comes from the PORT1/PORT2 field in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG register. (src_tag) PD (Packet Descriptor) Word 3. Source Tag Low bits[23-16] if RFLOW[a]_RFC.rx_src_tag_lo_sel = 0x4 or (src_tag) PD (Packet Descriptor) Word 3. Source Tag High bits[31-24] if RFLOW[a]_RFC.rx_src_tag_hi_sel = 0x4
15-0	RESERVED	Reserved.

Note

TX Status Data Word [0..3] are mapped to Host Packet Descriptor Protocol Specific Words if RFLOW[a]_RFA.rx_psinfo_present = 1 and RFLOW[a]_RFA.rx_ps_location = 0

Figure 12-167. TX Status Data Word 0 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMESTAMP[31:0]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP[31:0]															

Bit	Field	Description
31-0	TIMESTAMP[31:0]	Contains the lower 32-bits of the time stamp value.

Figure 12-168. TX Status Data Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMESTAMP[63:32]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMESTAMP[63:32]															

Bit	Field	Description
31-0	TIMESTAMP[63:32]	Contains the upper 32-bits of the time stamp value.

Figure 12-169. TX Status Data Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											IPV4_VALID	IPV6_VALID	TCP_UDP_N	FRAGMENT	CHECKSUM_ERROR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHECKSUM_ADD															

Bit	Field	Description
31-21	RESERVED	Reserved.
20	IPV4_VALID	An IPV4 TCP or UDP Packet was detected.
19	IPV6_VALID	An IPV6 TCP or UDP Packet was detected.
18	TCP_UDP_N	Valid only when either the IPV4_VALID or IPV6_VALID bits are set. 0h: Indicates UDP packet was detected. 1h: Indicates TCP packet was detected.
17	FRAGMENT	Indicates that an IP fragment was detected. Valid only when when either the IPV4_VALID or IPV6_VALID bits are set.

Bit	Field	Description
16	CHECKSUM_ERROR	Valid only when either the IPV4_VALID or IPV6_VALID bits are set.
15-0	CHECKSUM_ADD	This is the value that was summed during the checksum computation. This value is FFFFh for IPV4/6 UDP/TCP packets with no checksum error.

Figure 12-170. TX Status Data Word 3 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0															

Bit	Field	Description
31-0	RESERVED	Reserved.

12.3.1.4.8.2 Port 0 CPPI Receive Packet Streaming Interface (CPSW_3G Ingress)

Info Word 0/1/2/3 (INFO1 and INFO3 are ignored) are transferred on SOP. If a timestamp word (Extended Packet Info Word 0/1/2/3) is to be transferred it must be after SOP and before any packet data is transferred. Any following non-data type words will be dropped. The EOP word must be payload data.

Input receive packets cannot be aborted by the host. The INFO Word bit descriptions and Extended Packet INFO Word bit descriptions are shown below. The PASS_CRC bit indicates that the CRC is passed with the packet data. Packets that have a passed CRC that is an error CRC will be output on the Ethernet port with at least one CRC byte inverted to indicate the error if P0_RX_PASS_CRC_ERR bit is set, otherwise they are dropped. The packet is a directed packet when any of the TO_PORT bits are nonzero. A packet may be directed only to a single port. The packet will be sent to the port number indicated. For directed packets the lookup process is skipped to determine the destination. However, in vlan aware mode (when VLAN_AWARE bit in the CPSW3_CONTROL_REG register is set to 1h) the lookup is performed to determine untagged egress. Packets longer then the value in CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bit field are dropped. Packets shorter than 60-Bytes are padded to 64-Bytes (after adding pad and CRC) if P0_RX_PAD bit in the CPSW3_CONTROL_REG register is set and if PASS_CRC is clear, otherwise they are dropped. This means that packets shorter than 64-Bytes are dropped if the PASS_CRC info bit is set regardless of P0_RX_PAD bit (packets are padded only if they are short and do not have CRC).

A RX INFO word is a contiguous block of four 32-bit data words aligned on a 32-bit word boundary.

Note

RX Control Data Words [0..2] are mapped to Host Packet Descriptor Protocol Specific Words if (TCHAN[a]_TCFG.tx_filt_pswords = 0) and (Host PD Word 1.Protocol Specific Region Location.bit[28] = 0h) and (Host PD Word 1.Protocol Specific Valid Word Count.bits[22-27] = 4h)

Figure 12-171. RX INFO Word 0 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PASS_CRC	CRC_TYPE	RESERVED					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED															

Bit	Field	Description
31-24	RESERVED	Reserved.
23	PASS_CRC	The PASS_CRC bit indicates that the CRC is passed with the packet data. 0h: CRC is not passed with packet (CRC_TYPE is don't care) 1h: CRC of type CRC_TYPE is passed with the packet.

Bit	Field	Description
22 (Host PD (Packet Descriptor) Word 1. Protocol Specific Flags: bits[27-24])	CRC_TYPE	CRC Type 0h: Ethernet CRC 1h: Castagnoli CRC
21-0	RESERVED	Reserved.

Figure 12-172. RX INFO Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											TO_PORT				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED															

Bit	Field	Description
31-21	RESERVED	Reserved.
20-16 (Host PD (Packet Descriptor) Word 3. Dest Tag Low bits[8-0])	TO_PORT	Port number to send the directed packet to. This field is set by the host. This field is valid on SOP. Directed packets go to the directed port, but an ALE lookup is performed to determine untagged egress in VLAN_AWARE mode. 0h: Not directed 1h: Send the packet to port 1. 2h: Send the packet to port 2.
15-0	RESERVED	Reserved.

Figure 12-173. RX Control Data Word 1 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMESTAMP_EN	RESERVED			DOMAIN								MSG_TYPE			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEQUENCE_ID															

Bit	Field	Description
31	TIMESTAMP_EN	When set, this bit indicates that the packet will generate a timesync event on Ethernet egress (if the CPTS is configured properly) with the associated DOMAIN, MSG_TYPE, and SEQUENCE_ID.
30-28	RESERVED	Reserved.
27-20	DOMAIN	Timesync domain.
19-16	MSG_TYPE	Timesync message type.
15-0	SEQUENCE_ID	Timesync sequence ID.

Figure 12-174. RX Control Data Word 2 Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHECKSUM_RESULT								CHECKSUM_START_BYTE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Figure 12-174. RX Control Data Word 2 Format (continued)

CHECKSUM_INV	RESERVED	CHECKSUM_BYTECOUNT

Bit	Field	Description
31-24	CHECKSUM_RESULT	This is the packet byte number where the checksum result will be placed in the egress packet. The first packet byte which is the first byte of the destination address is Byte 1 (not byte zero).
23-16	CHECKSUM_START_BYTE	This is the packet byte number to start the checksum calculation on. The first packet byte is Byte 1.
15	CHECKSUM_INV	When set, a zero checksum value will be inverted and sent as FFFFh.
14	RESERVED	Reserved.
13-0	CHECKSUM_BYTECOUNT	This is the number of bytes to calculate the checksum on. The outgoing Ethernet packet will have a checksum inserted when this value is non-zero.

Other INFO words are not taken into account.

12.3.1.4.8.3 Cut-Thru

An Ethernet port received packet can be sent cut-thru to all destination ports when the following is true:

- The CPSW3_CONTROL_REG[19] CUT_THRU_ENABLE bit is set, and
- The receive port is full duplex, and
- The Ethernet receive port speed is non-zero, and
- The packet was received on an express priority, and
- The Ethernet receive port has the remapped received packet priority enabled via the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CUT_THRU_REG[15-8] RX_PRI_CUT_THRU_EN field, and
- All Ethernet destination ports have the remapped packet priority enabled via the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_CUT_THRU_REG[7-0] TX_PRI_CUT_THRU_EN field, and
- All Ethernet destination ports are full duplex, and
- All Ethernet destination ports are express priorities, and
- All Ethernet destination ports have a non-zero CPSW_PN_SPEED_REG_k[3-0] SPEED, and
- All Ethernet destination ports are equal to or slower in speed than the Ethernet receive port, and
- The host port is not in the destination port list unless the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG[19] CUT_MODE_ETH bit is set.

Whether or not a packet actually egresses cut-thru (with or without delay) on an Ethernet destination port depends on traffic congestion on that port. Cut-thru is compatible with Intersperced Express Traffic (IET) and Enhanced Scheduled Traffic (EST).

12.3.1.4.8.3.1 Host Port Cut-Thru Operations

Packets received (CPSW ingress) on the host port are sent store-and-forward to all Ethernet destination ports. Setting the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG[19] CUT_MODE_ETH bit enables Ethernet received packets to be sent cut-thru to a destination port mask that includes the host port. The packet can egress cut-thru on Ethernet ports, but the packet will not actually egress cut-thru on the host port. Setting CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG[19] CUT_MODE_ETH can cause head of line blocking on the host priority if multiple Ethernet ports are sending to the same host port priority. The head of line blocking issue is worsened if there are differing Ethernet port speeds. Clearing the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG[19] CUT_MODE_ETH bit causes packets with the host port in the destination mask to egress store-and-forward on all egress ports.

12.3.1.4.8.3.2 Cut-Thru Error Packets

Any received packets with errors sent cut-thru from an Ethernet receive port to any Ethernet transmit port(s) will egress with at least one byte of the generated outgoing packet CRC inverted to indicate the error. This is due to the fact that cut-thru operations begin before the end of packet when the receive port determines that the packet had an error (long/code/align/CRC).

Any packet also sent cut-thru with the host included in the destination port mask will be dropped to the host (TXST_PKT_DROP) with the packet error indicated on TXST_PKT_ERR[3:0].

Any long/Jabber/Code/Align/CRC errored Ethernet received packet that is not actually sent cut-thru by the receive port will dropped unless CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is set (which if set will cause the packet to be sent to the host port with the error indicated on TXST_PKT_ERR[3:0]. If a long/Jabber/Code/Align/CRC errored Ethernet received packet is sent cut-thru by the received port then a set CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN will not cause the errored packet to be sent to the host port since the packet has already been transferred to the destination ports.

The following cut-thru notes are valid:

- Any Ethernet received packet and that is sent cut-thru to any destination port will not be dropped at any destination port due to priority maximum lengths (CPSW3_CPSW_NU_TX_PRIx_MAXLEN_REG).
- Any Ethernet received packet that is decoded as a timesync packet will be sent store-and-forward to all destination ports.
- Cut-Thru is full duplex only.
- Cut-Thru is not compatible with any form of flow control.
- Cut-Thru should not be enabled for any receive port that is in ALE bypass mode.

12.3.1.4.8.4 Port Speed

Cut-thru operations require that the Ethernet port speeds be known. Port speed can be set manually by software or be automatically determined by the hardware. A zero port speed causes the port to be disabled for cut-thru operations, but does not disable the port. The port speed values are as follows:

- 0000 – Port speed operations disabled (not a port disable)
- 0001 – 10Mpbs
- 0010 – 100Mbps
- 0011 – 1G
- 0100 – 2.5G
- 0101 – 5G
- 0110 – 10G
- 0111 through 1111 Reserved

When the CPSW_PN_SPEED_REG_k[8] AUTO_SPEED_EN bit is cleared, the port speed is written by software. When the CPSW_PN_SPEED_REG_k[8] AUTO_SPEED_EN bit is set, the port speed is automatically detected by the hardware.

12.3.1.4.8.5 CPPI Checksum Offload

The CPPI host port can be enabled to perform checksum offload on host port packet ingress and egress. UDP (User Datagram Protocol) and TCP (Transmission Control Protocol) over IPV4 and IPV6 are supported. For the purposes of checksum description, the first packet byte (the first byte of the destination address) is byte 1 (not byte 0). That is, a 64 byte packet goes from byte 1 to byte 64. For all packet types, the S_CN_SWITCH bit in the CPSW3_CONTROL_REG register must be set for the Outer VLAN L type to be supported.

12.3.1.4.8.5.1 CPPI Transmit Checksum Offload

IPV4 and IPV6 UDP and TCP packets that are received on any Ethernet port and destined for port 0 egress are checked for correct checksum as described below. The byte counts below are shown for packets with no VLAN’s. The byte counts vary with one or two packet VLAN's. Packets received on an Ethernet port with errors are not checked for a correct checksum if they are passed to the host.

12.3.1.4.8.5.1.1 IPV4 UDP

- Byte 15 Upper Nibble = 4 for IPV4
- Byte 15 Lower Nibble = IHL - Nibble with number of 32-bit words in IPV4 header (5 to 15 supported).

- Bytes 20-21 = fragment[15-0] – Bit 13 is the MF bit and bits [12-0] are the Fragment offset. A packet is a fragment if the MF bit is set or if the fragment offset is non-zero. The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets have MF=0 and a zero offset. A count is output for packet fragments but no errors are reported. First fragments have the UDP header included in the count. Middle and last fragments have only data included in the count (there is no UDP header).
- Byte 24 = 0x11 for UDP protocol.
- Received packet UDP checksum of zero means that there is no IPV4 checksum sent with the packet so no error will be issued.
- Received packet UDP checksum of 0xFFFF means that the checksum was calculated to be 0xFFFF or 0x0000 but was sent in the transmitted packet as 0xFFFF by the sending originating entity.

12.3.1.4.8.5.1.2 IPV4 TCP

- Byte 15 Upper Nibble = 4 for IPV4
- Byte 15 Lower Nibble = IHL - Nibble with number of 32-bit words in IPV4 header (5 to 15 supported).
- Bytes 20-21 = fragment[15-0] – Bit 13 is the MF bit and bits [12-0] are the Fragment offset. A packet is a fragment if the MF bit is set or if the fragment offset is non-zero. The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets have MF=0 and a zero offset. A count is output for packet fragments but no errors are reported. First fragments have the UDP header included in the count. Middle and last fragments have only data included in the count (there is no TCP header).
- Byte 24 = 0x06 for TCP protocol.

12.3.1.4.8.5.1.3 IPV6 UDP

- Byte 15 upper nibble = 6 for IPV6.
- Byte 21 = 0x11 for UDP protocol as next header.
- Fragment extension headers are supported. First fragments have a fragment extension header (byte 21 = 0x2C) followed by a UDP header (byte 55 = 0x11). Middle and last fragments have a fragment extension header followed by data only (no UDP header). The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets do not have a fragment extension header. A count is output for packet fragments but no errors are reported.
- Received packet UDP checksum of zero means that there is no IPV6 checksum sent with the packet so no error will be issued.
- Received packet UDP checksum of 0xFFFF means that the checksum was calculated to be 0xFFFF or 0x0000 but was sent in the transmitted packet as 0xFFFF by the sending originating entity.

12.3.1.4.8.5.1.4 IPV6 TCP

- Byte 15 upper nibble = 6 for IPV6.
- Byte 21 = 0x06 for TCP protocol as next header.
- Fragment extension headers are supported. First fragments have a fragment extension header (byte 21 = 0x2C) followed by a UDP header (byte 55 = 0x06). Middle and last fragments have a fragment extension header followed by data only (no TCP header). The first packet fragment has MF=1 with a zero offset. Middle fragments have MF=1 with a nonzero offset. The last packet fragment has MF=0 with a nonzero offset. Non-fragmented packets do not have a fragment extension header. A count is output for packet fragments but no errors are reported.

12.3.1.4.8.6 CPPI Receive Checksum Offload

Packets sent from host port 0 (switch ingress) to any Ethernet port can have a checksum calculated and inserted into the Ethernet egress packet. The RX_CHECKSUM_EN bit in the CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG register must be set for receive checksum operation to be enabled. When bit RX_CHECKSUM_EN is enabled, Control Data Word 2 input on CPPI receive PSI interface determines how the checksum is calculated. The CHECKSUM_RESULT field in Control Data Word 2 determines where the checksum is inserted. The checksum result location is adjusted by the egress port if a VLAN is to be inserted or removed on Ethernet port egress.

12.3.1.4.8.7 Egress Packet Operations

Each CPSW egress port (Ethernet and Host) is capable of performing egress packet processing operations (CPSW3_CPSW_NU_ALE_EGRESSOP). IntraVLAN processing either adds, removes, or replaces VLAN information or does nothing. InterVLAN routing allows hardware routing between a limited number of VLANs - thereby allowing high-bandwidth or other routing operations to be offloaded from software to the CPSW (hardware). IntraVLAN processing and InterVLAN routing operations are mutually exclusive. In addition, the packet source and destination addresses can be swapped on egress to facilitate OAM or generic testing operations.

12.3.1.4.9 MII Management Interface (MDIO)

The MII Management interface module implements the 802.3 serial management interface to interrogate and control external Ethernet PHY using a two-wire bus.

12.3.1.4.9.1 MDIO Frame Formats

Table 12-214 shows the address, Table 12-215 shows the read format and Table 12-216 shows the write format of the supported Clause 45 MII Management interface frames. Post-increment accesses are not supported.

Table 12-214. MDIO Clause 45 Address Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	00	AAAAA	RRRRR	10	AAAA.AAAA.AAAA.AAAA

Table 12-215. MDIO Clause 45 Read Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	11	AAAAA	RRRRR	Z0	DDDD.DDDD.DDDD.DDDD

Table 12-216. MDIO Clause 45 Write Frame Format

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
FFFF FFFFh	00	01	AAAAA	RRRRR	10	DDDD.DDDD.DDDD.DDDD

The default or idle state of the two wire serial interface is a logic one. All tri-state drivers should be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic 1. Prior to initiating any other transaction, the station management entity shall send a preamble sequence of 32 contiguous logic 1 bits on the MDIO line with 32 corresponding cycles on MDCLK to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding MDCLK cycles before it responds to any other transaction. The MDIO CPSW3_MDIO_USER_ADDR0_REG register must be written before a read or write operation is performed to set the address used in the operation. Each read or write operation has a preceeding address frame.

Preamble

The start of a frame is indicated by a preamble, which consists of a sequence of 32 contiguous bits all of which are a 1. This sequence provides the PHY a pattern to use to establish synchronization. The preamble is required in clause 45 operation.

Start Delimiter

The preamble is followed by the start delimiter which is indicated by a 00 pattern.

Operation Code

The operation code for an address transaction is 00. The operation code for a read is 11, while the operation code for a write is a 01.

PHY Address

The PHY address is 5 bits allowing 32 unique values. The first bit transmitted is the MSB of the PHY address.

MMD Number

The MMD number is the 5 bits allowing 32 unique values. The first bit transmitted is the MSB.

Turnaround

An idle bit time during which no device actively drives the MDIO signal shall be inserted between the register address field and the data field of a read frame in order to avoid contention. During a read frame, the PHY shall drive a zero bit onto MDIO for the first bit time following the idle bit and preceding the Data field. During a write frame, this field shall consist of a one bit followed by a zero bit.

Address

The address field is 16 bits on address operations. The first bit transmitted is the MSB of the address word. Each read/write operation initiated has an automatic address operation initiated first that uses the MDIO CPSW3_MDIO_USER_ADDR0_REG/ CPSW3_MDIO_USER_ADDR1_REG register values as the 16-bit address.

Data

The Data field is 16 bits on read and write operations. The first bit transmitted and received is the MSB of the data word.

12.3.1.4.9.2 MDIO Functional Description

The MII Management I/F will remain idle until enabled by setting the ENABLE bit in the CPSW3_MDIO_CONTROL_REG register. The MII Management I/F will then continuously poll the link status from within the Generic Status Register of all possible 32 PHY addresses in turn recording the results in the MDIO CPSW3_MDIO_LINK_REG register. Individual PHY's can be enabled or disabled for polling the associated bit in the CPSW3_MDIO_POLL_EN_REG register. The CPSW3_MDIO_LINK_REG and CPSW3_MDIO_ALIVE_REG register bit values are updated on the poll of each PHY. The LINKSEL bit in the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k register determines the status input that is used. A change in the link status of the two PHYs being monitored will set the appropriate bit in the MDIO CPSW3_MDIO_LINK_INT_RAW_REG register and the MDIO CPSW3_MDIO_LINK_INT_MASKED_REG register, if enabled by the LINKINT_ENABLE bit in the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k register.

The MDIO CPSW3_MDIO_ALIVE_REG register is updated by the MII Management I/F module if the PHY acknowledged the read of the generic status register. In addition, any PHY register read transactions initiated by the host also cause the MDIO CPSW3_MDIO_ALIVE_REG register to be updated.

At any time, the host can define a transaction for the MII Management interface module to undertake using the DATA, PHYADR, REGADR, and WRITE fields in a CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register. When the host sets the GO bit in this register, the MII Management interface module will begin the transaction without any further intervention from the host. Upon completion, the MII Management interface will clear the GO bit and set the USERINTRAW field in the CPSW3_MDIO_USER_INT_RAW_REG register corresponding to the CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register being used. The corresponding bit in the CPSW3_MDIO_USER_INT_MASKED_REG register may also be set depending on the mask setting in the MDIO CPSW3_MDIO_USER_INT_MASK_SET_REG and CPSW3_MDIO_USER_INT_MASK_CLEAR_REG registers. A round-robin arbitration scheme is used to schedule transactions that may be queued by the host in different CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k registers. The host should check the status of the GO bit in the MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register before initiating a new transaction to ensure that the previous transaction has completed. The host can use the ACK bit in the MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register to determine the status of a read transaction.

It is necessary for software to use the MII Management interface module to setup the auto-negotiation parameters of each PHY attached to a MAC port, retrieve the negotiation results, and setup the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG register in the corresponding MAC.

12.3.1.5 CPSW0 Programming Guide

12.3.1.5.1 Initialization and Configuration of CPSW Subsystem

To configure the CPSW Ethernet Subsystem for operation, the host must perform the following:

1. Select the Interface (RMII, or RGMII) Mode. See the ENET1_CTRL and ENET2_CTRL[2-0] PORT_MODE_SEL fields.
2. Configure pads (pin muxing), as per the interface selected. Refer to *Pad Configuration Registers* and the device-specific data sheet.
3. Enable the CPSW Ethernet Subsystem clocks. See *CPSW Integration*
4. Ensure that at least 2000 CPPI_ICLK periods are run after reset is de-asserted.

5. Configure the CPSW3_CONTROL_REG register
6. Configure the Ethernet Port Source Address registers (CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_SA_L_REG_k and CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_SA_H_REG_k)
7. Configure the CPSW statistic port enable register CPSW3_CPSW_NU_STAT_PORT_EN_REG
8. Configure the ALE (Section 12.3.1.4.6.1, *Address Lookup Engine*)
9. Configure the MDIO (Section 12.3.1.5.3.1, *Initializing the MDIO Module*)
10. Configure Ethernet port, as per the desired mode of operations

12.3.1.5.2 CPSW Reset

To reset the Ethernet port, the host must perform the following:

1. Set CMD_IDLE bit to 1h in the Ethernet port control register: CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_CONTROL_REG.
2. Wait for IDLE bit to be set to 1h, which is indicated in the Ethernet port status register: CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_STATUS_REG.
3. Set SOFT_RESET bit to 1h in the Ethernet port software reset register: CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_SOFT_RESET_REG.
4. Wait for SOFT_RESET bit in the CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_SOFT_RESET_REG registers to be cleared to confirm reset completion.
5. Configure the Ethernet ports.
6. Re-configure registers reset to default value by CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_i_PN_MAC_SOFT_RESET_REG.

12.3.1.5.3 MDIO Software Interface

12.3.1.5.3.1 Initializing the MDIO Module

The following steps are performed by the application software or device driver to initialize the MDIO device:

1. Configure the PREAMBLE and CLKDIV bits in the MDIO Control register (CPSW3_MDIO_CONTROL_REG).
2. Enable the MDIO module by setting the ENABLE bit in CPSW3_MDIO_CONTROL_REG.
3. The MDIO PHY alive status register (MDIO CPSW3_MDIO_ALIVE_REG) can be read in polling fashion until a PHY connected to the system responded, and the MDIO PHY link status register (MDIO CPSW3_MDIO_LINK_REG) can determine whether this PHY already has a link.
4. Set the appropriate PHY addresses in the MDIO user PHY select register (CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k, where k = 0 or 1), and set the LINKINT_ENABLE bit to enable a link change event interrupt if desirable.
5. Set the appropriate LINKSEL bit in the CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_k register (where k = 0 or 1).
6. Set the appropriate USERINTMASKSET bit field in the CPSW3_MDIO_USER_INT_MASK_SET_REG register.
7. If an interrupt on general MDIO register access is desired, set the corresponding bit in the MDIO user command complete interrupt mask set register (MDIO CPSW3_MDIO_USER_INT_MASK_SET_REG) to use the MDIO user access register (MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k, where k = 0 or 1).

12.3.1.5.3.2 Writing Data To a PHY Register

The MDIO module includes a user access register (MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k, where k = 0 or 1) to directly access a specified PHY device.To write a PHY register, perform the following:

1. Check to ensure that the GO bit in the MDIO user access register (MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k) is cleared.
2. Write to the GO, WRITE, REGADR, PHYADR, and DATA bits in MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k corresponding to the PHY and PHY register SW wants to write.

3. The write operation to the PHY is scheduled and completed by the MDIO module. Completion of the write operation can be determined by polling the GO bit in MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k for a 0.
4. Completion of the operation sets the corresponding USERINTRAW bit (0 or 1) in the MDIO user command complete interrupt register (CPSW3_MDIO_USER_INT_RAW_REG) corresponding to MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k used. If interrupts have been enabled on this bit using the MDIO user command complete interrupt mask set register (CPSW3_MDIO_USER_INT_MASK_SET_REG), then the bit is also set in the MDIO user command complete interrupt register (CPSW3_MDIO_USER_INT_MASKED_REG) and an interrupt is triggered on the host processor.

12.3.1.5.3.3 Reading Data From a PHY Register

The MDIO module includes a user access register (MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k, where k = 0 or 1) to directly access a specified PHY device. To read a PHY register, perform the following:

1. Check to ensure that the GO bit in the MDIO user access register (CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k, where k = 0 or 1) is cleared.
2. Write to the GO, REGADR, and PHYADR bits in the CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register corresponding to the PHY and PHY register SW wants to read.
3. The read data value is available in the DATA bit field in MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register after the module completes the read operation on the serial bus. Completion of the read operation can be determined by polling the GO and ACK bits in CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k register. After the GO bit has cleared, the ACK bit is set on a successful read.
4. Completion of the operation sets the corresponding USERINTRAW bit (0 or 1) in the MDIO user command complete interrupt register (CPSW3_MDIO_USER_INT_RAW_REG) corresponding to MDIO CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_k used. If interrupts have been enabled on this bit using the MDIO user command complete interrupt mask set register (CPSW3_MDIO_USER_INT_MASK_SET_REG), then the bit is also set in the MDIO user command complete interrupt register (CPSW3_MDIO_USER_INT_MASKED_REG) and an interrupt is triggered on the host processor.

12.3.2 Universal Serial Bus Subsystem (USBSS)

This section describes the Universal Serial Bus Subsystem (USBSS) in the device.

12.3.2.1 USB Overview

USB (Universal Serial Bus) provides a low-cost connectivity solution for numerous consumer portable devices by implementing a mechanism for data transfer between USB devices.

The device instantiates two independent instances of a third-party USB subsystem (USB2SS) operating at up to USB2.0 speeds (480Mb/s), either of which can be independently configured to act as a USB Host or a USB Device. SuperSpeed (5.0 Gb/s) operation is not supported in either operational mode.

12.3.2.1.1 USB Features

The USB 2.0 subsystem supports the following USB Features:

- Operational modes:
  - Supports USB 2.0 Host mode at High-Speed (HS, 480 Mbps), Full-Speed (FS, 12 Mbps), and Low-Speed (LS, 1.5 Mbps)
  - Supports USB 2.0 Device mode at High-Speed (HS, 480 Mbps), and Full-Speed (FS, 12 Mbps). Low-Speed is not supported in Device mode.
  - Supports all modes of transfers - Control, Bulk, Interrupt, and Isochronous.
- A DRD (Dual-Role-Device - Host or Device) USB controller with the following features:
  - Compatible to the xHCI 1.0 specification in Host mode
  - Compatible with the USB 2.0 specification in Device mode
  - Supports 15 IN (Receive), 15 OUT (Transmit) endpoints (EPs), and one EP0 endpoint which is bidirectional
  - Internal DMA controller
  - Descriptor caching and data pre-fetching ensures high performance
  - Dynamic FIFO memory allocation for all endpoints
- Operation flexibility
  - Same programming model for HS, FS, and LS operation
  - Each controller instance can provide either USB Host or USB Device functionality

12.3.2.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

12.3.2.2 USB Environment

12.3.2.2.1 USB Pin List

The names of the pins used by the USB2SS with descriptions are shown in Table 12-217 and Table 12-218.

Table 12-217. USB Signal Pins Description

Pin Name	I/O[1]	Description
USBn_DP	I/O	USB 2.0 and 1.1 Specification-compliant signal pins. They are HS/FS/LS bidirectional differential data pins.
USBn_DM	I/O	

(1) I = Input, O = Output, A = Analog

Table 12-218. USB Control, Configuration, and Monitor Signal Pins

Pin Name	I/O[1]	Description
USBn_DRVVBUS	O	An active-high digital output signal for VBUS power supply. Used to enable an external charge pump to supply +5V power to the VBUS receptable when operating in USB Host mode.
USBn_VBUS[2]	A/I	An analog input for monitoring the voltage on VBUS.

Table 12-218. USB Control, Configuration, and Monitor Signal Pins (continued)

Pin Name	I/O[1]	Description
USBn_ID	I	USB operational mode identifier. This functionality is supported via GPIO.

(1) I = Input, O = Output, A = Analog
(2) This pin is not 5V tolerant. Refer to the device-specific datasheet for implementation requirements.

12.3.2.2.2 Typical Pin Connections of Device

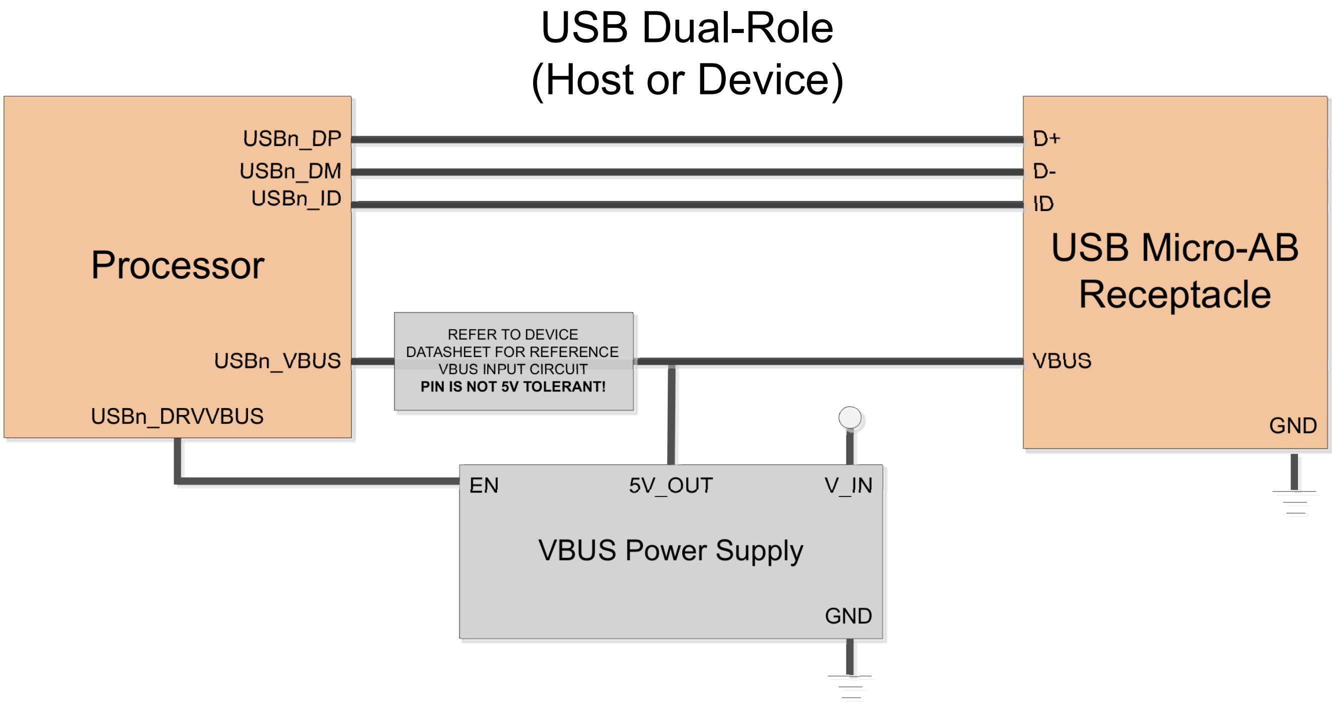


Figure 12-175. USB Dual-Role Connections

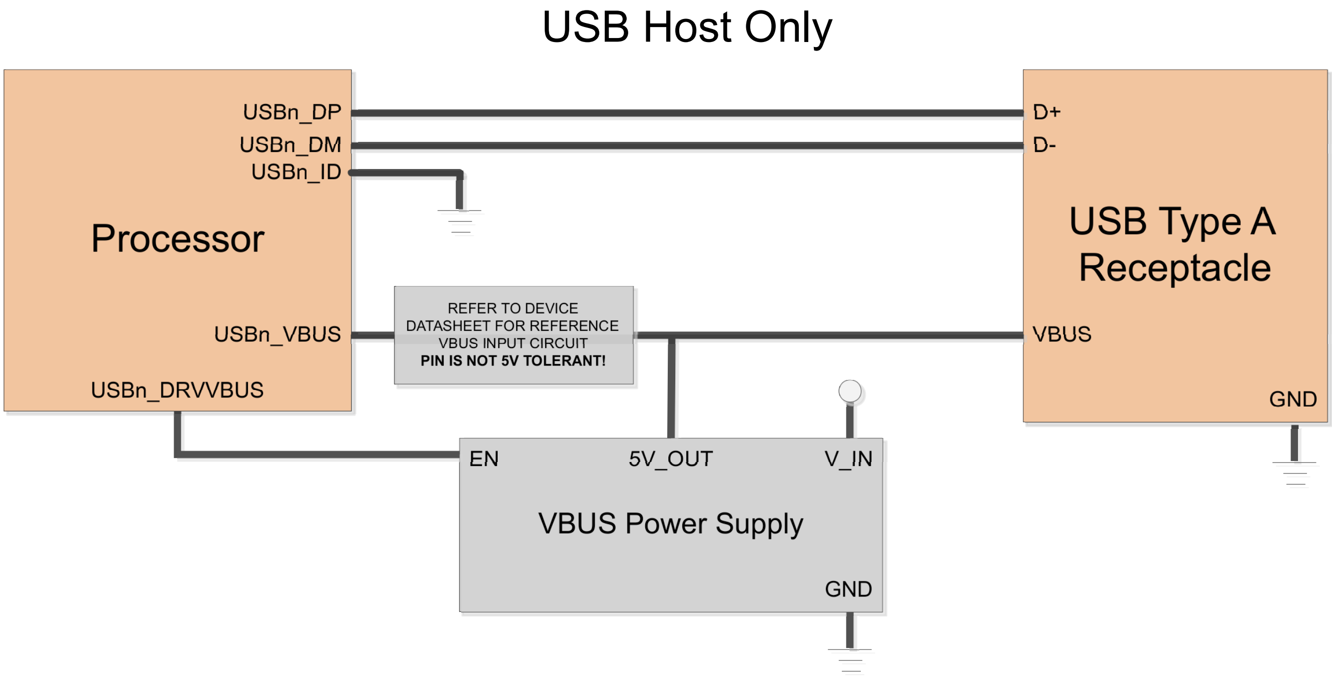


Figure 12-176. USB Host-Only Connections

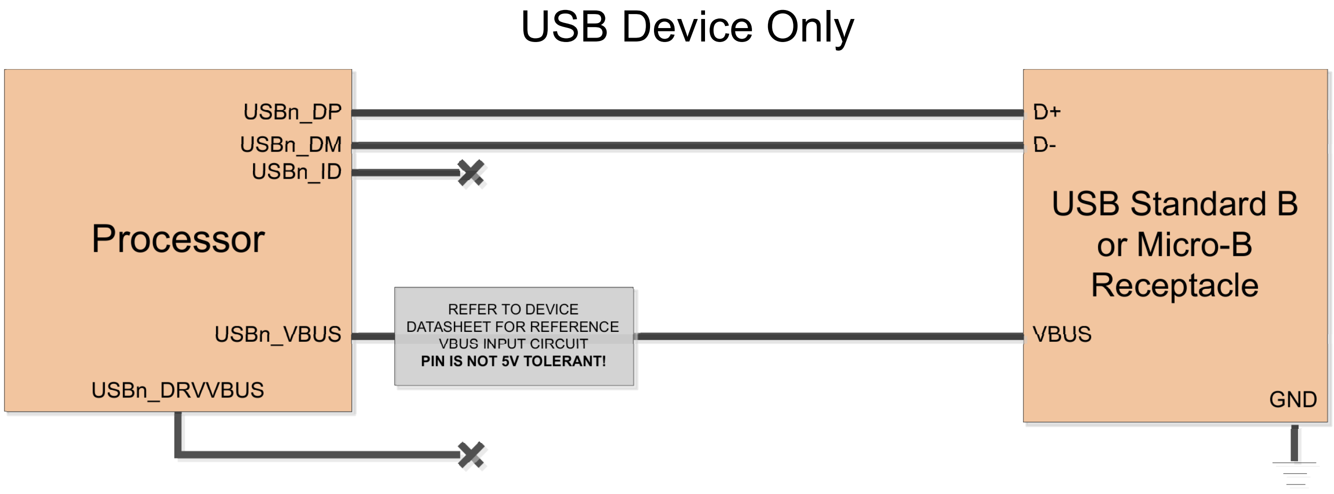


Figure 12-177. USB Device-Only Connections

12.3.2.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.3.2.4 Use Cases

This is a standard USB 2.0 module, and is optimized for following applications and systems:

- Portable electronic devices
- High-bandwidth applications

It supports all typical USB connections, and Table 12-219 shows some examples.

Table 12-219. Typical Use Cases In Terms of Connections

Connectors (Receptacle)	Signals to Use	SS	HS/FS	LS (Host only)	Comments
USB 2.0 Micro-AB	DP, DM, VBUS, ID	N	Y	Y	Support Host or Device operation, depending on state of the ID pin.
USB 2.0 Type-A	DP, DM, VBUS	N	Y	Y	Support HS/FS/LS Host
USB 2.0 Type-B	DP, DM, VBUS	N	Y	Y	Only used for USB2.0 Device (no LS)

12.3.2.4.1 USB Operational Mode Determination

USB[n]_ID Pin	USB[n]_VBUS Pin(1)	USB Role
FLOAT	FLOAT or GROUND	INDETERMINATE
GROUND	UNUSED	HOST
FLOAT	RAIL VOLTAGE	DEVICE

(1) PHY VBUS pin voltage is dependent on the divider circuit used on the board. Refer to the device datasheet for VBUS implementation requirements.

12.3.2.4.2 VBUS Voltage Sourcing Control

When either of the USB controllers assumes the role of a host, the controller is required to supply 5V to an attached device through its VBUS line. In order to achieve this task, the USB controller requires the use of external power logic (or a charge pump) capable of sourcing 5V power. The USB_DRVVBUS pin is used as a control signal to enable/disable this external power logic to either source or disable power on the VBUS line. The control on the USB_DRVVBUS is handled by the controller based on host software programming. The control should be transparent to the user so long as the proper hardware connection and software initialization are in place. The USB controller drives the USB_DRVVBUS signal high when it assumes the role of a host while the controller is in session. When assuming the role of a device, the controller drives the USB_DRVVBUS signal low disabling the external charge pump/power logic; hence, no power is driven on the VBUS line (in this case, power is expected to be provided by the external host).

Note that both USB controllers are self-powered and the device does not rely on the voltage on the VBUS line sourced by an external host for controller operation when assuming the role of a device. The voltage present on the VBUS line is used to identify the presence of a Host. The USB PHY continually monitors the voltage on the VBUS and reports the status to USB controller.

12.3.2.4.3 VBUS Detection

VBUS detection is supported by the USB2SS via the USB_VBUS pin, but **it is important that this pin not be connected directly to the connector 5V or any other 5V source.** Instead, an external circuit must be used to ensure that the recommended operating conditions of the pin are not exceeded. Refer to the device datasheet for requirements and example VBUS-sense circuitry.

The PHY includes session valid and VBUS valid comparators and provides corresponding status signals.

The Controller uses the session valid output from the PHY in device mode. One of the reasons is because the USB specification requires that the DP pull-up (implemented inside the PHY) must be be enabled only after VBUS is turned on by host. This PHY output also in general indicates that a connection is active from host and it can also be used to detect disconnects.

The USB2SS wrapper also includes logic to detect a change on session valid and VBUS valid outputs from PHY.

12.3.2.4.4 Pull-up/Pull-down Resistors

As the USB controllers are dual role controllers, capable of assuming a role of a host or device, the required pull-up/pull-down resistors cannot exist external to the device. These pull-up/pulldown resistors exist internal to the device, within the PHY to be more specific, and are enabled or disabled based on the role the controller assumes allowing for dynamic hardware configuration. When assuming the role of a host, the data lines are pulled low by the PHY enabling the internal 15KΩ resistors. When assuming the role of a device the required 1.5KΩ pull-up resistor on the D+ line is enabled automatically to signify the USB capability to the external host as a FS device (HS operation is negotiated during reset bus condition). Low-Speed Device functionality is not supported.

12.4 Memory Interfaces

This section describes the memory interfaces in the device.

12.4.1 Flash Subsystem (FSS)

The device contains two flash subsystems where:

- FSS0 supports Octal-SPI flash with XIP
  – See *Flash Subsystem 0 (FSS0)*, *OSPI Features*, and *OSPI Not Supported Features* for list of all features
- FSS1 supports Octal flash or HyperRAM
  – With Hyberbus for interconnect with HyperRAM
  – Provides access to external flash devices via OSPI
  – Review *Flash Subsystem 1 (FSS1)* for list of all features

The FSS implementation can support the following interfaces:

- Two OSPIs with:
  – FSS0 as FSS0_OSPI0 (also known as OSPI0)
  – FSS1 as FSS1_OSPI_0 (also known as OSPI1)
- One OSPI and one HyperRAM with
  – FSS0 as OSPI0
  – FSS1 as HyperRAM
- These Mode of Operations are also described in Table 12-220

Table 12-220. FSS Allowed Interface Combinations

Combination	FSS0	FSS1
1	FSS0_OSPI0	Not Used
2	FSS0_OSPI0	FSS1_OSPI0
3	Not Used	FSS1_OSPI0
4	FSS0_OSPI0	HyperBus Interface
5	Not Used	HyperBus Interface

12.4.1.1 Flash Subsystem 0 (FSS0)

This sub-section describes the FSS0 in the device.

12.4.1.1.1 FSS Overview

The Flash Subsystem (FSS) provides access to external Flash devices via Octal Serial Peripheral Interface (OSPI). FSS0 includes one OSPI. For more information, see *Octal Serial Peripheral Interface (OSPI)*.

Figure 12-178 shows a high level FSS block diagram

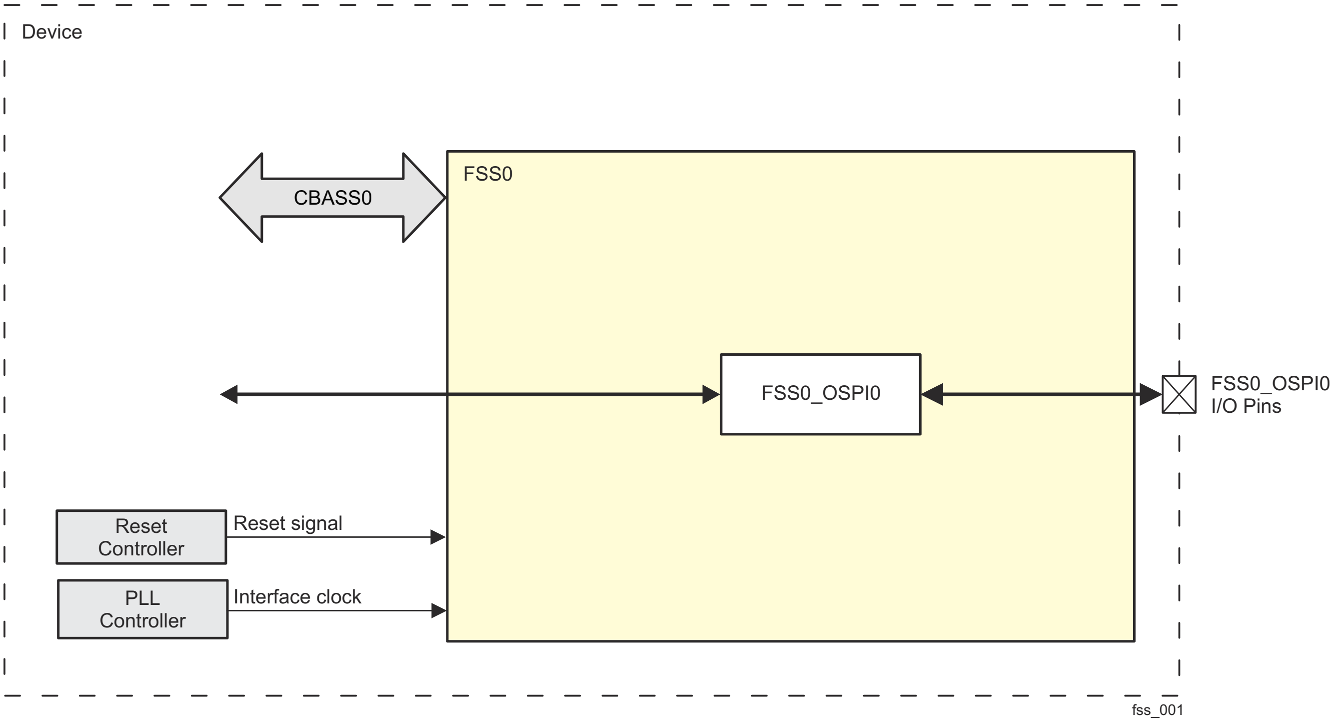


Figure 12-178. FSS Overview

12.4.1.1.2 FSS Environment

This section refers to FSS0 (aka fss_of_ul) as FSS.

12.4.1.1.2.1 FSS Typical Application

Figure 12-179 shows typical FSS application.

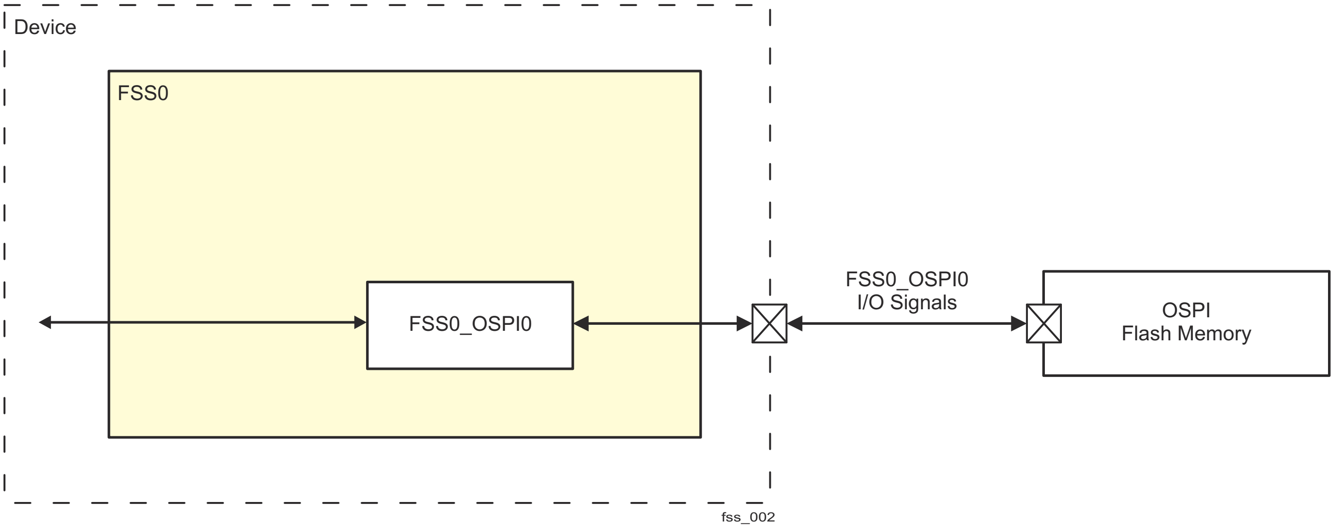


Figure 12-179. FSS Typical Application

FSS I/O Signals describes the FSS I/O signals.

Table 12-221. FSS I/O Signals

FSS0 Interface	I/O Signals
FSS0_OSPI0	For more information about OSPI I/O signals, see *OSPI Environment*.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.4.1.1.3 FSS Functional Description

12.4.1.1.3.1 FSS Block Diagram

Figure 12-180 shows the FSS block diagram.

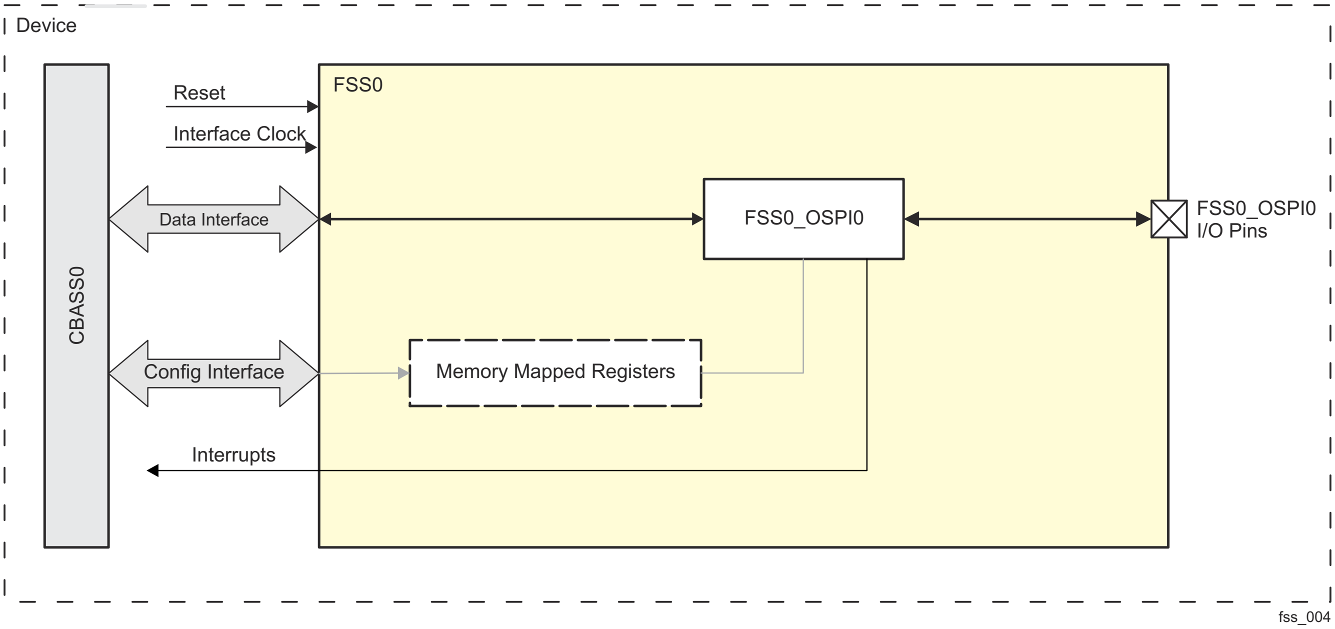


Figure 12-180. FSS Block Diagram

FSS Blocks:

- CBASS0: The CBASS0 interconnect allows FSS to communicate with the device modules and subsystems.
- Data Interface: It is 64-bit data/32-bit address multi issue data interface with coherent in-band bypass. It provides accessibility to the FSS0_OSPI0.
- Config Interface: It is used for configuration of the memory mapped registers within the FSS.
- For more information about Interface Clock, Resets, and Interrupts, see *Flash Subsystem (FSS)* in *Module Integration*
- Memory Mapped Registers: This block includes the FSS registers. The configuration of these registers defines which FSS features are used. For more information, see *Memory Interfaces Registers*.
- FSS0_OSPI0: For more information about OSPI, please see *Octal Serial Peripheral Interface (OSPI)*.
- FSS0_OSPI0 I/O Pins: For more information, see *OSPI I/O Signals*.

12.4.1.1.3.2 FSS Regions

12.4.1.1.3.2.1 FSS Regions Boot Size Configuration

The boot size for FSS defaults to 64 MB but can be configured to be 128 MB. Selection of boot block which will be used is also configurable. For more information see FSS0_CTRL0 register in *CTRL_MMR Registers*.

12.4.1.1.3.2.2 FSS Memory Regions

Section 12.4.1.1.3.2.2 shows the FSS memory regions.

Table 12-222. FSS Memory Regions

Address Range	Size	Description
0x4 0000 0000 - 0x4 FFFF FFFF	4 GB	External Memory Space (Region 0)
0x0 6000 0000 - 0x0 67FF FFFF	128 MB	Boot Space (Region 1)
0x5 0000 0000 - 0x5 FFFF FFFF	4 GB	External Memory Space (Region 3)

12.4.1.2 Flash Subsystem 1 (FSS1)

This sub-section describes the FSS1 in the device. The sub-section refers to FSS1 as FSS.

12.4.1.2.1 FSS1 Overview

The Flash Subsystem (FSS) provides access to external flash devices via Octal SPI (OSPI) and HyperBus™ interface along with encryption/decryption, authentication, and in-line ECC protection.

The FSS path has access to either OSPI or HyperBus interface and be configures for ECC, authentication, or both.

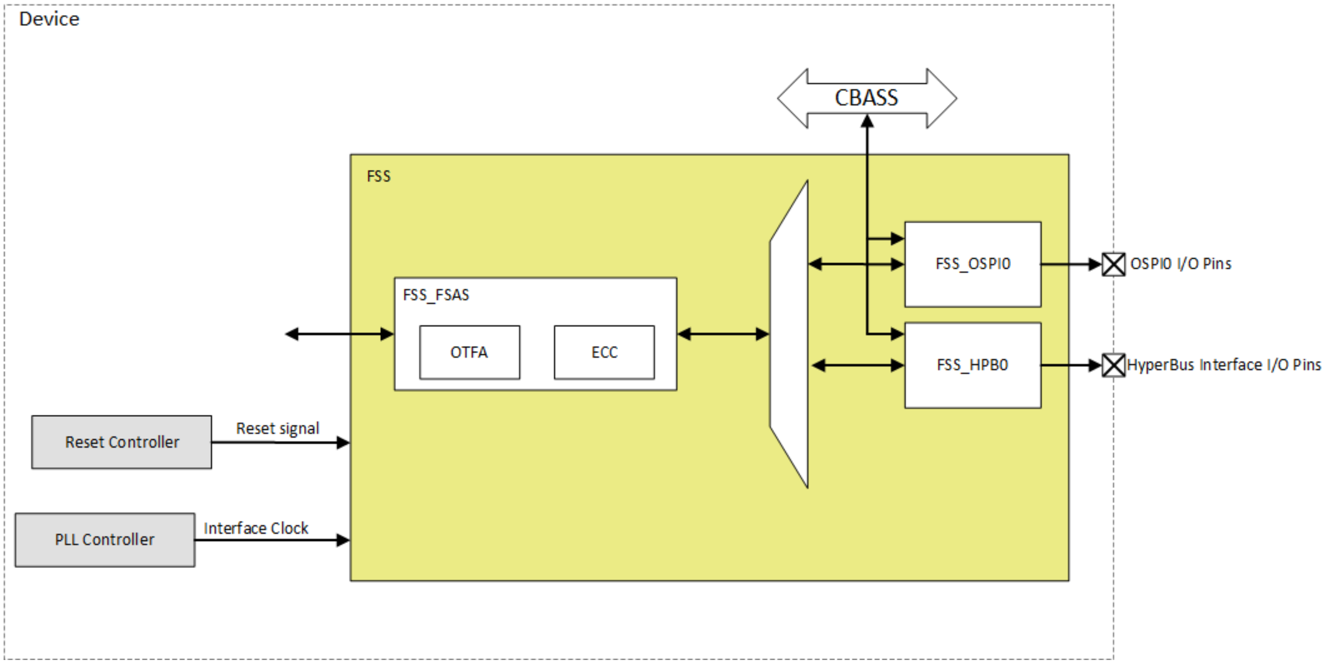


Figure 12-181. FSS Overview

12.4.1.2.1.1 FSS1 Features

The FSS has the following features:

- Two different flash interfaces:
  - OSPI (FSS1_OSPI0) OR
  - HyperBus interface
- OSPI0/HyperBus interface supports:
  - Execute in place (XIP) operation
  - 32-byte block copy (BC) operation
- OSPI support single, dual, quad, or octal SPI devices
- OSPI support up to 4 devices
- HyperBus interface supports up to 2 devices
- The OSPI and HyperBus interface have independent power management for low power operations

For more information, see *OSPI Unsupported Features*.

12.4.1.2.2 FSS Typical Application

Figure 12-182 show typical FSS applications.

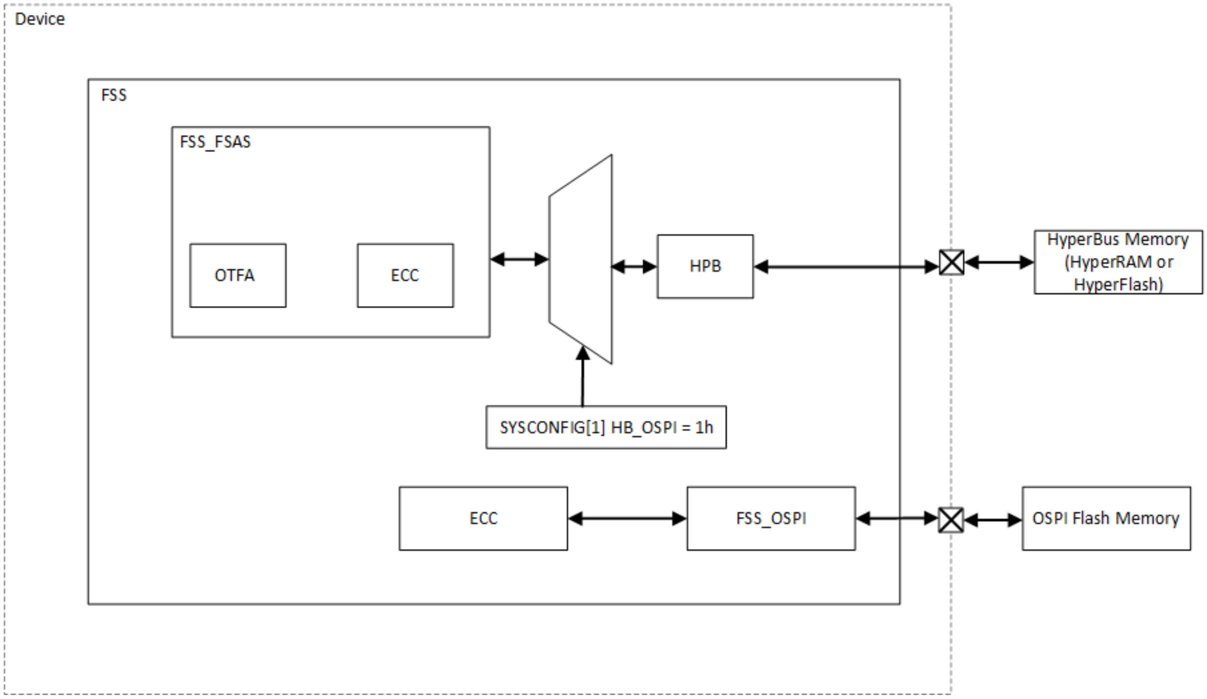


Figure 12-182. FSS Typical Application - HyperBus and OSPI

Section 12.4.1.2.2 describes the FSS I/O signals.

Table 12-223. FSS I/O Signals

FSS Interface	I/O Signals
OSPI	For more information about OSPI I/O signals, see *OSPI I/O Signals*.
HyperBus interface	For more information about HyperBus interface I/O signals, see *HyperBus I/O Signals*.

Note

For more information on the OSPI environment, see *OSPI Environment*.

For more information on the HyperBus environment, see *HyperBus Environment*.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.4.1.2.3 FSS Functional Description

12.4.1.2.3.1 FSS Block Diagram

The FSS provides access to external Flash and RAM devices. It supports XIP (Execute-in-Place) and BC (Block Copy) operations. The FSS consists of one OSPIs and one HyperBus interface.

Figure 12-183 shows the FSS block diagram

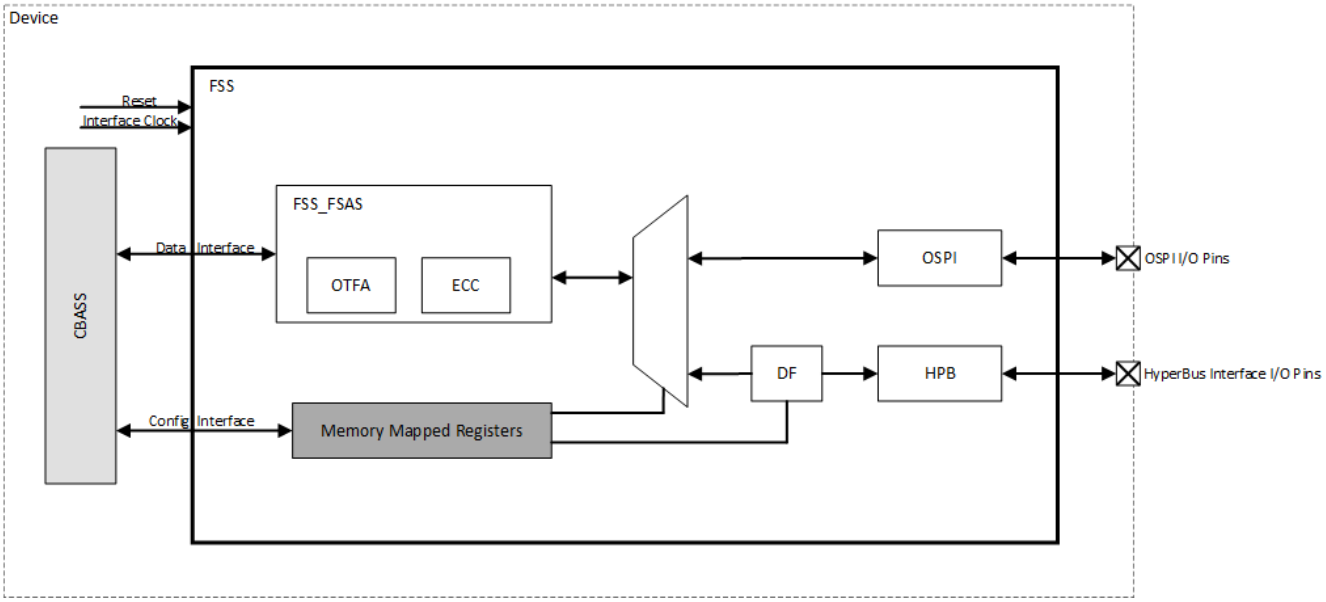


Figure 12-183. FSS Block Diagram

FSS Blocks:

- CBASS: The CBASS interconnect allows FSS to communicate with the device modules and subsystems.
- Data Interface (FSS): It is 64-bit data/32-bit address multi issue data interface with coherent in-band bypass. It provides accessibility to either the OSPI or HyperBus interface.
- Config Interface: It is used for configuration of the memory mapped registers within the FSS.
- For more information about Interface Clock, Resets, and Interrupts, see *Flash Subsystem (FSS)* in *Module Integration*
- Memory Mapped Registers: This block includes the FSS registers. The configuration of these registers defines which FSS features are used. For more information, see *Memory Interface Registers*.
- MUX: The Muxing (MUX) block is used as a software controlled switch in the interface. It defines which interface to be used (OSPI or HyperBus interface). The MUX block can switch only when the traffic is idle. The software has responsibility to cause the traffic to be stopped.
- DF: The Dynamic Fragmenter (DF) module is responsible for fragmenting write data to the flash region so that all writes to the flash region are done in 16-bits chunks (a requirement for HyperFlash). It passes all other transaction through unaffected.
- FSS Interfaces:
  - OSPI: Octal Serial Peripheral Interface. For more information, see *OSPI I/O Signals*
  - HPB: HyperBus interface. For more information, see *HyperBus I/O Signals*

12.4.1.2.3.2 FSS ECC Support

The Error Correcting Code (ECC) is a mechanism for providing increased system reliability via reduction of memory software errors by allowing single bit errors to be detected and corrected (SEC) and double bit errors to be detected (DED).

For more information about ECC, refer to *ECC Aggregator*.

For FSS1 path when the stand-alone ECC module is used:

- The input for the ECC module is 32-byte data block.

- The ECC module generates ECC codes for the 32-byte data block.
- The ECC module packs data + ECC, reformats the address and sends this to the flash controller (OSPI1 flash controller).

For more information, see *ECC Calculation*.

12.4.2 Octal Serial Peripheral Interface (OSPI)

This section describes the Octal Serial Peripheral Interface (OSPI) module for the device.

12.4.2.1 OSPI Overview

The Octal Serial Peripheral Interface (OSPI) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device controller at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

Figure 12-184 shows the OSPI module overview.

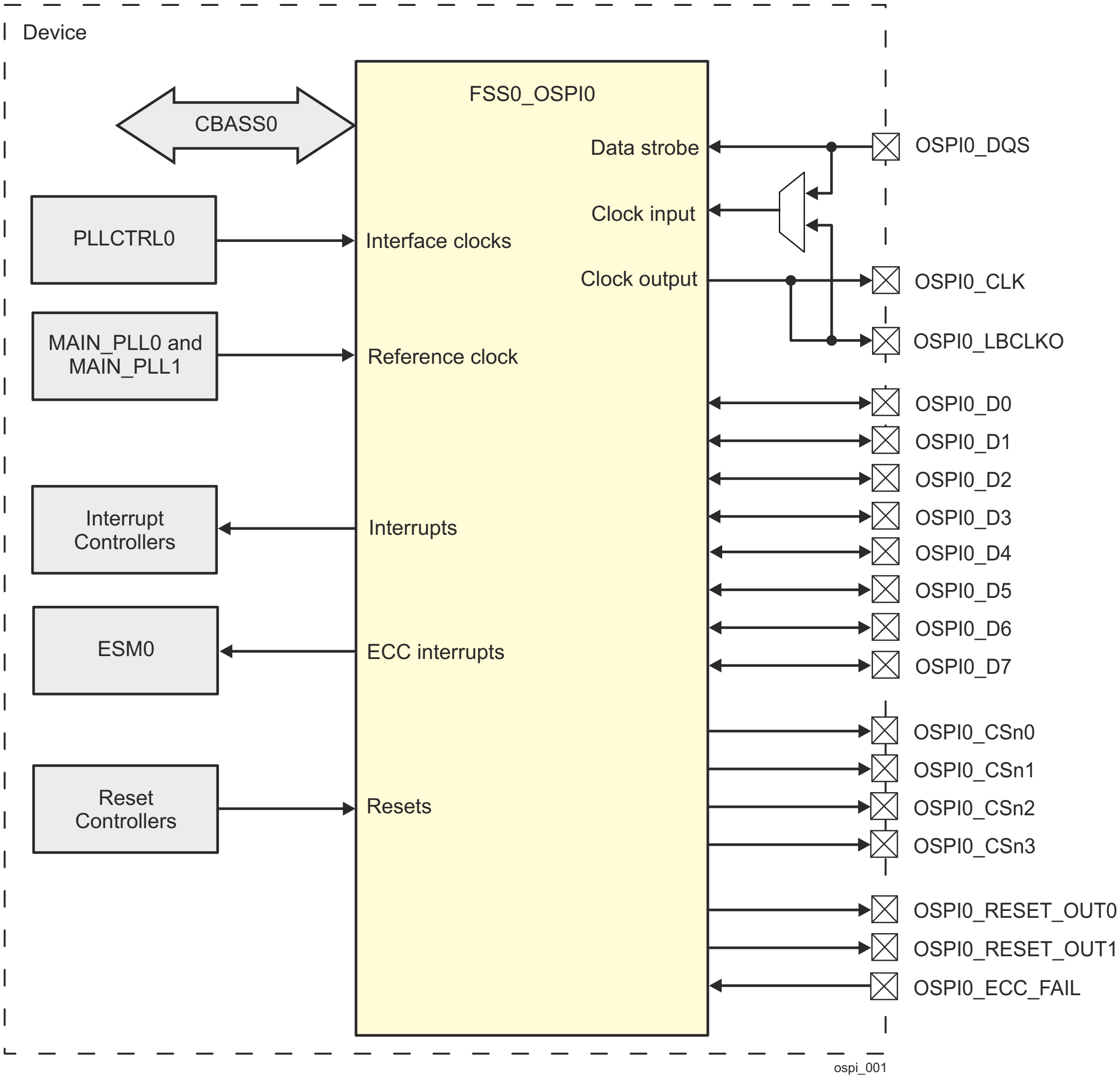


Figure 12-184. OSPI Overview

12.4.2.1.1 OSPI Features

The OSPI module has the following features:

- Support for single, dual, quad (QSPI mode) or octal I/O bus widths.
- Memory mapped ‘direct’ mode of operation for performing flash data transfers and executing code from flash memory.
- Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers.
- Local SRAM of configurable size to reduce advanced high-performance bus overhead and buffer flash data during indirect transfers.
- Set of software advanced peripheral bus accessible flash control registers to perform any flash command, including data transfers up to 8-bytes at a time.
- Additional addressable memory bank to accommodate more than 8-bytes at a time.
- Support for XIP, sometimes referred to as continuous mode.
- Programmable device sizes.
- Programmable write protected regions to block system writes from taking effect.
- Programmable delays between transactions.
- Legacy mode allowing software direct access to low level transmit and receive FIFOs, bypassing the higher layer processes.
- An independent reference clock to decouple bus clock from SPI clock – allows slow system clocks.
- Programmable baud rate generator to generate OSPI clocks.
- Features included to improve high speed read data capture mechanism.
- Option to use adapted clocks or DQS to further improve read data capturing.
- Programmable interrupt generation.
- Up to four external device selects - OSPI and QSPI devices can be mixed
- Programmable data decoder, enables continuous addressing mode for each of the connected devices and auto-detection of boundaries between devices.
- Supports BOOT mode.
- Bidirectional CRC on Multiple-SPI interface.
- Handling ECC errors for flash devices with embedded correction engine.
- Full integration with PHY module dedicated to more flexible and power efficient transfers.
- Supports RESET_OUT[1-0] and ECC_FAIL pins for external flash devices where ECC is checked on the flash.

12.4.2.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.4.2.2 OSPI Environment

The FSS0_OSPI0 module is hereinafter referred to as OSPI module.

This section describes the OSPI external connections (environment).

The OSPI module is primarily intended for fast booting from Octal- and Quad-SPI flash memories. Figure 12-185 shows a typical connection of the OSPI module to an external Octal-SPI flash memory.

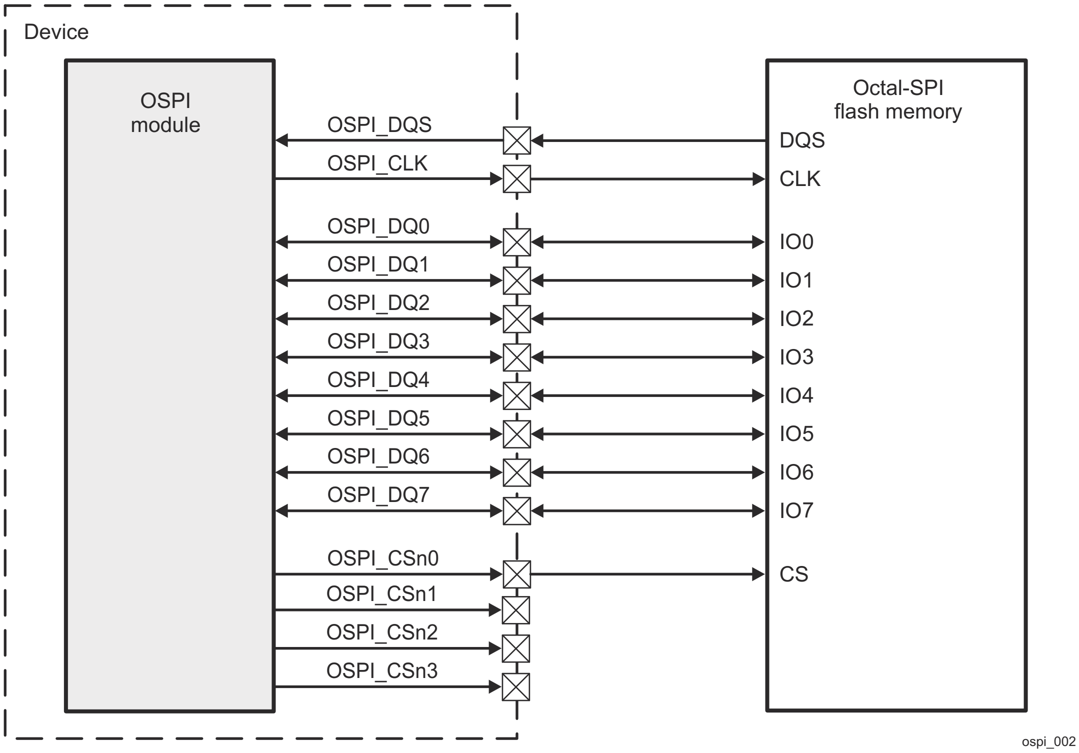


Figure 12-185. OSPI Connected to an External Octal-SPI Flash Memory

Table 12-224 lists and describes the FSS0_OSPI I/O signals.

Table 12-224. OSPI I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
			FSS0_OSPIi(4)	
DQ0	OSPIi(4)_D0	IO	FSS0_OSPIi(4) data input/output 0	HiZ
DQ1	OSPIi(4)_D1	IO	FSS0_OSPIi(4) data input/output 1	HiZ
DQ2	OSPIi(4)_D2	IO	FSS0_OSPIi(4) data input/output 2	HiZ
DQ3	OSPIi(4)_D3	IO	FSS0_OSPIi(4) data input/output 3	HiZ
DQ4	OSPIi(4)_D4	IO	FSS0_OSPIi(4) data input/output 4	HiZ
DQ5	OSPIi(4)_D5	IO	FSS0_OSPIi(4) data input/output 5	HiZ
DQ6	OSPIi(4)_D6	IO	FSS0_OSPIi(4) data input/output 6	HiZ
DQ7	OSPIi(4)_D7	IO	FSS0_OSPIi(4) data input/output 7	HiZ
N_SS_OUT0	OSPIi(4)_CSn0	O	FSS0_OSPIi(4) external flash device chip select 0	0x1
N_SS_OUT1	OSPIi(4)_CSn1	O	FSS0_OSPIi(4) external flash device chip select 1	0x1
N_SS_OUT2	OSPIi(4)_CSn2	O	FSS0_OSPIi(4) external flash device chip select 2	0x1
N_SS_OUT3	OSPIi(4)_CSn3	O	FSS0_OSPIi(4) external flash device chip select 3	0x1
OCLK	OSPIi(4)_CLK	O	FSS0_OSPIi(4) clock output for the external flash device	0x0
	OSPI0_LBCLKO	O	FSS0_OSPIi(4) external loopback output	0x0
DQS	OSPIi(4)_DQS	I(3)	FSS0_OSPIi(4) data strobe / external loopback input	Don't care

Table 12-224. OSPI I/O Signals (continued)

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
RESET_OUT0	OSPIi(4)_RESET_OUT0	O	FSS0_OSPIi(4) reset output 0 for the external flash device	0x1
RESET_OUT1	OSPIi(4)_RESET_OUT1	O	FSS0_OSPIi(4) reset output 1 for the external flash device	0x1
ECC_FAIL	OSPIi(4)_ECC_FAIL	I	FSS0_OSPIi(4) ECC status from the external flash device	0x1

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) When used as an external loopback input, the DQS signal can alternatively be referred to as LBCLKI. The LBCLKI clock input signal is a looped back version of the LBCLKO clock output signal and facilitates easier timing closure at higher speeds. The loopback has to be at board level in order to support higher OSPI speeds. The source of the loopback clock is defined by CTRLMMR_MCU_OSPIn_CLKSEL[4] LOOPCLK_SEL bit in *Control Module (CTRL_MMR)*.
(4) i represents an OSPI instance. See the device datasheet for available domains and OSPI instances.

Table 12-225 describes the OSPI I/O connectivity to external SPI devices.

Table 12-225. OSPI I/O Connectivity to External SPI Devices

Module Pin	I/O(1)	Description			
		4-pin(1) SPI - Single Read/Write (SIO) (DATA_XFER_TYPE_EXT_MODE_FLD=0x0)	**4-pin(1) SPI - Dual Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x1)**	**6-pin(1) SPI - Quad Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x2)**	**11-pin(1) SPI - Octal Read/ Write (DATA_XFER_TYPE_EXT_MODE_FLD=0x3)**
DQ0	IO	Used as SPI data output	Used as SPI data input 0 Used as SPI data output 0	Used as SPI data input 0 Used as SPI data output 0	Used as SPI data input 0 Used as SPI data output 0
DQ1	IO	Used as SPI data input	Used as SPI data input 1 Used as SPI data output 1	Used as SPI data input 1 Used as SPI data output 1	Used as SPI data input 1 Used as SPI data output 1
DQ2	IO	Not used	Not used	Used as SPI data input 2 Used as SPI data output 2	Used as SPI data input 2 Used as SPI data output 2
DQ3	IO	Not used	Not used	Used as SPI data input 3 Used as SPI data output 3	Used as SPI data input 3 Used as SPI data output 3
DQ4	IO	Not used	Not used	Not used	Used as SPI data input 4 Used as SPI data output 4
DQ5	IO	Not used	Not used	Not used	Used as SPI data input 5 Used as SPI data output 5
DQ6	IO	Not used	Not used	Not used	Used as SPI data input 6 Used as SPI data output 6
DQ7	IO	Not used	Not used	Not used	Used as SPI data input 7 Used as SPI data output 7
DQS	I(2)	Not used	Not used	Not used	Data strobe or loopback clock input
OCLK	O	Output clock or loopback clock output. For more information, see Table 12-224.			
N_SS_OUT0	O	External SPI device chip-select 0			
N_SS_OUT1	O	External SPI device chip-select 1			
N_SS_OUT2	O	External SPI device chip-select 2			
N_SS_OUT3	O	External SPI device chip-select 3			
RESET_OUT0	O	External SPI device reset 0			
RESET_OUT1	O	External SPI device reset 1			
ECC_FAIL	I	External SPI device ECC failure indication			

(1) This is the pin count at the external SPI flash memory side.
(2) When used as an external loopback input, the DQS signal can alternatively be referred to as LBCLKI. The LBCLKI clock input signal is a looped back version of the LBCLKO clock output signal and facilitates easier timing closure at higher speeds. The loopback has to be at board level in order to support higher OSPI speeds. The source of the loopback clock is defined by CTRLMMR_MCU_OSPIn_CLKSEL[4] LOOPCLK_SEL bit in *Control Module (CTRL_MMR)*.

Note

For OSPI0_CLK, OSPI0_LBCLKO, and OSPI0_DQS signals to work properly, the RXACTIVE bit of the appropriate registers should be set to 0x1 because of retiming purposes.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.4.2.3 OSPI Functional Description

12.4.2.3.1 OSPI Block Diagram

Figure 12-186 shows the OSPI module block diagram.

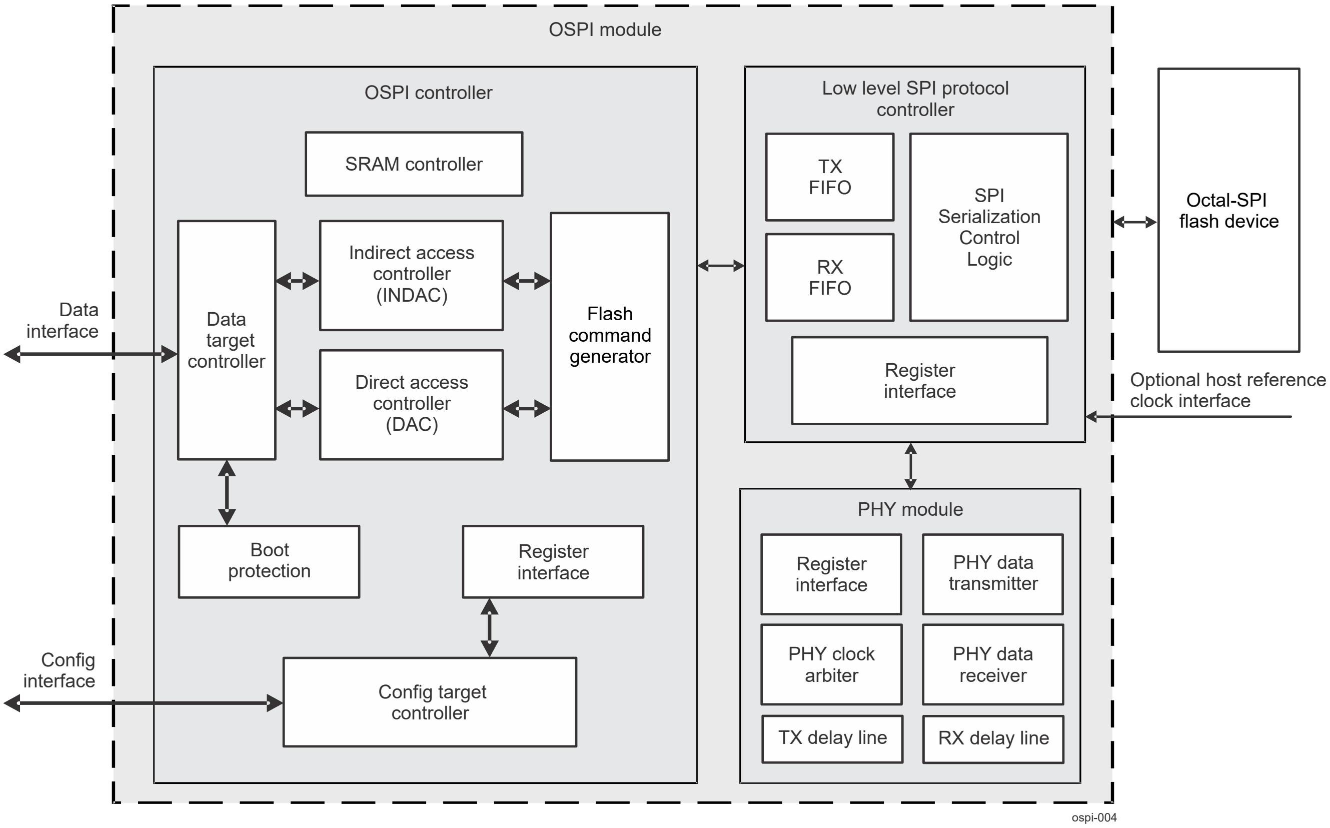


Figure 12-186. OSPI Block Diagram

The OSPI module is composed of three main blocks. The first one is the OSPI controller, the second one is the low level SPI protocol controller, and the third one is the integrated PHY.

The OSPI module has the following two target interfaces:

- Data target interface intended for data transfer.
- Configuration target interface intended for accessing the programmable set of registers.

12.4.2.3.1.1 Data Target Interface

The data interface is used for data transfer to external flash devices in direct and indirect mode of operation. The data target controller validates incoming data accesses, responds to invalid requests, performs any required byte and halfword reordering, blocks writes that violate the programmed write protection rules (only for direct access) and forwards the transfer request to either the direct access controller (DAC) or the indirect access controller (INDAC).

The data interface bus is 32-bits wide. Therefore only byte, halfword and word accesses are permitted. When the controller is configured to work in SPI Octal DDR Mode or Octal DDR Protocol (where 2 bytes are collected within single SPI clock cycle what exceeds the size of 1 byte transfer request), 8 bit transfer size is not allowed.

Note

Cache line wrap accesses over the data target port should be word aligned.

Data target port doesn't support cache line wrap bursts of 128 bytes.

12.4.2.3.1.2 Configuration Target Interface

The configuration interface is used to configure the OSPI module and perform software controlled flash accesses using the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register (for more information refer to Section 12.4.2.3.11, *OSPI Software Triggered Instruction Generator (STIG)*). Depending on the address it routes the incoming interconnect transfer to the Low level SPI protocol controller or to the ECC aggregator. The configuration port is also used to interact with the OSPI configuration and SRAM ECC registers.

Note

The configuration interface supports only 32-bit accesses. For single byte or halfword manipulations software should perform read-modify-write operations.

12.4.2.3.1.3 OSPI Clock Domains

The OSPI module has two main clock sources for the Octal-SPI controller.

- For interface clocks
- For reference clock

The source for the interface clocks corresponds to the configuration and data buses. The data bus clock (OSPI_HCLK) is the main system clock used to transfer data over the data bus between a controller on the system interconnect and the OSPI module. The data bus clock also drives the internal OSPI SRAM. The configuration bus clock (OSPI_PCLK) is used to access the OSPI configuration register and perform basic configuration and for interrupt handling. The OSPI reference clock (OSPI_RCLK) drives the SPI transmit and receive logic in the OSPI module. It is also used to generate the output SPI protocol clock (OSPI_OCLK) and for oversampling of the input data. Using the reference clock (OSPI_RCLK) allows the OSPI module to decouple the frequency of the SPI flash device from the device system clocks, thereby providing more flexible clocking solution.

Note

There is no particular clock ratio requirement between configuration (OSPI_PCLK) and data bus (OSPI_HCLK) clocks.

12.4.2.3.2 OSPI Modes

Note

Some of the OSPI features described in this section may not be supported on this family of devices. For more information, see *OSPI Not Supported Features*.

The OSPI module supports four SPI modes. These modes are defined through the OSPI_FLASH_CFG_CONFIG_REG[1] SEL_CLK_POL_FLD and OSPI_FLASH_CFG_CONFIG_REG[2] SEL_CLK_PHASE_FLD bits. The SEL_CLK_POL_FLD bit defines the clock polarity and the SEL_CLK_PHASE_FLD bit defines the data launch and data capture relation to the OSPI clock edges. Table 12-226 gives a brief description of these modes.

Table 12-226. OSPI Modes

SPI Mode	SEL_CLK_POL_FLD	SEL_CLK_PHASE_FLD	Description
0	0	0	Clock inactive state: low
			Data launch edge: clock falling edge
			Data capture edge: clock rising edge
1	0	1	Clock inactive state: low
			Data launch edge: clock rising edge
			Data capture edge: clock falling edge
2	1	0	Clock inactive state: high
			Data launch edge: clock rising edge
			Data capture edge: clock falling edge

Table 12-226. OSPI Modes (continued)

SPI Mode	SEL_CLK_POL_FLD	SEL_CLK_PHASE_FLD	Description
3	1	1	Clock inactive state: high
			Data launch edge: clock falling edge
			Data capture edge: clock rising edge

Octal flash devices provide DQS signal which allows source synchronous capture, but for Quad flash devices the OSPI module has a loopback mode. In this loopback mode the clock, looped back at board level, is used for registering the input data, and the edge used is same as the launch edge, thus giving a full cycle path (for more information, see Section 12.4.2.3.2.1, *Read Data Capture*).

12.4.2.3.2.1 Read Data Capture

Figure 12-187 shows the Read Data Capture Logic in the OSPI module.

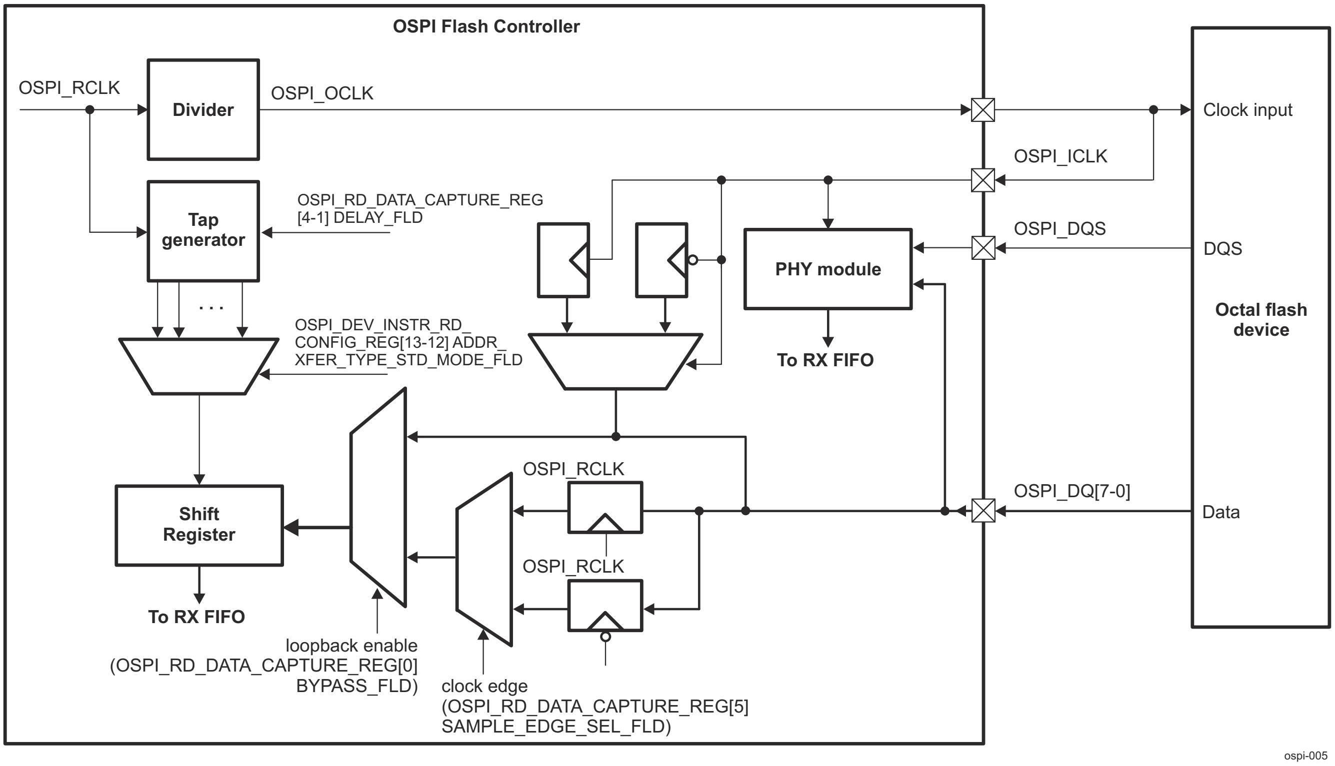


Figure 12-187. Read Data Capture Logic

The PHY module includes a DLL which allows adjustment of the sampling edge with respect to the incoming data to achieve maximum frequency. There are three sources for the sampling signal:

- The reference clock
- Output SPI clock external loopback
- The DQS (only available in Octal Flash devices)

The loopback mode (only for Quad flash devices) can work in two cases. The first one is when OSPI_FLASH_CFG_CONFIG_REG[2] SEL_CLK_PHASE_FLD=0. When SEL_CLK_PHASE_FLD=1 there aren't enough clock falling edges for the register pipeline to catch the last data driven, thus causing a functional failure. Additionally, since the capture edge is falling edge, it gives a full cycle input path only in SPI mode 0, that is when SEL_CLK_POL_FLD=0 and SEL_CLK_PHASE_FLD=0. Thus SPI mode 0 is the first of two modes that support high MHz operation (greater than 50 MHz). The second mode is when SEL_CLK_PHASE_FLD=1 and SEL_CLK_PHASE_FLD=1 (SPI mode 3). In this case the missing clock falling edge is compensated inside the OSPI controller when using the incorporated PHY module by inverting the loopback clock.

The loopback mode is enabled by writing 0x0 to OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[0] BYPASS_FLD. The taps are selected by programming OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[4-1] DELAY_FLD field. The taps delay the read data capturing logic by the programmed number of OSPI_RCLK cycles.

12.4.2.3.2.1.1 Mechanisms of Data Capturing

There are two mechanisms of data capturing in the OSPI module. They can be combined in some parts to ensure reliable sampling solution independent on the system requirements and the controller configuration. The mechanisms are as follows:

- Data capturing mechanism using taps
- Data capturing mechanism using PHY module.

12.4.2.3.2.1.2 Data Capturing Mechanism Using Taps

This section describes the data capturing mechanism where sampling point is adjusted for one of the reference clock edges inside divided OSPI clock.

After POR, the adapted loopback clock circuit and the OSPI_RCLK delay register line both wake in a disabled state. The OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG register provides the control for the mechanism using taps.

OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[5] SAMPLE_EDGE_SEL_FLD bit selects the edge of the reference clock, on which data outputs from flash memory are sampled.

OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[4-1] DELAY_FLD bit field controls the additional number of read data capture cycles (this is the fast reference clock, running at least x4 of the device clock) that should be applied to the internal read data capture circuit. The large clock-to-out delay of the flash memory together with trace delays as well as other device delays may impose a maximum flash clock frequency which is less than the flash memory device itself can operate at. To compensate, software shall set this register to a value that guarantees robust data captures.

12.4.2.3.2.1.3 Data Capturing Mechanism Using PHY Module

PHY module is responsible for data capturing. More detailed description of all internal PHY sampling mechanisms is included in *Read Data Capturing by the PHY Module*.

12.4.2.3.2.1.4 External Pull Down on DQS

Per the OSPI protocol, the FLASH device drives DQS while CS is asserted. When CS is not asserted the FLASH device presents HiZ on DQS. When configured to use DQS, the controller uses the DQS as a clock, which samples the incoming data into a FIFO. Noise on the DQS when it is HiZ can cause spurious false triggering of the FIFO and filling it with invalid data. There is no way to clear this data except to reset the OSPI module.

To avoid this issue, it is recommended to add a pull down on the DQS line.

During device wakeup, before the IO ring is configured properly, the CS to the FLASH device is HiZ. Depending on the actual level of the CS line the FLASH device might drive the DQS High, Low or HiZ. A pull down on DQS forces the DQS input to Low, but the DQS might still be High or in the presence of noise there might be transitions between Low and High. This again can cause the same issue of capturing garbage data in the Controller FIFO.

To avoid this issue it is recommended to release the OSPI from reset only after the IO ring is configured properly.

12.4.2.3.3 OSPI Power Management

Note

> The OSPI module does not provide any hardware signal for busy or idle status. Software need to ensure that the OSPI module is idle before clocks can be shut off by reading the OSPI_FLASH_CFG_CONFIG_REG[31] IDLE_FLD bit.

OSPI_PCLK and OSPI_HCLK share the same clock stop request/acknowledge and clock enable/acknowledge interface.

12.4.2.3.4 Auto HW Polling

The OSPI controller is capable of automatically testing the Flash device busy bit to guarantee no reads or writes are ignored by the flash when it is busy burning in programmed data.

At the end of a programming transaction, the Flash device goes into a burn-in state and becomes busy.

When Auto HW Polling is enabled, the OSPI controller keeps track of programming transactions and will initiate a Flash status read polling transactions automatically, until Flash indicates it is not busy, before any additional data read or programming operations are sent to the flash device. See OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG register and the associated registers.

The OSPI controller requires that the OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG[23-16] POLL_COUNT_FLD field should always be set with values greater or equal to 3 (>=3).

12.4.2.3.5 Flash Reset

OSPI provides Flash reset out ports. These ports are active low and controlled thru OSPI_FLASH_CFG_CONFIG_REG register.

12.4.2.3.6 OSPI Memory Regions

Note

For more information about the memory space, see *FSS Memory Regions*.

12.4.2.3.7 OSPI Interrupt Requests

The OSPI module generates three interrupts. The ECC interrupts (FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_0 and FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_0) are generated by the OSPI ECC aggregator.

The other interrupt (FSS0_OSPI_0_OSPI_LVL_INTR_0) is generated by the OSPI module.

Table 12-227 lists the event flags and the corresponding mask bits of the sources which can cause interrupts.

Table 12-227. OSPI Events

Event Flag	Event Mask	Description
OSPI_FLASH_CFG_IRQ_STATUS_REG[0] MODE_M_FAIL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[0] MODE_M_FAIL_MASK_FLD	Event Flag and Event Mask for the OSPI Interrupts.
OSPI_FLASH_CFG_IRQ_STATUS_REG[1] UNDERFLOW_DET_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[1] UNDERFLOW_DET_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[2] INDIRECT_OP_DONE_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[2] INDIRECT_OP_DONE_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[3] INDIRECT_READ_REJECT_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[3] INDIRECT_READ_REJECT_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[4] PROT_WR_ATTEMPT_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[4] PROT_WR_ATTEMPT_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[5] ILLEGAL_ACCESS_DET_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[5] ILLEGAL_ACCESS_DET_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[6] INDIRECT_XFER_LEVEL_BREACH_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[6] INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[7] RECV_OVERFLOW_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[7] RECV_OVERFLOW_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[8] TX_FIFO_NOT_FULL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[8] TX_FIFO_NOT_FULL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[9] TX_FIFO_FULL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[9] TX_FIFO_FULL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[10] RX_FIFO_NOT_EMPTY_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[10] RX_FIFO_NOT_EMPTY_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[11] RX_FIFO_FULL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[11] RX_FIFO_FULL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[12] INDRD_SRAM_FULL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[12] INDRD_SRAM_FULL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[13] POLL_EXP_INT_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[13] POLL_EXP_INT_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[14] STIG_REQ_INT_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[14] STIG_REQ_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[16] RX_CRC_DATA_ERR_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[16] RX_CRC_DATA_ERR_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[17] RX_CRC_DATA_VAL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[17] RX_CRC_DATA_VAL_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[18] TX_CRC_CHUNK_BRK_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[18] TX_CRC_CHUNK_BRK_MASK_FLD	
OSPI_FLASH_CFG_IRQ_STATUS_REG[19] ECC_FAIL_FLD	OSPI_FLASH_CFG_IRQ_MASK_REG[19] ECC_FAIL_MASK_FLD	

Table 12-227. OSPI Events (continued)

Event Flag	Event Mask	Description
OSPI_ECC_SEC_STATUS_REG0[0] SRAM_PEND	OSPI_ECC_SEC_ENABLE_SET_REG0[0] SRAM_ENABLE_SET OSPI_ECC_SEC_ENABLE_CLR_REG0[0] SRAM_ENABLE_CLR	Event Flag and Event Mask for the ECC Interrupts.
OSPI_ECC_DED_STATUS_REG0[0] SRAM_PEND	OSPI_ECC_DED_ENABLE_SET_REG0[0] SRAM_ENABLE_SET OSPI_ECC_DED_ENABLE_CLR_REG0[0] SRAM_ENABLE_CLR	
OSPI_ECC_AGGR_STATUS_SET[1-0] PARITY	OSPI_ECC_AGGR_ENABLE_SET[0] PARITY	
OSPI_ECC_AGGR_STATUS_SET[3-2] TIMEOUT	OSPI_ECC_AGGR_ENABLE_SET[1] TIMEOUT	
OSPI_ECC_AGGR_STATUS_CLR[1-0] PARITY	OSPI_ECC_AGGR_ENABLE_CLR[0] PARITY	
OSPI_ECC_AGGR_STATUS_CLR[3-2] TIMEOUT	OSPI_ECC_AGGR_ENABLE_CLR[1] TIMEOUT	

12.4.2.3.8 OSPI Data Interface

12.4.2.3.8.1 Data Interface Address Remapping

The incoming data interface address, by default, maps directly to the address sent serially to the FLASH device. If the FLASH device has a 24-bit address, then the 24 LSB's of the data address is forwarded. A remap feature is available to remap all incoming data addresses to ADDRESS + N, where N is the value stored in the OSPI_FLASH_CFG_REMAP_ADDR_REG[31-0] VALUE_FLD bit field. It is enabled via the OSPI_FLASH_CFG_CONFIG_REG[16] ENB_AHB_ADDR_REMAP_FLD bit. This feature could be used when software needs to move boot code to another FLASH region.

12.4.2.3.8.2 Write Protection

In order to protect the FLASH device, a software controlled write protection feature is supported. Any data write detected (by using DAC), pointing to an area of the FLASH that is protected, is not permitted.

A programmable region of the FLASH device, defined as a number of FLASH 'blocks' starting from a particular block number can be protected. Three programmable registers are provided. The first OSPI_FLASH_CFG_LOWER_WR_PROT_REG register defines the FLASH block that is located at the bottom of the region to be protected. The second OSPI_FLASH_CFG_UPPER_WR_PROT_REG register defines the FLASH block that is located at the top of the region to be protected. The third OSPI_FLASH_CFG_WR_PROT_CTRL_REG register is a control register consisting of 2 bits. The OSPI_FLASH_CFG_WR_PROT_CTRL_REG[0] INV_FLD bit allows software to invert the region that is being protected, causing the programmed region to become the only areas of FLASH memory that is not protected from writes. The OSPI_FLASH_CFG_WR_PROT_CTRL_REG[1] ENB_FLD bit is the write protection enable bit. When this bit is set to 0, the FLASH device is unprotected.

For implementation, the data interface must map the incoming address into its associated FLASH block. A block can be between 1 and 65 KB, programmed via the OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG register.

12.4.2.3.8.3 Access Forwarding

For legal accesses, the data interface will forward all accesses to one of two access controllers - the direct access and the indirect access controllers. Assuming DAC has been enabled via the OSPI_FLASH_CFG_CONFIG_REG[7] ENB_DIR_ACC_CTRL_FLD bit, then by default all accesses will be forwarded to this controller. Before any accesses can be forwarded to INDAC, it must first be configured by software. This process is fully explained in Section 12.4.2.3.10, *OSPI Indirect Controller (INDAC)*. If DAC is disabled, any incoming access that cannot be forwarded to INDAC will be completed immediately with an error. If DAC is enabled, the same access will be forwarded and serviced by DAC.

12.4.2.3.9 OSPI Direct Access Controller (DAC)

Direct access refers to the operation where data interface accesses directly trigger a read or write to FLASH memory. It is memory mapped and can be used to both access and directly execute code from external FLASH memory. Any incoming access that is not recognized as being within the programmable indirect trigger region is assumed to be a direct access and will be serviced by the DAC. Note that accesses that use DAC do not use the embedded SRAM. The data transfer stops when read or write burst is carried out. The amount of wait states applied will be dependent on the latency through the controller. Latency is kept to a minimum when the use of XIP read instructions are enabled (see OSPI_FLASH_CFG_CONFIG_REG[18] ENTER_XIP_MODE_IMM_FLD and OSPI_FLASH_CFG_CONFIG_REG[17] ENTER_XIP_MODE_FLD bits).

12.4.2.3.10 OSPI Indirect Access Controller (INDAC)

12.4.2.3.10.1 Indirect Read Controller

The aim of the indirect mode of operation is to read significant numbers of bytes from FLASH memory without requiring a data interface access to trigger it. Instead indirect operations are controlled and triggered by software via specific control/ configuration Indirect Read Transfer registers (OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG, OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG, OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG, and OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG). This block will communicate with an embedded low level SPI protocol state machine module to perform an efficient and optimized FLASH read burst, placing the read data into the local SRAM module ready for fast and low latency delivery to any external controller.

By default, the Indirect Read controller is disabled. Before enabling it, software must configure how much data is required and the start address. The start address and total number of bytes to be fetched is defined in OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG and OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG registers, respectively. Up to two indirect operations can be programmed at any one time. The second operation can be triggered while the first is in progress. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. For more information refer to Section 12.4.2.3.10.3, *Indirect Access Queuing*.

The total number of bytes to read in an indirect operation is not limited by the size of the SRAM. The size of SRAM will only limit the size of requests. In the case of SRAM overrun, the controller will back pressure FLASH reads until space becomes available in the SRAM. Back pressuring the reads on the SPI interface is handled by completing any current read burst, waiting until space in the SRAM becomes available and then issuing a new read burst at the address where the previous terminated burst ended.

An external controller will be able to fetch the data that the controller has read from external FLASH memory by issuing data interface reads to the OSPI module. The address of the incoming read access must be in the range of indirect trigger address programmed via the OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG register to indirect trigger address + 2**(indirect trigger address range) - 1. Default value of the range is equal to 16 locations. This allows a 16-beat burst to be applied starting from the indirect trigger address. The smaller bursts are possible to handle effectively as well with this approach. Furthermore it is not strict requirement to push consecutive address sequence. Actual address just has to be in the indirect range to grant SRAM as source. Each valid Indirect Read will cause the internal SRAM to be popped, thereby decoupling the incoming read access address from the FLASH address – that is not direct mapped. Therefore the indirect trigger address does not have any relationship with the FLASH address. It is just to indicate that data should take the SRAM as source instead of the FLASH memory array after triggering of any valid Indirect Read. The FLASH address for Indirect Read is taken from the OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG register. Assuming the requested data is present in the SRAM at the point the data interface access is received by the OSPI module, then the data will be fetched from the SRAM and the response to the read burst will be achieved with minimum latency. Once the data has been read from the SRAM, the OSPI module will free up the associated resource in the SRAM.

If a read access is received whose address is not within the range described above then that access will not be completed using the indirect controller. It will instead be serviced by the direct access controller.

If a read access is received whose address is within the range described above but the requested data is not immediately present in the SRAM then wait states will be applied until the data has been read from FLASH and pushed to the SRAM.

If a read burst is received whose access elements traverse the Indirect trigger range, then the accesses within the Indirect trigger range will be processed by the indirect controller and the rest will be taken by the direct access controller. This is likely to be a software configuration error.

The external controller is only permitted to issue 32-bit data interface reads until the last word of an indirect transfer. This helps keep the SRAM control logic less complex. On the final read, the external controller may issue a 16-bit (Halfword) or byte access to complete the transfer. It is also permitted for the external controller to always issue a 32-bit Word read on the last indirect access. The controller will pad the upper bits of the response with zero. The current expectation is that the SRAM will be kept fairly full while the read operation is carried out. The fill level of the SRAM is directly readable by software reading the OSPI_FLASH_CFG_SRAM_FILL_REG register.

An indirect operation may be cancelled at any time by setting 1 to OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[1] CANCEL_FLD bit.

Any bus controller should be allowed to initiate an indirect access. The OSPI module provide software access mechanism to the SRAM fill-level directly via configuration registers and then decide for itself when the data should be fetched from the local SRAM. The fill level watermark register (see OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG register) is provided. When the SRAM fill level passes this watermark, an interrupt is generated. If the watermark value is > 0, the watermark interrupt is also generated when the final byte of data has been read by the OSPI module and placed in the SRAM, even if the actual SRAM fill level has not risen above the watermark. This last feature is useful to avoid software tracking how much data has been read and resetting the watermark value for the last few bytes of an indirect read transfer.

Two further interrupt sources are provided to help understand the status of an indirect operation. Firstly, an interrupt is generated when an indirect operation has completed. Secondly, an interrupt is generated if an Indirect Read operation was requested but could not be accepted due to the fact 2 indirect operations have already been buffered by the OSPI module.

Setting the OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit starts an indirect read operation. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[2] RD_STATUS_FLD bit is available to check the status.

12.4.2.3.10.1.1 Indirect Read Transfer Process

The following sequence can be followed:

1. Setup OSPI_FLASH_CFG_CONFIG_REG register.
2. Setup the indirect transfer's FLASH start address in the OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG register.
3. Setup the number of bytes to be transferred in the OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG register.
4. Setup the indirect transfer's trigger address in the OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG register.
5. Setup the indirect transfer's trigger address range in the OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG register.
6. If the watermark interrupt feature is to be used, set the OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG register which will cause an interrupt to be generated when the fill level increases beyond the watermark level. Setting the watermark can be useful indication to software when to read the next part of the indirect read transfer. Note that if the watermark is set to a value other than zero, the watermark interrupt will always trigger once the final byte of indirect transfer has been fetched and placed in the embedded SRAM, even if the watermark value is higher than the actual completed fill level.
7. Trigger Indirect Read access by setting the OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit to 1.

8. If the watermark interrupt feature is to be used, wait for watermark interrupt. Else poll the SRAM fill level via the OSPI_FLASH_CFG_SRAM_FILL_REG register to decide when sufficient data is in the SRAM to trigger data fetches.
9. Read the expected amount of data from SRAM. If there is still more data to fetch in order to complete the indirect read transfer, then loop back to step 8. Otherwise continue to step 10.
10. The completion status of the Indirect Read operation can be polled via the OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD bit.
11. An Indirect Complete interrupt will be generated when the Indirect read operation has completed.

12.4.2.3.10.2 Indirect Write Controller

The aim of the indirect mode of operation is to perform bulk transfer of data from the processor into a FLASH memory in the most efficient manner. The fewest possible write cycles inside the FLASH device will be carried out for the indirect transfer, thus maximizing the life of the device. Indirect write operation can be thought of from a software perspective as the inverse of the indirect read. It is controlled and triggered by software via specific control/configuration Indirect Write Transfer registers (for more information see the following registers: OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG, OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG, OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG, and OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG). This block will await delivery of the write data via the external data interface controller, placing it in the local SRAM before communicating with the existing legacy SPI core to perform an efficient and optimized FLASH write burst.

By default, the indirect write controller is disabled. Before enabling it, the software must configure how much data is required and the start address. The start address and total number of bytes to be written is defined in OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG and OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG registers, respectively. Up to two indirect operations can be programmed at any one time. The second operation can be triggered while the first is in progress. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. The Indirect write queuing is very similar to indirect read queuing. For more information refer to Section 12.4.2.3.10.3, *Indirect Access Queuing*.

The total number of bytes to write in an indirect operation is not limited by the size of the SRAM. The size of SRAM will only limit the amount of data that can be accepted from the external controller. In the case of an SRAM overrun, the controller will back pressure the data interface with wait states. Note the fill level of the SRAM is readable via programmable OSPI_FLASH_CFG_SRAM_FILL_REG register and this can be used to avoid this situation.

An external controller will provide the write data and will transfer this to the OSPI module by issuing data interface writes. The address of the incoming write access must be in the range of Indirect trigger address programmed via the OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG register to Indirect trigger address + 2**(Indirect trigger address range) - 1. Default value of the range is equal to 16 locations. This allows a 16-beat burst to be applied starting from the Indirect trigger address. The smaller bursts are possible to handle effectively as well with this approach. Furthermore it is not strict requirement to push consecutive address sequence. Actual address just has to be in the Indirect Range to grant SRAM as source. Each write will cause the internal SRAM to be pushed, thereby decoupling the incoming write access address from the FLASH address – that is not direct mapped. Therefore Indirect trigger address does not have any relationship with FLASH address. It is just to indicate that data should take SRAM as source instead of FLASH Memory array after triggering of any valid Indirect Write. The FLASH address for Indirect Write is taken from the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG register. Assuming the SRAM is not full at the point the data interface access is received by the OSPI module, then the data will be pushed to the SRAM with minimum latency.

If a write access is received whose address is not within the range described above then that access will not be completed using the indirect controller. It will instead be serviced by the direct access controller.

If a write access is received whose address is within the range described above but the SRAM is full then wait states will be applied until some or all of the data has been pushed from the SRAM to the FLASH.

If a write burst is received whose access elements traverse the Indirect trigger range, then the accesses within the Indirect trigger range will be processed by the indirect controller, and the rest will be taken by the direct access controller. This is likely to be a software configuration error.

The external controller is only permitted to issue 32-bit data interface writes until the last word of an indirect transfer. This helps keep the SRAM control logic less complex. On the final write, the external controller may issue a 32-bit word, 16-bit (halfword) or a byte access to complete the transfer. If the number of bytes to write is less than 4 on the last transfer, the controller is still permitted to issue a 32-bit transfer. In these cases, the extra bytes are discarded by the controller.

When the SRAM holds a number of bytes equal to or greater than the size of a FLASH page (which itself is programmed into the OSPI module, with a default of 256 bytes) or when the SRAM holds all remaining bytes of the currently executing indirect transfer, the OSPI module will initiate a write burst to the flash command generator.

An indirect operation may be cancelled at any time by setting 1 to the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[1] CANCEL_FLD bit.

Any bus controller should be allowed to initiate an indirect access. The OSPI module provide software access mechanism to the SRAM fill-level directly via the configuration registers and then decide for itself when the data should be written to the local SRAM. The fill level watermark register (see OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG register) is provided. When the SRAM fill level falls below this watermark, an interrupt is generated.

Two further interrupt sources are provided to help understand the status of an indirect operation. Firstly, an interrupt is generated when an indirect operation has completed. Secondly, an interrupt is generated if an indirect write operation was requested but could not be accepted due to the fact 2 indirect operations have already been buffered by the OSPI module.

Setting the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit starts an indirect write operation. The OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[2] WR_STATUS_FLD bit is available to check the status.

12.4.2.3.10.2.1 Indirect Write Transfer Process

The following sequence can be followed:

1. Setup OSPI_FLASH_CFG_CONFIG_REG register.
2. Setup the indirect transfer’s FLASH start address in the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG register.
3. Setup the number of bytes to be transferred in the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG register.
4. Setup the indirect transfer’s trigger address in the OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG register.
5. Setup the indirect transfer's trigger address range in the OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG register.
6. It is functionally valid for software to simply write all the data to the SRAM in one block transfer. However, if the total number of bytes to write is greater than the size of the partitioned SRAM, then it is quite likely the SRAM will become full causing the OSPI to back-pressure the system data bus for a considerable time. This time is based on the FLASH data-rate and the page-write time of the device. To avoid sending all the write data in one block transfer, software can make use of the watermark interrupt to identify a convenient time to send data a page at a time to the SRAM module. Alternatively, software can poll the SRAM fill level register directly to identify how empty the SRAM is at any one time in order to make a judgment as to when the most practical time to send the next part of the transfer.
7. If the watermark interrupt feature is to be used, set the OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG register which will cause an interrupt to be generated when the fill level falls below the watermark. The watermark should be set to a number between zero and a page size. That is if the page size is 256 bytes, then setting the watermark to a value between 10 and 250 is reasonable and will cause the interrupt to trigger when the fill level drops below the

programmed number. Setting the watermark can be useful to provide an indication to software when to write the next page of data to the SRAM.

8. Trigger Indirect Write access by setting OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit.
9. If the remaining number of bytes still to be transferred into the SRAM for the current indirect transfer is greater than a FLASH page, then write 1 FLASH page worth of data to the SRAM. Otherwise send the remaining data from the indirect transfer to SRAM.
10. If all the data in the indirect transfer has now been sent to the SRAM, then go to 12 and await indirect complete status. Otherwise if there is more data still to be transferred then either:
    - If the watermark interrupt feature is being used, then wait for watermark interrupt.
    - Alternatively the SRAM fill level can be interrogated to identify a convenient time to send more data.
11. Loop back to 9.
12. Optional: The completion status of the Indirect write operation can be polled via OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD.
13. An Indirect Complete interrupt will be generated when the Indirect write operation has completed.

12.4.2.3.10.3 Indirect Access Queuing

Software is permitted to queue up to two indirect transfers for both the indirect write controller and the indirect read controller. Supporting two indirect operations allows a short turnaround time between the completion of one indirect operation and the start of the second. Any attempt to queue more than two operations will cause an interrupt to be generated. To take advantage of this feature, software should attempt to keep both indirect programming slots full at all times.

From the software perspective, indirect access queuing is achieved by triggering bit 0 of the indirect transfer control register (OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG[0] START_FLD bit or OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG[0] START_FLD bit) twice in short succession. The indirect number of bytes register (OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG or OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG register) and the indirect FLASH start address register (OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG or OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG register) must be setup with the relevant transfer data before START_FLD bit can be triggered for each transfer. Since these registers will change regularly, the hardware must keep sampled versions of these registers for the duration of the indirect transfer.

The internal register block will only issue an indirect start trigger to the key underlying datapath blocks one at a time. There are 2 independent datapath blocks in the indirect access controller that will receive and independently sample this information. The first is the datapath block on the data bus side of the SRAM. For indirect reads, this is a read interface, for indirect writes, it is a write interface. The second is the datapath block on the FLASH side of the SRAM. For indirect reads, this is a write interface, for indirect writes, it is a read interface. Both blocks will process the indirect transfers at different times. For example, for an indirect read operation, the datapath block on the FLASH side of the SRAM will be able to start processing the second queued transfer as soon as the last byte of the first transfer has been written to the SRAM. Before commencing the second transfer, this block must resample the OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG and OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG registers. Similarly, the datapath block on the bus side will resample the same registers locally when it has forwarded all the FLASH data associated with the first indirect transfer from the SRAM onto the data bus.

12.4.2.3.10.4 Consecutive Writes and Reads Using Indirect Transfers

It is permitted for software to trigger an indirect read operation while an indirect write operation is in progress. Similarly it is permitted to trigger an indirect write while an indirect read operation is in progress. Indirect write operations will take overall precedence.

12.4.2.3.10.5 Accessing the SRAM

The SRAM depth is separated in two segmets. The lower segment is reserved for indirect read use. The upper segment is for indirect write use only. The size of each segment is programmable via the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG register. This feature allows to allocate how many bits of the SRAM address bus are allocated to indirect read. By default, this is set so that exactly half of the SRAM is portioned for use by the indirect read controller. To ensure the read data bus is not directly fed by the SRAM read data through combinatorial logic, an extra bank of holding registers is included in the indirect read data path. These registers act as an extra location to be added to the allocated number of SRAM locations for indirect read.

To illustrate how the SRAM (and the extra bank of holding registers) can be allocated between indirect read and write, the following example is provided. The depth of the SRAM in this example is configured to be 8 bits. This is equal to 256 locations.

- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x00, then 256 locations are allocated to indirect writes and 1 location to indirect reads.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x01, then 255 locations are allocated to indirect writes and 2 locations to indirect reads.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0x02, then 254 locations are allocated to indirect writes and 3 locations to indirect reads.
- And so on until.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFD, then 3 locations are allocated to indirect writes and 254 locations to indirect reads.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFE, then 2 locations are allocated to indirect writes and 255 locations to indirect reads.
- If the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG[7-0] ADDR_FLD field is set to 0xFF, then 1 location is allocated to indirect writes and 256 locations to indirect reads.

Note

A value of 0xFF or 0x00 in the OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG register should be avoided by software, as only the bottom 8 bits of the SRAM fill level are accessible through software (up to 255 limit) via the OSPI_FLASH_CFG_SRAM_FILL_REG register. If the fill level reaches 256 on either the indirect read or write side, it will appear when reading the Fill Level to be 0.

There are four SRAM sources that are arbitrated and muxed onto the single SRAM port. Up to three sources can access this port at any one time. The sources are described as follows:

- Indirect Write, Write source. This is located on the data bus side of the SRAM.
- Indirect Write, Read source. This is located on the FLASH side of the SRAM.
- Indirect Read, Write source. This is located on the FLASH side of the SRAM.
- Indirect Read, Read source. This is located on the data bus side of the SRAM.

A fixed priority arbitration scheme is implemented. Table 12-228 shows priority allocated to these sources.

Table 12-228. SRAM Access Priority

SRAM Access Priority		
Indirect Write	Write to SRAM (from System Data Bus)	3rd (exclusive with Data Bus Read Request)
	Read from SRAM (from OSPI Module)	2nd
Indirect Read	Write to SRAM (from OSPI Module)	1st
	Read from SRAM (from System Data Bus)	3rd (exclusive with Data Bus Write Request)

Note

With the exception of the write port during an Indirect Read operation (on the FLASH side of the SRAM), the logic driving all four sources must not assume single cycle completion. Writes to the SRAM during an indirect read must be allowed to complete immediately to avoid data loss. Therefore this port is given maximum priority.

12.4.2.3.11 OSPI Software-Triggered Instruction Generator (STIG)

The DAC and INDAC are used to transfer data. In order to access the volatile and non-volatile configuration registers, the legacy SPI Status register, other status/protection registers as well as to perform ERASE functions, a separate software controller is required. The software triggered instruction generator (STIG) is controlled using the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register by setting up the command to issue to the FLASH device. This is a generic controller and can be used to perform any instruction that the FLASH device supports from the extended SPI protocol. Configuring of instructions which are not compliant with the specification of the FLASH devices could cause unpredicted behavior of the controller. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD bits should be set different than OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[7-0] RD_OPCODE_NON_XIP_FLD and OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[7-0] WR_OPCODE_FLD. The OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD bit is used to trigger the command. The OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit is used by software to poll the status of the command execution. For reads, when the command has been serviced (OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit toggles from '1' to '0'), up to 8 bytes of read data will be placed in the OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG registers. For writes, the write data should be placed in the OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG registers.

The completion of the STIG request could be also checked by the corresponding interrupt. The occurrence of the interrupt indicates that the controller is ready for accepting a new STIG request. It is important to notice that completion of the STIG request is not equivalent to completion it on SPI side. For example, if STIG is configured to the command composed of data to transmit only, the data is taken from the corresponding STIG register fields and put into TX FIFO. Since all bytes to write are known, another STIG can be queued before serialization of the current one is completed.

There are some commands which require more data to read than 8 bytes (for example READ ID command). The additional STIG Memory Bank is implemented in order to accommodate these data if needed. The STIG Memory Bank (internal component of the controller) is controlled by the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD bit. If enabled, the number of bytes to read in the STIG is extended to 16 as defined in OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[18-16] NB_OF_STIG_READ_BYTES_FLD bit field. It should be noticed that there are very few commands (excluding Read Array ones which are not intended to handle effectively in STIG Mode but in Direct/Indirect Modes) which return more than 8 bytes to the controller. If the maximum number of bytes to Read using STIG in target application is less than 16, the depth of the STIG Memory Bank can be set smaller what will result in saving noticeable part of the area.

If number of bytes to Read in the STIG as defined in OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[18-16] NB_OF_STIG_READ_BYTES_FLD bit field exceeds the Memory Bank Depth, remaining data will overwrite the STIG Memory Bank locations starting from its first address. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG keep the last 8 bytes read from the Flash Device by STIG when Memory Bank is enabled. Therefore, for example if the user wants to get just a single byte from the last eight bytes from long continuous read SPI data chain, there is no need to access the STIG Memory Bank since data can be taken from suitable Flash Command Read Data register. In order to access more data, STIG Memory Bank data request should be triggered. It is controlled by the OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG and works analogously for triggering STIG from the functional standpoint.

OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[0] TRIGGER_MEM_BANK_REQ_FLD bit is used to trigger the command, bit OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[1] MEM_BANK_REQ_IN_PROGRESS_FLD is used by software to poll the status of the command execution. When MEM_BANK_REQ_IN_PROGRESS_FLD bit toggles from "1" to "0", the byte of data (OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[15-8] MEM_BANK_READ_DATA_FLD) from corresponding address (OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG[28-20] MEM_BANK_ADDR_FLD bit field) is valid. The address should be set before triggering the STIG Memory Bank access. Each consecutive STIG access overwrites the previous one so that the data in the Bank always fit into byte index fetched by the last STIG access configured to use the Memory Bank (first incoming byte equals first address of the Memory Bank, second one equals the second address and so on).

12.4.2.3.11.1 Servicing a STIG Request

A STIG request will cause the OSPI Flash controller to interrogate the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register to determine what and how many bytes it should send to the FLASH device. The OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD field of this register indicate the instruction to be sent and is always pushed first. If there is an address to send, then the address (the size of which is also programmed in the same register) is sent next. The address itself is stored in the OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG register. If Mode bits are enabled by OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[18] ENB_MODE_BIT_FLD bit. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field are being sent right after address. If OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[18] ENB_MODE_BIT_FLD and OSPI_FLASH_CFG_CONFIG_REG[29] CRC_ENABLE_FLD are both enabled, STIG will replace XIP Mode bits (not applicable for CRC aware SPI interface) for automatically calculated address CRC byte. Therefore, to execute CRC aware STIGs (meaning the commands requiring sending address CRC byte), ENB_MODE_BIT_FLD bit should always be set. If there are any dummy cycles to send (the size of which is also programmed in OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register) then those are sent next. If there is data to write or read (the size of which is also programmed in OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register) then for the case of writes, up to 8 bytes can be sent (as stored in the Flash Command Write Data registers, OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG registers) next. In the read case, when the read data has been collected from the FLASH device, the OSPI Flash Controller stores that in the Flash Command Read Data Registers (OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG registers). Up to 8 bytes can be get if OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD bit is disabled or up to 512 when enabled. When the OSPI Flash controller starts to service a STIG request, it sets the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit to indicate a command execution is in progress. When the OSPI Flash controller is in the auto-polling state, servicing a STIG request is slightly different. Most of devices are largely inaccessible after a program operation until the device has completed that write. Some group of them has a possibility to suspend programming page. It can be controlled by the OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG[8] DEVICE_STATUS_VALID_FLD bit, which indicate active auto-polling phase. After requesting a STIG, the OSPI Flash Controller immediately issues appropriate OPCODE to Memory. During servicing a STIG (in auto-polling phase) the status bit of command execution remains steady and other parts of transfer such as ADDRESS or DUMMY BITS, and so forth, are disabled (to issued Program Suspend Command is needed OPCODE only). There is a programmable option to add delay between every repetitive poll operation (delay is defined by OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG[31-24] POLL_REP_DELAY_FLD bit field). This feature is implemented to free up SPI bandwidth if needed.

12.4.2.3.12 OSPI Arbitration Between Direct / Indirect Access Controller and STIG

When multiple controllers are active simultaneously, a simple fixed-priority arbitration scheme is used to arbitrate between each interface and access the external FLASH. The fixed priority is defined as follows, highest priority first.

- The Indirect Access Write
- The Direct Access Write
- The STIG
- The Direct Access Read
- The Indirect Access Read

12.4.2.3.13 OSPI Command Translation

Requests issued by the direct access controller, the indirect access controller or the STIG will be translated into a sequence of byte transfers to send downstream (before serialization to the FLASH device). These sequences depend on the requested transfer but an example of a typical 1-byte non sequential READ is shown below:

INSTRUCTION OPCODE -> ADDRESS -> Mode Byte -> Dummy Bytes -> 1 byte of don't care

For sequential accesses, an extra byte of data per read is pushed to the FLASH device on the back of the above sequence assuming it can be done so with no gap between each transferred byte.

When PHY mode is enabled and consequently no clock divider is configured, latency caused by multi domain synchronization may make an extra byte insufficient to avoid the transfer gap. To ensure the sequential access non-interrupted and keep the maximum performance of the controller, PHY Pipeline Mode is implemented. When enabled, number of don't care bytes is calculated based on the configuration.

The actual sequence sent to the FLASH device depends on the requested transfers, whether the transfer is non-sequential or sequential, whether the device has been configured in XIP mode and the state of the main Device Instruction Type programmable registers (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG and OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG).

For writes, the write enable latch (or WEL) within the FLASH device itself must be high before a write sequence can be issued. The OSPI Flash Controller will automatically issue the write enable latch command before triggering a write command via the direct or indirect access controllers (DAC/INDAC) – that is the user does not need to perform this operation. For increasing flexibility and performance user can turn off this feature by setting the OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[8] WEL_DIS_FLD bit. The opcode for WREN is typically 0x06 and is common between devices.

When write requests from the direct or indirect access controllers are no longer being received and all outstanding requests have been sent, the FLASH device will automatically start the page program write cycle. Any incoming request at this time will be held in wait states until the cycle has completed. The OSPI Flash Controller will automatically poll the FLASH device legacy SPI status register to identify when the write cycle has completed. This is achieved by sending the RDSR opcode to the FLASH device and waiting until the device itself has indicated the write cycle has completed (until the Write in Progress bit has cleared to zero and the write enable latch bit has also cleared to zero or device is ready bit has set to one). The WREN and the RDSR device instructions are the only ones that are sent by the controller under the hood. For any other specific instruction that the user determines should be sent to the device (for example if the device needs to be unprotected before a write command is issued), these should be handled separately by issuing FLASH commands via the STIG.

There is an option to trigger HOLD or RESET feature on I/Os of the Flash Device. The HOLD one is generally common across the devices and takes an alternative function of DQ3 pin (applicable when device operates neither in Quad SPI mode nor DDR). The transfer can be hold and then resumed by dedicated software trigger field (OSPI_FLASH_CFG_CONFIG_REG[4] HOLD_PIN_FLD). The devices which have the HOLD feature on DQ3 usually need another dedicated pin for hardware reset and ones without HOLD feature usually have alternative reset on DQ3 what makes the additional reset pin being redundant. The controller supports both variants and reset selection register field (OSPI_FLASH_CFG_CONFIG_REG[6] RESET_CFG_FLD) allows the user to configure which hardware reset solution is implemented in the device under usage.

After configuration is done, it is possible to trigger HOLD or RESET features using I/Os (OSPI_FLASH_CFG_CONFIG_REG[4] HOLD_PIN_FLD or OSPI_FLASH_CFG_CONFIG_REG[5] RESET_PIN_FLD bits). After HOLD activation the controller is introduced into waiting state and any other operations should not be requested before de-asserting of HOLD configuration bit. The HOLD feature is useful when any SPI transaction needs to be prolonged in order to adjust it into specific point in time. Note that any HOLD trigger issued during active SPI transaction may be synchronized into reference clock domain at the time the SPI transfer turns to be finished. In this case, there is nothing to hold so the low level SPI logic will not activate HOLD on DQ3. To check if HOLD request suspended the transfer OSPI_FLASH_CFG_CONFIG_REG[31] IDLE_FLD bit can be polled for. If SPI is not in the IDLE state, the transfer was successfully suspended. It is important for the software to take care of resetting OSPI_FLASH_CFG_CONFIG_REG[4] HOLD_PIN_FLD bit before newly triggered SPI transaction. In case HOLD request is set before the beginning of the transfer it will be HOLD right after it starts what may not always be a goal. The hardware RESET needs to be activated when CS is high (no valid transaction is present on SPI bus). It can be checked by polling of OSPI_FLASH_CFG_CONFIG_REG[31]. If the controller is in the IDLE state and no other transfer requests are queued to perform, the hardware RESET can be triggered. The RESET feature is useful when any write, program or erase operation needs to be cancelled. No transfer request is permitted before driving the reset back to being inactive. Triggering HOLD or RESET on DQ3 at the time the device is configured to work in Quad SPI mode or DDR will overwrite transfer data on DQ3 with '0'. This behavior is considered as a software error so it is advisable for the system to make sure that the flash device was introduced to suitable SPI mode (that is by polling its configuration register) before triggering alternative DQ3 function. There are four independent reset outputs implemented to separate between multiple devices connected to the controller (up to 4 are supported). The decision which reset output is to be activated after triggering OSPI_FLASH_CFG_CONFIG_REG[5] RESET_PIN_FLD bit is made based on OSPI_FLASH_CFG_CONFIG_REG[9] PERIPH_SEL_DEC_FLD and OSPI_FLASH_CFG_CONFIG_REG[13-10] PERIPH_CS_LINES_FLD bits. Reset output OSPI_ECC_VECTOR is to be directly driven into corresponding dedicated RESET pins of the devices with separated RESET pin and alternatively, Reset output OSPI_ECC_VECTOR is to be control OSPI_ECC_VECTOR of the DQ3 RESET devices enabling separating of DQ3 Controller Outputs on SoC integration level.

The controller supports all combinations of CPHA and CPOL for Serial Clock. It allows the controller to support any SPI target devices not limited to Flash Memories. Multiple-SPI flash devices use just a subset of these combinations depending on the Transfer Mode as defined in Table 12-229.

Table 12-229. Flash SPI Modes

(SEL_CLK_POL_FLD, SEL_CLK_PHASE_FLD)	Edge Mode	Support
0x00 (SPI MODE 0)	SDR	Yes
0x01 (SPI MODE 1)	SDR	No
0x10 (SPI MODE 2)	SDR	No
0x11 (SPI MODE 3)	SDR	No
0x00 (SPI MODE 0)	DDR	Yes
0x01 (SPI MODE 1)	DDR	No
0x10 (SPI MODE 2)	DDR	No
0x11 (SPI MODE 3)	DDR	No

12.4.2.3.14 Selecting the Flash Instruction Type

In order to send the correct READ and WRITE opcodes, software should initialize the OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG and the OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG registers. These registers include fields to setup the required instruction opcodes that is intended to be used to access the FLASH (default is basic READ and basic page program) as well as the instruction type, edge mode (DDR or SDR) and whether the instruction uses single, dual, quad or octal pins for address and data transfer. Providing this level of control to the user provides a future proofed generic solution. To ensure the controller can operate from a reset state, the registers will be reset to an opcode compatible with SIO devices what can be modified using BOOT feature.

Despite being applicable for both READs and WRITEs, the OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD field only appears once – it is not included in the OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG register. If software sets this to anything other than '0', then the address transfer type and the data transfer type bits of both OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG and OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG registers become don't care. It is made available to allow software to support the less common FLASH instructions where the opcode, address and data are sent on 2 or 4 lanes (the opcode from most instructions are sent serially to the FLASH device, even for dual/quad instructions).

There are devices capable to handling Read Operations in Dual Data Rate Mode (DDR) (it is also called Dual Transfer Rate Mode (DTR)). That means they can issue and capture the data on both rising and falling edges during working with dedicated command type. This enables the controller to maintain throughput at twice lower frequency of OSPI clock. The Device Read Instruction Register has DDR enable bit which informs Octal-SPI Flash Controller that opcode written into Read Opcode field is capable with DDR command type. The other field defined in OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[19-16] DDR_READ_DELAY_FLD which enables the controller to shift the transmitted data in DDR mode. By default, data are shifted by 1 clock cycle to ensure hold timing greater than 0 during DDR transactions. It may not be sufficient for high reference clock frequency in accordance with the high dividers.

Table 12-230 shows how software should configure the OSPI module for selected specific READ and WRITE instruction supported by the abovementioned device.

Table 12-230. READ and WRITE Instruction Configuration

READ							
OPCODE	OPCODE sent over how many lanes / edge mode?	ADDRESS / DUMMY / MODE sent over how many lanes / edge mode?	DATA bytes sent over how many lanes / edge mode?	Instruction Type (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD)	Address transfer type (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[13-12] ADDR_XFER_TYPE_STD_MODE_FLD)	Data transfer type (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[17-16] DATA_XFER_TYPE_EXT_MODE_FLD)	DDR bit enable (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[10] DDR_EN_FLD)
READ	1/SDR	1/SDR	1/SDR	0	0	0	0
FAST_READ	1/SDR	1/SDR	1/SDR	0	0	0	0
DTR_FAST_READ	1/SDR	1/DDR	1/DDR	0	0	0	1
DOFR (Dual O/p Fast Read)	1/SDR	1/SDR	2/SDR	0	0	1	0
DIOFR (Dual I/O Fast Read)	1/SDR	2/SDR	2/SDR	0	1	1	0
DDIOFR (DTR Dual I/ O Fast Read)	1/SDR	2/DDR	2/DDR	0	1	1	1
QOFR (Quad O/p Fast Read)	1/SDR	1/SDR	4/SDR	0	0	2	0
QIOFR (Quad I/O Fast Read)	1/SDR	4/SRD	4/SDR	0	2	2	0
DQIOFR (DTR Quad I/ O Fast Read)	1/SDR	4/DDR	4/DDR	0	2	2	1
OOFR (Octal O/p Fast Read)	1/SDR	1/SDR	8/SDR	0	0	3	0
OIOFR (Octal I/O Fast Read)	1/SDR	8/SDR	8/SDR	0	3	3	0
DOIOFR (DTR Octal O/p Fast Read)	1/SDR	1/DDR	8/DDR	0	0	3	1
4DOIOFR (4-byte DTR Octal I/O Fast Read)	1/SDR	8/DDR	8/DDR	0	3	3	1
DCFR (Dual Command Fast Read)	2/SDR	2/SDR	2/SDR	1	Don't care	Don't care	0
DDCFR (DTR Dual Command Fast Read)	2/SDR	2/DDR	2/DDR	1	Don't care	Don't care	1
QCFR (Quad Command Fast Read)	4/SDR	4/SRD	4/SDR	2	Don't care	Don't care	0
DQCFR (DTR Quad Command Fast Read)	4/SDR	4/DDR	4/DDR	2	Don't care	Don't care	1
OCFR (Octal Command Fast Read)	8/SDR	8/SDR	8/SDR	3	Don't care	Don't care	0

Table 12-230. READ and WRITE Instruction Configuration (continued)

4DOCFR (4-byte DTR Octal Command Fast Read)	8/SDR	8/DDR	8/DDR	3	Don't care	Don't care	1
WRITE							
OPCODE	OPCODE sent over how many lanes?	ADDRESS / DUMMY / MODE sent over how many lanes?	DATA bytes sent over how many lanes?	Instruction Type (OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[9-8] INSTR_TYPE_FLD)	Address transfer type (OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[13-12] ADDR_XFER_TYPE_STD_MODE_FLD)	Data transfer type (OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[17-16] DATA_XFER_TYPE_EXT_MODE_FLD)	
PP	1	1	1	0	0	0	
DIFP (Dual Input Fast Program)	1	1	2	0	0	1	
DIEFP (Dual Input Extended Fast Program)	1	2	2	0	1	1	
QIFP (Quad Input Fast Program)	1	1	4	0	0	2	
QIEFP (Quad Input Extended Fast Program)	1	4	4	0	2	2	
OIFP (Octal Input Fast Program)	1	1	8	0	0	3	
OIEFP (Octal Input Extended Fast Program)	1	8	8	0	3	3	
DCPP (Dual Command Fast Program)	2	2	2	1	Don't care	Don't care	
QCPP (Quad Command Fast Program)	4	4	4	2	Don't care	Don't care	
OCPP (Octal Command Fast Program)	8	8	8	3	Don't care	Don't care	

Note

This data are applicable for both 3-byte or 4-byte address variants of the commands if did not indicate otherwise.

Note

In DTR protocol all transfer phases (including opcode) take DDR edge mode independently on the command under execution. DTR protocol is to be enabled by OSPI_FLASH_CFG_CONFIG_REG[24] ENABLE_DTR_PROTOCOL_FLD bit. It has higher priority than DDR Mode enable bit from OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[10] DDR_EN_FLD.

12.4.2.3.15 OSPI PHY Module

OSPI module fully integrates PHY module dedicated to more flexible and power efficient transfers.

The PHY module communicates with the OSPI Flash controller via the aforementioned PHY Interface and handles data transfer on low-level stage of design hierarchy. However, when the OSPI_RCLK is configured to be equal to the SPI clock instead of alternative approach using clock divider, there is just one OSPI_RCLK cycle (not 4 or more) within single SPI period or half period for DDR Mode (SPI Control Module works on reference clock). Given that OSPI_RCLK is the input clock for RX FIFO and the output one for TX FIFO, the PHY solution incurs more restrictive requirement for value of system clock in order to synchronize data without SPI transfer interruption. For example, when the controller operates in DDR 1× octal Mode, 2 bytes of data (equivalent to one RX FIFO location) is gathered within just single OSPI_RCLK cycle. The controller cannot predict next data access while operating in the Direct Mode (meaning its size or whether it is sequential to the previous one or not). As a result, if the OSPI_HCLK is not significantly greater than OSPI_RCLK, the SPI transfer has to be suspended until the Flash Command Generator forwards new data to TX FIFO.

An optional PHY Pipeline Mode is implemented to avoid the necessity of stable clocking of the system clock for the Direct Mode when the PHY mode is enabled and to keep maximum performance while ensuring correct operation of the OSPI controller with the PHY using low frequencies from all its domains. This mode is a trade-off between large software overhead when operating in the Indirect Mode and the described limitations present in the Direct Mode. For more information about PHY Pipeline Mode, see Section 12.4.2.3.15.1, *PHY Pipeline Mode*.

When DDR 2× Mode is granted based on configuration – SPI transfer is automatically performed using the PHY module even if the OSPI_FLASH_CFG_CONFIG_REG[3] PHY_MODE_ENABLE_FLD is de-asserted. SDR 2× commands are handled with PHY module paths being bypassed. Nevertheless, dividers of 2, 4 or 6 for DDR and divider of 2 for SDR should not be configured based on controller requirements and these configurations are perceived as a software error.

Note

Please refer to the OSPI Controller PHY Tuning Algorithm Application Note for additional details related to the OSPI PHY Module and Tuning Algorithm,

12.4.2.3.15.1 PHY Pipeline Mode

This mode is used for Direct Read Mode of operation. If any other operations are intended to be executed, it is recommended to disable PHY Pipeline Mode and re-enable for subsequent Direct Reads in PHY mode. Since there is comprehensive software mechanism controlling Read data transfers in Indirect Mode, pipeline of data interface accesses is not effective for this mode. Enable PHY Pipeline feature when at least four 4-byte-sized data words are predicted to be read in sequentially. The Flash Command Generator pipelines and puts them into TX FIFO which causes CS to remain active because low level SPI protocol controller controls TX FIFO fill level. In order to correctly trigger Direct Read in Pipeline Mode TX FIFO must be empty. Therefore first polling of OSPI_FLASH_CFG_CONFIG_REG[31] IDLE_FLD bit needs to be done. The sequential data transfer will be interrupted when the data target select signal of the data interface is asserted to low. This information is also detected by Data Target Module which informs the Flash Command Generator that the next access is invalid and a TX FIFO locations can be flushed transparently for the system.

In PHY Pipeline Mode it is recommended for Data Controller not to introduce wait states in between consecutive occurrences of the data interface signal that indicates transfer has finished. It will ensure regular transfer rate on data side. Introducing wait states gradually slows data transfer rate down and may finally cause SPI transfer interruption because of TX FIFO data starvation. The system, however, may need to introduce some number of wait states after completion of sequential transfer (composed of 4-byte sized data words) for progressing the data. The dedicated buffer is implemented in Data Target Controller which collects all incoming data during wait states injection. In order to keep SPI transfer uninterrupted, number of wait states should be as little as possible. The higher the OSPI_HCLK/ OSPI_RCLK ratio the more wait states can be introduced without SPI transfer interruption. In case the system is able to launch a new transfer before wait states overflow, buffered data transfer to the host will continue. It compensates slowed down transfer by introducing wait states. In case the system is not able to launch a new transfer before wait states overflow, next incoming transfer is considered non-sequential and is executed after all pipelined data is flushed.

This mode can be enabled when following conditions are met:

- OSPI_HCLK > OSPI_RCLK (Comparing the slow data clock with the fast reference one makes Pipeline Mode ineffective – Suspend of SPI Transfer would be possible. Consequently, this condition has to be met to operate in this mode.)
- Only 4-byte sized Data Words are permitted (This ensures more data clock cycles for synchronization of FIFOs between consecutive pulses of the signal indicating transfer has finished.)
- The transfer with introduced wait states or non-sequential transfers can only be triggered in between at least four 4-byte sized Data Bursts sequential accesses (16 Bytes) to be sure that Data Controller can trust buffered incoming data during wait states injection.
- Do not use Pipeline Mode along with Continuous Mode (XIP). Benefit of XIP is limited for bulk data transfers intended to execute in Pipeline Mode.

12.4.2.3.15.2 Read Data Capturing by the PHY Module

Read Data Capturing by the PHY module is useful, as the user is not responsible for the design dedicated DLL being compatible with the Octal-SPI Flash Controller. Another benefit is an option to adjust both SPI clock and sampling clock in a very wide range to fit them into individual requirements of any system. If loopback clock (OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[0] BYPASS_FLD) and PHY mode (OSPI_FLASH_CFG_CONFIG_REG[3] PHY_MODE_ENABLE_FLD) are both enabled, the loopback clock is driven into RX DLL instead of gated reference clock. Because of the architecture of DLL, loopback clock needs to be provided in SPI Mode 0. If DQS (OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG[8] DQS_ENABLE_FLD) and PHY mode (OSPI_FLASH_CFG_CONFIG_REG[3] PHY_MODE_ENABLE_FLD) are both enabled, the DQS is driven into RX DLL instead of gated reference clock.

12.4.2.3.16 OSPI Programming Guide

12.4.2.3.16.1 Configuring the OSPI Controller for Use After Reset

The OSPI controller has been designed to wake up in a state that is suitable for performing basic reads and writes using the direct access controller. The BASIC read (opcode 0x03) and BASIC write (opcode 0x02) instructions are operations supported by all target devices. The controller also wakes up with a baud rate divider setting of divide-by-32. Assuming the reference clock is operating at 400 MHz after reset, then this means the effective SPI clock is just 12.5 MHz. This should be slow enough to meet all timing requirements of all target devices without any further device programming.

If the target device does not use 3 address bytes, the device size configuration register must be modified to the appropriate size.

If software plans to write to the device, and the number of bytes per device page is not equal to 256, then the device size configuration register must also be modified.

While not a requirement, it is prudent for software to enable the write protect feature prior to enabling the OSPI controller. This will block any data writes from taking effect. To do so, the protection registers (OSPI_FLASH_CFG_LOWER_WR_PROT_REG, OSPI_FLASH_CFG_UPPER_WR_PROT_REG and OSPI_FLASH_CFG_WR_PROT_CTRL_REG) should be setup and the number of bytes per device block in the device size configuration register should also be setup.

After Power-on Reset (POR), software can read from and write to the FLASH device (albeit slowly). Enabling/Disabling the controller and DAC is achieved with just one write to corresponding fields of the OSPI_FLASH_CFG_CONFIG_REG register. User shall take note to maintain the default values of the baud rate divisor and the default state of SEL_CLK_POL_FLD/ SEL_CLK_PHASE_FLD bits of this register. A write data value of 0x00780081 is recommended.

12.4.2.3.16.2 Configuring the OSPI Controller for Optimal Use

Note

When using the OSPI Controller, the opcodes in OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[7-0] RD_OPCODE_NON_XIP_FLD, OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG[7-0] WR_OPCODE_FLD and OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG[7-0] OPCODE_FLD bit fields shall not match the opcode in the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD bit field.

For high speed transfers PHY mode can be enabled and for optimal configuration PHY Pipeline mode is recommended. For more information, see *PHY Pipeline Mode*.

To access the flash optimally, software must configure the controller accurately:

1. Wait until any pending STIG or INDAC operation has completed or poll OSPI_FLASH_CFG_CONFIG_REG[31] IDLE_FLD bit.
2. Disable the DAC through OSPI_FLASH_CFG_CONFIG_REG[7] ENB_DIR_ACC_CTLR_FLD bit. It is permitted, but not necessary to also disable the OSPI controller completely via OSPI_FLASH_CFG_CONFIG_REG[0] ENB_SPI_FLD bit.
3. Update the OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG and OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG registers for the instruction type you wish to use for indirect and direct writes and reads.
4. Update the OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field if mode bits have been enabled in the OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG[20] MODE_BIT_ENABLE_FLD bit.
5. Update the OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG if the contents are incorrect. Note parts or all of this register may have been updated after initialization. The number of address bytes is a key configuration setting required for performing reads and writes. The number of bytes per page is required for performing any write. The number of bytes per device block is only required if the write protect feature is used. If the

default values are correct for the target device, or if some of the values (not including the number address bytes) were incorrect but device writes were not permitted.

6. Update the OSPI_FLASH_CFG_DEV_DELAY_REG. This register allows the user to tweak how the chip select is driven after each FLASH access. This is required as each device may have different timing requirements. As the serial clock frequency is increased, these timing requirements become more important. Note the numbers programmed in this register are based on the period of reference clock. Example: A device needs 50ns minimum time before CS can be re-asserted after it has been de-asserted. By default, the controller will only provide a minimum of 1 SCLK period. When the device is operating at 100 MHz, the SCLK period is only 10ns, so 40ns extra is required. Since the register defines the number of reference clock cycles to add, and reference clock is running at 400 MHz (2.5ns period), then the user should program a value of at least 16 to the OSPI_FLASH_CFG_DEV_DELAY_REG[31-24] D_NSS_FLD. This delay can be extended during auto-polling phase. There is possibility to define the polling repetition delay in the OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG[31-24] POLL_REP_DELAY_FLD bit field.
7. Update the OSPI_FLASH_CFG_REMAP_ADDR_REG register, if required. Affects DAC path only.
8. Setup and enable write protection registers (OSPI_FLASH_CFG_LOWER_WR_PROT_REG, OSPI_FLASH_CFG_UPPER_WR_PROT_REG and OSPI_FLASH_CFG_WR_PROT_CTRL_REG) if they are required and if they have not already been setup from post initialization.
9. Enable required interrupts via the OSPI_FLASH_CFG_IRQ_MASK_REG register.
10. Setup the baud rate divisor in the OSPI_FLASH_CFG_CONFIG_REG[22-19] MSTR_BAUD_DIV_FLD to define the required clock frequency of the target device.
11. Update the OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG register. This register will delay when the read data is captured and can help when the read data path from the device to the controller is long and the device clock frequency is high. An update to this register may not be necessary.
12. Enable the OSPI controller and the DAC via the OSPI_FLASH_CFG_CONFIG_REG.

12.4.2.3.16.3 Using the Flash Command Control Register (STIG Operation)

The OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register provides software means to access the FLASH device in a flexible and programmable manner. This is known as a STIG operation (Software Triggered Instruction Generator). The instruction opcode, number of address bytes (if any), the address itself, number of dummy cycles (if any), number of write data bytes (if any), the write data itself and the number of read data bytes (if any) can be programmed. Once these have been programmed, software can trigger the command via OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD bit and wait for its acceptance by polling OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[1] CMD_EXEC_STATUS_FLD bit. When CMD_EXEC_STATUS_FLD bit turns de-asserted, another STIG can be triggered. This method of accessing the FLASH is the typical mechanism that software would use to access the FLASH device's registers, as well as for performing ERASE operations. It can also be used to access the FLASH array itself, although the maximum of 8 data bytes may be read or written at any one time, defined in the Flash Command Write and Read Data registers (OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG, OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG, OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG and OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG). This number of bytes can be extended for Read Data commands using additional STIG Memory Bank controlled by OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG[2] STIG_MEM_BANK_EN_FLD and OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG.

Commands issued using this interface have a higher priority than all other READ accesses coming from data interface, and will therefore interrupt any READ commands being requested by the indirect or direct controllers.

12.4.2.3.16.4 Using SPI Legacy Mode

SPI legacy mode allows software to access the internal TX-FIFO and RX-FIFO directly, thus bypassing the direct, indirect and STIG controllers.

Legacy mode allows the user to issue any FLASH instruction to the device, but does place a heavy software overhead in order to manage the fill levels of the FIFO's effectively. This is because the legacy SPI core is bi-directional in nature, with data continuously being transferred in either direction while the chip select is enabled. Even if the driver only wishes to read data from the FLASH device, dummy data must be written out to ensure the chip select stays active, and vice versa for write transactions.

Since the TX-FIFO and RX-FIFO are of limited depth, software has a responsibility to maintain the FIFO levels to ensure the TX-FIFO does not become exhausted during the instruction execution and the RX-FIFO doesn't overflow. This can place a lot of overhead on software. Interrupts are provided to indicate when the fill levels pass programmable watermarks, which are themselves programmable registers OSPI_FLASH_CFG_TX_THRESH_REG and OSPI_FLASH_CFG_RX_THRESH_REG.

The limited depth may impose the limitation over execution of some specific SPI commands in legacy mode. Note that the controller interprets all transmitted bytes as valid. For example, if the Flash Device was configured to return valid data after many dummy cycles, the TX FIFO could become full before the controller sends all of dummy data.

12.4.2.3.16.5 Entering XIP Mode from POR

XIP is a mode that can be entered in a non-volatile way if the device has XIP enabled as a non-volatile configuration setting. Software will not be able to discover the state of XIP from POR via FLASH status register reads as the only operation a FLASH device will recognize when XIP mode is enabled is an XIP read operation.

If it is already known that the device will enter XIP from POR, then the OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG[7-0] MODE_FLD and OSPI_FLASH_CFG_CONFIG_REG[18] ENTER_XIP_MODE_IMM_FLD bits should be set in initial boot.

If it is not already known that the device will enter XIP from POR, and XIP from POR may be supported by the attached FLASH device, then software can attempt to exit XIP mode by issuing an XIP exit command using a STIG command (via the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG register). To do this, software must be aware of the mode bit requirements of that device, as XIP entry and exit changes per device.

12.4.2.3.16.6 Entering XIP Mode Otherwise

XIP mode is supported in most FLASH devices. Some of them use signature bits that are sent to the device immediately following the address bytes, other use signature bits and also require a FLASH device configuration register write to enable XIP. For the FLASH devices that must be compliant to the OSPI controller, the following steps can be taken by software to enter XIP mode:

1. Disable the DAC and INDAC (OSPI_FLASH_CFG_CONFIG_REG[7] ENB_DIR_ACC_CTLR_FLD) to ensure no new data read accesses will be sent to the FLASH device.
2. (Optional)Configure the OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG to issue a VCR write to FLASH memory, because XIP mode must first be enabled for some devices.
3. Configure the XIP mode bits in the OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG[7-0] MODE_FLD bit field.
4. Enable the local controllers XIP mode by setting OSPI_FLASH_CFG_CONFIG_REG[17] ENTER_XIP_MODE_FLD bit.
5. Re-enable the DAC and, if required, the INDAC.

12.4.2.3.16.7 Exiting XIP Mode

To exit XIP mode, software should first disable the DAC and INDAC to ensure no new data read accesses will be sent to the FLASH device. It should then set mode bits to other than the established in the corresponding Flash Device specifications. These are dependent on the FLASH device and manufacturer. Software should then reset OSPI_FLASH_CFG_CONFIG_REG[17] ENTER_XIP_MODE_FLD.

Note the FLASH device must see a READ instruction before it can disable its internal XIP mode state, so this means XIP mode will internally stay active until the next READ instruction is serviced. User must take care to ensure that XIP mode is disabled before the end of any READ sequence.

12.4.3 HyperBus

This section describes the Hyperbus Interface (HPB) for the device.

12.4.3.1 HyperBus Overview

The HyperBus module is a part of the device Flash Subsystem (FSS). For more information about FSS, see *Flash Subsystem (FSS)*.

The HyperBus module is a low pin count memory interface that provides high read/write performance. The HyperBus module connects to HyperBus memory (HyperFlash or HyperRAM) and uses simple HyperBus protocol for read and write transactions.

There is one HyperBus™ module inside the device. The HyperBus module includes one HyperBus Memory Controller (HBMC).

Figure 12-188 shows the HyperBus module overview.

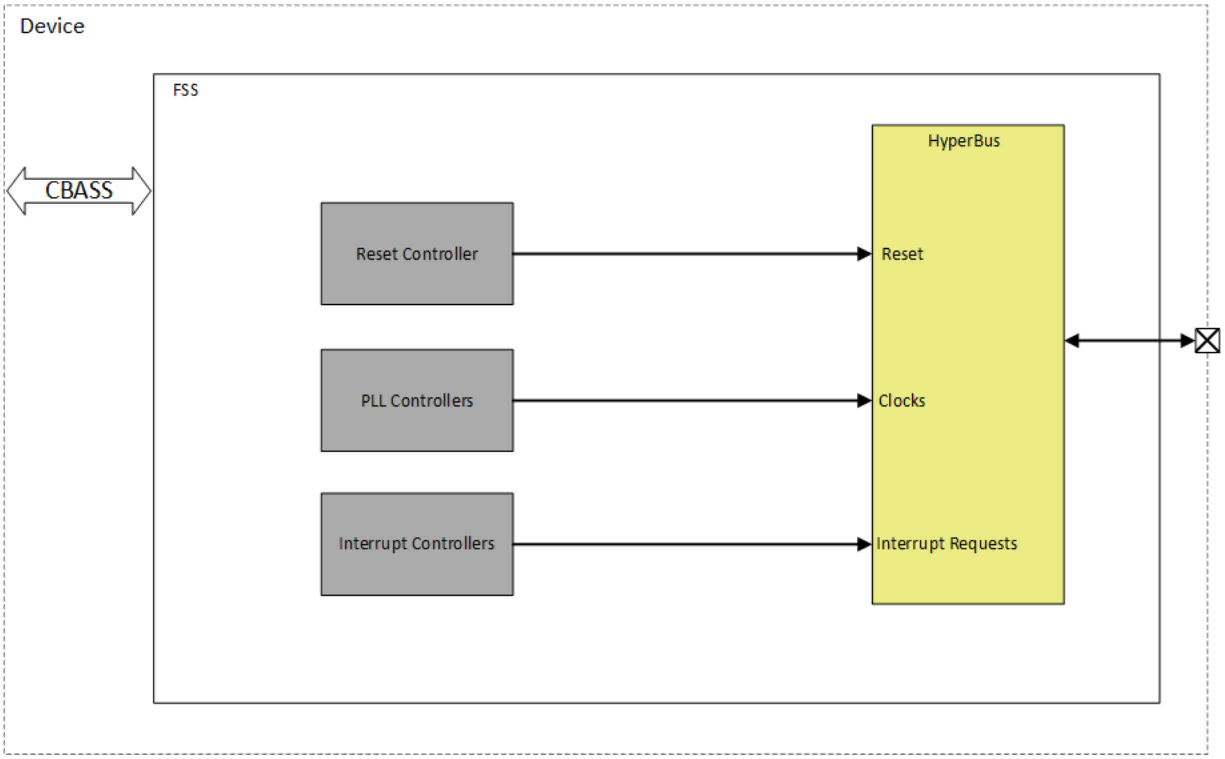


Figure 12-188. HyperBus Overview

12.4.3.1.1 HyperBus Features

- Support for Cypress® HyperFlash and HyperRAM
- Up to 166 MHz maximum memory bus operation for reads
  - Supports up to 166 MHz dual data rate (333 MBps) flash devices for system requiring rapid boot or instant-on displays
  - Supports up to 333 MBps external pseudo-RAM (HyperRAM) for systems

  Note: For more information, see section Timing and Switching Characteristics in the device-specific Datasheet.
- Low pin count interface with LVCMOS I/O pins (can be muxed with other FSS interfaces (OSPIs))
- Two memory chip selects
- Linear incrementing mode for reads and writes
- Up to 16 outstanding read transactions (see Section 12.4.3.3.3, *HyperBus True Continuous Read (TCR) Mode*)
- Asynchronous bus clock

12.4.3.1.2 HyperBus Not Supported Features

- Cache-line wrap and fixed address modes for reads or writes
- General Purpose Output register (MCU_FSS0_HPB0_MC_GPOR) of the HBMC is not used

12.4.3.2 HyperBus Environment

This section describes the HyperBus external connections (environment).

Figure 12-189 shows the HyperBus connected to HyperRAM or HyperFlash.

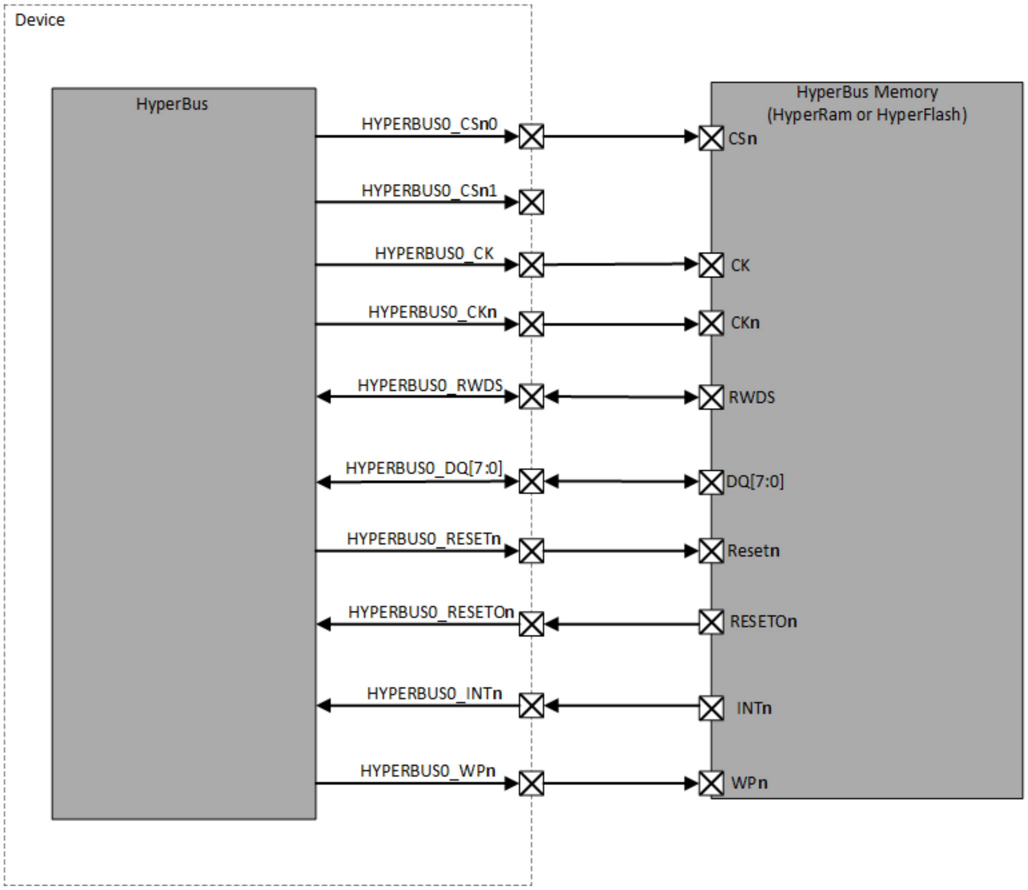


Figure 12-189. HyperBus Connected to HyperRAM or HyperFlash

HyperBus I/O Signals describes the HyperBus I/O signals.

Table 12-231. HyperBus I/O Signals

Module Pin	Device Level Signal[1]	I/O[2]	Description	Module Pin Reset Value
		MCU_FSS0_HPB0		
CK	HYPERBUS0_CK	O	HyperBus Clock Output (differential)	0x0
CK**n**	HYPERBUS0_CK**n**	O	HyperBus Inverted Clock Output (differential)	0x1
RWDS	HYPERBUS0_RWDS	I/O/HiZ	HyperBus Read/Write Data Strobe	0x1
DQ[7:0]	HYPERBUS0_DQ[7:0]	I/O/HiZ	HyperBus Data	0x0
CS**n**0	HYPERBUS0_CS**n**0	O	HyperBus Chip Select 0	0x1
CS**n**1	HYPERBUS0_CS**n**1	O	HyperBus Chip Select 1	0x1
RESET**n**	HYPERBUS0_RESET**n**	O	HyperBus Reset Output	0x1
RESETO**n**	HYPERBUS0_RESETO**n**	I	Reset State Indicator (output from HyperBus memory)	0x1
INT**n**	HYPERBUS0_INT**n**	I	Memory Interrupt (output from HyperBus memory)	0x1
WP**n** [3]	HYPERBUS0_WP**n**	O	HyperBus Write Protect (output to HyperBus memory)	0x1

(1) **n** - Active Low
(2) I = Input; O = Output; HiZ = High Impedance

(3) WP**n** pin is not used on Cypress flash devices.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.4.3.3 HyperBus Functional Description

The HyperBus module is a high throughput memory interface. It is a part of the device FSS and provides execute in place (XIP) operation and block copy access to HyperBus memory devices (HyperRAM and HyperFlash). The FSS enables in-line ECC protection and authentication features for the HyperBus module.

For more information about FSS, see *Flash Subsystem (FSS)*.

The HyperBus module is compliant to the *Cypress HyperBus™ Specification v1.2*.

Figure 12-190 shows the HyperBus module block diagram.

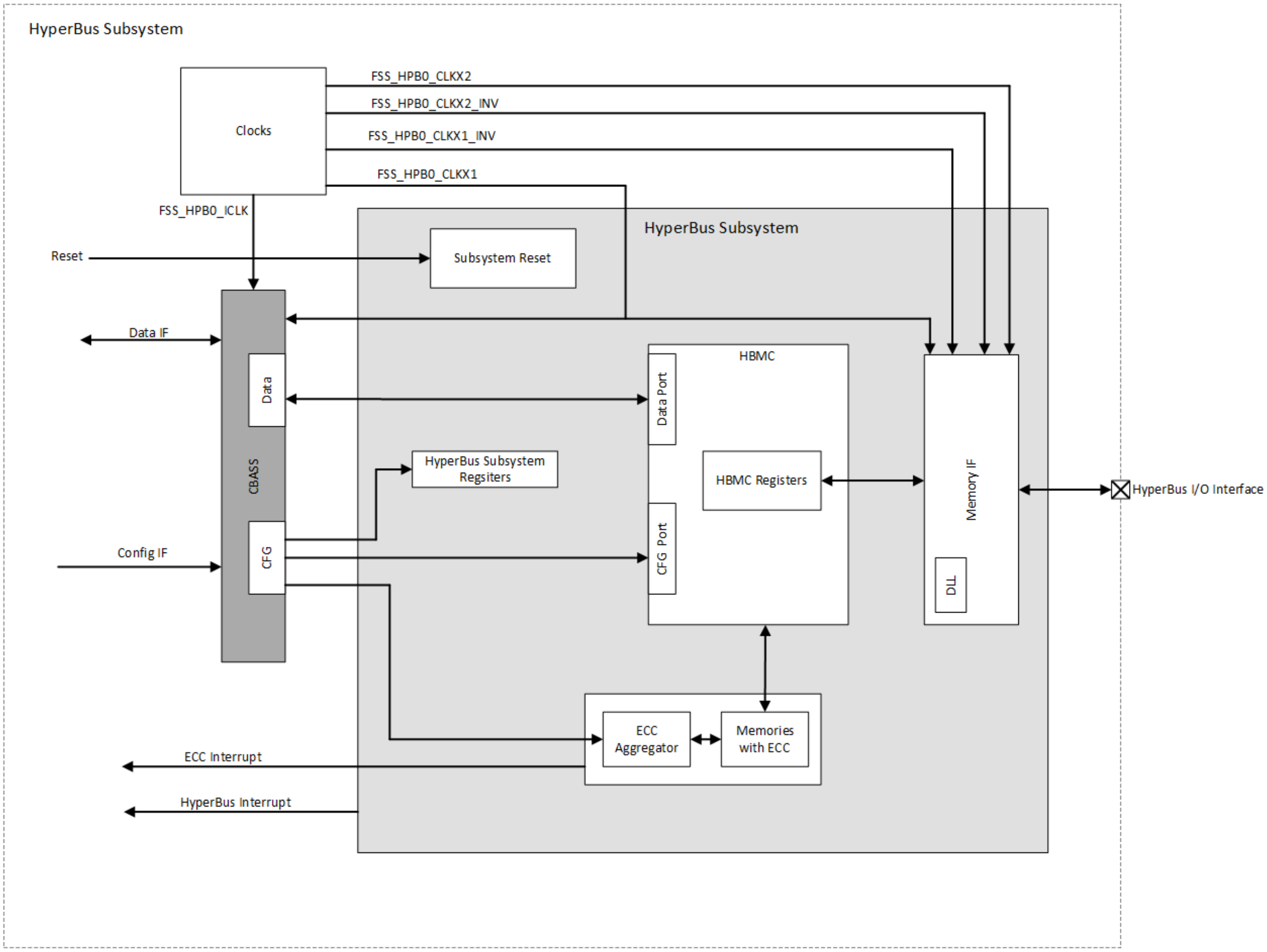


Figure 12-190. HyperBus Module Block Diagram

Basic Blocks:

- HBMC: The HyperBus Memory Controller (HBMC) is the main part (the core) of the HyperBus Subsystem and provides accessibility to external HyperBus memory (HyperFlash or HyperRAM) using simple HyperBus protocol for data read and write transfers.
  - The Data Port on the HBMC is used for CBASS data slave interface to access the external HyperBus memory.
  - The CFG Port on the HBMC is used for configuration of the HBMC registers.
- HyperBus I/O Interface: The HyperBus I/O Interface includes all used interface pins (for more information, see *HyperBus I/O Signals*).
- Memory IF: The Memory IF block implements the following functionality:
  - Use DLL to delay the incoming read data strobe from the memory

- FIFO Memories with ECC: There are internal HyperBus FIFOs implemented with memories that are used during read and write transactions. These FIFO memories are ECC protected (for more information about the FIFOs, see Section 12.4.3.3.2, *HyperBus Internal FIFOs*).
- ECC Aggregator: The ECC Aggregator facilitates aggregating and reporting internal HyperBus FIFO memory errors (for more information, *ECC Aggregator*).
- HBMC Registers: This block includes set of all used HBMC registers.
- HyperBus Subsystem Registers: This block implements memory-mapped registers at the HyperBus Subsystem level.
- ECC Aggregator Registers: This block includes all used ECC Aggregator registers.

  For more information about all HyperBus registers, see *FSS_HYPERBUS1P0_0*.
- CBASS: The CBASS interconnect implements the clock domain crossing bridges needed to separate the two main clock domains: CBASS clock domain and Memory clock domain.
- Data IF: The Data Slave IF on the interconnect is a 32-bit wide interface and is used to access an external HyperBus memory via the Data Port on the HBMC. The data interface supports linear incrementing addresses only. Cache-line wrap and fixed addressing modes are not supported.
- Config IF: The Config Slave IF on the interconnect is a 32-bit wide interface and is used to access the HBMC registers (via the CFG Port on the HBMC), HyperBus Subsystem registers, and ECC Aggregator registers. The config interface also supports linear incrementing address mode only.
- For more information about supported and not supported HyperBus features, see *HyperBus Overview*.
- Clocks, Subsystem Reset, Interrupts: For more information about HyperBus Clocks, Resets, and Interrupts, see *Module Integration*.

12.4.3.3.1 ECC Aggregator

For more information about ECC Aggregator, refer to *ECC Aggregato*r.

12.4.3.3.2 HyperBus Internal FIFOs

There are 10 FIFO buffers in the module that help improve performance. Table 12-232 shows the HyperBus FIFOs details.

Table 12-232. HyperBus FIFOs

Buffer Name	Size (Width x Depth)
Address (ADR) FIFO	Two port RAM – 16 x 46-bit
Write data (WDAT) FIFO	Two port RAM – 256 x 40-bit
Write status (BDAT) FIFO	Two port RAM – 16 x 2-bit
Read data (RDAT) FIFO	Two port RAM – 128 x 40-bit
Receive (RX) FIFO	Two port RAM – 256 x 20-bit
Address write (AW) FIFO	Two port RAM – 16 x 44-bit
Write ID (WID) FIFO	Two port RAM – 16 x 2-bit
Address write ID (AWID) FIFO	Two port RAM – 16 x 14-bit
Address read (AR) FIFO	Two port RAM – 16 x 44-bit
Address read ID (ARID) FIFO	Two port RAM – 16 x 18-bit

12.4.3.3.3 HyperBus True Continuous Read (TCR) Mode

The HBMC supports True Continuous Read (TCR) operation for HyperFlash. This feature is able to improve HyperFlash read performance.

When this feature is enabled, the HBMC can merge multiple up to 16 max burst read commands that are present in its command FIFO into a single memory read transaction to the HyperFlash memory. As a result, the command input and initial latency for the latter burst read commands are saved, which leads to improved throughput.

12.4.3.4 HyperBus Programming Guide

12.4.3.4.1 HyperBus Initialization Sequence

The HBMC provides two sets of Memory Base Address, Memory Configuration and Memory Timing registers to access devices connected to the two external chip selects. The following programming guidelines need to use the correct set of registers depending on which chip select is accessed.

The HBMC compares the input address bits [31-24] to the value programmed in the MCU_FSS0_HPB0_MC_MBAR_y registers to determine the external chip select that is accessed.

12.4.3.4.1.1 HyperFlash Access

Table 12-233. HyperFlash Access Sequence

Step	Description
1.	Ensure that the FIFO RAM auto-initialization is complete by reading the HYPERBUS_SYSCFG_RAM_STAT_REG[0] INIT_DONE bit .
2.	Lock MDLL:
	- To ensure that the MDLL in the HyperBus is locked, the reset to the HyperBus module should be de-asserted only after all the clock inputs are stable at the desired operating frequency. The MDLL can lose the lock if the frequencies of the clock inputs to the HyperBus module are changed during operation.
	- To ensure that the MDLL is stabilized, the following sequence is required. Boot code should attempt to read 64 bytes of Flash data, for 16 iterations, and if the data is the same in 4 successive iterations, the DLL can be considered to be stabilized and the software proceed with normal Flash access .
	- The HYPERBUS_SYSCFG_DLL_STAT_REG[0] MDLL_LOCK and HYPERBUS_SYSCFG_DLL_STAT_REG[1] SDL_LOCK bits can be used to determine if the controller delay line and target delay line have locked, respectively .
3.	Initialize Memory Configuration register (HYPERBUS_CORE_MCR_J):
	- HYPERBUS_CORE_MCR_J[31] MAXEN bit and HYPERBUS_CORE_MCR_J[26-18] MAXLEN bit field based on burst transaction length to memory.
	- HYPERBUS_CORE_MCR_J[17] TCMO = 1h, to enable HBMC to merge multiple accesses with sequential addresses into a single memory access. This improves memory throughput.
	- HYPERBUS_CORE_MCR_J16] ACS = 0h, to set 'No asymmetry cache system support'.
	- HYPERBUS_CORE_MCR_J[5] CRT = 0h, to set 'Memory space' instead 'CR space'.
	- HYPERBUS_CORE_MCR_J[4] DEVTYPE = 0h, to set 'HyperFlash' instead 'HyperRAM'.
	- HYPERBUS_CORE_MCR_J[1-0] WRAPSIZE = 00h, since the HBMC does not support wrap bursts.
4.	Initialize Memory Timing register (HYPERBUS_CORE_MTR_J) based on timing of the memory device being used.
5.	Initialize Memory Base Address register (HYPERBUS_CORE_MBAR_J):
	- HYPERBUS_CORE_MBAR_J[31-24] A_MSB = 8 MSB bits of memory address space. This defines the start of the 16 MB address region in the system memory where the HyperFlash can be accesed. The HBMC initiates HyperFlash access to any memory mapped access in this range.
6.	Check the HYPERBUS_CORE_CSR[10] RRSTOERR bit in Controller Status register to ensure that the HyperFlash is out of reset.
7.	Normal HyperFlash access can be performed after this.
8.	The HyperFlash device registers and CFI (Common Flash Interface) region can be accessed by read/write transactions to the offset from the base address as specified in the device command summary table.
9.	The HyperFlash memory data array can be read as memory mapped access.
10.	The HyperFlash write sequence needs to be followed to update contents of the memory array.

12.4.3.4.1.2 HyperRAM Access

Table 12-234. HyperRAM Access Sequence

Step	Description
1.	Wait 150µs for RAM to power up after reset. The HyperRAM does not provide any feedback on reset/ready state to the HBMC .
2.	Ensure that the FIFO RAM auto-initialization is complete by reading the HYPERBUS_SYSCFG_RAM_STAT_REG[0] INIT_DONE bit .
3.	Lock MDLL:
	- To ensure that the MDLL in the HyperBus is locked, the reset to the HyperBus module should be de-asserted only after all the clock inputs are stable at the desired operating frequency . The MDLL can lose the lock if the frequencies of the clock inputs to the HyperBus module are changed during operation.
	- To ensure that the MDLL is stabilized, the following sequence is required. Boot code should attempt to read 64 bytes of RAM data, for 16 iterations, and if the data is the same in 4 successive iterations, the DLL can be considered to be stabilized and the software proceed with normal RAM access .
	- The HYPERBUS_SYSCFG_DLL_STAT_REG [0] MDLL_LOCK and HYPERBUS_SYSCFG_DLL_STAT_REG 1] SDL_LOCK bits can be used to determine if the controller delay line and target delay line have locked, respectively .
4.	Initialize Memory Configuration register (HYPERBUS_CORE_MCR_J):
	- HYPERBUS_CORE_MCR_J[31] MAXEN bit and HYPERBUS_CORE_MCR_J[26-18] MAXLEN bit field based on burst transaction length to memory.
	- HYPERBUS_CORE_MCR_J[17] TCMO = 0h, since HBMC does not support command merging for HyperRAM accesses.
	- HYPERBUS_CORE_MCR_J[16] ACS = 0h, to set 'No asymmetry cache system support'.
	- HYPERBUS_CORE_MCR_J[5] CRT = 0h or 1h, depending on what needs to be accessed (memory or register space).
	- HYPERBUS_CORE_MCR_J[4] DEVTYPE = 1h, to set 'HyperRAM' instead 'HyperFlash'.
	- HYPERBUS_CORE_MCR_J[1-0] WRAPSIZE = 00h, since the HBMC does not support wrap bursts.
5.	Initialize HYPERBUS_CORE_MTR_J register based on timing of the memory device being used.
6.	Initialize HYPERBUS_CORE_MCR_J register:
	- HYPERBUS_CORE_MCR_J[31-24] A_MSB = 8 MSB bits of memory address space. This will define the start of the 16 MB address region in the system memory where the HyperRAM can be accesed. The controller will initiate HyperRAM access to any memory mapped access in this range.
7.	Check the HYPERBUS_SYSCFG_DLL_STAT_REG[0] MDLL_LOCK bit to ensure the Controller DLL is locked.
8.	Normal HyperRAM access can be performed after this.
9.	The HyperRAM device registers can be accessed by read/write transactions to the offset from the base address as specified in the device command summary table with HYPERBUS_CORE_MCR_J[5] CRT bit set to register space.
10.	The HyperRAM memory data array can be read/written to as memory mapped access with HYPERBUS_CORE_MCR_J[5] CRT bit set to memory space.

Note

HyperRAM devices have a 150µs startup time. Software needs to wait this duration after reset to initiate transactions to a HyperRAM device.

12.4.4 OptiFlash Submodules

12.4.4.1 Regional L2-Cache (RL2)

12.4.4.1.1 RL2 Overview

The Remote L2 (RL2) is responsible for caching 1 to 16MB of target space using system memory for the actual cache data storage (remote cache data storage memory). This significantly reduces the size of the L2 cache module while allowing flexible configuration for target applications.

The RL2 does not modify any request for the CPU that is within a RL2 caching range. This allows the critical word first (CWF) to be processed by the downstream module for best performance. A downstream CBA3-to-CBA4 bridge is suggested if it's required for a downstream CBA4 fabric be able to split any request that is a wrapping burst that is not aligned to the burst size boundary and targeting system SRAM.

Since the RL2 is expected to cache data from a slow peripheral like a Flash device, the request is aligned to the burst boundary and the RL2 restores the critical word first returned data to the CPU. RL2 supports split burst returns, all requested burst must be returned as full bus words (8 bytes). Split burst returns less than 8 bytes disable the RL2 or post an error.

The Remote L2 (RL2) is an 8 Way set associative read allocate LRU cache. The RL2 allocation is based on full cache line reads. The *SET* index is based on the programmed operating size.

The RL2 uses 32-byte cache lines which matches the R5 CPU cache line so that best performance is achieved. That is, the RL2 does not read more data than the CPU requested. Once a cache line is in the RL2, the CPU can read any quanta of data from that cache line.

Since the RL2 cache data is in system memory, the system must ensure the RL2 is protected from other accesses to prevent cache corruption. The RL2 passes the secure, priv and privid from the originating initiator for any operations that *DO NOT* go to the translated remote cache data storage memory. Any transaction to the translated remote cache data storage memory contains the secure, priv and privid from the RL2 Privilege InterFace (PIF).

Since the RL2 filters an address range to be cached, the RL2 passes through any address not within that range or crosses a cache line boundary, the SOC must ensure that the placement of the RL2 does not create a loop in the fabric. The proper use of the RL2 is that the CPUs are upstream to the RL2, and the flash, and remote cache data storage memory is downstream to the RL2.

The RL2 can be used to cache peripherals like flash, PCIe or Hyperlink, so the SOC need to ensure that these targets are downstream of the RL2.

The RL2 does not change the size or 32-byte offset of any transaction going through the module, that is, the byte count or offset (caddress[4:0]) of any command are left as is. This allows the cbytecnt, wcnt, rcnt, rbytecnt and ralign[4:0] to be passed through unmodified. Since the remote cache data storage memory addresses are aligned to 2K boundaries, and WAYs are aligned to 32 boundaries, the offset alignment within a cache access to the remote cache data storage memory is always the same as the requested offset.

The RL2 support a Dual Mode which allows two cache lines to share a single WAY, offering double the remote cache data storage memory while only using the same number of total cache line entries supported. Since Dual Mode shares the same bits within a WAY, the cacheable range is reduced to support the management for the two sub cache lines.

12.4.4.1.1.1 RL2 Supported Features

- UP to 4096 L2 cache lines supported
- 32 byte cache line size supported
- configurable cache size up to 4096 entries; 8K, 16K, 32K, 64K, 128K. Note: The cacheable target space will proportionately vary based on the cache size.
  - Up to 1MB of cacheable target space for 8KB of cache
  - Up to 2MB of cacheable target space for 16KB of cache
  - Up to 4MB of cacheable target space for 32KB of cache
  - Up to 8MB of cacheable target space for 64KB of cache
  - Up to 16MB of cacheable target space for 128KB of cache
  - Up to 8MB of cacheable target space for 256KB of cache (Dual Mode)
- 8-Way set associative LRU Cache
- ECC protected Tag LRU RAM

12.4.4.1.2 Environment

This section describes the OptiFlash module's connectivity and environment

12.4.4.1.2.1 Connectivity Examples

The Remote L2 OptiFlash module (RL2_OF) can be connected to multiple CPU or per CPU.

In the below figure, an example is shown where a single RL2_OF is used to RAT, FLC, and cache Flash code for multiple CPU

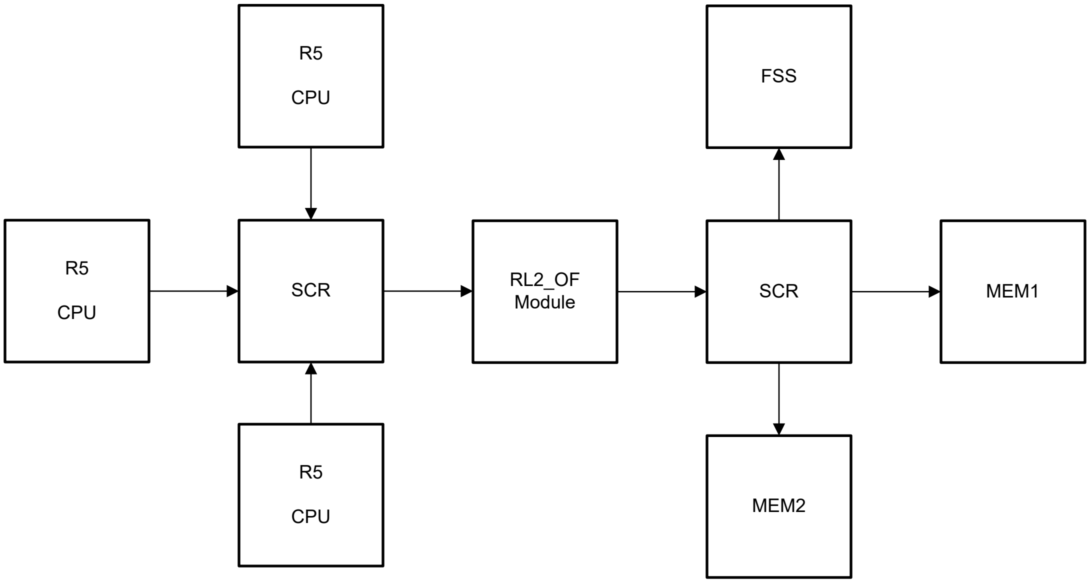


Figure 12-191. Connectivity of the RL2_OF Module - Multiple CPU

In the below example connectivity of a single RL2_OF for each CPU to RAT, FLC or cache Flash code. The benefit is that each CPU has a full use of a RL2_OF. However, if CPUs are executing code in common areas, would result in reading the same data for each CPU sharing code.

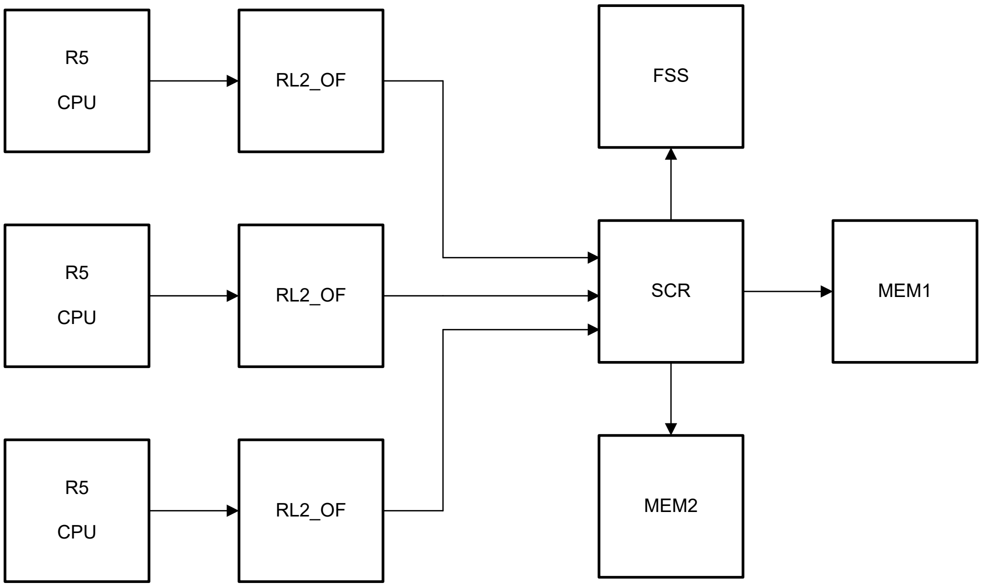


Figure 12-192. Connectivity of the RL2 Module - Per CPU

12.4.4.1.3 Functional Description

12.4.4.1.3.1 Block Diagram

Below is the Block Diagram for the OptiFlash module

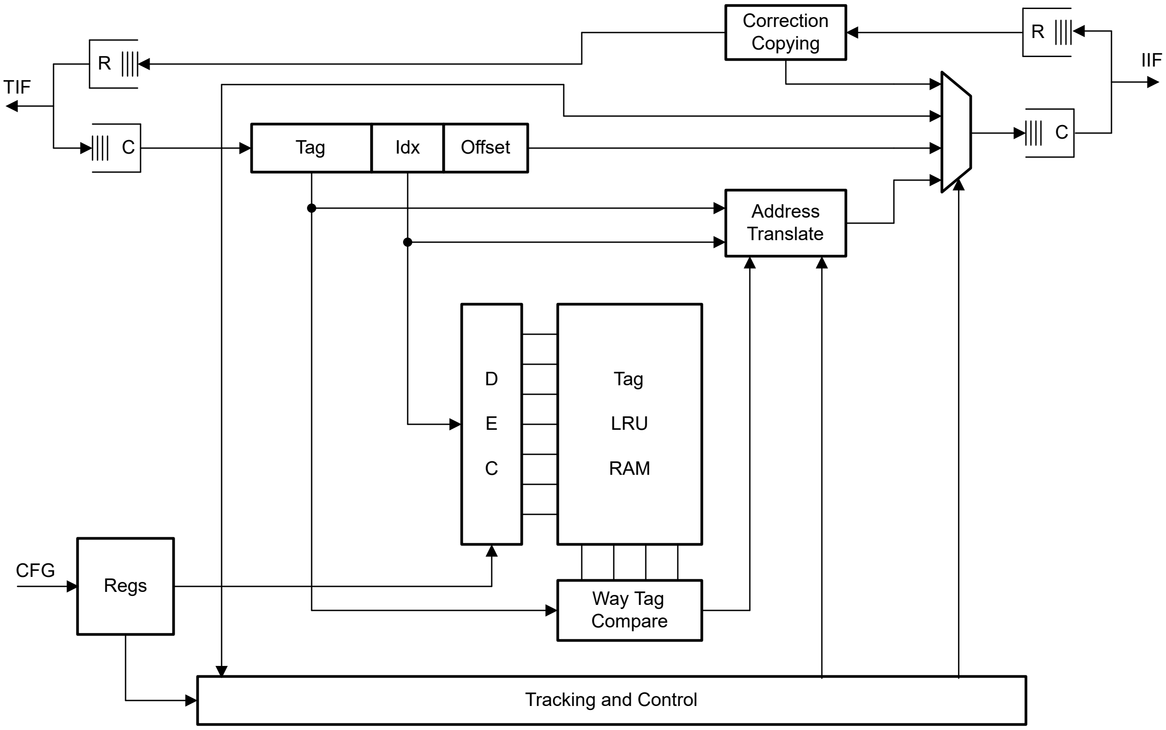


Figure 12-193. RL2 OptiFlash Block Diagram

12.4.4.1.3.1.1 C and R FIFO Blocks

The C and R FIFO blocks deal with the bus protocol to make sure the bus is retimed at the interface of the module

12.4.4.1.3.1.2 Correction and Copying Block

The Correction and Copying block are responsible for fixing the bus read alignment, ID back to meet the CBA requirements and also copies the data to be written to the remote cache data storage memory for RL2 cache data storage accesses.

12.4.4.1.3.1.3 Address Translation Block

The Address Translation block is responsible for remapping the CBA address for the RAT, FLC and RL2

For the RAT, the Address Translation Block it is purely an address translation.

For the FLC, the address is translated to the FLC remote SRAM when that address is within the FLC range and the data has previously been copied. Any access to the FLC remote SRAM uses the PIF security contest.

For RL2 of the request to the address of the remote cache data storage memory when a cache line hit is detected. The remote cache data storage memory address is referenced by *SET/WAY* so that a reduce *SET* selection can occur.

12.4.4.1.3.1.4 Tag LRU RAM Block

The tag LRU RAM within the RL2 holds the LRU states, *WAY* valid bits and the address tag for each *WAY* by the number of *SETs* for each cache line stored in the remote cache data storage memory

For each *WAY,* there are 3 bits for the LRU, a data valid bit, an address valid bit, and the 10 tag bits for address compare. In Dual mode, the two MS bits of the tag are used for the sub line valid bits. The format of the TAG RAM WAY in Dual Mode is 3 bits for the LRU, two data valid bits hi and lo, two address valid bits hi and lo, and the 8 tag bits

Based on the number of *SETs* in play, the tag is compared to the portion of the address just above the *SET* bits. The *SET* bits are normally the bits just above the address bits within the 32-byte burst. That is the *SET* bits are typically the address bits [n:5] where the address bits [4:0] are the byte address within the 32 byte burst. The width of the *SET* bits is controlled by the *rl2_regs_ctrl.size* register

Whatever the specified *rl2_regs_ctrl.size* register is programmed to; the tag gets compared to the bits just above the masked *SET* bits. This allows more memory to be cacheable when the *rl2_regs_ctrl.size* register specifies a greater amount of enabled cache

12.4.4.1.3.1.5 DEC Block

The DEC block decodes the incoming address for the *SET* selection, when using smaller L2 size configurations, the DEC block maskes out the bits so that a reduces *SET* that is used.

12.4.4.1.3.1.6 Regs Block

The Regs block stores the address ranges for L2 cache and well as the address ranges for remote cache data storage memory.

12.4.4.1.3.1.7 Way Tag Compare Block

The Way Tag Compare block determines which *'WAY'* the address was found within so that the address can be corrected accordingly.

12.4.4.1.3.1.8 Mux Block

The Mux block control which command is forwarded to the initiator interface.

12.4.4.1.3.1.9 Tracking and Control Block

The Tracking and Control block controls which addresses are Translated by the RAT, copied by the FLC or cached in the RL2 and manipulates the bus to save the data while returning the data to the original initiator.

12.4.4.1.3.2 Privilege Passing and Manipulation

The FLC passes the originating *secure, priv,* and *privid* from the original initiator on any command that is passed without address translation. All accesses to the FLC remote SRAM or accesses that copy the FLC range from the Flash carry the Privilege InterFace (PIF) *secure, priv,* and *privid* values. This allows the FLC remote data memory firewall to be able to determine who is the source of the operation and protect the FLC remote data memory from other initiators.

Note

Since FLC copy accesses to the Flash also use the PIF security context, the system must allow the PIF security context to access the FLC range in the Flash.

The RL2 passes the originating *secure, priv,* and *privid* from the original initiator on any command that is not modified due to L2 hit detection. When the remote cache data storage memory is written due to a read allocate or read due to an L2 hit; the Privilege InterFace (PIF) *secure, priv,* and *privid* values are used. This allows the remote cache data storage memory firewall to be able to determine who is the source of the operation and protect the cache data storage from other initiators.

12.4.4.1.3.3 Error Handling and Flushing

For all commands that are passed through, the return status is also passed through

For any read within cacheable range that is not currently cached, that meets RL2 allocation policy, and returns a read error, the following occurs:

- The error is passed through to the initiator
- The remote caceh data storage memory is written with the errant data.
- The cache line is marked invalid
- If not in Dual Mode or only a single cache line is allocated within the WAY, the WAY LRU is reverted and marked as the oldest WAY for future allocations

Any write to the cacheable range as defined by *L2_LO*i>=CachedRange<=*L2_HI* while the RL2 cache is enabled and operating, logically disables the RL2 cache and set the *wr_hit* error bit in the Interrupt Raw Status Register.

It is expected that the remote cache data storage memory area is protected using the ~PFI interface ~priv, *privid,* and *secure* parameters.

Any write to the remote cache data storage memory due to a read allocation that returns a write error, logically disables the RL2 cache and set the *wr_err* error bit in the Interrupt Raw Status Register.

The RL2_OF module gives out a single interrupt combining all the FLC/RL2 error/status events as follows:

1. FLC done: The FLC has completed the transfer to the FLC range. This is indicated by the *flc_don* bit in the Interrupt Raw Status Register.
2. FLC write error: A write error from FLC remote range (target memory) has occurred. This is indicated by the *flc_wrerr* bit in the Interrupt Raw Status Register and the FLC is logically disabled.
3. FLC read error: A read error on the data returned from FLC range has occurred. This is indicated by the *flc_rderr* bit in the Interrupt Raw Status Register and the FLC is logically disabled.
4. RL2 write hit: Any write to the RL2 cacheable range, while the RL2 cache is enabled and operating, has occurred potentially causing a coherency issue. This is indicated by the *wr_hit* bit in the Interrupt Raw Status Register and the RL2 is logically disabled.
5. RL2 write error: Any write to the remote cache data storage memory due to a read allocation (during cache miss) that returns a write error has occurred. This is indicated by the *wr_err* bit in the Interrupt Raw Status Register and the RL2 is logically disabled.

Any read or write error on the RAT translated memory range is pass through to the originator. Also, any read or write error on FLC ranges during the originator request is also pass through to the originator.

For any read within cacheable range that is not currently cached, that meets RL2 allocation policy, and returns a read error, the following occurs:

- The error is passed through to the initiator
- The remote cache data storage memory is written with the errant data.
- The cache line is marked invalid
- If not in Dual Mode or only a single cache line is allocated within the WAY, the WAY LRU is reverted and marked as the oldest WAY for future allocations

12.4.4.1.3.4 Tightly Coupled RL2 Tag Memory

The RL2 has Memory just outside the module for tag information that is *SETs* deep and *WAYs* times *WAY* info wide. This memory start auto initialization when a write to the *rl2_regs_ctrl.size* field occurs that changes the current size, or the rl2_regs_ctrl.enable bit is changed from a '0' to a '1' and all pending operations have completed. The RL2 performs any correctable ECC writeback in the event ECC is enables and a single error correct occurs. The memory is not used until the *rl2_regs_ctrl.size* field is written and the *enable bit is set.*

The tag memory auto initialization preloads the LRU info into each way of all the defined sets.

12.4.4.1.3.5 Remote Cache Data Storage Memory

The remote cache data storage memory stores the cache data managed by the RL2 module. This storage holds a number of 64 byte blocks as specified by the *rem*_len* registers. The remote cache data storage memory stores the 8 *WAYs* consecutively for each *SET* address. In Dual Mode each *WAY* has two 32 byte cache lines (64 bytes) versus other *l2_ctrl.size* values which only hold a single 32 byte cache line *WAY.* In dual Mode the *WAY* has a high and low sub cache line, the high is stored at the higher address and the low is stored at the *WAY* base.

Table 12-235. Remote Cache Data Storage Example

WAY N... WAY 0 - SET 0
WAY N... WAY 0 - SET 1
...
WAY N... WAY 0 - SET (M-1)
WAY N... WAY 0 - SET M

12.4.4.1.3.6 RL2 Cache Allocation

The RL2 does not modify the length of any transaction that the RL2 processes send to the slow memory it is intending to cache. As described earlier the RL2 allocation is based on full 32 byte read burst within the range of the specified target area. Once cached, any size or wrapping burst request to the same line can occur and can read the cached data. In the event that a allocated cache line returns an error on the read from the cacheable target, the allocation will restore the LRU aging such that the next allocated *WAY* is invalidated due to the target response error.

12.4.4.1.3.7 Dual Mode

The Dual Mode is an extension of the RL2 that supports two times that max remote cache data storage memory while keeping the tag RAM the same size. That is each way instead of representing a single cache line, represents two consecutive cache lines. This allows the remote cache data storage memory to be twice as large using the same tag RAM. When the *l2_ctrl.size* is set to 5 the dual mode is selected. In this mode there are the same number of cache line entries (4096), but the remote cache data storage memory is doubled. Each *WAY* now supports 64 bytes of cache data in two halves, a hi and lo sub cache line. This allows twice as much memory while keeping the same number of cache entries. When in this mode, the tag field is reduced by two bits to make room for the extra valid bits for the two sub lines held. This reduction reduces the cacheable range the RL2 can cache.

12.4.4.1.3.8 Emulation Debug

When the *EMUDBG* signal is set for a RAT transaction the region address translation occurs.

When the *EMUDBG* signal is set for a any transaction, the FLC pauses the copy function if copying until an non *EMUDBG* transaction is seen. This simulate what happens if user is single stepping the processor. The *dbgsusp* port also pauses the FLC without requiring a transaction. The FLC resumes after *dbgsusp* port goes back low.

When the *EMUDBG* signal is set for a RL2 transaction, the cache state is maintained. That is, *EMUDBG* request won't allocate a cache line in the case of a 'miss', or update the LRU state in the case of a 'hit'. But if the address is within the cache, the *EMUDBG* request gets the data from the remote cache data storage memory.

12.4.4.1.3.9 ASIL-D/SIL-3 Safety

The Automotive Safety Integrity Level (ASIL) or Safety Integrity Level (SIL) rating is determined by how OptiFlash is used in the SoC.

ASIL-D/SIL-3 can be obtained by duplicating the OptiFlash, supplying the same inputs to both copies, and comparing all the outputs for consistency (including RAM controls). If any output between the two copies do not match, an error has occurred. It is expected that both copies see the same external TAG memory contents. The RAM controls should be checked for consistency in this configuration.

There are cases that may require the safety version of the OptiFlash to be delayed by one cycle, so delaying all inputs to the safety copy and creating a delayed version of the outputs of the primary OptiFlash before comparing outputs.

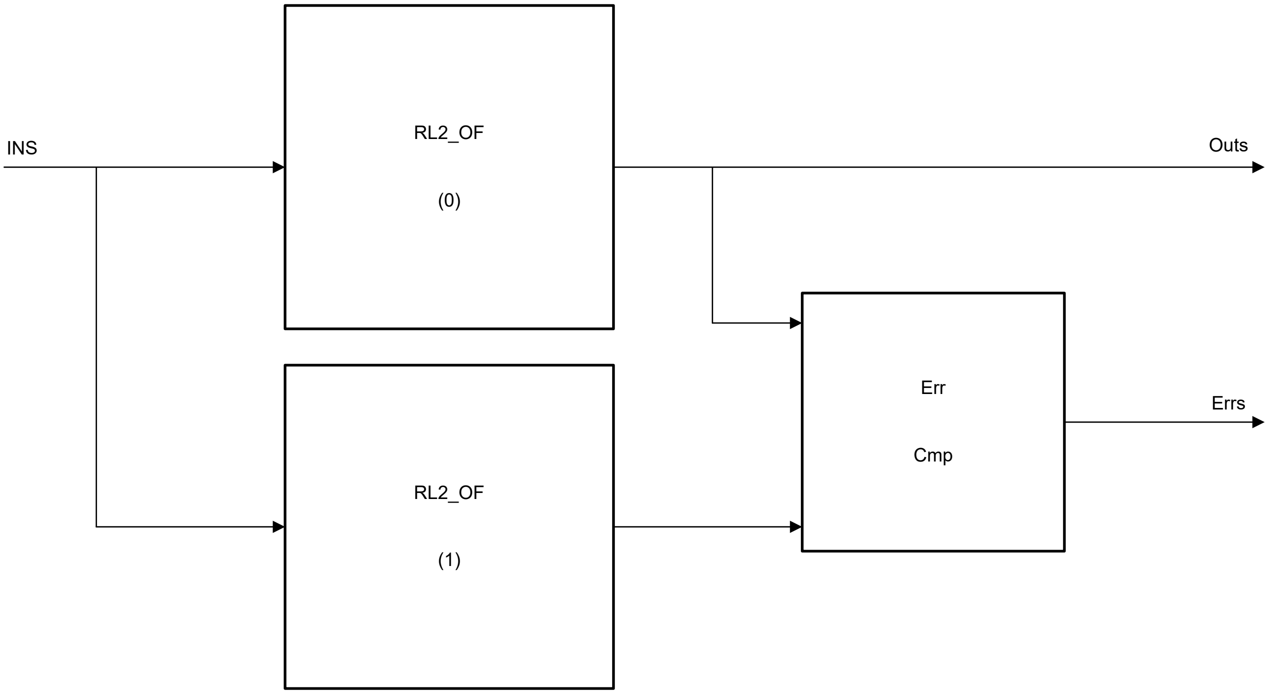


Figure 12-194. ASIL-D/SIL-3 Safety Implementation

Each R5F subsystem (R5FSS) in the device implements two instances of the RL2_OF modules that can run in lockstep. RL2 instances run in sync with the R5F CPU lockstep mode of operation, to detect faults that may result in unsafe operating conditions. The CCM-RL2_OF detects faults and signals them to the SOC error signaling module. Figure RL2_OF Lockstep Implementation shows the safety lockstep implementation of the RL2_OF modules.

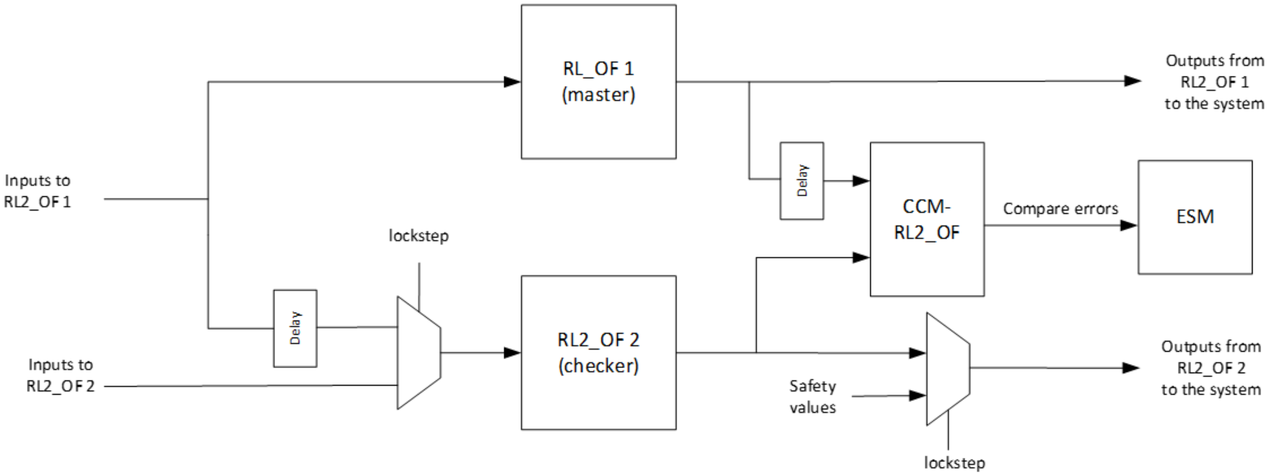


Figure 12-195. RL2_OF Lockstep Implementation

Input Handling:

Identical inputs are provided to both RL2_OF module copies CCM-RL2_OF compares all outputs from both copies, including:

1. Core bus outputs
2. RAM control signals

Error Detection:

CCMR compare error is triggered if outputs from the two copies mismatch

To prevent common mode failures:
1. *Primary RL2_OF:* Output signals are delayed by 2 cycles
2. *Checker RL2_OF:* Input signals are delayed by 2 cycles

During lockstep mode, outputs are clamped to inactive safe values

12.4.4.1.3.10 Latencies

OptiFlash was built with the ability for commands passing through to have 0 latency.

Commands that use the TAG memory have a 3-cycle delay to accommodate ram latencies and any ECC error correction from the RAM.

Commands are stalled when a write to RAM is done either through cache miss return or FLC copy is active.

12.4.4.1.3.11 Critical Word First (CWF)

Critical Word First is a CPU cache concept which states that although the CPU wishes to fetch a particular cache line, the CPU prefers to see an offset into the cache line prior to seeing the beginning of the cache line. This is also known as wrapping burst, where a burst request to a cache line is not aligned to the start of the cache line. For example, if the CPU jumps to the last word of a cache line not currently in the L1, the CPU requests a cache line burst, but the starting address of the burst is the last bus aligned word address. Say the cache line size is 32 bytes, and the bus width is 64 bits wide. If the CPU jumps to an address of 0x1c offset into a particular non-allocated cache line, the CPU requests address 0x18 in a wrapping burst of 32 bytes, resulting in offset addresses 0x18, 0x00, 0x08, 0x10 being the burst order requested. This is known as critical word first or wrapping burst request. That is the offset 0x18 is the critical word the CPU want to see in the cache line.

12.4.4.2 Fast Local Copy (FLC)

12.4.4.2.1 FLC Overview

The FLC allows a region of the slow memory like Flash to be dynamically copied to a section of system SRAM and at the same time run the code that was specified to be copied. The FLC redirects the request to the internal SRAM on the fly if the data has been transferred to the SRAM. Otherwise the request is sent to the slow device. This allow the SW to specify a piece of code to be resident in the system but executed out of the flash using internal system SRAM. The FLC ranges can start and end on any 4K Byte boundary. Care must be taken as to not create overlapping ranges. The minimum size of a FLC region is 4K Bytes.

The FLC does not modify any request for the CPU that is within a FLC range. This allows the critical word first (CWF) to be processed by the downstream module for best performance. A downstream CBA3-to-CBA4 bridge is suggested if it's required for a downstream CBA4 fabric be able to split any request that is a wrapping burst that is not aligned to the burst size boundary and targeting system SRAM.

Since the FLC is expected to copy data from a slow peripheral like a Flash device, the request is aligned to the burst boundary and the FLC restores the critical word first returned data to the CPU. FLC does not support split burst returns, all requested burst must be returned as a minimum of 8 byte burst return.

All FLC request are 32-byte or less, either wrapping burst or linear, but never cross a 32-byte aligned address. Any FLC request that crosses a 32-byte boundary is returned to the original address.

Since the copy of FLC range is independent from RAT ranges, the FLC copy function can be used to transfer the Flash data to the RAT target address. However, the FLC range access the target if it's already copied. So once copied, the FLC range must be disabled.

12.4.4.2.1.1 FLC Supported Features

- Supports 4 ranges that can be copied to a remote internal SRAM
- Ranges can start and finish on any 4KB boundary

12.4.5 Multi-Media Card Secure Digital (MMCSD) Interface

This section describes the MMCSD modules in the device.

12.4.5.1 MMCSD Overview

This device contains one or more MMCSD module instances. Each MMCSD instance includes one MMCSD Host Controller.

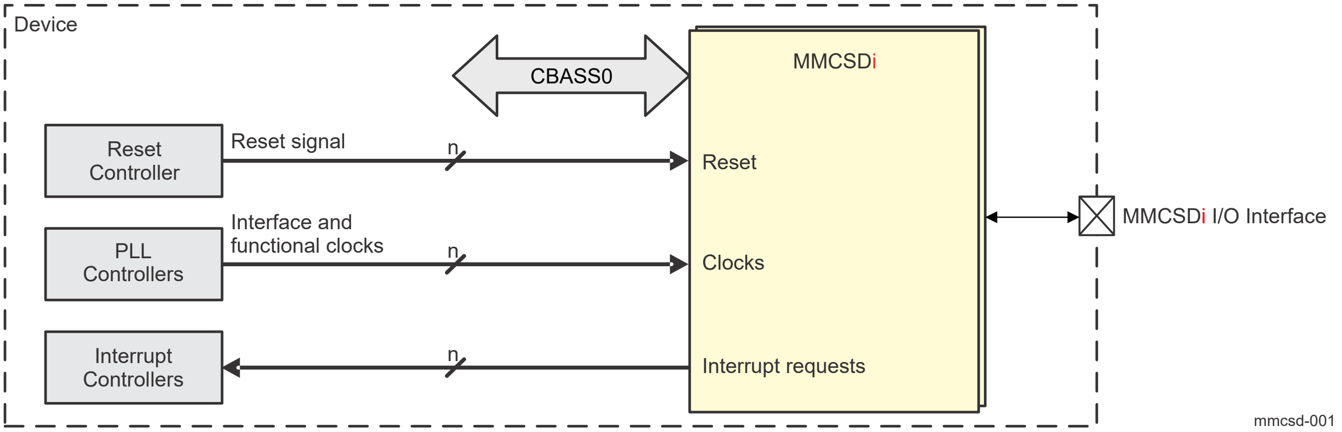
An instance supports either an 8-bit or 4-bit wide data bus.

A host controller can support eMMC and/or SD/SDIO. See the device specific datasheet for interfaces supported by the controller.

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded Multi-Media Card), SD 4.10 (Secure Digital), and SDIO 3.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

The MMCSD Host Controller provides accessibility to external MMC/SD/SDIO devices using a Programmed IO method or DMA data transfer method. In programmed IO method, the device CPU transfers data using the Buffer Data Port register (MMCSDi_DATA_PORT). In DMA data transfer method, the MMCSD Host Controller can read or write memory without device CPU intervention.

Figure 12-196 shows the MMCSDi module overview (where i represents a valid instance of MMCSD in a domain. Consult the device specific datasheet for available domains and instances).



A. i represents a valid instance of MMCSD in a domain.

Figure 12-196. MMCSDi Module Overview

12.4.5.1.1 MMCSD Features

Table 12-236. MMCSD Features

Feature		MMCSD0 (8-bit)	MMCSD1/2 (4-bit)
Muxing of other LVCMOS interfaces onto the MMCSD interface at the SoC level (See the device specific data sheet for supported interfaces, if applicable)		✓	✓
Controller			
Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3 (for more information about ADMA support, see Section 12.4.5.4.4, *Advanced DMA*)		✓	✓
System Bus Interface			
64-bit data width (host interface)		✓	✓
64-bit address		✓	✓
Clock asynchronous to eMMC/SD clock (MMCi_CLK)		✓	✓
Little endian only		✓	✓
Configuration Bus Interface			
32-bit data width (target interface)		✓	✓
Linear incrementing addressing mode		✓	✓
32-bit aligned accesses only		✓	✓
Little endian only		✓	✓
Multi-Media Card Support			
eMMC Electrical Standard 5.1 (JESD84-B51)		✓	✓
Backward compatible with earlier eMMC standards		✓	✓
Legacy MMC SDR	8-bit bus width, 0-25 MHz, 25 MBps	3.3/1.8v	N/A
	4-bit bus width, 0-25 MHz, 12.5 MBps		3.3/1.8v
	1-bit bus width, 0-25 MHz, 3.125 MBps		
High Speed SDR	8-bit bus width, 0-50 MHz, 50 MBps	3.3/1.8v	N/A
	4-bit bus width, 0-50 MHz, 25 MBps		3.3/1.8v
	1-bit bus width, 0-50 MHz, 6.25 MBps		
High Speed DDR	8-bit bus width, 0-50 MHz, 100 MBps	3.3/1.8v	N/A
	4-bit bus width, 0-50 MHz, 50 MBps		3.3/1.8v
HS200 SDR	0-200 MHz, 8-bit bus width, 200 MBps	1.8v	N/A
	0-200 MHz, 4-bit bus width, 100 MBps		1.8v
Secure Digital Card Support			
SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01		✓	✓
SDIO Specification v3.00		✓	✓
Backward compatible with earlier SD card specifications		✓	✓
Default Speed mode	3.3 V signaling, frequency up to 25 MHz, up to 12.5 MBps	✓	✓
High Speed mode	3.3 V signaling, frequency up to 50 MHz, up to 25 MBps	✓	✓
SDR12	UHS-I 1.8 V signaling, frequency up to 25 MHz, up to 12.5 MBps	✓	✓
SDR25	UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 25 MBps	✓	✓
SDR50	UHS-I 1.8 V signaling, frequency up to 100 MHz, up to 50 MBps		✓
DDR50	UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 50 MBps		✓
SDR104	UHS-I 1.8 V signaling, frequency up to 200 MHz, up to 100 MBps		✓

12.4.5.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

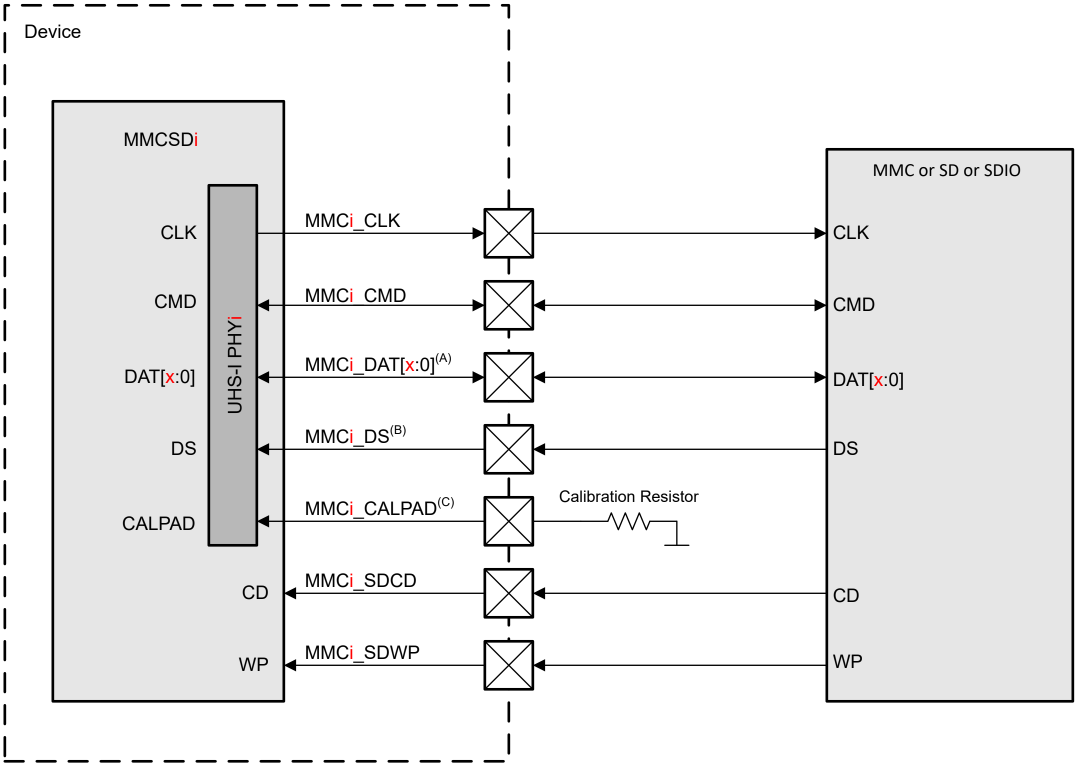
12.4.5.2 MMCSD Environment

The MMCSD instance is hereinafter referred to as MMCSDi module.

This section describes the MMCSDi external connections (environment).

The MMCSD (see the device specific datasheet for supported instances) can be used for connection to 1, 4, or 8-bit devices (dedicated for connection to eMMC devices). The MMCSD (see the device specific datasheet for supported instances) can be used for connection to 1 or 4-bit devices (dedicated for connection to SD or SDIO devices). For each MMCSD an integrated UHS-I PHY provides interface to external device.

Figure 12-197 shows the MMCSDi (where i represents a valid instance of MMCSD in a domain. See the device specific datasheet for available domains and MMCSD instances) connected to MMC, SD, or SDIO device.



A. x=7 for MMCSD (8-bit wide data bus); x=3 for MMCSD (4-bit wide data bus)

B. Used for HS400 mode (See the device specific datasheet for valid instances)

C. Used for PHY Calibration Resistor (See the device specific datasheet for valid instances)

Figure 12-197. MMCSDi Connected to MMC, SD, or SDIO Device

Table 12-237 describes the MMCSDi I/O signals.

Table 12-237. MMCSDi I/O Signals

Module Pin(4)	Device Level Signal	I/O(1)	Description
	MMCSDi(3)		
CLK	MMCi(3)_CLK	O	External Clock
CMD	MMCi(3)_CMD	I/O	Command Line
DAT[x:0](5)	MMCi(3)_DAT[x:0]	I/O	Data Signals
DS	MMCi(3)_DS	I	Data Strobe
CALPAD	MMCi(3)_CALPAD(2)	A	PHY Calibration Resistor
WP	MMCi(3)_SDWP	I	SD Card Write Protect
CD	MMCi(3)_SDCD	I	SD Card Detect

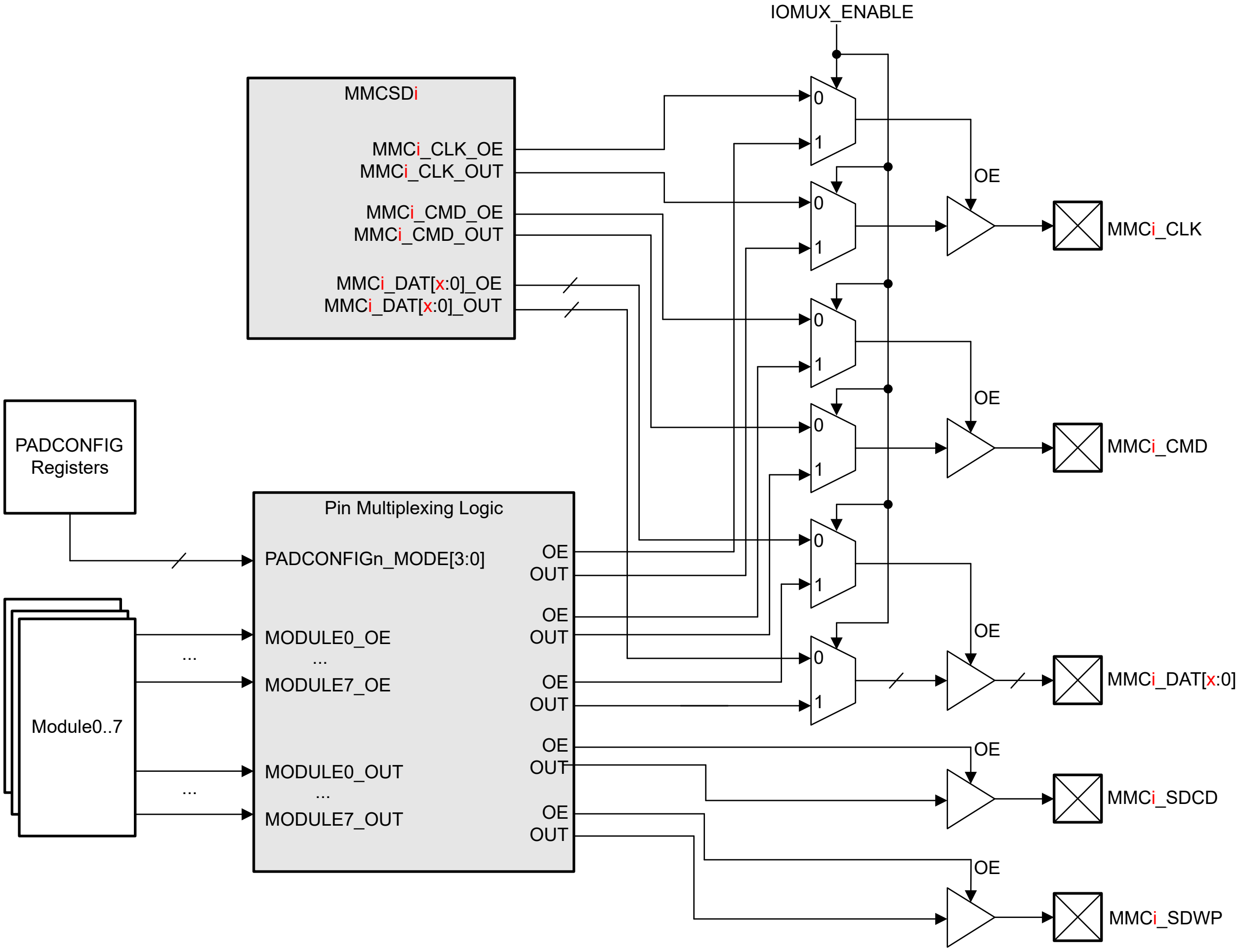
(1) I = Input; O = Output; HiZ = High Impedance; A = Analog
(2) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
(3) i represents an MMC instance. See the device datasheet for available domains and MMC instances.
(4) Some pins may not be pinned out or relevant to this device. See the device datasheet for specifics.
(5) x=7 for MMCSD (8-bit wide data bus); x=3 for MMCSD (4-bit wide data bus)

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), refer to the device-specific Datasheet.

12.4.5.2.1 MMCSD IO Multiplexer

Figure 12-198 describes the IOMUX_ENABLE multilplexer, which is controlled by the MMC_SSCFG_PHY_CTRL_1_REG[31] IOMUX_ENABLE bit.



A. i represents a valid instance of MMCSD. See the device data sheet for specifics.

B. x=7 for MMCSD (8-bit wide data bus); x=3 for MMCSD (4-bit wide data bus)

C. Only MMCi_CLK, MMCi_CMD and MMCi_DAT[n:0] are routed through the IOMUX_ENABLE multiplexer. MMCi_SDCD and MMCi_SDWP are not routed through the IOMUX_ENABLE multiplexer.

D. The IOMUX_ENABLE multiplexer does not affect the signal functions selected from the respective PADCONFIG register for the MMCi_SDCD or MMCi_SDWP pins.

Figure 12-198. MMCSD IOMUX_ENABLE Multiplexer

12.4.5.2.2 Protocol and Data Format

The bus protocol between the MMCSD Host Controller and the card is message-based. Each message is represented by one of the following parts:

- Command: A command starts an operation. The command is transferred serially from the MMCSD Host Controller to the card on the CMD line.
- Response: A response is an answer to a command. The response is sent from the card to the MMCSD Host Controller. It is transferred serially on the CMD line.
- Data: Data are transferred from the MMCSD Host Controller to the card or from the card to the MMCSD Host Controller using the data lines.
- Busy: The DAT[0] signal is maintained low by the card as far as it is programming the data received.
- CRC status: The CRC result is sent by the card through the DAT[0] line when executing a write transfer. In the case of transmission error, occurring on any of the active data lines, the card sends a negative CRC status on DAT[0]. In the case of successful transmission, over all active data lines, the card sends a positive CRC status on DAT[0] and starts the data programming procedure.

12.4.5.2.2.1 Protocol

There are two types of data transfer:

- Sequential operation
- Block-oriented operation

There are specific commands for each type of operation (sequential or block-oriented).

For information about commands and programming sequences supported by the MMC, SD, and SDIO devices, see the *Multi-Media Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification (Part E1)*.

Figure 12-199 and Figure 12-200 show how sequential operations are defined. Sequential operation is only for 1-bit transfer and initiates a continuous data stream. The transfer terminates when a stop command follows on the CMD line.

Note

Stream commands are supported only by MMCs.

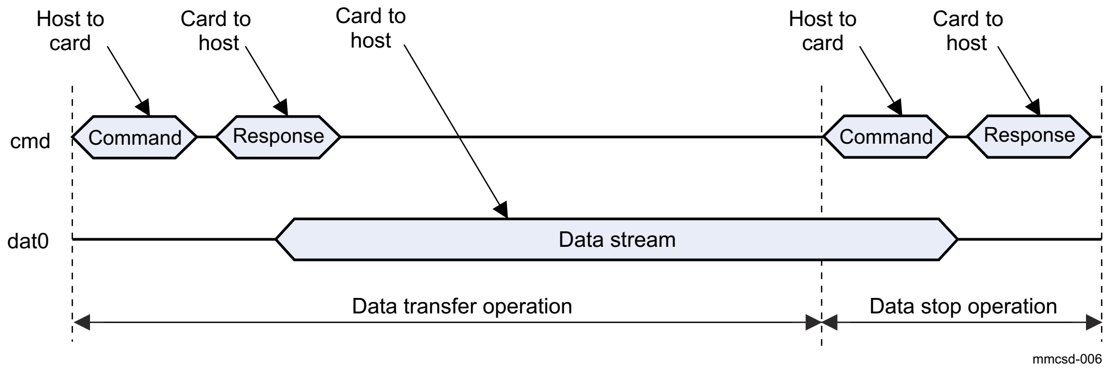


Figure 12-199. Sequential Read Operation (MMCs Only)

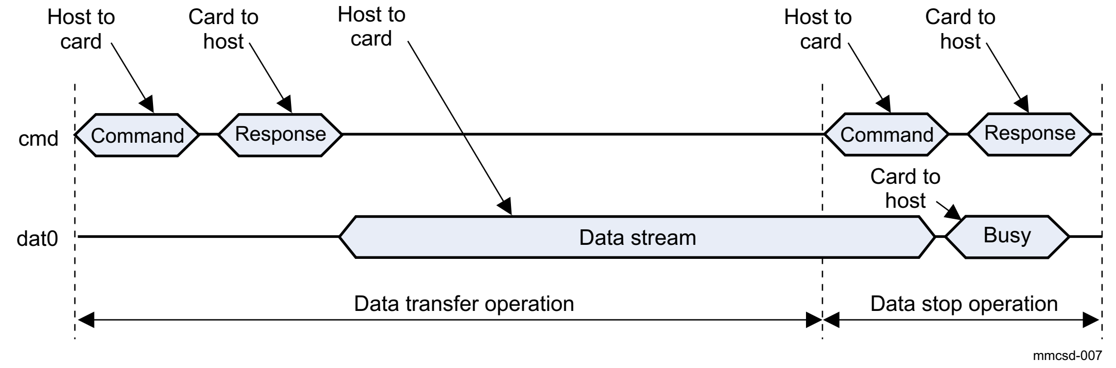


Figure 12-200. Sequential Write Operation (MMCs Only)

Figure 12-201 and Figure 12-202 show how multiple block-oriented operations are defined. A multiple block-oriented operation sends a data block plus CRC bits. The transfer terminates when a stop command follows on the CMD line. These operations are available for all kinds of devices (MMC, SD, SDIO).

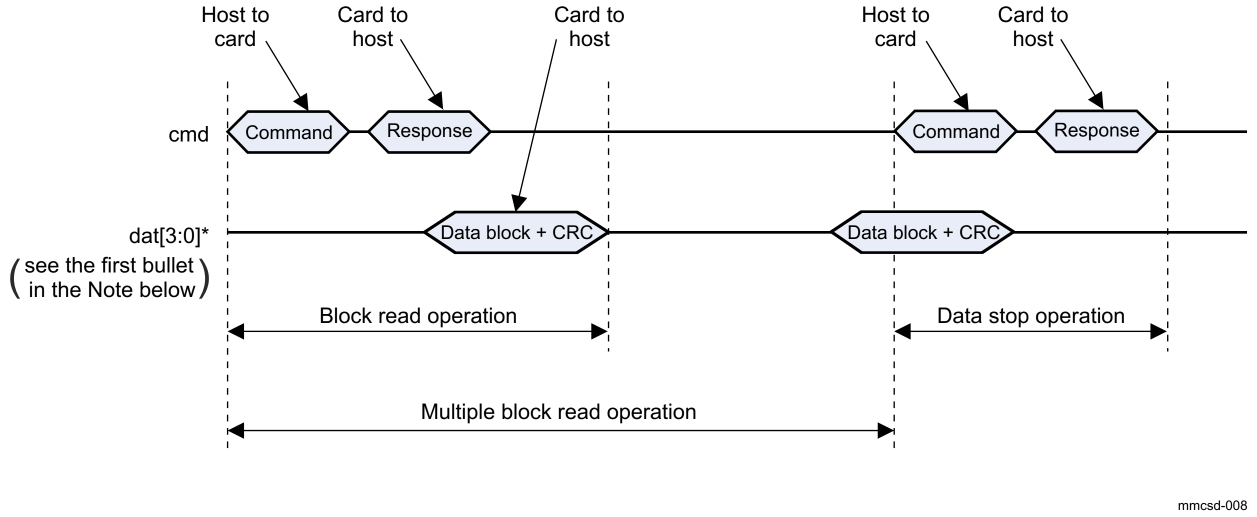


Figure 12-201. Multiple Block Read Operation

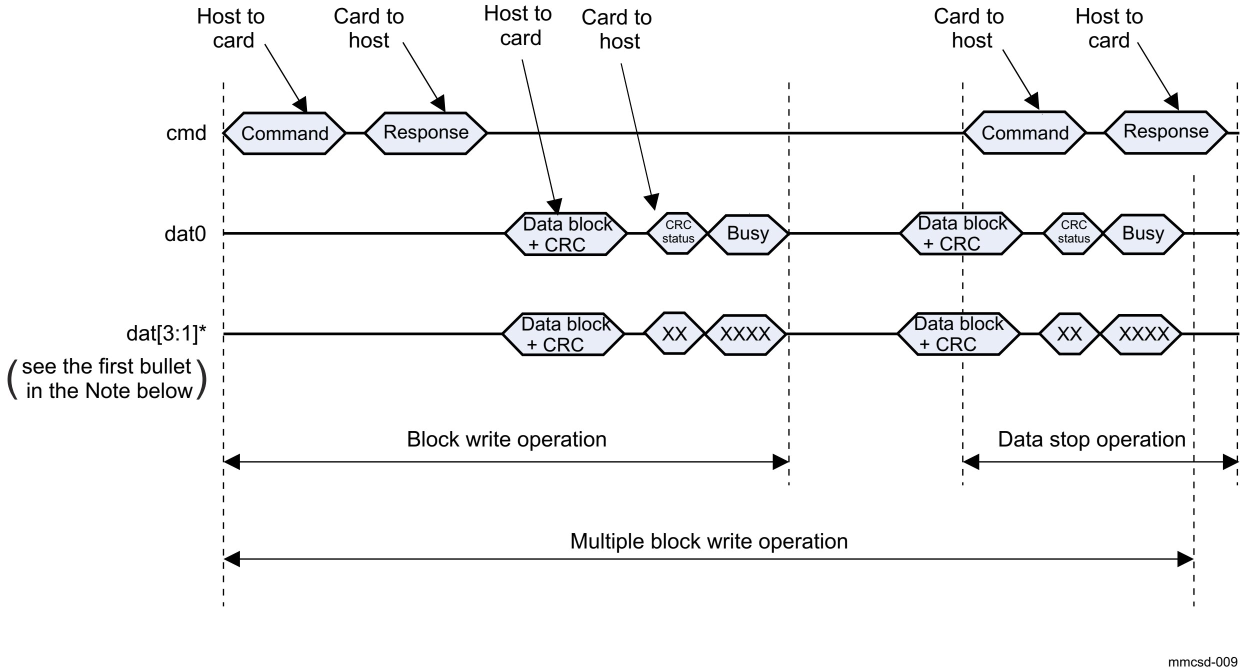


Figure 12-202. Multiple Block Write Operation With Card Busy Signal

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Note

- The card busy signal is not always generated by the card. Refer to Figure 12-201 and Figure 12-202, that show a particular case.
- Software must perform a software reset (see MMCSD0_SOFTWARE_RESET / MMCSD1_SOFTWARE_RESET register) after a data time-out to ensure that MMCi_CLK is stopped.
- For multiblock transfer, and especially for MMC devices, a transfer can be aborted without using a stop command. If a CMD23 is used before data transfer to define the number of blocks that will be transferred, then the transfer stops automatically after the last block (if the MMCs supports this feature).

12.4.5.2.2.2 Data Format

12.4.5.2.2.2.1 Coding Scheme for Command Token

Command tokens always start with 0 and end with 1. The second bit is a transmitter bit: 1 for a host command. The content is the command index (coded by 6 bits) and an argument (for example, an address), coded by 32 bits. The content is protected by 7-bit CRC checksum (see Figure 12-203).

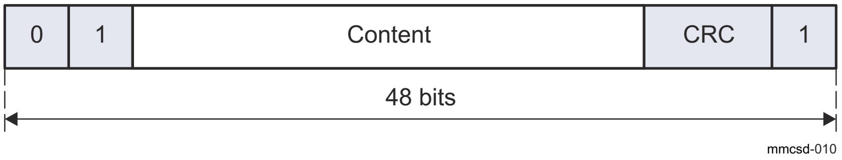


Figure 12-203. Command Token Format

12.4.5.2.2.2.2 Coding Scheme for Response Token

Response tokens always start with 0 and end with 1. The second bit is a transmitter bit: 0 for a card response. The content is different for each type of response (R1, R2, R3, R4, and R5, R6, R7 [for SD]) and the content is protected by 7-bit CRC checksum (see Figure 12-204 and Figure 12-205). Depending on the type of commands sent to the card, the MMCSD0_COMMAND / MMCSD1_COMMAND register must be configured differently to avoid false CRC or index errors to be flagged on command response (see Table 12-238). For more information about response types, see the *Multi-Media Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification (Part E1)*.

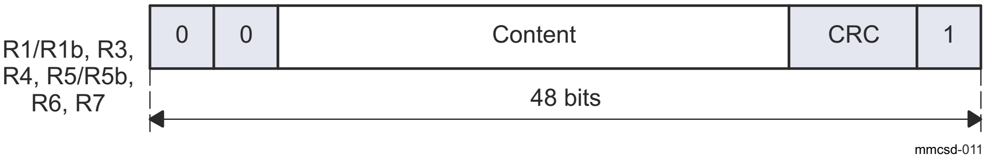


Figure 12-204. Response Token Format (R1/R1b, R3, R4, R5/R5b, R6, R7)

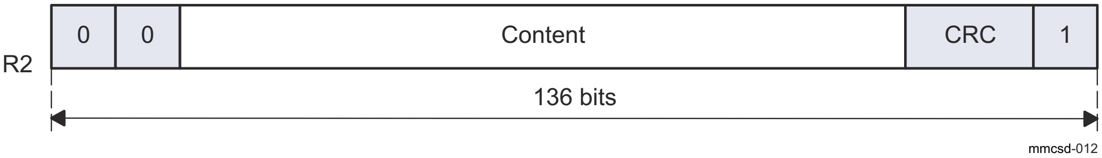


Figure 12-205. Response Token Format (R2)

Table 12-238. Relationship Between Configuration and Name of Response Type

Response Type MMCSD0_COMMAND[1-0] RESP_TYPE_SEL / MMCSD1_COMMAND[1-0] RESP_TYPE_SEL	Index Check Enable MMCSD0_COMMAND[4] CMD_INDEX_CHK_ENA / MMCSD1_COMMAND[4] CMD_INDEX_CHK_ENA	CRC Check Enable MMCSD0_COMMAND[3] CMD_CRC_CHK_ENA / MMCSD1_COMMAND[3] CMD_CRC_CHK_ENA	Name of Response Type
00	0	0	No response
01	0	1	R2
10	0	0	R3 (R4 for SD cards)
10	1	1	R1, R6, R5, (R7 for SD cards)
11	1	1	R1b, R5b

12.4.5.2.2.2.3 Coding Scheme for Data Token

Data tokens always start with 0 and end with 1 (see Figure 12-206 through Figure 12-208).

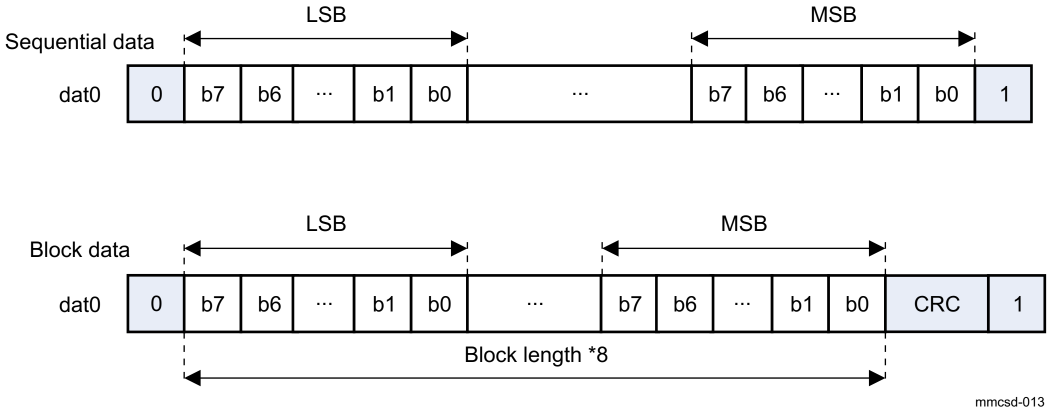


Figure 12-206. Data Token Format for 1-Bit Transfers

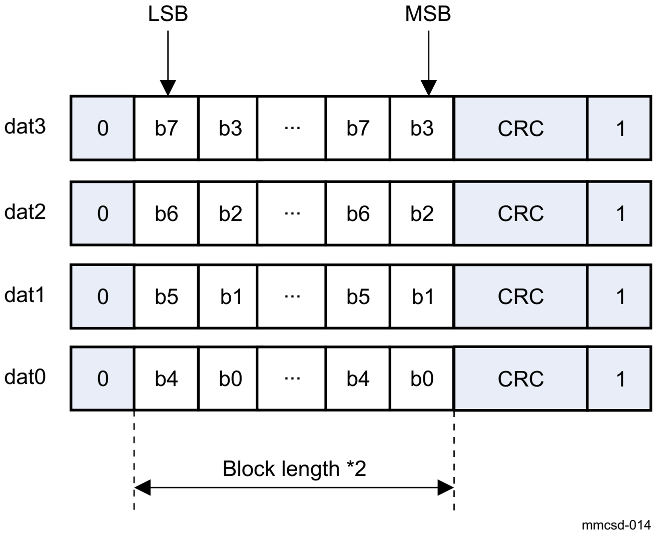


Figure 12-207. Data Token Format for 4-Bit Transfers

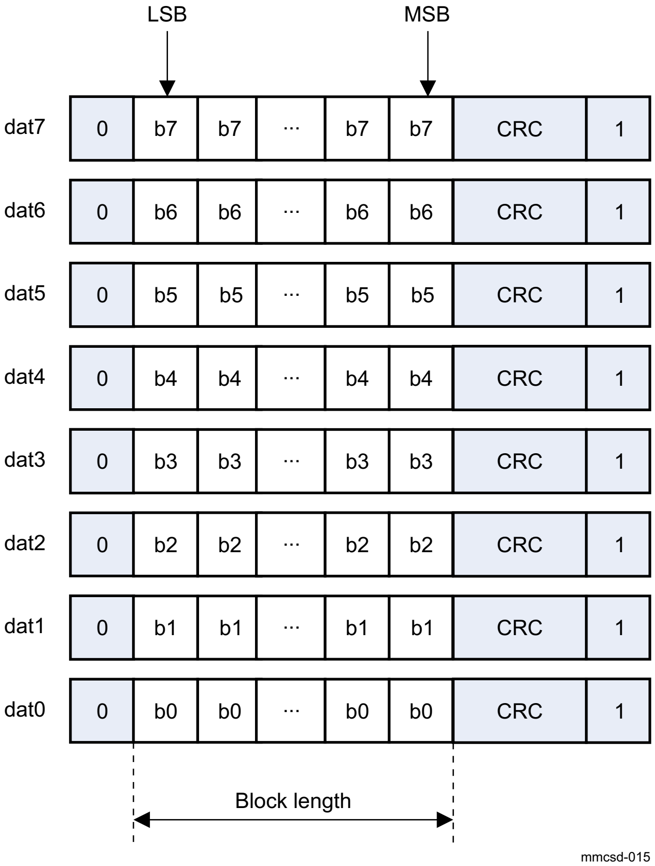


Figure 12-208. Data Token Format for 8-Bit Transfers

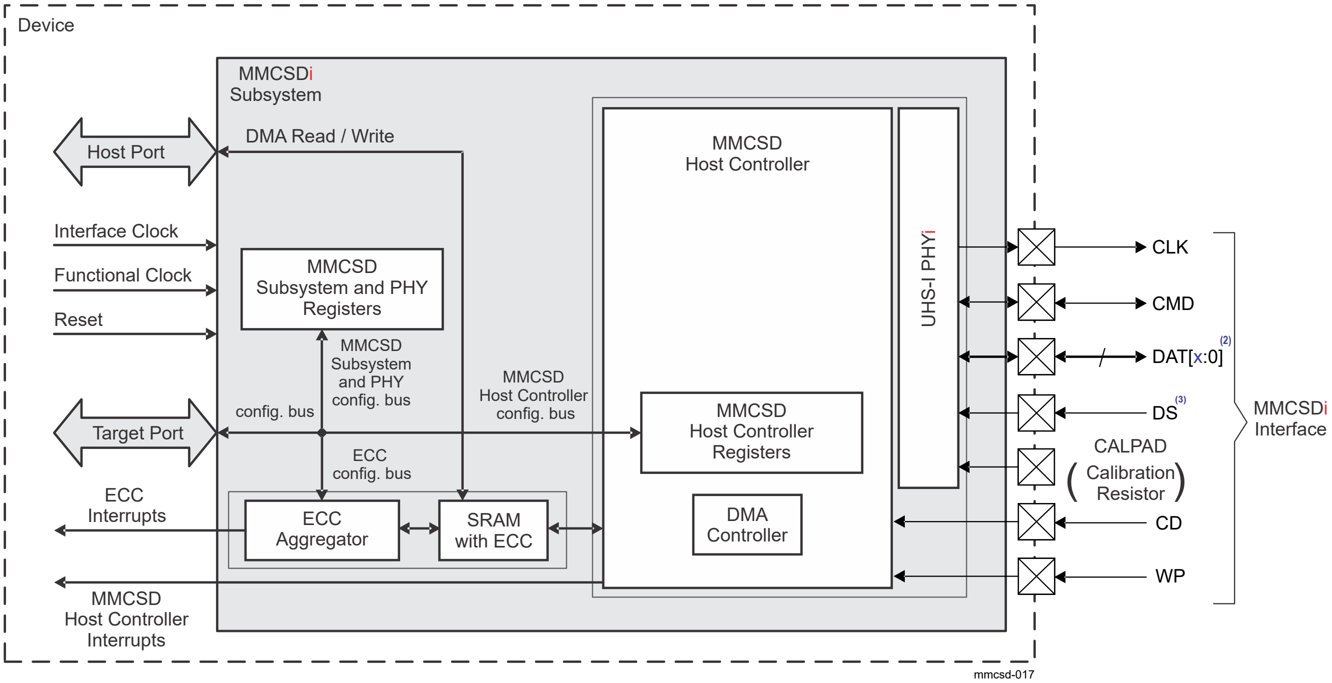
12.4.5.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.4.5.4 MMCSD Functional Description

12.4.5.4.1 Block Diagram

Figure 12-209 shows the MMCSDi module block diagram (where i represents a valid instance of MMCSD in a domain).



A. (1) i represents a valid instance of MMCSD in a domain. Consult the device specific datasheet for available domains and MMCSD instances.

B. (2) x = the maximum number of available DAT signals for an instance of MMCSD in a domain.

C. (3) Used for HS200 mode (Consult the datasheet for supported devices).

Figure 12-209. MMCSDi Module Block Diagram

Basic Blocks:

- MMCSD Host Controller: The MMCSD Host Controller is situated in the MMCSD Subsystem and provides accessibility to external MMC/SD/SDIO devices using a Programmed IO method or DMA data transfer method.
- UHS-I PHY: The integrated UHS-I PHY provides an interface between the MMCSD Host Controller and external MMC/SD/SDIO devices.
- MMCSDi Interface: The MMCSDi Interface includes all used interface pins (for more information, see Table 12-237).
- Host Port: Provides a 64-bit wide read/write interface between the device and the MMCSD Subsystem internal SRAM.
- Target Port: Provides a 32-bit wide interface between the device and the MMCSD Subsystem and MMCSD Host Controller parts.
- MMCSD Host Controller Registers: This block includes set of all MMCSD Host Controller registers.
- MMCSD Subsystem and PHY Registers: This block implements memory-mapped registers at the MMCSD Subsystem level and memory-mapped registers to control and program the MMCSD PHY.
- ECC Aggregator: The ECC Aggregator block facilitates aggregating and reporting internal SRAM ECC errors (for more information, see *ECC Support*).
- Internal SRAM with ECC: The internal SRAM block is used for data storage during read/write transactions.
- DMA Controller: Manages the data transfer between the device memory and the MMCSD Subsystem internal SRAM.
- System Clocks: There are asynchronous relationship between the interface (system) clock and functional clock (for more information, see *MMCSD Clocks*).
- System Reset: The reset to the MMCSD Subsystem provides reset to the all MMCSD Subsystem parts (for more information, see *MMCSD Clocks*).
- Interrupts: The MMCSD Subsystem sources one MMCSD Host Controller interrupt and four ECC Aggregator interrupts (for more information, see *MMCSD Hardware Requests* and *Interrupt Requests*).

For more information about all MMCSD registers, see *MMCSD Registers*.

The MMCSD Host Controller can use a Programmed IO method (PIO) or DMA data transfer method to access external MMC/SD/SDIO devices.

The target port is used for device CPU access to the MMCSD Host Controller register set. The MMCSD Host Controller register set provides the communication between the device CPU and the MMCSD Host Controller. In PIO method the device CPU transfers data using the MMCSD0_DATA_PORT / MMCSD1_DATA_PORT register. The data flow from the device memory to the external MMC/SD/SDIO device (and vice versa) is through the target port, the MMCSD0_DATA_PORT / MMCSD1_DATA_PORT register in the MMCSD Host Controller, and the PHY.

The host port is used for connection to the DMA controller (for more information about ADMA support, see *Advanced DMA* and MMCSD0_CAPABILITIES / MMCSD1_CAPABILITIES register). In DMA data transfer method the DMA controller uses the host port to transfer data between the device memory and the MMCSD Subsystem internal SRAM. The other side of the internal SRAM is connected to the MMCSD Host Controller. The data flow from the device memory to the external MMC/SD/SDIO device (and vice versa) is through the host port, internal SRAM, MMCSD Host Controller, and the PHY. The DMA controller manages the read/write operations from/to the internal SRAM without device CPU intervention.

12.4.5.4.2 Interrupt Requests

Each MMCSD instance sources one active high level MMCSD Host Controller interrupt and four active high level ECC Aggregator interrupts (see *Module Integration*). The MMCSD Host Controller interrupt is generated based on the bit values in the MMCSD0_NORMAL_INTR_STS / MMCSD1_NORMAL_INTR_STS and MMCSD0_NORMAL_INTR_STS_ENA / MMCSD1_NORMAL_INTR_STS_ENA registers. The ECC Aggregator interrupts are generated based on the ECC errors - single and double bit errors (for more information about ECC Aggregator interrupts, see *ECC Support*).

12.4.5.4.3 ECC Support

The Error Correcting Code (ECC) is a mechanism for providing increased system reliability via reduction of memory software errors by allowing single bit errors to be detected and corrected (SEC) and double bit errors to be detected (DED).

There are two SRAM memories (transmit SRAM and receive SRAM) within each MMCSD instance. These two memories are ECC protected.

The SEC logic detects and corrects a single bit error (single bit error per ECC word or per ECC data segment). The DED logic only detects (does not correct) double errors (double bit errors per ECC word or per ECC data segment).

12.4.5.4.3.1 ECC Aggregator

There are two SRAMs (each with size 4 KB - 512 words × 64-bit) in each MMCSD Subsystem. One SRAM dedicated for transmit and one SRAM dedicated for receive operations.

Figure 12-210 shows the ECC Aggregator block diagram.

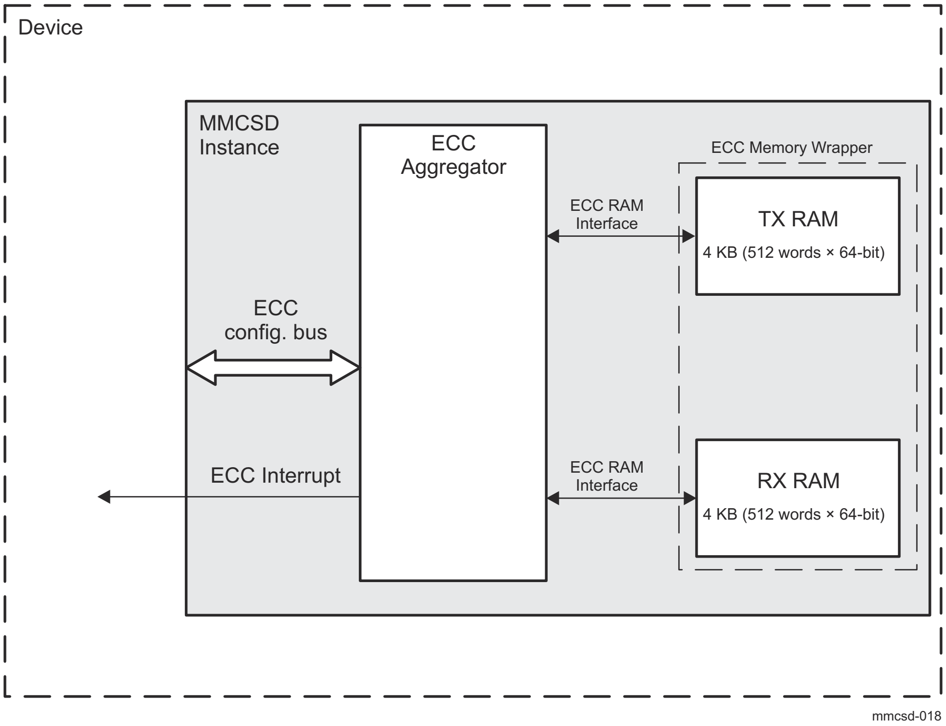


Figure 12-210. ECC Aggregator Block Diagram

Note

For more information about ECC Aggregator Registers, refer to *MMCSD Registers*.

12.4.5.4.4 Advanced DMA

The MMCSD modules support SD Advanced DMA – ADMA2 and ADMA3.

Note

For more information, refer to the SD Association specification titled *"SD Host Controller Simplified Specification, Part A2, Version 4.10"*.

12.4.5.5 MMCSD Programming Guide

12.4.5.5.1 Sequences

This section defines basic sequence flow chart divided into several sub sequences.

Note

UHSII is not supported. For more information, see *Not Supported Features*.

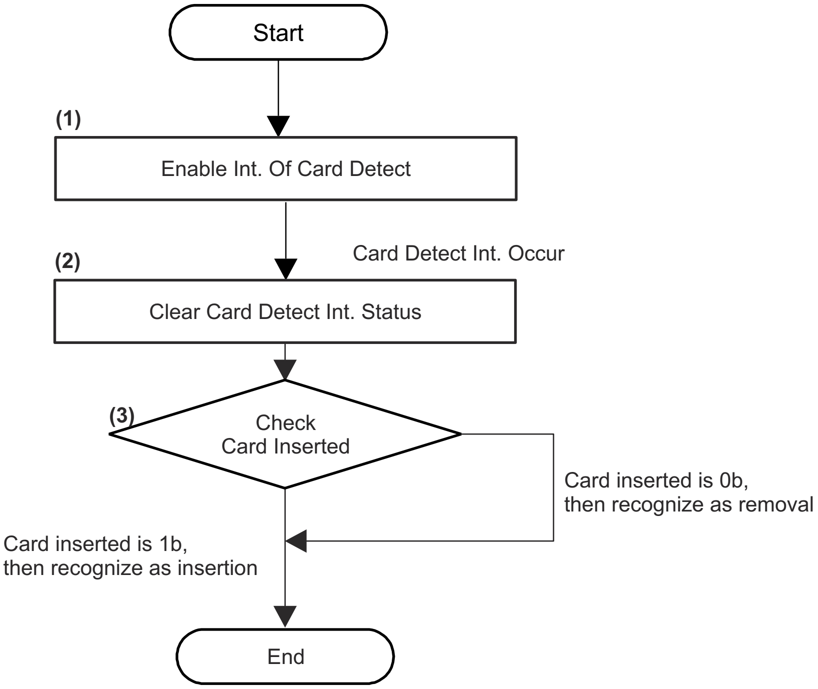
"Wait for interrupts" is used in the flow chart. This means the Host Driver waits until specified interrupts are asserted. If already asserted, then fall through that step in the flow chart. Timeout checking shall be always required to detect no interrupt generated but this is not described in the flow chart.

This specification uses the double box like Figure 12-211, (the step (1) in Figure 12-215), it means that the other flows, which already are shown, shall be performed. Therefore, the interrupt may be included in the other flows.

mmcsd-019

Figure 12-211. Double Box Notation

12.4.5.5.1.1 SD Card Detection



mmcsd-020

Figure 12-212. SD Card Detect Sequence

The flow chart for detecting a SD card is shown in Figure 12-212.

Each step is executed as follows:

To enable interrupt for card detection, write 1 to the following bits:

- MMCSD0_NORMAL_INTR_STS_ENA[6] CARD_INSERTION
- MMCSD0_NORMAL_INTR_SIG_ENA[6] CARD_INSERTION
- MMCSD0_NORMAL_INTR_STS_ENA[7] CARD_REMOVAL
- MMCSD0_NORMAL_INTR_SIG_ENA[7] CARD_REMOVAL

(1) When the Host Driver detects the card insertion or removal, clear its interrupt statuses. If Card Insertion interrupt is generated, write 1 to MMCSD0_NORMAL_INTR_STS_ENA[6] CARD_INSERTION bit. If Card Removal interrupt is generated, write 1 to MMCSD0_NORMAL_INTR_STS_ENA[7] CARD_REMOVAL bit.

(2) Check MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit. In the case where MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit is 1, the Host Driver can supply the power and the clock to the SD card. In the case where MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit is 0, the other executing processes of the Host Driver shall be immediately closed.

If miniSD adaptor is used for standard SD slot and miniSD card is inserted or extracted from the adaptor, card detect interrupt may not be generated. When host does not receive response to any commands, miniSD card is extracted or in idle state, the host should try to re-initialize the card. In this case, all card information shall be re-loaded.

12.4.5.5.1.2 SD Clock Control

12.4.5.5.1.2.1 Internal Clock Setup Sequence

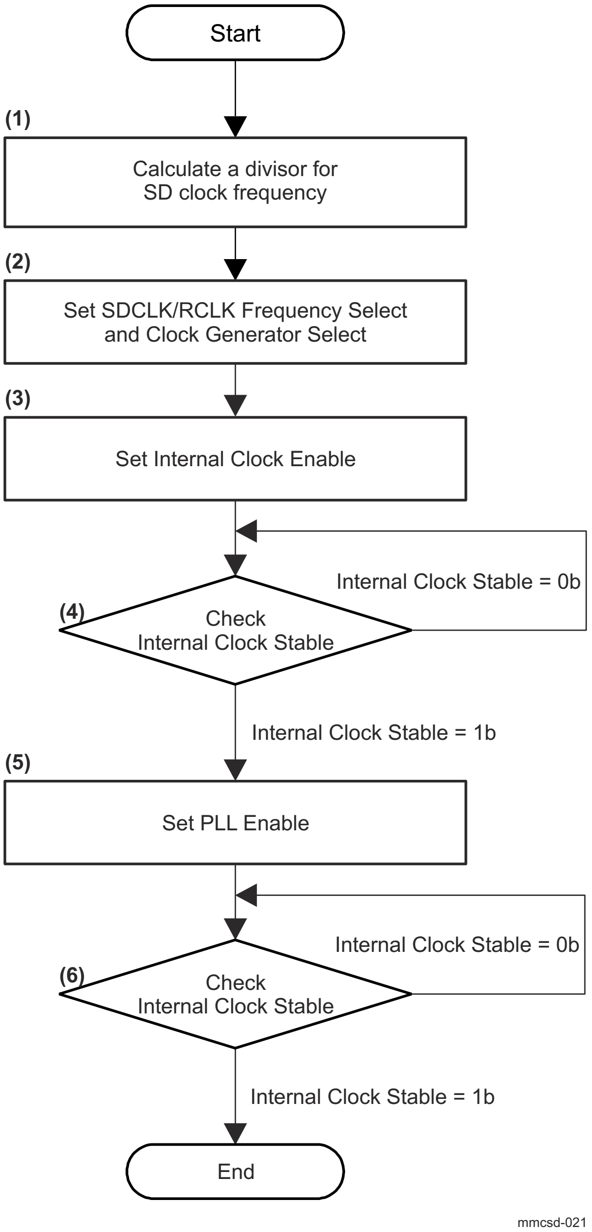


Figure 12-213. Internal Clock Setup Sequence

The sequence for supplying SD Clock to a SD card is described in Figure 12-213. From Version 4.10, MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is added. This sequence is also applicable to prior versions which do not support MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit.

(1) Calculate a divisor to determine SD Clock frequency for legacy IF or RCLK frequency for UHS-II IF by reading MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ and MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit fields. If non-zero value is set to MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field, Programmable Clock Mode can be used (for more information, see MMCSD0_CLOCK_CONTROL[5] CLKGEN_SEL bit). If MMCSD0_CAPABILITIES[15-8] BASE_CLK_FREQ bit field is 00 0000b, the Host System shall provide this information to the Host Driver by another method.

(2) Set MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field and MMCSD0_CLOCK_CONTROL[5] CLKGEN_SEL bit in accordance with the calculated result of step (1).

If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set, these bits are set by Host Controller automatically as specified in the Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10).

(3) Set MMCSD0_CLOCK_CONTROL[0] INT_CLK_ENA bit.

(4) Check MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE bit. Repeat this step until this status is 1. Clock will be stable in shorter time but timeout of this loop is defined as 150 ms.

(5) Set MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit. This step does not affect Host Controllers which do not support MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit.

(6) If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is supported, PLL locked may be checked by this status (if MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this status is supposed to indicate 1 by step (3)). Clock will be stable in shorter time but timeout of this loop is defined as 150 ms.

12.4.5.5.1.2.2 SD Clock Supply and Stop Sequence

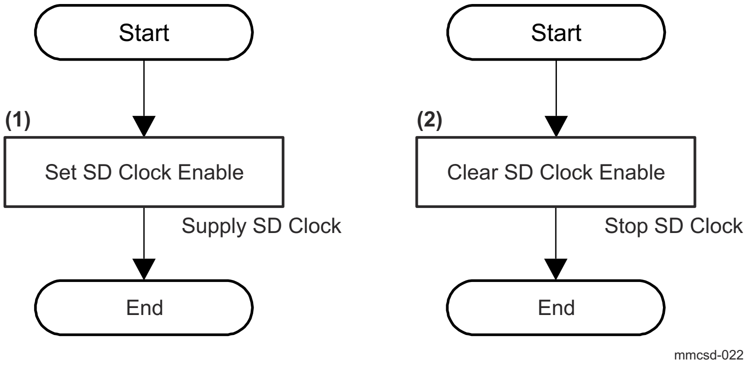


Figure 12-214. SD Clock Supply and Stop Sequence

The flow chart for stopping the SD Clock is shown in Figure 12-214. The Host Driver shall not stop the SD Clock when a SD transaction is occurring on the SD Bus -- namely, when either MMCSD0_PRESENTSTATE[1] INHIBIT_DAT or MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is set to 1.

(1) Setup Internal Clock (see Figure 12-213). Then set MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit to 1. Then, the Host Controller starts supplying the SD Clock.

(2) Set MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit to 0. Then, the Host Controller stops supplying the SD Clock. Internal Clock is still oscillating.

12.4.5.5.1.2.3 SD Clock Frequency Change Sequence

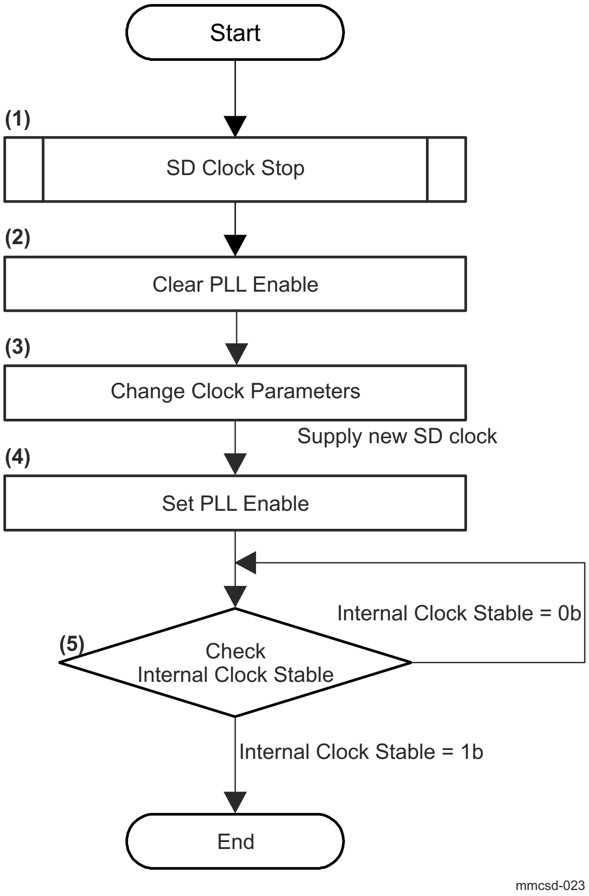


Figure 12-215. SD Clock Change Sequence

The sequence for changing SD Clock frequency is shown in Figure 12-215.

(1) Execute the SD Clock Stop Sequence (see Figure 12-214). If SD Clock supply to card is already stopped, skip this step.

(2) Clear MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit to 0. If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this step has no effect and may be skipped.

(3) When MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 0, change clock parameters in the MMCSD0_CLOCK_CONTROL register. When MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1, select Bus Speed Mode as described.

(4) Set MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit to 1. If MMCSD0_CLOCK_CONTROL[3] PLL_ENA bit is not supported, this step this step has no effect and may be skipped.

(5) Wait until MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE bit is set to 1. Clock will be stable in shorter time but timeout of this loop is defined as 150 ms. SD Clock Supply Sequence is required to provide clock to device (see Figure 12-214).

12.4.5.5.1.3 SD Bus Power Control

The sequence for controlling the SD Bus Power is described in Figure 12-216.

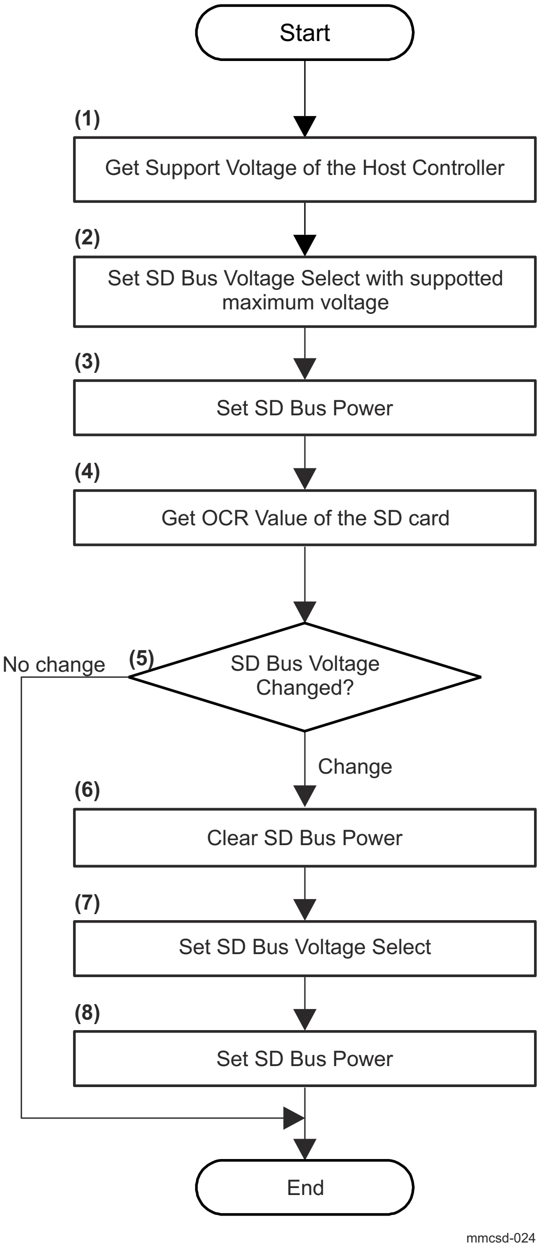


Figure 12-216. SD Bus Power Control Sequence

(1) By reading the MMCSD0_CAPABILITIES register, get the support voltage of the Host Controller.

(2) Set MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field with maximum voltage that the Host Controller supports.

(3) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit to 1.

(4) Get the OCR value of all function internal of SD card.

(5) Judge whether SD Bus voltage needs to be changed or not. In case where SD Bus voltage needs to be changed, go to step (6). In case where SD Bus voltage does not need to be changed, go to "End".

(6) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit to 0 for clearing this bit. The card requires voltage rising from 0 volt to detect it correctly. The Host Driver shall clear MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit before changing voltage by setting MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field.

(7) Set MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE bit field.

(8) Set MMCSD0_POWER_CONTROL[0] SD_BUS_POWER to 1.

Note: Step (2) and step (3) can be executed at same time. And also, step (7) and step (8) can be executed at same time.

12.4.5.5.1.4 Changing Bus Width

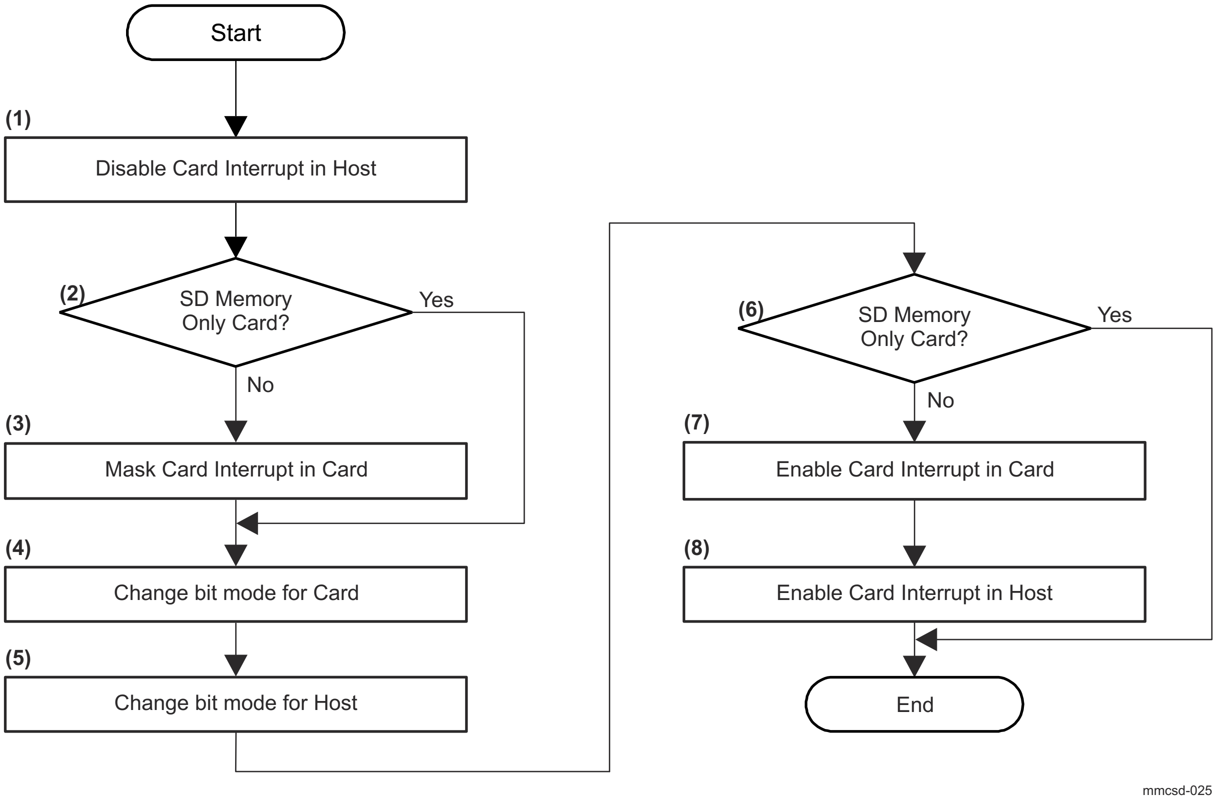


Figure 12-217. Change Bus Width Sequence

The sequence for changing bit mode on SD Bus is shown in Figure 12-217.

(1) Set MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 0 for masking incorrect interrupts that may occur while changing the bus width.

(2) In case of SD memory only card, go to step (4). In case of other card, go to step (3).

(3) Set "IENM" of the CCCR in a SDIO or SD combo card to 0 by CMD52.

(4) Change the bus width mode for a SD card. SD Memory Card bus width is changed by ACMD6 and SDIO card bus width is changed by setting Bus Width of Bus Interface Control register in CCCR.

(5) In case of changing to 4-bit mode, set MMCSD0_HOST_CONTROL1[1] DATA_WIDTH bit to 1. In another case (1-bit mode), set this bit to 0.

(6) In case of SD memory only card, go to the "End". In case of other card, go to step (7).

(7) Set "IENM" of the CCCR in a SDIO or SD combo card to 1 by CMD52.

(8) Set MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 1.

Note that if the card is locked, bus width cannot be changed. Unlock the card is required before changing bus width.

12.4.5.5.1.5 Timeout Setting on DAT Line

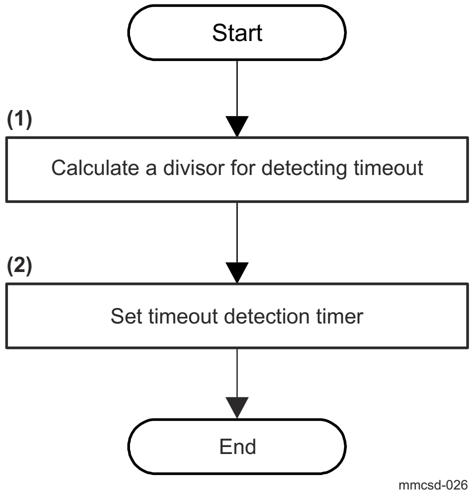


Figure 12-218. Timeout Setting Sequence

In order to detect timeout errors on DAT line, the Host Driver shall execute the following two steps before any SD transaction. For more information regarding SD transactions:

(1) Calculate a divisor to detect timeout errors by reading MMCSD0_CAPABILITIES[5-0] TIMEOUT_CLK_FREQ bit field and MMCSD0_CAPABILITIES[7] TIMEOUT_CLK_UNIT bit. If MMCSD0_CAPABILITIES[5-0] TIMEOUT_CLK_FREQ bit field is 00 0000b, the Host System shall provide this information to the Host Driver by another method.

(2) Set MMCSD0_TIMEOUT_CONTROL[3-0] COUNTER_VALUE bit field in accordance with the value from step (1) above.

12.4.5.5.1.6 Card Initialization and Identification (for SD I/F)

Figure 12-219 and Figure 12-220 shows initialization and card identification sequence for the Standard Capacity SD Memory Card (SDSC), the High Capacity SD Memory Card (SDHC) and the Extended Capacity SD Memory Card (SDXC) that was based on the Physical Layer Version 3.01. Refer to the latest sequence.

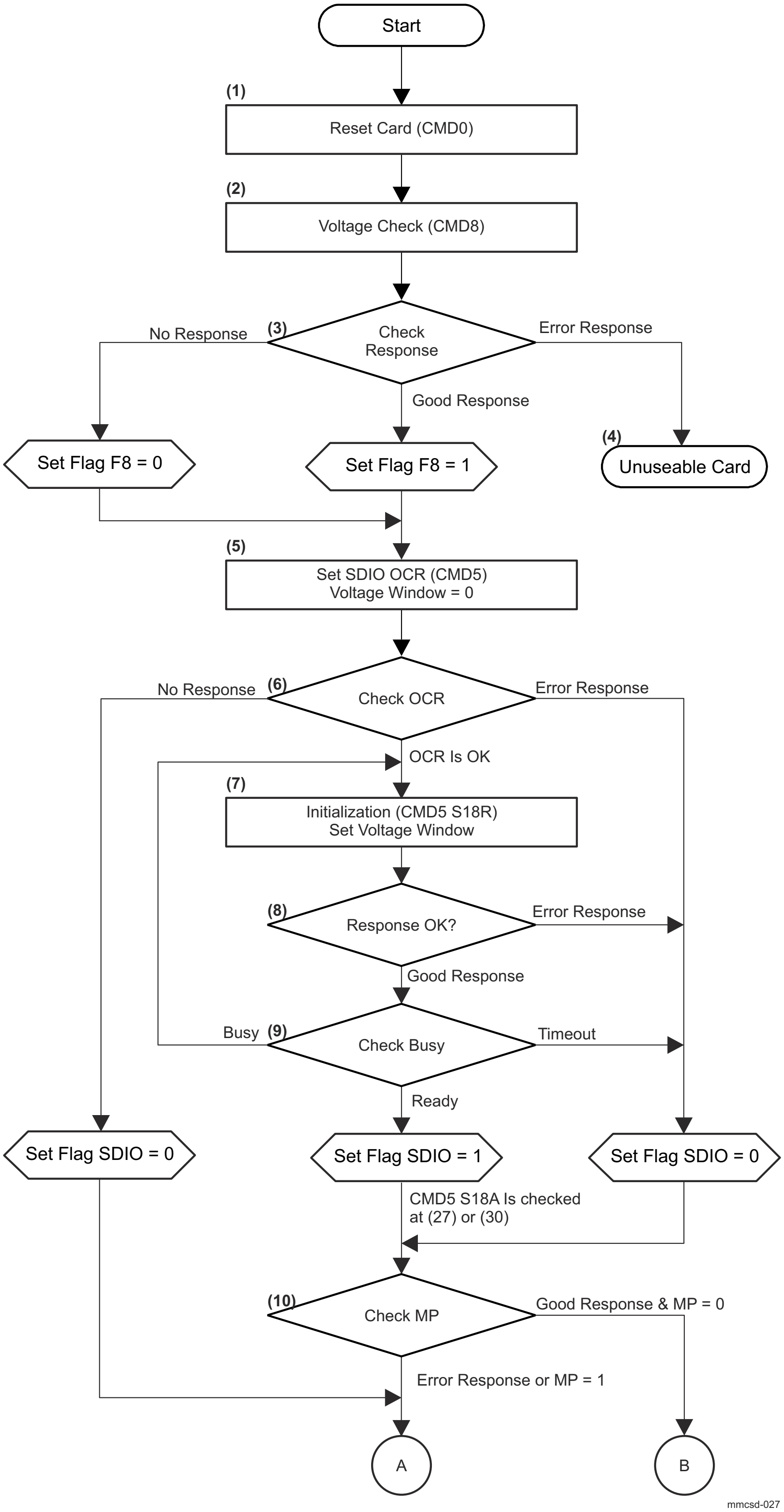


Figure 12-219. Card Initialization and Identification (1)

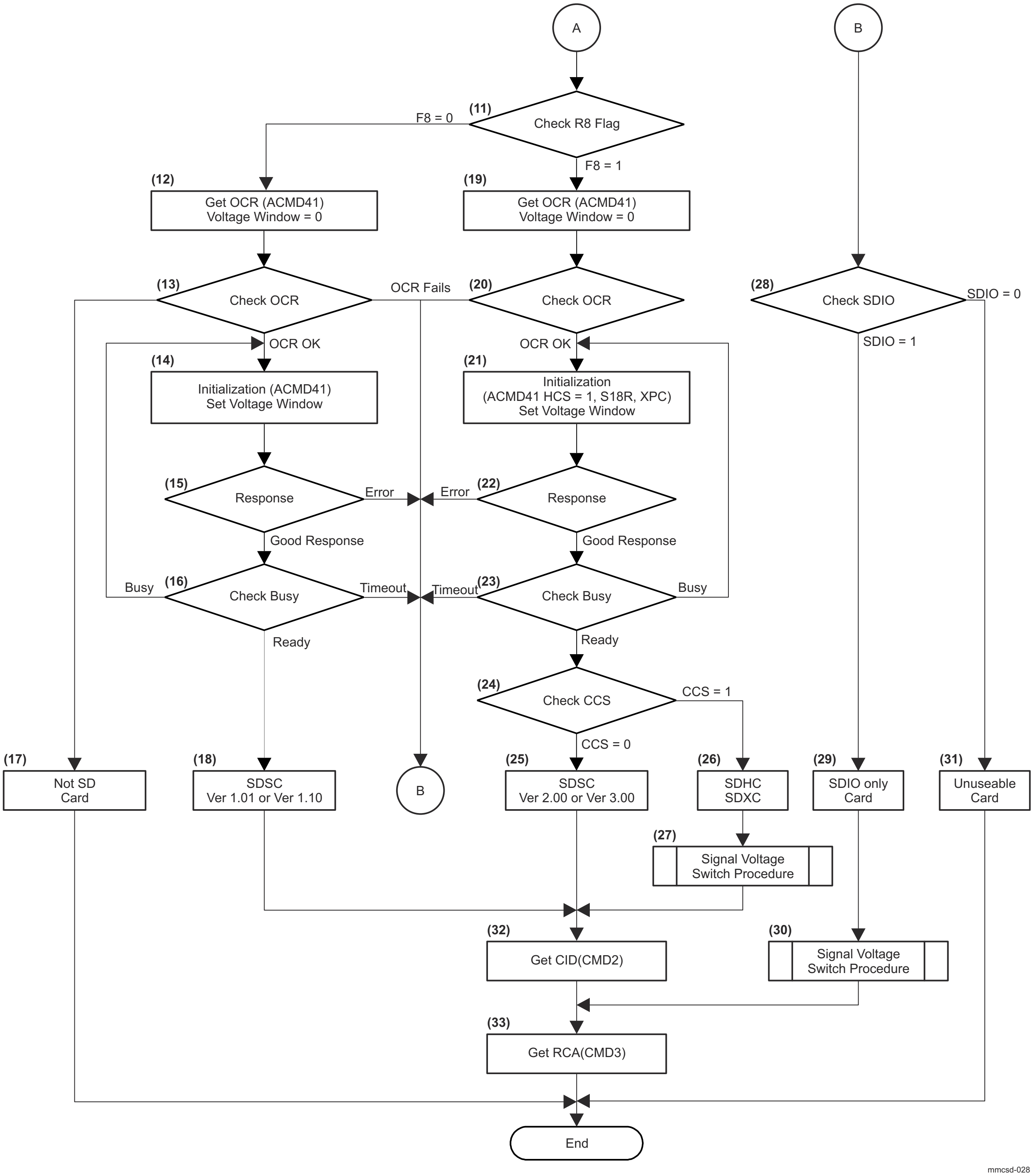


Figure 12-220. Card Initialization and Identification (2)

(1) SD Bus mode is selected by CMD0 (Keep Pin 1 to high during CMD0 execution).

(2) New CMD8 shall be issued after CMD0 to support High Capacity SD Memory Card.

(3) Voltage check command enables the Hosts to support future low voltage specification. However, at this time, only one voltage is defined. Legacy cards and Not SD cards do not respond to CMD8. In this case, set F8 to 0 (F8 is CMD8 valid flag used in step (11)) and go to Step (5). Only Version 2.00 or higher cards can respond to

CMD8. The host needs to check whether CRC of the response is valid and whether VHS and check pattern in the argument are equal to VCA and check pattern in the response. Passing all these checks results in CMD8 response OK. In this case, set F8 to 1 and go to step (5). If one of the checks is failed, go to step (4).

(4) Initialization is stopped by CMD8 fails. The Host Driver should retry step (1) to (3) one more time (this is not described in the figure).

(5) SDIO OCR is available by issuing CMD5 with setting voltage window (bit 23 to 0) in the argument to 0. SDIO initialization is not started.

(6) No response means the card does not have SDIO function. Set SDIO flag to 0 and go to step (11). If the card responds to CMD5 and the response is OK, go to step (7). If the response is error, set SDIO flag to 0 and go to step (10). SDIO flag indicates whether SDIO functions are initialized or not.

(7) The SDIO portion starts initialization by CMD5 with setting the supply voltage to the voltage window. UHS-I supported host sets S18R to 1. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(8) If no response or error response is receive, set SDIO flag to 0 and go to step (10). If good response is received, go to step (9).

(9) Check busy status in the response. If busy is released, set SDIO flag to 1 and go to step (10). Repeat from step (7) while busy is indicated. Detecting timeout of 1 second exits the loop. In this case, set SDIO flag to 0 and go to step (10).

(10) Good response in this step means that all responses received at (6) and (8) are valid. When response is good, MP (memory present) flag in the response can be checked. If the response valid and MP = 0, go to step (28). Otherwise, go to step (11).

(11) Check F8 flag set in step (3). If CMD8 is executed correctly (F8 = 1), go to step (19). Otherwise, go to step (12).

(12) OCR is available by issuing ACMD41 with the voltage window (bit 23 to 0) in the argument is set to 0. Memory initialization is not started. The response of CMD55 (ACMD41) may indicate illegal command error due to some SD cards do not recognized CMD8. The Host Driver should ignore this error or issue CMD0 before ACMD41 to clear this error status.

(13) If response of CMD55 is not received, the card is not SD cards and goes to (17). If the card responds to CMD55, it may also respond to CMD41. If the responses of ACMD41 are OK, go to Step (14). Otherwise, go to step (28). Locked card can be detected by the card status in the response of CMD55.

(14) The memory portion starts initialization by Issuing ACMD41 with setting the supply voltage to the voltage window. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(15) If no response or error response is received, go to step (28). If good response is received, go to step (16).

(16) Check busy status in the response. If busy is released, go to step (18). Repeat from step (14) while busy is indicated. The interval of ACMD41 shall be less than 50 ms. Detecting timeout of 1 second exits the loop and go to step (28).

(17) The host recognizes that the card is not SD memory card and quits SD card initialization.

(18) The host recognizes that the card is Version 1.xx Standard Capacity SD Memory Card. Go to Step (30).

(19) OCR is available by issuing ACMD41 with setting the voltage window (bit 23 to 0) in the argument is set to 0. Memory initialization is not started. Setting of HCS does not affect this operation.

(20) If the card responds to CMD55, it may also respond to CMD41. If the responses of ACMD41 are OK, go to Step (21). Otherwise, go to step (28). Locked card can be detected by the card status in the response of CMD55.

(21) The memory portion starts initialization by Issuing ACMD41 with setting the supply voltage to the voltage window. UHS-I supported host sets S18R to1. If the host can supply more than 150mA, XPC is set to 1. HCS in

the argument is set to 1, which indicates supporting High Capacity Memory Card. If the supplied voltage is not matched with voltage window of card, the card goes into inactive state and does not return the response.

(22) If no response or error response is received, go to step (28). If good response is received, go to step (23).

(23) Check busy status in the response. If busy is released, go to step (24). Repeat from step (21) while busy is indicated. The interval of ACMD41 shall be less than 50 ms. Detecting timeout of 1 second exits the loop and go to step (28).

(24) CCS in the response is valid after busy is released. If CCS = 0, it indicates the Standard Capacity SD Memory Card and go to step (25). If CCS = 1, it indicates the High Capacity SD Memory Card or Extended Capacity Memory Card and go to Step (26).

(25) The host recognizes that the card is Ver2.00 or Ver3.00 Standard Capacity SD Memory Card. Optimal functions defined in Version 2.00 or higher are available. Go to Step (32).

(26) The host recognizes that the card is the High Capacity SD Memory Card or Extended Capacity Memory Card.

(27) Perform the signal voltage switch procedure and go to step (32).

(28) Check SDIO flag. If SDIO = 1, go to step (28). Otherwise, go to step (31).

(29) The host recognizes that the card is SDIO only card and go to step (30).

(30) Perform the signal voltage switch procedure and go to step (33).

(31) The host recognizes that the card is unusable.

(32) In case of memory card, CMD2 is issued to get CID and Go to Step (31).

(33) CMD3 is issued to get RCA. If the RCA number is 0, the Host should issue CMD3 again.

12.4.5.5.1.6.1 Signal Voltage Switch Procedure (for UHS-I)

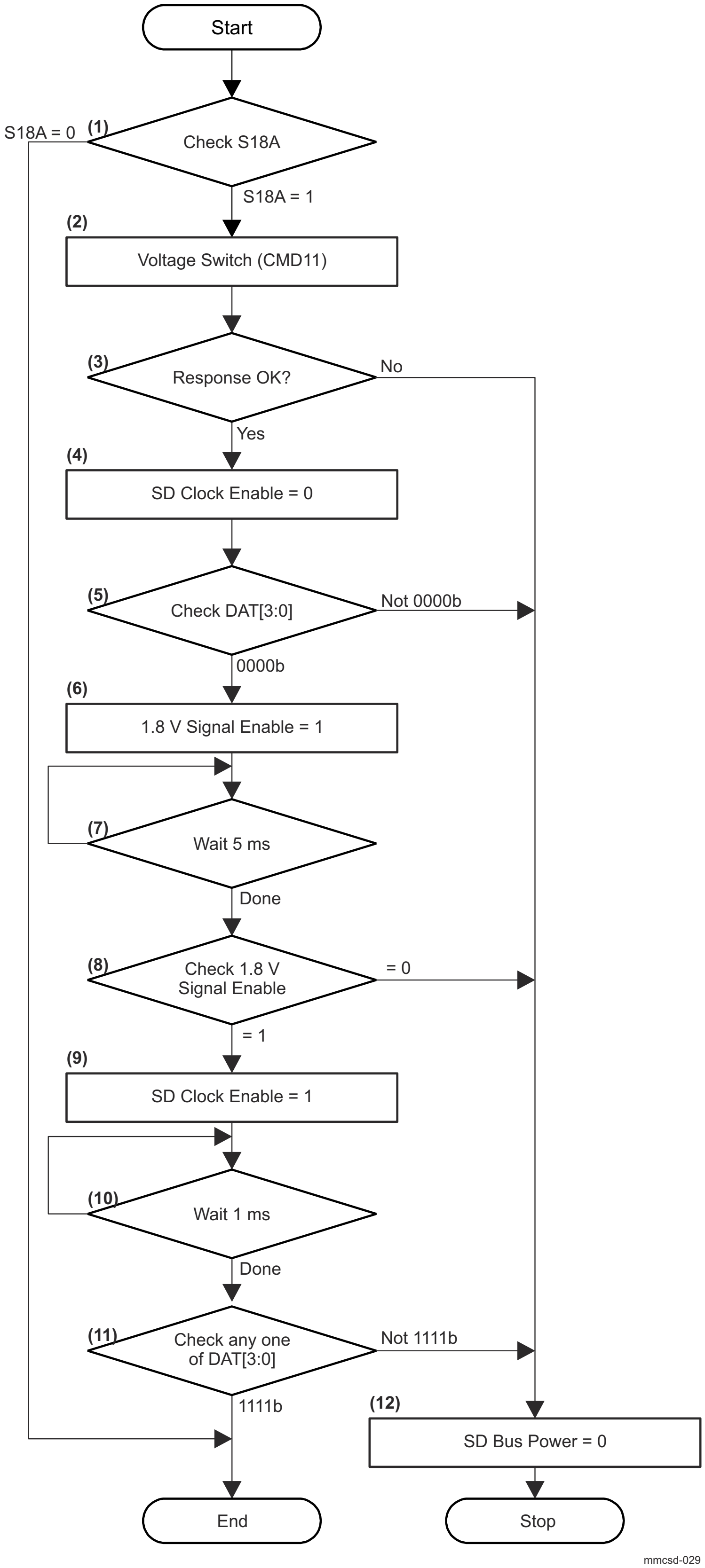


Figure 12-221. Signal Voltage Switch Procedure

(1) If S18A of CMD5 or S18A of ACMD41 is set to 1, signal voltage switch is performed according to the following steps. Otherwise, exits from this procedure.

(2) Issue CMD11.

(3) Check response and if an error is detected, go to step (12).

(4) Stop providing SD clock to the card.

(5) Check DAT[3:0] level. If the level is 0000b, the card is ready to start voltage switch sequence. Otherwise, go to (12) to quit the sequence.

(6) Set MMCSD0_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit.

(7) Wait 5 ms. 1.8 V voltage regulator shall be stable within this period.

(8) If MMCSD0_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit is cleared by Host Controller, go to step (12).

(9) Provide SD Clock to the card again.

(10) Wait 1 ms.

(11) Check DAT[3:0] level. If the level is 1111b, switch to 1.8 V signal level is completed successfully. Otherwise, go to (12).

(12) If an error occurs during voltage switch procedure, stop providing the power to the card. In this case, Host Driver should retry initialization procedure by setting S18R to 0 at step (7) and (21) in Figure 12-219 and Figure 12-220.

12.4.5.5.1.7 SD Transaction Generation

This section describes the sequences how to generate and control various kinds of SD transactions. SD transactions are classified into three cases:

(1) Transactions that do not use the DAT line.

(2) Transactions that use the DAT line only for the busy signal.

(3) Transactions that use the DAT line for transferring data.

In this specification the first and the second case's transactions are classified as "Transaction Control without Data Transfer using DAT Line", the third case's transaction is classified as "Transaction Control with Data Transfer using DAT Line". Refer to the latest SD Physical Layer Specification and SDIO Specification for more detail about SD commands specification.

12.4.5.5.1.7.1 Transaction Control without Data Transfer Using DAT Line

In this section, the sequence for how to issue SD Command and how to complete SD Command is explained. Figure 12-222 shows the sequence to issue a SD Command and Figure 12-223 shows the sequence to finalize a SD Command.

12.4.5.5.1.7.1.1 The Sequence to Issue a SD Command

The sequence to issue the SD Command is detailed in Figure 12-222.

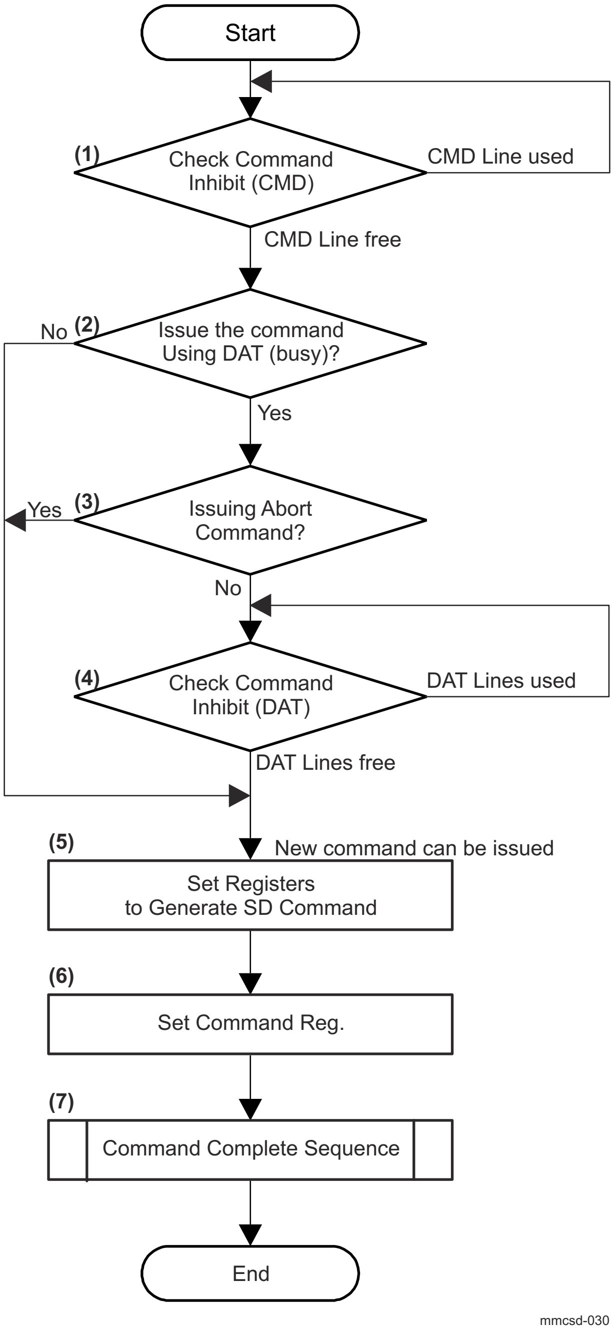


Figure 12-222. SD Command Issue Sequence

(1) Check MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit. Repeat this step until MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is 0. That is, when MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is 1, the Host Driver shall not issue a SD Command.

(2) If the Host Driver issues a SD Command using DAT lines including busy signal, go to step (3). If without using DAT lines including busy signal, go to step (5).

(3) If the Host Driver is issuing an abort command, go to step (5). In the case of nonabort command, go to step (4).

(4) Check MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit. Repeat this step until MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit is set to 0.

(5) Set registers except the MMCSD0_COMMAND register.

(6) Set the MMCSD0_COMMAND register.

Note: Writing the upper byte [3] in the MMCSD0_COMMAND register causes the Host Controller to issue a SD command to the SD card.

(7) Perform Command Completion Sequence in accordance.

12.4.5.5.1.7.1.2 The Sequence to Finalize a Command

Figure 12-223 shows the sequence to finalize a SD Command when response check is disabled. There is a possibility that some errors (Command Index/End bit/CRC/Timeout Error) occur during this sequence. If response check is enabled, error is indicated by Response Error Interrupt.

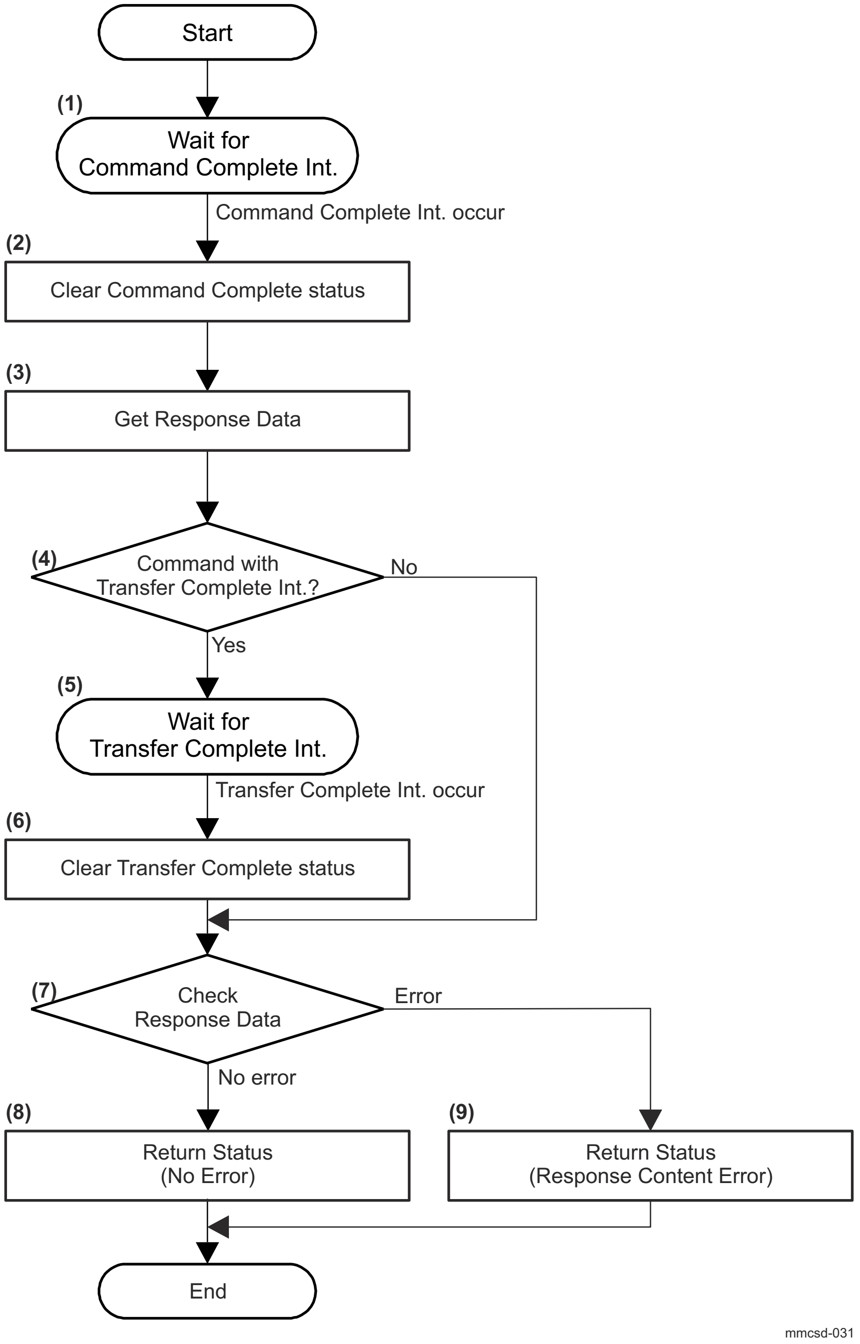


Figure 12-223. Command Complete Sequence

12.4.5.5.1.7.1.3

(1) If MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1 (response check is enabled), go to stop (4) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE). If the Command Complete Interrupt has occurred, go to step (2).

(2) Write 1 to MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(3) Read the Response register (see MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(4) Judge whether the command uses the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) or not. If it uses Transfer Complete, go to step (5). If not, go to step (7).

(5) Wait for the Transfer Complete Interrupt. If the Transfer Complete Interrupt has occurred, go to step (6).

(6) Write 1 to MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to clear this bit.

(7) Check for errors in Response Data (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7). If there is no error, go to step (8). If there is an error, go to step (9).

(8) Return Status of "No Error".

(9) Return Status of "Response Contents Error".

Note1: While waiting for the Transfer Complete interrupt, the Host Driver shall only issue commands that do not use the busy signal.

Note2: The Host Driver shall judge the Auto CMD12 complete by monitoring Transfer Complete.

Note3: When the last block of un-protected area is read using memory multiple block read command (CMD18), OUT_OF_RANGE error may occur even if the sequence is correct. The Host Driver should ignore it. This error will appear in the response of Auto CMD12 or in the response of the next memory command.

12.4.5.5.1.7.2 Transaction Control with Data Transfer Using DAT Line

Depending on whether DMA (optional) is used or not, there are two execution methods.

In addition, the sequences for SD transfers are classified into following three kinds according to how the number of blocks is specified:

(1) Single Block Transfer: The number of blocks is specified to the Host Controller before the transfer. The number of blocks specified is always one.

(2) Multiple Block Transfer: The number of blocks is specified to the Host Controller before the transfer. The number of blocks specified shall be one or more.

(3) Infinite Block Transfer: The number of blocks is not specified to the Host Controller before the transfer. This transfer is continued until an abort transaction is executed. This abort transaction is performed by CMD12 in the case of a SD memory card and by CMD52 in the case of a SDIO card.

12.4.5.5.1.7.2.1 Not using DMA

The sequence for not using DMA is shown in Figure 12-224.

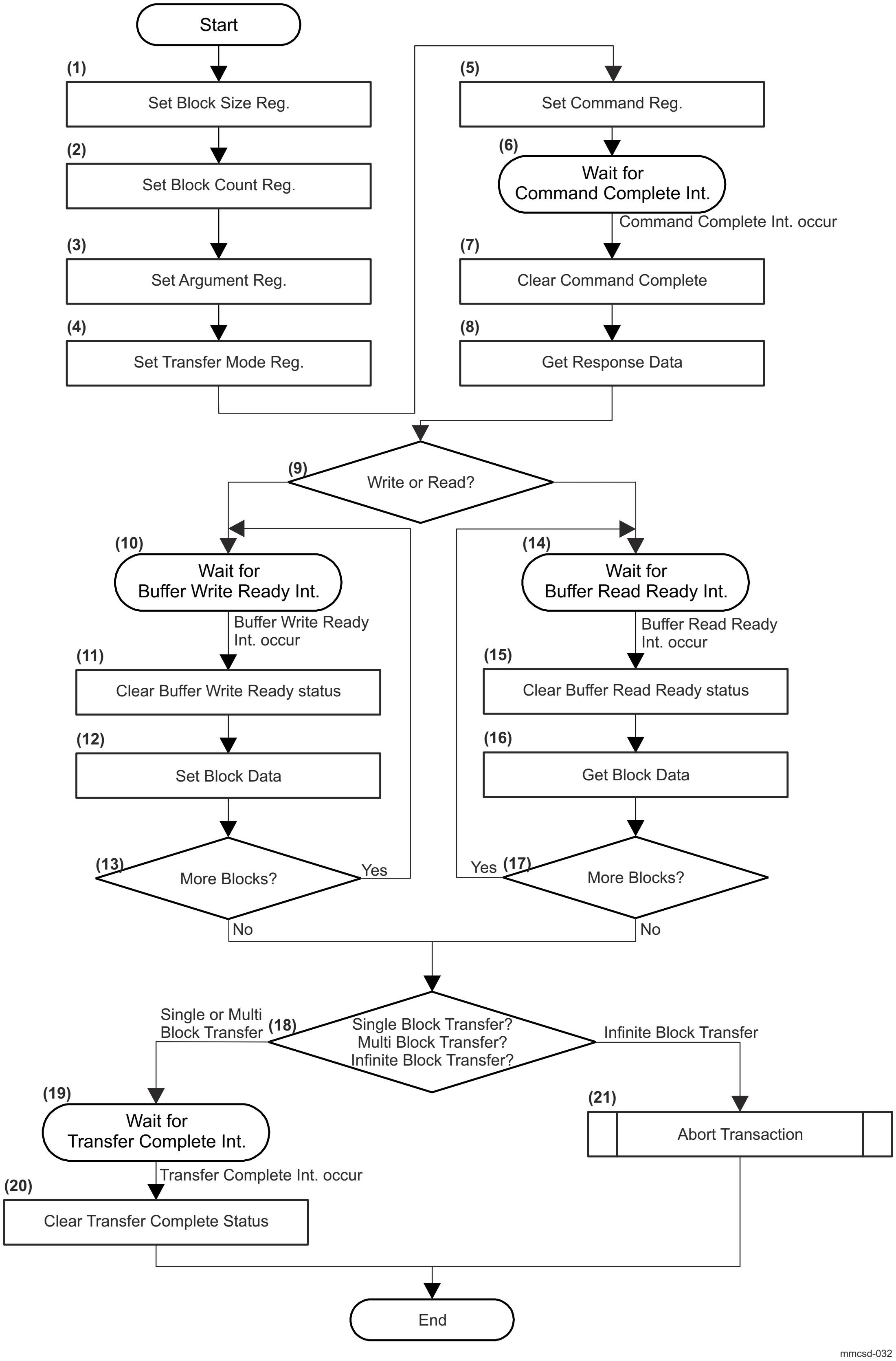


Figure 12-224. Transaction Control with Data Transfer Using DAT Line Sequence (Not using DMA)

(1) Set the value corresponding to the executed data byte length of one block to the MMCSD0_BLOCK_SIZE register.

(2) Set the value corresponding to the executed data block count to the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(3) Set the argument value to Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(4) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*.

If response check is enabled (MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5 (MMCSD0_TRANSFER_MODE[6] RESP_TYPE).

(5) Set the value to MMCSD0_COMMAND register.

Note: When writing the upper byte [3] of MMCSD0_COMMAND register, SD command is issued.

(6) If response check is enabled, go to stop (9) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(7) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit for clearing this bit.

(8) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(9) In the case where this sequence is for write to a card, go to step (10). In case of read from a card, go to step (14).

(10) Then wait for Buffer Write Ready Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[4] BUF_WR_READY).

(11) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[4] BUF_WR_READY bit for clearing this bit.

(12) Write block data (in according to the number of bytes specified at the step (1)) to MMCSD0_DATA_PORT register.

(13) Repeat until all blocks are sent and then go to step (18).

(14) Then wait for the Buffer Read Ready Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[5] BUF_RD_READY).

(15) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[5] BUF_RD_READY bit for clearing this bit.

(16) Read block data (in according to the number of bytes specified at the step (1)) from the MMCSD0_DATA_PORT register.

(17) Repeat until all blocks are received and then go to step (18).

(18) If this sequence is for Single or Multiple Block Transfer, go to step (19). In case of Infinite Block Transfer, go to step (21).

(19) Wait for Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(20) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit for clearing this bit.

(21) Perform the sequence for Abort Transaction in accordance with Section 12.4.5.5.1.8, *Abort Transaction*.

Note: Step (1) and Step (2) can be executed at same time. Step (4) and Step (5) can be executed at same time.

12.4.5.5.1.7.2.2 Using SDMA

The sequence for using SDMA is shown in Figure 12-225.

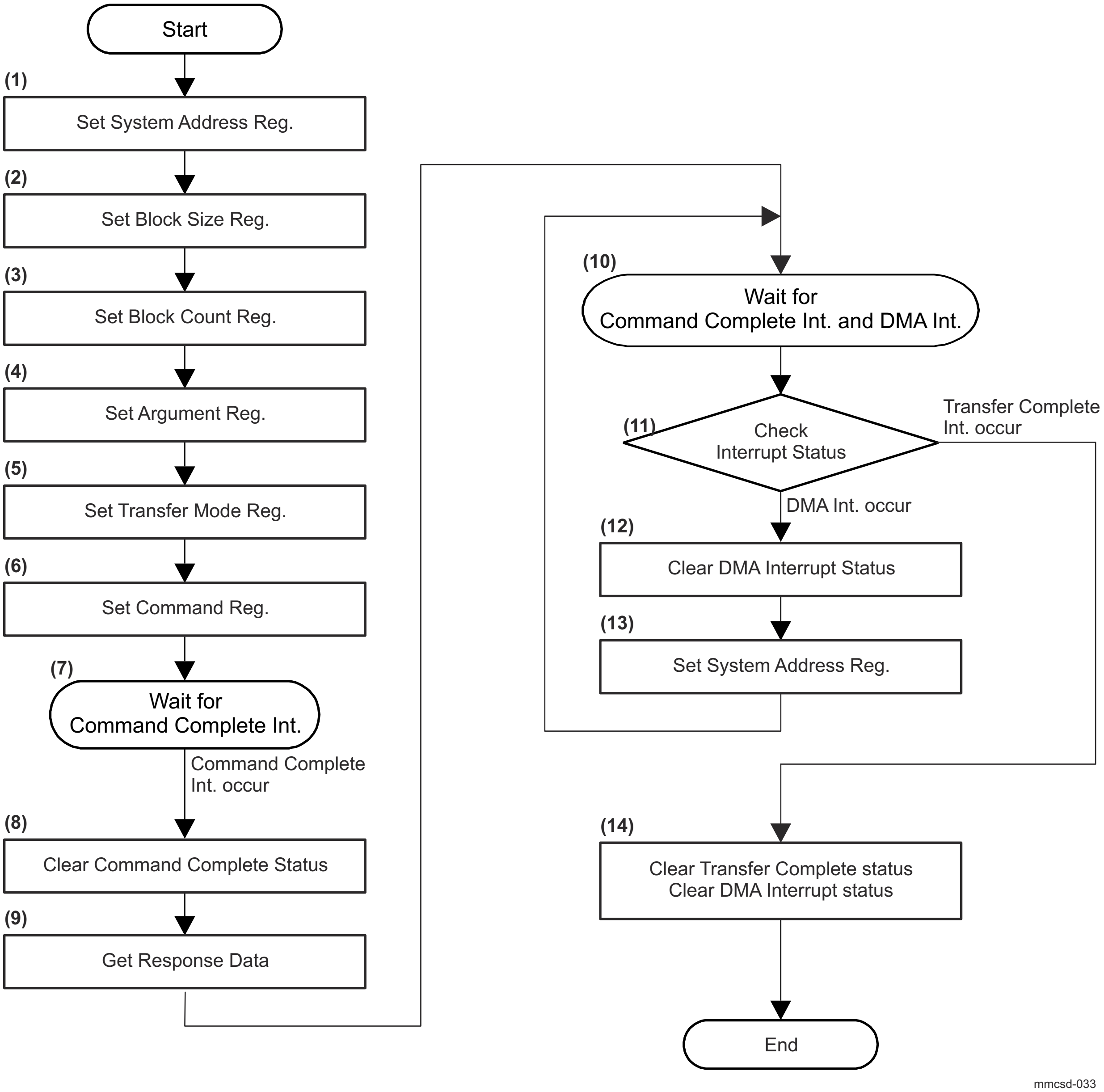


Figure 12-225. Transaction Control with Data Transfer Using DAT Line Sequence (Using SDMA)

(1) Data location of system memory is set to the SDMA System Address register if MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 0 or set to the MMCSD0_ADMA_SYS_ADDRESS register if MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1.

(2) Set the value corresponding to the executed data byte length of one block in the MMCSD0_BLOCK_SIZE register.

(3) Set the value corresponding to the executed data block count in the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(4) Set the argument value to the Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(5) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*. If response check is enabled (MMCSD0_TRANSFER_MODE[7]

RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5.

(6) Set the value to the MMCSD0_COMMAND register.

Note: When writing to the upper byte [3] of the MMCSD0_COMMAND register, the SD command is issued and SDMA is started.

(7) If response check is enabled, go to stop (10) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(8) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(9) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(10) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) and DMA Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT).

(11) If MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is set to 1, go to Step
(14) else if MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit is set to 1, go to Step
(12). The MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is higher priority than the MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit.

(12) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit to clear this bit.

(13) Set the next system address of the next data position to the System Address register (MMCSD0_ADMA_SYS_ADDRESS) and go to Step (10).

(14) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit and MMCSD0_NORMAL_INTR_STS_ENA[3] DMA_INTERRUPT bit to clear this bit.

Note: Step (2) and Step (3) can be executed simultaneously. Step (5) and Step (6) can also be executed simultaneously.

12.4.5.5.1.7.2.3 Using ADMA

The sequence for using ADMA is shown in Figure 12-226.

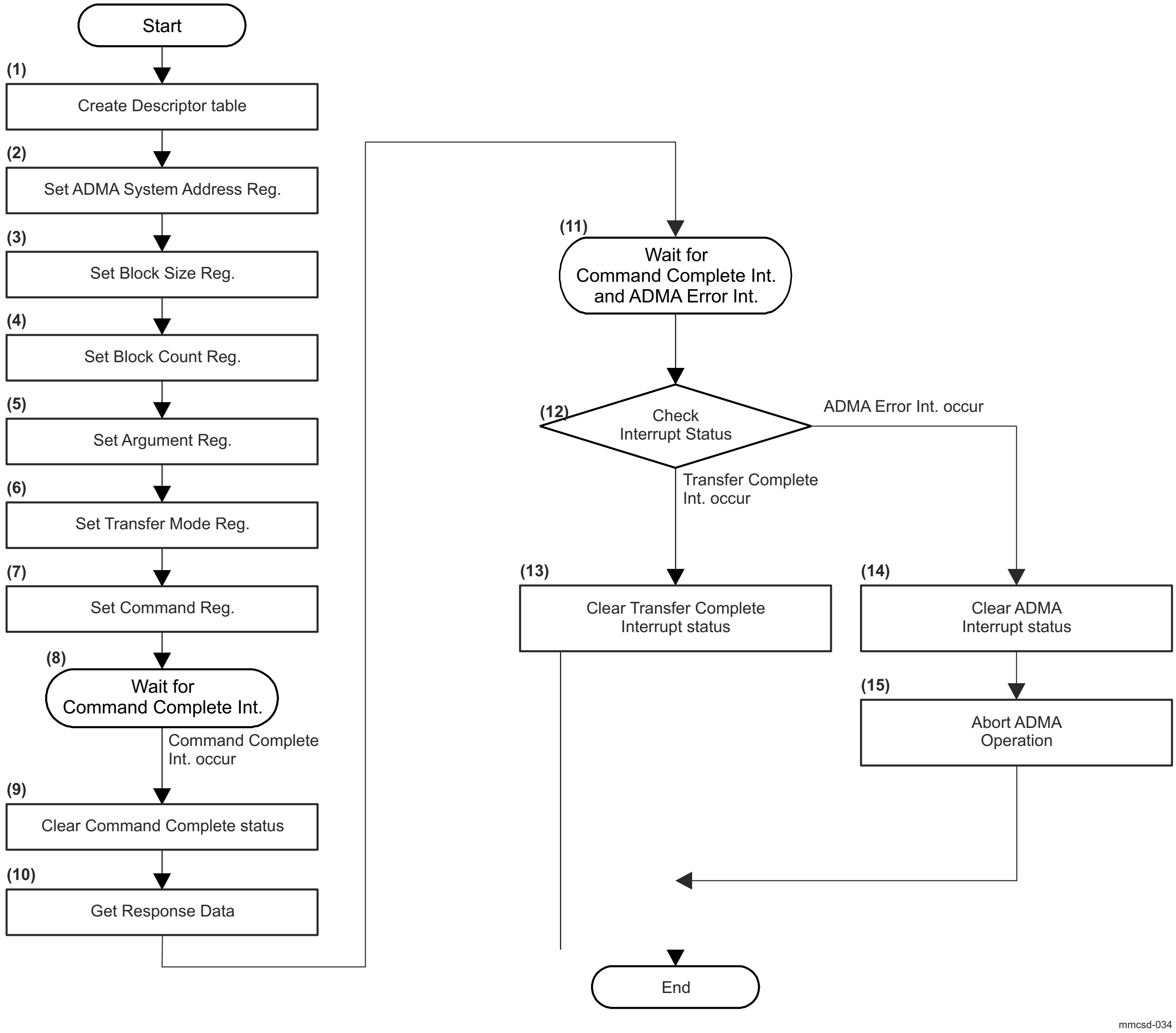


Figure 12-226. Transaction Control with Data Transfer Using DAT Line Sequence (Using ADMA)

(1) Create Descriptor table for ADMA in the system memory.

(2) Set the Descriptor address for ADMA in the MMCSD0_ADMA_SYS_ADDRESS register.

(3) Set the value corresponding to the executed data byte length of one block in the MMCSD0_BLOCK_SIZE register.

(4) Set the value corresponding to the executed data block count in the MMCSD0_BLOCK_COUNT register in accordance with *Determination of Transfer Type*.

(5) Set the argument value to the Argument register (MMCSD0_ARGUMENT1_LO and MMCSD0_ARGUMENT1_HI).

(6) Set the value to the MMCSD0_TRANSFER_MODE register. The Host Driver determines Multi/Single Block Select, Block Count Enable, Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the MMCSD0_TRANSFER_MODE register. Multi/Single Block Select and Block Count Enable are determined according to *Determination of Transfer Type*. If response check is enabled (MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1), set MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit to 1 and select Response Type R1/R5 (MMCSD0_TRANSFER_MODE[6] RESP_TYPE).

(7) Set the value to the MMCSD0_COMMAND register.

Note: When writing to the upper byte [3] of the MMCSD0_COMMAND register, the SD command is issued and DMA is started.

(8) If response check is enabled, go to stop (11) else wait for the Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit).

(9) Write 1 to the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit to clear this bit.

(10) Read Response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7) and get necessary information of the issued command.

(11) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE) and ADMA Error Interrupt (MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE).

(12) If MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit is set to 1, go to Step (13) else if MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE bit field is set to 1, go to Step (14).

(13) Write 1 to the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to clear this bit.

(14) Write 1 to the MMCSD0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE bit field to clear this bit.

(15) Abort ADMA operation. SD card operation should be stopped by issuing abort command. If necessary, the Host Driver checks MMCSD0_ADMA_ERR_STATUS register to detect why ADMA error is generated.

Note: Step (3) and Step (4) can be executed simultaneously. Step (6) and Step (7) can also be executed simultaneously.

12.4.5.5.1.8 Abort Transaction

An abort transaction is performed by issuing CMD12 for a SD memory card and by issuing CMD52 for a SDIO card. There are two cases where the Host Driver needs to do an Abort Transaction. The first case is when the Host Driver stops Infinite Block Transfers. The second case is when the Host Driver stops transfers while a Multiple Block Transfer is executing.

There are two ways to issue an Abort Command. The first is an asynchronous abort. The second is a synchronous abort. In an asynchronous abort sequence, the Host Driver can issue an Abort Command at any time unless MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit is set to 1. In a synchronous abort, the Host Driver shall issue an Abort Command after the data transfer stopped by using MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

12.4.5.5.1.8.1 Asynchronous Abort

The sequence for Asynchronous Abort is shown in Figure 12-227.

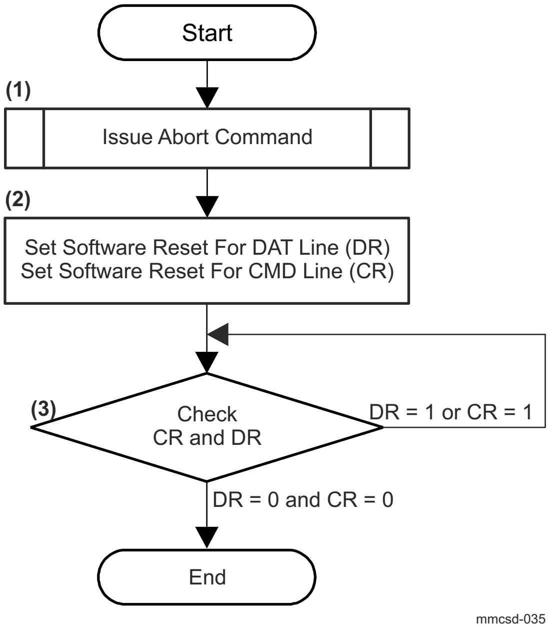


Figure 12-227. Asynchronous Abort Sequence

(1) Issue Abort Command in accordance.

(2) Set both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 to do software reset.

(3) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit are 0, go to "End". If either MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit or MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 1, go to step (3).

12.4.5.5.1.8.2 Synchronous Abort

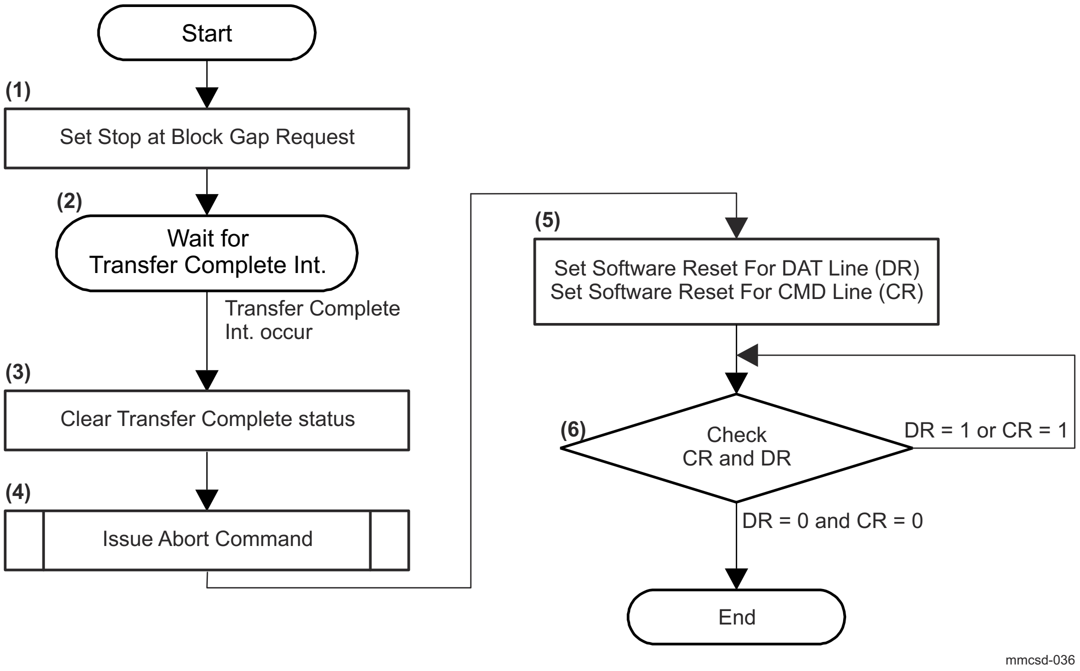


Figure 12-228. Synchronous Abort Sequence

(1) Set the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 1 to stop SD transactions.

(2) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(3) Set the MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE bit to 1 to clear this bit.

(4) Issue the Abort Command

(5) Set both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 to do software reset.

(6) Check both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If both MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit and MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit are 0, go to "End". If either MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit or MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 1, go to step (6).

12.4.5.5.1.9 Changing Bus Speed Mode

This section describes the sequence for switching the bus speed mode: Default Speed, High Speed mode and UHS-I mode. The switch command (CMD6) is used to change memory card bus speed mode. The EHS bit (SDIO Version 2.00) or BSS[2-0] bits (SDIO Version 3.00) in the CCCR register is used to change the bus speed mode for SDIO card. In case of Combo card, either of the switch method changes both memory and IO bus speed mode. This means the first switch is effective. Refer to the Physical Layer Specification Version 3.0x and the SDIO Specification Version 3.00 for more information about switching bus speed. Figure 12-229 shows the sequence for switching bus speed mode for Combo Card. Note that if the card is locked, bus width cannot be changed. Unlock the card is required before changing bus width.

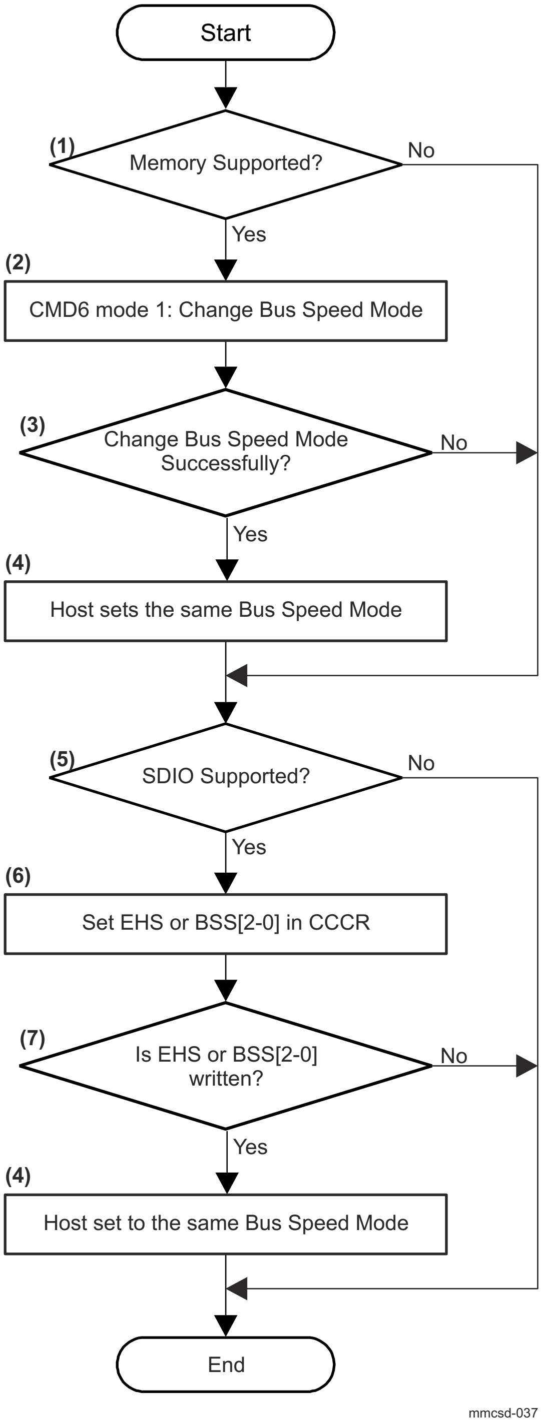


Figure 12-229. Changing Bus Speed Mode

(1) The Host Driver checks if the card supports memory. If not supported, go to (5).

(2) Issue CMD6 with mode 1 to change bus speed mode (Default, High Speed mode or UHS-I mode).

(3) Check the response of CMD6. If the card does not supports CMD6 (no response) or bus speed is not changed successfully, go to step (5). In this case, the card is in Default Speed mode.

(4) The Host Driver changes the Host Controller bus speed mode to the same mode.

(5) The Host Driver checks if the card supports SDIO. If not supported, go to the end.

(6) Issue CMD52 to write EHS bit or BSS[2-0] bits in CCCR to change bus speed mode (the same bus speed mode of (2) shall be set).

(7) If EHS or BSS[2-0] are not changed successfully, go to the end.

(8) The Host Driver changes the Host Controller bus speed to the same mode. In case of Combo card, bus speed is already changed at step (4) and this step does not affect changing bus speed.

12.4.5.5.1.10 Error Recovery

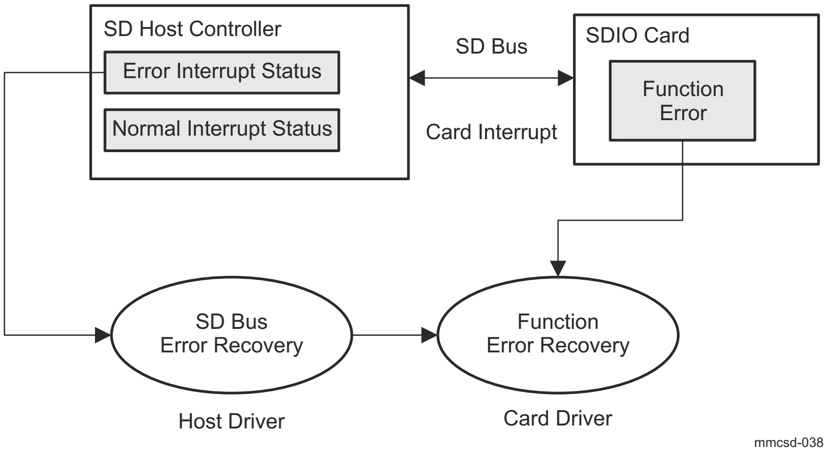


Figure 12-230. Error Report and Recovery

Figure 12-230 shows concept of error report and its recovery. The Host Controller has 2 interrupt status registers. If an error occurs in the SD Bus transaction, one of the bits is set in the MMCSD0_ERROR_INTR_STS register. If the function errors occur in the SDIO card, the card interrupt informs these function errors and the Card interrupt is set in the MMCSD0_NORMAL_INTR_STS_ENA register (the Card Interrupt is used to inform not only error statuses but also normal information. For example, to inform function ready). The Card Driver shall do function error recovery because the Host Driver does not know how to control the function. In the case that function error occurs due to SD Bus error, SD Bus error recovery is required before function error recovery. Abort command is used to recover SD Bus, and then the Host Driver should save error statuses related to SD Bus errors before issuing abort command and transfer these statuses to the Card Driver. These statuses may be used to recover function error. Following explanations are related to SD Bus error recovery. This specification does not specify the function error recovery.

When an error occurs during data transfer in 2L-HD UHS-II mode, there will be the case that Host Controller cannot drive D0 lane in input mode due to DIR LSS for retrieving lane direction is not detected. In this case, Host Driver cannot issue abort command for recovery. Then if DIR LSS is not detected, Host Controller sets MMCSD0_UHS2_ERR_INTR_STS[17] DEADLOCK_TIMEOUT bit. Host Driver should execute power cycle if MMCSD0_UHS2_ERR_INTR_STS[17] DEADLOCK_TIMEOUT bit is detected to recover from this error. Furthermore, if this type of error is detected several times in 2L-HD, Host Driver should use FD mode rather than using 2L-HD.

Implementation Note:

If the Card Driver cannot recover the function errors, the Host Driver should try following methods.

(9) Using IOEx for SDIO card

IOEx may be used as the reset per function basis. Sequence is as follows:

Clear IOEx = 0 and wait until IORx = 0 and then set IOEx = 1 again. SDIO may be recovered when IORx = 1.

(10) Using reset command for memory and SDIO card Re-initialization sequence is required.

(11) Off and on power supply for the SD Bus.

The card may be recovered by the power on reset. Re-initialization sequence is required.

The two cases where the Host Driver needs the "Error Recovery" sequence are classified as follows:

(1) Error Interrupt Recovery:

If error interrupt is indicated by the MMCSD0_ERROR_INTR_STS register, the Host Driver shall apply this sequence.

(2) Auto CMD12 Error Recovery:

If there are errors in Auto CMD12, the Host Driver shall apply this sequence. In terms of Return Status, Auto CMD12 Error Recovery is classified into 4 cases. It is shown in Figure 12-231. If error occurs during memory write transfer, strongly recommend using ACMD22 and then in the following recovery sequence, retry to send remaining blocks not written.

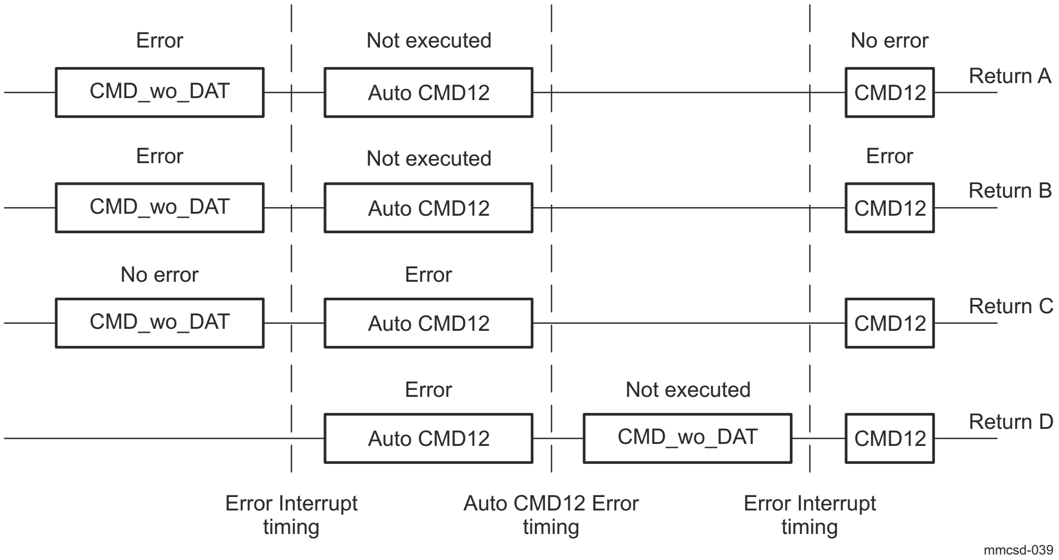


Figure 12-231. Return Status of Auto CMD12 Error Recovery

Implementation Note:

Abort command is used to recover from SD Bus error. SDIO transaction abort using CMD52 returns response but in the case of memory transaction abort using CMD12, response returns depending on the memory card state. If no response returns after issue CMD12, the Host Driver should check card state using CMD13. If the state is "tran" in the CURRENT_STATE, consider CMD12 is successful.

Implementation Note:

The following sequence is one possible error recovery flow. There may be another methods, sometimes using interrupts or polling. It can be possible to use another flows, based on Host System requirements.

In these error recovery sequences, return statuses for the next sequence. When the Host Controller cannot issue the next command due to SD Bus error, the error recovery sequences return "Non-recoverable" status. In this case, the Host System may cut off power to the SD Bus and then power on SD Bus and initialize both the Host Controller and the SD card again.

12.4.5.5.1.10.1 Error Interrupt Recovery

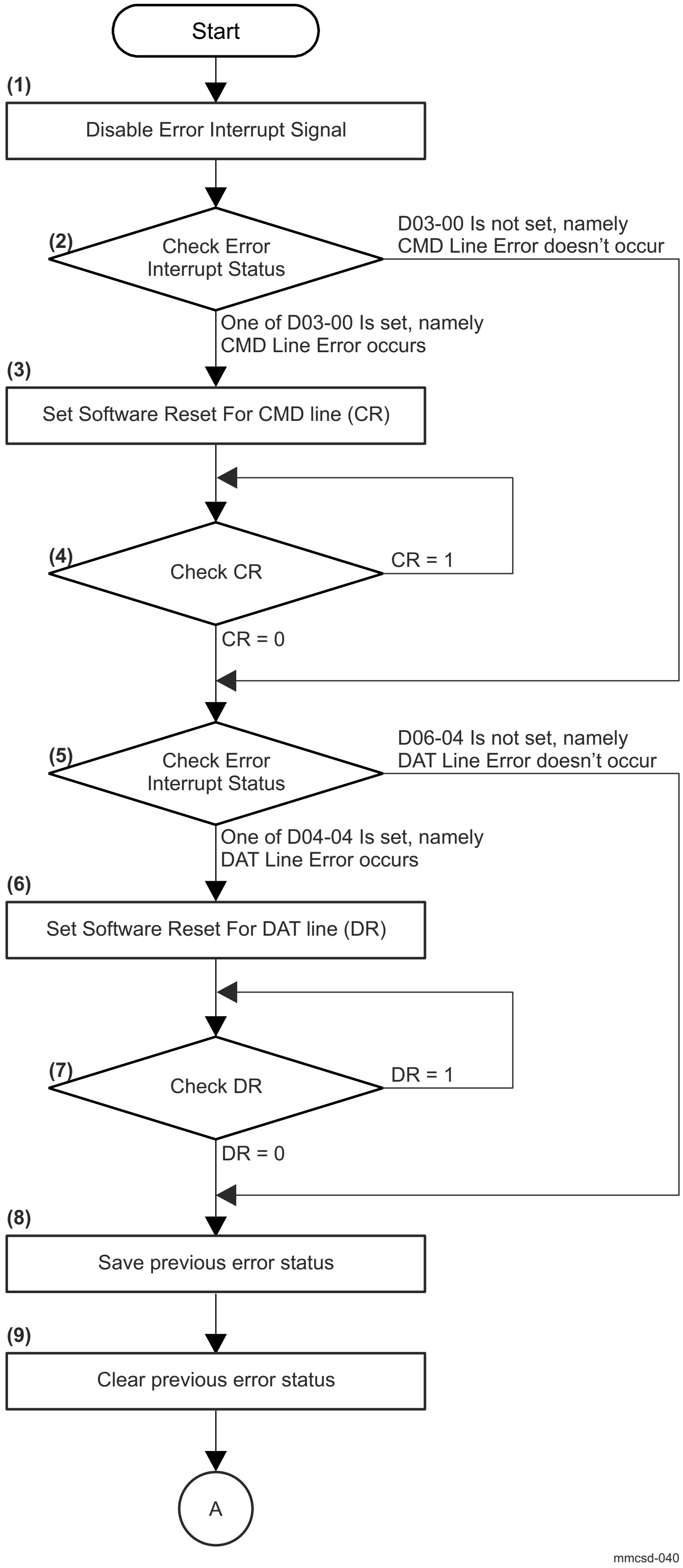


Figure 12-232. Error Interrupt Recovery Sequence (1)

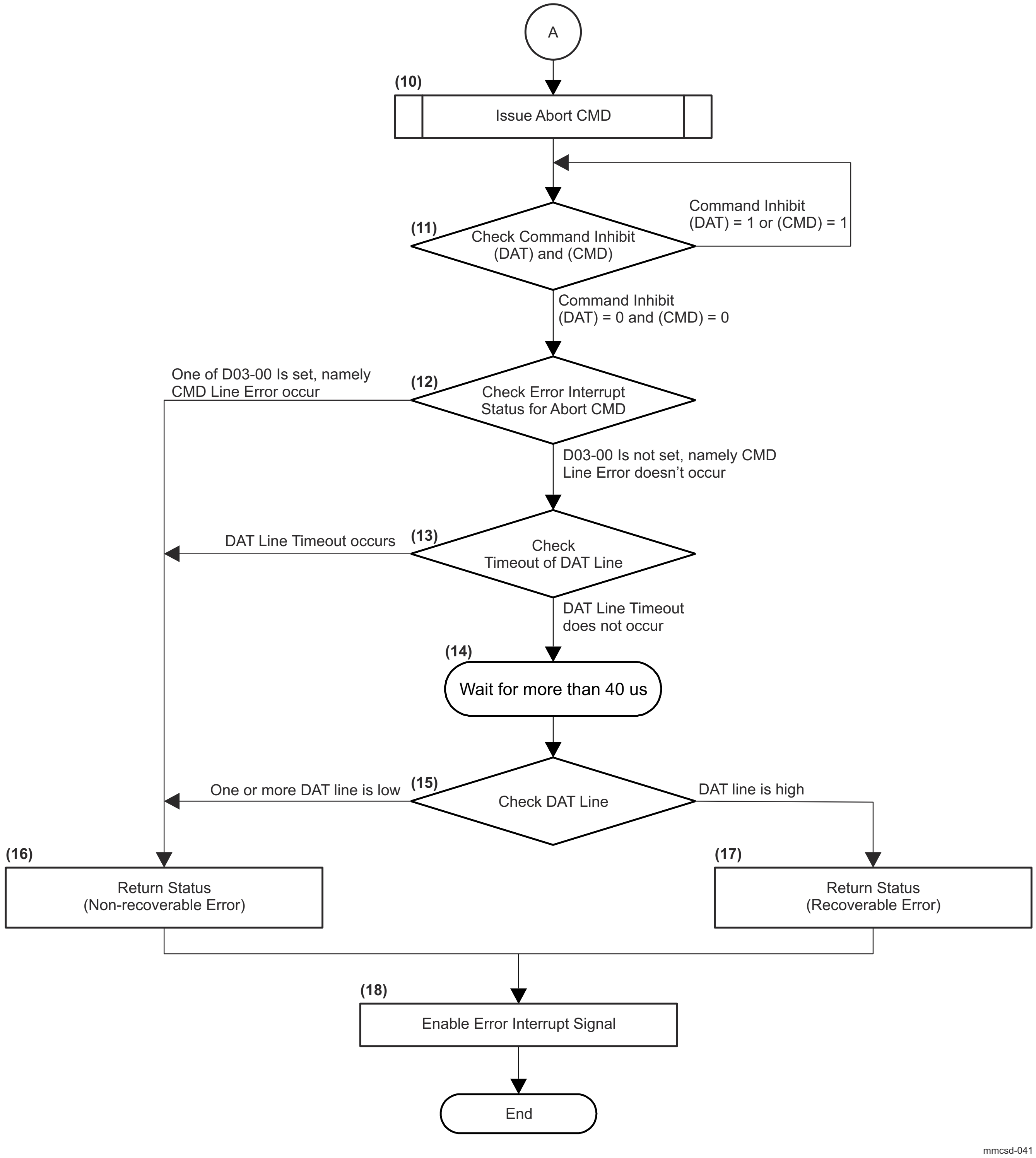


Figure 12-233. Error Interrupt Recovery Sequence (2)

(1) Disable the Error Interrupt Signal (MMCSD0_ERROR_INTR_SIG_ENA).

(2) Check bits D03-00 in the MMCSD0_ERROR_INTR_STS register. If one of these bits (D03-00) is set to 1, go to step (3). If none are set to 1 (all are 0), go to step (5).

(3) Set MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1.

(4) Check MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 0, go to step (5). If it is 1, go to step (4).

(5) Check bits D06-04 in the MMCSD0_ERROR_INTR_STS register. If one of these bits (D06-04) is set to 1, go to step (6). If none are set to 1 (all are 0), go to step (8).

(6) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(7) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (8). If it is 1, go to step (7).

(8) Save previous error status.

(9) Clear previous error status with setting them to 1.

(10) Issue Abort Command.

(11) MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit and MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit. Repeat this step until both MMCSD0_PRESENTSTATE[1] INHIBIT_DAT bit and MMCSD0_PRESENTSTATE[0] INHIBIT_CMD bit are set to 0.

(12) Check bits D03-00 in the MMCSD0_ERROR_INTR_STS register for Abort Command. If one of these bits is set to 1, go to step (16). If none of these bits are set to 1 (all are 0), go to step (13).

(13) Check MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If this bit is set to 1, go to step (16). If it is 0, go to step (14).

(14) Wait for more than 40 us.

(15) By monitoring the DAT [3:0] Line Signal Level in the MMCSD0_PRESENTSTATE register, judge whether the level of the DAT line is low or not. If one or more DAT lines are low, go to step (16). If the DAT lines are high, go to step (17).

(16) Return Status of "Non-recoverable Error".

(17) Return Status of "Recoverable Error".

(18) Enable the Error Interrupt Signal (MMCSD0_ERROR_INTR_SIG_ENA).

12.4.5.5.1.10.2 Auto CMD12 Error Recovery

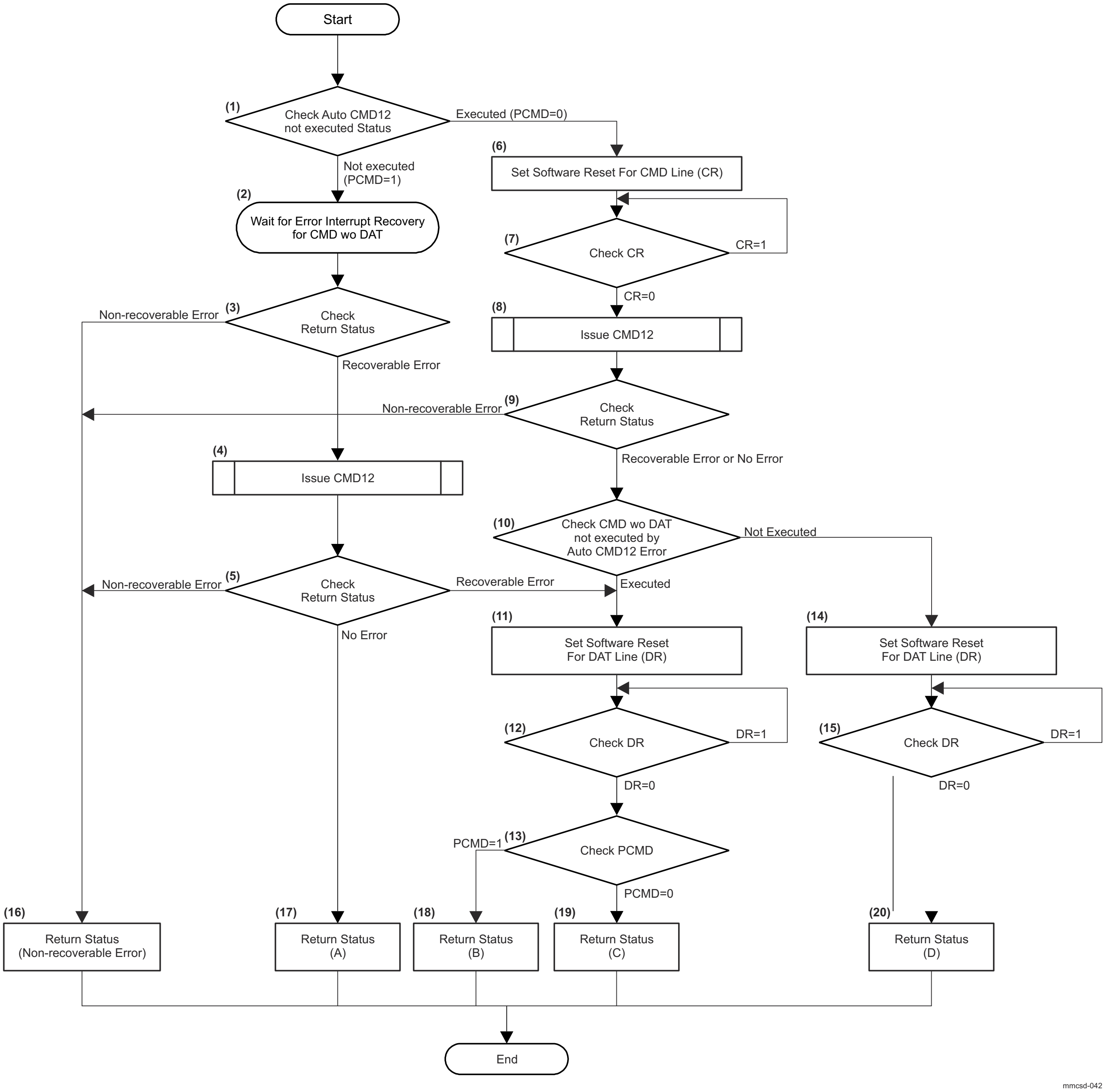


Figure 12-234. Auto CMD12 Error Recovery

The sequence for Auto CMD12 Error Recovery is shown in Figure 12-234. Following four cases A-D shall be covered.

A: An error occurred in CMD_wo_DAT, but not in the SD memory transfer.

B: An error occurred in CMD_wo_DAT, and also occurred in the SD memory transfer.

C: An error did not occur in CMD_wo_DAT, but an error occurred in the SD memory transfer.

D: CMD_wo_DAT was not issued, and an error occurred in the SD memory transfer.

(1) Check MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit. If this bit is set to 1, go to step (2). If this bit is set to 0, go to step (6). In addition, the Host Driver shall define PCMD flag, which changes to 1 if MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit is set to 1.

(2) Wait for Error Interrupt Recovery for CMD_wo_DAT.

(3) Check "Return Status". In the case of "Non-recoverable Error", go to step (16). In the case of "Recoverable Error", go to step (4).

(4) Issue CMD12 .

(5) If the CMD line errors occur for the CMD12 (one of D03-00 is set in the MMCSD0_ERROR_INTR_STS register), "Return Status" is "Non-recoverable Error" and go to step (16). If not CMD line error and busy timeout error occur (D04 is set in the MMCSD0_ERROR_INTR_STS register), "Return Status" is "Recoverable Error" and go to step (11). Otherwise, "Return Status" is "No error" and go to step (17).

(6) Set MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit to 1 for software reset of the CMD line.

(7) Check MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit. If MMCSD0_SOFTWARE_RESET[1] SWRST_FOR_CMD bit is 0, go to step (8). If it is 1, go to step (7).

(8) Issue CMD12 . Acceptance of CMD12 depends on the state of the card. CMD12 may make the card to return to tran state. If the card is already in tran state, the card does not response to CMD12.

(9) Check "Return Status" for CMD12. If "Return Status" returns "Non-recoverable Error", go to step (16). In the case of "Recoverable Error" or "No error", go to step (10).

(10) Check the MMCSD0_AUTOCMD_ERR_STS[0] ACMD12_NOT_EXEC bit. If this bit is 0, go to step (11). If it is 1, go to step (14).

(11) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(12) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (13). If it is 1, go to step (12).

(13) Check the PCMD flag. If PCMD is 1, go to step (18). If it is 0, go to step (19).

(14) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(15) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to step (20). If it is 1, go to step (15).

(16) Return Status of "Non-recoverable Error".

(17) Return Status that an error has occurred in CMD_wo_DAT, but not in the SD memory transfer.

(18) Return Status that an error has occurred in both CMD_wo_DAT, and the SD memory transfer.

(19) Return Status that an error has not occurred in CMD_wo_DAT, but has occurred in the SD memory transfer.

(20) Return Status that CMD_wo_DAT has not been issued, and an error has occurred in the SD memory transfer.

12.4.5.5.1.11 Wakeup Control (Optional)

After the Host System goes into standby mode, the Host System can resume from standby via a wakeup event initiated by one of the following three events:

(1) Interrupt from a SD card: If an SD card interrupt occurs, the Host System can resume from standby mode. If the Host System uses this wakeup factor, SD Bus power shall be kept on.

(2) Insertion of SD card: If a SD card is inserted, the Host System can resume from standby mode.

(3) Removal of SD card: If a SD card is removed, the Host System can resume from standby mode.

The sequence for preparing wakeup before the Host System goes into standby mode is shown in Figure 12-235.

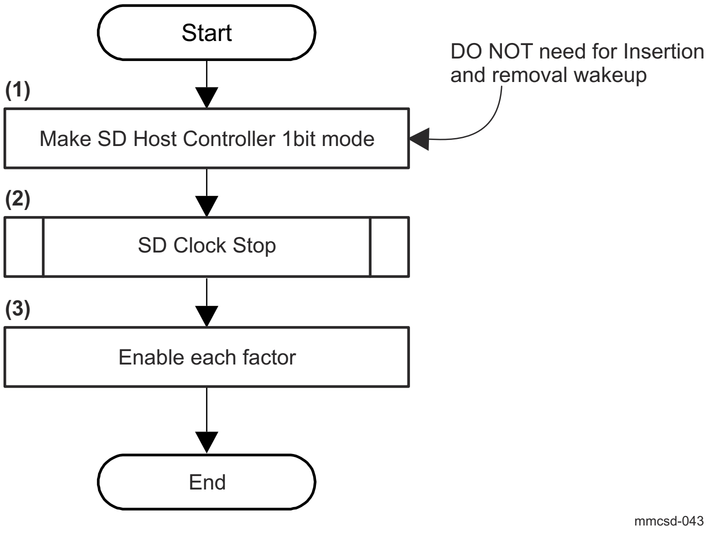


Figure 12-235. Wakeup Control before Standby Mode

(1) Set MMCSD0_HOST_CONTROL1[1] DATA_WIDTH bit to 0.

(2) Execute SD Clock Stop Sequence as described in Section 12.4.5.5.1.2.2, *SD Clock Supply and Stop Sequence*.

(3) Clear the MMCSD0_NORMAL_INTR_STS register and the MMCSD0_NORMAL_INTR_SIG_ENA register, and then set the enable bits of each wakeup event factor to 1 in the MMCSD0_WAKEUP_CONTROL register and set the bits of MMCSD0_ERROR_INTR_STS_ENA register to use wakeup.

The sequence for wakeup once in standby mode is shown in Figure 12-236.

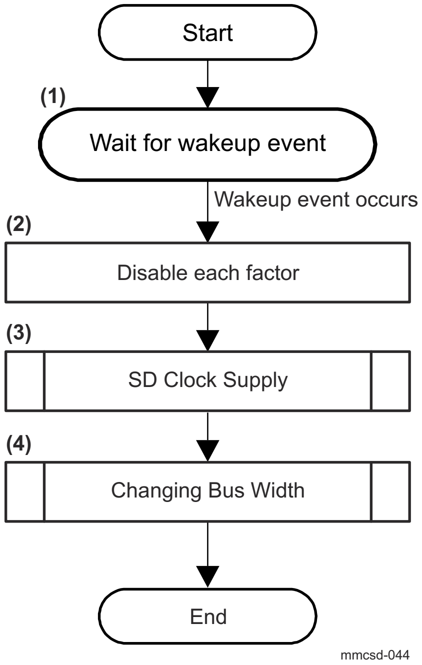


Figure 12-236. Wakeup from Standby

(1) Wait for wakeup event.

(2) Set the enable bits of each wakeup event factor to 0 in the MMCSD0_WAKEUP_CONTROL register and then clear event statuses in the MMCSD0_NORMAL_INTR_STS register. If necessary, set the MMCSD0_NORMAL_INTR_SIG_ENA register.

(3) Execute SD Clock Supply Sequence (see Section 12.4.5.5.1.2.2, *SD Clock Supply and Stop Sequence*).

(4) Set the SD Bus width (see Section 12.4.5.5.1.4, *Changing Bus Width*).

12.4.5.5.1.12 Suspend/Resume (Optional, Not Supported from Version 4.00)

If a SD card supports suspend and resume functionality, then the Host Controller can initiate suspend and resume. It is necessary for both the Host Controller and the SD card to support the function of "Read Wait". ADMA operation does not support this function.

12.4.5.5.1.12.1 Suspend Sequence

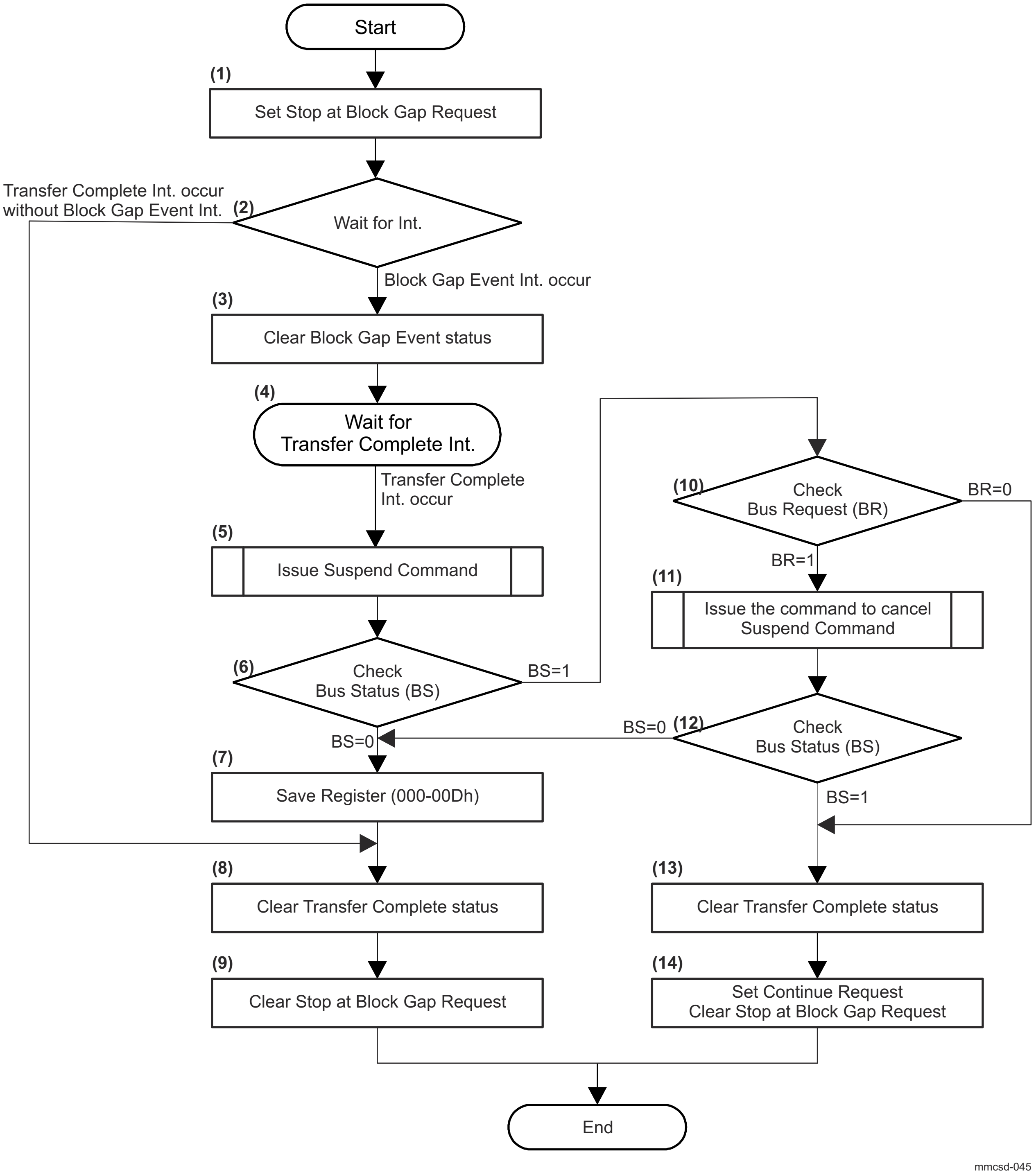


Figure 12-237. The Sequence for Suspend

(1) Set MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 1 to stop the SD transaction.

(2) Wait for an Interrupt. If MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit is set to 0 and MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is set to 1, go to step (8). If MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit is set to 1, go to step (3).

(3) Set MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit to 1 to clear this bit.

(4) Wait for the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS_ENA[1] XFER_COMPLETE).

(5) Issue the Suspend Command in accordance with Section 12.4.5.5.1.7.1, *Transaction Control without Data Transfer Using DAT Line*.

(6) Check the BS value of the response data. If BS is 0, go to step (7). If BS is 1, go to step (10).

(7) Save the register .

(8) Set MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit to 1 to clear this bit.

(9) Set MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to 0 to clear this bit.

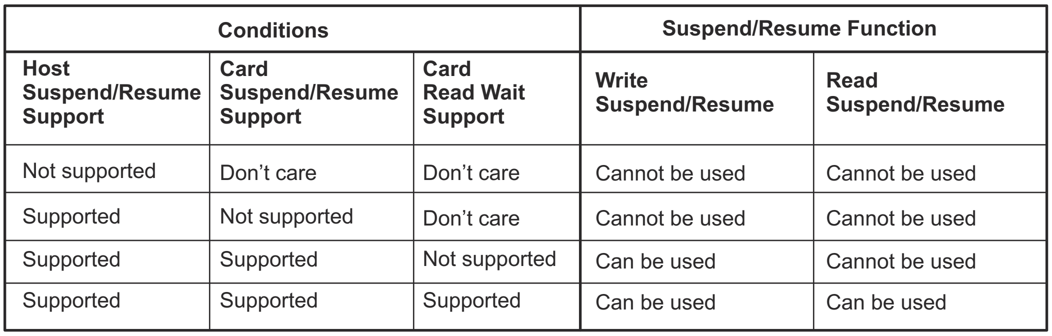
(10) Check the BR value of the response data. If BR is 1, go to step (11). If BR is 0, go to step (13).

(11) Issues the command to cancel the previous suspend command in accordance with Section 12.4.5.5.1.7.1, *Transaction Control without Data Transfer Using DAT Line*.

(12) Check the BS value of the response data. If BS is 0, go to step (7). If BS is 1, go to step (13).

(13) Set MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit to 1 to clear this bit.

(14) Set MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 to continue the transaction. At the same time, write 0 to MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit to clear this bit.



Conditions			Suspend/Resume Function	
Host Suspend/Resume Support	**Card Suspend/Resume Support**	**Card Read Wait Support**	**Write Suspend/Resume**	**Read Suspend/Resume**
Not supported	Don’t care	Don’t care	Cannot be used	Cannot be used
Supported	Not supported	Don’t care	Cannot be used	Cannot be used
Supported	Supported	Not supported	Can be used	Cannot be used
Supported	Supported	Supported	Can be used	Can be used

Figure 12-238. Suspend/Resume Condition

12.4.5.5.1.12.2 Resume Sequence

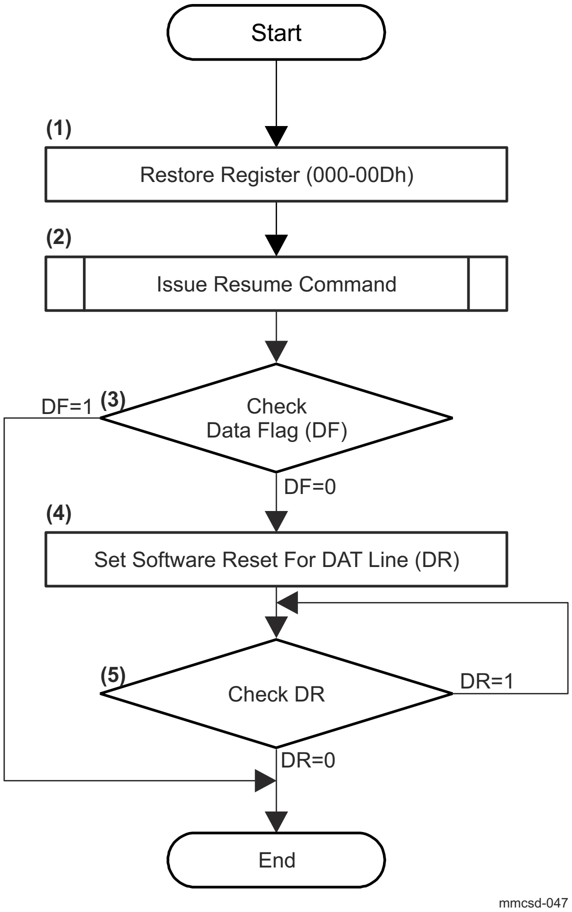


Figure 12-239. The Sequence for Resume

(1) Restore the register .

(2) Issue the Resume Command .

(3) Check the DF value of the response data. If DF is 0, go to step (4). If DF is 1, go to "End".

(4) Set MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit to 1 for software reset of the DAT line.

(5) Check MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit. If MMCSD0_SOFTWARE_RESET[2] SWRST_FOR_DAT bit is 0, go to "End". If it is 1, go to step (5).

12.4.5.5.1.12.3 Stop At Block Gap/Continue Timing for Read Transaction

The timing of Stop At Block Gap Request and Continue Request. The Transfer Complete interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is always generated by setting MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit where data transfer is stopped. However, generation of the Block Gap Event interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is dependent on whether the last data block is sent or not. Block Gap Event is not generated If all data blocks are transferred (the last block is transferred). It is not necessary to enable Block Gap Event interrupt. The status can be checked when transfer complete interrupt is detected. It is not necessary to use Continue Request (MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE) if Block Gap Event status is not set because there is no further data to be transferred. If Read Wait is not supported, Host Controller stops SD Clock at the block gap.

Implementation Note:

The MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL, MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE, MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bits shall be set and cleared by the Host Controller.

The MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set and cleared by the Host Driver. The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit shall be set by the Host Driver and be cleared by the Host Controller. The MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit and MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit shall be set by the Host Controller and be cleared by the Host Driver.

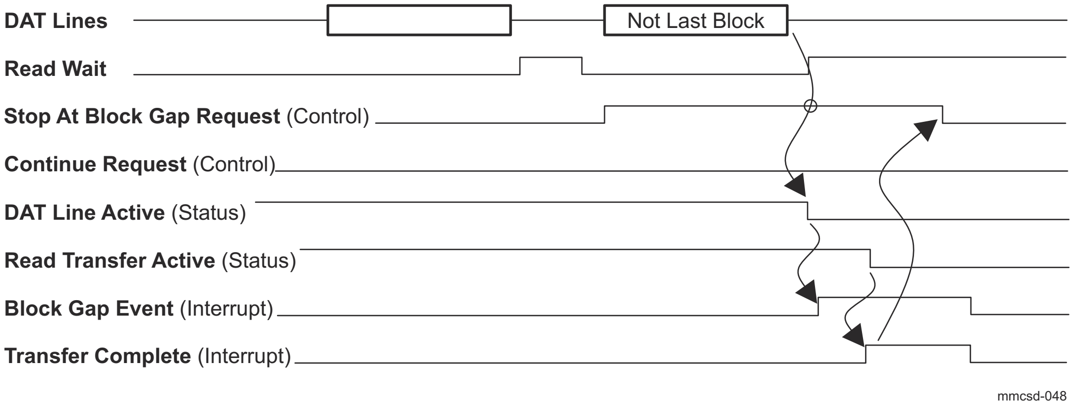


Figure 12-240. Wait Read Transfer by Stop At Block Gap Request

The Host Controller can accept a Stop At Block Gap Request (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP) when all the following conditions are met.

(1) It is at the block gap.

(2) The Host Controller can assert read wait or it is already asserted.

(3) The MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit is set to 1.

After accepting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit:

(1) Clear MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT).

(2) After all valid data has been read (No valid read data remains in the Host Controller), clear the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE).

(3) After accepting MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit, clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

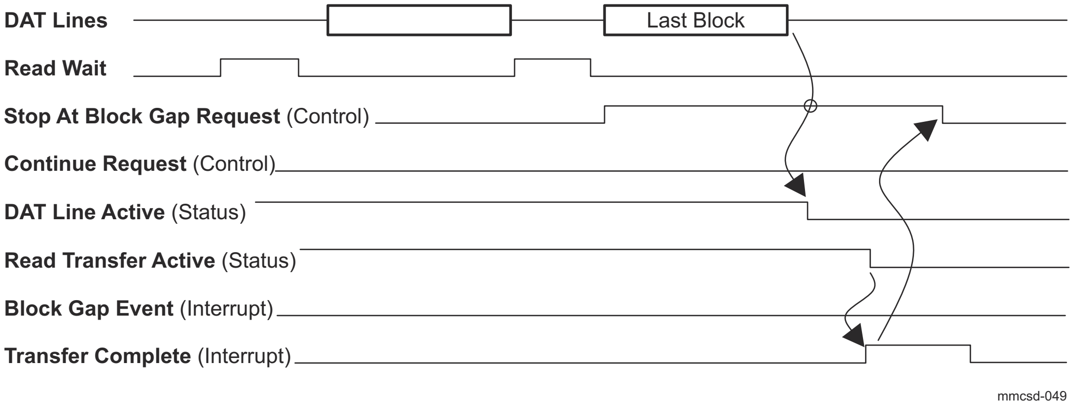


Figure 12-241. Stop At Block Gap Request is Not Accepted at the Last Block of the Read Transfer

If the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1 during the last block transfer, the Host Controller shall not accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and stops the transaction normally. The Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is not generated. When the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is generated, and if the MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit status is not set to 1, the driver shall clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

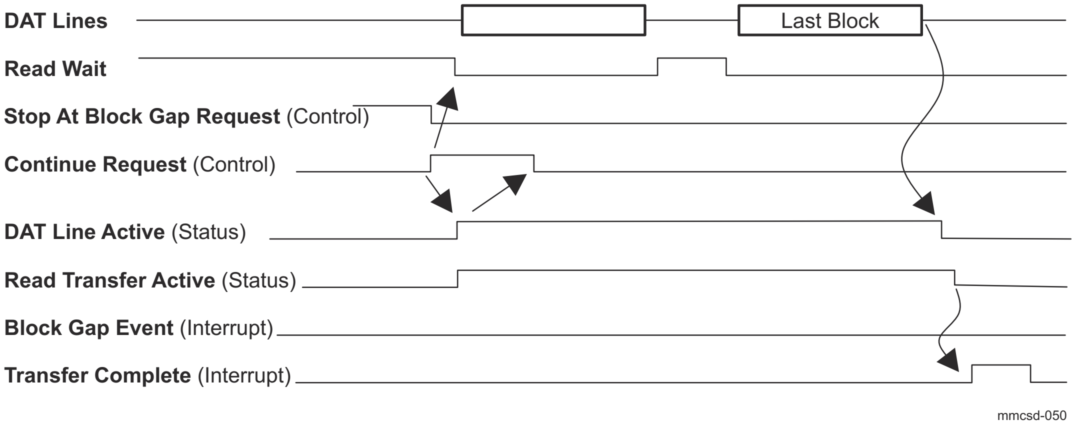


Figure 12-242. Continue Read Transfer by Continue Request

To restart a stopped data transfer, set the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 (the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set to 0).

After accepting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit:

(1) Release MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit (if the data block can accept the next data).

(2) Set the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit.

(3) The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit is automatically cleared by (2).

The end of the read transfer is specified by data length.

(1) Clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and do not generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit).

(2) After all valid data has been read (No valid read data remains in the Host Controller), clear the MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

12.4.5.5.1.12.4 Stop At Block Gap/Continue Timing for Write Transaction

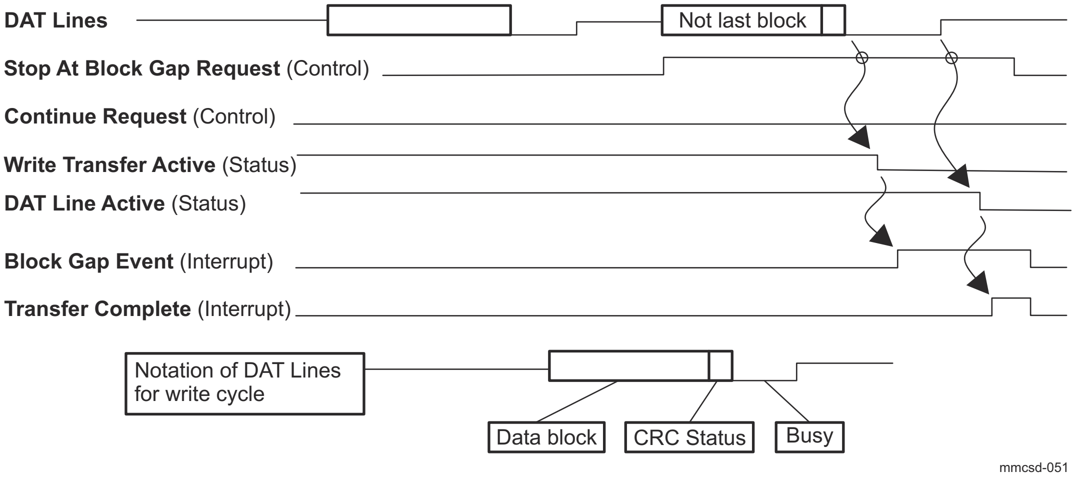


Figure 12-243. Wait Write Transfer by Stop At Block Gap Request

The Host Controller can accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit when matches all following conditions:

(1) It is at the block gap.

(2) No valid write data remains in the Host Controller.

After accepting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

(1) Clear the MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit and generate the Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT bit).

(2) After the busy signal is released, clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generate the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

(3) After accepting the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit), clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

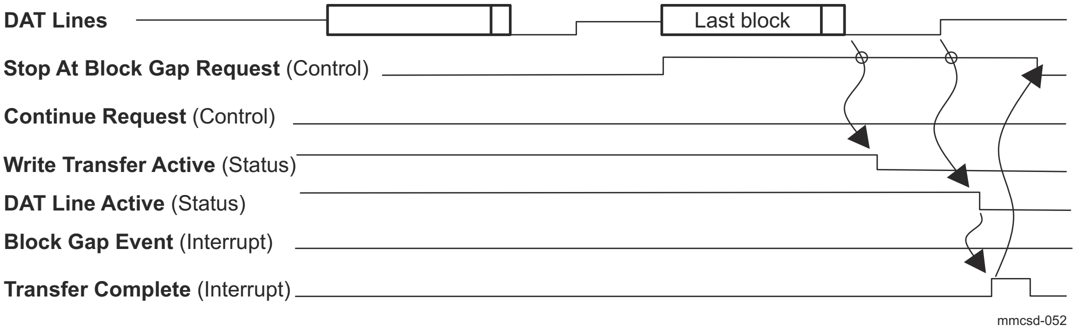


Figure 12-244. Stop At Block Gap Request is Not Accepted at the Last Block of the Write Transfer

If the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1 during the last block transfer, the Host Controller shall not accept the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and terminates the transaction normally. The Block Gap Event Interrupt (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVENT) is not generated. When the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE) is generated, and if the MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVEN bit is not set to 1, the driver shall clear the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit.

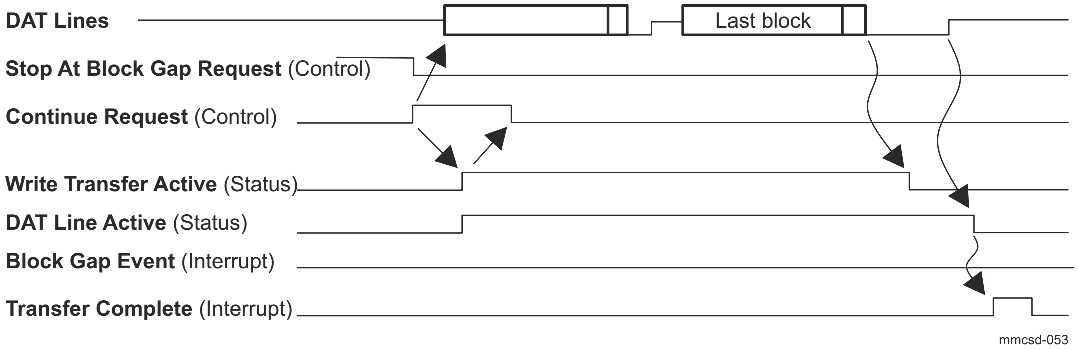


Figure 12-245. Continue Write Transfer by Continue Request

To restart a stopped data transfer, set the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to 1 (the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit shall be set to 0).

After accepting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit:

(1) Set the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit.

(2) The MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit is automatically cleared by (1).

The end of transfer is specified by data length.

(1) Clear the MMCSD0_PRESENTSTATE[8] WR_XFER_ACTIVE bit, and do not generate the (MMCSD0_NORMAL_INTR_STS[2] BLK_GAP_EVEN).

(2) After the busy signal is released, clear the MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit and generates the Transfer Complete Interrupt (MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit).

12.4.5.5.2 Driver Flow Sequence

Note

UHSII is not supported. For more information, see *Not Supported Features*.

12.4.5.5.2.1 Host Controller Setup and Card Detection

12.4.5.5.2.1.1 Host Controller Setup Sequence

Figure 12-246 and Table 12-239 show a Host Controller setup sequence.

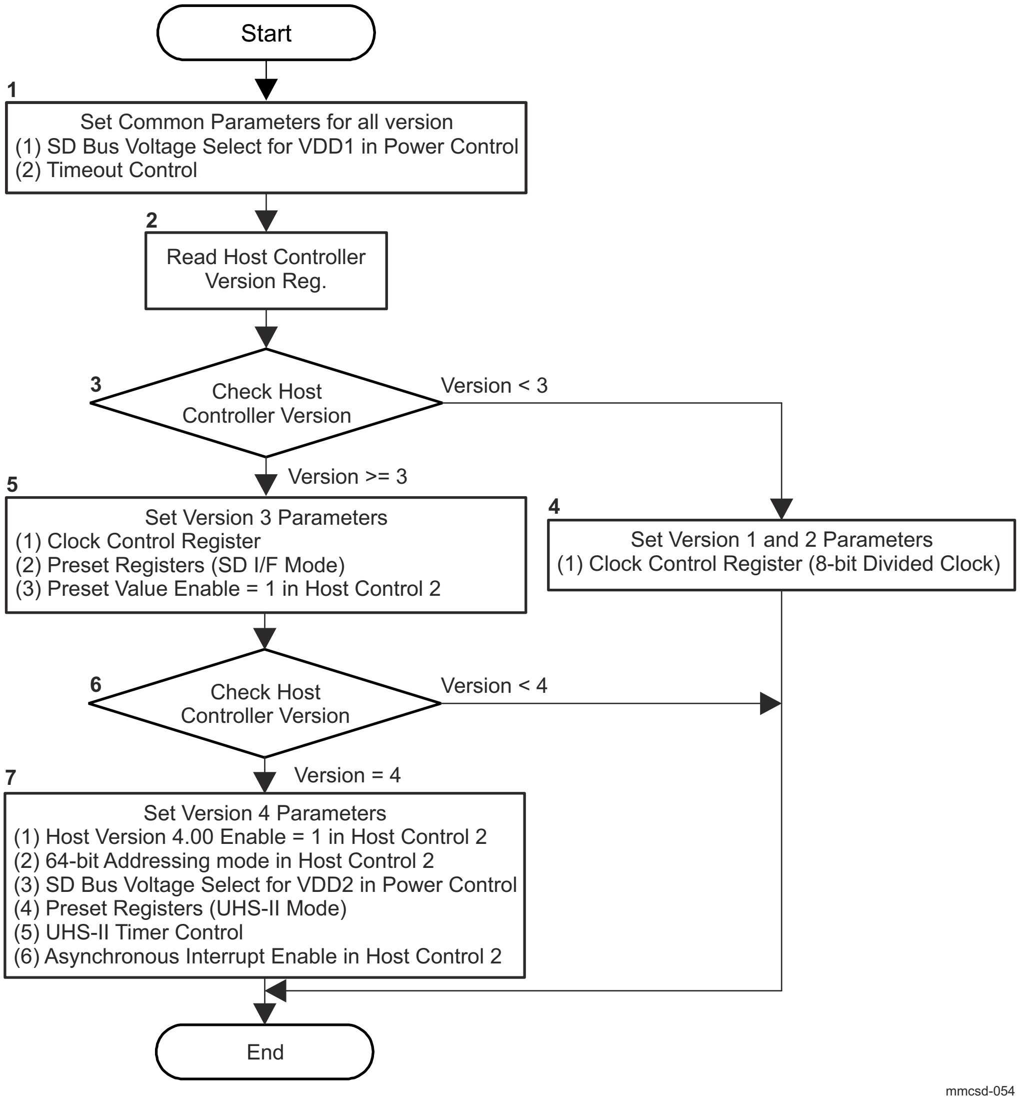


Figure 12-246. Host Controller Setup Sequence

Table 12-239. Host Controller Setup Sequence

Step	Description
1	Set parameters for all Host Controller version. Set the MMCSD0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE and MMCSD0_TIMEOUT_CONTROL[3-0] COUNTER_VALUE bit fields.
2	Read the MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM bit field.
3	If Specification Version number (MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM) is less than version 3, go to step (4), if it is version 3 or later go to step (5).
4	Set the MMCSD0_CLOCK_CONTROL register using 8-bit Divided Clock mode.

Table 12-239. Host Controller Setup Sequence (continued)

Step	Description
5	Set Version 3 parameters. The MMCSD0_CLOCK_CONTROL register is sets in 10-bit Divided Clock Mode or Programmable Clock Mode. If Clock Multiplier in the MMCSD0_CAPABILITIES register is not zero, Programmable Clock Mode should be used. If Preset Value is used, set Preset Values of SD I/F Modes in the Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10) and set the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit to 1.
6	If Specification Version number (MMCSD0_HOST_CONTROLLER_VER[7-0] SPEC_VER_NUM) is version 4, go to step (7), if it is less than version 4, exits.
7	Set Version 4 parameters. Set the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit to 1. If the MMCSD0_CAPABILITIES[27] ADDR_64BIT_SUPPORT_V4 bit is set to 1, set the MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit to 1. If UHS-II Support is set to 1 and 1.8 V VDD2 Support is set to 1 in the MMCSD0_CAPABILITIES register, set SD Bus Voltage Select for VDD2 to 1.8 V mode in the MMCSD0_POWER_CONTROL register, set preset value for UHS-II Mode to Preset Value register (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10) and set Timeout Counter Value for CMD_RES and Timeout Counter Value for Deadlock in the MMCSD0_UHS2_TIMER_CONTROL register based on Timeout Clock Frequency and Timeout Clock Unit in the MMCSD0_CAPABILITIES register. If Asynchronous Interrupt Support in the MMCSD0_CAPABILITIES register is set to 1, set Asynchronous Interrupt Enable to 1 in the MMCSD0_HOST_CONTROL2 register.

12.4.5.5.2.1.2 Card Interface Detection Sequence

This procedure is invoked by the Card Insertion interrupt. Figure 12-247 and Table 12-240 show a card interface detection sequence.

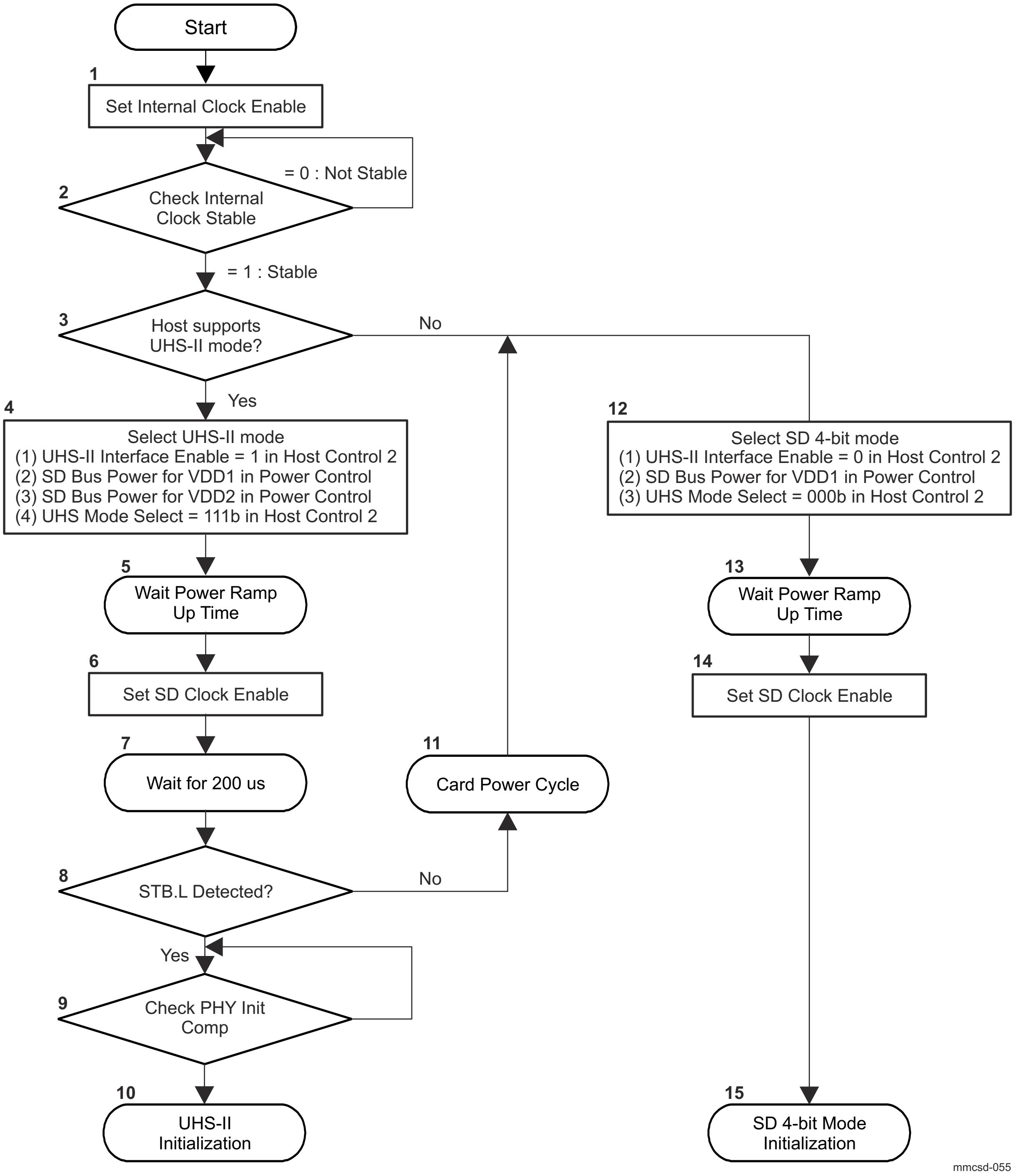


Figure 12-247. Card Interface Detection Sequence

Table 12-240. Card Interface Detection Sequence

Step	Description
1	Set Internal Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
2	Wait until Internal Clock Stable is set to 1 in the MMCSD0_CLOCK_CONTROL register.
3	If Host Supports UHS-II, go to step (4) else go to step (12).
4	Try to initialize a card to UHS-II mode. Set UHS-II Interface Enable to 1 in the MMCSD0_HOST_CONTROL2 register, set SD Bus Power for VDD1 and SD Bus Power for VDD2 to 1 in the MMCSD0_POWER_CONTROL register, and set UHS Mode Select to 111b in the MMCSD0_HOST_CONTROL2 register.
5	Wait power ramp up time. It is dependent on a Host System.

Table 12-240. Card Interface Detection Sequence (continued)

Step	Description
6	Set SD Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
7	Wait 200 µs to check a card supports UHS-II mode.
8	Check STB.L Detection in the MMCSD0_PRESENTSTATE register. If UHS-II IF is detected, go to step (9). If UHS-II IF is not detected, go to step (11).
9	Wait until Lane Synchronization in the MMCSD0_PRESENTSTATE register is set to 1 (PHY Initialization is completed).
10	Perform UHS-II initialization.
11	Perform card power cycle.
12	Try to initialize a card to SD 4-bit mode. Set UHS-II Interface Enable to 0 in the MMCSD0_HOST_CONTROL2 register, set SD Bus Power for VDD1 to 1 in the MMCSD0_POWER_CONTROL register, and set UHS Mode Select to 000b in the MMCSD0_HOST_CONTROL2 register.
13	Wait power ramp up time. It is dependent on a Host System.
14	Set SD Clock Enable to 1 in the MMCSD0_CLOCK_CONTROL register.
15	Perform SD 4-bit mode initialization. Refer to Section 12.4.5.5.1.6, *Card Initialization and Identification (for SD I/F)*.

12.4.5.5.2.2 Boot Operation

The boot operation sequence is shown in Figure 12-248.

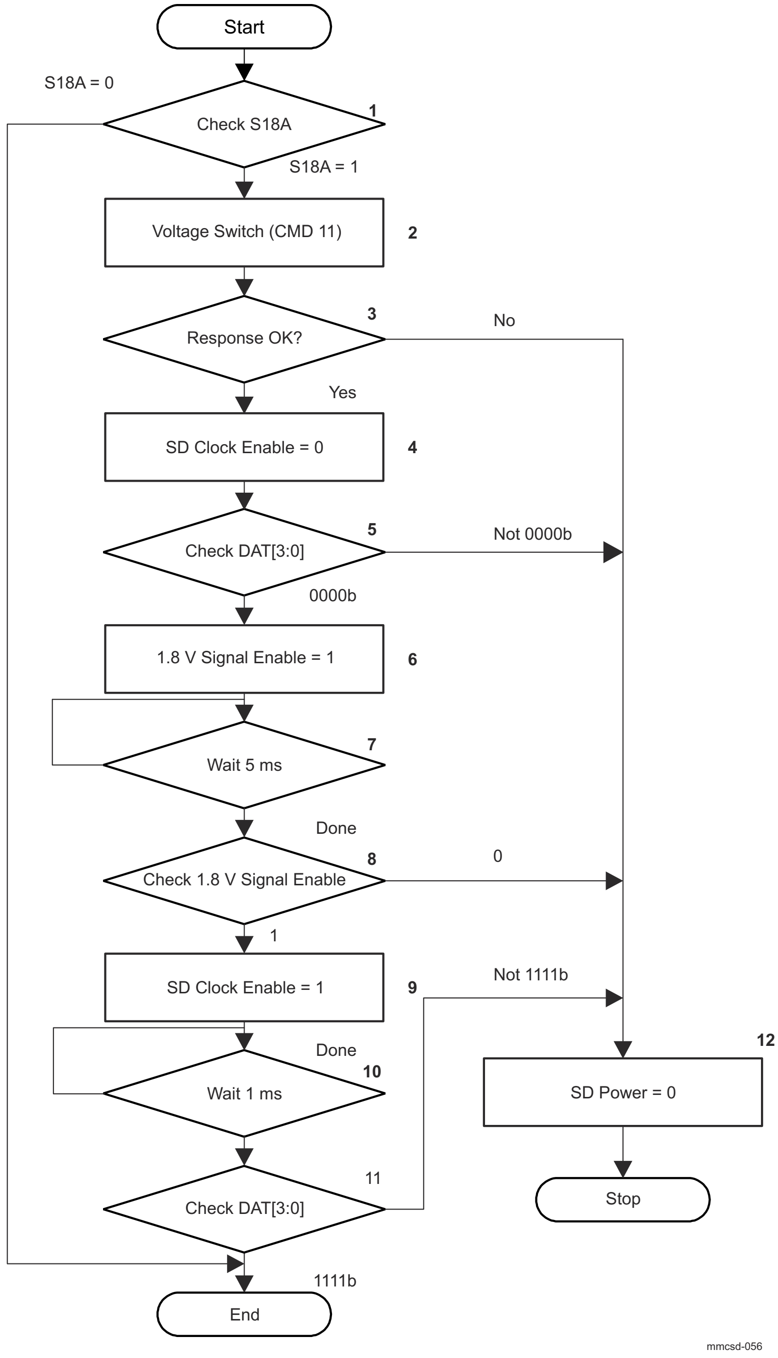


Figure 12-248. Boot Operation Sequence

12.4.5.5.2.2.1 Normal Boot Operation: (For Legacy eMMC 5.0)

The Host driver writes the boot timeout value into MMCSD0_BOOT_TIMEOUT_CONTROL register as per the eMMC4.3+ spec.

When the Host driver sets the "BOOT_ENABLE" to 1 in MMCSD0_BLOCK_GAP_CONTROL register and "DATA_XFER_DIR" bit to "1" in MMCSD0_TRANSFER_MODE register, the Host controller drives the CMD line to "0" for boot operation.

If the Host controller is configured to wait for boot acknowledgement from the eMMC4.3+ device, the controller receives the boot acknowledgement and asserts the "RCV_BOOT_ACK" interrupt to the driver (MMCSD0_NORMAL_INTR_STS[13] RCV_BOOT_ACK). If the Host controller doesn't receive the boot acknowledgement from the device within the timeout value, the Host controller will assert the data timeout error interrupt (MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT).

After servicing the boot acknowledge interrupt or data timeout error interrupt, the driver programs the MMCSD0_BOOT_TIMEOUT_CONTROL register with boot data timeout value.

The eMMC4.3+ device starts sending the boot data on the data line and Host controller sends the same to system whenever a block of data is received from device. The Host controller terminates the boot operation when the programmed number of blocks is transferred to the System. The Driver can writes "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register.

The boot operation can also be terminated in between the boot transfer (the Driver can set the "BOOT_ENABLE" as "0" anytime to disable the boot operation). After the boot termination, the Host controller asserts soft reset for CMD line and DATA line internally once the driver clears the BOOT_COMPLETE interrupt (MMCSD0_NORMAL_INTR_STS[14] BOOT_COMPLETE), to reset all the state machines to idle state.

There is no need to perform error recovery sequence in case data timeout interrupt occurs during boot operation (ignore sending abort command, soft reset and just clear the timeout interrupt and proceed with the boot flow).

If the device sends wrong acknowledgement to the Host, the Host controller will assert Data CRC Error interrupt (MMCSD0_ERROR_INTR_STS[5] DATA_CRC) on the Driver. In this case, the Host driver has to stop the boot mode operation by setting "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

If the device sends end bit as "0" in acknowledgement to the Host, the Host controller will assert Data End Bit Error interrupt (MMCSD0_ERROR_INTR_STS[6] DATA_ENDBIT) on the Driver.

The Host driver stops the boot mode operation by setting "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

Note: Enable the MMCSD0_BLOCK_GAP_CONTROL[7] BOOT_ACK_ENA bit during boot operation. If failed, the controller will not wait for boot acknowledge from the card and send out data CRC error when the card sends boot acknowledgement first and followed by boot data.

12.4.5.5.2.2.2 Alternate Boot Operation (For Legacy eMMC 5.0):

The Host driver writes the boot timeout value as per the eMMC4.3+ spec into MMCSD0_BOOT_TIMEOUT_CONTROL register.

If the "ALT_BOOT_MODE" and "BOOT_ENABLE" is set to 1 in MMCSD0_BLOCK_GAP_CONTROL register and "DATA_XFER_DIR" bit is set to 1 in MMCSD0_TRANSFER_MODE register, the host controller drives the CMD0 (0xFFFFFFFA) on the CMD line.

The system shall wait for command complete interrupt before "RCV_BOOT_ACK" interrupt (MMCSD0_NORMAL_INTR_STS[13] RCV_BOOT_ACK).

If the Host controller is configured to wait for boot acknowledgement from the eMMC4.3+ device, the controller receives the boot acknowledgement and asserts the "RCV_BOOT_ACK" interrupt to the driver.

The eMMC4.3+ device starts sending the boot data on the data line and Host controller sends the same to system whenever a block of data is received from device. The System needs to send CMD0 to inform the device about the boot operation complete. The system shall program MMCSD0_COMMAND register with argument "00000000h" for the CMD0 and waits for command complete.

The Host controller terminates the boot operation when the programmed number of blocks are transferred to the System and the Driver shall send CMD0 to eMMC card and then program "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register.

The boot operation can be terminated at any time (the Driver can send CMD0 and set the "BOOT_ENABLE" as "0" anytime to disable the boot operation). After the boot termination, all state machines in the Host controller need to move to IDLE state. The Host controller asserts the soft reset for CMD and data line internally when the driver clears the BOOT_COMPLETE interrupt (MMCSD0_NORMAL_INTR_STS[14] BOOT_COMPLETE) and all the state machine goes to the idle state.

If the Host controller doesn't receive the acknowledgement from the device with in timeout value the Host controller will assert the data timeout error interrupt (MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT).

The driver programs the MMCSD0_BOOT_TIMEOUT_CONTROL register with boot data timeout value.

There is no need to perform error recovery sequence in case of data timeout interrupt as mentioned above. If the device sends wrong acknowledgement to the Host, then Host controller will assert Data CRC Error interrupt to the Driver (MMCSD0_ERROR_INTR_STS[5] DATA_CRC). The Host driver has to stop the boot mode operation by setting "ALT_BOOT_MODE" and "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

If the device sends end bit as "0" in acknowledgement to the Host, the Host controller asserts Data End Bit Error interrupt (MMCSD0_ERROR_INTR_STS[6] DATA_ENDBIT) on the Driver. The Host driver stops the boot mode operation by setting "ALT_BOOT_MODE" and "BOOT_ENABLE" as "0" in MMCSD0_BLOCK_GAP_CONTROL register and write soft reset for CMD and data line.

Note: Enable the MMCSD0_BLOCK_GAP_CONTROL[7] BOOT_ACK_ENA bit during boot operation . If failed, the controller will not wait for boot acknowledge from the card and send out data CRC error when the card sends boot acknowledgement first and followed by boot data.

12.4.5.5.2.2.3 Boot Code Chunk Read Operation (For Legacy eMMC 5.0):

The following figure explains the boot code read done as chunks of data (the Driver can read the boot data as 2K, 4K, 1K and 8K etc. instead of 128K at a time

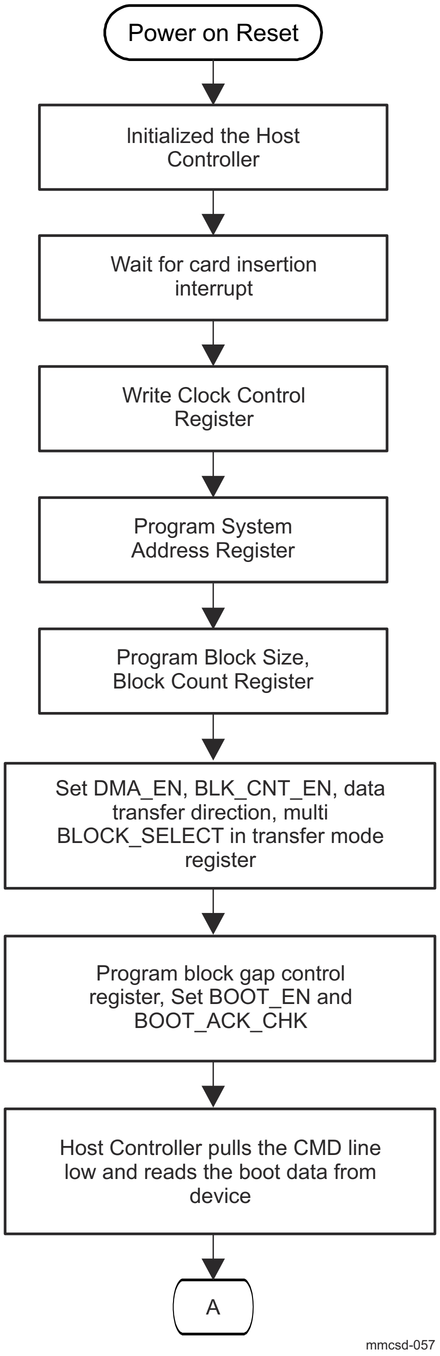


Figure 12-249. Boot Code Access Flow Diagram (1)

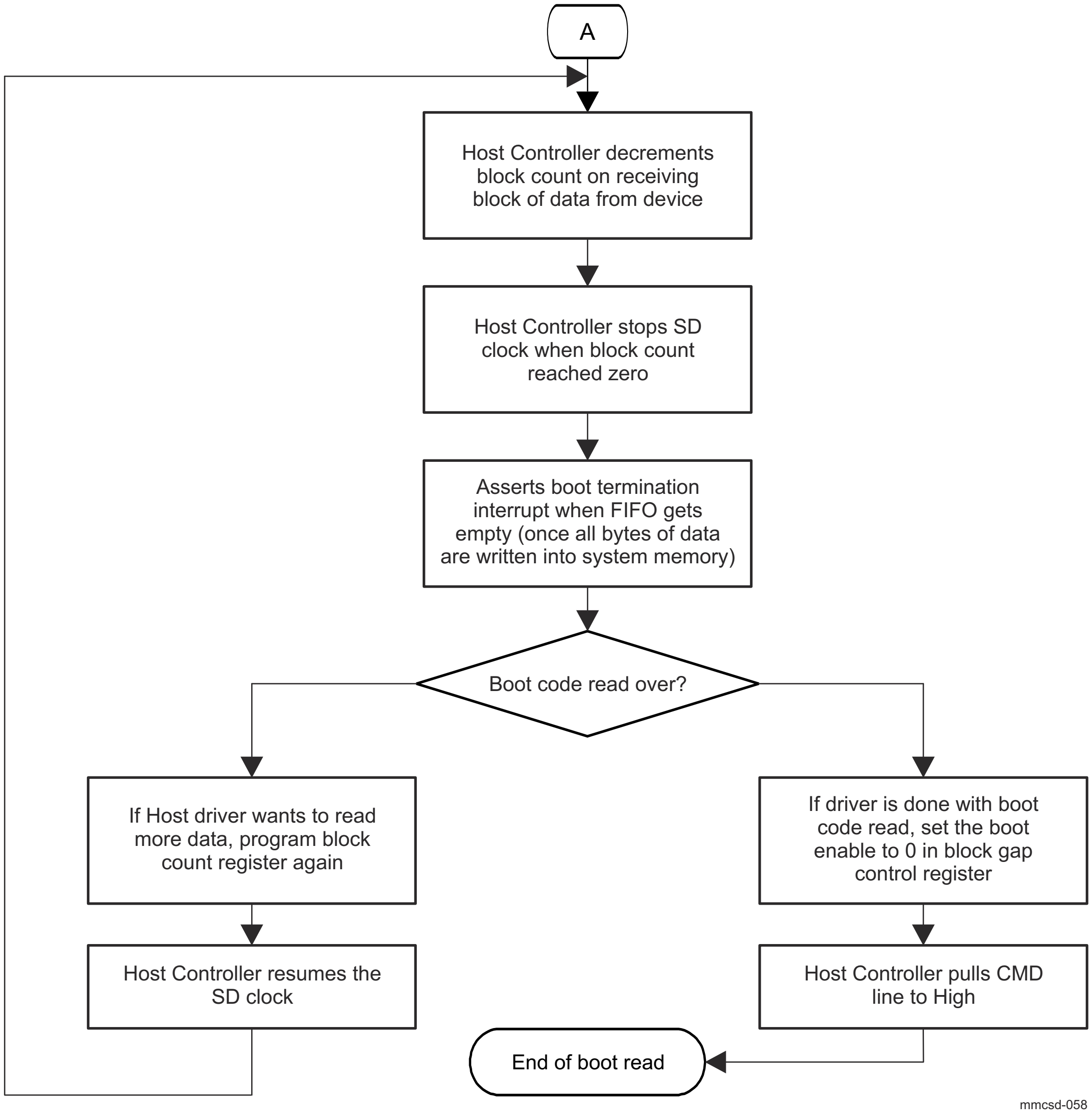


Figure 12-250. Boot Code Access Flow Diagram (2)

12.4.5.5.2.3 Retuning procedure (For Legacy Interface)

12.4.5.5.2.3.1 Sampling Clock Tuning

The SD bus can be operating in high clock frequency mode and then the data window from the card on CMD and DAT[3:0] lines gets smaller. The position of the data window will vary depending on the card and host system implementation. Therefore, the Host Controller shall support a tuning circuit when SDR104 or SDR50.

The Host Controller shall support a tuning circuit when SDR104 or SDR50 (if Use Tuning for SDR50 is set to 1 in the MMCSD0_CAPABILITIES register) is supported by executing the tuning procedure and adjusting the sampling clock. Execute Tuning and Sampling Clock Select in the MMCSD0_HOST_CONTROL2 register are used to control the tuning circuit.

See MMC SW Tuning Algorithm for more information.

12.4.5.5.2.3.2 Tuning Sequence

The Figure 12-251 defines sampling clock tuning procedure supported by Host Controller. In default, for lower frequency operation, fixed sampling clock is used to receive signals on CMD and DAT[3:0]. Before using SDR104, sampling clock tuning is required. Start of sampling clock tuning is requested by setting Execute Tuning to 1 and Sampling Clock Select to 0.

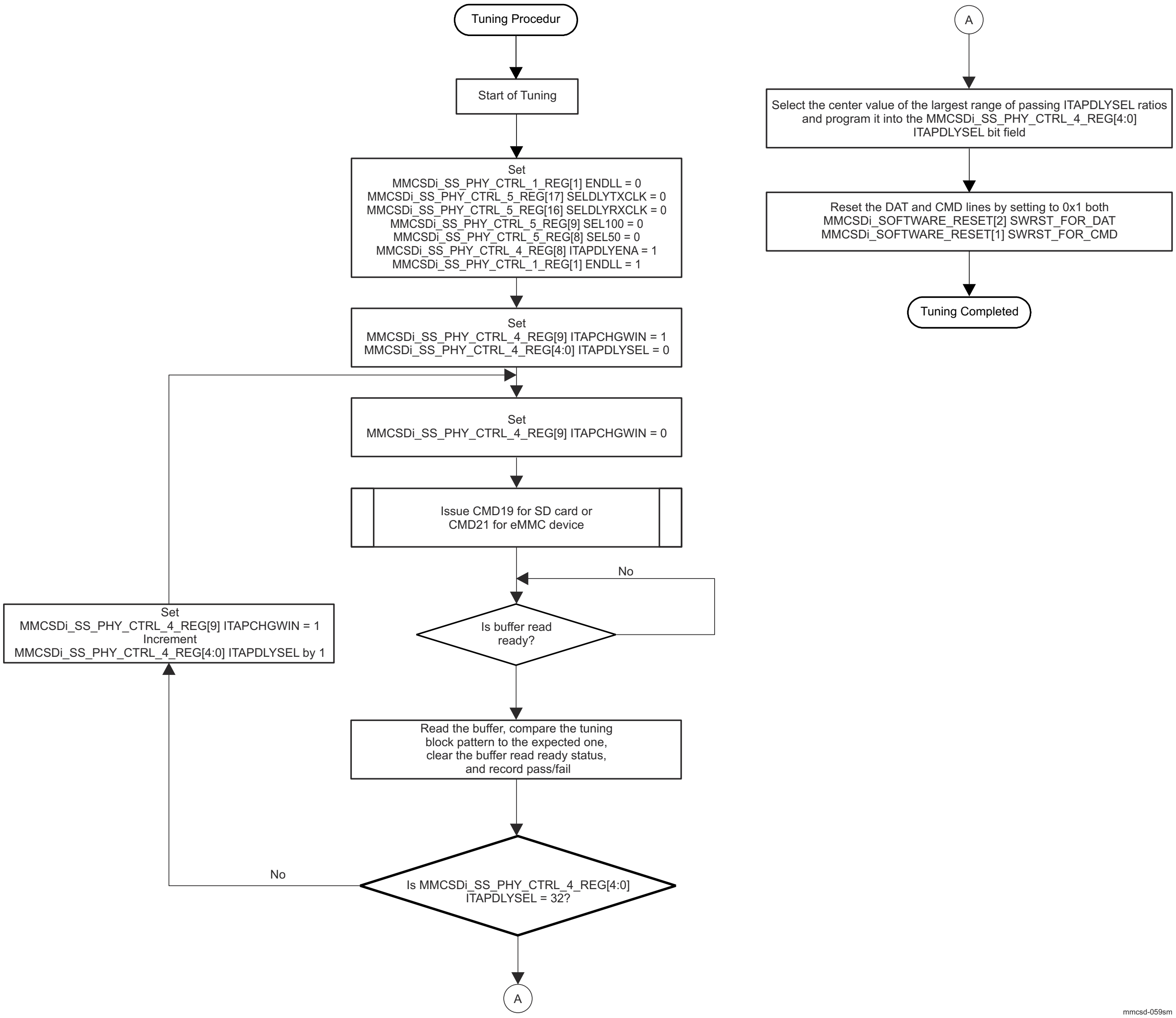


Figure 12-251. MMCSD Clock Tuning

Host driver issue CMD19 repeatedly until the host controller resets Execute Tuning to 0. Host Controller resets Execute Tuning to 0 when tuning is completed or tuning is not completed within 40 times. Host Driver can abort this loop by 40 times CMD19 issue or 150 ms time-out.

If tuning is completed successfully, Host Controller set Sampling Clock Select to 1 and this means the Host Controller start to use tuned sampling clock. If tuning is failed, Host Controller keeps Sampling Clock Select to 0. By writing Sampling Clock Select to 0, sampling clock is switched from tuned sampling clock to fixed sampling clock. Re-tuning time would be smaller than the first tuning time. CMD19 response errors are not indicated while tuning is performed.

The clock tuning tap delay values are selected using Variable sampling point detection. Fixed tap delay value is used for fixed tuning clock method.

12.4.5.5.2.3.3 Re-Tuning Modes

The re-tuning timing is specified by two methods: Re-Tuning Request generated by Host Controller and expiration of a re-tuning timer prepared by Host Driver.

(1) Re-Tuning Mode 1 The host controller does not have any internal logic to detect when the re-tuning needs to be performed. In this case, the Host Driver should maintain all re-tuning timings by using a Re-Tuning Timer. To

enable inserting the re-tuning procedure during data transfers, the data length per read/write command shall be limited up to 4 MB.

(2) Re-Tuning Mode 2 The host controller has the capability to indicate the re-tuning timing by Re-Tuning Request during data transfers. Then the data length per read/write command shall be limited up to 4 MB. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled.

12.4.5.5.2.4 Command Queuing Driver Flow Sequence

12.4.5.5.2.4.1 Command Queuing Initialization Sequence

Figure 12-252 and Table 12-241 show a Command Queuing initialization sequence.

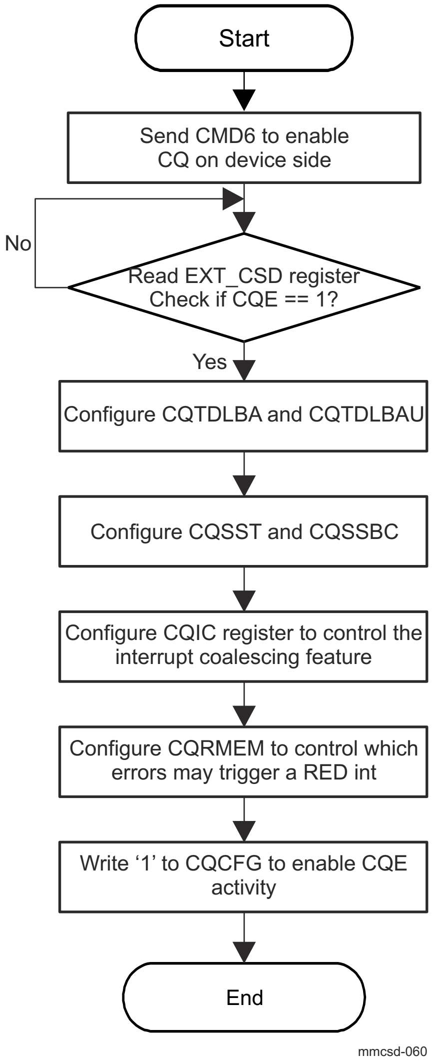


Figure 12-252. Command Queuing Initialization Sequence

Table 12-241. Command Queuing Initialization Sequence

Step	Description
1	Initialize and enable Command Queueing in the device.
2	Configure Task Descriptor size in MMCSD0_CQ_CONFIG register.
3	Configure MMCSD0_CQ_TDL_BASE_ADDR and MMCSD0_CQ_TDL_BASE_ADDR_UPBITS registers to point to the memory location allocated to the TDL in host memory.
4	Configure CQSST and CQSSBC to control when SEND_QUEUE_STATUS commands are sent to the device by CQE.
5	Configure MMCSD0_CQ_INTR_COALESCING register to control the interrupt coalescing feature: enable/disable, set interrupt count and timer protection.

Table 12-241. Command Queuing Initialization Sequence (continued)

Step	Description
6	Configure MMCSD0_CQ_RESP_ERR_MASK register to control which errors may trigger a RED interrupt (if different from reset values).
7	Write '1' to MMCSD0_CQ_CONFIG register to enable CQE activity.

12.4.5.5.2.4.2 Task Issuance Sequence

Figure 12-253 and Table 12-242 show a task issuance sequence.

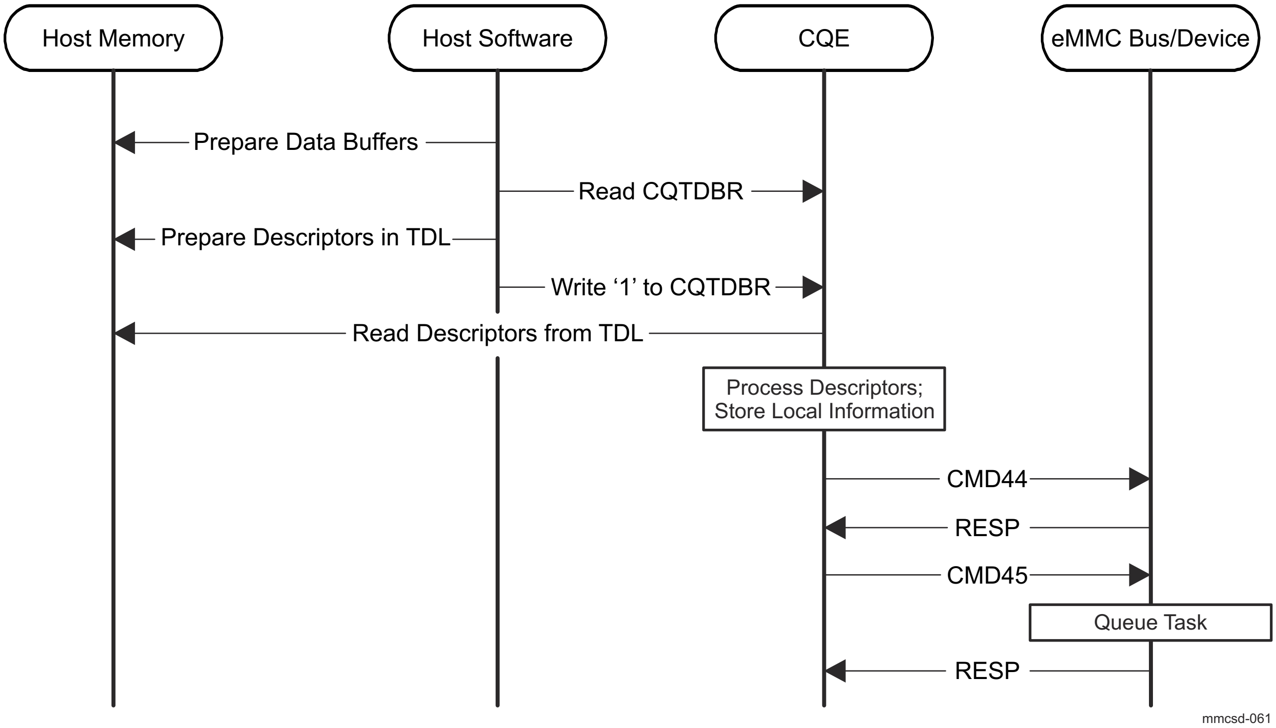


Figure 12-253. Task Issuance Sequence

Table 12-242. Task Issuance Sequence

Step	Description
1	Find an empty transfer request slot by reading the MMCSD0_CQ_TASK_DOOR_BELL register. An empty transfer request slot has its respective bit cleared to '0' in the MMCSD0_CQ_TASK_DOOR_BELL register.
2	Build a Task Descriptor at the 1st entry of the empty slot. Task Descriptor field values: • 1. Valid = 1, to indicate the descriptor is effective. • 2. End = 1, as required for Task Descriptors. • 3. Int = 1, if an interrupt on completion is required. Otherwise, Int = 0. • 4. Act = b101, to indicate a Task Descriptor . • 5. Data Direction = 1 for read commands, and 0 for write commands. • 6. Priority = 1 for high priority, and 0 for simple requests. • 7. QBR = 1 if Queue Barrier functionality is required. 0 otherwise. • 8. Forced Programming, Context ID, Tag Request, Reliable Write, Block Count, and Block Address programmed according to application requirements.
3	Build a Transfer Descriptor at the 2nd entry of the empty slot. Transfer Descriptor field values: • 1. Valid = 1, to indicate the descriptor is effective. • 2. End = 1, if a TRAN descriptor is used, to indicate the task only has one data buffer. End = 0 if LINK descriptor is used. • 3. Int = 0. Ignore in Command queueing. • 4. Act = b100, for TRAN descriptors, pointing directly to the task's single data buffer. Act = 401 b110, for LINK descriptors, point to a scatter/gather list (indirect). • 5. Address and Length programmed according to the data buffer supplied by the application.

Table 12-242. Task Issuance Sequence (continued)

Step	Description
4	If more than one transfer is requested, repeat step 1-3 for all needed transfers.
5	Set MMCSD0_CQ_TASK_DOOR_BELL register to indicate to the CQE that one or more transfer requests are ready to be sent to the attached device. Host software shall only write a '1' to the bit position that corresponds to new tasks; all other bit positions within MMCSD0_CQ_TASK_DOOR_BELL register should be written with a '0', which indicates no change to their current values.

12.4.5.5.2.4.3 Task Execution and Completion Sequence

The CQE is responsible for task execution, communication with the device and moving the data to the buffers in the host memory.

Figure 12-254 and Table 12-243 show a task execution and completion sequence.

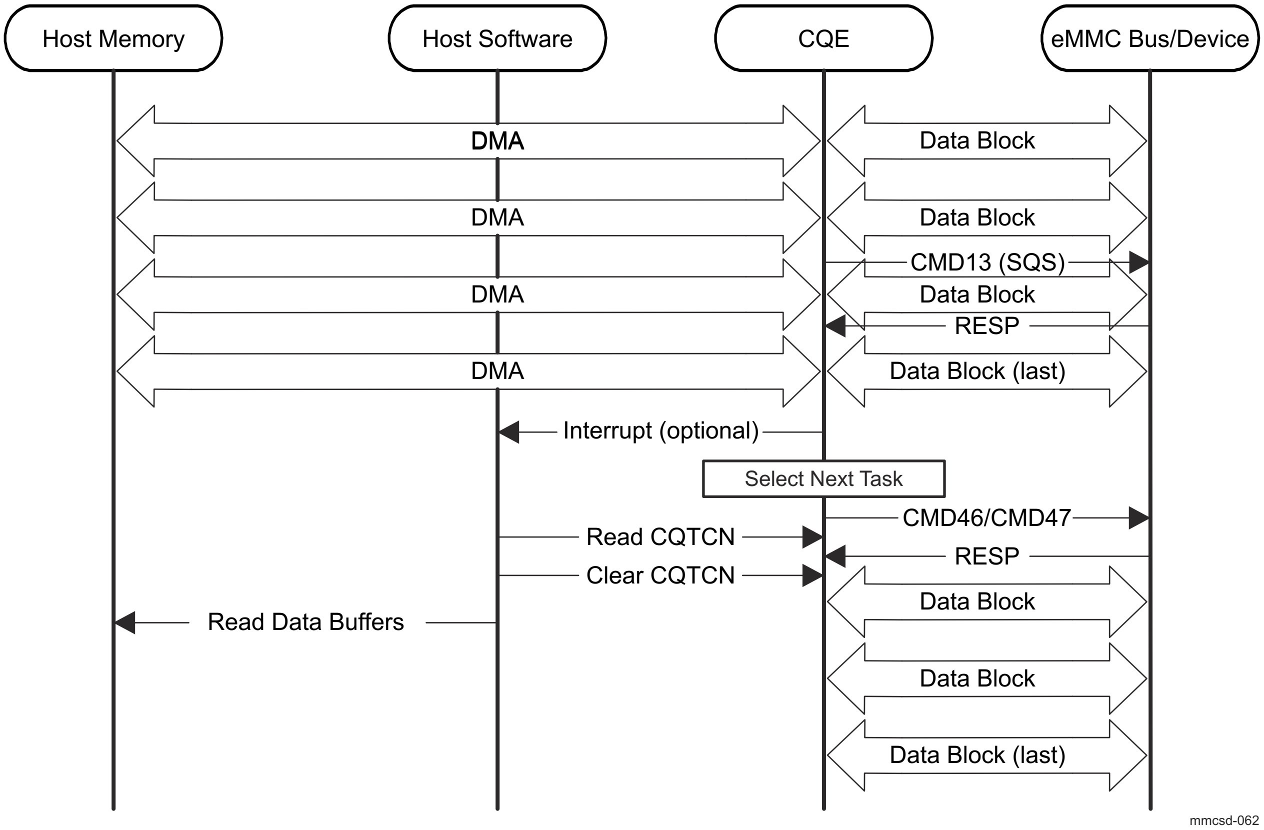


Figure 12-254. Task Execution and Completion Sequence

Table 12-243. Task Execution and Completion Sequence

Step	Description
1	Once the tasks are queued on the device side CQE sends CMD13 to determine the queue status. The queue status lets the CQE know which tasks are ready for execution.
2	The response to CMD13 may indicate no task is ready in which case the CQE is required to send CMD13 again at a later time as controlled CQSST register.
3	If a task is ready for execution then the host sends EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) to the device with the task id ordering it to execute a task.
4	When the task execution is completed, an interrupt may be generated, if requested, or as determined by Interrupt Coalescing mechanism.
5	The host software reads MMCSD0_CQ_TASK_COMP_NOTIF register to determine which task(s) has(have) been completed. Each bit set in MMCSD0_CQ_TASK_COMP_NOTIF register represents by index which task has completed but hasn't yet been served by software.
6	For every task completed clear the appropriate MMCSD0_CQ_TASK_COMP_NOTIF register bit.
7	Repeat steps 1-6 for the pending tasks.

12.4.5.5.2.4.4 Task Discard and Clear Sequence

Figure 12-255 and Table 12-244 show a task discard and clear sequence.

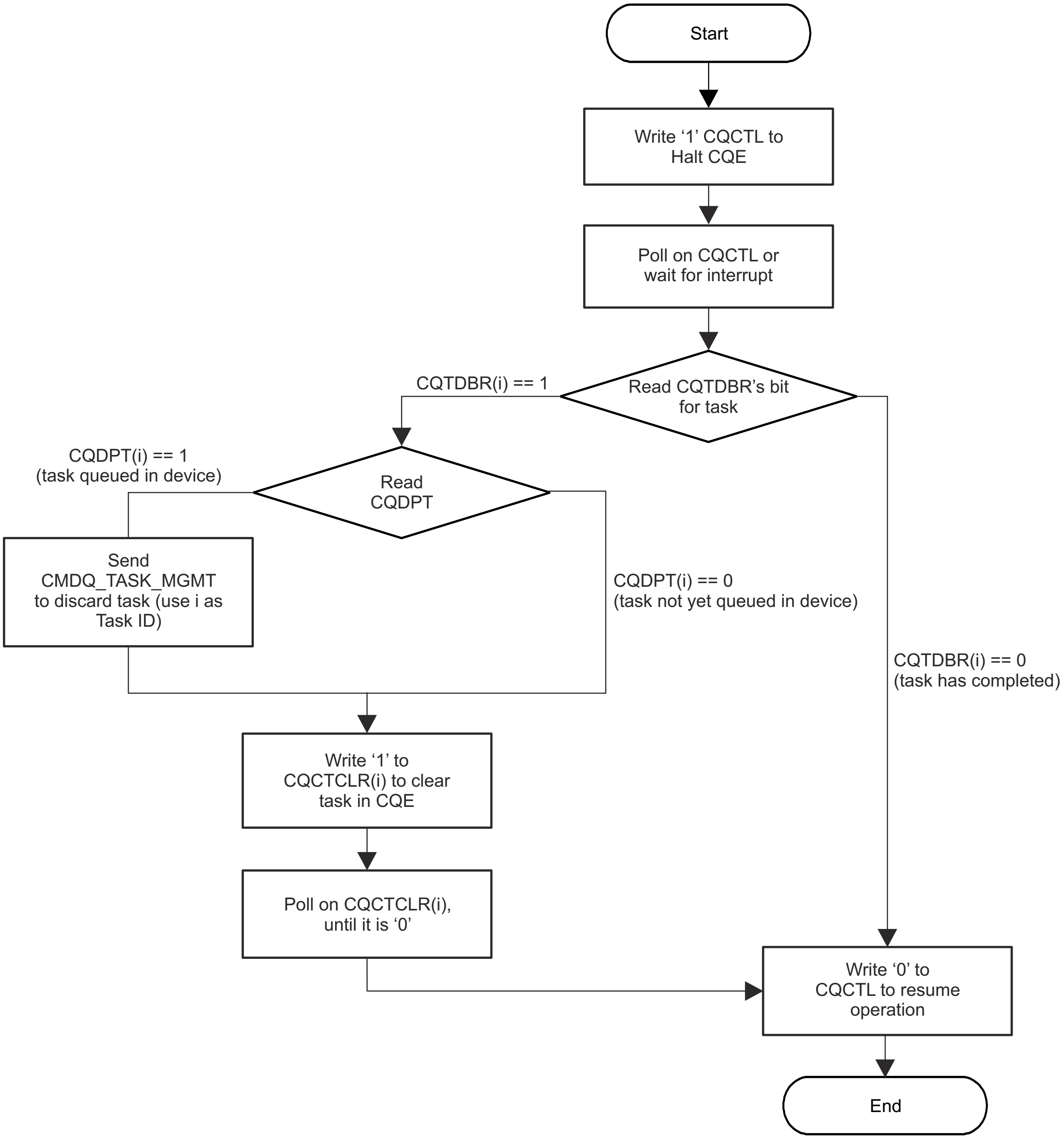


Figure 12-255. Task Discard and Clear Sequence

Table 12-244. Task Discard and Clear Sequence

Step	Description
1	While CQE is enabled write '1' to MMCSD0_CQ_CONTROL[0] HALT_BIT bit to halt CQE.
2	Poll on MMCSD0_CQ_INTR_STS[0] HALT_COMPLETE bit.
3	Read MMCSD0_CQ_TASK_DOOR_BELL register to determine if the task to be dicarded is set to 1.
4	Read MMCSD0_CQ_DEV_PENDING_TASKS register to check if the task is queued in the device.
5	Send CMDQ_TASK_MGMT(CMD48) to discard task using the task id as the argument.

Table 12-244. Task Discard and Clear Sequence (continued)

Step	Description
6	Write '1' to CQCTCLR[i] to clear task in CQE.
7	Poll on CQCTCLR[i] until it is '0'.
8	Write '0' to MMCSD0_CQ_CONTROL register to resume CQE.

12.4.5.5.2.4.5 Error Detect and Recovery when CQ is enabled

Figure 12-256 and Table 12-245 show an error detect and recovery sequence.

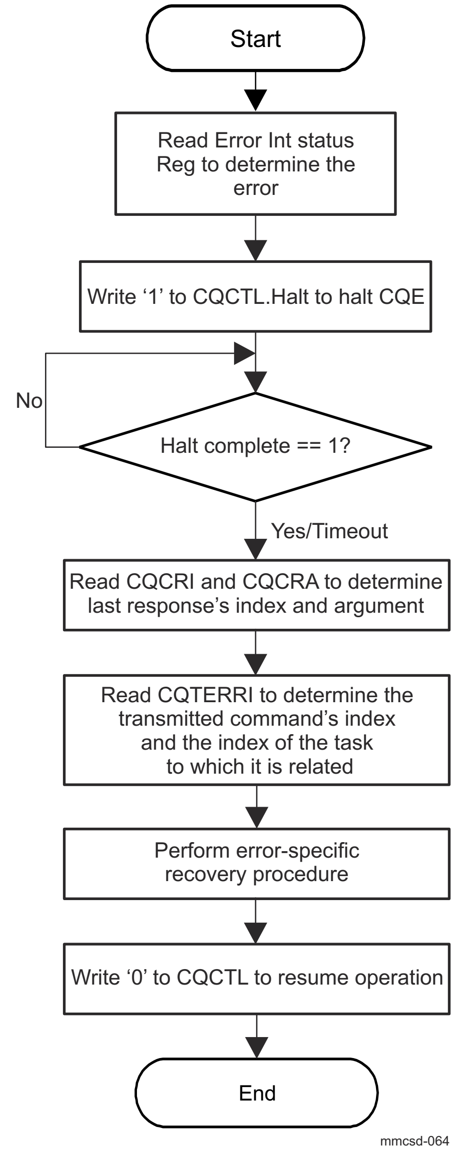


Figure 12-256. Error Detect and Recovery Sequence

Table 12-245. Error Detect and Recovery Sequence

Step	Description
1	Read eMMC host controller MMCSD0_ERROR_INTR_STS register and determine error is related to CQE.
2	Write '1' to MMCSD0_CQ_CONTROL[0] HALT_BIT bit to halt CQE.
3	Wait for MMCSD0_CQ_CONTROL[0] HALT_BIT bit to read '1'. In some error cases, this may not happen, so software should proceed to the next step after a sufficient time-out.
4	Read MMCSD0_CQ_CMD_RESP_INDEX and MMCSD0_CQ_CMD_RESP_ARG registers to determine last response's index and argument.

Table 12-245. Error Detect and Recovery Sequence (continued)

Step	Description
5	Read MMCSD0_CQ_TASK_ERR_INFO register to determine the transmitted command's index and the index of the task to which it is related.
6	Perform error-specific recovery procedure.
7	Write '0' to MMCSD0_CQ_CONTROL register to resume operation.

12.5 Industrial and Control Interfaces

This section describes the industrial and control interfaces in the device.

12.5.1 Modular Controller Area Network (MCAN)

This section describes the Modular Controller Area Network (MCAN) modules in the device.

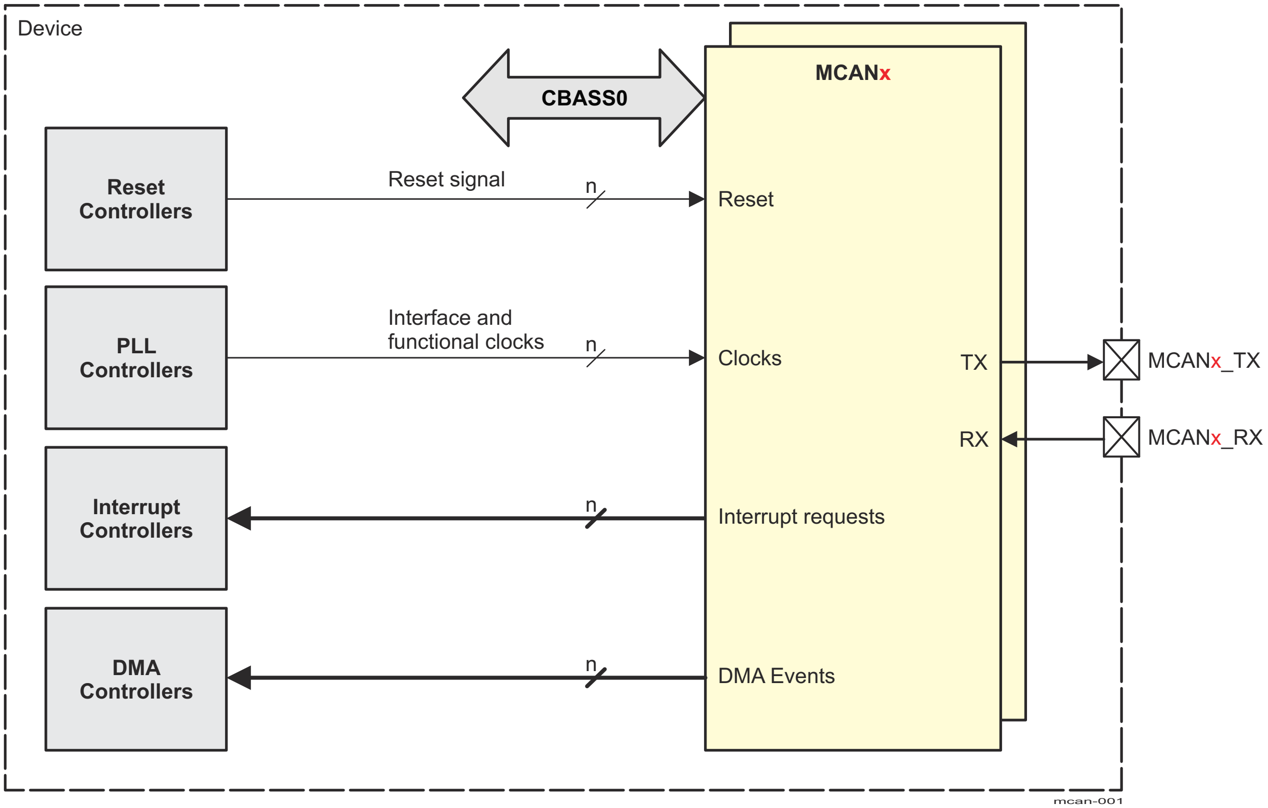
12.5.1.1 MCAN Overview

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control. CAN has high immunity to electrical interference. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

They connect to the physical layer of the CAN network through external (for the device) transceivers. Each MCAN module supports flexible bit rates greater than 1 Mbps and is compliant to ISO 11898-1:2015.

Figure 12-257 shows the MCAN modules overview.



A. x = 0 to number of MCAN in a domain -1

Figure 12-257. MCAN Modules Overview

12.5.1.1.1 MCAN Features

Each MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- SAE J1939 support
- AUTOSAR support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements

- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Internal Loopback mode for self-test
- Maskable interrupts, two interrupt lines
- Two clock domains (CAN clock/Host clock)
- Parity/ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Local power-down and wakeup support
- Timestamp Counter

12.5.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.5.1.2 MCAN Environment

This section describes the MCAN external connections (environment).

CAN network physical layer consists of two-wire differential bus, usually twisted pair, and provides high level of interference immunity. External CAN transceiver IC is needed to access a CAN bus by the MCAN.

Figure 12-258 shows the MCAN typical application.

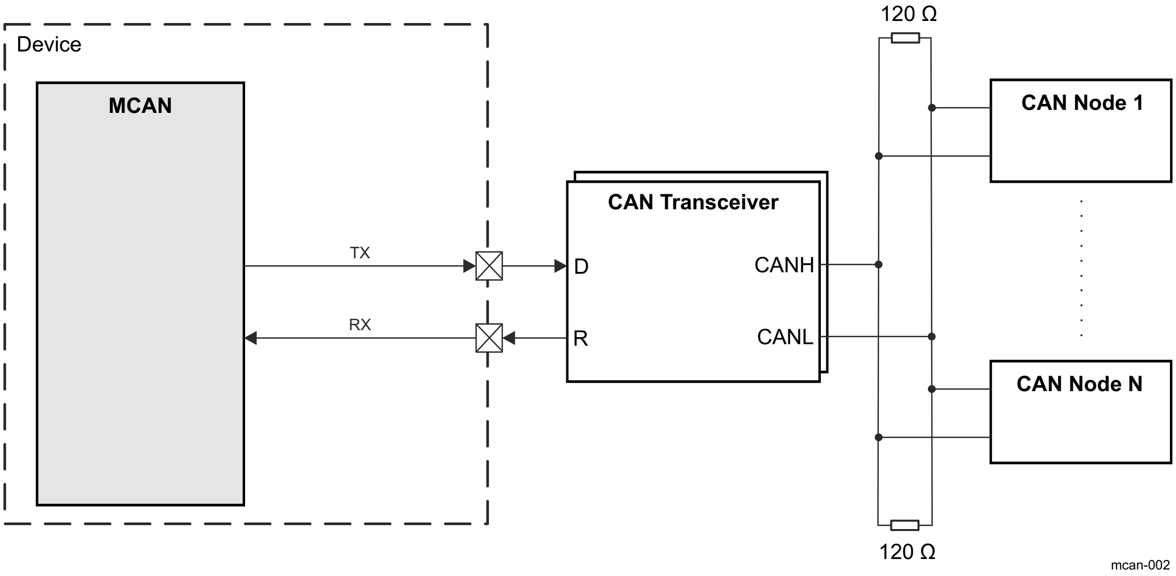


Figure 12-258. MCAN Typical Application

Table 12-246 describes the MCAN I/O signals.

Table 12-246. MCAN I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(1)
		MCANi(2)		
RX	MCANi(2)_RX	I	Serial data input from external CAN transceiver	HiZ
TX	MCANi(2)_TX	O	Serial data output to external CAN transceiver	1

(1) I = Input; O = Output; HiZ = High Impedance
(2) i represents an MCAN instance. See the device datasheet for available domains and MCAN instances.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.5.1.2.1 CAN Network Basics

- CAN bus is a 2-wire differential bus using Non-Return-to-Zero (NRZ) encoding and has two states:
  - Recessive state (logical 1)
  - Dominant state (logical 0)
- The network is multicontroller. When two or more nodes (ECUs) attempt to transmit at the same time, a non-destructive arbitration technique guarantees messages are sent in order of priority and no messages are lost.
- The message transmission is multicast. Data messages transmitted are identifier based, not address based.
- Content of message is labeled by the identifier that is unique throughout the network (for example: rpm, temperature, position, pressure, and so forth).
- All nodes on network receive the message and each performs an acceptance test on the identifier. If message is relevant, it is processed, otherwise it is ignored.
- The unique identifier also determines the priority of the message (the lower the numerical value of the identifier, the higher the priority is).
- Data is transmitted and received using message frames, consisting of the following basic fields:
  - Arbitration field
  - Control field
  - Data field (up to 8 bytes for Classical CAN and up to 64 bytes for CAN FD)
  - CRC field
  - ACK field

For more information, see *ISO 11898-1:2015: CAN data link layer and physical signaling*.

12.5.1.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.5.1.4 MCAN Functional Description

The MCAN module performs CAN protocol communication according to ISO 11898-1:2015. The bit rate can be programmed to values greater than 1 Mbps. Additional transceiver hardware is required for the connection to the physical layer (CAN bus).

For communication on a CAN network, individual message frames can be configured. The message frames and identifier masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the Message Handler.

The register set of the MCAN module can be accessed directly via the module interface. These registers are used to control and configure the CAN core and the Message Handler, and to access the Message RAM.

Figure 12-259 shows the MCAN module block diagram.

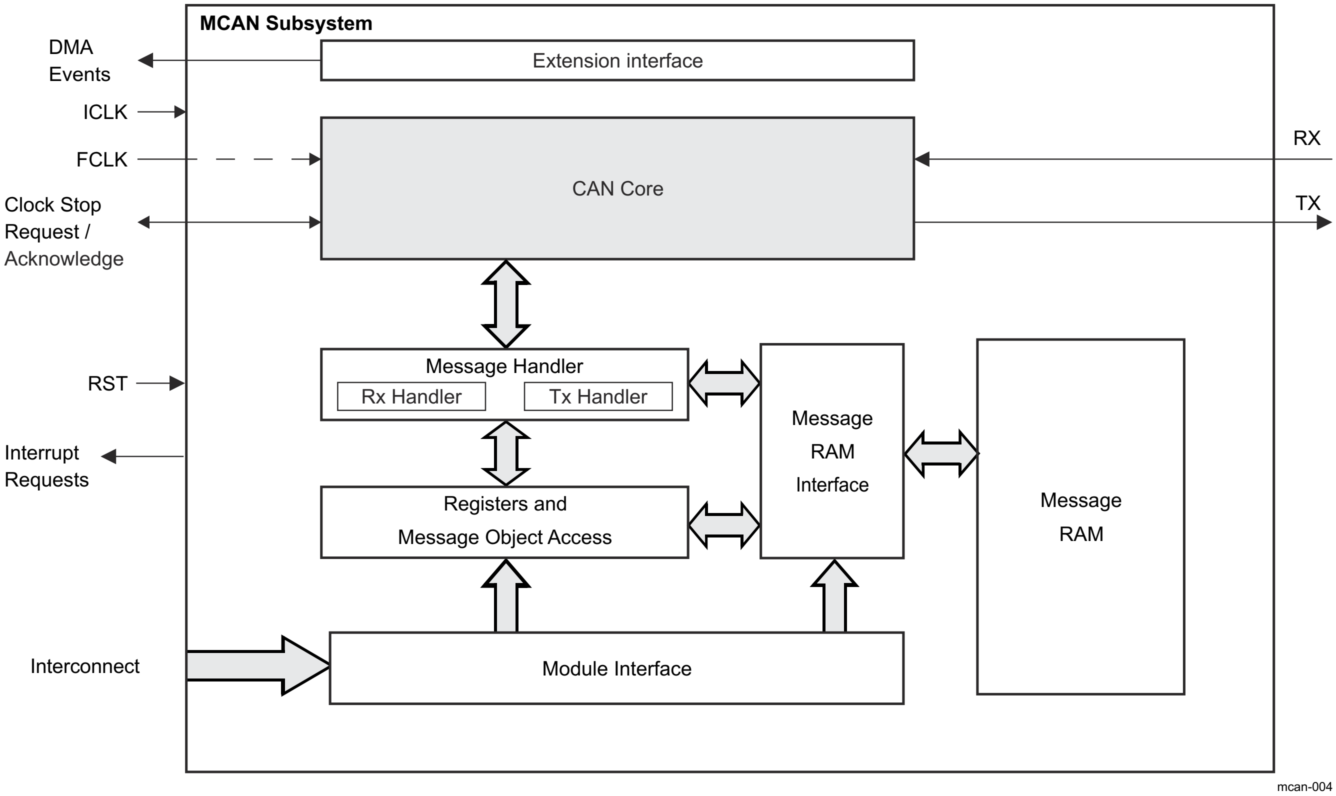


Figure 12-259. MCAN Block Diagram

The MCAN module blocks description:

- **CAN Core**: the CAN core consists of the CAN protocol controller and the Rx/Tx shift register. It handles all ISO 11898-1:2015 protocol functions and supports 11-bit and 29-bit identifiers.
- **Message Handler**: the Message Handler (Rx Handler and Tx Handler) is a state machine that controls the data transfer between the single-ported Message RAM and the CAN core's Rx/Tx shift register. It also handles the acceptance filtering and the Interrupt/DMA request generation as programmed in the control registers.
- **Message RAM**: the main purpose of the Message RAM is to store Rx/Tx messages, Tx Event elements, and Message ID Filter elements (for more information, see Section 12.5.1.4.10, *Message RAM*).
- **Message RAM Interface**: enables connection between the Message RAM and the other blocks in the MCAN module.
- **Registers and Message Object Access**: data consistency is ensured by indirect accesses to the message objects. The interface registers have the same word-length as the Message RAM.
- **Module Interface**: provides connection to the Registers and Message Object Access block and Message RAM Interface block

- **Clocking**: two clocks are provided to the MCAN module: the peripheral synchronous clock (interface clock ICLK) and the peripheral asynchronous clock (functional clock - FCLK). For more information, see *Module Integration*.
- **Extension Interface**: this interface is used for DMA requests signaling (see Section 12.5.1.4.2.2).

12.5.1.4.1 Module Clocking Requirements

Two clocks are provided to the MCAN module:

- the peripheral synchronous clock (ICLK) as the general module clock source
- and the peripheral asynchronous clock (FCLK) provided to the CAN core for generating the CAN bit timing.

Within the MCAN module there is a synchronization mechanism implemented to ensure safe data transfer between the two clock domains. There is synchronization between the signals from the Host clock domain to the CAN clock domain and vice versa and between the reset signal to the Host clock domain and to the CAN clock domain.

Note

ICLK must always be higher or equal to FCLK, in order to achieve a stable functionality of the MCAN module. Here, also the frequency shift of the modulated ICLK has to be considered:

$f_{0,\mathrm{ICLK}} \pm \Delta f_{\mathrm{FM,ICLK}} \geq f_{\mathrm{FCLK}}$

For more information on how to configure the relevant clock source registers, see *Clocking* and the device-specific Datasheet.

12.5.1.4.2 Interrupt and DMA Requests

The MCAN module provides interrupt and DMA requests. They are configured via the Host CPU. The Suspend Mode is requesting or forcing (based on MCANSS_CTRL[3] DBGSUSP_FREE bit) the MCAN module to go into initialization mode (see MCAN_CCCR[0] INIT bit) in which new interrupts and DMA requests will not be issued, that is to prevents the interrupt and DMA requests from propagating to the Host CPU (for more information, see Section 12.5.1.4.3.8.2, *Suspend Mode*).

12.5.1.4.2.1 Interrupt Requests

The MCAN module has two interrupt lines. There are 30 internal interrupt sources. Each source can be configured to drive one of the two interrupt lines. The interrupts are 'level high' interrupts.

The MCAN core provides two interrupt requests (for Line 0 and Line 1).

For more information, see the following registers:

- Interrupt Register (MCAN_IR)
- Interrupt Enable (MCAN_IE)
- Interrupt Line Select (MCAN_ILS)
- Interrupt Line Enable (MCAN_ILE)

The MCAN module is capable of issuing ECC interrupts. After clearing the ECC interrupt source, the application software must also write 1 to EOI register (MCANSS_ECC_SEC_EOI_REG/MCANSS_ECC_DED_EOI_REG). For more information, see *ECC Aggregator*.

The MCAN module supports External Timestamp Counter. When the External Timestamp Counter rolls over it produces an interrupt (see Section 12.5.1.4.4.1, *External Timestamp Counter*).

For more information, see the following registers:

- Interrupt Clear Shadow Register (MCANSS_ICS)
- Interrupt Raw Status Register (MCANSS_IRS)
- Interrupt Enable Clear Shadow Register (MCANSS_IECS)
- Interrupt Enable Register (MCANSS_IE)
- Interrupt Enable Status Register (MCANSS_IES)
- End Of Interrupt Register (MCANSS_EOI)
- External Timestamp Prescaler Register (MCANSS_EXT_TS_PRESCALER)

- External Timestamp Unserviced Interrupts Counter Register (MCANSS_EXT_TS_UNSERVICED_INTR_CNTR)

For more information about available Interrupt Requests, see *MCAN Hardware Requests*.

12.5.1.4.2.2 DMA Requests

Functional transmit and Filter DMA requests are generated by the MCAN module based on the signaling in the Extension Interface. The DMA signaling uses a simple DMA request active high pulse.

The active high pulse indicates a pending message is transmitted (see MCAN_TXBRP). This pulse can be used to transfer another message to the Tx Buffer, which would need to be followed by writing 1 to the corresponding MCAN_TXBAR[0] AR bit to mark a new Tx message pending transmission.

The Parity on Tx DMA Events is available using an EDC Controller which can be accessed through the ECC Aggregator.

Standard and Extended message filters can be set to issue a pulse when a filter match occurs. These 'Filter Events' can be used to DMA messages from the Rx FIFO. The events are high level single clock cycle pulses (ICLK).

12.5.1.4.3 Operating Modes

12.5.1.4.3.1 Software Initialization

Setting the MCAN_CCCR[0] INIT bit to 1 starts a software initialization. This is done either by software or by a hardware reset, when an uncorrected bit error was detected in the Message RAM, or by going Bus_Off state. While the MCAN_CCCR[0] INIT bit is set, the message transfer is stopped and the status of the output TX pin is recessive (high). The counters of the Error Management Logic (EML) are unchanged. Setting the MCAN_CCCR[0] INIT bit does not change any configuration register. Resetting the MCAN_CCCR[0] INIT bit finishes the software initialization. After waiting for the occurrence of a sequence of 11 consecutive recessive bits (indication for Bus_Idle state) the message transfer starts.

Access to the MCAN configuration registers is only enabled when both MCAN_CCCR[0] INIT and MCAN_CCCR[1] CCE bits are set (write protection).

The MCAN_CCCR[1] CCE bit can only be set/reset while the MCAN_CCCR[0] INIT = 1. The MCAN_CCCR[1] CCE bit is automatically reset when the MCAN_CCCR[0] INIT bit is reset.

The following registers are reset when the MCAN_CCCR[1] CCE bit is set:

- MCAN_HPMS - High Priority Message Status
- MCAN_RXF0S - Rx FIFO 0 Status
- MCAN_RXF1S - Rx FIFO 1 Status
- MCAN_TXFQS - Tx FIFO/Queue Status
- MCAN_TXBRP - Tx Buffer Request Pending
- MCAN_TXBTO - Tx Buffer Transmission Occurred
- MCAN_TXBCF - Tx Buffer Cancellation Finished
- MCAN_TXEFS - Tx Event FIFO Status

The Timeout Counter value MCAN_TOCV[15-0] TOC field is preset to the value configured by the MCAN_TOCC[31-16] TOP field when the MCAN_CCCR[1] CCE bit is set.

In addition the Tx Handler and Rx Handler are held in idle state while MCAN_CCCR[1] CCE = 1.

The following registers are only writeable while MCAN_CCCR[1] CCE = 0

- MCAN_TXBAR - Tx Buffer Add Request
- MCAN_TXBCR - Tx Buffer Cancellation Request

MCAN_CCCR[7] TEST and MCAN_CCCR[5] MON bits can only be set by the Host CPU while MCAN_CCCR[0] INIT = 1 and MCAN_CCCR[1] CCE = 1. Both bits may be reset at any time. The MCAN_CCCR[6] DAR bit can only be set/reset while MCAN_CCCR[0] INIT = 1
and MCAN_CCCR[1] CCE = 1.

Table 12-247 shows the steps to configure the MCAN module.

Table 12-247. Steps to Configure MCAN Module

Step	Operation	Description	Pseudo Code
1	Initialize MCAN_CCCR	Set MCAN_CCCR[0] INIT bit and check that it has been set	INIT = 1; If INIT ≠ 1, wait until it is
2	Unlock protected registers	Set MCAN_CCCR[1] CCE bit	CCE = 1;
3	Configure CAN mode	Set MCAN_CCCR[8] FDOE bit to CAN FD	FDOE = 1 for CAN FD FDOE = 0 for CAN
4	Configure Bit Rate Switching	Set MCAN_CCCR[9] BRSE bit	BRSE = 1 with bit rate switching BRSE = 0 without bit rate switching
5	Set bit timing	Set MCAN_NBTP register	
6	Lock protected registers	Clear MCAN_CCCR[1] CCE bit	CCE = 0;
7	Return MCAN module to normal operation	Clear MCAN_CCCR[0] INIT bit and check it has been cleared	INIT = 0; If INIT ≠ 0, wait until it is

12.5.1.4.3.2 Normal Operation

Once the MCAN module is initialized and the MCAN_CCCR[0] INIT bit is reset to zero, the MCAN module synchronizes itself to the CAN bus and is ready for communication. After passing the acceptance filtering, received messages including Message Identifier (ID) and Data Length Code (DLC) are stored into a dedicated Rx Buffer or into Rx FIFO 0/Rx FIFO 1.

For messages to be transmitted dedicated Tx Buffers and/or a Tx FIFO or a Tx Queue can be initialized or updated.

Note

Automated transmission on reception of remote frames is not supported.

12.5.1.4.3.3 CAN FD Operation

The CAN FD standard allows extended frames to be sent, up to 64 data bytes in a single frame at a higher bit rate for the data phase of a frame, up to 8 Mbps. The CAN FD standard introduces the ability to switch from one bit rate to another. Extended Data Length (EDL), as shown in Figure 12-260, sets a data length of up to 8 or up to 64 data bytes. Bit Rate Switching (BRS) indicates whether two bit rates (the data phase is transmitted at a different bit rate to the arbitration phase) are enabled.

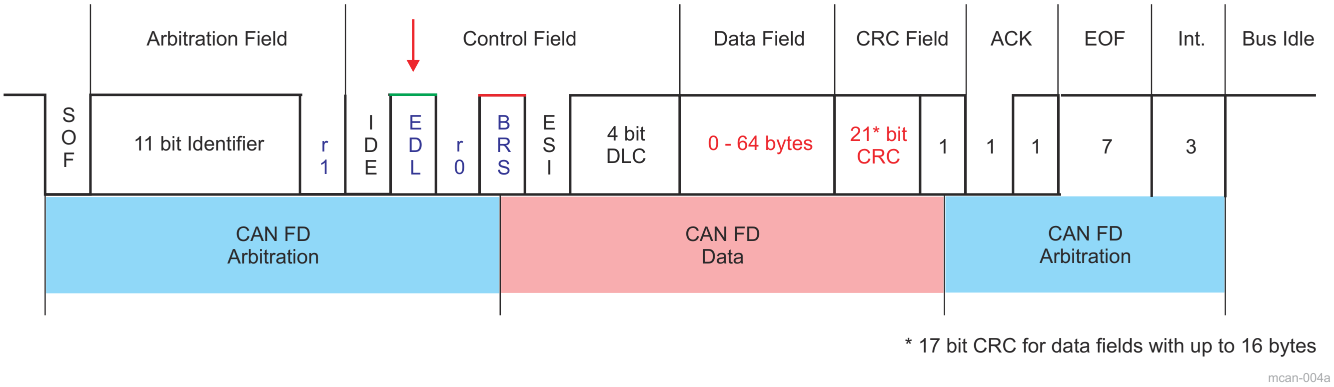


Figure 12-260. CAN FD Frame

Note

Figure 12-260 presents CAN FD frame according to the Non-ISO CAN FD (legacy) protocol. In the new ISO CAN FD protocol the CRC Field includes additional 5 bits (three stuff bit counter (SBC) bits and two parity bits). With these additional bits, a weakness identified in the error detection scheme chosen by the original protocol is removed. By setting MCAN_CCCR[15] NISO bit, the ISO or Non-ISO CAN FD format can be chosen. In CAN network ISO CAN FD and non-ISO CAN FD devices should never mix.

There are two variants of CAN FD frame transmission:

- CAN FD frame transmission without bit rate switching
- CAN FD frame transmission where control field, data field, and CRC field are transmitted with a higher bit rate than the beginning and the end of the frame

In the CAN frames FDF = recessive (logical 1) signifies a CAN FD frame, FDF = dominant (logical 0) signifies a Classic CAN frame. In a CAN FD frame, the two bits following FDF - res and BRS, decide whether the bit rate inside of this CAN FD frame is switched. A CAN FD bit rate switch is signified by res = dominant and BRS = recessive. Note that the coding of res = recessive is reserved for future expansion of the protocol. In case the MCAN module receives a frame with FDF = recessive and res = recessive, it will signal a Protocol Exception Event by setting the MCAN_PSR[14] EXE bit. When Protocol Exception Handling is enabled (MCAN_CCCR[12] PXHD = 0), this causes the operation state to change from Receiver (MCAN_PSR[4-3] ACT = 10) to Integrating (MCAN_PSR[4-3] ACT = 00) at the next sample point. In case Protocol Exception Handling is disabled (MCAN_CCCR[12] PXHD = 1), the MCAN will treat a recessive res bit as an form error and will respond with an error frame.

CAN FD operation is enabled by programming the MCAN_CCCR[8] FDOE bit. In case MCAN_CCCR[8] FDOE = 1, transmission and reception of CAN FD frames is enabled. Transmission and reception of Classic CAN frames is always possible. Whether a CAN FD frame or a Classic CAN frame is transmitted can be configured via the FDF bit in the respective Tx Buffer element.

With MCAN_CCCR[8] FDOE = 0, received frames are interpreted as Classic CAN frames, which leads to the transmission of an error frame when receiving a CAN FD frame. When CAN FD operation is disabled, no CAN FD frames are transmitted even if the FDF bit of a Tx Buffer element is set. The MCAN_CCCR[8] FDOE and MCAN_CCCR[9] BRSE bits can only be changed while the MCAN_CCCR[0] INIT and MCAN_CCCR[1] CCE bits are both set. With MCAN_CCCR[8] FDOE = 0, the setting of bits FDF and BRS is ignored and frames are transmitted in Classic CAN format.

With MCAN_CCCR[8] FDOE = 1 and MCAN_CCCR[9] BRSE = 0, only FDF bit of a Tx Buffer element is evaluated. With MCAN_CCCR[8] FDOE = 1 and MCAN_CCCR[9] BRSE = 1, transmission of CAN FD frames with bit rate switching is enabled. All Tx Buffer elements with bits FDF and BRS set are transmitted in CAN FD format with bit rate switching.

A mode change during CAN operation is only recommended under the following conditions:

- The failure rate in the CAN FD data phase is significant higher than in the CAN FD arbitration phase. In this case disable the CAN FD bit rate switching option for transmissions.
- During system startup all nodes are transmitting Classic CAN messages until it is verified that they are able to communicate in CAN FD format. If this is true, all nodes switch to CAN FD operation.
- Wakeup messages in CAN Partial Networking have to be transmitted in Classic CAN format.
- End-of-line programming in case not all nodes are CAN FD capable. Non CAN FD nodes are held in Silent mode until programming has completed. Then all nodes switch back to Classic CAN communication.

In the CAN FD format, the DLC coding differs from the standard CAN format (see Table 12-248).

Table 12-248. DLC Coding

DLC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Number of Data Bytes in Standard CAN	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8
Number of Data Bytes in CAN FD	0	1	2	3	4	5	6	7	8	12	16	20	24	32	48	64

For CAN FD frames, the bit timing will be switched inside the frame after the BRS (Bit Rate Switch) bit in case this bit is recessive. In the CAN FD arbitration phase, before the BRS bit, the nominal CAN bit timing (see Figure 12-261) is used as configured by the Nominal Bit Timing and Prescaler Register MCAN_NBTP. In the following CAN FD data phase, the data phase bit timing is used as configured by the Data Bit Timing and Prescaler Register MCAN_DBTP. The bit timing is switched back from the data phase timing at the CRC delimiter or when an error is detected, whichever occurs first.

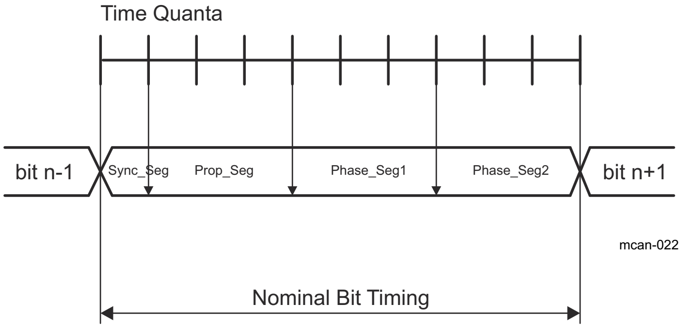


Figure 12-261. CAN Bit Timing

The maximum configurable data phase bit timing depends on the CAN clock frequency (FCLK). Example: with FCLK = 20 MHz and the shortest configurable bit time of 4 t_q (time quanta), the bit rate in the data phase is 5 Mbps.

In both data frame formats, CAN FD and CAN FD with bit rate switching, the value of the ESI (Error Status Indicator) bit depends on transmitter's error state (see MCAN_PSR[11] RESI bit) monitored at the start of the transmission. If the transmitter has error passive flag the ESI bit is transmitted recessive, else it is transmitted dominant.

12.5.1.4.3.4 Transmitter Delay Compensation

12.5.1.4.3.4.1 Description

When only one CAN FD node is transmitting and all others are receivers the length of the bus line has no impact. When transmitting via the TX pin the MCAN module receives the transmitted data from its local CAN transceiver via the RX pin. The received data is delayed. If the transmitter delay is greater than TSEG1 (time segment before sample point), a bit error is detected.

The MCAN module provides a delay compensation mechanism to compensate the transmitter delay. The compensation mechanism enables transmission with higher bit rates during the CAN FD data phase independent of the delay of a specific CAN transceiver. Without transmitter delay compensation the bit rate in the data phase is limited by the transmitter delay.

The mechanism enables configurations where the data bit time is shorter than the transmitter delay (it is described in detail in ISO 11898-1:2015). The transmitter delay compensation is enabled by setting the MCAN_DBTP[23] TDC bit to 1.

The delayed transmit data is compared against the received data at the Secondary Sample Point (SSP) in order to check for bit errors during the data phase of transmitting nodes. If a bit error is detected, the transmitter will react on this bit error at the next following regular sample point. During arbitration phase the delay compensation is always disabled.

The received bit is compared against the transmitted bit at the SSP. The SSP position is defined as the sum of the measured delay from the MCAN's transmit output TX pin through the transceiver to the receive input RX pin plus the transmitter delay compensation offset configured by the MCAN_TDCR[14-8] TDCO field (see Figure 12-262). The transmitter delay compensation offset is used to adjust the position of the SSP inside the received bit (example: half of the bit time in the data phase). The position of the SSP is rounded down to the next integer number of mtq.

The actual transmitter delay compensation value can be checked by reading the MCAN_PSR[22-16] TDCV field. This field is cleared when the MCAN_CCCR[0] INIT bit is set and is updated at each transmission of CAN FD frame while the MCAN_DBTP[23] TDC bit is set.

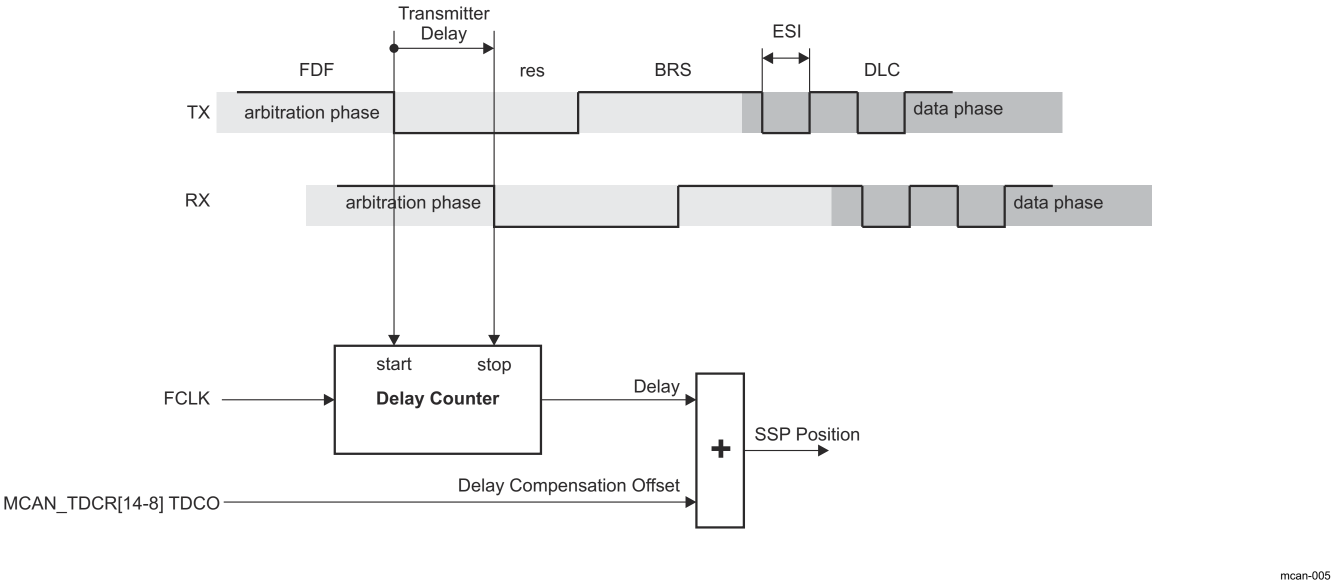


Figure 12-262. Transmitter Delay Measurement

12.5.1.4.3.4.2 Transmitter Delay Compensation Measurement

When transmitter delay compensation is enabled (by programming MCAN_DBTP[23] TDC = 1), the measurement is started within each transmitted CAN FD frame at the falling edge of FDF bit to bit res. The measurement is stopped when this edge is seen at the receive input RX pin of the transmitter. The resolution of this measurement is one mtq (see Figure 12-262). The mtq (minimum time quantum) dimension is equal to the CAN clock period (FCLK).

The use of a transmitter delay compensation filter window can be enabled by programming MCAN_TDCR[6-0] TDCF field. This filter feature defines a minimum value for the SSP position to avoid the case in which a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in an early taken SSP position. Dominant edges on the RX pin, that would result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least MCAN_TDCR[6-0] TDCF field and the RX pin is low.

The following boundary conditions have to be considered:

- The sum of the measured delay from the TX pin to the RX pin and the configured transmitter delay compensation offset (MCAN_TDCR[14-8] TDCO field) has to be less than 6 bit times in the data phase.
- The sum of the measured delay from the TX pin to the RX pin and the configured transmitter delay compensation offset (MCAN_TDCR[14-8] TDCO) field has to be less or equal 127 mtq. In case this sum exceeds 127 mtq, the maximum value of 127 mtq is used for transmitter delay compensation.
- The data phase ends at the sample point of the CRC delimiter, that stops checking of receive bits at the SSPs.

12.5.1.4.3.5 Restricted Operation Mode

In Restricted Operation Mode the CAN node is able to receive data and remote frames and to give acknowledge to valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The recieve and transmit error counters (MCAN_ECR[14-8] REC and MCAN_ECR[7-0] TEC) are frozen while CAN error logging (MCAN_ECR[23-16] CEL) is active. The Host CPU can set the MCAN module into Restricted Operation Mode by setting MCAN_CCCR[2] ASM bit. The bit can only be set by the Host CPU at any time when both MCAN_CCCR[2] CCE and MCAN_CCCR[0] INIT bits are set to 1.

The Restricted Operation Mode is automatically entered when the Tx Handler was not able to read data from the Message RAM in time. To leave Restricted Operation Mode, the Host CPU has to reset MCAN_CCCR[2] ASM bit. This mode can be used in applications that adapt themselves to different CAN bit rates. In this case the application tests different bit rates and leaves the Restricted Operation Mode after it has received a valid frame.

Note

The Restricted Operation Mode must not be combined with the Internal Loopback Mode .

12.5.1.4.3.6 Bus Monitoring Mode

Entering Bus Monitoring Mode is done by setting the MCAN_CCCR[5] MON bit to 1. In this mode (see ISO 11898-1:2015, *Bus Monitoring* section), the MCAN module is able to receive valid data and remote frames, but cannot start a transmission. The MCAN module sends only recessive bits on the CAN bus. If the MCAN module is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the MCAN module monitors this dominant bit, although the CAN bus may remain in recessive state. In Bus Monitoring Mode the MCAN_TXBRP register is held in reset state. The Bus Monitoring Mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits. Figure 12-263 shows the connection of the TX and RX signals to the MCAN module in Bus Monitoring Mode.

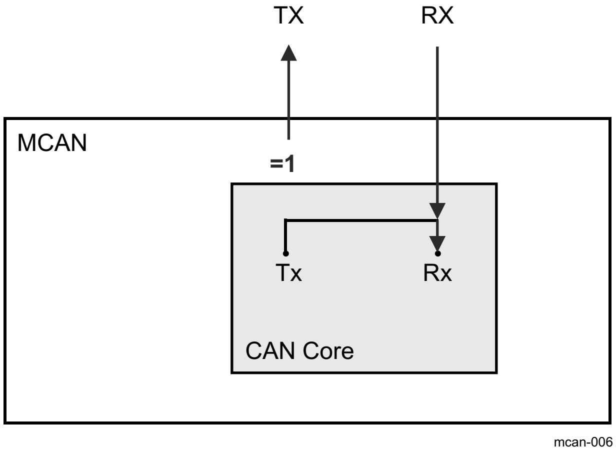


Figure 12-263. Connection of Signals in Bus Monitoring Mode

12.5.1.4.3.7 Disabled Automatic Retransmission (DAR) Mode

According to the CAN Specification (see ISO11898-1:2015, *Recovery Management* section), the MCAN module provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled (see the MCAN_CCCR[6] DAR bit).

12.5.1.4.3.7.1 Frame Transmission in DAR Mode

In DAR mode all transmissions are automatically cancelled after they started on the CAN bus. A Tx Buffer's Tx Request Pending MCAN_TXBRP[xx] TRPx bit is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

Successful transmission:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is set
- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is not set

Successful transmission in spite of cancellation:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is set
- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is set

Arbitration lost or frame transmission disturbed:

- Corresponding Tx Buffer Transmission Occurred MCAN_TXBTO[xx] TOx bit is not set

- Corresponding Tx Buffer Cancellation Finished MCAN_TXBCF[xx] CFx bit is set

In case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = 10 (transmission in spite of cancellation).

12.5.1.4.3.8 Power Down (Sleep Mode)

The entering in Power Down mode is controlled via two sources:

- PSC (via clock stop request signal)
- Software (by writing to the MCAN_CCCR[4] CSR bit)

As long as the clock stop request signal is active, the MCAN_CCCR[4] CSR bit is read as 1.

When all pending transmission requests have completed, the MCAN module waits until bus idle state is detected. Then the MCAN module sets the MCAN_CCCR[0] INIT bit to 1 to prevent any further CAN transfers.

The MCAN module acknowledges that it is ready for power down:

- By asserting clock stop acknowledge signal to the PSC (in case of PSC source).
- By setting the MCAN_CCCR[3] CSA flag bit to 1 (in case of Software source).

In this state, before the clocks are switched off, further register accesses can be made. Now the module clock inputs ICLK and FCLK may be switched off.

To leave power down mode, the application has to turn on the module clocks before resetting the input clock stop request signal respectively the MCAN_CCCR[4] CSR flag bit. The MCAN will acknowledge this by resetting the output clock stop acknowledge signal respectively the MCAN_CCCR[3] CSA flag bit. Afterwards, the application can restart CAN communication by resetting the MCAN_CCCR[0] INIT bit.

Restoring the clocks from clock stop mode, needs to be done according to how the clock stop was initiated:

- If Software asserts the MCAN_CCCR[3] CSA flag bit, once the MCAN module goes idle, the MCAN_CCCR[0] INIT bit is set. To get it started again, Software needs to write 0 to the MCAN_CCCR[0] INIT bit.
- If PSC is issuing a clock stop request, than there are two options for waking up:
  - After removing clock stop request signal, Software would need to write 0 to the MCAN_CCCR[0] INIT bit, or
  - If the MCANSS_CTRL[5] AUTOWAKEUP bit is set, than after removing clock stop request signal, an FSM inside the MCAN module will reset the MCAN_CCCR[0] INIT bit (without Software).

12.5.1.4.3.8.1 External Clock Stop Mode

The MCAN module supports two external clock stop modes:

- Immediate
- Graceful

In a graceful clock stop mode, when the clock stop request is asserted, the MCAN core will respond with clock stop acknowledge when all pending Tx messages have been processed and an Idle line had been detected. The MCAN_CCCR[0] INIT bit will be set, the MCAN core will go and stay Idle.

The automatic wakeup feature is enabled by setting the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits to 1 (for more information, see Section 12.5.1.4.3.8.3, *Wakeup request*). When external clock stop request is removed and no suspend request is active, a read-modify-write to the MCAN_CCCR[0] INIT bit is performed to clear it.

12.5.1.4.3.8.2 Suspend Mode

The MCAN module supports two suspend modes:

- Immediate
- Graceful

In a graceful suspend mode (see the MCANSS_CTRL[3] DBGSUSP_FREE bit), when the suspend request is asserted, a clock stop request to the MCAN core is performed. The MCAN core will respond with clock stop acknowledge when all pending Tx messages have been processed and an Idle line had been detected. At that point the MCAN_CCCR[0] INIT bit will be set, the MCAN core will go and stay Idle. The suspend state can be verified by reading MCAN_CCCR[0] INIT bit.

The automatic wakeup feature is enabled by setting the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits to 1 (for more information, see Section 12.5.1.4.3.8.3, *Wakeup request*). When suspend request is removed, if no external clock stop request is active, a read-modify-write to the MCAN_CCCR[0] INIT bit is performed to clear it.

During suspend mode the auto-clear feature is disabled. The following register fields have an auto-clear feature:

- MCAN_ECR[23-16] CEL
- MCAN_PSR[2-0] LEC
- MCAN_PSR[10-8] DLEC
- MCAN_PSR[11] RESI
- MCAN_PSR[12] RBRS
- MCAN_PSR[13] RFDF
- MCAN_PSR[14] PXE

12.5.1.4.3.8.3 Wakeup request

Issuing a clock stop request puts the MCAN module into Power Down mode (Sleep Mode). During transition from IDLE to ACTIVE, if the MCANSS_CTRL[5] AUTOWAKEUP and MCANSS_CTRL[4] WAKEUPREQEN bits are enabled, after the MCAN Core respond to the removal of the clock stop request with removing the clock stop acknowledge, a read-modify-write will be issued to clear the MCAN_CCCR[0] INIT bit and the MCAN core will resume operation.

If the MCANSS_CTRL[4] WAKEUPREQEN bit is set, the MCAN module provides a wakeup request on the following wakeup event:

- The receive RX pin is dominant (logical 0)

The wakeup request is de-asserted when any of the following conditions occur:

- Clock stop request is removed and clock stop acknowledge is de-asserted
- A reset is applied to the MCAN module

12.5.1.4.3.9 Test Modes

The MCAN_TEST register write access is enabled by setting the test mode enable MCAN_CCCR[7] TEST bit to 1. The MCAN_TEST register allows the configuration of the test modes and test functions.

The CAN transmit TX pin has four output functions. One of those functions can be selected by programming the MCAN_TEST[6-5] TX field. Additionally to its default function (the serial data output) it can drive the CAN Sample Point signal to monitor the MCAN's bit timing and it can drive constant dominant or recessive values.

The actual value of the CAN receive RX pin can be monitored from MCAN_TEST[7] RX bit. Both functions can be used to check the CAN bus physical layer. Due to the synchronization mechanism between CAN clock (FCLK) and Host clock (ICLK) domain, there may be a delay of several Host clock periods between writing to the MCAN_TEST[6-5] TX field until the new configuration is visible at the output TX pin. This applies also when reading input RX pin via the MCAN_TEST[7] RX bit.

Note

Test modes should be used for self test only. The software control for TX pin interferes with all CAN protocol functions. It is not recommended to use test modes for application.

12.5.1.4.3.9.1 Internal Loopback Mode

The MCAN module can be set into Internal Loopback Mode by programming MCAN_TEST[4] LBCK and MCAN_CCCR[5] MON bits to 1. The Internal Loopback Mode is used for a 'Hot Selftest'. The 'Hot Selftest' allows the MCAN module to be tested without affecting a running CAN system connected to the TX and RX pins. In this mode RX pin is disconnected from the MCAN module and TX pin is held recessive. Figure 12-264 shows the connection of the TX and RX pins to the MCAN module in case of Internal Loopback Mode.

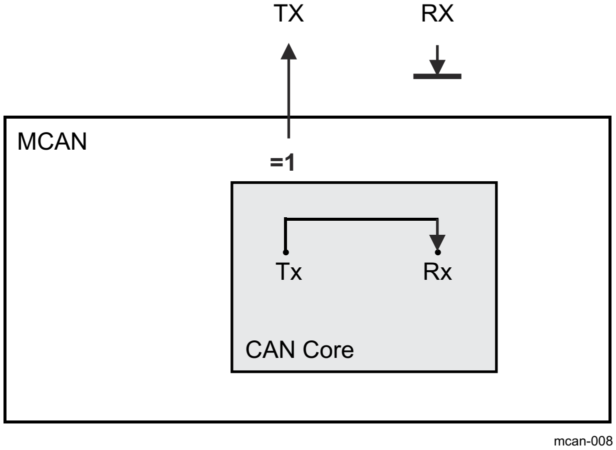


Figure 12-264. Internal Loopback Mode

12.5.1.4.4 Timestamp Generation

The MCAN module has integrated a 16-bit wrap-around counter for timestamp generation. The timestamp counter prescaler MCAN_TSCC[19-16] TCP field can be configured to clock the counter in multiples of CAN bit times (1-16). The counter is readable via the MCAN_TSCV[15-0] TSC field. A write access to the MCAN_TSCV register resets the counter to zero. When the timestamp counter wraps around the interrupt MCAN_IR[16] TSW flag is set. On start of a frame reception/transmission the counter value is captured and stored into the timestamp section of an Rx Buffer/Rx FIFO (RXTS[15-0]) or Tx Event FIFO (TXTS[15-0]) element. For more information, see Section 12.5.1.4.10, *Message RAM*.

12.5.1.4.4.1 External Timestamp Counter

For CAN FD operation mode the MCAN core requires an External Timestamp Counter. An externally generated 16-bit vector may substitute the integrated 16-bit CAN bit time counter (internal timestamp counter) for receive and transmit timestamp generation. An external 16-bit timestamp counter can be used by programming the MCAN_TSCC[1-0] TSS field.

The External Timestamp Counter uses the interface clock (ICLK) as a reference clock. The MCAN Core accepts a 16-bit timestamp. A 24-bit prescaler provides a programmable resolution for the timestamp (see MCANSS_EXT_TS_PRESCALER[23-0] PRESCALER bit field). The External Timestamp Counter counter can be enabled or disabled through the MCANSS_CTRL[6] EXT_TS_CNTR_EN bit. When disabled the counter is reset back to zero. While enabled the counter keeps incrementing. When the timestamp rolls over the MCAN timestamp interrupt is generated.

When the timestamp rolls over the MCANSS_IRS register is set (see Figure 12-265). The MCANSS_IE register can be affected by writing to the *MCANSS_IESS* register to set or to the MCANSS_IECS register to clear. The *MCANSS_IESS* register is a shadow register mapped to the same address as the MCANSS_IE register. The level interrupt is a reflection of both MCANSS_IRS and MCANSS_IE being set. The MCANSS_IES register reflects the level interrupt. When an rollover event occurs the interrupt counter is incremented. Writing to the MCANSS_ICS register to clear the MCANSS_IRS register will also decrement the interrupt counter. Writing to the MCANSS_EOI register will issue another pulse if the interrupt counter is not zero.

The rollover event can be artificially simulated by software through writing to the Interrupt Set Shadow register (*MCANSS_ISS*). The *MCANSS_ISS* register is a shadow register mapped to the same address as the MCANSS_IRS register.

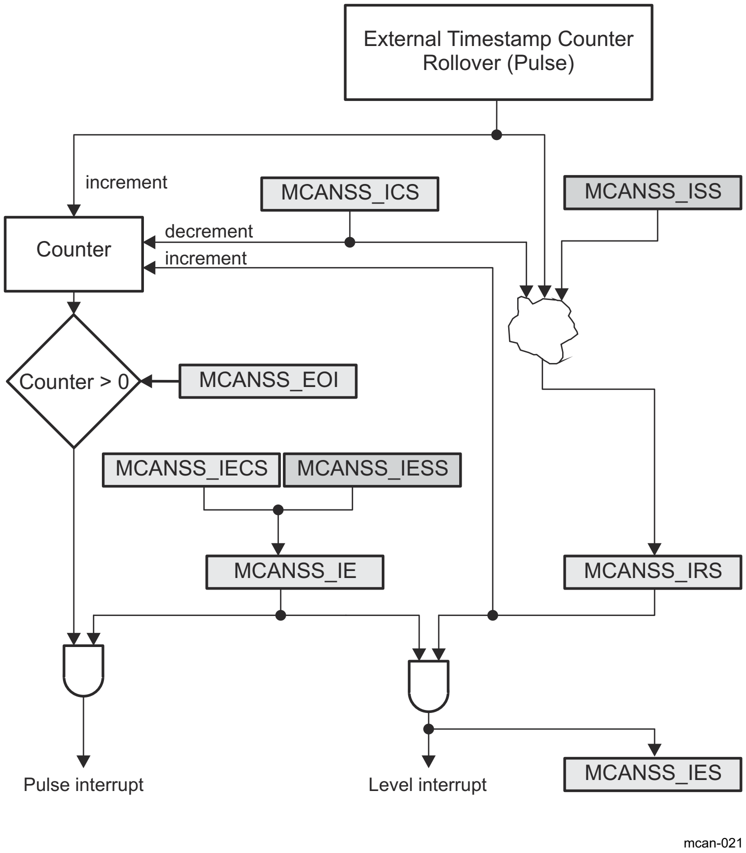


Figure 12-265. External Timestamp Counter Interrupt

12.5.1.4.5 Timeout Counter

The MCAN module has integrated a 16-bit Timeout Counter. It is used to signal timeout conditions for the Rx FIFO 0, Rx FIFO 1, and Tx Event FIFO Message RAM elements. The Timeout Counter is configured via the MCAN_TOCC register. It is enabled via the MCAN_TOCC[0] ETOC bit. The Timeout Counter operates as down-counter and uses the same prescaler programmed by the MCAN_TSCC[19-16] TCP field as the Timestamp Counter. The actual counter value can be monitored from the MCAN_TOCV[15-0] TOC field. The Timeout Counter can be started only when MCAN_CCCR[0] INIT = 0 and stopped when MCAN_CCCR[0] INIT = 1 (example: when the MCAN enters Bus_Off state). The operation mode is selected by the MCAN_TOCC[2-1] TOS field. When Continuous Mode is selected, the counter starts when MCAN_CCCR[0] INIT = 0, a write to the MCAN_TOCV register presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field and continues down-counting.

In case the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field. Down-counting is started when the first FIFO element is stored. Writing to the MCAN_TOCV register has no effect. When the counter reaches zero, the interrupt MCAN_IR[18] TOO flag is set.

In Continuous Mode, the counter is immediately restarted at the value configured by the MCAN_TOCC[31-16] TOP field.

12.5.1.4.6 ECC Support

The Message Memory is wrapped in an ECC wrapper providing SECDED parity functionality. The ECC wrapper is controlled by an ECC Aggregator.

12.5.1.4.6.1 ECC Wrapper

The ECC wrapper provides Single Error Correction (SEC) and Double Error Detection (DED) parity to the Message Memory content. It has side band signals for error notification. The ECC Wrapper implements an error injection test mode.

The error correction is done using a lazy write back. When an error is detected, it is noted in a FIFO Queue which waits for an access gap to write the data back and refresh the memory. If a transaction writes new data to the compromised entry before the lazy write back completes, the write back is discarded.

12.5.1.4.6.2 ECC Aggregator

Note

For more information about ECC Aggregator, refer to *ECC Aggregator*.

12.5.1.4.7 Rx Handling

The Rx Handler controls the following operations:

- Acceptance filtering
- The transfer of received messages to the Rx Buffers or to one of the two Rx FIFOs (Rx FIFO 0 or Rx FIFO 1)
- Rx FIFO Put and Get Index operations

12.5.1.4.7.1 Acceptance Filtering

The MCAN module is capable to configure two sets of acceptance filters - one set for standard and one set for extended identifiers. These filters can be assigned to an Rx Buffer or to one of the two Rx FIFOs.

The main features of the filter elements are:

- Each filter element can be configured as:
  - Range Filter (from - to)
  - Filter for specific IDs (for one or two dedicated IDs)
  - Classic Bit Mask Filter
- Each filter element can be enabled/disabled individually
- Each filter element can be configured for acceptance or rejection filtering
- Filters are checked sequentially and execution (acceptance filtering procedure) stops at the first matching filter element or when the end of the filter list is reached

Related configuration registers are:

- Global Filter Configuration (MCAN_GFC) register
- Standard ID Filter Configuration (MCAN_SIDFC) register
- Extended ID Filter Configuration (MCAN_XIDFC) register
- Extended ID AND Mask (MCAN_XIDAM) register

Depending on the configuration of the filter element (see SFEC/EFEC in Section 12.5.1.4.10, *Message RAM*) if filter matches, one of the following actions is performed:

- Received frame is stored in FIFO 0 or FIFO 1
- Received frame is stored in Rx Buffer
- Received frame is stored in Rx Buffer and generation of pulse at filter event pin is performed. This is high level single ICLK pulse. For more information, see Section 12.5.1.4.2.1, *DMA Requests*.
- Received frame is rejected
- Set High Priority Message interrupt flag MCAN_IR[8] HPM
- Set High Priority Message interrupt flag MCAN_IR[8] HPM and store received frame in FIFO 0 or FIFO 1

Acceptance filtering starts when complete Message ID is received. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If a filter element matches - the Rx Handler starts writing the received message data in portions of 32 bit to the matching Rx Buffer or Rx FIFO. If an error condition occurs (for example: CRC error), this message is rejected with the following impact on the affected Rx Buffer or Rx FIFO:

- Rx Buffer:

New Data flag (MCAN_NDAT1/MCAN_NDAT2) of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data (for error type see MCAN_PSR[2-0] LEC respectively MCAN_PSR[10-8] DLEC fields).

- Rx FIFO:
  Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data (for error type see MCAN_PSR[2-0] LEC respectively MCAN_PSR[10-8] DLEC fields). If matching Rx FIFO is configured to operate in overwrite mode, the boundary conditions described in Section 12.5.1.4.7.2.2 have to be considered.

12.5.1.4.7.1.1 Range Filter

Each filter element can be configured to operate as Range Filter (Standard Filter Type SFT = 00/Extended Filter Type EFT = 00). The filter matches for all received message frames with IDs in the range from SFID1 to SFID2 (SFID2 ≥ SFID1) respectively in the range from EFID1 to EFID2 (EFID2 ≥ EFID1). For more information see Section 12.5.1.4.10.5, *Standard Message ID Filter Element* and Section 12.5.1.4.10.6, *Extended Message ID Filter Element*.

There are two options for range filtering of extended frames:

- Extended Filter Type EFT = 00: The Extended ID AND Mask (MCAN_XIDAM) is used for Range Filtering. The Message ID of received frames is ANDed with the Extended ID AND Mask (MCAN_XIDAM) before the range filter is applied.
- Extended Filter Type EFT = 11: The Extended ID AND Mask (MCAN_XIDAM) is not used for Range Filtering.

12.5.1.4.7.1.2 Filter for specific IDs

Each filter element can be configured to filter one or two dedicated Message IDs (Standard Filter Type SFT =01/ Extended Filter Type EFT =01). To filter only one specific Message ID, the filter element has to be configured with SFID1 = SFID2 respectively EFID1 = EFID2. For more information see Section 12.5.1.4.10.5, *Standard Message ID Filter Element* and Section 12.5.1.4.10.6, *Extended Message ID Filter Element*.

12.5.1.4.7.1.3 Classic Bit Mask Filter

Classic bit mask filtering can filter groups of Message IDs (Standard Filter Type SFT =10/Extended Filter Type EFT =10). This is done by masking single bits of a received Message ID. In this case SFID1/EFID1 element is used as Message ID filter, while SFID2/EFID2 element is used as filter mask.

A 0 bit at the filter mask (SFID2/EFID2) will mask out the corresponding bit position of the configured Message ID filter (SFID1/EFID1) and the value of the received Message ID at that bit position is not relevant for acceptance filtering. Only those bits of the received Message ID where the corresponding mask bits are 1 are relevant for acceptance filtering.

There are two interesting cases:

- All mask bits are 1: a match occurs only when the received Message ID and the configured Message ID filter are identical.
- All mask bits are 0: all Message IDs match.

12.5.1.4.7.1.4 Standard Message ID Filtering

The standard Message ID (11-bit ID) filtering flow is shown in Figure 12-266. Section 12.5.1.4.10.5, *Standard Message ID Filter Element* describes the standard Message ID filter element.

The Remote Transmission Request (RTR) and Extended Identifier (XTD) bits of the received frames are compared against the list of configured filter elements. This is controlled by the following registers:

- Global Filter Configuration (MCAN_GFC) register
- Standard ID Filter Configuration (MCAN_SIDFC) register

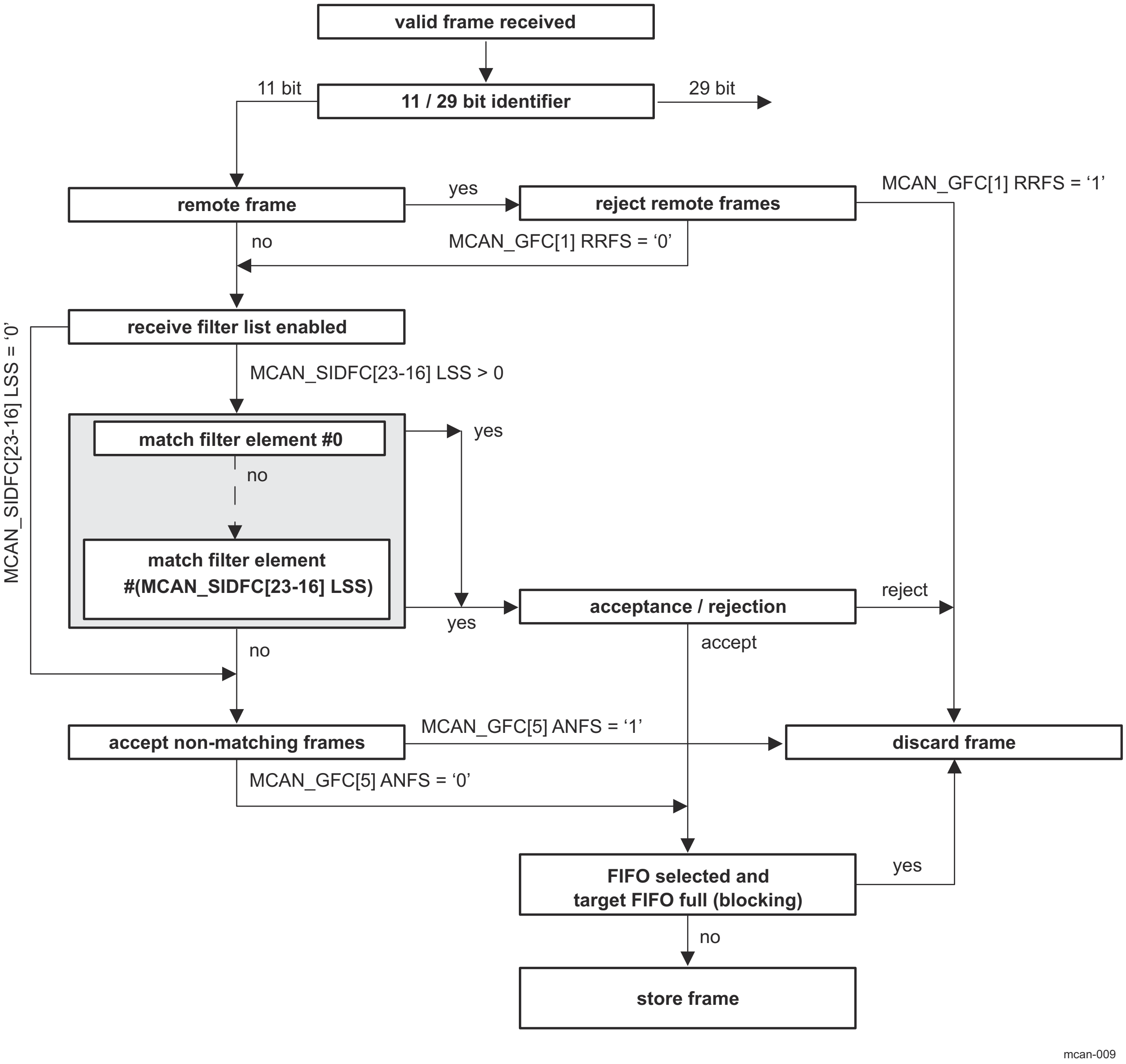


Figure 12-266. Standard Message ID Filter Path

12.5.1.4.7.1.5 Extended Message ID Filtering

The extended Message ID (29-bit ID) filtering flow is shown in Figure 12-267. Section 12.5.1.4.10.6, *Extended Message ID Filter Element* describes the extended Message ID filter element.

The Remote Transmission Request (RTR) and Extended Identifier (XTD) bits of the received frames are compared against the list of configured filter elements. This is controlled by the following registers:

- Global Filter Configuration (MCAN_GFC) register
- Extended ID Filter Configuration (MCAN_XIDFC) register

Note that before the filter list is executed the received identifier is ANDed with the Extended ID AND Mask (MCAN_XIDAM).

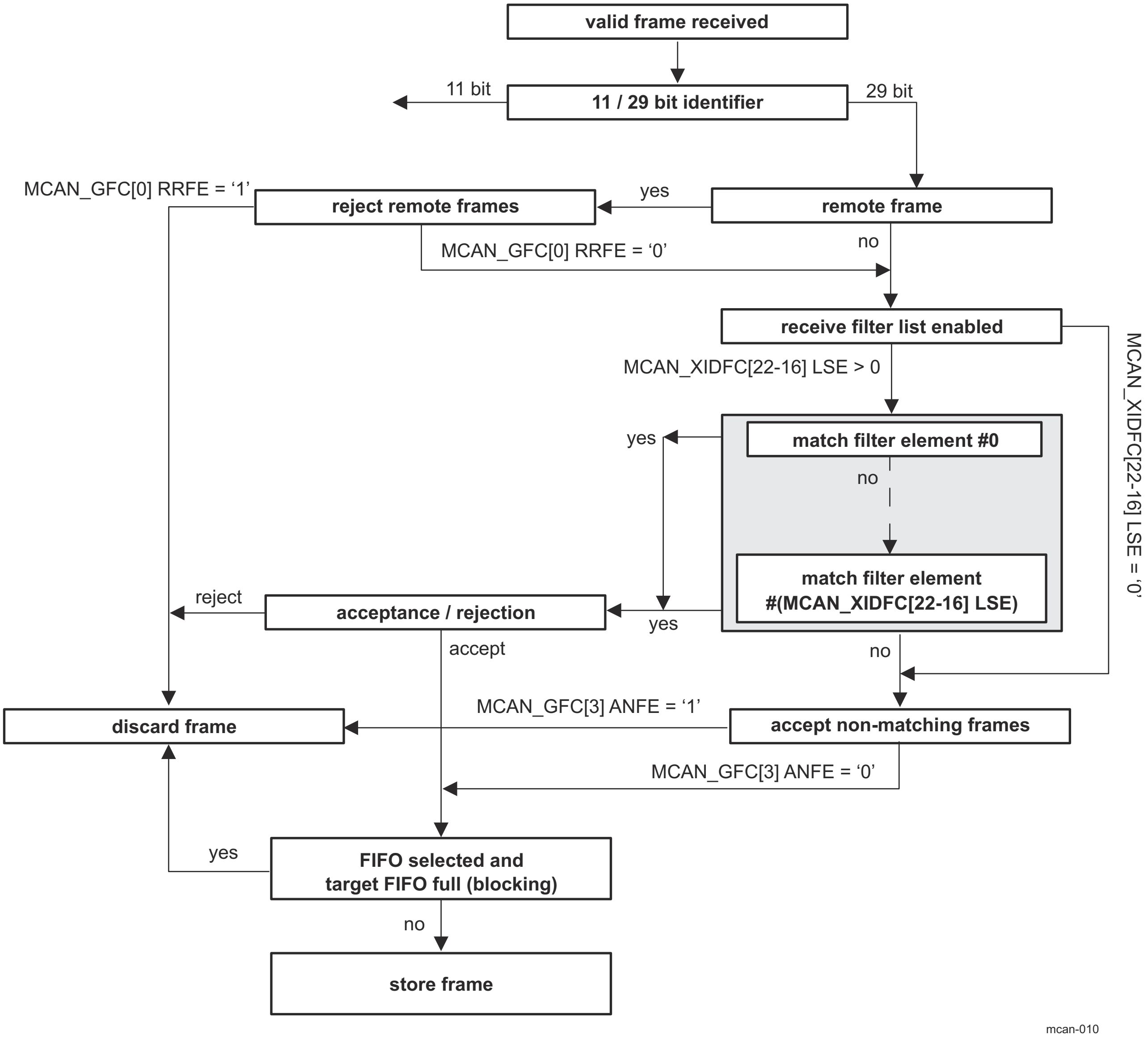


Figure 12-267. Extended Message ID Filter Path

12.5.1.4.7.2 Rx FIFOs

The configuration of the Rx FIFOs (Rx FIFO 0 and Rx FIFO 1) can be done via the MCAN_RXF0C and MCAN_RXF1C registers. Each Rx FIFO can be configured to store up to 64 received messages.

After acceptance filtering the received messages that passed are transferred to the Rx FIFO. The filter mechanisms available for the Rx FIFO 0 and Rx FIFO 1 is described in Section 12.5.1.4.7.1, *Acceptance Filtering*. Section 12.5.1.4.10.2, *Rx Buffer and FIFO Element* describes the Rx FIFO element.

The Rx FIFO watermark can be used to prevent an Rx FIFO overflow. If the Rx FIFO fill level reaches the Rx FIFO watermark configured by the MCAN_RXFnC[30-24] FnWM field (where: n = 0 or 1) an interrupt flag MCAN_IR[1] RF0W/MCAN_IR[5] RF1W is set.

When the Rx FIFO Put Index reaches the Rx FIFO Get Index (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI) an Rx FIFO Full condition is signalled by the MCAN_RXFnS[24] FnF status bit and interrupt flag MCAN_IR[2] RF0F/MCAN_IR[6] RF1F is set. Figure 12-268 shows Rx FIFO Status. The FIFOs fill level is presented in the MCAN_RXFnS[6-0] FnFL field (the number of elements stored in Rx FIFO).

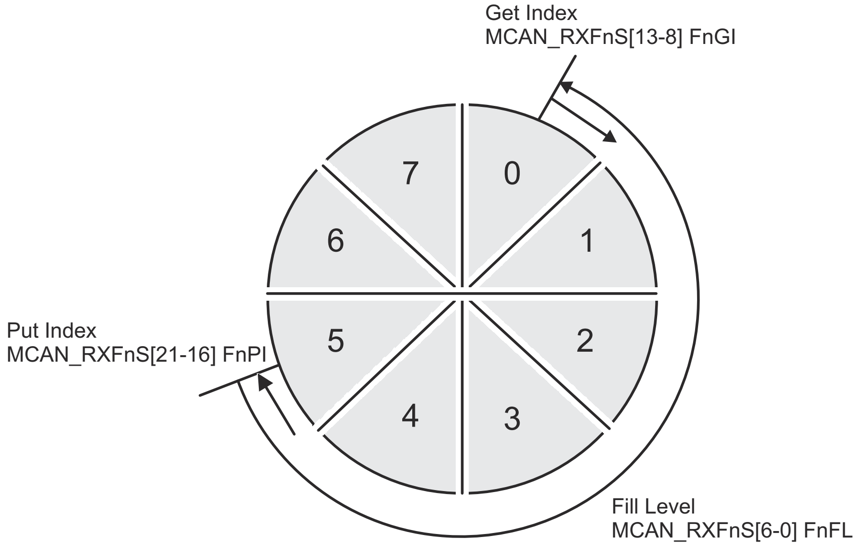


Figure 12-268. Rx FIFO Status

Rx FIFOs start address in the Message RAM (MCAN_RXFnC[15-2] FnSA field) have to be configured when reading from an Rx FIFO (Rx FIFO Get Index - MCAN_RXFnS[13-8] FnGI). Table 12-249 presents Rx Buffer/Rx FIFO Element Size for different Rx Buffer/Rx FIFO Data Field Size which is configured via the MCAN_RXESC register.

Table 12-249. Rx Buffer/Rx FIFO Element Size

MCAN_RXESC[10-8] RBDS MCAN_RXESC[2-0] F0DS/ MCAN_RXESC[6-4] F1DS	Data Field [bytes]	FIFO Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

12.5.1.4.7.2.1 Rx FIFO Blocking Mode

The Rx FIFO blocking mode is the default operation mode for the Rx FIFOs. It is configured by the MCAN_RXFnC[31] FnOM = 0.

If an Rx FIFO full condition is reached (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI), no further messages are written to the corresponding Rx FIFO until at least one message has been read out and the Rx FIFO Get Index has been incremented. An Rx FIFO full condition is signalled by the MCAN_RXFnS[24] FnF = 1 and interrupt flag MCAN_IR[2] RF0F/MCAN_IR[6] RF1F is set.

In case a message is received while the corresponding Rx FIFO is full, this message is rejected and the message lost condition is signalled by MCAN_RXFnS[25] RFnL = 1 and interrupt flag MCAN_IR[3] RFnL/ MCAN_IR[25] RFnL is set.

12.5.1.4.7.2.2 Rx FIFO Overwrite Mode

The Rx FIFO overwrite mode is configured by the MCAN_RXFnC[31] FnOM = 1. When an Rx FIFO full condition is reached (MCAN_RXFnS[21-16] FnPI = MCAN_RXFnS[13-8] FnGI) signalled by MCAN_RXFnS[24] FnF = 1, the next accepted message for the FIFO will overwrite the oldest FIFO message. Put index/Get index are both incremented by one.

In overwrite mode if an Rx FIFO full condition is signalled, reading of the Rx FIFO elements should start at least at get index + 1. The reason for that is, that it might happen, that a received message is written to the Message RAM (Put index) while the Host CPU is reading from the Message RAM (Get index). In this case inconsistent data may be read from the respective Rx FIFO element. The problem is solved by adding an offset to the Get index when reading from the Rx FIFO. The offset depends on how fast the Host CPU accesses the Rx FIFO. Figure 12-269 shows an offset of two with respect to the Get index when reading the Rx FIFO. In this case the two messages stored in element 1 and 2 are lost.

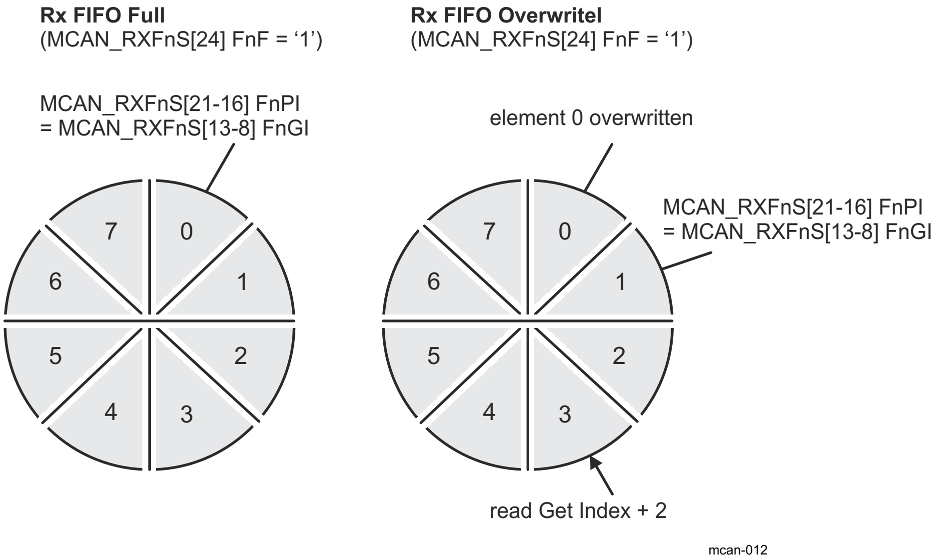


Figure 12-269. Rx FIFO Overflow Handling

After reading from the Rx FIFO, the number of the last element read has to be written to the Rx FIFO Acknowledge Index MCAN_RXFnA[5-0] FnAI. This increments the get index to that element number. In case the Put index has not been incremented to this Rx FIFO element, the Rx FIFO full condition is reset (MCAN_RXFnS[24] FnF = 0).

12.5.1.4.7.3 Dedicated Rx Buffers

The MCAN supports up to 64 dedicated Rx Buffers. The start address of the Rx Buffers section in the Message RAM is configured via MCAN_RXBC[15-2] RBSA field. To store in an Rx Buffer a Standard or Extended Message ID Filter Element with SFEC/EFEC = 111 and SFID2/EFID2[10-9] = 00 has to be configured (see Section 12.5.1.4.10.5, *Standard Message ID Filter Element* and Section 12.5.1.4.10.6, *Extended Message ID Filter Element*).

After a received message has been accepted by a filter element, the message is stored into the Rx Buffer in the Message RAM referenced by the filter element (the format is the same as for an Rx FIFO element). In addition the flag MCAN_IR[19] DRX (Message stored in Dedicated Rx Buffer) is set.

Table 12-250 shows Example Filter Configuration for Rx Buffers.

Table 12-250. Example Filter Configuration for Rx Buffers

Filter Element	SFID1[10-0] EFID1[28-0]	SFID2[10-9] EFID2[10-9]	SFID2[5-0] EFID2[5-0]
0	ID message 1	00	00 0000
1	ID message 2	00	00 0001
2	ID message 3	00	00 0010

After the last word of a matching received message has been written to the Message RAM, the respective New Data flag in register MCAN_NDAT1/MCAN_NDAT2 is set. As long as the New Data flag is set, the respective

Rx Buffer is locked against updates from received matching frames. The New Data flags have to be reset by the Host CPU by writing a 1 to the respective bit position.

While an Rx Buffer's New Data flag is set, a Message ID Filter Element referencing this specific Rx Buffer will not match, causing the acceptance filtering to continue. Following Message ID Filter Elements may cause the received message to be stored into another Rx Buffer, or into an Rx FIFO, or the message may be rejected, depending on filter configuration.

12.5.1.4.7.3.1 Rx Buffer Handling

Rx Buffer Handling include the following steps:

- Reset interrupt flag MCAN_IR[19] DRX
- Read New Data registers
- Read messages from Message RAM
- Reset New Data flags of processed messages

12.5.1.4.7.4 Debug on CAN Support

Debug DMA is not supported feature. Debug messages can be traced through the RX FIFO (see Section 12.5.1.4.7.2).

12.5.1.4.8 Tx Handling

The Tx Handler is used to handle the Tx requests. It controls the transfer of transmit messages from the dedicated Tx Buffers, the Tx FIFO, and the Tx Queue to the CAN Core, the Tx Event FIFO, and the Put and Get Index operations. The MCAN module supports up to 32 Tx Buffers. These Tx Buffers can be configured as dedicated Tx Buffers, Tx FIFO, or Tx Queue and as combination of dedicated Tx Buffers/Tx FIFO or dedicated Tx Buffers/Tx Queue. For each Tx Buffer element Classical CAN or CAN FD transmission mode can be configured. Section 12.5.1.4.10.3 describes the Tx Buffer Element. Table 12-251 shows the possible configurations for message transmission.

Table 12-251. Possible Configurations for Message Transmission

MCAN_CCCR		Tx Buffer Element		Frame Transmission
MCAN_CCCR[9] BRSE	MCAN_CCCR[8] FDOE	FDF	BRS	
ignored	0	ignored	ignored	Classic CAN
0	1	0	ignored	Classic CAN
0	1	1	ignored	CAN FD without bit rate switching
1	1	0	ignored	Classic CAN
1	1	1	0	CAN FD without bit rate switching
1	1	1	1	CAN FD with bit rate switching

When the Tx Buffer Request Pending MCAN_TXBRP register is updated, or when a transmission has been started the Tx Handler starts scanning to check for the highest priority pending Tx request. The Tx Buffer with lowest Message ID has highest priority.

Note

AUTOSAR requires at least three Tx Queue Buffers and support of transmit cancellation.

12.5.1.4.8.1 Transmit Pause

The transmit pause feature is intended for use in CAN networks where the CAN Message IDs are specific and cannot easily be changed. These Message IDs may have a higher priority than other defined Message IDs, while in a specific application their relative priority should be inverse. This allows for a case where one ECU sends a burst of CAN messages that cause another ECU's CAN messages to be delayed (paused).

The transmit pause feature is enabled by the MCAN_CCCR[14] TXP bit. By default this bit is disabled (MCAN_CCCR[14] TXP = 0). Each time after successfully transmitted message, a pause for two CAN bit times occurs before the start of the next transmission. This allows the other CAN nodes in the network to transmit messages even if their Message IDs have lower priority.

12.5.1.4.8.2 Dedicated Tx Buffers

Dedicated Tx Buffers are intended for message transmission under complete control of the Host CPU.

There are two options:

- Each dedicated Tx Buffer is configured with a specific Message ID.
- Two or more dedicated Tx Buffers are configured with the same Message ID. In this case the Tx Buffer with the lowest buffer number is transmitted first.

After the data section has been updated, a transmission is requested by an Add Request. This is done via the MCAN_TXBAR[x]ARn bit (where x = 0 - 31). The requested messages arbitrate internally with messages from an optional Tx FIFO or Tx Queue and externally with messages on the CAN bus, and are sent out according to their Message ID.

Table 12-252 shows Tx Buffer/Tx FIFO/Tx Queue Element Size. A Dedicated Tx Buffer allocates Element Size 32-bit words in the Message RAM. The start address of a dedicated Tx Buffer in the Message RAM is calculated by adding transmit buffer index from 0 to 31 (MCAN_TXFQS[20-16] TFQPI) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

Table 12-252. Tx Buffer/Tx FIFO/Tx Queue Element Size

MCAN_TXESC[2-0] TBDS	Data Field [bytes]	Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

12.5.1.4.8.3 Tx FIFO

Tx FIFO mode is configured by setting bit MCAN_TXBC[30] TFQM = 0. The stored in the Tx FIFO messages are transmitted starting with the message referenced by the Get Index MCAN_TXFQS[12-8] TFGI field. After each transmission the Get Index is incremented until the Tx FIFO is empty. The Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field indicates the number of the available free Tx FIFO elements. The Tx FIFO allows transmission of messages with the same Message ID from different Tx Buffers in the order these messages have been written to the Tx FIFO.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index MCAN_TXFQS[20-16] TFQPI field. After each Add Request (MCAN_TXBAR[x] ARn = 1) the Put Index is incemented to the next free Tx FIFO element. When the Put Index reaches the Get Index (MCAN_TXFQS[20-16] TFQPI = MCAN_TXFQS[12-8] TFGI), Tx FIFO Full condition is signalled by bit MCAN_TXFQS[21] TFQF = 1. In this case no further messages should be written to the Tx FIFO until the next message has been transmitted and the Get Index has been incremented.

The number of requested Tx buffers should not exceed the number of free Tx Buffers as indicated by the Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field.

In case a transmission request for the Tx Buffer referenced by the Get Index is cancelled, the Get Index is incremented to the next Tx Buffer with pending transmission request and the Tx FIFO Free Level MCAN_TXFQS[5-0] TFFL field is recalculated. In case transmission cancellation is applied to any other Tx Buffer - the Get Index and the FIFO Free Level remain unchanged.

A Tx FIFO element allocates Element Size 32-bit words in the Message RAM (see Table 12-252). The start address of the next available (free) Tx FIFO Buffer is calculated by adding Tx FIFO/Queue Put Index

MCAN_TXFQS[20-16] TFQPI (from 0 to 31) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

12.5.1.4.8.4 Tx Queue

Tx Queue mode is configured by setting bit MCAN_TXBC[30] TFQM = 1. The stored in the Tx Queue messages are transmitted starting with the highest priority message (lowest Message ID). In case two or more Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index MCAN_TXFQS[20-16] TFQPI field. Each Add Request cyclically increments the Put Index to the next free Tx Buffer. In case of Tx Queue Full condition (MCAN_TXFQS[21] TFQF = 1), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been cancelled.

The application may use the MCAN_TXBRP register instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

A Tx Queue Buffer allocates Element Size 32-bit words in the Message RAM (see Table 12-252). The start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index MCAN_TXFQS[20-16] TFQPI (from 0 to 31) × Element Size to the Tx Buffer Start Address MCAN_TXBC[15-2] TBSA field.

12.5.1.4.8.5 Mixed Dedicated Tx Buffers/Tx FIFO

For this combination the Tx Buffers section in the Message RAM is separated in two parts:

- Dedicated Tx Buffers: the number of Dedicated Tx Buffers is configured by the MCAN_TXBC[21-16] NDTB field
- Tx FIFO: the number of Tx Buffers assigned to the Tx FIFO is configured by the MCAN_TXBC[29-24] TFQS field

If the MCAN_TXBC[29-24] TFQS field is empty (zero) - only Dedicated Tx Buffers are used.

Tx prioritization:

- Scan Dedicated Tx Buffers and oldest pending Tx FIFO Buffer (referenced by the MCAN_TXFQS[12-8] TFGI field)
- Buffer with lowest Message ID gets highest priority and is transmitted next

Figure 12-270 shows Mixed Dedicated Tx Buffers/Tx FIFO example.

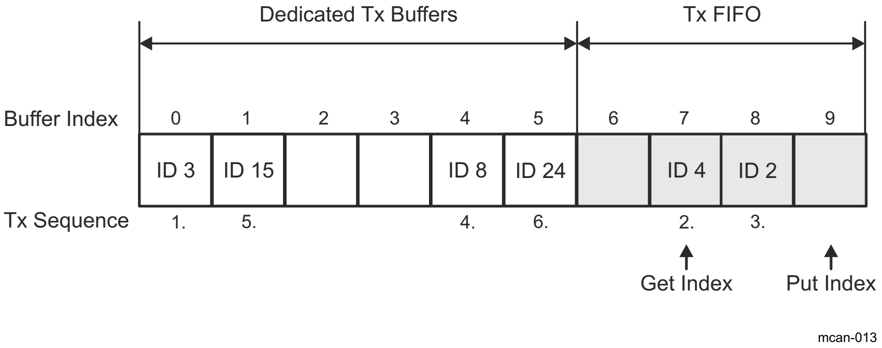


Figure 12-270. Mixed Dedicated Tx Buffers/Tx FIFO (example)

12.5.1.4.8.6 Mixed Dedicated Tx Buffers/Tx Queue

For this combination the Tx Buffers section in the Message RAM is separated in two parts:

- Dedicated Tx Buffers: the number of Dedicated Tx Buffers is configured by the MCAN_TXBC[21-16] NDTB field
- Tx Queue: the number of Tx Buffers assigned to the Tx Queue is configured by the MCAN_TXBC[29-24] TFQS field

If MCAN_TXBC[29-24] TFQS field is empty (zero) - only Dedicated Tx Buffers are used.

Tx prioritization:

- Scan all Tx Buffers with activated transmission request
- Tx Buffer with lowest Message ID gets highest priority and is transmitted next

Figure 12-271 shows Mixed Dedicated Tx Buffers/Tx Queue example.

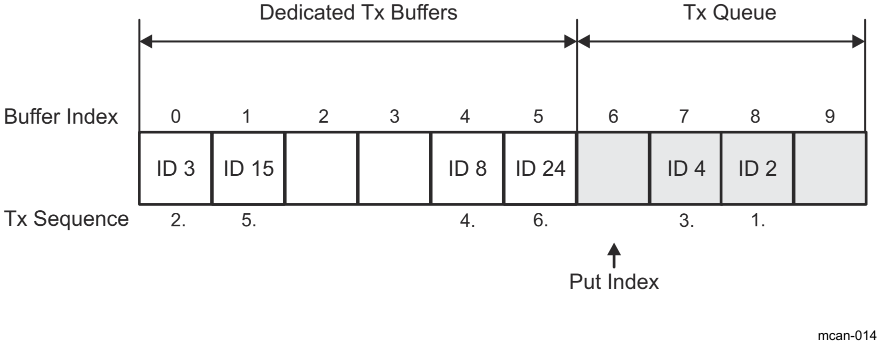


Figure 12-271. Mixed Dedicated Tx Buffers/Tx Queue (example)

12.5.1.4.8.7 Transmit Cancellation

This feature is especially intended for gateway and AUTOSAR based applications. The Host CPU can cancel a requested transmission from a dedicated Tx Buffer or a Tx Queue Buffer by setting bit MCAN_TXBCR[n] CRn = 1 (where n = 0 - 31). The corresponding bit position n is equivalent to the number of the Tx Buffer.

Transmit cancellation is not intended for Tx FIFO operation.

Successful cancellation is signalled by setting the corresponding bit of the MCAN_TXBCF register (MCAN_TXBCF[n] CFn = 1).

If transmission from a Tx Buffer is already ongoing and a transmit cancellation is requested, the corresponding MCAN_TXBRP[n] TRPn bit remains set as long as the transmission is in progress. If the transmission was successful, the corresponding MCAN_TXBTO[n] TOn and MCAN_TXBCF[n] CFn bits are set. If the transmission was not successful, only the corresponding bit MCAN_TXBCF[n] CFn = 1.

Note

If pending transmission is cancelled immediately before this transmission could have been started, a short time window occurs where no transmission is started even if another message is also pending in this node. This may enable another node to transmit a message which may have a lower priority than the second message in this node.

12.5.1.4.8.8 Tx Event Handling

To support Tx Event Handling the Message RAM has implemented a Tx Event FIFO section. Up to 32 Tx Event FIFO elements can be configured. Section 12.5.1.4.10.4 describes the Tx Event FIFO element. After message transmission on the CAN bus, Message ID and Timestamp are stored in a Tx Event FIFO element. To link a Tx Event to a Tx Event FIFO element, the Message Marker from the transmitted Tx Buffer is copied into the Tx Event FIFO element.

A Tx Event FIFO full condition is signalled by the MCAN_IR[14] TEFF bit. In this case no further elements are written to the Tx Event FIFO until at least one element has been read out and the Tx Event FIFO Get Index has been incremented (MCAN_TXEFS[12-8] EFGI). In case a Tx Event occurs while the Tx Event FIFO is full, this event is rejected and interrupt flag MCAN_IR[15] TEFL bit is set.

The Tx Event FIFO watermark can be configured to avoid a Tx Event FIFO overflow. When the Tx Event FIFO fill level reaches the Tx Event FIFO watermark configured by the MCAN_TXEFC[29-24] EFWM field, interrupt flag MCAN_IR[13] TEFW is set. When reading from the Tx Event FIFO, two times the Tx Event FIFO Get Index

MCAN_TXEFS[12-8] EFGI field has to be added to the Tx Event FIFO start address MCAN_TXEFC[15-2] EFSA field.

12.5.1.4.9 FIFO Acknowledge Handling

The Get Indices of the two Rx FIFOs (Rx FIFO 0 or Rx FIFO 1) and the Tx Event FIFO are controlled by writing to the corresponding FIFO Acknowledge Index (see MCAN_RXF0A, MCAN_RXF1A, and MCAN_TXEFA). Writing to the FIFO Acknowledge Index will set the FIFO Get Index to the FIFO Acknowledge Index plus one and thereby updates the FIFO Fill Level.

There are two use cases:

- A single element has been read from the FIFO: the Get Index value is written to the FIFO Acknowledge Index.
- A sequence of elements has been read from the FIFO: the Get Index value (Index of the last element read) is written to the FIFO Acknowledge Index at the end of that read sequence.

The Host CPU has free access to the Message RAM. The special care has to be taken when reading FIFO elements in an arbitrary order (Get Index not considered). This can be useful when reading a High Priority Message from one of the two Rx FIFOs. In this case the FIFO's Acknowledge Index should not be written because this would set the Get Index to a wrong position and also changes the FIFO's Fill Level. In this case some of the older FIFO elements would be lost.

Note

The application has to ensure that a valid value is written to the FIFO Acknowledge Index. The MCAN module does not check for erroneous values.

12.5.1.4.10 Message RAM

The MCAN module has implemented Message RAM. The main purpose of the Message RAM is to store:

- Receive Messages
- Transmit Messages
- Tx Event Elements
- Message ID Filter Elements

12.5.1.4.10.1 Message RAM Configuration

The MCAN module is configured to allocate 4352 words in the Message RAM. The Message RAM has a width of 32 bits.

The Message RAM is capable to include each of the sections listed in Figure 12-272. It is not necessary to configure each of the sections (a section in the Message RAM may be 0) and there is not restriction with respect to the sequence of the sections. For parity checking or ECC a respective number of bits has to be added to each word.

When the MCAN module addresses the Message RAM it addresses 32-bit words. The start addresses are configurable and they are 32-bit word addresses.

The element size can be configured for:

- Rx FIFO 0 via the MCAN_RXESC[2-0] F0DS field
- Rx FIFO 1 via the MCAN_RXESC[6-4] F1DS field
- Rx Buffers via the MCAN_RXESC[10-8] RBDS field
- Tx Buffers via the MCAN_TXESC[2-0] TBDS field

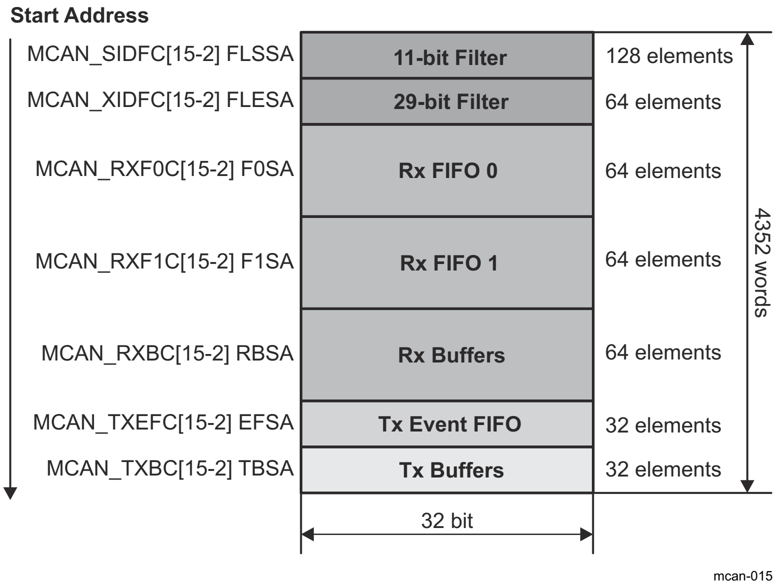


Figure 12-272. Message RAM Configuration

The Host CPU configures the following information in the Message RAM:

- Start addresses of the memory sections
- Number of elements in each section
- The size of the elements in some sections

Note

The MCAN module does not check for errors in the Message RAM configuration. The configuration of the start addresses of the different sections and the number of elements of each section has to be done carefully. This will prevent falsification or loss of data.

12.5.1.4.10.2 Rx Buffer and FIFO Element

Up to 64 Rx Buffers and two Rx FIFOs can be configured in the Message RAM. Each Rx FIFO section can be configured to store up to 64 received messages. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via the MCAN_RXESC register.

Figure 12-273 shows Rx Buffer/Rx FIFO element structure.

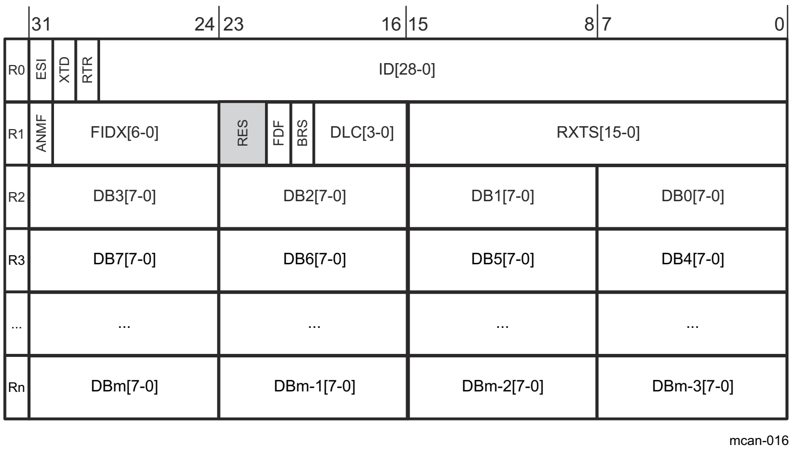


Figure 12-273. Rx Buffer/Rx FIFO Element Structure

Table 12-253 shows Rx Buffer/Rx FIFO element field descriptions.

Table 12-253. Rx Buffer/Rx FIFO Element Field Descriptions

Word	Bits	Field Name	Description
R0	31	ESI	Error State Indicator • 0h = Transmitting node is error active • 1h = Transmitting node is error passive
	30	XTD	Extended Identifier Signals to the Host CPU whether the received frame has a standard or extended identifier. • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier
	29	RTR	Remote Transmission Request Signals to the Host CPU whether the received frame is a data frame or a remote frame. • 0h = Received frame is a data frame • 1h = Received frame is a remote frame **Note:** There are no remote frames in CAN FD format. In case a CAN FD frame was received (FDF = 1), RTR bit reflects the state of the reserved r1 bit (RES[23]).
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier is stored into ID[28-18].

Table 12-253. Rx Buffer/Rx FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
R1	31	ANMF	Accepted Non-matching Frame Acceptance of non-matching frames may be enabled via the MCAN_GFC[5-4] ANFS and MCAN_GFC[3-2] ANFE fields. • 0h = Received frame matching filter index FIDX field • 1h = Received frame did not match any Rx filter element
	30-24	FIDX[6-0]	Filter Index 0h-7Fh (0-127): Index of matching Rx acceptance filter element (invalid if ANMF = 1). Range is 0 to MCAN_SIDFC[23-16] LSS - 1 respectively MCAN_XIDFC[22-16] LSE - 1.
	23-22	RES	Reserved
	21	FDF	FD Format • 0h = Standard frame format • 1h = CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch • 0h = Frame received without bit rate switching • 1h = Frame received with bit rate switching
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: received frame has 0-8 data bytes • 9h-Fh (9-15) = CAN: received frame has 8 data bytes • 9h-Fh (9-15) = CAN FD: received frame has 12/16/20/24/32/48/64 data bytes
	15-0	RXTS[15-0]	Rx Timestamp Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC[19-16] TCP.
R2	31-24	DB3[7-0]	Data Byte 3
	23-16	DB2[7-0]	Data Byte 2
	15-8	DB1[7-0]	Data Byte 1
	7-0	DB0[7-0]	Data Byte 0
R3	31-24	DB7[7-0]	Data Byte 7
	23-16	DB6[7-0]	Data Byte 6
	15-8	DB5[7-0]	Data Byte 5
	7-0	DB4[7-0]	Data Byte 4
...	...	...	...
Rn	31-24	DBm[7-0]	Data Byte m
	23-16	DBm-1[7-0]	Data Byte m-1
	15-8	DBm-2[7-0]	Data Byte m-2
	7-0	DBm-3[7-0]	Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_RXESC), between two and sixteen 32-bit words (Rn = 3-17) are used for storage of a CAN message's data field.

12.5.1.4.10.3 Tx Buffer Element

The Tx Buffers section can be configured to hold dedicated Tx Buffers as well as a Tx FIFO/Tx Queue. In case that the Tx Buffers section is shared by dedicated Tx buffers and a Tx FIFO/Tx Queue, the dedicated Tx Buffers start at the beginning of the Tx Buffers section followed by the buffers assigned to the Tx FIFO or Tx Queue. The Tx Handler makes difference between dedicated Tx Buffers and Tx FIFO/Tx Queue via the MCAN_TXBC[29-24] TFQS and MCAN_TXBC[21-16] NDTB fields. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via the MCAN_TXESC register.

Figure 12-274 shows Tx Buffer element structure.

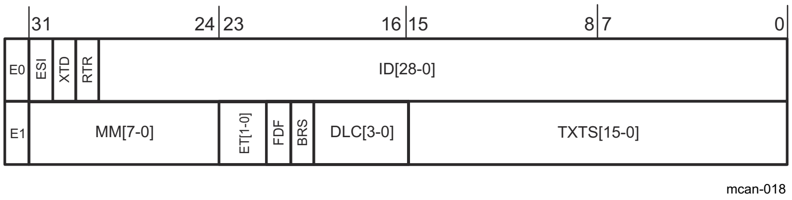


Figure 12-274. Tx Buffer Element Structure

Table 12-254 shows Tx Buffer element field descriptions.

Table 12-254. Tx Buffer Element Field Descriptions

Word	Bits	Field Name	Description
T0	31	ESI	Error State Indicator • 0h = ESI bit in CAN FD format depends only on error passive flag • 1h = ESI bit in CAN FD format transmitted recessive **Note:** The ESI bit of the transmit buffer is or'ed with the error passive flag to decide the value of the ESI bit in the transmitted CAN FD frame. As required by the CAN FD protocol specification, an error active node may optionally transmit the ESI bit recessive, but an error passive node will always transmit the ESI bit recessive.
	30	XTD	Extended Identifier • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier
	29	RTR	Remote Transmission Request • 0h = Transmit data frame • 1h = Transmit remote frame **Note:** When RTR = 1, the MCAN module transmits a remote frame according to ISO11898-1:2015, even if the MCAN_CCCR[8] FDOE bit enables the transmission in CAN FD format.
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier has to be written to ID[28-18].

Table 12-254. Tx Buffer Element Field Descriptions (continued)

Word	Bits	Field Name	Description
T1	31-24	MM[7-0]	Message Marker Written by Host CPU during Tx Buffer configuration. Copied into Tx Event FIFO element for identification of Tx message status (see also MM[7-0] field in Table 12-255).
	23	EFC	Event FIFO Control • 0h = Don't store Tx events • 1h = Store Tx events
	22	RES	Reserved
	21	FDF	FD Format • 0h = Frame transmitted in Classic CAN format • 1h = Frame transmitted in CAN FD format
	20	BRS	Bit Rate Switch • 0h = CAN FD frames transmitted without bit rate switching • 1h = CAN FD frames transmitted with bit rate switching **Note:** ESI, FDF, and BRS bits are only evaluated when CAN FD operation is enabled vie the MCAN_CCCR[8] FDOE bit. BRS bit is only evaluated when in addition the MCAN_CCCR[9] BRSE = 1.
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: transmit frame has 0-8 data bytes • 9h-Fh (9-15) = CAN: transmit frame has 8 data bytes • 9h-Fh (9-15) = CAN FD: transmit frame has 12/16/20/24/32/48/64 data bytes
	15-0	RES	Reserved
T2	31-24	DB3[7-0]	Data Byte 3
	23-16	DB2[7-0]	Data Byte 2
	15-8	DB1[7-0]	Data Byte 1
	7-0	DB0[7-0]	Data Byte 0
T3	31-24	DB7[7-0]	Data Byte 7
	23-16	DB6[7-0]	Data Byte 6
	15-8	DB5[7-0]	Data Byte 5
	7-0	DB4[7-0]	Data Byte 4
...	...	...	...
Tn	31-24	DBm[7-0]	Data Byte m
	23-16	DBm-1[7-0]	Data Byte m-1
	15-8	DBm-2[7-0]	Data Byte m-2
	7-0	DBm-3[7-0]	Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_TXESC), between two and sixteen 32-bit words (Tn = 3-17) are used for storage of a CAN message's data field.

12.5.1.4.10.4 Tx Event FIFO Element

Each element stores information about transmitted messages. By reading the Tx Event FIFO the Host CPU gets this information in the order the messages were transmitted. Status information about the Tx Event FIFO can be obtained from the MCAN_TXEFS register.

Figure 12-275 shows Tx Event FIFO element structure.

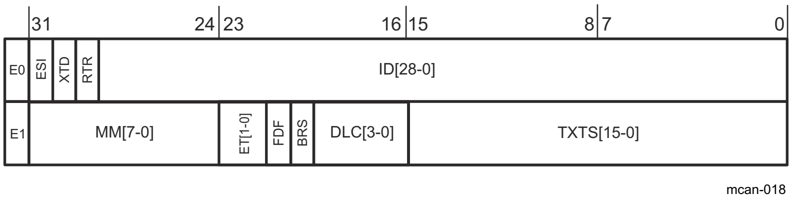


Figure 12-275. Tx Event FIFO Element Structure

Table 12-255 shows Tx Event FIFO element field descriptions.

Table 12-255. Tx Event FIFO Element Field Descriptions

Word	Bits	Field Name	Description
E0	31	ESI	Error State Indicator • 0h = Transmitting node is error active • 1h = Transmitting node is error passive
	30	XTD	Extended Identifier • 0h = 11-bit standard identifier • 1h = 29-bit extended identifier
	29	RTR	Remote Transmission Request • 0h = Data frame transmitted • 1h = Remote frame transmitted
	28-0	ID[28-0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier has to be written to ID[28-18].

Table 12-255. Tx Event FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
E1	31-24	MM[7-0]	Message Marker Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status (see also MM[7-0] field in Table 12-254).
	23-22	ET[1-0]	Event Type • 0h = Reserved • 1h = Tx event • 2h = Transmission in spite of cancellation (always set for transmissions in DAR mode) • 3h = Reserved
	21	FDF	FD Format • 0h = Standard frame format • 1h = CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch • 0h = Frame transmitted without bit rate switching • 1h = Frame transmitted with bit rate switching
	19-16	DLC[3-0]	Data Length Code • 0h-8h (0-8) = CAN + CAN FD: frame with 0-8 data bytes transmitted • 9h-Fh (9-15) = CAN: frame with 8 data bytes transmitted • 9h-Fh (9-15) = CAN FD: frame with 12/16/20/24/32/48/64 data bytes transmitted
	15-0	TXTS[15-0]	Tx Timestamp Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC[19-16] TCP field.

12.5.1.4.10.5 Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, its address is the Filter List Standard Start Address MCAN_SIDFC[15-2] FLSSA field plus the index of the filter element (0-127).

Figure 12-276 shows Standard Message ID Filter element structure.

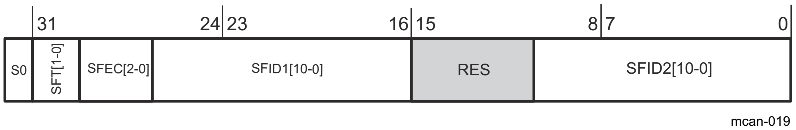


Figure 12-276. Standard Message ID Filter Element Structure

Table 12-256 shows Standard Message ID Filter element field descriptions.

Table 12-256. Standard Message ID Filter Element Field Descriptions

Word	Bits	Field Name	Description
S0	31-30	SFT[1-0]	Standard Filter Type • 0h = Range filter from SFID1 to SFID2 (SFID2 ≥ SFID1) • 1h = Dual ID filter for SFID1 or SFID2 • 2h = Classic filter: SFID1 = filter; SFID2 = mask • 3h = Filter element disabled **Note:** With SFT = 11 the filter element is disabled and the acceptance filtering continues (same behaviour as with SFEC = 000)
	29-27	SFEC[2-0]	Standard Filter Element Configuration All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = 100, 101, or 110 a match sets interrupt flag MCAN_IR[8]HPM and, if enabled, an interrupt is generated. In this case the MCAN_HPMS register is updated with the status of the priority match. • 0h = Disable filter element • 1h = Store in Rx FIFO 0 if filter matches • 2h = Store in Rx FIFO 1 if filter matches • 3h = Reject ID if filter matches • 4h = Set priority if filter matches • 5h = Set priority and store in FIFO 0 if filter matches • 6h = Set priority and store in FIFO 1 if filter matches • 7h = Store into Rx Buffer , configuration of SFT[1-0] ignored
	26-16	SFID1[10-0]	Standard Filter ID 1 When filtering for Rx Buffers this field defines the ID of a standard message to be stored. The received identifiers must match exactly, no masking mechanism is used.
	15-11	RES	Reserved
	10-0	SFID2[10-0]	Standard Filter ID 2 This bit field has a different meaning depending on the configuration of SFEC: • 1) SFEC = 001 - 110 Second ID of standard ID filter element • 2) SFEC = 111 Filter for Rx Buffers
		SFID2[10-9]	This field is decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. • 0h = Store message into an Rx Buffer • 1h = Debug Message A • 2h = Debug Message B • 3h = Debug Message C **Note:** Debug feature is not supported.
		SFID2[8-6]	This field is used to control the filter event pins at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one MCAN_ICKL period in case the filter matches. **Note:** Only three filter event pins are supported.
		SFID2[5-0]	This field defines the offset to the Rx Buffer Start Address MCAN_RXBC[15-2] RBSA field for storage of a matching message.

12.5.1.4.10.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address MCAN_XIDFC[15-2] FLESA field plus two times the index of the filter element (0-63).

Figure 12-277 shows Extended Message ID Filter element structure.

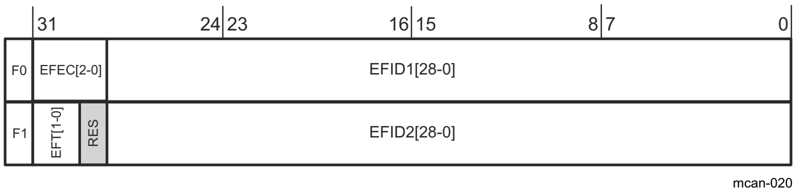


Figure 12-277. Extended Message ID Filter Element Structure

Table 12-257 shows Extended Message ID Filter element field descriptions.

Table 12-257. Extended Message ID Filter Element Field Descriptions

Word	Bits	Field Name	Description
F0	31-29	EFEC[2-0]	Extended Filter Element Configuration All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = 100, 101, or 110 a match sets interrupt flag MCAN_IR[8]HPM and, if enabled, an interrupt is generated. In this case the MCAN_HPMS register is updated with the status of the priority match. • 0h = Disable filter element • 1h = Store in Rx FIFO 0 if filter matches • 2h = Store in Rx FIFO 1 if filter matches • 3h = Reject ID if filter matches • 4h = Set priority if filter matches • 5h = Set priority and store in FIFO 0 if filter matches • 6h = Set priority and store in FIFO 1 if filter matches • 7h = Store into Rx Buffer or as debug message, configuration of EFT[1-0] ignored
	28-0	EFID1[28-0]	Extended Filter ID 1 First ID of extended ID filter element. When filtering for Rx Buffers this field defines the ID of an extended message to be stored. The received identifiers must match exactly, only XIDAM masking mechanism (see Section 12.5.1.4.7.1.5, *Extended Message ID Filtering*) is used.

Table 12-257. Extended Message ID Filter Element Field Descriptions (continued)

Word	Bits	Field Name	Description
F1	31-30	EFT[1-0]	Extended Filter Type • 0h = Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1) • 1h = Dual ID filter for EFID1 or EFID2 • 2h = Classic filter: EFID1 = filter, EFID2 = mask • 3h = Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1), XIDAM mask not applied
	29	RES	Reserved
	28-0	EFID2[28-0]	Extended Filter ID 2 This bit field has a different meaning depending on the configuration of EFEC: • 1) EFEC = 001 - 110 Second ID of extended ID filter element • 2) EFEC = 111 Filter for Rx Buffers
		EFID2[10-9]	This field decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. • 0h = Store message into an Rx Buffer • 1h = Debug Message A • 2h = Debug Message B • 3h = Debug Message C **Note:** Debug feature is not supported.
		EFID2[8-6]	This field is used to control the filter event pins at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one MCAN_ICKL period in case the filter matches. **Note:** Only three filter event pins are supported.
		EFID2[5-0]	This field defines the offset to the Rx Buffer Start Address MCAN_RXBC[15-2] RBSA field for storage of a matching message.

12.5.2 Enhanced Capture (ECAP) Module

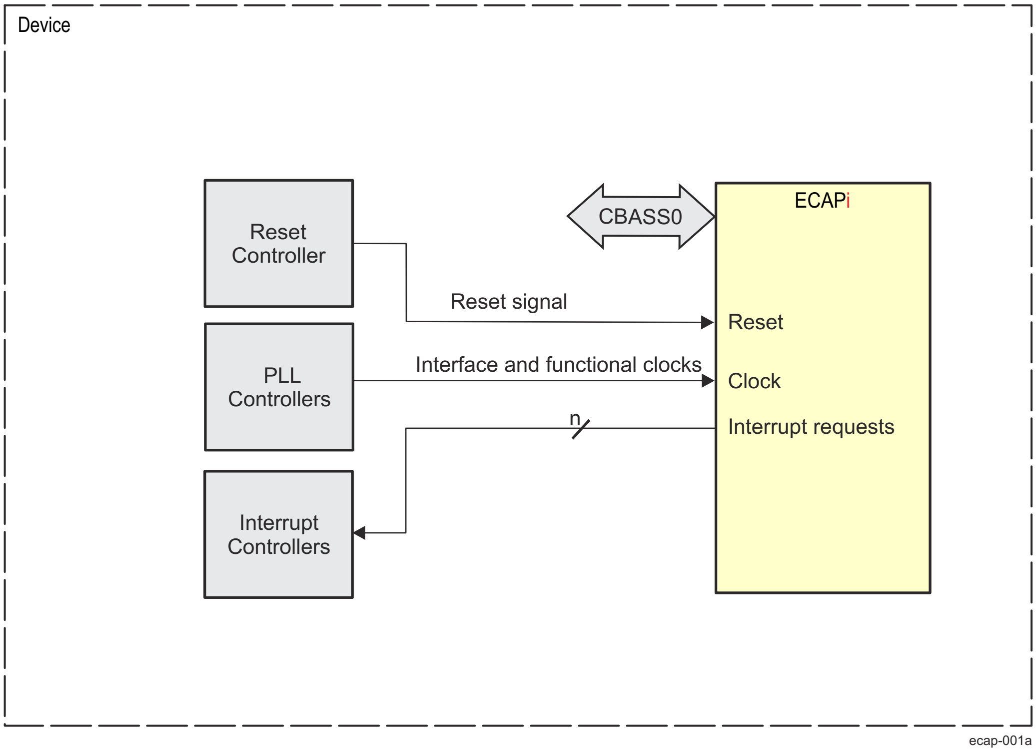
This section describes the Enhanced Capture (ECAP) module in the device.

12.5.2.1 ECAP Overview

The Enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

Figure 12-278 shows the ECAP modules overview.



A. i = 0 to number of instances - 1.

Figure 12-278. ECAP Overview

12.5.2.1.1 ECAP Features

The ECAP module includes the following features:

- 32-bit time base counter
- 4 × 32 bits event time-stamp capture registers (ECAP0_CAP1 through ECAP0_CAP4)
- 4-stage sequencer (Mod4 counter), synchronized to external events (ECAPx pin edges)
- Independent edge polarity (rising / falling edge) selection for all 4 sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Interrupt capabilities on any of the 4 capture events
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

12.5.2.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

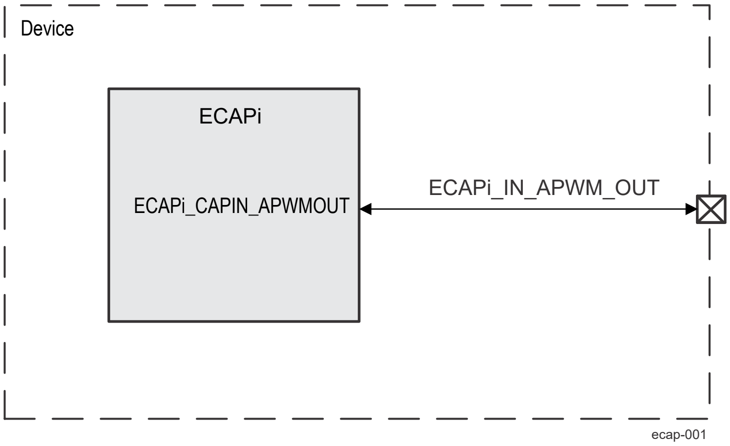
Some features may not be available. See *Module Integration* for more information.

12.5.2.2 ECAP Environment

12.5.2.2.1 ECAP I/O Interface

This section describes the ECAP external connections (environment).

Figure 12-279 shows the ECAP interface signals.



Note

i represents an ECAP instance. See the device datasheet for available domains and ECAP instances

Figure 12-279. ECAP External Interface I/Os

Table 12-258 describes the ECAP I/O signals.

Table 12-258. ECAP I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
		ECAPi[3]		
ECAPi[3]_CAPIN_APWMOUT	ECAPi[3]_IN_APWM_OUT	I/O	ECAPi[3] Capture input / PWM output	HiZ

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) i represents an ECAP instance. See the device datasheet for available domains and ECAP instances

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.5.2.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.5.2.4 ECAP Functional Description

The ECAP module represents one complete capture channel, which has the following independent key resources:

- Dedicated input capture pin
- 32 events selection mapping capability to the input capture pin
- 32-bit time base counter
- 4 × 32-bit time-stamp capture registers (ECAP0_CAP1 through ECAP0_CAP4)
- 4-stage sequencer (Mod4 counter) that is synchronized to external events, ECAP pin rising/falling edges.
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Input capture signal prescaling (from 2-62)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Control for continuous time-stamp captures using a 4-deep circular buffer (ECAP0_CAP1 through ECAP0_CAP4) scheme
- Interrupt capabilities on any of the 4 capture events

Multiple identical ECAP modules can be contained in a system as shown in Figure 12-280. For actual number of the ECAP modules integrated in the device, refer to *ECAP Integration*. The letter x within a signal or module name is used to indicate a generic ECAP instance on a device. For example, output interrupt request, ECAP1INT belongs to ECAP1, ECAP2INT belongs to ECAP2, and so forth.

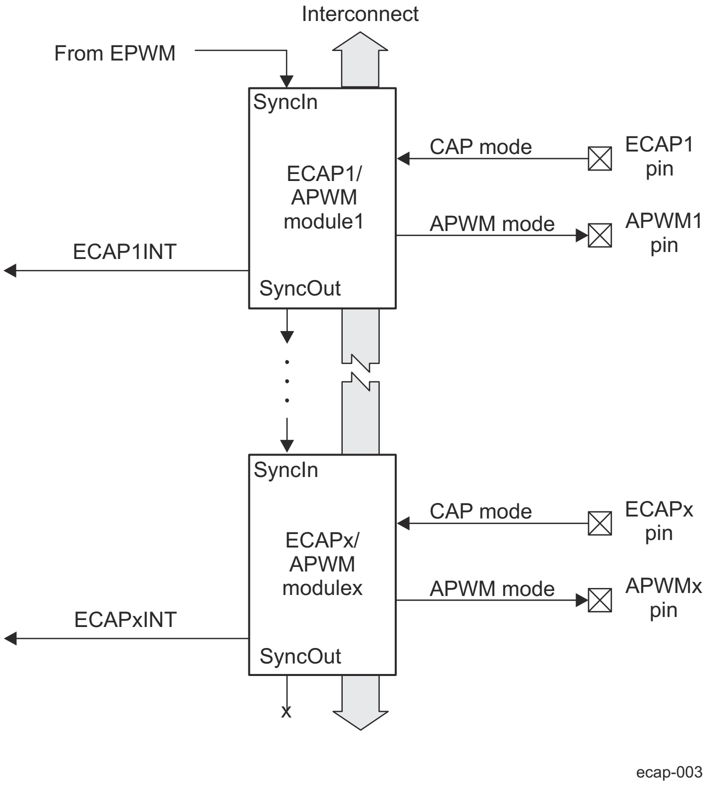
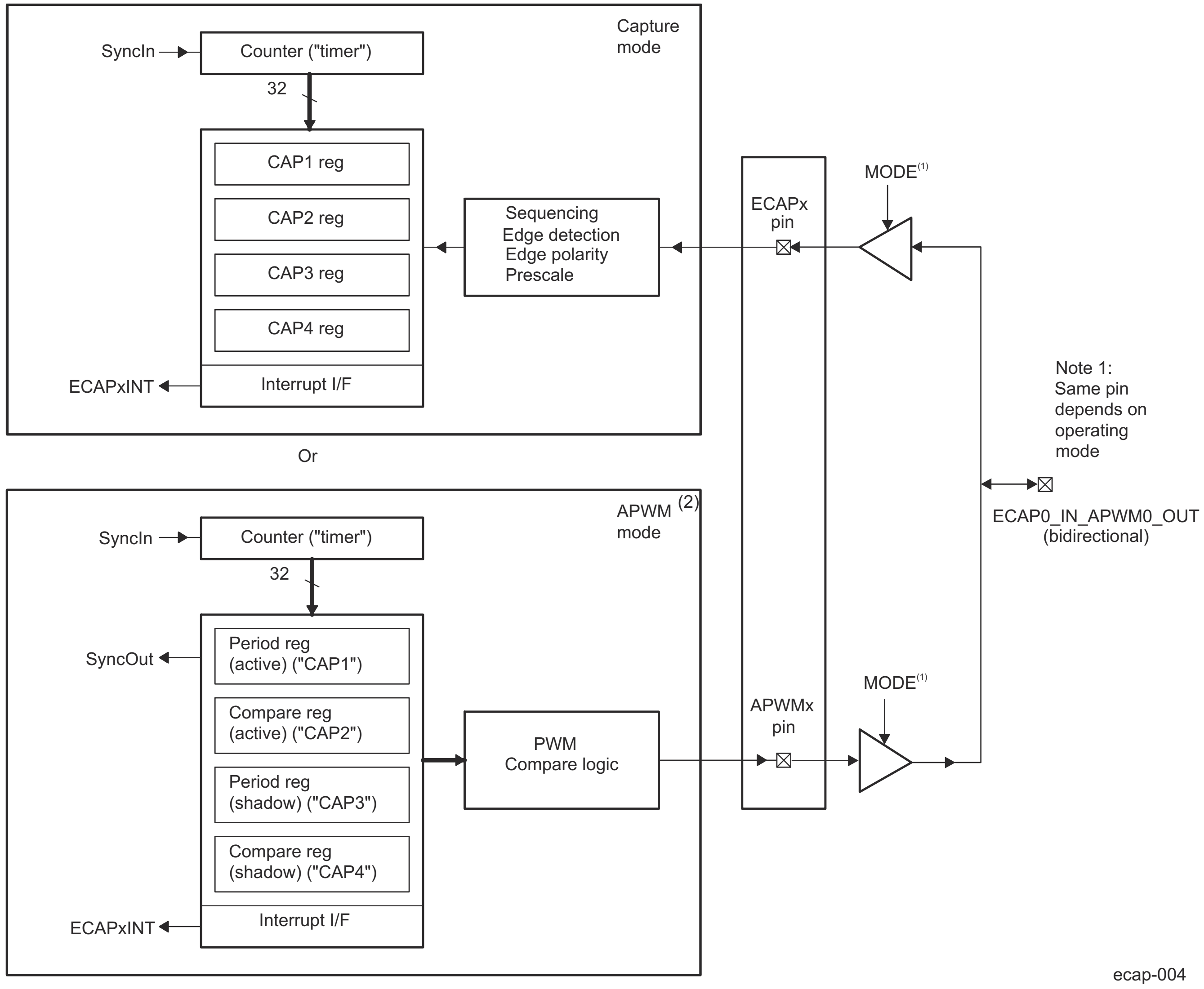


Figure 12-280. Multiple ECAP Modules

12.5.2.4.1 Capture and APWM Operating Modes

The ECAP module resources can be used to implement a single-channel PWM generator (with 32-bit capabilities) when it is not being used for input captures. The counter operates in count-up mode, providing a time-base for asymmetrical pulse width modulation (PWM) waveforms. The ECAP0_CAP1 and ECAP0_CAP2 registers become the active period and compare registers, respectively, while the ECAP0_CAP3 and ECAP0_CAP4 registers become the period and capture shadow registers, respectively. Figure 12-281 is a high-level view of both the capture and auxiliary pulse-width modulator (APWM) modes of operation.



A. A single pin is shared between CAP and APWM functions. In capture mode, it is an input. In APWM mode, it is an output.

B. In APWM mode, writing any value to the ECAP0_CAP1/ECAP0_CAP2 active registers also writes the same value to the corresponding shadow registers (ECAP0_CAP3/ECAP0_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP0_CAP3/ECAP0_CAP4) invokes the shadow mode.

Figure 12-281. Capture and APWM Modes of Operation

12.5.2.4.1.1 ECAP Capture Mode Description

Figure 12-282 shows the various components that implement the capture function.

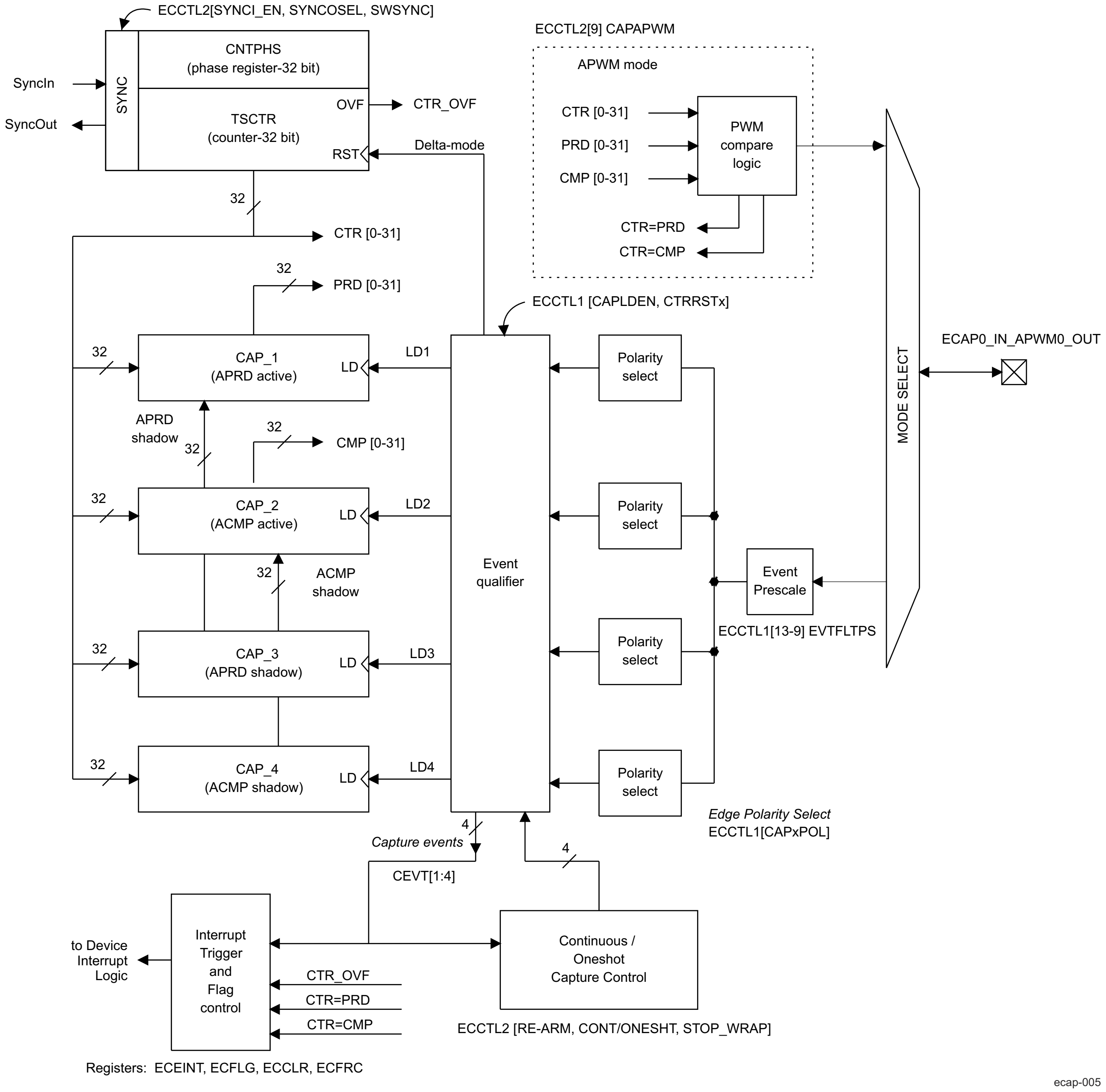
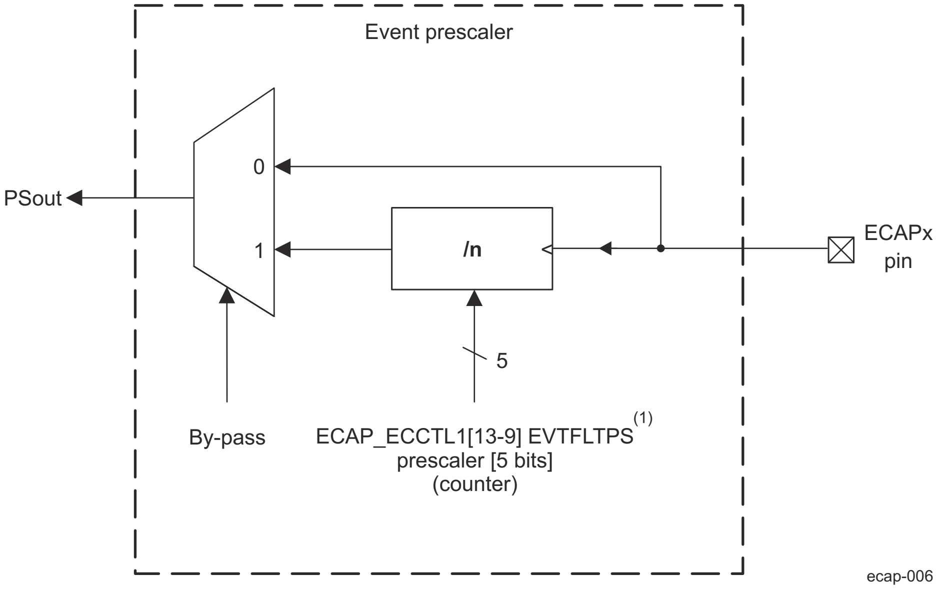


Figure 12-282. Capture Function Diagram

12.5.2.4.1.1.1 ECAP Event Prescaler

An input capture signal (pulse train) can be prescaled by N = 2-62 (in multiples of 2) or can bypass the prescaler. This is useful when very high frequency signals are used as inputs. Figure 12-283 shows a functional diagram and Figure 12-284 shows the operation of the prescale function.



A. When a prescale value of 1 is chosen (ECAP0_ECCTL[13-9] EVTFLTPS = 0b0000) the input capture signal by-passes the prescale logic completely.

Figure 12-283. Event Prescale Control

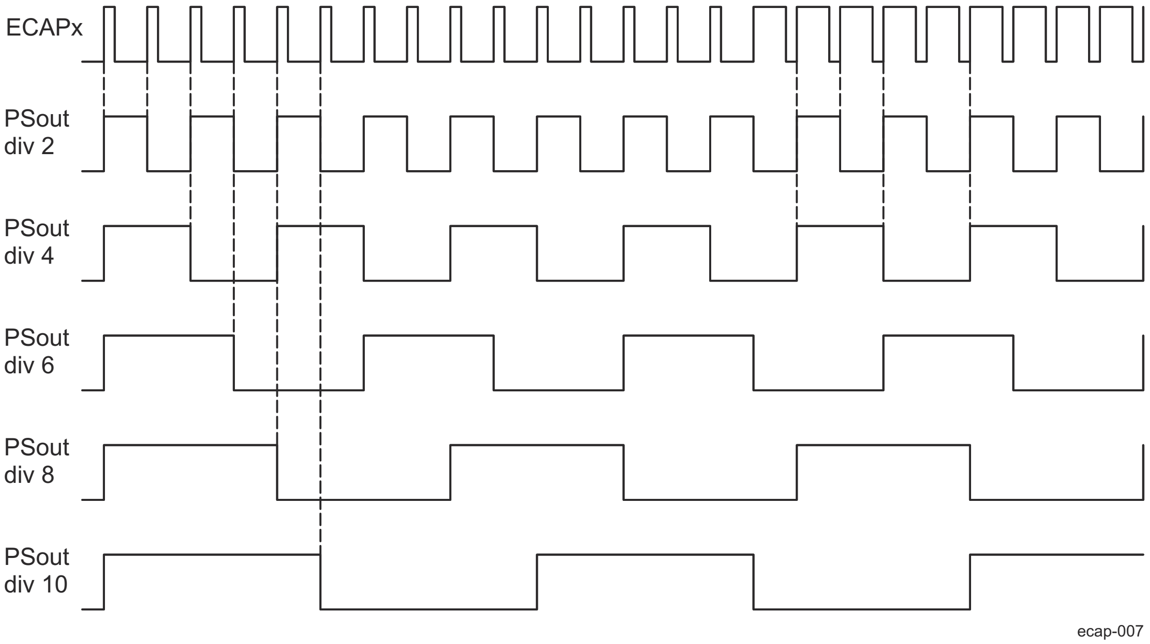


Figure 12-284. Prescale Function Waveforms

12.5.2.4.1.1.2 ECAP Edge Polarity Select and Qualifier

- Four independent edge polarity (rising edge/falling edge) selection multiplexers are used, one for each capture event.
- Each edge (up to 4) is event qualified by the Mod4 sequencer.
- The edge event is gated to its respective CAP*n* register by the Mod4 counter. The CAP*n* register is loaded on the falling edge.

12.5.2.4.1.1.3 ECAP Continuous/One-Shot Control

- The Mod4 (2-bit) counter is incremented via edge qualified events CEVT1 through CEVT4 (see the ECAP0_ECINT_EN_FLG register).
- The Mod4 counter continues counting (0->1->2->3->0) and wraps around unless stopped.
- A 2-bit stop register is used to compare the Mod4 counter output; when equal the Mod4 counter stops and inhibits further loads of the ECAP0_CAP1 through ECAP0_CAP4 registers. This occurs during one-shot operation.

The continuous/one-shot block (Figure 12-285) controls the start/stop and reset (zero) functions of the Mod4 counter via a mono-shot type of action that can be triggered by the stop-value comparator and re-armed via software control.

Once armed, the ECAP module waits for 1-4 (defined by stop-value) capture events before freezing both the Mod4 counter and contents of the ECAP0_CAP1 through ECAP0_CAP4 registers (time-stamps).

Re-arming prepares the ECAP module for another capture sequence. Also re-arming clears (to zero) the Mod4 counter and permits loading of the ECAP0_CAP1 through ECAP0_CAP4 registers again, providing the ECAP0_ECCTL[8] CAPLDEN bit is set.

In continuous mode, the Mod4 counter continues to run (0->1->2->3->0), the one-shot action is ignored, and capture values continue to be written to the ECAP0_CAP1 through ECAP0_CAP4 registers in a circular buffer sequence.

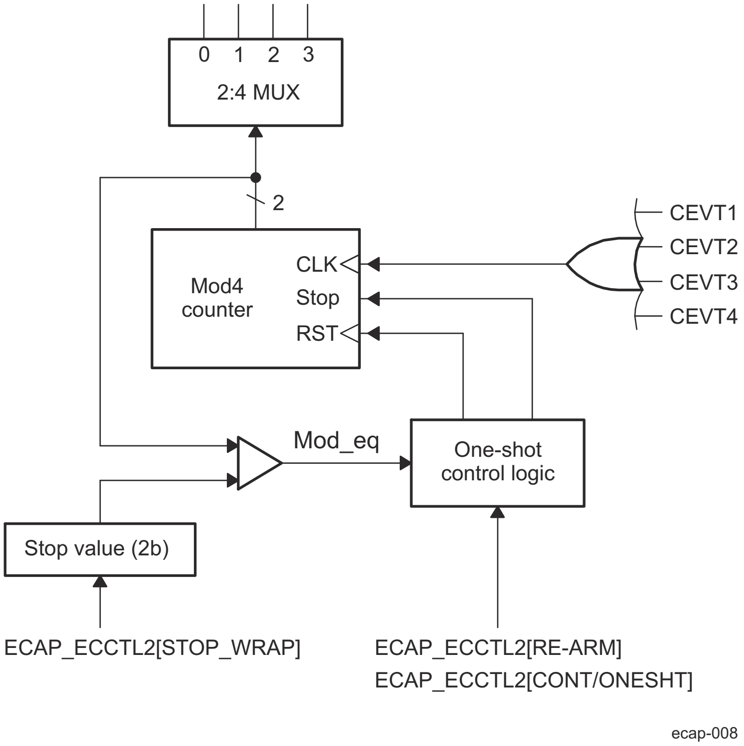


Figure 12-285. ECAP Continuous/One-shot Block Diagram

12.5.2.4.1.1.4 ECAP 32-Bit Counter and Phase Control

This counter (Figure 12-286) provides the time-base for event captures, and is clocked via the system clock.

A phase register is provided to achieve synchronization with other counters, via a hardware and software forced sync. This is useful in APWM mode when a phase offset between modules is needed.

On any of the four event loads, an option to reset the 32-bit counter is given. This is useful for time difference capture. The 32-bit counter value is captured first, then it is reset to 0 by any of the LD1 through LD4 signals.

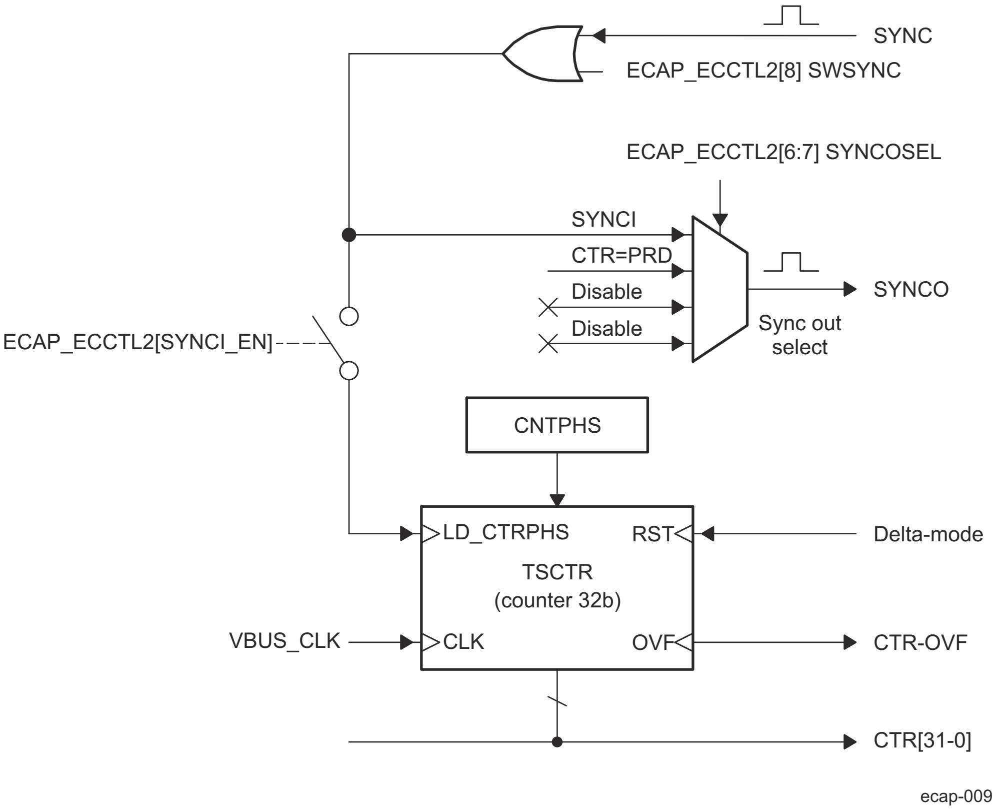


Figure 12-286. ECAP Counter and Synchronization Block Diagram

12.5.2.4.1.1.5 CAP1-CAP4 Registers

These 32-bit registers are fed by the 32-bit counter timer bus, CTR[0-31] and are loaded (capture a time-stamp) when their respective LD inputs are strobed.

Loading of the capture registers can be inhibited via the control ECAP0_ECCTL[8] CAPLDEN bit. During one-shot operation, this bit is cleared (loading is inhibited) automatically when a stop condition occurs, StopValue = Mod4.

The ECAP0_CAP1 and ECAP0_CAP2 registers become the active period and compare registers, respectively, in APWM mode.

The ECAP0_CAP3 and ECAP0_CAP4 registers become the respective shadow registers (APRD and ACMP) for the ECAP0_CAP1 and ECAP0_CAP2 registers during APWM operation.

12.5.2.4.1.1.6 ECAP Interrupt Control

An interrupt can be generated on capture events CEVT1 through CEVT4, CNTOVF (see the ECAP0_ECINT_EN_FLG[21] CNTOVF_FLG bit) or APWM events (TSCNT = PRD, TSCNT = CMP). See Figure 12-287.

A counter overflow event (FFFF FFFFh->0000 0000h) is also provided as an interrupt source (CNTOVF).

The capture events are edge and sequencer qualified (that is, ordered in time) by the polarity select and Mod4 gating, respectively.

One of these events can be selected as the interrupt source (from the ECAP*n* module) going to the interrupt controller.

Seven interrupt events (CEVT1, CEVT2, CEVT3, CEVT4, CNTOVF, TSCNT = PRD, TSCNT = CMP) can be generated. The interrupt enable register (ECAP0_ECINT_EN_FLG) is used to enable/disable individual interrupt event sources. The interrupt flag register (ECAP0_ECINT_EN_FLG) indicates if any interrupt event has been latched and contains the global interrupt flag ECAP0_ECINT_EN_FLG[16] INT_FLG bit. An interrupt pulse is generated to the interrupt controller only if any of the interrupt events are enabled, the flag bit is 1h, and the INT_FLG flag bit is 0h. The interrupt service routine must clear the global interrupt flag bit and the serviced event via the interrupt clear register (ECAP0_ECINT_CLR_FRC) before any other interrupt pulses are generated. The interrupt force register (ECAP0_ECINT_CLR_FRC) can force an interrupt event. This is useful for test purposes.

12.5.2.4.1.1.7 ECAP Shadow Load and Lockout Control

In capture mode, this logic inhibits (locks out) any shadow loading of the ECAP0_CAP1 or ECAP0_CAP2 registers from APRD and ACMP registers, respectively.

In APWM mode, shadow loading is active and two choices are permitted:

- Immediate - APRD or ACMP are transferred to the ECAP0_CAP1 or ECAP0_CAP2 register immediately upon writing a new value.
- On period equal, CTR[31-0] = PRD[31-0]

Note

The CEVT1_FLG, CEVT2_FLG, CEVT3_FLG, CEVT4_FLG flags are only active in capture mode (ECAP0_ECCTL[25] CAP_APWM == 0h). The TSCNT = PRD, TSCNT = CMP flags are only valid in APWM mode (ECAP0_ECCTL[25] CAP_APWM == 1h). CNTOVF_FLG flag is valid in both modes.

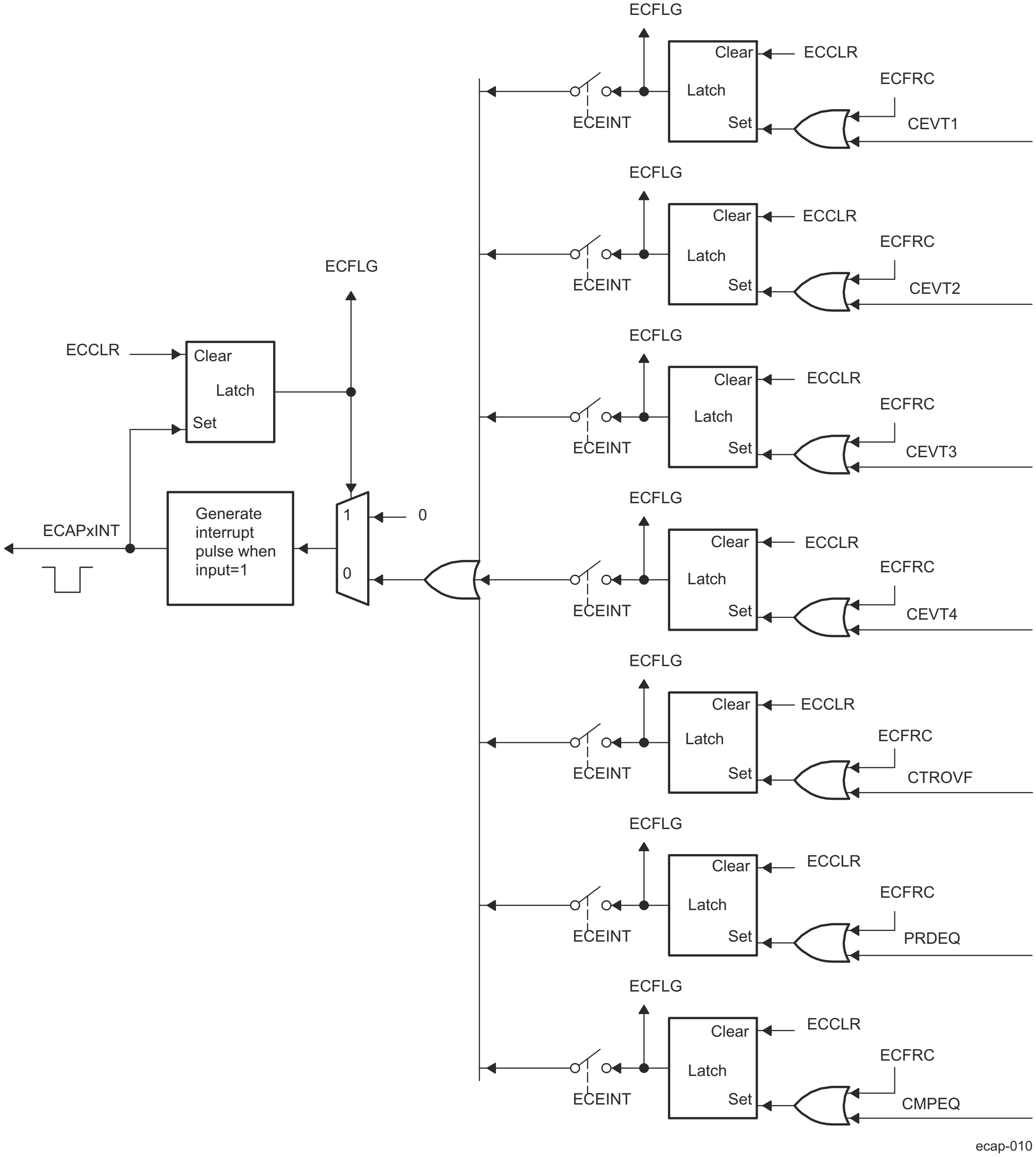


Figure 12-287. Interrupts in ECAP Module

12.5.2.4.1.2 ECAP APWM Mode Operation

Main operating highlights of the APWM section:

- The time-stamp counter bus is made available for comparison via 2 digital (32-bit) comparators.
- When the ECAP0_CAP1/ECAP0_CAP2 registers are not used in capture mode, their contents can be used as Period and Compare values in APWM mode.
- Double buffering is achieved via the shadow registers - APRD and ACMP (ECAP0_CAP3/ECAP0_CAP4). The shadow register contents are transferred over to ECAP0_CAP1/ECAP0_CAP2 registers either immediately upon a write, or on a TSCNT = PRD trigger.
- In APWM mode, writing to the ECAP0_CAP1/ECAP0_CAP2 active registers will also write the same value to the corresponding shadow registers (ECAP0_CAP3/ECAP0_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP0_CAP3/ECAP0_CAP4) will invoke the shadow mode.
- During initialization, software must write the PRD and CMP values to the active registers. This automatically copies the initial values into the shadow values. For subsequent compare updates, during run-time, software should use only shadow registers.

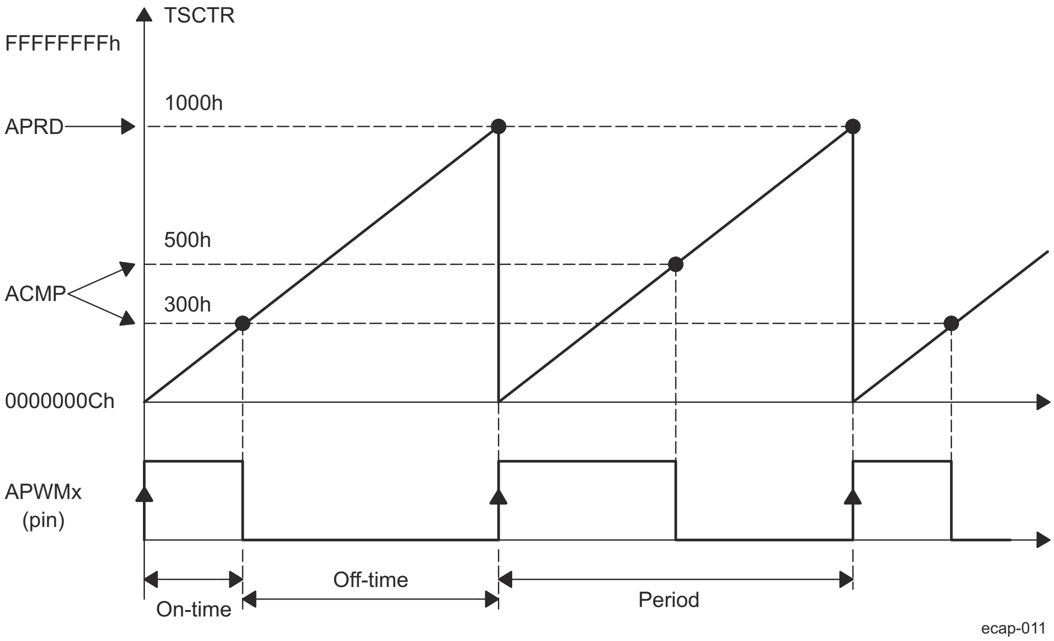


Figure 12-288. PWM Waveform Details of ECAP APWM Mode Operation

The behavior of APWM active-high mode (APWMPOL == 0) is:

```
CMP = 0x00000000, output low for duration of period (0% duty)
```

```
CMP = 0x00000001, output high 1 cycle
```

```
CMP = 0x00000002, output high 2 cycles
```

```
CMP = PERIOD, output high except for 1 cycle (<100% duty)
```

```
CMP = PERIOD+1, output high for complete period (100% duty)
```

```
CMP > PERIOD+1, output high for complete period
```

The behavior of APWM active-low mode (APWMPOL == 1) is:

```
CMP = 0x00000000, output high for duration of period (0% duty)
```

```
CMP = 0x00000001, output low 1 cycle
```

```
CMP = 0x00000002, output low 2 cycles
```

```
CMP = PERIOD, output low except for 1 cycle (<100% duty)
```

```
CMP = PERIOD+1, output low for complete period (100% duty)
```

```
CMP > PERIOD+1, output low for complete period
```

12.5.2.4.2 Summary of ECAP Functional Registers

Table 12-259 shows the ECAP module control and status register set. All 32-bit registers are aligned on even address boundaries and are organized in little-endian mode.

Note

In APWM mode, writing to the ECAP0_CAP1/ECAP0_CAP2 active registers also writes the same value to the corresponding shadow registers (ECAP0_CAP3/ECAP0_CAP4). This emulates immediate mode. Writing to the shadow registers (ECAP0_CAP3/ECAP0_CAP4) invokes the shadow mode.

Table 12-259. ECAP Control and Status Functional Registers

Offset	Register Name	Description	Size (×16)
0h	ECAP0_TSCNT	Time-Stamp Counter Register	2
4h	ECAP0_CNTPHS	Counter Phase Offset Value Register	2
8h	ECAP0_CAP1	Capture 1 Register	2
Ch	ECAP0_CAP2	Capture 2 Register	2
10h	ECAP0_CAP3	Capture 3 Register	2
14h	ECAP0_CAP4	Capture 4 Register	2
28h	ECAP0_ECCTL	Capture Control Register	2
2Ch	ECAP0_ECINT_EN_FLG	Capture Interrupt Enable and Flag Register	2
30h	ECAP0_ECINT_CLR_FRC	Capture Interrupt Clear and Forcing Register	2
5Ch	ECAP0_PID	Revision ID Register	2

Note

For more information on the ECAP registers, see *ECAP Registers.*

12.5.2.5 ECAP Use Cases

The following sections will provide applications examples and code snippets to show how to configure and operate the ECAP module. For clarity and ease of use, below are useful #defines which will help in the understanding of the examples.

```
// ECCTL1 ( ECAP Control Reg 1)
//==========================
// CAPxPOL bits
#defineEC_RISING      0x0
#defineEC_FALLING     0x1
// CTRRSTx bits
#defineEC_ABS_MODE    0x0
#defineEC_DELTA_MODE      0x1
// PRESCALE bits
#defineEC_BYPASS      0x0
#defineEC_DIV1        0x0
#defineEC_DIV2        0x1
#defineEC_DIV4        0x2
#defineEC_DIV6        0x3
#defineEC_DIV8        0x4
#defineEC_DIV10       0x5
// ECCTL2 ( ECAP Control Reg 2)
//==========================
// CONT/ONESHOT bit
#defineEC_CONTINUOUS      0x0
#defineEC_ONESHOT     0x1
// STOPVALUE bit
#defineEC_EVENT1      0x0
#defineEC_EVENT2      0x1
#defineEC_EVENT3      0x2
#defineEC_EVENT4      0x3
// RE-ARM bit
#defineEC_ARM         0x1
// TSCTRSTOP bit
#defineEC_FREEZE      0x0
#defineEC_RUN         0x1
// SYNCO_SEL bit
#defineEC_SYNCIN      0x0
#defineEC_CTR_PRD     0x1
#defineEC_SYNCO_DIS       0x2
// CAP/APWM mode bit
#defineEC_CAP_MODE    0x0
#defineEC_APWM_MODE       0x1
// APWMPOL bit
#defineEC_ACTV_HI     0x0
#defineEC_ACTV_LO     0x1
// Generic
#defineEC_DISABLE     0x0
#defineEC_ENABLE      0x1
#defineEC_FORCE       0x1
```

12.5.2.5.1 Absolute Time-Stamp Operation Rising Edge Trigger Example

Figure 12-289 shows an example of continuous capture operation (Mod4 counter wraps around). In this figure, TSCTR counts-up without resetting and capture events are qualified on the rising edge only, this gives period (and frequency) information.

On an event, the TSCTR contents (time-stamp) is first captured, then Mod4 counter is incremented to the next state. When the TSCTR reaches FFFF FFFFh (maximum value), it wraps around to 0000 0000h (not shown in Figure 12-289), if this occurs, the CNTOVF_FLG (counter overflow) flag is set, and an interrupt (if enabled) occurs. Captured time-stamps are valid at the point indicated by the diagram, after the 4-th event, hence event CEVT4 can conveniently be used to trigger an interrupt and the CPU can read data from the CAP*n* registers.

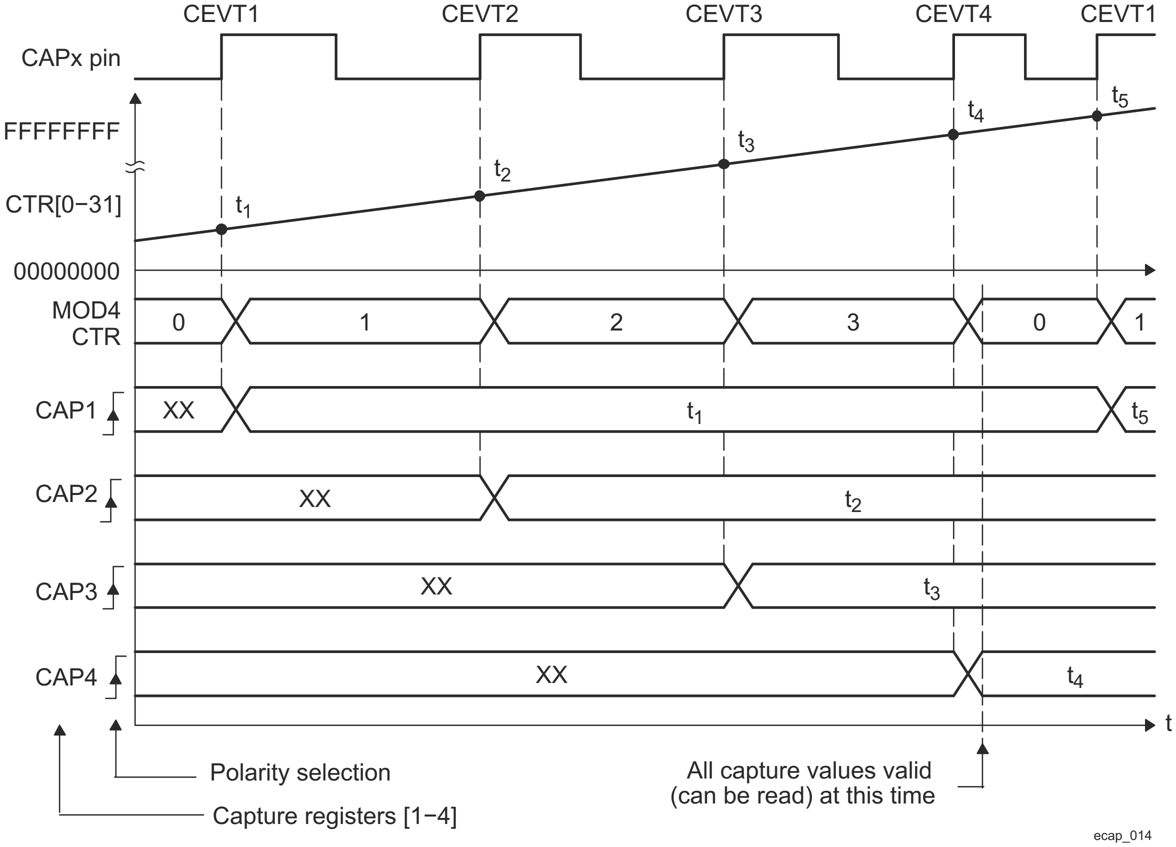


Figure 12-289. Capture Sequence for Absolute Time-Stamp, Rising Edge Detect

Table 12-260. ECAP Initialization for CAP Mode Absolute Time, Rising Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_RISING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_RISING
ECCTL1	CTRRST1	EC_ABS_MODE
ECCTL1	CTRRST2	EC_ABS_MODE
ECCTL1	CTRRST3	EC_ABS_MODE
ECCTL1	CTRRST4	EC_ABS_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Example 12-1. Code Snippet for CAP Mode Absolute Time, Rising Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising edge trigger
// Run Time ( e.g. CEVT4 triggered ISR call)
//==========================================
TSt1 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at t1
TSt2 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at t2
TSt3 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at t3
TSt4 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at t4
Period1 = TSt2-TSt1;// Calculate 1st period
Period2 = TSt3-TSt2;// Calculate 2nd period
Period3 = TSt4-TSt3;// Calculate 3rd period
```

12.5.2.5.2 Absolute Time-Stamp Operation Rising and Falling Edge Trigger Example

In Figure 12-290 the ECAP operating mode is almost the same as in the previous section except capture events are qualified as either rising or falling edge, this now gives both period and duty cycle information: Period1 = $t_3 - t_1$, Period2 = $t_5 - t_3$, …etc. Duty Cycle1 (on-time %) = $(t_2 - t_1)$ / Period1 x 100%, etc. Duty Cycle1 (off-time %) = $(t_3 - t_2)$ / Period1 x 100%, etc.

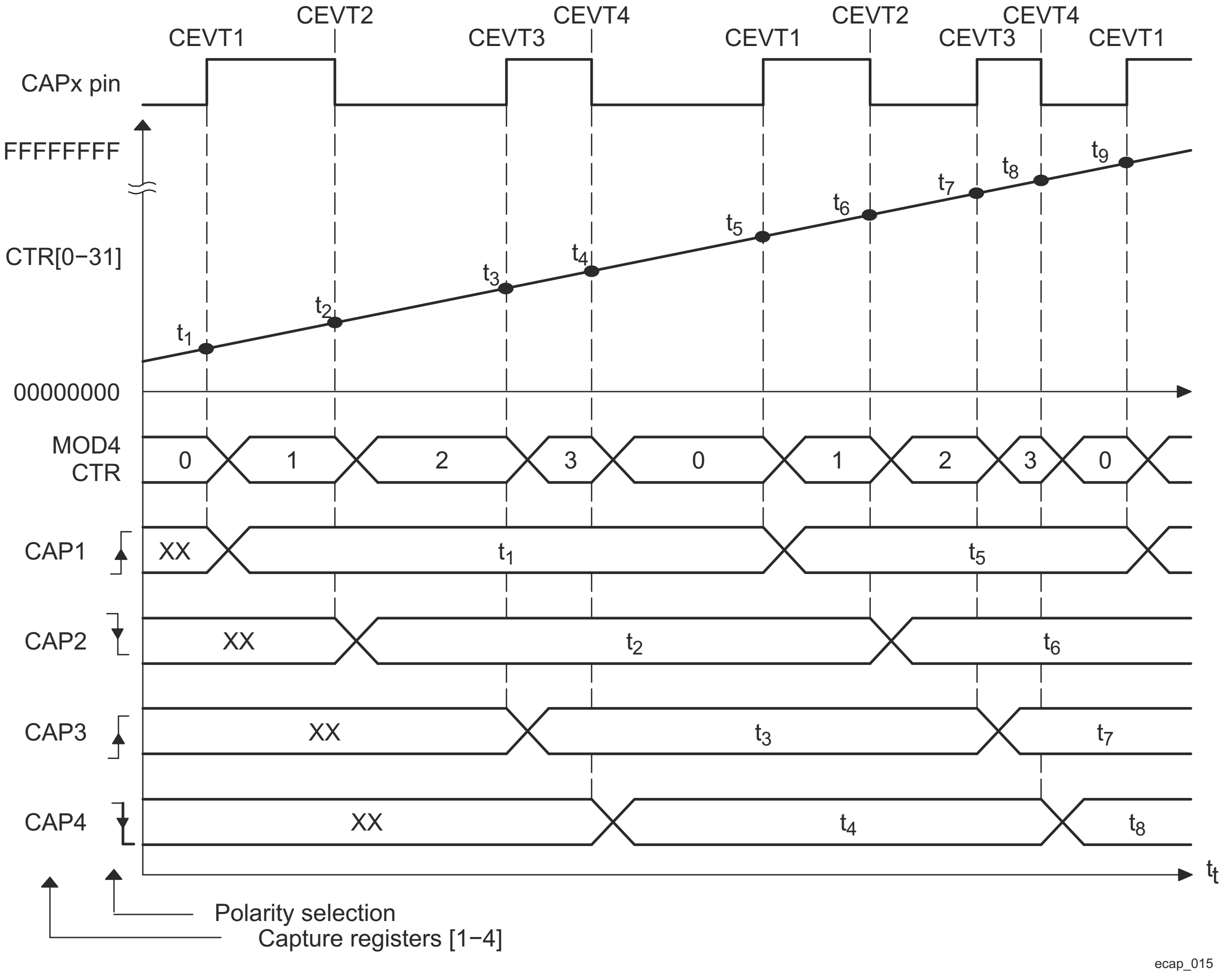


Figure 12-290. Capture Sequence for Absolute Time-Stamp, Rising and Falling Edge Detect

Table 12-261. ECAP Initialization for CAP Mode Absolute Time, Rising and Falling Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_FALLING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_FALLING
ECCTL1	CTRRST1	EC_ABS_MODE
ECCTL1	CTRRST2	EC_ABS_MODE
ECCTL1	CTRRST3	EC_ABS_MODE
ECCTL1	CTRRST4	EC_ABS_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Example 12-2. Code Snippet for CAP Mode Absolute Time, Rising and Falling Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising & Falling edge triggers
// Run Time ( e.g. CEVT4 triggered ISR call)
//==========================================
TSt1 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at t1
TSt2 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at t2
TSt3 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at t3
TSt4 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at t4
Period1 = TSt3-TSt1;// Calculate 1st period
DutyOnTime1 = TSt2-TSt1;// Calculate On time
DutyOffTime1 = TSt3-TSt2;// Calculate Off time
```

12.5.2.5.3 Time Difference (Delta) Operation Rising Edge Trigger Example

Figure 12-291 shows how the ECAP module can be used to collect Delta timing data from pulse train waveforms. Here Continuous Capture mode (TSCTR counts-up without resetting, and Mod4 counter wraps around) is used. In Delta-time mode, TSCTR is Reset back to Zero on every valid event. Here Capture events are qualified as Rising edge only. On an event, TSCTR contents (time-stamp) is captured first, and then TSCTR is reset to Zero. The Mod4 counter then increments to the next state. If TSCTR reaches FFFF FFFFh (maximum value), before the next event, it wraps around to 0000 0000h and continues, a CNTOVF_FLG (counter overflow) Flag is set, and an Interrupt (if enabled) occurs. The advantage of Delta-time Mode is that the CAP*n* contents directly give timing data without the need for CPU calculations: Period1 = T_1, Period2 = T_2,…etc. As shown in Figure 12-291, the CEVT1 event is a good trigger point to read the timing data, T_1, T_2, T_3, T_4 are all valid here.

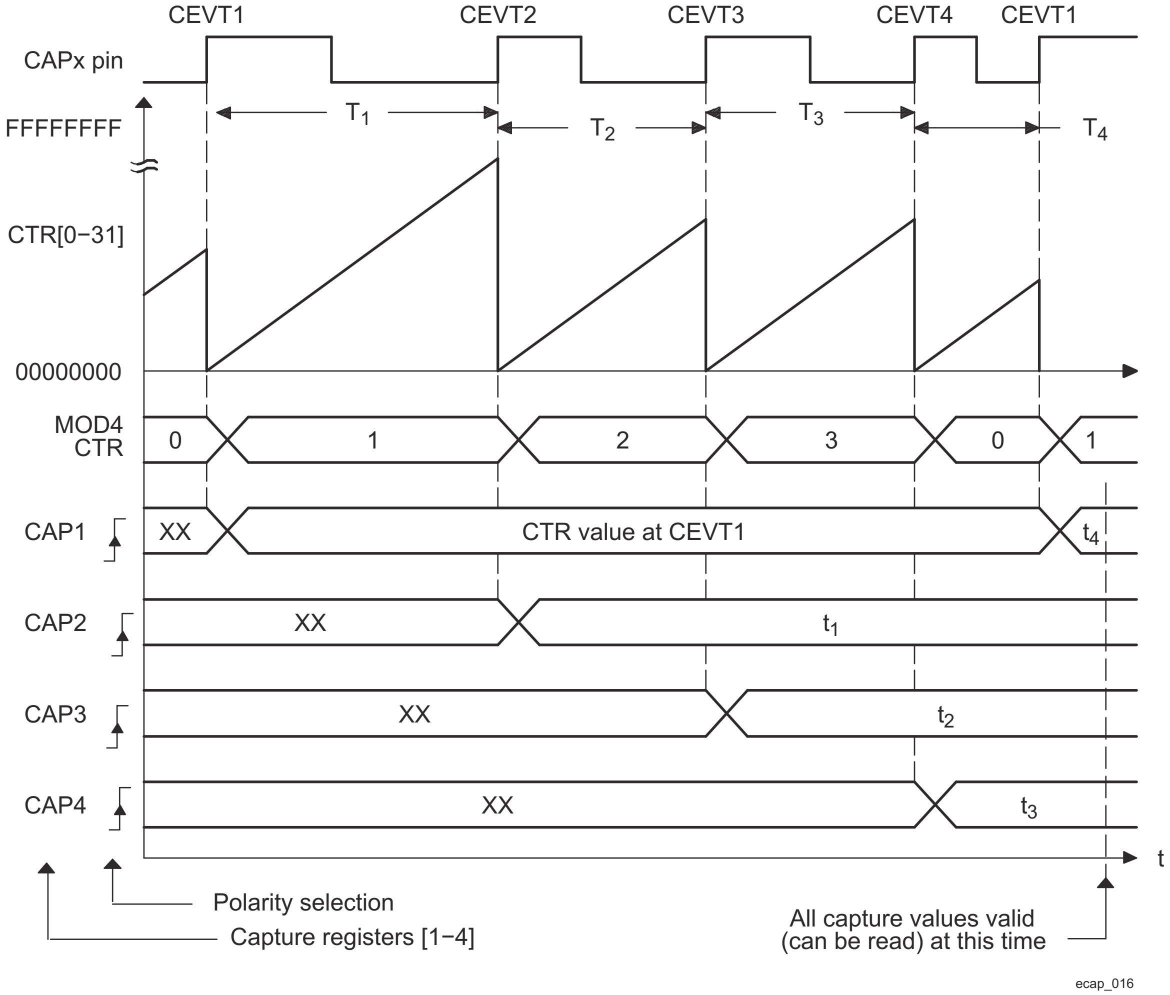


Figure 12-291. Capture Sequence for Delta Mode Time-Stamp, Rising Edge Detect

Table 12-262. ECAP Initialization for CAP Mode Delta Time, Rising Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_RISING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_RISING
ECCTL1	CTRRST1	EC_DELTA_MODE
ECCTL1	CTRRST2	EC_DELTA_MODE
ECCTL1	CTRRST3	EC_DELTA_MODE
ECCTL1	CTRRST4	EC_DELTA_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Example 12-3. Code Snippet for CAP Mode Delta Time, Rising Edge Trigger

```
// Code snippet for CAP mode Delta Time, Rising edge trigger
// Run Time ( e.g. CEVT1 triggered ISR call)
//==========================================
// Note: here Time-stamp directly represents the Period value.
Period4 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at T1
Period1 = ECAPxRegs.CAP2;// Fetch Time-Stamp captured at T2
Period2 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at T3
Period3 = ECAPxRegs.CAP4;// Fetch Time-Stamp captured at T4
```

12.5.2.5.4 Time Difference (Delta) Operation Rising and Falling Edge Trigger Example

In Figure 12-292 the ECAP operating mode is almost the same as in previous section except Capture events are qualified as either Rising or Falling edge, this now gives both Period and Duty cycle information: Period1 = T_1 + T_2, Period2 = T_3 + T_4, …etc Duty Cycle1 (on-time %) = T_1 / Period1 × 100%, etc Duty Cycle1 (off-time %) = T_2 / Period1 × 100%, etc.

During initialization, you must write to the active registers for both period and compare. This will then automatically copy the init values into the shadow values. For subsequent compare updates, that is, during run-time, only the shadow registers must be used.

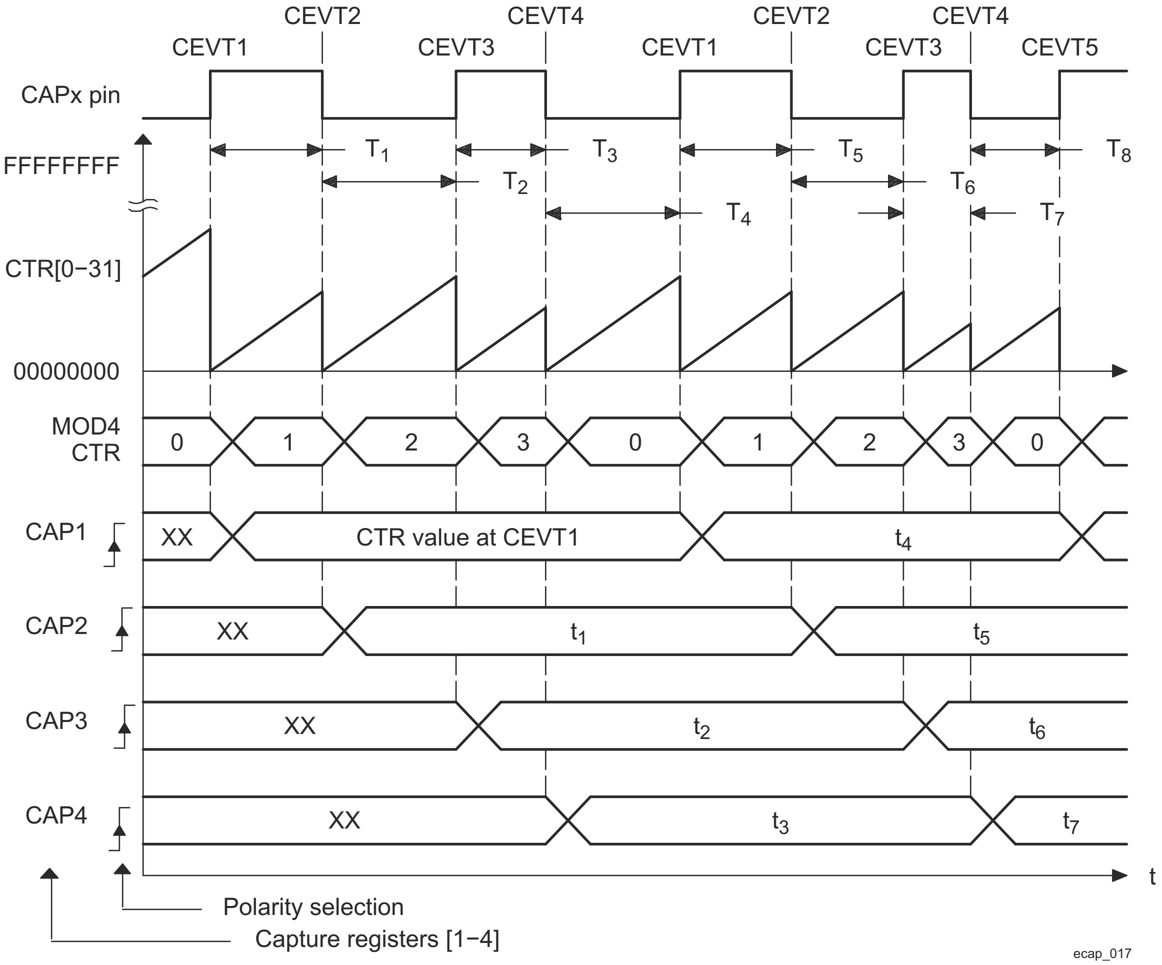


Figure 12-292. Capture Sequence for Delta Mode Time-Stamp, Rising and Falling Edge Detect

Table 12-263. ECAP Initialization for CAP Mode Delta Time, Rising and Falling Edge Triggers

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_FALLING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_FALLING
ECCTL1	CTRRST1	EC_DELTA_MODE
ECCTL1	CTRRST2	EC_DELTA_MODE
ECCTL1	CTRRST3	EC_DELTA_MODE
ECCTL1	CTRRST4	EC_DELTA_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Example 12-4. Code Snippet for CAP Mode Delta Time, Rising and Falling Edge Triggers

```
// Code snippet for CAP mode Delta Time, Rising and Falling edge triggers
// Run Time ( e.g. CEVT1 triggered ISR call)
//==========================================
// Note: here Time-stamp directly represents the Duty cycle values.
DutyOnTime1 =  ECAPxRegs.CAP2;// Fetch Time-Stamp captured at T2
DutyOffTime1 = ECAPxRegs.CAP3;// Fetch Time-Stamp captured at T3
DutyOnTime2 =  ECAPxRegs.CAP4;// Fetch Time-Stamp captured at T4
DutyOffTime2 = ECAPxRegs.CAP1;// Fetch Time-Stamp captured at T1
Period1 = DutyOnTime1 + DutyOffTime1;
Period2 = DutyOnTime2 + DutyOffTime2;
```

12.5.2.5.5 Application of the APWM Mode

12.5.2.5.5.1 Simple PWM Generation (Independent Channel/s) Example

In this example, the ECAP module is configured to operate as a PWM generator. Here a very simple single channel PWM waveform is generated from output pin APWM*n*. The PWM polarity is active high, which means that the compare value (CAP2 reg is now a compare register) represents the on-time (high level) of the period. Alternatively, if the APWMPOL bit is configured for active low, then the compare value represents the off-time.

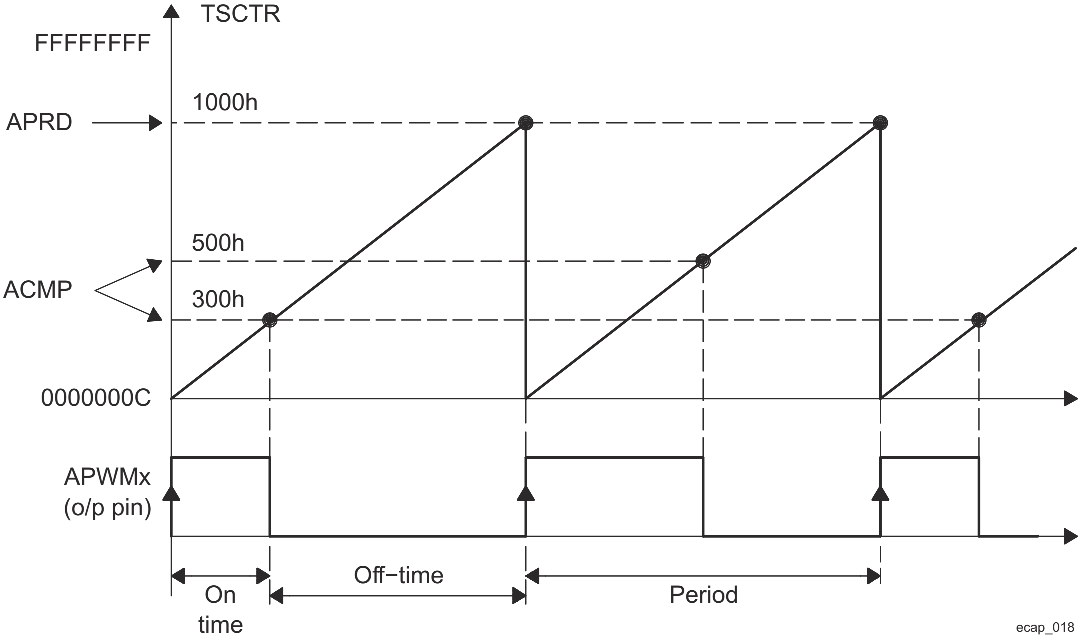


Figure 12-293. PWM Waveform Details of APWM Mode Operation

Table 12-264. ECAP Initialization for APWM Mode

Register	Bit	Value
CAP1	CAP1	0x1000
CTRPHS	CTRPHS	0x0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Example 12-5. Code Snippet for APWM Mode

```
// Code snippet for APWM mode Example 1
// Run Time (Instant 1, e.g. ISR call)
//======================
   ECAPxRegs.CAP2 = 0x300;      // Set Duty cycle i.e. compare value
// Run Time (Instant 2, e.g. another ISR call)
//======================
   ECAPxRegs.CAP2 = 0x500;      // Set Duty cycle i.e. compare value
```

12.5.2.5.5.2 Multichannel PWM Generation with Synchronization Example

Figure 12-294 takes advantage of the synchronization feature between the ECAP modules. Here 4 independent PWM channels are required with different frequencies, but at integer multiples of each other to avoid "beat" frequencies. Hence one ECAP module is configured as the Controller and the remaining 3 are Targets all receiving their synch pulse (CTR = PRD) from the controller. Note the Controller is chosen to have the lower frequency (F1 = 1/20,000) requirement. Here Target2 Freq = 2 × F1, Target3 Freq = 4 × F1 and Target4 Freq = 5 × F1. Note here values are in decimal notation. Also, only the APWM1 output waveform is shown.

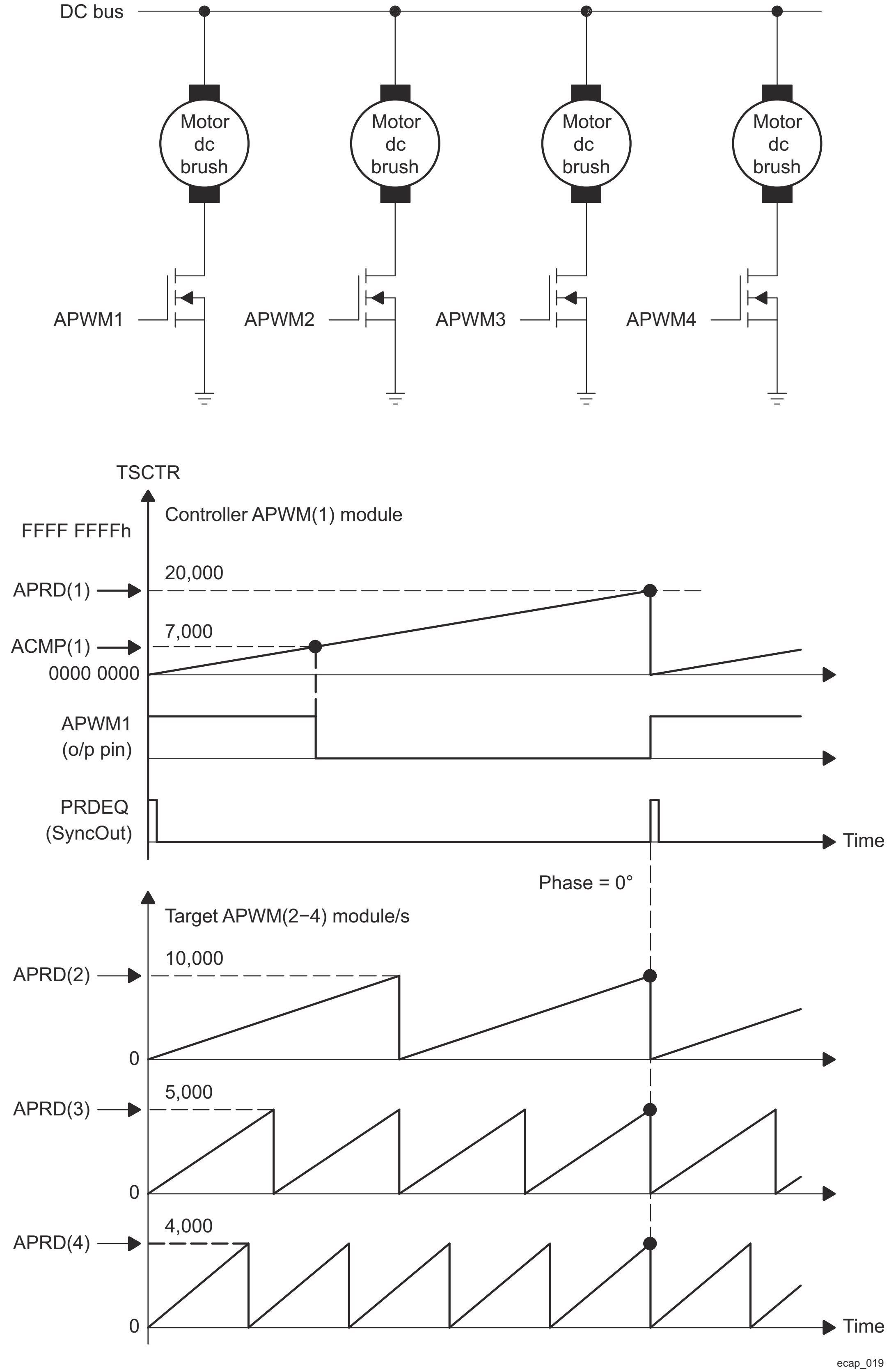


Figure 12-294. Multichannel PWM Example Using 4 ECAP Modules

Table 12-265. ECAP1 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	20000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_CTR_PRD
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-266. ECAP2 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	10000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-267. ECAP3 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	5000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-268. ECAP4 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	4000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Example 12-6. Code Snippet for Multichannel PWM Generation with Synchronization

```
// Code snippet for APWM mode Example 2
// Run Time (Note: Example execution of one run-time instant)
//============================================================
   ECAP1Regs.CAP2 = 7000;    // Set Duty cycle i.e., compare value = 7000
   ECAP2Regs.CAP2 = 2000;    // Set Duty cycle i.e., compare value = 2000
   ECAP3Regs.CAP2 = 550;     // Set Duty cycle i.e., compare value = 550
   ECAP4Regs.CAP2 = 6500;    // Set Duty cycle i.e., compare value = 6500
```

12.5.2.5.5.3 Multichannel PWM Generation with Phase Control Example

In Figure 12-295, the Phase control feature of the APWM mode is used to control a 3 phase Interleaved DC/DC converter topology. This topology requires each phase to be off-set by 120° from each other. Hence if "Leg" 1 (controlled by APWM1) is the reference Leg (or phase), that is, 0°, then Leg 2 need 120° off-set and Leg 3 needs 240° off-set. The waveforms in Figure 12-295 show the timing relationship between each of the phases (Legs). Note ECAP1 module is the Controller and issues a SyncOut pulse to the targets (modules 2, 3) whenever TSCTR = Period value.

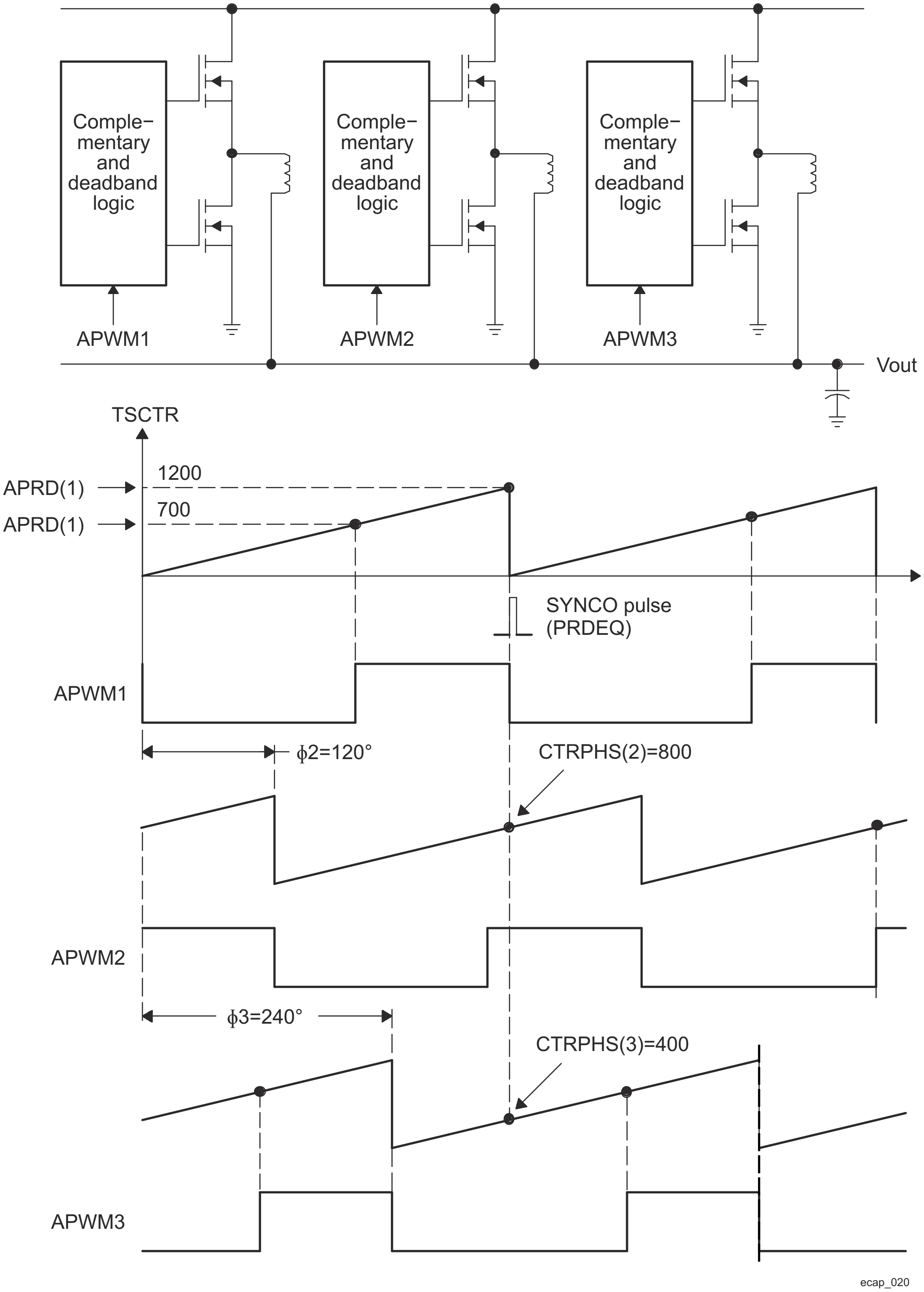


Figure 12-295. Multiphase (channel) Interleaved PWM Example Using 3 ECAP Modules

Table 12-269. ECAP1 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_CTR_PRD
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-270. ECAP2 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	800
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSCTRSTOP	EC_RUN

Table 12-271. ECAP3 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	400
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCI_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSCTRSTOP	EC_RUN

Example 12-7. Code Snippet for Multichannel PWM Generation with Phase Control

```
// Code snippet for APWM mode Example 3
// Run Time (Note: Example execution of one run-time instant)
//============================================================
// All phases are set to the same duty cycle
  ECAP1Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
  ECAP2Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
  ECAP3Regs.CAP2 = 700;     // Set Duty cycle i.e. compare value = 700
```

12.5.3 Enhanced Pulse Width Modulation (EPWM) Module

This chapter describes the Enhanced Pulse Width Modulation (EPWM) module in the device.

12.5.3.1 EPWM Overview

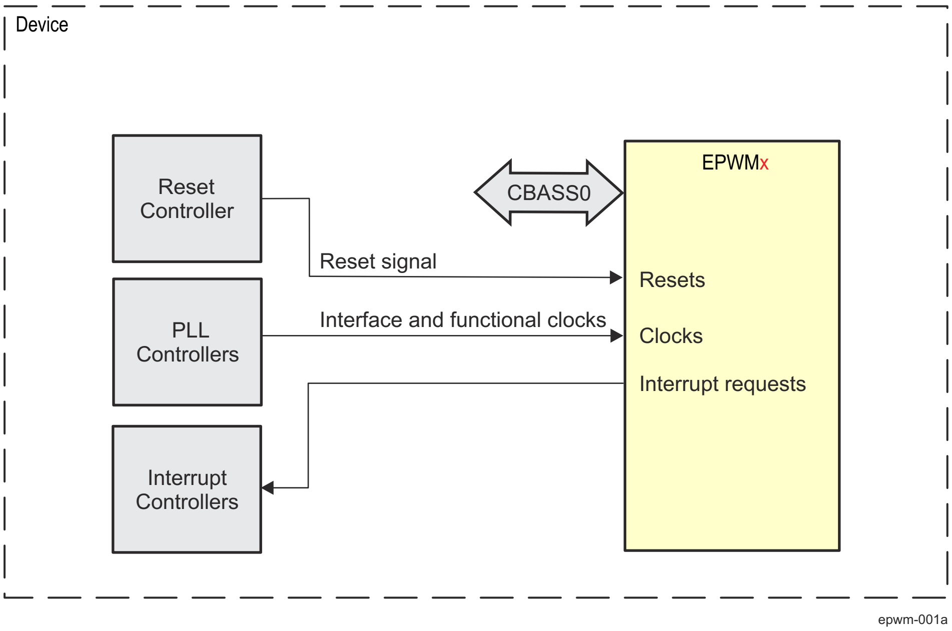
An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross-coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single-channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description, the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWMx instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

The EPWM module represents one complete PWM channel composed of two PWM outputs: EPWMxA and EPWMxB.

As also described in *Daisy-Chain Connectivity between EPWM Modules*, the EPWM modules are chained together via a clock synchronization scheme that allows them to operate as a single system when required. Additionally, this synchronization scheme can be extended to the Enhanced Capture (ECAP) peripheral module. The EPWM modules can also operate stand-alone.

Figure 12-296 shows the EPWM module overview.



A. x = 0 to number of instances

Figure 12-296. EPWM Overview

12.5.3.1.1 EPWM Features

Each EPWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Allows events to trigger both CPU interrupts and ADC start of conversions
- Programmable event prescaling minimizes CPU overhead on interrupts
- PWM chopping by a high-frequency carrier signal, useful for pulse transformer gate drives

12.5.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

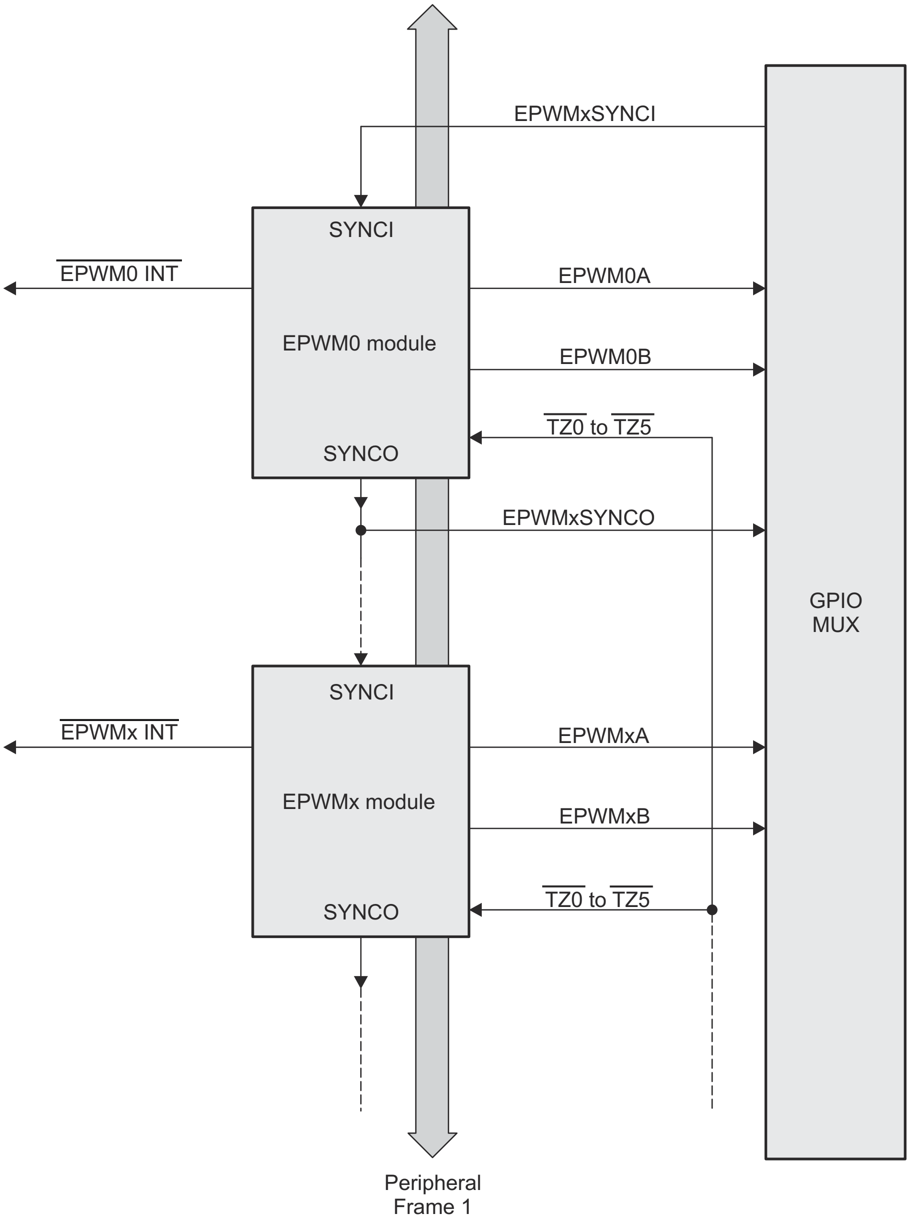
Note

Some features may not be available. See *Module Integration* for more information.

12.5.3.1.3 Multiple EPWM Module Details

Each EPWM module is connected to the input/output signals shown in Figure 12-297.

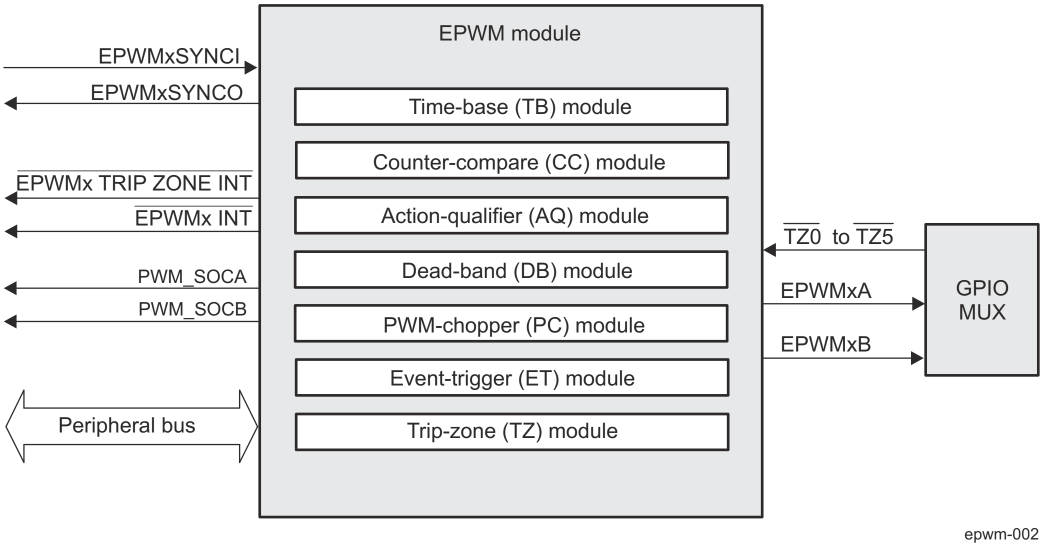
The order in which the EPWM modules are connected may differ from what is shown in Figure 12-297. See *Daisy-Chain Connectivity between EPWM Modules* for the actual synchronization scheme implemented in the device. Each EPWM module consists of seven submodules and is connected within a system via the signals shown in Figure 12-298.



epwm-001

A. x = 0 to number of instances

Figure 12-297. Multiple EPWM Modules



A. x = 0 to number of instances

Figure 12-298. Submodules and Signal Connections for an EPWM Module

Figure 12-299 shows more internal details of a single EPWM module.

The main signals used by the EPWM module are:

- **PWM output signals (EPWMxA and EPWMxB)**
  The PWM output signals are available external to the device through the GPIO peripheral.
- **Trip-zone signals ($\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$)**
  These input signals alert the EPWM module of an external fault condition. Each module on a device can be configured to either use or ignore any of the trip-zone signals. The trip-zone signal can be configured as an asynchronous input through the GPIO peripheral.
- **Time-base synchronization input (EPWMxSYNCI) and output (EPWMxSYNCO) signals**
  The synchronization signals daisy chain the EPWM modules together. Each module can be configured to either use or ignore its synchronization input. For more information see *Daisy-Chain Connectivity between EPWM Modules*.
- **ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB)**
  Each EPWM module has two ADC start of conversion signals (one for each sequencer). Any EPWM module can trigger a start of conversion for either sequencer. Which event triggers the start of conversion is configured in the Event-Trigger submodule of the EPWM module.
- **Peripheral Bus**
  The peripheral bus is 32-bits wide and allows both 16-bit and 32-bit writes to the EPWM registers.

Figure 12-299 also shows the key internal submodule interconnect signals. Each submodule is described in *EPWM Functional Description*.

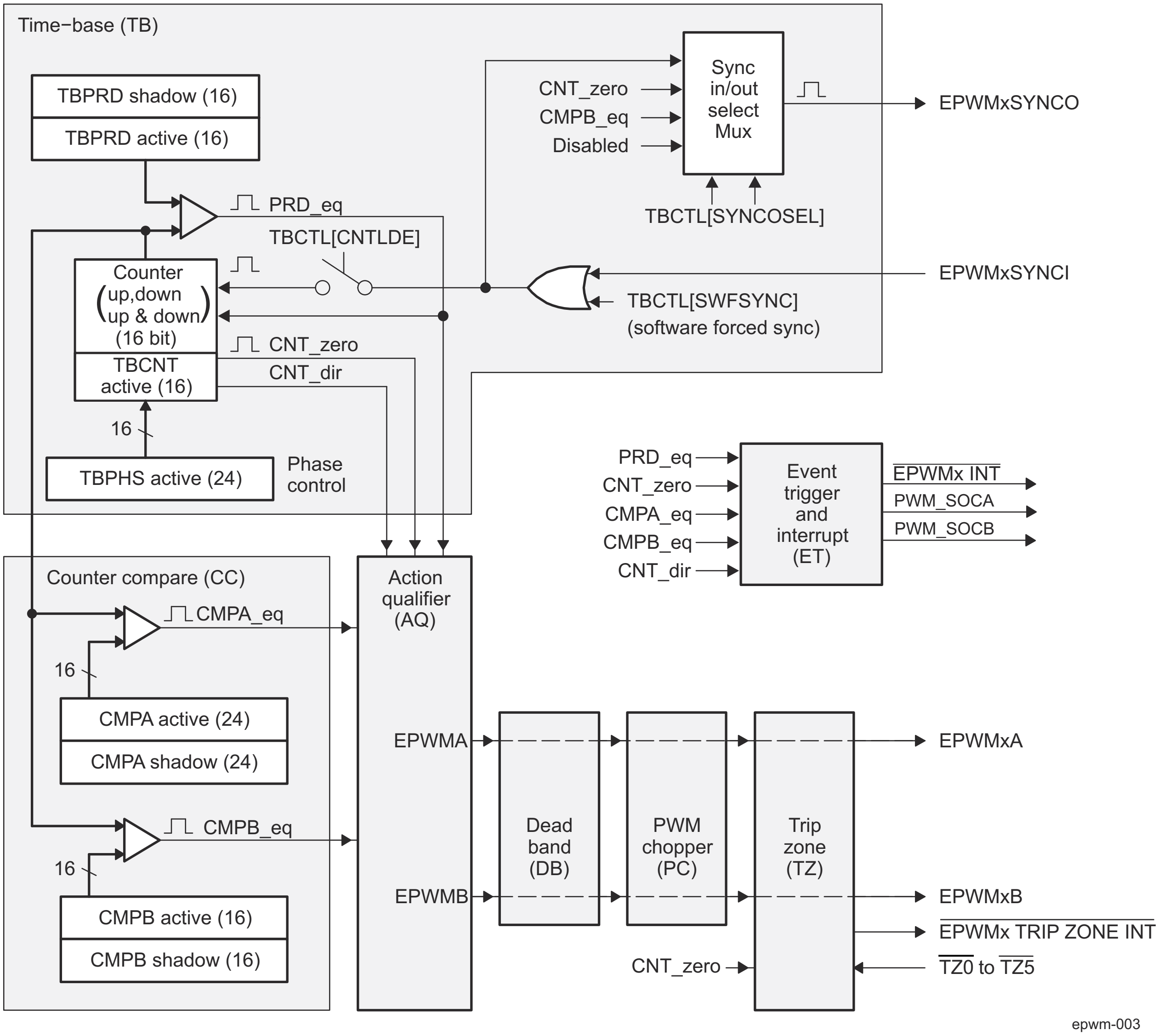


Figure 12-299. EPWM Submodule Interconnect Signals

12.5.3.2 EPWM Environment

The EPWMx (where x = 0 to number of instances) module is hereinafter referred to as EPWM module.

This section describes the EPWM external connections (environment).

Figure 12-300 shows the EPWM I/O interface signals.

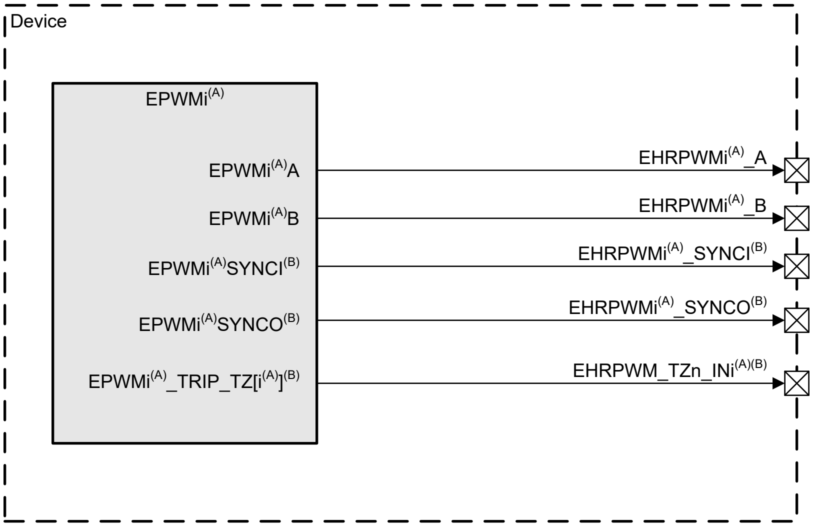


Figure 12-300. EPWM I/O Interface Signals

A. i represents a valid instance of EPWM in a domain. See the device datasheet for specifics.

B. Pin only available on specific instances. See the device datasheet for specifics.

Table 12-272 describes the EPWM I/O signals.

Table 12-272. EPWM I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value(2)
		EPWMi(3)		
EPWMi(3)A	EHRPWMi(3)_A	O	EPWMi(3) output A	0x0
EPWMi(3)B	EHRPWMi(3)_B	O	EPWMi(3) output B	0x0
EPWMi(3)SYNCI(4)	EHRPWMi(3)_SYNCI	I	EPWMi(3) Sync input	HiZ
EPWMi(3)SYNCO(4)	EHRPWMi(3)_SYNCO	O	EPWMi(3) Sync output	0x0
EPWMi(3)_TRIP_TZ[0](4)	EHRPWM_TZn_INi(3)	I	EPWMi(3) TripZone input	HiZ
		EPWM Start of Conversion		
PWM_SOCA	EHRPWM_SOCA	O	EPWM start of conversion output A	HiZ
PWM_SOCB	EHRPWM_SOCB	O	EPWM start of conversion output B	HiZ

(1) I = Input; O = Output
(2) HiZ = High Impedance
(3) i represents a valid instance of EPWM in a domain. See the device datasheet for specifics.
(4) Pin only available on specific instances. See the device datasheet for specifics.

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables Pin Attributes and Pin Multiplexing in the device-specific Datasheet.

12.5.3.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.5.3.4 EPWM Functional Description

Seven submodules are included in each EPWM peripheral. Each of these submodules performs specific tasks that can be configured by software.

12.5.3.4.1 EPWM Submodule Features

Table 12-273 lists the seven key submodules together with a list of their main configuration parameters.

Table 12-273. Submodule Configuration Parameters

Submodule	Configuration Parameter or Option
Time-base (TB)	• Scale the time-base clock (TBCLK) relative to the system clock (FICLK). • Configure the PWM time-base counter (TBCNT) frequency or period. • Time-base counter mode selection: – count-up mode: used for asymmetric PWM – count-down mode: used for asymmetric PWM – count-up-and-down mode: used for symmetric PWM • Configure the time-base phase relative to another EPWM module. • Synchronize the time-base counter between modules through hardware or software. • Configure the direction (up or down) of the time-base counter after a synchronization event. • Configure how the time-base counter will behave when the device is halted by an emulator. • Specify the source for the synchronization output of the EPWM module: – Synchronization input signal – Time-base counter equal to zero – Time-base counter equal to counter-compare B (CMPB) – No output synchronization signal generated
Counter-compare (CC)	• Specify the PWM duty cycle for output EPWMxA and/or output EPWMxB • Specify the time at which switching events occur on the EPWMxA or EPWMxB output
Action-qualifier (AQ)	• Specify the type of action taken when a time-base or counter-compare submodule event occurs: – No action taken – Output EPWMxA and/or EPWMxB switched high – Output EPWMxA and/or EPWMxB switched low – Output EPWMxA and/or EPWMxB toggled • Force the PWM output state through software control • Configure and control the PWM dead-band through software
Dead-band (DB)	• Control of traditional complementary dead-band relationship between upper and lower switches • Specify the output rising-edge-delay value • Specify the output falling-edge delay value • Bypass the dead-band module entirely. In this case the PWM waveform is passed through without modification
PWM-chopper (PC)	• Create a chopping (carrier) frequency • Pulse width of the first pulse in the chopped pulse train • Duty cycle of the second and subsequent pulses • Bypass the PWM-chopper module entirely. In this case the PWM waveform is passed through without modification.

Table 12-273. Submodule Configuration Parameters (continued)

Submodule	Configuration Parameter or Option
Trip-zone (TZ)	• Configure the EPWM module to react to one, all, or none of the trip-zone pins • Specify the tripping action taken when a fault occurs: – Force EPWMxA and/or EPWMxB high – Force EPWMxA and/or EPWMxB low – Force EPWMxA and/or EPWMxB to a high-impedance state – Configure EPWMxA and/or EPWMxB to ignore any trip condition • Configure how often the EPWM will react to the trip-zone pin: – One-shot – Cycle-by-cycle • Enable the trip-zone to initiate an interrupt • Bypass the trip-zone module entirely
Event-trigger (ET)	• Enable the EPWM events that will trigger an interrupt. • Specify the rate at which events cause triggers (every occurrence or every second or third occurrence) • Poll, set, or clear event flags

Some examples on various EPWM module configurations are shown below. These examples use the constant definitions shown in Example 12-8.

Constant Definitions Used in the EPWM Code Examples

```
// TBCTL (Time-Base Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// TBCNT MODE bits
#define         TB_COUNT_UP         0x0
#define         TB_COUNT_DOWN       0x1
#define         TB_COUNT_UPDOWN     0x2
#define         TB_FREEZE           0x3
// PHSEN bit
#define         TB_DISABLE          0x0
#define         TB_ENABLE           0x1
// PRDLD bit
#define         TB_SHADOW           0x0
#define         TB_IMMEDIATE        0x1
// SYNCOSEL bits
#define         TB_SYNC_IN          0x0
#define         TB_CTR_ZERO         0x1
#define         TB_CTR_CMPB         0x2
#define         TB_SYNC_DISABLE     0x3
// HSPCLKDIV and CLKDIV bits
#define         TB_DIV1             0x0
#define         TB_DIV2             0x1
#define         TB_DIV4             0x2
// PHSDIR bit
#define         TB_DOWN             0x0
#define         TB_UP               0x1
```

```
// CMPCTL (Compare Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// LOADAMODE and LOADBMODE bits
#define         CC_CTR_ZERO         0x0
#define         CC_CTR_PRD          0x1
#define         CC_CTR_ZERO_PRD     0x2
#define         CC_LD_DISABLE       0x3
// SHDWAMODE and SHDWBMODE bits
```

```
#define         CC_SHADOW          0x0
#define         CC_IMMEDIATE       0x1
// AQCTLA and AQCTLB (Action-qualifier Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// ZRO, PRD, CAU, CAD, CBU, CBD bits
#define         AQ_NO_ACTION       0x0
#define         AQ_CLEAR           0x1
#define         AQ_SET             0x2
#define         AQ_TOGGLE          0x3
// DBCTL (Dead-Band Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// MODE bits
#define         DB_DISABLE         0x0
#define         DBA_ENABLE         0x1
#define         DBB_ENABLE         0x2
#define DB_FULL_ENABLE 0x3
// POLSEL bits
#define         DB_ACTV_HI         0x0
#define         DB_ACTV_LOC        0x1
#define         DB_ACTV_HIC        0x2
#define         DB_ACTV_LO         0x3
// PCCTL (chopper control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// CHPEN bit
#define         CHP_ENABLE         0x0
#define CHP_DISABLE 0x1
// CHPFREQ bits
#define         CHP_DIV1           0x0
#define         CHP_DIV2           0x1
#define         CHP_DIV3           0x2
#define         CHP_DIV4           0x3
#define         CHP_DIV5           0x4
#define         CHP_DIV6           0x5
#define         CHP_DIV7           0x6
#define         CHP_DIV8           0x7
// CHPDUTY bits
#define         CHP1_8TH           0x0
#define         CHP2_8TH           0x1
#define         CHP3_8TH           0x2
#define         CHP4_8TH           0x3
#define         CHP5_8TH           0x4
#define         CHP6_8TH           0x5
#define         CHP7_8TH           0x6
// TZSEL (Trip-zone Select)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// CBCn and OSHTn bits
#define         TZ_ENABLE          0x0
#define         TZ_DISABLE         0x1
// TZCTL (Trip-zone Control)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// TZA and TZB bits
#define         TZ_HIZ             0x0
#define         TZ_FORCE_HI        0x1
#define         TZ_FORCE_LO        0x2
#define         TZ_DISABLE         0x3
// ETSEL (Event-trigger Select)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// INTSEL, SOCASEL, SOCBSEL bits
#define         ET_CTR_ZERO        0x1
#define         ET_CTR_PRD         0x2
#define         ET_CTRU_CMPA       0x4
#define         ET_CTRD_CMPA       0x5
#define         ET_CTRU_CMPB       0x6
#define         ET_CTRD_CMPB       0x7
// ETPS (Event-trigger Prescale)
// = = = = = = = = = = = = = = = = = = = = = = = = = =
// INTPRD, SOCAPRD, SOCBPRD bits
#define         ET_DISABLE         0x0
#define         ET_1ST             0x1
#define         ET_2ND             0x2
#define         ET_3RD             0x3
```

12.5.3.4.2 EPWM Time-Base (TB) Submodule

This section describes the Time-Base (TB) submodule in the PWM module.

12.5.3.4.2.1 Overview

Each EPWM module has its own time-base submodule that determines all of the timing events. Built-in synchronization logic allows the time-base of multiple EPWM modules (EPWMx) to work together as a single system. Figure 12-301 illustrates the time-base module's place within the EPWM.

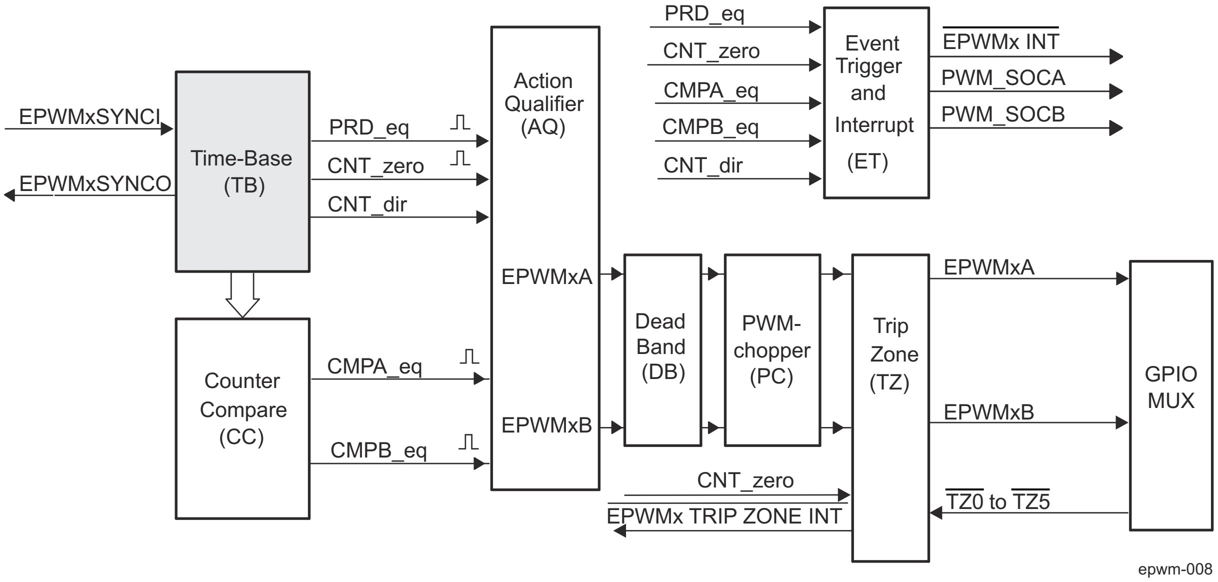


Figure 12-301. EPWM Time-Base Submodule

12.5.3.4.2.2 Controlling and Monitoring the EPWM Time-Base Submodule

Table 12-274 lists the registers used to control and monitor the time-base submodule.

Table 12-274. EPWM Time-Base Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_TBCTL	Time-Base Control Register	0h	No
EPWM_TBSTS	Time-Base Status Register	2h	No
EPWM_TBPHS	Time-Base Phase Register	6h	No
EPWM_TBCNT	Time-Base Counter Register	8h	No
EPWM_TBPRD	Time-Base Period Register	Ah	Yes

Figure 12-302 shows the critical signals and registers of the time-base submodule. Table 12-275 provides descriptions of the key signals associated with the time-base submodule.

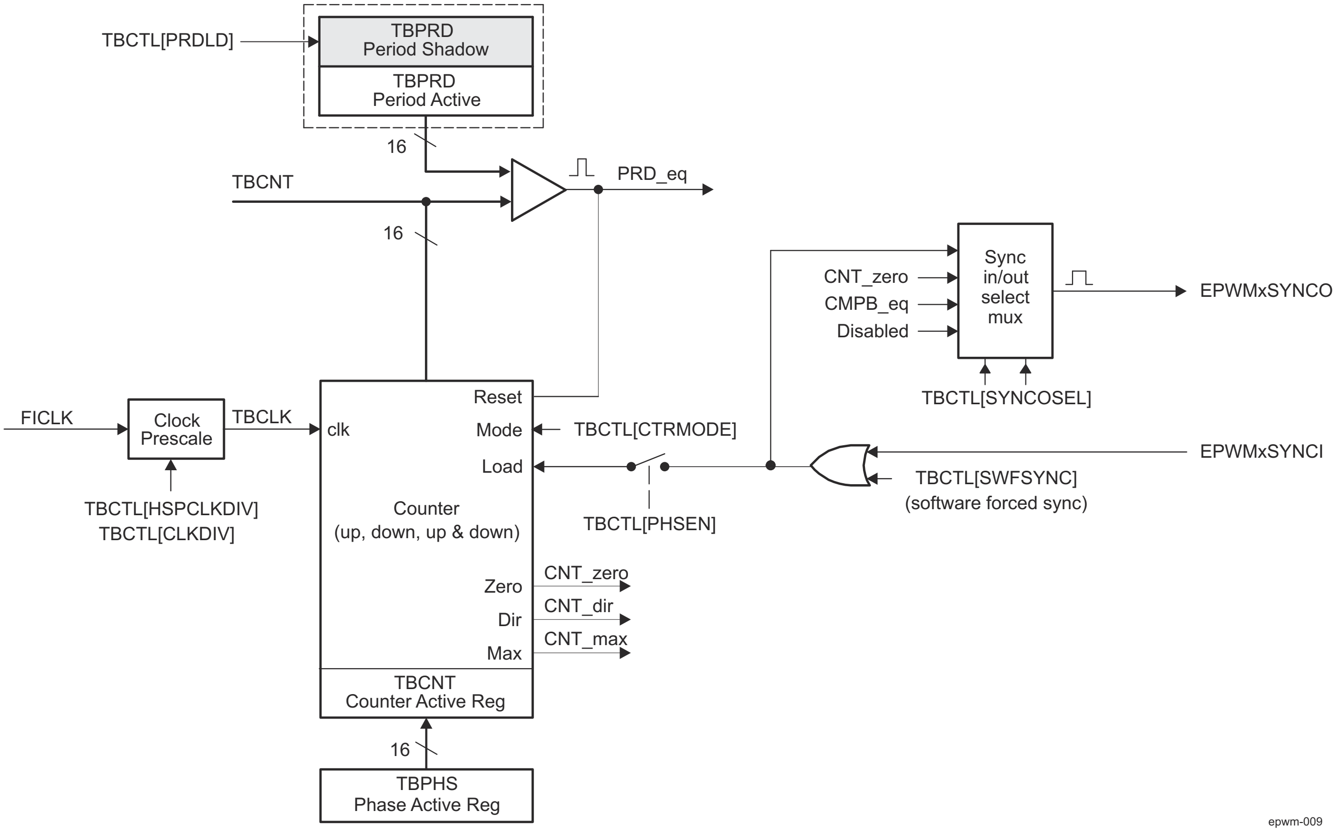


Figure 12-302. EPWM Time-Base Submodule Signals and Registers

Table 12-275. EPWM Time-Base Submodule Key Signals

Signal	Description
EPWMxSYNCI	Time-base synchronization input. Input pulse used to synchronize the time-base counter with the counter of another EPWM module earlier in the synchronization chain. An EPWM peripheral can be configured to use or ignore this signal. For the first EPWM module (EPWM0) this signal comes from a device pin. For subsequent EPWM modules this signal is passed from another EPWM peripheral. For example, EPWM2SYNCI is generated by the EPWM1 peripheral and the EPWM3SYNCI is generated (optional through internal multiplexer) by EPWM2 or from a device pin. See Section 12.5.3.4.2.3.2 for information on the synchronization order of a particular device.
EPWMxSYNCO	Time-base synchronization output. This output pulse is used to synchronize the counter of an EPWM module later in the synchronization chain. The EPWM module generates this signal from one of three event sources: 1. EPWMxSYNCI (Synchronization input pulse) 2. TBCNT = 0: The time-base counter (EPWM_TBCNT register) equal to zero (TBCNT = 0000h). 3. TBCNT = CMPB: The time-base counter (EPWM_TBCNT register) equal to the counter-compare B register — EPWM_CMPB (that is bitfield TBCNT = bitfield CMPB).
PRD_eq	Time-base counter equal to the specified period. This signal is generated whenever the counter value is equal to the active period register value. That is when TBCNT = TBPRD.
CNT_zero	Time-base counter equal to zero. This signal is generated whenever the counter value is zero. That is when TBCNT equals 0000h.
CMPB_eq	Time-base counter equal to active counter-compare B register (TBCNT = CMPB). This event is generated by the counter-compare submodule and used by the synchronization out logic.
CNT_dir	Time-base counter direction. Indicates the current direction of the EPWM's time-base counter. This signal is high when the counter is increasing and low when it is decreasing.

Table 12-275. EPWM Time-Base Submodule Key Signals (continued)

Signal	Description
CNT_max	Time-base counter equal max value (TBCNT = FFFFh). Generated event when the EPWM_TBCNT register value reaches its maximum value. This signal is only used only as a status bit.
TBCLK	Time-base clock. This is a prescaled version of the system clock — FICLK and is used by all submodules within the EPWMn. This clock determines the rate at which time-base counter increments or decrements.

12.5.3.4.2.3 Calculating PWM Period and Frequency

The frequency of PWM events is controlled by the time-base period register (EPWM_TBPRD) and the mode of the time-base counter. Figure 12-303 shows the period (T_{pwm}) and frequency (F_{pwm}) relationships for the up-count, down-count, and up-down-count time-base counter modes when the period is set to 4 (EPWM_TBPRD[15-0] TBPRD = 0x4). The time increment for each step is defined by the time-base clock (TBCLK) which is a prescaled version of the system clock (FICLK).

The time-base counter has three modes of operation selected by the time-base control register (EPWM_TBCTL):

- **Up-Down-Count Mode:** In up-down-count mode, the time-base counter starts from zero and increments until the period (TBPRD) value is reached. When the period value is reached, the time-base counter then decrements until it reaches zero. At this point the counter repeats the pattern and begins to increment.
- **Up-Count Mode:** In this mode, the time-base counter starts from zero and increments until it reaches the value in the period register (TBPRD). When the period value is reached, the time-base counter resets to zero and begins to increment once again.
- **Down-Count Mode:** In down-count mode, the time-base counter starts from the period (TBPRD) value and decrements until it reaches zero. When it reaches zero, the time-base counter is reset back to the period value and it repeats this pattern.

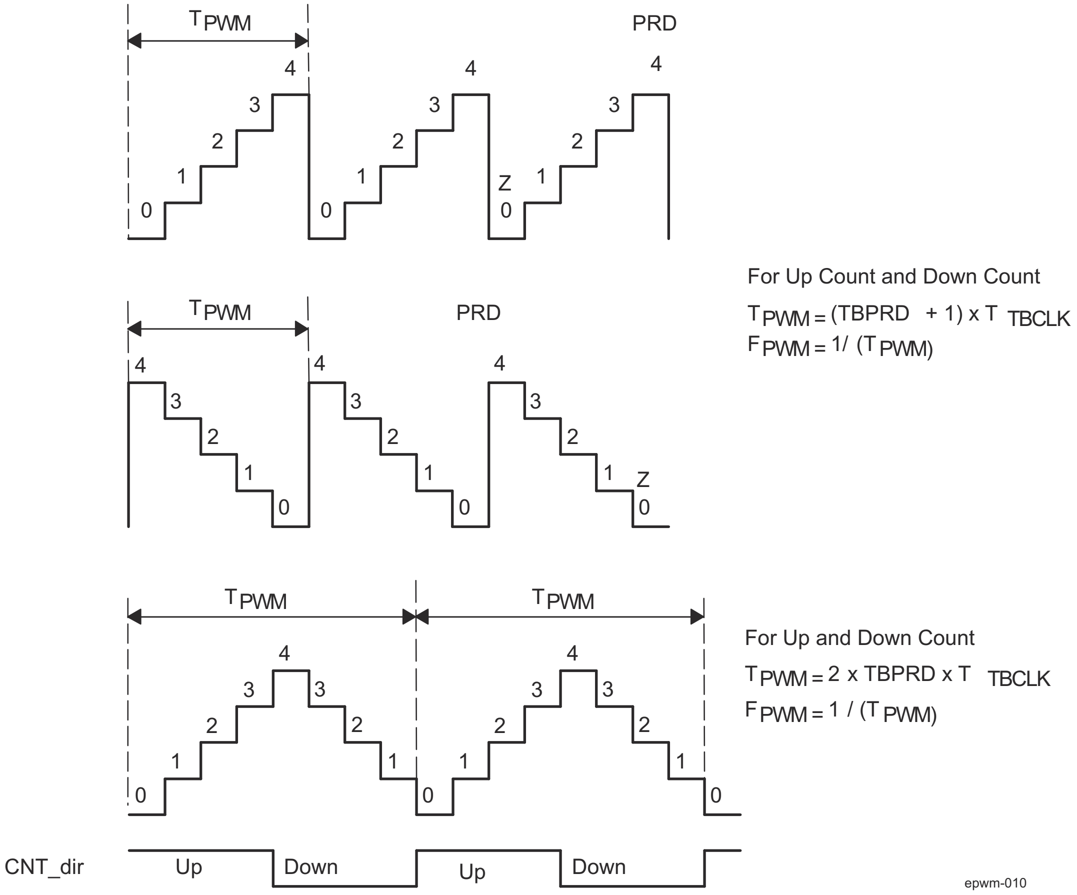


Figure 12-303. EPWM Time-Base Frequency and Period

12.5.3.4.2.3.1 EPWM Time-Base Period Shadow Register

The time-base period register (EPWM_TBPRD) has a shadow register. Shadowing allows the register update to be synchronized with the hardware. The following definitions are used to describe all shadow registers in the EPWM module:

- **Active Register:** The active register controls the hardware and is responsible for actions that the hardware causes or invokes.
- **Shadow Register:** The shadow register buffers or provides a temporary holding location for the active register. It has no direct effect on any control hardware. At a strategic point in time the shadow register's content is transferred to the active register. This prevents corruption or spurious operation due to the register being asynchronously modified by software.

The memory address of the shadow period register is the same as the active register. Which register is written to or read from is determined by the EPWM_TBCTL[3] PRDLD bit. This bit enables and disables the EPWM_TBPRD shadow register as follows:

- **Time-Base Period Shadow Mode:** The EPWM_TBPRD shadow register is enabled when EPWM_TBCTL[3] PRDLD = 0h. Reads from and writes to the EPWM_TBPRD register memory address go to the shadow register. The shadow register contents are transferred to the active register (EPWM_TBPRD (Active) ← EPWM_TBPRD (shadow)) when the time-base counter register (EPWM_TBCNT) equals zero (TBCNT = 0000h). By default the EPWM_TBPRD shadow register is enabled.
- **Time-Base Period Immediate Load Mode:** If immediate load mode is selected (EPWM_TBCTL[3] PRDLD = 1h), then a read from or a write to the TBPRD memory address goes directly to the active register.

12.5.3.4.2.3.2 EPWM Time-Base Counter Synchronization

A time-base synchronization scheme connects all of the EPWM modules on a device. Each EPWM module has a synchronization input (EPWMxSYNCI) and a synchronization output (EPWMxSYNCO). The input synchronization for the first instance (EPWM0) comes from an external pin. For the device EPWM environment sync pin details refer to the Section 12.5.3.2. The possible synchronization connections for the remaining EPWM modules is shown in Figure 12-304.

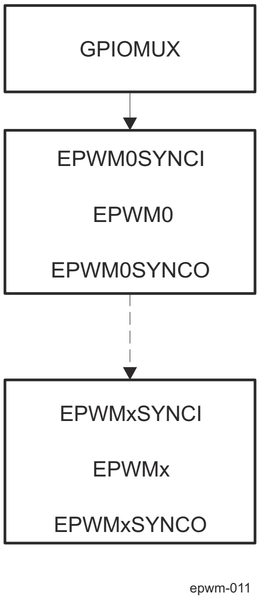


Figure 12-304. EPWM Time-Base Counter Synchronization Scheme 1

Each EPWM module can be configured to use or ignore the synchronization input. If the EPWM_TBCTL[2] PHSEN bit is set, then the time-base counter (TBCNT) of the EPWM module (EPWM_TBCNT register) will be automatically loaded with the phase register (EPWM_TBPHS) contents when one of the following conditions occur:

- **EPWMxSYNCI: Synchronization Input Pulse:** The value of the phase register is loaded into the counter register when an input synchronization pulse is detected (EPWM_TBPHS → EPWM_TBCNT). This operation occurs on the next valid time-base clock (TBCLK) edge.
- **Software Forced Synchronization Pulse:** Writing a 1h to the EPWM_TBCTL[6] SWFSYNC control bit invokes a software forced synchronization. This pulse is ORed with the synchronization input signal, and therefore has the same effect as a pulse on EPWMxSYNCI.

This feature enables the EPWM module to be automatically synchronized to the time base of another EPWM module. Lead or lag phase control can be added to the waveforms generated by different EPWM modules to synchronize them. In up-down-count mode, the EPWM_TBCTL[13] PHSDIR bit configures the direction of the time-base counter immediately after a synchronization event. The new direction is independent of the direction prior to the synchronization event. The TBPHS bit is ignored in count-up or count-down modes. See Figure 12-305 through Figure 12-308 for examples.

Clearing the EPWM_TBCTL[2] PHSEN bit configures the EPWM to ignore the synchronization input pulse. The synchronization pulse can still be allowed to flow-through to the EPWMxSYNCO and be used to synchronize other EPWM modules. In this way, a controller time-base (for example: EPWM1) and downstream modules (EPWM2–EPWMx) can be set and they may select to run in synchronization with the controller.

12.5.3.4.2.4 Phase Locking the Time-Base Clocks of Multiple EPWM Modules

As already described in the *EPWM Modules Time-Base Clock Gating*, TB_CLKEN bit in the EPWMn_CTRL (where n = 0 to number of instances on the device) register of the device CTRL_MMR can be used to individually control or globally synchronize the time-base clocks of all enabled EPWM modules on a device. When all TB_CLKEN bits are set to 0h, the time-base clocks of all EPWMx (where x = 0 to 8) modules are stopped (default). When all TB_CLKEN bits are simultaneously set in software to 1h, all EPWMx modules time-base clocks are started with the rising edge of TBCLK aligned. For perfectly synchronized TBCLKs, the prescaler bits in the EPWM_TBCTL register of each EPWM module must be set identically. The proper procedure for enabling the EPWM clocks is as follows:

1. Enable the EPWM module clocks.
2. Set TB_CLKEN = 0. This will stop the time-base clock within any enabled EPWMx module.
3. Configure the prescaler values and desired EPWM modes per each involved EPWMx.
4. Simultaneously set TB_CLKEN bits to 1h.

12.5.3.4.2.5 EPWM Time-Base Counter Modes and Timing Waveforms

The time-base counter operates in one of four modes:

- Up-count mode which is asymmetrical.
- Down-count mode which is asymmetrical.
- Up-down-count which is symmetrical.
- Frozen where the time-base counter is held constant at the current value.

To illustrate the operation of the first three modes, Figure 12-305 to Figure 12-308 show when events are generated and how the time-base responds to an EPWMxSYNCI signal.

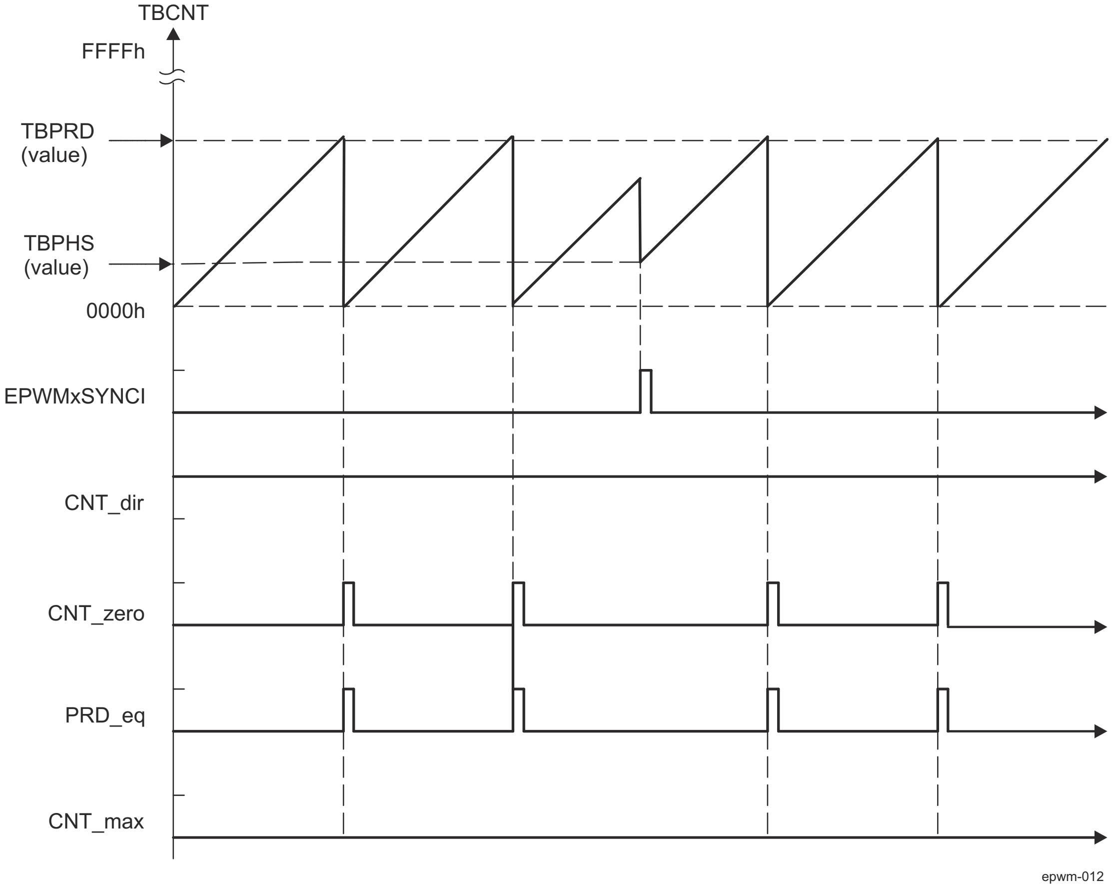


Figure 12-305. EPWM Time-Base Up-Count Mode Waveforms

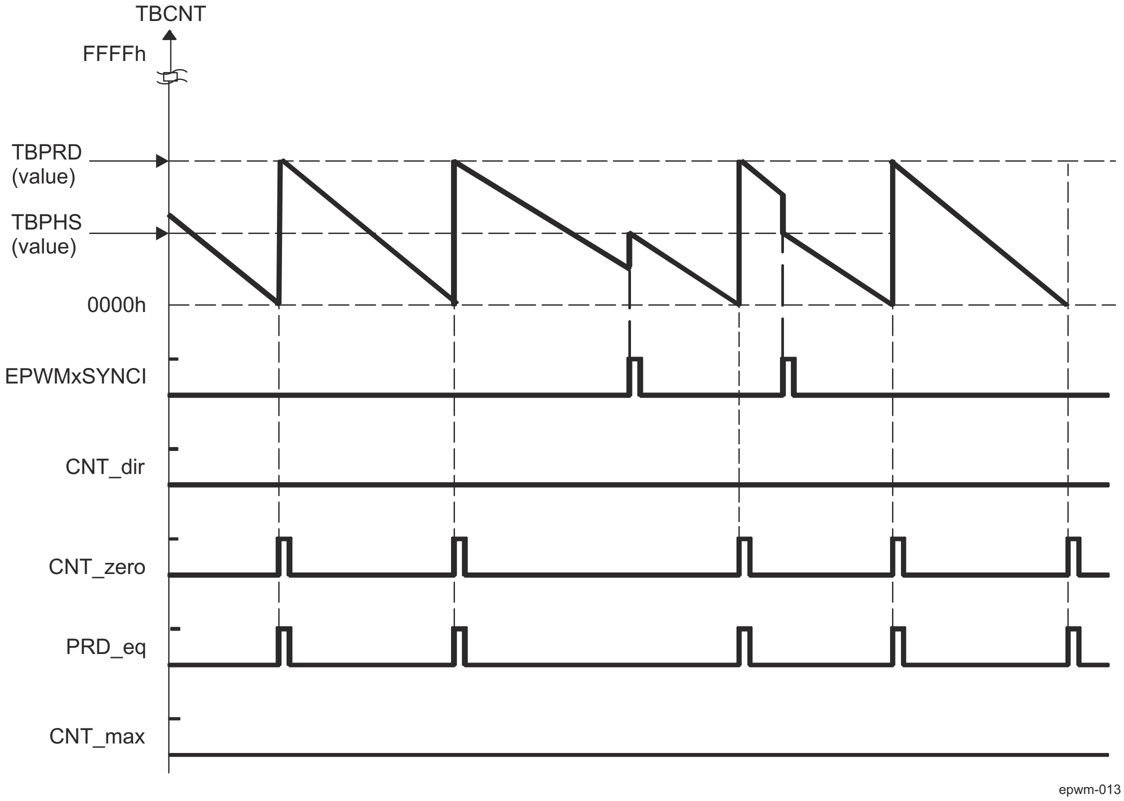


Figure 12-306. EPWM Time-Base Down-Count Mode Waveforms

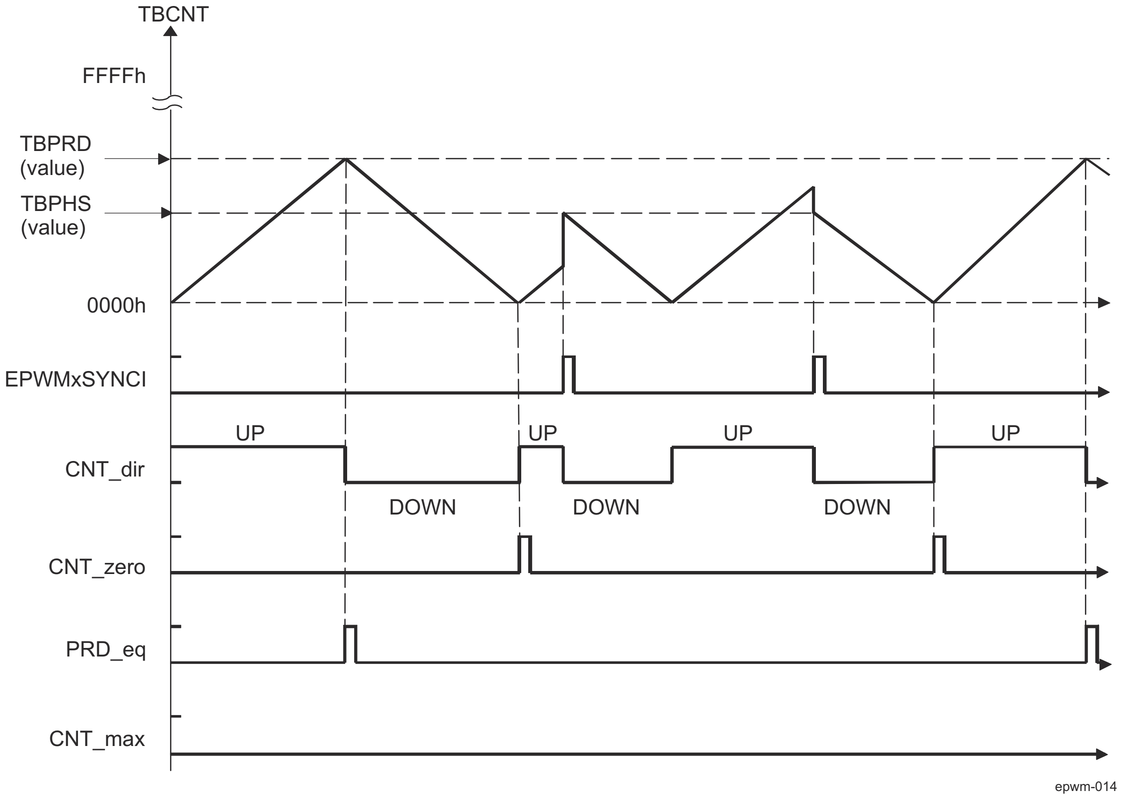


Figure 12-307. EPWM Time-Base Up-Down-Count Waveforms, EPWM_TBCTL[13] PHSDIR = 0 Count Down on Synchronization Event

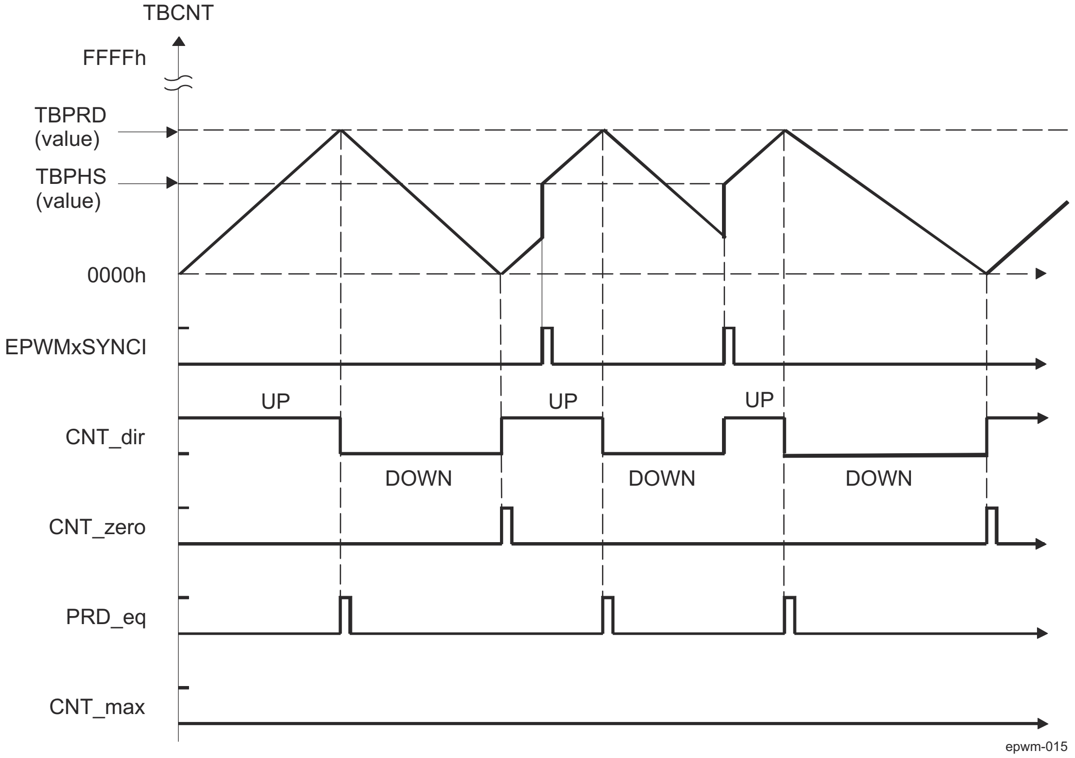


Figure 12-308. EPWM Time-Base Up-Down Count Waveforms, EPWM_TBCTL[13] PHSDIR = 1 Count Up on Synchronization Event

12.5.3.4.3 EPWM Counter-Compare (CC) Submodule

This section describes the Counter-Compare (CC) submodule in the PWM module.

12.5.3.4.3.1 Overview

Figure 12-309 illustrates the counter-compare submodule within the EPWM. Figure 12-310 shows the basic structure of the counter-compare submodule.

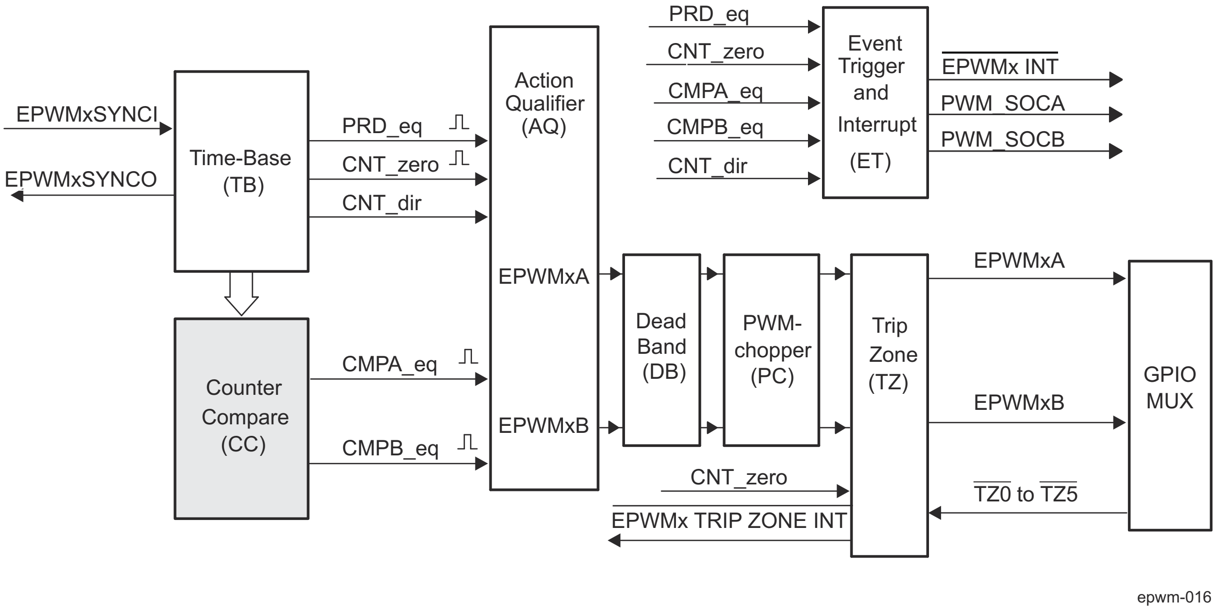


Figure 12-309. EPWM Counter-Compare Submodule

CC module features:

- Generates events based on programmable time stamps using the EPWM_CMPA and EPWM_CMPB registers
  - CMPA_eq (Time-base counter equals counter-compare A register (TBCNT = CMPA)).
  - CMPB_eq (Time-base counter equals counter-compare B register (TBCNT = CMPB)).
- Controls the PWM duty cycle if the action-qualifier submodule is configured appropriately
- Shadows new compare values to prevent corruption or glitches during the active PWM cycle.

The counter-compare submodule takes as input the time-base counter value. This value is continuously compared to the counter-compare A (EPWM_CMPA) and counter-compare B (EPWM_CMPB) registers. When the time-base counter is equal to one of the compare registers, the counter-compare unit generates an appropriate event.

12.5.3.4.3.2 Controlling and Monitoring the EPWM Counter-Compare Submodule

Table 12-276 lists the registers used to control and monitor the counter-compare submodule. Table 12-277 lists the key signals associated with the counter-compare submodule.

Table 12-276. EPWM Counter-Compare Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_CMPCTL	Counter-Compare Control Register.	Eh	No
EPWM_CMPA	Counter-Compare A Register	12h	Yes
EPWM_CMPB	Counter-Compare B Register	14h	Yes

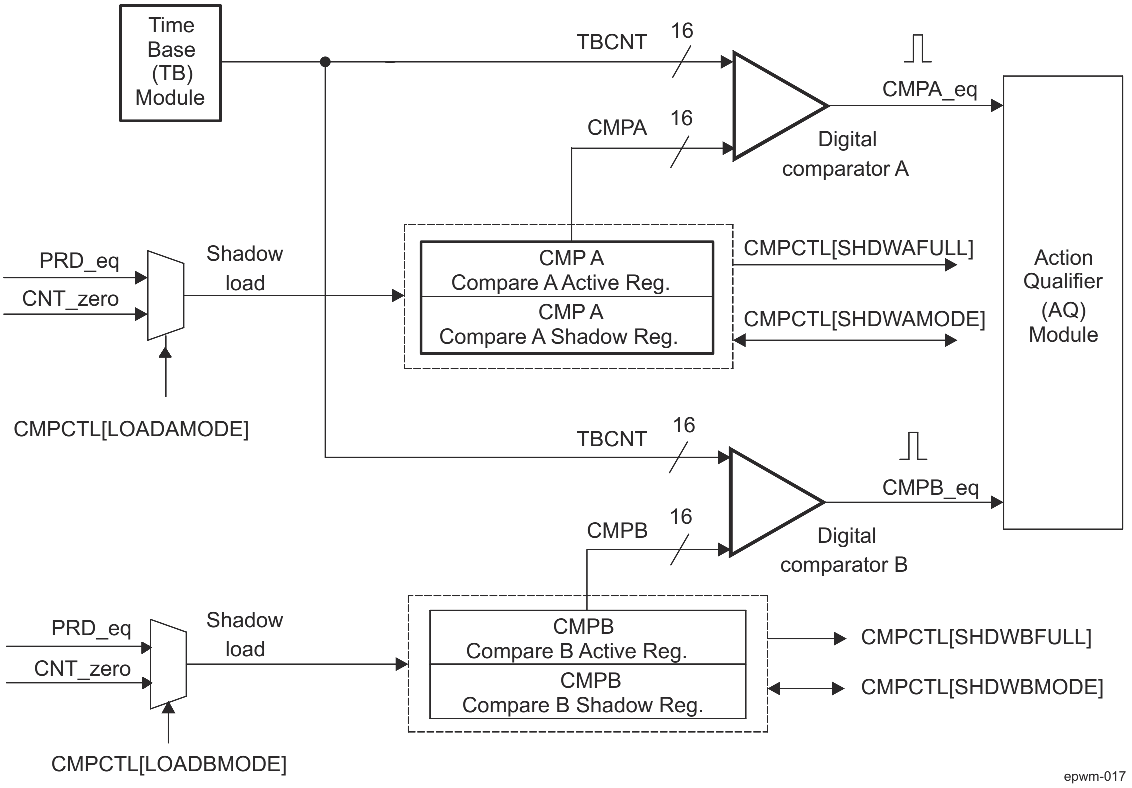


Figure 12-310. EPWM Counter-Compare Submodule Signals and Registers

Table 12-277. EPWM Counter-Compare Submodule Key Signals

Signal	Description of Event	Register Bitfields Compared
CMPA_eq	Time-base counter equal to the active counter-compare A value	TBCNT = CMPA
CMPB_eq	Time-base counter equal to the active counter-compare B value	TBCNT = CMPB
PRD_eq	Time-base counter equal to the active period. Used to load active counter-compare A and B registers from the shadow register	TBCNT = TBPRD
CNT_zero	Time-base counter equal to zero. Used to load active counter-compare A and B registers from the shadow register	TBCNT = 0000h

12.5.3.4.3.3 Operational Highlights for the EPWM Counter-Compare Submodule

The counter-compare submodule is responsible for generating two independent compare events based on two compare registers:

1. CMPA: Time-base counter equal to counter-compare A register (EPWM_TBCNT = EPWM_CMPA).
2. CMPB: Time-base counter equal to counter-compare B register (EPWM_TBCNT = EPWM_CMPB).

For up-count or down-count mode, each event occurs only once per cycle. For up-down-count mode each event occurs twice per cycle, if the compare value is between 0000h and TBPRD; and occurs once per cycle, if the compare value is equal to 0000h or equal to TBPRD. These events are fed into the action-qualifier submodule where they are qualified by the counter direction and converted into actions if enabled. Refer to Section 12.5.3.4.4 for more details.

The counter-compare EPWM_CMPA and EPWM_CMPB registers each have an associated shadow register. Shadowing provides a way to keep updates to the registers synchronized with the hardware. When shadowing is used, updates to the active registers only occurs at strategic points. This prevents corruption or spurious operation due to the register being asynchronously modified by software. The memory address of the active register and the shadow register is identical. Which register is written to or read from is determined by the EPWM_CMPCTL[4] SHDWAMODE and EPWM_CMPCTL[6] SHDWBMODE bits. These bits enable and disable the EPWM_CMPA shadow register and EPWM_CMPB shadow register respectively. The behavior of the two load modes is described below:

- **Shadow Load Mode:**
  The shadow mode for the EPWM_CMPA register is enabled by clearing the EPWM_CMPCTL[4] SHDWAMODE bit and the shadow register for EPWM_CMPB register is enabled by clearing the EPWM_CMPCTL[6] SHDWBMODE bit. Shadow mode is enabled by default for both EPWM_CMPA and EPWM_CMPB register.

  If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events:
  - PRD_eq: Time-base counter equal to the period (TBCNT = TBPRD).
  - CNT_zero: Time-base counter equal to zero (TBCNT = 0000h)
  - Both PRD_eq and CNT_zero events occurrence

  Which of these three events will drive the counter compare module is specified by the EPWM_CMPCTL[1-0] LOADAMODE and EPWM_CMPCTL[3-2] LOADBMODE register bit fields. Only the active register contents are used by the counter-compare submodule to generate events to be sent to the action-qualifier.
- **Immediate Load Mode:**
  If immediate load mode is selected (EPWM_CMPCTL[4] SHDWAMODE = 1h or EPWM_CMPCTL[6] SHDWBMODE = 1h), then a read from or a write to the register will go directly to the active register.

Figure 12-311 and Figure 12-312 show Compare A and B Dual Shadow registers.

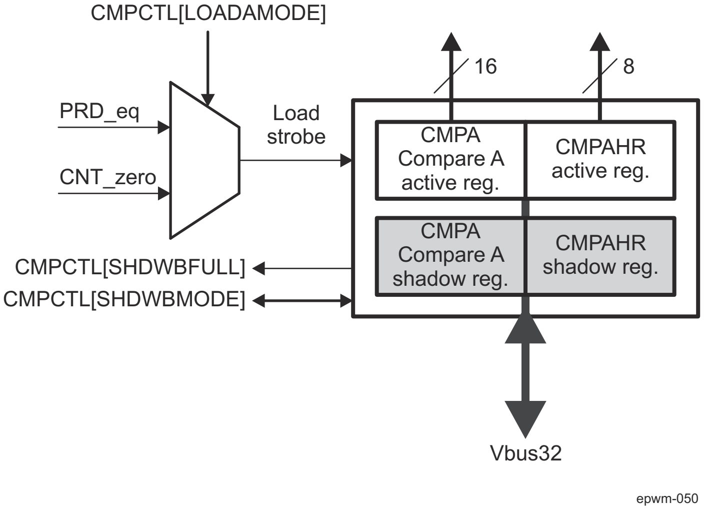


Figure 12-311. Compare A Dual Shadow register

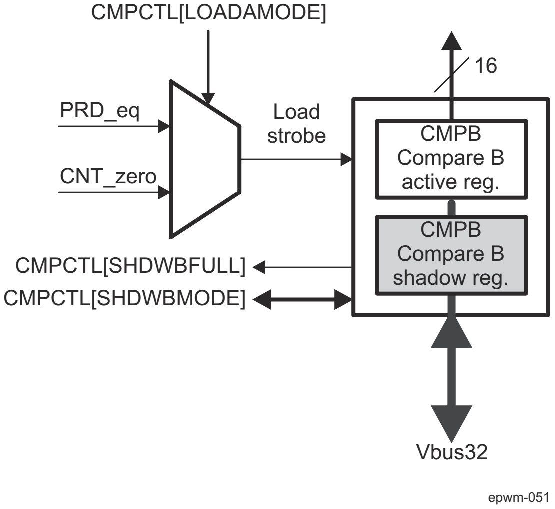


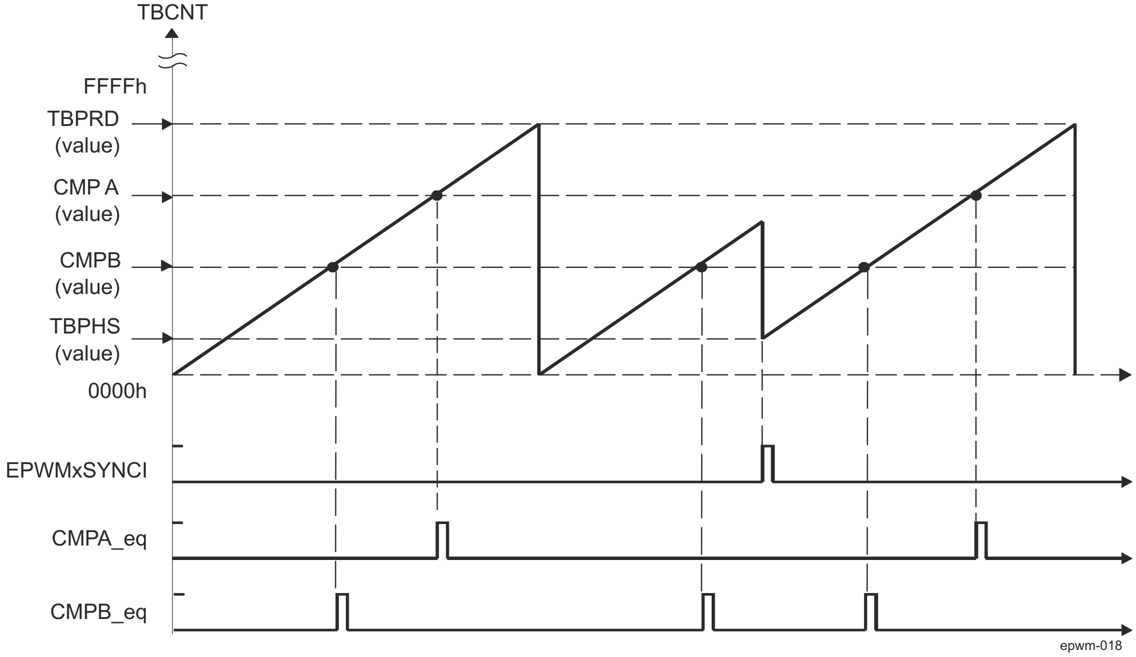
Figure 12-312. Compare B Dual Shadow register

12.5.3.4.3.4 EPWM Counter-Compare Submodule Timing Waveforms

As described in Section 12.5.3.4.2, the Time Base (TB) module can be configured to operate in 3 distinct count modes:

- Up-count mode: used to generate an asymmetrical PWM waveform.
- Down-count mode: used to generate an asymmetrical PWM waveform.
- Up-down-count mode: used to generate a symmetrical PWM waveform.

The timing diagrams in Figure 12-313 to Figure 12-316 show how CMPA and CMPB events are generated in each of the 3 count modes and how the EPWMxSYNCI signal interacts.



An EPWMxSYNCI external synchronization event can cause a discontinuity in the TBCNT count sequence. This can lead to a compare event being skipped. This skipping is considered normal operation and must be taken into account.

Figure 12-313. EPWM Counter-Compare Event Waveforms in Up-Count Mode

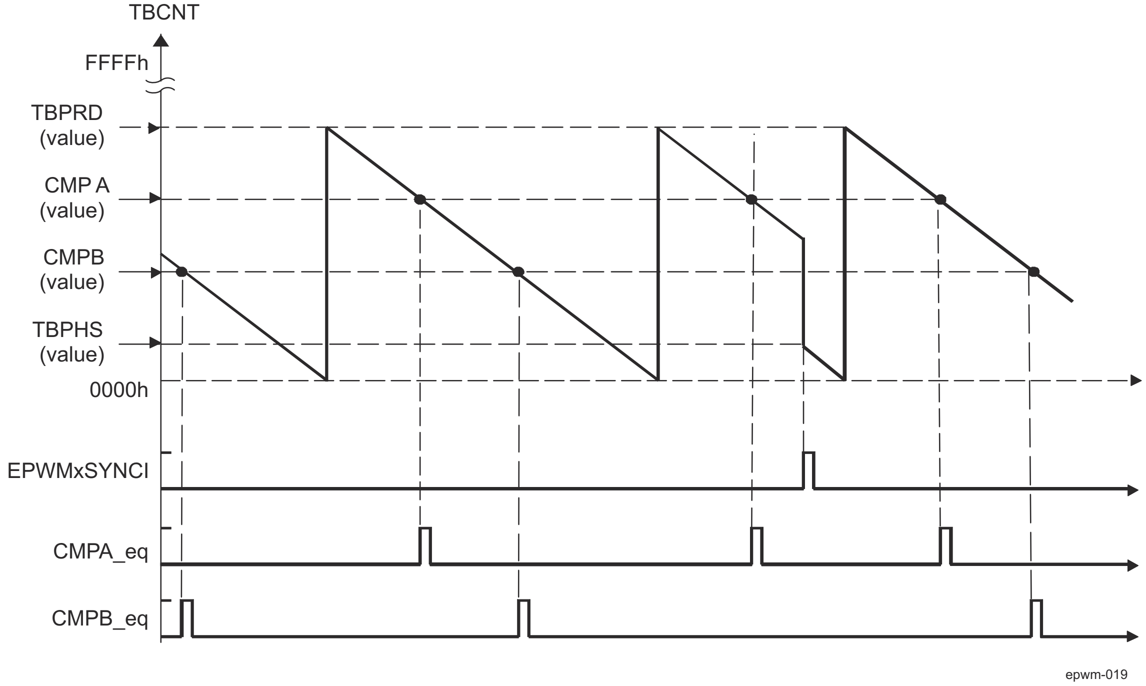


Figure 12-314. EPWM Counter-Compare Events in Down-Count Mode

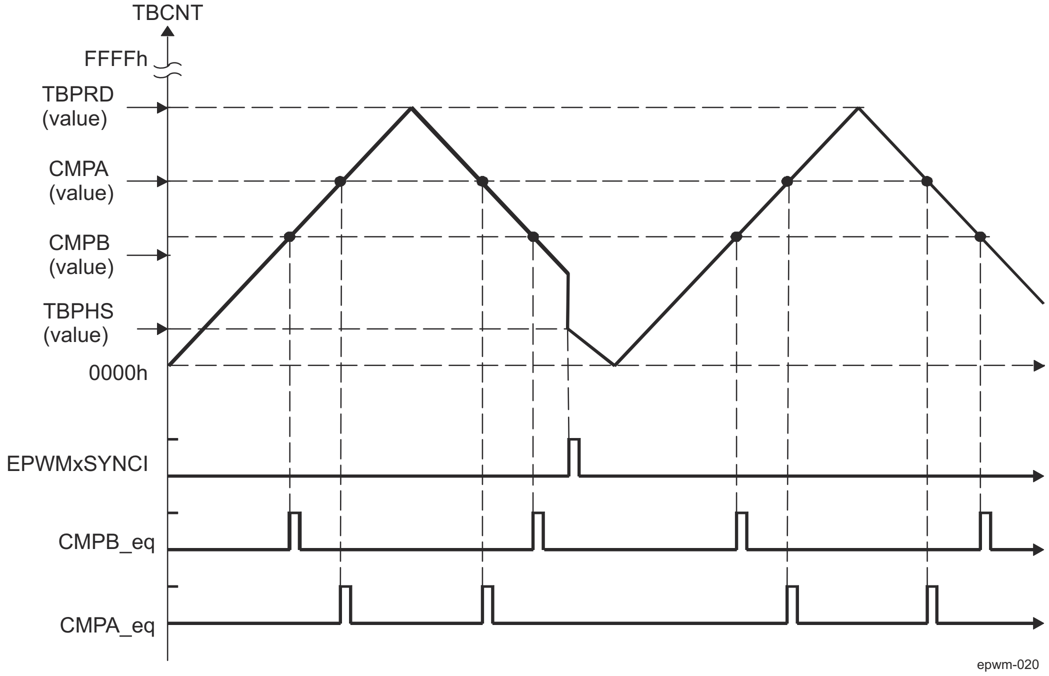


Figure 12-315. EPWM Counter-Compare Events in Up-Down-Count Mode, EPWM_TBCTL[13] PHSDIR = 0 Count Down on Synchronization Event

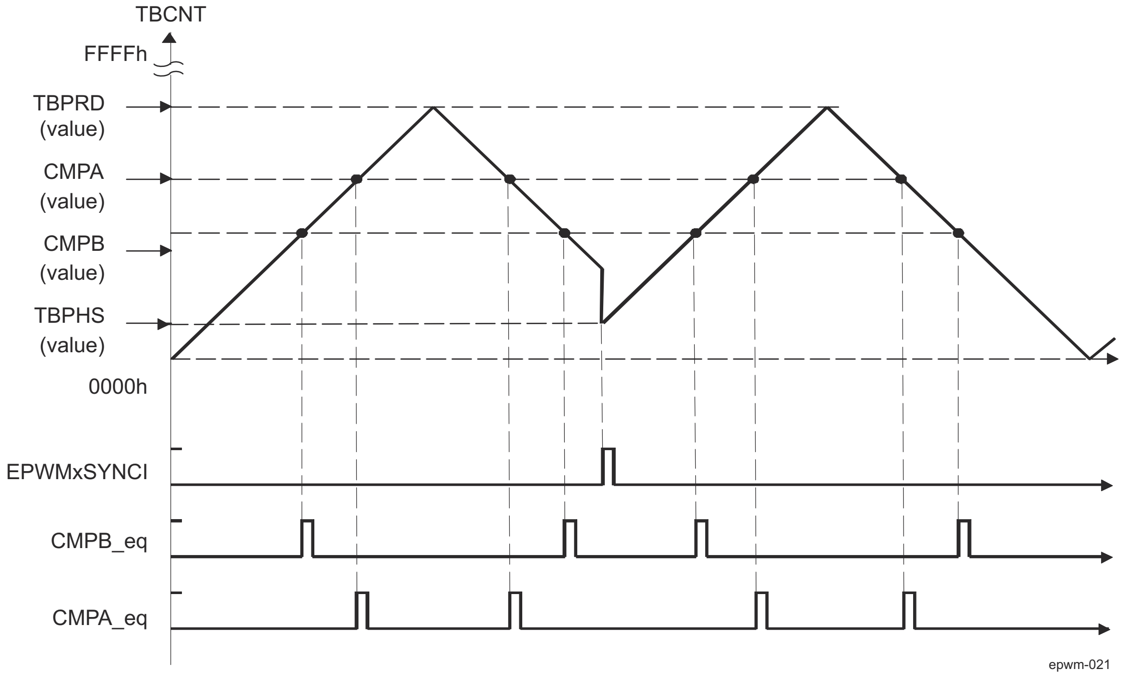


Figure 12-316. EPWM Counter-Compare Events in Up-Down-Count Mode, EPWM_TBCTL[13] PHSDIR = 1 Count Up on Synchronization Event

12.5.3.4.4 EPWM Action-Qualifier (AQ) Submodule

This section describes the Action-Qualifier (AQ) submodule in the PWM module.

12.5.3.4.4.1 Overview

Figure 12-317 shows the action-qualifier (AQ) submodule in the EPWM system. This submodule has the most important role in waveform construction and PWM generation. It decides which events are converted into various action types, thereby producing the required switched waveforms at the EPWMxA and EPWMxB outputs.

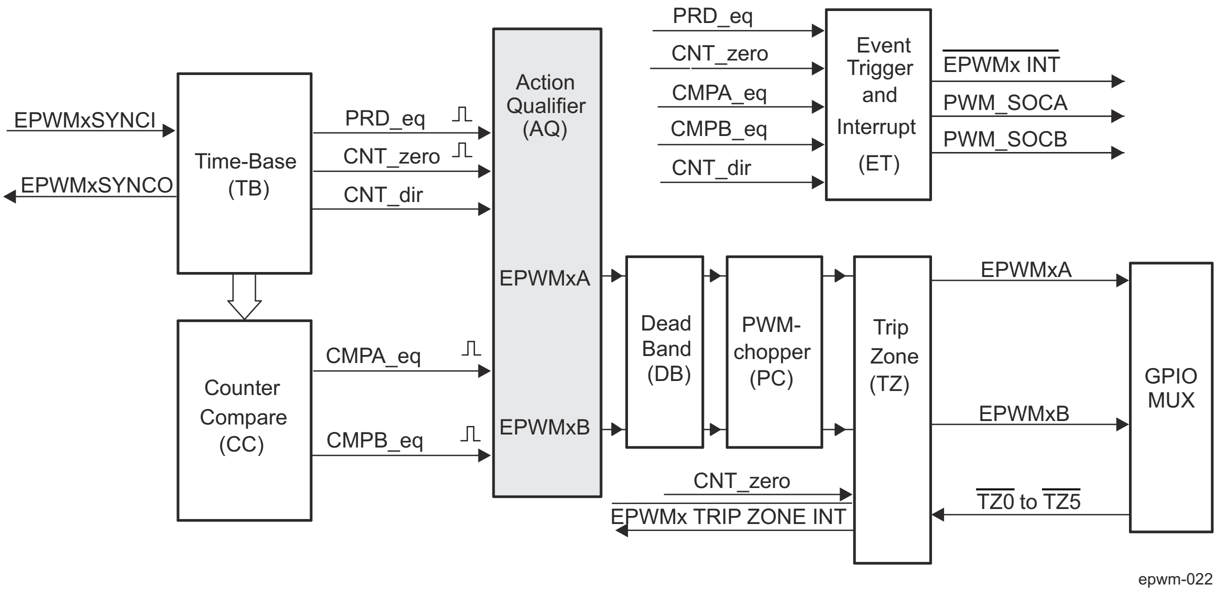


Figure 12-317. EPWM Action-Qualifier Submodule

AQ module features:

- Qualifying and generating actions (set, clear, toggle) based on the following events:
  - PRD_eq: Time-base counter equal to the period (TBCNT = TBPRD)
  - CNT_zero: Time-base counter equal to zero (TBCNT = 0000h)
  - CMPA_eq: Time-base counter equal to the counter-compare A register (TBCNT = CMPA)
  - CMPB_eq: Time-base counter equal to the counter-compare B register (TBCNT = CMPB)
- Managing priority when these events occur concurrently
- Providing independent control of events when the time-base counter is increasing and when it is decreasing

12.5.3.4.4.2 Controlling and Monitoring the EPWM Action-Qualifier Submodule

Table 12-278 lists the registers used to control and monitor the action-qualifier submodule.

Table 12-278. EPWM Action-Qualifier Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_AQCTLA	Action-Qualifier Control Register For Output A (EPWMxA)	16h	No
EPWM_AQCTLB	Action-Qualifier Control Register For Output B (EPWMxB)	18h	No
EPWM_AQSFRC	Action-Qualifier Software Force Register	1Ah	No
EPWM_AQCSFRC	Action-Qualifier Continuous Software Force	1Ch	Yes

The action-qualifier submodule is based on event-driven logic. It can be thought of as a programmable cross switch with events at the input and actions at the output, all of which are software controlled via the set of registers as shown in Figure 12-318. The possible input events are summarized again in Table 12-279.

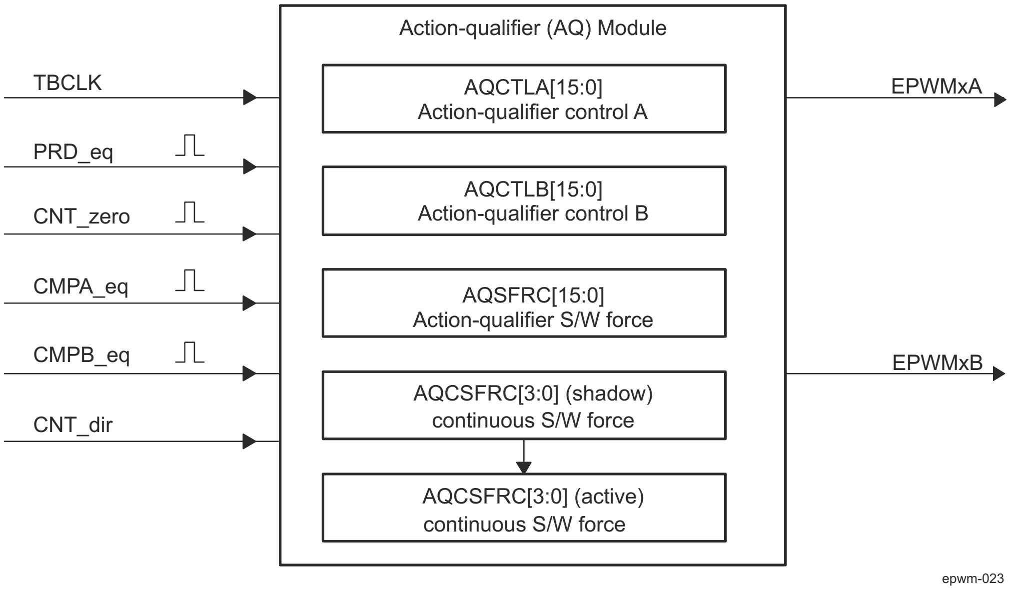


Figure 12-318. EPWM Action-Qualifier Submodule Inputs and Outputs

Table 12-279. EPWM Action-Qualifier Submodule Possible Input Events

Signal	Description	Register Bitfield Compared
PRD_eq	Time-base counter equal to the period value	TBCNT = TBPRD
CNT_zero	Time-base counter equal to zero	TBCNT = 0000h
CMPA_eq	Time-base counter equal to the counter-compare A	TBCNT = CMPA
CMPB_eq	Time-base counter equal to the counter-compare B	TBCNT = CMPB
Software forced event	Asynchronous event initiated by software	

The software forced action is a useful asynchronous event. This control is handled by EPWM_AQSFRC and EPWM_AQCSFRC registers.

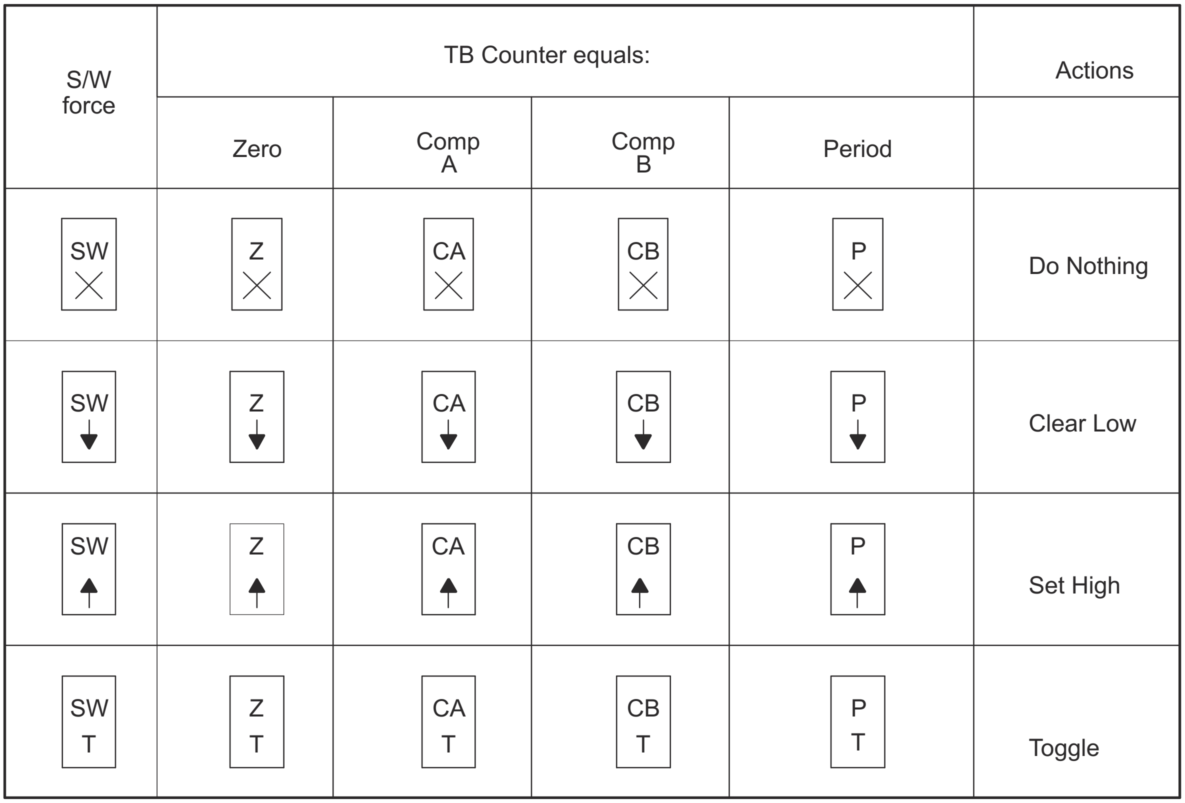
The action-qualifier submodule controls how the two outputs EPWMxA and EPWMxB behave when a particular event occurs. The event inputs to the action-qualifier submodule are further qualified by the counter direction (up or down). This allows for independent action on outputs on both the count-up and count-down phases.

The possible actions imposed on outputs EPWMxA and EPWMxB are:

- **Set High:** Set output EPWMxA or EPWMxB to a high level.
- **Clear Low:** Set output EPWMxA or EPWMxB to a low level.
- **Toggle:** If EPWMxA or EPWMxB is currently pulled high, then pull the output low. If EPWMxA or EPWMxB is currently pulled low, then pull the output high.
- **Do Nothing:** Keep outputs EPWMxA and EPWMxB at same level as currently set. Although the "Do Nothing" option prevents an event from causing an action on the EPWMxA and EPWMxB outputs, this event can still trigger interrupts. See the Event_Trigger (ET) submodule description in Section 12.5.3.4.8 for details.

Actions are specified independently for either output (EPWMxA or EPWMxB). Any or all events can be configured to generate actions on a given output. All qualifier actions are configured via the control registers found at the end of this section.

For clarity, the drawings in this chapter use a set of symbolic actions. These symbols are summarized in Figure 12-319. Each symbol represents an action as a marker in time. Some actions are fixed in time (zero and period) while the CMPA and CMPB actions are moveable and their time positions are programmed via the counter-compare A and B registers, respectively. To turn off or disable an action, use the "Do Nothing option"; it is the default at reset.



S/W force	TB Counter equals:				Actions
	Zero	Comp A	Comp B	Period	
SW ✕	Z ✕	CA ✕	CB ✕	P ✕	Do Nothing
SW ↓	Z ↓	CA ↓	CB ↓	P ↓	Clear Low
SW ↑	Z ↑	CA ↑	CB ↑	P ↑	Set High
SW T	Z T	CA T	CB T	P T	Toggle

epwm-024

Figure 12-319. Possible Action-Qualifier Actions for EPWMxA and EPWMxB Outputs

12.5.3.4.4.3 EPWM Action-Qualifier Event Priority

It is possible for the EPWM action qualifier to receive more than one event at the same time. In this case events are assigned a priority by the hardware. The general rule is: events occurring later in time have a higher priority and software forced events always have the highest priority. The event priority levels for up-down-count mode are shown in Table 12-280. A priority level 1 is the highest priority and level 7 is the lowest. The priority changes slightly depending on the direction of TBCNT.

Table 12-280. EPWM Action-Qualifier Event Priority for Up-Down-Count Mode

Priority Level	Event if TBCNT is Incrementing TBCNT = 0 up to TBCNT = TBPRD	Event if TBCNT is Decrementing TBCNT = TBPRD down to TBCNT = 1
1 (Highest)	Software forced event	Software forced event
2	Counter equals CMPB on up-count (CBU)	Counter equals CMPB on down-count (CBD)
3	Counter equals CMPA on up-count (CAU)	Counter equals CMPA on down-count (CAD)
4	Counter equals zero	Counter equals period (TBPRD in EPWM_TBPRD active register)
5	Counter equals CMPB on down-count (CBD) (1)	Counter equals CMPB on up-count (CBU) (1)
6 (Lowest)	Counter equals CMPA on down-count (CAD) (1)	Counter equals CMPA on up-count (CBU) (1)

(1) To maintain symmetry for up-down-count mode, both up-events (CAU/CBU) and down-events (CAD/CBD) can be generated for TBPRD. Otherwise, up-events can occur only when the counter is incrementing and down-events can occur only when the counter is decrementing.

Table 12-281 shows the action-qualifier priority for up-count mode. In this case, the counter direction is always defined as up and thus down-count events will never be taken.

Table 12-281. EPWM Action-Qualifier Event Priority for Up-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to period (TBPRD)
3	Counter equal to CMPB on up-count (CBU)
4	Counter equal to CMPA on up-count (CAU)
5 (Lowest)	Counter equal to Zero

Table 12-282 shows the action-qualifier priority for down-count mode. In this case, the counter direction is always defined as down and thus up-count events will never be taken.

Table 12-282. EPWM Action-Qualifier Event Priority for Down-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to Zero
3	Counter equal to CMPB on down-count (CBD)
4	Counter equal to CMPA on down-count (CAD)
5 (Lowest)	Counter equal to period (TBPRD)

It is possible to set the compare value greater than the period. In this case the action will take place as shown in Table 12-283.

Table 12-283. Behavior if CMPA/CMPB is Greater than the Period

Counter Mode	Compare on Up-Count Event CAU/CBU	Compare on Down-Count Event CAU/CBU
Up-Count Mode	If CMPA/CMPB ≤ TBPRD period, then the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB > TBPRD, then the event will not occur.	Never occurs.
Down-Count Mode	Never occurs.	If CMPA/CMPB < TBPRD, the event will occur on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB ≥ TBPRD, the event will occur on a period match (TBCNT = TBPRD).
Up-Down-Count Mode	If CMPA/CMPB < TBPRD and the counter is incrementing, the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB is ≥ TBPRD, the event will occur on a period match (TBCNT = TBPRD).	If CMPA/CMPB < TBPRD and the counter is decrementing, the event occurs on a compare match (TBCNT = CMPA or CMPB). If CMPA/CMPB ≥ TBPRD, the event occurs on a period match (TBCNT = TBPRD).

12.5.3.4.4.4 Waveforms for Common EPWM Configurations

Note

The waveforms in this chapter show the EPWMs behavior for a static compare register value. In a running system, the active compare registers (EPWM_CMPA and EPWM_CMPB) are typically updated from their respective shadow registers once every period. The user specifies when the update will take place — either when the time-base counter reaches zero or when the time-base counter reaches period. There are some cases when the action based on the new value can be delayed by one period or the action based on the old value can take effect for an extra period. Some PWM configurations avoid this situation. These include, but are not limited to, the following:

Use up-down-count mode to generate a symmetric PWM:

- If EPWM_CMPA / EPWM_CMPB is loaded on zero, then use EPWM_CMPA / EPWM_CMPB values greater than or equal to 1.
- If EPWM_CMPA / EPWM_CMPB is loaded on period, then use EPWM_CMPA / EPWM_CMPB values less than or equal to TBPRD - 1.

  This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

Use up-down-count mode to generate an asymmetric PWM:

- To achieve 50-0% asymmetric PWM use the following configuration: Load EPWM_CMPA / EPWM_CMPB on period and use the period action to clear the PWM and a compare-up action to set the PWM. Modulate the compare value from 0 to TBPRD to achieve 50-0% PWM duty.

When using up-count mode to generate an asymmetric PWM:

- To achieve 0-100% asymmetric PWM use the following configuration: Load EPWM_CMPA / EPWM_CMPB on TBPRD. Use the Zero action to set the PWM and a compare-up action to clear the PWM. Modulate the compare value from 0 to TBPRD+1 to achieve 0-100% PWM duty.

Figure 12-320 shows how a symmetric PWM waveform can be generated using the up-down-count mode of the TBCNT. In this mode 0-100% DC modulation is achieved by using equal compare matches on the up count and down count portions of the waveform. In the example shown, CMPA is used to make the comparison. When the counter is incrementing the CMPA match will pull the PWM output high. Likewise, when the counter is decrementing the compare match will pull the PWM signal low. When EPWM_CMPA = EPWM_TBPRD, the PWM signal is low for the entire period giving the 0% duty waveform. When CMPA = 0, the PWM signal is high achieving 100% duty.

When using this configuration in practice, if CMPA/CMPB is loaded on zero, then use CMPA/CMPB values greater than or equal to 1. If CMPA/CMPB is loaded on period, then use CMPA/CMPB values less than or equal to TBPRD - 1. This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

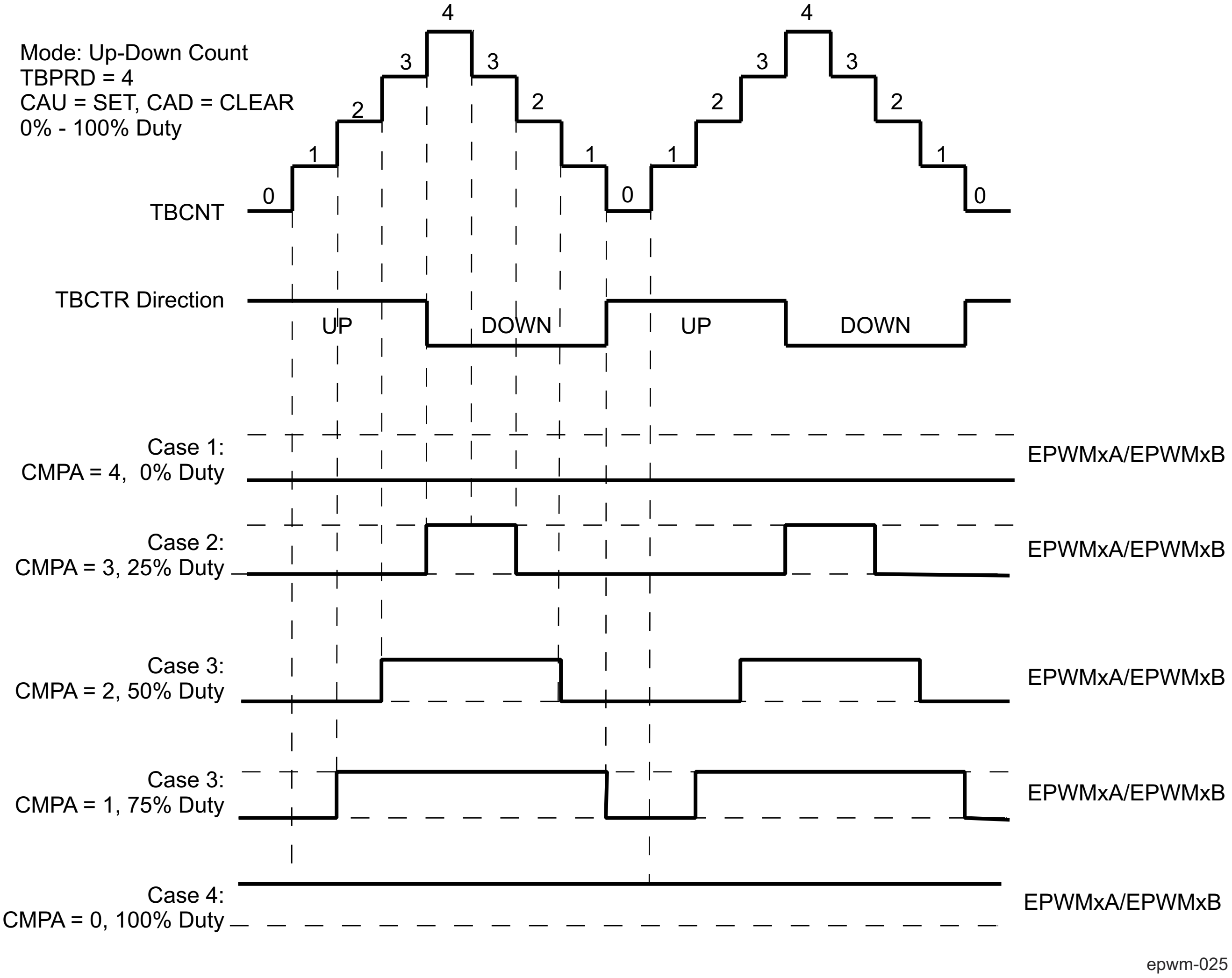
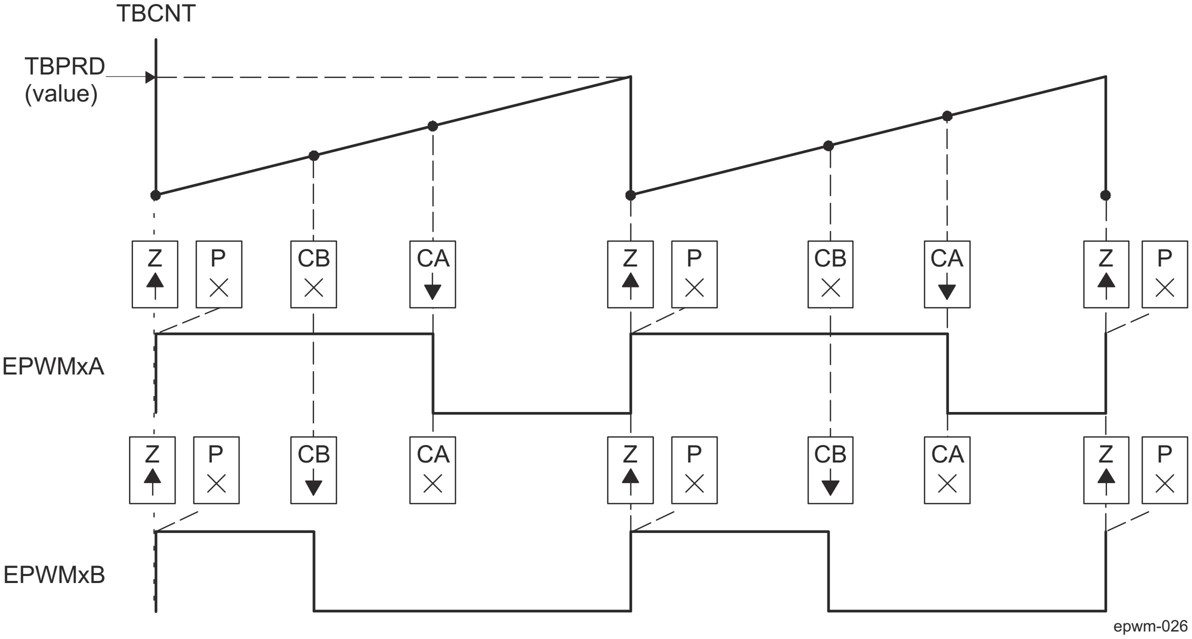


Figure 12-320. EPWM Up-Down-Count Mode Symmetrical Waveform

The PWM waveforms in Figure 12-321 through Figure 12-326 show some common action-qualifier configurations. Some conventions used in the figures are as follows:

- TBPRD, CMPA, and CMPB refer to the value written in their respective registers (EPWM_TBPRD, EPWM_CMPA, and EPWM_CMPB). The active register, not the shadow register, is used by the hardware.
- CMPx, refers to either CMPA or CMPB.
- EPWMxA and EPWMxB refer to the output signals from EPWMx
- Up-Down means Count-up-and-down mode, Up means up-count mode and Dwn means down-count mode
- Sym = Symmetric, Asym = Asymmetric

Table 12-284 and Table 12-285 contain initialization and runtime register configurations for the waveforms in Figure 12-321.



A. PWM period = (TBPRD + 1) × T_{TBCLK}

B. Duty modulation for EPWMxA is set by CMPA, and is active high (that is, high time duty proportional to CMPA).

C. Duty modulation for EPWMxB is set by CMPB and is active high (that is, high time duty proportional to CMPB).

D. The "Do Nothing" actions (X) are shown for completeness, but will not be shown on subsequent diagrams.

E. Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCNT wraps from period to 0000h.

Figure 12-321. Up, Single Edge Asymmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Active High

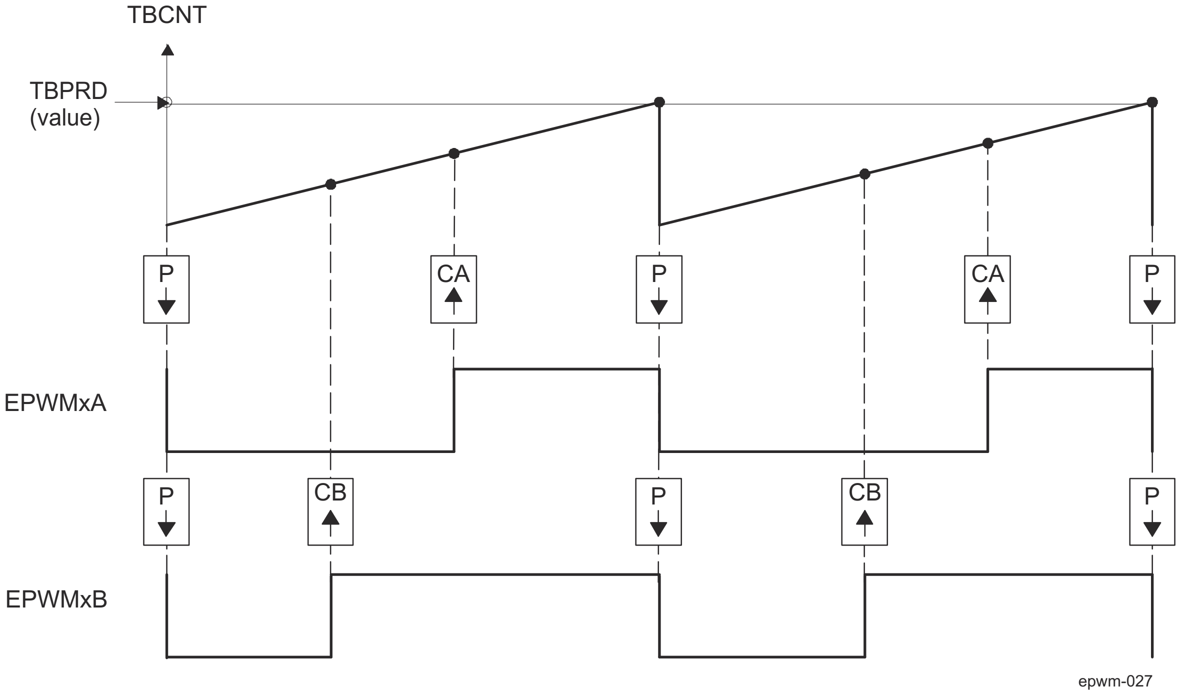
Table 12-284. EPWMx Initialization for Figure 12-321

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	200 (C8h)	Compare B = 200 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	ZRO	AQ_SET	
	CAU	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_SET	
	CBU	AQ_CLEAR	

Table 12-285. EPWMx Run Time Changes for Figure 12-321

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-286 and Table 12-287 contain initialization and runtime register configurations for the waveforms in Figure 12-322.



A. PWM period = (TBPRD + 1) × T_{TBCLK}

B. Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).

C. Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

D. The Do Nothing actions (X) are shown for completeness here, but will not be shown on subsequent diagrams.

E. Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCNT wraps from period to 0000h.

Figure 12-322. Up, Single Edge Asymmetric Waveform With Independent Modulation on EPWMxA and EPWMxB — Active Low

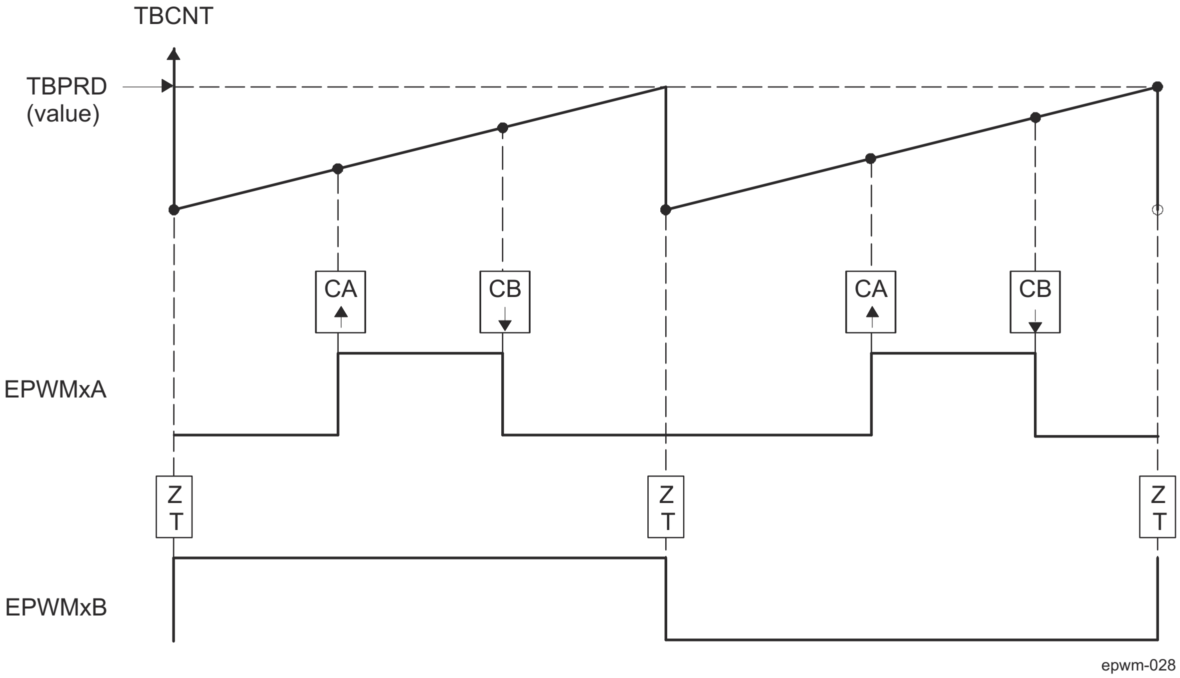
Table 12-286. EPWMx Initialization for Figure 12-322

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	200 (C8h)	Compare B = 200 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	PRD	AQ_CLEAR	
	CAU	AQ_SET	
EPWM_AQCTLB	PRD	AQ_CLEAR	
	CBU	AQ_SET	

Table 12-287. EPWMx Run Time Changes for Figure 12-322

Register	Bit	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-288 and Table 12-289 contain initialization and runtime register configurations for the waveforms Figure 12-323. Use the code in Example 12-8 to define the headers.



A. PWM frequency = 1/((TBPRD + 1) × T_{TBCLK})
B. Pulse can be placed anywhere within the PWM cycle (0000h - TBPRD)
C. High time duty proportional to (CMPB - CMPA)
D. EPWMxB can be used to generate a 50% duty square wave with frequency = 1/2 × ((TBPRD + 1) × TBCLK)

Figure 12-323. Up-Count, Pulse Placement Asymmetric Waveform With Independent Modulation on EPWMxA

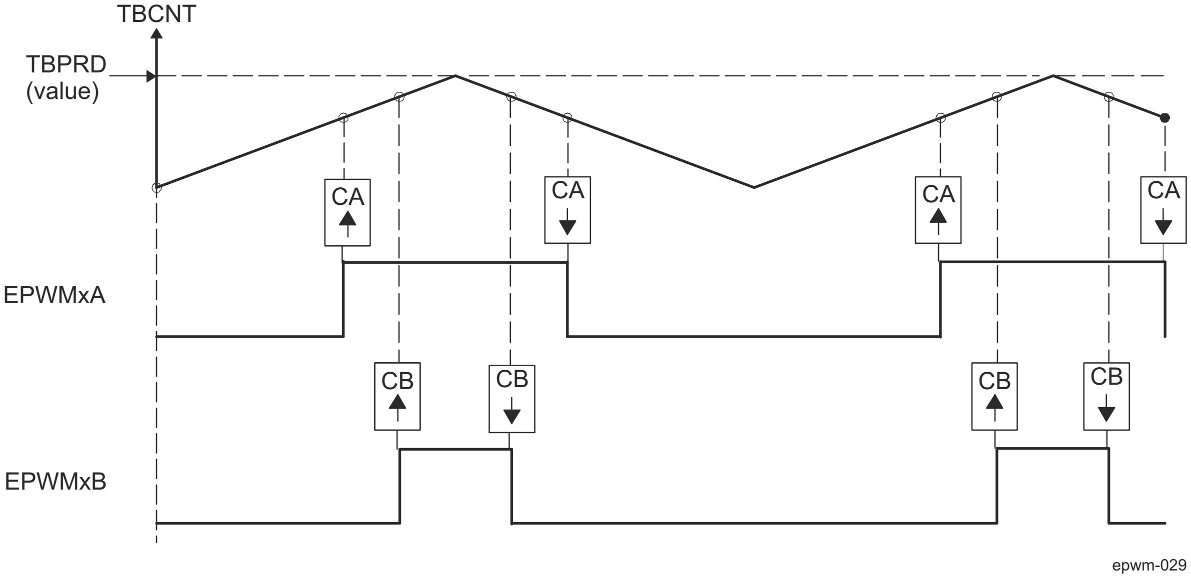
Table 12-288. EPWMx Initialization for Figure 12-323

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UP	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	200 (C8h)	Compare A = 200 TBCLK counts
EPWM_CMPB	CMPB	400 (190h)	Compare B = 400 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CBU	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_TOGGLE	

Table 12-289. EPWMx Run Time Changes for Figure 12-323

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	EdgePosA	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	EdgePosB	

Table 12-290 and Table 12-291 contain initialization and runtime register configurations for the waveforms in Figure 12-324. Use the code in Example 12-8 to define the headers.



A. PWM period = 2 x TBPRD × T_{TBCLK}

B. Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).

C. Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

D. Outputs EPWMxA and EPWMxB can drive independent power switches.

Figure 12-324. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Active Low

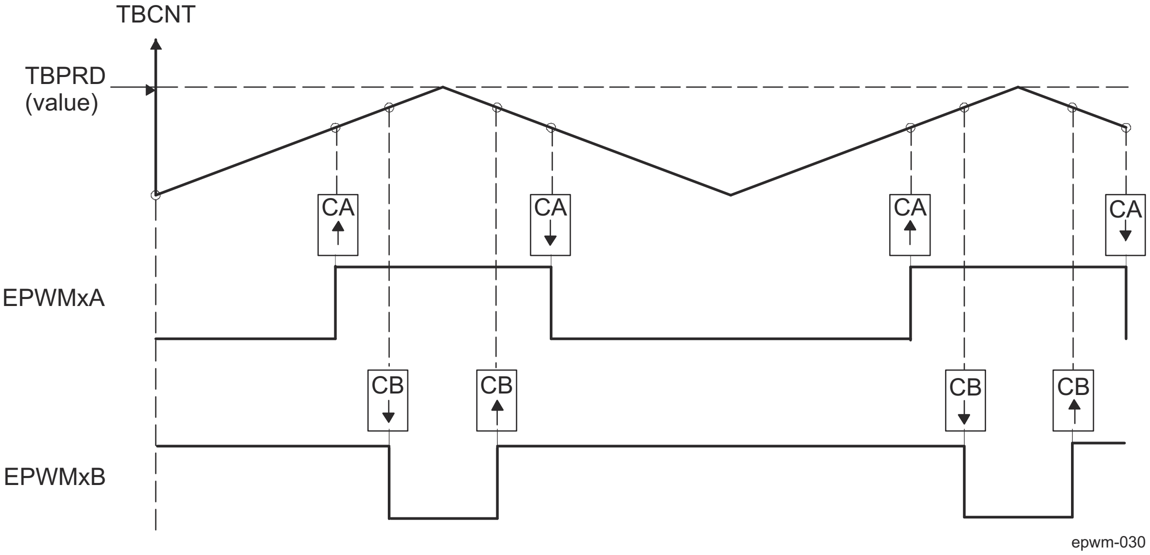
Table 12-290. EPWMx Initialization for Figure 12-324

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	400 (190h)	Compare A = 400 TBCLK counts
EPWM_CMPB	CMPB	500 (1F4h)	Compare B = 500 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CAD	AQ_CLEAR	
EPWM_AQCTLB	CBU	AQ_SET	
	CBD	AQ_CLEAR	

Table 12-291. EPWMx Run Time Changes for Figure 12-324

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-292 and Table 12-293 contain initialization and runtime register configurations for the waveforms in Figure 12-325. Use the code in Example 12-8 to define the headers.



A. PWM period = 2 × TBPRD × T_{TBCLK}
B. Duty modulation for EPWMxA is set by CMPA, and is active low, that is, low time duty proportional to CMPA.
C. Duty modulation for EPWMxB is set by CMPB and is active high, that is, high time duty proportional to CMPB.
D. Outputs EPWMx can drive upper/lower (complementary) power switches.
E. Dead-band = CMPB - CMPA (fully programmable edge placement by software). Note the dead-band module is also available if the more classical edge delay method is required.

Figure 12-325. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB — Complementary

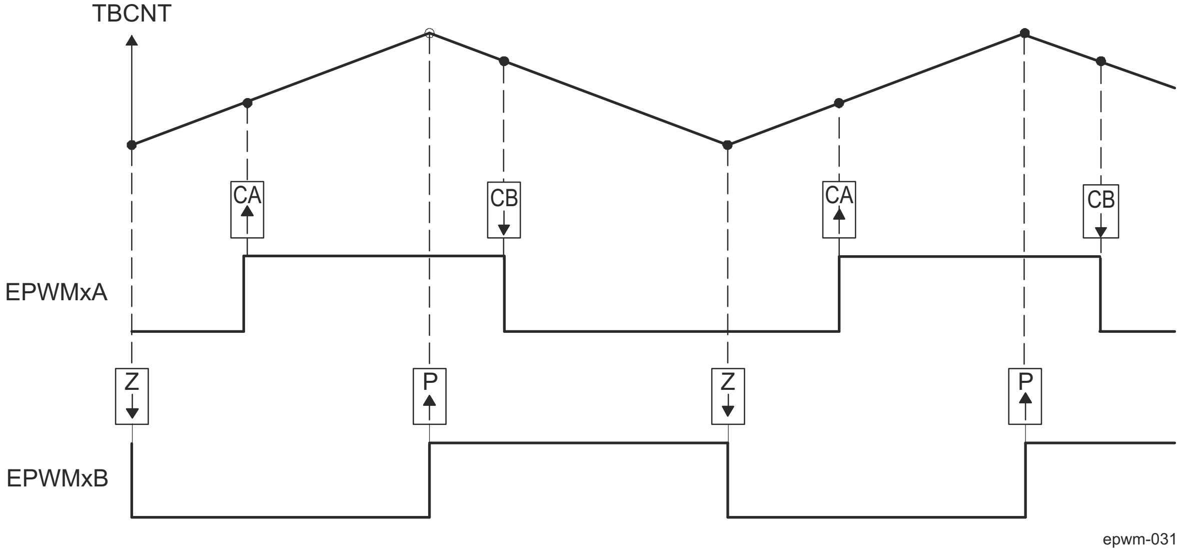
Table 12-292. EPWMx Initialization for Figure 12-325

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	350 (15Eh)	Compare A = 350 TBCLK counts
EPWM_CMPB	CMPB	400 (190h)	Compare B = 400 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CAD	AQ_CLEAR	
EPWM_AQCTLB	CBU	AQ_CLEAR	
	CBD	AQ_SET	

Table 12-293. EPWMx Run Time Changes for Figure 12-325

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	Duty1A	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	Duty1B	Adjust duty for output EPWM1B

Table 12-294 and Table 12-295 contain initialization and runtime register configurations for the waveforms in Figure 12-326. Use the code in Example 12-8 to define the headers.



A. PWM period = 2 × TBPRD × TBCLK

B. Rising edge and falling edge can be asymmetrically positioned within a PWM cycle. This allows for pulse placement techniques.

C. Duty modulation for EPWMxA is set by CMPA and CMPB.

D. Low time duty for EPWMxA is proportional to (CMPA + CMPB).

E. To change this example to active high, CMPA and CMPB actions need to be inverted (that is, Set ! Clear and Clear Set).

F. Duty modulation for EPWMxB is fixed at 50% (utilizes spare action resources for EPWMxB).

Figure 12-326. Up-Down-Count, Dual Edge Asymmetric Waveform, With Independent Modulation on EPWMxA — Active Low

Table 12-294. EPWMx Initialization for Figure 12-326

Register	Bitfield	Value	Comments
EPWM_TBPRD	TBPRD	600 (258h)	Period = 601 TBCLK counts
EPWM_TBPHS	TBPHS	0	Clear Phase Register to 0
EPWM_TBCNT	TBCNT	0	Clear TB counter
EPWM_TBCTL	CTRMODE	TB_UPDOWN	
	PHSEN	TB_DISABLE	Phase loading disabled
	PRDLD	TB_SHADOW	
	SYNCOSEL	TB_SYNC_DISABLE	
	HSPCLKDIV	TB_DIV1	TBCLK = FICLK
	CLKDIV	TB_DIV1	
EPWM_CMPA	CMPA	250 (FAh)	Compare A = 250 TBCLK counts
EPWM_CMPB	CMPB	450 (1C2h)	Compare B = 450 TBCLK counts
EPWM_CMPCTL	SHDWAMODE	CC_SHADOW	
	SHDWBMODE	CC_SHADOW	
	LOADAMODE	CC_CTR_ZERO	Load on TBCNT = 0
	LOADBMODE	CC_CTR_ZERO	Load on TBCNT = 0
EPWM_AQCTLA	CAU	AQ_SET	
	CBD	AQ_CLEAR	
EPWM_AQCTLB	ZRO	AQ_CLEAR	
	PRD	AQ_SET	

Table 12-295. EPWMx Run Time Changes for Figure 12-326

Register	Bitfield	Value	Comments
EPWM_CMPA	CMPA	EdgePosA	Adjust duty for output EPWM1A
EPWM_CMPB	CMPB	EdgePosB	Adjust duty for output EPWM1B

12.5.3.4.5 EPWM Dead-Band Generator (DB) Submodule

This section describes the Dead-Band Generator (DB) submodule in the PWM module.

12.5.3.4.5.1 Overview

Figure 12-327 illustrates the dead-band generator submodule within the EPWM module.

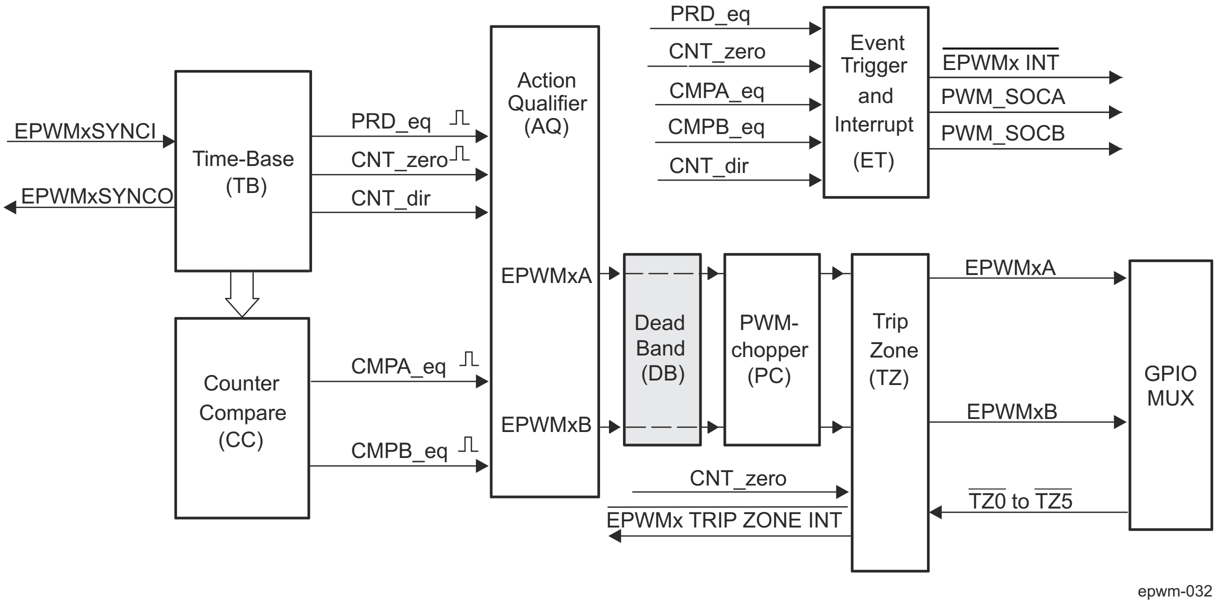


Figure 12-327. Dead-Band Generator Submodule

The "Action-qualifier (AQ) Module" section discussed how it is possible to generate the required dead-band by having full control over edge placement using both the CMPA and CMPB resources of the EPWM module. However, if the more classical edge delay-based dead-band with polarity control is required, then the dead-band generator submodule should be used.

The key functions of the dead-band generator submodule are:

- Generating appropriate signal pairs (EPWMxA and EPWMxB) with dead-band relationship from a single EPWMxA input
- Programming signal pairs for:
  - Active high (AH)
  - Active low (AL)
  - Active high complementary (AHC)
  - Active low complementary (ALC)
- Adding programmable delay to rising edges (RED)
- Adding programmable delay to falling edges (FED)
- Can be totally bypassed from the signal path (note dotted lines in Figure 12-327)

12.5.3.4.5.2 Controlling and Monitoring the EPWM Dead-Band Submodule

The dead-band generator submodule operation is controlled and monitored via the following registers:

Table 12-296. Dead-Band Generator Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_DBCTL	Dead-Band Control Register	1Eh	No
EPWM_DBRED	Dead-Band Rising Edge Delay Count Register	20h	No
EPWM_DBFED	Dead-Band Falling Edge Delay Count Register	22h	No

12.5.3.4.5.3 Operational Highlights for the EPWM Dead-Band Generator Submodule

The dead-band submodule has two groups of independent selection options as shown in Figure 12-328.

- **Input Source Selection:** The input signals to the dead-band module are the EPWMxA and EPWMxB output signals from the action-qualifier. In this section they will be referred to as EPWMxA In and EPWMxB In. Using the EPWM_DBCTL[5-4] IN_MODE control bits, the signal source for each delay, falling-edge or rising-edge, can be selected:
  - EPWMxA In is the source for both falling-edge and rising-edge delay. This is the default mode.
  - EPWMxA In is the source for falling-edge delay, EPWMxB In is the source for rising-edge delay.
  - EPWMxA In is the source for rising edge delay, EPWMxB In is the source for falling-edge delay.
  - EPWMxB In is the source for both falling-edge and rising-edge delay.
- **Output Mode Control:** The output mode is configured by way of the EPWM_DBCTL[1-0] OUT_MODE bit fields. These bits determine if the falling-edge delay, rising-edge delay, neither, or both are applied to the input signals.
- **Polarity Control:** The polarity control (EPWM_DBCTL[3-2] POLSEL) allows to be specified whether the rising-edge delayed signal and/or the falling-edge delayed signal is to be inverted before being sent out of the dead-band submodule.

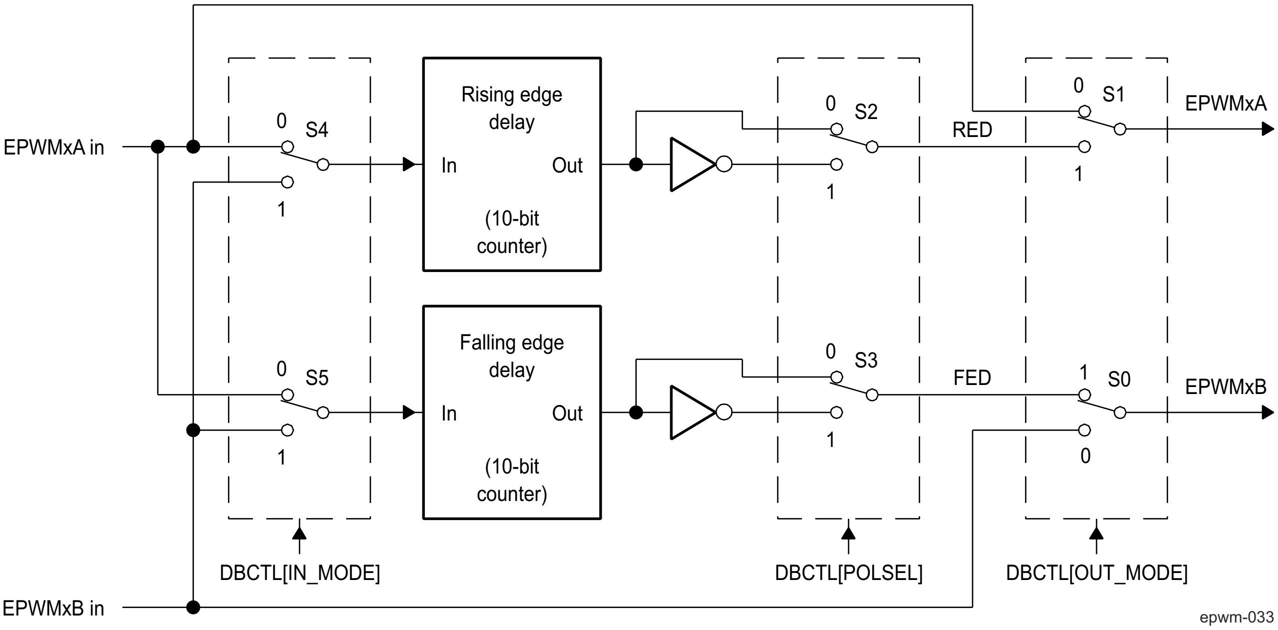


Figure 12-328. Configuration Options for the EPWM Dead-Band Generator Submodule

Although all combinations are supported, not all are typical usage modes. Table 12-297 lists some classical dead-band configurations. These modes assume that the EPWM_DBCTL[5-4] IN_MODE is configured such that EPWMxA In is the source for both falling-edge and rising-edge delay. Enhanced, or non-traditional modes can be achieved by changing the input signal source. The modes shown in Table 12-297 fall into the following categories:

- **Mode 1: Bypass both falling-edge delay (FED) and rising-edge delay (RED)** Allows to be fully disabled the dead-band submodule from the PWM signal path.
- **Mode 2-5: Classical Dead-Band Polarity Settings** These represent typical polarity configurations that should address all the active high/low modes required by available industry power switch gate drivers. The waveforms for these typical cases are shown in Figure 12-329. Note that to generate equivalent waveforms to Figure 12-329, configure the action-qualifier submodule to generate the signal as shown for EPWMxA.
- **Mode 6: Bypass rising-edge-delay and Mode 7: Bypass falling-edge-delay** Finally the last two entries in Table 12-297 show combinations where either the falling-edge-delay (FED) or rising-edge-delay (RED) blocks are bypassed.

Table 12-297. Classical Dead-Band Operating Modes

		EPWM_DBCTL[3-2] POLSEL		EPWM_DBCTL[1-0] OUT_MODE	
Mode	**Mode Description** (1)	**S3**	**S2**	**S1**	**S0**
1	EPWMxA and EPWMxB Passed Through (No Delay)	x	x	0	0
2	Active High Complementary (AHC)	1	0	1	1
3	Active Low Complementary (ALC)	0	1	1	1
4	Active High (AH)	0	0	1	1
5	Active Low (AL)	1	1	1	1
6	EPWMxA Out = EPWMxA In (No Delay) EPWMxB Out = EPWMxA In with Falling Edge Delay	0 or 1	0 or 1	0	1
7	EPWMxA Out = EPWMxA In with Rising Edge Delay EPWMxB Out = EPWMxB In with No Delay	0 or 1	0 or 1	1	0

(1) These are classical dead-band modes and assume that EPWM_DBCTL[5-4] IN_MODE = 0h0. That is, EPWMxA in is the source for both the falling-edge and rising-edge delays. Enhanced, non-traditional modes can be achieved by changing the IN_MODE configuration.

Figure 12-329 shows waveforms for typical cases where 0% < duty < 100%.

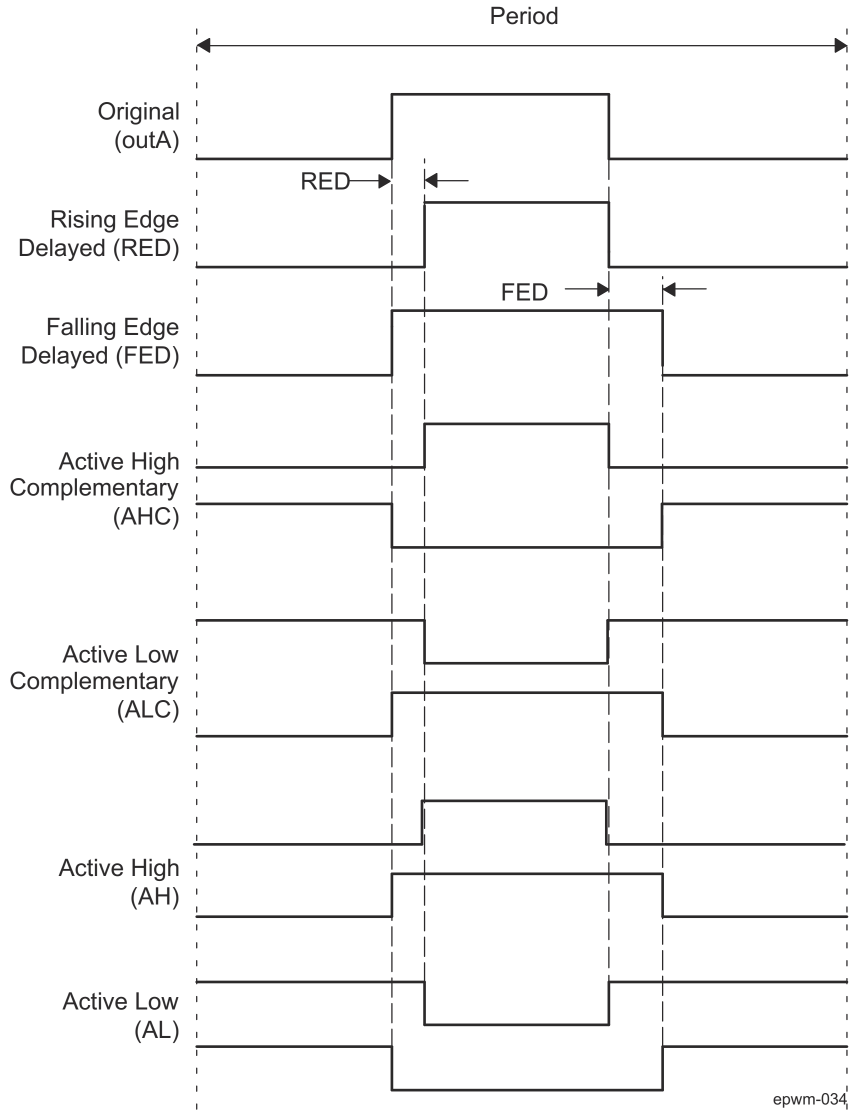


Figure 12-329. Dead-Band Waveforms for Typical Cases (0% < Duty < 100%)

The dead-band submodule supports independent values for rising-edge (RED) and falling-edge (FED) delays. The amount of delay is programmed using the EPWM_DBRED and EPWM_DBFED registers. These are 10-bit registers and their value represents the number of time-base clock, TBCLK, periods a signal edge is delayed by. For example, the formulas to calculate falling-edge-delay and rising-edge-delay are:

$\text{FED} = \text{EPWM\_DBFED} \times T_{\text{TBCLK}}$

$\text{RED} = \text{EPWM\_DBRED} \times T_{\text{TBCLK}}$

Where T_{TBCLK} is the period of TBCLK, the prescaled version of FICLK.

12.5.3.4.6 EPWM-Chopper (PC) Submodule

This section describes the PWM-Chopper (PC) submodule in the PWM module.

12.5.3.4.6.1 Overview

Figure 12-330 illustrates the PWM-chopper (PC) submodule within the EPWM module. The PWM-chopper submodule allows a high-frequency carrier signal to modulate the PWM waveform generated by the action-qualifier and dead-band submodules. This capability is important if a pulse transformer-based gate drivers to control the power switching elements is needed.

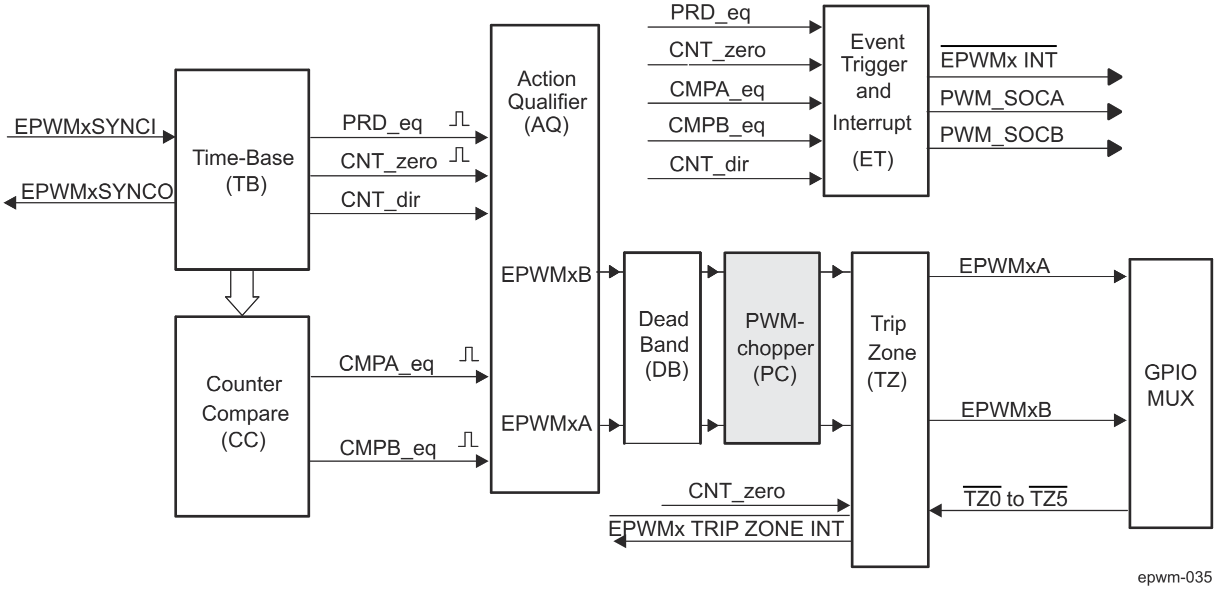


Figure 12-330. PWM-Chopper Submodule

12.5.3.4.6.2

PC module key features:

- Programmable chopping (carrier) frequency
- Programmable pulse width of first pulse
- Programmable duty cycle of second and subsequent pulses
- Can be fully bypassed if not required

12.5.3.4.6.3 Controlling the EPWM-Chopper Submodule

The EPWM-chopper submodule operation is controlled via the register in Table 12-298.

Table 12-298. EPWM-Chopper Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_PCCTL	PWM-chopper Control Register	3Ch	No

12.5.3.4.6.4 Operational Highlights for the EPWM-Chopper Submodule

Figure 12-331 shows the operational details of the EPWM-chopper submodule. The carrier clock is derived from FICLK. Its frequency and duty cycle are controlled via the CHPFREQ and CHPDUTY bits in the EPWM_PCCTL register. The one-shot block is a feature that provides a high energy first pulse to ensure hard and fast power switch turn on, while the subsequent pulses sustain pulses, ensuring the power switch remains on. The one-shot width is programmed via the OSHTWTH bits. The PWM-chopper submodule can be fully disabled (bypassed) via the CHPEN bit.

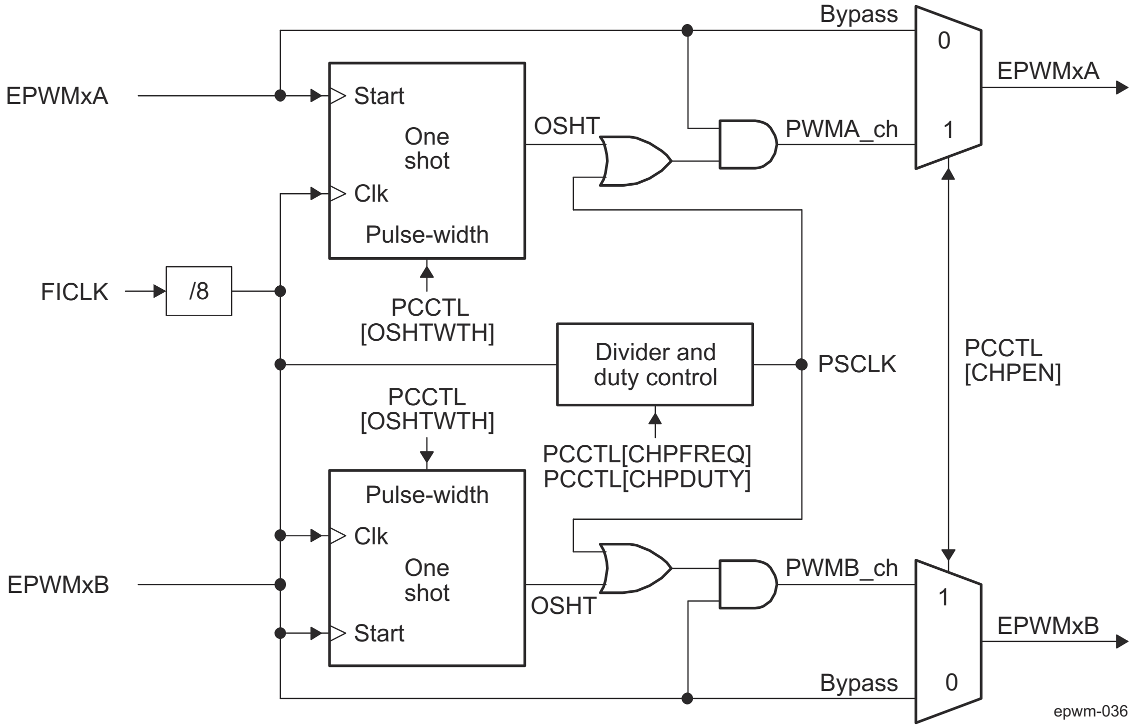


Figure 12-331. PWM-Chopper Submodule Signals and Registers

12.5.3.4.6.5 EPWM-Chopper Waveforms

Figure 12-332 shows simplified waveforms of the chopping action only; one-shot and duty-cycle control are not shown. Details of the one-shot and duty-cycle control are discussed in the following sections.

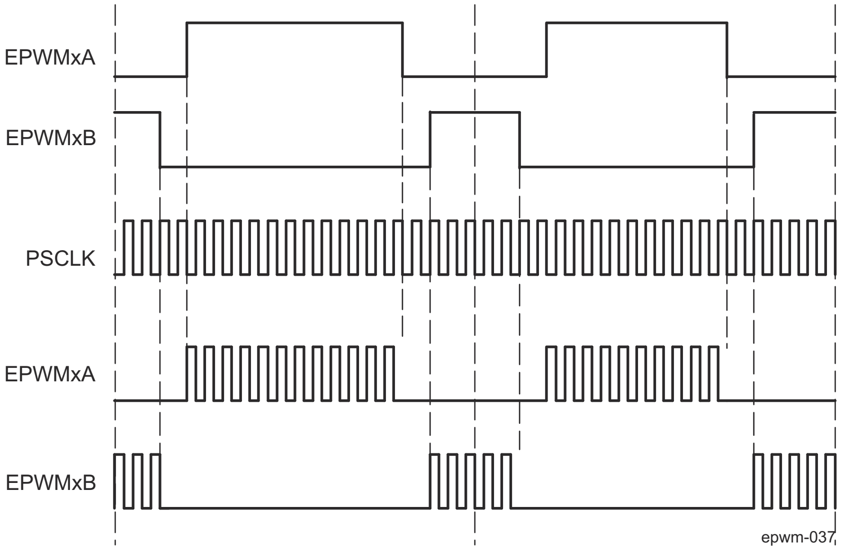


Figure 12-332. Simple EPWM-Chopper Submodule Waveforms Showing Chopping Action Only

12.5.3.4.6.5.1 EPWM-Chopper One-Shot Pulse

The width of the first pulse can be programmed to any of 16 possible pulse width values. The width or period of the first pulse is given by:

$T_{1stpulse} = T_{FICLK} \times 8 \times OSHTWTH$

Where T_{FICLK} is the period of the system clock (FICLK) and OSHTWTH is the four control bits (value from 1 to 16)

Figure 12-333 shows the first and subsequent sustaining pulses.

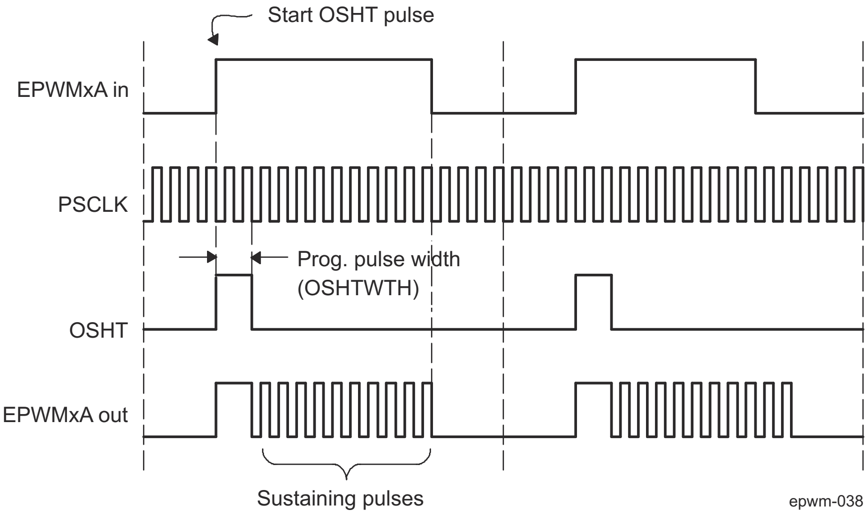


Figure 12-333. EPWM-Chopper Submodule Waveforms Showing the First Pulse and Subsequent Sustaining Pulses

12.5.3.4.6.5.2 EPWM-Chopper Duty Cycle Control

Pulse transformer-based gate drive designs need to comprehend the magnetic properties or characteristics of the transformer and associated circuitry. Saturation is one such consideration. To assist the gate drive designer, the duty cycles of the second and subsequent pulses have been made programmable. These sustaining pulses ensure the correct drive strength and polarity is maintained on the power switch gate during the on period, and hence a programmable duty cycle allows a design to be tuned or optimized via software control.

Figure 12-334 shows the duty cycle control that is possible by programming the CHPDUTY bits. One of seven possible duty ratios can be selected ranging from 12.5 to 87.5%.

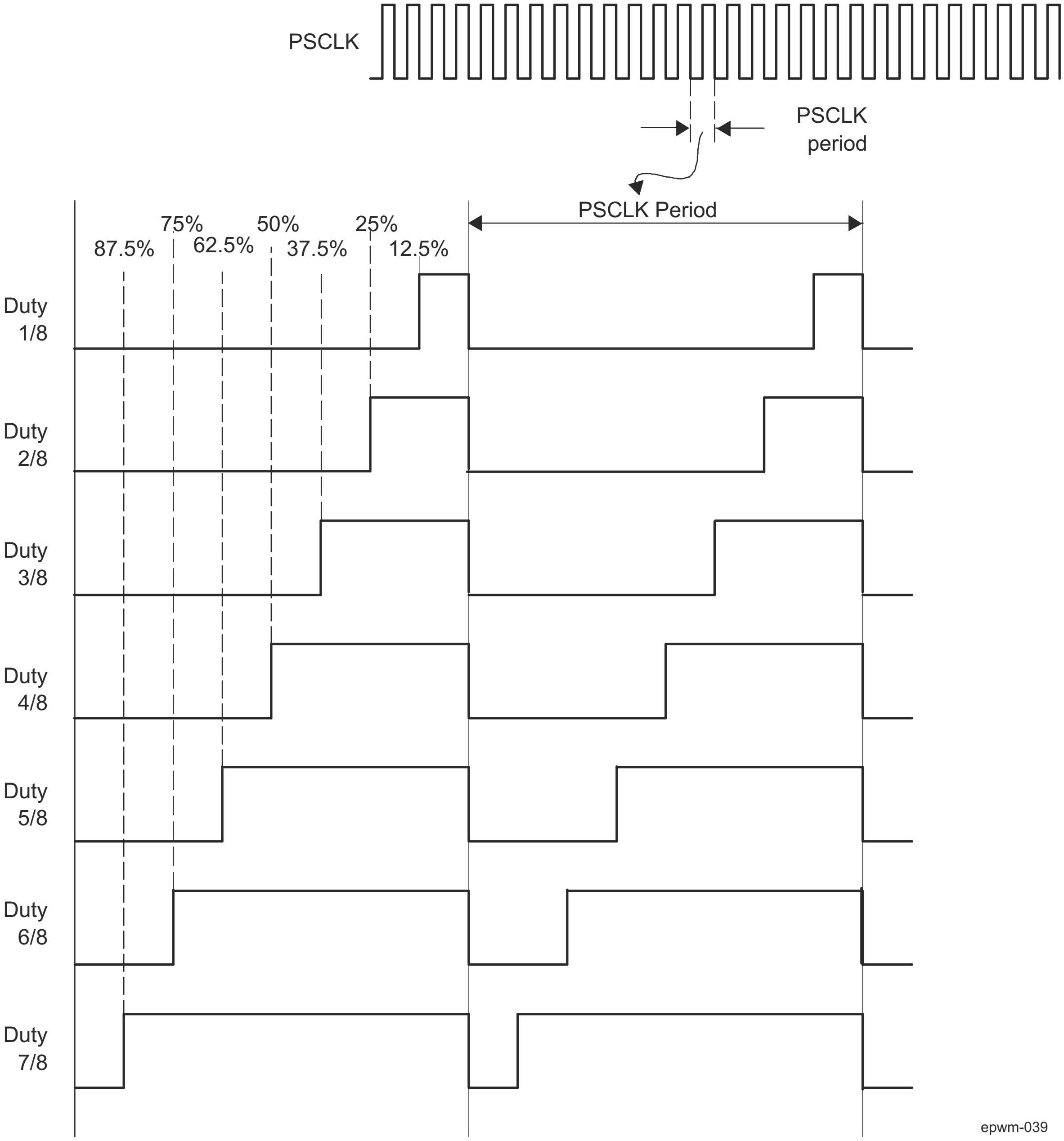


Figure 12-334. EPWM-Chopper Submodule Waveforms Showing the Pulse Width (Duty Cycle) Control of Sustaining Pulses

12.5.3.4.7 EPWM Trip-Zone (TZ) Submodule

This section describes the Trip-Zone (TZ) submodule in the PWM module.

12.5.3.4.7.1 Overview

Figure 12-335 shows how the trip-zone (TZ) submodule fits within the EPWM module. Each EPWM module is connected to six $\overline{\mathrm{TZ}}$ signals ($\overline{\mathrm{TZ0}}$ to $\overline{\mathrm{TZ5}}$) that are sourced from the GPIO MUX. These signals indicates external fault or trip conditions, and the EPWM outputs can be programmed to respond accordingly when faults occur. See *EPWM Integration* to determine the number of trip-zone pins available for the device.

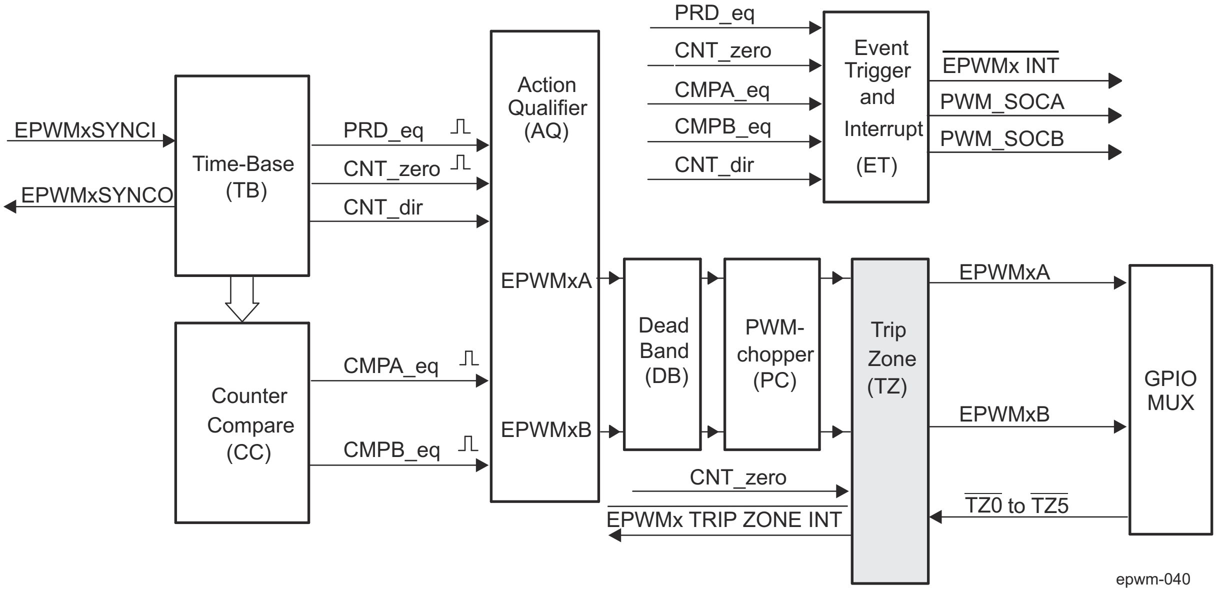


Figure 12-335. EPWM Trip-Zone Submodule

The key functions of the trip-zone submodule are:

- Trip inputs $\overline{\mathrm{TZ0}}$ to $\overline{\mathrm{TZ5}}$ can be flexibly mapped to any EPWM module.
- Upon a fault condition, outputs EPWMxA and EPWMxB can be forced to one of the following:
  - High
  - Low
  - High-impedance
  - No action taken
- Support for one-shot trip (OSHT) for major short circuits or over-current conditions.
- Support for cycle-by-cycle tripping (CBC) for current limiting operation.
- Each trip-zone input pin can be allocated to either one-shot or cycle-by-cycle operation.
- Interrupt generation is possible on any trip-zone pin.
- Software-forced tripping is also supported.
- The trip-zone submodule can be fully bypassed if it is not required.

Note

For each EPWMx module, 6 tripzone input events are supported ($\overline{\mathrm{EPWMx\_TRIP\_TZ[5:0]}}$). Each tripzone input for all EPWMx modules are tied to a common tripzone input pin, so that any EPWMx can be triggered by any of the six tripzone inputs.

12.5.3.4.7.2 Controlling and Monitoring the EPWM Trip-Zone Submodule

The trip-zone submodule operation is controlled and monitored through the following registers:

Table 12-299. EPWM Trip-Zone Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_TZSEL	Trip-Zone Select Register (1)	24h	No
EPWM_TZCTL	Trip-Zone Control Register (1)	28h	No
EPWM_TZEINT	Trip-Zone Enable Interrupt Register (1)	2Ah	No
EPWM_TZFLG	Trip-Zone Flag Register (1)	2Ch	No
EPWM_TZCLR	Trip-Zone Clear Register (1)	2Eh	No
EPWM_TZFRC	Trip-Zone Force Register (1)	30h	No

(1) All trip-zone registers are EALLOW protected and can be modified only after executing the EALLOW instruction.

12.5.3.4.7.3 Operational Highlights for the EPWM Trip-Zone Submodule

The trip-zone signals at pin $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ is an active-low input signal. When the pin goes low, it indicates that a trip event has occurred. Each EPWM module can be individually configured to ignore or use each of the trip-zone pins. Which trip-zone pins are used by a particular EPWM module is determined by the EPWM_TZSEL register for that specific EPWM module. The trip-zone signal may or may not be synchronized to the system clock (FICLK). A minimum of 1 FICLK low pulse on the $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs is sufficient to trigger a fault condition in the EPWM module. The asynchronous trip makes sure that if clocks are missing for any reason, the outputs can still be tripped by a valid event present on the $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs.

The $\overline{\text{TZ0}}$ to $\overline{\text{TZ5}}$ inputs can be individually configured to provide either a cycle-by-cycle or one-shot trip event for a EPWM module. The configuration is determined by the EPWM_TZSEL[5-0] CBCk and EPWM_TZSEL[13-8] OSHTk bit field (where k = 0 to 5 corresponds to the trip pin), respectively.

- **Cycle-by-Cycle (CBC):** When a cycle-by-cycle trip event occurs, the action specified in the EPWM_TZCTL register is carried out immediately on the EPWMxA and/or EPWMxB output. Table 12-300 lists the possible actions. In addition, the cycle-by-cycle trip event flag (EPWM_TZFLG[1] CBC) is set and a EPWMxTZINT interrupt is generated if it is enabled in the EPWM_TZEINT register.

  The specified condition on the pins is automatically cleared when the EPWM time-base counter reaches zero (EPWM_TBCNT[15-0] TBCNT = 0000h) if the trip event is no longer present. Therefore, in this mode, the trip event is cleared or reset every PWM cycle. The EPWM_TZFLG[1] CBC flag bit will remain set until it is manually cleared by writing to the EPWM_TZCLR[1] CBC bit. If the cycle-by-cycle trip event is still present when the EPWM_TZFLG[1] CBC bit is cleared, then it will again be immediately set.
- **One-Shot (OSHT):** When a one-shot trip event occurs, the action specified in the EPWM_TZCTL register is carried out immediately on the EPWMxA and/or EPWMxB output. Table 12-300 lists the possible actions. In addition, the one-shot trip event flag (EPWM_TZFLG[2] OST) is set and a EPWMxTZINT interrupt is generated if it is enabled in the EPWM_TZEINT register. The one-shot trip condition must be cleared manually by writing to the EPWM_TZCLR[2] OST bit.

The action taken when a trip event occurs can be configured individually for each of the EPWM output pins by way of the EPWM_TZCTL[1-0] TZA and EPWM_TZCTL[3-2] TZB register bit field. One of four possible actions, shown in Table 12-300, can be taken on a trip event.

Table 12-300. Possible Actions On an EPWM Trip Event

EPWM_TZCTL[1-0] TZA and/or EPWM_TZCTL[3-2] TZB	EPWMxA and/or EPWMxB	Comment
0	High-Impedance	Tripped
1h	Force to High State	Tripped
2h	Force to Low State	Tripped
3h	No Change	Do Nothing. No change is made to the output.

Example of EPWM Trip-Zone Configurations

A one-shot trip event on $\overline{TZ0}$ pulls both EPWM1A, EPWM1B low and also forces EPWM2A and EPWM2B high.

- Configure the EPWM1 registers as follows:
  - EPWM_TZSEL[8] OSHT1 = 1: enables $\overline{TZ}$ as a one-shot event source for EPWM1
  - EPWM_TZCTL[1-0] TZA = 2: EPWM1A will be forced low on a trip event
  - EPWM_TZCTL[3-2] TZB = 2: EPWM1B will be forced low on a trip event
- Configure the EPWM2 registers as follows:
  - EPWM_TZSEL[8] OSHT1 = 1: enables $\overline{TZ}$ as a one-shot event source for EPWM2
  - EPWM_TZCTL[1-0] TZA = 1: EPWM2A will be forced high on a trip event
  - EPWM_TZCTL[3-2] TZB = 1: EPWM2B will be forced high on a trip event

12.5.3.4.7.4 Generating EPWM Trip-Event Interrupts

Figure 12-336 and Figure 12-337 illustrate the trip-zone submodule control and interrupt logic, respectively.

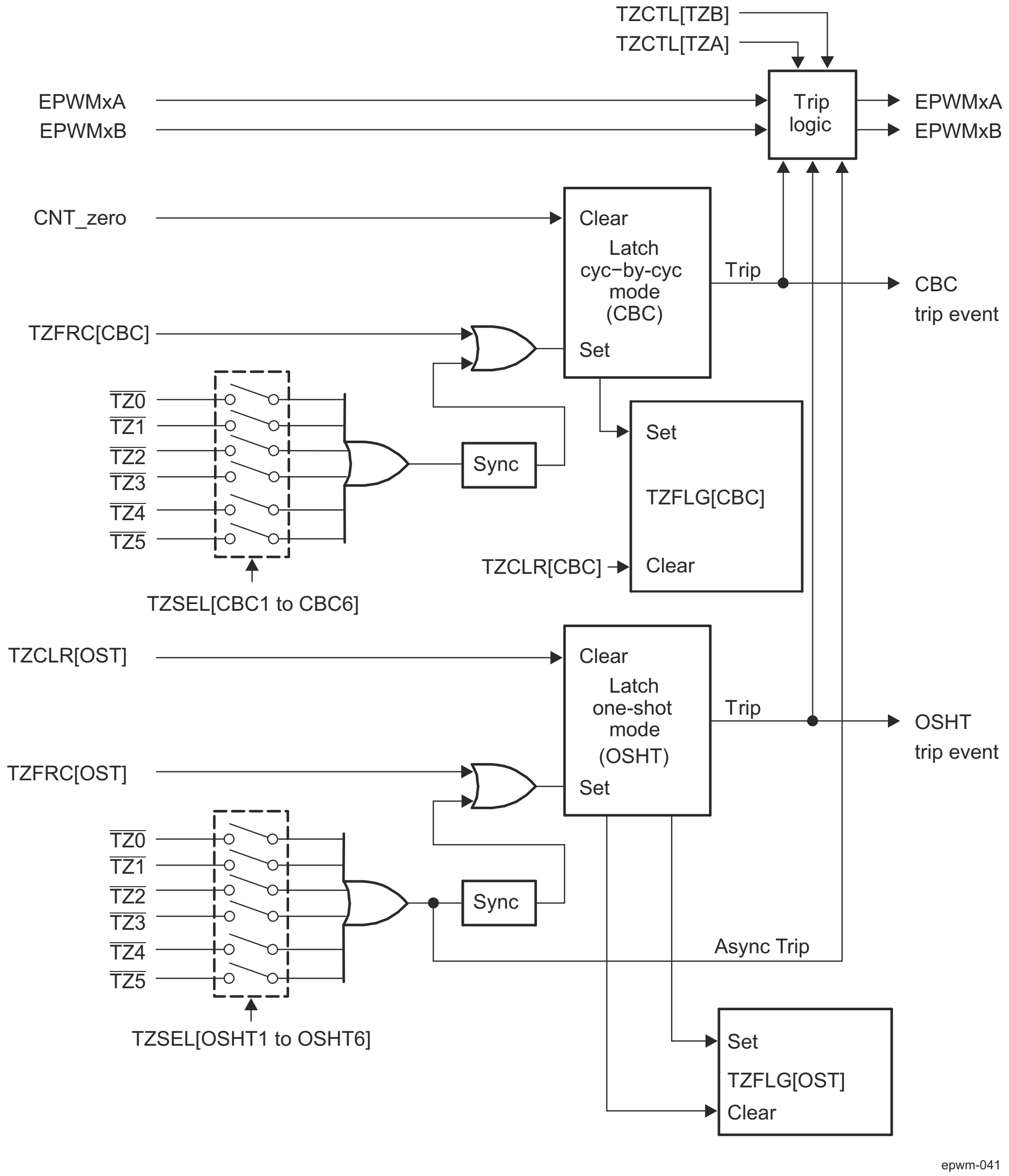


Figure 12-336. EPWM Trip-Zone Submodule Mode Control Logic

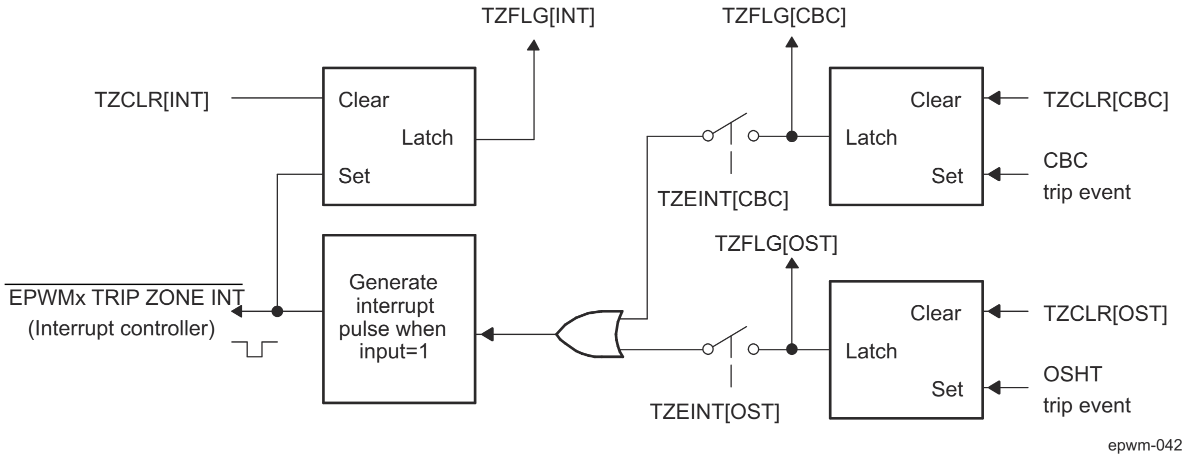


Figure 12-337. EPWM Trip-Zone Submodule Interrupt Logic

12.5.3.4.8 EPWM Event-Trigger (ET) Submodule

This section describes the Event-Trigger (ET) submodule in the PWM module.

12.5.3.4.8.1 Overview

Figure 12-338 shows the event-trigger (ET) submodule in the EPWM system. The event-trigger submodule manages the events generated by the time-base submodule and the counter-compare submodule to generate an aggregated interrupt request.

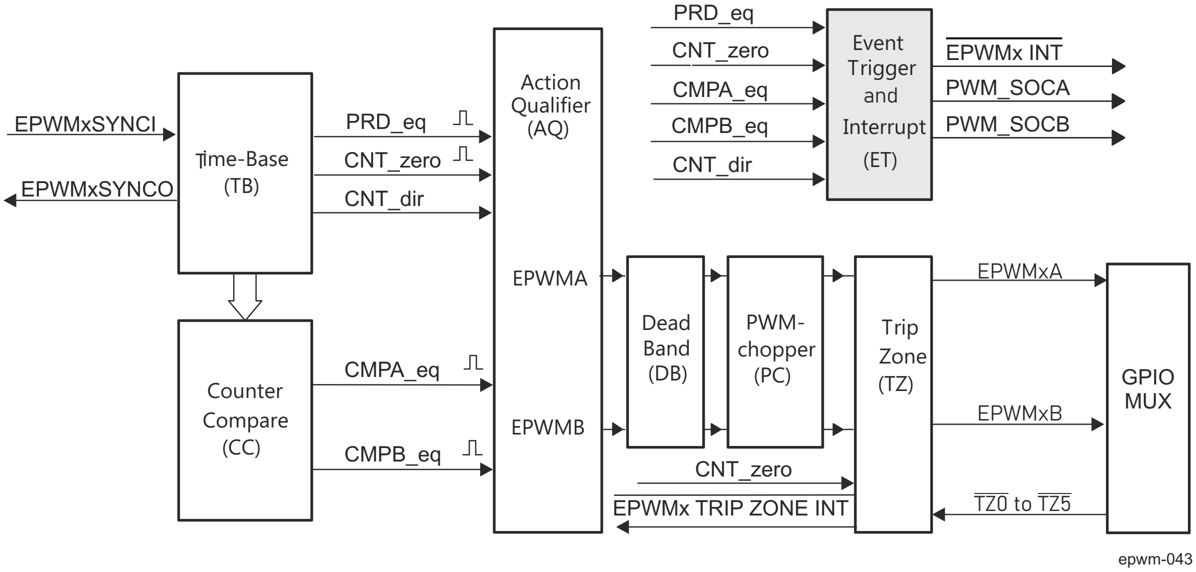


Figure 12-338. EPWM Event-Trigger Submodule

The key functions of the event-trigger submodule are:

- Receives event inputs generated by the time-base and counter-compare submodules
- Uses the time-base direction information for up/down event qualification
- Uses prescaling logic to issue interrupt requests at:
  - Every event
  - Every second event
  - Every third event
- Provides full visibility of event generation via event counters and flags

12.5.3.4.8.2 Controlling and Monitoring the EPWM Event-Trigger Submodule

The key registers used to configure the event-trigger submodule are shown in Table 12-301:

Table 12-301. EPWM Event-Trigger Submodule Registers

Acronym	Register Description	Address Offset	Shadowed
EPWM_ETSEL	Event-Trigger Selection Register	32h	No
EPWM_ETPS	Event-Trigger Prescale Register	34h	No
EPWM_ETFLG	Event-Trigger Flag Register	36h	No
EPWM_ETCLR	Event-Trigger Clear Register	38h	No
EPWM_ETFRC	Event-Trigger Force Register	3Ah	No

12.5.3.4.8.3 Operational Overview of the EPWM Event-Trigger Submodule

Each EPWM module has one interrupt request line as shown in Figure 12-339. Mapping interrupt lines to device host interrupt controllers is device specific and is covered in *EPWM Integration*.

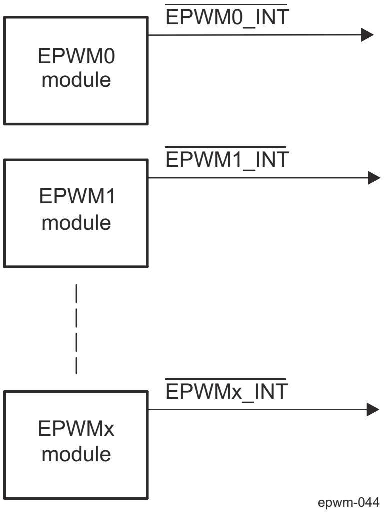


Figure 12-339. EPWM Event-Trigger Submodule Inter-Connectivity to Interrupt Controller

The event-trigger submodule monitors various event conditions (the left side inputs to event-trigger submodule shown in Figure 12-340) and can be configured to prescale these events before issuing an Interrupt request. The event-trigger prescaling logic can issue Interrupt requests at:

- Every event
- Every second event
- Every third event

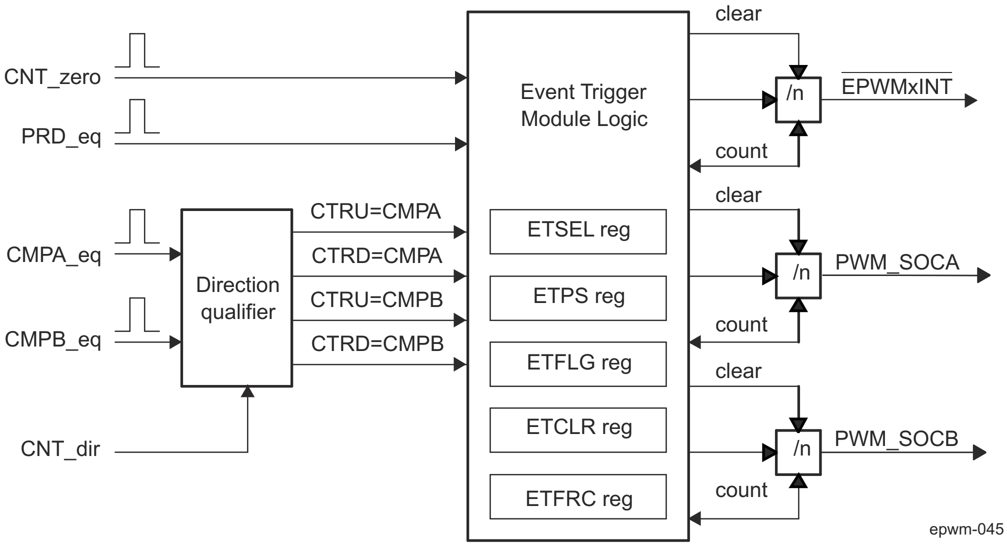


Figure 12-340. EPWM Event-Trigger Submodule Showing Event Inputs and Prescaled Outputs

- ETSEL — This selects which of the possible events will trigger an interrupt.
- ETPS — This programs the event prescaling options previously mentioned.
- ETFLG — These are flag bits indicating status of the selected and prescaled events.
- ETCLR — These bits allow to clear the flag bits in the EPWM_ETFLG register via software.
- ETFRC — These bits allow software forcing of an event. Useful for debugging or software intervention.

A more detailed look at how the various register bits interact with the Interrupt is shown in Figure 12-341.

Figure 12-341 shows the event-trigger's interrupt generation logic. The interrupt-period (EPWM_ETPS[1-0] INTPRD) bits specify the number of events required to cause an interrupt pulse to be generated. The choices available are:

- Do not generate an interrupt
- Generate an interrupt on every event
- Generate an interrupt on every second event
- Generate an interrupt on every third event

An interrupt cannot be generated on every fourth or more events.

Which event can cause an interrupt is configured by the interrupt selection (EPWM_ETSEL[2-0] INTSEL) bits. The event can be one of the following:

- Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h).
- Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD).
- Time-base counter equal to the compare A register (EPWM_CMPA) when the timer is incrementing.
- Time-base counter equal to the compare A register (EPWM_CMPA) when the timer is decrementing.
- Time-base counter equal to the compare B register (EPWM_CMPB) when the timer is incrementing.
- Time-base counter equal to the compare B register (EPWM_CMPB) when the timer is decrementing.

The number of events that have occurred can be read from the interrupt event counter (EPWM_ETPS[3-2] INTCNT) register bits. That is, when the specified event occurs the EPWM_ETPS[3-2] INTCNT bits are incremented until they reach the value specified by the EPWM_ETPS[1-0] INTPRD bit field. When EPWM_ETPS[3-2] INTCNT = EPWM_ETPS[1-0] INTPRD the counter stops counting and its output is set. The counter is only cleared when an interrupt is sent to the interrupt controller.

When EPWM_ETPS[3-2] INTCNT reaches EPWM_ETPS[1-0] INTPRD, one of the following behaviors will occur:

- If interrupts are enabled, EPWM_ETSEL[3] INTEN = 1h and the interrupt flag is clear, EPWM_ETFLG[0] INT = 0h, then an interrupt pulse is generated and the interrupt flag is set, EPWM_ETFLG[0] INT = 1h, and the event counter is cleared EPWM_ETPS[3-2] INTCNT = 0h. The counter will begin counting events again.
- If interrupts are disabled, EPWM_ETSEL[3] INTEN = 0h, or the interrupt flag is set, EPWM_ETFLG[0] INT = 1h, the counter stops counting events when it reaches the period value EPWM_ETPS[3-2] INTCNT = EPWM_ETPS[1-0] INTPRD.
- If interrupts are enabled, but the interrupt flag is already set, then the counter will hold its output high until the ENTFLG[0] INT flag is cleared. This allows for one interrupt to be pending while one is serviced.

Writing to the INTPRD bits will automatically clear the counter INTCNT = 0 and the counter output will be reset (so no interrupts are generated). Writing a 1h to the EPWM_ETFRC[0] INT bit will increment the event counter INTCNT. The counter will behave as described above when INTCNT = INTPRD. When INTPRD = 0h, the counter is disabled and hence no events will be detected and the EPWM_ETFRC[0] INT bit is also ignored.

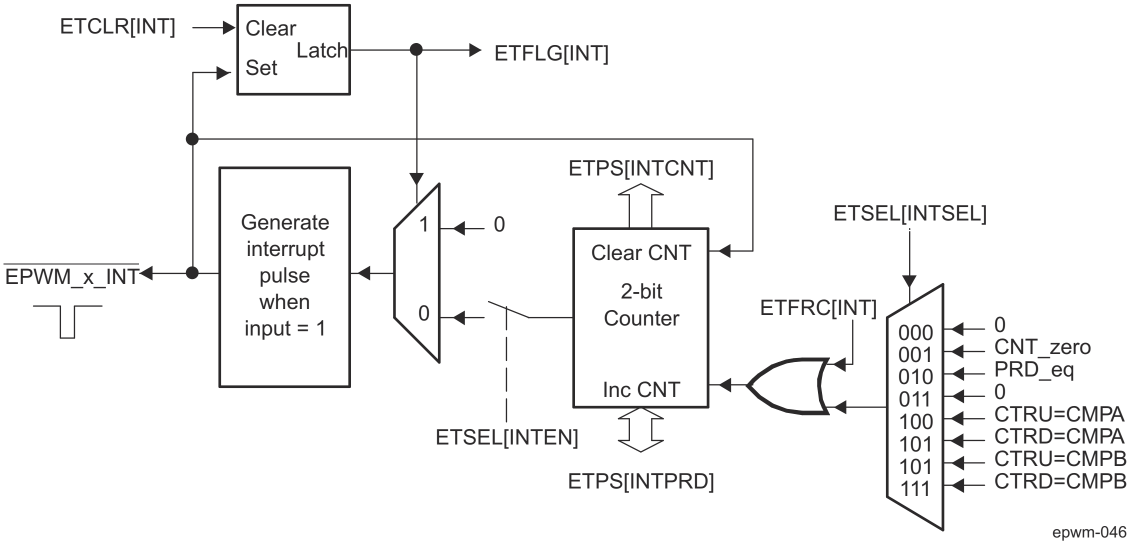


Figure 12-341. EPWM Event-Trigger Interrupt Generator

12.5.3.4.8.4 Operation Overview of the EPWM SOCx Pulse Generator

Figure 12-342 shows the operation of the event-trigger's start-of-conversion-A (SOCA) pulse generator. The EPWM_ETPS[11-10] SOCACNT counter and EPWM_ETPS[9-8] SOCAPRD period values behave similarly to the interrupt generator except that the pulses are continuously generated. That is, the pulse flag EPWM_ETFLG[2] SOCA is latched when a pulse is generated, but it does not stop further pulse generation. The enable/disable EPWM_ETSEL[11] SOCAEN bit stops pulse generation, but input events can still be counted until the period value is reached as with the interrupt generation logic. The event that will trigger an SOCA and SOCB pulse can be configured separately in the EPWM_ETSEL[10-8] SOCASEL and EPWM_ETSEL[14-12] SOCBSEL bit field. The possible events are the same events that can be specified for the interrupt generation logic.

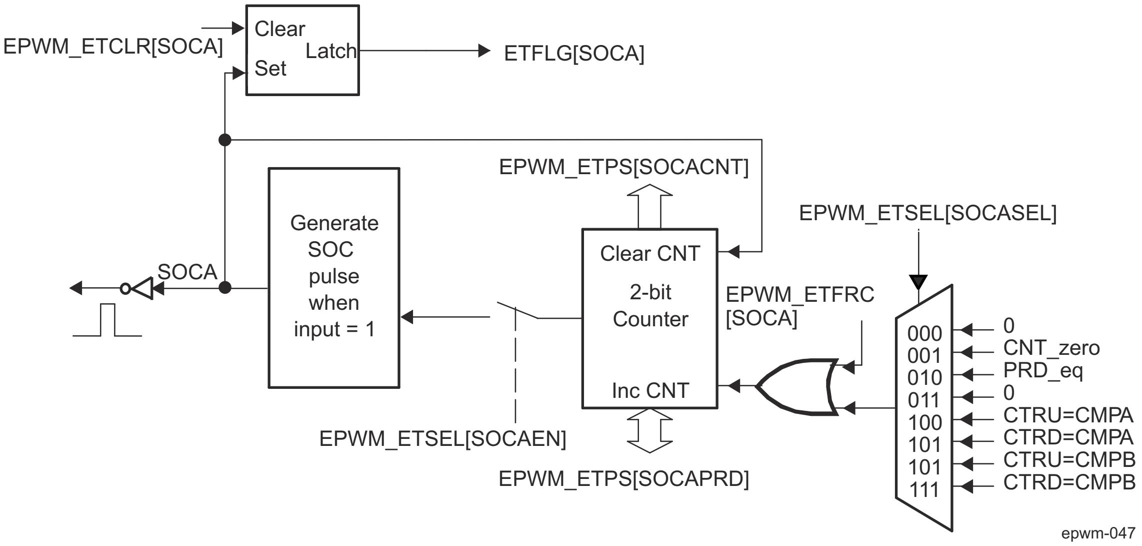


Figure 12-342. EPWM Event-Trigger SOCA Pulse Generator

Figure 12-343 shows the operation of the event-trigger's start-of-conversion-B (SOCB) pulse generator. The event-trigger's SOCB pulse generator operates the same way as the SOCA.

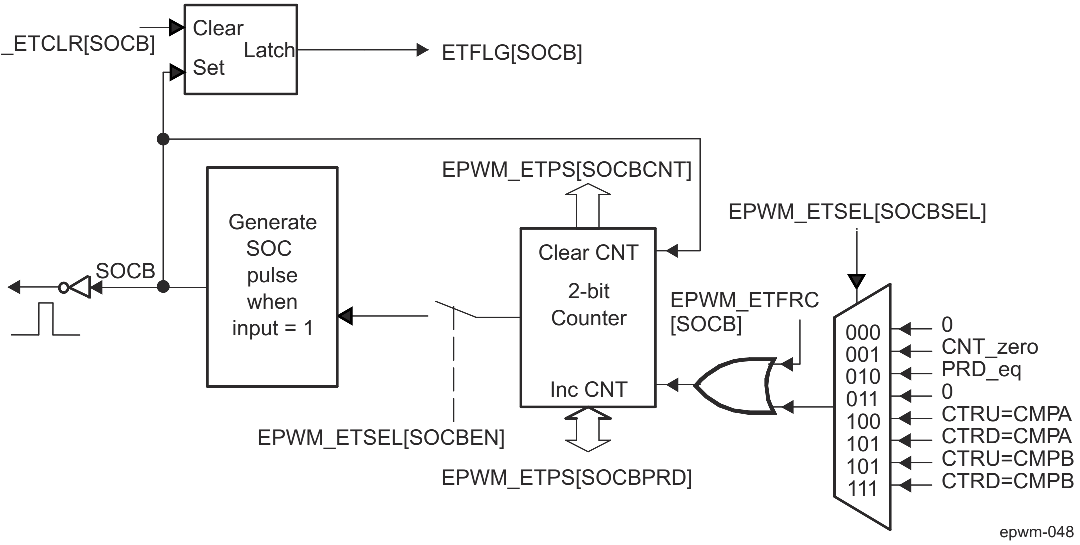


Figure 12-343. EPWM Event-Trigger SOCB Pulse Generator

12.5.3.4.9 EPWM Functional Register Groups

The Table 12-302 lists the groups of EPWM module registers according to their functionalities.

Table 12-302. EPWM Module Control and Status Registers Grouped by Submodule

Register Name	Offset	Size (×16)	Shadow	Register Description
		Time-Base (TB) Submodule Registers		
EPWM_TBCTL	0h	1	No	Time-Base Control Register
EPWM_TBSTS	2h	1	No	Time-Base Status Register
EPWM_TBPHS	6h	1	No	Time-Base Phase Register
EPWM_TBCNT	8h	1	No	Time-Base Counter Register
EPWM_TBPRD	Ah	1	Yes	Time-Base Period Register
		Counter-Compare (CC) Submodule Registers		
EPWM_CMPCTL	Eh	1	No	Counter-Compare Control Register
EPWM_CMPA	12h	1	Yes	Counter-Compare A Register
EPWM_CMPB	14h	1	Yes	Counter-Compare B Register
		Action-Qualifier (AQ) Submodule Registers		
EPWM_AQCTLA	16h	1	No	Action-Qualifier Control Register for Output A (EPWMxA)
EPWM_AQCTLB	18h	1	No	Action-Qualifier Control Register for Output B (EPWMxB)
EPWM_AQSFRC	1Ah	1	No	Action-Qualifier Software Force Register
EPWM_AQCSFRC	1Ch	1	Yes	Action-Qualifier Continuous S/W Force Register Set
		Dead-Band (DB) Generator Submodule Registers		
EPWM_DBCTL	1Eh	1	No	Dead-Band Generator Control Register
EPWM_DBRED	20h	1	No	Dead-Band Generator Rising Edge Delay Count Register
EPWM_DBFED	22h	1	No	Dead-Band Generator Falling Edge Delay Count Register
		Trip-Zone (TZ) Submodule Registers		
EPWM_TZSEL	24h	1	No	Trip-Zone Select Register(1)
EPWM_TZCTL	28h	1	No	Trip-Zone Control Register (1)
EPWM_TZEINT	2Ah	1	No	Trip-Zone Enable Interrupt Register (1)
EPWM_TZFLG	2Ch	1	No	Trip-Zone Flag Register (1)
EPWM_TZCLR	2Eh	1	No	Trip-Zone Clear Register (1)

Table 12-302. EPWM Module Control and Status Registers Grouped by Submodule (continued)

Register Name	Offset	Size (×16)	Shadow	Register Description
EPWM_TZFRC	30h	1	No	Trip-Zone Force Register (1)
		Event-Trigger (ET) Submodule Registers		
EPWM_ETSEL	32h	1	No	Event-Trigger Selection Register
EPWM_ETPS	34h	1	No	Event-Trigger Pre-Scale Register
EPWM_ETFLG	36h	1	No	Event-Trigger Flag Register
EPWM_ETCLR	38h	1	No	Event-Trigger Clear Register
EPWM_ETFRC	3Ah	1	No	Event-Trigger Force Register
		PWM-Chopper Submodule Registers		
EPWM_PCCTL	3Ch	1	No	PWM-Chopper Control Register

(1) EALLOW protected registers.

12.5.3.4.10 Proper EPWM Interrupt Initialization Procedure

When the EPWM peripheral clock is enabled it is possible that interrupt flags may be set due to spurious events as the EPWM registers not being properly initialized. The proper procedure for initializing the EPWM peripheral is:

1. Disable global interrupts (CPU INTM flag)
2. Disable EPWM interrupts
3. Initialize peripheral registers
4. Clear any spurious EPWM flags
5. Enable EPWM interrupts
6. Enable global interrupts

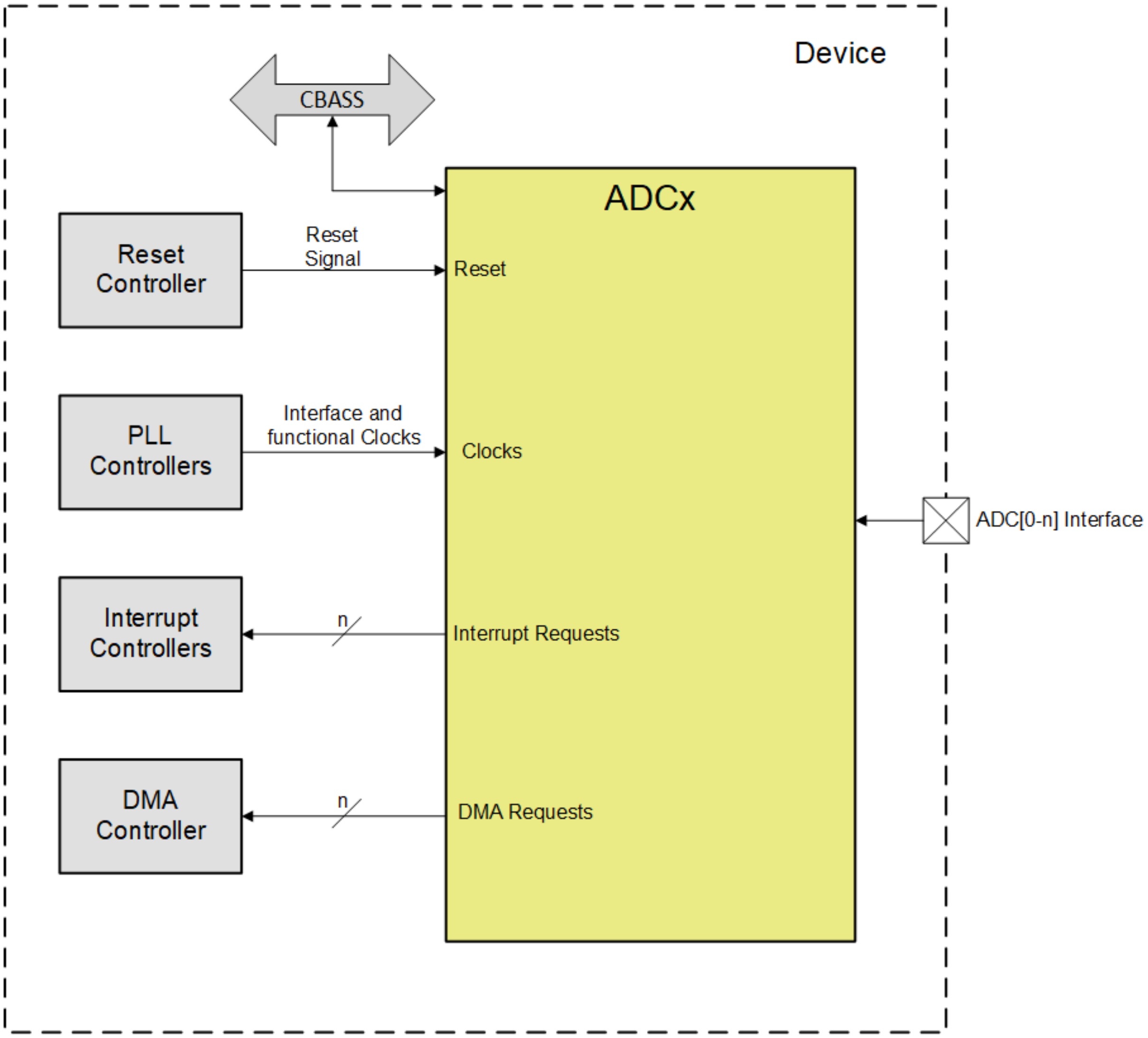
12.5.4 Analog-to-Digital Converter (ADC)

This chapter describes the Analog-to-Digital Converter (ADC) in the device.

12.5.4.1 ADC Overview

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels).

ADC Modules Overview presents an overview of the ADC modules.



A. x represents a valid instance of ADC in a domain. See the device data sheet for specifics.

B. n represents the maximum number of available ADC signals -1.

Figure 12-344. ADC Modules Overview

12.5.4.1.1 ADC Features

Each ADC module has the following features:

- 4 MSPS rate with a 60 MHz SMPL_CLK
- Single-ended or differential input options
- Programmable Finite State Machine (FSM) sequencer that supports the following:
  - Software initiated start of conversion
  - Optional hardware start of conversion (SOC), synchronized to external hardware event
  - Single conversion (one-shot mode)
  - Continuous conversions (continuous mode)
  - Sequence through all enabled steps based on a mask
  - Programmable open delay before executing each step
  - Programmable sampling delay for each step
  - Programmable averaging (16, 8, 4, 2, or 1) of input samples for each step
  - Store data in either of two FIFOs – 256-word × 16-bit
  - Option to encode input (channel) number with data

  - Support for servicing FIFOs via DMA or processor
  - Programmable DMA request event (for each FIFO)
- Support for the following interrupts and status, with masking:
  - Interrupt if AFE fails to return end of conversion (EOC)
  - Interrupt after a sequence of conversions (all non-masked steps)
  - Interrupt for FIFO threshold levels
  - Interrupt if sampled data is out of a programmable range
  - Interrupt for FIFO overflow and underflow conditions
  - Status bit to indicate if ADC is busy converting

Unsupported Features:

- See the Module Integration section of this document for a list of module features not supported by the integration on this Device.

12.5.4.2 ADC Environment

This section describes the ADC external connections (environment).

Table 12-303 describes the ADC I/O signals.

Table 12-303. ADC I/O Signals

Module Pin	I/O[1]	Description
AIN0	A/I	Analog input 0
AIN1	A/I	Analog input 1
AIN2	A/I	Analog input 2
AIN3	A/I	Analog input 3
AIN4	A/I	Analog input 4
AIN5	A/I	Analog input 5
AIN6	A/I	Analog input 6
AIN7	A/I	Analog input 7
REFN	A	ADC Reference (Negative)
REFP	A	ADC Reference (Positive)

(1) I = Input; A = Analog

12.5.4.3 ADC Functional Description

12.5.4.3.1 ADC FSM Sequencer Functional Description

The FSM sequencer supports up to 16 steps that can be configured to perform analog-to-digital conversions. Each of the 16 steps can individually be enabled and configured to operate as software enabled steps or hardware enabled steps. Each step has its own programmable step configuration (ADC_CONFIG_j) and step delay (ADC_DELAY_j) registers that allow users to configure the ADC operation on a per-step basis.

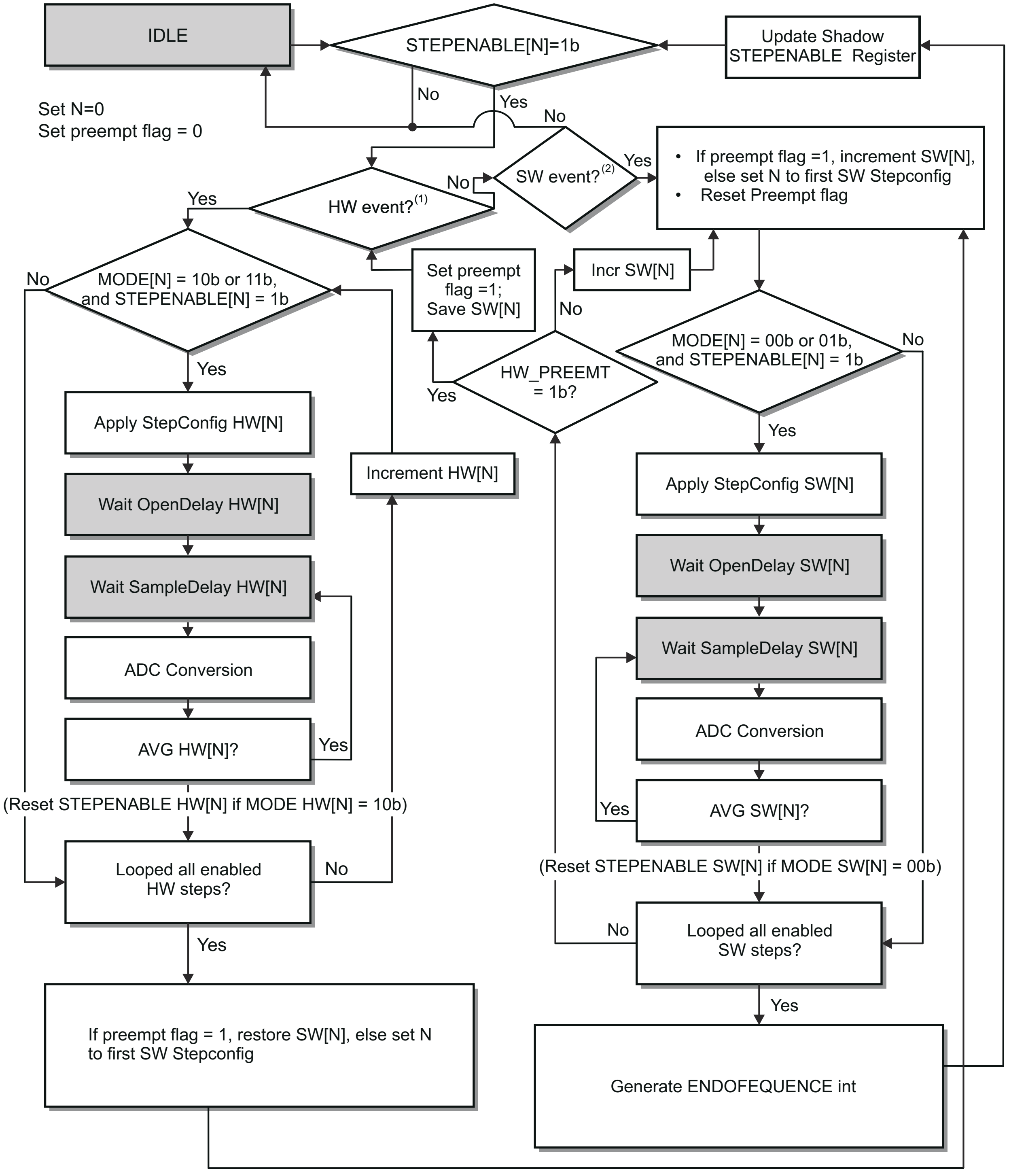
The FSM sequencer enters Idle immediately after the ADC is enabled and remains in Idle while waiting for any of the 16 programmable steps to be enabled. When one or more step is enabled, the FSM sequencer will begin executing or skipping each step starting with the lowest and incrementing up through each step until the highest step has been executed or skipped. The FSM sequencer will execute enabled steps and skip disabled steps. Once all of the steps have been executed or skipped, the FSM sequencer will return to Idle or immediately begin repeating steps configured for continuous mode.

An ENDOFEQUENCE interrupt can be generated after the last enabled step has been executed. If any software enabled steps are configured for continuous operation and they are still enabled when the FSM sequencer has incremented through all the steps, the FSM sequencer will start the sequence again with the first enabled step. Hardware enabled steps are mapped to a hardware event and will need the hardware event to occur before being scheduled.

Figure 12-345 illustrates how the FSM sequencer works. Each shaded box represents a FSM state.

Note

Figure 12-345 does not represent the number of SMPL_CLK cycles required by each state since some states implement user programmable delays that may require more than one SMPL_CLK cycle to complete.



(1) MODE[N] = 10b or 11b, STEPENABLE[N] = 1b, and HW Event = 1

(2) MODE[N] = 00b or 01b and STEPENABLE[N] = 1b

Figure 12-345. Sequencer FSM

12.5.4.3.1.1 Step Enable

A step is enabled or disabled via the ADC_STEPENABLE register. The system software should only write to the ADC_STEPENABLE register when the ADC is disabled or the FSM sequencer is idle. Therefore, it may be necessary to disable the ADC before updating the ADC_STEPENABLE register if the FSM sequencer is executing back-to-back steps where it never enters idle.

12.5.4.3.1.2 Step Configuration

12.5.4.3.1.2.1 One-Shot (Single) or Continuous Mode

Each step can be configured to operate in one-shot or continuous mode via the least significant bit of the MODE bit-field of the respective ADC_CONFIG_j register. Steps configured for one-shot mode will perform a single conversion before being disabled by the FSM sequencer. Steps configured for continuous mode will automatically be re-enabled by the FSM sequencer after each conversion until disabled by software.

12.5.4.3.1.2.2 Software- or Hardware-Enabled Steps

Each step can be configured to operate in SW Enabled mode or HW Enabled mode independently via the most significant bit of the MODE bit-field in the respective ADC_CONFIG_j register. However, the hardware event source is applied globally to all HW Enabled steps and configured via the ADC_CONTROL register.

The user can configure each step to begin immediately after the step is enabled by software (SW Enabled), or wait for a hardware event to occur (HW Enabled).

The EXT_TRIGGER input signal is used by HW Enabled steps. The trigger input has the option of being sourced from a device input pin or several on-device peripherals via a multiplexer controlled by TRIG_SEL of the respective registers:

- ADCi_CTRL where i represents a ADC instance see the device datas heet for available domains and ADC instances.
- MCU_ADCi_CTRL where i represents a ADC instance see the device data sheet for available domains and ADC instances.

When this option is selected, the hardware event will be triggered after the EXT_TRIGGER input signal transitions from low to high and is held high for a period greater than two cycles of SYS_CLK. This hardware event will only schedule one complete sequence, even for continuous mode. If HW Enabled steps need to be executed again, a new hardware event must be generated after the previously triggered sequence has completed.

SW Enabled steps can be preempted by HW Enabled steps when the HW_PREEMPT bit in the ADC_CONTROL register is set.

12.5.4.3.1.2.3 Averaging of Samples

Each step can be configured, via the respective ADC_CONFIG_j register, to sample an input 1, 2, 4, 8, or 16 times and provide an average data value. If a step is configured to sample more than once, the additional samples are taken back-to-back immediately after the first sample. However, open delay is only applied to the first sample while sample delay is applied to all samples. Once the last sample has been taken the average data value will be stored in the FIFO.

12.5.4.3.1.2.4 Analog Multiplexer Input Select

The AFE contains two 9-to-1 analog multiplexers which are used to select the source connected to the positive input (INP) and negative input (INM) of the ADC. Each step can be configured, via the respective ADC_CONFIG_j register, to select the appropriate input sources. For more information, refer to the functional block diagram and the ADC_CONFIG_j register field descriptions.

12.5.4.3.1.2.5 Differential Control

The ADC supports differential inputs and each step can be configured, via the respective ADC_CONFIG_j register, to select single-ended input mode or differential input mode.

Note

The ADC INM input must be sourced from REFN for any steps configured to operate in single-ended mode.

12.5.4.3.1.2.6 FIFO Select

The ADC contains two FIFOs and each step can be configured, via the respective ADC_CONFIG_j register, to store its ADC data into either FIFO.

12.5.4.3.1.2.7 Range Check Interrupt Enable

Each step can be configured, via the respective ADC_CONFIG_j register, to compare the value of ADC data to high and low limits programmed in the ADC_RANGE register. The out-of-range interrupt is generated if the value of ADC data is greater than the value of HIRANGE or less than the value of LOWRANGE. Refer to the ADC_RANGE register field descriptions for information related to setting the high and low limits that trigger an out-of-range interrupt.

12.5.4.3.1.3 Open Delay and Sample Delay

The FSM sequencer provides two programmable delays for each step. The value of OPENDELAY is used to control when the acquisition begins after the step starts and the value of SAMPLEDELAY is used to control the acquisition period. Delays for each of the 16 steps can be configured independently via the respective ADC_DELAY_j register.

12.5.4.3.1.3.1 Open Delay

OPENDELAY defaults to a value of zero which causes the acquisition period to begin as soon as the step starts. The start of the acquisition period can be delayed one SMPL_CLK clock period for each incremental value of OPENDELAY.

12.5.4.3.1.3.2 Sample Delay

SAMPLEDELAY defaults to a value of zero which causes the acquisition period to be equal to two SMPL_CLK clock periods. The acquisition period can be extended one SMPL_CLK clock for each incremental value of SAMPLEDELAY.

The value of SAMPLEDELAY should be configured to provide enough time for the respective external voltage source to completely charge the AFE input capacitance during the acquisition period.

12.5.4.3.1.4 Interrupts

The ADC has 9 internal events that can trigger an interrupt to the processor. These events are logically or'ed together to produce a single interrupt to the processor. The user can individually enable or disable each interrupt source via the ADC_ENABLE_SET and ADC_ENABLE_CLR registers. Once an interrupt is generated, the ADC_STATUS register can be read to determine which interrupt source(s) interrupted the processor. The interrupt source(s) can be cleared by writing a ‘1’ to the corresponding bit of the ADC_STATUS register.

The following interrupts are supported by the device ADC:

- An ENDOFEQUENCE interrupt is generated after the FSM sequencer completes the last enabled step.
- FIFO0UNFL/FIFO1UNFL or FIFO0OVFL/FIFO1OVFL interrupts. Each FIFO also has the ability to generate overrun and underflow interrupts. The ADC does not recover from overrun or underflow conditions automatically. Therefore, software will need to disable and re-enable the ADC after this occurs. The FSM sequencer must be Idle before turning the ADC module back on. This can be confirmed by reading the ADC_SEQUENCER_STAT register, when FSM_BUSY = 0x0 and STEP_IDLE = 0x10000.
- FIFO0THRS and FIFO1THRS interrupts. Each FIFO has the ability to generate an interrupt when the FIFO word count has reached a programmable threshold value. The FIFO0THRS and FIFO1THRS interrupt is generated when the value of NUMWDS in the respective ADC_FIFO0WC or ADC_FIFO1WC register equals the word count threshold value programmed in THRESHOLD of the respective ADC_FIFO0THRESHOLD or ADC_FIFO1THRESHOLD register.
- OUTOFRANGE interrupt. This interrupt can be enabled or disabled on each step. If enabled, the ADC data value is compared to the low and high thresholds programmed in the global ADC_RANGE register. The OUTOFRANGE interrupt is generated if the ADC data value is greater than the value programmed in HIRANGE or less than the value programmed in LOWRANGE.
- AFE_EOC_MISSING interrupt. This interrupt is generated when the FSM sequencer does not receive an expected EOC from the AFE.

12.5.4.3.1.5 Power Management

The software also has the option to turn off the AFE power by writing to the ADC_CONTROL[4] PD bit. By default, after the initial power on the AFE is powered down and software is responsible for turning it on. Software must wait minimum 4 µs after a AFE power up and before starting a conversion (must be followed every time the AFE is powered up). It is the software's responsibility to empty the FIFO before requesting the ADC to enter sleep state.

12.5.4.3.1.6 DMA Requests

Each FIFO can be serviced by the processor or DMA. The user can individually enable or disable each FIFO DMA request via the ADC_DMAENABLE_SET and ADC_DMAENABLE_CLR registers.

12.5.4.3.2 ADC AFE Functional Description

The AFE contains a single 10-bit successive approximation ADC which can be connected to one of eight user selectable analog inputs for each step executed by the FSM sequencer. There is also an option to configure the ADC to operate in differential mode where it samples the differential voltage applied to two of eight user selectable analog inputs.

The ADC sits idle until the FSM sequencer sends a Start of Conversion (SOC) pulse. Once the FSM sequencer sends a SOC pulse to the ADC, it begins sampling the analog input signal on the rising edge of SOC and continues sampling the analog input signal one cycle of SMPL_CLK after the falling edge of SOC. The SOC pulse width will be the value of SAMPLEDELAY plus one SMPL_CLK periods, so the total ADC acquisition time will be the value of SAMPLEDELAY plus two SMPL_CLK periods. The ADC captures the analog input signal at the end of the acquisition period and starts conversion, which requires thirteen SMPL_CLK periods to digitize the sampled input. An EOC signal is returned to the FSM sequencer to indicate the digital data is ready.

The ADC output is positive binary weighted data ranging from 0 to (2^{10} - 1). When configured for single-ended mode, ADC output data values 0 to (2^{10} - 1) represents a corresponding input voltage that ranges from the ADC negative reference (REFN) voltage to the ADC positive reference (REFP) voltage. When configured for differential mode, ADC output data values 0 to ((2^{10}/2) - 1) represents a corresponding negative differential input voltage that ranges from the REFP voltage to the REFN voltage and output data values (2^{10}/2) to (2^{10} - 1) represents a corresponding positive differential input voltage that ranges from the REFN voltage to the REFP voltage.

Using the minimum values of OPENDELAY and SAMPLEDELAY, the ADC can sample an analog input every 15 SMPL_CLK periods.

Example Timing Diagram for Sequencer illustrates the operation of the FSM sequencer and ADC AFE, with indicators showing when the hardware configuration defined by ADC_CONFIG_j and ADC_DELAY_j registers are applied.

Note

Example Timing Diagram for Sequencer assumes both steps shown are software enabled with averaging turned off, an OPENDELAY value of 1, and SAMPLEDELAY value of 0. The analog input is sampled for the duration of the SOC pulse plus one cycle of the SMPL_CLK. If the value of OPENDELAY were 0, it would appear as if the time associated with the Open portion of the FSM waveform would be removed from all the waveforms.

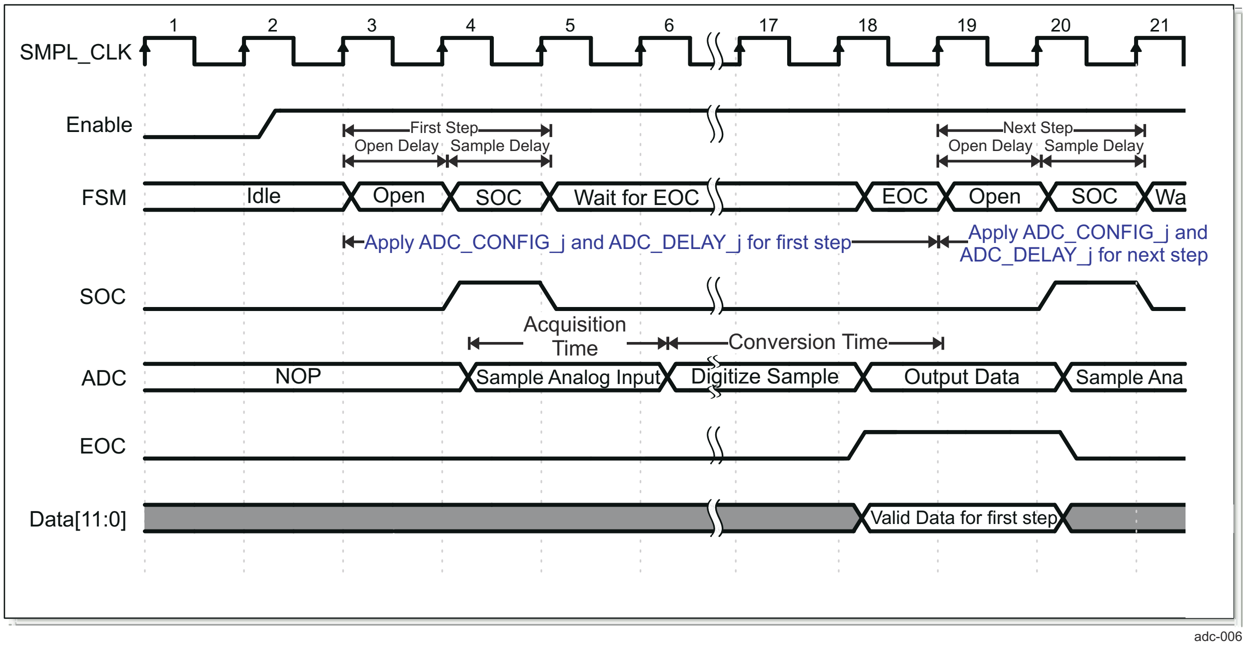


Figure 12-346. Example Timing Diagram for Sequencer

12.5.4.3.2.1 AFE Functional Block Diagram

The AFE has 8 analog inputs which can be configured as either singled-ended or differential inputs to the ADC. The user may configure a step to use any 1 of the 8 inputs when operating in single-ended mode or any 2 of the 8 inputs when operating in differential mode. For more information, refer to Figure 12-347 and the ADC_CONFIG_j register field descriptions.

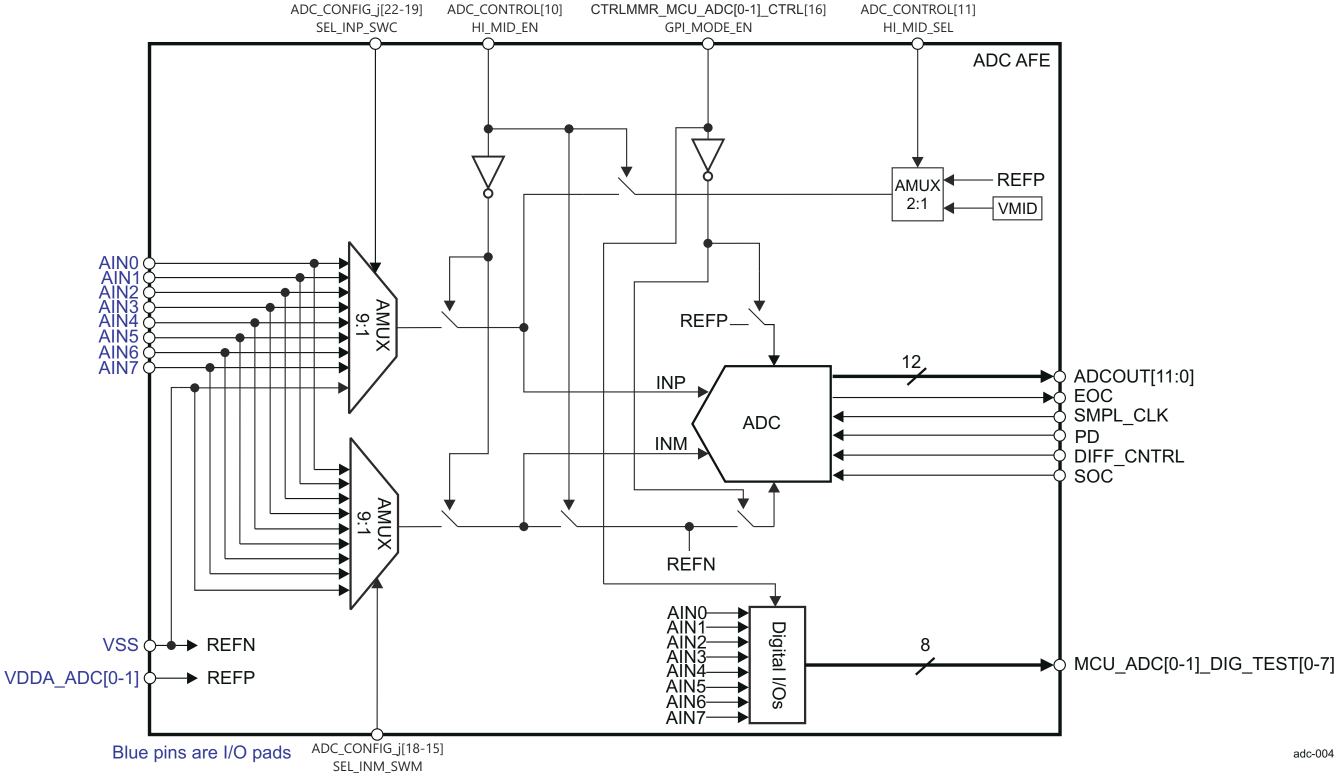
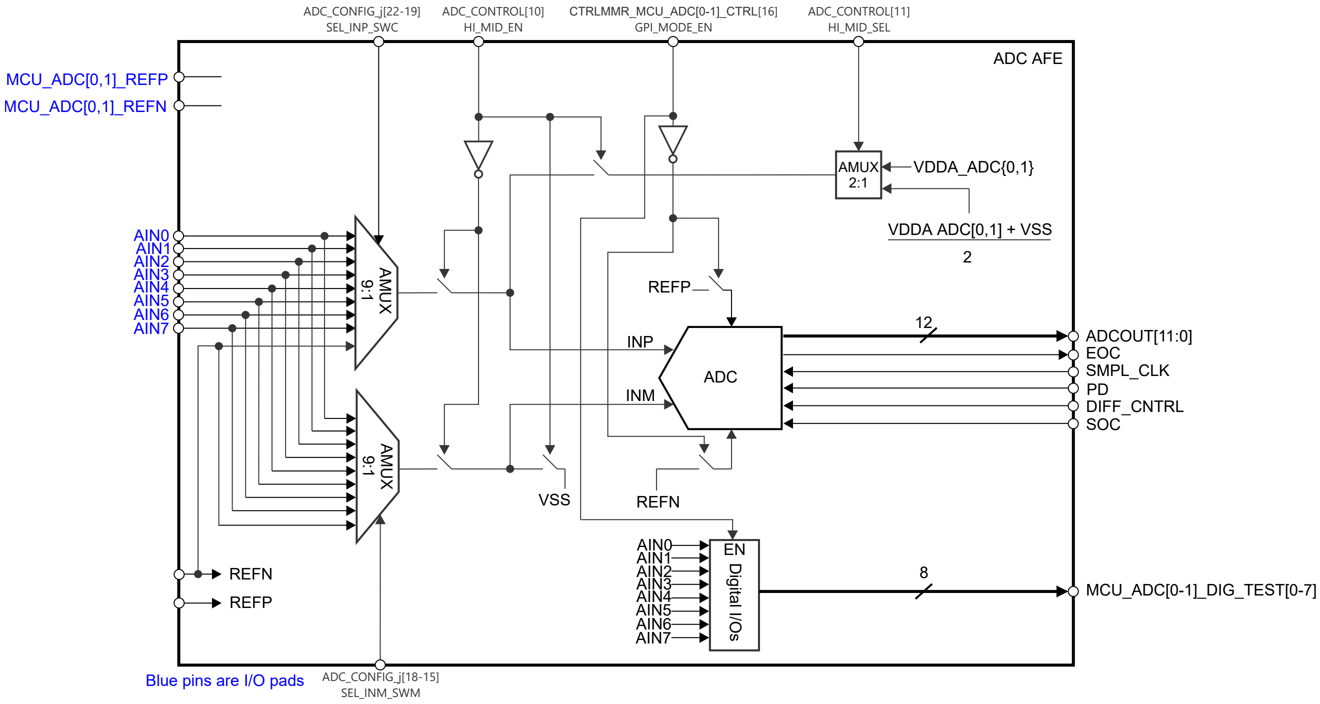


Figure 12-347. Functional Block Diagram



for switch control: 0 is open

MCU_ADC[0-1]_REFP is connected to VDDA_ADC[0-1] unless otherwise noted in the module integration section;
and MCU_ADC[0-1]_REFN is connected to VSS unless otherwise noted in the module integration section

12.5.4.3.3 ADC FIFOs and DMA

12.5.4.3.3.1 FIFOs

There are two sample FIFOs (ADC_FIFO0 and ADC_FIFO1), which store sample data from the AFE. Can be configured, via the respective ADC_CONFIG_j register.

The processor can read ADC data directly from the FIFO by using the respective ADC_FIFO0DATA or ADC_FIFO1DATA register. The internal logic will pop the next data from the FIFO and increment the FIFO read pointers.

The FIFO data will no longer be accessible after the ADC is disabled because the FIFO pointers are reset. Therefore, it is important to read all FIFO data before disabling the ADC.

12.5.4.3.3.2 DMA

The ADC has a dedicated slave port for the DMA which allows it to perform continuous burst reads when accessing the FIFOs.

Each FIFO has its own DMA request which can be enabled via the ADC_DMAENABLE_SET register and disabled via the ADC_DMAENABLE_CLR register.

The first DMA request is generated after the FIFO leaves the EMPTY state and fills to the level programmed in DMAREQLEVEL of the respective ADC_FIFO0DMAREQ or ADC_FIFO1DMAREQ register.

Subsequently, a new DMA request is automatically generated on the next clock cycle after the current DMA access completes if the previous DMA access did not empty the FIFO.

12.5.4.3.4 ADC Error Correcting Code (ECC)

The Error Correcting Code (ECC) is a mechanism for providing increased system reliability (via reduction of memory soft errors) by allowing single bit errors to be detected and corrected and double bit errors to be detected.

The ECC Aggregator provides a single EOI-handshake based interrupt to the host (for both single and double error detections).

The ECC Aggregator will write 0's to all of memory after reset is released. The ADC_SEQUENCER_STAT[6] MEM_INIT_DONE bit will be 0 during this period and will be set to 1 upon completion.

For more information about the ECC Aggregator, see *ECC Aggregator* and *ADC ECC Registers*.

See also *Testing ECC Error Injection* and *ADC ECC Registers*.

12.5.4.3.4.1 Testing ECC Error Injection

The read enable (REN) input to the RAMs instantiated in this module are constantly tied to 1'b1. As a result, read is continuously in progress.

In order to test ECC single error injection on a particular RAM row, the following conditions have to be maintained before setting the ADC_ECC_CTRL[3] FORCE_SEC bit:

- ADC_ECC_CTRL[5] FORCE_N_ROW bit has to be clear. This is required in order to configure required row in
- ADC_ECC_CTRL[6] ERROR_ONCE bit has to be clear. If this bit is set, the ECC error occurs immediately after setting ADC_ECC_CTRL[3] FORCE_SEC bit since REN is always set
- ADC_ECC_ERR_CTRL1[31-0] ECC_ROW bit field has to be point to the required row address

12.5.4.3.5 ADC Functional Debug Mode

The ADC function can be validated by measuring known reference voltage sources. This feature provides register control that connects the AFE to known reference voltage sources. However, it does not automatically configure the FSM to perform conversions to measure these sources. Software will need to configure the FSM to perform a measurement after selecting this mode of operation.

ADC_CONTROL[10] HI_MID_EN is used to disconnect the AFE from all analog inputs and connect it to one of two known reference voltage sources. ADC_CONTROL[11] HI_MID_SEL is used to select REFP or VMID as the known reference voltage source.

The conversion results is expected to produce a full scale value when the AFE is connected to REFP and approximate half scale value when the AFE is connected to VMID.

The steps are:

- Disable the ADC if previously enabled and wait until the FSM is not busy.
- Put the AFE in a functional debug mode by setting the ADC_CONTROL[10] HI_MID_EN bit to 1.
- Select one of the two reference voltage sources by setting the ADC_CONTROL[11] HI_MID_SEL bit.
  - 0 selects VMID
  - 1 selects REFP
- Configure the FSM to measure the selected reference voltage source.
- Enable the ADC and evaluate the results.
- When debug is complete, disable the ADC and wait until the FSM is not busy, re-program the FSM for functional operation, then re-enable the ADC.

12.5.4.4 ADC Programming Guide

12.5.4.4.1 ADC Low-Level Programming Models

12.5.4.4.1.1 During Operation

Table 12-304. Turn-Off

Step	Register/Bit Field/Programming Model	Value
Turn off ADC module enable bit when finished. This will stop the ADC after the current step is complete.	ADC_CONTROL[0] MODULE_ENABLE	0

Table 12-305. Turn-On After Turn-Off

Step	Register/Bit Field/Programming Model	Value
Enable the ADC module enable bit	ADC_CONTROL[0] MODULE_ENABLE	1

12.6 Timer Modules

This section describes the timer modules in the device.

12.6.1 Global Timebase Counter (GTC)

This section describes the global timebase counter (GTC) in the device.

12.6.1.1 GTC Overview

The GTC module provides a continuous running counter that can be used for time synchronization and debug trace time stamping.

12.6.1.1.1 GTC Features

The GTC supports the following features:

- 64-bit up counter
- No rollover during the lifetime of the device
- Compatible with ARMv8 system counter requirements:
  - Disabled at power-up
  - Register definition and memory map aligned to ARMv8 definition
  - Implements memory-mapped counter control and status frames
- Outputs reflected binary (Gray) encoded timer value for system timer bus distribution to other modules
- Selectable counter bit output as a push event that can be used by CPTS modules, timers or interface protocols

12.6.1.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.6.1.2 GTC Functional Description

12.6.1.2.1 GTC Block Diagram

The GTC is essentially comprised of a 64-bit up counter, a Gray encoder, a 64-bit multiplexer, and memory-mapped control registers. Figure 12-348 shows a high-level block diagram of the GTC.

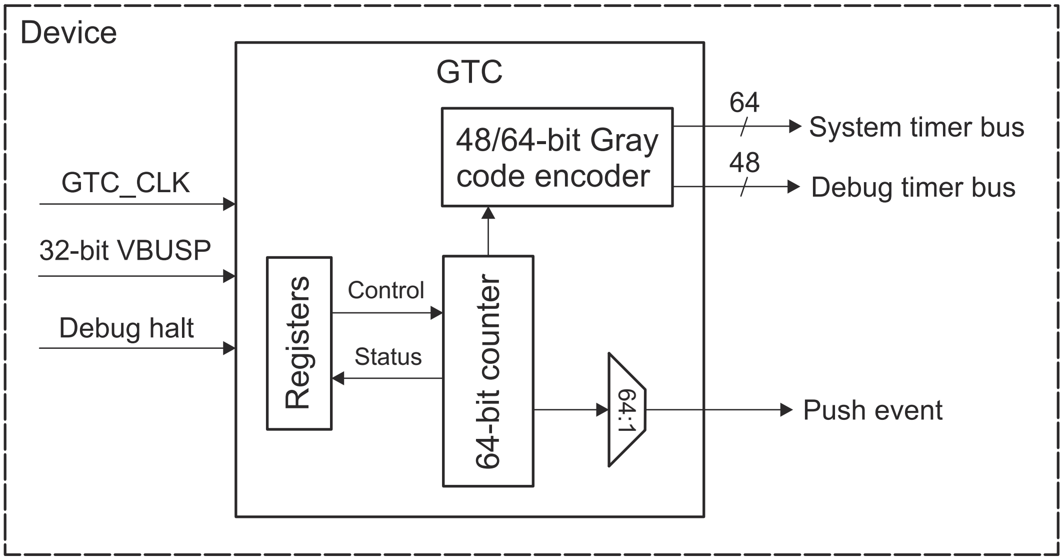


Figure 12-348. GTC Block Diagram

12.6.1.2.2 GTC Counter

The counter is a 64-bit binary up counter that increments on every GTC_CLK rising edge. The source for GTC_CLK is selected through a mux which is controlled via the GTC_CLKSEL[2-0] register bit field.

The counter is disabled by default (at power-on-reset) and increments only when enabled by setting the *GTC_CFG1_CNTCR*[0] EN bit to '1'. The current counter value is readable via the combined COUNTVALUE bit field of both *GTC_CFG1_CNTCV_HI* (upper 32 bits) and *GTC_CFG1_CNTCV_LO* (lower 32 bits) registers.

When counting is disabled, a new counter value can be loaded via a software write to the combined COUNTVALUE bit field. In this case, when the counter gets re-enabled, it will start counting from the last value written to this field.

The counter can be optionally configured to stop incrementing when a debug halt signal is issued, by writing a '1' to the *GTC_CFG1_CNTCR*[1] HDBG bit. This condition is indicated through the *GTC_CFG1_CNTSR*[1] DBGH status bit.

12.6.1.2.2.1 Steps to Clear the Counter Value to Zero

1. Disable the GTC
2. Clear GTC_CNTCV_LO (First)
3. Clear GTC_CNTCV_HI (Second)
4. Enable the GTC

Once the GTC is enabled, the GTC_CNTCV_HI bit will be cleared to zero.

12.6.1.2.3 GTC Register Partitioning

The ARMv8 architecture spec requires specific system-level components, each with one or two register frames. To accommodate this, the GTC memory-mapped registers (MMRs) are divided into four separate regions (4KB each):

- Peripheral MMRs (GTC0_GTC_CFG0): This region includes standard peripheral identification registers and any other control registers not associated with the ARMv8 system timer functions.
- Counter control MMRs (GTC0_GTC_CFG1): This region includes registers that provide control over the operation of the system timer.

- Counter status MMRs (GTC0_GTC_CFG2): This region includes registers that provide a mechanism for reading the status of the system timer.
- Timer control MMRs (GTC0_GTC_CFG3): This region includes registers that identify and provide a control mechanism for memory-mapped timer implementations. For this device, no memory-mapped timers are implemented and only the minimum registers required to indicate the presence of no timers are necessary.

12.6.2 RTI-Windowed Watchdog Timer (WWDT)

This section describes the Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module in the device.

CAUTION

The RTI module shall be used to serve only as a Digital Windowed Watchdog (DWWD).

The Real Time Interrupt module provides timer functionality for operating systems and for benchmarking code. The module incorporates several counters, which define the timebases needed for scheduling in the operating system.

This module is specifically designed to fulfill the requirements for OSEK (“Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug”; “Open Systems and the Corresponding Interfaces for Automotive Electronics”) as well as OSEK/Time compliant operating systems.

The timers also provide the ability to benchmark certain areas of code by reading the counter contents at the beginning and the end of the desired code range and calculating the difference between the values.

12.6.2.1 RTI Features

The RTI modules include the following main features:

- Windowed Watchdog Timer (WWDT) feature.
- Two independent 64 bit counter blocks (counter block0 or counter block1). Each block consists of
  - One 32 bit up counter
  - One 32 bit free running counter
  - Two capture registers for capturing the prescale and free running counter on a special event.
- Free running counter 0 can be incremented by either the internal prescale counter or by an external event.
- Four configurable compare registers for generating operating system ticks . Each event can be driven by either counter block0 or counter block1.
- Fast enabling/disabling of events.
- RTI clock input derived from any of the available clock sources, selectable in the System Module
- Optional capability to drive a pulse-width modulated signal out on an interrupt line.

12.6.2.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.6.2.3 RTI Functional Description

The MCU_RTI0 and RTI modules are hereinafter referred to as RTI module.

12.6.2.3.1 RTI Digital Windowed Watchdog

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Note

Digital windowed watchdog (DWWD) timer is implemented using the digital windowed watchdog function of the RTI modules. Real time interrupt functionality is not supported. In this mode, the timer should default to disabled and user can adjust the period as desired before enabling the watchdog.

In addition to the time-out boundary configurable via the digital watchdog (DWD), some applications may also want to configure the start-time boundary of the watchdog. This is enabled by the digital windowed watchdog (DWWD) feature.

Functional Behavior

The DWWD opens a configurable time window in which the watchdog must be serviced. Any attempt to service the watchdog outside this time window, or a failure to service the watchdog in this time window, will cause the watchdog to generate either a reset or a non-maskable interrupt to the CPU. This is controlled by configuring the RTI_RTIDWWDRXNCTRL register. As stated earlier, when the watchdog needs to be enabled by software, the watchdog counter is disabled on a system reset. When the DWWD is configured to generate a non-maskable interrupt on a window violation, the watchdog counter continues to count down. The RTI_INTR_WWD interrupt handler needs to clear the watchdog violation status flag(s) and then service the watchdog by writing the correct sequence in the watchdog key RTI_RTIWDKEY register. This service will cause the watchdog counter to get reloaded from the preload value and start counting down. If the RTI_INTR_WWD handler does not service the watchdog in time, it could count down all the way to zero and wrap around. No second exception for a time out is generated in this case.

Configuration of DWWD

The DWWD preload value (same as DWD preload) can only be configured when the DWWD counter is disabled. The window size and watchdog reaction to a violation can be configured even after the watchdog has been enabled. Any changes to the window size and watchdog reaction configurations will only take effect after the next servicing of the DWWD.

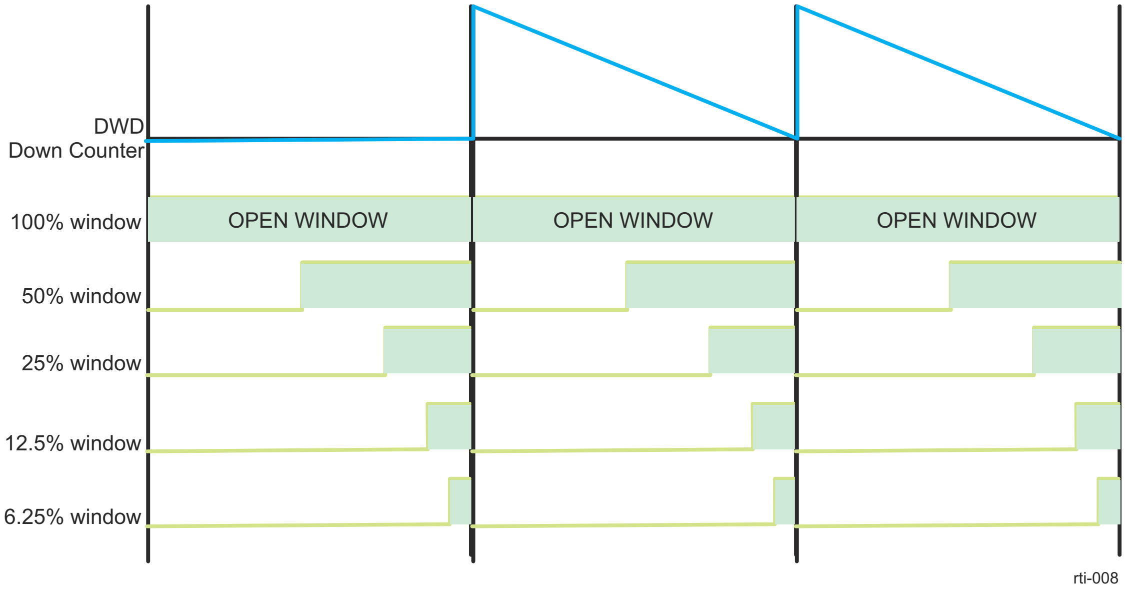


Figure 12-349. RTI Digital Windowed Watchdog Timing Example

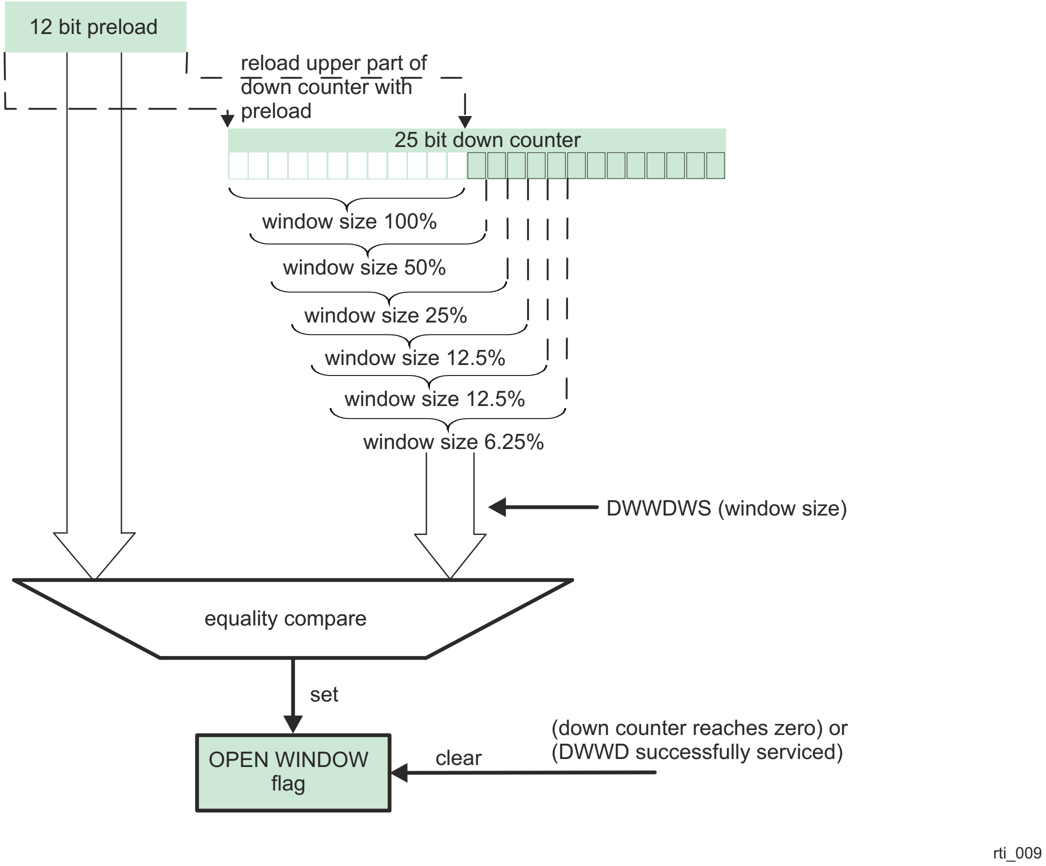


Figure 12-350. RTI Digital Windowed Watchdog Operation Block Diagram

12.6.2.3.1.1 RTI Debug Mode Behavior

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Once the system enters debug mode, the behavior of the RTI depends on the RTI_RTIGCTRL[15] COS bit. If the bit is cleared and debug mode is active, all counters will stop operation. If the bit is set to one, all counters will be clocked normally and the RTI will work like in normal mode.

The DWD counter will not decrement in debug mode and will hold its current value, regardless of the RTI_RTIGCTRL[15] COS bit.

Note

The user must not service the watchdog while in debug mode.

12.6.2.3.1.2 RTI Low Power Mode Operation

The operation of the RTI module is guaranteed in run, doze and snooze mode. In sleep or hibernate mode all clocks will be switched off and the RTI module will not work.

In doze and snooze modes all parts of the RTI are active, since it has to be able to wake up the device with compare and timebases interrupts. Capturing events generated by the interrupt module is also possible since in both modes the peripheral modules are able to generate interrupts, which can trigger capture events. The RTI module will generate compare and timebases interrupts. The compare interrupts will periodically wake up the device.

Note

In the special case of doze mode with DPLL off, RTI_FCLK might have a different period than with DPLL enabled, since RTI_FCLK will be derived from the oscillator output. It has to be ensured that the RTI_ICLK to RTI_FCLK ratio is at least 3:1.

The DWD/DWWD remains active when the device enters low power mode as long as the RTI_FCLK is kept active.

Whenever the LPSC that controls an RTI is in any state other than Enable (see , *Module States*), the RTI cannot count or generate interrupts. For more information, see , *Power Control Modules*.

During standard SoC warm reset the RTI and the rest of the SoC are reset. In this case, the RTI counters are stopped and interrupts are not issued. During reset-isolated warm reset, if an R5FSS is put in reset-isolation, then the associated RTI also becomes reset isolated. As such, the R5FSS and the RTI are not reset, but RTI stops counting and cannot generate interrupts until R5FSS is taken out of CLKSTOP (brought to Enable state).

12.6.2.3.2 RTI Digital Watchdog

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Some applications might use a digital watchdog (DWD) integrated in the RTI module. The digital watchdog generates resets after a programmable period, if no correct key sequence is written to the RTI_RTIWDKEY register. Figure 12-351 shows the digital watchdog functional block.

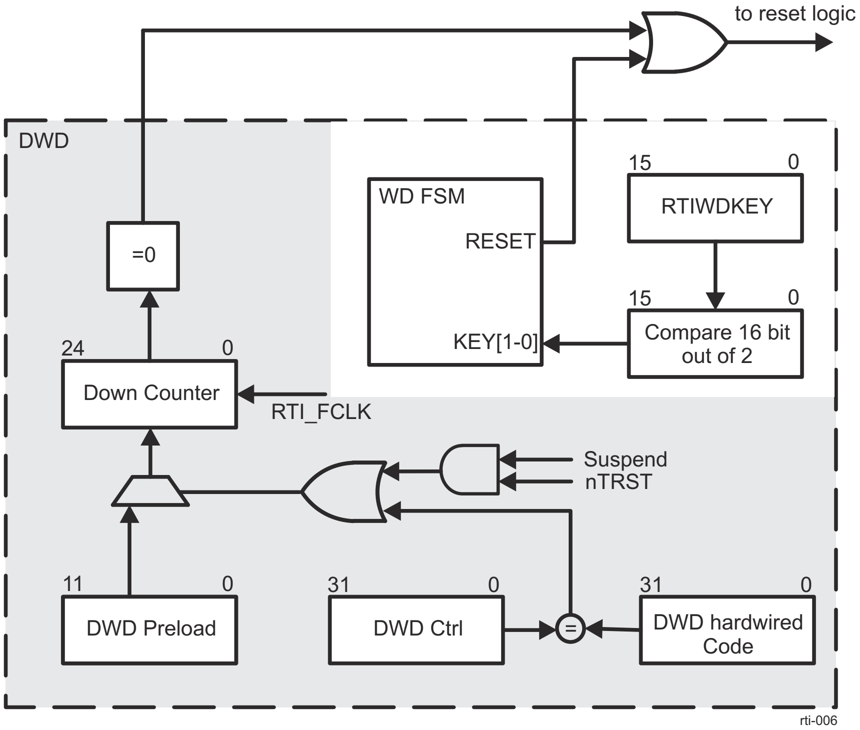


Figure 12-351. RTI Digital Watchdog Functional Block Diagram

The digital watchdog functionality is implemented such that it can be enabled by software.

The DWD starts counting down from the reset value of the RTI_RTIDWDCNTR (DWD Counter Register). The DWD preload register can be configured at any time by the application according to the desired time-out period.

When enabled by software, the digital watchdog is disabled after system reset. If it should be used, it has to be enabled by writing A98559DAh to the RTI_RTIDWDCTRL register. The DWD timeout period must be configured using the DWD preload register before the DWD is enabled. The DWD cannot be disabled by the application once it is enabled.

Note

When the DWD is enabled by software, any system reset will disable the DWD. This reset could have been generated by the watchdog itself.

If the correct key sequence is written to the RTI_RTIWDKEY register (E51Ah followed by A35Ch), the 25-bit DWD Down Counter is reloaded with the 12-bit preload value stored in RTI_RTIDWDPRLD register. If any incorrect value is written to the RTI_RTIWDKEY register, a watchdog reset will occur immediately. A reset will also be generated, when the DWD Down Counter is decremented to 0.

The user has to take into account that the write to the RTI_RTIWDKEY register takes 3 RTI_ICLK cycles. This needs to be considered for the DWD expiration calculation.

The DWD Down Counter will be decremented with RTI_FCLK frequency. If the RTI_FCLK is switched off via the disable registers of the Clock management, the DWD counter stops decrementing. The DWD module cannot generate a reset under this condition.

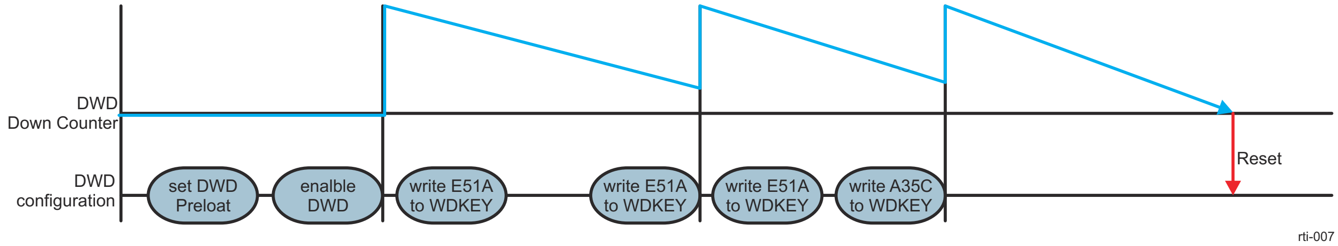


Figure 12-352. RTI Digital Watchdog Operation

The expiration time of the DWD Down Counter can be determined with following equation:

$$t_{exp} = (RTI\_RTIDWDPRLD + 1) \times 2^{13} / RTI\_FCLK \quad (2)$$

where RTI_RTIDWDPRLD = 0...4095

12.6.2.3.3 RTI Counter Operation

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Figure 12-353 shows the RTI module counter blocks. The RTI module supports two counter blocks.

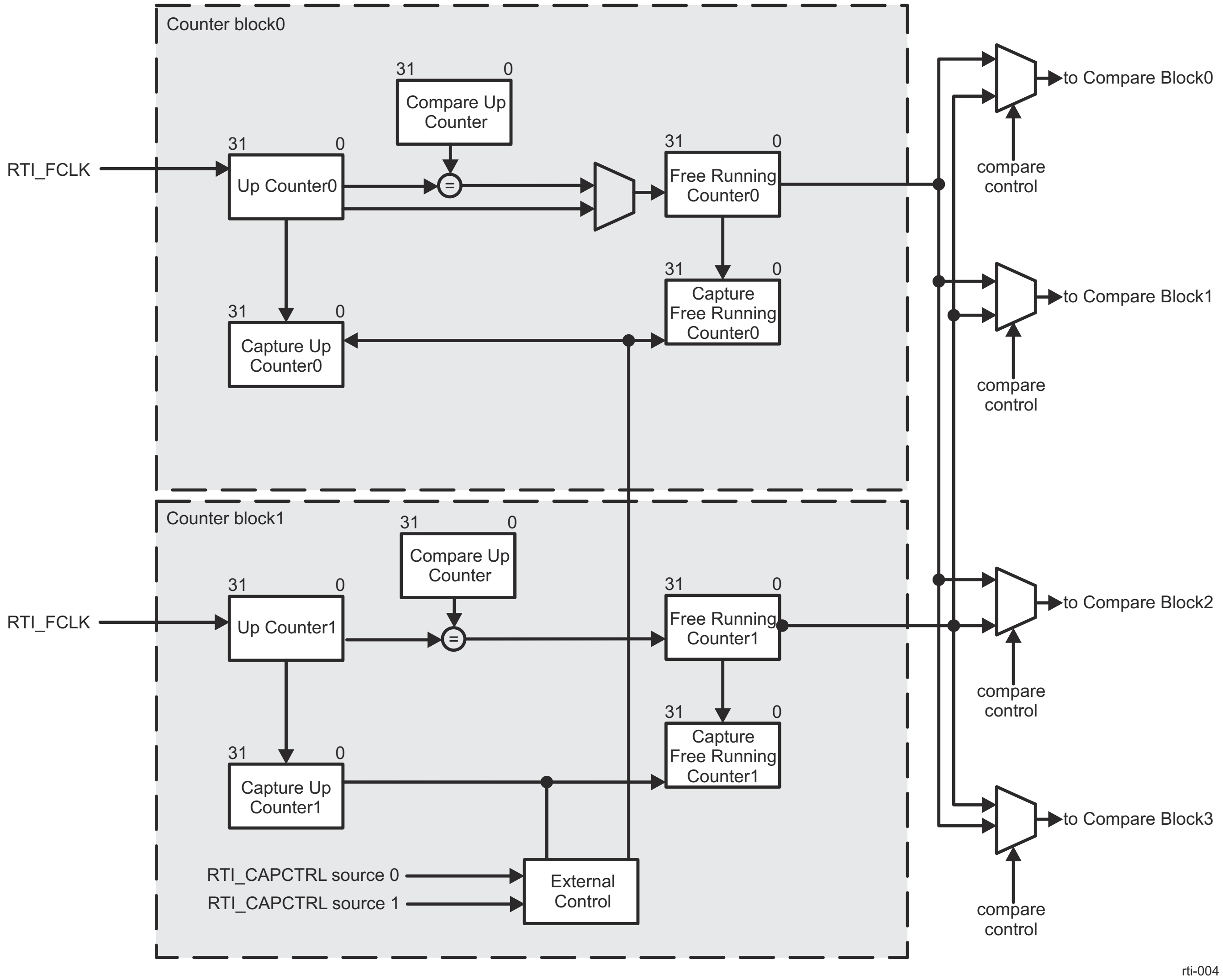


Figure 12-353. RTI Counters Block Diagram

Each block consists of two 32 bit up counters - Up Counter (UC) and Free Running Counter (FRC). The Up Counter (RTI_RTICAUC0 or RTI_RTICAUC1 register) is driven by the RTI_FCLK and counts up until the compare value in the Compare Up Counter register (RTI_RTICPUC0 or RTI_RTICPUC1) is reached. When the compare matches, the second counter (RTI_RTICAFRC0 or RTI_RTICAFRC1 register), which is a free running counter, is incremented. At the same time UCx is reset to zero.

To ensure the consistency of the counters, when both counter value have to be determined, the Free Running Counter has to be read first. This will ensure that at the CPU read cycle, the Up Counter value is stored in the counter register. The second read is done on the Up Counter register, which holds then the value of the counter cycle of the previous read on the Free Running Counter register.

Both blocks provide also a capture feature on external events. Two capture sources can trigger the capture event. Which event triggers block 0 or block 1 is configurable from the RTI_RTICAPCTRL register. The sources are coming from the interrupt manager, in order to be able to generate a capture event when one of the peripheral modules has generated an interrupt. The peripheral, which can generate an event is configured in the interrupt manager. When the event is detected, UCx and FRCx are stored in Capture Up Counter (RTI_RTICAUC0 or RTI_RTICAUC1) and Capture Free Running Counter (RTI_RTICAFRC0 or RTI_RTICAFRC1) registers. The read order of the captured values has to be like the order of the actual counters. So the CAFRCx has to be read first and the CAUCx registers has to be read after the CAFRCx value was determined. While the CAFRCx is read the CAUCx value is loaded into a shadow register to ensure data consistency, if during the two reads of the captured data another capture event happens. If the application fails to read the two registers before a second capture event happens, the previous data will be overwritten.

Figure 12-354 shows the block diagram for one compare block. The RTI module supports four compare blocks.

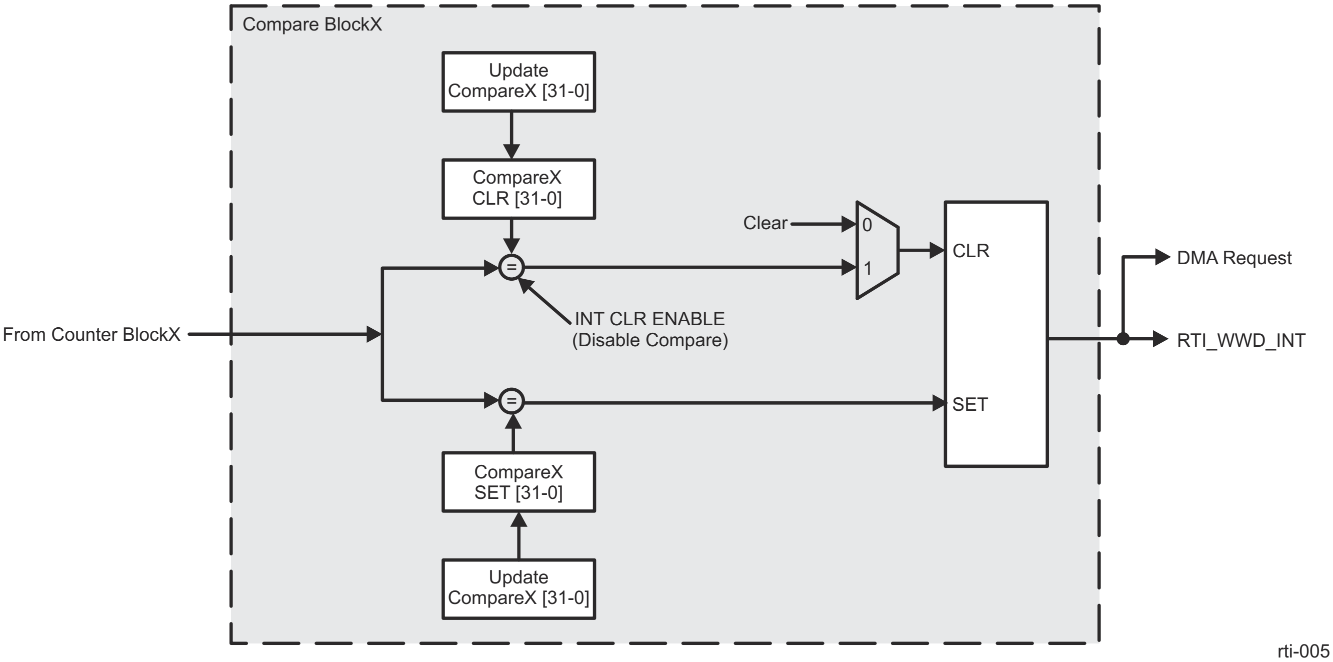


Figure 12-354. RTI Compare Block Diagram

In order to generate interrupt requests to the interrupt manager, there are four compare registers (RTI_RTICOMP0, RTI_RTICOMP1, RTI_RTICOMP2, and RTI_RTICOMP3). Each of the compare registers can be configured to work either on FRC0 (Counter block0) or FRC1 (Counter block1). When the counter value matches the compare value, an interrupt is generated. This sets an interrupt request line to the interrupt manager. The compare value gets updated automatically with the value stored in Update Compare (RTI_RTIUDCP0, RTI_RTIUDCP1, RTI_RTIUDCP2, and RTI_RTIUDCP3) registers when the compare matches. This gives the ability to generate periodic interrupts/DMA requests without having to update the compare value by software.

An optional feature allows an application to program another compare value which is then used to clear the interrupt request line. This feature is supported by four compare clear registers (RTI_RTICOMP0CLR, RTI_RTICOMP1CLR, RTI_RTICOMP2CLR, and RTI_RTICOMP3CLR). When the counter value matches the compare clear value, the interrupt line is cleared. This clears the interrupt request line to the interrupt manager. The compare clear value gets updated automatically with the value stored in Update Compare (RTI_RTIUDCPx) registers when the compare matches.

12.6.3 Real-Time Clock (RTC)

12.6.3.1 RTC Overview

The basic purpose for the RTC is to keep time of day. The other equally important purpose of RTC is for Digital Rights management. Some degree of tamper proofing is needed to ensure that simply stopping, resetting, or corrupting the RTC does not go unnoticed so that if this occurs, the application can re-acquire the time of day from a trusted source. The final purpose of the RTC is to wake the rest of chip up from a power down state.

12.6.3.1.1 RTC Features

The real-time clock (RTC) provides the following features:

- With Analog IP block
  - 2 digital voltage domains with integrated LVL/ISO cells

        - CORE or volatile domain, same as core SOC
        - RTC or Always ON domain
    - Without Analog IP block
        - 1 digital voltage domain, no lvl.iso
- 15 bit 32768Hz counter
- 48 bit seconds counter with +/- 1 30uS upto +/- 1 S drift adjustment every 4048 Seconds
- 256 bits of Scratch PAD
- 1 ON_OFF compare event, 48-bits
- 1 OFF_ON compare event, 48-bits
- 2 event outputs OFF_ON and ON_OFF to CORE
- Support active external 32768 Hz and inactive/gated 32768 Hz
- This allows HOST PROCESSOR to use some of the counter registers as general purpose
- CORE protection logic which enables loose ISO assertion
- Functional lockout, unlock by special vbusp sequence
- DFT lockout, unlock by special 1500 sequence
- HOST PROCESSOR can issue OFF now cmd
- HOST PROCESSOR can update MMRs without polling, thanks to HW Shadow/Auto Sync
- HOST PROCESSOR can read time without polling, thanks to HW Shadow/Auto Sync
- External IOs *(Optional)*
    - 4 wakeup inputs with active high/low including optional debounce
        - Async wake up supported
    - 1 pmic_enable output
- Analog Interface *(Optional)*
    - 32 bit Analog Config output
    - ISO input
    - 32KHz input

12.6.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.6.3.2 RTC Integration

This device includes a Real-Time (RTC) module to allow easy tracking of time and date and the generation of real time alarms.

The following tables provide pin level detail for each of the interfaces on this module.

Table 12-306 describes the 1500 Interface for the DFT unlock circuit.

Table 12-306. 1500 Interface

Signal Name	Direction	Default Value	Description
jtag_wrck	In	1'd0	1500 wrapper clock
jtag_wrstn_n	In	1'd1	1500 wrapper reset (active low)
jtag_wsi	In	1'd0	1500 wrapper serial input
jtag_selectwir	In	1'd0	1500 select wrapper instruction register
jtag_shiftwr	In	1'd0	1500 shift wrapper register
jtag_updatewr	In	1'd0	1500 update wrapper register
jtag_capturewr	In	1'd0	1500 capture wrapper register
jtag_wso	Out	1'd0	1500 wrapper serial out

Table 12-307 describes the PMIC Control External Wakeup and PMIC ON/OFF Control IOs.

Table 12-307. PMIC Control IOs

Signal Name	Direction	Default Value	Description
pmic_ext_wakeup0_io	In	1'd0	RTC Wakeup0
pmic_ext_wakeup1_io	In	1'd0	RTC Wakeup1
pmic_ext_wakeup2_io	In	1'd0	RTC Wakeup2
pmic_ext_wakeup3_io	In	1'd0	RTC Wakeup3
pmic_pmic_enable_io	Out	1'd1	RTC PMIC Enable 1 = ON 0 = OFF

Table 12-308. Analog Interface

Signal Name	Direction	Default Value	Description
ana_osc32k_clk	In	NA	Analog 32768 buffered Crystal clock If no analog, provide a near 32768 clock
ana_iso	In	1'd0	Analog ISO 1 = Isolated 0 = Not Isolated If no analog, tie 1’b0
ana_porz	In	NA	Analog PowerOnReset 1 = not asserted 0 = asserted This will assert when ON/BAT domain is powering up If no analog, then you can connect same reset which was used for rst_mod_g_rst_n You can also use por_rst_n class, it’s a don’t care
ana_cfg[31:0]	Out	TBD	Analog config If no analog, NC

Table 12-309. PSC Interface

Signal	Direction	Default Value	Description
pwri_clkstop_idle	Out	1'd1	The IP is in IDLE state, output of an IP
pwrs_clkstop_req	In	1'd0	Clock stop request
pwrs_clkstop_ack	Out	1'd0	Clock stop acknowledge
pwrw_clkstop_wakeup	Out	1'd0	Wakeup It requires clock stop protocol to be active and active vclk_clk
pwr_clk_clk_en	In	1'd1	Clock-gate enable to IP
pwr_clk_clk_en_ack	Out	pwr_clk_clk_en	Clock-gate enable acknowledge from IP

Table 12-310 describes the Main IP DFT Interface.

Table 12-310. IP DFT Interface

Signal Name	Direction	Default Value	Description
dft_partition_en	In	1'd0	dft_partition_en
dft_scan_en	In	1'd0	dft_scan_en
dft_clk_force_en	In	1'd0	dft_clk_force_en
dft_async_rst_sel	In	1'd0	dft_async_rst_sel
dft_test_async_rst_n	In	1'd1	dft_test_async_rst_n
dft_tft_mcp_dis	In	1'd0	Assert High to block MCP path
dft_local_clk_en	In	1'd0	dft_local_clk_en
dft_mode_atpg	In	1'd0	ATPG

The reset shown in Table 12-311 only goes to the core domain.

Table 12-311. Reset Interface

Signal Name	Direction	Default Value	Description
rst_mod_g_rst_n	In	1'd1	Module level main reset

Table 12-312 describes the Main on only VBUSP target port

Table 12-312. VBUSP Target Port

Signal Name	Direction	Default Value	Description
pr1_slv_req	In	1'b0	Request
pr1_slv_dir	In	1'b0	Direction
pr1_slv_address[31:0]	In	32'd0	Address
pr1_slv_xcnt[2:0]	In	3'd4	Good Byte Count
pr1_slv_byten[3:0]	In	{4{1'b1}}	Byte Enables
pr1_slv_wdata[31:0]	In	32'd0	Write Data
pr1_slv_wready	Out	1'b1	Write Ready
pr1_slv_rdatap[31:0]	Out	32'd0	Read Data (Pipelined)
pr1_slv_rready	Out	1'b1	Read Ready
pr1_slv_emudbg	In	1'b0	Emulation Debug Attribute

12.6.3.3 RTC Functional Description

12.6.3.3.1 RTC Block Diagram

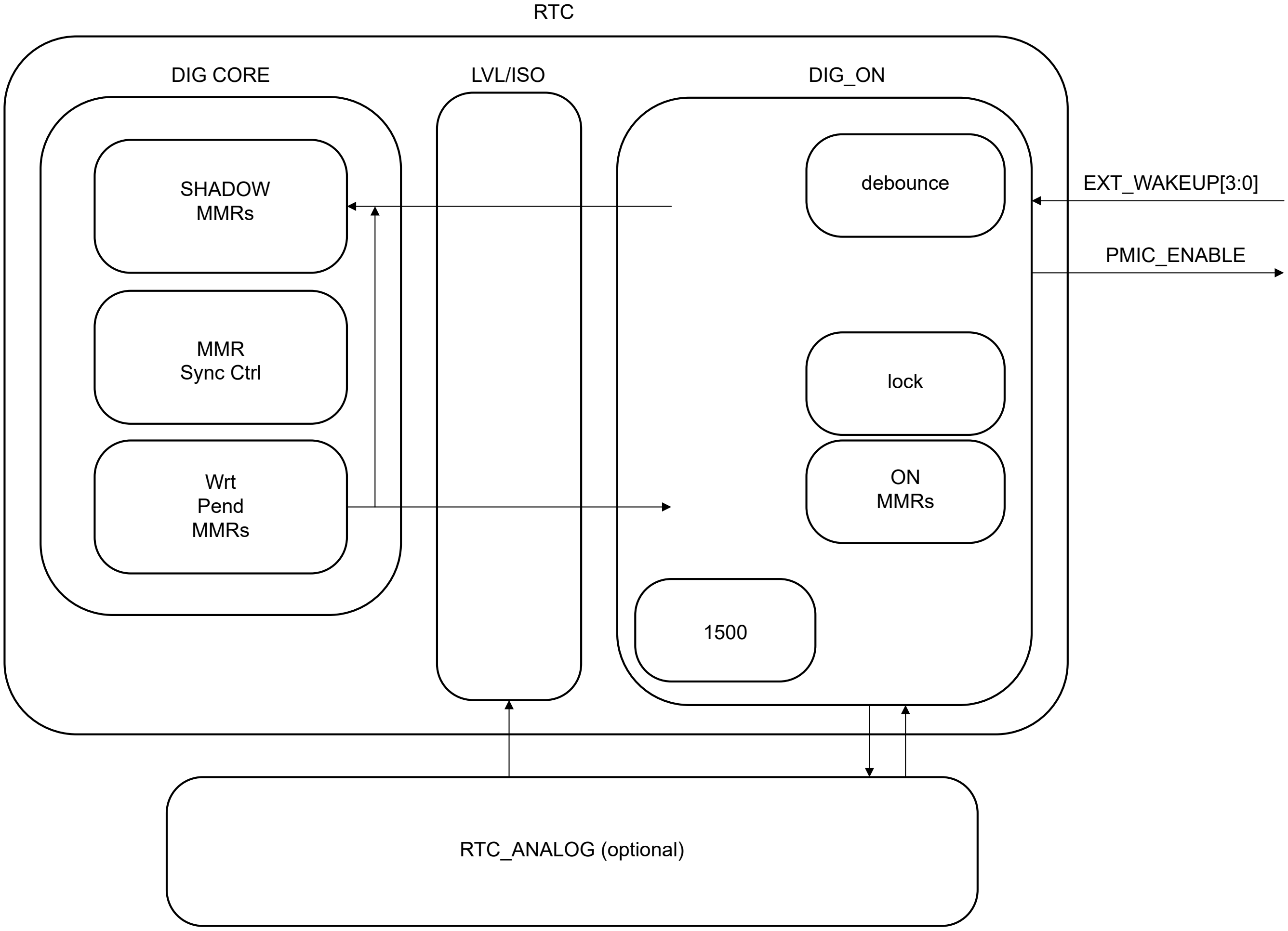


Figure 12-355. RTC Block Diagram

The RTC is composed of 3 major blocks, DIG_CORE, DIG_ON, and LVL_ISO.

12.6.3.3.1.1 DIG_CORE uARCH

The DIG_CORE block is on the CORE power domain which will power OFF/ON when the SOC powers OFF/ON. It contains, CORE IF logic, Shadow MMRs and MMR Sync logic.

The MMR Sync logic has 2 modes of operation

- Refresh/Sync after Core Reset
- Sync after HOST PROCESSOR Updates Shadow MMRs

Refresh/Sync after Core Reset Deassertion

After every Core Reset event, the MMR Sync logic we refresh ALL Shadow MMRs by copying the contents of ON MMRs into the Shadow MMRs.

Core Reset DeAssertion

The internal state machine Reads All MMRs in linear order

- If(GENRAL_CTL..32K_CLK_EN = 1)
  - Max delay of 2 32768Hz period delay
- If(GENRAL_CTL..32K_CLK_EN = 0)

  - Max delay 1.2uS = 32 * vbus_clk period delay(27MHz)
  - It will not wait for high to low 32768 event to read MMRs

The internal state machine Sets SYNCPEND.RD_DONE bit when the copy from the ON domain is completed. The host processor needs to wait for this status bit assertion before it reads the other MMRs

Sync after HOST PROCESSOR Updates Shadow MMRs

host processor UNLOCK

host processor Wrts to MMRs

The ON domain MMRs will get updated after a finite delay

- If(GENRAL_CTL..32K_CLK_EN = 1)
  - Max delay of 2 32768Hz period delay
- If(GENRAL_CTL..32K_CLK_EN = 0)
  - Max delay 8uS = 32 * vbus_clk period delay
  - It will not wait for high to low 32768 event to read MMRs

The internal state machine sets SYNCPEND.WR_DONE bit. This needs to get cleared before the next **HOST PROCESSOR Updates Shadow MMRs**

Note

The CORE domain has its own copy of the sub-second counter and second counter along with the compensation logic. The 2 domains will always be in sync after a reset or after host processor does a update to the counters or compensation

12.6.3.3.1.2 DIG_ON uARCH

The DIG_ON block is in the always ON domain, the power is provided by the ANALOG Block. It contains the always ON MMRs which will preserve state of the Shadow MMRs when the CORE is OFF state.

The 15 bit 32786Hz counter and the 48 bit second counter maintains count when the CORE is OFF. It has 2 comparators one for OFF_ON and one for ON_OFF event. It has External Wakeup events which can get de-bounced to control the PMIC_ENABLE. It controls the PMIC_ENABLE output which can change state based on ON_OFF, OFF_ON, and HOST PROCESSOR OFF now events.

The functional lockout and the dft lockout (1500) logic resides in this domain.

12.6.3.3.1.3 ISO_LVL uARCH

The ISO_LVL module constrains all DIG_CORE <-> DIG_ON Level/Isolation cells between these 2 domains. They use tibox to instantiate them. If No Analog support, then SOC integration team will not add in these RTC.

12.6.3.3.1.4 DIG_CORE to DIG_ON updates uARCH

Note

If No Analog support, then DIG_CORE and DIG_ON will be on a common V domain.

This section defines how the DIG_CORE Shadow MMRs maintain coherences with the DIG_ON Live MMR domain. All vbusp transactions terminate in the DIG_CORE block. All vbusp write transaction which require DIG_ON updates is completed by the Shadow to Live HW sequencer.

This HW sequencer has 2 modes of operation.

- Immediate Write Mode
  - When GENRAL_CTL.32K_OSC_DEP_EN = 0
  - It will start the write updates immediately
- Delayed Write Mode
  - When GENRAL_CTL.32K_OSC_DEP_EN = 1
  - It will start the write updates after the first 32khz_clk high to low transition

In Delayed Write Mode

For example, HOST PROCESSOR updates OFF_ON_S_CNT_LSW and OFF_ON_S_CNT_MSW.

After the HOST PROCESSOR completes the OFF_ON_S_CNT_MSW, the HW sequencer will start the process of updating the DIG_ON domain at the first available 32khz_clk is low cycle.

Note

32khz_clk is already low, the circuit will wait next low cycle to insure we have the full low period to do all pending updates. The HOST PROCESSOR can observe the SYNCPEND.WR_DONE bit, when set the write operations has completed to the DIG_ON domain

---

Note

If GENRAL_CTL..32K_CLK_EN = 0, then the HW sequencer will not wait for 32khz_clk high to low event, since this will force 32khz_clk low. This removes the dependency of an active 32768Hz clock

---

ALL MMR write transaction require full 4 Bytes writes in order to reduce the logic size of the DIG_ON domain.

RULE: Require 4 Bytes writes (less logic and iso)

Note

ON domain MMRs have a write lock protection circuit to prevent corruption of the DIG_ON domain during a power down event since ISO assertion can be late.

Due to this fact, the HOST PROCESSOR must first unlock write access by performing the unlock sequence, by simply writing Kick0 and Kick1 with the correct pattern and sequence. After this is done, the RTC is in an unlock date. The HOST PROCESSOR will need to relocking by writing any pattern to Kick1

12.6.3.3.2 CPU Interrupt Support

12.6.3.3.2.1 CPU Interrupts

The RTC can produce one HW event output active high level and active high pulse. This one output will assert on 3 internal HW events.

1. Timer ON_OFF event
2. Timer OFF_ON event
3. External Wakeup event

HOST PROCESSOR can read the Interrupt MMR status to determine which events caused the RTC event output to assert. vbus_clk can be on or off, the active high level will assert on either scenario. The 32768Hz clock must be active to cause a ON_OFF or OFF_ON event. The External Wakeup event can occur without 32768Hz clock if debounce is not enabled.

The Interrupt MMR programing model uses the standard Keystone3 schema which allows HOST PROCESSOR to issue debug event. Also, the enabling of the events are backed up in the ON domain, so HOST PROCESSOR will not enable to enable events on every power cycle of the CORE domain.

12.6.3.3.3 Programming Usage Guide

12.6.3.3.3.1 No Analog Support

DIG_ON domain MMR Write Rules

- UnLock DIG_CORE (Wrt Kick0 and Wrt Kick1)
  - Keep it UnLock
- Write all MMRs in the same address order has MMRs from low to high
  - For example . Wrt Scratch Storage 0 through Scratch Storage 7
- HOST PROCESSOR poles until SYNCPEND.WR_PEND is 0
  - Max completion is 60 uSeconds when GENRAL_CTL. 32K_OSC_DEP_EN is set
  - Max completion is 10 uSeconds when GENRAL_CTL. 32K_OSC_DEP_EN is clr
- HOST PROCESSOR is not allowed to perform new write without waiting for clearing of SYNCPEND.WR_PEND

After every new power up of the SOC

- Unlock RTC by writing correct pattern in Kick0 and Kick1
- Keep it UnLock
- HOST PROCESSOR can verify that 32Khz_osc_clk is toggling by reading SYNCPEND. 32K_CLK_OBS
- Should not be required, since the 32Khz_osc_clk will always will be active
- HOST PROCESSOR sets GENRAL_CTL.32K_OSC_DEP_EN
- Wait for 60 uSec
- Initialize ALL RTC MMRs in the DIG_ON domain in the same order as the address map
- The RTCs MMRs do not have a reset state in general, only a few required MMRs bits have one.
- HOST PROCESSOR must initialize all bits of the MMRs which reside in DIG_ON domain
  - Ie wrt <value>@0x00, <value>@0x04, <value>@0x08 ….<value>@0x50
- HOST PROCESSOR poll SYNCPEND.WR_PEND until null
  - This means all DIG_ON domain MMRs have been written to

RTC is now in an operational state and fully configured.

32768Hz time adjustment

- HOST PROCESSOR UnLock RTC(required for writes to DIG_ON domain)
- HOST PROCESSOR can readSUB_S_CNT(1st), S_CNT_LSW(2nd), S_CNT_MSW(3rd)
- HOST PROCESSOR can write new time by writing to SUB_S_CNT(1st), S_CNT_LSW(2nd), S_CNT_MSW(3rd)
- HOST PROCESSOR ReLock RTC(writing 0x0000_0000 to KICK1)
- HOST PROCESSOR poll SYNCPEND.WR_PEND until null

32768Hz time drift adjustment

- HOST PROCESSOR UnLocks RTC(required for writes to DIG_ON domain)
- HOST PROCESSOR can readSUB_S_CNT(1st), S_CNT_LSW(2nd), S_CNT_MSW(3rd)
- SW determines drift rate
- HOST PROCESSOR updates or enables drift adjustment by HOST PROCESSOR write new COMP_LSB and COMP_MSB
- HOST PROCESSOR ReLock RTC(writing 0x0000_0000 to KICK1)
- HOST PROCESSOR poll SYNCPEND.WR_PEND until null

12.6.3.3.3.2 With Analog Support

DIG_ON domain MMR Write Rules

- UnLock DIG_CORE (Wrt Kick0 and Wrt Kick1)
- Write all MMRs in the same address order has MMRs from low to high
- For example . Wrt Scratch Storage 0 through Scratch Storage 7
- ReLock DIG_CORE (Wrt 0x0000_0000 to Kick1)
- HOST PROCESSOR poles until SYNCPEND.WR_PEND is 0
  - Max completion is 60 uSeconds when GENRAL_CTL. 32K_OSC_DEP_EN is set
  - Max completion is 10 uSeconds when GENRAL_CTL. 32K_OSC_DEP_EN is clr
- HOST PROCESSOR is not allowed to perform new write without waiting for clearing of SYNCPEND.WR_PEND

First Time Powered ON(DIG_ON)

- Unlock RTC by writing correct pattern in Kick0 and Kick1
- HOST PROCESSOR updates ANALOG_CTRL MMR
  - Set the correct parameters
  - Enable 32768Hz OSC
  - Wait for 3 seconds to allow the 32768Hz OSC to lock
- HOST PROCESSOR can verify that 32Khz_osc_clk is toggling by reading SYNCPEND. 32K_CLK_OBS
- HOST PROCESSOR sets GENRAL_CTL.32K_OSC_DEP_EN
- HOST PROCESSOR ReLock DIG_CORE (Wrt 0x0000_0000 to Kick1)

Initialize ALL RTC MMRs in the DIG_ON domain in the same order as the address map except for the first 2 writes which should always be to the 2 KICK0/KICK1 MMRs to unlock write transaction and the last write which should relock by writing 0x0 to KICK1

- The RTCs MMRs do not have a reset state in general, only a few required MMRs bits have one.
- HOST PROCESSOR must initialize all bits of the MMRs which reside in DIG_ON domain
- HOST PROCESSOR UnLock
- Ie wrt <value>@0x00, <value>@0x04, <value>@0x08 ….<value>@0x50
- HOST PROCESSOR ReLock RTC(writing 0x0000_0000 to KICK1)
- HOST PROCESSOR poll SYNCPEND.WR_PEND until null
- This means all DIG_ON domain MMRs have been written to

RTC is now in an operational state and fully configured

32768Hz time adjustment

- HOST PROCESSOR UnLock RTC(required for writes to DIG_ON domain)
- HOST PROCESSOR can readSUB_S_CNT(1st), S_CNT_LSW(2nd), S_CNT_MSW(3rd)
- HOST PROCESSOR can write new time by writing to SUB_S_CNT(1st), S_CNT_LSW(2nd), S_CNT_MSW(3rd)
- HOST PROCESSOR ReLock RTC(writing 0x0000_0000 to KICK1)
- HOST PROCESSOR poll SYNCPEND.WR_PEND until null

32768Hz time drift adjustment

- HOST PROCESSOR UnLocks RTC(required for writes to DIG_ON domain)
- HOST PROCESSOR can readSUB_S_CNT(1st), S_CNT_LSW(2nd), S_CNT_MSW(3rd)
- SW determines drift rate
- HOST PROCESSOR updates or enables drift adjustment by
  - HOST PROCESSOR write new COMP_LSB and COMP_MSB
- HOST PROCESSOR ReLock RTC(writing 0x0000_0000 to KICK1)
- HOST PROCESSOR poll SYNCPEND.WR_PEND until null

Update OFF_ON and/or ON_OFF times

- HOST PROCESSOR poll SYNCPEND.WR_PEND until null (ACTION PRE vs POST)
- HOST PROCESSOR UnLocks RTC(required for writes to DIG_ON domain)
- HOST PROCESSOR update OFF_ON_S_CNT_LSW/MSW and/or ON_FF_S_CNT_LSW/MSW
- HOST PROCESSOR can update SCRATCH0/7
- HOST PROCESSOR update GENRAL_CTL to enable if required
- HOST PROCESSOR ReLock RTC(writing 0x0000_0000 to KICK1)
- HOST PROCESSOR poll SYNCPEND.WR_PEND until null

Note

The new OFF time must be at least 2 seconds in the future

OFF NOW

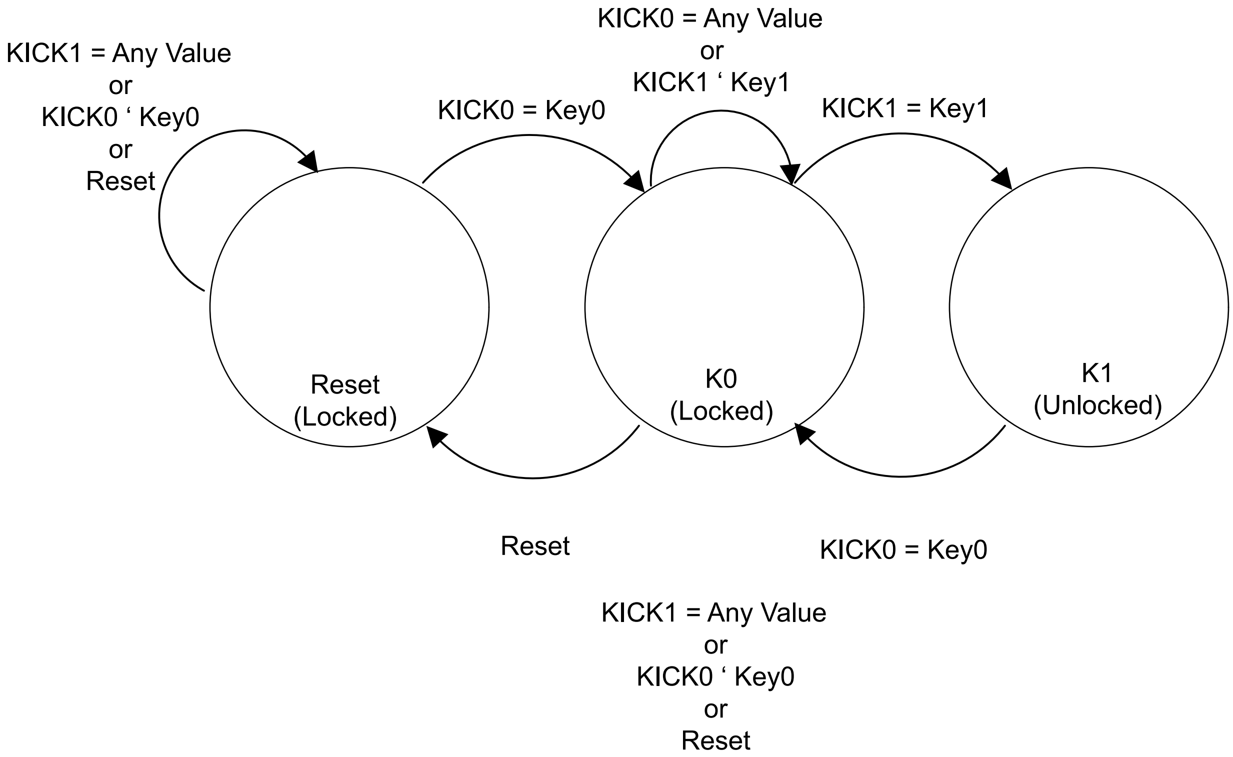
- HOST PROCESSOR UnLocks RTC(required for writes to DIG_ON domain)
- Optional (HOST PROCESSOR can update SCRATCH0/7)
- HOST PROCESSOR issues a SW_OFF in GENRAL_CTL
- HOST PROCESSOR does a dead loop, wait for power OFF

Note

Note any Write to SW_OFF will cause a Auto ReLock

12.6.3.3.3.2.1 MMR Spurious WRT Protection

The module also contains a kicker mechanism (Figure 12-356) to prevent any spurious writes from changing the register values. This mechanism requires two MMR writes to the Kick0 and Kick1 registers with exact data values before the kicker lock mechanism is released. Once released, the MMRs are writeable. The Kick0 data is 83E7 0B13h; the Kick1 data is 95A4 F1E0h. Note that it remains in an unlocked state until an OCP reset or invalid data pattern is written to one of the Kick0 or Kick1 registers.



- Key0 = 83E7 0B13h
- Key1 = 95A4 F1E0h
- Locked = Write protection enabled
- Unlocked = Write protection disabled

Figure 12-356. Kick Register State Machine Diagram

- S0 is the Reset/Idle state
- S1 is an wrt cycle of 83E7 0B13h at Kick0 completed state
- S2 is the UNLOCK MMR WRT state
- S0 → S1 when wrt cycle of 83E7 0B13h at Kick0
- S1 → S2 when wrt cycle of 95A4 F1E0h at Kick1
- S1 → S0 when reset event
- S2 → S0 when reset event OR OCP wrt cycle of NOT 83E7 0B13h at Kick0 OR OCP wrt cycle at Kick1
- S2 → S1 when wrt cycle of 83E7 0B13h at Kick0

12.6.3.3.3.2.2 Crystal Compensation

In order to compensate for any inaccuracy of the 32768HZ oscillator, the HOST can perform a calibration of the oscillator frequency, calculate the drift compensation versus one-hour period and load the compensation registers with the drift compensation value. If the COMP_REG value is positive, compensation occurs after the second change event. COMP_REG cycles are removed from the next second. If the COMP_REG value is negative, compensation occurs before the second change event. -COMP_REG cycles are added to the current second. This enables to compensate with a 132 kHz period accuracy each 4096 Seconds. The waveform below summarizes positive and negative compensation effect.

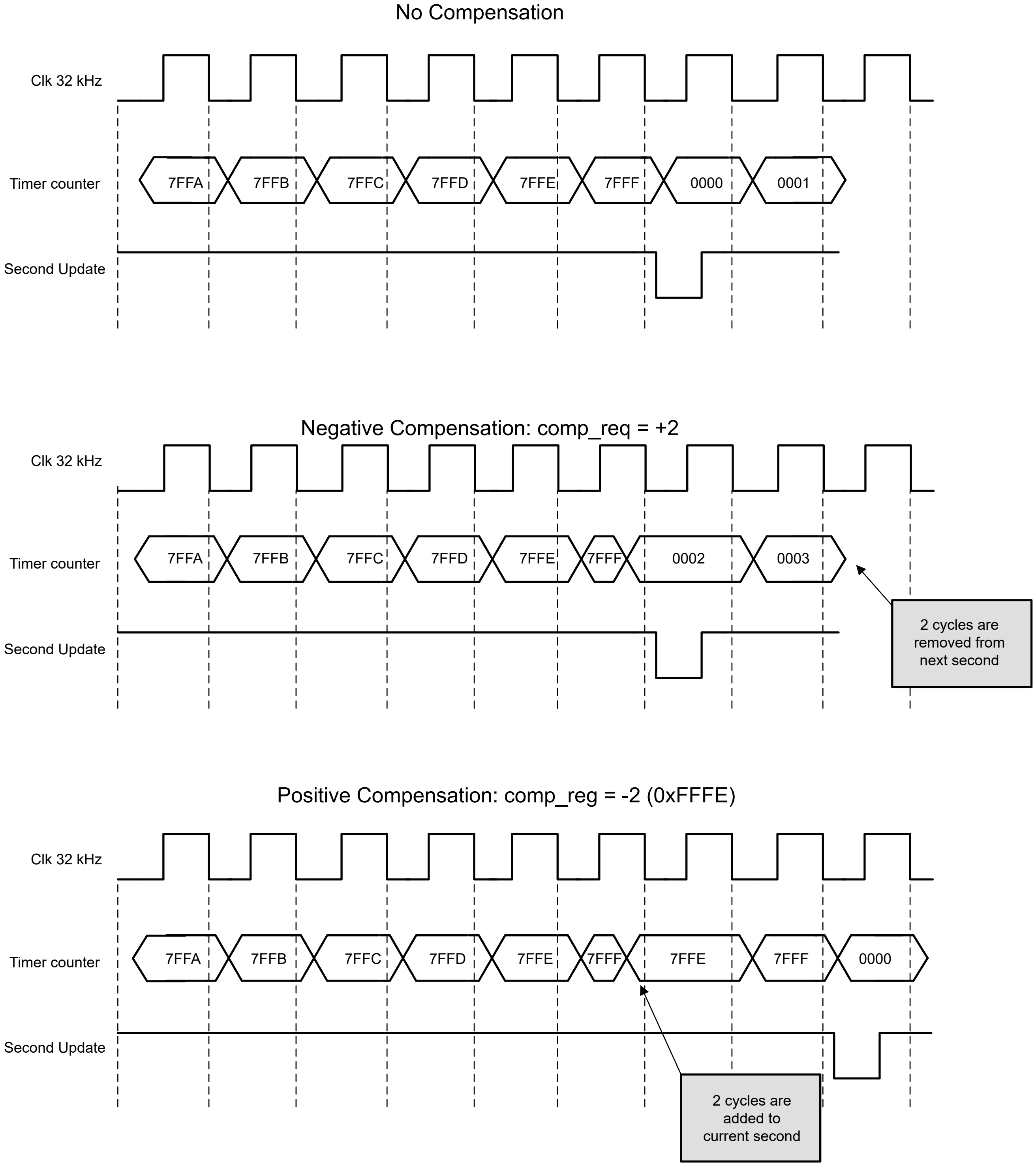


Figure 12-357. Compensation Illustration

12.6.3.3.4 Scratch Registers

The RTC provides eight general-purpose registers (SCRATCHx_REG) that can be used to store 32-bit words -- these registers have no functional purpose for the RTC. Software using the RTC may find the SCRATCHx registers to be useful in indicating RTC states. For example, the SCRATCHx_REG registers may be used to indicate write-protection lock status or unintentional power downs. To indicate write-protection, the software should write a unique value to one of the SCRATCHx_REG registers when write-protection is disabled and another unique value when write-protection is enabled again. In this way, the lock-status of the registers can be determined quickly by reading the SCRATCH register. To indicate unintentional power downs, the software should write a unique value to one of the SCRATCHx_REG registers when RTC is configured and enabled. If the RTC is unintentionally powered down, the value written to the SCRATCH register is cleared. For more information, *see RTCSS Registers*.

12.6.3.3.5 KS3 Clock Stop Protocol

The IP is complaint to KS3 Clock Stop Protocol, please refer to its spec.

For this IP

- pwri_clkstop_idle = !(RD_PEND or WR_PEND or EVENT_OFF_ON or EVENT_ON_OFF)
- If any of these MMRs are set, pwri_clkstop_idle = 0 or busy
- pwrs_clkstop_ack will not assert per spec unless pwrs_clkstop_req == 1 and pwri_clkstop_idle == 1
- pwrw_clkstop_wakeup will not assert unless pwrs_clkstop_ack == 1 AND vclk_clk is active

  It will assert rtc_event_pend_intr asserts
- The integration guideline is to always use rtc_event_pend_intr for wakeup event since it has NO dependencies on clock stop protocol nor active vclk_clk is required, just 32k_clk needs to be active

12.6.4 Timers

This section describes the Timer modules for the device.

12.6.4.1 Timers Overview

All timers include specific functions to generate accurate tick interrupts to the operating system.

Each timer can be clocked from several different independent clocks. The selection of clock source is made from the TIMERn_CLKSEL registers, where n is in the instance .

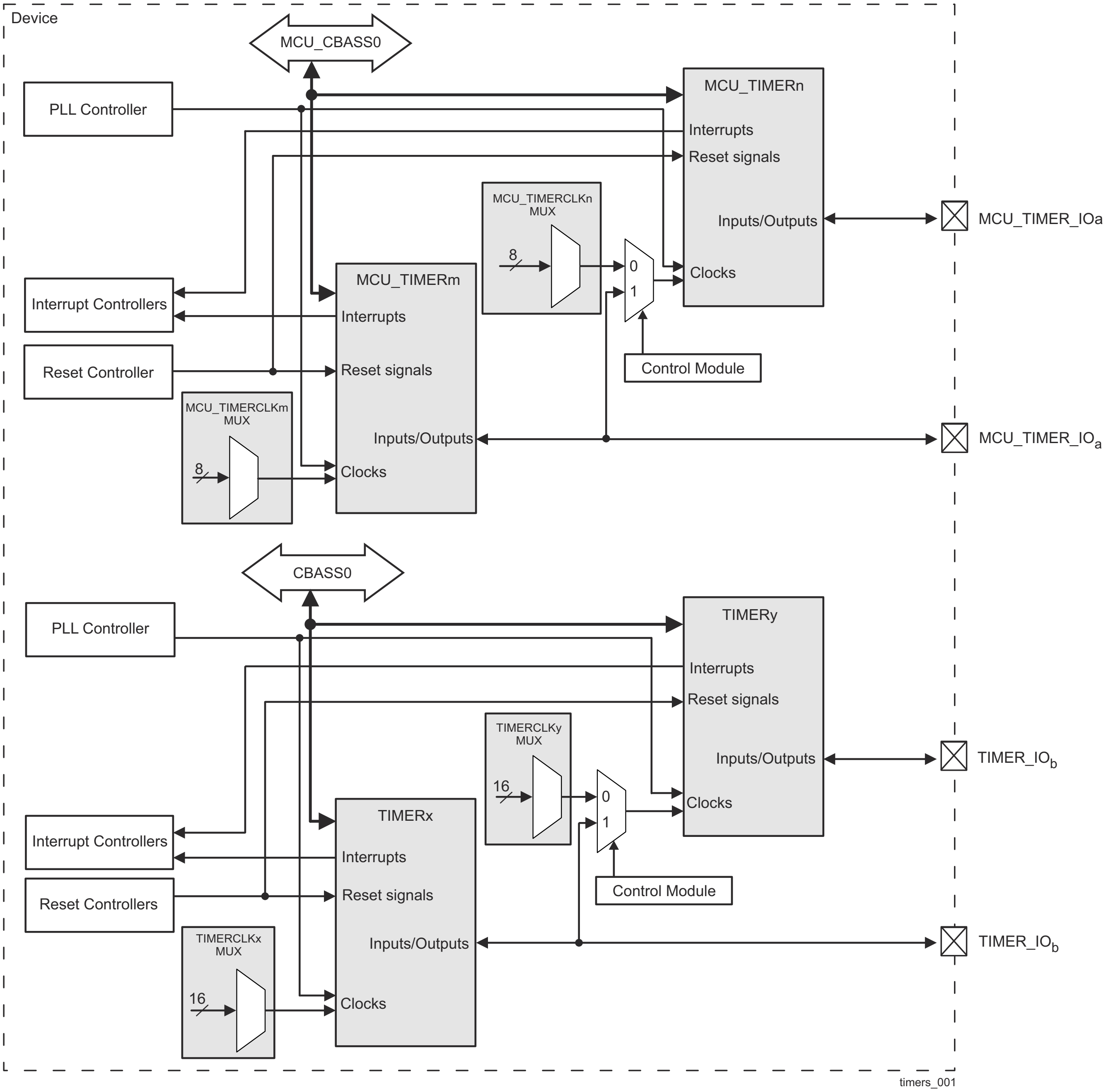
In the MCU domain the device provides up to 4 timer pins, one for each instance, to be used as MCU Timer Capture inputs or as MCU Timer PWM outputs. (See *Module Integration* and the device specific datasheet to see if MCU Timers apply)

In the MAIN domain the device provides up to 11 timer pins, one for each instance, to be used as Timer Capture inputs or as Timer PWM outputs. (See device specific datasheet to see details on timer pins.)

Each odd numbered timer instance from each of the domains may be optionally cascaded with the previous even numbered timer instance from the same domain to form up to a 64-bit timer. For example, TIMER1 may be cascaded to TIMER0, MCU_TIMER1 may be cascaded to MCU_TIMER0, etc.

When cascaded, TIMERi acts as a 32-bit prescaler to TIMERi+1, as well as MCU_TIMERn acts as a 32-bit prescaler to MCU_TIMERn+1. TIMERi / MCU_TIMERn must be configured to generate a PWM output edge at the desired rate to increment the TIMERi+1/ MCU_TIMERn+1 counter.

Figure 12-358 is an overview of the timers.



m = even instances of MCU Timer. See the device datasheet for valid domains and instances.

x = even instances of Timer. See the device datasheet for valid domains and instances

Note

n = odd instances of MCU Timer. See the device datasheet for valid domains and instances.

Note

y = odd instances of Timer. See the device datasheet for valid domains and instances

Figure 12-358. Timers Overview

12.6.4.1.1 Timers Features

The following are the main features of the timer controllers:

- Target interface supports:

  - 32-bit data bus width
  - 32-bit access supported
  - 10-bit address bus width
  - Write nonposted transaction mode supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start/stop mode
- Programmable divider clock source (2^n, where n = [0-8])
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- On-the-fly read/write register (while counting)
- Generates a 1-ms tick clock with a 32.768 kHz functional clock sourced from the LFOSC

12.6.4.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.6.4.2 Timers Environment

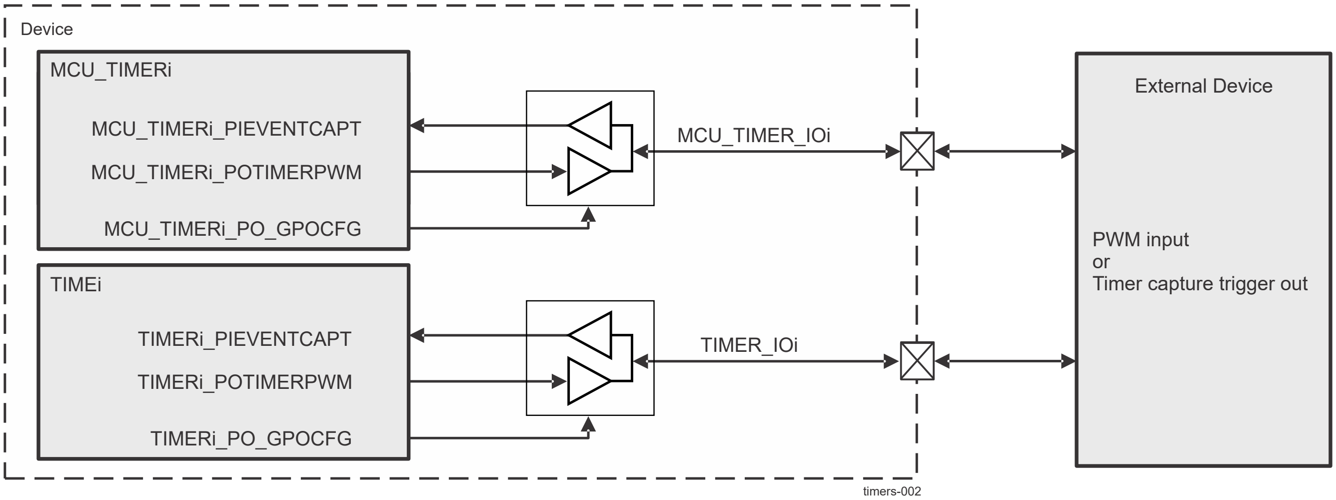
The MCU_TIMER[3-0] and TIMER[11-0] modules are hereinafter referred to as timer module.

This section describes the timers external connections (environment).

12.6.4.2.1 Timer External System Interface

Each timer can send or receive stimulus to/from the external (off-chip) system. In the device all timers are configured to output a PWM pulse or receive an external event signal used as a trigger to capture the current timer count.

Figure 12-359 shows the external system interface for the timers, and Table 12-313 describes the timer inputs and outputs.



Note

i represents a TIMER instance. See the device datasheet for available domains and TIMER instances.

Figure 12-359. Timers External System Interface

Table 12-313. Timer I/O Signals

Module Pin	Device Level Signal	I/O[1]	Description	Module Pin Reset Value[2]
		MCU_TIMERi[2]		
MCU_TIMER_IOi[2]	MCU_TIMERi[2]_PIEVENTCAPT MCU_TIMERi[2]_POTIMERPWM	I/O	MCU_TIMERi[2] trigger input or MCU_TIMERi[2] output	0
		TIMERi[2]		
TIMER_IOi[2]	TIMERi[2]_PIEVENTCAPT TIMERi[2]_POTIMERPWM	I/O	TIMERi[2] trigger input or TIMERi[2] PWM output	0

(1) When configured for that function; I = Input, O = Output
(2) i represents a TIMER instance. See the device datasheet for available domains and TIMER instances.

Note

Each MCU_TIMER_PO_GPOCFG and TIMER_PO_GPOCFG signals are used as an output enable to control the function of the MCU_TIMER_IO[3-0], and respectively TIMER_IO[11-0], as the PWM output (PO_GPOCFG = 0) or capture input (PO_GPOCFG = 1).

Note

For more information about device level signals (pull-up/down resistors, buffer type, and others), see tables *Pin Attributes* in the device-specific Datasheet.

12.6.4.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.6.4.4 Timers Functional Description

Each timer contains a free-running upward counter with autoreload capability on overflow. The timer counter can be read and written on-the-fly (while counting). Each timer includes compare logic to allow an interrupt event on a programmable counter matching value. A dedicated output signal can be pulsed or toggled on either an overflow or a match event. This offers time-stamp trigger signaling or PWM signal sources. A dedicated input signal can be used to trigger an automatic timer counter capture or an interrupt event on a programmable input signal transition. A programmable clock divider (prescaler) allows reduction of the timer input clock frequency. All internal timer interrupt sources are merged into one module interrupt line and one wake-up line.

Each internal interrupt source can be independently enabled and disabled by a dedicated bit in the DMTIMER1MS_IRQSTATUS_SET and DMTIMER1MS_IRQSTATUS_CLR register for the interrupt features, and a dedicated bit of the DMTIMER1MS_IRQWAKEEN register for a wake-up. In addition, timers have a mechanism implemented to generate an accurate tick interrupt.

For each timer implemented in the device, there are two possible clock sources:

- 32-kHz clock (sourced from the LFOSC)
- System clock

For more information of the selection of the input clock source, see *Clocking*.

Note

Application software must ensure that DMTIMER bus interface clock frequency be greater than input clock frequency before accessing DMTIMER registers. Failure to do so will result in bus hang condition.

Each timer supports three functional modes:

- Timer mode
- Capture mode
- Compare mode

The capture and compare modes are disabled by default after core reset.

12.6.4.4.1 Timer Block Diagram

Figure 12-360 is a block diagram of the timers.

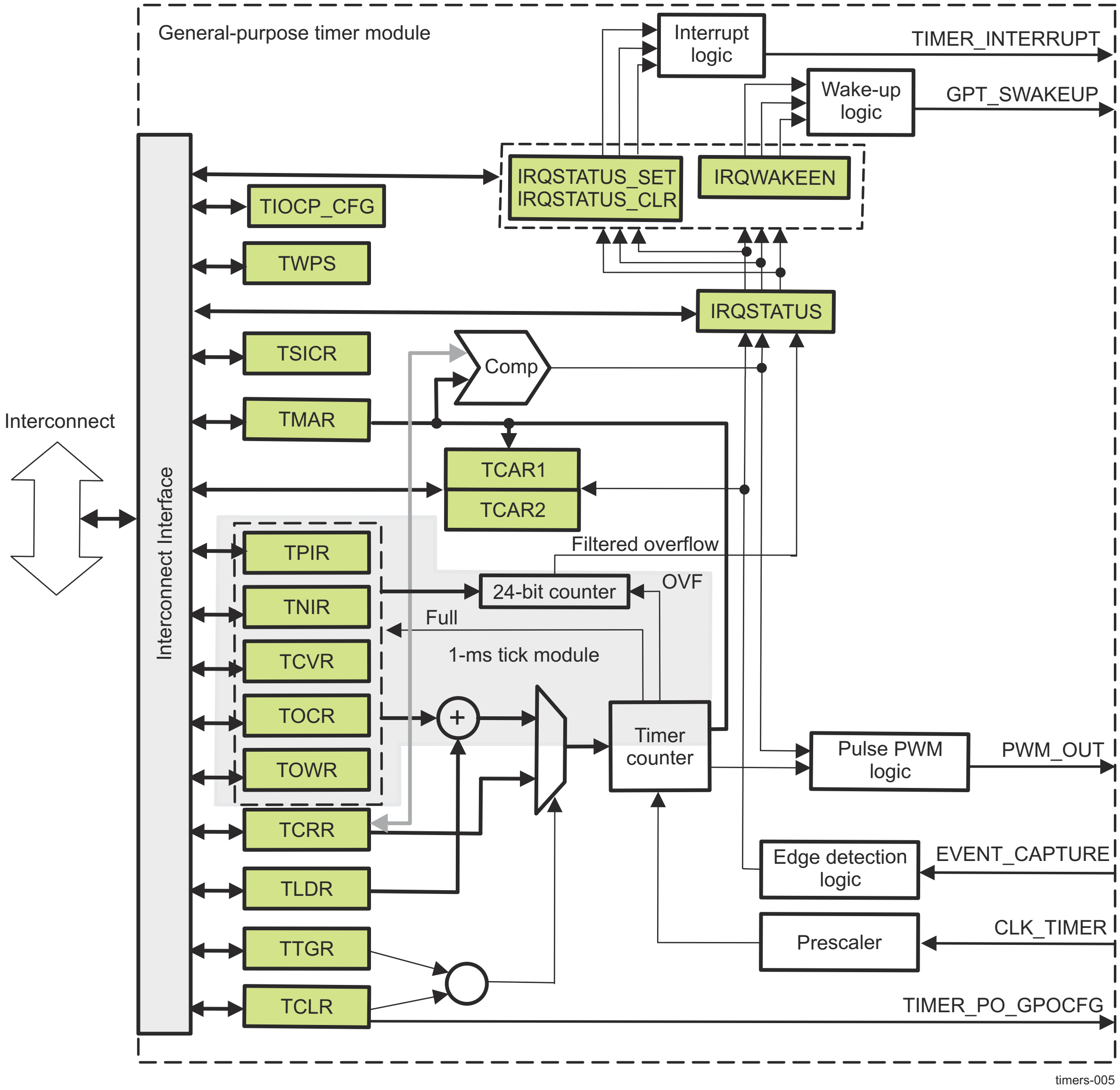


Figure 12-360. Timer Block Diagram

12.6.4.4.2 Timer Power Management

Note

Some of the timers features described in this section may not be supported on this family of devices. For more information, see *Module Integration* for specifics..

The way the timer acknowledges the LPSC clock stop request is configurable through the DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE bit field.

Table 12-314 lists the IDLEMODE settings and the related acknowledgment modes.

Table 12-314. IDLEMODE Settings

IDLEMODE Value	Selected Mode	Description
00	Force-idle	The clock stop request is unconditionally acknowledged from the timer, regardless of its internal operations. This mode must be used carefully, because it does not prevent the loss of data when the clock is switched off.
01	No-idle	The clock stop request is never acknowledged from the timer. This mode is safe from a module point of view but is not efficient from a power-saving perspective because the clocks remain active.

Table 12-314. IDLEMODE Settings (continued)

IDLEMODE Value	Selected Mode	Description
10	Smart-idle	The timer acknowledges the clock stop request, basing its decision on its internal activity. The acknowledge signal is asserted only when all pending transactions and interrupt requests are treated. This is the best approach to efficient system power management.
11	Smart-idleWakeup	The module behaves like in Smart-idle mode, with the exception, that it can issue a wake-up request in sleep mode, if the functional clock is not cut off.

12.6.4.4.2.1 Wake-Up Capability

Note

Some of the timers features described in this section may not be supported on this family of devices. For more information, see *Timers Not Supported Features*.

If the DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE bit field sets the smart-idle mode or smart-idle with wake-up mode, the timer evaluates its internal capability to have the interface clock switched off. When there is no further internal activity (no pending interrupt sources: match, overflow, or timer capture events), the clock stop acknowledge signal is asserted and the timer enters sleep mode, ready to issue a wake-up request if configured in smart-idle with wake-up mode.

Figure 12-361 shows the wake-up request generation.

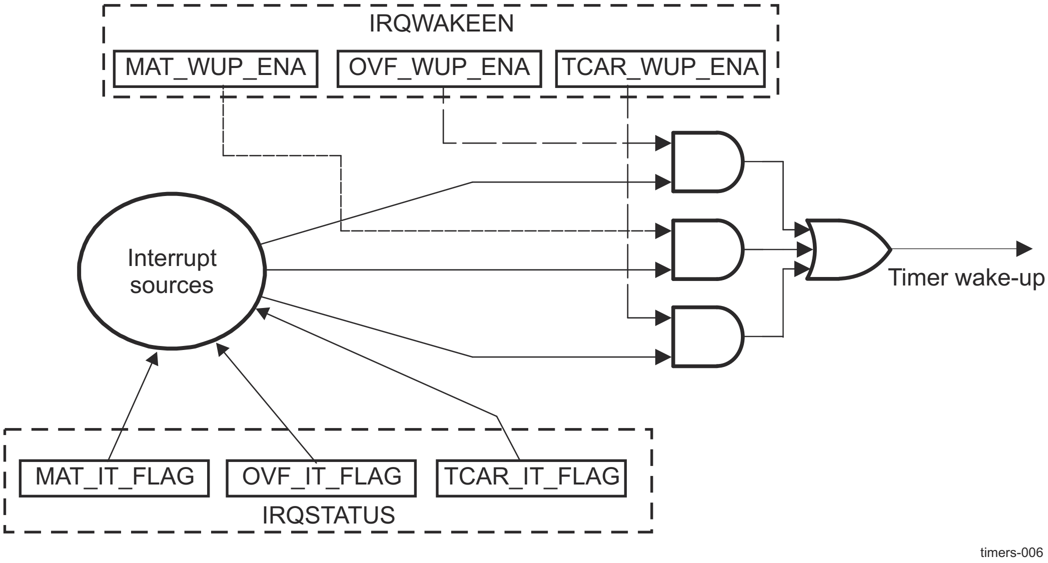


Figure 12-361. Wake-Up Request Generation

The timer wake-up-enable register allows masking of the expected source of the wake-up event that generates a wake-up request. The register is synchronously programmed with the interface clock before the Clock magagemet sends a clock stop request. The expected source of the wake-up event is an overflow (DMTIMER1MS_TCRR), a timer match (the compare result of DMTIMER1MS_TCRR and DMTIMER1MS_TMAR matches the counter value), and a timer capture (detection of an external pulse transition of the correct polarity on the TIMER_PIEVENTCAPT).

When the wake-up event is issued, the associated interrupt status bit is set in the timer status register (DMTIMER1MS_IRQSTATUS). The pending wake-up event is reset when the set status bit is overwritten with 1.

Note

The status bit must be reset to re-enter idle mode.

12.6.4.4.3 Timer Software Reset

DMTIMER1MS_TIOCP_CFG[0] SOFTRESET bit can initiate a software reset of the timer. This bit is autocleared to 0 when the reset is complete.

Before accessing or using the timer, the local host must ensure that internal reset is released by reading the DMTIMER1MS_TIOCP_CFG[0] SOFTRESET bit. This bit monitors the internal reset status.

12.6.4.4.4 Timer Interrupts

The timer can issue an overflow interrupt, a timer match interrupt, and a timer capture interrupt. Each internal interrupt source can be independently enabled and disabled in the interrupt-enable register (DMTIMER1MS_IRQSTATUS_SET) and disabled in the interrupt-disable register (DMTIMER1MS_IRQSTATUS_CLR). When the interrupt event is issued, the associated interrupt status bit is set in the timer status register (DMTIMER1MS_IRQSTATUS).

12.6.4.4.5 Timer Mode Functionality

The timer is an upward counter that can be started and stopped at any time through the timer control register (the DMTIMER1MS_TCLR[0] ST bit). The timer counter register (DMTIMER1MS_TCRR) can be loaded when stopped or on-the-fly (while counting). DMTIMER1MS_TCRR can be loaded directly by a DMTIMER1MS_TCRR write access with a new timer value. DMTIMER1MS_TCRR can also be loaded with the value held in the timer load register (DMTIMER1MS_TLDR) by a trigger register (DMTIMER1MS_TTGR) write access. The loading of DMTIMER1MS_TCRR is done regardless of the written value of DMTIMER1MS_TTGR. The value of DMTIMER1MS_TCRR can be read when stopped or captured on-the-fly by a DMTIMER1MS_TCRR read access. The timer is stopped and the counter value is set to 0 when the module reset is asserted. The timer is maintained at stop after the reset is released.

In one-shot mode (the DMTIMER1MS_TCLR[1] AR bit is set to 0), the counter is stopped after counting overflow occurs (the counter value remains at 0).

When the autoreload mode is enabled (the DMTIMER1MS_TCLR[1] AR bit is set to 1), DMTIMER1MS_TCRR is reloaded with the value of DMTIMER1MS_TLDR after a counting overflow occurs.

CAUTION

Do not put the overflow value (0xFFFF FFFF) in the DMTIMER1MS_TLDR register because it can lead to undesirable results.

An interrupt can be issued on overflow if the overflow interrupt-enable bit is set in the timer interrupt-enable register (the DMTIMER1MS_IRQSTATUS_SET[1] OVF_EN_FLAG bit is set to 1). A dedicated output pin (POTIMERPWM) can be programmed in the DMTIMER1MS_TCLR[12] PT bit through the DMTIMER1MS_TCLR[11-10] (PT and TRG bits) to generate one positive pulse (prescaler duration) or to invert the current value (toggle mode) when an overflow occurs. The DMTIMER1MS_TCLR[12] PT bit selects pulse/toggle modulation (the DMTIMER1MS_TCLR[11-10] TRG bit field selects trigger mode).

Figure 12-362 shows the DMTIMER1MS_TCRR timing value.

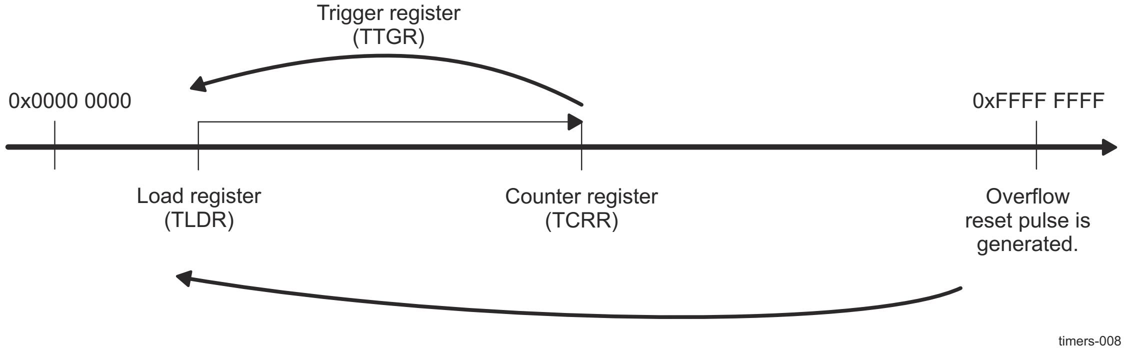


Figure 12-362. DMTIMER1MS_TCRR Timing Value

12.6.4.4.5.1 1-ms Tick Generation

The interrupt period is not exactly 1 ms, because the timer input clock is 32.768 kHz. If the clock counts up to 32, it obtains a 0.977-ms period; if it counts up to 33, it obtains a 1.007-ms period. For large granularity, the error is cumulative and can generate important deviations from the standard value.

To minimize the error between a true 1-ms tick and the tick generated by the 32.768-kHz timer, the sequencing of periods less than 1 ms and periods greater than 1 ms must be shuffled. An additional 1-ms block is used to correct this error. See Figure 12-363.

Note

The only available source for a 32.768-kHz clock is the LFOSC. The HFOSC is not capable of generating a true 32.788-kHz frequency.

In this implementation, the increment sequencing is automatically managed by the timer to minimize the error. The user must define only the value of the timer positive increment register (the DMTIMER1MS_TPIR[31-0] POSITIVE_INC_VALUE bit field) and the timer negative increment register (the DMTIMER1MS_TNIR[31-0] NEGATIVE_INC_VALUE bit field). An automatic adaptation mechanism is used to simplify the programming model.

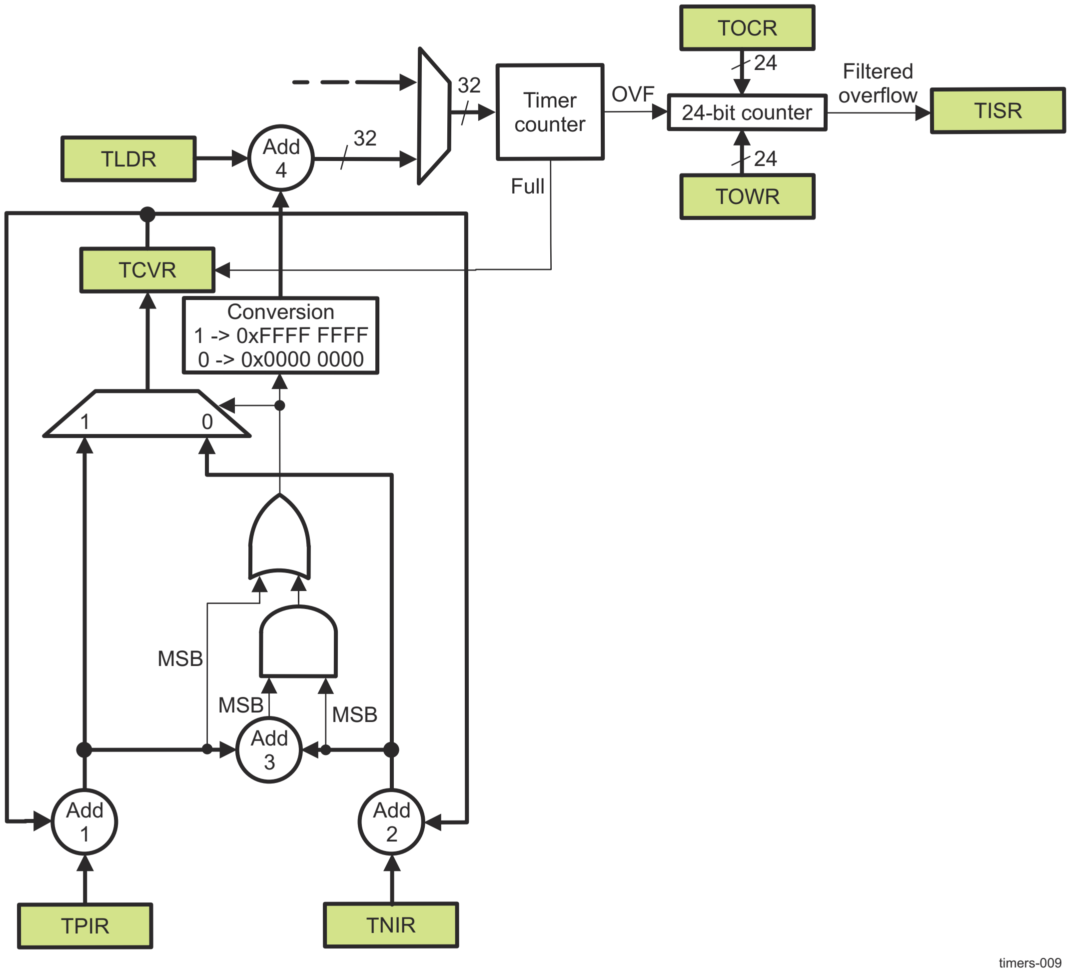


Figure 12-363. Block Diagram of the 1-ms Tick Module

The DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, and DMTIMER1MS_TCVR registers and adders Add1, Add2, and Add3 are used to define whether the next value loaded in the timer counter register (the DMTIMER1MS_TCRR[31-0] TIMER_COUNTER bit field) is the value of the DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field (period less than 1 ms) or the value of DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1 (period greater than 1 ms).

Table 12-315 lists the value loaded in the DMTIMER1MS_TCRR according to the sign of the result of Add1, Add2, and Add3.

MSB = 0: Positive value; MSB = 1: Negative value

Table 12-315. Value Loaded in DMTIMER1MS_TCRR to Generate 1-ms Tick

Add1 MSB	Add2 MSB	Add3 MSB	Value of DMTIMER1MS_TCRR Register
0	0	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	0	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	1	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE bit field
0	1	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1
1	0	0	N/A
1	0	1	N/A
1	1	0	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1
1	1	1	DMTIMER1MS_TLDR[31-0] LOAD_VALUE –1

The values of the DMTIMER1MS_TPIR and DMTIMER1MS_TNIR registers are calculated using the following formulas:

- Positive increment value = (INTEGER[F_{clk} × T_{tick}] + 1) × 1e6) – (F_{clk} × T_{tick} × 1e6)
- Negative increment value = (INTEGER[F_{clk} × T_{tick}] × 1e6) – (F_{clk} × T_{tick} × 1e6)

Note

F_{clk} clock frequency (kHz)

T_{tick} tick period (ms)

The timer overflow counter register (DMTIMER1MS_TOCR) and the timer overflow wrapping register (DMTIMER1MS_TOWR) are used to filter interrupts. When the timer overflows, it increments the 24-bit DMTIMER1MS_TOCR. When the values in the 24-bit DMTIMER1MS_TOCR match the values in the 24-bit DMTIMER1MS_TOWR and the timer overflow is asserted, the DMTIMER1MS_TOCR is reset and an interrupt is generated to the DMTIMER1MS_IRQSTATUS register.

Note

DMTIMER1MS_TOWR has to be set to requested value. For example, if no interrupt needs to be masked DMTIMER1MS_TOWR must be set to 0, if one interrupt needs to be masked DMTIMER1MS_TOWR must be set to 1, if two interrupts need to be masked DMTIMER1MS_TOWR must be set to 2 and so on.

It is important to have in mind that the case when FFFFFF interrupts need to be masked is not possible.

With the conversion block in reset state (the positive increment register, negative increment register, and counter value register are zeroed), the programming model and the behavior of timers remain unchanged.

For 1-ms tick with a 32.768-kHz clock:

- DMTIMER1MS_TPIR[31-0] POSITIVE_INC_VALUE = 232,000
- DMTIMER1MS_TNIR[31-0] NEGATIVE_INC_VALUE = –768,000
- DMTIMER1MS_TLDR[31-0] LOAD_VALUE = 0xFFFF FFE0

Note

Any value of the tick period can be generated with the appropriate value of the DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, and DMTIMER1MS_TLDR.

By default, the DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR and the associated logic are in reset mode (all 0s) and have no effect on the programming model.

12.6.4.4.6 Timer Capture Mode Functionality

When a transition is detected on the module input pin (PIEVENTCAPT), the timer value in the DMTIMER1MS_TCRR can be captured and saved in the DMTIMER1MS_TCAR1 or DMTIMER1MS_TCAR2 register function of the mode selected in the DMTIMER1MS_TCLR[13] CAPT_MODE bit. The edge detection circuitry monitors transitions on the input pin (PIEVENTCAPT).

The rising edge, falling edge, or both, can be selected in the DMTIMER1MS_TCLR[9-8] TCM bit field to trigger the timer counter capture. The module sets the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit when an active edge is detected, and at the same time, the counter value DMTIMER1MS_TCRR is stored in timer capture register DMTIMER1MS_TCAR1 or DMTIMER1MS_TCAR2, as follows:

- If the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 0, on the first enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR1 register, and the next events are ignored (no update on the DMTIMER1MS_TCAR1 register and no interrupt triggering) until the detection logic is reset or the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG is cleared by writing 1 to it.
- If the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 1, on the first enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR1 register, and on the second enabled capture event, the value of the counter register is saved in the DMTIMER1MS_TCAR2 register. If a capture interrupt is enabled, the interrupt triggers on the second event capture. All other events are ignored (no update on DMTIMER1MS_TCAR1/DMTIMER1MS_TCAR2 and no interrupt triggering) until the detection logic is reset or the DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit is cleared by writing 1 to it. This mechanism is useful for period calculation of a clock, if that clock is connected to the PIEVENTCAPT input pin.

The edge detection logic is reset (a new capture is enabled) when the active capture interrupt is served. The DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG bit is cleared by writing 1 to it or when the edge detection mode bits (the DMTIMER1MS_TCLR[9-8] TCM bit field) are changed from no-capture mode detection to any other mode. The timer functional clock (input to prescaler) is used to sample the input pin (PIEVENTCAPT). A negative or positive pulse input can be detected when the pulse time is greater than the functional clock period. An interrupt is issued on edge detection if the capture interrupt-enable bit is set in the DMTIMER1MS_IRQSTATUS_SET[2] TCAR_EN_FLAG bit. See the examples in Figure 12-364 and Figure 12-365.

In Figure 12-364, the value of the DMTIMER1MS_TCLR[9-8] TCM bit field is 1h, and the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 0. Only the rising edge of PIEVENTCAPT triggers a capture in the DMTIMER1MS_TCAR1 and DMTIMER1MS_TCAR2 registers, and only the DMTIMER1MS_TCAR1 register updates.

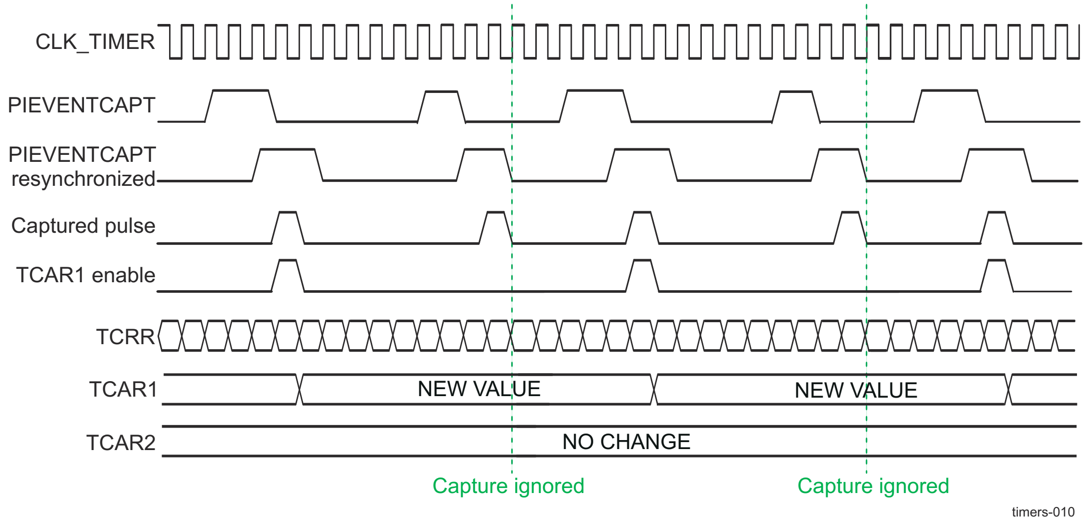


Figure 12-364. Capture Wave Example for DMTIMER1MS_TCLR[13] CAPT_MODE = 0

In Figure 12-365, the value of the DMTIMER1MS_TCLR[9-8] TCM bit field is 1h, and the DMTIMER1MS_TCLR[13] CAPT_MODE bit is 1. Only the rising edge of PIEVENTCAPT triggers a capture in the DMTIMER1MS_TCAR1 register on the first enabled event, and the DMTIMER1MS_TCAR2 register updates on the second enabled event.

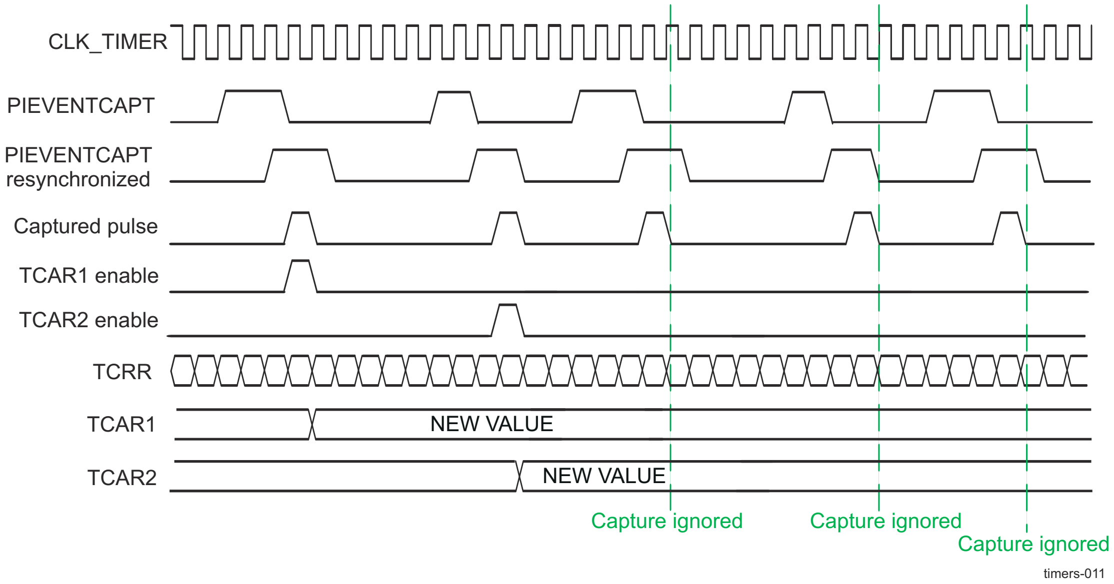


Figure 12-365. Capture Wave Example for DMTIMER1MS_TCLR[13] CAPT_MODE = 1

12.6.4.4.7 Timer Compare Mode Functionality

When the compare-enable register DMTIMER1MS_TCLR[6] CE bit is set to 1, the timer value (the DMTIMER1MS_TCRR[31-0] TIMER_COUNTER bit field) is continuously compared to the value held in the timer match register (DMTIMER1MS_TMAR). The value of the DMTIMER1MS_TMAR[31-0] COMPARE_VALUE bit field can be loaded at any time (timer counting or stopped). When the DMTIMER1MS_TCRR and the DMTIMER1MS_TMAR values match, an interrupt is issued, if the DMTIMER1MS_IRQSTATUS_SET[0] MAT_EN_FLAG bit is set.

To prevent any unwanted interrupts due to reset value matching effect, write a compare value to the DMTIMER1MS_TMAR before setting the DMTIMER1MS_TCLR[6] CE bit.

The dedicated output pin (POTIMERPWM) can be programmed in the DMTIMER1MS_TCLR[12] PT bit through the DMTIMER1MS_TCLR[11-10] TRG bit field to generate one positive pulse (timer clock duration) or to invert the current value (toggle mode) when an overflow or a match occurs.

12.6.4.4.8 Timer Prescaler Functionality

A prescaler can be used to divide the timer counter input clock frequency. The prescaler is enabled when the DMTIMER1MS_TCLR[5] PRE bit is set. The DMTIMER1MS_TCLR[4-2] PTV bit field sets the 2^n division ratio (prescaler value is $2^{(PTV + 1)}$). The prescaler counter is reset when the timer counter is stopped or reloaded on-the-fly.

Table 12-316 lists the prescaler/timer reload values versus contexts.

Table 12-316. Prescaler/Timer Reload Values Versus Contexts

Context	Prescaler	Timer Counter
Overflow (when autoreload is on)	Reset	DMTIMER1MS_TLDR[31-0]
DMTIMER1MS_TCRR write	Reset	DMTIMER1MS_TCRR[31-0]
DMTIMER1MS_TTGR write	Reset	DMTIMER1MS_TLDR[31-0]
Stop	Reset	Frozen

12.6.4.4.9 Timer Pulse-Width Modulation

The timer can be configured to provide a programmable PWM output. The timer PWM (POTIMERPWM) output pin can be configured to toggle on an event. The DMTIMER1MS_TCLR[11-10] TRG bit field determines on which register value the PWM pin toggles. Either overflow or both overflow and match can be selected to toggle the timer PWM pin when a compare condition occurs.

Note

In toggle mode, when DMTIMER1MS_TCLR[11-10] TRG = 0x2 (overflow and match), the first event that toggles the PWM line is an overflow event.

The DMTIMER1MS_TCLR[7] SCPWM bit can be programmed to set or clear the timer PWM output signal only while the counter is stopped or the trigger is off. This allows setting the output pin to a known state before modulation starts. Modulation synchronously stops when the DMTIMER1MS_TCLR[11-10] TRG bit field is cleared and overflow occurs. This allows fixing a deterministic state of the output pin when modulation stops.

In Figure 12-366, the internal overflow pulse is set each time the (0xFFFF FFFF – DMTIMER1MS_TLDR[31-0] LOAD_VALUE + 1) value is reached, and the internal match pulse is set when the counter reaches the value of DMTIMER1MS_TMAR. Depending on the value of the DMTIMER1MS_TCLR[12] PT bit and DMTIMER1MS_TCLR[11-10] TRG bit field, the timer provides pulse or PWM event on the output pin (POTIMERPWM).

The DMTIMER1MS_TLDR and DMTIMER1MS_TMAR must keep values below the overflow value (0xFFFF FFFF) by at least two units. If the PWM trigger events are both overflow and match, the difference between the values kept in the DMTIMER1MS_TMAR and the value in the DMTIMER1MS_TLDR must be at least two units. When match event is used, the compare mode DMTIMER1MS_TCLR[6] CE bit must be set.

In Figure 12-366, the DMTIMER1MS_TCLR[7] SCPWM bit is set to 0. In Figure 12-367, the DMTIMER1MS_TCLR[7] SCPWM bit is set to 1. To obtain the desired wave form, start the counter at 0xFFFF FFFE value (to ensure an overflow first) or adjust the line polarity (DMTIMER1MS_TCLR[7] SCPWM bit).

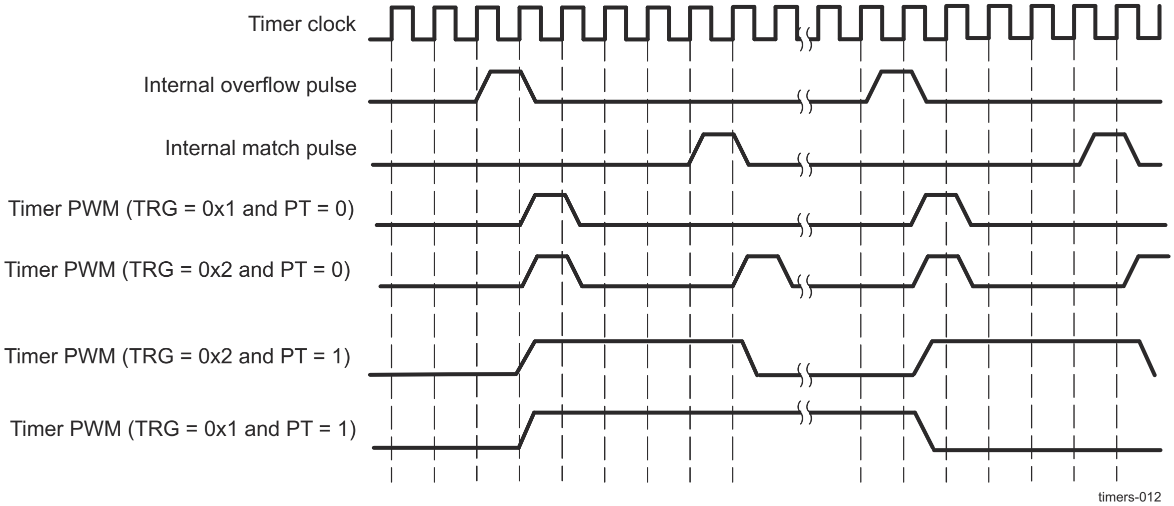


Figure 12-366. Timing Diagram of PWM With DMTIMER1MS_TCLR[7] SCPWM Bit = 0

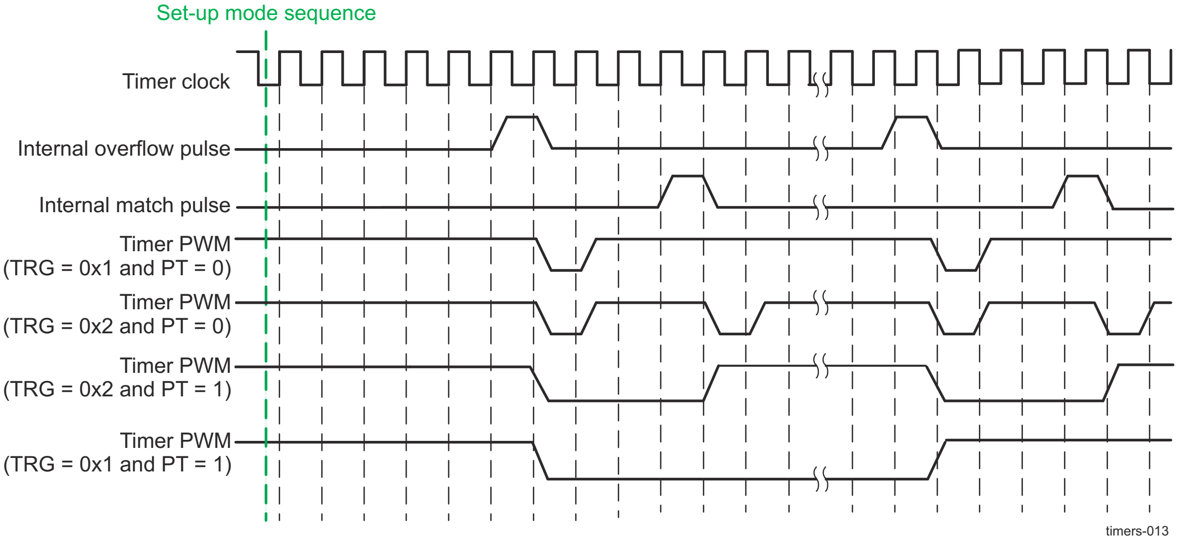


Figure 12-367. Timing Diagram of PWM With DMTIMER1MS_TCLR[7] SCPWM Bit = 1

12.6.4.4.10 Timer Counting Rate

The timer rate is defined by the following values:

- Value of the prescaler fields (the DMTIMER1MS_TCLR[5] PRE bit and DMTIMER1MS_TCLR[4-2] PTV bit field)
- Value loaded into the DMTIMER1MS_TLDR

Table 12-317 lists the prescaler clock ratio values.

Table 12-317. Prescaler Clock Ratio Values

DMTIMER1MS_TCLR[5] PRE	DMTIMER1MS_TCLR[4-2] PTV	Divisor (PS)
0	X	1
1	0	2
1	1	4
1	2	8
1	3	16
1	4	32
1	5	64
1	6	128

Table 12-317. Prescaler Clock Ratio Values (continued)

DMTIMER1MS_TCLR[5] PRE	DMTIMER1MS_TCLR[4-2] PTV	Divisor (PS)
1	7	256

Thus, the timer overflow rate is expressed as:

OVF_Rate = (0xFFFF FFFF – DMTIMER1MS_TLDR + 1) × (timer-functional clock period) × PS

With (timer-functional clock period) = 1/(timer-functional clock frequency) and PS = $2^{(PTV + 1)}$ if prescaler is enabled, or PS = 1 if prescaler is disabled.

CAUTION

Internal resynchronization causes any write to the DMTIMER1MS_TCLR[1] ST bit to have some latency before the register is updated:

2.5 × functional clock cycles write_DMTIMER1MS_TCLR_latency 3.5 × functional clock cycles

Remember to consider this latency whenever the timer must be started or stopped by a software change to the DMTIMER1MS_TCLR[1] ST bit.

CAUTION

- In non-PWM mode, DMTIMER1MS_TLDR must be maintained at less than or equal to 0xFFFF FFFE.
- In PWM mode, DMTIMER1MS_TLDR must be maintained at less than or equal to 0xFFFF FFFD.

For example, with a timer clock input of 32 kHz and the DMTIMER1MS_TCLR[5] PRE bit set to 0, the timer output period is as listed in Table 12-318.

Table 12-318. Value and Corresponding Interrupt Period

DMTIMER1MS_TLDR[31-0] LOAD_VALUE	Interrupt Period
0x0000 0000	37 h
0xFFFF 0000	2 s
0xFFFF FFF0	500 µs
0xFFFF FFFE	62.5 µs

12.6.4.4.11 Timer Under Emulation

During emulation mode, the timer continues to run according to the value of the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit.

If the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit is set to 1, timer execution is not stopped in emulation mode and the interrupt is still generated when overflow or match is reached.

If the DMTIMER1MS_TIOCP_CFG[1] EMUFREE bit is set to 0, the prescaler and timer are frozen and both resume on exit from emulation mode. The asynchronous external input pin (MCU_TIMER_IO[9-0] or TIMER_IO[7-0]) is internally synchronized on two timer-clock rising edges.

12.6.4.4.12 Accessing Timer Registers

All accesses are posted mode, under the assumption that freq(timer clock) < freq(interface clock)/4, until software reconfiguration. In addition, it is not recommended to access the timer registers prior to the PLLs generating the timer and interface clocks have been configured and the clocks have stabilized. All registers are 32 bits wide, accessible through the configuration interface with 32-bit access (read/write).

Write operations to the following functional registers must be complete (the MSB must be written even if the MSB data is not used):

- DMTIMER1MS_TCLR
- DMTIMER1MS_TCRR

- DMTIMER1MS_TLDR
- DMTIMER1MS_TTGR
- DMTIMER1MS_TMAR
- DMTIMER1MS_TPIR
- DMTIMER1MS_TNIR
- DMTIMER1MS_TCVR
- DMTIMER1MS_TOCR
- DMTIMER1MS_TOWR

The following registers are not affected by the posted/nonposted mode selection; the write/read operation is effective and acknowledged (command accepted) after one interface clock cycle from command assertion:

- DMTIMER1MS_TIDR
- DMTIMER1MS_TIOCP_CFG
- DMTIMER1MS_IRQSTATUS
- DMTIMER1MS_IRQSTATUS_RAW
- DMTIMER1MS_IRQSTATUS_SET
- DMTIMER1MS_IRQSTATUS_CLR
- DMTIMER1MS_IRQWAKEEN
- DMTIMER1MS_TWPS
- DMTIMER1MS_TSICR

12.6.4.4.12.1 Writing to Timer Registers

The host uses the configuration interface to write to the following registers synchronously with the timer interface clock:

- DMTIMER1MS_TLDR
- DMTIMER1MS_TCRR
- DMTIMER1MS_TCLR
- DMTIMER1MS_TIOCP_CFG
- DMTIMER1MS_IRQSTATUS
- DMTIMER1MS_IRQSTATUS_SET
- DMTIMER1MS_IRQSTATUS_CLR
- DMTIMER1MS_IRQWAKEEN
- DMTIMER1MS_TTGR
- DMTIMER1MS_TSICR
- DMTIMER1MS_TMAR
- DMTIMER1MS_TPIR
- DMTIMER1MS_TNIR
- DMTIMER1MS_TCVR
- DMTIMER1MS_TOCR
- DMTIMER1MS_TOWR

12.6.4.4.12.1.1 Write Posting Synchronization Mode

This mode is used if the DMTIMER1MS_TSICR[2] POSTED bit is set to 1 (default value).

This mode uses a posted write scheme to update any internal register (DMTIMER1MS_TCLR, DMTIMER1MS_TCRR, DMTIMER1MS_TLDR, DMTIMER1MS_TTGR, DMTIMER1MS_TMAR, DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR). Therefore, the write transaction is immediately acknowledged on the configuration interface, although the effective write operation occurs later because of a resynchronization in the timer clock domain. The advantage is that neither the interconnect, nor the device that requested the write transaction is stalled.

For each register, a status bit is provided in the timer write-posted status (DMTIMER1MS_TWPS) register. In this mode, it is mandatory that software check this status bit before any write access. If a write is attempted to a register with a previous access pending, the previous access is discarded without notice.

The timer module updates the value of the timer counter register synchronously with the interface clock. Consequently, any read access to DMTIMER1MS_TCRR does not add any resynchronization latency; the current value is always available.

Note

Because the overflow IRQ is generated when the value of DMTIMER1MS_TCRR reaches 0xFFFF FFFF, and not when it changes its value to the value after overflow, it is necessary to wait a delay of (1 × PS × timer functional clock period) before any read access to DMTIMER1MS_TCRR to ensure a correct reading of its content.

Note

If DMTIMER1MS_TTGR register is written during a posted write to DMTIMER1MS_TCRR, the value to be written to DMTIMER1MS_TCRR will be discarded.

If a posted write to DMTIMER1MS_TCVR is started, the user must not write to DMTIMER1MS_TPIR or DMTIMER1MS_TNIR before the DMTIMER1MS_TCVR write is finished, because the value of DMTIMER1MS_TCVR is re-evaluated, so both the value to be written, and the recalculated value will be discarded.

If a write access is pending for a register, reading from this register does not yield a correct result. Software synchronization must be used to avoid incorrect results.

Functional frequency range: freq(timer clock) < freq(interface clock)/4.

12.6.4.4.12.1.2 Write Nonposting Synchronization Mode

This mode is used if the DMTIMER1MS_TSICR[2] POSTED bit is set to 0. It uses a nonposted write scheme to update any internal register. Therefore, the write transaction is not acknowledged on the configuration interface until the effective write operation occurs after the resynchronization in the timer functional clock domain. The drawback is that the interconnect and the device that requested the write transaction are stalled during this period.

The same full resynchronization scheme is used for a read transaction, and the same stall period applies. A register read following a write to the same register is always coherent.

This mode is functional regardless of the ratio between the configuration interface frequency and the timer clock frequency.

12.6.4.4.12.2 Reading From Timer Counter Registers

Note

LSB/MSB accesses cannot be interleaved (that is, the sequence LSB register 1, LSB register 2, MSB register 1, MSB register 2 is not supported).

The DMTIMER1MS_TCRR is a 32-bit “atomic datum” and its 16-bit capture is done on the 16-bit LSB first to allow atomic LSB16 + MSB16 capture. This capture scheme is also performed for the DMTIMER1MS_TCAR1 and DMTIMER1MS_TCAR2 registers as they can be changed due to internal processes too.

12.6.4.4.12.2.1 Read Posted

This mode is functional regardless of the ratio between the configuration interface frequency and the functional clock frequency. The recommended functional frequency range is freq(timer) < freq(interface clock)/4.

Read posted mode is used if DMTIMER1MS_TSICR[2] POSTED = 0x1 or DMTIMER1MS_TSICR[3] READ_MODE is set to 0. This mode uses a posted-read scheme for reading any internal timer register. The read transaction is immediately acknowledged on the configuration interface, prior to the value to be read has been resynchronized. With this method, neither the interconnect nor the device that requested the read transaction are stalled.

Read posted mode applies to DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR, which needs resynchronization from functional to interface clock domains.

Note that in Posted mode, if the DMTIMER1MS_TCRR is read immediately after wake-up and the interface clock is off during idle state, then it is possible to get an old value from just before going to idle state due to the fact the interface clock is needed for synchronization.

In order to avoid this situation, another synchronization mechanism is used for the first read operation after idle state. The DMTIMER1MS_TSICR[4] READ_AFTER_IDLE bit is used to enable/disable the mechanism.

When the synchronization mechanism is disabled (READ_AFTER_IDLE bit is set to 1), first read transaction takes only 2 interface clock cycles, but the read value of DMTIMER1MS_TCRR could be wrong.

When the synchronization mechanism is enabled (READ_AFTER_IDLE bit is set to 0), first read value of DMTIMER1MS_TCRR is correct, but the read transaction takes more than 2 interface clock cycles.

12.6.4.4.12.2.2 Read Non-Posted

This mode is functional regardless of the ratio between the configuration interface frequency and the functional clock frequency. Recommended functional frequency range is freq(timer) >= freq(interface clock)/4.

Read non-posted mode is used if DMTIMER1MS_TSICR[2] POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x1. This mode uses a non-posted read scheme for reading internal timer registers. The read transaction is not acknowledged on the configuration interface until the effective read operation occurs, after the resynchronization in the timer clock domain. The result is that both the interconnect and the device that requested the read transaction are stalled during this period.

This mode applies to DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR, which need resynchronization from functional to interface clock domains.

12.6.4.4.13 Timer Posted Mode Selection

A choice between two synchronization modes is made taking into account the frequency ratio and the stall periods that can be supported by the system, without impacting the global performance.

The posted mode selection applies only to registers that require synchronization on or from the timer clock domain. For write operation, the registers affected by posted and non-posted selection are DMTIMER1MS_TCLR, DMTIMER1MS_TLDR, DMTIMER1MS_TCRR, DMTIMER1MS_TTGR, DMTIMER1MS_TMAR, DMTIMER1MS_TPIR, DMTIMER1MS_TNIR, DMTIMER1MS_TCVR, DMTIMER1MS_TOCR, and DMTIMER1MS_TOWR. For read operation, the registers affected by this selection are: DMTIMER1MS_TCRR, DMTIMER1MS_TCAR1, DMTIMER1MS_TCAR2, DMTIMER1MS_TCVR, and DMTIMER1MS_TOWR.

The interface clock domain synchronous registers DMTIMER1MS_TIDR, DMTIMER1MS_TIOCP_CFG, DMTIMER1MS_IRQSTATUS, DMTIMER1MS_IRQSTATUS_SET, DMTIMER1MS_IRQWAKEEN, DMTIMER1MS_TWPS, and DMTIMER1MS_TSICR are not affected by posted and non-posted mode selection. The operation (read or write) is effective and acknowledged after one interface clock cycle from the command assertion.

The configuration of posted or non-posted mode can be changed (overwritten) by software by writing in DMTIMER1MS_TSICR[2] POSTED bit. The DMTIMER1MS_TSICR[3] READ_MODE defines how the read operation is performed when the module is configured in non-posted mode (see DMTIMER1MS_TSICR). The following cases are possible:

- DMTIMER1MS_TSICR[2] POSTED = 0x1 and DMTIMER1MS_TSICR[3] READ_MODE = x (don’t care): read and write operations are expected in posted mode.
- DMTIMER1MS_TSICR[2] POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x0: the write operation is executed in non-posted mode and read is executed in posted mode.
- DMTIMER1MS_TSICR[2]POSTED = 0x0 and DMTIMER1MS_TSICR[3] READ_MODE = 0x1: write is executed in non-posted mode and read is executed in non-posted mode.

12.6.4.5 Timers Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

12.6.4.5.1 Timer Global Initialization

12.6.4.5.1.1 Main Sequence – Timer Module Global Initialization

Table 12-319 identifies the main steps for initializing the timer module when the module is to be used for the first time.

Table 12-319. Timer Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	DMTIMER1MS_TIOCP_CFG[0] SOFTRESET	0x1
Wait until reset release?	DMTIMER1MS_TIOCP_CFG[0] SOFTRESET	0x0
Configure idle mode.	DMTIMER1MS_TIOCP_CFG[3-2] IDLEMODE	0x-
Enable wake-up interrupt events.	DMTIMER1MS_IRQWAKEEN[2-0]	0x-
Select posted mode.	DMTIMER1MS_TSICR[2] POSTED	0x-

12.6.4.5.2 Timer Operational Mode Configuration

12.6.4.5.2.1 Timer Mode

12.6.4.5.2.1.1 Main Sequence – Timer Mode Configuration

Table 12-320 lists the steps in the timer mode configuration.

Table 12-320. Timer Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Enable overflow interrupt.	DMTIMER1MS_IRQSTATUS_SET[1] OVF_EN_FLAG	0x1
Load timer counter value.	DMTIMER1MS_TCRR	0x-
Load timer load value.	DMTIMER1MS_TLDR	0x-
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.6.4.5.2.2 Timer Compare Mode

12.6.4.5.2.2.1 Main Sequence – Timer Compare Mode Configuration

Table 12-321 lists the steps in the timer compare mode configuration.

Table 12-321. Timer Compare Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Enable match interrupt.	DMTIMER1MS_IRQSTATUS_SET[0] MAT_EN_FLAG	0x1
Load timer counter value.	DMTIMER1MS_TCRR	0x-
Load timer compare value.	DMTIMER1MS_TMAR	0x-
Enable compare mode.	DMTIMER1MS_TCLR[6] CE	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.6.4.5.2.3 Timer Capture Mode

12.6.4.5.2.3.1 Main Sequence – Timer Capture Mode Configuration

Table 12-322 lists the steps in the timer capture mode configuration.

Table 12-322. Timer Capture Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Initialize capture mode.	See Section 12.6.4.5.2.3.2.	
Enable capture interrupt.	DMTIMER1MS_IRQSTATUS_SET[2] TCAR_EN_FLAG	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1
Detect event.	See Section 12.6.4.5.2.3.3.	

12.6.4.5.2.3.2 Subsequence – Initialize Capture Mode

Table 12-323 lists the steps to initialize capture mode.

Table 12-323. Initialize Capture Mode

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Select TIMER[11-0] or MCU_TIMER[3-0] Capture input at device pins TIMER_IO[11-0] for TIMER[11-0] or at pins MCU_TIMER_IO[3-0] for MCU_TIMER[3-0].	DMTIMER1MS_TCLR[14] GPO_CFG	0x1
Select single or second event capture.	DMTIMER1MS_TCLR[13] CAPT_MODE	0x-
Select transition capture mode.	DMTIMER1MS_TCLR[9-8] TCM	0x-

12.6.4.5.2.3.3 Subsequence – Detect Event

Table 12-324 lists the steps in detecting an event.

Table 12-324. Detect Event

Step	Register/Bit Field/Programming Model	Value
Wait until event detected?	DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG	= 0x1
Read timer capture value.	DMTIMER1MS_TCAR1 and/or DMTIMER1MS_TCAR2	
Clear capture interrupt request.	DMTIMER1MS_IRQSTATUS[2] TCAR_IT_FLAG	0x1

12.6.4.5.2.4 Timer PWM Mode

12.6.4.5.2.4.1 Main Sequence – Timer PWM Mode Configuration

Table 12-325 lists the steps in the timer PWM mode configuration.

Table 12-325. Timer PWM Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	DMTIMER1MS_TCLR[1] AR	0x-
Set prescale timer value.	DMTIMER1MS_TCLR[4-2] PTV	0x-
Enable prescaler.	DMTIMER1MS_TCLR[5] PRE	0x1
Select trigger output mode.	DMTIMER1MS_TCLR[11-10] TRG	0x-
Select pulse or toggle modulation PWM mode.	DMTIMER1MS_TCLR[12] PT	0x-
Select TIMER[11-0] or MCU_TIMER[3-0] PWM output at device pins TIMER_IO[11-0] for TIMER[11-0] or at pins MCU_TIMER_IO[3-0] for MCU_TIMER[3-0].	DMTIMER1MS_TCLR[14] GPO_CFG	0x0
Configure PWM output pin default value.	DMTIMER1MS_TCLR[7] SCPWM	0x-
Load timer load value.	DMTIMER1MS_TLDR	0x-
Load timer compare value.	DMTIMER1MS_TMAR	0x-
Enable compare.	DMTIMER1MS_TCLR[6] CE	0x1
Start the timer.	DMTIMER1MS_TCLR[0] ST	0x1

12.7 Internal Diagnostics Modules

This section describes the internal diagnostics modules in the device.

12.7.1 Dual Clock Comparator (DCC)

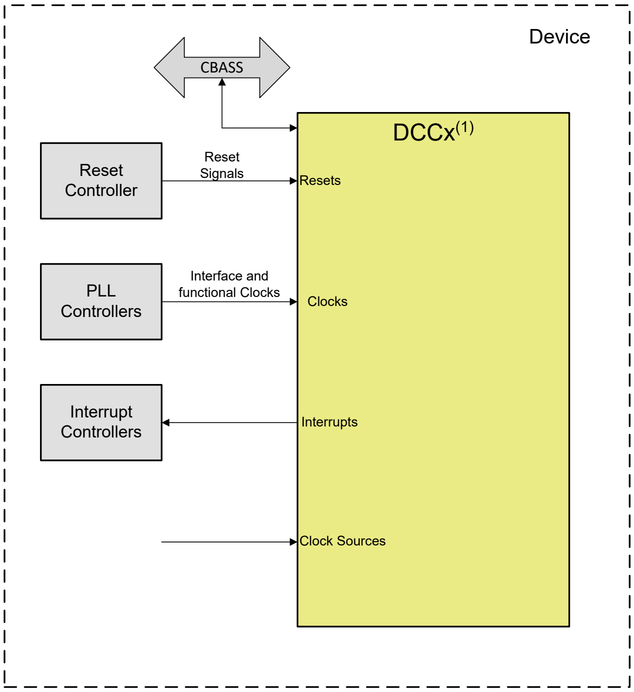
This section describes the Dual Clock Comparator (DCC) modules in the device.

12.7.1.1 DCC Overview

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

The device has instances of DCC modules.

Figure 12-368 shows the DCC modules overview.



1. x represents a valid instance of UART in a domain. See the device data sheet for valid domains and instances.

Figure 12-368. DCC Modules Overview

12.7.1.1.1 DCC Features

The DCC uses two independent clock sources to detect when one is out of specification. Each DCC module implements the following features:

- Two independent counter blocks count clock pulses from each clock source
- Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
- Configurable timebase for error signal
- Error signal generation when one of the clocks is out of specification
- Clock frequency measurement

12.7.1.1.2 Unsupported Features

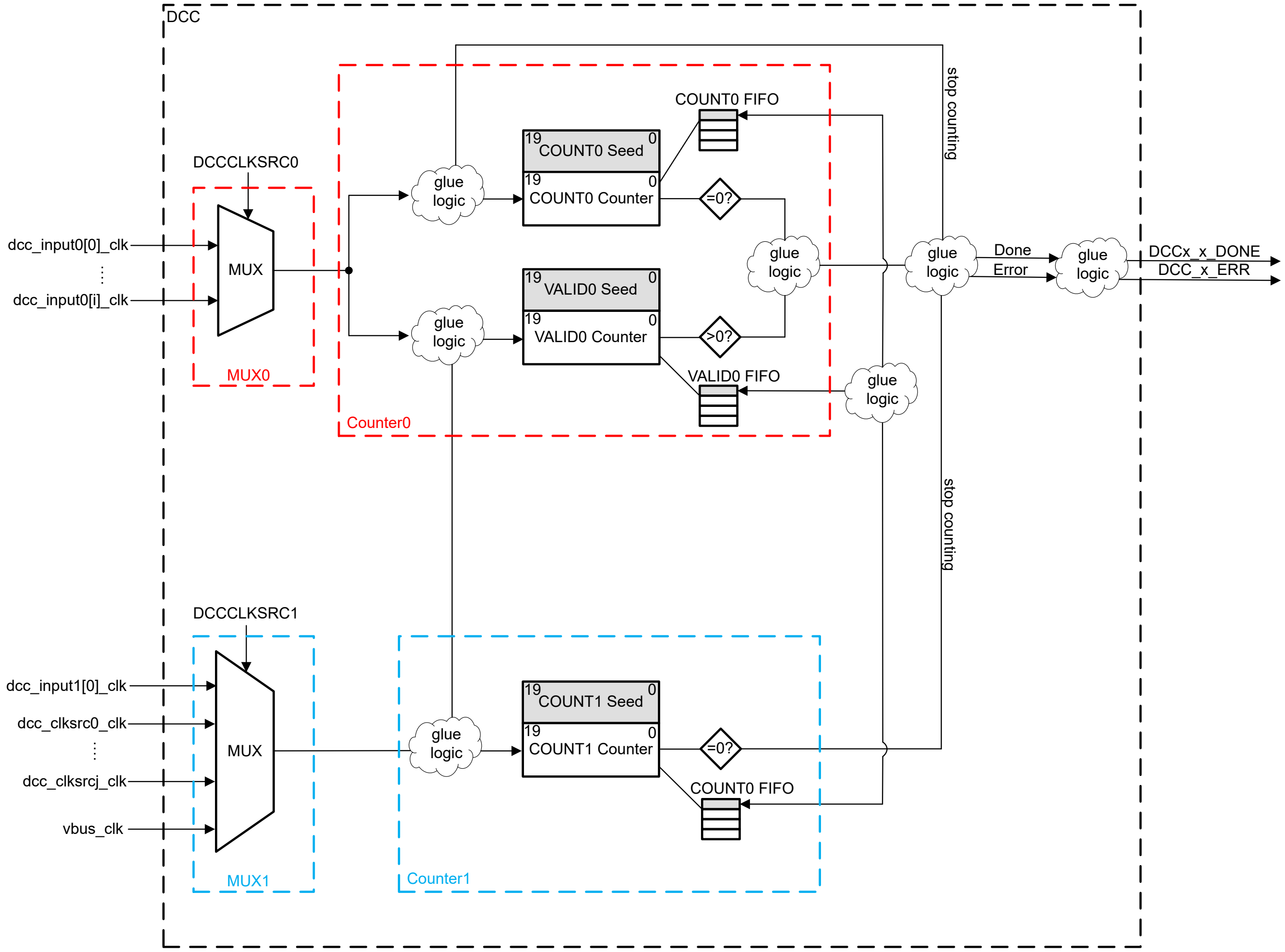
See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.7.1.2 DCC Functional Description

The DCC module supports two selectable clock sources for Counter0 and Counter1. Figure 12-369 shows the DCC functional block diagram.



i represents a valid clock input into DCCCLKSRC0, see the Module Integration Section for valid clock signals.
j represents a valid clock input into DCCCLKSRC1, see the Module Integration Section for valid clock signals.

Figure 12-369. DCC Functional Block Diagram

12.7.1.2.1 DCC Counter Operation

Note

For detailed DCC compute calculations, refer to Continuous Monitor of the PLL Frequency With the DCC App Note.

The DCC has two parallel counters that count clock pulses for two independent clock sources:

- Counter0 generates a fixed-width counting window (VALID0) after a pre-programmed number of pulses (COUNT0). The values for VALID0 and COUNT0 can be programmed in DCC2_DCCVALIDSEED0 and DCC2_DCCCNTSEED0 registers respectively.
- Counter1 generates a fixed-width pulse (1 cycle) after a pre-programmed number of pulses (COUNT1). This pulse sets an error signal if Counter1 does not reach 0 during the time when VALID0 is running. The seed value for COUNT1 can be programmed in DCC2_DCCCNTSEED1 register.

The error signal is generated by any one of the following conditions:

- Clock1 expires before the COUNT0 reaches 0.

- Clock1 expires after both COUNT0 and VALID0 reach 0.
- Clock1 not present.
- Clock0 not present.

Any of these errors causes the counters to stop counting. An application must then read out the counter values to determine what caused the error. Once the error is detected, the counters are stopped after 3 FICLK and 2 source clock cycles due to the cross clock domain synchronisation.

Reloads or restarts occur under two conditions:

- The module is reset or restarted through software (that is, software starts the module after reset, or software checks an error condition and decides to restart the module).
- COUNT0, COUNT1, and VALID0 all reach 0 without error.

CAUTION

The DCC module does not check jitter for Clock0 or Clock1.

As the counter preset signal is synchronized to either of the source clock domains, the counters begin downcounting after two corresponding source clock cycles.

The error signal is captured to the FICLK domain. There is 1 FICLK period uncertainty on either side of the fixed width counting window (VALID0) in generating the error signal since the counters work in different clock domains. This should be accounted for when setting the count value for VALID0.

Figure 12-370 through Figure 12-374 shows examples of counters relationship and error generation.

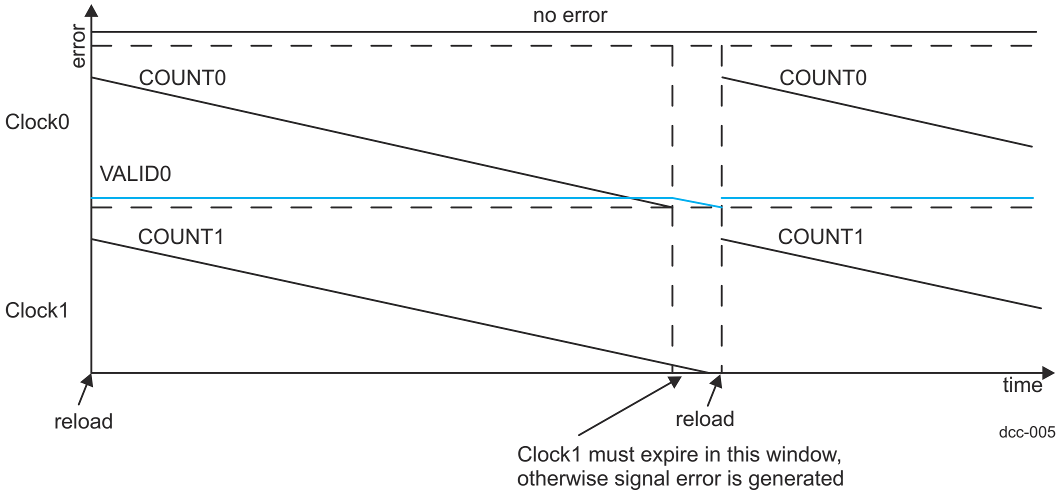


Figure 12-370. DCC Clock0 and Clock1 With no Error

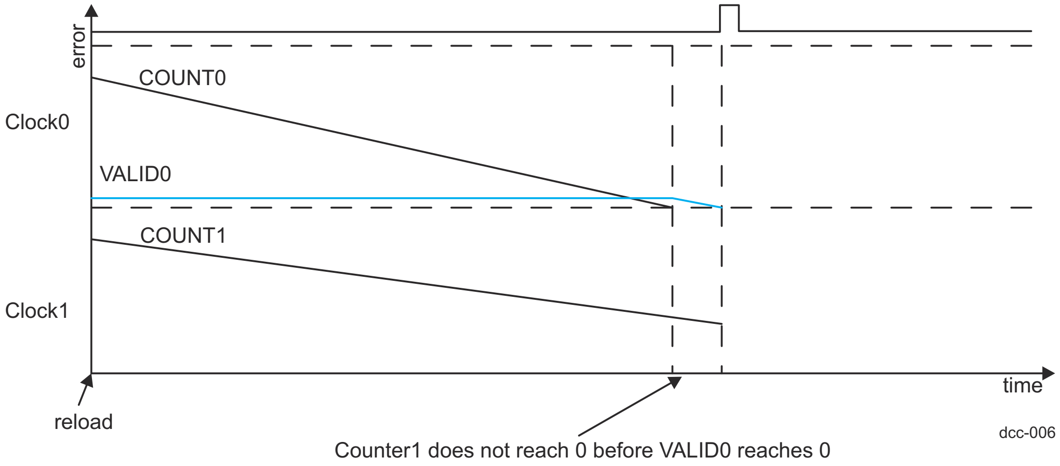


Figure 12-371. DCC Clock1 slower than Clock0 results in an error and stops counting

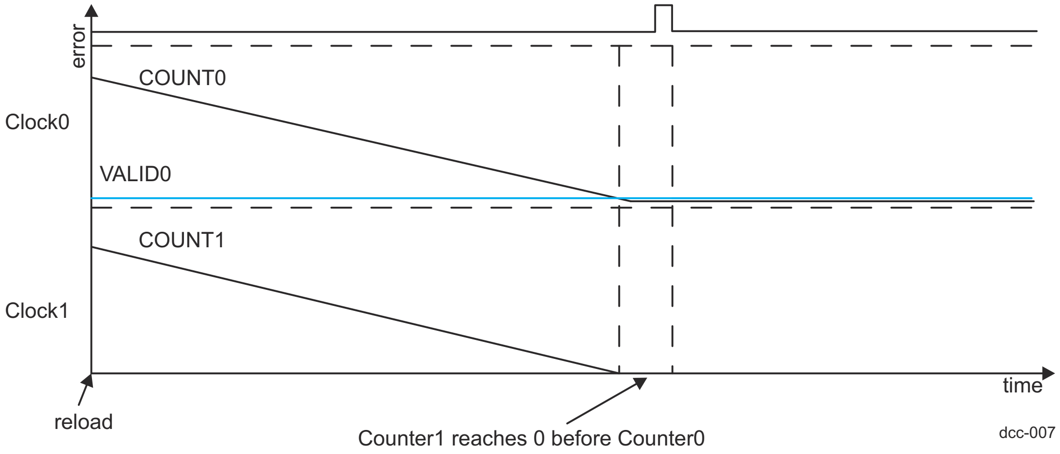


Figure 12-372. DCC Clock1 faster than Clock0 results in an error and stops counting

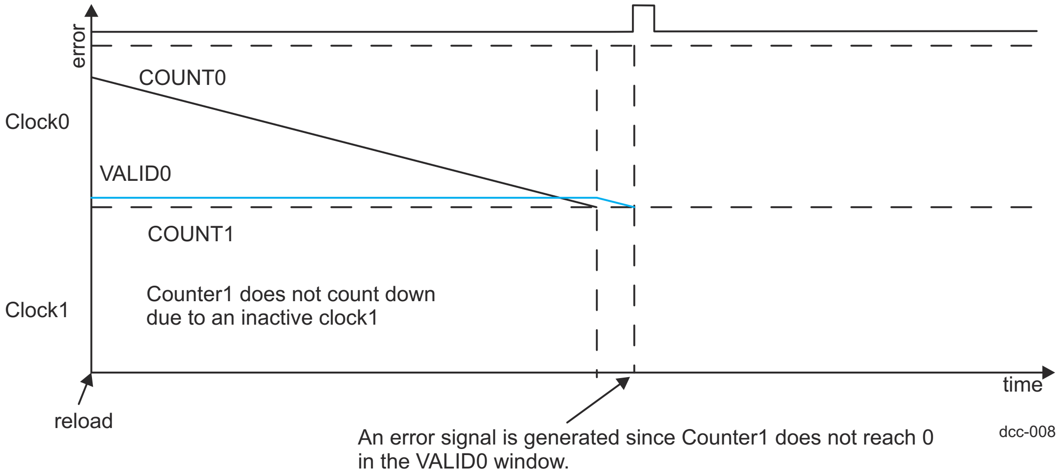


Figure 12-373. DCC Clock1 not present results in an error and stops counting

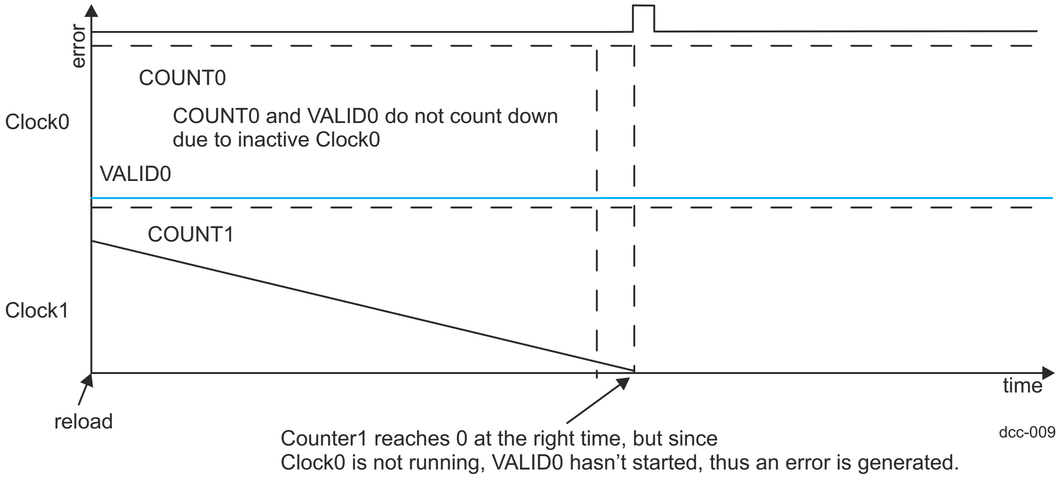


Figure 12-374. DCC Clock0 not present results in an error and stops counting

12.7.1.2.2 DCC Low Power Mode Operation

The DCC module does not function in Low Power Mode. It is the responsibility of software to stop the module before entering low power mode and to restart the module after exiting low power mode.

12.7.1.2.3 DCC Suspend Mode Behavior

The DCC module will continue running regardless of the state of emulation. All registers are readable via emulation reads.

12.7.1.2.4 DCC Single-Shot Mode

The DCC can be programmed to count down one time using single-shot mode. In this mode, the DCC stops operation when both COUNT0 and VALID0 reach 0.

At the end of one sequence in single-shot mode the DCC2_DCCGCTRL[3-0] DCCENA bitfield is set to disabled, which stops further counting. Single-shot mode is enabled from the DCC2_DCCGCTRL[11-8] SINGLESHOT bitfield.

At the end of one sequence in single-shot mode, if there is no error which stops counting, then the done status bit is set in the DCC2_DCCSTATUS[1] DONEFLG bitfield and a done interrupt DCC_x_INT is generated. Software must clear the done bit before restarting the counting.

12.7.1.2.5 DCC Continuous mode

When DCC runs in continuous mode both the counts shall get reloaded with seed value upon completion of counts without error. If the counts end in error DCC stops the operation and counts are not reloaded.

12.7.1.2.5.1 DCC Continue on Error

During debug, if there are events which are causing clocks to be anomalous over short period covering more than one evaluation window then it would be important to capture trajectory of error event and period around such event. To allow capturing the successive error events DCC can be programmed to continue after error. [3-0] CONT_ON_ERR shall be set to value other than "0101" to enable this mode. It is recommended to write "1010" to avoid single soft errors.

12.7.1.2.5.2 DCC Error Count

DCC also counts the number of error pulses generated since reset or since last time the error count is cleared. This is read/write register for CPU to clear when new trace of number of errors is required to be maintained.

12.7.1.2.6 DCC Control and count hand-off across clock domains

As the counters run in two different selectable clock domains and the register interface runs on the fixed bus clock domain, control signals and counter value hand-off have synchronizers implemented. These add to the margins of error while comparing the counts.

1. With all three counts synchronized to FICLK domain for comparison error detection there is delay in terms of FICLK domain.
2. Based on the error signal, the enable for the counters is synchronized back to the respective clock domains of the counters, which adds latency in terms of clock periods which are different, this would create a skew between start of count. Depending upon frequency ratios of the clocks used, the difference between two could vary.

Application needs to consider the worst case delay differences while measuring the clocks.

12.7.1.2.7 DCC Error Trajectory record

Once the clock errors out, the host can read the counter values to determine the extent of error to analyze type of failure. For short window comparisons this would become difficult, specially if there are back to back errors due to some transient event. Secondly, for random events which can cause an interrupt during the critical phase of application running, then event if not recorded may get overwritten and also not provide meaningful trace of error.

12.7.1.2.7.1 DCC FIFO capturing for Errors

DCC provides the FIFO for capturing COUNT0, VALID0, and COUNT1 information which captures all three counts upon "Error" event. For "Done" event no results are captured by default.

12.7.1.2.7.2 DCC FIFO in continuous capture mode

To track the VALID0 counter values regardless of "Error" or not, FIFOs can be configured to capture the count for each compare window. This is useful in validation and characterization exercise. [11-7] FIFO_NONERR control when set to value other than "0101" this mode is set; it is recommended to write "1010" to avoid single soft errors. Note, this capture is applicable only in continuous mode and not in single shot mode.

12.7.1.2.7.3 DCC FIFO Details

The FIFO is 4 deep for each count and updates new count information for all the non-full FIFOs. Information is updated on every configured trigger of error or cycle completion. If full, the next values are not written till at-least one entry is read. Application owns responsibility to read the FIFOs uniformly to keep synchronisation between three entries of the FIFO. Both empty and full indications for individual FIFOs is provided through the .

12.7.1.2.7.4 DCC FIFO Debug mode behavior

Upon debug access, the FIFO pointers should not advance hence not impacting the functional behavior. This requirement is same as other functional blocks in the device.

12.7.1.2.8 DCC Count read registers

DCC has provision to read the counts during operation. This is performed using , , and registers. Read from these registers in default mode allows reading the present value of count. This is useful when in single shot mode or mode where DCC stops upon error.

These registers can be used to read the FIFO through the [7-4] FIFO_READ configuration. Reads on the empty FIFO shall provide the contents of last pointed location. Application shall track the empty/full conditions of the FIFOs to track the count records consistently.

Regardless of FIFO_READ configuration, the FIFO internally keeps updating records based on configured triggers till full.

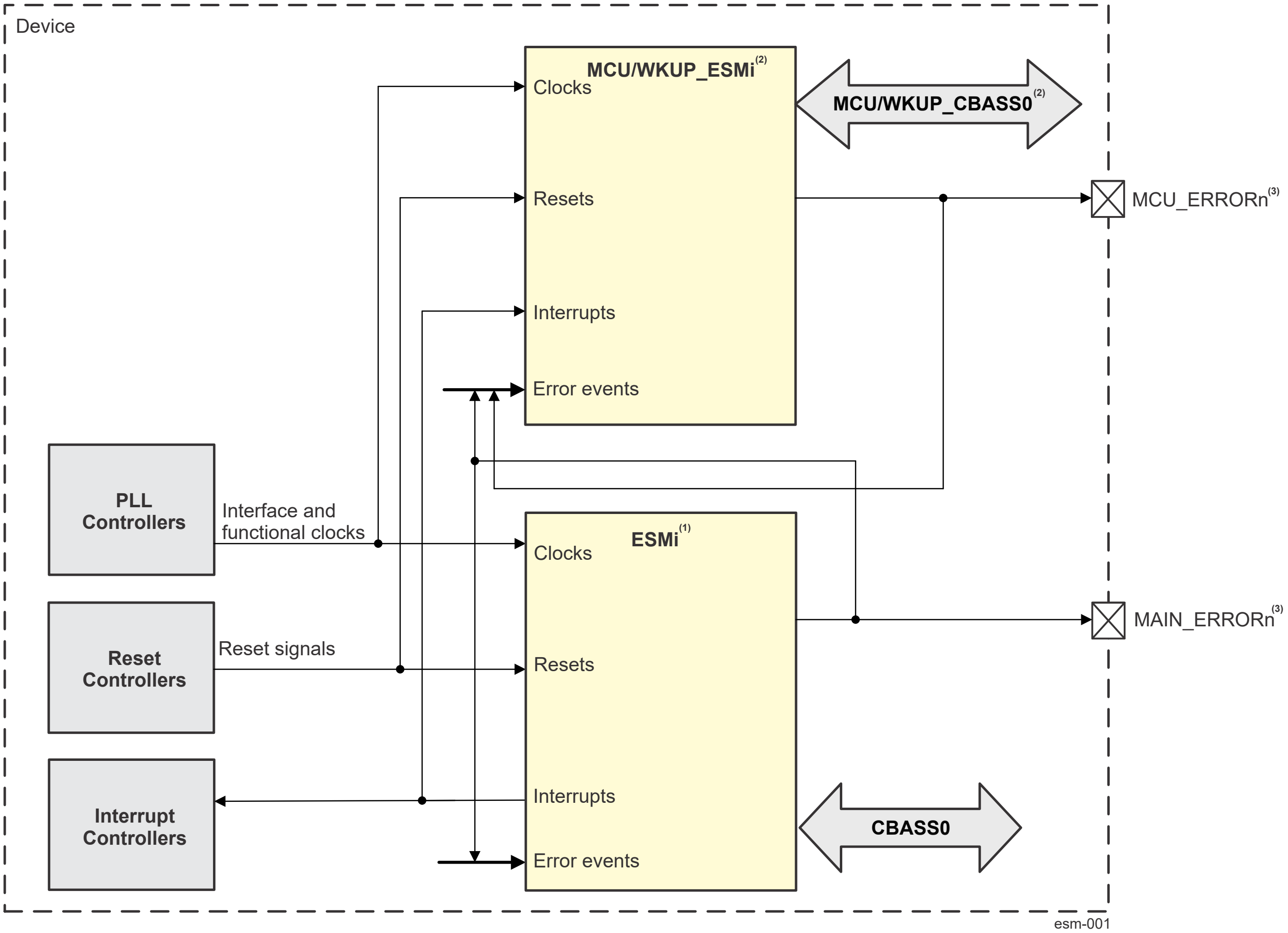
12.7.2 Error Signaling Module (ESM)

This section describes the Error Signaling Module (ESM) in the device.

12.7.2.1 ESM Overview

The Error Signaling Module (ESM) aggregates events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with an event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in a safe, known state.

Figure 12-375 shows the ESM modules overview.



1. i represents a valid instance of ESM in a domain. Consult the device datasheet for available domains and ESM instances.
2. i represents a valid instance of ESM in a MCU or WKUP domain. Consult the device datasheet for available domains and ESM instances.
3. Not all pins are valid for all devices. Consult the device datasheet for specifics.

Note

The MAIN_ERRORn pin, if valid, is used for observation only.

Figure 12-375. ESM Modules Overview

12.7.2.1.1 ESM Features

Each ESM module implements the following features:

- Up to 1024 error event inputs
  - Implemented in groups of 32 events

  - Level or Pulse inputs (Pulse inputs are triple redundant)
- Selectable low and high priority interrupt error pin prioritization of each error event
- Error pin to signal severe device failure
  - Support of level or PWM modes
- Configurable timebase for error signal
- Error forcing capability
- Internal redundant flops on critical fields

12.7.2.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

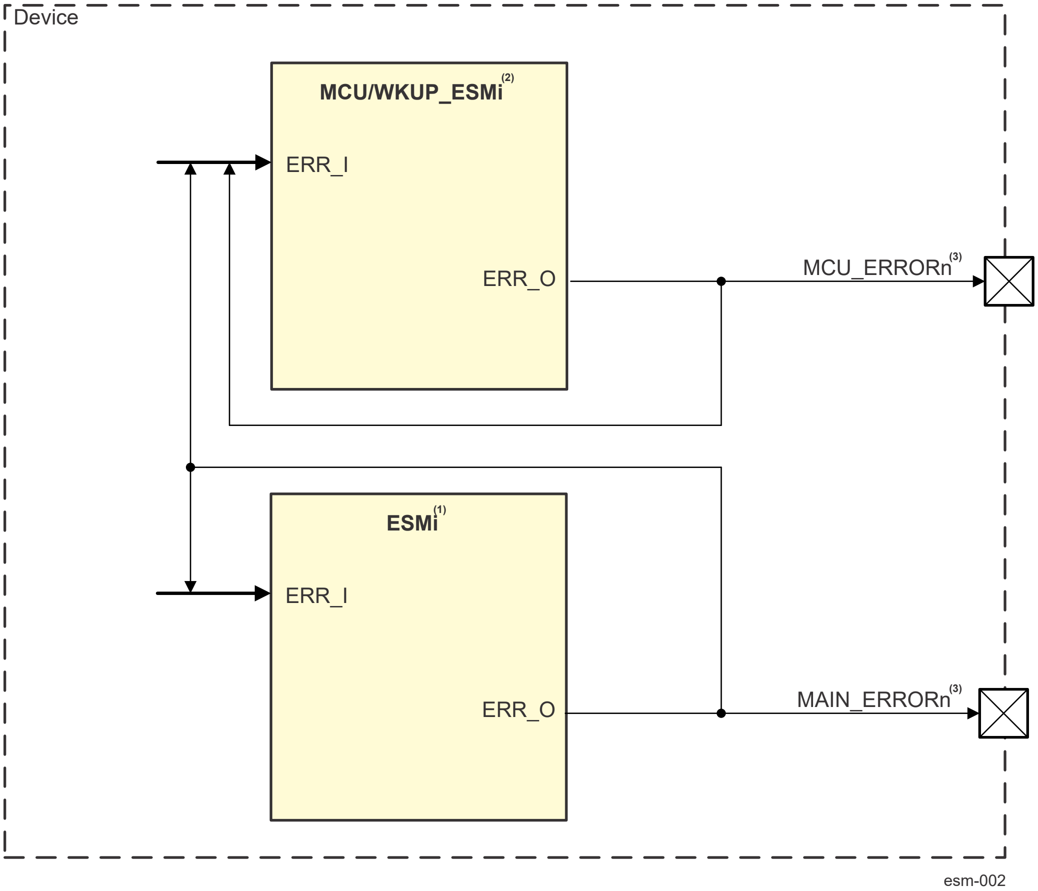
Some features may not be available. See *Module Integration* for more information.

12.7.2.2 ESM Environment

The MCU_ESM0 and ESM0 modules are hereinafter referred to as ESM module.

This section describes the ESM external connections (environment).

Figure 12-376 shows the ESM pins used for typical connections with external devices.



1. i represents a valid instance of ESM in a domain. See the device specific datasheet for available domains and ESM instances.
2. i represents a valid instance of ESM in a MCU or WKUP domain. See the device specific datasheet for available domains and ESM instances.
3. Not all pins are valid. See the device datasheet for specifics.

Note

The MAIN_ERRORn pin, if valid, is used for observation only.

Figure 12-376. ESM Modules Environment

Note

For more information about device level signals (pull-up/down resistors, buffer type, multiplexing and others), see tables *Pin Attributes* and *Pin Multiplexing* in the device-specific Datasheet.

12.7.2.3 Integration

See the *Module Integration* section for information about clocks, resets and hardware requests.

12.7.2.4 ESM Functional Description

The Error Signaling Module (ESM) centralizes fault reports. It provides mechanisms to classify errors by severity and to provide programmable error response. The error classification in the ESM is determined by programmed configuration for each individual error input. For each individual error input the configuration can be set to assert an output error pin, or generate an interrupt to a CPU, or both. When an individual error input is configured to generate an interrupt, the configuration will also select whether the interrupt that is generated will be one of high priority or low priority.

By reporting the faults in a central location, the system may determine what caused the fault and what action can be taken. In general, the faults can be split into two categories:

- Corrected faults
- Non-corrected faults

The ESM reports errors in two ways:

- An interrupt to a processor in the device. This allows the device to analyze and try to recover from an error.
- An external ERROR pin. This allows the system outside of the SoC to monitor for potentially fatal errors(errors that the device cannot self-recover from). Moreover, the external I/O (ERROR pin) can operate in level or PWM modes. In level mode, the output will remain asserted (active low) for a minimum period of time. After that period of time, if the error has been cleared by an internal processor, the pin will go inactive (high). If it does not go inactive in that time, then an external agent should intervene, as there may be an unrecoverable error. In PWM mode, the error will cause the output pin to maintain its value for a minimum period of time. After that period of time, if the error has been cleared by an internal processor, the pin will continue the PWM pattern. If it does not go inactive in that time, then an external agent should intervene, as there may be an unrecoverable error.

Both mechanisms can be used at the same time for the same fault, signaling both an interrupt and the external ERROR pin. This allows the device to attempt to recover, but if it fails, then the external system is still alerted. If it succeeds, then it can remove the ERROR pin assertion so that the external system knows that a potentially unsafe condition was avoided.

Lastly, the ESM does not specify any methods of intervention, only the process of alerting internal CPUs and external monitor(s) of an existing error event.

Figure 12-377 shows the ESM module block diagram. Note that not all instances may be pinned out in the device. For more information, see Section 12.7.2.2, *ESM Environment*.

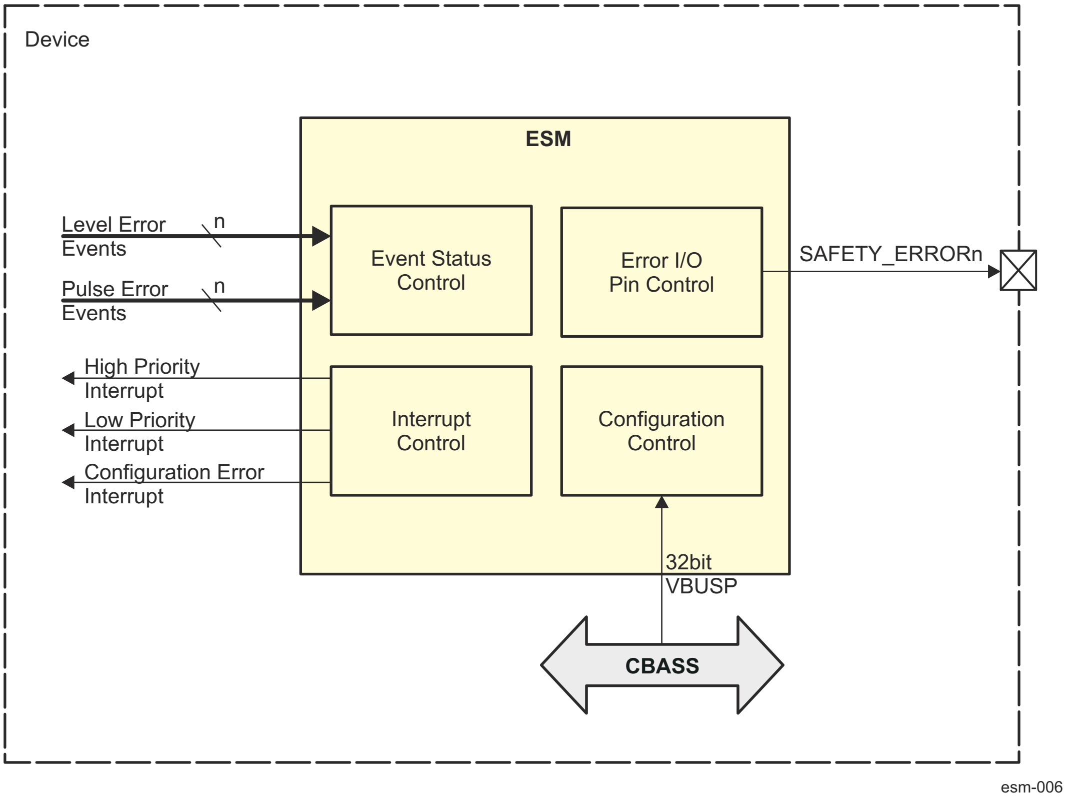


Figure 12-377. ESM Block Diagram

12.7.2.4.1 ESM Interrupt Requests

The ESM module generates three output interrupts to the device interrupt controllers:

- Configuration error interrupt (see Section 12.7.2.4.1.1)
- High priority error interrupt (see Section 12.7.2.4.1.2)
- Low priority error interrupt (see Section 12.7.2.4.1.3)

The error interrupt outputs are provided so that a processor in the device can be signaled to intervene when an error event occurs. Each error event input can be enabled, via software, to cause an error interrupt to occur (via the ESM_INTR_EN_SET_j register). Additionally, each error event input can be programmed to influence either the low priority (default) interrupt or the high priority interrupt (via the ESM_INT_PRIO_j). The low priority interrupt is intended for events that are of interest, but do not require immediate intervention. For example, an indication that there was a single bit error that was corrected may signal a low priority interrupt, so that information can be collected for statistical purposes. A high priority interrupt is intended for events that need immediate attention. For example, an indication that there was an uncorrected two-bit error may be signaled as a high priority interrupt.

12.7.2.4.1.1 ESM Configuration Error Interrupt

The configuration error interrupt (ESM_INT_CFG_LVL_0) indicates that there is an inconsistency in the configuration of one (or more) error group *j* registers (MMRs).

In such inconsistency in the internal copies of any of the MMRs caused by fault associated with error group *j*, the corresponding raw status will be set in the ESM_ERR_RAW register. If the corresponding bit is enabled in the ESM_ERR_EN_SET register, a configuration error interrupt will be triggered.

When a configuration error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_ERR_STS register to determine which group has a configuration error
2. Write the correct values to the following group registers:

Note

If there has been a configuration error, the values in the below registers cannot be guaranteed to be correct anymore. Therefore, software should maintain a copy of the correct values prior to an error to ensure that they can be re-programmed with the correct configuration.

   a. ESM_INTR_EN_SET_j
   b. ESM_INTR_EN_CLR_j
   c. ESM_INT_PRIO_j
   d. ESM_PIN_EN_SET_j
   e. ESM_PIN_EN_CLR_j

3. Service any pending interrupts in steps 4, 5, and 6 below

Note

The raw status of any pending interrupts may be inconsistent. Servicing the interrupt will return it to consistency via the error group ESM_RAW_j register.

4. Write 0x1 to the appropriate bits in the ESM_ERR_STS register. This step will clear the raw status
   a. If the error event is still asserted (or re-asserted) the raw status will be set back to 0x1
   b. If there are no additional errors, the level interrupt will go low
5. Write the end of interrupt vector to the ESM_EOI register
   a. If there are additional configuration error interrupts pending, then a new pulse will be generated and the level interrupt will remain asserted
   b. If there are no additional low priority error interrupts pending, there will be no new pulse.

12.7.2.4.1.2 ESM Low Priority Error Interrupt

Events mapped to the low priority error interrupt (ESM_INT_LOW_LVL_0) are intended to be events of interest that should be addressed eventually, not events that require immediate attention. An example would be an event indicating a corrected error. The system may want to track this for statistical purposes, but it does not require immediate attention.

Any error event can be mapped to the low priority error interrupt. A low priority error interrupt will be generated when an event is enabled to cause an interrupt (via the ESM_INTR_EN_SET_j register) and mapped to the low priority error interrupt (via ESM_INT_PRIO_j register) and the raw status is set (via the ESM_RAW_j register).

When a low priority error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_LOW_PRI register
   a. If both [31-16]PLS and [15-0]LVL bit fields are equal to 0xFFFF, then interrupt is no longer asserted and the interrupt routine has ended.
   b. If either [31-16]PLS or [15-0]LVL bit fields are not equal to 0xFFFF, software has two options for determining what event to service:
      i. First option: Record the value in [31-16]PLS and [15-0]LVL bit fields. Determine which is higher priority. This is based on the global event map number of the highest priority low priority error event

Note

The global event map is neither defined by nor maintain in ESM. The global event map must be defined and maintained by software using software determined memory resources. It is conceivable that the global event map will be predefined and loaded during the execution of a secondary boot loader.

      ii. Second option:
         1. Read the ESM_LOW register to determine which event group(s) have pending low priority error interrupts

        2. Read the desired error group *j* ESM_STS_j register
        3. Identify which low priority interrupt to service

2. Determine, based on the global event map for the device, where the error event came from
3. Service the error event based on the IP's specification:
    a. The system may take several actions including (but not limited to):
        i. Fixing the error
        ii. Resetting the errored IP peripheral
        iii. Resetting the device
        iv. Communicating outside the device via the error pin for outside intervention

The rest of the steps assume that the error has been handled and the system wants to clear the error event. Clearing the error event depends on whether the event is a level (see Section 12.7.2.4.1.2.1) or pulse (see Section 12.7.2.4.1.2.2) event.

12.7.2.4.1.2.1 ESM Low Priority Error Level Event

When a low priority error level event has to be cleared, the acting processor must perform the following steps:

1. Clear the low priority error level event at the source
2. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This step will clear the raw status
    a. If the error event is still asserted (or re-asserted) the raw status will be set back to 0x1
    b. If there are no error events, the level will de-assert

Note

There is a possible software race condition if software manages to write to the Clear register before the de-asserted level from the source has been synchronized to the ESM clock. If this is an issue, software may perform a read-back at the source IP before writing the clear register to insure order.

3. Write the end of interrupt vector to the ESM_EOI interrupt register
    a. If there are low priority error level events enabled and pending, then a new pulse will be generated
    b. If there are no additional low priority error level events enabled and pending, there will be no new pulse
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j*ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.7.2.4.1.2.2 ESM Low Priority Error Pulse Event

When a low priority error pulse event has to be cleared, the acting processor must perform the following steps:

1. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This will clear the raw status and will de-assert the level interrupt.
2. Write the end of interrupt vector to the ESM_EOI interrupt register
    a. If there are additional low priority error pulse events enabled and pending, then a new pulse will be generated and the level interrupt will remain asserted
    b. If there are no additional low priority error pulse events enabled and pending, there will be no new pulse
3. Clear the error event at the source. The source may generate a new pulse which will show up as a new error event at the ESM
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j*ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.7.2.4.1.3 ESM High Priority Error Interrupt

Events mapped to the high priority error interrupt are intended to be events that require immediate intervention from the system because a potentially dangerous error has occurred. An example would be an event indicating an uncorrected error. The system will want to diagnose the issue and intervene to ensure there are no violations.

Any error event can be mapped to the high priority error interrupt. A high priority error interrupt will be generated when an event is enabled to cause an interrupt (via the ESM_INTR_EN_SET_j) register and mapped to the high priority interrupt (via the ESM_INT_PRIO_j) register and the raw status is set (via the ESM_RAW_j).

When a high priority error interrupt is received, the acting processor must perform the following steps:

1. Read the ESM_HI_PRI register
    a. If both [31-16] PLS and [15-0] LVL bit fields are equal to 0xFFFF, then interrupt is no longer asserted and the interrupt routine has ended.
    b. If either [31-16] PLS or [15-0] LVL bit fields are not equal to 0xFFFF, software has two options for determining what event to service:
        i. First option: Record the value in [31-16] PLS and [15-0] LVL bit fields. Determine which is higher priority. This is based on the global event map number of the highest priority high priority error event.

        Note

        The global event map is neither defined by nor maintain in ESM. The global event map must be defined and maintained by software using software determined memory resources. It is conceivable that the global event map will be predefined and loaded during the execution of a secondary boot loader.

        ii. Second option:
            1. Read the ESM_HI register to determine which event group(s) have pending high priority error interrupts
            2. Read the desired error group *j*ESM_STS_j register
            3. Identify which high priority error interrupt to service
2. Determine, based on the global event map for the device, where the error event came from
3. Service the error event based on the IP's specification:
    a. The system may take several actions including (but not limited to):
        i. Fixing the error
        ii. Resetting the errored IP peripheral
        iii. Resetting the device
        iv. Communicating outside the device via the error pin for outside intervention

The rest of the steps assume that the error has been handled and the system wants to clear the error event. Clearing the error event depends on whether the event is a level (see Section 12.7.2.4.1.3.1) or pulse (see Section 12.7.2.4.1.3.2) event.

12.7.2.4.1.3.1 ESM High Priority Error Level Event

When a high priority error level event has to be cleared, the acting processor must perform the following steps:

1. Clear the error event at the source
2. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This step will clear the raw status
    a. If the error event is still asserted (or re-asserted) the raw status will be set back to 0x1
    b. If there are no error events, the level will de-assert

---

Note

There is a possible software race condition if software manages to write to the Clear register before the de-asserted level from the source has been synchronized to the ESM clock. If this is an issue, software may perform a read-back at the source IP before writing the clear register to insure order.

---

3. Write the end of interrupt vector to the ESM_EOI interrupt register
   a. If there are high priority error level events enabled and pending, then a new pulse will be generated
   b. If there are no additional high priority error level events enabled and pending, there will be no new pulse
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j*ESM_PIN_EN_SET_j register, but may be done regardless as an extra CLEAR is not harmful.

12.7.2.4.1.3.2 ESM High Priority Error Pulse Event

When a high priority error pulse event has to be cleared, the acting processor must perform the following steps:

1. Write 0x1 to the appropriate bit in the error group *j* of the ESM_STS_j register. This will clear the raw status and will de-assert the level interrupt.
2. Write the end of interrupt vector to the ESM_EOI interrupt register
   a. If there are high priority error pulse events enabled and pending, then a new pulse will be generated and the level interrupt will remain asserted
   b. If there are no additional high priority error pulse events enabled and pending, there will be no new pulse
3. Clear the error event at the source. The source may generate a new pulse which will show up as a new error event at the ESM
4. Write a CLEAR (0x5) to the ESM_PIN_CTRL register. This step is optional if the event is not enabled to influence the error pin (error group *j*ESM_PIN_EN_SET_j register), but may be done regardless as an extra CLEAR is not harmful.

12.7.2.4.2 ESM Error Event Inputs

The ESM can have up to 1024 error event inputs, configurable by groups of 32. For the mapping of system interrupt error events to ESM interrupt inputs, see *Interrupt Sources*.

Level error events (active high) are synchronized to the ESM clock. This synchronized value is captured in to a flop.

Pulse error events use rising edge detection. Each pulse error event has 3 redundant inputs. Each input has its own edge detection logic. Multiple transmission protects against Single Event Upsets (SEUs, transient errors) causing a pulse to be lost during transmission and against failure of the edge detection logic. Once an edge has been detected on any of the three inputs, the ESM_RAW_j status is set. Subsequent pulses are likely to come concurrently or quickly enough that software will not have reacted yet. This logic is intentionally biased against false negatives and towards false positives. An SEU that causes an event where none actually occurred will cause software to be called in to action. Software must observe that there is no real error and clear the false status.

12.7.2.4.3 ESM Error Pin Output

The error pin output (ERR_O) is used to signal an external agent that it needs to (or may need to) intervene because of an error. Each error event input can be programmed, via software, to influence the error pin output (via the ESM_PIN_EN_SET_j register). The error pin output is active low or PWM based on the ESM_EN[7-4] PWM_EN field. This bit field should only be modified when the ESM is disabled, based on the ESM_EN register.

During Power-On Reset (POR), the error pin is active (asserted low) and the device drives this via a weak internal pull-down. The I/O is under the control of the device. When POR is removed from the ESM, it will be driving the error pin so the device can hand over control to the ESM. The user may also add an external pull-down that is only active when the device is in reset.

During a warm reset the state of the error pin is unchanged, that is the error pin logic is only reset by a POR. The device leaves the I/O active during a warm reset.

The ESM has also a software error forcing capability on the error pin. That is, a force error can be set via the ESM_EN[3-0] KEY bit field.

CAUTION

The isolation value for the ERR_O output of ESM is active (0). This is intended and supposed to protect against an accidental transition to a low power state. If the actual low power mode transition is intended, the PMIC should be made aware by software to ignore the ESM error signal. Otherwise device resets will be asserted from companion chip.

Figure 12-378 describes the behavior of the error pin. Not shown is that a reset (Power-On-Reset only) will immediately transition the error pin to the ESM_RESET state and a Global Soft Reset will immediately transition the error pin to the ESM_IDLE state. A pending error interrupt event is any error event with the raw state set and the error pin Influence enabled. There are two types of "clear" events associated with servicing the error pin. The first is to clear the status of the pending event (see Section 12.7.2.4.1 for how to clear level and pulse pending events). The second is the CLEAR event meant to de-assert the error pin.

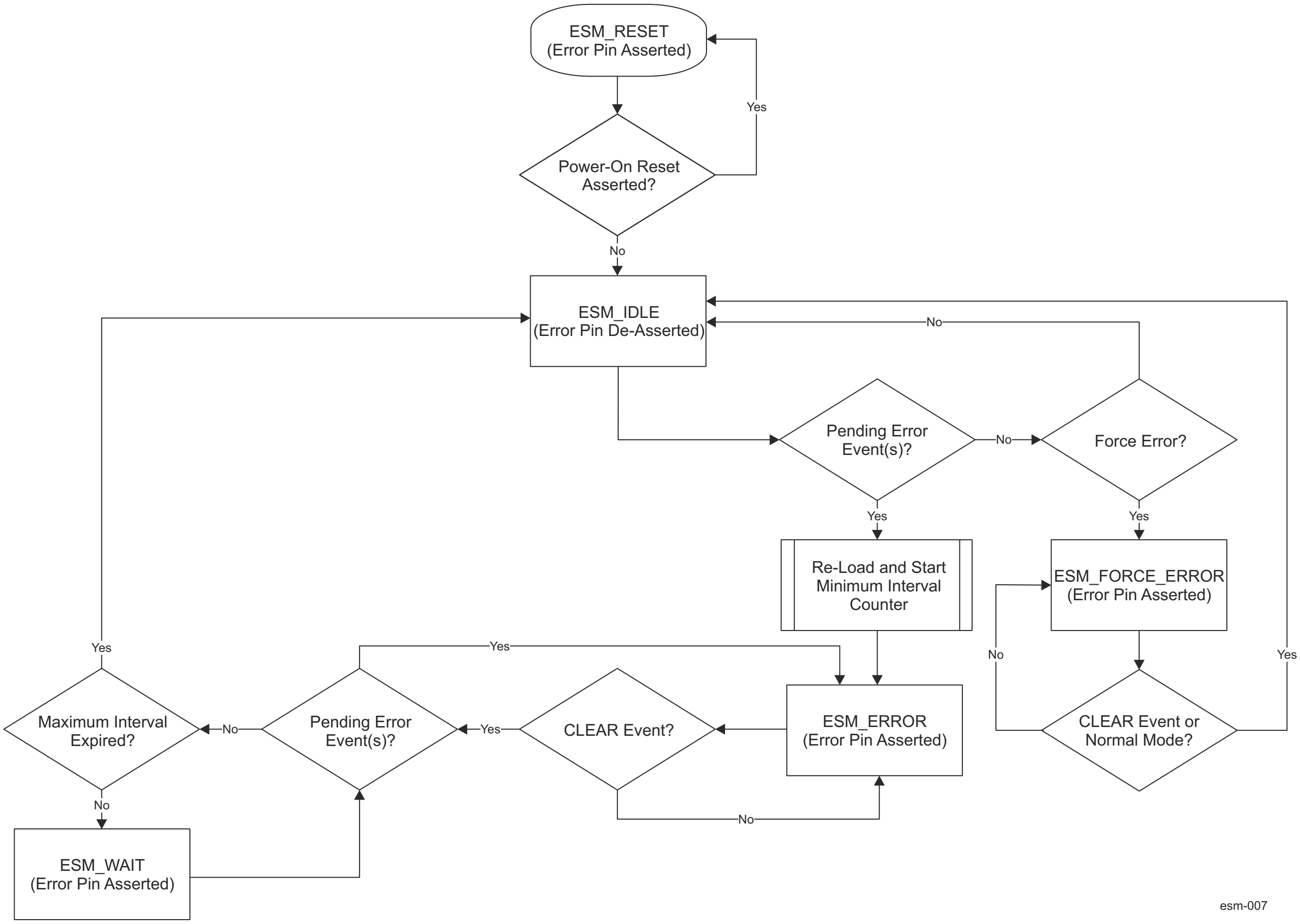


Figure 12-378. ESM Error Pin State Flowchart

If an error event happens that has been programmed to influence the error pin, the error pin will assert (active low) for a minimum time (as programmed by the ESM_PIN_CNTR_PRE register). In order for the error pin to de-assert, the following 3 things must happen:

1. The minimum time interval must expire

2. The event that caused the error pin to assert must be cleared (see Section 12.7.2.4.1)
3. A CLEAR (0x5) must be written to the ESM_PIN_CTRL register.

Note

Step 3 should happen after step 2, but either (or both) of these steps may happen before or after step 1.

Figure 12-379 shows a typical error pin assertion.

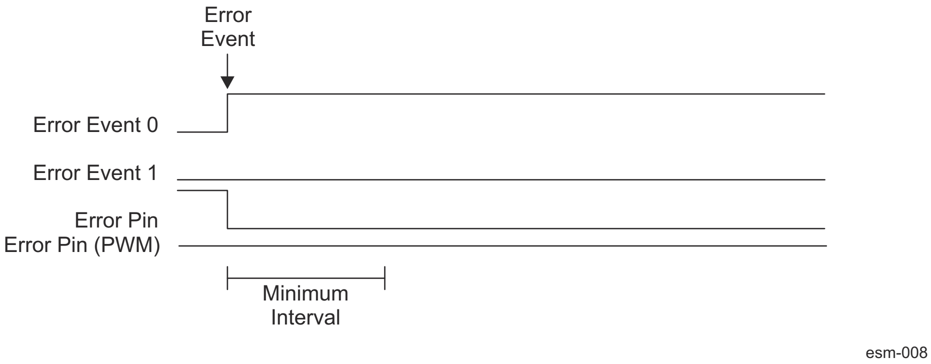


Figure 12-379. ESM Error Pin Assertion

If, during the minimum time, CLEAR is written to the error key, then the error pin will de-assert after the minimum time interval, as shown in Figure 12-380.

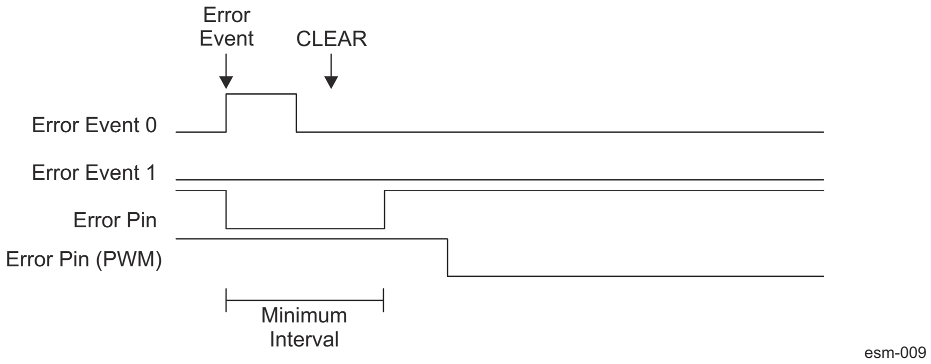


Figure 12-380. ESM Error Pin Assertion with CLEAR during Minimum Interval

If CLEAR is not written till after the minimum time interval, the error pin will de-assert when CLEAR is written. This is regardless of whether the error interrupt event itself is removed before or after the minimum time interval, as shown by the dotted line in Figure 12-381.

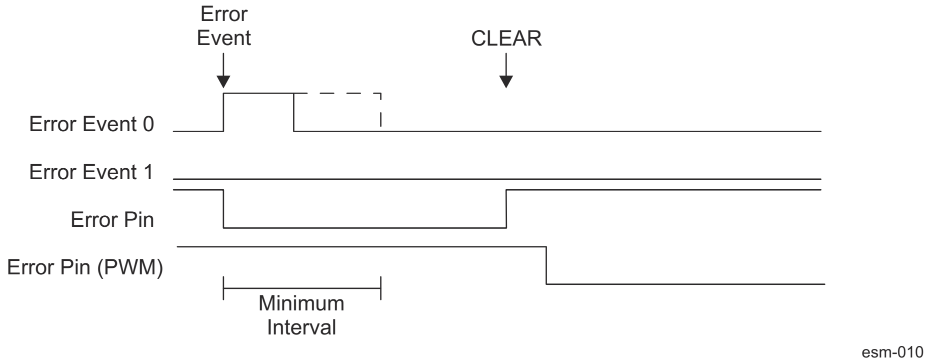


Figure 12-381. ESM Error Pin Asserting with CLEAR after Minimum Interval

When in the ESM_ERROR state and a CLEAR event happen, if there are still pending error events, the ESM stays in the ESM_ERROR state with the error pin asserted. Multiple error events when in the ESM_ERROR state do not reset the minimum time interval counter as shown in Figure 12-382.

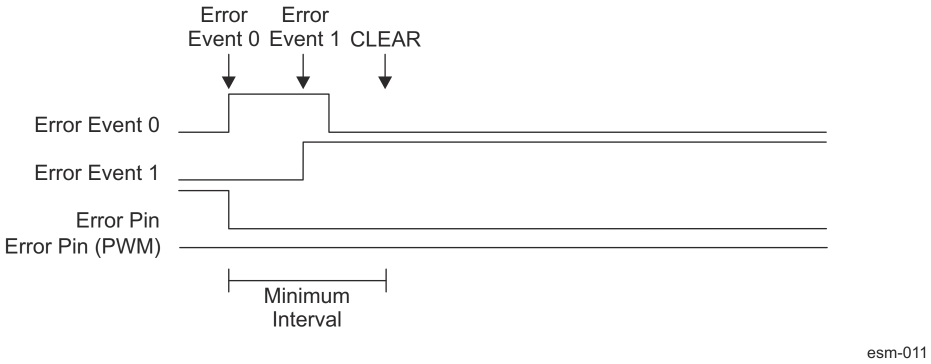


Figure 12-382. ESM Error Pin Asserting with Interval Reset by Additional Error Event(s)

A CLEAR event causes a re-evaluation of whether there are any pending error events. As such, a single CLEAR can be used to clear the error pin after multiple error events. Multiple CLEAR events can occur (such as the one with the dotted arrow shown in Figure 12-383), but are not necessary. No matter how many error events occur nor when (or how many) CLEAR events occur, the error pin will always be asserted for at least the minimum time interval

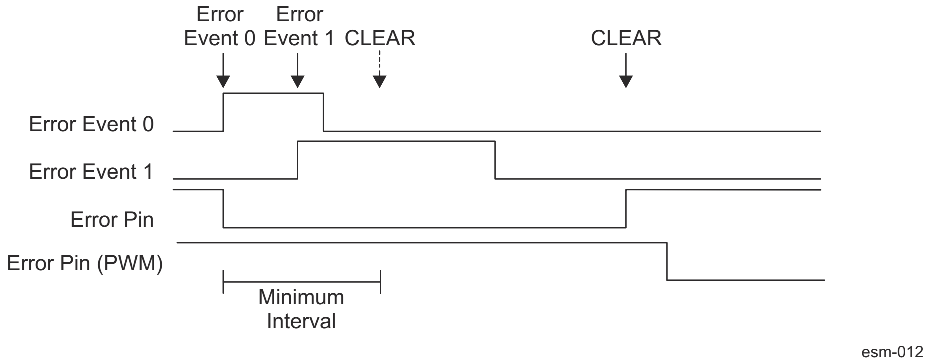


Figure 12-383. ESM Error Pin Asserting with Single CLEAR for Multiple Events

If all error events are cleared and the ESM is in the ESM_WAIT state, waiting for the minimum time interval to expire, and a new error interrupt event occurs, the ESM will go back to the ESM_ERROR state. The minimum time interval will not reset, but a new CLEAR event will be required as shown in Figure 12-384.

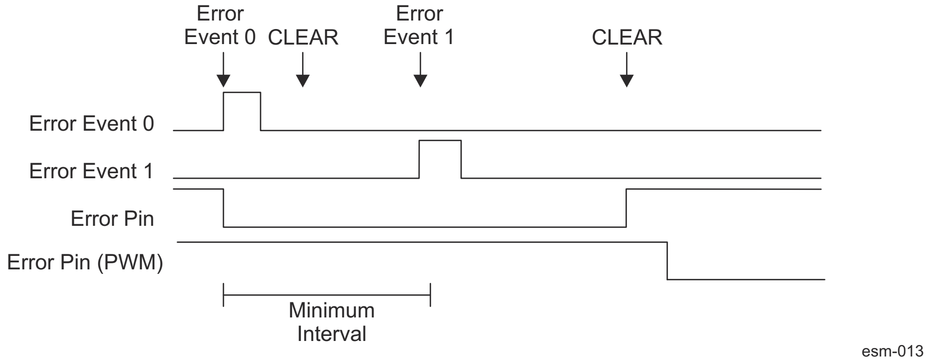


Figure 12-384. ESM Error Pin Asserting with New Error During Minimum Time Interval

Table 12-326 shows some common scenarios of how the error pin as well as the two associated registers (ESM_PIN_CTRL and ESM_PIN_STS) will be set.

Table 12-326. ESM Error Pin Scenarios

Scenario	Error Pin State Value	ESM_PIN_CTRL[3-0] KEY	ESM_PIN_STS[0] VAL status value	Additional Notes
POR Asserted	0	N/A	N/A	Registers are inaccessible. Device disables the I/O and pulls down internally.
After de-assertion of POR	1	0x0 (Normal Mode)	0x0	-
After de-assertion of Warm Reset (error was not asserted when reset asserted)	1	0x0 (Normal Mode)	0x0	-
After de-assertion of Warm Reset (error was asserted when reset asserted)	0	0x0 (Normal Mode)	0x1	-
Force error pin	0	0xA (Force Error Mode)	0x0	Forcing error on the pin via software.

12.7.2.4.4 PWM Mode

If the error output pin is in PWM mode then when no error is detected it will toggle according to programmable MMR widths for high and low periods. When an error occurs, the error pin stops toggling and remains constant until the error is cleared. An external PMIC that is detecting the PWM toggles can identify the error if the pin stops toggling. The periods should be programmed such that they fit within the expectation of the external PMIC.

12.7.2.4.5 ESM Minimum Time Interval

The minimum time interval is the minimum amount of time that the error pin will be asserted (active low) when an enabled error interrupt event happens. This value is system dependent, but should be enough time so that the external monitoring agent can always see the error pin asserted, but short enough so that if all of the error events are cleared, then the error pin can be de-asserted before the external agent decides to intervene. This is highly dependent on the application and the Fault Tolerant Time Interval.

The Minimum Time Interval counter is clock cycle based, therefore the time of the interval is a combination of the value in the ESM_PIN_CNTR_PRE register and the clock frequency of the ESM. Software must calculate the value accordingly. The Minimum Time Interval should be set according to the needs of the application.

12.7.2.4.6 ESM Protection for Registers

The configuration for each error group *j* of registers are backed up by 3 flops in order to protect against single or double-bit errors. When written, all 3 bits are set to the same value. When read (and for functioning of the internal state machines) the value is the OR of all 3 bits. Whenever any of the bits disagree, the Configuration Error interrupt is asserted (if enabled). The registers covered by this mechanism are:

- ESM_ERR_RAW
- ESM_ERR_STS
- ESM_ERR_EN_SET
- ESM_ERR_EN_CLR
- ESM_RAW_j
- ESM_STS_j
- ESM_INTR_EN_SET_j
- ESM_INTR_EN_CLR_j
- ESM_INT_PRIO_j
- ESM_PIN_EN_SET_j
- ESM_PIN_EN_CLR_j

The error pin control register ESM_PIN_CTRL contains a multi-bit field KEY. The key value ensures normal operation on the error pin and that an error even will be generated if one occurs. Software should periodically read check the KEY bit field value and make sure it is 0x0. If the value is not 0x0, software must re-write it to this key value (unless in test mode forcing an error on the pin) to ensure the normal operation. Table 12-327 lists the KEY values and their respective meaning.

Table 12-327. ESM Error Pin Control Values

ESM_PIN_CTRL[3-0] KEY	Description
N/A	Registers are inaccessible. Device disables the I/O and pulls down internally.
0x0 (Normal)	Normal operation mode - Error pin will activate when an enabled error event occurs.
0xA (Force Error)	Force error mode - Forces the error pin active. To clear the error pin (return to the ESM_IDLE state) write this field back to normal mode (writing a CLEAR event will also work). Force error mode must be set only while in IDLE. Attempting force error while in another state will have no effect.
0x5 (CLEAR)	CLEAR Event - generates a CLEAR event to the ESM state machine. KEY will return to normal mode (0x0) on the next cycle.
Other Values	All other values - Normal mode. Writing any of these values will have no effect. When reading any of these values indicates that one or more bits have experienced a single event upset, software should write the field back to 0x0. The ESM will continue to operate in normal mode.

The error pin counter pre-load register ESM_PIN_CNTR_PRE should also be read and checked periodically by software.

12.7.2.4.7 ESM Clock Stop

The ESM can only be put in to clock stop if all of the internal state machines are idle and the [3-0] KEY bit field for the global enable command is cleared in the ESM_EN register.

12.7.3 Memory Cyclic Redundancy Check (MCRC) Controller

This chapter describes the Memory Cyclic Redundancy Check (MCRC) controller in the device.

12.7.3.1 MCRC Overview

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system.

12.7.3.1.1 MCRC Features

MCRC has the following features:

- Four channels to perform background signature verification on any memory subsystem
- Data compression on 8-, 16-, 32-, and 64-bit data size
- Maximum-length PSA (Parallel Signature Analysis) register constructed based on 64-bit primitive polynomial
- Each channel has a CRC Value Register which contains the pre-determined CRC value
- Use timed base event trigger from timer to initiate DMA data transfer
- Programmable 20-bit pattern counter per channel to count the number of data patterns for compression
- Three modes of operation:
  - Auto
  - Semi-CPU
  - Full-CPU
- For each channel, CRC can be performed either by MCRC Controller or by CPU
- Automatically performs signature verification without CPU intervention in AUTO mode
- Generates interrupt to CPU in Semi-CPU mode to allow CPU to perform signature verification itself
- Generates CRC fail interrupt in AUTO mode if signature verification fails
- Generates Timeout interrupt if CRC is not performed within the time limit
- Generates DMA request per channel to initiate CRC value transfer
- An 128-byte block burst address for the PSA register to DMA without constant mode bus attribute

12.7.3.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

Note

Some features may not be available. See *Module Integration* for more information.

12.7.3.2 MCRC Functional Description

12.7.3.2.1 MCRC Block Diagram

Figure 12-385 shows the MCRC internal blocks.

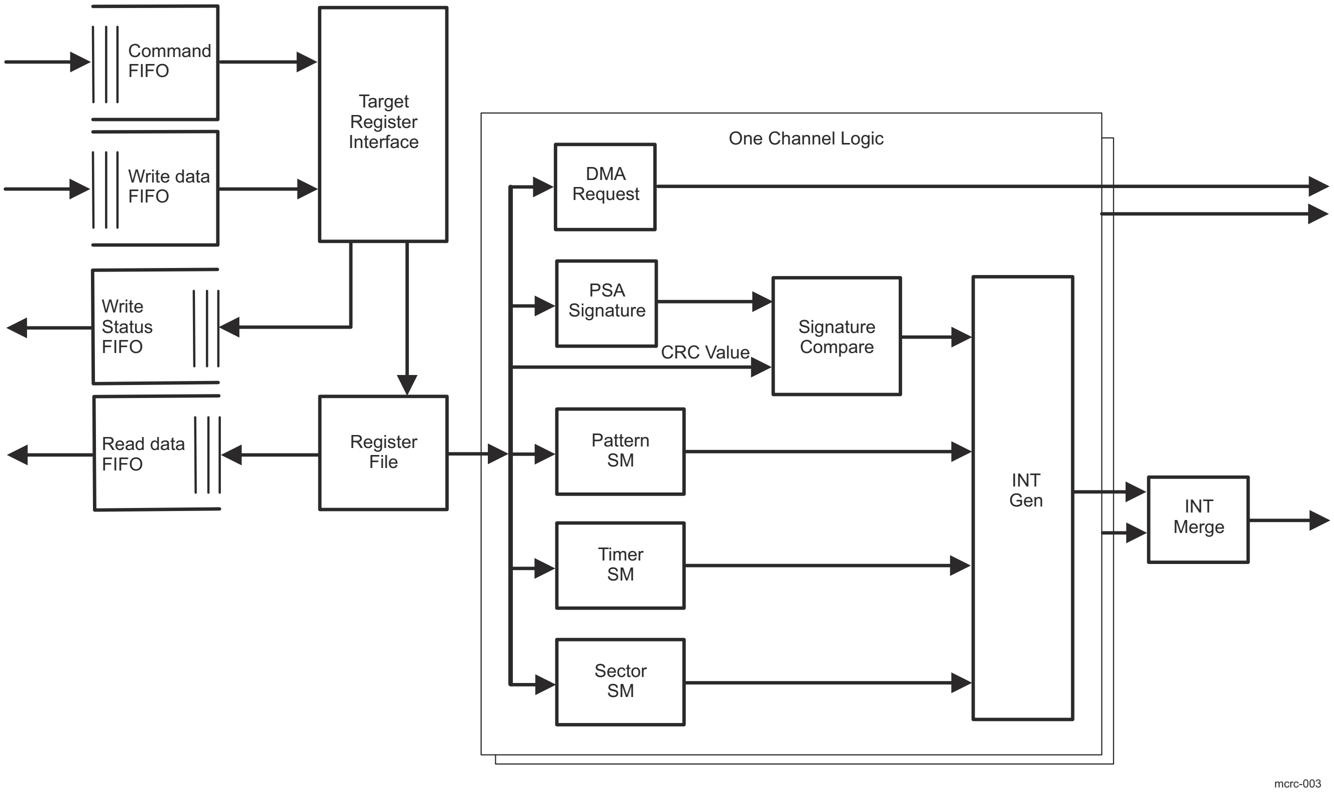


Figure 12-385. MCRC Block Diagram

- **Command FIFO**: The Command FIFO pipelines the commands to the target register interface. The Command and Write FIFOs allow the data to be coincident for processing. If there is no space for writes in the Write Status FIFO or no space in the Read Data FIFO for reads, the command processing will be halted until there is space in the appropriate FIFO. This FIFO is 4 elements deep.
- **Write FIFO**: The Write FIFO pipelines the write data to the target register interface. The Command and Write FIFOs allow the data to be coincident for processing. If there is no space for writes in the Write Status FIFO or no space in the Read Data FIFO for reads, the command processing will be halted until there is space in the appropriate FIFO. This FIFO is 2 elements deep.
- **Write Status FIFO**: The Write Status FIFO pipelines the write status back to the VBUSM. A write status will be issued on the final data phase of a write command. This FIFO is 2 elements deep.
- **Read Data FIFO**: The Read Data FIFO pipelines the read data back to the VBUSM. This FIFO is 3 elements deep.
- **Target Register Interface**: The Target Register Interface directs the written data to the register file.
- **PSA Signature**: The PSA Signature creates the signature of the data written. This data will then be compared to the CRC Value or read by software to determine goodness.
- **Pattern State Machine**: The Pattern State Machine determines when a block of data has been serviced.
- **Timer State Machine**: The Timer State Machine determines when overrun and under-run events are detected.
- **Sector State Machine**: The Sector State Machine determines when a sector error should be captured so the software can determine the errant block of data.
- **Signature Compare**: The Signature Compare block compares the current signature to the CRC Value register and sends the result to the Interrupt Generation block.

12.7.3.2.2 MCRC General Operation

There are four channels in MCRC controller and for each channel there is a PSA (Parallel Signature Analysis) Signature Register (MCRC64_0_PSA_SIGREGL1-4) and a CRC (Cyclic Redundancy Check) Value Register (MCRC64_0_CRC_REGL1-4).

A memory can be organized into multiple sectors with each sector consisting of multiple data patterns. A data pattern can be a 8-, 16-, 32-, or 64-bit data. MCRC module performs the signature calculation and compares the signature to a pre-determined value. The PSA Signature Register compresses an incoming data pattern into a signature when it is written. When one sector of data patterns are written into PSA Signature Register, a final signature corresponding to the sector is obtained. CRC Value Register stores the pre-determined signature corresponding to one sector of data patterns. The calculated signature and the pre-determined signature are then compared to each other for signature verification. To minimize CPU's involvement, data patterns transfer can be carried out at the background of CPU using DMA controller. DMA is setup to transfer data from memory of which the contents to be verified to the memory mapped PSA Signature Register. When DMA transfers data to the memory mapped PSA Signature Register, a signature is generated.

A programmable 20-bit data pattern counter is used for each channel to define the number of data patterns to calculate for each sector. Signature verification can be performed automatically by MCRC controller in AUTO mode or by CPU itself in Semi-CPU or Full-CPU mode. In AUTO mode, a self-sustained CRC signature calculation can be achieved without any CPU intervention.

12.7.3.2.3 MCRC Modes of Operation

MCRC Controller can operate in AUTO, Semi-CPU, and Full-CPU modes.

12.7.3.2.3.1 AUTO Mode

In AUTO mode, MCRC Controller in conjunction with DMA controller can perform CRC without CPU intervention. A sustained transfer of data to both the PSA Signature Register (MCRC64_0_PSA_SIGREGL1-4) and a CRC (Cyclic Redundancy Check) Value Register (MCRC64_0_CRC_REGL1-4) are performed in the background of CPU. When a mismatch is detected, an interrupt is generated to the CPU. A 16-bit, current sector ID register (MCRC64_0_CRC_CURSEC_REG1-4) is provided to identify which sector causes a CRC failure.

12.7.3.2.3.2 Semi-CPU Mode

In Semi-CPU mode, DMA controller is also utilized to perform data patterns transfer to PSA Signature Register (MCRC64_0_PSA_SIGREGL1-4). Instead of performing signature verification automatically, the CRC controller generates an compression complete interrupt to CPU after each sector is compressed. Upon responding to the interrupt the CPU performs the signature verification by reading the calculated signature stored at the PSA Sector Signature Register (MCRC64_0_PSA_SECSIGREGL1-4) and compare it to a pre-determined CRC value.

12.7.3.2.3.3 Full-CPU Mode

In Full-CPU mode, the CPU does the data patterns transfer and signature verification all by itself. When CPU has enough throughput, it can perform data patterns transfer by reading data from the memory system to the PSA Signature Register (MCRC64_0_PSA_SIGREGL1). After certain number of data patterns are compressed, the CPU can read from the PSA Signature Register and compare the calculated signature to the pre-determined CRC signature value. In Full-CPU mode, neither interrupt nor DMA request is generated. All counters are also disabled.

12.7.3.2.4 PSA Signature Register

The 64-bit PSA Signature Register (MCRC64_0_PSA_SIGREGL1-4 and MCRC64_0_PSA_SIGREGH1-4) is based on the primitive polynomial found in (EQ 1) to produce the maximum length LFSR (Linear Feedback Shift Register).

$$f(x) = x^{64} + x^4 + x^3 + x + 1 \tag{3}$$

A. More details of the 64-bit primitive polynomial can be found at W. Stahnke, Primitive binary polynomials, Math. Comp. 27 (1973), 977--980.

There is one PSA Signature Register per CRC channel. PSA Signature Register can be both read and written. When it is written, it can either compress the data or just capture the data depending on the state of CHi_MODE bits (where i = 1 to 4). If CHi_MODE=0x0 (Data Capture), a seed value can be planted in the PSA Signature Register without compression. Other modes other than Data Capture will result with the data compressed by PSA Signature Register when it is written. Each channel can be planted with different seed value before compression starts. When PSA Signature Register is read, it gives the calculated signature.

MCRC Controller should be used in conjunction with the on-chip DMA controller to produce optimal system performance. The incoming data pattern to PSA Signature Register is typically initiated by the DMA controller. When DMA is properly setup, it would read data from the pre-determined memory system and write them to the memory mapped PSA Signature Register. Each time PSA Signature Register is written a signature is generated. CPU itself can also perform data transfer by reading from the memory system and perform write operation to PSA Signature Register if CPU has enough throughput to handle data patterns transfer.

After a system reset and when AUTO mode is enabled, MCRC Controller automatically generates a DMA request to request the pre-determined CRC value corresponding to the first sector of memory to be checked.

In AUTO mode, when one sector of data patterns is compressed, the signature stored at the PSA Signature Register is first copied to the PSA Sector Signature Register (MCRC64_0_PSA_SECSIGREGL1-4) and PSA Signature Register is then cleared out to all zeros. An automatic signature verification is then performed by comparing the signature stored at the PSA Sector Signature Register to the CRC Value Register (MCRC64_0_CRC_REGL1-4). After the comparison the MCRC Controller can generate a DMA request. Upon receiving the DMA request the DMA controller will update the CRC Value Register by transferring the next pre-determined signature value associated with the next sector of memory system. If the signature verification fails then MCRC Controller can generate a CRC fail interrupt.

In Full-CPU mode, no DMA request and interrupt are generated at all. The number of data patterns to be compressed is determined by CPU itself. Full-CPU mode is useful when DMA controller is not available to perform background data patterns transfer. Software can periodically generate a software interrupt to CPU and use CPU to accomplish data transfer and signature verification.

MCRC Controller supports double word, word, half word and byte access to the PSA Signature Register. During a non-doubleword write access, all unwritten byte lanes are padded with zeros before compression. Note that comparison between PSA Sector Signature Register and CRC Value Register is always in 64 bits because a compressed value is always expressed in 64 bits.

There is a software reset per channel for PSA Signature Register. When set, the PSA Signature Register is reset to all zeros.

PSA Signature Register is reset to zero under the following conditions:

- System reset
- PSA Software reset
- One sector of data patterns are compressed

12.7.3.2.5 PSA Sector Signature Register

After one sector of data is compressed, the final resulting signature calculated by PSA Signature Register is transferred to the 64-bit PSA Sector Signature Register (MCRC64_0_PSA_SECSIGREGL1-4 and MCRC64_0_PSA_SECSIGREGH1-4). PSA Signature Register is a read-only register. During Semi-CPU mode, the host CPU must read from the PSA Sector Signature Register instead of reading from PSA Signature Register for signature verification to avoid data coherency issue. The PSA Signature Register can be updated with new signature before the host CPU is able to retrieve it.

In Semi-CPU mode, no DMA request is generated. When one sector of data patterns is compressed, CRC controller first generates a compression complete interrupt. Responding to the interrupt, CPU will read the PSA Sector Signature Register and compare it to the known good signature or write the signature value to another memory location to build a signature file. In Semi-CPU mode, CPU must perform the signature verification in a manner to prevent any overrun condition. The overrun condition occurs when the compression complete interrupt is generated after one sector of data patterns is compressed and CPU has not read from the PSA

Sector Signature Register to perform necessary signature verification before PSA Sector Signature Register is overridden with a new value. An overrun interrupt can be enabled to generate when overrun condition occurs.

12.7.3.2.6 CRC Value Register

Associated with each channel there is a 64-bit CRC Value Register (MCRC64_0_CRC_REGL1-4 and MCRC64_0_CRC_REGH1-4).

The CRC Value Register stores the pre-determined CRC value. After one sector of data patterns is compressed by PSA Signature Register, MCRC Controller can automatically compare the resulting signature stored at the PSA Sector Signature Register with the pre-determined value stored at the CRC Value Register if AUTO mode is enabled. If the signature verification fails, MCRC Controller can be enabled to generate an CRC fail interrupt. When the channel is set up for Semi-CPU mode, CRC controller first generates a compression complete interrupt to CPU. Upon servicing the interrupt, CPU will then read the PSA Sector Signature Register and then read the corresponding CRC value stored at another location and compare them. CPU must not read from the CRC Value Register during Semi-CPU or Full-CPU mode because the CRC Value Register is not updated during these two modes.

In AUTO mode, for first sector’s signature, DMA request is generated when mode is programmed to AUTO. For subsequent sectors, DMA request is generated after each sector is compressed. Responding to the DMA request, DMA controller reloads the CRC Value Register for the next sector of memory system to be checked. The user software needs to configure the DMA to ensure that the DMA first writes to the MCRC64_0_CRC_REGL1 followed by the MCRC64_0_CRC_REGH1 register in during the AUTO Mode.

When CRC Value Register is updated with a new CRC value, an internal flag is set to indicate that CRC Value Register contains the most current value. This flag is cleared when CRC comparison is performed. Each time at the end of the final data pattern compression of a sector, MCRC Controller first checks to see if the corresponding CRC Value Register has the most current CRC value stored in it by polling the flag. If the flag is set then the CRC comparison can be performed. If the flag is not set then it means the CRC Value Register contains stale information. A CRC underrun interrupt is generated. When an underrun condition is detected, signature verification is not performed.

MCRC Controller supports double word, word, half word and byte access to the CRC Value Register. As noted before comparison between PSA Sector Signature Register and CRC Value Register during AUTO mode is carried out in 64 bits.

12.7.3.2.7 Raw Data Register

The raw or un-compressed data written to the PSA Signature Register is also saved in the 64-bit Raw Data Register (MCRC64_0_RAW_DATAREGL1-4 and MCRC64_0_RAW_DATAREGH1-4). This register is read only.

12.7.3.2.8 Example DMA Controller Setup

DMA controller needs to be setup properly in either AUTO or Semi-CPU mode as DMA controller is used to transfer data patterns. Hardware or a combination of hardware and software DMA triggering are supported.

12.7.3.2.8.1 AUTO Mode Using Hardware Timer Trigger

There are two DMA channels associated with each CRC channel when in AUTO mode. One DMA channel is setup to transfer data patterns from the source memory to the PSA Signature Register (MCRC64_0_PSA_SIGREGL1-4). The second DMA channel is setup to transfer the pre-determined signature to the CRC Value Register (MCRC64_0_CRC_REGL1-4). The trigger source for the first DMA channel can be either by hardware or by software. As illustrated in Figure 12-386, a timer can be used to trigger a DMA request to initiate transfer from the source memory system to PSA Signature Register. In AUTO mode, MCRC Controller also generates DMA request after one sector of data patterns is compressed to initiate transfer of the next CRC value corresponding to the next sector of memory. Thus a new CRC value is always updated in the CRC Value Register (MCRC64_0_CRC_REGL1-4)by DMA synchronized to each sector of memory.

A block of system memory is usually divided into many sectors. All sectors are the same size. The sector size is programmed in the MCRC64_0_CRC_PCOUNT_REG1-4 and the number of sectors in one block is programmed in the MCRC64_0_CRC_SCOUNT_REG1-4 of the respective channel.

MCRC64_0_CRC_PCOUNT_REG1-4 multiplies MCRC64_0_CRC_SCOUNT_REG1-4 and multiplies transfer size of each data pattern should give the total block size in number of bytes.

The total size of the memory system to be examined is also programmed in the respective transfer count register inside DMA module. The DMA transfer count register is divided into two parts. They are element count and frame count. Note that a hardware DMA request can be programmed to trigger either one frame or one entire block transfer. In Figure 12-386, a hardware DMA request from a timer is used as a trigger source to initiate DMA transfer. If all four CRC channels are active in AUTO mode then a total of four DMA requests would be generated by MCRC Controller.

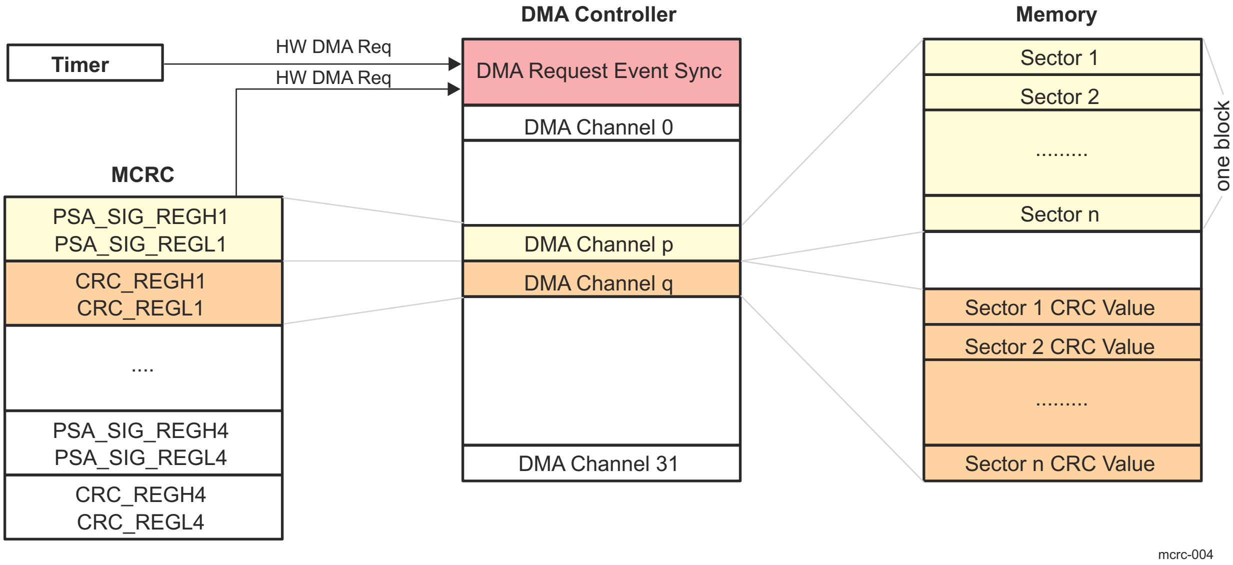


Figure 12-386. AUTO Mode Using Hardware Timer Trigger

12.7.3.2.8.2 AUTO Mode Using Software Trigger

The data patterns transfer can also be initiated by software. CPU can generate a software DMA request to activate the DMA channel to transfer data patterns from source memory system to the PSA Signature Register. To generate a software DMA request CPU needs to set the corresponding DMA channel in the DMA software trigger register. Note that just one software DMA request from CPU is enough to complete the entire data patterns transfer for all sectors. Please see Figure 12-387 for illustration.

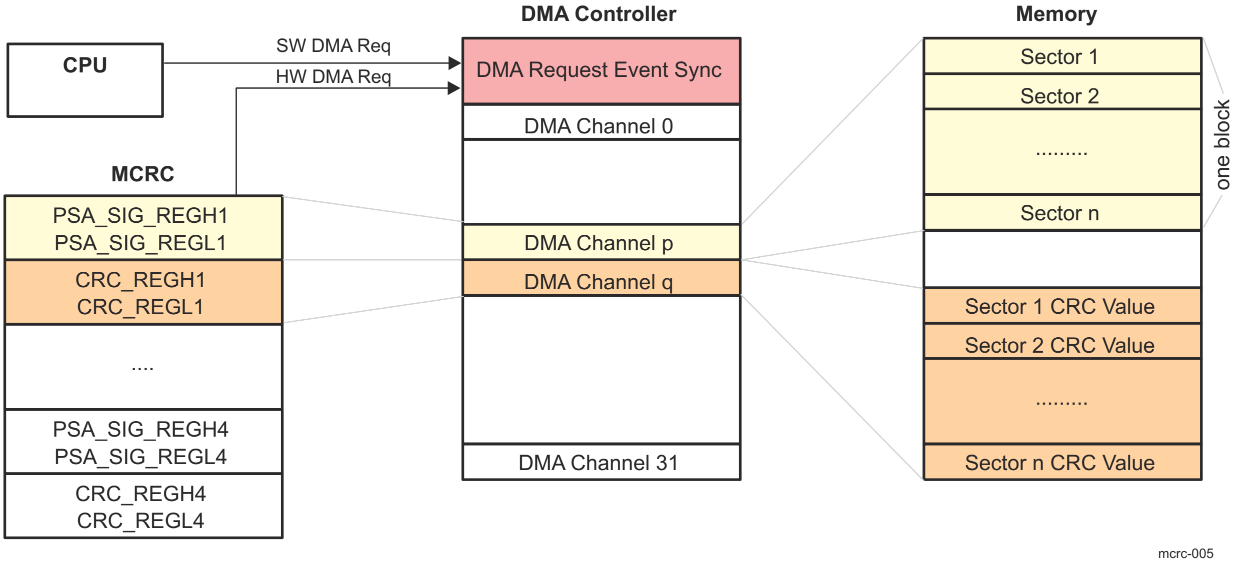


Figure 12-387. AUTO Mode With Software CPU Trigger

12.7.3.2.8.3 Semi-CPU Mode Using Hardware Timer Trigger

During Semi-CPU mode, no DMA request is generated by CRC controller. Therefore, no DMA channel is allocated to update CRC Value Register. CPU should not read from CRC Value Register in semi-CPU mode as it contains stale value. Note that no signature verification is performed at all during this mode. Similar to AUTO mode, either by hardware or by software DMA request can be used as a trigger for data patterns transfer. Figure 12-388 illustrates the DMA setup using semi-CPU mode with hardware timer trigger.

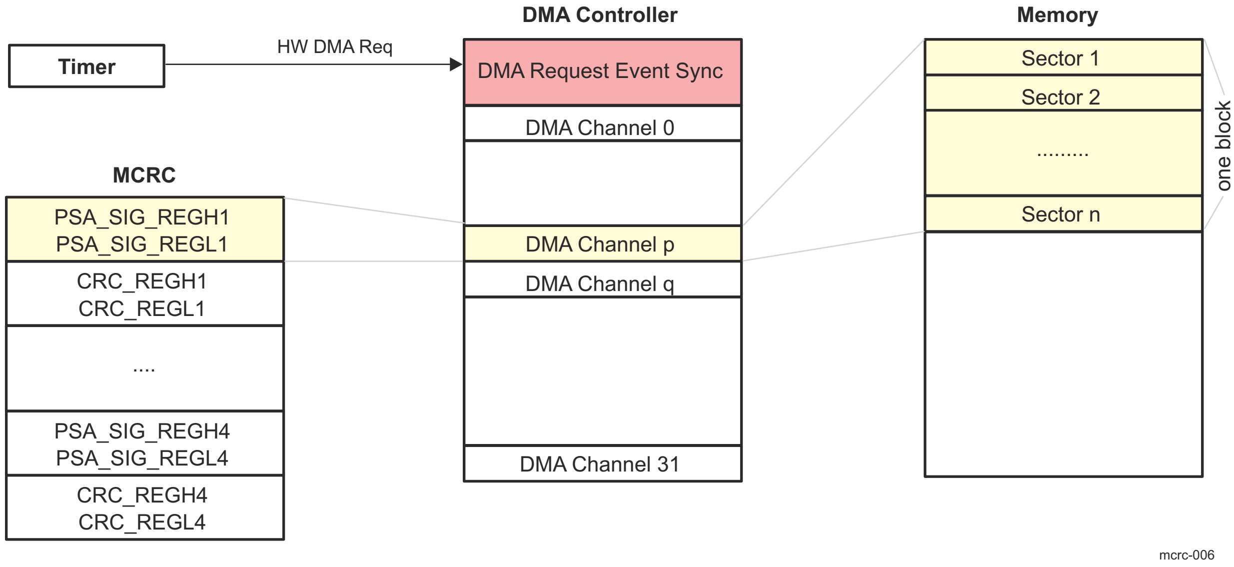


Figure 12-388. Semi-CPU Mode With Hardware Timer Trigger

Table 12-328. DMA Request and Counter Logic Operation According to CRC Mode

CRC Mode	DMA Request	Pattern Counter	Sector Counter	Timeout Counter
AUTO	Active	Active	Active	Active
Semi-CPU	Inactive	Active	Active	Active
Full CPU	Inactive	Inactive	Inactive	Inactive

12.7.3.2.9 Pattern Count Register

There is a 20-bit data pattern counter for every CRC channel. The data pattern counter is a down counter and can be pre-loaded with a programmable value stored in the Pattern Count Register (MCRC64_0_CRC_PCOUNT_REG1-4). When the data pattern counter reaches zero, a compression complete interrupt is generated in Semi-CPU mode and an automatic signature verification is performed in AUTO mode. In AUTO only, DMA request is generated to trigger the DMA controller to update the CRC Value Register.

Note

The data pattern count must be divisible by the total transfer count as programmed in DMA controller. The total transfer count is the product of element count and frame count.

12.7.3.2.10 Sector Count Register/Current Sector Register

Each channel contains a 16-bit sector counter. The sector count register stores the number of sectors. Sector counter is a free running counter and is incremented by one each time when one sector of data patterns is compressed. When the signature verification fails, the current value stored in the sector counter is saved into current sector register (MCRC64_0_CRC_CURSEC_REG1-4). If signature verification fails, CPU can read from the current sector register to identify the sector which causes the CRC mismatch. To aid and facilitate the CPU in determining the cause of a CRC failure it is advisable to use the following equation during CRC and DMA setup.

$$\text{CRC Pattern Count} \times \text{CRC Sector Count} = \text{DMA Element Count} \times \text{DMA Frame Count} \quad (4)$$

The current sector register is frozen from being updated until both the current sector register is read and CRC fail (CHi_CRC_FAIL) status bit is cleared by CPU. If CPU does not respond to the CRC failure in a timely manner before another sector produces a signature verification failure, the current sector register is not updated with the new sector number. An overrun interrupt is generate instead. If current sector register is already frozen with an erroneous sector and emulation is entered with SUSPEND signal goes to high then the register still remains frozen even it is read.

In Semi-CPU mode, the current sector register is used to indicate the sector for which the compression complete has last happened.

Current sector register is reset when the PSA software reset is enabled.

Note

Both data pattern count and sector count registers must be greater than or equal to one for the counters to count. After reset, pattern count and sector count registers default to zero and the associated counters are inactive.

12.7.3.2.11 Interrupts

CRC generate several types of interrupts per channel. Associated with each interrupt there is a interrupt enable bit (see MCRC64_0_CRC_INTS). No interrupt is generated in Full-CPU mode.

- Compression complete interrupt
- CRC fail interrupt
- Overrun interrupt
- Underrun interrupt
- Timeout interrupt

Table 12-329. Interrupt Conditions Per CRC Mode

CRC Mode	Compression Complete	CRC Fail	Overrun	Underrun	Timeout
AUTO	No	Yes	Yes	Yes	Yes
Semi-CPU	Yes	No	Yes	No	Yes
Full-CPU	No	No	No	No	No

12.7.3.2.11.1 Overrun Interrupt

Overrun Interrupt is generated in either AUTO or Semi-CPU mode. During AUTO mode, if a CRC fail is detected then the current sector number is recorded in the current sector register (MCRC64_0_CRC_CURSEC_REG1-4). If CRC fail status bit is not cleared and current sector register is not read by the host CPU before another CRC fail is detected for another sector then an overrun interrupt is generated. During Semi-CPU mode, when the data pattern counter finishes counting, it generates a compression complete interrupt. At the same time the signature is copied into the PSA Sector Signature Register (MCRC64_0_PSA_SECSIGREGL1-4). If the host CPU does not read the signature from PSA Sector Signature Register before it is updated again with a new signature value then an overrun interrupt is generated.

12.7.3.2.11.2 Timeout Interrupt

To ensure that the memory system is examined within a pre-defined time frame and no loss of incoming data there is a 24-bit timeout counter per CRC channel. The timeout counter can be pre-loaded with two different pre-load values, watchdog timeout pre-load value (MCRC64_0_CRC_WDTOPLD1-4) and block complete timeout pre-load value (MCRC64_0_CRC_BCTOPLD1-4). The timeout counter is clocked by a prescaler clock which is permanently running at division 64 of FICLK clock.

Watchdog timeout pre-load register (MCRC64_0_CRC_WDTOPLD1-4) is used to check if DMA does supply a block of data responding to a request in a given time frame. Block complete timeout pre-load register (MCRC64_0_CRC_BCTOPLD1-4) is used to check if one complete block of data patterns are compressed within a specific time frame. The timeout counter is first pre-loaded with MCRC64_0_CRC_WDTOPLD1-4 after either AUTO or Semi-CPU mode is selected and starts to down count. If the timeout counter expires before DMA transfers any data pattern to PSA Signature Register then a timeout interrupt is generated. An incoming data pattern before the timeout counter expires will automatically pre-load the timeout counter with MCRC64_0_CRC_BCTOPLD1-4 the block complete timeout pre-load value.

Block complete timeout pre-load value is used to check it one block of data patterns are compressed within a given time limit. If the timeout counter pre-loaded with MCRC64_0_CRC_BCTOPLD1-4 value expires before one block of data patterns are compressed a timeout interrupt is generated. When one block (pattern count × sector count) of data patterns are compressed before the counter has expired, the counter is pre-loaded with MCRC64_0_CRC_WDTOPLD1-4 value again. If the timeout counter is pre-loaded with zero then the counter is disable and no timeout interrupt is generated.

12.7.3.2.11.3 Underrun Interrupt

Underrun interrupt only occurs in AUTO mode. The interrupt is generated when the CRC Value Register is not updated with the corresponding signature when the data pattern counter finishes counting. During AUTO mode, MCRC Controller generates DMA request to update CRC Value Register in synchronization to the corresponding sector of the memory. Signature verification is also performed if underrun condition is detected. And CRC fail interrupt is generated at the same time as the underrun interrupt.

12.7.3.2.11.4 Compression Complete Interrupt

Compression complete interrupt is generated in Semi-CPU mode only. When the data pattern counter reaches zero, the compression complete flag is set and the interrupt is generated

12.7.3.2.11.5 Interrupt Offset Register

MCRC Controller only generates one interrupt request to interrupt manager. An interrupt offset register (MCRC64_0_CRC_INT_OFFSET_REG) is provided to indicate the source of the pending interrupt with highest priority. Table 12-330 shows the offset interrupt vector address of each interrupt in an ascending order of priority.

Table 12-330. Interrupt Offset Mapping

Interrupt Condition	Offset Value
Phantom	0x0
Ch1 CRC Fail	0x1
Ch2 CRC Fail	0x2
Ch3 CRC Fail	0x3
Ch4 CRC Fail	0x4
reserved	0x5-0x8
Ch1 Compression Complete	0x9
Ch2 Compression Complete	0xA
Ch3 Compression Complete	0xB
Ch4 Compression Complete	0xC
reserved	0xD-0x10
Ch1 Overrun	0x11
Ch2 Overrun	0x12
Ch3 Overrun	0x13
Ch4 Overrun	0x14
reserved	0x15-0x18
Ch1 Underrun	0x19
Ch2 Underrun	0x1A
Ch3 Underrun	0x1B
Ch4 Underrun	0x1C
reserved	0x1D-0x20
Ch1 Timeout	0x21
Ch2 Timeout	0x22
Ch3 Timeout	0x23

Table 12-330. Interrupt Offset Mapping (continued)

Interrupt Condition	Offset Value
Ch4 Timeout	0x24

12.7.3.2.11.6 Error Handling

When an interrupt is generated, host CPU must take appropriate actions to identify the source of error and restart the respective channel in DMA and MCRC module. To restart a CRC channel user must perform the following steps in the ISR:

1. Write to software reset bit in MCRC64_0_CRC_CTRL0 register to reset the respective PSA Signature Register
2. Reset the CHi_MODE bits to 0 in MCRC64_0_CRC_CTRL2 register as Data capture mode
3. Set the CHi_MODE bits in MCRC64_0_CRC_CTRL2 register to desired new mode again
4. Release software reset

The host CPU must use byte write to restart each individual channel.

12.7.3.2.12 Power Down Mode

MCRC module can be put into power down mode when the power down control bit MCRC64_0_CRC_CTRL1[0] PWDN is set. The module wakes up when the PWDN bit is cleared. When MCRC controller is in power down mode, no data tracing alone will happen.

12.7.3.2.13 Emulation

A read access from a register in functional mode can sometimes trigger a certain internal event to follow. For example, reading interrupt offset register triggers an event to clear the corresponding interrupt status flag. During emulation when SUSPEND signal is high, a read access from any register should only return the register contents to the bus and should not trigger or mask any event as it would have in functional mode. This is to prevent debugger from reading the interrupt offset register, that is, during refreshing screen and cause the corresponding interrupt status flag to get cleared. Timeout counters are stopped to generate timeout interrupts in emulation mode. No VBUSM bus error will be generated if reading from the unimplemented locations. .

CEMUDBG is the VBUSM suspend signal which need not explicitly indicate that whether CPU is in suspend mode or not. In data trace mode, a separate suspend signal CPU_EMUSP, is used to indicate MCRC controller that the CPU is in suspend mode or not.

12.7.3.3 MCRC Programming Examples

12.7.3.3.1 Example: Auto Mode Using Time Based Event Triggering

A large memory area with 2 Mbyte (256 k × 32-bit [doubleword]) is to be checked in the background of CPU. CRC is to be performed every 1 Kbyte (128 doubleword). Therefore there will be 2048 pre-recorded CRC values. For illustration purpose, we map MCRC64_0_CRC_REGL1 register to DMA channel 1 and MCRC64_0_PSA_SIGREGL1 register to DMA channel 2. Let's assume all DMA transfers are carried out in 64-bit transfer size.

12.7.3.3.1.1 DMA Setup

- Setup DMA channel 1 with the starting address from which the pre-determined CRC values are stored. Setup the destination address to the MCRC64_0_CRC_REGL1. Put the source address at post increment addressing mode and put the destination address at constant addressing mode. Use hardware DMA request for channel 1 to trigger a frame transfer.
- Setup DMA channel 2 with the source address from which the contents of memory to be verified. Setup the destination address to the MCRC64_0_PSA_SIGREGL1. Program the element transfer count to 128 and the frame transfer count to 2048. Program the read and write element size to 64 bits. Put the source address at post increment addressing mode and put the destination address at constant address mode. Use hardware DMA request for channel 2 to trigger an entire block transfer.

12.7.3.3.1.2 Timer Setup

The timer can be any general purpose timer which is capable of generating a time based DMA request.

- Setup Timer to generate DMA request associated with DMA channel 2. For example, software can setup the timer to generate a DMA request every 10 ms.

12.7.3.3.1.3 CRC Setup

- Program the pattern count MCRC64_0_CRC_PCOUNT_REG1 to 128
- Program the sector count MCRC64_0_CRC_SCOUNT_REG1 to 2048
- For example, we want the entire 2 Mbytes to be compressed within 5 ms. We can program the block complete timeout pre-load (MCRC64_0_CRC_BCTOPLD1-4) value to 15625 (5 ms / (1 FICLK period × 64)) if CRC is operating at 200 MHz.
- Enable AUTO mode and all interrupts.

After AUTO mode is selected MCRC Controller automatically generates a DMA request on channel 1. Around the same time the timer module also generates a DMA request on DMA channel 2. When the first incoming data pattern arrives at the MCRC64_0_PSA_SIGREGL1/H1, the MCRC Controller will compress it. After some time, the DMA controller would update the CMCRC_CRC_REGL1/H1 with a pre-determined value matching the calculated signature for the first sector of 128 64-bit data patterns. After one sector of data patterns are compressed, the MCRC Controller generate a CRC fail interrupt if signature stored at the MCRC64_0_PSA_SECSIGREGL1/H1 does not match the MCRC64_0_CRC_REGL1/H1 Register. MCRC Controller generates a DMA request on DMA channel 1 when one sector of data patterns are compressed. This routine will continue until the entire 2 Mbytes are consumed. If the timeout counter reached zero before the entire 2 Mbytes are compressed, a timeout interrupt is generated. After 2Mbytes are transferred, the DMA can generate an interrupt to CPU. The entire operation will continue again when DMA responds to the DMA request from both the timer and MCRC Controller. The CRC is performed totally without any CPU intervention.

12.7.3.3.2 Example: Auto Mode Without Using Time Based Triggering

A small but highly secured memory area with 1 Kbytes is to be checked in the background of CPU. CRC is to be performed every 1 Kbytes. Therefore, there is only one pre-recorded CRC value. For illustration purpose, we map channel 1 MCRC64_0_CRC_REGL1/H1 to DMA channel 1 and channel 1 MCRC64_0_PSA_SIGREGL1/H1 to DMA channel 2. Assume all transfers carried out by DMA are in 64-bit transfer size.

12.7.3.3.2.1 DMA Setup

- Setup DMA channel 1 with the source address from which the pre-determined CRC value is stored. Setup the destination address to the MCRC64_0_CRC_REGL1 Register. Put the source address at constant addressing mode and put the destination address at constant addressing mode. Use hardware DMA request for channel 1.

- Setup DMA channel 2 with the source address from which the memory area to be verified. Setup the destination address to the MCRC64_0_PSA_SIGREGL1/H1. Program the element transfer count to 128 and the frame transfer count to 1. Put the source address at post increment addressing mode and put the destination address at constant address mode. Generate a software DMA request on channel 2 after CRC has completed its setup. Enable autoinitiation for DMA channel 2.

12.7.3.3.2.2 CRC Setup

- Program the MCRC64_0_CRC_PCOUNT_REG1 to 128
- Program the MCRC64_0_CRC_SCOUNT_REG1 to 1
- Leaving the timeout count MCRC64_0_CRC_BCTOPLD1 register with the reset value of zero means no timeout interrupt is generated
- Enable AUTO mode and all interrupts

After AUTO mode is selected the MCRC Controller automatically generates a DMA request on channel 1. At the same time the CPU generates a software DMA request on DMA channel 2. When the first incoming data pattern arrives at the MCRC64_0_PSA_SIGREGL1/H1, the MCRC Controller will compress it. After some time, the DMA controller would update the MCRC64_0_CRC_REGL1/H1 with a pre-determined value matching the calculated signature for the first sector of 128 64-bit data patterns. After one sector of data patterns are compressed, the MCRC Controller generate a CRC fail interrupt if signature stored at the MCRC64_0_PSA_SECSIGREGL1/H1 does not match the MCRC64_0_CRC_REGL1/H1. MCRC Controller generate a DMA request on DMA channel 1 again after one sector is compressed. After 1 Kbytes are transferred, the DMA can generate an interrupt to CPU. Responding to the DMA interrupt CPU can restart the CRC routine by generating a software DMA request onto channel 2 again.

12.7.3.3.3 Example: Semi-CPU Mode

If DMA controller is available in a system the CRC module can also operate in semi-CPU mode. This means that CPU can still make use of the DMA to perform data patterns transfer to CRC controller in the background. The difference between semi-CPU mode and AUTO mode is that CRC controller does not automatically perform the signature verification. CRC controllers generates a compression complete interrupt to CPU when the one sector of data patterns are compressed. CPU needs to perform the signature verification itself.

A memory area with 2 Mbytes is to be verified with the help of the CPU. CRC operation is to be performed every 1 Kbyte. Since there are 2 Mbytes (256 K doublewords) of memory to be check and we want to perform a CRC every 1 Kbytes (128 doublewords) and therefore there must be 2048 pre-recorded CRC values. In Semi-CPU mode, the MCRC64_0_CRC_REGL1/H1 is not updated and contains indeterminate data.

12.7.3.3.3.1 DMA Setup

- Setup DMA channel 1 with the source address from which the memory area to be verified are mapped. Setup the destination address to the MCRC64_0_PSA_SIGREGL1/H1. Put the starting address at post increment addressing mode and put the destination address at constant address mode. Use hardware DMA request to trigger an entire block transfer for channel 1. Disable autoinitiation for DMA channel 1.

12.7.3.3.3.2 Timer Setup

The timer can be any general purpose timer which is capable of generating a time-based DMA request.

- Setup Timer to generate DMA request associated with DMA channel 1. For example, software can setup the timer to generate a DMA request every 10 ms.

12.7.3.3.3.3 CRC Setup

- Program the MCRC64_0_CRC_PCOUNT_REG1 to 128
- Program the MCRC64_0_CRC_SCOUNT_REG1 to 2048
- For example, we want the entire 2 Mbytes to be compressed within 5 ms. We can program the block complete timeout pre-load value MCRC64_0_CRC_BCTOPLD1 to 15625 (5 ms / (1 FICLK period × 64)) if CRC is operating at 200 MHz
- Enable AUTO mode and all interrupts.

The timer module first generates a DMA request on DMA channel 1 when it is enabled. When the first incoming data pattern arrives at the MCRC64_0_PSA_SIGREGL1/H1, the CRC controller will compress it. After one sector of data patterns are compressed, the CRC controller generate a compression complete interrupt. Upon responding to the interrupt the CPU would read from the MCRC64_0_PSA_SECSIGREGL1/H1. It is up to the CPU on how to deal with the PSA value just read. It can compare it to a known signature value or it can write it to another memory location to build a signature file or even transfer the signature out of the device via SCI or SPI. This routine will continue until the entire 2 Mbytes are consumed. The latency of the interrupt response from CPU can cause overrun condition. If CPU does not read from MCRC64_0_PSA_SECSIGREGL1 before the PSA value is overridden with the signature of the next sector of memory, an overrun interrupt will be generated by CRC controller.

12.7.3.3.4 Example: Full-CPU Mode

In a system without the availability of DMA controller, the CRC routine can be operated by CPU provided the CPU has enough throughput. CPU needs to read from the memory area from which CRC is to be performed.

A memory area with 2 Mbytes is to be checked with the help of the CPU. CRC operation is to be performed every 1 Kbyte. In CPU mode, the MCRC64_0_CRC_REGL1/H1 is not updated and contains indeterminate data.

12.7.3.3.4.1 CRC Setup

- All control registers can be left in their reset state. Only enable Full-CPU mode.

CPU itself reads from the memory and write the data to the MCRC64_0_PSA_SIGREGL1/H1 inside MCRC Controller. When the first incoming data pattern arrives at the MCRC64_0_PSA_SIGREGL1/H1, the MCRC Controller will compress it. After n data patterns are compressed, CPU can read from the MCRC64_0_PSA_SIGREGL1/H1. It is up to the CPU on how to deal with the PSA signature value just read. It can compare it to a known signature value stored at another memory location.

12.7.4 ECC Aggregator

This section describes the common ECC aggregator functionality.

12.7.4.1 ECC Aggregator Overview

To increase functional and system reliability the memories (for example, FIFOs, queues, SRAMs and others) in many device modules and subsystems are protected by error correcting code (ECC). This is accomplished through an ECC aggregator and ECC wrapper. The ECC aggregator is connected to these memories (hereinafter ECC RAMs) and involved in the ECC process. Each memory is surrounded by an ECC wrapper which performs the ECC detection and correction. The wrapper communicates via serial interface with the aggregator which has memory mapped configuration interface.

The ECC aggregator is also connected to interconnect ECC components that protect the command, address and data buses of the system interconnect. ECC is calculated for the data bus and parity and redundancy for the command and address buses. Each interconnect ECC component has the same serial interface for communication with the aggregator as the ECC wrapper. An ECC aggregator may be connected to both endpoints - the ECC wrapper and interconnect ECC component.

The ECC aggregator, ECC wrapper and interconnect ECC component are considered as single entity and are hereinafter referred to as ECC aggregator unless otherwise explicitly specified.

See *Module Integration* for device modules and subsystems which have ECC aggregator.

12.7.4.1.1 ECC Aggregator Features

The ECC aggregator has the following features:

- Reduces memory software errors via single error correction (SEC) and double error detection (DED)
- Provides a mechanism to control and monitor the ECC protected memories in a module or subsystem
- SEC and DED over the system interconnect data bus and parity and redundancy for the system interconnect command and address buses
- Generates an interrupt for correctable error
- Generates an interrupt for non-correctable error
- Supports inject only mode for diagnostic purposes
- Supports software readable status for single and double-bit ECC errors and associated information such as row address where error has occurred and data bits that have been flipped
- Supports up to 256 ECC endpoints. An ECC endpoint can be either ECC RAM or interconnect ECC component.
- Detects single bit error via parity checking on:
  - Memory mapped configuration interface FIFO
  - Serial interface FIFO
  - Serial interface transaction
- Single bit error detection via parity checking results in a non-correctable error interrupt
- Supports timeout mechanism on transactions over the ECC serial interface. Timeout occurrence results in a non-correctable error interrupt.
- Certain control bits have redundancy and if a bit flips an interrupt is generated

12.7.4.1.2 Unsupported Features

See the *Module Integration* section for information about unsupported features.

12.7.4.2 ECC Aggregator Functional Description

This section describes the architecture and functional details of the ECC aggregator.

12.7.4.2.1 ECC Aggregator Block Diagram

Figure 12-389 shows the ECC aggregator block diagram.

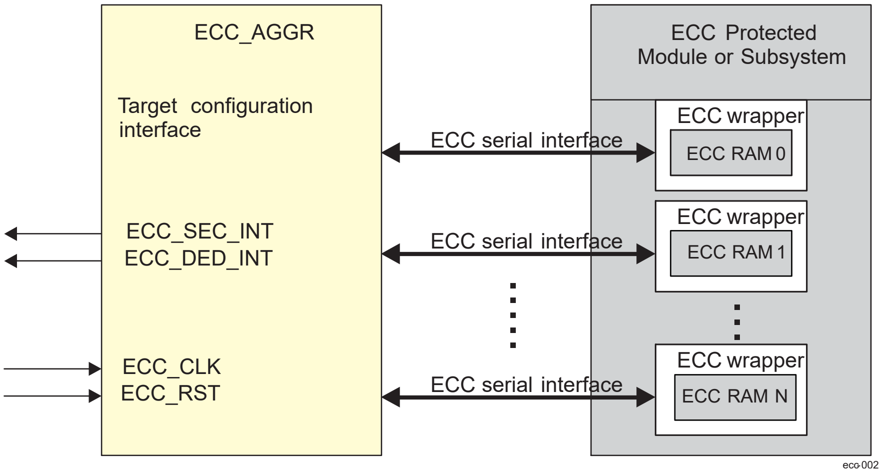


Figure 12-389. ECC Aggregator Block Diagram

The ECC aggregator is connected to one or more ECC endpoints each of which has assigned a unique ID used when the endpoint is accessed for status information or configuration. The ECC aggregator provides software access to all ECC related registers through its memory mapped target configuration interface while the serial interface is used to communicate with the ECC endpoints. Upon detection of single or double-bit error the corresponding interrupt line is asserted.

12.7.4.2.2 ECC Aggregator Register Groups

The ECC aggregator has ECC control, status and interrupt registers for each ECC endpoint in a module or subsystem. These registers are memory mapped and occupy 1 KB address space although part of it may contain reserved locations. The registers are split in the following types:

- **Global registers**. They are common to all ECC endpoints associated with the ECC aggregator and include the ECC_VECTOR and ECC_REV registers. Each ECC endpoint has assigned a unique ID. When this ID is written to the ECC_VECTOR[10-0] ECC_VECTOR field the corresponding endpoint is selected either for control or for status reading.
- **ECC control and status registers**. These registers are specific to each ECC endpoint and reside in the range from address offset 0x10 to 0x28, if the endpoint is ECC RAM or from 0x10 to 0x24, if the endpoint is interconnect ECC component. They are memory mapped but are accessed through the ECC serial interface. They are also selected by the ECC endpoint ID written to the ECC_VECTOR[10-0] ECC_VECTOR field. Because of latency on the serial interface the ECC control and status registers are read by performing special sequence as described in Section 12.7.4.2.3. These registers have also different functionality for both types of endpoints - ECC RAM and interconnect ECC component.
- **Interrupt registers**. They include interrupt status, interrupt enable, interrupt disable, and EOI registers. For more information, see *Interrupts*.

Note

For description of each register, see *ECC_AGGR Registers*.

12.7.4.2.3 Read Access to the ECC Control and Status Registers

Read accesses to the ECC control and status registers for each ECC endpoint represent read operations over the ECC serial interface and are triggered by performing the following sequence:

1. Software writes the following in the ECC_VECTOR register:
   - The ECC endpoint ID in the ECC_VECTOR[10-0] ECC_VECTOR field to select particular ECC endpoint.
   - The register read address in the ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field to select which register has to be read through the ECC serial interface.
   - A value of 0x1 in the ECC_VECTOR[15] RD_SVBUS bit to trigger read operation through the ECC serial interface.
2. Software polls the ECC_VECTOR[24] RD_SVBUS_DONE bit to check if it is 0x1. This indicates that the read operation on the ECC serial interface has completed.
3. Software reads the data from the register previously selected by the ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field.

The following is an example for serial read operation:

1. Write 0x0010 8005 to the ECC_VECTOR register. This sends read request to the ECC_WRAP_REV or ECC_CBASS_REV register (address = 0x10) associated with ECC endpoint with ID = 5.
2. Poll the ECC_VECTOR[24] RD_SVBUS_DONE bit until value of 0x1 is read.
3. Read the ECC_WRAP_REV or ECC_CBASS_REV register to get its value.

12.7.4.2.4 Serial Write Operation

Write operations over the ECC serial interface are performed as follows:

1. Software specifies the ECC endpoint ID in the ECC_VECTOR[10-0] ECC_VECTOR field. The ECC_VECTOR[23-16] RD_SVBUS_ADDRESS field is a don't care but the ECC_VECTOR[15] RD_SVBUS bit must be set to 0x0.
2. Software performs regular write operation to the desired address. If the ECC endpoint ID has already been specified, step 1 can be skipped. Unlike serial read operations it is not necessary to always specify the endpoint ID before performing serial write operation.

The following is an example for serial write operation:

1. Write 0x0000 0008 to the ECC_VECTOR register.
2. Write 0x0000 000F to the ECC_CTRL register. This sends write request with data 0x0000 000F to the ECC_CTRL register associated with ECC RAM with ID = 8.

12.7.4.2.5 Interrupts

The ECC aggregator generates the following interrupts:

- Correctable interrupt (ECC_SEC_INT) where hardware can correct the error but notifies the system in case of SEC.
- Non-correctable interrupt (ECC_DED_INT) where hardware cannot correct the error in cases of DED, parity check, redundancy check or timeout occurrence.

The following is the sequence for servicing interrupts:

- Software enables the interrupts for an ECC endpoint by writing 0x1 to the corresponding bit of the following interrupt enable registers:
  - ECC_SEC_ENABLE_SET_REG0 through ECC_SEC_ENABLE_SET_REG7 for the correctable interrupt
  - ECC_DED_ENABLE_SET_REG0 through ECC_DED_ENABLE_SET_REG7 for the non-correctable interrupt
- On receiving an interrupt, software checks which ECC endpoint has caused the error by reading the following interrupt status registers:
  - ECC_SEC_STATUS_REG0 through ECC_SEC_STATUS_REG7 for the correctable interrupt
  - ECC_DED_STATUS_REG0 through ECC_DED_STATUS_REG7 for the non-correctable interrupt
- Software performs serial read operations as described in Section 12.7.4.2.3 to read the following status registers that contain details about the error:

  - If the endpoint is ECC RAM:
    - ECC_ERR_STAT1
    - ECC_ERR_STAT2
    - ECC_ERR_STAT3
  - If the endpoint is interconnect ECC component:
    - ECC_CBASS_ERR_STAT1
    - ECC_CBASS_ERR_STAT2
- After the interrupt has been serviced, depending on the error type, software should clear the corresponding status bits in the ECC_ERR_STAT1 and ECC_ERR_STAT3 registers or in the ECC_CBASS_ERR_STAT1 register. Software has to poll these registers to guarantee that status bits are cleared as there is no other indication for write completion over the ECC serial interface.
  The value of the *_PEND_CLR fields in the ECC_CBASS_ERR_STAT1 register must be read and then written back to decrement the count of each field back to 0x0. A further error capture into the ECC_CBASS_ERR_STAT1 register does not occur unless all its fields are 0x0. The decrement value should not be larger than the read value. If a field in the ECC_CBASS_ERR_STAT1 register should not be modified, write a value of 0x0 to that field.
- Software writes 0x1 to the corresponding end of interrupt register to clear the interrupt:
  - ECC_SEC_EOI_REG for the correctable interrupt
  - ECC_DED_EOI_REG for the non-correctable interrupt

12.7.4.2.6 Inject Only Mode

There are modules that already perform the ECC generation and checking as part of their data path. In this case, the ECC wrapper may be configured in inject only mode, if needed. In this mode the ECC wrapper does not perform ECC detection and correction. The inject only mode allows users to inject single or double-bit errors so that the module logic can be tested for diagnostic purposes.

Note

There is no software control to enable inject only mode. It is configured via tie-off value. Inject only and ECC modes are mutually exclusive.

The interconnect ECC component also supports error injection mode. There is error injection logic for testing of the error checking logic (checkers). The injection logic can be configured to inject either single or double bit error and what data pattern to be used for injection (ECC_CBASS_CTRL[11-8] ECC_PATTERN). The ECC_CBASS_ERR_CTRL1 and ECC_CBASS_ERR_CTRL2 registers should be written first to setup the injection. Then, either the ECC_CBASS_CTRL[3] FORCE_SE or the ECC_CBASS_CTRL[4] FORCE_DE bit must be set to 0x1 to start the injection. Both bits must not be set at the same time. If the injection should continue in incrementing mode, then the ECC_CBASS_CTRL[5] FORCE_N_BIT bit should be set to 0x1. Once the FORCE_N_BIT is set, then each successive injection can simply write the ECC_CBASS_CTRL register to set the FORCE_SE or FORCE_DE again. Reading 0x0 from either the FORCE_SE or the FORCE_DE bit indicates that the injection has completed, as these bits automatically clear when the checker indicates that it has performed the injection. The time for an injection to complete is not guaranteed, so some delay is needed between successive injections.

12.7.5 Interconnect ECC Aggregators

13 On-Chip Debug

This chapter describes the on-chip debug support.

Note

This chapter serves to provide the reader an understanding of the device's debug capability and does not provide the sufficient operational and integration details necessary to develop tooling support around it. Tools developers that wish to provide support for this device can contact TI for more information on how to obtain the appropriate documentation.

13.1 On-Chip Debug Overview

This chapter describes the properties and capabilities of the various features available through the On-Chip Debug framework deployed on this device.

The On-Chip Debug framework enables various Debug and Trace use-cases, including:

- **JTAG Tooling** – Access to on-chip debug resources are supported by an IEEE 1149.1 (JTAG) compliant interface that is supported by an Arm® CoreSight™ DAP JTAG-DP.
- **Self-Hosted Tooling** – code running on programmable cores within the device is able to use on-chip debug resources to enable embedded tooling solutions.
- **PCB-level interconnect testing** – IEEE 1149.1 and IEEE 1149.6 compliant Boundary Scan supports product level integration testing
- **Low Power Operation** – When on-chip JTAG and debug management logic is in a low power state, activity sensed on the JTAG interface will cause this logic to be placed in a functional state.
- **Stop Mode debugging** – Debug of embedded processors is supported using various mechanisms that can halt the pipeline of a CPU. Breakpoints (Software and Hardware), Watchpoints, Cross-Triggering, and On-demand (e.g. user requested) halt request mechanisms may be supported based on the capabilities of a given processor.
- **Debug-aware Peripherals** – Peripheral awareness of processor execution state allows safe suspension of peripheral operation. Supported by select peripherals.
- **Synchronized Debug** – Wide deployment of Cross-Triggering allows multiple processors and/or debug elements to be grouped together to process various actions based on a common event occurrence.
- **Processor Trace** – Support for the generation of a trace stream with the encoding of processor state that may include some combination of program flow, timing details (execution and stall), and memory references (address and/or data) with the goal of facilitating processor state reconstruction for debug purposes.
- **Software Messaging Trace** – Support for software messaging trace where embedded code running within the device can be instrumented to use memory writes to send important debug information to a trace stream.
- **System Traffic Trace** – Strategically selected points in the SoC topology are instrumented with trace-capable bus probes that support transaction trace, read-latency monitoring, and throughput computation.
- **Trace Correlation (through timestamping)** – Support for the correlation of different trace streams is enabled through the use of a common global timestamp that is distributed to supported trace sources.
- **Trace data movement** – Trace data movement on chip is supported using standard Arm ATB trace infrastructure components. Concurrent use of the trace bus by multiple trace sources is supported, with each trace source identifiable through a unique ID. An Arm CoreSight Trace Router supports sending a trace stream off-chip (TPIU), to dedicated memory on-chip (TBR), or broadcasted to both (TPIU + TBR).
- **On-Chip trace collection via dedicated buffer** – An on-chip trace buffer is supported by logic that implements capturing trace data until either the memory fills (stop-on-full, system-bridge) or continuously until a request to stop is received (circular buffer). Interleaving of multiple trace, streams is made possible through the use of a standardized encoding that embeds trace data along with the corresponding trace source ID.
- **Trace export over TPIU** – Trace data is exported over device LVCMOS pins using a standard protocol that embeds trace data along with the corresponding trace source ID.
- **Trace export over USB** – The on-chip trace buffer is used as an intermediate buffer allowing trace data to be exported over an USB endpoint in real-time.

13.2 On-Chip Debugs Features

The On-Chip Debug framework provides a comprehensive hardware platform for a rich debug and development experience. The On-Chip Debug framework supports these features:

- An IEEE 1149.1 (JTAG and Boundary Scan) compliant device interface
- Cross-triggering and Debug boot mode device interface
- Trace port device interface
- Advanced power, reset, and clock management to facilitate debug across complex low power modes
- Breakpoint-based debug
- Cross-triggering
- Program flow trace
- System traffic monitoring trace

- Software instrumentation trace
- Trace export via trace port device interface
- Trace capture on-chip via dedicated buffer with options to support stop-on-full, circular-buffer, or data hand-off to various peripherals
- Arm® CoreSight™ compliant debug components deployed to streamline 3rd party tooling support

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Note

Some features may not be available. See *Module Integration* for more information.

13.3 On-Chip Debug Functional Description

13.3.1 Block Diagram

A logical partitioning of the On-Chip Debug features deployed on this device is illustrated in the figure below.

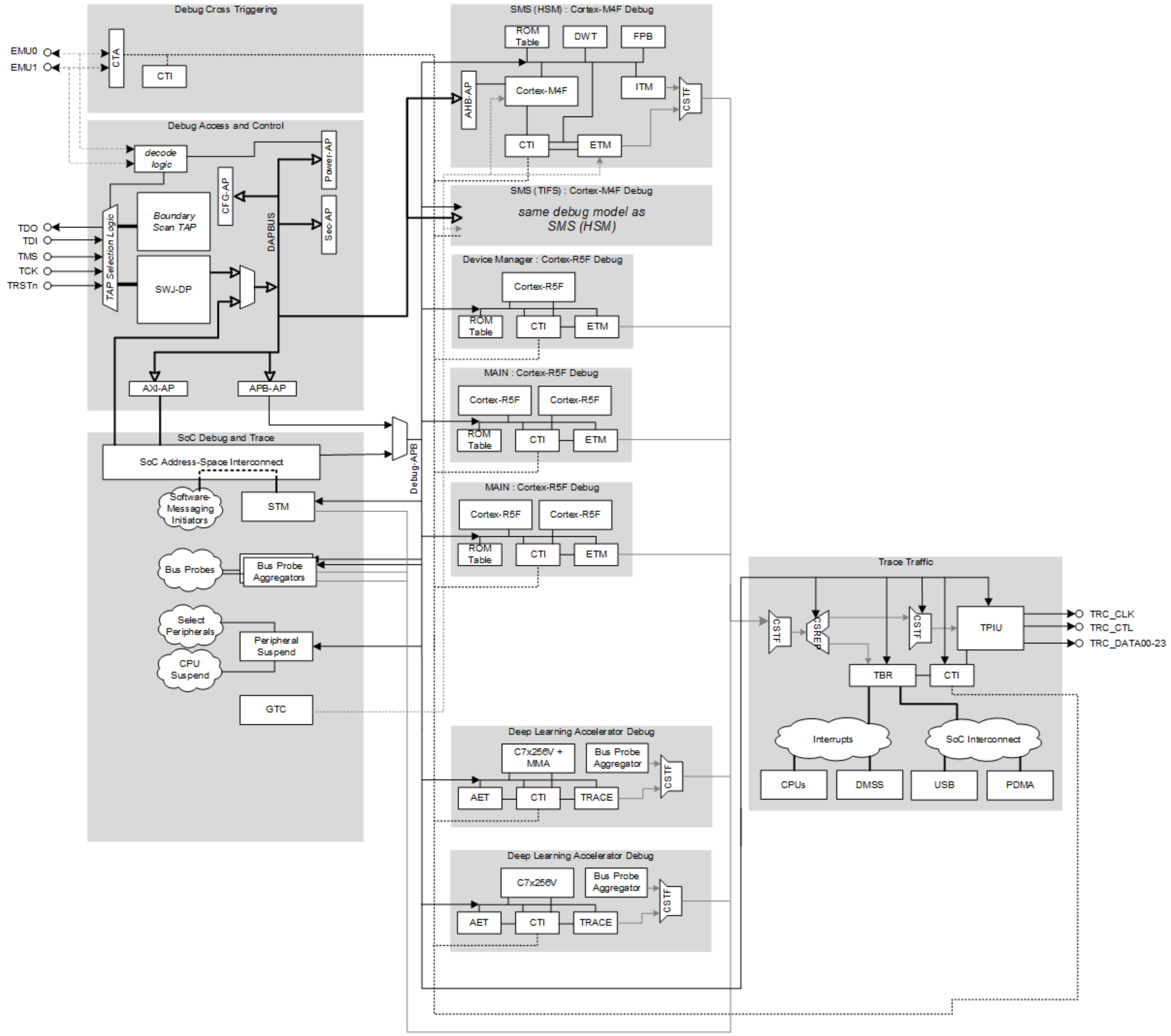

Figure 13-1. On-Chip Debug Block Diagram

13.3.2 Device Interfaces

On-Chip Debug features are supported through three device interfaces:

- **JTAG**: IEEE 1149.1 compliant interface that provides access to Boundary Scan and acts as the primary interface for off-chip access to On-Chip debug resources
- **Trigger and Debug Boot Mode**: Multi-functional interface that supports product level cross-triggering and debug-related boot modes
- **Trace Port**: Arm TPIU compliant Trace Port interface is used to facilitate export of trace

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. The following document is a good reference for guidelines: Emulation and Trace Headers (SPRU655). More information can also be found here: XDS Target Connection Guide.

The previous link connects to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use

13.3.2.1 JTAG Interface

Table 13-1. JTAG Interface Signals

Signal Name	I/O Type	Description
TRSTn	I	*Test Reset*. Initializes and disables the test interface
TCK	I	*Test Clock*. Controls the timing of the test interface independently from any system clocks. TCK is pulsed by the equipment controlling the test and not by the tested device.
TMS	I	*Test Mode Select*. Controls the transitions of the test interface state machine.
TDI	I	*Test Data Input*. Supplies the data to the JTAG registers.
TDO	O/Z	*Test Data Output*. Used to serially output the data from the JTAG registers to the equipment controlling the test.

Note

I = Input; I/O = Input or Output, O = Output; O/Z = Output or three-state

13.3.2.2 Trigger and Debug Boot Mode Interface

Table 13-2. Trigger and Debug Boot Mode Interface Signals

Signal Name	I/O Type	Description
EMU0	I/O	Channel 0 trigger or boot mode select
EMU1	I/O	Channel 1 trigger or boot mode select

13.3.2.3 Trace Port Interface

Table 13-3. Trace Port Signals

Pin Name	TPIU Signal Name	I/O Type	Description
TRC_CLK	TRACECLK	O	Trace CLock
TRC_CTL	TRACECTL	O	Trace Control
TRC_DATA[n:0]	TRACEDATA[n:0]	O	Trace Data [n:0]

Note

Trace Port interface signals are exposed on device pins that are multiplexed with other functions.

13.3.3 Debug and Boundary Scan Access and Control

On-Chip debug resources are mode available through three mechanisms:

- JTAG access via DAP and related Aps
- JTAG access via Boundary Scan TAP

- Embedded access to debug resources via SoC address space

DAP

Off-chip debug tools are able to access On-Chip debug resources via the JTAG interface when not in Boundary Scan mode (see below). A CoreSight Compliant DAP architecture provides access via a DP and a collection of Aps:

- **SWJ-DP**: Arm CoreSight compliant SWJ Debug Port provides support for a JTAG interface with a 4-bit IR.
- **APB-AP**: Arm CoreSight APB Access Port provides access to the Debug-APB address space which is the primary configuration space for On-Chip Debug resources.
- **AXI-AP**: Arm CoreSight AXI Access Port provides access to the SoC address space, allowing visibility and control over system resources.
- **Config-AP**: TI AP supports access to SoC debug management registers
- **Power-AP**: TI AP supports advanced power, reset, and clock management.
- **SEC-AP** : TI AP supports debug authentication

> **Note**
>
> Even though an SWJ-DP is deployed on-chip, only JTAG is supported. This device does not support SWD.

The below tale describes the APSEL assignment for this device.

Table 13-4. DAP APSEL Assignment

APSEL	AP	Description
0	Config-AP	TI AP - Reserved
1	APB-AP	Provides access to Debug Config Plane
2	AXI-AP	Provides access to SoC Address Space
3	Power-AP	TI AP - Extended Power/Reset/Clock Control
4-5	Reserved	Reserved for future use
6	SEC-AP	TI AP - Authentication Interface
7	SMS TIFS M4F	
8	Reserved	Reserved for future use
9	SMS HSM M4F	
10-31	Reserved	Reserved for future use

Boundary Scan

This device supports boundary scan using an IEEE 1149.1 compliant JTAG TAP that is made visible through the use of a compliance-enable mode IEEE 1149.1 and 1149.6 Boundary Scan support are defined in device-specific BSDL files that can be found in the respective device’s product folder on ti.com

SoC Address Space

The device architecture provides access to On-Chip debug resources through the SoC Address Space. This includes access to all DAP Access Ports (Aps) as well as the Debug-APB address space.

13.3.4 Debug Boot Modes and Boundary Scan Compliance

The EMU1 and EMU0 device pins are used to convey debug boot mode behavior and can also be used as part of a boundary scan compliance sequence to enable boundary scan features.

Debug Boot Mode

EMU1 and EMU0 are sampled when MCU_PORz is de-asserted and the decoded value determines the debug boot mode behavior as detailed in the following table:

Table 13-5. Debug Boot Modes

Sample Time	EMU1	EMU0	Boot Mde	Behavior
MCU_PORz dessertion	0	0	Reserved	Reserved
	0	1	Reserved	Reserved
	1	0	Wait-In-Reset (WIR)	Device will remain quiescent until a debug connection is established and the debugger releases WIR. This mode is useful for debugging boot sequences.
	1	1	Normal	Device boots normally. Debug can connect at any time but the context will be post-boot.

Boundary Scan Compliance

EMU1 and EMU0 are sampled when TRSTn is de-asserted and the decoded value determines the debug boot mode behavior as detailed in the following table:

Table 13-6. Boundary Scan Compliance

Sample Time	EMU1	EMU0	Boundary Compliance	Scan	Behavior
TRSTn deassertion	0	1	Boundary Enabled	Scan	The devices Boundary Scan TAP is connected to the device's JTAG interface.
	0	0	Boundary Disabled	Scan	The device's SWJ-DP is connected to the device's JTAG interface.
	1	0			
	1	1			

13.3.5 Power, Reset, Clock Management

This device includes advanced power, reset, and clock management debug capabilities, including:

- **Wakeup support for debug logic**: logic within the device is able to sense JTAG activity and ensure that debug logic is on and able to service JTAG requests.
- **Reset isolation:** critical configuration and trace data paths and logic are not sensitive to warm reset
- **Configuration independence**: debug configuration occurs over a debug-only interconnect, separate from SoC traffic to ensure debug logic remains available even during deadlock scenarios.
- **Power-AP:** a CoreSight compliant Access Port (AP) developed by TI that provides a standard interface for debug tooling to access status and control over power, reset, and clocking for the system and various LPSC-defined sub-domains.

13.3.6 Debug Cross Triggering

This device supports an Arm CoreSight compliant four-channel programmable on-chip Cross Triggering network. In addition to the four-channel on-chip network, this device implements two channels of product level triggering via the EMU0 and EMU1 device pins.

Conceptually, each channel of Cross Triggering can be viewed as mapping of a user-defined set of events to a user-defined set of actions, where the occurrence of any event in the set-of-events results in the generation of the set-of-actions. The below table provides a domain-level summary of the supported events and actions.

Table 13-7. Domain-level Summary of Triggering Capability

Domain	Events	Actions
Product-Level	Zero detected on EMU0 input pin	EMU0 output pin driven to Zero
	Zero detected on EMU1 input pin	EMU1 output pin driven to Zero

Table 13-7. Domain-level Summary of Triggering Capability (continued)

Domain	Events	Actions
SoC Debug	TBR Acquisition Complete	TPIU insert trigger packet
	TBR Embedded buffer is full	TPIU start flush process
	System reset asserted	TBR insert trigger packet
	Bus Probe-n match	TBR start flush process
	STM write to a TRIG location	Bus Probe-n Start
	STM write to a trigger-enabled stimulus port	Bus Probe-n Stop
MAIN_R5F	MAIN_R5F has halted	MAIN_R5F – halt request
	PMU generated interrupt	MAIN_R5F – resume request
	ETM Trigger outputs	ETM Trigger inputs
WKUP_R5F	WKUP_R5F has halted	WKUP_R5F – halt request
	PMU generated interrupt	WKUP_R5F – resume request
	ETM Trigger outputs	ETM Trigger inputs
C7XSS0/C7XSS1	C7XSS core has halted	C7XSS core – halt request
	AET Trigger output	C7XSS core – resume reques
	--	AET Trigger input

13.3.7 MAIN_R5F and WKUP_R5F Debug

MAIN_R5FSS and WKUP_R5F include an Arm Cortex R5 with embedded debug capability, including:

- Independent debug configuration
- ROM Table
- Basic debug functionality
- Cross Triggering
- PMU: Performance Monitor Unit
- ETM: Embedded Trace Macrocell

A summary of the MAIN_R5FSS and WKUP_R5F debug capabilities is detailed in the following table

Table 13-8. MAIN_R5F and WKUP_R5F Debug Capabilities

Capability	Feature	Notes
Basic Debug	Independent debug configuration	Debug resource configuration is performed over a configuration interface that is isolated from functional traffic
	ROM Table	Facilitates discovery of debug resources within debug configuration address space
	Processor Halt	Support user-requested entry into the suspended stat
	Single Step	Execution of a single instruction before entering the suspended state
	Software Breakpoints	Software breakpoints are supported via opcode replacement
	Hardware Breakpoints	Eight Debug Breakpoint resources support hardware breakpoints
	Hardware Watchpoints	Eight Debug Watchpoint resources support data address breakpoints
	Core Register Access	Access to processor core registers
	System Memory Access	Access to memory from perspective of CPU
	Vector Catch	Halting in response to an exception
	Arm TrustZone Debug Authentication	Provisioning for DBGEN and NIDEN

Table 13-8. MAIN_R5F and WKUP_R5F Debug Capabilities (continued)

Capability	Feature	Notes
Cross Triggering	Debug State	Support for controlling execution state (run, halt) via triggers and creating triggers upon entry into debug state
	PMU	PMU interrupt trigger
	ETM	Five ETM external triggers (one ETM Trigger, two external out event triggers, two external in event triggers)
PMU	Profile Counters	Three counters can be used to count different events available for gathering statistics on the operation of the processor and memory system
	Cycle Counters	One dedicated counter available for counting CPU clock cycles
ETM	Triggering Infrastructure	Comprehensive triggering infrastructure supports use of comparators (address, data value, context ID), counters, sequencer state, an external inputs and outputs to control the enabling of trace
	Instruction Trace	Supports tracing of instruction flow
	Cycle-Accurate Tracing	Supports inclusion of a precise cycle count of executed instructions
	Branch Broadcast Tracing	Support for tracing branch address details even in circumstances where that information might be discoverable from object code
	Data Tracing	Support for data address and data value tracing

13.3.8 SMS0_HSM Debug

SMS0_HSM includes an Arm Cortex M4F with embedded debug capability, including:

- Independent debug configuration via AHB-AP
- ROM Table
- Basic debug functionality
- Cross Triggering
- DWT: Data Watchpoint and Trace
- FPB: Flash Patch Breakpoint
- ITM: Instrumentation Trace Macrocell
- ETM: Embedded Trace Macrocell

A summary of the SMS0_HSM debug capabilities is detailed in teh following table

Table 13-9. SMS0_HSM and SMS0_TIFS Debug Capabilties

Capability	Feature	Notes
Basic Debug	AHB-AP	AHB-AP provides access to resources
	ROM table	Facilitates discovery of debug resources within AHB-AP address space
	Processor halt	Support user-requested entry into the suspended state
	Single step	Execution of a single instruction before entering the suspended state
	Core register access	Access to processor core registers
	Vector catch	Halting in response to an exception
	Software breakpoints	Software breakpoints are supported via opcode replacement
	System memory access	Access to M4F address space is supported via AHB-AP
	Arm TrustZone debug authentication	Provisioning for DBGEN and NIDEN

Table 13-9. SMS0_HSM and SMS0_TIFS Debug Capabilties (continued)

Capability	Feature	Notes
Cross Triggering	Debug State	Support for controlling execution state (run, halt) via triggers and creating triggers upon entry into debug state
	ETM	Six ETM external triggers (One ETMTRIG output, two EXTIN inputs, 3 ETMTRIGGER outputs)
DWT	Watchpoints	Four comparators implemented that can be configured to support watchpoints, data address trace, ETM signaling and PC sampling
	Data address trace	
	ETM signaling	
	PC sampling trace	
	Cycle count matching	
	Performance counting	Profiling counter support provides visibility into instruction cycle count, exception overhead, sleep overhead, load-store overhead, and folded instruction count
FPB	Hardware breakpoints	Six instruction address comparators support hardware breakpoints
	Remapping of literal and instruction fetch accesses	Two comparators support address remapping of literal or instruction accesses to facilitate software patching
ITM	Software trace	Software writes to ITM stimulus registers provoke the generation of trace packets that convey the values written
	DWT hardware trace	Support for conveying DWT output using trace
	Timestamping	Support for attaching a local timestamp to trace traffic
	Global timestamping	Support for attaching a global timestamp to trace traffic
ETM	Program execution trace	Support for tracing instruction execution
	Global timestamping	Support for attaching a global timestamp to trace traffic

13.3.9 C7XSS0 and C7XSS1 Debug

The C7XSS0 and C7XSS1 are a single-core C7xV-256 subsystem with embedded debug capability and features, including:

- Independent debug configuration
- Basic debug functionality
- Cross Triggering
- AET: Advanced Event Triggering
- Processor Trace
- Traffic Monitoring Trace

A summary of the C7XSS0 and C7XSS1 debug capabilities and features is detailed in the following table.

Table 13-10. C7XSS0 and C7XSS1 Debug Capabilities

Capability	Feature	Notes
Basic Debug	Independent Debug Configuration	Debug resource configuration is performed over a configuration interface that is isolated from functional traffic
	ROM Table	Facilitates discovery of debug resources within debug configuration address space
	Processor Halt	Support user-requested entry into the suspended state
	Single Step	Execution of a single instruction before entering the suspended state
	Software Breakpoints	Software breakpoints are supported via opcode replacement
	Hardware Breakpoints	Four Debug Breakpoint resources support hardware breakpoints
	Core Regsiter Access	Access to processor core registers
	System Memory Access	Access to memory from perspective of CPU
	Arm TrustZone Debug Authentication	Provisioning for DBGEN, NIDEN, SPIDEN, SPNIDEN, SUIDEN, and SUNIDEN
Cross Triggering	Debug State	Support for controlling execution state (run, halt) via triggers and creating triggers upon entry into debug state
	AET	Two channels of AET external triggers (input and output)
AET	Profile Counters	Two counters can be used to count different events available for gathering statistics on the operation of the processor and memory system. Includes watermark support
	Application Context Sensitive Trigger	Supports generation of events based on the context of application execution (e.g. Thread-ID, Virtual Machine ID, Program bus activity, Memory bus activity)
	Visibility and Detection of Events	Provided by CPU, Subsystem, and SOC
	Range Detection	Of Program and Memory bus activity
	Programmable State Machine	Supports complex, state-based event detection
	Trace Stream Filtering/Windowing	Supports the management of trace windows

Table 13-10. C7XSS0 and C7XSS1 Debug Capabilities (continued)

Capability	Feature	Notes
Trace	Historical Record	Creates a customized (based on trace stream filtering/windowing) historical account of the CPU's behavior through the use of different types of trace streams
	Program Flow Trace	Records program flow execution, including discontinuities resulting from branches, interrupts, or exceptions
	Cycle Accurate Trace	Records cycle-accurate timing information
	Memory Reference Trace	Records data log activity (address, data, address and data)
	Event Trace	Records information about the occurrence, duration, or relationship of one or more events
	Stream Buffer Parameter Trace	Records the parameters used to start a stream buffer operation allowing off-line reconstruction
	Application Context Trace	Records changes in the context of the application (virtual machine ID, thread-ID)
	Stall Control	Support for stalling the C7X processor to avoid Trace overflows
	Global Timestamping	Support for attaching a global timestamp to trace traffic
	Traffic Monitoring	Traffic monitoring bus probes are deployed within C7XSS0 memory subsystem

13.3.10 SoC Debug and Trace

This device includes debug capabilities deployed at the system level, including:

- Software messaging trace
- Debug-aware peripherals
- Traffic monitoring with bus probes
- Global timestamping for trace

13.3.10.1 Software Messaging Trace

Software messaging trace is supported on this device by an MIPI STP-V2 compliant Arm CoreSight STM with supporting logic that maps initiator IDs to specific STP Major Source IDs. The following device initiators support software messaging:

- C7XSS0
- C7XSS1
- MAIN_R5FSS0
- MAIN_R5FSS1
- WKUP_R5F
- SMS0_HSM
- SMS0_TIFS
- DMSS BCDMA
- DMSS PktDMA
- DAP AXI-AP

13.3.10.2 Debug-Aware Peripherals

Select peripherals support a debug feature that allows them to react to the debug state of a controlling processor. For instance, a timer peripheral that is allocated to a particular processor could be configured to stop counting when the associated processor is in the halted state. This device includes programmable support for shared peripherals that allows the developer to select the processor whose debug state a given peripheral should receive Peripherals that are debug aware include programmable support to enable or disable sensitivity to debug.

A list of the processors and peripherals that support this debug model can be found below.

- Supported Processors
  - C7XSS0
  - C7XSS1
  - MAIN_R5FSS0
  - MAIN_R5FSS1
  - WKUP_R5F
  - SMS0_HSM
- Supported Peripherals
  - GTC
  - CPSW3G
  - DMSS
  - SA3SS
  - TIMER Instances
  - EPWM Instances
  - MCAN Instances
  - I2C Instances
  - ECAP Instances
  - PDAM_AASRC
  - PDMA_SPI
  - PDMA_UART
  - PDMA_MCASP
  - RTI/WWDT Instances

13.3.10.3 Traffic Monitoring with Bus Probes

Traffic monitoring bus probes are deployed at strategic points in the system interconnect and support the following capabilities:

- MIPI STP-V2 compliant trace messaging support with global timestamping support
- Latency Statistics Collection: Statistics on the timeliness of responses to read requests are collected during a sampling window and then read by a profiling entity (application thread or encoded into a trace message)
- Throughput Statistics Collection: Statistics on the amount of data moving across an interface are collected during a sampling window and then read by a profiling entity (application thread or encoded into a trace message)
- Transaction Trace: Information about specific transactions occurring at a probed location are captured and encoded into a trace message
- Complex filtering support allows discrimination of traffic being monitored
- Cross-Trigger support for enabling and disabling probe monitoring

The below table details the locations in the system interconnect that are probed:

Table 13-11. Bus Probe Points

Probe Point	Bus Monitoring Details
C7XSS0 Deep Learning Accelerator SDMA Target	Monitors traffic to DLA SDMA port
C7XSS1 Deep Learning Accelerator SDMA Target	Monitors traffic to DLA SDMA port
C7XSS0 Deep Learning Accelerator MDMA Initiator	Monitors traffic initiated by DLA MDMA
C7XSS1 Deep Learning Accelerator MDMA Initiator	Monitors traffic initiated by DLA MDMA
R5SS0 :: cpu0 rmst initiator	Monitors R5 read port
R5SS0 :: cpu0 wmst initiator	Monitors R5 write port
R5SS0 :: cpu1 rmst initiator	Monitors R5 read port
R5SS0 :: cpu1 wmst initiator	Monitors R5 write port
R5SS1 :: cpu0 rmst initiator	Monitors R5 read port

Table 13-11. Bus Probe Points (continued)

Probe Point	Bus Monitoring Details
R5SS1 :: cpu0 wmst initiator	Monitors R5 write port
R5SS1 :: cpu1 rmst initiator	Monitors R5 read port
R5SS1 :: cpu1 wmst initiator	Monitors R5 write port
FSS OSPI0 Target	Monitors traffic to FSS
FSS OSPI1 Target	Monitors traffic to FSS
FSS of ul OSPI1 Target	Monitors traffic to FSS
OCSRAM Bank 0	Monitors traffic to OCSRAM Bank 0
OCSRAM Bank 1	Monitors traffic to OCSRAM Bank 1
OCSRAM Bank 2	Monitors traffic to OCSRAM Bank 2
OCSRAM Bank 3	Monitors traffic to OCSRAM Bank 3
OCSRAM Bank 4	Monitors traffic to OCSRAM Bank 4
OCSRAM Bank 5	Monitors traffic to OCSRAM Bank 5
Audio CBASS targets	Monitors traffic to these targets: MCASP# AASRC# ATL#
Peripheral CBASS Targets	Monitors traffic to these targets: ECAP# EQEP# I2C# MCAN# SPI# UART#
WKUP CBASS Targets	Monitors traffic from MAIN to WKUP, including these targets: WKUP_GTC WKUP_R5F WKUP_TIMER# WKUP_RTI WKUP_I2C# WKUP_CTRL_MMR0 WKUP_VTM0
Infrastructure CBASS Targets	Monitors traffic to these targets: CMP_EVENT_INTROUTER CTRL_MMR DCC# DDPA DFTSS ESM PSRAM256x32 GPIO0 GPIO1 EFUSE GPIOMUX_INTROUTER PADCFG_CTRL_MMR0 PLL_MMR0 PLLCTRL PSC TIMESYNC_EVENT_ROUTE

13.3.10.4 Global Timestamping for Trace

Support for a global timestamp for use by debug is enabled by a 48-bit continuous timestamp managed by the device's GTC. This 48-bit global timestamp is readable by embedded software, via the GTC, and distributed across the device to various trace sources where it is used as a time reference when timestamping trace streams. Trace sources that support global timestamping, include:

- C7XSS0 cores: Trace
- C7XSS1 cores: Trace
- STM
- SMS0_HSM: ITM and ETM
- SMS_TIFS: ITM and ETM
- Bus Probes

13.3.11 Trace Traffic

Trace traffic originates from a trace source, is distributed across the device using Arm CoreSight compliant trace infrastructure components, and reaches one of two possible trace sinks.

13.3.11.1 Trace Sources

A summary of the trace sources present on this device is included in the following table.

Table 13-12. Trace Sources

Domain	Trace Source
SoC Debug	Bus Probes
	STM
MAIN_R5FSS0	ETM
MAIN_R5FSS1	ETM
SMS0_HSM	ETM, ITM/DWT
WKUP_R5F	ETM
C7XSS0	Processor Trace
C7XSS1	Processor Trace

13.3.11.2 Trace Infrastructure

Trace distribution is accomplished using standard Arm CoreSight compliant trace infrastructure components:

- CoreSight Trace Funnels (CSTF): Non-programmable CSTFs are used at points of interleaving where multiple trace sources converge and form a single stream of trace traffic. This device includes one instance of a programmable CSTF that is deployed immediately before the TPIU.
- CoreSight Trace Replicator (CSREP): A programmable CSREP is used as a routing device, that can be used to forward trace traffic, based on its ID, to one, both, or none of the device trace sinks.

13.3.11.3 Trace Sinks

Two trace sinks are supported on this device:

- Arm CoreSight TPIU: TPIU supports export of trace off-chip via LVCMOS device pins for capture by an external receiver.
- TI Trace Buffer Router (TBR) with 64KB of storage: the TBR can function as a trace buffer or as a system bridge. As a trace buffer, the TBR can be setup to capture trace data until the internal buffer fills or it can operate as a circular buffer that will capture continuously. When configured as a system bridge the TBR’s storage becomes an elastic buffer that supports the concurrent queueing and dequeuing of trace traffic. The system bridge mode supports interrupt and event notification capabilities that support integration with device level CPUs and/or DMAs to support a variety of use cases, including, for e.g., relocation of trace data to DDR and off-chip export over USB.

14 Registers

14.1 System Interconnect Registers

14.1.1 CBASS

CBASS

14.1.1.1 CBASS Summaries

CBASS Summaries

Table 14-1. CBASS_ERR Registers, Base Address=2B40 0000h, Length=1024

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
0h	32	CBASS_ERR_PID	2B40 0000h
4h	32	CBASS_ERR_DESTINATION_ID	2B40 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	2B40 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	2B40 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	2B40 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	2B40 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	2B40 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	2B40 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	2B40 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	2B40 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	2B40 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	2B40 005Ch
60h	32	CBASS_ERR_EOI	2B40 0060h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
0h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL	4500 8000h
4h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0	4500 8004h
8h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1	4500 8008h
Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2	4500 800Ch
10h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L	4500 8010h
14h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H	4500 8014h
18h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L	4500 8018h
1Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H	4500 801Ch
20h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL	4500 8020h
24h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0	4500 8024h
28h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1	4500 8028h
2Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2	4500 802Ch
30h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L	4500 8030h
34h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H	4500 8034h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
38h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L	4500 8038h
3Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H	4500 803Ch
40h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL	4500 8040h
44h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0	4500 8044h
48h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1	4500 8048h
4Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2	4500 804Ch
50h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L	4500 8050h
54h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H	4500 8054h
58h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L	4500 8058h
5Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H	4500 805Ch
60h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL	4500 8060h
64h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0	4500 8064h
68h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1	4500 8068h
6Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2	4500 806Ch
70h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L	4500 8070h
74h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H	4500 8074h
78h	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L	4500 8078h
7Ch	32	CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H	4500 807Ch
400h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL	4500 8400h
404h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0	4500 8404h
408h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1	4500 8408h
40Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2	4500 840Ch
410h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L	4500 8410h
414h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H	4500 8414h
418h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L	4500 8418h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
41Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H	4500 841Ch
420h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL	4500 8420h
424h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0	4500 8424h
428h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1	4500 8428h
42Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2	4500 842Ch
430h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L	4500 8430h
434h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H	4500 8434h
438h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L	4500 8438h
43Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H	4500 843Ch
440h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL	4500 8440h
444h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0	4500 8444h
448h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1	4500 8448h
44Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2	4500 844Ch
450h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L	4500 8450h
454h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H	4500 8454h
458h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L	4500 8458h
45Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H	4500 845Ch
460h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL	4500 8460h
464h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0	4500 8464h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
468h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1	4500 8468h
46Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2	4500 846Ch
470h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L	4500 8470h
474h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H	4500 8474h
478h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L	4500 8478h
47Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H	4500 847Ch
480h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL	4500 8480h
484h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0	4500 8484h
488h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1	4500 8488h
48Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2	4500 848Ch
490h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L	4500 8490h
494h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H	4500 8494h
498h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L	4500 8498h
49Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H	4500 849Ch
4A0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL	4500 84A0h
4A4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0	4500 84A4h
4A8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1	4500 84A8h
4ACh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2	4500 84ACh
4B0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L	4500 84B0h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
4B4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H	4500 84B4h
4B8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L	4500 84B8h
4BCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H	4500 84BCh
4C0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL	4500 84C0h
4C4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0	4500 84C4h
4C8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1	4500 84C8h
4CCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2	4500 84CCh
4D0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L	4500 84D0h
4D4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H	4500 84D4h
4D8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L	4500 84D8h
4DCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H	4500 84DCh
4E0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL	4500 84E0h
4E4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0	4500 84E4h
4E8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1	4500 84E8h
4ECh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2	4500 84ECh
4F0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L	4500 84F0h
4F4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H	4500 84F4h
4F8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L	4500 84F8h
4FCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H	4500 84FCh

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
500h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL	4500 8500h
504h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0	4500 8504h
508h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1	4500 8508h
50Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2	4500 850Ch
510h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L	4500 8510h
514h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H	4500 8514h
518h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L	4500 8518h
51Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H	4500 851Ch
520h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL	4500 8520h
524h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0	4500 8524h
528h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1	4500 8528h
52Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2	4500 852Ch
530h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L	4500 8530h
534h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H	4500 8534h
538h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L	4500 8538h
53Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H	4500 853Ch
540h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL	4500 8540h
544h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0	4500 8544h
548h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1	4500 8548h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
54Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2	4500 854Ch
550h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L	4500 8550h
554h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H	4500 8554h
558h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L	4500 8558h
55Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H	4500 855Ch
560h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL	4500 8560h
564h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0	4500 8564h
568h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1	4500 8568h
56Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2	4500 856Ch
570h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L	4500 8570h
574h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H	4500 8574h
578h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L	4500 8578h
57Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H	4500 857Ch
580h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL	4500 8580h
584h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0	4500 8584h
588h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1	4500 8588h
58Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2	4500 858Ch
590h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L	4500 8590h
594h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H	4500 8594h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
598h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L	4500 8598h
59Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H	4500 859Ch
5A0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL	4500 85A0h
5A4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0	4500 85A4h
5A8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1	4500 85A8h
5ACh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2	4500 85ACh
5B0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L	4500 85B0h
5B4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H	4500 85B4h
5B8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L	4500 85B8h
5BCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H	4500 85BCh
5C0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL	4500 85C0h
5C4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0	4500 85C4h
5C8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1	4500 85C8h
5CCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2	4500 85CCh
5D0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L	4500 85D0h
5D4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H	4500 85D4h
5D8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L	4500 85D8h
5DCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H	4500 85DCh
5E0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL	4500 85E0h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
5E4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0	4500 85E4h
5E8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1	4500 85E8h
5ECh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2	4500 85ECh
5F0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L	4500 85F0h
5F4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H	4500 85F4h
5F8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L	4500 85F8h
5FCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H	4500 85FCh
800h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_CONTROL	4500 8800h
804h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_0	4500 8804h
808h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_1	4500 8808h
80Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_2	4500 880Ch
810h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L	4500 8810h
814h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H	4500 8814h
818h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L	4500 8818h
81Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H	4500 881Ch
820h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_CONTROL	4500 8820h
824h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_0	4500 8824h
828h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_1	4500 8828h
82Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_2	4500 882Ch
830h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L	4500 8830h
834h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H	4500 8834h
838h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L	4500 8838h
83Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H	4500 883Ch
840h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_CONTROL	4500 8840h
844h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_0	4500 8844h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
848h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_1	4500 8848h
84Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_2	4500 884Ch
850h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L	4500 8850h
854h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H	4500 8854h
858h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L	4500 8858h
85Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H	4500 885Ch
860h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_CONTROL	4500 8860h
864h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_0	4500 8864h
868h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_1	4500 8868h
86Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_2	4500 886Ch
870h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L	4500 8870h
874h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H	4500 8874h
878h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L	4500 8878h
87Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H	4500 887Ch
880h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_CONTROL	4500 8880h
884h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_0	4500 8884h
888h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_1	4500 8888h
88Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_2	4500 888Ch
890h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L	4500 8890h
894h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H	4500 8894h
898h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L	4500 8898h
89Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H	4500 889Ch
8A0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_CONTROL	4500 88A0h
8A4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_0	4500 88A4h
8A8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_1	4500 88A8h
8ACh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_2	4500 88ACh
8B0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L	4500 88B0h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
8B4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H	4500 88B4h
8B8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L	4500 88B8h
8BCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H	4500 88BCh
8C0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_CONTROL	4500 88C0h
8C4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_0	4500 88C4h
8C8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_1	4500 88C8h
8CCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_2	4500 88CCh
8D0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L	4500 88D0h
8D4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H	4500 88D4h
8D8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L	4500 88D8h
8DCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H	4500 88DCh
8E0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_CONTROL	4500 88E0h
8E4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_0	4500 88E4h
8E8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_1	4500 88E8h
8ECh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_2	4500 88ECh
8F0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L	4500 88F0h
8F4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H	4500 88F4h
8F8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L	4500 88F8h
8FCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H	4500 88FCh
900h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_CONTROL	4500 8900h
904h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_0	4500 8904h
908h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_1	4500 8908h
90Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_2	4500 890Ch
910h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L	4500 8910h
914h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H	4500 8914h
918h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L	4500 8918h
91Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H	4500 891Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
920h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_CONTROL	4500 8920h
924h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_0	4500 8924h
928h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_1	4500 8928h
92Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_2	4500 892Ch
930h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L	4500 8930h
934h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H	4500 8934h
938h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L	4500 8938h
93Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H	4500 893Ch
940h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_CONTROL	4500 8940h
944h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_0	4500 8944h
948h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_1	4500 8948h
94Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_2	4500 894Ch
950h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L	4500 8950h
954h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H	4500 8954h
958h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L	4500 8958h
95Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H	4500 895Ch
960h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_CONTROL	4500 8960h
964h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_0	4500 8964h
968h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_1	4500 8968h
96Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_2	4500 896Ch
970h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L	4500 8970h
974h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H	4500 8974h
978h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L	4500 8978h
97Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H	4500 897Ch
980h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_CONTROL	4500 8980h
984h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_0	4500 8984h
988h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_1	4500 8988h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
98Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_2	4500 898Ch
990h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L	4500 8990h
994h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H	4500 8994h
998h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L	4500 8998h
99Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H	4500 899Ch
9A0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_CONTROL	4500 89A0h
9A4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_0	4500 89A4h
9A8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_1	4500 89A8h
9ACh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_2	4500 89ACh
9B0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L	4500 89B0h
9B4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H	4500 89B4h
9B8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L	4500 89B8h
9BCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H	4500 89BCh
9C0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_CONTROL	4500 89C0h
9C4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_0	4500 89C4h
9C8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_1	4500 89C8h
9CCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_2	4500 89CCh
9D0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L	4500 89D0h
9D4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H	4500 89D4h
9D8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L	4500 89D8h
9DCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H	4500 89DCh
9E0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_CONTROL	4500 89E0h
9E4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_0	4500 89E4h
9E8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_1	4500 89E8h
9ECh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_2	4500 89ECh
9F0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L	4500 89F0h
9F4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H	4500 89F4h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
9F8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L	4500 89F8h
9FCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H	4500 89FCh
A00h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_CONTROL	4500 8A00h
A04h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_0	4500 8A04h
A08h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_1	4500 8A08h
A0Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_2	4500 8A0Ch
A10h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_L	4500 8A10h
A14h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_H	4500 8A14h
A18h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_L	4500 8A18h
A1Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_H	4500 8A1Ch
A20h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_CONTROL	4500 8A20h
A24h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_0	4500 8A24h
A28h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_1	4500 8A28h
A2Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_2	4500 8A2Ch
A30h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_L	4500 8A30h
A34h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_H	4500 8A34h
A38h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_L	4500 8A38h
A3Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_H	4500 8A3Ch
A40h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_CONTROL	4500 8A40h
A44h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_0	4500 8A44h
A48h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_1	4500 8A48h
A4Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_2	4500 8A4Ch
A50h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_L	4500 8A50h
A54h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_H	4500 8A54h
A58h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_L	4500 8A58h
A5Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_H	4500 8A5Ch
A60h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_CONTROL	4500 8A60h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
A64h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_0	4500 8A64h
A68h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_1	4500 8A68h
A6Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_2	4500 8A6Ch
A70h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_L	4500 8A70h
A74h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_H	4500 8A74h
A78h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_L	4500 8A78h
A7Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_H	4500 8A7Ch
A80h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_CONTROL	4500 8A80h
A84h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_0	4500 8A84h
A88h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_1	4500 8A88h
A8Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_2	4500 8A8Ch
A90h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_L	4500 8A90h
A94h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_H	4500 8A94h
A98h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_L	4500 8A98h
A9Ch	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_H	4500 8A9Ch
AA0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_CONTROL	4500 8AA0h
AA4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_0	4500 8AA4h
AA8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_1	4500 8AA8h
AACh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_2	4500 8AACh
AB0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_L	4500 8AB0h
AB4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_H	4500 8AB4h
AB8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_L	4500 8AB8h
ABCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_H	4500 8ABCh
AC0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_CONTROL	4500 8AC0h
AC4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_0	4500 8AC4h
AC8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_1	4500 8AC8h
ACCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_2	4500 8ACCh

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
AD0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_L	4500 8AD0h
AD4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_H	4500 8AD4h
AD8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_L	4500 8AD8h
ADCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_H	4500 8ADCh
AE0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_CONTROL	4500 8AE0h
AE4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_0	4500 8AE4h
AE8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_1	4500 8AE8h
AECh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_2	4500 8AECh
AF0h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_L	4500 8AF0h
AF4h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_H	4500 8AF4h
AF8h	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_L	4500 8AF8h
AFCh	32	CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_H	4500 8AFCh
C00h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL	4500 8C00h
C04h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0	4500 8C04h
C08h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1	4500 8C08h
C0Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2	4500 8C0Ch
C10h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L	4500 8C10h
C14h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H	4500 8C14h
C18h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L	4500 8C18h
C1Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H	4500 8C1Ch
C20h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL	4500 8C20h
C24h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0	4500 8C24h
C28h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1	4500 8C28h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
C2Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2	4500 8C2Ch
C30h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L	4500 8C30h
C34h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H	4500 8C34h
C38h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L	4500 8C38h
C3Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H	4500 8C3Ch
C40h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL	4500 8C40h
C44h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0	4500 8C44h
C48h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1	4500 8C48h
C4Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2	4500 8C4Ch
C50h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L	4500 8C50h
C54h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H	4500 8C54h
C58h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L	4500 8C58h
C5Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H	4500 8C5Ch
C60h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL	4500 8C60h
C64h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0	4500 8C64h
C68h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1	4500 8C68h
C6Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2	4500 8C6Ch
C70h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L	4500 8C70h
C74h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H	4500 8C74h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
C78h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L	4500 8C78h
C7Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H	4500 8C7Ch
C80h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL	4500 8C80h
C84h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0	4500 8C84h
C88h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1	4500 8C88h
C8Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2	4500 8C8Ch
C90h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L	4500 8C90h
C94h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H	4500 8C94h
C98h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L	4500 8C98h
C9Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H	4500 8C9Ch
CA0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL	4500 8CA0h
CA4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0	4500 8CA4h
CA8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1	4500 8CA8h
CACh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2	4500 8CACh
CB0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L	4500 8CB0h
CB4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H	4500 8CB4h
CB8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L	4500 8CB8h
CBCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H	4500 8CBCh
CC0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL	4500 8CC0h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
CC4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0	4500 8CC4h
CC8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1	4500 8CC8h
CCCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2	4500 8CCCh
CD0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L	4500 8CD0h
CD4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H	4500 8CD4h
CD8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L	4500 8CD8h
CDCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H	4500 8CDCh
CE0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL	4500 8CE0h
CE4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0	4500 8CE4h
CE8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1	4500 8CE8h
CECh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2	4500 8CECh
CF0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L	4500 8CF0h
CF4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H	4500 8CF4h
CF8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L	4500 8CF8h
CFCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H	4500 8CFCh
D00h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL	4500 8D00h
D04h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0	4500 8D04h
D08h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1	4500 8D08h
D0Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2	4500 8D0Ch

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
D10h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L	4500 8D10h
D14h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H	4500 8D14h
D18h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L	4500 8D18h
D1Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H	4500 8D1Ch
D20h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL	4500 8D20h
D24h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0	4500 8D24h
D28h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1	4500 8D28h
D2Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2	4500 8D2Ch
D30h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L	4500 8D30h
D34h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H	4500 8D34h
D38h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L	4500 8D38h
D3Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H	4500 8D3Ch
D40h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL	4500 8D40h
D44h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0	4500 8D44h
D48h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1	4500 8D48h
D4Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2	4500 8D4Ch
D50h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L	4500 8D50h
D54h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H	4500 8D54h
D58h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L	4500 8D58h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
D5Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H	4500 8D5Ch
D60h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL	4500 8D60h
D64h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0	4500 8D64h
D68h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1	4500 8D68h
D6Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2	4500 8D6Ch
D70h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L	4500 8D70h
D74h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H	4500 8D74h
D78h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L	4500 8D78h
D7Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H	4500 8D7Ch
D80h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL	4500 8D80h
D84h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0	4500 8D84h
D88h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1	4500 8D88h
D8Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2	4500 8D8Ch
D90h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L	4500 8D90h
D94h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H	4500 8D94h
D98h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L	4500 8D98h
D9Ch	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H	4500 8D9Ch
DA0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL	4500 8DA0h
DA4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0	4500 8DA4h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
DA8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1	4500 8DA8h
DACh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2	4500 8DACh
DB0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L	4500 8DB0h
DB4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H	4500 8DB4h
DB8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L	4500 8DB8h
DBCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H	4500 8DBCh
DC0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL	4500 8DC0h
DC4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0	4500 8DC4h
DC8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1	4500 8DC8h
DCCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2	4500 8DCCh
DD0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L	4500 8DD0h
DD4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H	4500 8DD4h
DD8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L	4500 8DD8h
DDCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H	4500 8DDCh
DE0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL	4500 8DE0h
DE4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0	4500 8DE4h
DE8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1	4500 8DE8h
DECh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2	4500 8DECh
DF0h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L	4500 8DF0h

Table 14-2. CBASS_FW Registers, Base Address=4500 8000h, Length=16384 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
DF4h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H	4500 8DF4h
DF8h	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L	4500 8DF8h
DFCh	32	CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H	4500 8DFCh
2000h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_CONTROL	4500 A000h
2004h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0	4500 A004h
2008h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1	4500 A008h
200Ch	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2	4500 A00Ch
2010h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L	4500 A010h
2014h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H	4500 A014h
2018h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L	4500 A018h
201Ch	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H	4500 A01Ch
2400h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_CONTROL	4500 A400h
2404h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0	4500 A404h
2408h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1	4500 A408h
240Ch	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2	4500 A40Ch
2410h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L	4500 A410h
2414h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H	4500 A414h
2418h	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L	4500 A418h
241Ch	32	CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H	4500 A41Ch

Table 14-3. CBASS_ISC Registers, Base Address=4581 4000h, Length=4096

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
0h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL	4581 4000h
10h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L	4581 4010h
14h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H	4581 4014h
18h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L	4581 4018h
1Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H	4581 401Ch

Table 14-3. CBASS_ISC Registers, Base Address=4581 4000h, Length=4096 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
20h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL	4581 4020h
30h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L	4581 4030h
34h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H	4581 4034h
38h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L	4581 4038h
3Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H	4581 403Ch
40h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL	4581 4040h
50h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L	4581 4050h
54h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H	4581 4054h
58h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L	4581 4058h
5Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H	4581 405Ch
60h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL	4581 4060h
70h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L	4581 4070h
74h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H	4581 4074h
78h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L	4581 4078h
7Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H	4581 407Ch
80h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL	4581 4080h
400h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL	4581 4400h
410h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L	4581 4410h
414h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H	4581 4414h
418h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L	4581 4418h
41Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H	4581 441Ch
420h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL	4581 4420h
430h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L	4581 4430h
434h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H	4581 4434h
438h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L	4581 4438h
43Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H	4581 443Ch
440h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL	4581 4440h

Table 14-3. CBASS_ISC Registers, Base Address=4581 4000h, Length=4096 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
450h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L	4581 4450h
454h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H	4581 4454h
458h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L	4581 4458h
45Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H	4581 445Ch
460h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL	4581 4460h
470h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L	4581 4470h
474h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H	4581 4474h
478h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L	4581 4478h
47Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H	4581 447Ch
480h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL	4581 4480h
800h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL	4581 4800h
810h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L	4581 4810h
814h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H	4581 4814h
818h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L	4581 4818h
81Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H	4581 481Ch
820h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL	4581 4820h
830h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L	4581 4830h
834h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H	4581 4834h
838h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L	4581 4838h
83Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H	4581 483Ch
840h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL	4581 4840h
850h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L	4581 4850h
854h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H	4581 4854h
858h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L	4581 4858h
85Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H	4581 485Ch
860h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL	4581 4860h
870h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L	4581 4870h

Table 14-3. CBASS_ISC Registers, Base Address=4581 4000h, Length=4096 (continued)

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
874h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H	4581 4874h
878h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L	4581 4878h
87Ch	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H	4581 487Ch
880h	32	CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL	4581 4880h

Table 14-4. CBASS_GLB Registers, Base Address=45B0 3000h, Length=1024

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
0h	32	CBASS_GLB_PID	45B0 3000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 3004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 3020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 3024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 3028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 302Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 3030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 3034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 3038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 3040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 3044h

Table 14-5. CBASS_QOS Registers, Base Address=45D1 4000h, Length=4096

Offset	Length	Register Name	WKUP_CBASS0 Physical Address
100h	32	CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0	45D1 4100h
500h	32	CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0	45D1 4500h
900h	32	CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0	45D1 4900h

14.1.1.2 CBASS Registers

CBASS Registers

14.1.1.2.1 CBASS_ERR_PID Register

14.1.1.2.1.1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66006102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-6. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0000h

Figure 14-1. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Ch					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-7. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
15:11	RTL	R	Ch	RTL revision. Will vary depending on release. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.2 CBASS_ERR_DESTINATION_ID Register

14.1.1.2.2.1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-8. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0004h

Figure 14-2. CBASS_ERR_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

14.1.1.2.3.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-10. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0024h

Figure 14-3. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-11. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

14.1.1.2.4.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-12. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0028h

Figure 14-4. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-13. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.1.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

14.1.1.2.5.1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-14. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 002Ch

Figure 14-5. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

14.1.1.2.6.1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

Return to Summary Table

Table 14-16. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0030h

Figure 14-6. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-17. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

14.1.1.2.7.1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-18. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0034h

Figure 14-7. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ROUTEID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRITE</td><td>READ</td><td>DEBUG</td><td>CACHEABLE</td><td>PRIV</td><td>SECURE</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-19. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

14.1.1.2.8.1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-20. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0038h

Figure 14-8. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BYTECNT							
R							
0h							

Table 14-21. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

14.1.1.2.9.1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-22. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0050h

Figure 14-9. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-23. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

14.1.1.2.10.1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-24. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0054h

Figure 14-10. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-25. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

14.1.1.2.11.1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-26. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0058h

Figure 14-11. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTR_ENABLE_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-27. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

14.1.1.2.12.1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-28. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 005Ch

Figure 14-12. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTR_ENABLE_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-29. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.13 CBASS_ERR_EOI Register

14.1.1.2.13.1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-30. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	2B40 0060h

Figure 14-13. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-31. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_32_DM_CLK4_rst_mod_g_rst_n

14.1.1.2.14 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL Register

14.1.1.2.14.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-32. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4500 8000h

Figure 14-14. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-33. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.15 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.1.2.15.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-34. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8004h

Figure 14-15. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-35. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-35. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.16 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.1.2.16.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-36. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8008h

Figure 14-16. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-37. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-37. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.17 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.1.2.17.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-38. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 800Ch

Figure 14-17. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-39. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-39. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.18 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.1.2.18.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 78000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-40. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8010h

Figure 14-18. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
78000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
78000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
78000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-41. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	78000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.19 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.1.2.19.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-42. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8014h

Figure 14-19. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-43. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.20 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.1.2.20.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 78007FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-44. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8018h

Figure 14-20. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
78007h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
78007h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
78007h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-45. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	78007h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.21 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.1.2.21.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 0 firewall.

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Table 14-46. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 801Ch

Figure 14-21. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-47. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.22 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL Register

14.1.1.2.22.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL Register (Offset = 20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-48. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8020h

Figure 14-22. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-49. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.23 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Register

14.1.1.2.23.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-50. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8024h

Figure 14-23. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-51. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-51. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.24 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Register

14.1.1.2.24.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-52. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8028h

Figure 14-24. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-53. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-53. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.25 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Register

14.1.1.2.25.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-54. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 802Ch

Figure 14-25. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-55. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-55. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.26 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L Register

14.1.1.2.26.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 78100000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-56. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8030h

Figure 14-26. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
78100h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
78100h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
78100h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-57. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	78100h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.27 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H Register

14.1.1.2.27.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-58. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8034h

Figure 14-27. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-59. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.28 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L Register

14.1.1.2.28.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = 78107FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-60. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8038h

Figure 14-28. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
78107h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
78107h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
78107h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-61. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	78107h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.29 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H Register

14.1.1.2.29.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 1 firewall.

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Table 14-62. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 803Ch

Figure 14-29. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-63. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.30 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL Register

14.1.1.2.30.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL Register (Offset = 40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-64. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8040h

Figure 14-30. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-65. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.31 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Register

14.1.1.2.31.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-66. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8044h

Figure 14-31. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-67. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-67. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.32 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Register

14.1.1.2.32.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-68. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8048h

Figure 14-32. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-69. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-69. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.33 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Register

14.1.1.2.33.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-70. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 804Ch

Figure 14-33. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-71. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-71. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.34 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L Register

14.1.1.2.34.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 74000000h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-72. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8050h

Figure 14-34. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
74000h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
74000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
74000h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-73. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	74000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.35 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H Register

14.1.1.2.35.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-74. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8054h

Figure 14-35. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-75. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.36 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L Register

14.1.1.2.36.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = 747FFFFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-76. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8058h

Figure 14-36. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
747FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
747FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
747FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-77. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	747FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.37 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H Register

14.1.1.2.37.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 2 firewall.

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Table 14-78. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 805Ch

Figure 14-37. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-79. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.38 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL Register

14.1.1.2.38.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL Register (Offset = 60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-80. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8060h

Figure 14-38. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-81. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.39 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Register

14.1.1.2.39.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-82. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8064h

Figure 14-39. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-83. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-83. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.40 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Register

14.1.1.2.40.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-84. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8068h

Figure 14-40. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-85. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-85. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.41 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Register

14.1.1.2.41.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-86. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 806Ch

Figure 14-41. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-87. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-87. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.42 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L Register

14.1.1.2.42.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 74800000h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-88. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8070h

Figure 14-42. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
74800h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
74800h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
74800h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-89. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	74800h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.43 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H Register

14.1.1.2.43.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-90. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8074h

Figure 14-43. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-91. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.44 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L Register

14.1.1.2.44.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = 74FFFFFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-92. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8078h

Figure 14-44. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
74FFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
74FFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
74FFFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-93. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	74FFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.45 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H Register

14.1.1.2.45.1 CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Ipulsar_ul_wkup_0.cpu0_slv region 3 firewall.

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Table 14-94. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 807Ch

Figure 14-45. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-95. CBASS_FW_IPULSAR_UL_WKUP_0_CPU0_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.46 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Register

14.1.1.2.46.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Register (Offset = 400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 0 firewall.

Return to Summary Table

Table 14-96. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8400h

Figure 14-46. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-97. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-97. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.47 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register

14.1.1.2.47.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-98. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8404h

Figure 14-47. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-99. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-99. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.48 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register

14.1.1.2.48.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-100. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8408h

Figure 14-48. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-101. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-101. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.49 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register

14.1.1.2.49.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-102. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 840Ch

Figure 14-49. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-103. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-103. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.50 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register

14.1.1.2.50.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-104. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8410h

Figure 14-50. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-105. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.51 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register

14.1.1.2.51.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-106. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8414h

Figure 14-51. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-107. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.52
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register

14.1.1.2.52.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-108. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8418h

Figure 14-52. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-109. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.53 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register

14.1.1.2.53.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 0 firewall.

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Table 14-110. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 841Ch

Figure 14-53. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-111. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.54 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Register

14.1.1.2.54.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Register (Offset = 420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-112. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8420h

Figure 14-54. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-113. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-113. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.55 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register

14.1.1.2.55.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-114. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8424h

Figure 14-55. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-115. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-115. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.56 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register

14.1.1.2.56.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-116. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8428h

Figure 14-56. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-117. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-117. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.57
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register

14.1.1.2.57.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 42Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 1 firewall.

Return to Summary Table

Table 14-118. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 842Ch

Figure 14-57. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-119. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-119. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.58 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register

14.1.1.2.58.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 1 firewall.

Return to Summary Table

Table 14-120. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8430h

Figure 14-58. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-121. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.59 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register

14.1.1.2.59.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-122. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8434h

Figure 14-59. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-123. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.60 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register

14.1.1.2.60.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-124. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8438h

Figure 14-60. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-125. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.61 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register

14.1.1.2.61.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 1 firewall.

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Table 14-126. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 843Ch

Figure 14-61. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-127. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.62 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Register

14.1.1.2.62.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Register (Offset = 440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-128. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8440h

Figure 14-62. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-129. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-129. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.63 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register

14.1.1.2.63.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-130. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8444h

Figure 14-63. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-131. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-131. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.64 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register

14.1.1.2.64.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-132. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8448h

Figure 14-64. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-133. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-133. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.65 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register

14.1.1.2.65.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 44Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-134. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 844Ch

Figure 14-65. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-135. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-135. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.66 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register

14.1.1.2.66.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-136. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8450h

Figure 14-66. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-137. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.67 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register

14.1.1.2.67.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-138. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8454h

Figure 14-67. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-139. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.68 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register

14.1.1.2.68.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-140. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8458h

Figure 14-68. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-141. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.69 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register

14.1.1.2.69.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 2 firewall.

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Table 14-142. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 845Ch

Figure 14-69. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-143. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.70
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Register

14.1.1.2.70.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Register (Offset = 460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 3 firewall.

Return to Summary Table

Table 14-144. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8460h

Figure 14-70. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-145. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-145. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.71 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register

14.1.1.2.71.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 3 firewall.

Return to Summary Table

Table 14-146. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8464h

Figure 14-71. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-147. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-147. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.72 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register

14.1.1.2.72.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-148. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8468h

Figure 14-72. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-149. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-149. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.73 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register

14.1.1.2.73.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 46Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 3 firewall.

Return to Summary Table

Table 14-150. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 846Ch

Figure 14-73. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-151. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-151. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.74 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register

14.1.1.2.74.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-152. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8470h

Figure 14-74. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-153. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.75 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register

14.1.1.2.75.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-154. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8474h

Figure 14-75. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-155. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.76
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register

14.1.1.2.76.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 3 firewall.

Return to Summary Table

Table 14-156. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8478h

Figure 14-76. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-157. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.77 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register

14.1.1.2.77.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 3 firewall.

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Table 14-158. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 847Ch

Figure 14-77. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-159. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.78 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Register

14.1.1.2.78.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Register (Offset = 480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-160. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8480h

Figure 14-78. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-161. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-161. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.79 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register

14.1.1.2.79.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-162. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8484h

Figure 14-79. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-163. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-163. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.80 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register

14.1.1.2.80.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-164. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8488h

Figure 14-80. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-165. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-165. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.81
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register

14.1.1.2.81.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 48Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-166. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 848Ch

Figure 14-81. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-167. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-167. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.82
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register

14.1.1.2.82.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-168. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8490h

Figure 14-82. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-169. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.83
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register

14.1.1.2.83.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-170. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8494h

Figure 14-83. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-171. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.84 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register

14.1.1.2.84.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-172. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8498h

Figure 14-84. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-173. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.85
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register

14.1.1.2.85.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 49Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-174. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 849Ch

Figure 14-85. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-175. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.86 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Register

14.1.1.2.86.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Register (Offset = 4A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-176. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84A0h

Figure 14-86. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-177. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-177. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.87 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register

14.1.1.2.87.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 4A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 5 firewall.

Return to Summary Table

Table 14-178. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84A4h

Figure 14-87. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-179. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-179. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.88 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register

14.1.1.2.88.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 4A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-180. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84A8h

Figure 14-88. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-181. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-181. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.89 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register

14.1.1.2.89.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 4ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 5 firewall.

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Table 14-182. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84ACh

Figure 14-89. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-183. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-183. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.90 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register

14.1.1.2.90.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 4B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 5 firewall.

Return to Summary Table

Table 14-184. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84B0h

Figure 14-90. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-185. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.91 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register

14.1.1.2.91.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 4B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 5 firewall.

Return to Summary Table

Table 14-186. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84B4h

Figure 14-91. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-187. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.92

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register

14.1.1.2.92.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 4B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 5 firewall.

Return to Summary Table

Table 14-188. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84B8h

Figure 14-92. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-189. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.93 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register

14.1.1.2.93.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 4BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 5 firewall.

Return to Summary Table

Table 14-190. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84BCh

Figure 14-93. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-191. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.94 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Register

14.1.1.2.94.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Register (Offset = 4C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 6 firewall.

Return to Summary Table

Table 14-192. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84C0h

Figure 14-94. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-193. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-193. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.95 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register

14.1.1.2.95.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 4C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 6 firewall.

Return to Summary Table

Table 14-194. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84C4h

Figure 14-95. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-195. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-195. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.96 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register

14.1.1.2.96.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 4C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 6 firewall.

Return to Summary Table

Table 14-196. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84C8h

Figure 14-96. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-197. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-197. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.97 *CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register*

14.1.1.2.97.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 4CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 6 firewall.

Return to Summary Table

Table 14-198. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84CCh

Figure 14-97. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-199. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-199. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.98
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register

14.1.1.2.98.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 4D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-200. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84D0h

Figure 14-98. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-201. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.99 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register

14.1.1.2.99.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 4D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 6 firewall.

Return to Summary Table

Table 14-202. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84D4h

Figure 14-99. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-203. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.100

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register

14.1.1.2.100.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 4D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 6 firewall.

Return to Summary Table

Table 14-204. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84D8h

Figure 14-100. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-205. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.101 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register

14.1.1.2.101.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 4DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 6 firewall.

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Table 14-206. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84DCh

Figure 14-101. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-207. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.102 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Register

14.1.1.2.102.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Register (Offset = 4E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-208. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84E0h

Figure 14-102. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-209. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-209. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.103 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register

14.1.1.2.103.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 4E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-210. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84E4h

Figure 14-103. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-211. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-211. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.104 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register

14.1.1.2.104.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 4E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-212. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84E8h

Figure 14-104. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-213. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-213. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.105 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register

14.1.1.2.105.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 4ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-214. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84ECh

Figure 14-105. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-215. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-215. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.106 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register

14.1.1.2.106.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 4F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-216. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84F0h

Figure 14-106. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-217. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.107 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register

14.1.1.2.107.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 4F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-218. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84F4h

Figure 14-107. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-219. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.108 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register

14.1.1.2.108.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 4F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-220. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84F8h

Figure 14-108. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-221. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.109
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register

14.1.1.2.109.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 4FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 7 firewall.

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Table 14-222. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 84FCh

Figure 14-109. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-223. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.110
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Register

14.1.1.2.110.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Register (Offset = 500h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 8 firewall.

Return to Summary Table

Table 14-224. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8500h

Figure 14-110. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-225. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-225. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.111 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register

14.1.1.2.111.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 504h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 8 firewall.

Return to Summary Table

Table 14-226. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8504h

Figure 14-111. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-227. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-227. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.112 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register

14.1.1.2.112.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 508h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 8 firewall.

Return to Summary Table

Table 14-228. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8508h

Figure 14-112. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-229. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-229. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.113 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register

14.1.1.2.113.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 50Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 8 firewall.

Return to Summary Table

Table 14-230. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 850Ch

Figure 14-113. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-231. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-231. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.114 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register

14.1.1.2.114.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 510h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 8 firewall.

Return to Summary Table

Table 14-232. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8510h

Figure 14-114. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-233. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.115 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register

14.1.1.2.115.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 514h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-234. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8514h

Figure 14-115. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-235. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.116 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register

14.1.1.2.116.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 518h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 8 firewall.

Return to Summary Table

Table 14-236. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8518h

Figure 14-116. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-237. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.117
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register

14.1.1.2.117.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 51Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 8 firewall.

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Table 14-238. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 851Ch

Figure 14-117. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-239. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.118
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Register

14.1.1.2.118.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Register (Offset = 520h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-240. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8520h

Figure 14-118. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-241. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-241. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.119 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register

14.1.1.2.119.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 524h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-242. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8524h

Figure 14-119. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-243. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-243. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.120
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register

14.1.1.2.120.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 528h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-244. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8528h

Figure 14-120. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-245. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-245. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.121 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register

14.1.1.2.121.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 52Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-246. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 852Ch

Figure 14-121. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-247. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-247. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.122 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register

14.1.1.2.122.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 530h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-248. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8530h

Figure 14-122. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-249. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.123 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register

14.1.1.2.123.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 534h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-250. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8534h

Figure 14-123. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-251. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.124 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register

14.1.1.2.124.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 538h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-252. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8538h

Figure 14-124. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-253. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.125 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register

14.1.1.2.125.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 53Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 9 firewall.

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Table 14-254. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 853Ch

Figure 14-125. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-255. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.126 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Register

14.1.1.2.126.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Register (Offset = 540h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-256. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8540h

Figure 14-126. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-257. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-257. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.127 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register

14.1.1.2.127.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 544h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-258. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8544h

Figure 14-127. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-259. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-259. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.128 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register

14.1.1.2.128.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 548h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-260. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8548h

Figure 14-128. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-261. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-261. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.129 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register

14.1.1.2.129.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 54Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-262. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 854Ch

Figure 14-129. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-263. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-263. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.130

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register

14.1.1.2.130.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 550h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-264. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8550h

Figure 14-130. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-265. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.131 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register

14.1.1.2.131.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 554h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-266. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8554h

Figure 14-131. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-267. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.132 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register

14.1.1.2.132.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 558h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-268. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8558h

Figure 14-132. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-269. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.133 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register

14.1.1.2.133.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 55Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 10 firewall.

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Table 14-270. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 855Ch

Figure 14-133. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-271. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.134 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Register

14.1.1.2.134.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Register (Offset = 560h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-272. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8560h

Figure 14-134. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-273. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-273. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.135

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register

14.1.1.2.135.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 564h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 11 firewall.

Return to Summary Table

Table 14-274. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8564h

Figure 14-135. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-275. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-275. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.136 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register

14.1.1.2.136.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 568h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-276. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8568h

Figure 14-136. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-277. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-277. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.137 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register

14.1.1.2.137.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 56Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-278. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 856Ch

Figure 14-137. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-279. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-279. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.138

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register

14.1.1.2.138.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 570h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-280. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8570h

Figure 14-138. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-281. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.139 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register

14.1.1.2.139.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 574h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-282. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8574h

Figure 14-139. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-283. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.140 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register

14.1.1.2.140.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 578h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-284. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8578h

Figure 14-140. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-285. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.141 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register

14.1.1.2.141.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 57Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 11 firewall.

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Table 14-286. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 857Ch

Figure 14-141. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-287. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.142 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Register

14.1.1.2.142.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Register (Offset = 580h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-288. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8580h

Figure 14-142. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-289. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-289. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.143 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register

14.1.1.2.143.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 584h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-290. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8584h

Figure 14-143. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-291. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-291. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.144 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register

14.1.1.2.144.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 588h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-292. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8588h

Figure 14-144. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-293. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-293. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.145

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register

14.1.1.2.145.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 58Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-294. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 858Ch

Figure 14-145. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-295. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-295. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.146 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register

14.1.1.2.146.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 590h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-296. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8590h

Figure 14-146. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-297. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.147 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register

14.1.1.2.147.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 594h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-298. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8594h

Figure 14-147. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-299. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.148
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register

14.1.1.2.148.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 598h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-300. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8598h

Figure 14-148. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-301. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.149 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register

14.1.1.2.149.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 59Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 12 firewall.

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Table 14-302. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 859Ch

Figure 14-149. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-303. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.150 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Register

14.1.1.2.150.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Register (Offset = 5A0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-304. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85A0h

Figure 14-150. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-305. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-305. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.151 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register

14.1.1.2.151.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 5A4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-306. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85A4h

Figure 14-151. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-307. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-307. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.152 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register

14.1.1.2.152.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 5A8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 13 firewall.

Return to Summary Table

Table 14-308. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85A8h

Figure 14-152. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-309. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-309. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.153
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register

14.1.1.2.153.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 5ACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 13 firewall.

Return to Summary Table

Table 14-310. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85ACh

Figure 14-153. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-311. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-311. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.154
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register

14.1.1.2.154.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 5B0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 13 firewall.

Return to Summary Table

Table 14-312. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85B0h

Figure 14-154. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-313. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.155 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register

14.1.1.2.155.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 5B4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-314. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85B4h

Figure 14-155. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-315. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.156
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register

14.1.1.2.156.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 5B8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 13 firewall.

Return to Summary Table

Table 14-316. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85B8h

Figure 14-156. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-317. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.157 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register

14.1.1.2.157.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 5BCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 13 firewall.

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Table 14-318. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85BCh

Figure 14-157. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-319. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.158 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Register

14.1.1.2.158.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Register (Offset = 5C0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-320. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85C0h

Figure 14-158. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-321. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-321. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.159 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register

14.1.1.2.159.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 5C4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-322. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85C4h

Figure 14-159. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-323. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-323. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.160 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register

14.1.1.2.160.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 5C8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-324. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85C8h

Figure 14-160. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-325. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-325. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.161 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register

14.1.1.2.161.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 5CCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-326. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85CCh

Figure 14-161. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-327. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-327. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.162
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register

14.1.1.2.162.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 5D0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-328. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85D0h

Figure 14-162. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-329. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.163 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register

14.1.1.2.163.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 5D4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-330. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85D4h

Figure 14-163. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-331. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.164 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register

14.1.1.2.164.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 5D8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-332. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85D8h

Figure 14-164. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-333. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.165 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register

14.1.1.2.165.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 5DCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 14 firewall.

Return to Summary Table

Table 14-334. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85DCh

Figure 14-165. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-335. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.166 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Register

14.1.1.2.166.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Register (Offset = 5E0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 15 firewall.

Return to Summary Table

Table 14-336. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85E0h

Figure 14-166. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-337. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-337. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.167 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register

14.1.1.2.167.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 5E4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 15 firewall.

Return to Summary Table

Table 14-338. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85E4h

Figure 14-167. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-339. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-339. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.168 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register

14.1.1.2.168.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 5E8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 15 firewall.

Return to Summary Table

Table 14-340. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85E8h

Figure 14-168. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-341. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-341. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.169 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register

14.1.1.2.169.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 5ECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 15 firewall.

Return to Summary Table

Table 14-342. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85ECh

Figure 14-169. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-343. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-343. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.170

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register

14.1.1.2.170.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 5F0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 15 firewall.

Return to Summary Table

Table 14-344. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85F0h

Figure 14-170. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-345. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.171 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register

14.1.1.2.171.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 5F4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 15 firewall.

Return to Summary Table

Table 14-346. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85F4h

Figure 14-171. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-347. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.172 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register

14.1.1.2.172.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 5F8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 15 firewall.

Return to Summary Table

Table 14-348. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85F8h

Figure 14-172. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-349. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.173 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register

14.1.1.2.173.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 5FCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_main_infra_cbass_data_l0.slv region 15 firewall.

Return to Summary Table

Table 14-350. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 85FCh

Figure 14-173. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-351. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_MAIN_INFRA_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.174 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_CONTROL Register

14.1.1.2.174.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_CONTROL Register (Offset = 800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 0 firewall.

Return to Summary Table

Table 14-352. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8800h

Figure 14-174. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-353. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.175 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Register

14.1.1.2.175.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Register (Offset = 804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 0 firewall.

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Table 14-354. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8804h

Figure 14-175. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-355. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-355. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.176 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Register

14.1.1.2.176.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Register (Offset = 808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 0 firewall.

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Table 14-356. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8808h

Figure 14-176. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-357. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-357. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.177 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Register

14.1.1.2.177.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Register (Offset = 80Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 0 firewall.

Return to Summary Table

Table 14-358. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 880Ch

Figure 14-177. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-359. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-359. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.178 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register

14.1.1.2.178.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 0 firewall.

Return to Summary Table

Table 14-360. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8810h

Figure 14-178. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-361. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.179 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register

14.1.1.2.179.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 0 firewall.

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Table 14-362. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8814h

Figure 14-179. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-363. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.180 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register

14.1.1.2.180.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 0 firewall.

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Table 14-364. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8818h

Figure 14-180. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-365. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.181 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register

14.1.1.2.181.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 0 firewall.

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Table 14-366. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 881Ch

Figure 14-181. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-367. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.182 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_CONTROL Register

14.1.1.2.182.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_CONTROL Register (Offset = 820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 1 firewall.

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Table 14-368. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8820h

Figure 14-182. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-369. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.183 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Register

14.1.1.2.183.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Register (Offset = 824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 1 firewall.

Return to Summary Table

Table 14-370. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8824h

Figure 14-183. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-371. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-371. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.184 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Register

14.1.1.2.184.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Register (Offset = 828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 1 firewall.

Return to Summary Table

Table 14-372. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8828h

Figure 14-184. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-373. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-373. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.185 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Register

14.1.1.2.185.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Register (Offset = 82Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 1 firewall.

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Table 14-374. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 882Ch

Figure 14-185. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-375. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-375. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.186 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register

14.1.1.2.186.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 1 firewall.

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Table 14-376. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8830h

Figure 14-186. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-377. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.187 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register

14.1.1.2.187.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 1 firewall.

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Table 14-378. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8834h

Figure 14-187. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-379. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.188 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register

14.1.1.2.188.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 1 firewall.

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Table 14-380. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8838h

Figure 14-188. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-381. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.189 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register

14.1.1.2.189.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 1 firewall.

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Table 14-382. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 883Ch

Figure 14-189. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-383. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.190 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_CONTROL Register

14.1.1.2.190.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_CONTROL Register (Offset = 840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 2 firewall.

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Table 14-384. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8840h

Figure 14-190. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-385. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.191 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Register

14.1.1.2.191.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Register (Offset = 844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 2 firewall.

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Table 14-386. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8844h

Figure 14-191. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-387. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-387. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.192 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Register

14.1.1.2.192.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Register (Offset = 848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 2 firewall.

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Table 14-388. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8848h

Figure 14-192. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-389. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-389. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.193 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Register

14.1.1.2.193.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Register (Offset = 84Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 2 firewall.

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Table 14-390. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 884Ch

Figure 14-193. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-391. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-391. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.194 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register

14.1.1.2.194.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 2 firewall.

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Table 14-392. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8850h

Figure 14-194. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-393. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.195 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register

14.1.1.2.195.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 2 firewall.

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Table 14-394. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8854h

Figure 14-195. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-395. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.196 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register

14.1.1.2.196.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 2 firewall.

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Table 14-396. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8858h

Figure 14-196. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-397. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.197 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register

14.1.1.2.197.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 2 firewall.

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Table 14-398. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 885Ch

Figure 14-197. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-399. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.198 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_CONTROL Register

14.1.1.2.198.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_CONTROL Register (Offset = 860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 3 firewall.

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Table 14-400. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8860h

Figure 14-198. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-401. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.199 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Register

14.1.1.2.199.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Register (Offset = 864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 3 firewall.

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Table 14-402. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8864h

Figure 14-199. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-403. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-403. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.200 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Register

14.1.1.2.200.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Register (Offset = 868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 3 firewall.

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Table 14-404. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8868h

Figure 14-200. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-405. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-405. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.201 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Register

14.1.1.2.201.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Register (Offset = 86Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 3 firewall.

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Table 14-406. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 886Ch

Figure 14-201. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-407. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-407. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.202 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register

14.1.1.2.202.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 3 firewall.

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Table 14-408. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8870h

Figure 14-202. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-409. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.203 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register

14.1.1.2.203.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 3 firewall.

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Table 14-410. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8874h

Figure 14-203. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-411. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.204 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register

14.1.1.2.204.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 3 firewall.

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Table 14-412. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8878h

Figure 14-204. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-413. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.205 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register

14.1.1.2.205.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 3 firewall.

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Table 14-414. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 887Ch

Figure 14-205. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-415. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.206 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_CONTROL Register

14.1.1.2.206.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_CONTROL Register (Offset = 880h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 4 firewall.

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Table 14-416. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8880h

Figure 14-206. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-417. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.207 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Register

14.1.1.2.207.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Register (Offset = 884h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 4 firewall.

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Table 14-418. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8884h

Figure 14-207. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-419. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-419. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.208 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Register

14.1.1.2.208.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Register (Offset = 888h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 4 firewall.

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Table 14-420. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8888h

Figure 14-208. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-421. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-421. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.209 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Register

14.1.1.2.209.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Register (Offset = 88Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 4 firewall.

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Table 14-422. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 888Ch

Figure 14-209. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-423. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-423. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.210 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register

14.1.1.2.210.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = 890h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 4 firewall.

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Table 14-424. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8890h

Figure 14-210. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-425. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.211
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register

14.1.1.2.211.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = 894h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 4 firewall.

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Table 14-426. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8894h

Figure 14-211. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-427. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.212 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register

14.1.1.2.212.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = 898h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 4 firewall.

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Table 14-428. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8898h

Figure 14-212. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-429. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.213 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register

14.1.1.2.213.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = 89Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 4 firewall.

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Table 14-430. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 889Ch

Figure 14-213. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-431. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.214 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_CONTROL Register

14.1.1.2.214.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_CONTROL Register (Offset = 8A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 5 firewall.

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Table 14-432. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88A0h

Figure 14-214. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-433. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.215 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Register

14.1.1.2.215.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Register (Offset = 8A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 5 firewall.

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Table 14-434. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88A4h

Figure 14-215. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-435. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-435. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.216 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Register

14.1.1.2.216.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Register (Offset = 8A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 5 firewall.

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Table 14-436. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88A8h

Figure 14-216. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-437. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-437. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.217 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Register

14.1.1.2.217.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Register (Offset = 8ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 5 firewall.

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Table 14-438. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88ACh

Figure 14-217. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-439. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-439. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.218 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register

14.1.1.2.218.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = 8B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 5 firewall.

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Table 14-440. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88B0h

Figure 14-218. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-441. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.219 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register

14.1.1.2.219.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = 8B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 5 firewall.

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Table 14-442. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88B4h

Figure 14-219. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-443. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.220 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register

14.1.1.2.220.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = 8B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 5 firewall.

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Table 14-444. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88B8h

Figure 14-220. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-445. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.221 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register

14.1.1.2.221.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = 8BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 5 firewall.

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Table 14-446. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88BCh

Figure 14-221. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-447. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.222 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_CONTROL Register

14.1.1.2.222.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_CONTROL Register (Offset = 8C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 6 firewall.

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Table 14-448. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88C0h

Figure 14-222. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-449. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.223 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Register

14.1.1.2.223.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Register (Offset = 8C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 6 firewall.

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Table 14-450. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88C4h

Figure 14-223. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-451. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-451. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.224 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Register

14.1.1.2.224.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Register (Offset = 8C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 6 firewall.

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Table 14-452. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88C8h

Figure 14-224. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-453. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-453. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.225 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Register

14.1.1.2.225.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Register (Offset = 8CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 6 firewall.

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Table 14-454. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88CCh

Figure 14-225. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-455. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-455. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.226 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register

14.1.1.2.226.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = 8D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 6 firewall.

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Table 14-456. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88D0h

Figure 14-226. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-457. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.227 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register

14.1.1.2.227.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = 8D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 6 firewall.

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Table 14-458. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88D4h

Figure 14-227. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-459. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.228 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register

14.1.1.2.228.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = 8D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 6 firewall.

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Table 14-460. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88D8h

Figure 14-228. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-461. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.229 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register

14.1.1.2.229.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = 8DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 6 firewall.

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Table 14-462. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88DCh

Figure 14-229. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-463. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.230 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_CONTROL Register

14.1.1.2.230.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_CONTROL Register (Offset = 8E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 7 firewall.

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Table 14-464. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88E0h

Figure 14-230. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-465. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.231 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Register

14.1.1.2.231.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Register (Offset = 8E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 7 firewall.

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Table 14-466. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88E4h

Figure 14-231. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-467. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-467. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.232 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Register

14.1.1.2.232.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Register (Offset = 8E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 7 firewall.

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Table 14-468. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88E8h

Figure 14-232. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-469. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-469. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.233 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Register

14.1.1.2.233.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Register (Offset = 8ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 7 firewall.

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Table 14-470. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88ECh

Figure 14-233. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-471. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-471. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.234 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register

14.1.1.2.234.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = 8F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 7 firewall.

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Table 14-472. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88F0h

Figure 14-234. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-473. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.235 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register

14.1.1.2.235.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = 8F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 7 firewall.

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Table 14-474. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88F4h

Figure 14-235. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-475. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.236 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register

14.1.1.2.236.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = 8F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 7 firewall.

Return to Summary Table

Table 14-476. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88F8h

Figure 14-236. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-477. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.237 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register

14.1.1.2.237.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = 8FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 7 firewall.

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Table 14-478. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 88FCh

Figure 14-237. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-479. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.238 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_CONTROL Register

14.1.1.2.238.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_CONTROL Register (Offset = 900h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 8 firewall.

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Table 14-480. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8900h

Figure 14-238. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-481. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.239 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Register

14.1.1.2.239.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Register (Offset = 904h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 8 firewall.

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Table 14-482. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8904h

Figure 14-239. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-483. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-483. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.240 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Register

14.1.1.2.240.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Register (Offset = 908h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 8 firewall.

Return to Summary Table

Table 14-484. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8908h

Figure 14-240. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-485. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-485. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.241 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Register

14.1.1.2.241.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Register (Offset = 90Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 8 firewall.

Return to Summary Table

Table 14-486. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 890Ch

Figure 14-241. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-487. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-487. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.242 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L Register

14.1.1.2.242.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = 910h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 8 firewall.

Return to Summary Table

Table 14-488. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8910h

Figure 14-242. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-489. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.243 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H Register

14.1.1.2.243.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = 914h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 8 firewall.

Return to Summary Table

Table 14-490. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8914h

Figure 14-243. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-491. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.244 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L Register

14.1.1.2.244.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = 918h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 8 firewall.

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Table 14-492. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8918h

Figure 14-244. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-493. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.245 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H Register

14.1.1.2.245.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = 91Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 8 firewall.

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Table 14-494. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 891Ch

Figure 14-245. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-495. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.246 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_CONTROL Register

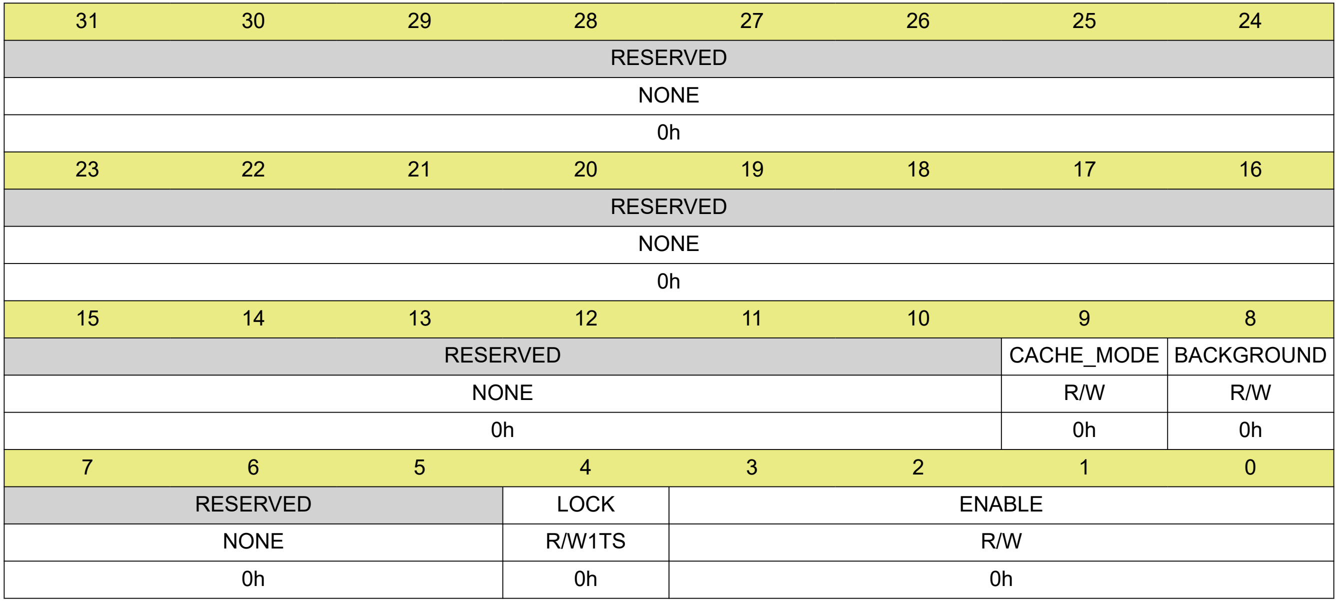
14.1.1.2.246.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_CONTROL Register (Offset = 920h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 9 firewall.

Return to Summary Table

Table 14-496. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8920h



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<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Figure 14-246. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_CONTROL Name Register

Table 14-497. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.247 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Register

14.1.1.2.247.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Register (Offset = 924h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 9 firewall.

Return to Summary Table

Table 14-498. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8924h

Figure 14-247. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-499. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-499. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.248 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Register

14.1.1.2.248.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Register (Offset = 928h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 9 firewall.

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Table 14-500. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8928h

Figure 14-248. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-501. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-501. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.249 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Register

14.1.1.2.249.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Register (Offset = 92Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 9 firewall.

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Table 14-502. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 892Ch

Figure 14-249. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-503. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-503. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.250 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L Register

14.1.1.2.250.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = 930h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 9 firewall.

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Table 14-504. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8930h

Figure 14-250. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-505. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.251
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H Register

14.1.1.2.251.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = 934h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 9 firewall.

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Table 14-506. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8934h

Figure 14-251. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-507. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.252 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L Register

14.1.1.2.252.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = 938h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 9 firewall.

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Table 14-508. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8938h

Figure 14-252. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-509. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.253 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H Register

14.1.1.2.253.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = 93Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 9 firewall.

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Table 14-510. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 893Ch

Figure 14-253. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-511. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.254 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_CONTROL Register

14.1.1.2.254.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_CONTROL Register (Offset = 940h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 10 firewall.

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Table 14-512. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8940h

Figure 14-254. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-513. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.255 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Register

14.1.1.2.255.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Register (Offset = 944h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 10 firewall.

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Table 14-514. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8944h

Figure 14-255. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-515. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-515. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.256 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Register

14.1.1.2.256.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Register (Offset = 948h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 10 firewall.

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Table 14-516. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8948h

Figure 14-256. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-517. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-517. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.257 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Register

14.1.1.2.257.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Register (Offset = 94Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 10 firewall.

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Table 14-518. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 894Ch

Figure 14-257. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-519. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-519. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.258 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L Register

14.1.1.2.258.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = 950h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 10 firewall.

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Table 14-520. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8950h

Figure 14-258. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-521. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.259 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H Register

14.1.1.2.259.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = 954h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 10 firewall.

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Table 14-522. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8954h

Figure 14-259. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-523. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.260 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L Register

14.1.1.2.260.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = 958h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 10 firewall.

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Table 14-524. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8958h

Figure 14-260. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-525. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.261 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H Register

14.1.1.2.261.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = 95Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 10 firewall.

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Table 14-526. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 895Ch

Figure 14-261. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-527. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.262 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_CONTROL Register

14.1.1.2.262.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_CONTROL Register (Offset = 960h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 11 firewall.

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Table 14-528. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8960h

Figure 14-262. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-529. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.263 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Register

14.1.1.2.263.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Register (Offset = 964h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 11 firewall.

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Table 14-530. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8964h

Figure 14-263. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-531. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-531. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.264 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Register

14.1.1.2.264.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Register (Offset = 968h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 11 firewall.

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Table 14-532. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8968h

Figure 14-264. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-533. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-533. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.265 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Register

14.1.1.2.265.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Register (Offset = 96Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 11 firewall.

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Table 14-534. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 896Ch

Figure 14-265. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-535. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-535. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.266
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L Register

14.1.1.2.266.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = 970h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 11 firewall.

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Table 14-536. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8970h

Figure 14-266. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-537. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.267 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H Register

14.1.1.2.267.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = 974h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 11 firewall.

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Table 14-538. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8974h

Figure 14-267. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-539. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.268 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L Register

14.1.1.2.268.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = 978h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 11 firewall.

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Table 14-540. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8978h

Figure 14-268. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-541. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.269 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H Register

14.1.1.2.269.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = 97Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 11 firewall.

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Table 14-542. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 897Ch

Figure 14-269. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-543. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.270 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_CONTROL Register

14.1.1.2.270.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_CONTROL Register (Offset = 980h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 12 firewall.

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Table 14-544. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4500 8980h

Figure 14-270. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-545. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.271 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Register

14.1.1.2.271.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Register (Offset = 984h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 12 firewall.

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Table 14-546. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8984h

Figure 14-271. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-547. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-547. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.272 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Register

14.1.1.2.272.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Register (Offset = 988h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 12 firewall.

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Table 14-548. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8988h

Figure 14-272. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-549. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-549. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.273 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Register

14.1.1.2.273.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Register (Offset = 98Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 12 firewall.

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Table 14-550. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 898Ch

Figure 14-273. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-551. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-551. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.274 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L Register

14.1.1.2.274.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = 990h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 12 firewall.

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Table 14-552. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8990h

Figure 14-274. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-553. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.275 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H Register

14.1.1.2.275.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = 994h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 12 firewall.

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Table 14-554. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8994h

Figure 14-275. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-555. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.276 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L Register

14.1.1.2.276.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = 998h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 12 firewall.

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Table 14-556. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8998h

Figure 14-276. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-557. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.277 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H Register

14.1.1.2.277.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = 99Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 12 firewall.

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Table 14-558. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 899Ch

Figure 14-277. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-559. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.278 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_CONTROL Register

14.1.1.2.278.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_CONTROL Register (Offset = 9A0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 13 firewall.

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Table 14-560. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89A0h

Figure 14-278. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-561. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.279 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Register

14.1.1.2.279.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Register (Offset = 9A4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 13 firewall.

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Table 14-562. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89A4h

Figure 14-279. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-563. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-563. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.280 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Register

14.1.1.2.280.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Register (Offset = 9A8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 13 firewall.

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Table 14-564. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89A8h

Figure 14-280. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-565. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-565. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.281 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Register

14.1.1.2.281.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Register (Offset = 9ACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 13 firewall.

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Table 14-566. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89ACh

Figure 14-281. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-567. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-567. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.282 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L Register

14.1.1.2.282.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = 9B0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 13 firewall.

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Table 14-568. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89B0h

Figure 14-282. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-569. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.283 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H Register

14.1.1.2.283.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = 9B4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 13 firewall.

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Table 14-570. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89B4h

Figure 14-283. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-571. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.284 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L Register

14.1.1.2.284.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = 9B8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 13 firewall.

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Table 14-572. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89B8h

Figure 14-284. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-573. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.285
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H Register

14.1.1.2.285.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = 9BCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 13 firewall.

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Table 14-574. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89BCh

**Figure 14-285.
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H Name Register**

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

**Table 14-575.
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions**

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.286 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_CONTROL Register

14.1.1.2.286.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_CONTROL Register (Offset = 9C0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 14 firewall.

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Table 14-576. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89C0h

Figure 14-286. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-577. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.287 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Register

14.1.1.2.287.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Register (Offset = 9C4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 14 firewall.

Return to Summary Table

Table 14-578. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89C4h

Figure 14-287. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-579. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-579. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.288 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Register

14.1.1.2.288.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Register (Offset = 9C8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 14 firewall.

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Table 14-580. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89C8h

Figure 14-288. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-581. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-581. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.289 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Register

14.1.1.2.289.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Register (Offset = 9CCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 14 firewall.

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Table 14-582. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89CCh

Figure 14-289. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-583. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-583. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.290 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L Register

14.1.1.2.290.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = 9D0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 14 firewall.

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Table 14-584. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89D0h

Figure 14-290. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-585. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.291 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H Register

14.1.1.2.291.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = 9D4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 14 firewall.

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Table 14-586. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89D4h

Figure 14-291. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-587. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.292 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L Register

14.1.1.2.292.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = 9D8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 14 firewall.

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Table 14-588. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89D8h

Figure 14-292. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-589. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.293

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H Register

14.1.1.2.293.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = 9DCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 14 firewall.

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Table 14-590. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89DCh

Figure 14-293. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-591. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.294 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_CONTROL Register

14.1.1.2.294.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_CONTROL Register (Offset = 9E0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 15 firewall.

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Table 14-592. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89E0h

Figure 14-294. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-593. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.295 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Register

14.1.1.2.295.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Register (Offset = 9E4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 15 firewall.

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Table 14-594. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89E4h

Figure 14-295. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-595. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-595. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.296 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Register

14.1.1.2.296.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Register (Offset = 9E8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 15 firewall.

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Table 14-596. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89E8h

Figure 14-296. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-597. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-597. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.297 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Register

14.1.1.2.297.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Register (Offset = 9ECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 15 firewall.

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Table 14-598. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89ECh

Figure 14-297. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-599. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-599. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.298 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L Register

14.1.1.2.298.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = 9F0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 15 firewall.

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Table 14-600. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89F0h

Figure 14-298. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-601. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.299 *CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H Register*

14.1.1.2.299.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = 9F4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 15 firewall.

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Table 14-602. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89F4h

Figure 14-299. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-603. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.300 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L Register

14.1.1.2.300.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = 9F8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 15 firewall.

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Table 14-604. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89F8h

Figure 14-300. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-605. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.301 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H Register

14.1.1.2.301.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = 9FCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 15 firewall.

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Table 14-606. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 89FCh

Figure 14-301. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-607. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.302 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_CONTROL Register

14.1.1.2.302.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_CONTROL Register (Offset = A00h) [reset = 0h]

The FW Region 16 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 16 firewall.

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Table 14-608. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A00h

Figure 14-302. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-609. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.303 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_0 Register

14.1.1.2.303.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_0 Register (Offset = A04h) [reset = 0h]

The FW Region 16 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 16 firewall.

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Table 14-610. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A04h

Figure 14-303. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-611. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-611. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.304 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_1 Register

14.1.1.2.304.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_1 Register (Offset = A08h) [reset = 0h]

The FW Region 16 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 16 firewall.

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Table 14-612. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A08h

Figure 14-304. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-613. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-613. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.305 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_2 Register

14.1.1.2.305.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_2 Register (Offset = A0Ch) [reset = 0h]

The FW Region 16 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 16 firewall.

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Table 14-614. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A0Ch

Figure 14-305. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-615. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-615. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.306 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_L Register

14.1.1.2.306.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_L Register (Offset = A10h) [reset = 0h]

The FW Region 16 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 16 firewall.

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Table 14-616. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A10h

Figure 14-306. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-617. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.307 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_H Register

14.1.1.2.307.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_H Register (Offset = A14h) [reset = 0h]

The FW Region 16 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 16 firewall.

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Table 14-618. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A14h

Figure 14-307. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-619. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.308 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_L Register

14.1.1.2.308.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_L Register (Offset = A18h) [reset = FFFh]

The FW Region 16 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 16 firewall.

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Table 14-620. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A18h

Figure 14-308. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-621. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.309 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_H Register

14.1.1.2.309.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_H Register (Offset = A1Ch) [reset = 0h]

The FW Region 16 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 16 firewall.

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Table 14-622. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A1Ch

Figure 14-309. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-623. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_16_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.310 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_CONTROL Register

14.1.1.2.310.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_CONTROL Register (Offset = A20h) [reset = 0h]

The FW Region 17 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 17 firewall.

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Table 14-624. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A20h

Figure 14-310. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-625. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.311 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_0 Register

14.1.1.2.311.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_0 Register (Offset = A24h) [reset = 0h]

The FW Region 17 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 17 firewall.

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Table 14-626. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A24h

Figure 14-311. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-627. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-627. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.312 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_1 Register

14.1.1.2.312.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_1 Register (Offset = A28h) [reset = 0h]

The FW Region 17 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 17 firewall.

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Table 14-628. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A28h

Figure 14-312. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-629. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-629. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.313 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_2 Register

14.1.1.2.313.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_2 Register (Offset = A2Ch) [reset = 0h]

The FW Region 17 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 17 firewall.

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Table 14-630. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A2Ch

Figure 14-313. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-631. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-631. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.314 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_L Register

14.1.1.2.314.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_L Register (Offset = A30h) [reset = 0h]

The FW Region 17 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 17 firewall.

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Table 14-632. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A30h

Figure 14-314. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-633. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.315 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_H Register

14.1.1.2.315.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_H Register (Offset = A34h) [reset = 0h]

The FW Region 17 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 17 firewall.

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Table 14-634. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A34h

Figure 14-315. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-635. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.316 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_L Register

14.1.1.2.316.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_L Register (Offset = A38h) [reset = FFFh]

The FW Region 17 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 17 firewall.

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Table 14-636. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A38h

Figure 14-316. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-637. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.317 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_H Register

14.1.1.2.317.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_H Register (Offset = A3Ch) [reset = 0h]

The FW Region 17 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 17 firewall.

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Table 14-638. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A3Ch

Figure 14-317. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-639. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_17_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.318 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_CONTROL Register

14.1.1.2.318.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_CONTROL Register (Offset = A40h) [reset = 0h]

The FW Region 18 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 18 firewall.

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Table 14-640. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A40h

Figure 14-318. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-641. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.319 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_0 Register

14.1.1.2.319.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_0 Register (Offset = A44h) [reset = 0h]

The FW Region 18 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 18 firewall.

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Table 14-642. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A44h

Figure 14-319. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-643. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-643. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.320 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_1 Register

14.1.1.2.320.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_1 Register (Offset = A48h) [reset = 0h]

The FW Region 18 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 18 firewall.

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Table 14-644. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A48h

Figure 14-320. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-645. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-645. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.321 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_2 Register

14.1.1.2.321.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_2 Register (Offset = A4Ch) [reset = 0h]

The FW Region 18 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 18 firewall.

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Table 14-646. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A4Ch

Figure 14-321. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-647. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-647. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.322 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_L Register

14.1.1.2.322.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_L Register (Offset = A50h) [reset = 0h]

The FW Region 18 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 18 firewall.

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Table 14-648. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A50h

Figure 14-322. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-649. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.323 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_H Register

14.1.1.2.323.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_H Register (Offset = A54h) [reset = 0h]

The FW Region 18 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 18 firewall.

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Table 14-650. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A54h

Figure 14-323. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-651. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.324 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_L Register

14.1.1.2.324.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_L Register (Offset = A58h) [reset = FFFh]

The FW Region 18 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 18 firewall.

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Table 14-652. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A58h

Figure 14-324. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-653. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.325 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_H Register

14.1.1.2.325.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_H Register (Offset = A5Ch) [reset = 0h]

The FW Region 18 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 18 firewall.

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Table 14-654. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A5Ch

Figure 14-325. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-655. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_18_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.326 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_CONTROL Register

14.1.1.2.326.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_CONTROL Register (Offset = A60h) [reset = 0h]

The FW Region 19 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 19 firewall.

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Table 14-656. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A60h

Figure 14-326. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-657. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.327 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_0 Register

14.1.1.2.327.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_0 Register (Offset = A64h) [reset = 0h]

The FW Region 19 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 19 firewall.

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Table 14-658. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A64h

Figure 14-327. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-659. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-659. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.328 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_1 Register

14.1.1.2.328.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_1 Register (Offset = A68h) [reset = 0h]

The FW Region 19 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 19 firewall.

Return to Summary Table

Table 14-660. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A68h

Figure 14-328. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-661. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-661. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.329 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_2 Register

14.1.1.2.329.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_2 Register (Offset = A6Ch) [reset = 0h]

The FW Region 19 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 19 firewall.

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Table 14-662. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A6Ch

Figure 14-329. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-663. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-663. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.330 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_L Register

14.1.1.2.330.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_L Register (Offset = A70h) [reset = 0h]

The FW Region 19 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 19 firewall.

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Table 14-664. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A70h

Figure 14-330. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-665. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.331 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_H Register

14.1.1.2.331.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_H Register (Offset = A74h) [reset = 0h]

The FW Region 19 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 19 firewall.

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Table 14-666. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A74h

Figure 14-331. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-667. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.332 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_L Register

14.1.1.2.332.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_L Register (Offset = A78h) [reset = FFFh]

The FW Region 19 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 19 firewall.

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Table 14-668. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A78h

Figure 14-332. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-669. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.333
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_H Register

14.1.1.2.333.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_H Register (Offset = A7Ch) [reset = 0h]

The FW Region 19 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 19 firewall.

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Table 14-670. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A7Ch

Figure 14-333. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-671. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_19_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.334 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_CONTROL Register

14.1.1.2.334.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_CONTROL Register (Offset = A80h) [reset = 0h]

The FW Region 20 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 20 firewall.

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Table 14-672. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A80h

Figure 14-334. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-673. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.335 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_0 Register

14.1.1.2.335.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_0 Register (Offset = A84h) [reset = 0h]

The FW Region 20 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 20 firewall.

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Table 14-674. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A84h

Figure 14-335. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-675. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-675. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.336 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_1 Register

14.1.1.2.336.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_1 Register (Offset = A88h) [reset = 0h]

The FW Region 20 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 20 firewall.

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Table 14-676. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A88h

Figure 14-336. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-677. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-677. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.337 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_2 Register

14.1.1.2.337.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_2 Register (Offset = A8Ch) [reset = 0h]

The FW Region 20 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 20 firewall.

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Table 14-678. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A8Ch

Figure 14-337. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-679. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-679. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.338 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_L Register

14.1.1.2.338.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_L Register (Offset = A90h) [reset = 0h]

The FW Region 20 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 20 firewall.

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Table 14-680. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A90h

Figure 14-338. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-681. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.339 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_H Register

14.1.1.2.339.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_H Register (Offset = A94h) [reset = 0h]

The FW Region 20 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 20 firewall.

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Table 14-682. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A94h

Figure 14-339. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-683. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.340 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_L Register

14.1.1.2.340.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_L Register (Offset = A98h) [reset = FFFh]

The FW Region 20 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 20 firewall.

Return to Summary Table

Table 14-684. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A98h

Figure 14-340. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-685. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.341 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_H Register

14.1.1.2.341.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_H Register (Offset = A9Ch) [reset = 0h]

The FW Region 20 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 20 firewall.

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Table 14-686. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8A9Ch

Figure 14-341. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-687. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_20_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.342 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_CONTROL Register

14.1.1.2.342.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_CONTROL Register (Offset = AA0h) [reset = 0h]

The FW Region 21 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 21 firewall.

Return to Summary Table

Table 14-688. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AA0h

Figure 14-342. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-689. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.343 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_0 Register

14.1.1.2.343.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_0 Register (Offset = AA4h) [reset = 0h]

The FW Region 21 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 21 firewall.

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Table 14-690. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AA4h

Figure 14-343. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-691. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-691. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.344 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_1 Register

14.1.1.2.344.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_1 Register (Offset = AA8h) [reset = 0h]

The FW Region 21 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 21 firewall.

Return to Summary Table

Table 14-692. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AA8h

Figure 14-344. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-693. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-693. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.345 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_2 Register

14.1.1.2.345.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_2 Register (Offset = AACh) [reset = 0h]

The FW Region 21 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 21 firewall.

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Table 14-694. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AACh

Figure 14-345. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-695. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-695. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.346
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_L Register

14.1.1.2.346.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_L Register (Offset = AB0h) [reset = 0h]

The FW Region 21 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 21 firewall.

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Table 14-696. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AB0h

Figure 14-346. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-697. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.347 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_H Register

14.1.1.2.347.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_H Register (Offset = AB4h) [reset = 0h]

The FW Region 21 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 21 firewall.

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Table 14-698. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AB4h

Figure 14-347. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-699. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.348 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_L Register

14.1.1.2.348.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_L Register (Offset = AB8h) [reset = FFFh]

The FW Region 21 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 21 firewall.

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Table 14-700. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AB8h

Figure 14-348. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-701. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.349 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_H Register

14.1.1.2.349.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_H Register (Offset = ABCh) [reset = 0h]

The FW Region 21 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 21 firewall.

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Table 14-702. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8ABCh

Figure 14-349. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-703. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_21_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.350 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_CONTROL Register

14.1.1.2.350.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_CONTROL Register (Offset = AC0h) [reset = 0h]

The FW Region 22 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 22 firewall.

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Table 14-704. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AC0h

Figure 14-350. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-705. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.351 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_0 Register

14.1.1.2.351.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_0 Register (Offset = AC4h) [reset = 0h]

The FW Region 22 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 22 firewall.

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Table 14-706. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AC4h

Figure 14-351. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-707. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-707. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.352 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_1 Register

14.1.1.2.352.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_1 Register (Offset = AC8h) [reset = 0h]

The FW Region 22 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 22 firewall.

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Table 14-708. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AC8h

Figure 14-352. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-709. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-709. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.353 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_2 Register

14.1.1.2.353.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_2 Register (Offset = ACCh) [reset = 0h]

The FW Region 22 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 22 firewall.

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Table 14-710. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8ACCh

Figure 14-353. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-711. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-711. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.354 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_L Register

14.1.1.2.354.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_L Register (Offset = AD0h) [reset = 0h]

The FW Region 22 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 22 firewall.

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Table 14-712. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AD0h

Figure 14-354. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-713. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.355
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_H Register

14.1.1.2.355.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_H Register (Offset = AD4h) [reset = 0h]

The FW Region 22 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 22 firewall.

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Table 14-714. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AD4h

Figure 14-355. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-715. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.356 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_L Register

14.1.1.2.356.1
CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_L Register (Offset = AD8h) [reset = FFFh]

The FW Region 22 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 22 firewall.

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Table 14-716. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AD8h

Figure 14-356. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-717. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.357 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_H Register

14.1.1.2.357.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_H Register (Offset = ADCh) [reset = 0h]

The FW Region 22 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 22 firewall.

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Table 14-718. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8ADCh

Figure 14-357. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-719. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_22_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.358 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_CONTROL Register

14.1.1.2.358.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_CONTROL Register (Offset = AE0h) [reset = 0h]

The FW Region 23 Control Register defines the control fields for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 23 firewall.

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Table 14-720. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4500 8AE0h

Figure 14-358. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-721. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_CONTROL Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.359 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_0 Register

14.1.1.2.359.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_0 Register (Offset = AE4h) [reset = 0h]

The FW Region 23 Permission 0 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 23 firewall.

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Table 14-722. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AE4h

Figure 14-359. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-723. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-723. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.360 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_1 Register

14.1.1.2.360.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_1 Register (Offset = AE8h) [reset = 0h]

The FW Region 23 Permission 1 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 23 firewall.

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Table 14-724. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AE8h

Figure 14-360. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-725. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-725. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.361 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_2 Register

14.1.1.2.361.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_2 Register (Offset = AECh) [reset = 0h]

The FW Region 23 Permission 2 Register defines the permissions for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 23 firewall.

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Table 14-726. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AECh

Figure 14-361. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-727. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-727. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.362 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_L Register

14.1.1.2.362.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_L Register (Offset = AF0h) [reset = 0h]

The FW Region 23 Start Address Low Register defines the start address bits 31 to 0 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 23 firewall.

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Table 14-728. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AF0h

Figure 14-362. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-729. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.363

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_H Register

14.1.1.2.363.1

CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_H Register (Offset = AF4h) [reset = 0h]

The FW Region 23 Start Address High Register defines the start address bits 47 to 32 for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 23 firewall.

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Table 14-730. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AF4h

Figure 14-363. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-731. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.364 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_L Register

14.1.1.2.364.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_L Register (Offset = AF8h) [reset = FFFh]

The FW Region 23 End Address Low Register defines the end address bits 31 to 0 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 23 firewall.

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Table 14-732. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AF8h

Figure 14-364. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-733. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.365 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_H Register

14.1.1.2.365.1 CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_H Register (Offset = AFCh) [reset = 0h]

The FW Region 23 End Address High Register defines the end address bits 47 to 32 to include for the target br_SCRM_64_DM_CLK1_to_SCRP_32_DM_CLK4_l0 region 23 firewall.

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Table 14-734. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8AFCh

Figure 14-365. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-735. CBASS_FW_BR_SCRM_64_DM_CLK1_TO_SCRP_32_DM_CLK4_L0_FW_REGION_23_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.366 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Register

14.1.1.2.366.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Register (Offset = C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-736. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C00h

Figure 14-366. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-737. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-737. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.367 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register

14.1.1.2.367.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register (Offset = C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-738. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C04h

Figure 14-367. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-739. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-739. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.368 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register

14.1.1.2.368.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register (Offset = C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-740. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C08h

Figure 14-368. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-741. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-741. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.369 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register

14.1.1.2.369.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register (Offset = C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-742. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C0Ch

Figure 14-369. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-743. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-743. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.370 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register

14.1.1.2.370.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 0h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-744. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C10h

Figure 14-370. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-745. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.371 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register

14.1.1.2.371.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-746. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C14h

Figure 14-371. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-747. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.372 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register

14.1.1.2.372.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-748. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C18h

Figure 14-372. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-749. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.373 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register

14.1.1.2.373.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 0 firewall.

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Table 14-750. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C1Ch

Figure 14-373. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-751. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.374 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Register

14.1.1.2.374.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Register (Offset = C20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-752. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C20h

Figure 14-374. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-753. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-753. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.375 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register

14.1.1.2.375.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register (Offset = C24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-754. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C24h

Figure 14-375. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-755. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-755. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.376 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register

14.1.1.2.376.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register (Offset = C28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-756. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C28h

Figure 14-376. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-757. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-757. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.377 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register

14.1.1.2.377.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register (Offset = C2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-758. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C2Ch

Figure 14-377. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-759. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-759. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.378 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register

14.1.1.2.378.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register (Offset = C30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-760. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C30h

Figure 14-378. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-761. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.379 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register

14.1.1.2.379.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register (Offset = C34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-762. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C34h

Figure 14-379. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-763. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.380 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register

14.1.1.2.380.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register (Offset = C38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-764. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C38h

Figure 14-380. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-765. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.381 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register

14.1.1.2.381.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register (Offset = C3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 1 firewall.

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Table 14-766. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C3Ch

Figure 14-381. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-767. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.382 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Register

14.1.1.2.382.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Register (Offset = C40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-768. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C40h

Figure 14-382. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-769. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-769. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.383 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register

14.1.1.2.383.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register (Offset = C44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-770. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C44h

Figure 14-383. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-771. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-771. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.384 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register

14.1.1.2.384.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register (Offset = C48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-772. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C48h

Figure 14-384. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-773. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-773. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.385 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register

14.1.1.2.385.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register (Offset = C4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 2 firewall.

Return to Summary Table

Table 14-774. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C4Ch

Figure 14-385. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-775. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-775. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.386
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register

14.1.1.2.386.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register (Offset = C50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 2 firewall.

Return to Summary Table

Table 14-776. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C50h

Figure 14-386. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-777. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.387
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register

14.1.1.2.387.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register (Offset = C54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-778. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C54h

Figure 14-387. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-779. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.388
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register

14.1.1.2.388.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register (Offset = C58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-780. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C58h

Figure 14-388. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-781. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.389

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register

14.1.1.2.389.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register (Offset = C5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 2 firewall.

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Table 14-782. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C5Ch

Figure 14-389. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-783. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.390 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Register

14.1.1.2.390.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Register (Offset = C60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-784. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C60h

Figure 14-390. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-785. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-785. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.391
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register

14.1.1.2.391.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register (Offset = C64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-786. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C64h

Figure 14-391. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-787. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-787. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.392 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register

14.1.1.2.392.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register (Offset = C68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-788. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C68h

Figure 14-392. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-789. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-789. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.393 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register

14.1.1.2.393.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register (Offset = C6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-790. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C6Ch

Figure 14-393. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-791. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-791. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.394 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register

14.1.1.2.394.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register (Offset = C70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-792. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C70h

Figure 14-394. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-793. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.395 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register

14.1.1.2.395.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register (Offset = C74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-794. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C74h

Figure 14-395. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-795. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.396 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register

14.1.1.2.396.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register (Offset = C78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-796. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C78h

Figure 14-396. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-797. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.397 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register

14.1.1.2.397.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register (Offset = C7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 3 firewall.

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Table 14-798. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C7Ch

Figure 14-397. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-799. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.398 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Register

14.1.1.2.398.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Register (Offset = C80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-800. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C80h

Figure 14-398. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-801. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-801. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.399 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register

14.1.1.2.399.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register (Offset = C84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-802. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C84h

Figure 14-399. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-803. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-803. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.400 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register

14.1.1.2.400.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register (Offset = C88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-804. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C88h

Figure 14-400. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-805. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-805. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.401 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register

14.1.1.2.401.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register (Offset = C8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-806. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C8Ch

Figure 14-401. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-807. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-807. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.402 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register

14.1.1.2.402.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register (Offset = C90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 4 firewall.

Return to Summary Table

Table 14-808. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C90h

Figure 14-402. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-809. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.403 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register

14.1.1.2.403.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register (Offset = C94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-810. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C94h

Figure 14-403. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-811. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.404
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register

14.1.1.2.404.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register (Offset = C98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-812. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C98h

Figure 14-404. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-813. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.405 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register

14.1.1.2.405.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register (Offset = C9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 4 firewall.

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Table 14-814. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8C9Ch

Figure 14-405. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-815. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.406 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Register

14.1.1.2.406.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Register (Offset = CA0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-816. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CA0h

Figure 14-406. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-817. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-817. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.407

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register

14.1.1.2.407.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register (Offset = CA4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-818. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CA4h

Figure 14-407. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-819. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-819. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.408 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register

14.1.1.2.408.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register (Offset = CA8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-820. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CA8h

Figure 14-408. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-821. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-821. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.409 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register

14.1.1.2.409.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register (Offset = CACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-822. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CACh

Figure 14-409. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-823. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-823. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.410 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register

14.1.1.2.410.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register (Offset = CB0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-824. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CB0h

Figure 14-410. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-825. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.411 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register

14.1.1.2.411.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register (Offset = CB4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-826. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CB4h

Figure 14-411. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-827. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.412 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register

14.1.1.2.412.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register (Offset = CB8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-828. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CB8h

Figure 14-412. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-829. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.413 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register

14.1.1.2.413.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register (Offset = CBCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 5 firewall.

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Table 14-830. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CBCh

Figure 14-413. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-831. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.414 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Register

14.1.1.2.414.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Register (Offset = CC0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-832. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CC0h

Figure 14-414. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-833. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-833. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.415 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register

14.1.1.2.415.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register (Offset = CC4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-834. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CC4h

Figure 14-415. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-835. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-835. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.416 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register

14.1.1.2.416.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register (Offset = CC8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-836. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CC8h

Figure 14-416. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-837. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-837. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.417 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register

14.1.1.2.417.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register (Offset = CCCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-838. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CCCh

Figure 14-417. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-839. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-839. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.418 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register

14.1.1.2.418.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register (Offset = CD0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-840. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CD0h

Figure 14-418. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-841. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.419

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register

14.1.1.2.419.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register (Offset = CD4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-842. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CD4h

Figure 14-419. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-843. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.420 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register

14.1.1.2.420.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register (Offset = CD8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-844. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CD8h

Figure 14-420. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-845. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.421
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register

14.1.1.2.421.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register (Offset = CDCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 6 firewall.

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Table 14-846. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CDCh

Figure 14-421. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-847. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.422 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Register

14.1.1.2.422.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Register (Offset = CE0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-848. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CE0h

Figure 14-422. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-849. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-849. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.423 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register

14.1.1.2.423.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register (Offset = CE4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-850. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CE4h

Figure 14-423. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-851. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-851. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.424 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register

14.1.1.2.424.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register (Offset = CE8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-852. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CE8h

Figure 14-424. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-853. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-853. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.425 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register

14.1.1.2.425.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register (Offset = CECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-854. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CECh

Figure 14-425. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-855. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-855. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.426 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register

14.1.1.2.426.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register (Offset = CF0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-856. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CF0h

Figure 14-426. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-857. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.427 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register

14.1.1.2.427.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register (Offset = CF4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-858. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CF4h

Figure 14-427. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-859. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.428 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register

14.1.1.2.428.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register (Offset = CF8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-860. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CF8h

Figure 14-428. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-861. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.429 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register

14.1.1.2.429.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register (Offset = CFCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 7 firewall.

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Table 14-862. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8CFCh

Figure 14-429. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-863. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.430 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Register

14.1.1.2.430.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Register (Offset = D00h) [reset = 0h]

The FW Region 8 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-864. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D00h

Figure 14-430. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-865. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-865. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.431 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register

14.1.1.2.431.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register (Offset = D04h) [reset = 0h]

The FW Region 8 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-866. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D04h

Figure 14-431. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-867. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-867. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.432 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register

14.1.1.2.432.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register (Offset = D08h) [reset = 0h]

The FW Region 8 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-868. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D08h

Figure 14-432. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-869. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-869. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.433 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register

14.1.1.2.433.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register (Offset = D0Ch) [reset = 0h]

The FW Region 8 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-870. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D0Ch

Figure 14-433. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-871. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-871. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.434
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register

14.1.1.2.434.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register (Offset = D10h) [reset = 0h]

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-872. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D10h

Figure 14-434. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-873. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.435
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register

14.1.1.2.435.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register (Offset = D14h) [reset = 0h]

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-874. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D14h

Figure 14-435. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-875. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.436
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register

14.1.1.2.436.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register (Offset = D18h) [reset = FFFh]

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-876. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D18h

Figure 14-436. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-877. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.437 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register

14.1.1.2.437.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register (Offset = D1Ch) [reset = 0h]

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 8 firewall.

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Table 14-878. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D1Ch

Figure 14-437. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-879. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.438

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Register

14.1.1.2.438.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Register (Offset = D20h) [reset = 0h]

The FW Region 9 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-880. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D20h

Figure 14-438. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-881. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-881. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.439 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register

14.1.1.2.439.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register (Offset = D24h) [reset = 0h]

The FW Region 9 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-882. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D24h

Figure 14-439. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-883. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-883. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.440 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register

14.1.1.2.440.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register (Offset = D28h) [reset = 0h]

The FW Region 9 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 9 firewall.

Return to Summary Table

Table 14-884. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D28h

Figure 14-440. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-885. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-885. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.441 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register

14.1.1.2.441.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register (Offset = D2Ch) [reset = 0h]

The FW Region 9 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-886. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D2Ch

Figure 14-441. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-887. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-887. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.442
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register

14.1.1.2.442.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register (Offset = D30h) [reset = 0h]

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 9 firewall.

Return to Summary Table

Table 14-888. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D30h

Figure 14-442. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-889. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.443

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register

14.1.1.2.443.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register (Offset = D34h) [reset = 0h]

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-890. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D34h

Figure 14-443. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-891. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.444 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register

14.1.1.2.444.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register (Offset = D38h) [reset = FFFh]

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-892. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D38h

Figure 14-444. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-893. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.445 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register

14.1.1.2.445.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register (Offset = D3Ch) [reset = 0h]

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 9 firewall.

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Table 14-894. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D3Ch

Figure 14-445. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-895. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.446

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Register

14.1.1.2.446.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Register (Offset = D40h) [reset = 0h]

The FW Region 10 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-896. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D40h

Figure 14-446. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-897. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-897. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.447 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register

14.1.1.2.447.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register (Offset = D44h) [reset = 0h]

The FW Region 10 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-898. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D44h

Figure 14-447. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-899. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-899. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.448 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register

14.1.1.2.448.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register (Offset = D48h) [reset = 0h]

The FW Region 10 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-900. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D48h

Figure 14-448. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-901. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-901. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.449 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register

14.1.1.2.449.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register (Offset = D4Ch) [reset = 0h]

The FW Region 10 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-902. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D4Ch

Figure 14-449. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-903. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-903. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.450
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register

14.1.1.2.450.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register (Offset = D50h) [reset = 0h]

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-904. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D50h

Figure 14-450. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-905. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.451 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register

14.1.1.2.451.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register (Offset = D54h) [reset = 0h]

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-906. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D54h

Figure 14-451. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-907. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.452 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register

14.1.1.2.452.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register (Offset = D58h) [reset = FFFh]

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 10 firewall.

Return to Summary Table

Table 14-908. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D58h

Figure 14-452. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-909. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.453 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register

14.1.1.2.453.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register (Offset = D5Ch) [reset = 0h]

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 10 firewall.

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Table 14-910. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D5Ch

Figure 14-453. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-911. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.454 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Register

14.1.1.2.454.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Register (Offset = D60h) [reset = 0h]

The FW Region 11 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 11 firewall.

Return to Summary Table

Table 14-912. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D60h

Figure 14-454. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-913. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-913. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.455 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register

14.1.1.2.455.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register (Offset = D64h) [reset = 0h]

The FW Region 11 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-914. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D64h

Figure 14-455. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-915. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-915. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.456 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register

14.1.1.2.456.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register (Offset = D68h) [reset = 0h]

The FW Region 11 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-916. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D68h

Figure 14-456. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-917. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-917. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.457 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register

14.1.1.2.457.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register (Offset = D6Ch) [reset = 0h]

The FW Region 11 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-918. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D6Ch

Figure 14-457. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-919. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-919. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.458 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register

14.1.1.2.458.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register (Offset = D70h) [reset = 0h]

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-920. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D70h

Figure 14-458. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-921. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.459 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register

14.1.1.2.459.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register (Offset = D74h) [reset = 0h]

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-922. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D74h

Figure 14-459. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-923. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.460 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register

14.1.1.2.460.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register (Offset = D78h) [reset = FFFh]

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 11 firewall.

Return to Summary Table

Table 14-924. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D78h

Figure 14-460. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-925. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.461 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register

14.1.1.2.461.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register (Offset = D7Ch) [reset = 0h]

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 11 firewall.

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Table 14-926. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D7Ch

Figure 14-461. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-927. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.462 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Register

14.1.1.2.462.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Register (Offset = D80h) [reset = 0h]

The FW Region 12 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-928. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D80h

Figure 14-462. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-929. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-929. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.463 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register

14.1.1.2.463.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register (Offset = D84h) [reset = 0h]

The FW Region 12 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-930. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D84h

Figure 14-463. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-931. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-931. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.464 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register

14.1.1.2.464.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register (Offset = D88h) [reset = 0h]

The FW Region 12 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-932. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D88h

Figure 14-464. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-933. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-933. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.465 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register

14.1.1.2.465.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register (Offset = D8Ch) [reset = 0h]

The FW Region 12 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-934. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D8Ch

Figure 14-465. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-935. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-935. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.466 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register

14.1.1.2.466.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register (Offset = D90h) [reset = 0h]

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-936. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D90h

Figure 14-466. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-937. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.467

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register

14.1.1.2.467.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register (Offset = D94h) [reset = 0h]

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-938. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D94h

Figure 14-467. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-939. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.468 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register

14.1.1.2.468.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register (Offset = D98h) [reset = FFFh]

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-940. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D98h

Figure 14-468. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-941. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.469 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register

14.1.1.2.469.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register (Offset = D9Ch) [reset = 0h]

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 12 firewall.

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Table 14-942. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8D9Ch

Figure 14-469. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-943. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.470
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Register

14.1.1.2.470.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Register (Offset = DA0h) [reset = 0h]

The FW Region 13 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-944. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4500 8DA0h

Figure 14-470. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-945. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-945. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.471 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register

14.1.1.2.471.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register (Offset = DA4h) [reset = 0h]

The FW Region 13 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-946. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DA4h

Figure 14-471. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-947. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-947. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.472 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register

14.1.1.2.472.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register (Offset = DA8h) [reset = 0h]

The FW Region 13 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-948. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DA8h

Figure 14-472. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-949. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-949. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.473 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register

14.1.1.2.473.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register (Offset = DACh) [reset = 0h]

The FW Region 13 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-950. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DACh

Figure 14-473. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-951. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-951. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.474 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register

14.1.1.2.474.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register (Offset = DB0h) [reset = 0h]

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-952. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DB0h

Figure 14-474. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-953. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.475 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register

14.1.1.2.475.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register (Offset = DB4h) [reset = 0h]

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-954. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DB4h

Figure 14-475. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-955. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.476 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register

14.1.1.2.476.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register (Offset = DB8h) [reset = FFFh]

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 13 firewall.

Return to Summary Table

Table 14-956. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DB8h

Figure 14-476. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-957. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.477 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register

14.1.1.2.477.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register (Offset = DBCh) [reset = 0h]

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 13 firewall.

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Table 14-958. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DBCh

Figure 14-477. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-959. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.478 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Register

14.1.1.2.478.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Register (Offset = DC0h) [reset = 0h]

The FW Region 14 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-960. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DC0h

Figure 14-478. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-961. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-961. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.479 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register

14.1.1.2.479.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register (Offset = DC4h) [reset = 0h]

The FW Region 14 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-962. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DC4h

Figure 14-479. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-963. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-963. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.480 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register

14.1.1.2.480.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register (Offset = DC8h) [reset = 0h]

The FW Region 14 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-964. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DC8h

Figure 14-480. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-965. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-965. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.481 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register

14.1.1.2.481.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register (Offset = DCCh) [reset = 0h]

The FW Region 14 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-966. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DCCh

Figure 14-481. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-967. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-967. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.482 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register

14.1.1.2.482.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register (Offset = DD0h) [reset = 0h]

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-968. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DD0h

Figure 14-482. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-969. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.483 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register

14.1.1.2.483.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register (Offset = DD4h) [reset = 0h]

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-970. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DD4h

Figure 14-483. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-971. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.484 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register

14.1.1.2.484.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register (Offset = DD8h) [reset = FFFh]

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-972. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DD8h

Figure 14-484. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-973. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.485 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register

14.1.1.2.485.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register (Offset = DDCh) [reset = 0h]

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 14 firewall.

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Table 14-974. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DDCh

Figure 14-485. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-975. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.486

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Register

14.1.1.2.486.1

CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Register (Offset = DE0h) [reset = 0h]

The FW Region 15 Control Register defines the control fields for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-976. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DE0h

Figure 14-486. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-977. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-977. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.487 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register

14.1.1.2.487.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register (Offset = DE4h) [reset = 0h]

The FW Region 15 Permission 0 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-978. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DE4h

Figure 14-487. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-979. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-979. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.488 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register

14.1.1.2.488.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register (Offset = DE8h) [reset = 0h]

The FW Region 15 Permission 1 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-980. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DE8h

Figure 14-488. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-981. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-981. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.489 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register

14.1.1.2.489.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register (Offset = DECh) [reset = 0h]

The FW Region 15 Permission 2 Register defines the permissions for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-982. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DECh

Figure 14-489. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-983. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-983. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.490 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register

14.1.1.2.490.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register (Offset = DF0h) [reset = 0h]

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-984. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DF0h

Figure 14-490. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-985. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.491 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register

14.1.1.2.491.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register (Offset = DF4h) [reset = 0h]

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-986. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DF4h

Figure 14-491. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-987. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.492
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register

14.1.1.2.492.1
CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register (Offset = DF8h) [reset = FFFh]

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-988. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DF8h

Figure 14-492. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-989. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.493 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register

14.1.1.2.493.1 CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register (Offset = DFCh) [reset = 0h]

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the target export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0.slv region 15 firewall.

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Table 14-990. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 8DFCh

Figure 14-493. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-991. CBASS_FW_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.494 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_CONTROL Register

14.1.1.2.494.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_CONTROL Register (Offset = 2000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Idmtimer_dmc1ms_wkup_0.timer_cfg_vbp region 0 firewall.

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Table 14-992. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A000h

Figure 14-494. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-993. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.495 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Register

14.1.1.2.495.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Register (Offset = 2004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Idmtimer_dmc1ms_wkup_0.timer_cfg_vbp region 0 firewall.

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Table 14-994. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A004h

Figure 14-495. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-995. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-995. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.496 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Register

14.1.1.2.496.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Register (Offset = 2008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Idmtimer_dmc1ms_wkup_0.timer_cfg_vbp region 0 firewall.

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Table 14-996. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A008h

Figure 14-496. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-997. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-997. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.497 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Register

14.1.1.2.497.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Register (Offset = 200Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Idmtimer_dmc1ms_wkup_0.timer_cfg_vbp region 0 firewall.

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Table 14-998. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A00Ch

Figure 14-497. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-999. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-999. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.498 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L Register

14.1.1.2.498.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L Register (Offset = 2010h) [reset = 2B100000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Idmtimer_dmc1ms_wkup_0.timer_cfg_vbp region 0 firewall.

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Table 14-1000. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A010h

Figure 14-498. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2B100h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
2B100h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2B100h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1001. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2B100h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.499 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H Register

14.1.1.2.499.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H Register (Offset = 2014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Idmtimer_dmc1ms_wkup_0.timer_cfg_vbp region 0 firewall.

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Table 14-1002. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A014h

Figure 14-499. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1003. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.500 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L Register

14.1.1.2.500.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L Register (Offset = 2018h) [reset = 2B100FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmtimer_dmc1ms_wkup_0.timer_cfg_vbp region 0 firewall.

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Table 14-1004. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A018h

Figure 14-500. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2B100h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
2B100h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2B100h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1005. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2B100h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.501 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H Register

14.1.1.2.501.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H Register (Offset = 201Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Idmtimer_dmc1ms_wkup_0.timer_cfg_vbp region 0 firewall.

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Table 14-1006. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A01Ch

Figure 14-501. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1007. CBASS_FW_IDMTIMER_DMC1MS_WKUP_0_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.502 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_CONTROL Register

14.1.1.2.502.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_CONTROL Register (Offset = 2400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Idmtimer_dmc1ms_wkup_1.timer_cfg_vbp region 0 firewall.

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Table 14-1008. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A400h

Figure 14-502. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1009. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.503 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Register

14.1.1.2.503.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Register (Offset = 2404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Idmtimer_dmc1ms_wkup_1.timer_cfg_vbp region 0 firewall.

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Table 14-1010. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A404h

Figure 14-503. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1011. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1011. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.504 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Register

14.1.1.2.504.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Register (Offset = 2408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Idmtimer_dmc1ms_wkup_1.timer_cfg_vbp region 0 firewall.

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Table 14-1012. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A408h

Figure 14-504. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1013. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1013. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.505 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Register

14.1.1.2.505.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Register (Offset = 240Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Idmtimer_dmc1ms_wkup_1.timer_cfg_vbp region 0 firewall.

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Table 14-1014. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A40Ch

Figure 14-505. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1015. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1015. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.506 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L Register

14.1.1.2.506.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L Register (Offset = 2410h) [reset = 2B110000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Idmtimer_dmc1ms_wkup_1.timer_cfg_vbp region 0 firewall.

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Table 14-1016. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A410h

Figure 14-506. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2B110h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
2B110h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2B110h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1017. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2B110h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.507 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H Register

14.1.1.2.507.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H Register (Offset = 2414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Idmtimer_dmc1ms_wkup_1.timer_cfg_vbp region 0 firewall.

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Table 14-1018. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A414h

Figure 14-507. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1019. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.508 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L Register

14.1.1.2.508.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L Register (Offset = 2418h) [reset = 2B110FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmtimer_dmc1ms_wkup_1.timer_cfg_vbp region 0 firewall.

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Table 14-1020. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A418h

Figure 14-508. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2B110h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2B110h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2B110h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1021. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2B110h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.509 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H Register

14.1.1.2.509.1 CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H Register (Offset = 241Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Idmtimer_dmc1ms_wkup_1.timer_cfg_vbp region 0 firewall.

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Table 14-1022. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4500 A41Ch

Figure 14-509. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1023. CBASS_FW_IDMTIMER_DMC1MS_WKUP_1_TIMER_CFG_VBP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.510 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Register

14.1.1.2.510.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Register (Offset = 0h) [reset = 10D400h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-1024. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4000h

Figure 14-510. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1025. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1025. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.511 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register

14.1.1.2.511.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-1026. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4010h

Figure 14-511. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1027. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.512 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register

14.1.1.2.512.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-1028. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4014h

Figure 14-512. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1029. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.513 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register

14.1.1.2.513.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-1030. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4018h

Figure 14-513. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1031. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.514 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register

14.1.1.2.514.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 0 ISC.

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Table 14-1032. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 401Ch

Figure 14-514. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1033. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.515 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Register

14.1.1.2.515.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Register (Offset = 20h) [reset = 10D400h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-1034. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4020h

Figure 14-515. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1035. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1035. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.516 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register

14.1.1.2.516.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-1036. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4030h

Figure 14-516. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1037. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.517 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register

14.1.1.2.517.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-1038. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4034h

Figure 14-517. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1039. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.518 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register

14.1.1.2.518.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-1040. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4038h

Figure 14-518. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1041. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.519 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register

14.1.1.2.519.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 1 ISC.

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Table 14-1042. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 403Ch

Figure 14-519. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1043. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.520 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Register

14.1.1.2.520.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Register (Offset = 40h) [reset = 10D400h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-1044. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4040h

Figure 14-520. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1045. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1045. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.521 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register

14.1.1.2.521.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-1046. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4050h

Figure 14-521. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-1047. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.522 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register

14.1.1.2.522.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-1048. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4054h

Figure 14-522. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1049. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.523 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register

14.1.1.2.523.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-1050. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4581 4058h

Figure 14-523. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1051. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.524 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register

14.1.1.2.524.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 2 ISC.

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Table 14-1052. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 405Ch

Figure 14-524. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1053. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.525 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Register

14.1.1.2.525.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Register (Offset = 60h) [reset = 10D400h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-1054. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4060h

Figure 14-525. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1055. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1055. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.526 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register

14.1.1.2.526.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-1056. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4070h

Figure 14-526. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1057. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.527 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register

14.1.1.2.527.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-1058. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4074h

Figure 14-527. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1059. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.528 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register

14.1.1.2.528.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-1060. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4078h

Figure 14-528. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1061. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.529 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register

14.1.1.2.529.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 3 ISC.

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Table 14-1062. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 407Ch

Figure 14-529. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1063. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.530 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register

14.1.1.2.530.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 80h) [reset = 10D44Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst region 4 ISC.

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Table 14-1064. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4080h

Figure 14-530. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-1065. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1065. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.531 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Register

14.1.1.2.531.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Register (Offset = 400h) [reset = 10D400h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-1066. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4400h

Figure 14-531. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1067. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1067. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.532 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register

14.1.1.2.532.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-1068. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4410h

Figure 14-532. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-1069. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.533 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register

14.1.1.2.533.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-1070. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4414h

Figure 14-533. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1071. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.534 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register

14.1.1.2.534.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-1072. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4418h

Figure 14-534. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1073. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.535 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register

14.1.1.2.535.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 0 ISC.

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Table 14-1074. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 441Ch

Figure 14-535. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1075. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.536 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Register

14.1.1.2.536.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Register (Offset = 420h) [reset = 10D400h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-1076. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4420h

Figure 14-536. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1077. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1077. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.537 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register

14.1.1.2.537.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-1078. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4430h

Figure 14-537. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1079. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.538 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register

14.1.1.2.538.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-1080. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4434h

Figure 14-538. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1081. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.539 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register

14.1.1.2.539.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-1082. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4581 4438h

Figure 14-539. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1083. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.540 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register

14.1.1.2.540.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 1 ISC.

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Table 14-1084. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 443Ch

Figure 14-540. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1085. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.541 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Register

14.1.1.2.541.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Register (Offset = 440h) [reset = 10D400h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-1086. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4440h

Figure 14-541. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1087. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1087. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.542 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register

14.1.1.2.542.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-1088. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4450h

Figure 14-542. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1089. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.543 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register

14.1.1.2.543.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-1090. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4454h

Figure 14-543. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-1091. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.544 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register

14.1.1.2.544.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-1092. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4458h

Figure 14-544. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1093. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.545 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register

14.1.1.2.545.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 2 ISC.

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Table 14-1094. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 445Ch

Figure 14-545. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1095. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.546 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Register

14.1.1.2.546.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Register (Offset = 460h) [reset = 10D400h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-1096. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4460h

Figure 14-546. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1097. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1097. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.547 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register

14.1.1.2.547.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-1098. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4470h

Figure 14-547. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1099. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.548 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register

14.1.1.2.548.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-1100. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4474h

Figure 14-548. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1101. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.549 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register

14.1.1.2.549.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-1102. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4478h

Figure 14-549. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1103. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.550 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register

14.1.1.2.550.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 3 ISC.

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Table 14-1104. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4581 447Ch

Figure 14-550. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1105. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.551 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register

14.1.1.2.551.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register (Offset = 480h) [reset = 10D44Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_rmst region 4 ISC.

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Table 14-1106. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4480h

Figure 14-551. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-1107. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1107. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_RMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.552 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Register

14.1.1.2.552.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Register (Offset = 800h) [reset = 10D400h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-1108. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4800h

Figure 14-552. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1109. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1109. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.553 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register

14.1.1.2.553.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-1110. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4810h

Figure 14-553. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-1111. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.554 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register

14.1.1.2.554.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-1112. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4814h

Figure 14-554. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1113. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.555 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register

14.1.1.2.555.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-1114. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4818h

Figure 14-555. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1115. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.556 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register

14.1.1.2.556.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 0 ISC.

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Table 14-1116. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 481Ch

Figure 14-556. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1117. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.557 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Register

14.1.1.2.557.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Register (Offset = 820h) [reset = 10D400h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-1118. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4820h

Figure 14-557. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1119. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1119. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.558 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register

14.1.1.2.558.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-1120. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4830h

Figure 14-558. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1121. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.559 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register

14.1.1.2.559.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-1122. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4834h

Figure 14-559. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1123. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.560 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register

14.1.1.2.560.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-1124. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4838h

Figure 14-560. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1125. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.561 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register

14.1.1.2.561.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 1 ISC.

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Table 14-1126. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 483Ch

Figure 14-561. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1127. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.562 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Register

14.1.1.2.562.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Register (Offset = 840h) [reset = 10D400h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-1128. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4840h

Figure 14-562. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1129. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1129. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.563 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register

14.1.1.2.563.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-1130. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4850h

Figure 14-563. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-1131. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.564 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register

14.1.1.2.564.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-1132. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4854h

Figure 14-564. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1133. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.565 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register

14.1.1.2.565.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-1134. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4858h

Figure 14-565. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1135. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.566 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register

14.1.1.2.566.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 2 ISC.

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Table 14-1136. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4581 485Ch

Figure 14-566. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1137. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.567 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Register

14.1.1.2.567.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Register (Offset = 860h) [reset = 10D400h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-1138. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4860h

Figure 14-567. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-1139. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-1139. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.568 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register

14.1.1.2.568.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-1140. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4870h

Figure 14-568. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1141. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.569 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register

14.1.1.2.569.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-1142. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4874h

Figure 14-569. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1143. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.570 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register

14.1.1.2.570.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-1144. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 4878h

Figure 14-570. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1145. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.571 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register

14.1.1.2.571.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 3 ISC.

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Table 14-1146. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	4581 487Ch

Figure 14-571. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							

7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1147. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.572 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register

14.1.1.2.572.1 CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register (Offset = 880h) [reset = 10D44Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_ul_wkup_0.cpu0_wmst region 4 ISC.

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Table 14-1148. Instance Table

Instance Name	**Physical Address**
WKUP_CBASS0	4581 4880h

Figure 14-572. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D4h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-1149. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1149. CBASS_ISC_IPULSAR_UL_WKUP_0_CPU0_WMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D4h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.573 CBASS_GLB_PID Register

14.1.1.2.573.1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66006102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-1150. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3000h

Figure 14-573. CBASS_GLB_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">600h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">600h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">Ch</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">2h</td></tr>
</table>

Table 14-1151. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	Ch	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.574 CBASS_GLB_DESTINATION_ID Register

14.1.1.2.574.1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-1152. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3004h

Figure 14-574. CBASS_GLB_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1153. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.575 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

14.1.1.2.575.1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-1154. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3020h

Figure 14-575. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-1155. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.576 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

14.1.1.2.576.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-1156. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3024h

Figure 14-576. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-1157. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.577 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

14.1.1.2.577.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

Return to Summary Table

Table 14-1158. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3028h

Figure 14-577. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-1159. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.1.2.578 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

14.1.1.2.578.1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-1160. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 302Ch

Figure 14-578. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-1161. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.579 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

14.1.1.2.579.1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-1162. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3030h

Figure 14-579. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-1163. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.580 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

14.1.1.2.580.1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-1164. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3034h

Figure 14-580. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-1165. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.581 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

14.1.1.2.581.1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-1166. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3038h

Figure 14-581. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-1167. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.582 CBASS_GLB_EXCEPTION_PEND_SET Register

14.1.1.2.582.1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-1168. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3040h

Figure 14-582. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-1169. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.583 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

14.1.1.2.583.1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-1170. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45B0 3044h

Figure 14-583. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PEND_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-1171. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.1.2.584 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0 Register

14.1.1.2.584.1 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0 Register (Offset = 100h) [reset = 7000h]

The Map Register defines the fields for the initiator Ipulsar_ul_wkup_0.cpu0_pmst per channel.

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Table 14-1172. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45D1 4100h

Figure 14-584. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-1173. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.585 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0 Register

14.1.1.2.585.1 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0 Register (Offset = 500h) [reset = 7000h]

The Map Register defines the fields for the initiator WKUP_R5FSS0 CPU0 Read Port per channel

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Table 14-1174. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45D1 4500h

Figure 14-585. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-1175. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_RMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.1.2.586 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0 Register

14.1.1.2.586.1 CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0 Register (Offset = 900h) [reset = 7000h]

The Map Register defines the fields for the initiator WKUP_R5FSS0 CPU0 Write Port per channel

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Table 14-1176. Instance Table

Instance Name	Physical Address
WKUP_CBASS0	45D1 4900h

Figure 14-586. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-1177. CBASS_QOS_IPULSAR_UL_WKUP_0_CPU0_WMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.2 CBASS_DBG

CBASS_DBG

14.1.2.1 CBASS_DBG Summaries

CBASS_DBG Summaries

Table 14-1178. CBASS_ERR Registers, Base Address=0020 0000h, Length=1024

Offset	Length	Register Name	CBASS_DBG0 Physical Address
0h	32	CBASS_ERR_PID	0020 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0020 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0020 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0020 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0020 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0020 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0020 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0020 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0020 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0020 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0020 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0020 005Ch
60h	32	CBASS_ERR_EOI	0020 0060h

14.1.2.2 CBASS_DBG Registers

CBASS_DBG Registers

14.1.2.2.1 CBASS_ERR_PID Register

14.1.2.2.1.1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66005102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-1179. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0000h

Figure 14-587. CBASS_ERR_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">600h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">600h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">Ah</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">2h</td></tr>
</table>

Table 14-1180. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:11	RTL	R	Ah	RTL revision. Will vary depending on release. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.2 CBASS_ERR_DESTINATION_ID Register

14.1.2.2.2.1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-1181. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0004h

Figure 14-588. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-1182. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

14.1.2.2.3.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-1183. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0024h

Figure 14-589. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-1184. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

14.1.2.2.4.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-1185. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0028h

Figure 14-590. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-1186. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.2.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

14.1.2.2.5.1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-1187. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 002Ch

Figure 14-591. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-1188. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

14.1.2.2.6.1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-1189. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0030h

Figure 14-592. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-1190. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

14.1.2.2.7.1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-1191. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0034h

Figure 14-593. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-1192. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

14.1.2.2.8.1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-1193. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0038h

Figure 14-594. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1194. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

14.1.2.2.9.1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-1195. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0050h

Figure 14-595. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-1196. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

14.1.2.2.10.1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-1197. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0054h

Figure 14-596. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-1198. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

14.1.2.2.11.1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-1199. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0058h

Figure 14-597. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-1200. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

14.1.2.2.12.1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-1201. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 005Ch

Figure 14-598. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-1202. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.2.2.13 CBASS_ERR_EOI Register

14.1.2.2.13.1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-1203. Instance Table

Instance Name	Physical Address
CBASS_DBG0	0020 0060h

Figure 14-599. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-1204. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3 CBASS_INFRA

CBASS_INFRA

14.1.3.1 CBASS_INFRA Summaries

CBASS_INFRA Summaries

Table 14-1205. CBASS_ERR Registers, Base Address=0021 0000h, Length=1024

Offset	Length	Register Name	CBASS_INFRA1 Physical Address
0h	32	CBASS_ERR_PID	0021 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0021 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0021 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0021 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0021 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0021 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0021 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0021 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0021 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0021 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0021 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0021 005Ch
60h	32	CBASS_ERR_EOI	0021 0060h

Table 14-1206. CBASS_FW Registers, Base Address=4502 0000h, Length=1024

Offset	Length	Register Name	CBASS_INFRA1 Physical Address
0h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_CONTROL	4502 0000h
4h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_0	4502 0004h
8h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_1	4502 0008h
Ch	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_2	4502 000Ch
20h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_CONTROL	4502 0020h
24h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_0	4502 0024h
28h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_1	4502 0028h
2Ch	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_2	4502 002Ch
40h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_CONTROL	4502 0040h
44h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_0	4502 0044h
48h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_1	4502 0048h
4Ch	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_2	4502 004Ch
60h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_CONTROL	4502 0060h
64h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_0	4502 0064h

Table 14-1206. CBASS_FW Registers, Base Address=4502 0000h, Length=1024 (continued)

Offset	Length	Register Name	CBASS_INFRA1 Physical Address
68h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_1	4502 0068h
6Ch	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_2	4502 006Ch
80h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_CONTROL	4502 0080h
84h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_0	4502 0084h
88h	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_1	4502 0088h
8Ch	32	CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_2	4502 008Ch

Table 14-1207. CBASS_GLB Registers, Base Address=45B0 9000h, Length=1024

Offset	Length	Register Name	CBASS_INFRA1 Physical Address
0h	32	CBASS_GLB_PID	45B0 9000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 9004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 9020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 9024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 9028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 902Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 9030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 9034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 9038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 9040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 9044h

14.1.3.2 CBASS_INFRA Registers

CBASS_INFRA Registers

14.1.3.2.1 CBASS_ERR_PID Register

14.1.3.2.1.1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66006102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-1208. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0000h

Figure 14-600. CBASS_ERR_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">600h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">600h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">Ch</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">2h</td></tr>
</table>

Table 14-1209. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:11	RTL	R	Ch	RTL revision. Will vary depending on release. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.2 CBASS_ERR_DESTINATION_ID Register

14.1.3.2.2.1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-1210. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0004h

Figure 14-601. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-1211. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

14.1.3.2.3.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-1212. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0024h

Figure 14-602. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-1213. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

14.1.3.2.4.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-1214. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0028h

Figure 14-603. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1215. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.3.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

14.1.3.2.5.1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-1216. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 002Ch

Figure 14-604. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-1217. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

14.1.3.2.6.1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-1218. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0030h

Figure 14-605. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-1219. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

14.1.3.2.7.1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-1220. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0034h

Figure 14-606. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			

23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-1221. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

14.1.3.2.8.1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-1222. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0038h

Figure 14-607. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-1223. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

14.1.3.2.9.1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-1224. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0050h

Figure 14-608. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-1225. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

14.1.3.2.10.1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-1226. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0054h

Figure 14-609. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-1227. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

14.1.3.2.11.1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-1228. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0058h

Figure 14-610. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-1229. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

14.1.3.2.12.1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-1230. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 005Ch

Figure 14-611. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-1231. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.13 CBASS_ERR_EOI Register

14.1.3.2.13.1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-1232. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	0021 0060h

Figure 14-612. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-1233. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.3.2.14 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_CONTROL Register

14.1.3.2.14.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Channel 0 Control Register defines the control fields for the target Iam275_main_psc_wrap_main_0.vbus region 0 channel 0 firewall.

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Table 14-1234. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0000h

Figure 14-613. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
NONE						R/W	NONE
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1235. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.15 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_0 Register

14.1.3.2.15.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Channel 0 Permission 0 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 0 channel 0 firewall.

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Table 14-1236. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0004h

Figure 14-614. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1237. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1237. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.16 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_1 Register

14.1.3.2.16.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Channel 0 Permission 1 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 0 channel 0 firewall.

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Table 14-1238. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0008h

Figure 14-615. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1239. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1239. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.17 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_2 Register

14.1.3.2.17.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Channel 0 Permission 2 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 0 channel 0 firewall.

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Table 14-1240. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 000Ch

Figure 14-616. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1241. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1241. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_0_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.18 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_CONTROL Register

14.1.3.2.18.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_CONTROL Register (Offset = 20h) [reset = 0h]

The FW Region 1 Channel 0 Control Register defines the control fields for the target Iam275_main_psc_wrap_main_0.vbus region 1 channel 0 firewall.

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Table 14-1242. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0020h

Figure 14-617. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
NONE						R/W	NONE
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1243. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.19 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_0 Register

14.1.3.2.19.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_0 Register (Offset = 24h) [reset = 0h]

The FW Region 1 Channel 0 Permission 0 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 1 channel 0 firewall.

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Table 14-1244. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0024h

Figure 14-618. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1245. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1245. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.20 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_1 Register

14.1.3.2.20.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_1 Register (Offset = 28h) [reset = 0h]

The FW Region 1 Channel 0 Permission 1 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 1 channel 0 firewall.

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Table 14-1246. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0028h

Figure 14-619. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1247. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1247. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.21 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_2 Register

14.1.3.2.21.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_2 Register (Offset = 2Ch) [reset = 0h]

The FW Region 1 Channel 0 Permission 2 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 1 channel 0 firewall.

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Table 14-1248. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 002Ch

Figure 14-620. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1249. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1249. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_1_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.22 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_CONTROL Register

14.1.3.2.22.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_CONTROL Register (Offset = 40h) [reset = 0h]

The FW Region 2 Channel 0 Control Register defines the control fields for the target Iam275_main_psc_wrap_main_0.vbus region 2 channel 0 firewall.

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Table 14-1250. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0040h

Figure 14-621. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>NONE</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1251. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.23 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_0 Register

14.1.3.2.23.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_0 Register (Offset = 44h) [reset = 0h]

The FW Region 2 Channel 0 Permission 0 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 2 channel 0 firewall.

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Table 14-1252. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0044h

Figure 14-622. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1253. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1253. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.24 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_1 Register

14.1.3.2.24.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_1 Register (Offset = 48h) [reset = 0h]

The FW Region 2 Channel 0 Permission 1 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 2 channel 0 firewall.

Return to Summary Table

Table 14-1254. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0048h

Figure 14-623. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1255. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1255. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.25 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_2 Register

14.1.3.2.25.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_2 Register (Offset = 4Ch) [reset = 0h]

The FW Region 2 Channel 0 Permission 2 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 2 channel 0 firewall.

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Table 14-1256. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 004Ch

Figure 14-624. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1257. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1257. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_2_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.26 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_CONTROL Register

14.1.3.2.26.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_CONTROL Register (Offset = 60h) [reset = 0h]

The FW Region 3 Channel 0 Control Register defines the control fields for the target Iam275_main_psc_wrap_main_0.vbus region 3 channel 0 firewall.

Return to Summary Table

Table 14-1258. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0060h

Figure 14-625. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>NONE</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1259. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.27 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_0 Register

14.1.3.2.27.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_0 Register (Offset = 64h) [reset = 0h]

The FW Region 3 Channel 0 Permission 0 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 3 channel 0 firewall.

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Table 14-1260. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0064h

Figure 14-626. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1261. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1261. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.28 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_1 Register

14.1.3.2.28.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_1 Register (Offset = 68h) [reset = 0h]

The FW Region 3 Channel 0 Permission 1 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 3 channel 0 firewall.

Return to Summary Table

Table 14-1262. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0068h

Figure 14-627. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1263. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1263. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.29 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_2 Register

14.1.3.2.29.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_2 Register (Offset = 6Ch) [reset = 0h]

The FW Region 3 Channel 0 Permission 2 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 3 channel 0 firewall.

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Table 14-1264. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 006Ch

Figure 14-628. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1265. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1265. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_3_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.30 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_CONTROL Register

14.1.3.2.30.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_CONTROL Register (Offset = 80h) [reset = 0h]

The FW Region 4 Channel 0 Control Register defines the control fields for the target Iam275_main_psc_wrap_main_0.vbus region 4 channel 0 firewall.

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Table 14-1266. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0080h

Figure 14-629. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CACHE_MODE	RESERVED
NONE						R/W	NONE
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1267. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.31 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_0 Register

14.1.3.2.31.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_0 Register (Offset = 84h) [reset = 0h]

The FW Region 4 Channel 0 Permission 0 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 4 channel 0 firewall.

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Table 14-1268. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0084h

Figure 14-630. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1269. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1269. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.32 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_1 Register

14.1.3.2.32.1 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_1 Register (Offset = 88h) [reset = 0h]

The FW Region 4 Channel 0 Permission 1 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 4 channel 0 firewall.

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Table 14-1270. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 0088h

Figure 14-631. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1271. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1271. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.33 CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_2 Register

14.1.3.2.33.1

CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_2 Register (Offset = 8Ch) [reset = 0h]

The FW Region 4 Channel 0 Permission 2 Register defines the permissions for the target Iam275_main_psc_wrap_main_0.vbus region 4 channel 0 firewall.

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Table 14-1272. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	4502 008Ch

Figure 14-632. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1273. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1273. CBASS_FW_IAM275_MAIN_PSC_WRAP_MAIN_0_VBUS_FWCH_REGION_4_CH_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.34 CBASS_GLB_PID Register

14.1.3.2.34.1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66006102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-1274. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9000h

Figure 14-633. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Ch					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-1275. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	Ch	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.35 CBASS_GLB_DESTINATION_ID Register

14.1.3.2.35.1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-1276. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9004h

Figure 14-634. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-1277. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.36 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

14.1.3.2.36.1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-1278. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9020h

Figure 14-635. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-1279. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.37 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

14.1.3.2.37.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-1280. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9024h

Figure 14-636. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-1281. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.38 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

14.1.3.2.38.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-1282. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9028h

Figure 14-637. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CODE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-1283. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.3.2.39 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

14.1.3.2.39.1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

Return to Summary Table

Table 14-1284. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 902Ch

Figure 14-638. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-1285. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.40 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

14.1.3.2.40.1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-1286. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9030h

Figure 14-639. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-1287. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.41 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

14.1.3.2.41.1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-1288. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9034h

Figure 14-640. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ROUTEID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRITE</td><td>READ</td><td>DEBUG</td><td>CACHEABLE</td><td>PRIV</td><td>SECURE</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1289. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.42 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

14.1.3.2.42.1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-1290. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9038h

Figure 14-641. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-1291. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.43 CBASS_GLB_EXCEPTION_PEND_SET Register

14.1.3.2.43.1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-1292. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9040h

Figure 14-642. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-1293. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.3.2.44 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

14.1.3.2.44.1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-1294. Instance Table

Instance Name	Physical Address
CBASS_INFRA1	45B0 9044h

Figure 14-643. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-1295. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.4 CBASS_MCASP

CBASS_MCASP

14.1.4.1 CBASS_MCASP Summaries

CBASS_MCASP Summaries

Table 14-1296. CBASS_ERR Registers, Base Address=0FEF 0000h, Length=1024

Offset	Length	Register Name	CBASS_MCASP0 Physical Address
0h	32	CBASS_ERR_PID	0FEF 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0FEF 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0FEF 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0FEF 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0FEF 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0FEF 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0FEF 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0FEF 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0FEF 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0FEF 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0FEF 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0FEF 005Ch
60h	32	CBASS_ERR_EOI	0FEF 0060h

14.1.4.2 CBASS_MCASP Registers

CBASS_MCASP Registers

14.1.4.2.1 CBASS_ERR_PID Register

14.1.4.2.1.1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66005102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-1297. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0000h

Figure 14-644. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Ah					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-1298. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
15:11	RTL	R	Ah	RTL revision. Will vary depending on release. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.2 CBASS_ERR_DESTINATION_ID Register

14.1.4.2.2.1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-1299. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0004h

Figure 14-645. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-1300. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

14.1.4.2.3.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-1301. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0024h

Figure 14-646. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TYPE_F</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1302. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

14.1.4.2.4.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-1303. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0028h

Figure 14-647. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1304. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.4.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

14.1.4.2.5.1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

Return to Summary Table

Table 14-1305. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 002Ch

Figure 14-648. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-1306. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

14.1.4.2.6.1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-1307. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0030h

Figure 14-649. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-1308. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

14.1.4.2.7.1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-1309. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0034h

Figure 14-650. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ROUTEID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRITE</td><td>READ</td><td>DEBUG</td><td>CACHEABLE</td><td>PRIV</td><td>SECURE</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1310. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

14.1.4.2.8.1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-1311. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0038h

Figure 14-651. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-1312. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

14.1.4.2.9.1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-1313. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0050h

Figure 14-652. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-1314. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

14.1.4.2.10.1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-1315. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0054h

Figure 14-653. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>ENABLED_INTR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-1316. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

14.1.4.2.11.1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-1317. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0058h

Figure 14-654. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-1318. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

14.1.4.2.12.1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-1319. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 005Ch

Figure 14-655. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-1320. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.4.2.13 CBASS_ERR_EOI Register

14.1.4.2.13.1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-1321. Instance Table

Instance Name	Physical Address
CBASS_MCASP0	0FEF 0060h

Figure 14-656. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-1322. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_32_CLK2_rst_mod_g_rst_n

14.1.5 CBASS_MEM

CBASS_MEM

14.1.5.1 CBASS_MEM Summaries

CBASS_MEM Summaries

Table 14-1323. CBASS_ERR Registers, Base Address=2020 0000h, Length=1024

Offset	Length	Register Name	CBASS_MEM0 Physical Address
0h	32	CBASS_ERR_PID	2020 0000h
4h	32	CBASS_ERR_DESTINATION_ID	2020 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	2020 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	2020 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	2020 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	2020 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	2020 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	2020 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	2020 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	2020 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	2020 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	2020 005Ch
60h	32	CBASS_ERR_EOI	2020 0060h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192

Offset	Length	Register Name	CBASS_MEM0 Physical Address
0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL	4504 0000h
4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0	4504 0004h
8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1	4504 0008h
Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2	4504 000Ch
10h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L	4504 0010h
14h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H	4504 0014h
18h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L	4504 0018h
1Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H	4504 001Ch
20h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL	4504 0020h
24h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0	4504 0024h
28h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1	4504 0028h
2Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2	4504 002Ch
30h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L	4504 0030h
34h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H	4504 0034h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
38h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L	4504 0038h
3Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H	4504 003Ch
40h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL	4504 0040h
44h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0	4504 0044h
48h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1	4504 0048h
4Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2	4504 004Ch
50h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L	4504 0050h
54h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H	4504 0054h
58h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L	4504 0058h
5Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H	4504 005Ch
60h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL	4504 0060h
64h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0	4504 0064h
68h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1	4504 0068h
6Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2	4504 006Ch
70h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L	4504 0070h
74h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H	4504 0074h
78h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L	4504 0078h
7Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H	4504 007Ch
80h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL	4504 0080h
84h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0	4504 0084h
88h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1	4504 0088h
8Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2	4504 008Ch
90h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L	4504 0090h
94h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H	4504 0094h
98h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L	4504 0098h
9Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H	4504 009Ch
A0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL	4504 00A0h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
A4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0	4504 00A4h
A8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1	4504 00A8h
ACh	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2	4504 00ACh
B0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L	4504 00B0h
B4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H	4504 00B4h
B8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L	4504 00B8h
BCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H	4504 00BCh
C0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL	4504 00C0h
C4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0	4504 00C4h
C8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1	4504 00C8h
CCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2	4504 00CCh
D0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L	4504 00D0h
D4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H	4504 00D4h
D8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L	4504 00D8h
DCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H	4504 00DCh
E0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL	4504 00E0h
E4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0	4504 00E4h
E8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1	4504 00E8h
ECh	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2	4504 00ECh
F0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L	4504 00F0h
F4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H	4504 00F4h
F8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L	4504 00F8h
FCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H	4504 00FCh
400h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_CONTROL	4504 0400h
404h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0	4504 0404h
408h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1	4504 0408h
40Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2	4504 040Ch

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
410h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L	4504 0410h
414h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H	4504 0414h
418h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L	4504 0418h
41Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H	4504 041Ch
420h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_CONTROL	4504 0420h
424h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0	4504 0424h
428h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1	4504 0428h
42Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2	4504 042Ch
430h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L	4504 0430h
434h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H	4504 0434h
438h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L	4504 0438h
43Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H	4504 043Ch
440h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_CONTROL	4504 0440h
444h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0	4504 0444h
448h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1	4504 0448h
44Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2	4504 044Ch
450h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L	4504 0450h
454h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H	4504 0454h
458h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L	4504 0458h
45Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H	4504 045Ch
460h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_CONTROL	4504 0460h
464h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0	4504 0464h
468h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1	4504 0468h
46Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2	4504 046Ch
470h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L	4504 0470h
474h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H	4504 0474h
478h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L	4504 0478h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
47Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H	4504 047Ch
480h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_CONTROL	4504 0480h
484h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_0	4504 0484h
488h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_1	4504 0488h
48Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_2	4504 048Ch
490h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_L	4504 0490h
494h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_H	4504 0494h
498h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_L	4504 0498h
49Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_H	4504 049Ch
4A0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_CONTROL	4504 04A0h
4A4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_0	4504 04A4h
4A8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_1	4504 04A8h
4ACh	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_2	4504 04ACh
4B0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_L	4504 04B0h
4B4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_H	4504 04B4h
4B8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_L	4504 04B8h
4BCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_H	4504 04BCh
4C0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_CONTROL	4504 04C0h
4C4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_0	4504 04C4h
4C8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_1	4504 04C8h
4CCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_2	4504 04CCh
4D0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_L	4504 04D0h
4D4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_H	4504 04D4h
4D8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_L	4504 04D8h
4DCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_H	4504 04DCh
4E0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_CONTROL	4504 04E0h
4E4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_0	4504 04E4h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
4E8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_1	4504 04E8h
4ECh	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_2	4504 04ECh
4F0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_L	4504 04F0h
4F4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_H	4504 04F4h
4F8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_L	4504 04F8h
4FCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_H	4504 04FCh
800h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_CONTROL	4504 0800h
804h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0	4504 0804h
808h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1	4504 0808h
80Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2	4504 080Ch
810h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L	4504 0810h
814h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H	4504 0814h
818h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L	4504 0818h
81Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H	4504 081Ch
820h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_CONTROL	4504 0820h
824h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0	4504 0824h
828h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1	4504 0828h
82Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2	4504 082Ch
830h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L	4504 0830h
834h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H	4504 0834h
838h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L	4504 0838h
83Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H	4504 083Ch
840h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_CONTROL	4504 0840h
844h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0	4504 0844h
848h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1	4504 0848h
84Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2	4504 084Ch
850h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L	4504 0850h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
854h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H	4504 0854h
858h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L	4504 0858h
85Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H	4504 085Ch
860h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_CONTROL	4504 0860h
864h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0	4504 0864h
868h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1	4504 0868h
86Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2	4504 086Ch
870h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L	4504 0870h
874h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H	4504 0874h
878h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L	4504 0878h
87Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H	4504 087Ch
880h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_CONTROL	4504 0880h
884h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_0	4504 0884h
888h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_1	4504 0888h
88Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_2	4504 088Ch
890h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_L	4504 0890h
894h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_H	4504 0894h
898h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_L	4504 0898h
89Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_H	4504 089Ch
8A0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_CONTROL	4504 08A0h
8A4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_0	4504 08A4h
8A8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_1	4504 08A8h
8ACh	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_2	4504 08ACh
8B0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_L	4504 08B0h
8B4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_H	4504 08B4h
8B8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_L	4504 08B8h
8BCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_H	4504 08BCh

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
8C0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_CONTROL	4504 08C0h
8C4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_0	4504 08C4h
8C8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_1	4504 08C8h
8CCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_2	4504 08CCh
8D0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_L	4504 08D0h
8D4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_H	4504 08D4h
8D8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_L	4504 08D8h
8DCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_H	4504 08DCh
8E0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_CONTROL	4504 08E0h
8E4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_0	4504 08E4h
8E8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_1	4504 08E8h
8ECh	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_2	4504 08ECh
8F0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_L	4504 08F0h
8F4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_H	4504 08F4h
8F8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_L	4504 08F8h
8FCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_H	4504 08FCh
C00h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_CONTROL	4504 0C00h
C04h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0	4504 0C04h
C08h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1	4504 0C08h
C0Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2	4504 0C0Ch
C10h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L	4504 0C10h
C14h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H	4504 0C14h
C18h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L	4504 0C18h
C1Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H	4504 0C1Ch
C20h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_CONTROL	4504 0C20h
C24h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0	4504 0C24h
C28h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1	4504 0C28h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
C2Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2	4504 0C2Ch
C30h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L	4504 0C30h
C34h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H	4504 0C34h
C38h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L	4504 0C38h
C3Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H	4504 0C3Ch
C40h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_CONTROL	4504 0C40h
C44h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0	4504 0C44h
C48h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1	4504 0C48h
C4Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2	4504 0C4Ch
C50h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L	4504 0C50h
C54h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H	4504 0C54h
C58h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L	4504 0C58h
C5Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H	4504 0C5Ch
C60h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_CONTROL	4504 0C60h
C64h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0	4504 0C64h
C68h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1	4504 0C68h
C6Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2	4504 0C6Ch
C70h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L	4504 0C70h
C74h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H	4504 0C74h
C78h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L	4504 0C78h
C7Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H	4504 0C7Ch
C80h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_CONTROL	4504 0C80h
C84h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_0	4504 0C84h
C88h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_1	4504 0C88h
C8Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_2	4504 0C8Ch
C90h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_L	4504 0C90h
C94h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_H	4504 0C94h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
C98h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_L	4504 0C98h
C9Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_H	4504 0C9Ch
CA0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_CONTROL	4504 0CA0h
CA4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_0	4504 0CA4h
CA8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_1	4504 0CA8h
CACh	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_2	4504 0CACh
CB0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_L	4504 0CB0h
CB4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_H	4504 0CB4h
CB8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_L	4504 0CB8h
CBCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_H	4504 0CBCh
CC0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_CONTROL	4504 0CC0h
CC4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_0	4504 0CC4h
CC8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_1	4504 0CC8h
CCCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_2	4504 0CCCh
CD0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_L	4504 0CD0h
CD4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_H	4504 0CD4h
CD8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_L	4504 0CD8h
CDCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_H	4504 0CDCh
CE0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_CONTROL	4504 0CE0h
CE4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_0	4504 0CE4h
CE8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_1	4504 0CE8h
CECh	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_2	4504 0CECh
CF0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_L	4504 0CF0h
CF4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_H	4504 0CF4h
CF8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_L	4504 0CF8h
CFCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_H	4504 0CFCh
1000h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_CONTROL	4504 1000h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
1004h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0	4504 1004h
1008h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1	4504 1008h
100Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2	4504 100Ch
1010h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L	4504 1010h
1014h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H	4504 1014h
1018h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L	4504 1018h
101Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H	4504 101Ch
1020h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_CONTROL	4504 1020h
1024h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0	4504 1024h
1028h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1	4504 1028h
102Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2	4504 102Ch
1030h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L	4504 1030h
1034h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H	4504 1034h
1038h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L	4504 1038h
103Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H	4504 103Ch
1040h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_CONTROL	4504 1040h
1044h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0	4504 1044h
1048h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1	4504 1048h
104Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2	4504 104Ch
1050h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L	4504 1050h
1054h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H	4504 1054h
1058h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L	4504 1058h
105Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H	4504 105Ch
1060h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_CONTROL	4504 1060h
1064h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0	4504 1064h
1068h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1	4504 1068h
106Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2	4504 106Ch

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
1070h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L	4504 1070h
1074h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H	4504 1074h
1078h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L	4504 1078h
107Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H	4504 107Ch
1080h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_CONTROL	4504 1080h
1084h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_0	4504 1084h
1088h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_1	4504 1088h
108Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_2	4504 108Ch
1090h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_L	4504 1090h
1094h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_H	4504 1094h
1098h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_L	4504 1098h
109Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_H	4504 109Ch
10A0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_CONTROL	4504 10A0h
10A4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_0	4504 10A4h
10A8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_1	4504 10A8h
10ACh	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_2	4504 10ACh
10B0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_L	4504 10B0h
10B4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_H	4504 10B4h
10B8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_L	4504 10B8h
10BCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_H	4504 10BCh
10C0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_CONTROL	4504 10C0h
10C4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_0	4504 10C4h
10C8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_1	4504 10C8h
10CCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_2	4504 10CCh
10D0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_L	4504 10D0h
10D4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_H	4504 10D4h
10D8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_L	4504 10D8h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
10DCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_H	4504 10DCh
10E0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_CONTROL	4504 10E0h
10E4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_0	4504 10E4h
10E8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_1	4504 10E8h
10ECh	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_2	4504 10ECh
10F0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_L	4504 10F0h
10F4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_H	4504 10F4h
10F8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_L	4504 10F8h
10FCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_H	4504 10FCh
1400h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_CONTROL	4504 1400h
1404h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0	4504 1404h
1408h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1	4504 1408h
140Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2	4504 140Ch
1410h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L	4504 1410h
1414h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H	4504 1414h
1418h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L	4504 1418h
141Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H	4504 141Ch
1420h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_CONTROL	4504 1420h
1424h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0	4504 1424h
1428h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1	4504 1428h
142Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2	4504 142Ch
1430h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L	4504 1430h
1434h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H	4504 1434h
1438h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L	4504 1438h
143Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H	4504 143Ch
1440h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_CONTROL	4504 1440h
1444h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0	4504 1444h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
1448h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1	4504 1448h
144Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2	4504 144Ch
1450h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L	4504 1450h
1454h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H	4504 1454h
1458h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L	4504 1458h
145Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H	4504 145Ch
1460h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_CONTROL	4504 1460h
1464h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0	4504 1464h
1468h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1	4504 1468h
146Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2	4504 146Ch
1470h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L	4504 1470h
1474h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H	4504 1474h
1478h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L	4504 1478h
147Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H	4504 147Ch
1480h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_CONTROL	4504 1480h
1484h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_0	4504 1484h
1488h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_1	4504 1488h
148Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_2	4504 148Ch
1490h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_L	4504 1490h
1494h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_H	4504 1494h
1498h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_L	4504 1498h
149Ch	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_H	4504 149Ch
14A0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_CONTROL	4504 14A0h
14A4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_0	4504 14A4h
14A8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_1	4504 14A8h
14ACh	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_2	4504 14ACh
14B0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_L	4504 14B0h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
14B4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_H	4504 14B4h
14B8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_L	4504 14B8h
14BCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_H	4504 14BCh
14C0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_CONTROL	4504 14C0h
14C4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_0	4504 14C4h
14C8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_1	4504 14C8h
14CCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_2	4504 14CCh
14D0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_L	4504 14D0h
14D4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_H	4504 14D4h
14D8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_L	4504 14D8h
14DCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_H	4504 14DCh
14E0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_CONTROL	4504 14E0h
14E4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_0	4504 14E4h
14E8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_1	4504 14E8h
14ECh	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_2	4504 14ECh
14F0h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_L	4504 14F0h
14F4h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_H	4504 14F4h
14F8h	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_L	4504 14F8h
14FCh	32	CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_H	4504 14FCh
1800h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL	4504 1800h
1804h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0	4504 1804h
1808h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1	4504 1808h
180Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2	4504 180Ch
1810h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L	4504 1810h
1814h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H	4504 1814h
1818h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L	4504 1818h
181Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H	4504 181Ch

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
1820h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL	4504 1820h
1824h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0	4504 1824h
1828h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1	4504 1828h
182Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2	4504 182Ch
1830h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L	4504 1830h
1834h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H	4504 1834h
1838h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L	4504 1838h
183Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H	4504 183Ch
1840h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL	4504 1840h
1844h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0	4504 1844h
1848h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1	4504 1848h
184Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2	4504 184Ch
1850h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L	4504 1850h
1854h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H	4504 1854h
1858h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L	4504 1858h
185Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H	4504 185Ch
1860h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL	4504 1860h
1864h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0	4504 1864h
1868h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1	4504 1868h
186Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2	4504 186Ch
1870h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L	4504 1870h
1874h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H	4504 1874h
1878h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L	4504 1878h
187Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H	4504 187Ch
1880h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL	4504 1880h
1884h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0	4504 1884h
1888h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1	4504 1888h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
188Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2	4504 188Ch
1890h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L	4504 1890h
1894h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H	4504 1894h
1898h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L	4504 1898h
189Ch	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H	4504 189Ch
18A0h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL	4504 18A0h
18A4h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0	4504 18A4h
18A8h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1	4504 18A8h
18ACh	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2	4504 18ACh
18B0h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L	4504 18B0h
18B4h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H	4504 18B4h
18B8h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L	4504 18B8h
18BCh	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H	4504 18BCh
18C0h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL	4504 18C0h
18C4h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0	4504 18C4h
18C8h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1	4504 18C8h
18CCh	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2	4504 18CCh
18D0h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L	4504 18D0h
18D4h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H	4504 18D4h
18D8h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L	4504 18D8h
18DCh	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H	4504 18DCh
18E0h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL	4504 18E0h
18E4h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0	4504 18E4h
18E8h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1	4504 18E8h
18ECh	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2	4504 18ECh
18F0h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L	4504 18F0h
18F4h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H	4504 18F4h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
18F8h	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L	4504 18F8h
18FCh	32	CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H	4504 18FCh
1C00h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL	4504 1C00h
1C04h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0	4504 1C04h
1C08h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1	4504 1C08h
1C0Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2	4504 1C0Ch
1C10h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L	4504 1C10h
1C14h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H	4504 1C14h
1C18h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L	4504 1C18h
1C1Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H	4504 1C1Ch
1C20h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL	4504 1C20h
1C24h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0	4504 1C24h
1C28h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1	4504 1C28h
1C2Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2	4504 1C2Ch
1C30h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L	4504 1C30h
1C34h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H	4504 1C34h
1C38h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L	4504 1C38h
1C3Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H	4504 1C3Ch
1C40h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL	4504 1C40h
1C44h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0	4504 1C44h
1C48h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1	4504 1C48h
1C4Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2	4504 1C4Ch
1C50h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L	4504 1C50h
1C54h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H	4504 1C54h
1C58h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L	4504 1C58h
1C5Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H	4504 1C5Ch
1C60h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL	4504 1C60h

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
1C64h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0	4504 1C64h
1C68h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1	4504 1C68h
1C6Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2	4504 1C6Ch
1C70h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L	4504 1C70h
1C74h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H	4504 1C74h
1C78h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L	4504 1C78h
1C7Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H	4504 1C7Ch
1C80h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL	4504 1C80h
1C84h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0	4504 1C84h
1C88h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1	4504 1C88h
1C8Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2	4504 1C8Ch
1C90h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L	4504 1C90h
1C94h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H	4504 1C94h
1C98h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L	4504 1C98h
1C9Ch	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H	4504 1C9Ch
1CA0h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL	4504 1CA0h
1CA4h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0	4504 1CA4h
1CA8h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1	4504 1CA8h
1CACh	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2	4504 1CACh
1CB0h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L	4504 1CB0h
1CB4h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H	4504 1CB4h
1CB8h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L	4504 1CB8h
1CBCh	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H	4504 1CBCh
1CC0h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL	4504 1CC0h
1CC4h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0	4504 1CC4h
1CC8h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1	4504 1CC8h
1CCCh	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2	4504 1CCCh

Table 14-1324. CBASS_FW Registers, Base Address=4504 0000h, Length=8192 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
1CD0h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L	4504 1CD0h
1CD4h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H	4504 1CD4h
1CD8h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L	4504 1CD8h
1CDCh	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H	4504 1CDCh
1CE0h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL	4504 1CE0h
1CE4h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0	4504 1CE4h
1CE8h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1	4504 1CE8h
1CECh	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2	4504 1CECh
1CF0h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L	4504 1CF0h
1CF4h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H	4504 1CF4h
1CF8h	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L	4504 1CF8h
1CFCh	32	CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H	4504 1CFCh

Table 14-1325. CBASS_ISC Registers, Base Address=4583 0000h, Length=16384

Offset	Length	Register Name	CBASS_MEM0 Physical Address
0h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL	4583 0000h
10h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L	4583 0010h
14h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H	4583 0014h
18h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L	4583 0018h
1Ch	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H	4583 001Ch
20h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL	4583 0020h
30h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L	4583 0030h
34h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H	4583 0034h
38h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L	4583 0038h
3Ch	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H	4583 003Ch
40h	32	CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL	4583 0040h
400h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL	4583 0400h
410h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L	4583 0410h

Table 14-1325. CBASS_ISC Registers, Base Address=4583 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
414h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H	4583 0414h
418h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L	4583 0418h
41Ch	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H	4583 041Ch
420h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL	4583 0420h
430h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L	4583 0430h
434h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H	4583 0434h
438h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L	4583 0438h
43Ch	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H	4583 043Ch
440h	32	CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL	4583 0440h
800h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_CONTROL	4583 0800h
810h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L	4583 0810h
814h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H	4583 0814h
818h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L	4583 0818h
81Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H	4583 081Ch
820h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_CONTROL	4583 0820h
830h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L	4583 0830h
834h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H	4583 0834h
838h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L	4583 0838h
83Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H	4583 083Ch
840h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_CONTROL	4583 0840h
850h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L	4583 0850h
854h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H	4583 0854h
858h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L	4583 0858h
85Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H	4583 085Ch
860h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_CONTROL	4583 0860h
870h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L	4583 0870h
874h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H	4583 0874h

Table 14-1325. CBASS_ISC Registers, Base Address=4583 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
878h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L	4583 0878h
87Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H	4583 087Ch
880h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_DEF_CONTROL	4583 0880h
C00h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_CONTROL	4583 0C00h
C10h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L	4583 0C10h
C14h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H	4583 0C14h
C18h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L	4583 0C18h
C1Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H	4583 0C1Ch
C20h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_CONTROL	4583 0C20h
C30h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L	4583 0C30h
C34h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H	4583 0C34h
C38h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L	4583 0C38h
C3Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H	4583 0C3Ch
C40h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_CONTROL	4583 0C40h
C50h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L	4583 0C50h
C54h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H	4583 0C54h
C58h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L	4583 0C58h
C5Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H	4583 0C5Ch
C60h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_CONTROL	4583 0C60h
C70h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L	4583 0C70h
C74h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H	4583 0C74h
C78h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L	4583 0C78h
C7Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H	4583 0C7Ch
C80h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_DEF_CONTROL	4583 0C80h
1000h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_CONTROL	4583 1000h
1010h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L	4583 1010h
1014h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H	4583 1014h

Table 14-1325. CBASS_ISC Registers, Base Address=4583 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
1018h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L	4583 1018h
101Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H	4583 101Ch
1020h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_CONTROL	4583 1020h
1030h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L	4583 1030h
1034h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H	4583 1034h
1038h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L	4583 1038h
103Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H	4583 103Ch
1040h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_CONTROL	4583 1040h
1050h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L	4583 1050h
1054h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H	4583 1054h
1058h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L	4583 1058h
105Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H	4583 105Ch
1060h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_CONTROL	4583 1060h
1070h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L	4583 1070h
1074h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H	4583 1074h
1078h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L	4583 1078h
107Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H	4583 107Ch
1080h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_DEF_CONTROL	4583 1080h
1400h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_CONTROL	4583 1400h
1410h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L	4583 1410h
1414h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H	4583 1414h
1418h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L	4583 1418h
141Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H	4583 141Ch
1420h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_CONTROL	4583 1420h
1430h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L	4583 1430h
1434h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H	4583 1434h
1438h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L	4583 1438h

Table 14-1325. CBASS_ISC Registers, Base Address=4583 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
143Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H	4583 143Ch
1440h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_CONTROL	4583 1440h
1450h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L	4583 1450h
1454h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H	4583 1454h
1458h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L	4583 1458h
145Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H	4583 145Ch
1460h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_CONTROL	4583 1460h
1470h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L	4583 1470h
1474h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H	4583 1474h
1478h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L	4583 1478h
147Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H	4583 147Ch
1480h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_DEF_CONTROL	4583 1480h
1800h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_CONTROL	4583 1800h
1810h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L	4583 1810h
1814h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H	4583 1814h
1818h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L	4583 1818h
181Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H	4583 181Ch
1820h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_CONTROL	4583 1820h
1830h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L	4583 1830h
1834h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H	4583 1834h
1838h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L	4583 1838h
183Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H	4583 183Ch
1840h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_CONTROL	4583 1840h
1850h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L	4583 1850h
1854h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H	4583 1854h
1858h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L	4583 1858h
185Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H	4583 185Ch

Table 14-1325. CBASS_ISC Registers, Base Address=4583 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
1860h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_CONTROL	4583 1860h
1870h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L	4583 1870h
1874h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H	4583 1874h
1878h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L	4583 1878h
187Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H	4583 187Ch
1880h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_DEF_CONTROL	4583 1880h
1C00h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_CONTROL	4583 1C00h
1C10h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L	4583 1C10h
1C14h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H	4583 1C14h
1C18h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L	4583 1C18h
1C1Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H	4583 1C1Ch
1C20h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_CONTROL	4583 1C20h
1C30h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L	4583 1C30h
1C34h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H	4583 1C34h
1C38h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L	4583 1C38h
1C3Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H	4583 1C3Ch
1C40h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_CONTROL	4583 1C40h
1C50h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L	4583 1C50h
1C54h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H	4583 1C54h
1C58h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L	4583 1C58h
1C5Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H	4583 1C5Ch
1C60h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_CONTROL	4583 1C60h
1C70h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L	4583 1C70h
1C74h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H	4583 1C74h
1C78h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L	4583 1C78h
1C7Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H	4583 1C7Ch
1C80h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_DEF_CONTROL	4583 1C80h

Table 14-1325. CBASS_ISC Registers, Base Address=4583 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
2000h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_CONTROL	4583 2000h
2010h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L	4583 2010h
2014h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H	4583 2014h
2018h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L	4583 2018h
201Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H	4583 201Ch
2020h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_CONTROL	4583 2020h
2030h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L	4583 2030h
2034h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H	4583 2034h
2038h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L	4583 2038h
203Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H	4583 203Ch
2040h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_CONTROL	4583 2040h
2050h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L	4583 2050h
2054h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H	4583 2054h
2058h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L	4583 2058h
205Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H	4583 205Ch
2060h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_CONTROL	4583 2060h
2070h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L	4583 2070h
2074h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H	4583 2074h
2078h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L	4583 2078h
207Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H	4583 207Ch
2080h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_DEF_CONTROL	4583 2080h
2400h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_CONTROL	4583 2400h
2410h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L	4583 2410h
2414h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H	4583 2414h
2418h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L	4583 2418h
241Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H	4583 241Ch
2420h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_CONTROL	4583 2420h

Table 14-1325. CBASS_ISC Registers, Base Address=4583 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
2430h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L	4583 2430h
2434h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H	4583 2434h
2438h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L	4583 2438h
243Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H	4583 243Ch
2440h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_CONTROL	4583 2440h
2450h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L	4583 2450h
2454h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H	4583 2454h
2458h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L	4583 2458h
245Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H	4583 245Ch
2460h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_CONTROL	4583 2460h
2470h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L	4583 2470h
2474h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H	4583 2474h
2478h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L	4583 2478h
247Ch	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H	4583 247Ch
2480h	32	CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_DEF_CONTROL	4583 2480h

Table 14-1326. CBASS_GLB Registers, Base Address=45B0 2000h, Length=1024

Offset	Length	Register Name	CBASS_MEM0 Physical Address
0h	32	CBASS_GLB_PID	45B0 2000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 2004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 2020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 2024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 2028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 202Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 2030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 2034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 2038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 2040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 2044h

Table 14-1327. CBASS_QOS Registers, Base Address=45D3 0000h, Length=16384

Offset	Length	Register Name	CBASS_MEM0 Physical Address
100h	32	CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP0	45D3 0100h
104h	32	CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP1	45D3 0104h

Table 14-1327. CBASS_QOS Registers, Base Address=45D3 0000h, Length=16384 (continued)

Offset	Length	Register Name	CBASS_MEM0 Physical Address
500h	32	CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP0	45D3 0500h
504h	32	CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP1	45D3 0504h
900h	32	CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_MAP0	45D3 0900h
D00h	32	CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_MAP0	45D3 0D00h
1100h	32	CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_MAP0	45D3 1100h
1500h	32	CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_MAP0	45D3 1500h
1900h	32	CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_MAP0	45D3 1900h
1D00h	32	CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_MAP0	45D3 1D00h
2100h	32	CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_MAP0	45D3 2100h
2500h	32	CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_MAP0	45D3 2500h

14.1.5.2 CBASS_MEM Registers

CBASS_MEM Registers

14.1.5.2.1 CBASS_ERR_PID Register

14.1.5.2.1.1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66005102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-1328. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0000h

Figure 14-657. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			

23	22	21	20	19	18	17	16
FUNC							
R							
600h							

15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Ah					1h		

7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-1329. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
15:11	RTL	R	Ah	RTL revision. Will vary depending on release. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.2 CBASS_ERR_DESTINATION_ID Register

14.1.5.2.2.1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-1330. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0004h

Figure 14-658. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEST_ID							
R/W							
0h							

Table 14-1331. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

14.1.5.2.3.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-1332. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0024h

Figure 14-659. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TYPE_F</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1333. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

14.1.5.2.4.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-1334. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0028h

Figure 14-660. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-1335. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.5.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

14.1.5.2.5.1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-1336. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 002Ch

Figure 14-661. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1337. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

14.1.5.2.6.1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-1338. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0030h

Figure 14-662. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-1339. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

14.1.5.2.7.1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-1340. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0034h

Figure 14-663. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ROUTEID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td>WRITE</td><td>READ</td><td>DEBUG</td><td>CACHEABLE</td><td>PRIV</td><td>SECURE</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1341. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

14.1.5.2.8.1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-1342. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0038h

Figure 14-664. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-1343. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

14.1.5.2.9.1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-1344. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0050h

Figure 14-665. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-1345. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

14.1.5.2.10.1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-1346. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0054h

Figure 14-666. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-1347. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

14.1.5.2.11.1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-1348. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0058h

Figure 14-667. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTR_ENABLE_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-1349. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

14.1.5.2.12.1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-1350. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 005Ch

Figure 14-668. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-1351. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.13 CBASS_ERR_EOI Register

14.1.5.2.13.1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-1352. Instance Table

Instance Name	Physical Address
CBASS_MEM0	2020 0060h

Figure 14-669. CBASS_ERR_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1353. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRM_256_MAIN_R5SS_CLK2_rst_mod_g_rst_n

14.1.5.2.14 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL Register

14.1.5.2.14.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imsram32kx256e_main_0.slv region 0 firewall.

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Table 14-1354. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0000h

Figure 14-670. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1355. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.15 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.5.2.15.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 0 firewall.

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Table 14-1356. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0004h

Figure 14-671. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1357. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1357. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.16 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.5.2.16.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 0 firewall.

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Table 14-1358. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0008h

Figure 14-672. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1359. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1359. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.17 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.5.2.17.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 0 firewall.

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Table 14-1360. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 000Ch

Figure 14-673. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1361. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1361. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.18 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.5.2.18.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 43C40000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_0.slv region 0 firewall.

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Table 14-1362. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0010h

Figure 14-674. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
43C40h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
43C40h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
43C40h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1363. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	43C40h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.19 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.5.2.19.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_0.slv region 0 firewall.

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Table 14-1364. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0014h

Figure 14-675. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1365. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.20 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.5.2.20.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 43D3FFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_0.slv region 0 firewall.

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Table 14-1366. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0018h

Figure 14-676. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
43D3Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
43D3Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
43D3Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1367. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	43D3Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.21 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.5.2.21.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_0.slv region 0 firewall.

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Table 14-1368. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 001Ch

Figure 14-677. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1369. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.22 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL Register

14.1.5.2.22.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL Register (Offset = 20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Imsram32kx256e_main_0.slv region 1 firewall.

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Table 14-1370. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0020h

Figure 14-678. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1371. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.23 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register

14.1.5.2.23.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 1 firewall.

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Table 14-1372. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0024h

Figure 14-679. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1373. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1373. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.24 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register

14.1.5.2.24.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 1 firewall.

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Table 14-1374. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0028h

Figure 14-680. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1375. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1375. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.25 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register

14.1.5.2.25.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 1 firewall.

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Table 14-1376. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 002Ch

Figure 14-681. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1377. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1377. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.26 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register

14.1.5.2.26.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_0.slv region 1 firewall.

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Table 14-1378. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0030h

Figure 14-682. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1379. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.27 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register

14.1.5.2.27.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_0.slv region 1 firewall.

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Table 14-1380. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0034h

Figure 14-683. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1381. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.28 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register

14.1.5.2.28.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_0.slv region 1 firewall.

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Table 14-1382. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0038h

Figure 14-684. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1383. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.29 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register

14.1.5.2.29.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_0.slv region 1 firewall.

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Table 14-1384. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 003Ch

Figure 14-685. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1385. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.30 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL Register

14.1.5.2.30.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL Register (Offset = 40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Imsram32kx256e_main_0.slv region 2 firewall.

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Table 14-1386. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0040h

Figure 14-686. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1387. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.31 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register

14.1.5.2.31.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 2 firewall.

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Table 14-1388. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0044h

Figure 14-687. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1389. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1389. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.32 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register

14.1.5.2.32.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 2 firewall.

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Table 14-1390. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0048h

Figure 14-688. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1391. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1391. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.33 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register

14.1.5.2.33.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 2 firewall.

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Table 14-1392. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 004Ch

Figure 14-689. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1393. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1393. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.34 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register

14.1.5.2.34.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_0.slv region 2 firewall.

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Table 14-1394. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0050h

Figure 14-690. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1395. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.35 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register

14.1.5.2.35.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_0.slv region 2 firewall.

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Table 14-1396. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0054h

Figure 14-691. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1397. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.36 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register

14.1.5.2.36.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_0.slv region 2 firewall.

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Table 14-1398. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0058h

Figure 14-692. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1399. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.37 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register

14.1.5.2.37.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_0.slv region 2 firewall.

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Table 14-1400. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 005Ch

Figure 14-693. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1401. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.38 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL Register

14.1.5.2.38.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL Register (Offset = 60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Imsram32kx256e_main_0.slv region 3 firewall.

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Table 14-1402. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0060h

Figure 14-694. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1403. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.39 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register

14.1.5.2.39.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 3 firewall.

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Table 14-1404. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0064h

Figure 14-695. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1405. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1405. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.40 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register

14.1.5.2.40.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 3 firewall.

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Table 14-1406. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0068h

Figure 14-696. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1407. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1407. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.41 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register

14.1.5.2.41.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 3 firewall.

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Table 14-1408. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 006Ch

Figure 14-697. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1409. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1409. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.42 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register

14.1.5.2.42.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_0.slv region 3 firewall.

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Table 14-1410. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0070h

Figure 14-698. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1411. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.43 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register

14.1.5.2.43.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_0.slv region 3 firewall.

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Table 14-1412. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0074h

Figure 14-699. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1413. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.44 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register

14.1.5.2.44.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_0.slv region 3 firewall.

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Table 14-1414. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0078h

Figure 14-700. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1415. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.45 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register

14.1.5.2.45.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_0.slv region 3 firewall.

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Table 14-1416. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 007Ch

Figure 14-701. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1417. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.46 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL Register

14.1.5.2.46.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL Register (Offset = 80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Imsram32kx256e_main_0.slv region 4 firewall.

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Table 14-1418. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0080h

Figure 14-702. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1419. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.47 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Register

14.1.5.2.47.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 4 firewall.

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Table 14-1420. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0084h

Figure 14-703. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1421. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1421. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.48 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Register

14.1.5.2.48.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 4 firewall.

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Table 14-1422. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0088h

Figure 14-704. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1423. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1423. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.49 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Register

14.1.5.2.49.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 4 firewall.

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Table 14-1424. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 008Ch

Figure 14-705. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1425. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1425. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.50 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L Register

14.1.5.2.50.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_0.slv region 4 firewall.

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Table 14-1426. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0090h

Figure 14-706. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1427. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.51 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H Register

14.1.5.2.51.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_0.slv region 4 firewall.

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Table 14-1428. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0094h

Figure 14-707. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1429. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.52 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L Register

14.1.5.2.52.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_0.slv region 4 firewall.

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Table 14-1430. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0098h

Figure 14-708. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1431. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.53 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H Register

14.1.5.2.53.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_0.slv region 4 firewall.

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Table 14-1432. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 009Ch

Figure 14-709. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1433. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.54 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL Register

14.1.5.2.54.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL Register (Offset = A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Imsram32kx256e_main_0.slv region 5 firewall.

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Table 14-1434. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00A0h

Figure 14-710. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1435. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.55 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Register

14.1.5.2.55.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 5 firewall.

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Table 14-1436. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00A4h

Figure 14-711. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1437. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1437. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.56 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Register

14.1.5.2.56.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 5 firewall.

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Table 14-1438. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00A8h

Figure 14-712. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1439. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1439. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.57 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Register

14.1.5.2.57.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 5 firewall.

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Table 14-1440. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00ACh

Figure 14-713. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1441. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1441. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.58 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L Register

14.1.5.2.58.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_0.slv region 5 firewall.

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Table 14-1442. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00B0h

Figure 14-714. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1443. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.59 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H Register

14.1.5.2.59.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_0.slv region 5 firewall.

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Table 14-1444. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00B4h

Figure 14-715. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1445. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.60 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L Register

14.1.5.2.60.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_0.slv region 5 firewall.

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Table 14-1446. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00B8h

Figure 14-716. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1447. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.61 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H Register

14.1.5.2.61.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_0.slv region 5 firewall.

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Table 14-1448. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00BCh

Figure 14-717. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1449. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.62 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL Register

14.1.5.2.62.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL Register (Offset = C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Imsram32kx256e_main_0.slv region 6 firewall.

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Table 14-1450. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00C0h

Figure 14-718. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1451. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.63 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Register

14.1.5.2.63.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 6 firewall.

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Table 14-1452. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00C4h

Figure 14-719. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1453. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1453. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.64 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Register

14.1.5.2.64.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 6 firewall.

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Table 14-1454. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00C8h

Figure 14-720. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1455. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1455. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.65 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Register

14.1.5.2.65.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 6 firewall.

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Table 14-1456. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00CCh

Figure 14-721. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1457. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1457. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.66 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L Register

14.1.5.2.66.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_0.slv region 6 firewall.

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Table 14-1458. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00D0h

Figure 14-722. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1459. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.67 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H Register

14.1.5.2.67.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_0.slv region 6 firewall.

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Table 14-1460. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00D4h

Figure 14-723. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1461. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.68 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L Register

14.1.5.2.68.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_0.slv region 6 firewall.

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Table 14-1462. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00D8h

Figure 14-724. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1463. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.69 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H Register

14.1.5.2.69.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_0.slv region 6 firewall.

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Table 14-1464. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00DCh

Figure 14-725. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1465. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.70 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL Register

14.1.5.2.70.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL Register (Offset = E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Imsram32kx256e_main_0.slv region 7 firewall.

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Table 14-1466. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00E0h

Figure 14-726. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1467. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.71 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Register

14.1.5.2.71.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 7 firewall.

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Table 14-1468. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00E4h

Figure 14-727. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1469. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1469. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.72 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Register

14.1.5.2.72.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 7 firewall.

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Table 14-1470. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00E8h

Figure 14-728. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1471. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1471. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.73 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Register

14.1.5.2.73.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_0.slv region 7 firewall.

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Table 14-1472. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00ECh

Figure 14-729. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1473. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1473. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.74 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L Register

14.1.5.2.74.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_0.slv region 7 firewall.

Return to Summary Table

Table 14-1474. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00F0h

Figure 14-730. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1475. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.75 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H Register

14.1.5.2.75.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_0.slv region 7 firewall.

Return to Summary Table

Table 14-1476. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00F4h

Figure 14-731. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1477. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.76 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L Register

14.1.5.2.76.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_0.slv region 7 firewall.

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Table 14-1478. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00F8h

Figure 14-732. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1479. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.77 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H Register

14.1.5.2.77.1 CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_0.slv region 7 firewall.

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Table 14-1480. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 00FCh

Figure 14-733. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1481. CBASS_FW_IMSRAM32KX256E_MAIN_0_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.78 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_CONTROL Register

14.1.5.2.78.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_CONTROL Register (Offset = 400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imsram32kx256e_main_1.slv region 0 firewall.

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Table 14-1482. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0400h

Figure 14-734. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1483. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.79 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.5.2.79.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 0 firewall.

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Table 14-1484. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0404h

Figure 14-735. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1485. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1485. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.80 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.5.2.80.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 0 firewall.

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Table 14-1486. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0408h

Figure 14-736. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1487. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1487. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.81 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.5.2.81.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 0 firewall.

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Table 14-1488. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 040Ch

Figure 14-737. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1489. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1489. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.82 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.5.2.82.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 72100000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_1.slv region 0 firewall.

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Table 14-1490. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0410h

Figure 14-738. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">72100h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">72100h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">72100h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1491. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	72100h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.83 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.5.2.83.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_1.slv region 0 firewall.

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Table 14-1492. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0414h

Figure 14-739. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1493. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.84 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.5.2.84.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = 721FFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_1.slv region 0 firewall.

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Table 14-1494. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0418h

Figure 14-740. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
721FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
721FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
721FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1495. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	721FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.85 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.5.2.85.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_1.slv region 0 firewall.

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Table 14-1496. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 041Ch

Figure 14-741. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1497. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.86 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_CONTROL Register

14.1.5.2.86.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_CONTROL Register (Offset = 420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Imsram32kx256e_main_1.slv region 1 firewall.

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Table 14-1498. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0420h

Figure 14-742. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1499. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.87 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Register

14.1.5.2.87.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 1 firewall.

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Table 14-1500. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0424h

Figure 14-743. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1501. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1501. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.88 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Register

14.1.5.2.88.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 1 firewall.

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Table 14-1502. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0428h

Figure 14-744. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1503. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1503. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.89 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Register

14.1.5.2.89.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 42Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 1 firewall.

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Table 14-1504. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 042Ch

Figure 14-745. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1505. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1505. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.90 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L Register

14.1.5.2.90.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_1.slv region 1 firewall.

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Table 14-1506. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0430h

Figure 14-746. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1507. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.91 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H Register

14.1.5.2.91.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_1.slv region 1 firewall.

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Table 14-1508. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0434h

Figure 14-747. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-1509. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.92 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L Register

14.1.5.2.92.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_1.slv region 1 firewall.

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Table 14-1510. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0438h

Figure 14-748. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1511. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.93 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H Register

14.1.5.2.93.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_1.slv region 1 firewall.

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Table 14-1512. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 043Ch

Figure 14-749. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1513. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.94 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_CONTROL Register

14.1.5.2.94.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_CONTROL Register (Offset = 440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Imsram32kx256e_main_1.slv region 2 firewall.

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Table 14-1514. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0440h

Figure 14-750. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1515. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.95 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Register

14.1.5.2.95.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 2 firewall.

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Table 14-1516. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0444h

Figure 14-751. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1517. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1517. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.96 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Register

14.1.5.2.96.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 2 firewall.

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Table 14-1518. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0448h

Figure 14-752. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1519. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1519. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.97 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Register

14.1.5.2.97.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 44Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 2 firewall.

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Table 14-1520. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 044Ch

Figure 14-753. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1521. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1521. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.98 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L Register

14.1.5.2.98.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_1.slv region 2 firewall.

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Table 14-1522. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0450h

Figure 14-754. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1523. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.99 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H Register

14.1.5.2.99.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_1.slv region 2 firewall.

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Table 14-1524. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0454h

Figure 14-755. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1525. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.100 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L Register

14.1.5.2.100.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_1.slv region 2 firewall.

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Table 14-1526. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0458h

Figure 14-756. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1527. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.101 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H Register

14.1.5.2.101.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_1.slv region 2 firewall.

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Table 14-1528. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 045Ch

Figure 14-757. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1529. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.102 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_CONTROL Register

14.1.5.2.102.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_CONTROL Register (Offset = 460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Imsram32kx256e_main_1.slv region 3 firewall.

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Table 14-1530. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0460h

Figure 14-758. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1531. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.103 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Register

14.1.5.2.103.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 3 firewall.

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Table 14-1532. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0464h

Figure 14-759. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1533. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1533. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.104 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Register

14.1.5.2.104.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 3 firewall.

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Table 14-1534. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0468h

Figure 14-760. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1535. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1535. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.105 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Register

14.1.5.2.105.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 46Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 3 firewall.

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Table 14-1536. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 046Ch

Figure 14-761. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1537. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1537. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.106 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L Register

14.1.5.2.106.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_1.slv region 3 firewall.

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Table 14-1538. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0470h

Figure 14-762. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1539. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.107 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H Register

14.1.5.2.107.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_1.slv region 3 firewall.

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Table 14-1540. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0474h

Figure 14-763. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1541. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.108 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L Register

14.1.5.2.108.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_1.slv region 3 firewall.

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Table 14-1542. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0478h

Figure 14-764. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1543. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.109 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H Register

14.1.5.2.109.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_1.slv region 3 firewall.

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Table 14-1544. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 047Ch

Figure 14-765. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1545. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.110 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_CONTROL Register

14.1.5.2.110.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_CONTROL Register (Offset = 480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Imsram32kx256e_main_1.slv region 4 firewall.

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Table 14-1546. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0480h

Figure 14-766. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1547. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.111 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_0 Register

14.1.5.2.111.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 4 firewall.

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Table 14-1548. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0484h

Figure 14-767. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1549. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1549. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.112 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_1 Register

14.1.5.2.112.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 4 firewall.

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Table 14-1550. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0488h

Figure 14-768. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1551. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1551. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.113 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_2 Register

14.1.5.2.113.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 48Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 4 firewall.

Return to Summary Table

Table 14-1552. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 048Ch

Figure 14-769. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1553. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1553. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.114 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_L Register

14.1.5.2.114.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_1.slv region 4 firewall.

Return to Summary Table

Table 14-1554. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0490h

Figure 14-770. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1555. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.115 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_H Register

14.1.5.2.115.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_1.slv region 4 firewall.

Return to Summary Table

Table 14-1556. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0494h

Figure 14-771. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1557. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.116 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_L Register

14.1.5.2.116.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_1.slv region 4 firewall.

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Table 14-1558. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0498h

Figure 14-772. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1559. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.117 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_H Register

14.1.5.2.117.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 49Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_1.slv region 4 firewall.

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Table 14-1560. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 049Ch

Figure 14-773. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1561. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.118 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_CONTROL Register

14.1.5.2.118.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_CONTROL Register (Offset = 4A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Imsram32kx256e_main_1.slv region 5 firewall.

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Table 14-1562. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04A0h

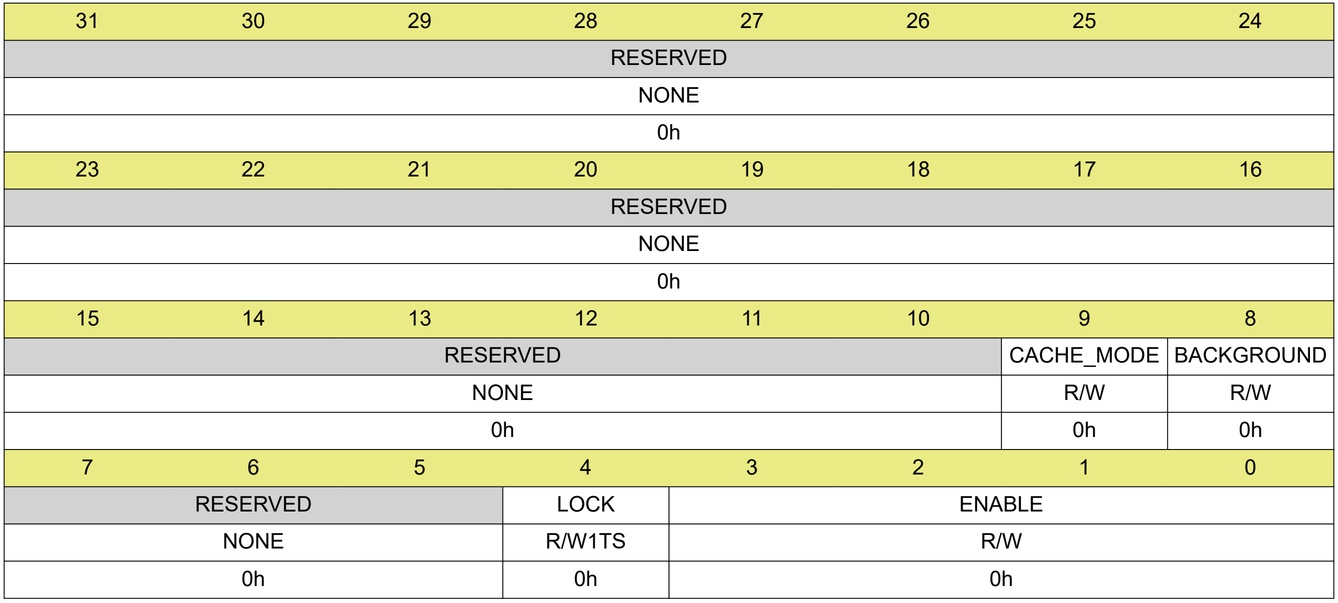

Figure 14-774. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1563. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.119 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_0 Register

14.1.5.2.119.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 4A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 5 firewall.

Return to Summary Table

Table 14-1564. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04A4h

Figure 14-775. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1565. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1565. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.120 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_1 Register

14.1.5.2.120.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 4A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 5 firewall.

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Table 14-1566. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04A8h

Figure 14-776. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1567. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1567. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.121 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_2 Register

14.1.5.2.121.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 4ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 5 firewall.

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Table 14-1568. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04ACh

Figure 14-777. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1569. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1569. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.122 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_L Register

14.1.5.2.122.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 4B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_1.slv region 5 firewall.

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Table 14-1570. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04B0h

Figure 14-778. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1571. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.123 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_H Register

14.1.5.2.123.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 4B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_1.slv region 5 firewall.

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Table 14-1572. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04B4h

Figure 14-779. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1573. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.124 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_L Register

14.1.5.2.124.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 4B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_1.slv region 5 firewall.

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Table 14-1574. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04B8h

Figure 14-780. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1575. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.125 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_H Register

14.1.5.2.125.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 4BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_1.slv region 5 firewall.

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Table 14-1576. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04BCh

Figure 14-781. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1577. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.126 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_CONTROL Register

14.1.5.2.126.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_CONTROL Register (Offset = 4C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Imsram32kx256e_main_1.slv region 6 firewall.

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Table 14-1578. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04C0h

Figure 14-782. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1579. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.127 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_0 Register

14.1.5.2.127.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 4C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 6 firewall.

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Table 14-1580. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04C4h

Figure 14-783. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1581. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1581. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.128 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_1 Register

14.1.5.2.128.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 4C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 6 firewall.

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Table 14-1582. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04C8h

Figure 14-784. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1583. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1583. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.129 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_2 Register

14.1.5.2.129.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 4CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 6 firewall.

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Table 14-1584. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04CCh

Figure 14-785. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1585. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1585. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.130 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_L Register

14.1.5.2.130.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 4D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_1.slv region 6 firewall.

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Table 14-1586. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04D0h

Figure 14-786. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1587. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.131 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_H Register

14.1.5.2.131.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 4D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_1.slv region 6 firewall.

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Table 14-1588. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04D4h

Figure 14-787. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1589. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.132 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_L Register

14.1.5.2.132.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 4D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_1.slv region 6 firewall.

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Table 14-1590. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04D8h

Figure 14-788. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1591. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.133 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_H Register

14.1.5.2.133.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 4DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_1.slv region 6 firewall.

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Table 14-1592. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04DCh

Figure 14-789. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1593. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.134 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_CONTROL Register

14.1.5.2.134.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_CONTROL Register (Offset = 4E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Imsram32kx256e_main_1.slv region 7 firewall.

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Table 14-1594. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04E0h

Figure 14-790. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h

7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1595. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.135 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_0 Register

14.1.5.2.135.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 4E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 7 firewall.

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Table 14-1596. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04E4h

Figure 14-791. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1597. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1597. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.136 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_1 Register

14.1.5.2.136.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 4E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 7 firewall.

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Table 14-1598. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04E8h

Figure 14-792. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1599. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1599. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.137 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_2 Register

14.1.5.2.137.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 4ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_1.slv region 7 firewall.

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Table 14-1600. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04ECh

Figure 14-793. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1601. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1601. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.138 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_L Register

14.1.5.2.138.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 4F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_1.slv region 7 firewall.

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Table 14-1602. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04F0h

Figure 14-794. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1603. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.139 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_H Register

14.1.5.2.139.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 4F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_1.slv region 7 firewall.

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Table 14-1604. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04F4h

Figure 14-795. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1605. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.140 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_L Register

14.1.5.2.140.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 4F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_1.slv region 7 firewall.

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Table 14-1606. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04F8h

Figure 14-796. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1607. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.141 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_H Register

14.1.5.2.141.1 CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 4FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_1.slv region 7 firewall.

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Table 14-1608. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 04FCh

Figure 14-797. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-1609. CBASS_FW_IMSRAM32KX256E_MAIN_1_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.142 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_CONTROL Register

14.1.5.2.142.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_CONTROL Register (Offset = 800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imsram32kx256e_main_2.slv region 0 firewall.

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Table 14-1610. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0800h

Figure 14-798. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1611. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.143 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.5.2.143.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 0 firewall.

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Table 14-1612. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0804h

Figure 14-799. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1613. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1613. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.144 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.5.2.144.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 0 firewall.

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Table 14-1614. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0808h

Figure 14-800. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1615. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1615. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.145 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.5.2.145.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 80Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 0 firewall.

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Table 14-1616. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 080Ch

Figure 14-801. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1617. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1617. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.146 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.5.2.146.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 72200000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_2.slv region 0 firewall.

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Table 14-1618. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0810h

Figure 14-802. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
72200h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
72200h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
72200h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1619. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	72200h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.147 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.5.2.147.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_2.slv region 0 firewall.

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Table 14-1620. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0814h

Figure 14-803. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1621. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.148 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.5.2.148.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = 722FFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_2.slv region 0 firewall.

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Table 14-1622. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0818h

Figure 14-804. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">722FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">722FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">722FFh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1623. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	722FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.149 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.5.2.149.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_2.slv region 0 firewall.

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Table 14-1624. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 081Ch

Figure 14-805. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1625. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.150 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_CONTROL Register

14.1.5.2.150.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_CONTROL Register (Offset = 820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Imsram32kx256e_main_2.slv region 1 firewall.

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Table 14-1626. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0820h

Figure 14-806. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1627. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.151 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Register

14.1.5.2.151.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 1 firewall.

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Table 14-1628. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0824h

Figure 14-807. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1629. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1629. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.152 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Register

14.1.5.2.152.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 1 firewall.

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Table 14-1630. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0828h

Figure 14-808. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1631. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1631. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.153 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Register

14.1.5.2.153.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 82Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 1 firewall.

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Table 14-1632. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 082Ch

Figure 14-809. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1633. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1633. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.154 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L Register

14.1.5.2.154.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_2.slv region 1 firewall.

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Table 14-1634. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0830h

Figure 14-810. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1635. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.155 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H Register

14.1.5.2.155.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_2.slv region 1 firewall.

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Table 14-1636. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0834h

Figure 14-811. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1637. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.156 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L Register

14.1.5.2.156.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_2.slv region 1 firewall.

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Table 14-1638. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0838h

Figure 14-812. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1639. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.157 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H Register

14.1.5.2.157.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_2.slv region 1 firewall.

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Table 14-1640. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 083Ch

Figure 14-813. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1641. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.158 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_CONTROL Register

14.1.5.2.158.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_CONTROL Register (Offset = 840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Imsram32kx256e_main_2.slv region 2 firewall.

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Table 14-1642. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0840h

Figure 14-814. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1643. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.159 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Register

14.1.5.2.159.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 2 firewall.

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Table 14-1644. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0844h

Figure 14-815. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1645. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1645. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.160 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Register

14.1.5.2.160.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 2 firewall.

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Table 14-1646. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0848h

Figure 14-816. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1647. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1647. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.161 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Register

14.1.5.2.161.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 84Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 2 firewall.

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Table 14-1648. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 084Ch

Figure 14-817. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1649. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1649. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.162 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L Register

14.1.5.2.162.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_2.slv region 2 firewall.

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Table 14-1650. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0850h

Figure 14-818. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1651. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.163 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H Register

14.1.5.2.163.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_2.slv region 2 firewall.

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Table 14-1652. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0854h

Figure 14-819. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1653. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.164 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L Register

14.1.5.2.164.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_2.slv region 2 firewall.

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Table 14-1654. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0858h

Figure 14-820. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1655. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.165 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H Register

14.1.5.2.165.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_2.slv region 2 firewall.

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Table 14-1656. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 085Ch

Figure 14-821. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1657. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.166 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_CONTROL Register

14.1.5.2.166.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_CONTROL Register (Offset = 860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Imsram32kx256e_main_2.slv region 3 firewall.

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Table 14-1658. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0860h

Figure 14-822. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1659. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.167 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Register

14.1.5.2.167.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 3 firewall.

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Table 14-1660. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0864h

Figure 14-823. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1661. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1661. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.168 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Register

14.1.5.2.168.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 3 firewall.

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Table 14-1662. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0868h

Figure 14-824. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1663. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1663. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.169 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Register

14.1.5.2.169.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 86Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 3 firewall.

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Table 14-1664. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 086Ch

Figure 14-825. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1665. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1665. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.170 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L Register

14.1.5.2.170.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_2.slv region 3 firewall.

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Table 14-1666. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0870h

Figure 14-826. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1667. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.171 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H Register

14.1.5.2.171.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_2.slv region 3 firewall.

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Table 14-1668. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0874h

Figure 14-827. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1669. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.172 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L Register

14.1.5.2.172.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_2.slv region 3 firewall.

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Table 14-1670. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0878h

Figure 14-828. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1671. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.173 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H Register

14.1.5.2.173.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_2.slv region 3 firewall.

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Table 14-1672. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 087Ch

Figure 14-829. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1673. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.174 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_CONTROL Register

14.1.5.2.174.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_CONTROL Register (Offset = 880h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Imsram32kx256e_main_2.slv region 4 firewall.

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Table 14-1674. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0880h

Figure 14-830. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1675. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.175 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_0 Register

14.1.5.2.175.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 884h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 4 firewall.

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Table 14-1676. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0884h

Figure 14-831. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1677. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1677. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.176 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_1 Register

14.1.5.2.176.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 888h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 4 firewall.

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Table 14-1678. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0888h

Figure 14-832. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1679. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1679. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.177 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_2 Register

14.1.5.2.177.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 88Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 4 firewall.

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Table 14-1680. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 088Ch

Figure 14-833. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1681. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1681. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.178 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_L Register

14.1.5.2.178.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 890h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_2.slv region 4 firewall.

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Table 14-1682. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0890h

Figure 14-834. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1683. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.179 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_H Register

14.1.5.2.179.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 894h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_2.slv region 4 firewall.

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Table 14-1684. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0894h

Figure 14-835. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1685. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.180 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_L Register

14.1.5.2.180.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 898h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_2.slv region 4 firewall.

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Table 14-1686. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0898h

Figure 14-836. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1687. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.181 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_H Register

14.1.5.2.181.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 89Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_2.slv region 4 firewall.

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Table 14-1688. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 089Ch

Figure 14-837. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1689. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.182 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_CONTROL Register

14.1.5.2.182.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_CONTROL Register (Offset = 8A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Imsram32kx256e_main_2.slv region 5 firewall.

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Table 14-1690. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08A0h

Figure 14-838. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1691. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.183 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_0 Register

14.1.5.2.183.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 8A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 5 firewall.

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Table 14-1692. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08A4h

Figure 14-839. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1693. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1693. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.184 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_1 Register

14.1.5.2.184.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 8A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 5 firewall.

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Table 14-1694. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08A8h

Figure 14-840. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1695. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1695. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.185 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_2 Register

14.1.5.2.185.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 8ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 5 firewall.

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Table 14-1696. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08ACh

Figure 14-841. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1697. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1697. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.186 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_L Register

14.1.5.2.186.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 8B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_2.slv region 5 firewall.

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Table 14-1698. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08B0h

Figure 14-842. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1699. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.187 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_H Register

14.1.5.2.187.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 8B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_2.slv region 5 firewall.

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Table 14-1700. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08B4h

Figure 14-843. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-1701. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.188 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_L Register

14.1.5.2.188.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 8B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_2.slv region 5 firewall.

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Table 14-1702. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08B8h

Figure 14-844. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1703. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.189 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_H Register

14.1.5.2.189.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 8BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_2.slv region 5 firewall.

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Table 14-1704. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08BCh

Figure 14-845. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1705. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.190 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_CONTROL Register

14.1.5.2.190.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_CONTROL Register (Offset = 8C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Imsram32kx256e_main_2.slv region 6 firewall.

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Table 14-1706. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08C0h

Figure 14-846. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1707. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.191 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_0 Register

14.1.5.2.191.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 8C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 6 firewall.

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Table 14-1708. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08C4h

Figure 14-847. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1709. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1709. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.192 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_1 Register

14.1.5.2.192.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 8C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 6 firewall.

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Table 14-1710. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08C8h

Figure 14-848. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1711. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1711. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.193 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_2 Register

14.1.5.2.193.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 8CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 6 firewall.

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Table 14-1712. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08CCh

Figure 14-849. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1713. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1713. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.194 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_L Register

14.1.5.2.194.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 8D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_2.slv region 6 firewall.

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Table 14-1714. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08D0h

Figure 14-850. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1715. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.195 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_H Register

14.1.5.2.195.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 8D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_2.slv region 6 firewall.

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Table 14-1716. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08D4h

Figure 14-851. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1717. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.196 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_L Register

14.1.5.2.196.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 8D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_2.slv region 6 firewall.

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Table 14-1718. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08D8h

Figure 14-852. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1719. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.197 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_H Register

14.1.5.2.197.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 8DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_2.slv region 6 firewall.

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Table 14-1720. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08DCh

Figure 14-853. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1721. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.198 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_CONTROL Register

14.1.5.2.198.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_CONTROL Register (Offset = 8E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Imsram32kx256e_main_2.slv region 7 firewall.

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Table 14-1722. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08E0h

Figure 14-854. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1723. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.199 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_0 Register

14.1.5.2.199.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 8E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 7 firewall.

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Table 14-1724. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08E4h

Figure 14-855. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1725. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1725. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.200 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_1 Register

14.1.5.2.200.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 8E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 7 firewall.

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Table 14-1726. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08E8h

Figure 14-856. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1727. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1727. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.201 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_2 Register

14.1.5.2.201.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 8ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_2.slv region 7 firewall.

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Table 14-1728. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08ECh

Figure 14-857. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1729. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1729. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.202 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_L Register

14.1.5.2.202.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 8F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_2.slv region 7 firewall.

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Table 14-1730. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08F0h

Figure 14-858. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1731. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.203 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_H Register

14.1.5.2.203.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 8F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_2.slv region 7 firewall.

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Table 14-1732. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08F4h

Figure 14-859. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1733. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.204 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_L Register

14.1.5.2.204.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 8F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_2.slv region 7 firewall.

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Table 14-1734. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08F8h

Figure 14-860. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1735. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.205 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_H Register

14.1.5.2.205.1 CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 8FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_2.slv region 7 firewall.

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Table 14-1736. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 08FCh

Figure 14-861. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1737. CBASS_FW_IMSRAM32KX256E_MAIN_2_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.206 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_CONTROL Register

14.1.5.2.206.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_CONTROL Register (Offset = C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imsram32kx256e_main_3.slv region 0 firewall.

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Table 14-1738. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C00h

Figure 14-862. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1739. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.207 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.5.2.207.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 0 firewall.

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Table 14-1740. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C04h

Figure 14-863. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1741. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1741. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.208 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.5.2.208.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 0 firewall.

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Table 14-1742. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C08h

Figure 14-864. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1743. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1743. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.209 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.5.2.209.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 0 firewall.

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Table 14-1744. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C0Ch

Figure 14-865. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1745. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1745. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.210 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.5.2.210.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 72300000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_3.slv region 0 firewall.

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Table 14-1746. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C10h

Figure 14-866. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
72300h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
72300h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
72300h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1747. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	72300h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.211 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.5.2.211.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_3.slv region 0 firewall.

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Table 14-1748. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C14h

Figure 14-867. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1749. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.212 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.5.2.212.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = 723FFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_3.slv region 0 firewall.

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Table 14-1750. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C18h

Figure 14-868. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
723FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
723FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
723FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1751. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	723FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.213 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.5.2.213.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_3.slv region 0 firewall.

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Table 14-1752. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C1Ch

Figure 14-869. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1753. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.214 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_CONTROL Register

14.1.5.2.214.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_CONTROL Register (Offset = C20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Imsram32kx256e_main_3.slv region 1 firewall.

Return to Summary Table

Table 14-1754. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C20h

Figure 14-870. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1755. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.215 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Register

14.1.5.2.215.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = C24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 1 firewall.

Return to Summary Table

Table 14-1756. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C24h

Figure 14-871. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1757. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1757. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.216 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Register

14.1.5.2.216.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = C28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 1 firewall.

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Table 14-1758. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C28h

Figure 14-872. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1759. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1759. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.217 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Register

14.1.5.2.217.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = C2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 1 firewall.

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Table 14-1760. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C2Ch

Figure 14-873. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1761. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1761. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.218 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L Register

14.1.5.2.218.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = C30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_3.slv region 1 firewall.

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Table 14-1762. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C30h

Figure 14-874. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1763. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.219 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H Register

14.1.5.2.219.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = C34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_3.slv region 1 firewall.

Return to Summary Table

Table 14-1764. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C34h

Figure 14-875. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1765. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.220 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L Register

14.1.5.2.220.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = C38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_3.slv region 1 firewall.

Return to Summary Table

Table 14-1766. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C38h

Figure 14-876. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1767. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.221 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H Register

14.1.5.2.221.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = C3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_3.slv region 1 firewall.

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Table 14-1768. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C3Ch

Figure 14-877. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1769. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.222 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_CONTROL Register

14.1.5.2.222.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_CONTROL Register (Offset = C40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Imsram32kx256e_main_3.slv region 2 firewall.

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Table 14-1770. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C40h

Figure 14-878. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1771. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.223 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Register

14.1.5.2.223.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = C44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 2 firewall.

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Table 14-1772. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C44h

Figure 14-879. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1773. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1773. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.224 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Register

14.1.5.2.224.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = C48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 2 firewall.

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Table 14-1774. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C48h

Figure 14-880. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1775. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1775. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.225 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Register

14.1.5.2.225.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = C4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 2 firewall.

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Table 14-1776. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C4Ch

Figure 14-881. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1777. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1777. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.226 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L Register

14.1.5.2.226.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = C50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_3.slv region 2 firewall.

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Table 14-1778. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C50h

Figure 14-882. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1779. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.227 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H Register

14.1.5.2.227.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = C54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_3.slv region 2 firewall.

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Table 14-1780. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C54h

Figure 14-883. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1781. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.228 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L Register

14.1.5.2.228.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = C58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_3.slv region 2 firewall.

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Table 14-1782. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C58h

Figure 14-884. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1783. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.229 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H Register

14.1.5.2.229.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = C5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_3.slv region 2 firewall.

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Table 14-1784. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C5Ch

Figure 14-885. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1785. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.230 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_CONTROL Register

14.1.5.2.230.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_CONTROL Register (Offset = C60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Imsram32kx256e_main_3.slv region 3 firewall.

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Table 14-1786. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C60h

Figure 14-886. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1787. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.231 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Register

14.1.5.2.231.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = C64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 3 firewall.

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Table 14-1788. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C64h

Figure 14-887. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1789. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1789. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.232 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Register

14.1.5.2.232.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = C68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 3 firewall.

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Table 14-1790. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C68h

Figure 14-888. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1791. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1791. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.233 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Register

14.1.5.2.233.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = C6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 3 firewall.

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Table 14-1792. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C6Ch

Figure 14-889. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1793. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1793. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.234 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L Register

14.1.5.2.234.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = C70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_3.slv region 3 firewall.

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Table 14-1794. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C70h

Figure 14-890. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1795. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.235 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H Register

14.1.5.2.235.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = C74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_3.slv region 3 firewall.

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Table 14-1796. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C74h

Figure 14-891. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1797. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.236 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L Register

14.1.5.2.236.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = C78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_3.slv region 3 firewall.

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Table 14-1798. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C78h

Figure 14-892. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1799. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.237 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H Register

14.1.5.2.237.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = C7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_3.slv region 3 firewall.

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Table 14-1800. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C7Ch

Figure 14-893. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1801. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.238 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_CONTROL Register

14.1.5.2.238.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_CONTROL Register (Offset = C80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Imsram32kx256e_main_3.slv region 4 firewall.

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Table 14-1802. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C80h

Figure 14-894. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1803. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.239 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_0 Register

14.1.5.2.239.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = C84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 4 firewall.

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Table 14-1804. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C84h

Figure 14-895. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1805. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1805. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.240 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_1 Register

14.1.5.2.240.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = C88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 4 firewall.

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Table 14-1806. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C88h

Figure 14-896. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1807. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1807. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.241 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_2 Register

14.1.5.2.241.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = C8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 4 firewall.

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Table 14-1808. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C8Ch

Figure 14-897. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1809. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1809. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.242 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_L Register

14.1.5.2.242.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = C90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_3.slv region 4 firewall.

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Table 14-1810. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C90h

Figure 14-898. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1811. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.243 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_H Register

14.1.5.2.243.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = C94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_3.slv region 4 firewall.

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Table 14-1812. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C94h

Figure 14-899. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1813. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.244 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_L Register

14.1.5.2.244.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = C98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_3.slv region 4 firewall.

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Table 14-1814. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C98h

Figure 14-900. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1815. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.245 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_H Register

14.1.5.2.245.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = C9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_3.slv region 4 firewall.

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Table 14-1816. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0C9Ch

Figure 14-901. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1817. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.246 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_CONTROL Register

14.1.5.2.246.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_CONTROL Register (Offset = CA0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Imsram32kx256e_main_3.slv region 5 firewall.

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Table 14-1818. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CA0h

Figure 14-902. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1819. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.247 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_0 Register

14.1.5.2.247.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = CA4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 5 firewall.

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Table 14-1820. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CA4h

Figure 14-903. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1821. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1821. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.248 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_1 Register

14.1.5.2.248.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = CA8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 5 firewall.

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Table 14-1822. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CA8h

Figure 14-904. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1823. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1823. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.249 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_2 Register

14.1.5.2.249.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = CACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 5 firewall.

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Table 14-1824. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CACh

Figure 14-905. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1825. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1825. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.250 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_L Register

14.1.5.2.250.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = CB0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_3.slv region 5 firewall.

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Table 14-1826. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CB0h

Figure 14-906. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1827. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.251 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_H Register

14.1.5.2.251.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = CB4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_3.slv region 5 firewall.

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Table 14-1828. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CB4h

Figure 14-907. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1829. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.252 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_L Register

14.1.5.2.252.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = CB8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_3.slv region 5 firewall.

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Table 14-1830. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CB8h

Figure 14-908. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1831. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.253 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_H Register

14.1.5.2.253.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = CBCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_3.slv region 5 firewall.

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Table 14-1832. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CBCh

Figure 14-909. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1833. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.254 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_CONTROL Register

14.1.5.2.254.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_CONTROL Register (Offset = CC0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Imsram32kx256e_main_3.slv region 6 firewall.

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Table 14-1834. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CC0h

Figure 14-910. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1835. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.255 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_0 Register

14.1.5.2.255.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = CC4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 6 firewall.

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Table 14-1836. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CC4h

Figure 14-911. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1837. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1837. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.256 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_1 Register

14.1.5.2.256.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = CC8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 6 firewall.

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Table 14-1838. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CC8h

Figure 14-912. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1839. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1839. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.257 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_2 Register

14.1.5.2.257.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = CCCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 6 firewall.

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Table 14-1840. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CCCh

Figure 14-913. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1841. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1841. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.258 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_L Register

14.1.5.2.258.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = CD0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_3.slv region 6 firewall.

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Table 14-1842. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CD0h

Figure 14-914. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1843. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.259 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_H Register

14.1.5.2.259.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = CD4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_3.slv region 6 firewall.

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Table 14-1844. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CD4h

Figure 14-915. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1845. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.260 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_L Register

14.1.5.2.260.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = CD8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_3.slv region 6 firewall.

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Table 14-1846. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CD8h

Figure 14-916. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1847. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.261 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_H Register

14.1.5.2.261.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = CDCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_3.slv region 6 firewall.

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Table 14-1848. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CDCh

Figure 14-917. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1849. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.262 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_CONTROL Register

14.1.5.2.262.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_CONTROL Register (Offset = CE0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Imsram32kx256e_main_3.slv region 7 firewall.

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Table 14-1850. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CE0h

Figure 14-918. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1851. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.263 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_0 Register

14.1.5.2.263.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = CE4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 7 firewall.

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Table 14-1852. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CE4h

Figure 14-919. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1853. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1853. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.264 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_1 Register

14.1.5.2.264.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = CE8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 7 firewall.

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Table 14-1854. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CE8h

Figure 14-920. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1855. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1855. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.265 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_2 Register

14.1.5.2.265.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = CECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_3.slv region 7 firewall.

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Table 14-1856. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CECh

Figure 14-921. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1857. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1857. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.266 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_L Register

14.1.5.2.266.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = CF0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_3.slv region 7 firewall.

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Table 14-1858. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CF0h

Figure 14-922. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-1859. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.267 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_H Register

14.1.5.2.267.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = CF4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_3.slv region 7 firewall.

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Table 14-1860. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CF4h

Figure 14-923. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-1861. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.268 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_L Register

14.1.5.2.268.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = CF8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_3.slv region 7 firewall.

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Table 14-1862. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CF8h

Figure 14-924. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1863. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.269 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_H Register

14.1.5.2.269.1 CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = CFCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_3.slv region 7 firewall.

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Table 14-1864. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 0CFCh

Figure 14-925. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1865. CBASS_FW_IMSRAM32KX256E_MAIN_3_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.270 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_CONTROL Register

14.1.5.2.270.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_CONTROL Register (Offset = 1000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imsram32kx256e_main_4.slv region 0 firewall.

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Table 14-1866. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1000h

Figure 14-926. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1867. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.271 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.5.2.271.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 1004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 0 firewall.

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Table 14-1868. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1004h

Figure 14-927. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1869. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1869. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.272 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.5.2.272.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 1008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 0 firewall.

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Table 14-1870. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1008h

Figure 14-928. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1871. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1871. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.273 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.5.2.273.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 100Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 0 firewall.

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Table 14-1872. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 100Ch

Figure 14-929. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1873. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1873. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.274 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.5.2.274.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 1010h) [reset = 72400000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_4.slv region 0 firewall.

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Table 14-1874. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1010h

Figure 14-930. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
72400h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
72400h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
72400h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1875. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	72400h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.275 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.5.2.275.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 1014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_4.slv region 0 firewall.

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Table 14-1876. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1014h

Figure 14-931. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1877. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.276 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.5.2.276.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 1018h) [reset = 724FFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_4.slv region 0 firewall.

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Table 14-1878. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1018h

Figure 14-932. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
724FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
724FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
724FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1879. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	724FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.277 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.5.2.277.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 101Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_4.slv region 0 firewall.

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Table 14-1880. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 101Ch

Figure 14-933. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1881. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.278 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_CONTROL Register

14.1.5.2.278.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_CONTROL Register (Offset = 1020h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Imsram32kx256e_main_4.slv region 1 firewall.

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Table 14-1882. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1020h

Figure 14-934. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1883. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.279 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Register

14.1.5.2.279.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 1024h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 1 firewall.

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Table 14-1884. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1024h

Figure 14-935. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1885. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1885. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.280 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Register

14.1.5.2.280.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 1028h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 1 firewall.

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Table 14-1886. Instance Table

Instance Name	**Physical Address**
CBASS_MEM0	4504 1028h

Figure 14-936. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1887. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1887. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.281 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Register

14.1.5.2.281.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 102Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 1 firewall.

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Table 14-1888. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 102Ch

Figure 14-937. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1889. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1889. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.282 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L Register

14.1.5.2.282.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 1030h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_4.slv region 1 firewall.

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Table 14-1890. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1030h

Figure 14-938. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1891. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.283 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H Register

14.1.5.2.283.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 1034h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_4.slv region 1 firewall.

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Table 14-1892. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1034h

Figure 14-939. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1893. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.284 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L Register

14.1.5.2.284.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 1038h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_4.slv region 1 firewall.

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Table 14-1894. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1038h

Figure 14-940. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1895. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.285 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H Register

14.1.5.2.285.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 103Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_4.slv region 1 firewall.

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Table 14-1896. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 103Ch

Figure 14-941. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-1897. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.286 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_CONTROL Register

14.1.5.2.286.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_CONTROL Register (Offset = 1040h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Imsram32kx256e_main_4.slv region 2 firewall.

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Table 14-1898. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1040h

Figure 14-942. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1899. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.287 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Register

14.1.5.2.287.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 1044h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 2 firewall.

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Table 14-1900. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1044h

Figure 14-943. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1901. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1901. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.288 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Register

14.1.5.2.288.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 1048h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 2 firewall.

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Table 14-1902. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1048h

Figure 14-944. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1903. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1903. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.289 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Register

14.1.5.2.289.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 104Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 2 firewall.

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Table 14-1904. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 104Ch

Figure 14-945. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1905. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1905. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.290 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L Register

14.1.5.2.290.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 1050h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_4.slv region 2 firewall.

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Table 14-1906. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1050h

Figure 14-946. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1907. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.291 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H Register

14.1.5.2.291.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 1054h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_4.slv region 2 firewall.

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Table 14-1908. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1054h

Figure 14-947. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1909. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.292 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L Register

14.1.5.2.292.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 1058h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_4.slv region 2 firewall.

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Table 14-1910. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1058h

Figure 14-948. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1911. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.293 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H Register

14.1.5.2.293.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 105Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_4.slv region 2 firewall.

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Table 14-1912. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 105Ch

Figure 14-949. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1913. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.294 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_CONTROL Register

14.1.5.2.294.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_CONTROL Register (Offset = 1060h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Imsram32kx256e_main_4.slv region 3 firewall.

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Table 14-1914. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1060h

Figure 14-950. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1915. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.295 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Register

14.1.5.2.295.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 1064h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 3 firewall.

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Table 14-1916. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1064h

Figure 14-951. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1917. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1917. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.296 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Register

14.1.5.2.296.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 1068h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 3 firewall.

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Table 14-1918. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1068h

Figure 14-952. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1919. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1919. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.297 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Register

14.1.5.2.297.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 106Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 3 firewall.

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Table 14-1920. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 106Ch

Figure 14-953. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1921. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1921. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.298 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L Register

14.1.5.2.298.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 1070h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_4.slv region 3 firewall.

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Table 14-1922. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1070h

Figure 14-954. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1923. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.299 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H Register

14.1.5.2.299.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 1074h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_4.slv region 3 firewall.

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Table 14-1924. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1074h

Figure 14-955. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1925. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.300 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L Register

14.1.5.2.300.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 1078h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_4.slv region 3 firewall.

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Table 14-1926. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1078h

Figure 14-956. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-1927. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.301 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H Register

14.1.5.2.301.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 107Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_4.slv region 3 firewall.

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Table 14-1928. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 107Ch

Figure 14-957. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1929. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.302 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_CONTROL Register

14.1.5.2.302.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_CONTROL Register (Offset = 1080h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Imsram32kx256e_main_4.slv region 4 firewall.

Return to Summary Table

Table 14-1930. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1080h

Figure 14-958. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1931. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.303 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_0 Register

14.1.5.2.303.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 1084h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 4 firewall.

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Table 14-1932. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1084h

Figure 14-959. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1933. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1933. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.304 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_1 Register

14.1.5.2.304.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 1088h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 4 firewall.

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Table 14-1934. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1088h

Figure 14-960. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1935. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1935. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.305 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_2 Register

14.1.5.2.305.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 108Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 4 firewall.

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Table 14-1936. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 108Ch

Figure 14-961. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1937. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1937. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.306 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_L Register

14.1.5.2.306.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 1090h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_4.slv region 4 firewall.

Return to Summary Table

Table 14-1938. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1090h

Figure 14-962. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-1939. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.307 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_H Register

14.1.5.2.307.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 1094h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_4.slv region 4 firewall.

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Table 14-1940. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1094h

Figure 14-963. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1941. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.308 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_L Register

14.1.5.2.308.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 1098h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_4.slv region 4 firewall.

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Table 14-1942. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1098h

Figure 14-964. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1943. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.309 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_H Register

14.1.5.2.309.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 109Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_4.slv region 4 firewall.

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Table 14-1944. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 109Ch

Figure 14-965. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1945. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.310 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_CONTROL Register

14.1.5.2.310.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_CONTROL Register (Offset = 10A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Imsram32kx256e_main_4.slv region 5 firewall.

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Table 14-1946. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10A0h

Figure 14-966. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1947. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.311 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_0 Register

14.1.5.2.311.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 10A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 5 firewall.

Return to Summary Table

Table 14-1948. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10A4h

Figure 14-967. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-1949. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1949. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.312 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_1 Register

14.1.5.2.312.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 10A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 5 firewall.

Return to Summary Table

Table 14-1950. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10A8h

Figure 14-968. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1951. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1951. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.313 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_2 Register

14.1.5.2.313.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 10ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 5 firewall.

Return to Summary Table

Table 14-1952. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10ACh

Figure 14-969. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1953. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1953. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.314 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_L Register

14.1.5.2.314.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 10B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_4.slv region 5 firewall.

Return to Summary Table

Table 14-1954. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10B0h

Figure 14-970. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1955. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.315 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_H Register

14.1.5.2.315.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 10B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_4.slv region 5 firewall.

Return to Summary Table

Table 14-1956. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10B4h

Figure 14-971. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1957. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.316 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_L Register

14.1.5.2.316.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 10B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_4.slv region 5 firewall.

Return to Summary Table

Table 14-1958. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10B8h

Figure 14-972. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1959. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.317 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_H Register

14.1.5.2.317.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 10BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_4.slv region 5 firewall.

Return to Summary Table

Table 14-1960. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10BCh

Figure 14-973. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1961. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.318 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_CONTROL Register

14.1.5.2.318.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_CONTROL Register (Offset = 10C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Imsram32kx256e_main_4.slv region 6 firewall.

Return to Summary Table

Table 14-1962. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10C0h

Figure 14-974. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1963. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.319 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_0 Register

14.1.5.2.319.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 10C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 6 firewall.

Return to Summary Table

Table 14-1964. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10C4h

Figure 14-975. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1965. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1965. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.320 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_1 Register

14.1.5.2.320.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 10C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 6 firewall.

Return to Summary Table

Table 14-1966. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10C8h

Figure 14-976. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1967. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1967. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.321 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_2 Register

14.1.5.2.321.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 10CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 6 firewall.

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Table 14-1968. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10CCh

Figure 14-977. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1969. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1969. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.322 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_L Register

14.1.5.2.322.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 10D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_4.slv region 6 firewall.

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Table 14-1970. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10D0h

Figure 14-978. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1971. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.323 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_H Register

14.1.5.2.323.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 10D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_4.slv region 6 firewall.

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Table 14-1972. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10D4h

Figure 14-979. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1973. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.324 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_L Register

14.1.5.2.324.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 10D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_4.slv region 6 firewall.

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Table 14-1974. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10D8h

Figure 14-980. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1975. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.325 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_H Register

14.1.5.2.325.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 10DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_4.slv region 6 firewall.

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Table 14-1976. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10DCh

Figure 14-981. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1977. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.326 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_CONTROL Register

14.1.5.2.326.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_CONTROL Register (Offset = 10E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Imsram32kx256e_main_4.slv region 7 firewall.

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Table 14-1978. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10E0h

Figure 14-982. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-1979. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.327 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_0 Register

14.1.5.2.327.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 10E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 7 firewall.

Return to Summary Table

Table 14-1980. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10E4h

Figure 14-983. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1981. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1981. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.328 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_1 Register

14.1.5.2.328.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 10E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 7 firewall.

Return to Summary Table

Table 14-1982. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10E8h

Figure 14-984. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1983. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1983. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.329 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_2 Register

14.1.5.2.329.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 10ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_4.slv region 7 firewall.

Return to Summary Table

Table 14-1984. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10ECh

Figure 14-985. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1985. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1985. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.330 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_L Register

14.1.5.2.330.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 10F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_4.slv region 7 firewall.

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Table 14-1986. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10F0h

Figure 14-986. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-1987. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.331 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_H Register

14.1.5.2.331.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 10F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_4.slv region 7 firewall.

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Table 14-1988. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10F4h

Figure 14-987. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-1989. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.332 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_L Register

14.1.5.2.332.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 10F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_4.slv region 7 firewall.

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Table 14-1990. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10F8h

Figure 14-988. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-1991. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.333 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_H Register

14.1.5.2.333.1 CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 10FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_4.slv region 7 firewall.

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Table 14-1992. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 10FCh

Figure 14-989. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-1993. CBASS_FW_IMSRAM32KX256E_MAIN_4_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.334 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_CONTROL Register

14.1.5.2.334.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_CONTROL Register (Offset = 1400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imsram32kx256e_main_5.slv region 0 firewall.

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Table 14-1994. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1400h

Figure 14-990. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-1995. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.335 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.5.2.335.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 1404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 0 firewall.

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Table 14-1996. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1404h

Figure 14-991. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1997. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1997. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.336 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.5.2.336.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 1408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 0 firewall.

Return to Summary Table

Table 14-1998. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1408h

Figure 14-992. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-1999. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-1999. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.337 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.5.2.337.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 140Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 0 firewall.

Return to Summary Table

Table 14-2000. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 140Ch

Figure 14-993. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2001. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2001. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.338 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.5.2.338.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 1410h) [reset = 72500000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_5.slv region 0 firewall.

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Table 14-2002. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1410h

Figure 14-994. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">72500h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">72500h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">72500h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2003. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	72500h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.339 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.5.2.339.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 1414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_5.slv region 0 firewall.

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Table 14-2004. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1414h

Figure 14-995. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2005. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.340 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.5.2.340.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 1418h) [reset = 725FFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_5.slv region 0 firewall.

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Table 14-2006. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1418h

Figure 14-996. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
725FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
725FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
725FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2007. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	725FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.341 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.5.2.341.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 141Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_5.slv region 0 firewall.

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Table 14-2008. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 141Ch

Figure 14-997. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2009. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.342 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_CONTROL Register

14.1.5.2.342.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_CONTROL Register (Offset = 1420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Imsram32kx256e_main_5.slv region 1 firewall.

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Table 14-2010. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1420h

Figure 14-998. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2011. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.343 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Register

14.1.5.2.343.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Register (Offset = 1424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 1 firewall.

Return to Summary Table

Table 14-2012. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1424h

Figure 14-999. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2013. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2013. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.344 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Register

14.1.5.2.344.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Register (Offset = 1428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 1 firewall.

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Table 14-2014. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1428h

Figure 14-1000. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2015. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2015. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.345 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Register

14.1.5.2.345.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Register (Offset = 142Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 1 firewall.

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Table 14-2016. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 142Ch

Figure 14-1001. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2017. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2017. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.346 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L Register

14.1.5.2.346.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L Register (Offset = 1430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_5.slv region 1 firewall.

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Table 14-2018. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1430h

Figure 14-1002. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2019. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.347 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H Register

14.1.5.2.347.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H Register (Offset = 1434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_5.slv region 1 firewall.

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Table 14-2020. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1434h

Figure 14-1003. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2021. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.348 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L Register

14.1.5.2.348.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L Register (Offset = 1438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_5.slv region 1 firewall.

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Table 14-2022. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1438h

Figure 14-1004. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2023. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.349 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H Register

14.1.5.2.349.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H Register (Offset = 143Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_5.slv region 1 firewall.

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Table 14-2024. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 143Ch

Figure 14-1005. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2025. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.350 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_CONTROL Register

14.1.5.2.350.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_CONTROL Register (Offset = 1440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Imsram32kx256e_main_5.slv region 2 firewall.

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Table 14-2026. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1440h

Figure 14-1006. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2027. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.351 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Register

14.1.5.2.351.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Register (Offset = 1444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 2 firewall.

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Table 14-2028. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1444h

Figure 14-1007. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2029. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2029. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.352 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Register

14.1.5.2.352.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Register (Offset = 1448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 2 firewall.

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Table 14-2030. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1448h

Figure 14-1008. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2031. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2031. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.353 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Register

14.1.5.2.353.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Register (Offset = 144Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 2 firewall.

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Table 14-2032. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 144Ch

Figure 14-1009. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2033. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2033. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.354 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L Register

14.1.5.2.354.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L Register (Offset = 1450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_5.slv region 2 firewall.

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Table 14-2034. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1450h

Figure 14-1010. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2035. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.355 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H Register

14.1.5.2.355.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H Register (Offset = 1454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_5.slv region 2 firewall.

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Table 14-2036. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1454h

Figure 14-1011. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2037. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.356 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L Register

14.1.5.2.356.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L Register (Offset = 1458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_5.slv region 2 firewall.

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Table 14-2038. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1458h

Figure 14-1012. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2039. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.357 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H Register

14.1.5.2.357.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H Register (Offset = 145Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_5.slv region 2 firewall.

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Table 14-2040. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 145Ch

Figure 14-1013. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2041. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.358 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_CONTROL Register

14.1.5.2.358.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_CONTROL Register (Offset = 1460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Imsram32kx256e_main_5.slv region 3 firewall.

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Table 14-2042. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1460h

Figure 14-1014. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2043. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.359 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Register

14.1.5.2.359.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Register (Offset = 1464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 3 firewall.

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Table 14-2044. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1464h

Figure 14-1015. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2045. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2045. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.360 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Register

14.1.5.2.360.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Register (Offset = 1468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 3 firewall.

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Table 14-2046. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1468h

Figure 14-1016. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2047. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2047. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.361 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Register

14.1.5.2.361.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Register (Offset = 146Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 3 firewall.

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Table 14-2048. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 146Ch

Figure 14-1017. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2049. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2049. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.362 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L Register

14.1.5.2.362.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L Register (Offset = 1470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_5.slv region 3 firewall.

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Table 14-2050. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1470h

Figure 14-1018. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2051. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.363 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H Register

14.1.5.2.363.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H Register (Offset = 1474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_5.slv region 3 firewall.

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Table 14-2052. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1474h

Figure 14-1019. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2053. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.364 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L Register

14.1.5.2.364.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L Register (Offset = 1478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_5.slv region 3 firewall.

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Table 14-2054. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1478h

Figure 14-1020. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2055. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.365 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H Register

14.1.5.2.365.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H Register (Offset = 147Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_5.slv region 3 firewall.

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Table 14-2056. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 147Ch

Figure 14-1021. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2057. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.366 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_CONTROL Register

14.1.5.2.366.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_CONTROL Register (Offset = 1480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Imsram32kx256e_main_5.slv region 4 firewall.

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Table 14-2058. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1480h

Figure 14-1022. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2059. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.367 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_0 Register

14.1.5.2.367.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_0 Register (Offset = 1484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 4 firewall.

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Table 14-2060. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1484h

Figure 14-1023. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2061. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2061. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.368 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_1 Register

14.1.5.2.368.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_1 Register (Offset = 1488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 4 firewall.

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Table 14-2062. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1488h

Figure 14-1024. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2063. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2063. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.369 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_2 Register

14.1.5.2.369.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_2 Register (Offset = 148Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 4 firewall.

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Table 14-2064. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 148Ch

Figure 14-1025. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2065. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2065. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.370 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_L Register

14.1.5.2.370.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_L Register (Offset = 1490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_5.slv region 4 firewall.

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Table 14-2066. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1490h

Figure 14-1026. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2067. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.371 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_H Register

14.1.5.2.371.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_H Register (Offset = 1494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_5.slv region 4 firewall.

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Table 14-2068. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1494h

Figure 14-1027. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2069. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.372 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_L Register

14.1.5.2.372.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_L Register (Offset = 1498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_5.slv region 4 firewall.

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Table 14-2070. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1498h

Figure 14-1028. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2071. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.373 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_H Register

14.1.5.2.373.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_H Register (Offset = 149Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_5.slv region 4 firewall.

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Table 14-2072. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 149Ch

Figure 14-1029. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2073. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.374 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_CONTROL Register

14.1.5.2.374.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_CONTROL Register (Offset = 14A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Imsram32kx256e_main_5.slv region 5 firewall.

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Table 14-2074. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14A0h

Figure 14-1030. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2075. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.375 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_0 Register

14.1.5.2.375.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_0 Register (Offset = 14A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 5 firewall.

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Table 14-2076. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14A4h

Figure 14-1031. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2077. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2077. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.376 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_1 Register

14.1.5.2.376.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_1 Register (Offset = 14A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 5 firewall.

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Table 14-2078. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14A8h

Figure 14-1032. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2079. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2079. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.377 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_2 Register

14.1.5.2.377.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_2 Register (Offset = 14ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 5 firewall.

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Table 14-2080. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14ACh

Figure 14-1033. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2081. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2081. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.378 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_L Register

14.1.5.2.378.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_L Register (Offset = 14B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_5.slv region 5 firewall.

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Table 14-2082. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14B0h

Figure 14-1034. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2083. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.379 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_H Register

14.1.5.2.379.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_H Register (Offset = 14B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_5.slv region 5 firewall.

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Table 14-2084. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14B4h

Figure 14-1035. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2085. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.380 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_L Register

14.1.5.2.380.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_L Register (Offset = 14B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_5.slv region 5 firewall.

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Table 14-2086. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14B8h

Figure 14-1036. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2087. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.381 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_H Register

14.1.5.2.381.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_H Register (Offset = 14BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_5.slv region 5 firewall.

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Table 14-2088. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14BCh

Figure 14-1037. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2089. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.382 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_CONTROL Register

14.1.5.2.382.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_CONTROL Register (Offset = 14C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Imsram32kx256e_main_5.slv region 6 firewall.

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Table 14-2090. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14C0h

Figure 14-1038. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2091. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.383 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_0 Register

14.1.5.2.383.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_0 Register (Offset = 14C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 6 firewall.

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Table 14-2092. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14C4h

Figure 14-1039. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2093. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2093. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.384 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_1 Register

14.1.5.2.384.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_1 Register (Offset = 14C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 6 firewall.

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Table 14-2094. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14C8h

Figure 14-1040. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2095. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2095. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.385 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_2 Register

14.1.5.2.385.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_2 Register (Offset = 14CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 6 firewall.

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Table 14-2096. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14CCh

Figure 14-1041. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2097. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2097. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.386 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_L Register

14.1.5.2.386.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_L Register (Offset = 14D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_5.slv region 6 firewall.

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Table 14-2098. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14D0h

Figure 14-1042. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2099. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.387 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_H Register

14.1.5.2.387.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_H Register (Offset = 14D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_5.slv region 6 firewall.

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Table 14-2100. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14D4h

Figure 14-1043. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2101. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.388 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_L Register

14.1.5.2.388.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_L Register (Offset = 14D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_5.slv region 6 firewall.

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Table 14-2102. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14D8h

Figure 14-1044. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2103. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.389 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_H Register

14.1.5.2.389.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_H Register (Offset = 14DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_5.slv region 6 firewall.

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Table 14-2104. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14DCh

Figure 14-1045. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2105. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.390 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_CONTROL Register

14.1.5.2.390.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_CONTROL Register (Offset = 14E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Imsram32kx256e_main_5.slv region 7 firewall.

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Table 14-2106. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14E0h

Figure 14-1046. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2107. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.391 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_0 Register

14.1.5.2.391.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_0 Register (Offset = 14E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 7 firewall.

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Table 14-2108. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14E4h

Figure 14-1047. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2109. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2109. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.392 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_1 Register

14.1.5.2.392.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_1 Register (Offset = 14E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 7 firewall.

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Table 14-2110. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14E8h

Figure 14-1048. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2111. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2111. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.393 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_2 Register

14.1.5.2.393.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_2 Register (Offset = 14ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Imsram32kx256e_main_5.slv region 7 firewall.

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Table 14-2112. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14ECh

Figure 14-1049. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2113. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2113. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.394 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_L Register

14.1.5.2.394.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_L Register (Offset = 14F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Imsram32kx256e_main_5.slv region 7 firewall.

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Table 14-2114. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14F0h

Figure 14-1050. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2115. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.395 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_H Register

14.1.5.2.395.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_H Register (Offset = 14F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Imsram32kx256e_main_5.slv region 7 firewall.

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Table 14-2116. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14F4h

Figure 14-1051. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2117. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.396 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_L Register

14.1.5.2.396.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_L Register (Offset = 14F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Imsram32kx256e_main_5.slv region 7 firewall.

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Table 14-2118. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14F8h

Figure 14-1052. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2119. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.397 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_H Register

14.1.5.2.397.1 CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_H Register (Offset = 14FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Imsram32kx256e_main_5.slv region 7 firewall.

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Table 14-2120. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 14FCh

Figure 14-1053. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2121. CBASS_FW_IMSRAM32KX256E_MAIN_5_SLV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.398 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register

14.1.5.2.398.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register (Offset = 1800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 0 firewall.

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Table 14-2122. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1800h

Figure 14-1054. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2123. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.399 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register

14.1.5.2.399.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register (Offset = 1804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 0 firewall.

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Table 14-2124. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1804h

Figure 14-1055. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2125. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2125. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.400 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register

14.1.5.2.400.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register (Offset = 1808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 0 firewall.

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Table 14-2126. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1808h

Figure 14-1056. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2127. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2127. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.401 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register

14.1.5.2.401.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register (Offset = 180Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 0 firewall.

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Table 14-2128. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 180Ch

Figure 14-1057. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2129. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2129. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.402 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register

14.1.5.2.402.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register (Offset = 1810h) [reset = 7E000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 0 firewall.

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Table 14-2130. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1810h

Figure 14-1058. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7E000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2131. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7E000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.403 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register

14.1.5.2.403.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register (Offset = 1814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 0 firewall.

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Table 14-2132. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1814h

Figure 14-1059. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2133. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.404 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register

14.1.5.2.404.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register (Offset = 1818h) [reset = 7E1FFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 0 firewall.

Return to Summary Table

Table 14-2134. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1818h

Figure 14-1060. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7E1FFFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7E1FFFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7E1FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2135. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7E1FFFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.405 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register

14.1.5.2.405.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register (Offset = 181Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 0 firewall.

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Table 14-2136. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 181Ch

Figure 14-1061. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2137. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.406 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register

14.1.5.2.406.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register (Offset = 1820h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 1 firewall.

Return to Summary Table

Table 14-2138. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1820h

Figure 14-1062. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2139. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.407 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register

14.1.5.2.407.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register (Offset = 1824h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 1 firewall.

Return to Summary Table

Table 14-2140. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1824h

Figure 14-1063. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2141. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2141. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.408 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register

14.1.5.2.408.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register (Offset = 1828h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 1 firewall.

Return to Summary Table

Table 14-2142. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1828h

Figure 14-1064. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2143. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2143. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.409 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register

14.1.5.2.409.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register (Offset = 182Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 1 firewall.

Return to Summary Table

Table 14-2144. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 182Ch

Figure 14-1065. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2145. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2145. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.410 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register

14.1.5.2.410.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register (Offset = 1830h) [reset = 7E200000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 1 firewall.

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Table 14-2146. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1830h

Figure 14-1066. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E200h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E200h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7E200h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2147. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7E200h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.411 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register

14.1.5.2.411.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register (Offset = 1834h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 1 firewall.

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Table 14-2148. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1834h

Figure 14-1067. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2149. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.412 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register

14.1.5.2.412.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register (Offset = 1838h) [reset = 7E23FFFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 1 firewall.

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Table 14-2150. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1838h

Figure 14-1068. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E23Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E23Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7E23Fh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2151. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7E23Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.413 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register

14.1.5.2.413.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register (Offset = 183Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 1 firewall.

Return to Summary Table

Table 14-2152. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 183Ch

Figure 14-1069. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2153. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.414 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register

14.1.5.2.414.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register (Offset = 1840h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 2 firewall.

Return to Summary Table

Table 14-2154. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1840h

Figure 14-1070. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2155. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.415 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register

14.1.5.2.415.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register (Offset = 1844h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 2 firewall.

Return to Summary Table

Table 14-2156. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1844h

Figure 14-1071. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2157. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2157. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.416 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register

14.1.5.2.416.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register (Offset = 1848h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 2 firewall.

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Table 14-2158. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1848h

Figure 14-1072. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2159. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2159. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.417 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register

14.1.5.2.417.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register (Offset = 184Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 2 firewall.

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Table 14-2160. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 184Ch

Figure 14-1073. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2161. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2161. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.418 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register

14.1.5.2.418.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register (Offset = 1850h) [reset = 7C000000h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 2 firewall.

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Table 14-2162. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1850h

Figure 14-1074. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7C000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2163. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.419 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register

14.1.5.2.419.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register (Offset = 1854h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 2 firewall.

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Table 14-2164. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1854h

Figure 14-1075. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2165. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.420 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register

14.1.5.2.420.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register (Offset = 1858h) [reset = 7C01FFFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 2 firewall.

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Table 14-2166. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1858h

Figure 14-1076. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C01Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C01Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7C01Fh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2167. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C01Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.421 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register

14.1.5.2.421.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register (Offset = 185Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 2 firewall.

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Table 14-2168. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 185Ch

Figure 14-1077. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2169. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.422 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register

14.1.5.2.422.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register (Offset = 1860h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 3 firewall.

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Table 14-2170. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1860h

Figure 14-1078. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2171. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.423 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register

14.1.5.2.423.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register (Offset = 1864h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 3 firewall.

Return to Summary Table

Table 14-2172. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1864h

Figure 14-1079. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2173. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2173. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.424 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register

14.1.5.2.424.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register (Offset = 1868h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 3 firewall.

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Table 14-2174. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1868h

Figure 14-1080. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2175. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2175. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.425 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register

14.1.5.2.425.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register (Offset = 186Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 3 firewall.

Return to Summary Table

Table 14-2176. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 186Ch

Figure 14-1081. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2177. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2177. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.426 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register

14.1.5.2.426.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register (Offset = 1870h) [reset = 7C400000h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 3 firewall.

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Table 14-2178. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1870h

Figure 14-1082. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C400h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C400h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7C400h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2179. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C400h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.427 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register

14.1.5.2.427.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register (Offset = 1874h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 3 firewall.

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Table 14-2180. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1874h

Figure 14-1083. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2181. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.428 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register

14.1.5.2.428.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register (Offset = 1878h) [reset = 7C403FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 3 firewall.

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Table 14-2182. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1878h

Figure 14-1084. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C403h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7C403h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C403h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2183. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C403h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.429 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register

14.1.5.2.429.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register (Offset = 187Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 3 firewall.

Return to Summary Table

Table 14-2184. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 187Ch

Figure 14-1085. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2185. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.430 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register

14.1.5.2.430.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register (Offset = 1880h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 4 firewall.

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Table 14-2186. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1880h

Figure 14-1086. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2187. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.431 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register

14.1.5.2.431.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register (Offset = 1884h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 4 firewall.

Return to Summary Table

Table 14-2188. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1884h

Figure 14-1087. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2189. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2189. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.432 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register

14.1.5.2.432.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register (Offset = 1888h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 4 firewall.

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Table 14-2190. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1888h

Figure 14-1088. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2191. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2191. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.433 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register

14.1.5.2.433.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register (Offset = 188Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 4 firewall.

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Table 14-2192. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 188Ch

Figure 14-1089. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2193. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2193. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.434 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register

14.1.5.2.434.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register (Offset = 1890h) [reset = 7C408000h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 4 firewall.

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Table 14-2194. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1890h

Figure 14-1090. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7C408h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
7C408h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7C408h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2195. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C408h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.435 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register

14.1.5.2.435.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register (Offset = 1894h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 4 firewall.

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Table 14-2196. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1894h

Figure 14-1091. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2197. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.436 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register

14.1.5.2.436.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register (Offset = 1898h) [reset = 7C40FFFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 4 firewall.

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Table 14-2198. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1898h

Figure 14-1092. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C40Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C40Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7C40Fh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2199. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C40Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.437 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register

14.1.5.2.437.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register (Offset = 189Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 4 firewall.

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Table 14-2200. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 189Ch

Figure 14-1093. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2201. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.438 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register

14.1.5.2.438.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register (Offset = 18A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 5 firewall.

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Table 14-2202. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18A0h

Figure 14-1094. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2203. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.439 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register

14.1.5.2.439.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register (Offset = 18A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 5 firewall.

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Table 14-2204. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18A4h

Figure 14-1095. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2205. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2205. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.440 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register

14.1.5.2.440.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register (Offset = 18A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 5 firewall.

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Table 14-2206. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18A8h

Figure 14-1096. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2207. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2207. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.441 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register

14.1.5.2.441.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register (Offset = 18ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 5 firewall.

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Table 14-2208. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18ACh

Figure 14-1097. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2209. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2209. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.442 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register

14.1.5.2.442.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register (Offset = 18B0h) [reset = 7C404000h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 5 firewall.

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Table 14-2210. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18B0h

Figure 14-1098. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7C404h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
7C404h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7C404h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2211. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C404h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.443 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register

14.1.5.2.443.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register (Offset = 18B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 5 firewall.

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Table 14-2212. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18B4h

Figure 14-1099. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2213. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.444 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register

14.1.5.2.444.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register (Offset = 18B8h) [reset = 7C407FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 5 firewall.

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Table 14-2214. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18B8h

Figure 14-1100. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C407h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7C407h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C407h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2215. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C407h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.445 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register

14.1.5.2.445.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register (Offset = 18BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 5 firewall.

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Table 14-2216. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18BCh

Figure 14-1101. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2217. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.446 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register

14.1.5.2.446.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register (Offset = 18C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 6 firewall.

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Table 14-2218. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18C0h

Figure 14-1102. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2219. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.447 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register

14.1.5.2.447.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register (Offset = 18C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 6 firewall.

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Table 14-2220. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18C4h

Figure 14-1103. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2221. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2221. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.448 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register

14.1.5.2.448.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register (Offset = 18C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 6 firewall.

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Table 14-2222. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18C8h

Figure 14-1104. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2223. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2223. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.449 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register

14.1.5.2.449.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register (Offset = 18CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 6 firewall.

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Table 14-2224. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18CCh

Figure 14-1105. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2225. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2225. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.450 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register

14.1.5.2.450.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register (Offset = 18D0h) [reset = 7C440000h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 6 firewall.

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Table 14-2226. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18D0h

Figure 14-1106. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7C440h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
7C440h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7C440h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2227. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C440h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.451 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register

14.1.5.2.451.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register (Offset = 18D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 6 firewall.

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Table 14-2228. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18D4h

Figure 14-1107. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2229. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.452 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register

14.1.5.2.452.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register (Offset = 18D8h) [reset = 7C45FFFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 6 firewall.

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Table 14-2230. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18D8h

Figure 14-1108. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C45Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7C45Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7C45Fh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2231. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C45Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.453 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register

14.1.5.2.453.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register (Offset = 18DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 6 firewall.

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Table 14-2232. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18DCh

Figure 14-1109. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2233. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.454 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register

14.1.5.2.454.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register (Offset = 18E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 7 firewall.

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Table 14-2234. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18E0h

Figure 14-1110. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2235. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.455 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register

14.1.5.2.455.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register (Offset = 18E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 7 firewall.

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Table 14-2236. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18E4h

Figure 14-1111. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2237. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2237. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.456 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register

14.1.5.2.456.1
CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register (Offset = 18E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 7 firewall.

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Table 14-2238. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18E8h

Figure 14-1112. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2239. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2239. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.457 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register

14.1.5.2.457.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register (Offset = 18ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 7 firewall.

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Table 14-2240. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18ECh

Figure 14-1113. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2241. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2241. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.458 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register

14.1.5.2.458.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register (Offset = 18F0h) [reset = 7C460000h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 7 firewall.

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Table 14-2242. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18F0h

Figure 14-1114. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7C460h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
7C460h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7C460h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2243. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7C460h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.459 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register

14.1.5.2.459.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register (Offset = 18F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 7 firewall.

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Table 14-2244. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18F4h

Figure 14-1115. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2245. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.460 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register

14.1.5.2.460.1

CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register (Offset = 18F8h) [reset = 7C47FFFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 7 firewall.

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Table 14-2246. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18F8h

Figure 14-1116. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7C47Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7C47Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7C47Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2247. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7C47Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.461 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register

14.1.5.2.461.1 CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register (Offset = 18FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_0_main_0.soc_c7xv region 7 firewall.

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Table 14-2248. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 18FCh

Figure 14-1117. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2249. CBASS_FW_IAM275_C7XV_WRAP_0_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.462 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register

14.1.5.2.462.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register (Offset = 1C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 0 firewall.

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Table 14-2250. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C00h

Figure 14-1118. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2251. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.463 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register

14.1.5.2.463.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register (Offset = 1C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 0 firewall.

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Table 14-2252. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C04h

Figure 14-1119. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2253. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2253. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.464 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register

14.1.5.2.464.1

CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register (Offset = 1C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 0 firewall.

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Table 14-2254. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C08h

Figure 14-1120. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2255. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2255. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.465 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register

14.1.5.2.465.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register (Offset = 1C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 0 firewall.

Return to Summary Table

Table 14-2256. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C0Ch

Figure 14-1121. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2257. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2257. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.466 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register

14.1.5.2.466.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register (Offset = 1C10h) [reset = 7F000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 0 firewall.

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Table 14-2258. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C10h

Figure 14-1122. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7F000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
7F000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7F000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2259. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7F000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.467 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register

14.1.5.2.467.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register (Offset = 1C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 0 firewall.

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Table 14-2260. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C14h

Figure 14-1123. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2261. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.468 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register

14.1.5.2.468.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register (Offset = 1C18h) [reset = 7F1FFFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 0 firewall.

Return to Summary Table

Table 14-2262. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C18h

Figure 14-1124. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7F1FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7F1FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7F1FFh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2263. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7F1FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.469 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register

14.1.5.2.469.1

CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register (Offset = 1C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 0 firewall.

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Table 14-2264. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C1Ch

Figure 14-1125. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2265. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.470 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register

14.1.5.2.470.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register (Offset = 1C20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 1 firewall.

Return to Summary Table

Table 14-2266. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C20h

Figure 14-1126. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2267. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.471 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register

14.1.5.2.471.1

CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register (Offset = 1C24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 1 firewall.

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Table 14-2268. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C24h

Figure 14-1127. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2269. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2269. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.472 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register

14.1.5.2.472.1

CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register (Offset = 1C28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 1 firewall.

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Table 14-2270. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C28h

Figure 14-1128. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2271. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2271. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.473 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register

14.1.5.2.473.1

CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register (Offset = 1C2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 1 firewall.

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Table 14-2272. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C2Ch

Figure 14-1129. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2273. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2273. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.474 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register

14.1.5.2.474.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register (Offset = 1C30h) [reset = 7F200000h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 1 firewall.

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Table 14-2274. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C30h

Figure 14-1130. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7F200h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
7F200h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7F200h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2275. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7F200h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.475 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register

14.1.5.2.475.1

CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register (Offset = 1C34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 1 firewall.

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Table 14-2276. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C34h

Figure 14-1131. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2277. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.476 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register

14.1.5.2.476.1
CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register (Offset = 1C38h) [reset = 7F23FFFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 1 firewall.

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Table 14-2278. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C38h

Figure 14-1132. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7F23Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7F23Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7F23Fh</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2279. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7F23Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.477 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register

14.1.5.2.477.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register (Offset = 1C3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 1 firewall.

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Table 14-2280. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C3Ch

Figure 14-1133. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2281. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.478 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register

14.1.5.2.478.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register (Offset = 1C40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 2 firewall.

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Table 14-2282. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C40h

Figure 14-1134. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2283. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.479 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register

14.1.5.2.479.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register (Offset = 1C44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 2 firewall.

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Table 14-2284. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C44h

Figure 14-1135. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2285. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2285. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.480 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register

14.1.5.2.480.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register (Offset = 1C48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 2 firewall.

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Table 14-2286. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C48h

Figure 14-1136. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2287. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2287. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.481 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register

14.1.5.2.481.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register (Offset = 1C4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 2 firewall.

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Table 14-2288. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C4Ch

Figure 14-1137. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2289. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2289. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.482 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register

14.1.5.2.482.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register (Offset = 1C50h) [reset = 7D000000h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 2 firewall.

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Table 14-2290. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C50h

Figure 14-1138. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7D000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7D000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7D000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2291. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7D000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.483 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register

14.1.5.2.483.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register (Offset = 1C54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 2 firewall.

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Table 14-2292. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C54h

Figure 14-1139. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2293. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.484 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register

14.1.5.2.484.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register (Offset = 1C58h) [reset = 7D01FFFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 2 firewall.

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Table 14-2294. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C58h

Figure 14-1140. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7D01Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7D01Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7D01Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2295. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7D01Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.485 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register

14.1.5.2.485.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register (Offset = 1C5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 2 firewall.

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Table 14-2296. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C5Ch

Figure 14-1141. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2297. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.486 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register

14.1.5.2.486.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register (Offset = 1C60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 3 firewall.

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Table 14-2298. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C60h

Figure 14-1142. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2299. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.487 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register

14.1.5.2.487.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register (Offset = 1C64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 3 firewall.

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Table 14-2300. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C64h

Figure 14-1143. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2301. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2301. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.488 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register

14.1.5.2.488.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register (Offset = 1C68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 3 firewall.

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Table 14-2302. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C68h

Figure 14-1144. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2303. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2303. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.489 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register

14.1.5.2.489.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register (Offset = 1C6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 3 firewall.

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Table 14-2304. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C6Ch

Figure 14-1145. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2305. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2305. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.490 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register

14.1.5.2.490.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register (Offset = 1C70h) [reset = 7D400000h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 3 firewall.

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Table 14-2306. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C70h

Figure 14-1146. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7D400h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
7D400h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7D400h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2307. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7D400h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.491 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register

14.1.5.2.491.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register (Offset = 1C74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 3 firewall.

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Table 14-2308. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C74h

Figure 14-1147. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2309. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.492 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register

14.1.5.2.492.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register (Offset = 1C78h) [reset = 7D403FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 3 firewall.

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Table 14-2310. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C78h

Figure 14-1148. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7D403h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
7D403h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7D403h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2311. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7D403h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.493 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register

14.1.5.2.493.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register (Offset = 1C7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 3 firewall.

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Table 14-2312. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C7Ch

Figure 14-1149. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2313. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.494 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register

14.1.5.2.494.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register (Offset = 1C80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 4 firewall.

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Table 14-2314. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C80h

Figure 14-1150. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2315. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.495 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register

14.1.5.2.495.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register (Offset = 1C84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 4 firewall.

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Table 14-2316. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C84h

Figure 14-1151. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2317. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2317. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.496 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register

14.1.5.2.496.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register (Offset = 1C88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 4 firewall.

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Table 14-2318. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C88h

Figure 14-1152. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2319. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2319. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.497 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register

14.1.5.2.497.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register (Offset = 1C8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 4 firewall.

Return to Summary Table

Table 14-2320. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C8Ch

Figure 14-1153. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2321. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2321. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.498 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register

14.1.5.2.498.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register (Offset = 1C90h) [reset = 7D408000h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 4 firewall.

Return to Summary Table

Table 14-2322. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C90h

Figure 14-1154. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7D408h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7D408h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7D408h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2323. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7D408h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.499 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register

14.1.5.2.499.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register (Offset = 1C94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 4 firewall.

Return to Summary Table

Table 14-2324. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C94h

Figure 14-1155. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2325. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.500 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register

14.1.5.2.500.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register (Offset = 1C98h) [reset = 7D40FFFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 4 firewall.

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Table 14-2326. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C98h

Figure 14-1156. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7D40Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7D40Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7D40Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2327. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7D40Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.501 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register

14.1.5.2.501.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register (Offset = 1C9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 4 firewall.

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Table 14-2328. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1C9Ch

Figure 14-1157. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2329. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.502 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register

14.1.5.2.502.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register (Offset = 1CA0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 5 firewall.

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Table 14-2330. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CA0h

Figure 14-1158. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2331. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.503 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register

14.1.5.2.503.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register (Offset = 1CA4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 5 firewall.

Return to Summary Table

Table 14-2332. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CA4h

Figure 14-1159. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2333. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2333. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.504 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register

14.1.5.2.504.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register (Offset = 1CA8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 5 firewall.

Return to Summary Table

Table 14-2334. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CA8h

Figure 14-1160. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2335. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2335. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.505 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register

14.1.5.2.505.1

CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register (Offset = 1CACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 5 firewall.

Return to Summary Table

Table 14-2336. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CACh

Figure 14-1161. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2337. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2337. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.506 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register

14.1.5.2.506.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register (Offset = 1CB0h) [reset = 7D404000h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 5 firewall.

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Table 14-2338. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CB0h

Figure 14-1162. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7D404h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
7D404h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7D404h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2339. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7D404h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.507 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register

14.1.5.2.507.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register (Offset = 1CB4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 5 firewall.

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Table 14-2340. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CB4h

Figure 14-1163. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2341. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.508 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register

14.1.5.2.508.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register (Offset = 1CB8h) [reset = 7D407FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 5 firewall.

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Table 14-2342. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CB8h

Figure 14-1164. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7D407h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7D407h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7D407h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2343. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7D407h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.509 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register

14.1.5.2.509.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register (Offset = 1CBCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 5 firewall.

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Table 14-2344. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CBCh

Figure 14-1165. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2345. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.510 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register

14.1.5.2.510.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register (Offset = 1CC0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 6 firewall.

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Table 14-2346. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CC0h

Figure 14-1166. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2347. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.511 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register

14.1.5.2.511.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register (Offset = 1CC4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 6 firewall.

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Table 14-2348. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CC4h

Figure 14-1167. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2349. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2349. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.512 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register

14.1.5.2.512.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register (Offset = 1CC8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 6 firewall.

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Table 14-2350. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CC8h

Figure 14-1168. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2351. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2351. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.513 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register

14.1.5.2.513.1

CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register (Offset = 1CCCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 6 firewall.

Return to Summary Table

Table 14-2352. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CCCh

Figure 14-1169. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2353. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2353. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.514 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register

14.1.5.2.514.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register (Offset = 1CD0h) [reset = 7D440000h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 6 firewall.

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Table 14-2354. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CD0h

Figure 14-1170. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7D440h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
7D440h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7D440h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2355. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7D440h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.515 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register

14.1.5.2.515.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register (Offset = 1CD4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 6 firewall.

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Table 14-2356. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CD4h

Figure 14-1171. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2357. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.516 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register

14.1.5.2.516.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register (Offset = 1CD8h) [reset = 7D45FFFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 6 firewall.

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Table 14-2358. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CD8h

Figure 14-1172. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7D45FFh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7D45FFh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7D45FFh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2359. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7D45FFh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.517 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register

14.1.5.2.517.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register (Offset = 1CDCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 6 firewall.

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Table 14-2360. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CDCh

Figure 14-1173. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2361. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.518 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register

14.1.5.2.518.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register (Offset = 1CE0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 7 firewall.

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Table 14-2362. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CE0h

Figure 14-1174. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2363. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.519 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register

14.1.5.2.519.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register (Offset = 1CE4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 7 firewall.

Return to Summary Table

Table 14-2364. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CE4h

Figure 14-1175. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2365. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2365. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.520 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register

14.1.5.2.520.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register (Offset = 1CE8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 7 firewall.

Return to Summary Table

Table 14-2366. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CE8h

Figure 14-1176. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2367. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2367. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.521 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register

14.1.5.2.521.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register (Offset = 1CECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 7 firewall.

Return to Summary Table

Table 14-2368. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CECh

Figure 14-1177. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2369. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2369. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.522 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register

14.1.5.2.522.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register (Offset = 1CF0h) [reset = 7D460000h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 7 firewall.

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Table 14-2370. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CF0h

Figure 14-1178. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
7D460h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
7D460h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
7D460h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2371. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	7D460h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.523 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register

14.1.5.2.523.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register (Offset = 1CF4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 7 firewall.

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Table 14-2372. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CF4h

Figure 14-1179. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2373. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.524 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register

14.1.5.2.524.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register (Offset = 1CF8h) [reset = 7D47FFFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 7 firewall.

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Table 14-2374. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CF8h

Figure 14-1180. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
7D47Fh							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
7D47Fh							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
7D47Fh				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2375. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	7D47Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.525 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register

14.1.5.2.525.1 CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register (Offset = 1CFCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_c7xv_wrap_1_main_0.soc_c7xv region 7 firewall.

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Table 14-2376. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4504 1CFCh

Figure 14-1181. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2377. CBASS_FW_IAM275_C7XV_WRAP_1_MAIN_0_SOC_C7XV_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.526 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register

14.1.5.2.526.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register (Offset = 0h) [reset = 102000h]

The ISC Region 0 Control Register defines the control fields for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 0 ISC.

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Table 14-2378. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0000h

Figure 14-1182. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2379. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	20h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2379. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.527 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.527.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 0 ISC.

Return to Summary Table

Table 14-2380. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0010h

Figure 14-1183. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2381. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.528 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.528.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 0 ISC.

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Table 14-2382. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0014h

Figure 14-1184. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2383. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.529 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.529.1

CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 0 ISC.

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Table 14-2384. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0018h

Figure 14-1185. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2385. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.530 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.530.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 0 ISC.

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Table 14-2386. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 001Ch

Figure 14-1186. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2387. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.531 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register

14.1.5.2.531.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register (Offset = 20h) [reset = 102000h]

The ISC Region 1 Control Register defines the control fields for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 1 ISC.

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Table 14-2388. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0020h

Figure 14-1187. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
20h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2389. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	20h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2389. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.532 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.532.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 1 ISC.

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Table 14-2390. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0030h

Figure 14-1188. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2391. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.533 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.533.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 1 ISC.

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Table 14-2392. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0034h

Figure 14-1189. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2393. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.534 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.534.1

CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 1 ISC.

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Table 14-2394. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0038h

Figure 14-1190. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2395. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.535 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.535.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 1 ISC.

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Table 14-2396. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 003Ch

Figure 14-1191. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2397. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.536 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register

14.1.5.2.536.1 CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register (Offset = 40h) [reset = 10204Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc region 2 ISC.

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Table 14-2398. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0040h

Figure 14-1192. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
20h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2399. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2399. CBASS_ISC_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	20h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.537 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register

14.1.5.2.537.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register (Offset = 400h) [reset = 102100h]

The ISC Region 0 Control Register defines the control fields for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 0 ISC.

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Table 14-2400. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0400h

Figure 14-1193. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
21h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2401. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	21h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2401. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.538 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.538.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 0 ISC.

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Table 14-2402. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0410h

Figure 14-1194. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2403. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.539 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.539.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 0 ISC.

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Table 14-2404. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0414h

Figure 14-1195. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2405. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.540 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.540.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 0 ISC.

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Table 14-2406. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0418h

Figure 14-1196. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2407. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.541 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.541.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 0 ISC.

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Table 14-2408. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 041Ch

Figure 14-1197. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2409. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.542 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register

14.1.5.2.542.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register (Offset = 420h) [reset = 102100h]

The ISC Region 1 Control Register defines the control fields for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 1 ISC.

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Table 14-2410. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0420h

Figure 14-1198. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
21h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2411. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	21h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2411. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.543 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.543.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 1 ISC.

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Table 14-2412. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0430h

Figure 14-1199. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2413. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.544 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.544.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 1 ISC.

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Table 14-2414. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0434h

Figure 14-1200. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2415. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.545 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.545.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 1 ISC.

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Table 14-2416. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0438h

Figure 14-1201. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2417. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.546 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.546.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 1 ISC.

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Table 14-2418. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 043Ch

Figure 14-1202. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2419. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.547 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register

14.1.5.2.547.1 CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register (Offset = 440h) [reset = 10214Ah]

The ISC Default Region Control Register defines the control fields for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc region 2 ISC.

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Table 14-2420. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0440h

Figure 14-1203. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
21h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2421. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2421. CBASS_ISC_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	21h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.548 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_CONTROL Register

14.1.5.2.548.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_CONTROL Register (Offset = 800h) [reset = 10D800h]

The ISC Region 0 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 0 ISC.

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Table 14-2422. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0800h

Figure 14-1204. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D8h							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2423. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2423. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.549 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.549.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 0 ISC.

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Table 14-2424. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0810h

Figure 14-1205. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2425. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.550 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.550.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 0 ISC.

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Table 14-2426. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0814h

Figure 14-1206. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2427. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.551 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.551.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 0 ISC.

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Table 14-2428. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0818h

Figure 14-1207. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2429. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.552 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.552.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 0 ISC.

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Table 14-2430. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 081Ch

Figure 14-1208. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2431. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.553 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_CONTROL Register

14.1.5.2.553.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_CONTROL Register (Offset = 820h) [reset = 10D800h]

The ISC Region 1 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 1 ISC.

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Table 14-2432. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0820h

Figure 14-1209. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2433. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2433. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.554 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.554.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 1 ISC.

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Table 14-2434. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0830h

Figure 14-1210. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2435. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.555 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.555.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 1 ISC.

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Table 14-2436. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0834h

Figure 14-1211. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2437. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.556 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.556.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 1 ISC.

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Table 14-2438. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0838h

Figure 14-1212. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2439. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.557 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.557.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 1 ISC.

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Table 14-2440. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 083Ch

Figure 14-1213. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2441. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.558 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_CONTROL Register

14.1.5.2.558.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_CONTROL Register (Offset = 840h) [reset = 10D800h]

The ISC Region 2 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 2 ISC.

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Table 14-2442. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0840h

Figure 14-1214. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2443. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2443. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.559 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L Register

14.1.5.2.559.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 2 ISC.

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Table 14-2444. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0850h

Figure 14-1215. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2445. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.560 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H Register

14.1.5.2.560.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 2 ISC.

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Table 14-2446. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0854h

Figure 14-1216. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2447. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.561 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L Register

14.1.5.2.561.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 2 ISC.

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Table 14-2448. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0858h

Figure 14-1217. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2449. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.562 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H Register

14.1.5.2.562.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 2 ISC.

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Table 14-2450. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 085Ch

Figure 14-1218. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2451. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.563 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_CONTROL Register

14.1.5.2.563.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_CONTROL Register (Offset = 860h) [reset = 10D800h]

The ISC Region 3 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 3 ISC.

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Table 14-2452. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0860h

Figure 14-1219. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2453. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2453. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.564 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L Register

14.1.5.2.564.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 3 ISC.

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Table 14-2454. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0870h

Figure 14-1220. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2455. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.565 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H Register

14.1.5.2.565.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 3 ISC.

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Table 14-2456. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0874h

Figure 14-1221. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2457. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.566 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L Register

14.1.5.2.566.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 3 ISC.

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Table 14-2458. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0878h

Figure 14-1222. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2459. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.567 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H Register

14.1.5.2.567.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 3 ISC.

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Table 14-2460. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 087Ch

Figure 14-1223. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2461. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.568 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_DEF_CONTROL Register

14.1.5.2.568.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_DEF_CONTROL Register (Offset = 880h) [reset = 10D84Ah]

The ISC Default Region Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifr region 4 ISC.

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Table 14-2462. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0880h

Figure 14-1224. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2463. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2463. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.569 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_CONTROL Register

14.1.5.2.569.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_CONTROL Register (Offset = C00h) [reset = 10D800h]

The ISC Region 0 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 0 ISC.

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Table 14-2464. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C00h

Figure 14-1225. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2465. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2465. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.570 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.570.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 0 ISC.

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Table 14-2466. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C10h

Figure 14-1226. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2467. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.571 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.571.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 0 ISC.

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Table 14-2468. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C14h

Figure 14-1227. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2469. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.572 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.572.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator lrl2_of_cba4_main_r5_0_core0.iifw region 0 ISC.

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Table 14-2470. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C18h

Figure 14-1228. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2471. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.573 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.573.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 0 ISC.

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Table 14-2472. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C1Ch

Figure 14-1229. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2473. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.574 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_CONTROL Register

14.1.5.2.574.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_CONTROL Register (Offset = C20h) [reset = 10D800h]

The ISC Region 1 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 1 ISC.

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Table 14-2474. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C20h

Figure 14-1230. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2475. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2475. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.575 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.575.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L Register (Offset = C30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 1 ISC.

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Table 14-2476. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C30h

Figure 14-1231. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2477. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.576 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.576.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H Register (Offset = C34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 1 ISC.

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Table 14-2478. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C34h

Figure 14-1232. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-2479. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.577 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.577.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L Register (Offset = C38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 1 ISC.

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Table 14-2480. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C38h

Figure 14-1233. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2481. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.578 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.578.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H Register (Offset = C3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator lrl2_of_cba4_main_r5_0_core0.iifw region 1 ISC.

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Table 14-2482. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C3Ch

Figure 14-1234. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2483. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.579 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_CONTROL Register

14.1.5.2.579.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_CONTROL Register (Offset = C40h) [reset = 10D800h]

The ISC Region 2 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 2 ISC.

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Table 14-2484. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C40h

Figure 14-1235. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D8h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2485. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2485. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.580 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L Register

14.1.5.2.580.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L Register (Offset = C50h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 2 ISC.

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Table 14-2486. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C50h

Figure 14-1236. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2487. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.581 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H Register

14.1.5.2.581.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H Register (Offset = C54h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 2 ISC.

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Table 14-2488. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C54h

Figure 14-1237. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2489. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.582 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L Register

14.1.5.2.582.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L Register (Offset = C58h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 2 ISC.

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Table 14-2490. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C58h

Figure 14-1238. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2491. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.583 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H Register

14.1.5.2.583.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H Register (Offset = C5Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 2 ISC.

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Table 14-2492. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C5Ch

Figure 14-1239. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2493. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.584 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_CONTROL Register

14.1.5.2.584.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_CONTROL Register (Offset = C60h) [reset = 10D800h]

The ISC Region 3 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 3 ISC.

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Table 14-2494. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C60h

Figure 14-1240. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2495. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2495. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.585 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L Register

14.1.5.2.585.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L Register (Offset = C70h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 3 ISC.

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Table 14-2496. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C70h

Figure 14-1241. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2497. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.586 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H Register

14.1.5.2.586.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H Register (Offset = C74h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 3 ISC.

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Table 14-2498. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C74h

Figure 14-1242. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2499. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.587 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L Register

14.1.5.2.587.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L Register (Offset = C78h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 3 ISC.

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Table 14-2500. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C78h

Figure 14-1243. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2501. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.588 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H Register

14.1.5.2.588.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H Register (Offset = C7Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 3 ISC.

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Table 14-2502. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C7Ch

Figure 14-1244. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2503. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.589 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_DEF_CONTROL Register

14.1.5.2.589.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_DEF_CONTROL Register (Offset = C80h) [reset = 10D84Ah]

The ISC Default Region Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifw region 4 ISC.

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Table 14-2504. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 0C80h

Figure 14-1245. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2505. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2505. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.590 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_CONTROL Register

14.1.5.2.590.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_CONTROL Register (Offset = 1000h) [reset = 10D900h]

The ISC Region 0 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 0 ISC.

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Table 14-2506. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1000h

Figure 14-1246. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2507. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2507. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.591 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.591.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 0 ISC.

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Table 14-2508. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1010h

Figure 14-1247. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2509. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.592 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.592.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 0 ISC.

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Table 14-2510. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1014h

Figure 14-1248. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2511. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.593 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.593.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 0 ISC.

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Table 14-2512. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1018h

Figure 14-1249. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2513. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.594 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.594.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 101Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 0 ISC.

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Table 14-2514. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 101Ch

Figure 14-1250. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2515. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.595 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_CONTROL Register

14.1.5.2.595.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_CONTROL Register (Offset = 1020h) [reset = 10D900h]

The ISC Region 1 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 1 ISC.

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Table 14-2516. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1020h

Figure 14-1251. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2517. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2517. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.596 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.596.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L Register (Offset = 1030h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 1 ISC.

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Table 14-2518. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1030h

Figure 14-1252. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2519. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.597 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.597.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H Register (Offset = 1034h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 1 ISC.

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Table 14-2520. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1034h

Figure 14-1253. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2521. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.598 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.598.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L Register (Offset = 1038h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 1 ISC.

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Table 14-2522. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1038h

Figure 14-1254. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2523. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.599 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.599.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H Register (Offset = 103Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator lrl2_of_cba4_main_r5_0_core1.iifr region 1 ISC.

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Table 14-2524. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 103Ch

Figure 14-1255. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2525. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.600 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_CONTROL Register

14.1.5.2.600.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_CONTROL Register (Offset = 1040h) [reset = 10D900h]

The ISC Region 2 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 2 ISC.

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Table 14-2526. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1040h

Figure 14-1256. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2527. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2527. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.601 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L Register

14.1.5.2.601.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L Register (Offset = 1050h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 2 ISC.

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Table 14-2528. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1050h

Figure 14-1257. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2529. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.602 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H Register

14.1.5.2.602.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H Register (Offset = 1054h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 2 ISC.

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Table 14-2530. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1054h

Figure 14-1258. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2531. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.603 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L Register

14.1.5.2.603.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L Register (Offset = 1058h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 2 ISC.

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Table 14-2532. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1058h

Figure 14-1259. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2533. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.604 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H Register

14.1.5.2.604.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H Register (Offset = 105Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 2 ISC.

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Table 14-2534. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 105Ch

Figure 14-1260. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2535. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.605 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_CONTROL Register

14.1.5.2.605.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_CONTROL Register (Offset = 1060h) [reset = 10D900h]

The ISC Region 3 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 3 ISC.

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Table 14-2536. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1060h

Figure 14-1261. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D9h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2537. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2537. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.606 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L Register

14.1.5.2.606.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L Register (Offset = 1070h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 3 ISC.

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Table 14-2538. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1070h

Figure 14-1262. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2539. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.607 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H Register

14.1.5.2.607.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H Register (Offset = 1074h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 3 ISC.

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Table 14-2540. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1074h

Figure 14-1263. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2541. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.608 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L Register

14.1.5.2.608.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L Register (Offset = 1078h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator lrl2_of_cba4_main_r5_0_core1.iifr region 3 ISC.

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Table 14-2542. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1078h

Figure 14-1264. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2543. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.609 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H Register

14.1.5.2.609.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H Register (Offset = 107Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 3 ISC.

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Table 14-2544. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 107Ch

Figure 14-1265. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2545. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.610 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_DEF_CONTROL Register

14.1.5.2.610.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_DEF_CONTROL Register (Offset = 1080h) [reset = 10D94Ah]

The ISC Default Region Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifr region 4 ISC.

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Table 14-2546. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1080h

Figure 14-1266. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2547. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2547. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.611 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_CONTROL Register

14.1.5.2.611.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_CONTROL Register (Offset = 1400h) [reset = 10D900h]

The ISC Region 0 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 0 ISC.

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Table 14-2548. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1400h

Figure 14-1267. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2549. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2549. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.612 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.612.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 0 ISC.

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Table 14-2550. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1410h

Figure 14-1268. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2551. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.613 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.613.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 0 ISC.

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Table 14-2552. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1414h

Figure 14-1269. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2553. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.614 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.614.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 0 ISC.

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Table 14-2554. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1418h

Figure 14-1270. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2555. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.615 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.615.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H Register (Offset = 141Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 0 ISC.

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Table 14-2556. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 141Ch

Figure 14-1271. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2557. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.616 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_CONTROL Register

14.1.5.2.616.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_CONTROL Register (Offset = 1420h) [reset = 10D900h]

The ISC Region 1 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 1 ISC.

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Table 14-2558. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1420h

Figure 14-1272. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D9h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2559. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2559. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.617 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.617.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L Register (Offset = 1430h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 1 ISC.

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Table 14-2560. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1430h

Figure 14-1273. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2561. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.618 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.618.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H Register (Offset = 1434h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 1 ISC.

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Table 14-2562. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1434h

Figure 14-1274. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2563. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.619 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.619.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L Register (Offset = 1438h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 1 ISC.

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Table 14-2564. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1438h

Figure 14-1275. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2565. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.620 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.620.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H Register (Offset = 143Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 1 ISC.

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Table 14-2566. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 143Ch

Figure 14-1276. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2567. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.621 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_CONTROL Register

14.1.5.2.621.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_CONTROL Register (Offset = 1440h) [reset = 10D900h]

The ISC Region 2 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 2 ISC.

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Table 14-2568. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1440h

Figure 14-1277. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2569. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2569. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.622 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L Register

14.1.5.2.622.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L Register (Offset = 1450h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 2 ISC.

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Table 14-2570. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1450h

Figure 14-1278. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2571. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.623 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H Register

14.1.5.2.623.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H Register (Offset = 1454h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 2 ISC.

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Table 14-2572. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1454h

Figure 14-1279. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2573. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.624 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L Register

14.1.5.2.624.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L Register (Offset = 1458h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator lrl2_of_cba4_main_r5_0_core1.iifw region 2 ISC.

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Table 14-2574. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1458h

Figure 14-1280. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2575. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.625 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H Register

14.1.5.2.625.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H Register (Offset = 145Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 2 ISC.

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Table 14-2576. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 145Ch

Figure 14-1281. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2577. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.626 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_CONTROL Register

14.1.5.2.626.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_CONTROL Register (Offset = 1460h) [reset = 10D900h]

The ISC Region 3 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 3 ISC.

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Table 14-2578. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1460h

Figure 14-1282. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2579. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2579. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.627 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L Register

14.1.5.2.627.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L Register (Offset = 1470h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 3 ISC.

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Table 14-2580. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1470h

Figure 14-1283. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2581. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.628 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H Register

14.1.5.2.628.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H Register (Offset = 1474h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 3 ISC.

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Table 14-2582. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1474h

Figure 14-1284. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2583. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.629 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L Register

14.1.5.2.629.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L Register (Offset = 1478h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 3 ISC.

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Table 14-2584. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1478h

Figure 14-1285.
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2585.
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.630 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H Register

14.1.5.2.630.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H Register (Offset = 147Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 3 ISC.

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Table 14-2586. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 147Ch

Figure 14-1286. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2587. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.631 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_DEF_CONTROL Register

14.1.5.2.631.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_DEF_CONTROL Register (Offset = 1480h) [reset = 10D94Ah]

The ISC Default Region Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifw region 4 ISC.

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Table 14-2588. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1480h

Figure 14-1287. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2589. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2589. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.632 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_CONTROL Register

14.1.5.2.632.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_CONTROL Register (Offset = 1800h) [reset = 10DB00h]

The ISC Region 0 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 0 ISC.

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Table 14-2590. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1800h

Figure 14-1288. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DBh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2591. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2591. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.633 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.633.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 0 ISC.

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Table 14-2592. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1810h

Figure 14-1289. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2593. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.634 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.634.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 0 ISC.

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Table 14-2594. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1814h

Figure 14-1290. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2595. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.635 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.635.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 0 ISC.

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Table 14-2596. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1818h

Figure 14-1291. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2597. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.636 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.636.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 181Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 0 ISC.

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Table 14-2598. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 181Ch

Figure 14-1292. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2599. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.637 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_CONTROL Register

14.1.5.2.637.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_CONTROL Register (Offset = 1820h) [reset = 10DB00h]

The ISC Region 1 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 1 ISC.

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Table 14-2600. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1820h

Figure 14-1293. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DBh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2601. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2601. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.638 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.638.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L Register (Offset = 1830h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 1 ISC.

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Table 14-2602. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1830h

Figure 14-1294. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2603. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.639 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.639.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H Register (Offset = 1834h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 1 ISC.

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Table 14-2604. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1834h

Figure 14-1295. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2605. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.640 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.640.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L Register (Offset = 1838h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 1 ISC.

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Table 14-2606. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1838h

Figure 14-1296. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2607. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.641 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.641.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H Register (Offset = 183Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 1 ISC.

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Table 14-2608. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 183Ch

Figure 14-1297. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2609. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.642 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_CONTROL Register

14.1.5.2.642.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_CONTROL Register (Offset = 1840h) [reset = 10DB00h]

The ISC Region 2 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 2 ISC.

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Table 14-2610. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1840h

Figure 14-1298. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DBh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2611. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2611. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.643 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L Register

14.1.5.2.643.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L Register (Offset = 1850h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 2 ISC.

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Table 14-2612. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1850h

Figure 14-1299. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2613. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.644 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H Register

14.1.5.2.644.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H Register (Offset = 1854h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 2 ISC.

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Table 14-2614. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1854h

Figure 14-1300. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2615. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.645 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L Register

14.1.5.2.645.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L Register (Offset = 1858h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 2 ISC.

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Table 14-2616. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1858h

Figure 14-1301. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2617. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.646 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H Register

14.1.5.2.646.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H Register (Offset = 185Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 2 ISC.

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Table 14-2618. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 185Ch

Figure 14-1302. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2619. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.647 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_CONTROL Register

14.1.5.2.647.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_CONTROL Register (Offset = 1860h) [reset = 10DB00h]

The ISC Region 3 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 3 ISC.

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Table 14-2620. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1860h

Figure 14-1303. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DBh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2621. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2621. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.648 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L Register

14.1.5.2.648.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L Register (Offset = 1870h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 3 ISC.

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Table 14-2622. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1870h

Figure 14-1304. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			

7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2623. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.649 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H Register

14.1.5.2.649.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H Register (Offset = 1874h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 3 ISC.

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Table 14-2624. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1874h

Figure 14-1305. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2625. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.650 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L Register

14.1.5.2.650.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L Register (Offset = 1878h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 3 ISC.

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Table 14-2626. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1878h

Figure 14-1306. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2627. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.651 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H Register

14.1.5.2.651.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H Register (Offset = 187Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 3 ISC.

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Table 14-2628. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 187Ch

Figure 14-1307. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2629. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.652 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_DEF_CONTROL Register

14.1.5.2.652.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_DEF_CONTROL Register (Offset = 1880h) [reset = 10DB4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifr region 4 ISC.

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Table 14-2630. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1880h

Figure 14-1308. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DBh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2631. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2631. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.653 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_CONTROL Register

14.1.5.2.653.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_CONTROL Register (Offset = 1C00h) [reset = 10DB00h]

The ISC Region 0 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 0 ISC.

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Table 14-2632. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C00h

Figure 14-1309. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DBh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2633. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2633. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.654 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.654.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L Register (Offset = 1C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 0 ISC.

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Table 14-2634. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C10h

Figure 14-1310. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2635. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.655 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.655.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H Register (Offset = 1C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 0 ISC.

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Table 14-2636. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C14h

Figure 14-1311. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2637. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.656 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.656.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L Register (Offset = 1C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 0 ISC.

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Table 14-2638. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C18h

Figure 14-1312. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2639. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.657 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.657.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 0 ISC.

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Table 14-2640. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C1Ch

Figure 14-1313. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2641. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.658 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_CONTROL Register

14.1.5.2.658.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_CONTROL Register (Offset = 1C20h) [reset = 10DB00h]

The ISC Region 1 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 1 ISC.

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Table 14-2642. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C20h

Figure 14-1314. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DBh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2643. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2643. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.659 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.659.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L Register (Offset = 1C30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 1 ISC.

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Table 14-2644. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C30h

Figure 14-1315. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2645. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.660 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.660.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H Register (Offset = 1C34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 1 ISC.

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Table 14-2646. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C34h

Figure 14-1316. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2647. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.661 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.661.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L Register (Offset = 1C38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 1 ISC.

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Table 14-2648. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C38h

Figure 14-1317. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2649. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.662 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.662.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H Register (Offset = 1C3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 1 ISC.

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Table 14-2650. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C3Ch

Figure 14-1318. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2651. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.663 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_CONTROL Register

14.1.5.2.663.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_CONTROL Register (Offset = 1C40h) [reset = 10DB00h]

The ISC Region 2 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 2 ISC.

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Table 14-2652. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C40h

Figure 14-1319. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DBh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2653. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2653. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.664 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L Register

14.1.5.2.664.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L Register (Offset = 1C50h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 2 ISC.

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Table 14-2654. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C50h

Figure 14-1320. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2655. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.665 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H Register

14.1.5.2.665.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H Register (Offset = 1C54h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 2 ISC.

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Table 14-2656. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C54h

Figure 14-1321. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2657. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.666 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L Register

14.1.5.2.666.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L Register (Offset = 1C58h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 2 ISC.

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Table 14-2658. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C58h

Figure 14-1322. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2659. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.667 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H Register

14.1.5.2.667.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H Register (Offset = 1C5Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 2 ISC.

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Table 14-2660. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C5Ch

Figure 14-1323. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2661. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.668 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_CONTROL Register

14.1.5.2.668.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_CONTROL Register (Offset = 1C60h) [reset = 10DB00h]

The ISC Region 3 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 3 ISC.

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Table 14-2662. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C60h

Figure 14-1324. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DBh							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2663. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2663. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.669 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L Register

14.1.5.2.669.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L Register (Offset = 1C70h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 3 ISC.

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Table 14-2664. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C70h

Figure 14-1325. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2665. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.670 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H Register

14.1.5.2.670.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H Register (Offset = 1C74h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 3 ISC.

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Table 14-2666. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C74h

Figure 14-1326. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2667. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.671 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L Register

14.1.5.2.671.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L Register (Offset = 1C78h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 3 ISC.

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Table 14-2668. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C78h

Figure 14-1327. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2669. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.672 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H Register

14.1.5.2.672.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H Register (Offset = 1C7Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core0.iifw region 3 ISC.

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Table 14-2670. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 1C7Ch

Figure 14-1328. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2671. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.673 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_DEF_CONTROL Register

14.1.5.2.673.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_DEF_CONTROL Register (Offset = 1C80h) [reset = 10DB4Ah]

The ISC Default Region Control Register defines the control fields for the initiator lrl2_of_cba4_main_r5_1_core0.iifw region 4 ISC.

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Table 14-2672. Instance Table

Instance Name	**Physical Address**
CBASS_MEM0	4583 1C80h

Figure 14-1329. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DBh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2673. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2673. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.674 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_CONTROL Register

14.1.5.2.674.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_CONTROL Register (Offset = 2000h) [reset = 10DC00h]

The ISC Region 0 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 0 ISC.

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Table 14-2674. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2000h

Figure 14-1330. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DCh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2675. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2675. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.675 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.675.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2010h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 0 ISC.

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Table 14-2676. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2010h

Figure 14-1331. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2677. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.676 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.676.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2014h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 0 ISC.

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Table 14-2678. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2014h

Figure 14-1332. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2679. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.677 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.677.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2018h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 0 ISC.

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Table 14-2680. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2018h

Figure 14-1333. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2681. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.678 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.678.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H Register (Offset = 201Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 0 ISC.

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Table 14-2682. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 201Ch

Figure 14-1334. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2683. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.679 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_CONTROL Register

14.1.5.2.679.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_CONTROL Register (Offset = 2020h) [reset = 10DC00h]

The ISC Region 1 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 1 ISC.

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Table 14-2684. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2020h

Figure 14-1335. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DCh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2685. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2685. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.680 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.680.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L Register (Offset = 2030h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator lrl2_of_cba4_main_r5_1_core1.iifr region 1 ISC.

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Table 14-2686. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2030h

Figure 14-1336. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2687. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.681 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.681.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H Register (Offset = 2034h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 1 ISC.

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Table 14-2688. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2034h

Figure 14-1337. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2689. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.682 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.682.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L Register (Offset = 2038h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 1 ISC.

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Table 14-2690. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2038h

Figure 14-1338. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2691. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.683 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.683.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H Register (Offset = 203Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 1 ISC.

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Table 14-2692. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 203Ch

Figure 14-1339. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2693. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.684 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_CONTROL Register

14.1.5.2.684.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_CONTROL Register (Offset = 2040h) [reset = 10DC00h]

The ISC Region 2 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 2 ISC.

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Table 14-2694. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2040h

Figure 14-1340. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DCh							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2695. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2695. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.685 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L Register

14.1.5.2.685.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L Register (Offset = 2050h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 2 ISC.

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Table 14-2696. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2050h

Figure 14-1341. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2697. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.686 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H Register

14.1.5.2.686.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H Register (Offset = 2054h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 2 ISC.

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Table 14-2698. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2054h

Figure 14-1342. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2699. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.687 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L Register

14.1.5.2.687.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L Register (Offset = 2058h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator lrl2_of_cba4_main_r5_1_core1.iifr region 2 ISC.

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Table 14-2700. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2058h

Figure 14-1343. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2701. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.688 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H Register

14.1.5.2.688.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H Register (Offset = 205Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 2 ISC.

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Table 14-2702. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 205Ch

Figure 14-1344. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2703. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.689 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_CONTROL Register

14.1.5.2.689.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_CONTROL Register (Offset = 2060h) [reset = 10DC00h]

The ISC Region 3 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 3 ISC.

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Table 14-2704. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2060h

Figure 14-1345. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DCh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2705. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2705. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.690 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L Register

14.1.5.2.690.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L Register (Offset = 2070h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 3 ISC.

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Table 14-2706. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2070h

Figure 14-1346. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2707. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.691 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H Register

14.1.5.2.691.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H Register (Offset = 2074h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 3 ISC.

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Table 14-2708. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2074h

Figure 14-1347. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2709. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.692 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L Register

14.1.5.2.692.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L Register (Offset = 2078h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 3 ISC.

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Table 14-2710. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2078h

Figure 14-1348. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2711. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.693 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H Register

14.1.5.2.693.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H Register (Offset = 207Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 3 ISC.

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Table 14-2712. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 207Ch

Figure 14-1349. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2713. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.694 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_DEF_CONTROL Register

14.1.5.2.694.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_DEF_CONTROL Register (Offset = 2080h) [reset = 10DC4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifr region 4 ISC.

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Table 14-2714. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2080h

Figure 14-1350. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DCh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2715. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2715. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.695 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_CONTROL Register

14.1.5.2.695.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_CONTROL Register (Offset = 2400h) [reset = 10DC00h]

The ISC Region 0 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 0 ISC.

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Table 14-2716. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2400h

Figure 14-1351. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DCh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2717. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2717. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.696 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L Register

14.1.5.2.696.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L Register (Offset = 2410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 0 ISC.

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Table 14-2718. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2410h

Figure 14-1352. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2719. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.697 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H Register

14.1.5.2.697.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H Register (Offset = 2414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 0 ISC.

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Table 14-2720. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2414h

Figure 14-1353. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2721. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.698 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L Register

14.1.5.2.698.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L Register (Offset = 2418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 0 ISC.

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Table 14-2722. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2418h

Figure 14-1354. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2723. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.699 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H Register

14.1.5.2.699.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H Register (Offset = 241Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 0 ISC.

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Table 14-2724. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 241Ch

Figure 14-1355. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2725. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.700 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_CONTROL Register

14.1.5.2.700.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_CONTROL Register (Offset = 2420h) [reset = 10DC00h]

The ISC Region 1 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 1 ISC.

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Table 14-2726. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2420h

Figure 14-1356. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DCh							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2727. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2727. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.701 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L Register

14.1.5.2.701.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L Register (Offset = 2430h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 1 ISC.

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Table 14-2728. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2430h

Figure 14-1357. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2729. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.702 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H Register

14.1.5.2.702.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H Register (Offset = 2434h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 1 ISC.

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Table 14-2730. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2434h

Figure 14-1358. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2731. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.703 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L Register

14.1.5.2.703.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L Register (Offset = 2438h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 1 ISC.

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Table 14-2732. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2438h

Figure 14-1359. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2733. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.704 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H Register

14.1.5.2.704.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H Register (Offset = 243Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 1 ISC.

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Table 14-2734. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 243Ch

Figure 14-1360. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2735. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.705 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_CONTROL Register

14.1.5.2.705.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_CONTROL Register (Offset = 2440h) [reset = 10DC00h]

The ISC Region 2 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 2 ISC.

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Table 14-2736. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2440h

Figure 14-1361. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">NOPRIV</td><td colspan="2">PRIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PASS</td><td>NONSEC</td><td colspan="4">SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">DCh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DEF</td><td>CH_MODE</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td>NONE</td><td>R</td><td>R/W</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2737. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2737. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.706 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L Register

14.1.5.2.706.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L Register (Offset = 2450h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 2 ISC.

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Table 14-2738. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2450h

Figure 14-1362. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2739. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.707 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H Register

14.1.5.2.707.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H Register (Offset = 2454h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 2 ISC.

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Table 14-2740. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2454h

Figure 14-1363. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2741. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.708 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L Register

14.1.5.2.708.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L Register (Offset = 2458h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator lrl2_of_cba4_main_r5_1_core1.iifw region 2 ISC.

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Table 14-2742. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2458h

Figure 14-1364. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2743. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.709 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H Register

14.1.5.2.709.1

CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H Register (Offset = 245Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 2 ISC.

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Table 14-2744. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 245Ch

Figure 14-1365. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2745. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.710 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_CONTROL Register

14.1.5.2.710.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_CONTROL Register (Offset = 2460h) [reset = 10DC00h]

The ISC Region 3 Control Register defines the control fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 3 ISC.

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Table 14-2746. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2460h

Figure 14-1366. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DCh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-2747. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-2747. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.711 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L Register

14.1.5.2.711.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L Register (Offset = 2470h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator lrl2_of_cba4_main_r5_1_core1.iifw region 3 ISC.

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Table 14-2748. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2470h

Figure 14-1367. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-2749. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.712 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H Register

14.1.5.2.712.1
CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H Register (Offset = 2474h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 3 ISC.

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Table 14-2750. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2474h

Figure 14-1368. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2751. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.713 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L Register

14.1.5.2.713.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L Register (Offset = 2478h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 3 ISC.

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Table 14-2752. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2478h

Figure 14-1369. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2753. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.714 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H Register

14.1.5.2.714.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H Register (Offset = 247Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Irl2_of_cba4_main_r5_1_core1.iifw region 3 ISC.

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Table 14-2754. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 247Ch

Figure 14-1370. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2755. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.715 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_DEF_CONTROL Register

14.1.5.2.715.1 CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_DEF_CONTROL Register (Offset = 2480h) [reset = 10DC4Ah]

The ISC Default Region Control Register defines the control fields for the initiator lrl2_of_cba4_main_r5_1_core1.iifw region 4 ISC.

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Table 14-2756. Instance Table

Instance Name	Physical Address
CBASS_MEM0	4583 2480h

Figure 14-1371. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DCh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-2757. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2757. CBASS_ISC_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.716 CBASS_GLB_PID Register

14.1.5.2.716.1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66005102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-2758. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2000h

Figure 14-1372. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Ah					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-2759. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	Ah	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.717 CBASS_GLB_DESTINATION_ID Register

14.1.5.2.717.1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-2760. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2004h

Figure 14-1373. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEST_ID							
R/W							
0h							

Table 14-2761. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.718 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

14.1.5.2.718.1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-2762. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2020h

Figure 14-1374. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-2763. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.719 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

14.1.5.2.719.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-2764. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2024h

Figure 14-1375. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-2765. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.720 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

14.1.5.2.720.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-2766. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2028h

Figure 14-1376. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-2767. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.5.2.721 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

14.1.5.2.721.1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-2768. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 202Ch

Figure 14-1377. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-2769. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.722 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

14.1.5.2.722.1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-2770. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2030h

Figure 14-1378. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDR_H							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR_H							
R							
0h							

Table 14-2771. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.723 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

14.1.5.2.723.1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-2772. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2034h

Figure 14-1379. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-2773. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.724 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

14.1.5.2.724.1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-2774. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2038h

Figure 14-1380. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2775. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.725 CBASS_GLB_EXCEPTION_PEND_SET Register

14.1.5.2.725.1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-2776. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2040h

Figure 14-1381. CBASS_GLB_EXCEPTION_PEND_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PEND_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-2777. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.726 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

14.1.5.2.726.1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-2778. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45B0 2044h

Figure 14-1382. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-2779. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.5.2.727 CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP0 Register

14.1.5.2.727.1 CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP0 Register (Offset = 100h) [reset = 0h]

The Map Register defines the fields for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc per channel.

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Table 14-2780. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 0100h

Figure 14-1383. CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2781. CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.728 CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP1 Register

14.1.5.2.728.1 CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP1 Register (Offset = 104h) [reset = 0h]

The Map Register defines the fields for the initiator Iam275_c7xv_wrap_0_main_0.c7xv_soc per channel.

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Table 14-2782. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 0104h

Figure 14-1384. CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3"></td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-2783. CBASS_QOS_IAM275_C7XV_WRAP_0_MAIN_0_C7XV_SOC_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.729 CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP0 Register

14.1.5.2.729.1 CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP0 Register (Offset = 500h) [reset = 0h]

The Map Register defines the fields for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc per channel.

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Table 14-2784. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 0500h

Figure 14-1385. CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2785. CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.730 CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP1 Register

14.1.5.2.730.1 CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP1 Register (Offset = 504h) [reset = 0h]

The Map Register defines the fields for the initiator Iam275_c7xv_wrap_1_main_0.c7xv_soc per channel.

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Table 14-2786. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 0504h

Figure 14-1386. CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2787. CBASS_QOS_IAM275_C7XV_WRAP_1_MAIN_0_C7XV_SOC_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.731 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_MAP0 Register

14.1.5.2.731.1 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_MAP0 Register (Offset = 900h) [reset = 7000h]

The Map Register defines the fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifr per channel.

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Table 14-2788. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 0900h

Figure 14-1387. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2789. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.732 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_MAP0 Register

14.1.5.2.732.1 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_MAP0 Register (Offset = D00h) [reset = 7000h]

The Map Register defines the fields for the initiator Irl2_of_cba4_main_r5_0_core0.iifw per channel.

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Table 14-2790. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 0D00h

Figure 14-1388. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2791. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE0_IIFW_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.733 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_MAP0 Register

14.1.5.2.733.1 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_MAP0 Register (Offset = 1100h) [reset = 7000h]

The Map Register defines the fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifr per channel.

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Table 14-2792. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 1100h

Figure 14-1389. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2793. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.734 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_MAP0 Register

14.1.5.2.734.1 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_MAP0 Register (Offset = 1500h) [reset = 7000h]

The Map Register defines the fields for the initiator Irl2_of_cba4_main_r5_0_core1.iifw per channel.

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Table 14-2794. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 1500h

Figure 14-1390. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2795. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_0_CORE1_IIFW_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.735 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_MAP0 Register

14.1.5.2.735.1 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_MAP0 Register (Offset = 1900h) [reset = 7000h]

The Map Register defines the fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifr per channel.

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Table 14-2796. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 1900h

Figure 14-1391. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2797. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.736 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_MAP0 Register

14.1.5.2.736.1 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_MAP0 Register (Offset = 1D00h) [reset = 7000h]

The Map Register defines the fields for the initiator Irl2_of_cba4_main_r5_1_core0.iifw per channel.

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Table 14-2798. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 1D00h

Figure 14-1392. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_MAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EPRIORITY</td><td colspan="4">ASEL</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ORDERID</td><td>RESERVED</td><td colspan="3"></td></tr>
<tr><td colspan="4">R/W</td><td>NONE</td><td colspan="3"></td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-2799. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE0_IIFW_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.737 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_MAP0 Register

14.1.5.2.737.1 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_MAP0 Register (Offset = 2100h) [reset = 7000h]

The Map Register defines the fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifr per channel.

Return to Summary Table

Table 14-2800. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 2100h

Figure 14-1393. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2801. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.5.2.738 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_MAP0 Register

14.1.5.2.738.1 CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_MAP0 Register (Offset = 2500h) [reset = 7000h]

The Map Register defines the fields for the initiator Irl2_of_cba4_main_r5_1_core1.iifw per channel.

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Table 14-2802. Instance Table

Instance Name	Physical Address
CBASS_MEM0	45D3 2500h

Figure 14-1394. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-2803. CBASS_QOS_IRL2_OF_CBA4_MAIN_R5_1_CORE1_IIFW_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.6 CBASS_MISC_PERI

CBASS_MISC_PERI

14.1.6.1 CBASS_MISC_PERI Summaries

CBASS_MISC_PERI Summaries

Table 14-2804. CBASS_ERR Registers, Base Address=201F 0000h, Length=1024

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
0h	32	CBASS_ERR_PID	201F 0000h
4h	32	CBASS_ERR_DESTINATION_ID	201F 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	201F 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	201F 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	201F 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	201F 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	201F 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	201F 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	201F 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	201F 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	201F 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	201F 005Ch
60h	32	CBASS_ERR_EOI	201F 0060h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
0h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_CONTROL	4503 0000h
4h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_0	4503 0004h
8h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_1	4503 0008h
Ch	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_2	4503 000Ch
10h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_L	4503 0010h
14h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_H	4503 0014h
18h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_L	4503 0018h
1Ch	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_H	4503 001Ch
400h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_CONTROL	4503 0400h
404h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_0	4503 0404h
408h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_1	4503 0408h
40Ch	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_2	4503 040Ch
410h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_L	4503 0410h
414h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_H	4503 0414h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
418h	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_L	4503 0418h
41Ch	32	CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_H	4503 041Ch
800h	32	CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL	4503 0800h
804h	32	CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0	4503 0804h
808h	32	CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1	4503 0808h
80Ch	32	CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2	4503 080Ch
810h	32	CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L	4503 0810h
814h	32	CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H	4503 0814h
818h	32	CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L	4503 0818h
81Ch	32	CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H	4503 081Ch
C00h	32	CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_CONTROL	4503 0C00h
C04h	32	CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_0	4503 0C04h
C08h	32	CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_1	4503 0C08h
C0Ch	32	CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_2	4503 0C0Ch
C10h	32	CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 0C10h
C14h	32	CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 0C14h
C18h	32	CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 0C18h
C1Ch	32	CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 0C1Ch
1000h	32	CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_CONTROL	4503 1000h
1004h	32	CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_0	4503 1004h
1008h	32	CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_1	4503 1008h
100Ch	32	CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_2	4503 100Ch
1010h	32	CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 1010h
1014h	32	CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 1014h
1018h	32	CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 1018h
101Ch	32	CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 101Ch
1400h	32	CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_CONTROL	4503 1400h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
1404h	32	CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_0	4503 1404h
1408h	32	CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_1	4503 1408h
140Ch	32	CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_2	4503 140Ch
1410h	32	CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 1410h
1414h	32	CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 1414h
1418h	32	CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 1418h
141Ch	32	CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 141Ch
1800h	32	CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_CONTROL	4503 1800h
1804h	32	CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_0	4503 1804h
1808h	32	CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_1	4503 1808h
180Ch	32	CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_2	4503 180Ch
1810h	32	CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 1810h
1814h	32	CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 1814h
1818h	32	CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 1818h
181Ch	32	CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 181Ch
1C00h	32	CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_CONTROL	4503 1C00h
1C04h	32	CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_0	4503 1C04h
1C08h	32	CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_1	4503 1C08h
1C0Ch	32	CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_2	4503 1C0Ch
1C10h	32	CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 1C10h
1C14h	32	CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 1C14h
1C18h	32	CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 1C18h
1C1Ch	32	CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 1C1Ch
2000h	32	CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_CONTROL	4503 2000h
2004h	32	CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_0	4503 2004h
2008h	32	CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_1	4503 2008h
200Ch	32	CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_2	4503 200Ch

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
2010h	32	CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 2010h
2014h	32	CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 2014h
2018h	32	CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 2018h
201Ch	32	CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 201Ch
2400h	32	CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_CONTROL	4503 2400h
2404h	32	CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_0	4503 2404h
2408h	32	CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_1	4503 2408h
240Ch	32	CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_2	4503 240Ch
2410h	32	CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 2410h
2414h	32	CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 2414h
2418h	32	CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 2418h
241Ch	32	CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 241Ch
2800h	32	CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_CONTROL	4503 2800h
2804h	32	CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_0	4503 2804h
2808h	32	CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_1	4503 2808h
280Ch	32	CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_2	4503 280Ch
2810h	32	CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 2810h
2814h	32	CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 2814h
2818h	32	CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 2818h
281Ch	32	CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 281Ch
2C00h	32	CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_CONTROL	4503 2C00h
2C04h	32	CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_0	4503 2C04h
2C08h	32	CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_1	4503 2C08h
2C0Ch	32	CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_2	4503 2C0Ch
2C10h	32	CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 2C10h
2C14h	32	CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 2C14h
2C18h	32	CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 2C18h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
2C1Ch	32	CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 2C1Ch
3000h	32	CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_CONTROL	4503 3000h
3004h	32	CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_0	4503 3004h
3008h	32	CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_1	4503 3008h
300Ch	32	CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_2	4503 300Ch
3010h	32	CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 3010h
3014h	32	CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 3014h
3018h	32	CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 3018h
301Ch	32	CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 301Ch
3400h	32	CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_CONTROL	4503 3400h
3404h	32	CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_0	4503 3404h
3408h	32	CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_1	4503 3408h
340Ch	32	CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_2	4503 340Ch
3410h	32	CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 3410h
3414h	32	CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 3414h
3418h	32	CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 3418h
341Ch	32	CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 341Ch
3800h	32	CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_CONTROL	4503 3800h
3804h	32	CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_0	4503 3804h
3808h	32	CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_1	4503 3808h
380Ch	32	CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_2	4503 380Ch
3810h	32	CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 3810h
3814h	32	CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 3814h
3818h	32	CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 3818h
381Ch	32	CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 381Ch
3C00h	32	CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_CONTROL	4503 3C00h
3C04h	32	CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_0	4503 3C04h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
3C08h	32	CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_1	4503 3C08h
3C0Ch	32	CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_2	4503 3C0Ch
3C10h	32	CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 3C10h
3C14h	32	CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 3C14h
3C18h	32	CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 3C18h
3C1Ch	32	CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 3C1Ch
4000h	32	CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_CONTROL	4503 4000h
4004h	32	CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_0	4503 4004h
4008h	32	CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_1	4503 4008h
400Ch	32	CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_2	4503 400Ch
4010h	32	CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 4010h
4014h	32	CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 4014h
4018h	32	CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 4018h
401Ch	32	CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 401Ch
4400h	32	CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_CONTROL	4503 4400h
4404h	32	CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_0	4503 4404h
4408h	32	CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_1	4503 4408h
440Ch	32	CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_2	4503 440Ch
4410h	32	CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 4410h
4414h	32	CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 4414h
4418h	32	CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 4418h
441Ch	32	CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 441Ch
4800h	32	CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_CONTROL	4503 4800h
4804h	32	CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_0	4503 4804h
4808h	32	CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_1	4503 4808h
480Ch	32	CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_2	4503 480Ch
4810h	32	CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 4810h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
4814h	32	CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 4814h
4818h	32	CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 4818h
481Ch	32	CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 481Ch
4C00h	32	CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_CONTROL	4503 4C00h
4C04h	32	CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0	4503 4C04h
4C08h	32	CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1	4503 4C08h
4C0Ch	32	CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2	4503 4C0Ch
4C10h	32	CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 4C10h
4C14h	32	CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 4C14h
4C18h	32	CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 4C18h
4C1Ch	32	CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 4C1Ch
5000h	32	CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_CONTROL	4503 5000h
5004h	32	CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0	4503 5004h
5008h	32	CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1	4503 5008h
500Ch	32	CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2	4503 500Ch
5010h	32	CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 5010h
5014h	32	CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 5014h
5018h	32	CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 5018h
501Ch	32	CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 501Ch
5400h	32	CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_CONTROL	4503 5400h
5404h	32	CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0	4503 5404h
5408h	32	CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1	4503 5408h
540Ch	32	CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2	4503 540Ch
5410h	32	CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 5410h
5414h	32	CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 5414h
5418h	32	CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 5418h
541Ch	32	CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 541Ch

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
5800h	32	CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_CONTROL	4503 5800h
5804h	32	CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0	4503 5804h
5808h	32	CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1	4503 5808h
580Ch	32	CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2	4503 580Ch
5810h	32	CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 5810h
5814h	32	CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 5814h
5818h	32	CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 5818h
581Ch	32	CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 581Ch
5C00h	32	CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_CONTROL	4503 5C00h
5C04h	32	CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0	4503 5C04h
5C08h	32	CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1	4503 5C08h
5C0Ch	32	CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2	4503 5C0Ch
5C10h	32	CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L	4503 5C10h
5C14h	32	CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H	4503 5C14h
5C18h	32	CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L	4503 5C18h
5C1Ch	32	CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H	4503 5C1Ch
6000h	32	CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL	4503 6000h
6004h	32	CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0	4503 6004h
6008h	32	CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1	4503 6008h
600Ch	32	CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2	4503 600Ch
6010h	32	CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L	4503 6010h
6014h	32	CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H	4503 6014h
6018h	32	CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L	4503 6018h
601Ch	32	CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H	4503 601Ch
6400h	32	CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL	4503 6400h
6404h	32	CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0	4503 6404h
6408h	32	CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1	4503 6408h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
640Ch	32	CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2	4503 640Ch
6410h	32	CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L	4503 6410h
6414h	32	CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H	4503 6414h
6418h	32	CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L	4503 6418h
641Ch	32	CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H	4503 641Ch
6800h	32	CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL	4503 6800h
6804h	32	CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0	4503 6804h
6808h	32	CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1	4503 6808h
680Ch	32	CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2	4503 680Ch
6810h	32	CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L	4503 6810h
6814h	32	CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H	4503 6814h
6818h	32	CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L	4503 6818h
681Ch	32	CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H	4503 681Ch
6C00h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_CONTROL	4503 6C00h
6C04h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_0	4503 6C04h
6C08h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_1	4503 6C08h
6C0Ch	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_2	4503 6C0Ch
6C10h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_L	4503 6C10h
6C14h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_H	4503 6C14h
6C18h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_L	4503 6C18h
6C1Ch	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_H	4503 6C1Ch
7000h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_CONTROL	4503 7000h
7004h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_0	4503 7004h
7008h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_1	4503 7008h
700Ch	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_2	4503 700Ch
7010h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_L	4503 7010h
7014h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_H	4503 7014h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
7018h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_L	4503 7018h
701Ch	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_H	4503 701Ch
7400h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_CONTROL	4503 7400h
7404h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_0	4503 7404h
7408h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_1	4503 7408h
740Ch	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_2	4503 740Ch
7410h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_L	4503 7410h
7414h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_H	4503 7414h
7418h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_L	4503 7418h
741Ch	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_H	4503 741Ch
7800h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_CONTROL	4503 7800h
7804h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_0	4503 7804h
7808h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_1	4503 7808h
780Ch	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_2	4503 780Ch
7810h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_L	4503 7810h
7814h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_H	4503 7814h
7818h	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_L	4503 7818h
781Ch	32	CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_H	4503 781Ch
7C00h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_CONTROL	4503 7C00h
7C04h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_0	4503 7C04h
7C08h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_1	4503 7C08h
7C0Ch	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_2	4503 7C0Ch
7C10h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_L	4503 7C10h
7C14h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_H	4503 7C14h
7C18h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_L	4503 7C18h
7C1Ch	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_H	4503 7C1Ch
8000h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_CONTROL	4503 8000h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
8004h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_0	4503 8004h
8008h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_1	4503 8008h
800Ch	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_2	4503 800Ch
8010h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_L	4503 8010h
8014h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_H	4503 8014h
8018h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_L	4503 8018h
801Ch	32	CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_H	4503 801Ch
8400h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_CONTROL	4503 8400h
8404h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_0	4503 8404h
8408h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_1	4503 8408h
840Ch	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_2	4503 840Ch
8410h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_L	4503 8410h
8414h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_H	4503 8414h
8418h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_L	4503 8418h
841Ch	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_H	4503 841Ch
8800h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_CONTROL	4503 8800h
8804h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_0	4503 8804h
8808h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_1	4503 8808h
880Ch	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_2	4503 880Ch
8810h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_L	4503 8810h
8814h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_H	4503 8814h
8818h	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_L	4503 8818h
881Ch	32	CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_H	4503 881Ch
8C00h	32	CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_CONTROL	4503 8C00h
8C04h	32	CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_0	4503 8C04h
8C08h	32	CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_1	4503 8C08h
8C0Ch	32	CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_2	4503 8C0Ch

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
8C10h	32	CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L	4503 8C10h
8C14h	32	CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H	4503 8C14h
8C18h	32	CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L	4503 8C18h
8C1Ch	32	CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H	4503 8C1Ch
9000h	32	CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_CONTROL	4503 9000h
9004h	32	CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_0	4503 9004h
9008h	32	CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_1	4503 9008h
900Ch	32	CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_2	4503 900Ch
9010h	32	CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L	4503 9010h
9014h	32	CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H	4503 9014h
9018h	32	CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L	4503 9018h
901Ch	32	CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H	4503 901Ch
9400h	32	CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_CONTROL	4503 9400h
9404h	32	CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_0	4503 9404h
9408h	32	CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_1	4503 9408h
940Ch	32	CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_2	4503 940Ch
9410h	32	CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L	4503 9410h
9414h	32	CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H	4503 9414h
9418h	32	CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L	4503 9418h
941Ch	32	CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H	4503 941Ch
9800h	32	CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_CONTROL	4503 9800h
9804h	32	CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_0	4503 9804h
9808h	32	CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_1	4503 9808h
980Ch	32	CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_2	4503 980Ch
9810h	32	CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L	4503 9810h
9814h	32	CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H	4503 9814h
9818h	32	CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L	4503 9818h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
981Ch	32	CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H	4503 981Ch
9C00h	32	CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_CONTROL	4503 9C00h
9C04h	32	CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_0	4503 9C04h
9C08h	32	CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_1	4503 9C08h
9C0Ch	32	CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_2	4503 9C0Ch
9C10h	32	CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L	4503 9C10h
9C14h	32	CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H	4503 9C14h
9C18h	32	CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L	4503 9C18h
9C1Ch	32	CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H	4503 9C1Ch
A000h	32	CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_CONTROL	4503 A000h
A004h	32	CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_0	4503 A004h
A008h	32	CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_1	4503 A008h
A00Ch	32	CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_2	4503 A00Ch
A010h	32	CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L	4503 A010h
A014h	32	CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H	4503 A014h
A018h	32	CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L	4503 A018h
A01Ch	32	CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H	4503 A01Ch
A400h	32	CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_CONTROL	4503 A400h
A404h	32	CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_0	4503 A404h
A408h	32	CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_1	4503 A408h
A40Ch	32	CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_2	4503 A40Ch
A410h	32	CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L	4503 A410h
A414h	32	CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H	4503 A414h
A418h	32	CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L	4503 A418h
A41Ch	32	CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H	4503 A41Ch
A800h	32	CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_CONTROL	4503 A800h
A804h	32	CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_0	4503 A804h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
A808h	32	CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_1	4503 A808h
A80Ch	32	CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_2	4503 A80Ch
A810h	32	CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L	4503 A810h
A814h	32	CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H	4503 A814h
A818h	32	CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L	4503 A818h
A81Ch	32	CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H	4503 A81Ch
AC00h	32	CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_CONTROL	4503 AC00h
AC04h	32	CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_0	4503 AC04h
AC08h	32	CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_1	4503 AC08h
AC0Ch	32	CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_2	4503 AC0Ch
AC10h	32	CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L	4503 AC10h
AC14h	32	CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H	4503 AC14h
AC18h	32	CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L	4503 AC18h
AC1Ch	32	CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H	4503 AC1Ch
B000h	32	CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_CONTROL	4503 B000h
B004h	32	CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_0	4503 B004h
B008h	32	CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_1	4503 B008h
B00Ch	32	CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_2	4503 B00Ch
B010h	32	CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L	4503 B010h
B014h	32	CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H	4503 B014h
B018h	32	CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L	4503 B018h
B01Ch	32	CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H	4503 B01Ch
B400h	32	CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_CONTROL	4503 B400h
B404h	32	CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_0	4503 B404h
B408h	32	CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_1	4503 B408h
B40Ch	32	CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_2	4503 B40Ch
B410h	32	CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L	4503 B410h

Table 14-2805. CBASS_FW Registers, Base Address=4503 0000h, Length=65536 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
B414h	32	CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H	4503 B414h
B418h	32	CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L	4503 B418h
B41Ch	32	CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H	4503 B41Ch
B800h	32	CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_CONTROL	4503 B800h
B804h	32	CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_0	4503 B804h
B808h	32	CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_1	4503 B808h
B80Ch	32	CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_2	4503 B80Ch
B810h	32	CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L	4503 B810h
B814h	32	CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H	4503 B814h
B818h	32	CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L	4503 B818h
B81Ch	32	CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H	4503 B81Ch
BC00h	32	CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL	4503 BC00h
BC04h	32	CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0	4503 BC04h
BC08h	32	CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1	4503 BC08h
BC0Ch	32	CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2	4503 BC0Ch
BC10h	32	CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L	4503 BC10h
BC14h	32	CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H	4503 BC14h
BC18h	32	CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L	4503 BC18h
BC1Ch	32	CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H	4503 BC1Ch

Table 14-2806. CBASS_ISC Registers, Base Address=4584 0000h, Length=4096

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
0h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL	4584 0000h
10h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L	4584 0010h
14h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H	4584 0014h
18h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L	4584 0018h
1Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H	4584 001Ch

Table 14-2806. CBASS_ISC Registers, Base Address=4584 0000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
20h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_CONTROL	4584 0020h
30h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L	4584 0030h
34h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H	4584 0034h
38h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L	4584 0038h
3Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H	4584 003Ch
40h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_CONTROL	4584 0040h
50h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L	4584 0050h
54h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H	4584 0054h
58h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L	4584 0058h
5Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H	4584 005Ch
60h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_CONTROL	4584 0060h
70h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L	4584 0070h
74h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H	4584 0074h
78h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L	4584 0078h
7Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H	4584 007Ch
80h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL	4584 0080h
400h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL	4584 0400h
410h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L	4584 0410h
414h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H	4584 0414h
418h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L	4584 0418h
41Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H	4584 041Ch
420h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_CONTROL	4584 0420h
430h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L	4584 0430h
434h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H	4584 0434h
438h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L	4584 0438h
43Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H	4584 043Ch
440h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_CONTROL	4584 0440h

Table 14-2806. CBASS_ISC Registers, Base Address=4584 0000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
450h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L	4584 0450h
454h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H	4584 0454h
458h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L	4584 0458h
45Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H	4584 045Ch
460h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_CONTROL	4584 0460h
470h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L	4584 0470h
474h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H	4584 0474h
478h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L	4584 0478h
47Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H	4584 047Ch
480h	32	CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL	4584 0480h
800h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL	4584 0800h
810h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L	4584 0810h
814h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H	4584 0814h
818h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L	4584 0818h
81Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H	4584 081Ch
820h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_CONTROL	4584 0820h
830h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L	4584 0830h
834h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H	4584 0834h
838h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L	4584 0838h
83Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H	4584 083Ch
840h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_CONTROL	4584 0840h
850h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L	4584 0850h
854h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H	4584 0854h
858h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L	4584 0858h
85Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H	4584 085Ch
860h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_CONTROL	4584 0860h
870h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L	4584 0870h

Table 14-2806. CBASS_ISC Registers, Base Address=4584 0000h, Length=4096 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
874h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H	4584 0874h
878h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L	4584 0878h
87Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H	4584 087Ch
880h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL	4584 0880h
C00h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL	4584 0C00h
C10h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L	4584 0C10h
C14h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H	4584 0C14h
C18h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L	4584 0C18h
C1Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H	4584 0C1Ch
C20h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_CONTROL	4584 0C20h
C30h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L	4584 0C30h
C34h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H	4584 0C34h
C38h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L	4584 0C38h
C3Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H	4584 0C3Ch
C40h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_CONTROL	4584 0C40h
C50h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L	4584 0C50h
C54h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H	4584 0C54h
C58h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L	4584 0C58h
C5Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H	4584 0C5Ch
C60h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_CONTROL	4584 0C60h
C70h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L	4584 0C70h
C74h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H	4584 0C74h
C78h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L	4584 0C78h
C7Ch	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H	4584 0C7Ch
C80h	32	CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL	4584 0C80h

Table 14-2807. CBASS_GLB Registers, Base Address=45B0 A000h, Length=1024

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
0h	32	CBASS_GLB_PID	45B0 A000h

Table 14-2807. CBASS_GLB Registers, Base Address=45B0 A000h, Length=1024 (continued)

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
4h	32	CBASS_GLB_DESTINATION_ID	45B0 A004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 A020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 A024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 A028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 A02Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 A030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 A034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 A038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 A040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 A044h

Table 14-2808. CBASS_QOS Registers, Base Address=45D4 0000h, Length=4096

Offset	Length	Register Name	CBASS_MISC_PERI0 Physical Address
100h	32	CBASS_QOS_IPULSAR_SL_MAIN_0_CPU0_PMST_MAP0	45D4 0100h
500h	32	CBASS_QOS_IPULSAR_SL_MAIN_0_CPU1_PMST_MAP0	45D4 0500h
900h	32	CBASS_QOS_IPULSAR_SL_MAIN_1_CPU0_PMST_MAP0	45D4 0900h
D00h	32	CBASS_QOS_IPULSAR_SL_MAIN_1_CPU1_PMST_MAP0	45D4 0D00h

14.1.6.2 CBASS_MISC_PERI Registers

CBASS_MISC_PERI Registers

14.1.6.2.1 CBASS_ERR_PID Register

14.1.6.2.1.1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66005102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-2809. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0000h

Figure 14-1395. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Ah					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-2810. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:11	RTL	R	Ah	RTL revision. Will vary depending on release. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.2 CBASS_ERR_DESTINATION_ID Register

14.1.6.2.2.1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-2811. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0004h

Figure 14-1396. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-2812. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

14.1.6.2.3.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-2813. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0024h

Figure 14-1397. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TYPE_F</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2814. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

14.1.6.2.4.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-2815. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0028h

Figure 14-1398. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-2816. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.6.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

14.1.6.2.5.1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-2817. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 002Ch

Figure 14-1399. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDR_L							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDR_L							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR_L							
R							
0h							

Table 14-2818. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

14.1.6.2.6.1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-2819. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0030h

Figure 14-1400. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-2820. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

14.1.6.2.7.1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-2821. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0034h

Figure 14-1401. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-2822. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

14.1.6.2.8.1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-2823. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0038h

Figure 14-1402. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-2824. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

14.1.6.2.9.1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-2825. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0050h

Figure 14-1403. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-2826. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

14.1.6.2.10.1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-2827. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0054h

Figure 14-1404. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-2828. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

14.1.6.2.11.1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-2829. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0058h

Figure 14-1405. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-2830. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

14.1.6.2.12.1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-2831. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 005Ch

Figure 14-1406. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-2832. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.13 CBASS_ERR_EOI Register

14.1.6.2.13.1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-2833. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	201F 0060h

Figure 14-1407. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-2834. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_32_CLK4_rst_mod_g_rst_n

14.1.6.2.14 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_CONTROL Register

14.1.6.2.14.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iadc12fc_16ffc_main_0.cba0_cfg region 0 firewall.

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Table 14-2835. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0000h

Figure 14-1408. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2836. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.15 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.15.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iadc12fc_16ffc_main_0.cba0_cfg region 0 firewall.

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Table 14-2837. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0004h

Figure 14-1409. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2838. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2838. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.16 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.16.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iadc12fc_16ffc_main_0.cba0_cfg region 0 firewall.

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Table 14-2839. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0008h

Figure 14-1410. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2840. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2840. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.17 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.17.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iadc12fc_16ffc_main_0.cba0_cfg region 0 firewall.

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Table 14-2841. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 000Ch

Figure 14-1411. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2842. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2842. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.18 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.18.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 20600000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iadc12fc_16ffc_main_0.cba0_cfg region 0 firewall.

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Table 14-2843. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0010h

Figure 14-1412. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20600h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20600h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20600h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2844. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20600h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.19 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.19.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iadc12fc_16ffc_main_0.cba0_cfg region 0 firewall.

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Table 14-2845. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0014h

Figure 14-1413. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2846. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.20 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.20.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 20600FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iadc12fc_16ffc_main_0.cba0_cfg region 0 firewall.

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Table 14-2847. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0018h

Figure 14-1414. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20600h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20600h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20600h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2848. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20600h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.21 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.21.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iadc12fc_16ffc_main_0.cba0_cfg region 0 firewall.

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Table 14-2849. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 001Ch

Figure 14-1415. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2850. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA0_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.22 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_CONTROL Register

14.1.6.2.22.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_CONTROL Register (Offset = 400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iadc12fc_16ffc_main_0.cba1_dma region 0 firewall.

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Table 14-2851. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0400h

Figure 14-1416. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2852. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.23 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.23.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_0 Register (Offset = 404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iadc12fc_16ffc_main_0.cba1_dma region 0 firewall.

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Table 14-2853. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0404h

Figure 14-1417. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2854. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2854. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.24 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.24.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_1 Register (Offset = 408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iadc12fc_16ffc_main_0.cba1_dma region 0 firewall.

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Table 14-2855. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0408h

Figure 14-1418. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2856. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2856. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.25 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.25.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_2 Register (Offset = 40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iadc12fc_16ffc_main_0.cba1_dma region 0 firewall.

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Table 14-2857. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 040Ch

Figure 14-1419. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-2858. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2858. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.26 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.26.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 20608000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iadc12fc_16ffc_main_0.cba1_dma region 0 firewall.

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Table 14-2859. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0410h

Figure 14-1420. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20608h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20608h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20608h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2860. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20608h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.27 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.27.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iadc12fc_16ffc_main_0.cba1_dma region 0 firewall.

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Table 14-2861. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0414h

Figure 14-1421. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2862. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.28 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.28.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = 20608FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iadc12fc_16ffc_main_0.cba1_dma region 0 firewall.

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Table 14-2863. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0418h

Figure 14-1422. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20608h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20608h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20608h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2864. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20608h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.29 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.29.1 CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iadc12fc_16ffc_main_0.cba1_dma region 0 firewall.

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Table 14-2865. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 041Ch

Figure 14-1423. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2866. CBASS_FW_IADC12FC_16FFC_MAIN_0_CBA1_DMA_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.30 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.30.1 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL Register (Offset = 800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iam275_main_mem_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-2867. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0800h

Figure 14-1424. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2868. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.31 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.31.1

CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iam275_main_mem_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-2869. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0804h

Figure 14-1425. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2870. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2870. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.32 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.32.1 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iam275_main_mem_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-2871. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0808h

Figure 14-1426. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2872. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2872. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.33 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.33.1

CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 80Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iam275_main_mem_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-2873. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 080Ch

Figure 14-1427. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2874. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2874. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.34 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.34.1 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 20200000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_main_mem_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-2875. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0810h

Figure 14-1428. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20200h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
20200h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20200h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2876. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20200h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.35 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.35.1 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_main_mem_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-2877. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0814h

Figure 14-1429. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2878. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.36 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.36.1 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = 20200FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_main_mem_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-2879. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0818h

Figure 14-1430. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20200h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20200h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20200h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2880. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20200h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.37 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.37.1 CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_main_mem_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-2881. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 081Ch

Figure 14-1431. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2882. CBASS_FW_IAM275_MAIN_MEM_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.38 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.38.1 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_CONTROL Register (Offset = C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iecap_main_0.ecap_vbusp region 0 firewall.

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Table 14-2883. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0C00h

Figure 14-1432. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2884. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.39 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.39.1 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iecap_main_0.ecap_vbusp region 0 firewall.

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Table 14-2885. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0C04h

Figure 14-1433. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2886. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2886. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.40 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.40.1 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iecap_main_0.ecap_vbusp region 0 firewall.

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Table 14-2887. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0C08h

Figure 14-1434. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2888. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2888. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.41 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.41.1 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iecap_main_0.ecap_vbusp region 0 firewall.

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Table 14-2889. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0C0Ch

Figure 14-1435. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2890. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2890. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.42 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.42.1 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 23100000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iecap_main_0.ecap_vbusp region 0 firewall.

Return to Summary Table

Table 14-2891. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0C10h

Figure 14-1436. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23100h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23100h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">23100h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2892. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23100h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.43 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.43.1 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iecap_main_0.ecap_vbusp region 0 firewall.

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Table 14-2893. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0C14h

Figure 14-1437. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2894. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.44 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.44.1 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = 23100FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iecap_main_0.ecap_vbusp region 0 firewall.

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Table 14-2895. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0C18h

Figure 14-1438. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
23100h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
23100h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
23100h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2896. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23100h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.45 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.45.1 CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iecap_main_0.ecap_vbusp region 0 firewall.

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Table 14-2897. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 0C1Ch

Figure 14-1439. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2898. CBASS_FW_IECAP_MAIN_0_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.46 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.46.1 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_CONTROL Register (Offset = 1000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iecap_main_1.ecap_vbusp region 0 firewall.

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Table 14-2899. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1000h

Figure 14-1440. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2900. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.47 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.47.1 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 1004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iecap_main_1.ecap_vbusp region 0 firewall.

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Table 14-2901. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1004h

Figure 14-1441. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2902. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2902. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.48 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.48.1 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 1008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iecap_main_1.ecap_vbusp region 0 firewall.

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Table 14-2903. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1008h

Figure 14-1442. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2904. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2904. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.49 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.49.1 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 100Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iecap_main_1.ecap_vbusp region 0 firewall.

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Table 14-2905. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 100Ch

Figure 14-1443. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2906. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2906. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.50 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.50.1 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 1010h) [reset = 23110000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iecap_main_1.ecap_vbusp region 0 firewall.

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Table 14-2907. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1010h

Figure 14-1444. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
23110h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
23110h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
23110h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2908. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23110h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.51 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.51.1 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 1014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iecap_main_1.ecap_vbusp region 0 firewall.

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Table 14-2909. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1014h

Figure 14-1445. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2910. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.52 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.52.1 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 1018h) [reset = 23110FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iecap_main_1.ecap_vbusp region 0 firewall.

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Table 14-2911. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1018h

Figure 14-1446. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23110h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23110h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">23110h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2912. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23110h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.53 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.53.1 CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 101Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iecap_main_1.ecap_vbusp region 0 firewall.

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Table 14-2913. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 101Ch

Figure 14-1447. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2914. CBASS_FW_IECAP_MAIN_1_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.54 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.54.1 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_CONTROL Register (Offset = 1400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iecap_main_2.ecap_vbusp region 0 firewall.

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Table 14-2915. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1400h

Figure 14-1448. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2916. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.55 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.55.1 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 1404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iecap_main_2.ecap_vbusp region 0 firewall.

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Table 14-2917. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1404h

Figure 14-1449. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2918. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2918. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.56 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.56.1 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 1408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iecap_main_2.ecap_vbusp region 0 firewall.

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Table 14-2919. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1408h

Figure 14-1450. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2920. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2920. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.57 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.57.1 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 140Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iecap_main_2.ecap_vbusp region 0 firewall.

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Table 14-2921. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 140Ch

Figure 14-1451. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2922. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2922. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.58 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.58.1 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 1410h) [reset = 23120000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iecap_main_2.ecap_vbusp region 0 firewall.

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Table 14-2923. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1410h

Figure 14-1452. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23120h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23120h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">23120h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2924. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23120h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.59 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.59.1 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 1414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iecap_main_2.ecap_vbusp region 0 firewall.

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Table 14-2925. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1414h

Figure 14-1453. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2926. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.60 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.60.1 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 1418h) [reset = 23120FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iecap_main_2.ecap_vbusp region 0 firewall.

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Table 14-2927. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1418h

Figure 14-1454. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
23120h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
23120h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
23120h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2928. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23120h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.61 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.61.1 CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 141Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iecap_main_2.ecap_vbusp region 0 firewall.

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Table 14-2929. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 141Ch

Figure 14-1455. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2930. CBASS_FW_IECAP_MAIN_2_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.62 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.62.1 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_CONTROL Register (Offset = 1800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iecap_main_3.ecap_vbusp region 0 firewall.

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Table 14-2931. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1800h

Figure 14-1456. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2932. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.63 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.63.1 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 1804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iecap_main_3.ecap_vbusp region 0 firewall.

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Table 14-2933. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1804h

Figure 14-1457. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2934. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2934. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.64 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.64.1 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 1808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iecap_main_3.ecap_vbusp region 0 firewall.

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Table 14-2935. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1808h

Figure 14-1458. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2936. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2936. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.65 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.65.1 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 180Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iecap_main_3.ecap_vbusp region 0 firewall.

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Table 14-2937. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 180Ch

Figure 14-1459. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2938. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2938. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.66 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.66.1 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 1810h) [reset = 23130000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iecap_main_3.ecap_vbusp region 0 firewall.

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Table 14-2939. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1810h

Figure 14-1460. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
23130h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
23130h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
23130h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-2940. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23130h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.67 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.67.1 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 1814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iecap_main_3.ecap_vbusp region 0 firewall.

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Table 14-2941. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1814h

Figure 14-1461. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2942. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.68 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.68.1 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 1818h) [reset = 23130FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iecap_main_3.ecap_vbusp region 0 firewall.

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Table 14-2943. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1818h

Figure 14-1462. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
23130h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
23130h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
23130h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-2944. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23130h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.69 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.69.1 CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 181Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iecap_main_3.ecap_vbusp region 0 firewall.

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Table 14-2945. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 181Ch

Figure 14-1463. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2946. CBASS_FW_IECAP_MAIN_3_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.70 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.70.1 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_CONTROL Register (Offset = 1C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iecap_main_4.ecap_vbusp region 0 firewall.

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Table 14-2947. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1C00h

Figure 14-1464. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-2948. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.71 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.71.1 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 1C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iecap_main_4.ecap_vbusp region 0 firewall.

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Table 14-2949. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1C04h

Figure 14-1465. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2950. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2950. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.72 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.72.1 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 1C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iecap_main_4.ecap_vbusp region 0 firewall.

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Table 14-2951. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1C08h

Figure 14-1466. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2952. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2952. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.73 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.73.1 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 1C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iecap_main_4.ecap_vbusp region 0 firewall.

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Table 14-2953. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1C0Ch

Figure 14-1467. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2954. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2954. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.74 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.74.1 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 1C10h) [reset = 23140000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iecap_main_4.ecap_vbusp region 0 firewall.

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Table 14-2955. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1C10h

Figure 14-1468. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23140h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23140h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">23140h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2956. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23140h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.75 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.75.1 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 1C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iecap_main_4.ecap_vbusp region 0 firewall.

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Table 14-2957. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1C14h

Figure 14-1469. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2958. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.76 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.76.1 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 1C18h) [reset = 23140FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iecap_main_4.ecap_vbusp region 0 firewall.

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Table 14-2959. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1C18h

Figure 14-1470. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23140h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23140h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">23140h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2960. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23140h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.77 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.77.1 CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 1C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iecap_main_4.ecap_vbusp region 0 firewall.

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Table 14-2961. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 1C1Ch

Figure 14-1471. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2962. CBASS_FW_IECAP_MAIN_4_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.78 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.78.1 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_CONTROL Register (Offset = 2000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iecap_main_5.ecap_vbusp region 0 firewall.

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Table 14-2963. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2000h

Figure 14-1472. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2964. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.79 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.79.1 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 2004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iecap_main_5.ecap_vbusp region 0 firewall.

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Table 14-2965. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2004h

Figure 14-1473. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2966. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2966. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.80 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.80.1 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 2008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iecap_main_5.ecap_vbusp region 0 firewall.

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Table 14-2967. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2008h

Figure 14-1474. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2968. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2968. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.81 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.81.1 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 200Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iecap_main_5.ecap_vbusp region 0 firewall.

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Table 14-2969. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 200Ch

Figure 14-1475. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2970. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2970. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.82 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.82.1 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 2010h) [reset = 23150000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iecap_main_5.ecap_vbusp region 0 firewall.

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Table 14-2971. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2010h

Figure 14-1476. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
23150h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
23150h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
23150h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-2972. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23150h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.83 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.83.1 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 2014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iecap_main_5.ecap_vbusp region 0 firewall.

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Table 14-2973. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2014h

Figure 14-1477. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2974. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.84 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.84.1 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 2018h) [reset = 23150FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iecap_main_5.ecap_vbusp region 0 firewall.

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Table 14-2975. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2018h

Figure 14-1478. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23150h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23150h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">23150h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2976. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23150h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.85 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.85.1 CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 201Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iecap_main_5.ecap_vbusp region 0 firewall.

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Table 14-2977. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 201Ch

Figure 14-1479. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2978. CBASS_FW_IECAP_MAIN_5_ECAP_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.86 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.86.1 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_CONTROL Register (Offset = 2400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ik3_epwm_main_0.epwm_vbusp region 0 firewall.

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Table 14-2979. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2400h

Figure 14-1480. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2980. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.87 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.87.1 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 2404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ik3_epwm_main_0.epwm_vbusp region 0 firewall.

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Table 14-2981. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2404h

Figure 14-1481. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2982. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2982. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.88 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.88.1 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 2408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ik3_epwm_main_0.epwm_vbusp region 0 firewall.

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Table 14-2983. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2408h

Figure 14-1482. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2984. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2984. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.89 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.89.1 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 240Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ik3_epwm_main_0.epwm_vbusp region 0 firewall.

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Table 14-2985. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 240Ch

Figure 14-1483. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2986. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2986. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.90 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.90.1 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 2410h) [reset = 23000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ik3_epwm_main_0.epwm_vbusp region 0 firewall.

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Table 14-2987. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2410h

Figure 14-1484. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">23000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-2988. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.91 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.91.1 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 2414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ik3_epwm_main_0.epwm_vbusp region 0 firewall.

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Table 14-2989. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2414h

Figure 14-1485. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-2990. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.92 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.92.1 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 2418h) [reset = 23000FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ik3_epwm_main_0.epwm_vbusp region 0 firewall.

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Table 14-2991. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2418h

Figure 14-1486. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">23000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">23000h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-2992. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23000h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.93 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.93.1 CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 241Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ik3_epwm_main_0.epwm_vbusp region 0 firewall.

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Table 14-2993. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 241Ch

Figure 14-1487. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-2994. CBASS_FW_IK3_EPWM_MAIN_0_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.94 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.94.1 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_CONTROL Register (Offset = 2800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ik3_epwm_main_1.epwm_vbusp region 0 firewall.

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Table 14-2995. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2800h

Figure 14-1488. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-2996. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.95 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.95.1 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 2804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ik3_epwm_main_1.epwm_vbusp region 0 firewall.

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Table 14-2997. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2804h

Figure 14-1489. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-2998. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-2998. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.96 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.96.1 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 2808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ik3_epwm_main_1.epwm_vbusp region 0 firewall.

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Table 14-2999. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2808h

Figure 14-1490. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3000. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3000. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.97 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.97.1 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 280Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ik3_epwm_main_1.epwm_vbusp region 0 firewall.

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Table 14-3001. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 280Ch

Figure 14-1491. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3002. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3002. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.98 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.98.1 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 2810h) [reset = 23010000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ik3_epwm_main_1.epwm_vbusp region 0 firewall.

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Table 14-3003. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2810h

Figure 14-1492. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
23010h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
23010h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
23010h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3004. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23010h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.99 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.99.1 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 2814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ik3_epwm_main_1.epwm_vbusp region 0 firewall.

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Table 14-3005. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2814h

Figure 14-1493. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3006. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.100 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.100.1 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 2818h) [reset = 23010FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ik3_epwm_main_1.epwm_vbusp region 0 firewall.

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Table 14-3007. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2818h

Figure 14-1494. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
23010h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
23010h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
23010h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3008. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23010h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.101 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.101.1 CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 281Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ik3_epwm_main_1.epwm_vbusp region 0 firewall.

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Table 14-3009. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 281Ch

Figure 14-1495. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3010. CBASS_FW_IK3_EPWM_MAIN_1_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.102 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.102.1 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_CONTROL Register (Offset = 2C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ik3_epwm_main_2.epwm_vbusp region 0 firewall.

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Table 14-3011. Instance Table

Instance Name	**Physical Address**
CBASS_MISC_PERI0	4503 2C00h

Figure 14-1496. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3012. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.103 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.103.1 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 2C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ik3_epwm_main_2.epwm_vbusp region 0 firewall.

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Table 14-3013. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2C04h

Figure 14-1497. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3014. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3014. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.104 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.104.1 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 2C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ik3_epwm_main_2.epwm_vbusp region 0 firewall.

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Table 14-3015. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2C08h

Figure 14-1498. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3016. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3016. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.105 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.105.1 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 2C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ik3_epwm_main_2.epwm_vbusp region 0 firewall.

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Table 14-3017. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2C0Ch

Figure 14-1499. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3018. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3018. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.106 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.106.1 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 2C10h) [reset = 23020000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ik3_epwm_main_2.epwm_vbusp region 0 firewall.

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Table 14-3019. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2C10h

Figure 14-1500. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
23020h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
23020h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
23020h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3020. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	23020h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.107 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.107.1 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 2C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ik3_epwm_main_2.epwm_vbusp region 0 firewall.

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Table 14-3021. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2C14h

Figure 14-1501. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3022. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.108 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.108.1 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 2C18h) [reset = 23020FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ik3_epwm_main_2.epwm_vbusp region 0 firewall.

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Table 14-3023. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2C18h

Figure 14-1502. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
23020h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
23020h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
23020h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3024. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	23020h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.109 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.109.1 CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 2C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ik3_epwm_main_2.epwm_vbusp region 0 firewall.

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Table 14-3025. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 2C1Ch

Figure 14-1503. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3026. CBASS_FW_IK3_EPWM_MAIN_2_EPWM_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.110 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.110.1 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_CONTROL Register (Offset = 3000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imshsi2c_main_0.vbusp region 0 firewall.

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Table 14-3027. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3000h

Figure 14-1504. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3028. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.111 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.111.1 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 3004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imshsi2c_main_0.vbusp region 0 firewall.

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Table 14-3029. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3004h

Figure 14-1505. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3030. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3030. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.112 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.112.1 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 3008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imshsi2c_main_0.vbusp region 0 firewall.

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Table 14-3031. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3008h

Figure 14-1506. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3032. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3032. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.113 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.113.1 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 300Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imshsi2c_main_0.vbusp region 0 firewall.

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Table 14-3033. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 300Ch

Figure 14-1507. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3034. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3034. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.114 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.114.1 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 3010h) [reset = 20000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imshsi2c_main_0.vbusp region 0 firewall.

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Table 14-3035. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3010h

Figure 14-1508. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3036. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.115 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.115.1 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 3014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imshsi2c_main_0.vbusp region 0 firewall.

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Table 14-3037. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3014h

Figure 14-1509. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3038. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.116 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.116.1 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 3018h) [reset = 20000FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imshsi2c_main_0.vbusp region 0 firewall.

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Table 14-3039. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3018h

Figure 14-1510. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20000h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20000h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20000h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3040. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20000h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.117 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.117.1 CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 301Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imshsi2c_main_0.vbusp region 0 firewall.

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Table 14-3041. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 301Ch

Figure 14-1511. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3042. CBASS_FW_IMSHSI2C_MAIN_0_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.118 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.118.1 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_CONTROL Register (Offset = 3400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imshsi2c_main_1.vbusp region 0 firewall.

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Table 14-3043. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3400h

Figure 14-1512. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3044. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.119 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.119.1 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 3404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imshsi2c_main_1.vbusp region 0 firewall.

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Table 14-3045. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3404h

Figure 14-1513. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3046. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3046. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.120 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.120.1 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 3408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imshsi2c_main_1.vbusp region 0 firewall.

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Table 14-3047. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3408h

Figure 14-1514. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3048. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3048. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.121 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.121.1 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 340Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imshsi2c_main_1.vbusp region 0 firewall.

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Table 14-3049. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 340Ch

Figure 14-1515. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3050. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3050. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.122 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.122.1 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 3410h) [reset = 20010000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imshsi2c_main_1.vbusp region 0 firewall.

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Table 14-3051. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3410h

Figure 14-1516. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20010h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20010h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20010h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3052. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20010h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.123 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.123.1 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 3414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imshsi2c_main_1.vbusp region 0 firewall.

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Table 14-3053. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3414h

Figure 14-1517. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3054. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.124 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.124.1 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 3418h) [reset = 20010FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imshsi2c_main_1.vbusp region 0 firewall.

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Table 14-3055. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3418h

Figure 14-1518. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20010h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20010h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20010h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3056. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20010h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.125 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.125.1 CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 341Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imshsi2c_main_1.vbusp region 0 firewall.

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Table 14-3057. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 341Ch

Figure 14-1519. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3058. CBASS_FW_IMSHSI2C_MAIN_1_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.126 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.126.1 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_CONTROL Register (Offset = 3800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imshsi2c_main_2.vbusp region 0 firewall.

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Table 14-3059. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3800h

Figure 14-1520. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3060. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.127 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.127.1 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 3804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imshsi2c_main_2.vbusp region 0 firewall.

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Table 14-3061. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3804h

Figure 14-1521. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3062. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3062. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.128 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.128.1 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 3808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imshsi2c_main_2.vbusp region 0 firewall.

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Table 14-3063. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3808h

Figure 14-1522. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3064. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3064. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.129 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.129.1 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 380Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imshsi2c_main_2.vbusp region 0 firewall.

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Table 14-3065. Instance Table

Instance Name	**Physical Address**
CBASS_MISC_PERI0	4503 380Ch

Figure 14-1523. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3066. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3066. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.130 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.130.1 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 3810h) [reset = 20020000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imshsi2c_main_2.vbusp region 0 firewall.

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Table 14-3067. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3810h

Figure 14-1524. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20020h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20020h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20020h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3068. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20020h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.131 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.131.1 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 3814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imshsi2c_main_2.vbusp region 0 firewall.

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Table 14-3069. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3814h

Figure 14-1525. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3070. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.132 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.132.1 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 3818h) [reset = 20020FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imshsi2c_main_2.vbusp region 0 firewall.

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Table 14-3071. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3818h

Figure 14-1526. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20020h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20020h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20020h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3072. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20020h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.133 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.133.1 CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 381Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imshsi2c_main_2.vbusp region 0 firewall.

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Table 14-3073. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 381Ch

Figure 14-1527. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3074. CBASS_FW_IMSHSI2C_MAIN_2_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.134 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.134.1 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_CONTROL Register (Offset = 3C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imshsi2c_main_3.vbusp region 0 firewall.

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Table 14-3075. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3C00h

Figure 14-1528. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3076. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.135 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.135.1 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 3C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imshsi2c_main_3.vbusp region 0 firewall.

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Table 14-3077. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3C04h

Figure 14-1529. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3078. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3078. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.136 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.136.1 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 3C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imshsi2c_main_3.vbusp region 0 firewall.

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Table 14-3079. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3C08h

Figure 14-1530. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3080. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3080. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.137 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.137.1 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 3C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imshsi2c_main_3.vbusp region 0 firewall.

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Table 14-3081. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3C0Ch

Figure 14-1531. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3082. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3082. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.138 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.138.1 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 3C10h) [reset = 20030000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imshsi2c_main_3.vbusp region 0 firewall.

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Table 14-3083. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3C10h

Figure 14-1532. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20030h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
20030h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20030h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3084. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20030h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.139 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.139.1 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 3C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imshsi2c_main_3.vbusp region 0 firewall.

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Table 14-3085. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3C14h

Figure 14-1533. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3086. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.140 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.140.1 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 3C18h) [reset = 20030FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imshsi2c_main_3.vbusp region 0 firewall.

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Table 14-3087. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3C18h

Figure 14-1534. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20030h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20030h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20030h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3088. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20030h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.141 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.141.1 CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 3C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imshsi2c_main_3.vbusp region 0 firewall.

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Table 14-3089. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 3C1Ch

Figure 14-1535. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3090. CBASS_FW_IMSHSI2C_MAIN_3_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.142 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.142.1 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_CONTROL Register (Offset = 4000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imshsi2c_main_4.vbusp region 0 firewall.

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Table 14-3091. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4000h

Figure 14-1536. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3092. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.143 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.143.1 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 4004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imshsi2c_main_4.vbusp region 0 firewall.

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Table 14-3093. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4004h

Figure 14-1537. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3094. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3094. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.144 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.144.1 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 4008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imshsi2c_main_4.vbusp region 0 firewall.

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Table 14-3095. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4008h

Figure 14-1538. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3096. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3096. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.145 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.145.1 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 400Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imshsi2c_main_4.vbusp region 0 firewall.

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Table 14-3097. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 400Ch

Figure 14-1539. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3098. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3098. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.146 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.146.1 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 4010h) [reset = 20040000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imshsi2c_main_4.vbusp region 0 firewall.

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Table 14-3099. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4010h

Figure 14-1540. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20040h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20040h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20040h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3100. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20040h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.147 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.147.1 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 4014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imshsi2c_main_4.vbusp region 0 firewall.

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Table 14-3101. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4014h

Figure 14-1541. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3102. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.148 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.148.1 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 4018h) [reset = 20040FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imshsi2c_main_4.vbusp region 0 firewall.

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Table 14-3103. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4018h

Figure 14-1542. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20040h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20040h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20040h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3104. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20040h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.149 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.149.1 CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 401Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imshsi2c_main_4.vbusp region 0 firewall.

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Table 14-3105. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 401Ch

Figure 14-1543. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3106. CBASS_FW_IMSHSI2C_MAIN_4_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.150 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.150.1 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_CONTROL Register (Offset = 4400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imshsi2c_main_5.vbusp region 0 firewall.

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Table 14-3107. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4400h

Figure 14-1544. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3108. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.151 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.151.1 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 4404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imshsi2c_main_5.vbusp region 0 firewall.

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Table 14-3109. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4404h

Figure 14-1545. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3110. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3110. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.152 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.152.1 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 4408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imshsi2c_main_5.vbusp region 0 firewall.

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Table 14-3111. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4408h

Figure 14-1546. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3112. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3112. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.153 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.153.1 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 440Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imshsi2c_main_5.vbusp region 0 firewall.

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Table 14-3113. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 440Ch

Figure 14-1547. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3114. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3114. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.154 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.154.1 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 4410h) [reset = 20050000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imshsi2c_main_5.vbusp region 0 firewall.

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Table 14-3115. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4410h

Figure 14-1548. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20050h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20050h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20050h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3116. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20050h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.155 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.155.1 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 4414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imshsi2c_main_5.vbusp region 0 firewall.

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Table 14-3117. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4414h

Figure 14-1549. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3118. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.156 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.156.1 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 4418h) [reset = 20050FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imshsi2c_main_5.vbusp region 0 firewall.

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Table 14-3119. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4418h

Figure 14-1550. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20050h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
20050h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20050h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3120. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20050h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.157 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.157.1 CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 441Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imshsi2c_main_5.vbusp region 0 firewall.

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Table 14-3121. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 441Ch

Figure 14-1551. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3122. CBASS_FW_IMSHSI2C_MAIN_5_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.158 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.158.1 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_CONTROL Register (Offset = 4800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imshsi2c_main_6.vbusp region 0 firewall.

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Table 14-3123. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4800h

Figure 14-1552. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3124. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.159 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.159.1 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 4804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imshsi2c_main_6.vbusp region 0 firewall.

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Table 14-3125. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4804h

Figure 14-1553. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3126. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3126. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.160 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.160.1 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 4808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imshsi2c_main_6.vbusp region 0 firewall.

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Table 14-3127. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4808h

Figure 14-1554. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3128. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3128. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.161 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.161.1 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 480Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imshsi2c_main_6.vbusp region 0 firewall.

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Table 14-3129. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 480Ch

Figure 14-1555. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3130. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3130. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.162 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.162.1 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 4810h) [reset = 20060000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imshsi2c_main_6.vbusp region 0 firewall.

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Table 14-3131. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4810h

Figure 14-1556. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20060h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20060h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20060h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3132. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20060h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.163 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.163.1 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 4814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imshsi2c_main_6.vbusp region 0 firewall.

Return to Summary Table

Table 14-3133. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4814h

Figure 14-1557. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3134. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.164 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.164.1 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 4818h) [reset = 20060FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imshsi2c_main_6.vbusp region 0 firewall.

Return to Summary Table

Table 14-3135. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4818h

Figure 14-1558. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20060h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
20060h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20060h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3136. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20060h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.165 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.165.1 CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 481Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imshsi2c_main_6.vbusp region 0 firewall.

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Table 14-3137. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 481Ch

Figure 14-1559. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3138. CBASS_FW_IMSHSI2C_MAIN_6_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.166 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.166.1 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_CONTROL Register (Offset = 4C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imcanss_main_0.mcanss_vbusp region 0 firewall.

Return to Summary Table

Table 14-3139. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4C00h

Figure 14-1560. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3140. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.167 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.167.1 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 4C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imcanss_main_0.mcanss_vbusp region 0 firewall.

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Table 14-3141. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4C04h

Figure 14-1561. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3142. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3142. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.168 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.168.1 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 4C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imcanss_main_0.mcanss_vbusp region 0 firewall.

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Table 14-3143. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4C08h

Figure 14-1562. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3144. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3144. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.169 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.169.1 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 4C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imcanss_main_0.mcanss_vbusp region 0 firewall.

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Table 14-3145. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4C0Ch

Figure 14-1563. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3146. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3146. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.170 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.170.1 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 4C10h) [reset = 20700000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imcanss_main_0.mcanss_vbusp region 0 firewall.

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Table 14-3147. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4C10h

Figure 14-1564. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20700h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20700h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20700h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3148. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20700h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.171 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.171.1 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 4C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imcanss_main_0.mcanss_vbusp region 0 firewall.

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Table 14-3149. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4C14h

Figure 14-1565. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3150. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.172 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.172.1 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 4C18h) [reset = 20700FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imcanss_main_0.mcanss_vbusp region 0 firewall.

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Table 14-3151. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4C18h

Figure 14-1566. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20700h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
20700h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20700h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3152. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20700h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.173 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.173.1 CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 4C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imcanss_main_0.mcanss_vbusp region 0 firewall.

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Table 14-3153. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 4C1Ch

Figure 14-1567. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3154. CBASS_FW_IMCANSS_MAIN_0_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.174 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.174.1 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_CONTROL Register (Offset = 5000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imcanss_main_1.mcanss_vbusp region 0 firewall.

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Table 14-3155. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5000h

Figure 14-1568. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3156. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.175 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.175.1 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 5004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imcanss_main_1.mcanss_vbusp region 0 firewall.

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Table 14-3157. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5004h

Figure 14-1569. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3158. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3158. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.176 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.176.1 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 5008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imcanss_main_1.mcanss_vbusp region 0 firewall.

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Table 14-3159. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5008h

Figure 14-1570. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3160. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3160. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.177 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.177.1 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 500Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imcanss_main_1.mcanss_vbusp region 0 firewall.

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Table 14-3161. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 500Ch

Figure 14-1571. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3162. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3162. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.178 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.178.1 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 5010h) [reset = 20710000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imcanss_main_1.mcanss_vbusp region 0 firewall.

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Table 14-3163. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5010h

Figure 14-1572. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20710h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20710h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20710h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3164. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20710h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.179 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.179.1 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 5014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imcanss_main_1.mcanss_vbusp region 0 firewall.

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Table 14-3165. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5014h

Figure 14-1573. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3166. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.180 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.180.1 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 5018h) [reset = 20710FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imcanss_main_1.mcanss_vbusp region 0 firewall.

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Table 14-3167. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5018h

Figure 14-1574. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20710h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20710h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20710h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3168. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20710h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.181 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.181.1 CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 501Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imcanss_main_1.mcanss_vbusp region 0 firewall.

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Table 14-3169. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 501Ch

Figure 14-1575. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3170. CBASS_FW_IMCANSS_MAIN_1_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.182 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.182.1 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_CONTROL Register (Offset = 5400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imcanss_main_2.mcanss_vbusp region 0 firewall.

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Table 14-3171. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5400h

Figure 14-1576. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3172. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.183 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.183.1 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 5404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imcanss_main_2.mcanss_vbusp region 0 firewall.

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Table 14-3173. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5404h

Figure 14-1577. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3174. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3174. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.184 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.184.1 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 5408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imcanss_main_2.mcanss_vbusp region 0 firewall.

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Table 14-3175. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5408h

Figure 14-1578. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3176. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3176. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.185 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.185.1 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 540Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imcanss_main_2.mcanss_vbusp region 0 firewall.

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Table 14-3177. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 540Ch

Figure 14-1579. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3178. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3178. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.186 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.186.1 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 5410h) [reset = 20720000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imcanss_main_2.mcanss_vbusp region 0 firewall.

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Table 14-3179. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5410h

Figure 14-1580. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20720h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20720h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20720h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3180. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20720h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.187 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.187.1 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 5414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imcanss_main_2.mcanss_vbusp region 0 firewall.

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Table 14-3181. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5414h

Figure 14-1581. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3182. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.188 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.188.1 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 5418h) [reset = 20720FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imcanss_main_2.mcanss_vbusp region 0 firewall.

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Table 14-3183. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5418h

Figure 14-1582. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20720h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20720h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20720h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3184. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20720h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.189 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.189.1 CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 541Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imcanss_main_2.mcanss_vbusp region 0 firewall.

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Table 14-3185. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 541Ch

Figure 14-1583. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3186. CBASS_FW_IMCANSS_MAIN_2_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.190 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.190.1 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_CONTROL Register (Offset = 5800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imcanss_main_3.mcanss_vbusp region 0 firewall.

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Table 14-3187. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5800h

Figure 14-1584. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3188. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.191 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.191.1 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 5804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imcanss_main_3.mcanss_vbusp region 0 firewall.

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Table 14-3189. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5804h

Figure 14-1585. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3190. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3190. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.192 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.192.1 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 5808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imcanss_main_3.mcanss_vbusp region 0 firewall.

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Table 14-3191. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5808h

Figure 14-1586. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3192. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3192. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.193 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.193.1 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 580Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imcanss_main_3.mcanss_vbusp region 0 firewall.

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Table 14-3193. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 580Ch

Figure 14-1587. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3194. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3194. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.194 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.194.1 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 5810h) [reset = 20730000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imcanss_main_3.mcanss_vbusp region 0 firewall.

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Table 14-3195. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5810h

Figure 14-1588. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20730h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20730h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20730h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3196. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20730h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.195 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.195.1 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 5814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imcanss_main_3.mcanss_vbusp region 0 firewall.

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Table 14-3197. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5814h

Figure 14-1589. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3198. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.196 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.196.1 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 5818h) [reset = 20730FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imcanss_main_3.mcanss_vbusp region 0 firewall.

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Table 14-3199. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5818h

Figure 14-1590. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20730h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20730h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20730h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3200. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20730h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.197 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.197.1 CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 581Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imcanss_main_3.mcanss_vbusp region 0 firewall.

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Table 14-3201. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 581Ch

Figure 14-1591. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3202. CBASS_FW_IMCANSS_MAIN_3_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.198 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_CONTROL Register

14.1.6.2.198.1 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_CONTROL Register (Offset = 5C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Imcanss_main_4.mcanss_vbusp region 0 firewall.

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Table 14-3203. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5C00h

Figure 14-1592. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3204. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.199 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.199.1 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register (Offset = 5C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Imcanss_main_4.mcanss_vbusp region 0 firewall.

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Table 14-3205. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5C04h

Figure 14-1593. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3206. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3206. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.200 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.200.1 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register (Offset = 5C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Imcanss_main_4.mcanss_vbusp region 0 firewall.

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Table 14-3207. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5C08h

Figure 14-1594. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3208. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3208. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.201 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.201.1 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register (Offset = 5C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Imcanss_main_4.mcanss_vbusp region 0 firewall.

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Table 14-3209. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5C0Ch

Figure 14-1595. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3210. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3210. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.202 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.202.1 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register (Offset = 5C10h) [reset = 20740000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Imcanss_main_4.mcanss_vbusp region 0 firewall.

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Table 14-3211. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5C10h

Figure 14-1596. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20740h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20740h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20740h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3212. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20740h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.203 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.203.1 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register (Offset = 5C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Imcanss_main_4.mcanss_vbusp region 0 firewall.

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Table 14-3213. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5C14h

Figure 14-1597. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3214. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.204 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.204.1 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register (Offset = 5C18h) [reset = 20740FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Imcanss_main_4.mcanss_vbusp region 0 firewall.

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Table 14-3215. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5C18h

Figure 14-1598. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20740h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
20740h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20740h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3216. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20740h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.205 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.205.1 CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register (Offset = 5C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Imcanss_main_4.mcanss_vbusp region 0 firewall.

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Table 14-3217. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 5C1Ch

Figure 14-1599. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3218. CBASS_FW_IMCANSS_MAIN_4_MCANSS_VBUSP_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.206 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register

14.1.6.2.206.1 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register (Offset = 6000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isam67_pdma_spi_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3219. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6000h

Figure 14-1600. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3220. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.207 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.207.1

CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 6004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isam67_pdma_spi_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3221. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6004h

Figure 14-1601. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3222. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3222. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.208 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.208.1 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 6008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isam67_pdma_spi_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3223. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6008h

Figure 14-1602. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3224. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3224. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.209 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.209.1

CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = 600Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isam67_pdma_spi_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3225. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 600Ch

Figure 14-1603. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3226. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3226. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.210 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.210.1 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 6010h) [reset = C00000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isam67_pdma_spi_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3227. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6010h

Figure 14-1604. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
C00h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
C00h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
C00h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3228. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	C00h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.211 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.211.1 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 6014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isam67_pdma_spi_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3229. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6014h

Figure 14-1605. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3230. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.212 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.212.1 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 6018h) [reset = C00FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam67_pdma_spi_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3231. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6018h

Figure 14-1606. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
C00h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
C00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
C00h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3232. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	C00h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.213 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.213.1 CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 601Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isam67_pdma_spi_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3233. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 601Ch

Figure 14-1607. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3234. CBASS_FW_ISAM67_PDMA_SPI_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.214 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register

14.1.6.2.214.1 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register (Offset = 6400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iam275_pdma_spi1_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3235. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6400h

Figure 14-1608. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3236. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.215 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.215.1 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 6404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iam275_pdma_spi1_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3237. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6404h

Figure 14-1609. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3238. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3238. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.216 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.216.1 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 6408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iam275_pdma_spi1_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3239. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6408h

Figure 14-1610. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3240. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3240. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.217 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.217.1 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = 640Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iam275_pdma_spi1_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3241. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 640Ch

Figure 14-1611. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3242. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3242. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.218 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.218.1 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 6410h) [reset = C02000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_pdma_spi1_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3243. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6410h

Figure 14-1612. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
C02h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
C02h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
C02h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3244. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	C02h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.219 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.219.1 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 6414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_pdma_spi1_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3245. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6414h

Figure 14-1613. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3246. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.220 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.220.1 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 6418h) [reset = C02FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_pdma_spi1_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3247. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6418h

Figure 14-1614. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
C02h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
C02h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
C02h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3248. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	C02h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.221 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.221.1 CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 641Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_pdma_spi1_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3249. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 641Ch

Figure 14-1615. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3250. CBASS_FW_IAM275_PDMA_SPI1_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.222 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register

14.1.6.2.222.1 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register (Offset = 6800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isam62_pdma_uart_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3251. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6800h

Figure 14-1616. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3252. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.223 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.223.1 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 6804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isam62_pdma_uart_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3253. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6804h

Figure 14-1617. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3254. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3254. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.224 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.224.1 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 6808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isam62_pdma_uart_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3255. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6808h

Figure 14-1618. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3256. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3256. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.225 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.225.1 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = 680Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isam62_pdma_uart_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3257. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 680Ch

Figure 14-1619. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3258. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3258. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.226 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.226.1 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 6810h) [reset = C01000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isam62_pdma_uart_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3259. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6810h

Figure 14-1620. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">C01h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">C01h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">C01h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3260. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	C01h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.227 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.227.1 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 6814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isam62_pdma_uart_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3261. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6814h

Figure 14-1621. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3262. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.228 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.228.1 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 6818h) [reset = C01FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isam62_pdma_uart_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3263. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6818h

Figure 14-1622. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
C01h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
C01h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
C01h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3264. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	C01h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.229 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.229.1 CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 681Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isam62_pdma_uart_main_0.eccaggr_cfg region 0 firewall.

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Table 14-3265. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 681Ch

Figure 14-1623. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3266. CBASS_FW_ISAM62_PDMA_UART_MAIN_0_ECCAGGR_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.230 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_CONTROL Register

14.1.6.2.230.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_CONTROL Register (Offset = 6C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target lrl2_of_cba4_main_r5_0_core0.cfg region 0 firewall.

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Table 14-3267. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6C00h

Figure 14-1624. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3268. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.231 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.231.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 6C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Irl2_of_cba4_main_r5_0_core0.cfg region 0 firewall.

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Table 14-3269. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6C04h

Figure 14-1625. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3270. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3270. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.232 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.232.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 6C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Irl2_of_cba4_main_r5_0_core0.cfg region 0 firewall.

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Table 14-3271. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6C08h

Figure 14-1626. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3272. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3272. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.233 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.233.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = 6C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Irl2_of_cba4_main_r5_0_core0.cfg region 0 firewall.

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Table 14-3273. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6C0Ch

Figure 14-1627. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3274. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3274. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.234 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.234.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 6C10h) [reset = 25000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Irl2_of_cba4_main_r5_0_core0.cfg region 0 firewall.

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Table 14-3275. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6C10h

Figure 14-1628. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">25000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">25000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">25000h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3276. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	25000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.235 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.235.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 6C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Irl2_of_cba4_main_r5_0_core0.cfg region 0 firewall.

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Table 14-3277. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6C14h

Figure 14-1629. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3278. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.236 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.236.1
CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 6C18h) [reset = 25000FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Irl2_of_cba4_main_r5_0_core0.cfg region 0 firewall.

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Table 14-3279. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6C18h

Figure 14-1630. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
25000h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
25000h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
25000h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3280. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	25000h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.237 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.237.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 6C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Irl2_of_cba4_main_r5_0_core0.cfg region 0 firewall.

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Table 14-3281. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 6C1Ch

Figure 14-1631. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3282. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE0_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.238 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_CONTROL Register

14.1.6.2.238.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_CONTROL Register (Offset = 7000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target lrl2_of_cba4_main_r5_0_core1.cfg region 0 firewall.

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Table 14-3283. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7000h

Figure 14-1632. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3284. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.239 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.239.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 7004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Irl2_of_cba4_main_r5_0_core1.cfg region 0 firewall.

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Table 14-3285. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7004h

Figure 14-1633. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3286. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3286. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.240 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.240.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 7008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Irl2_of_cba4_main_r5_0_core1.cfg region 0 firewall.

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Table 14-3287. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7008h

Figure 14-1634. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3288. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3288. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.241 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.241.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = 700Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target lrl2_of_cba4_main_r5_0_core1.cfg region 0 firewall.

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Table 14-3289. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 700Ch

Figure 14-1635. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3290. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3290. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.242 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.242.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 7010h) [reset = 25001000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Irl2_of_cba4_main_r5_0_core1.cfg region 0 firewall.

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Table 14-3291. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7010h

Figure 14-1636. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">25001h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">25001h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">25001h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3292. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	25001h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.243 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.243.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 7014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Irl2_of_cba4_main_r5_0_core1.cfg region 0 firewall.

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Table 14-3293. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7014h

Figure 14-1637. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3294. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.244 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.244.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 7018h) [reset = 25001FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Irl2_of_cba4_main_r5_0_core1.cfg region 0 firewall.

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Table 14-3295. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7018h

Figure 14-1638. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
25001h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
25001h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
25001h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3296. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	25001h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.245 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.245.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 701Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Irl2_of_cba4_main_r5_0_core1.cfg region 0 firewall.

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Table 14-3297. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 701Ch

Figure 14-1639. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3298. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_0_CORE1_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.246 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_CONTROL Register

14.1.6.2.246.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_CONTROL Register (Offset = 7400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Irl2_of_cba4_main_r5_1_core0.cfg region 0 firewall.

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Table 14-3299. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7400h

Figure 14-1640. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3300. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.247 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.247.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 7404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Irl2_of_cba4_main_r5_1_core0.cfg region 0 firewall.

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Table 14-3301. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7404h

Figure 14-1641. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3302. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3302. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.248 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.248.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 7408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Irl2_of_cba4_main_r5_1_core0.cfg region 0 firewall.

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Table 14-3303. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7408h

Figure 14-1642. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3304. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3304. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.249 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.249.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = 740Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target lrl2_of_cba4_main_r5_1_core0.cfg region 0 firewall.

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Table 14-3305. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 740Ch

Figure 14-1643. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3306. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3306. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.250 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.250.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 7410h) [reset = 25002000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Irl2_of_cba4_main_r5_1_core0.cfg region 0 firewall.

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Table 14-3307. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7410h

Figure 14-1644. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
25002h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
25002h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
25002h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3308. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	25002h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.251 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.251.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 7414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Irl2_of_cba4_main_r5_1_core0.cfg region 0 firewall.

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Table 14-3309. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7414h

Figure 14-1645. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3310. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.252 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.252.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 7418h) [reset = 25002FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Irl2_of_cba4_main_r5_1_core0.cfg region 0 firewall.

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Table 14-3311. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7418h

Figure 14-1646. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
25002h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
25002h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
25002h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3312. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	25002h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.253 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.253.1

CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 741Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Irl2_of_cba4_main_r5_1_core0.cfg region 0 firewall.

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Table 14-3313. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 741Ch

Figure 14-1647. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3314. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE0_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.254 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_CONTROL Register

14.1.6.2.254.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_CONTROL Register (Offset = 7800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target lrl2_of_cba4_main_r5_1_core1.cfg region 0 firewall.

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Table 14-3315. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7800h

Figure 14-1648. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3316. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.255 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.255.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 7804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Irl2_of_cba4_main_r5_1_core1.cfg region 0 firewall.

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Table 14-3317. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7804h

Figure 14-1649. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3318. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3318. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.256 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.256.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_1 Register (Offset = 7808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Irl2_of_cba4_main_r5_1_core1.cfg region 0 firewall.

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Table 14-3319. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7808h

Figure 14-1650. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3320. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3320. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.257 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.257.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_2 Register (Offset = 780Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Irl2_of_cba4_main_r5_1_core1.cfg region 0 firewall.

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Table 14-3321. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 780Ch

Figure 14-1651. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3322. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3322. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.258 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.258.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 7810h) [reset = 25003000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Irl2_of_cba4_main_r5_1_core1.cfg region 0 firewall.

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Table 14-3323. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7810h

Figure 14-1652. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
25003h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
25003h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
25003h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3324. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	25003h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.259 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.259.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 7814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Irl2_of_cba4_main_r5_1_core1.cfg region 0 firewall.

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Table 14-3325. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7814h

Figure 14-1653. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-3326. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.260 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.260.1

CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 7818h) [reset = 25003FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Irl2_of_cba4_main_r5_1_core1.cfg region 0 firewall.

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Table 14-3327. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7818h

Figure 14-1654. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">25003h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">25003h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">25003h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3328. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	25003h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.261 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.261.1 CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 781Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target lrl2_of_cba4_main_r5_1_core1.cfg region 0 firewall.

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Table 14-3329. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 781Ch

Figure 14-1655. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3330. CBASS_FW_IRL2_OF_CBA4_MAIN_R5_1_CORE1_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.262 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.262.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_CONTROL Register (Offset = 7C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Irti_cfg1_main_r5_0_core0.slv region 0 firewall.

Return to Summary Table

Table 14-3331. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7C00h

Figure 14-1656. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3332. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.263 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.263.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 7C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Irti_cfg1_main_r5_0_core0.slv region 0 firewall.

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Table 14-3333. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7C04h

Figure 14-1657. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3334. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3334. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.264 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.264.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 7C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Irti_cfg1_main_r5_0_core0.slv region 0 firewall.

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Table 14-3335. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7C08h

Figure 14-1658. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3336. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3336. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.265 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.265.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 7C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Irti_cfg1_main_r5_0_core0.slv region 0 firewall.

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Table 14-3337. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7C0Ch

Figure 14-1659. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3338. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3338. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.266 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.266.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 7C10h) [reset = 20800000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Irti_cfg1_main_r5_0_core0.slv region 0 firewall.

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Table 14-3339. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7C10h

Figure 14-1660. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20800h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20800h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20800h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3340. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20800h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.267 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.267.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 7C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Irti_cfg1_main_r5_0_core0.slv region 0 firewall.

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Table 14-3341. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7C14h

Figure 14-1661. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3342. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.268 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.268.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 7C18h) [reset = 20800FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Irti_cfg1_main_r5_0_core0.slv region 0 firewall.

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Table 14-3343. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7C18h

Figure 14-1662. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20800h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20800h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20800h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3344. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20800h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.269 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.269.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 7C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Irti_cfg1_main_r5_0_core0.slv region 0 firewall.

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Table 14-3345. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 7C1Ch

Figure 14-1663. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3346. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE0_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.270 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.270.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_CONTROL Register (Offset = 8000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Irti_cfg1_main_r5_0_core1.slv region 0 firewall.

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Table 14-3347. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8000h

Figure 14-1664. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3348. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.271 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.271.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 8004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Irti_cfg1_main_r5_0_core1.slv region 0 firewall.

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Table 14-3349. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8004h

Figure 14-1665. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3350. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3350. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.272 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.272.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 8008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Irti_cfg1_main_r5_0_core1.slv region 0 firewall.

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Table 14-3351. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8008h

Figure 14-1666. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3352. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3352. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.273 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.273.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 800Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Irti_cfg1_main_r5_0_core1.slv region 0 firewall.

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Table 14-3353. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 800Ch

Figure 14-1667. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3354. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3354. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.274 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.274.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 8010h) [reset = 20810000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Irti_cfg1_main_r5_0_core1.slv region 0 firewall.

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Table 14-3355. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8010h

Figure 14-1668. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20810h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20810h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20810h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3356. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20810h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.275 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.275.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 8014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Irti_cfg1_main_r5_0_core1.slv region 0 firewall.

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Table 14-3357. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8014h

Figure 14-1669. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3358. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.276 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.276.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 8018h) [reset = 20810FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Irti_cfg1_main_r5_0_core1.slv region 0 firewall.

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Table 14-3359. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8018h

Figure 14-1670. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20810h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
20810h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20810h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3360. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20810h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.277 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.277.1 CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 801Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Irti_cfg1_main_r5_0_core1.slv region 0 firewall.

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Table 14-3361. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 801Ch

Figure 14-1671. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3362. CBASS_FW_IRTI_CFG1_MAIN_R5_0_CORE1_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.278 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.278.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_CONTROL Register (Offset = 8400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Irti_cfg1_main_r5_1_core0.slv region 0 firewall.

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Table 14-3363. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8400h

Figure 14-1672. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3364. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.279 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.279.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 8404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Irti_cfg1_main_r5_1_core0.slv region 0 firewall.

Return to Summary Table

Table 14-3365. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8404h

Figure 14-1673. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3366. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3366. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.280 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.280.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 8408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Irti_cfg1_main_r5_1_core0.slv region 0 firewall.

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Table 14-3367. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8408h

Figure 14-1674. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3368. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3368. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.281 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.281.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 840Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Irti_cfg1_main_r5_1_core0.slv region 0 firewall.

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Table 14-3369. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 840Ch

Figure 14-1675. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3370. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3370. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.282 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.282.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 8410h) [reset = 20820000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Irti_cfg1_main_r5_1_core0.slv region 0 firewall.

Return to Summary Table

Table 14-3371. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8410h

Figure 14-1676. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20820h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20820h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20820h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3372. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20820h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.283 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.283.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 8414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Irti_cfg1_main_r5_1_core0.slv region 0 firewall.

Return to Summary Table

Table 14-3373. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8414h

Figure 14-1677. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3374. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.284 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.284.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 8418h) [reset = 20820FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Irti_cfg1_main_r5_1_core0.slv region 0 firewall.

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Table 14-3375. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8418h

Figure 14-1678. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20820h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20820h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20820h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3376. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20820h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.285 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.285.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 841Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target lrti_cfg1_main_r5_1_core0.slv region 0 firewall.

Return to Summary Table

Table 14-3377. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 841Ch

Figure 14-1679. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3378. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE0_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.286 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.286.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_CONTROL Register (Offset = 8800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Irti_cfg1_main_r5_1_core1.slv region 0 firewall.

Return to Summary Table

Table 14-3379. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8800h

Figure 14-1680. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3380. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.287 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.287.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 8804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Irti_cfg1_main_r5_1_core1.slv region 0 firewall.

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Table 14-3381. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8804h

Figure 14-1681. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3382. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3382. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.288 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.288.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 8808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Irti_cfg1_main_r5_1_core1.slv region 0 firewall.

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Table 14-3383. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8808h

Figure 14-1682. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3384. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3384. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.289 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.289.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 880Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Irti_cfg1_main_r5_1_core1.slv region 0 firewall.

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Table 14-3385. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 880Ch

Figure 14-1683. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3386. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3386. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.290 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.290.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 8810h) [reset = 20830000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Irti_cfg1_main_r5_1_core1.slv region 0 firewall.

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Table 14-3387. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8810h

Figure 14-1684. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20830h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
20830h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20830h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3388. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20830h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.291 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.291.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 8814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target lrti_cfg1_main_r5_1_core1.slv region 0 firewall.

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Table 14-3389. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8814h

Figure 14-1685. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3390. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.292 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.292.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 8818h) [reset = 20830FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Irti_cfg1_main_r5_1_core1.slv region 0 firewall.

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Table 14-3391. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8818h

Figure 14-1686. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20830h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20830h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20830h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3392. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20830h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.293 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.293.1 CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 881Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Irti_cfg1_main_r5_1_core1.slv region 0 firewall.

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Table 14-3393. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 881Ch

Figure 14-1687. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3394. CBASS_FW_IRTI_CFG1_MAIN_R5_1_CORE1_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.294 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.294.1 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_CONTROL Register (Offset = 8C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ispi_main_0.slv region 0 firewall.

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Table 14-3395. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8C00h

Figure 14-1688. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3396. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.295 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.295.1 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 8C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ispi_main_0.slv region 0 firewall.

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Table 14-3397. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8C04h

Figure 14-1689. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3398. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3398. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.296 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.296.1 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 8C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ispi_main_0.slv region 0 firewall.

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Table 14-3399. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8C08h

Figure 14-1690. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3400. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3400. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.297 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.297.1 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 8C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ispi_main_0.slv region 0 firewall.

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Table 14-3401. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8C0Ch

Figure 14-1691. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3402. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3402. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.298 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.298.1 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 8C10h) [reset = 20100000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ispi_main_0.slv region 0 firewall.

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Table 14-3403. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8C10h

Figure 14-1692. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20100h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
20100h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20100h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3404. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20100h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.299 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.299.1 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 8C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ispi_main_0.slv region 0 firewall.

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Table 14-3405. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8C14h

Figure 14-1693. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3406. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.300 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.300.1 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 8C18h) [reset = 20100FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ispi_main_0.slv region 0 firewall.

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Table 14-3407. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8C18h

Figure 14-1694. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20100h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20100h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">20100h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3408. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20100h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.301 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.301.1 CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 8C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ispi_main_0.slv region 0 firewall.

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Table 14-3409. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 8C1Ch

Figure 14-1695. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3410. CBASS_FW_ISPI_MAIN_0_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.302 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.302.1 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_CONTROL Register (Offset = 9000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ispi_main_1.slv region 0 firewall.

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Table 14-3411. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9000h

Figure 14-1696. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3412. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.303 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.303.1 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 9004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ispi_main_1.slv region 0 firewall.

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Table 14-3413. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9004h

Figure 14-1697. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3414. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3414. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.304 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.304.1 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 9008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ispi_main_1.slv region 0 firewall.

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Table 14-3415. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9008h

Figure 14-1698. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3416. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3416. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.305 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.305.1 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 900Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ispi_main_1.slv region 0 firewall.

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Table 14-3417. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 900Ch

Figure 14-1699. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3418. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3418. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.306 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.306.1 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 9010h) [reset = 20110000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ispi_main_1.slv region 0 firewall.

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Table 14-3419. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9010h

Figure 14-1700. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20110h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20110h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20110h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3420. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20110h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.307 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.307.1 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 9014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ispi_main_1.slv region 0 firewall.

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Table 14-3421. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9014h

Figure 14-1701. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3422. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.308 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.308.1 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 9018h) [reset = 20110FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ispi_main_1.slv region 0 firewall.

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Table 14-3423. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9018h

Figure 14-1702. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20110h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
20110h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20110h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3424. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20110h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.309 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.309.1 CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 901Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ispi_main_1.slv region 0 firewall.

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Table 14-3425. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 901Ch

Figure 14-1703. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3426. CBASS_FW_ISPI_MAIN_1_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.310 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.310.1 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_CONTROL Register (Offset = 9400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ispi_main_2.slv region 0 firewall.

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Table 14-3427. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9400h

Figure 14-1704. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3428. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.311 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.311.1 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 9404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ispi_main_2.slv region 0 firewall.

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Table 14-3429. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9404h

Figure 14-1705. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3430. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3430. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.312 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.312.1 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 9408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ispi_main_2.slv region 0 firewall.

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Table 14-3431. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9408h

Figure 14-1706. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3432. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3432. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.313 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.313.1 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 940Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ispi_main_2.slv region 0 firewall.

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Table 14-3433. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 940Ch

Figure 14-1707. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3434. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3434. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.314 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.314.1 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 9410h) [reset = 20120000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ispi_main_2.slv region 0 firewall.

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Table 14-3435. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9410h

Figure 14-1708. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20120h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20120h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20120h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3436. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20120h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.315 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.315.1 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 9414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ispi_main_2.slv region 0 firewall.

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Table 14-3437. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9414h

Figure 14-1709. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3438. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.316 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.316.1 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 9418h) [reset = 20120FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ispi_main_2.slv region 0 firewall.

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Table 14-3439. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9418h

Figure 14-1710. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20120h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20120h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20120h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3440. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20120h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.317 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.317.1 CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 941Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ispi_main_2.slv region 0 firewall.

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Table 14-3441. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 941Ch

Figure 14-1711. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3442. CBASS_FW_ISPI_MAIN_2_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.318 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.318.1 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_CONTROL Register (Offset = 9800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ispi_main_3.slv region 0 firewall.

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Table 14-3443. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9800h

Figure 14-1712. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3444. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.319 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.319.1 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 9804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ispi_main_3.slv region 0 firewall.

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Table 14-3445. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9804h

Figure 14-1713. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3446. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3446. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.320 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.320.1 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 9808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ispi_main_3.slv region 0 firewall.

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Table 14-3447. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9808h

Figure 14-1714. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3448. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3448. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.321 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.321.1 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 980Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ispi_main_3.slv region 0 firewall.

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Table 14-3449. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 980Ch

Figure 14-1715. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3450. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3450. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.322 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.322.1 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 9810h) [reset = 20130000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ispi_main_3.slv region 0 firewall.

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Table 14-3451. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9810h

Figure 14-1716. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20130h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
20130h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20130h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3452. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20130h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.323 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.323.1 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 9814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ispi_main_3.slv region 0 firewall.

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Table 14-3453. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9814h

Figure 14-1717. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3454. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.324 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.324.1 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 9818h) [reset = 20130FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ispi_main_3.slv region 0 firewall.

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Table 14-3455. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9818h

Figure 14-1718. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20130h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
20130h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20130h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3456. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20130h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.325 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.325.1 CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 981Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Ispi_main_3.slv region 0 firewall.

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Table 14-3457. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 981Ch

Figure 14-1719. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3458. CBASS_FW_ISPI_MAIN_3_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.326 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.326.1 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_CONTROL Register (Offset = 9C00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Ispi_main_4.slv region 0 firewall.

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Table 14-3459. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9C00h

Figure 14-1720. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3460. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.327 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.327.1 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = 9C04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Ispi_main_4.slv region 0 firewall.

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Table 14-3461. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9C04h

Figure 14-1721. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3462. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3462. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.328 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.328.1 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = 9C08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Ispi_main_4.slv region 0 firewall.

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Table 14-3463. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9C08h

Figure 14-1722. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3464. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3464. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.329 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.329.1 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = 9C0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Ispi_main_4.slv region 0 firewall.

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Table 14-3465. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9C0Ch

Figure 14-1723. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3466. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3466. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.330 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.330.1 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = 9C10h) [reset = 20140000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Ispi_main_4.slv region 0 firewall.

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Table 14-3467. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9C10h

Figure 14-1724. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
20140h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
20140h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
20140h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3468. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	20140h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.331 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.331.1 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = 9C14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Ispi_main_4.slv region 0 firewall.

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Table 14-3469. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9C14h

Figure 14-1725. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3470. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.332 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.332.1 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = 9C18h) [reset = 20140FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Ispi_main_4.slv region 0 firewall.

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Table 14-3471. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9C18h

Figure 14-1726. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
20140h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
20140h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
20140h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3472. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	20140h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.333 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.333.1 CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = 9C1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target lspi_main_4.slv region 0 firewall.

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Table 14-3473. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 9C1Ch

Figure 14-1727. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3474. CBASS_FW_ISPI_MAIN_4_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.334 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_CONTROL Register

14.1.6.2.334.1 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_CONTROL Register (Offset = A000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iusart_main_0.vbusp_cba region 0 firewall.

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Table 14-3475. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A000h

Figure 14-1728. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3476. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.335 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.335.1 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register (Offset = A004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iusart_main_0.vbusp_cba region 0 firewall.

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Table 14-3477. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A004h

Figure 14-1729. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3478. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3478. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.336 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.336.1 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register (Offset = A008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iusart_main_0.vbusp_cba region 0 firewall.

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Table 14-3479. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A008h

Figure 14-1730. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3480. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3480. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.337 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.337.1 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register (Offset = A00Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iusart_main_0.vbusp_cba region 0 firewall.

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Table 14-3481. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A00Ch

Figure 14-1731. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3482. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3482. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.338 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.338.1 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register (Offset = A010h) [reset = 2800000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iusart_main_0.vbusp_cba region 0 firewall.

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Table 14-3483. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A010h

Figure 14-1732. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2800h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2800h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2800h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3484. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2800h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.339 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.339.1 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register (Offset = A014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iusart_main_0.vbusp_cba region 0 firewall.

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Table 14-3485. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A014h

Figure 14-1733. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3486. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.340 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.340.1 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register (Offset = A018h) [reset = 2800FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iusart_main_0.vbusp_cba region 0 firewall.

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Table 14-3487. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A018h

Figure 14-1734. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2800h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
2800h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2800h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3488. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2800h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.341 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.341.1 CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register (Offset = A01Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iusart_main_0.vbusp_cba region 0 firewall.

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Table 14-3489. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A01Ch

Figure 14-1735. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3490. CBASS_FW_IUSART_MAIN_0_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.342 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_CONTROL Register

14.1.6.2.342.1 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_CONTROL Register (Offset = A400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iusart_main_1.vbusp_cba region 0 firewall.

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Table 14-3491. Instance Table

Instance Name	**Physical Address**
CBASS_MISC_PERI0	4503 A400h

Figure 14-1736. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3492. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.343 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.343.1 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register (Offset = A404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iusart_main_1.vbusp_cba region 0 firewall.

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Table 14-3493. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A404h

Figure 14-1737. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3494. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3494. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.344 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.344.1 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register (Offset = A408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iusart_main_1.vbusp_cba region 0 firewall.

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Table 14-3495. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A408h

Figure 14-1738. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3496. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3496. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.345 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.345.1 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register (Offset = A40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iusart_main_1.vbusp_cba region 0 firewall.

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Table 14-3497. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A40Ch

Figure 14-1739. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3498. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3498. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.346 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.346.1 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register (Offset = A410h) [reset = 2810000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iusart_main_1.vbusp_cba region 0 firewall.

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Table 14-3499. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A410h

Figure 14-1740. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2810h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
2810h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2810h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3500. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2810h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.347 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.347.1 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register (Offset = A414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iusart_main_1.vbusp_cba region 0 firewall.

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Table 14-3501. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A414h

Figure 14-1741. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3502. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.348 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.348.1 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register (Offset = A418h) [reset = 2810FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iusart_main_1.vbusp_cba region 0 firewall.

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Table 14-3503. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A418h

Figure 14-1742. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2810h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2810h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2810h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3504. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2810h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.349 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.349.1 CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register (Offset = A41Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iusart_main_1.vbusp_cba region 0 firewall.

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Table 14-3505. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A41Ch

Figure 14-1743. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3506. CBASS_FW_IUSART_MAIN_1_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.350 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_CONTROL Register

14.1.6.2.350.1 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_CONTROL Register (Offset = A800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iusart_main_2.vbusp_cba region 0 firewall.

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Table 14-3507. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A800h

Figure 14-1744. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3508. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.351 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.351.1 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register (Offset = A804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iusart_main_2.vbusp_cba region 0 firewall.

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Table 14-3509. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A804h

Figure 14-1745. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3510. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3510. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.352 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.352.1 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register (Offset = A808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iusart_main_2.vbusp_cba region 0 firewall.

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Table 14-3511. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A808h

Figure 14-1746. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRIV_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NONSEC_USER_DEBUG</td><td>NONSEC_USER_CACHEABLE</td><td>NONSEC_USER_READ</td><td>NONSEC_USER_WRITE</td><td>NONSEC_SUPV_DEBUG</td><td>NONSEC_SUPV_CACHEABLE</td><td>NONSEC_SUPV_READ</td><td>NONSEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SEC_USER_DEBUG</td><td>SEC_USER_CACHEABLE</td><td>SEC_USER_READ</td><td>SEC_USER_WRITE</td><td>SEC_SUPV_DEBUG</td><td>SEC_SUPV_CACHEABLE</td><td>SEC_SUPV_READ</td><td>SEC_SUPV_WRITE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-3512. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3512. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.353 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.353.1 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register (Offset = A80Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iusart_main_2.vbusp_cba region 0 firewall.

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Table 14-3513. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A80Ch

Figure 14-1747. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3514. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3514. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.354 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.354.1 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register (Offset = A810h) [reset = 2820000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iusart_main_2.vbusp_cba region 0 firewall.

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Table 14-3515. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A810h

Figure 14-1748. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2820h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2820h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2820h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3516. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2820h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.355 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.355.1 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register (Offset = A814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iusart_main_2.vbusp_cba region 0 firewall.

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Table 14-3517. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A814h

Figure 14-1749. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3518. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.356 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.356.1 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register (Offset = A818h) [reset = 2820FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iusart_main_2.vbusp_cba region 0 firewall.

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Table 14-3519. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A818h

Figure 14-1750. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2820h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
2820h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2820h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3520. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2820h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.357 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.357.1 CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register (Offset = A81Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iusart_main_2.vbusp_cba region 0 firewall.

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Table 14-3521. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 A81Ch

Figure 14-1751. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3522. CBASS_FW_IUSART_MAIN_2_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.358 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_CONTROL Register

14.1.6.2.358.1 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_CONTROL Register (Offset = AC00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iusart_main_3.vbusp_cba region 0 firewall.

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Table 14-3523. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 AC00h

Figure 14-1752. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3524. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.359 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.359.1 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register (Offset = AC04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iusart_main_3.vbusp_cba region 0 firewall.

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Table 14-3525. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 AC04h

Figure 14-1753. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3526. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3526. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.360 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.360.1 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register (Offset = AC08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iusart_main_3.vbusp_cba region 0 firewall.

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Table 14-3527. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 AC08h

Figure 14-1754. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3528. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3528. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.361 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.361.1 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register (Offset = AC0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iusart_main_3.vbusp_cba region 0 firewall.

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Table 14-3529. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 AC0Ch

Figure 14-1755. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3530. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3530. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.362 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.362.1 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register (Offset = AC10h) [reset = 2830000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iusart_main_3.vbusp_cba region 0 firewall.

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Table 14-3531. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 AC10h

Figure 14-1756. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2830h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2830h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2830h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3532. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2830h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.363 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.363.1 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register (Offset = AC14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iusart_main_3.vbusp_cba region 0 firewall.

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Table 14-3533. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 AC14h

Figure 14-1757. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3534. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.364 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.364.1 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register (Offset = AC18h) [reset = 2830FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iusart_main_3.vbusp_cba region 0 firewall.

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Table 14-3535. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 AC18h

Figure 14-1758. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2830h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2830h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2830h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3536. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2830h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.365 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.365.1 CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register (Offset = AC1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iusart_main_3.vbusp_cba region 0 firewall.

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Table 14-3537. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 AC1Ch

Figure 14-1759. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3538. CBASS_FW_IUSART_MAIN_3_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.366 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_CONTROL Register

14.1.6.2.366.1 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_CONTROL Register (Offset = B000h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iusart_main_4.vbusp_cba region 0 firewall.

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Table 14-3539. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B000h

Figure 14-1760. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3540. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.367 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.367.1 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register (Offset = B004h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iusart_main_4.vbusp_cba region 0 firewall.

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Table 14-3541. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B004h

Figure 14-1761. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3542. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3542. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.368 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.368.1 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register (Offset = B008h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iusart_main_4.vbusp_cba region 0 firewall.

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Table 14-3543. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B008h

Figure 14-1762. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3544. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3544. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.369 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.369.1 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register (Offset = B00Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iusart_main_4.vbusp_cba region 0 firewall.

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Table 14-3545. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B00Ch

Figure 14-1763. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3546. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3546. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.370 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.370.1 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register (Offset = B010h) [reset = 2840000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iusart_main_4.vbusp_cba region 0 firewall.

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Table 14-3547. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B010h

Figure 14-1764. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2840h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
2840h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2840h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3548. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2840h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.371 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.371.1 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register (Offset = B014h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iusart_main_4.vbusp_cba region 0 firewall.

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Table 14-3549. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B014h

Figure 14-1765. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3550. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.372 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.372.1 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register (Offset = B018h) [reset = 2840FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iusart_main_4.vbusp_cba region 0 firewall.

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Table 14-3551. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B018h

Figure 14-1766. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2840h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
2840h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2840h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3552. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2840h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.373 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.373.1 CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register (Offset = B01Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iusart_main_4.vbusp_cba region 0 firewall.

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Table 14-3553. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B01Ch

Figure 14-1767. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3554. CBASS_FW_IUSART_MAIN_4_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.374 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_CONTROL Register

14.1.6.2.374.1 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_CONTROL Register (Offset = B400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iusart_main_5.vbusp_cba region 0 firewall.

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Table 14-3555. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B400h

Figure 14-1768. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3556. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.375 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.375.1 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register (Offset = B404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iusart_main_5.vbusp_cba region 0 firewall.

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Table 14-3557. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B404h

Figure 14-1769. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3558. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3558. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.376 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.376.1 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register (Offset = B408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iusart_main_5.vbusp_cba region 0 firewall.

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Table 14-3559. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B408h

Figure 14-1770. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3560. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3560. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.377 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.377.1 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register (Offset = B40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iusart_main_5.vbusp_cba region 0 firewall.

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Table 14-3561. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B40Ch

Figure 14-1771. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3562. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3562. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.378 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.378.1 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register (Offset = B410h) [reset = 2850000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iusart_main_5.vbusp_cba region 0 firewall.

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Table 14-3563. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B410h

Figure 14-1772. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2850h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
2850h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2850h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3564. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2850h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.379 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.379.1 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register (Offset = B414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iusart_main_5.vbusp_cba region 0 firewall.

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Table 14-3565. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B414h

Figure 14-1773. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3566. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.380 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.380.1 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register (Offset = B418h) [reset = 2850FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iusart_main_5.vbusp_cba region 0 firewall.

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Table 14-3567. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B418h

Figure 14-1774. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2850h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2850h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">2850h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3568. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2850h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.381 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.381.1 CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register (Offset = B41Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iusart_main_5.vbusp_cba region 0 firewall.

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Table 14-3569. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B41Ch

Figure 14-1775. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3570. CBASS_FW_IUSART_MAIN_5_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.382 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_CONTROL Register

14.1.6.2.382.1 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_CONTROL Register (Offset = B800h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iusart_main_6.vbusp_cba region 0 firewall.

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Table 14-3571. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B800h

Figure 14-1776. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3572. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.383 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.383.1 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register (Offset = B804h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iusart_main_6.vbusp_cba region 0 firewall.

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Table 14-3573. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B804h

Figure 14-1777. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3574. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3574. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.384 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.384.1 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register (Offset = B808h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iusart_main_6.vbusp_cba region 0 firewall.

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Table 14-3575. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B808h

Figure 14-1778. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3576. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3576. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.385 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.385.1 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register (Offset = B80Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iusart_main_6.vbusp_cba region 0 firewall.

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Table 14-3577. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B80Ch

Figure 14-1779. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3578. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3578. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.386 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.386.1 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register (Offset = B810h) [reset = 2860000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iusart_main_6.vbusp_cba region 0 firewall.

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Table 14-3579. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B810h

Figure 14-1780. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
2860h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
2860h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
2860h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-3580. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	2860h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.387 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.387.1 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register (Offset = B814h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iusart_main_6.vbusp_cba region 0 firewall.

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Table 14-3581. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B814h

Figure 14-1781. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3582. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.388 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.388.1 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register (Offset = B818h) [reset = 2860FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iusart_main_6.vbusp_cba region 0 firewall.

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Table 14-3583. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B818h

Figure 14-1782. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
2860h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
2860h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
2860h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3584. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	2860h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.389 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.389.1 CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register (Offset = B81Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iusart_main_6.vbusp_cba region 0 firewall.

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Table 14-3585. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 B81Ch

Figure 14-1783. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3586. CBASS_FW_IUSART_MAIN_6_VBUSP_CBA_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.390 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL Register

14.1.6.2.390.1 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL Register (Offset = BC00h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Iam275_main_misc_peri_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-3587. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 BC00h

Figure 14-1784. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3588. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.391 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Register

14.1.6.2.391.1 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Register (Offset = BC04h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Iam275_main_misc_peri_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-3589. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 BC04h

Figure 14-1785. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3590. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3590. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.392 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Register

14.1.6.2.392.1 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Register (Offset = BC08h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Iam275_main_misc_peri_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-3591. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 BC08h

Figure 14-1786. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3592. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3592. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.393 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Register

14.1.6.2.393.1 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Register (Offset = BC0Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Iam275_main_misc_peri_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-3593. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 BC0Ch

Figure 14-1787. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3594. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3594. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.394 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L Register

14.1.6.2.394.1 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L Register (Offset = BC10h) [reset = 201F0000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Iam275_main_misc_peri_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-3595. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 BC10h

Figure 14-1788. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
201F0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
201F0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
201F0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3596. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	201F0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.395 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H Register

14.1.6.2.395.1 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H Register (Offset = BC14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Iam275_main_misc_peri_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-3597. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 BC14h

Figure 14-1789. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3598. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.396 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L Register

14.1.6.2.396.1 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L Register (Offset = BC18h) [reset = 201F0FFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Iam275_main_misc_peri_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-3599. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 BC18h

Figure 14-1790. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
201F0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
201F0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
201F0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3600. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	201F0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.397 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H Register

14.1.6.2.397.1 CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H Register (Offset = BC1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Iam275_main_misc_peri_cbass_main_0.cbass_err_slv region 0 firewall.

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Table 14-3601. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4503 BC1Ch

Figure 14-1791. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3602. CBASS_FW_IAM275_MAIN_MISC_PERI_CBASS_MAIN_0_CBASS_ERR_SLV_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.398 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Register

14.1.6.2.398.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Register (Offset = 0h) [reset = 10D800h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu0_pmst region 0 ISC.

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Table 14-3603. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0000h

Figure 14-1792. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D8h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3604. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3604. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.399 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register

14.1.6.2.399.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 0 ISC.

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Table 14-3605. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0010h

Figure 14-1793. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3606. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.400 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register

14.1.6.2.400.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 0 ISC.

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Table 14-3607. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0014h

Figure 14-1794. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3608. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.401 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register

14.1.6.2.401.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 0 ISC.

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Table 14-3609. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0018h

Figure 14-1795. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3610. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.402 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register

14.1.6.2.402.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 0 ISC.

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Table 14-3611. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 001Ch

Figure 14-1796. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3612. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.403 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_CONTROL Register

14.1.6.2.403.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_CONTROL Register (Offset = 20h) [reset = 10D800h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu0_pmst region 1 ISC.

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Table 14-3613. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0020h

Figure 14-1797. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D8h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3614. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3614. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.404 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register

14.1.6.2.404.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 1 ISC.

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Table 14-3615. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0030h

Figure 14-1798. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3616. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.405 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register

14.1.6.2.405.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 1 ISC.

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Table 14-3617. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0034h

Figure 14-1799. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3618. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.406 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register

14.1.6.2.406.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 1 ISC.

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Table 14-3619. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0038h

Figure 14-1800. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3620. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.407 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register

14.1.6.2.407.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 1 ISC.

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Table 14-3621. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 003Ch

Figure 14-1801. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3622. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.408 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_CONTROL Register

14.1.6.2.408.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_CONTROL Register (Offset = 40h) [reset = 10D800h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu0_pmst region 2 ISC.

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Table 14-3623. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0040h

Figure 14-1802. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D8h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3624. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3624. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.409 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register

14.1.6.2.409.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 2 ISC.

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Table 14-3625. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0050h

Figure 14-1803. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3626. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.410 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register

14.1.6.2.410.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 2 ISC.

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Table 14-3627. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0054h

Figure 14-1804. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-3628. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.411 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register

14.1.6.2.411.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 2 ISC.

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Table 14-3629. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0058h

Figure 14-1805. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3630. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.412 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register

14.1.6.2.412.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 2 ISC.

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Table 14-3631. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 005Ch

Figure 14-1806. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3632. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.413 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_CONTROL Register

14.1.6.2.413.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_CONTROL Register (Offset = 60h) [reset = 10D800h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu0_pmst region 3 ISC.

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Table 14-3633. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0060h

Figure 14-1807. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D8h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3634. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3634. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.414 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register

14.1.6.2.414.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 3 ISC.

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Table 14-3635. Instance Table

Instance Name	**Physical Address**
CBASS_MISC_PERI0	4584 0070h

Figure 14-1808. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3636. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.415 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register

14.1.6.2.415.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 3 ISC.

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Table 14-3637. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0074h

Figure 14-1809. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3638. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.416 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register

14.1.6.2.416.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 3 ISC.

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Table 14-3639. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0078h

Figure 14-1810. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3640. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.417 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register

14.1.6.2.417.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu0_pmst region 3 ISC.

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Table 14-3641. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 007Ch

Figure 14-1811. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-3642. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.418 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register

14.1.6.2.418.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 80h) [reset = 10D84Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu0_pmst region 4 ISC.

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Table 14-3643. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0080h

Figure 14-1812. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D8h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3644. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3644. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D8h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.419 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Register

14.1.6.2.419.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Register (Offset = 400h) [reset = 10D900h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu1_pmst region 0 ISC.

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Table 14-3645. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0400h

Figure 14-1813. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3646. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3646. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.420 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register

14.1.6.2.420.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 0 ISC.

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Table 14-3647. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0410h

Figure 14-1814. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3648. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.421 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register

14.1.6.2.421.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 0 ISC.

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Table 14-3649. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0414h

Figure 14-1815. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3650. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.422 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register

14.1.6.2.422.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 0 ISC.

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Table 14-3651. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0418h

Figure 14-1816. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3652. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.423 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register

14.1.6.2.423.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 0 ISC.

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Table 14-3653. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 041Ch

Figure 14-1817. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3654. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.424 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_CONTROL Register

14.1.6.2.424.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_CONTROL Register (Offset = 420h) [reset = 10D900h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu1_pmst region 1 ISC.

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Table 14-3655. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0420h

Figure 14-1818. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
D9h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3656. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3656. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.425 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L Register

14.1.6.2.425.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 1 ISC.

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Table 14-3657. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0430h

Figure 14-1819. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3658. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.426 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H Register

14.1.6.2.426.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 1 ISC.

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Table 14-3659. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0434h

Figure 14-1820. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_H							
R/W							
0h							

Table 14-3660. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.427 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L Register

14.1.6.2.427.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 1 ISC.

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Table 14-3661. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0438h

Figure 14-1821. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3662. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.428 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H Register

14.1.6.2.428.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 1 ISC.

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Table 14-3663. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 043Ch

Figure 14-1822. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3664. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.429 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_CONTROL Register

14.1.6.2.429.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_CONTROL Register (Offset = 440h) [reset = 10D900h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu1_pmst region 2 ISC.

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Table 14-3665. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0440h

Figure 14-1823. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D9h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3666. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3666. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.430 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L Register

14.1.6.2.430.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 2 ISC.

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Table 14-3667. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0450h

Figure 14-1824. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3668. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.431 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H Register

14.1.6.2.431.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 2 ISC.

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Table 14-3669. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0454h

Figure 14-1825. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3670. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.432 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L Register

14.1.6.2.432.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 2 ISC.

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Table 14-3671. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0458h

Figure 14-1826. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3672. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.433 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H Register

14.1.6.2.433.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 2 ISC.

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Table 14-3673. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 045Ch

Figure 14-1827. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3674. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.434 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_CONTROL Register

14.1.6.2.434.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_CONTROL Register (Offset = 460h) [reset = 10D900h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu1_pmst region 3 ISC.

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Table 14-3675. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0460h

Figure 14-1828. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D9h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3676. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3676. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.435 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L Register

14.1.6.2.435.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 3 ISC.

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Table 14-3677. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0470h

Figure 14-1829. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3678. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.436 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H Register

14.1.6.2.436.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 3 ISC.

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Table 14-3679. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0474h

Figure 14-1830. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3680. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.437 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L Register

14.1.6.2.437.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 3 ISC.

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Table 14-3681. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0478h

Figure 14-1831. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3682. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.438 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H Register

14.1.6.2.438.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_0.cpu1_pmst region 3 ISC.

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Table 14-3683. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 047Ch

Figure 14-1832. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3684. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.439 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Register

14.1.6.2.439.1 CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 480h) [reset = 10D94Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_sl_main_0.cpu1_pmst region 4 ISC.

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Table 14-3685. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0480h

Figure 14-1833. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
D9h							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3686. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3686. CBASS_ISC_IPULSAR_SL_MAIN_0_CPU1_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	D9h	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.440 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Register

14.1.6.2.440.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Register (Offset = 800h) [reset = 10DB00h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu0_pmst region 0 ISC.

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Table 14-3687. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0800h

Figure 14-1834. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DBh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3688. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3688. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.441 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register

14.1.6.2.441.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = 810h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 0 ISC.

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Table 14-3689. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0810h

Figure 14-1835. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3690. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.442 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register

14.1.6.2.442.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = 814h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 0 ISC.

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Table 14-3691. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0814h

Figure 14-1836. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3692. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.443 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register

14.1.6.2.443.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = 818h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 0 ISC.

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Table 14-3693. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0818h

Figure 14-1837. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3694. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.444 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register

14.1.6.2.444.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = 81Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 0 ISC.

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Table 14-3695. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 081Ch

Figure 14-1838. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3696. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.445 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_CONTROL Register

14.1.6.2.445.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_CONTROL Register (Offset = 820h) [reset = 10DB00h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu0_pmst region 1 ISC.

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Table 14-3697. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0820h

Figure 14-1839. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DBh							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3698. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3698. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.446 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register

14.1.6.2.446.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = 830h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 1 ISC.

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Table 14-3699. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0830h

Figure 14-1840. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3700. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.447 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register

14.1.6.2.447.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = 834h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 1 ISC.

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Table 14-3701. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0834h

Figure 14-1841. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3702. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.448 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register

14.1.6.2.448.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = 838h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 1 ISC.

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Table 14-3703. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0838h

Figure 14-1842. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3704. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.449 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register

14.1.6.2.449.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = 83Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 1 ISC.

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Table 14-3705. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 083Ch

Figure 14-1843. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3706. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.450 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_CONTROL Register

14.1.6.2.450.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_CONTROL Register (Offset = 840h) [reset = 10DB00h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu0_pmst region 2 ISC.

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Table 14-3707. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0840h

Figure 14-1844. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DBh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3708. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3708. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.451 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register

14.1.6.2.451.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = 850h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 2 ISC.

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Table 14-3709. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0850h

Figure 14-1845. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3710. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.452 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register

14.1.6.2.452.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = 854h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 2 ISC.

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Table 14-3711. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0854h

Figure 14-1846. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3712. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.453 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register

14.1.6.2.453.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = 858h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 2 ISC.

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Table 14-3713. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0858h

Figure 14-1847. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3714. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.454 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register

14.1.6.2.454.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = 85Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 2 ISC.

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Table 14-3715. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 085Ch

Figure 14-1848. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3716. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.455 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_CONTROL Register

14.1.6.2.455.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_CONTROL Register (Offset = 860h) [reset = 10DB00h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu0_pmst region 3 ISC.

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Table 14-3717. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0860h

Figure 14-1849. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	

23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			

15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DBh							

7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3718. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3718. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.456 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register

14.1.6.2.456.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = 870h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 3 ISC.

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Table 14-3719. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0870h

Figure 14-1850. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3720. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.457 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register

14.1.6.2.457.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = 874h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 3 ISC.

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Table 14-3721. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0874h

Figure 14-1851. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3722. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.458 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register

14.1.6.2.458.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = 878h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 3 ISC.

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Table 14-3723. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0878h

Figure 14-1852. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3724. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.459 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register

14.1.6.2.459.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = 87Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu0_pmst region 3 ISC.

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Table 14-3725. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 087Ch

Figure 14-1853. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3726. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.460 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Register

14.1.6.2.460.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Register (Offset = 880h) [reset = 10DB4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu0_pmst region 4 ISC.

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Table 14-3727. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0880h

Figure 14-1854. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DBh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3728. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3728. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU0_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DBh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.461 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Register

14.1.6.2.461.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Register (Offset = C00h) [reset = 10DC00h]

The ISC Region 0 Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu1_pmst region 0 ISC.

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Table 14-3729. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C00h

Figure 14-1855. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DCh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3730. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3730. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.462 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register

14.1.6.2.462.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register (Offset = C10h) [reset = 0h]

The ISC Region 0 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 0 ISC.

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Table 14-3731. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C10h

Figure 14-1856. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3732. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.463 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register

14.1.6.2.463.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register (Offset = C14h) [reset = 0h]

The ISC Region 0 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 0 ISC.

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Table 14-3733. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C14h

Figure 14-1857. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3734. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.464 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register

14.1.6.2.464.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register (Offset = C18h) [reset = FFFh]

The ISC Region 0 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 0 ISC.

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Table 14-3735. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C18h

Figure 14-1858. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3736. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.465 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register

14.1.6.2.465.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register (Offset = C1Ch) [reset = 0h]

The ISC Region 0 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 0 ISC.

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Table 14-3737. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C1Ch

Figure 14-1859. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3738. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.466 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_CONTROL Register

14.1.6.2.466.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_CONTROL Register (Offset = C20h) [reset = 10DC00h]

The ISC Region 1 Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu1_pmst region 1 ISC.

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Table 14-3739. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C20h

Figure 14-1860. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DCh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3740. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3740. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.467 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L Register

14.1.6.2.467.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L Register (Offset = C30h) [reset = 0h]

The ISC Region 1 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 1 ISC.

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Table 14-3741. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C30h

Figure 14-1861. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3742. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.468 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H Register

14.1.6.2.468.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H Register (Offset = C34h) [reset = 0h]

The ISC Region 1 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 1 ISC.

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Table 14-3743. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C34h

Figure 14-1862. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3744. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.469 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L Register

14.1.6.2.469.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L Register (Offset = C38h) [reset = FFFh]

The ISC Region 1 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 1 ISC.

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Table 14-3745. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C38h

Figure 14-1863. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							

23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							

15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			

7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3746. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.470 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H Register

14.1.6.2.470.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H Register (Offset = C3Ch) [reset = 0h]

The ISC Region 1 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 1 ISC.

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Table 14-3747. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C3Ch

Figure 14-1864. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3748. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.471 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_CONTROL Register

14.1.6.2.471.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_CONTROL Register (Offset = C40h) [reset = 10DC00h]

The ISC Region 2 Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu1_pmst region 2 ISC.

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Table 14-3749. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C40h

Figure 14-1865. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DCh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3750. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3750. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.472 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L Register

14.1.6.2.472.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L Register (Offset = C50h) [reset = 0h]

The ISC Region 2 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 2 ISC.

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Table 14-3751. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C50h

Figure 14-1866. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3752. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.473 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H Register

14.1.6.2.473.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H Register (Offset = C54h) [reset = 0h]

The ISC Region 2 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 2 ISC.

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Table 14-3753. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C54h

Figure 14-1867. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3754. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.474 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L Register

14.1.6.2.474.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L Register (Offset = C58h) [reset = FFFh]

The ISC Region 2 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 2 ISC.

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Table 14-3755. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C58h

Figure 14-1868. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3756. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.475 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H Register

14.1.6.2.475.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H Register (Offset = C5Ch) [reset = 0h]

The ISC Region 2 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 2 ISC.

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Table 14-3757. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C5Ch

Figure 14-1869. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3758. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.476 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_CONTROL Register

14.1.6.2.476.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_CONTROL Register (Offset = C60h) [reset = 10DC00h]

The ISC Region 3 Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu1_pmst region 3 ISC.

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Table 14-3759. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C60h

Figure 14-1870. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W							
DCh							
7	6	5	4	3	2	1	0
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R/W	R/W1TS	R/W			
0h	0h	0h	0h	0h			

Table 14-3760. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement, pass through value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. Reset Source: domain_default_rst_mod_g_rst_n
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-3760. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEF	R	0h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R/W	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.477 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L Register

14.1.6.2.477.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L Register (Offset = C70h) [reset = 0h]

The ISC Region 3 Start Address Low Register defines the start address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 3 ISC.

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Table 14-3761. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C70h

Figure 14-1871. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R/W							
0h							

Table 14-3762. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R/W	0h	Start address bits 11 to 0 must be 0 as address must be 4KB aligned in address mode. Can also be channel number in channel mode. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.478 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H Register

14.1.6.2.478.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H Register (Offset = C74h) [reset = 0h]

The ISC Region 3 Start Address High Register defines the start address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 3 ISC.

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Table 14-3763. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C74h

Figure 14-1872. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3764. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.479 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L Register

14.1.6.2.479.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L Register (Offset = C78h) [reset = FFFh]

The ISC Region 3 End Address Low Register defines the end included address bits 31 to 0 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 3 ISC.

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Table 14-3765. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C78h

Figure 14-1873. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3766. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to Fs as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.480 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H Register

14.1.6.2.480.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H Register (Offset = C7Ch) [reset = 0h]

The ISC Region 3 End Address High Register defines the end address bits 47 to 32 for the initiator Ipulsar_sl_main_1.cpu1_pmst region 3 ISC.

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Table 14-3767. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C7Ch

Figure 14-1874. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3768. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.481 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Register

14.1.6.2.481.1 CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Register (Offset = C80h) [reset = 10DC4Ah]

The ISC Default Region Control Register defines the control fields for the initiator Ipulsar_sl_main_1.cpu1_pmst region 4 ISC.

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Table 14-3769. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	4584 0C80h

Figure 14-1875. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
NONE				R/W		R/W	
0h				0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PASS	NONSEC	SEC			
NONE		R/W	R/W	R/W			
0h		0h	1h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRIV_ID							
R/W							
DCh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DEF	CH_MODE	LOCK	ENABLE			
NONE	R	R	R/W1TS	R			
0h	1h	0h	0h	Ah			

Table 14-3770. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set, else the bit is unchanged. Do not set both priv and nopriv for the same bit. Reset Source: domain_default_rst_mod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	PASS	R/W	0h	No privID replacement. A value of 1 will pass through privid value. A value of 0 will replace privid with priv_id field value. Reset Source: domain_default_rst_mod_g_rst_n
20	NONSEC	R/W	1h	Make outgoing non-secure. A value of 1 forces secure clear, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3770. CBASS_ISC_IPULSAR_SL_MAIN_1_CPU1_PMST_ISC_REGION_DEF_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	SEC	R/W	0h	Make outgoing secure. A value of 0xA forces secure set, others do nothing. Do not set both sec and nonsec. Reset Source: domain_default_rst_mod_g_rst_n
15:8	PRIV_ID	R/W	DCh	Priv ID value to use if pass is 0. Reset Source: domain_default_rst_mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	DEF	R	1h	Default region indication. The default region is used when all other regions do not match. Reset Source: domain_default_rst_mod_g_rst_n
5	CH_MODE	R	0h	Enable channel mode to match region to a chanid value. Otherwise use address mode to match region to an address range. Reset Source: domain_default_rst_mod_g_rst_n
4	LOCK	R/W1TS	0h	Lock region. Once set, the region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R	Ah	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.482 CBASS_GLB_PID Register

14.1.6.2.482.1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66005102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-3771. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A000h

Figure 14-1876. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Ah					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-3772. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	Ah	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.483 CBASS_GLB_DESTINATION_ID Register

14.1.6.2.483.1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-3773. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A004h

Figure 14-1877. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-3774. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.484 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

14.1.6.2.484.1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-3775. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A020h

Figure 14-1878. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-3776. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.485 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

14.1.6.2.485.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-3777. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A024h

Figure 14-1879. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TYPE_F</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SRC_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3778. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.486 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

14.1.6.2.486.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-3779. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A028h

Figure 14-1880. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3780. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.6.2.487 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

14.1.6.2.487.1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-3781. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A02Ch

Figure 14-1881. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-3782. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.488 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

14.1.6.2.488.1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-3783. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A030h

Figure 14-1882. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-3784. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.489 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

14.1.6.2.489.1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-3785. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A034h

Figure 14-1883. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-3786. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.490 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

14.1.6.2.490.1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-3787. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A038h

Figure 14-1884. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-3788. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.491 CBASS_GLB_EXCEPTION_PEND_SET Register

14.1.6.2.491.1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-3789. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A040h

Figure 14-1885. CBASS_GLB_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-3790. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.492 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

14.1.6.2.492.1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-3791. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45B0 A044h

Figure 14-1886. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-3792. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.6.2.493 CBASS_QOS_IPULSAR_SL_MAIN_0_CPU0_PMST_MAP0 Register

14.1.6.2.493.1 CBASS_QOS_IPULSAR_SL_MAIN_0_CPU0_PMST_MAP0 Register (Offset = 100h) [reset = 7000h]

The Map Register defines the fields for the initiator Ipulsar_sl_main_0.cpu0_pmst per channel.

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Table 14-3793. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45D4 0100h

Figure 14-1887. CBASS_QOS_IPULSAR_SL_MAIN_0_CPU0_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-3794. CBASS_QOS_IPULSAR_SL_MAIN_0_CPU0_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.6.2.494 CBASS_QOS_IPULSAR_SL_MAIN_0_CPU1_PMST_MAP0 Register

14.1.6.2.494.1 CBASS_QOS_IPULSAR_SL_MAIN_0_CPU1_PMST_MAP0 Register (Offset = 500h) [reset = 7000h]

The Map Register defines the fields for the initiator Ipulsar_sl_main_0.cpu1_pmst per channel.

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Table 14-3795. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45D4 0500h

Figure 14-1888. CBASS_QOS_IPULSAR_SL_MAIN_0_CPU1_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-3796. CBASS_QOS_IPULSAR_SL_MAIN_0_CPU1_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.6.2.495 CBASS_QOS_IPULSAR_SL_MAIN_1_CPU0_PMST_MAP0 Register

14.1.6.2.495.1 CBASS_QOS_IPULSAR_SL_MAIN_1_CPU0_PMST_MAP0 Register (Offset = 900h) [reset = 7000h]

The Map Register defines the fields for the initiator Ipulsar_sl_main_1.cpu0_pmst per channel.

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Table 14-3797. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45D4 0900h

Figure 14-1889. CBASS_QOS_IPULSAR_SL_MAIN_1_CPU0_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	6	5	4	3	2	1	0
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-3798. CBASS_QOS_IPULSAR_SL_MAIN_1_CPU0_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.6.2.496 CBASS_QOS_IPULSAR_SL_MAIN_1_CPU1_PMST_MAP0 Register

14.1.6.2.496.1 CBASS_QOS_IPULSAR_SL_MAIN_1_CPU1_PMST_MAP0 Register (Offset = D00h) [reset = 7000h]

The Map Register defines the fields for the initiator Ipulsar_sl_main_1.cpu1_pmst per channel.

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Table 14-3799. Instance Table

Instance Name	Physical Address
CBASS_MISC_PERI0	45D4 0D00h

Figure 14-1890. CBASS_QOS_IPULSAR_SL_MAIN_1_CPU1_PMST_MAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	EPRIORITY			ASEL			
NONE	R/W			R/W			
0h	7h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID				RESERVED			
R/W				NONE			
0h				0h	0h		

Table 14-3800. CBASS_QOS_IPULSAR_SL_MAIN_1_CPU1_PMST_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EPRIORITY	R/W	7h	epriority signal for channel N. This is the strict priority arbitration priority at the destination Reset Source: domain_default_rst_mod_g_rst_n
11:8	ASEL	R/W	0h	Only used for PCIe, and cache coherency with A53 ACP. So traffic to MSRAM or DDR with asel set to below values will be routed via A53 cache controller. ASEL=0 | normal ASEL=1 | PCIe address space for the entire address ASEL=14 | W | cause L2 cache allocation: for cache warming feature ASEL=14 | R | does not cause L2 cache allocation ASEL=15 | R/W | does not cause L2 cache allocation Reset Source: domain_default_rst_mod_g_rst_n
7:4	ORDERID	R/W	0h	orderid signal for channel N. Selects to route for load balancing (0-7 uses one route, 8-15 another). Also used by DDR4/LPDDR4 re-ordering to maximize throughput. Order of transactions is only guaranteed with the same orderid Reset Source: domain_default_rst_mod_g_rst_n
3	RESERVED	NONE	0h	Reserved

14.1.7 CBASS_SAFE

CBASS_SAFE

14.1.7.1 CBASS_SAFE Summaries

CBASS_SAFE Summaries

Table 14-3801. CBASS_ERR Registers, Base Address=0460 0000h, Length=1024

Offset	Length	Register Name	WKUP_CBASS_SAFE1 Physical Address
0h	32	CBASS_ERR_PID	0460 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0460 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0460 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0460 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0460 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0460 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0460 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0460 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0460 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0460 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0460 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0460 005Ch
60h	32	CBASS_ERR_EOI	0460 0060h

14.1.7.2 CBASS_SAFE Registers

CBASS_SAFE Registers

14.1.7.2.1 CBASS_ERR_PID Register

14.1.7.2.1.1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66005102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-3802. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0000h

Figure 14-1891. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Ah					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-3803. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
15:11	RTL	R	Ah	RTL revision. Will vary depending on release. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.2 CBASS_ERR_DESTINATION_ID Register

14.1.7.2.2.1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-3804. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0004h

Figure 14-1892. CBASS_ERR_DESTINATION_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DEST_ID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3805. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

14.1.7.2.3.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-3806. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0024h

Figure 14-1893. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-3807. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

14.1.7.2.4.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-3808. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0028h

Figure 14-1894. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GROUP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CODE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3809. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.7.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

14.1.7.2.5.1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-3810. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 002Ch

Figure 14-1895. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3811. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

14.1.7.2.6.1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-3812. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0030h

Figure 14-1896. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_H</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_H</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3813. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

14.1.7.2.7.1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-3814. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0034h

Figure 14-1897. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ROUTEID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIV_ID							
R							
0h							

Table 14-3815. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

14.1.7.2.8.1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-3816. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0038h

Figure 14-1898. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-3817. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

14.1.7.2.9.1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-3818. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0050h

Figure 14-1899. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-3819. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

14.1.7.2.10.1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-3820. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0054h

Figure 14-1900. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-3821. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

14.1.7.2.11.1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-3822. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0058h

Figure 14-1901. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-3823. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

14.1.7.2.12.1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-3824. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 005Ch

Figure 14-1902. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-3825. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.7.2.13 CBASS_ERR_EOI Register

14.1.7.2.13.1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

Return to Summary Table

Table 14-3826. Instance Table

Instance Name	Physical Address
WKUP_CBASS_SAFE1	0460 0060h

Figure 14-1903. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-3827. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRP_32_SAFE_MCU_CLK4_rst_mod_g_rst_n

14.1.8 am275_main_IPCSS_cbass

am275_main_IPCSS_cbass

14.1.8.1 am275_main_IPCSS_cbass Summaries

am275_main_IPCSS_cbass Summaries

Table 14-3828. CBASS_ERR Registers, Base Address=0023 0000h, Length=1024

Offset	Length	Register Name	IPCSS_CBASS0 Physical Address
0h	32	CBASS_ERR_PID	0023 0000h
4h	32	CBASS_ERR_DESTINATION_ID	0023 0004h
24h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER0	0023 0024h
28h	32	CBASS_ERR_EXCEPTION_LOGGING_HEADER1	0023 0028h
2Ch	32	CBASS_ERR_EXCEPTION_LOGGING_DATA0	0023 002Ch
30h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA1	0023 0030h
34h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA2	0023 0034h
38h	32	CBASS_ERR_EXCEPTION_LOGGING_DATA3	0023 0038h
50h	32	CBASS_ERR_ERR_INTR_RAW_STAT	0023 0050h
54h	32	CBASS_ERR_ERR_INTR_ENABLED_STAT	0023 0054h
58h	32	CBASS_ERR_ERR_INTR_ENABLE_SET	0023 0058h
5Ch	32	CBASS_ERR_ERR_INTR_ENABLE_CLR	0023 005Ch
60h	32	CBASS_ERR_EOI	0023 0060h

Table 14-3829. CBASS_FW Registers, Base Address=4502 8000h, Length=2048

Offset	Length	Register Name	IPCSS_CBASS0 Physical Address
0h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL	4502 8000h
4h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0	4502 8004h
8h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1	4502 8008h
Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2	4502 800Ch
10h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L	4502 8010h
14h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H	4502 8014h
18h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L	4502 8018h
1Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H	4502 801Ch
20h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL	4502 8020h
24h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0	4502 8024h
28h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1	4502 8028h
2Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2	4502 802Ch
30h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L	4502 8030h
34h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H	4502 8034h

Table 14-3829. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	IPCSS_CBASS0 Physical Address
38h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L	4502 8038h
3Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H	4502 803Ch
40h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL	4502 8040h
44h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0	4502 8044h
48h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1	4502 8048h
4Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2	4502 804Ch
50h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L	4502 8050h
54h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H	4502 8054h
58h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L	4502 8058h
5Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H	4502 805Ch
60h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL	4502 8060h
64h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0	4502 8064h
68h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1	4502 8068h
6Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2	4502 806Ch
70h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L	4502 8070h
74h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H	4502 8074h
78h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L	4502 8078h
7Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H	4502 807Ch
80h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL	4502 8080h
84h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0	4502 8084h
88h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1	4502 8088h
8Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2	4502 808Ch
90h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L	4502 8090h
94h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H	4502 8094h
98h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L	4502 8098h
9Ch	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H	4502 809Ch
A0h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL	4502 80A0h

Table 14-3829. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	IPCSS_CBASS0 Physical Address
A4h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0	4502 80A4h
A8h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1	4502 80A8h
ACh	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2	4502 80ACh
B0h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L	4502 80B0h
B4h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H	4502 80B4h
B8h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L	4502 80B8h
BCh	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H	4502 80BCh
C0h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL	4502 80C0h
C4h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0	4502 80C4h
C8h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1	4502 80C8h
CCh	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2	4502 80CCh
D0h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L	4502 80D0h
D4h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H	4502 80D4h
D8h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L	4502 80D8h
DCh	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H	4502 80DCh
E0h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL	4502 80E0h
E4h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0	4502 80E4h
E8h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1	4502 80E8h
ECh	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2	4502 80ECh
F0h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L	4502 80F0h
F4h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H	4502 80F4h
F8h	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L	4502 80F8h
FCh	32	CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H	4502 80FCh
400h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL	4502 8400h
404h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0	4502 8404h
408h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1	4502 8408h
40Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2	4502 840Ch

Table 14-3829. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	IPCSS_CBASS0 Physical Address
410h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L	4502 8410h
414h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H	4502 8414h
418h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L	4502 8418h
41Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H	4502 841Ch
420h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL	4502 8420h
424h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0	4502 8424h
428h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1	4502 8428h
42Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2	4502 842Ch
430h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L	4502 8430h
434h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H	4502 8434h
438h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L	4502 8438h
43Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H	4502 843Ch
440h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL	4502 8440h
444h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0	4502 8444h
448h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1	4502 8448h
44Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2	4502 844Ch
450h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L	4502 8450h
454h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H	4502 8454h
458h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L	4502 8458h
45Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H	4502 845Ch
460h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL	4502 8460h
464h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0	4502 8464h
468h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1	4502 8468h
46Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2	4502 846Ch
470h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L	4502 8470h
474h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H	4502 8474h
478h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L	4502 8478h

Table 14-3829. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	IPCSS_CBASS0 Physical Address
47Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H	4502 847Ch
480h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL	4502 8480h
484h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0	4502 8484h
488h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1	4502 8488h
48Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2	4502 848Ch
490h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L	4502 8490h
494h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H	4502 8494h
498h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L	4502 8498h
49Ch	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H	4502 849Ch
4A0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL	4502 84A0h
4A4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0	4502 84A4h
4A8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1	4502 84A8h
4ACh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2	4502 84ACh
4B0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L	4502 84B0h
4B4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H	4502 84B4h
4B8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L	4502 84B8h
4BCh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H	4502 84BCh
4C0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL	4502 84C0h
4C4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0	4502 84C4h
4C8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1	4502 84C8h
4CCh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2	4502 84CCh
4D0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L	4502 84D0h
4D4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H	4502 84D4h
4D8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L	4502 84D8h
4DCh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H	4502 84DCh
4E0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL	4502 84E0h
4E4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0	4502 84E4h

Table 14-3829. CBASS_FW Registers, Base Address=4502 8000h, Length=2048 (continued)

Offset	Length	Register Name	IPCSS_CBASS0 Physical Address
4E8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1	4502 84E8h
4ECh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2	4502 84ECh
4F0h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L	4502 84F0h
4F4h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H	4502 84F4h
4F8h	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L	4502 84F8h
4FCh	32	CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H	4502 84FCh

Table 14-3830. CBASS_GLB Registers, Base Address=45B0 1000h, Length=1024

Offset	Length	Register Name	IPCSS_CBASS0 Physical Address
0h	32	CBASS_GLB_PID	45B0 1000h
4h	32	CBASS_GLB_DESTINATION_ID	45B0 1004h
20h	32	CBASS_GLB_EXCEPTION_LOGGING_CONTROL	45B0 1020h
24h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER0	45B0 1024h
28h	32	CBASS_GLB_EXCEPTION_LOGGING_HEADER1	45B0 1028h
2Ch	32	CBASS_GLB_EXCEPTION_LOGGING_DATA0	45B0 102Ch
30h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA1	45B0 1030h
34h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA2	45B0 1034h
38h	32	CBASS_GLB_EXCEPTION_LOGGING_DATA3	45B0 1038h
40h	32	CBASS_GLB_EXCEPTION_PEND_SET	45B0 1040h
44h	32	CBASS_GLB_EXCEPTION_PEND_CLEAR	45B0 1044h

14.1.8.2 am275_main_IPCSS_cbass Registers

am275_main_IPCSS_cbass Registers

14.1.8.2.1 CBASS_ERR_PID Register

14.1.8.2.1.1 CBASS_ERR_PID Register (Offset = 0h) [reset = 66006102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-3831. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0000h

Figure 14-1904. CBASS_ERR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	22	21	20	19	18	17	16
FUNC							
R							
600h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Ch					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-3832. CBASS_ERR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
15:11	RTL	R	Ch	RTL revision. Will vary depending on release. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.2 CBASS_ERR_DESTINATION_ID Register

14.1.8.2.2.1 CBASS_ERR_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-3833. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0004h

Figure 14-1905. CBASS_ERR_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-3834. CBASS_ERR_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.3 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register

14.1.8.2.3.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-3835. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0024h

Figure 14-1906. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-3836. CBASS_ERR_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 7 = CBASS. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Always 0. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.4 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register

14.1.8.2.4.1 CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-3837. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0028h

Figure 14-1907. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-3838. CBASS_ERR_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Always 0. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. 0 = CBASS decode error. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.8.2.5 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register

14.1.8.2.5.1 CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-3839. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 002Ch

Figure 14-1908. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-3840. CBASS_ERR_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.6 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register

14.1.8.2.6.1 CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-3841. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0030h

Figure 14-1909. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-3842. CBASS_ERR_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.7 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register

14.1.8.2.7.1 CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-3843. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0034h

Figure 14-1910. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-3844. CBASS_ERR_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.8 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register

14.1.8.2.8.1 CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-3845. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0038h

Figure 14-1911. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-3846. CBASS_ERR_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.9 CBASS_ERR_ERR_INTR_RAW_STAT Register

14.1.8.2.9.1 CBASS_ERR_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = 0h]

The interrupt raw status register indicates if there is null interrupt regardless of interrupt enable

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Table 14-3847. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0050h

Figure 14-1912. CBASS_ERR_ERR_INTR_RAW_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR
NONE							R/W1TS
0h							0h

Table 14-3848. CBASS_ERR_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR	R/W1TS	0h	Level Interrupt status Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.10 CBASS_ERR_ERR_INTR_ENABLED_STAT Register

14.1.8.2.10.1 CBASS_ERR_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = 0h]

The interrupt status register is gated by the interrupt enable

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Table 14-3849. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0054h

Figure 14-1913. CBASS_ERR_ERR_INTR_ENABLED_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
NONE							R/W1TC
0h							0h

Table 14-3850. CBASS_ERR_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLED_INTR	R/W1TC	0h	Level Enabled Interrupt status Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.11 CBASS_ERR_ERR_INTR_ENABLE_SET Register

14.1.8.2.11.1 CBASS_ERR_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = 0h]

Only when this register is set, null access will cause interrupt to be generated.

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Table 14-3851. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0058h

Figure 14-1914. CBASS_ERR_ERR_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-3852. CBASS_ERR_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.12 CBASS_ERR_ERR_INTR_ENABLE_CLR Register

14.1.8.2.12.1 CBASS_ERR_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = 0h]

Setting this register disables the null interrupt generation

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Table 14-3853. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 005Ch

Figure 14-1915. CBASS_ERR_ERR_INTR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTR_ENABLE_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-3854. CBASS_ERR_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTR_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.13 CBASS_ERR_EOI Register

14.1.8.2.13.1 CBASS_ERR_EOI Register (Offset = 60h) [reset = 0h]

Writing to EOI Register indicates that current interrupt has been serviced which then allows next interrupt to be generated

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Table 14-3855. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	0023 0060h

Figure 14-1916. CBASS_ERR_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 14-3856. CBASS_ERR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	End Of Interrupt Register Reset Source: SCRM_64_HSM_CLK2_rst_mod_g_rst_n

14.1.8.2.14 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register

14.1.8.2.14.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Idmss_am275_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3857. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8000h

Figure 14-1917. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3858. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.15 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register

14.1.8.2.15.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3859. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8004h

Figure 14-1918. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3860. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3860. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.16 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register

14.1.8.2.16.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register (Offset = 8h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3861. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8008h

Figure 14-1919. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3862. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3862. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.17 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register

14.1.8.2.17.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register (Offset = Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3863. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 800Ch

Figure 14-1920. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3864. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3864. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.18 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register

14.1.8.2.18.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 4D000000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am275_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3865. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8010h

Figure 14-1921. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
4D000h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
4D000h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
4D000h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3866. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	4D000h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.19 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register

14.1.8.2.19.1

CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am275_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3867. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8014h

Figure 14-1922. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3868. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.20 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register

14.1.8.2.20.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 4D07FFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3869. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8018h

Figure 14-1923. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
4D07Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
4D07Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
4D07Fh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3870. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	4D07Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.21 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register

14.1.8.2.21.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3871. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 801Ch

Figure 14-1924. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3872. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.22 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register

14.1.8.2.22.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register (Offset = 20h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Idmss_am275_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-3873. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8020h

Figure 14-1925. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3874. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.23 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register

14.1.8.2.23.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register (Offset = 24h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-3875. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8024h

Figure 14-1926. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3876. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3876. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.24 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register

14.1.8.2.24.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register (Offset = 28h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-3877. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8028h

Figure 14-1927. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3878. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3878. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.25 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register

14.1.8.2.25.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register (Offset = 2Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-3879. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 802Ch

Figure 14-1928. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3880. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3880. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.26 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register

14.1.8.2.26.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am275_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-3881. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8030h

Figure 14-1929. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3882. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.27 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register

14.1.8.2.27.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am275_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-3883. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8034h

Figure 14-1930. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3884. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.28 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register

14.1.8.2.28.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-3885. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8038h

Figure 14-1931. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-3886. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.29 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register

14.1.8.2.29.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-3887. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 803Ch

Figure 14-1932. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3888. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.30 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register

14.1.8.2.30.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register (Offset = 40h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Idmss_am275_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-3889. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8040h

Figure 14-1933. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3890. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.31 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register

14.1.8.2.31.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register (Offset = 44h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-3891. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8044h

Figure 14-1934. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3892. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3892. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.32 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register

14.1.8.2.32.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register (Offset = 48h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-3893. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8048h

Figure 14-1935. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3894. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3894. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.33 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register

14.1.8.2.33.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register (Offset = 4Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-3895. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 804Ch

Figure 14-1936. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3896. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3896. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.34 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register

14.1.8.2.34.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register (Offset = 50h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am275_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-3897. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8050h

Figure 14-1937. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3898. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.35 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register

14.1.8.2.35.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am275_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-3899. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8054h

Figure 14-1938. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3900. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.36 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register

14.1.8.2.36.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register (Offset = 58h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-3901. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8058h

Figure 14-1939. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3902. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.37 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register

14.1.8.2.37.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-3903. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 805Ch

Figure 14-1940. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3904. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.38 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register

14.1.8.2.38.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register (Offset = 60h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Idmss_am275_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-3905. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8060h

Figure 14-1941. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>CACHE_MODE</td><td>BACKGROUND</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>LOCK</td><td colspan="4">ENABLE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W1TS</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-3906. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.39 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register

14.1.8.2.39.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register (Offset = 64h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-3907. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8064h

Figure 14-1942. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3908. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3908. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.40 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register

14.1.8.2.40.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register (Offset = 68h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-3909. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8068h

Figure 14-1943. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3910. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3910. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.41 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register

14.1.8.2.41.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register (Offset = 6Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-3911. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 806Ch

Figure 14-1944. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3912. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3912. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.42 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register

14.1.8.2.42.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register (Offset = 70h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am275_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-3913. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8070h

Figure 14-1945. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3914. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.43 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register

14.1.8.2.43.1

CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am275_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-3915. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8074h

Figure 14-1946. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3916. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.44 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register

14.1.8.2.44.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register (Offset = 78h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-3917. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8078h

Figure 14-1947. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3918. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.45 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register

14.1.8.2.45.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-3919. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 807Ch

Figure 14-1948. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3920. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.46 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register

14.1.8.2.46.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register (Offset = 80h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Idmss_am275_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-3921. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8080h

Figure 14-1949. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3922. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.47 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register

14.1.8.2.47.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register (Offset = 84h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-3923. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8084h

Figure 14-1950. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3924. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3924. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.48 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register

14.1.8.2.48.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register (Offset = 88h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-3925. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8088h

Figure 14-1951. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3926. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3926. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.49 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register

14.1.8.2.49.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register (Offset = 8Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-3927. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 808Ch

Figure 14-1952. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3928. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3928. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.50 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register

14.1.8.2.50.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register (Offset = 90h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am275_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-3929. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8090h

Figure 14-1953. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3930. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.51 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register

14.1.8.2.51.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register (Offset = 94h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am275_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-3931. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8094h

Figure 14-1954. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3932. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.52 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register

14.1.8.2.52.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register (Offset = 98h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-3933. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8098h

Figure 14-1955. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3934. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.53 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register

14.1.8.2.53.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register (Offset = 9Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-3935. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 809Ch

Figure 14-1956. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3936. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.54 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register

14.1.8.2.54.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register (Offset = A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Idmss_am275_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-3937. Instance Table

Instance Name	**Physical Address**
IPCSS_CBASS0	4502 80A0h

Figure 14-1957. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3938. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.55 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register

14.1.8.2.55.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register (Offset = A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-3939. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80A4h

Figure 14-1958. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3940. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3940. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.56 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register

14.1.8.2.56.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register (Offset = A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-3941. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80A8h

Figure 14-1959. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3942. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3942. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.57 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register

14.1.8.2.57.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register (Offset = ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-3943. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80ACh

Figure 14-1960. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3944. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3944. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.58 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register

14.1.8.2.58.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register (Offset = B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am275_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-3945. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80B0h

Figure 14-1961. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3946. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.59 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register

14.1.8.2.59.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register (Offset = B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am275_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-3947. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80B4h

Figure 14-1962. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3948. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.60 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register

14.1.8.2.60.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register (Offset = B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-3949. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80B8h

Figure 14-1963. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3950. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.61 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register

14.1.8.2.61.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register (Offset = BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-3951. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80BCh

Figure 14-1964. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3952. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.62 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register

14.1.8.2.62.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register (Offset = C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Idmss_am275_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-3953. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80C0h

Figure 14-1965. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3954. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.63 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register

14.1.8.2.63.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register (Offset = C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-3955. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80C4h

Figure 14-1966. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3956. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3956. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.64 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register

14.1.8.2.64.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register (Offset = C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-3957. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80C8h

Figure 14-1967. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3958. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3958. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.65 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register

14.1.8.2.65.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register (Offset = CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-3959. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80CCh

Figure 14-1968. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRIV_ID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3960. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3960. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.66 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register

14.1.8.2.66.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register (Offset = D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am275_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-3961. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80D0h

Figure 14-1969. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3962. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.67 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register

14.1.8.2.67.1

CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register (Offset = D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am275_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-3963. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80D4h

Figure 14-1970. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-3964. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.68 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register

14.1.8.2.68.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register (Offset = D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-3965. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80D8h

Figure 14-1971. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3966. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.69 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register

14.1.8.2.69.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register (Offset = DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-3967. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80DCh

Figure 14-1972. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3968. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.70 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register

14.1.8.2.70.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register (Offset = E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Idmss_am275_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-3969. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80E0h

Figure 14-1973. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3970. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.71 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register

14.1.8.2.71.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register (Offset = E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-3971. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80E4h

Figure 14-1974. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3972. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3972. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.72 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register

14.1.8.2.72.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register (Offset = E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-3973. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80E8h

Figure 14-1975. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3974. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3974. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.73 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register

14.1.8.2.73.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register (Offset = ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Idmss_am275_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-3975. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80ECh

Figure 14-1976. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3976. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3976. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.74 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register

14.1.8.2.74.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register (Offset = F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Idmss_am275_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-3977. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80F0h

Figure 14-1977. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3978. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.75 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register

14.1.8.2.75.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register (Offset = F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Idmss_am275_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-3979. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80F4h

Figure 14-1978. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3980. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.76 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register

14.1.8.2.76.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register (Offset = F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-3981. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80F8h

Figure 14-1979. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3982. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.77 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register

14.1.8.2.77.1 CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register (Offset = FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Idmss_am275_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-3983. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 80FCh

Figure 14-1980. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-3984. CBASS_FW_IDMSS_AM275_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.78 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register

14.1.8.2.78.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register (Offset = 400h) [reset = 0h]

The FW Region 0 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3985. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8400h

Figure 14-1981. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-3986. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.79 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register

14.1.8.2.79.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register (Offset = 404h) [reset = 0h]

The FW Region 0 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3987. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8404h

Figure 14-1982. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3988. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3988. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.80 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register

14.1.8.2.80.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register (Offset = 408h) [reset = 0h]

The FW Region 0 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3989. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8408h

Figure 14-1983. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3990. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3990. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.81 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register

14.1.8.2.81.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register (Offset = 40Ch) [reset = 0h]

The FW Region 0 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3991. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 840Ch

Figure 14-1984. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							

15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-3992. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-3992. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.82 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register

14.1.8.2.82.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register (Offset = 410h) [reset = 43600000h]

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3993. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8410h

Figure 14-1985. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
43600h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
43600h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
43600h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-3994. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	43600h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.83 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register

14.1.8.2.83.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register (Offset = 414h) [reset = 0h]

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3995. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8414h

Figure 14-1986. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-3996. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.84 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register

14.1.8.2.84.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register (Offset = 418h) [reset = 4360FFFFh]

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3997. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8418h

Figure 14-1987. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
4360Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
4360Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
4360Fh				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-3998. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	4360Fh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.85 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register

14.1.8.2.85.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register (Offset = 41Ch) [reset = 0h]

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 0 firewall.

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Table 14-3999. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 841Ch

Figure 14-1988. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4000. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.86 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register

14.1.8.2.86.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register (Offset = 420h) [reset = 0h]

The FW Region 1 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-4001. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8420h

Figure 14-1989. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4002. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.87 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register

14.1.8.2.87.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register (Offset = 424h) [reset = 0h]

The FW Region 1 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-4003. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8424h

Figure 14-1990. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4004. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4004. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.88 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register

14.1.8.2.88.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register (Offset = 428h) [reset = 0h]

The FW Region 1 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-4005. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8428h

Figure 14-1991. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4006. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4006. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.89 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register

14.1.8.2.89.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register (Offset = 42Ch) [reset = 0h]

The FW Region 1 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-4007. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 842Ch

Figure 14-1992. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4008. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4008. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.90 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register

14.1.8.2.90.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register (Offset = 430h) [reset = 0h]

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-4009. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8430h

Figure 14-1993. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4010. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.91 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register

14.1.8.2.91.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register (Offset = 434h) [reset = 0h]

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-4011. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8434h

Figure 14-1994. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4012. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.92 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register

14.1.8.2.92.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register (Offset = 438h) [reset = FFFh]

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-4013. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8438h

Figure 14-1995. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4014. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.93 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register

14.1.8.2.93.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register (Offset = 43Ch) [reset = 0h]

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 1 firewall.

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Table 14-4015. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 843Ch

Figure 14-1996. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4016. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.94 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register

14.1.8.2.94.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register (Offset = 440h) [reset = 0h]

The FW Region 2 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-4017. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8440h

Figure 14-1997. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4018. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.95 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register

14.1.8.2.95.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register (Offset = 444h) [reset = 0h]

The FW Region 2 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-4019. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8444h

Figure 14-1998. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4020. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4020. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.96 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register

14.1.8.2.96.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register (Offset = 448h) [reset = 0h]

The FW Region 2 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-4021. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8448h

Figure 14-1999. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4022. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4022. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.97 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register

14.1.8.2.97.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register (Offset = 44Ch) [reset = 0h]

The FW Region 2 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-4023. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 844Ch

Figure 14-2000. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4024. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4024. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.98 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register

14.1.8.2.98.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register (Offset = 450h) [reset = 0h]

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-4025. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8450h

Figure 14-2001. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4026. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.99 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register

14.1.8.2.99.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register (Offset = 454h) [reset = 0h]

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-4027. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8454h

Figure 14-2002. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4028. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.100 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register

14.1.8.2.100.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register (Offset = 458h) [reset = FFFh]

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-4029. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8458h

Figure 14-2003. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4030. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.101 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register

14.1.8.2.101.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register (Offset = 45Ch) [reset = 0h]

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 2 firewall.

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Table 14-4031. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 845Ch

Figure 14-2004. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_H							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_H							
R/W							
0h							

Table 14-4032. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.102 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register

14.1.8.2.102.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register (Offset = 460h) [reset = 0h]

The FW Region 3 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-4033. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8460h

Figure 14-2005. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4034. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.103 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register

14.1.8.2.103.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register (Offset = 464h) [reset = 0h]

The FW Region 3 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-4035. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8464h

Figure 14-2006. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4036. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4036. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.104 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register

14.1.8.2.104.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register (Offset = 468h) [reset = 0h]

The FW Region 3 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-4037. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8468h

Figure 14-2007. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4038. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4038. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.105 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register

14.1.8.2.105.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register (Offset = 46Ch) [reset = 0h]

The FW Region 3 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-4039. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 846Ch

Figure 14-2008. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4040. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4040. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.106 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register

14.1.8.2.106.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register (Offset = 470h) [reset = 0h]

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-4041. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8470h

Figure 14-2009. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4042. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.107 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register

14.1.8.2.107.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register (Offset = 474h) [reset = 0h]

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-4043. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8474h

Figure 14-2010. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4044. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.108 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register

14.1.8.2.108.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register (Offset = 478h) [reset = FFFh]

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-4045. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8478h

Figure 14-2011. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4046. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.109 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register

14.1.8.2.109.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register (Offset = 47Ch) [reset = 0h]

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 3 firewall.

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Table 14-4047. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 847Ch

Figure 14-2012. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_H</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4048. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.110 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register

14.1.8.2.110.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register (Offset = 480h) [reset = 0h]

The FW Region 4 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-4049. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8480h

Figure 14-2013. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4050. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.111 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register

14.1.8.2.111.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register (Offset = 484h) [reset = 0h]

The FW Region 4 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-4051. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8484h

Figure 14-2014. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4052. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4052. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.112 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register

14.1.8.2.112.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register (Offset = 488h) [reset = 0h]

The FW Region 4 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-4053. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8488h

Figure 14-2015. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4054. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4054. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.113 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register

14.1.8.2.113.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register (Offset = 48Ch) [reset = 0h]

The FW Region 4 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-4055. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 848Ch

Figure 14-2016. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4056. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4056. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.114 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register

14.1.8.2.114.1
CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register (Offset = 490h) [reset = 0h]

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-4057. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8490h

Figure 14-2017. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4058. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.115 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register

14.1.8.2.115.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register (Offset = 494h) [reset = 0h]

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-4059. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8494h

Figure 14-2018. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4060. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.116 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register

14.1.8.2.116.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register (Offset = 498h) [reset = FFFh]

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-4061. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 8498h

Figure 14-2019. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	6	5	4	3	2	1	0
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4062. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.117 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register

14.1.8.2.117.1
CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register (Offset = 49Ch) [reset = 0h]

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 4 firewall.

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Table 14-4063. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 849Ch

Figure 14-2020. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4064. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.118 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register

14.1.8.2.118.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register (Offset = 4A0h) [reset = 0h]

The FW Region 5 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-4065. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84A0h

Figure 14-2021. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4066. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.119 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register

14.1.8.2.119.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register (Offset = 4A4h) [reset = 0h]

The FW Region 5 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-4067. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84A4h

Figure 14-2022. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4068. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4068. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.120 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register

14.1.8.2.120.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register (Offset = 4A8h) [reset = 0h]

The FW Region 5 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-4069. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84A8h

Figure 14-2023. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4070. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4070. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.121 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register

14.1.8.2.121.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register (Offset = 4ACh) [reset = 0h]

The FW Region 5 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-4071. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84ACh

Figure 14-2024. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4072. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4072. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.122 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register

14.1.8.2.122.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register (Offset = 4B0h) [reset = 0h]

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-4073. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84B0h

Figure 14-2025. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_LSB							
R							
0h							

Table 14-4074. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.123 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register

14.1.8.2.123.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register (Offset = 4B4h) [reset = 0h]

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-4075. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84B4h

Figure 14-2026. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4076. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.124 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register

14.1.8.2.124.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register (Offset = 4B8h) [reset = FFFh]

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-4077. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84B8h

Figure 14-2027. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4078. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.125 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register

14.1.8.2.125.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register (Offset = 4BCh) [reset = 0h]

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 5 firewall.

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Table 14-4079. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84BCh

Figure 14-2028. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4080. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.126 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register

14.1.8.2.126.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register (Offset = 4C0h) [reset = 0h]

The FW Region 6 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-4081. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84C0h

Figure 14-2029. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4082. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.127 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register

14.1.8.2.127.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register (Offset = 4C4h) [reset = 0h]

The FW Region 6 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-4083. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84C4h

Figure 14-2030. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4084. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4084. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.128 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register

14.1.8.2.128.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register (Offset = 4C8h) [reset = 0h]

The FW Region 6 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-4085. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84C8h

Figure 14-2031. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4086. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4086. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.129 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register

14.1.8.2.129.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register (Offset = 4CCh) [reset = 0h]

The FW Region 6 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-4087. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84CCh

Figure 14-2032. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4088. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4088. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.130 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register

14.1.8.2.130.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register (Offset = 4D0h) [reset = 0h]

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-4089. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84D0h

Figure 14-2033. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">START_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">START_ADDRESS_L</td><td colspan="4">START_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">START_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4090. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.131 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register

14.1.8.2.131.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register (Offset = 4D4h) [reset = 0h]

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-4091. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84D4h

Figure 14-2034. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4092. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.132 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register

14.1.8.2.132.1

CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register (Offset = 4D8h) [reset = FFFh]

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-4093. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84D8h

Figure 14-2035. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">END_ADDRESS_L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">END_ADDRESS_L</td><td colspan="4">END_ADDRESS_LSB</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">END_ADDRESS_LSB</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFh</td></tr>
</table>

Table 14-4094. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.133 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register

14.1.8.2.133.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register (Offset = 4DCh) [reset = 0h]

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 6 firewall.

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Table 14-4095. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84DCh

Figure 14-2036. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4096. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.134 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register

14.1.8.2.134.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register (Offset = 4E0h) [reset = 0h]

The FW Region 7 Control Register defines the control fields for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-4097. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84E0h

Figure 14-2037. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
NONE						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
NONE			R/W1TS	R/W			
0h			0h	0h			

Table 14-4098. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions. Reset Source: domain_default_rst_mod_g_rst_n
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region. Reset Source: domain_default_rst_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	LOCK	R/W1TS	0h	Lock region. Once set region values cannot be modified. Reset Source: domain_default_rst_mod_g_rst_n
3:0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.135 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register

14.1.8.2.135.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register (Offset = 4E4h) [reset = 0h]

The FW Region 7 Permission 0 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-4099. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84E4h

Figure 14-2038. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4100. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4100. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.136 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register

14.1.8.2.136.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register (Offset = 4E8h) [reset = 0h]

The FW Region 7 Permission 1 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-4101. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84E8h

Figure 14-2039. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4102. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4102. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.137 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register

14.1.8.2.137.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register (Offset = 4ECh) [reset = 0h]

The FW Region 7 Permission 2 Register defines the permissions for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-4103. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84ECh

Figure 14-2040. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-4104. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	PRIV_ID	R/W	0h	Allowed privid. Reset Source: domain_default_rst_mod_g_rst_n
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n

Table 14-4104. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
5	SEC_USER_READ	R/W	0h	Secure user read allowed. Reset Source: domain_default_rst_mod_g_rst_n
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed. Reset Source: domain_default_rst_mod_g_rst_n
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed. Reset Source: domain_default_rst_mod_g_rst_n
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed. Reset Source: domain_default_rst_mod_g_rst_n
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed. Reset Source: domain_default_rst_mod_g_rst_n
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.138 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register

14.1.8.2.138.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register (Offset = 4F0h) [reset = 0h]

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-4105. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84F0h

Figure 14-2041. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
START_ADDRESS_L							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDRESS_L							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_L				START_ADDRESS_LSB			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
START_ADDRESS_LSB							
R							
0h							

Table 14-4106. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.139 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register

14.1.8.2.139.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register (Offset = 4F4h) [reset = 0h]

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-4107. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84F4h

Figure 14-2042. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
START_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDRESS_H							
R/W							
0h							

Table 14-4108. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.140 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register

14.1.8.2.140.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register (Offset = 4F8h) [reset = FFFh]

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-4109. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84F8h

Figure 14-2043. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Name Register

31	30	29	28	27	26	25	24
END_ADDRESS_L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDRESS_L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDRESS_L				END_ADDRESS_LSB			
R/W				R			
0h				FFFh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDRESS_LSB							
R							
FFFh							

Table 14-4110. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned. Reset Source: domain_default_rst_mod_g_rst_n
11:0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.141 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register

14.1.8.2.141.1 CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register (Offset = 4FCh) [reset = 0h]

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the target Isa3ss_am62a_main_0.ipcss_vbm_dst region 7 firewall.

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Table 14-4111. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	4502 84FCh

Figure 14-2044. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
END_ADDRESS_H							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDRESS_H							
R/W							
0h							

Table 14-4112. CBASS_FW_ISA3SS_AM62A_MAIN_0_IPCSS_VBM_DST_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.142 CBASS_GLB_PID Register

14.1.8.2.142.1 CBASS_GLB_PID Register (Offset = 0h) [reset = 66006102h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-4113. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1000h

Figure 14-2045. CBASS_GLB_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		600h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
600h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Ch					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		2h					

Table 14-4114. CBASS_GLB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: domain_default_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: domain_default_rst_mod_g_rst_n
27:16	FUNC	R	600h	Module ID Reset Source: domain_default_rst_mod_g_rst_n
15:11	RTL	R	Ch	RTL revision. Will vary depending on release. Reset Source: domain_default_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: domain_default_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: domain_default_rst_mod_g_rst_n
5:0	MINOR	R	2h	Minor revision Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.143 CBASS_GLB_DESTINATION_ID Register

14.1.8.2.143.1 CBASS_GLB_DESTINATION_ID Register (Offset = 4h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-4115. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1004h

Figure 14-2046. CBASS_GLB_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-4116. CBASS_GLB_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.144 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register

14.1.8.2.144.1 CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-4117. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1020h

Figure 14-2047. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-4118. CBASS_GLB_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_PEND	R/W	0h	Disables logging pending when set. Reset Source: domain_default_rst_mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.145 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register

14.1.8.2.145.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-4119. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1024h

Figure 14-2048. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-4120. CBASS_GLB_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. Reset Source: domain_default_rst_mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: domain_default_rst_mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.146 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register

14.1.8.2.146.1 CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-4121. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1028h

Figure 14-2049. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4122. CBASS_GLB_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: domain_default_rst_mod_g_rst_n
23:16	CODE	R	0h	Code. Reset Source: domain_default_rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.1.8.2.147 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register

14.1.8.2.147.1 CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-4123. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 102Ch

Figure 14-2050. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_L</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4124. CBASS_GLB_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.148 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register

14.1.8.2.148.1 CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-4125. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1030h

Figure 14-2051. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-4126. CBASS_GLB_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 16 bits. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.149 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register

14.1.8.2.149.1 CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-4127. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1034h

Figure 14-2052. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-4128. CBASS_GLB_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: domain_default_rst_mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: domain_default_rst_mod_g_rst_n
12	READ	R	0h	Read. Reset Source: domain_default_rst_mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: domain_default_rst_mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: domain_default_rst_mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: domain_default_rst_mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: domain_default_rst_mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.150 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register

14.1.8.2.150.1 CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data.

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Table 14-4129. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1038h

Figure 14-2053. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 14-4130. CBASS_GLB_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.151 CBASS_GLB_EXCEPTION_PEND_SET Register

14.1.8.2.151.1 CBASS_GLB_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = 0h]

The Exception Logging Pending Set Register allows to set the pend signal.

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Table 14-4131. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1040h

Figure 14-2054. CBASS_GLB_EXCEPTION_PEND_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PEND_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-4132. CBASS_GLB_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.1.8.2.152 CBASS_GLB_EXCEPTION_PEND_CLEAR Register

14.1.8.2.152.1 CBASS_GLB_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = 0h]

The Exception Logging Pending Clear Register allows to clear the pend signal.

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Table 14-4133. Instance Table

Instance Name	Physical Address
IPCSS_CBASS0	45B0 1044h

Figure 14-2055. CBASS_GLB_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-4134. CBASS_GLB_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: domain_default_rst_mod_g_rst_n

14.2 Device Configuration Registers

14.2.1 Control Module (CTRL_MMR)

14.2.1.1 General Purpose Control Registers

Note

CTRL_MMR is also known as CTRLMMR, and MAIN_CTRL_MMR0 is also known as CTRL_MMR0.

14.2.1.1.1 MAIN_CTRL_MMR

MAIN_CTRL_MMR

14.2.1.1.1.1 MAIN_CTRL_MMR Summaries

MAIN_CTRL_MMR Summaries

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
0h	32	MAIN_CTRL_MMR_CFG0_PID	0010 0000h
8h	32	MAIN_CTRL_MMR_CFG0_MMR_CFG1	0010 0008h
100h	32	MAIN_CTRL_MMR_CFG0_IPC_SET_J	0010 0100h + formula
140h	32	MAIN_CTRL_MMR_CFG0_IPC_SET16	0010 0140h
144h	32	MAIN_CTRL_MMR_CFG0_IPC_SET17	0010 0144h
148h	32	MAIN_CTRL_MMR_CFG0_IPC_SET18	0010 0148h
14Ch	32	MAIN_CTRL_MMR_CFG0_IPC_SET19	0010 014Ch
180h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR_J	0010 0180h + formula
1C0h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR16	0010 01C0h
1C4h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR17	0010 01C4h
1C8h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR18	0010 01C8h
1CCh	32	MAIN_CTRL_MMR_CFG0_IPC_CLR19	0010 01CCh
1008h	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK0	0010 1008h
100Ch	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK1	0010 100Ch
1010h	32	MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS	0010 1010h
1014h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	0010 1014h
1018h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE	0010 1018h
101Ch	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	0010 101Ch
1020h	32	MAIN_CTRL_MMR_CFG0_EOI	0010 1020h
1024h	32	MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS	0010 1024h
1028h	32	MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	0010 1028h
102Ch	32	MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	0010 102Ch
1030h	32	MAIN_CTRL_MMR_CFG0_FAULT_CLEAR	0010 1030h
1100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	0010 1100h
1108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY	0010 1108h
110Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY	0010 110Ch
1118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY	0010 1118h
2000h	32	MAIN_CTRL_MMR_CFG0_PID_PROXY	0010 2000h
2008h	32	MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY	0010 2008h
2100h	32	MAIN_CTRL_MMR_CFG0_IPC_SET_PROXY_J	0010 2100h + formula
2140h	32	MAIN_CTRL_MMR_CFG0_IPC_SET16_PROXY	0010 2140h
2144h	32	MAIN_CTRL_MMR_CFG0_IPC_SET17_PROXY	0010 2144h
2148h	32	MAIN_CTRL_MMR_CFG0_IPC_SET18_PROXY	0010 2148h
214Ch	32	MAIN_CTRL_MMR_CFG0_IPC_SET19_PROXY	0010 214Ch
2180h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR_PROXY_J	0010 2180h + formula
21C0h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR16_PROXY	0010 21C0h

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
21C4h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR17_PROXY	0010 21C4h
21C8h	32	MAIN_CTRL_MMR_CFG0_IPC_CLR18_PROXY	0010 21C8h
21CCh	32	MAIN_CTRL_MMR_CFG0_IPC_CLR19_PROXY	0010 21CCh
3008h	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	0010 3008h
300Ch	32	MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	0010 300Ch
3010h	32	MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	0010 3010h
3014h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	0010 3014h
3018h	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	0010 3018h
301Ch	32	MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	0010 301Ch
3020h	32	MAIN_CTRL_MMR_CFG0_EOI_PROXY	0010 3020h
3024h	32	MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	0010 3024h
3028h	32	MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	0010 3028h
302Ch	32	MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	0010 302Ch
3030h	32	MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	0010 3030h
3100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0	0010 3100h
3104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1	0010 3104h
3108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2	0010 3108h
310Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3	0010 310Ch
3110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4	0010 3110h
3114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5	0010 3114h
3118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6	0010 3118h
4044h	32	MAIN_CTRL_MMR_CFG0_ENET1_CTRL	0010 4044h
4048h	32	MAIN_CTRL_MMR_CFG0_ENET2_CTRL	0010 4048h
4130h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN	0010 4130h
4140h	32	MAIN_CTRL_MMR_CFG0_EPWM0_CTRL	0010 4140h
4144h	32	MAIN_CTRL_MMR_CFG0_EPWM1_CTRL	0010 4144h
4148h	32	MAIN_CTRL_MMR_CFG0_EPWM2_CTRL	0010 4148h
4200h	32	MAIN_CTRL_MMR_CFG0_TIMER0_CTRL	0010 4200h
4204h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL	0010 4204h
4208h	32	MAIN_CTRL_MMR_CFG0_TIMER2_CTRL	0010 4208h
420Ch	32	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL	0010 420Ch
4210h	32	MAIN_CTRL_MMR_CFG0_TIMER4_CTRL	0010 4210h
4214h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL	0010 4214h
4218h	32	MAIN_CTRL_MMR_CFG0_TIMER6_CTRL	0010 4218h
421Ch	32	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL	0010 421Ch
4220h	32	MAIN_CTRL_MMR_CFG0_TIMER8_CTRL	0010 4220h
4224h	32	MAIN_CTRL_MMR_CFG0_TIMER9_CTRL	0010 4224h
4228h	32	MAIN_CTRL_MMR_CFG0_TIMER10_CTRL	0010 4228h
422Ch	32	MAIN_CTRL_MMR_CFG0_TIMER11_CTRL	0010 422Ch
4230h	32	MAIN_CTRL_MMR_CFG0_TIMER12_CTRL	0010 4230h
4234h	32	MAIN_CTRL_MMR_CFG0_TIMER13_CTRL	0010 4234h
4238h	32	MAIN_CTRL_MMR_CFG0_TIMER14_CTRL	0010 4238h
423Ch	32	MAIN_CTRL_MMR_CFG0_TIMER15_CTRL	0010 423Ch

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
4280h	32	MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL	0010 4280h
4284h	32	MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL	0010 4284h
4288h	32	MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL	0010 4288h
428Ch	32	MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL	0010 428Ch
4290h	32	MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL	0010 4290h
4294h	32	MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL	0010 4294h
4298h	32	MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL	0010 4298h
429Ch	32	MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL	0010 429Ch
4300h	32	MAIN_CTRL_MMR_CFG0_C7XV_CTRL0	0010 4300h
4308h	32	MAIN_CTRL_MMR_CFG0_C7XV_CTRL1	0010 4308h
44C0h	32	MAIN_CTRL_MMR_CFG0_EMMC0_STAT	0010 44C0h
44D0h	32	MAIN_CTRL_MMR_CFG0_ADC0_CTRL	0010 44D0h
44F0h	32	MAIN_CTRL_MMR_CFG0_ADC0_CAL	0010 44F0h
4700h	32	MAIN_CTRL_MMR_CFG0_FSS0_CTRL0	0010 4700h
4704h	32	MAIN_CTRL_MMR_CFG0_FSS0_CTRL1	0010 4704h
4710h	32	MAIN_CTRL_MMR_CFG0_FSS1_CTRL0	0010 4710h
4750h	32	MAIN_CTRL_MMR_CFG0_DCC_STAT	0010 4750h
4760h	32	MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL	0010 4760h
4764h	32	MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL	0010 4764h
4770h	32	MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL	0010 4770h
4774h	32	MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL	0010 4774h
5008h	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK0	0010 5008h
500Ch	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK1	0010 500Ch
5100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	0010 5100h
5108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY	0010 5108h
510Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	0010 510Ch
5110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	0010 5110h
5118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY	0010 5118h
5120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY	0010 5120h
5124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY	0010 5124h
6044h	32	MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY	0010 6044h
6048h	32	MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY	0010 6048h
6130h	32	MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY	0010 6130h
6140h	32	MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY	0010 6140h
6144h	32	MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY	0010 6144h
6148h	32	MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY	0010 6148h
6200h	32	MAIN_CTRL_MMR_CFG0_TIMER0_CTRL_PROXY	0010 6200h
6204h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY	0010 6204h
6208h	32	MAIN_CTRL_MMR_CFG0_TIMER2_CTRL_PROXY	0010 6208h
620Ch	32	MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY	0010 620Ch
6210h	32	MAIN_CTRL_MMR_CFG0_TIMER4_CTRL_PROXY	0010 6210h

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
6214h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY	0010 6214h
6218h	32	MAIN_CTRL_MMR_CFG0_TIMER6_CTRL_PROXY	0010 6218h
621Ch	32	MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY	0010 621Ch
6220h	32	MAIN_CTRL_MMR_CFG0_TIMER8_CTRL_PROXY	0010 6220h
6224h	32	MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY	0010 6224h
6228h	32	MAIN_CTRL_MMR_CFG0_TIMER10_CTRL_PROXY	0010 6228h
622Ch	32	MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY	0010 622Ch
6230h	32	MAIN_CTRL_MMR_CFG0_TIMER12_CTRL_PROXY	0010 6230h
6234h	32	MAIN_CTRL_MMR_CFG0_TIMER13_CTRL_PROXY	0010 6234h
6238h	32	MAIN_CTRL_MMR_CFG0_TIMER14_CTRL_PROXY	0010 6238h
623Ch	32	MAIN_CTRL_MMR_CFG0_TIMER15_CTRL_PROXY	0010 623Ch
6280h	32	MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL_PROXY	0010 6280h
6284h	32	MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL_PROXY	0010 6284h
6288h	32	MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL_PROXY	0010 6288h
628Ch	32	MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL_PROXY	0010 628Ch
6290h	32	MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL_PROXY	0010 6290h
6294h	32	MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL_PROXY	0010 6294h
6298h	32	MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL_PROXY	0010 6298h
629Ch	32	MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL_PROXY	0010 629Ch
6300h	32	MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY	0010 6300h
6308h	32	MAIN_CTRL_MMR_CFG0_C7XV_CTRL1_PROXY	0010 6308h
64C0h	32	MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY	0010 64C0h
64D0h	32	MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY	0010 64D0h
64F0h	32	MAIN_CTRL_MMR_CFG0_ADC0_CAL_PROXY	0010 64F0h
6700h	32	MAIN_CTRL_MMR_CFG0_FSS0_CTRL0_PROXY	0010 6700h
6704h	32	MAIN_CTRL_MMR_CFG0_FSS0_CTRL1_PROXY	0010 6704h
6710h	32	MAIN_CTRL_MMR_CFG0_FSS1_CTRL0_PROXY	0010 6710h
6750h	32	MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY	0010 6750h
6760h	32	MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL_PROXY	0010 6760h
6764h	32	MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL_PROXY	0010 6764h
6770h	32	MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL_PROXY	0010 6770h
6774h	32	MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL_PROXY	0010 6774h
7008h	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	0010 7008h
700Ch	32	MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	0010 700Ch
7100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0	0010 7100h
7104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1	0010 7104h
7108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2	0010 7108h
710Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3	0010 710Ch
7110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4	0010 7110h
7114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5	0010 7114h
7118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6	0010 7118h
711Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7	0010 711Ch
7120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8	0010 7120h

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
7124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9	0010 7124h
7128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10	0010 7128h
712Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11	0010 712Ch
7130h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12	0010 7130h
7134h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13	0010 7134h
7138h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14	0010 7138h
8000h	32	MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL	0010 8000h
8010h	32	MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL	0010 8010h
8060h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL	0010 8060h
8064h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL	0010 8064h
8068h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL	0010 8068h
8070h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL	0010 8070h
807Ch	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL	0010 807Ch
8098h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL	0010 8098h
8140h	32	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL	0010 8140h
8160h	32	MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL	0010 8160h
81B0h	32	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL	0010 81B0h
81B4h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL	0010 81B4h
81B8h	32	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL	0010 81B8h
81BCh	32	MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL	0010 81BCh
81C0h	32	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL	0010 81C0h
81C4h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL	0010 81C4h
81C8h	32	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL	0010 81C8h
81CCh	32	MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL	0010 81CCh
81D0h	32	MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL	0010 81D0h
81D4h	32	MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL	0010 81D4h
81D8h	32	MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL	0010 81D8h
81DCh	32	MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL	0010 81DCh
81E0h	32	MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL	0010 81E0h
81E4h	32	MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL	0010 81E4h
81E8h	32	MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL	0010 81E8h
81ECh	32	MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL	0010 81ECh
8200h	32	MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL	0010 8200h
8204h	32	MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL	0010 8204h
8208h	32	MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL	0010 8208h
820Ch	32	MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL	0010 820Ch
8210h	32	MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL	0010 8210h
8240h	32	MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL	0010 8240h
8244h	32	MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL	0010 8244h
8248h	32	MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL	0010 8248h
824Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL	0010 824Ch
8250h	32	MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL	0010 8250h
8254h	32	MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL	0010 8254h
8258h	32	MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL	0010 8258h
8280h	32	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL	0010 8280h
8284h	32	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL	0010 8284h

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
8288h	32	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL	0010 8288h
828Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL	0010 828Ch
8290h	32	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL	0010 8290h
8294h	32	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL	0010 8294h
8298h	32	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL	0010 8298h
82B0h	32	MAIN_CTRL_MMR_CFG0_ATL_CLKSEL	0010 82B0h
82C0h	32	MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL	0010 82C0h
82C4h	32	MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL	0010 82C4h
82C8h	32	MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL	0010 82C8h
82CCh	32	MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL	0010 82CCh
82D0h	32	MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL	0010 82D0h
82D4h	32	MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL	0010 82D4h
82D8h	32	MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL	0010 82D8h
82DCh	32	MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL	0010 82DCh
82E0h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL	0010 82E0h
82E4h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL	0010 82E4h
82E8h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL	0010 82E8h
82F0h	32	MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL	0010 82F0h
8330h	32	MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL	0010 8330h
8334h	32	MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL	0010 8334h
8338h	32	MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL	0010 8338h
833Ch	32	MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL	0010 833Ch
8340h	32	MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL	0010 8340h
8350h	32	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL	0010 8350h
8354h	32	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL	0010 8354h
8358h	32	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL	0010 8358h
835Ch	32	MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL	0010 835Ch
8360h	32	MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL	0010 8360h
8380h	32	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL	0010 8380h
8384h	32	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL	0010 8384h
8388h	32	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL	0010 8388h
838Ch	32	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL	0010 838Ch
8390h	32	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL	0010 8390h
8394h	32	MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL	0010 8394h
83E0h	32	MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL	0010 83E0h
83E4h	32	MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL	0010 83E4h
83E8h	32	MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL	0010 83E8h
83ECh	32	MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL	0010 83ECh
83F0h	32	MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL	0010 83F0h
8480h	32	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL	0010 8480h
8484h	32	MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL	0010 8484h
8488h	32	MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL	0010 8488h
848Ch	32	MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL	0010 848Ch
8490h	32	MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL	0010 8490h
84C0h	32	MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL	0010 84C0h
84C4h	32	MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL	0010 84C4h

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
84C8h	32	MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL	0010 84C8h
84CCh	32	MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL	0010 84CCh
84D0h	32	MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL	0010 84D0h
84D4h	32	MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL	0010 84D4h
84D8h	32	MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL	0010 84D8h
84DCh	32	MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL	0010 84DCh
84E0h	32	MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL	0010 84E0h
84E4h	32	MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL	0010 84E4h
84E8h	32	MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL	0010 84E8h
84ECh	32	MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL	0010 84ECh
84F0h	32	MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL	0010 84F0h
84F4h	32	MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL	0010 84F4h
84F8h	32	MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL	0010 84F8h
84FCh	32	MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL	0010 84FCh
8500h	32	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL	0010 8500h
8504h	32	MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL	0010 8504h
8510h	32	MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL	0010 8510h
8580h	32	MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL	0010 8580h
8584h	32	MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL	0010 8584h
9008h	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK0	0010 9008h
900Ch	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK1	0010 900Ch
9100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY	0010 9100h
9104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY	0010 9104h
9108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY	0010 9108h
910Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY	0010 910Ch
9110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY	0010 9110h
9114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY	0010 9114h
9118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY	0010 9118h
911Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY	0010 911Ch
9124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY	0010 9124h
9128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY	0010 9128h
A000h	32	MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY	0010 A000h
A010h	32	MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY	0010 A010h
A060h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY	0010 A060h
A064h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY	0010 A064h
A068h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY	0010 A068h
A070h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL_PROXY	0010 A070h
A07Ch	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY	0010 A07Ch

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
A098h	32	MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY	0010 A098h
A140h	32	MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY	0010 A140h
A160h	32	MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY	0010 A160h
A1B0h	32	MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY	0010 A1B0h
A1B4h	32	MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY	0010 A1B4h
A1B8h	32	MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY	0010 A1B8h
A1BCh	32	MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY	0010 A1BCh
A1C0h	32	MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY	0010 A1C0h
A1C4h	32	MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY	0010 A1C4h
A1C8h	32	MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY	0010 A1C8h
A1CCh	32	MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY	0010 A1CCh
A1D0h	32	MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY	0010 A1D0h
A1D4h	32	MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY	0010 A1D4h
A1D8h	32	MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY	0010 A1D8h
A1DCh	32	MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY	0010 A1DCh
A1E0h	32	MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL_PROXY	0010 A1E0h
A1E4h	32	MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL_PROXY	0010 A1E4h
A1E8h	32	MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL_PROXY	0010 A1E8h
A1ECh	32	MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL_PROXY	0010 A1ECh
A200h	32	MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY	0010 A200h
A204h	32	MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY	0010 A204h
A208h	32	MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY	0010 A208h
A20Ch	32	MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY	0010 A20Ch
A210h	32	MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY	0010 A210h
A240h	32	MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY	0010 A240h
A244h	32	MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY	0010 A244h
A248h	32	MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY	0010 A248h
A24Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY	0010 A24Ch
A250h	32	MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY	0010 A250h
A254h	32	MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY	0010 A254h
A258h	32	MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY	0010 A258h
A280h	32	MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY	0010 A280h
A284h	32	MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY	0010 A284h
A288h	32	MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY	0010 A288h
A28Ch	32	MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY	0010 A28Ch
A290h	32	MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY	0010 A290h
A294h	32	MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY	0010 A294h
A298h	32	MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY	0010 A298h
A2B0h	32	MAIN_CTRL_MMR_CFG0_ATL_CLKSEL_PROXY	0010 A2B0h
A2C0h	32	MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL_PROXY	0010 A2C0h
A2C4h	32	MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL_PROXY	0010 A2C4h
A2C8h	32	MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL_PROXY	0010 A2C8h
A2CCh	32	MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL_PROXY	0010 A2CCh
A2D0h	32	MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL_PROXY	0010 A2D0h
A2D4h	32	MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL_PROXY	0010 A2D4h

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
A2D8h	32	MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL_PROXY	0010 A2D8h
A2DCh	32	MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL_PROXY	0010 A2DCh
A2E0h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY	0010 A2E0h
A2E4h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY	0010 A2E4h
A2E8h	32	MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL_PROXY	0010 A2E8h
A2F0h	32	MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL_PROXY	0010 A2F0h
A330h	32	MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY	0010 A330h
A334h	32	MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY	0010 A334h
A338h	32	MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY	0010 A338h
A33Ch	32	MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL_PROXY	0010 A33Ch
A340h	32	MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL_PROXY	0010 A340h
A350h	32	MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY	0010 A350h
A354h	32	MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY	0010 A354h
A358h	32	MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY	0010 A358h
A35Ch	32	MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL_PROXY	0010 A35Ch
A360h	32	MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL_PROXY	0010 A360h
A380h	32	MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY	0010 A380h
A384h	32	MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY	0010 A384h
A388h	32	MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY	0010 A388h
A38Ch	32	MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY	0010 A38Ch
A390h	32	MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY	0010 A390h
A394h	32	MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL_PROXY	0010 A394h
A3E0h	32	MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL_PROXY	0010 A3E0h
A3E4h	32	MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL_PROXY	0010 A3E4h
A3E8h	32	MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL_PROXY	0010 A3E8h
A3ECh	32	MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL_PROXY	0010 A3ECh
A3F0h	32	MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL_PROXY	0010 A3F0h
A480h	32	MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY	0010 A480h
A484h	32	MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY	0010 A484h
A488h	32	MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL_PROXY	0010 A488h
A48Ch	32	MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL_PROXY	0010 A48Ch
A490h	32	MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL_PROXY	0010 A490h
A4C0h	32	MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL_PROXY	0010 A4C0h
A4C4h	32	MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL_PROXY	0010 A4C4h
A4C8h	32	MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL_PROXY	0010 A4C8h
A4CCh	32	MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL_PROXY	0010 A4CCh

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
A4D0h	32	MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL_PROXY	0010 A4D0h
A4D4h	32	MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL_PROXY	0010 A4D4h
A4D8h	32	MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL_PROXY	0010 A4D8h
A4DCh	32	MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL_PROXY	0010 A4DCh
A4E0h	32	MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL_PROXY	0010 A4E0h
A4E4h	32	MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL_PROXY	0010 A4E4h
A4E8h	32	MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL_PROXY	0010 A4E8h
A4ECh	32	MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL_PROXY	0010 A4ECh
A4F0h	32	MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL_PROXY	0010 A4F0h
A4F4h	32	MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL_PROXY	0010 A4F4h
A4F8h	32	MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL_PROXY	0010 A4F8h
A4FCh	32	MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL_PROXY	0010 A4FCh
A500h	32	MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY	0010 A500h
A504h	32	MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL_PROXY	0010 A504h
A510h	32	MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY	0010 A510h
A580h	32	MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL_PROXY	0010 A580h
A584h	32	MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL_PROXY	0010 A584h
B008h	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY	0010 B008h
B00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY	0010 B00Ch
B100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0	0010 B100h
B104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1	0010 B104h
B108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2	0010 B108h
B10Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3	0010 B10Ch
B110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4	0010 B110h
B114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5	0010 B114h
B118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6	0010 B118h
B11Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7	0010 B11Ch
B120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8	0010 B120h
B124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9	0010 B124h
B128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10	0010 B128h
B12Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R11	0010 B12Ch
C000h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL	0010 C000h
C004h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT	0010 C004h
C008h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0	0010 C008h
C00Ch	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1	0010 C00Ch
C010h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0	0010 C010h
C014h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1	0010 C014h

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
C018h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT	0010 C018h
C01Ch	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR	0010 C01Ch
C020h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL	0010 C020h
C024h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT	0010 C024h
C028h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0	0010 C028h
C02Ch	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1	0010 C02Ch
C030h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0	0010 C030h
C034h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1	0010 C034h
C038h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT	0010 C038h
C03Ch	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR	0010 C03Ch
C280h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SIG	0010 C280h
C2A0h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SIG	0010 C2A0h
D008h	32	MAIN_CTRL_MMR_CFG0_LOCK3_KICK0	0010 D008h
D00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK3_KICK1	0010 D00Ch
D100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY	0010 D100h
D114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY	0010 D114h
E000h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL_PROXY	0010 E000h
E004h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT_PROXY	0010 E004h
E008h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0_PROXY	0010 E008h
E00Ch	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1_PROXY	0010 E00Ch
E010h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0_PROXY	0010 E010h
E014h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1_PROXY	0010 E014h
E018h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT_PROXY	0010 E018h
E01Ch	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR_PROXY	0010 E01Ch
E020h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL_PROXY	0010 E020h
E024h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT_PROXY	0010 E024h
E028h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0_PROXY	0010 E028h
E02Ch	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1_PROXY	0010 E02Ch
E030h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0_PROXY	0010 E030h
E034h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1_PROXY	0010 E034h
E038h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT_PROXY	0010 E038h
E03Ch	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR_PROXY	0010 E03Ch
E280h	32	MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SIG_PROXY	0010 E280h
E2A0h	32	MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SIG_PROXY	0010 E2A0h
F008h	32	MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY	0010 F008h
F00Ch	32	MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY	0010 F00Ch
F100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0	0010 F100h

Table 14-4135. MAIN_CTRL_MMR_CFG0 Registers, Base Address=0010 0000h, Length=131072 (continued)

Offset	Length	Register Name	MAIN_CTRL_MMR0 Physical Address
F104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1	0010 F104h
F108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2	0010 F108h
F10Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3	0010 F10Ch
F110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4	0010 F110h
F114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5	0010 F114h
11128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY	0011 1128h
11138h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY	0011 1138h
13100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0	0011 3100h
13104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1	0011 3104h
13108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2	0011 3108h
1310Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3	0011 310Ch
13110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4	0011 3110h
13114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5	0011 3114h
13118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6	0011 3118h
1311Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7	0011 311Ch
13120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8	0011 3120h
13124h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9	0011 3124h
13128h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10	0011 3128h
1312Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11	0011 312Ch
13130h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12	0011 3130h
13134h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R13	0011 3134h
13138h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14	0011 3138h
1B100h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0	0011 B100h
1B104h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1	0011 B104h
1B108h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2	0011 B108h
1B10Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3	0011 B10Ch
1B110h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4	0011 B110h
1B114h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5	0011 B114h
1B118h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6	0011 B118h
1B11Ch	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7	0011 B11Ch
1B120h	32	MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8	0011 B120h

14.2.1.1.1.2 MAIN_CTRL_MMR Registers

MAIN_CTRL_MMR Registers

14.2.1.1.1.2.1 MAIN_CTRL_MMR_CFG0_PID Register

14.2.1.1.1.2.1.1 MAIN_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-4136. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 0000h

Figure 14-2056. MAIN_CTRL_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MSB16							
R							
6180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PID_CUSTOM		PID_MINOR					
R		R					
0h		15h					

Table 14-4137. MAIN_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.1.2.2 MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register

14.2.1.1.1.2.2.1 MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 8000005Fh]

Indicates the MMR configuration

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Table 14-4138. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 0008h

Figure 14-2057. MAIN_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
5Fh							

Table 14-4139. MAIN_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	5Fh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.1.2.3 MAIN_CTRL_MMR_CFG0_IPC_SET_j Register

14.2.1.1.1.2.3.1 MAIN_CTRL_MMR_CFG0_IPC_SET_j Register (Offset = 100h) [reset = 0h]

Generate interprocessor communication interrupt to C71x core0

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Table 14-4140. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 0100h + formula

Figure 14-2058. MAIN_CTRL_MMR_CFG0_IPC_SET_j Name Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4141. MAIN_CTRL_MMR_CFG0_IPC_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SRC_SET	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.4 MAIN_CTRL_MMR_CFG0_IPC_SET16 Register

14.2.1.1.1.2.4.1 MAIN_CTRL_MMR_CFG0_IPC_SET16 Register (Offset = 140h) [reset = 0h]

Generate interprocessor communication interrupt to MAIN R5 cluster0 core0

Return to Summary Table

Table 14-4142. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 0140h

Figure 14-2059. MAIN_CTRL_MMR_CFG0_IPC_SET16 Name Register

31	30	29	28	27	26	25	24
IPC_SET16_IPC_SRC_SET							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
IPC_SET16_IPC_SRC_SET							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
IPC_SET16_IPC_SRC_SET							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
IPC_SET16_IPC_SRC_SET				RESERVED			IPC_SET16_IPC_SET
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4143. MAIN_CTRL_MMR_CFG0_IPC_SET16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET16_IPC_SRC_SET	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET16_IPC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.5 MAIN_CTRL_MMR_CFG0_IPC_SET17 Register

14.2.1.1.1.2.5.1 MAIN_CTRL_MMR_CFG0_IPC_SET17 Register (Offset = 144h) [reset = 0h]

Generate interprocessor communication interrupt to MAIN R5 cluster0 core1

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Table 14-4144. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 0144h

Figure 14-2060. MAIN_CTRL_MMR_CFG0_IPC_SET17 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_SET17_IPC_SRC_SET</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_SET17_IPC_SRC_SET</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_SET17_IPC_SRC_SET</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_SET17_IPC_SRC_SET</td><td colspan="3">RESERVED</td><td>IPC_SET17_IPC_SET</td></tr>
<tr><td colspan="4">R/W1TS</td><td colspan="3">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-4145. MAIN_CTRL_MMR_CFG0_IPC_SET17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET17_IPC_SRC_SET	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET17_IPC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.6 MAIN_CTRL_MMR_CFG0_IPC_SET18 Register

14.2.1.1.1.2.6.1 MAIN_CTRL_MMR_CFG0_IPC_SET18 Register (Offset = 148h) [reset = 0h]

Generate interprocessor communication interrupt to MAIN R5 cluster1 core0

Return to Summary Table

Table 14-4146. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 0148h

Figure 14-2061. MAIN_CTRL_MMR_CFG0_IPC_SET18 Name Register

31	30	29	28	27	26	25	24
IPC_SET18_IPC_SRC_SET							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPC_SET18_IPC_SRC_SET							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPC_SET18_IPC_SRC_SET							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPC_SET18_IPC_SRC_SET				RESERVED			IPC_SET18_IPC_SET
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4147. MAIN_CTRL_MMR_CFG0_IPC_SET18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET18_IPC_SRC_SET	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET18_IPC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.7 MAIN_CTRL_MMR_CFG0_IPC_SET19 Register

14.2.1.1.1.2.7.1 MAIN_CTRL_MMR_CFG0_IPC_SET19 Register (Offset = 14Ch) [reset = 0h]

Generate interprocessor communication interrupt to MAIN R5 cluster1 core1

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Table 14-4148. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 014Ch

Figure 14-2062. MAIN_CTRL_MMR_CFG0_IPC_SET19 Name Register

31	30	29	28	27	26	25	24
IPC_SET19_IPC_SRC_SET							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPC_SET19_IPC_SRC_SET							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPC_SET19_IPC_SRC_SET							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPC_SET19_IPC_SRC_SET				RESERVED			IPC_SET19_IPC_SET
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4149. MAIN_CTRL_MMR_CFG0_IPC_SET19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET19_IPC_SRC_SET	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET19_IPC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.8 MAIN_CTRL_MMR_CFG0_IPC_CLR_j Register

14.2.1.1.1.2.8.1 MAIN_CTRL_MMR_CFG0_IPC_CLR_j Register (Offset = 180h) [reset = 0h]

Acknowledge interprocessor communication interrupt to C71x core0

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Table 14-4150. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 0180h + formula

Figure 14-2063. MAIN_CTRL_MMR_CFG0_IPC_CLR_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_SRC_CLR</td><td colspan="3">RESERVED</td><td>IPC_CLR</td></tr>
<tr><td colspan="4">R/W1TC</td><td colspan="3">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-4151. MAIN_CTRL_MMR_CFG0_IPC_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SRC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.9 MAIN_CTRL_MMR_CFG0_IPC_CLR16 Register

14.2.1.1.1.2.9.1 MAIN_CTRL_MMR_CFG0_IPC_CLR16 Register (Offset = 1C0h) [reset = 0h]

Acknowledge interprocessor communication interrupt to MAIN R5 cluster0 core0

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Table 14-4152. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 01C0h

Figure 14-2064. MAIN_CTRL_MMR_CFG0_IPC_CLR16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_CLR16_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_CLR16_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_CLR16_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_CLR16_IPC_SRC_CLR</td><td colspan="3">RESERVED</td><td>IPC_CLR16_IPC_CLR</td></tr>
<tr><td colspan="4">R/W1TC</td><td colspan="3">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-4153. MAIN_CTRL_MMR_CFG0_IPC_CLR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR16_IPC_SRC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR16_IPC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.10 MAIN_CTRL_MMR_CFG0_IPC_CLR17 Register

14.2.1.1.1.2.10.1 MAIN_CTRL_MMR_CFG0_IPC_CLR17 Register (Offset = 1C4h) [reset = 0h]

Acknowledge interprocessor communication interrupt to MAIN R5 cluster0 core1

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Table 14-4154. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 01C4h

Figure 14-2065. MAIN_CTRL_MMR_CFG0_IPC_CLR17 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_CLR17_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_CLR17_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_CLR17_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_CLR17_IPC_SRC_CLR</td><td colspan="3">RESERVED</td><td>IPC_CLR17_IPC_CLR</td></tr>
<tr><td colspan="4">R/W1TC</td><td colspan="3">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-4155. MAIN_CTRL_MMR_CFG0_IPC_CLR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR17_IPC_SRC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR17_IPC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.11 MAIN_CTRL_MMR_CFG0_IPC_CLR18 Register

14.2.1.1.1.2.11.1 MAIN_CTRL_MMR_CFG0_IPC_CLR18 Register (Offset = 1C8h) [reset = 0h]

Acknowledge interprocessor communication interrupt to MAIN R5 cluster1 core2

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Table 14-4156. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 01C8h

Figure 14-2066. MAIN_CTRL_MMR_CFG0_IPC_CLR18 Name Register

31	30	29	28	27	26	25	24
IPC_CLR18_IPC_SRC_CLR							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
IPC_CLR18_IPC_SRC_CLR							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
IPC_CLR18_IPC_SRC_CLR							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
IPC_CLR18_IPC_SRC_CLR				RESERVED			IPC_CLR18_IPC_CLR
R/W1TC				NONE			R/W1TC
0h				0h			0h

Table 14-4157. MAIN_CTRL_MMR_CFG0_IPC_CLR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR18_IPC_SRC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR18_IPC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.12 MAIN_CTRL_MMR_CFG0_IPC_CLR19 Register

14.2.1.1.1.2.12.1 MAIN_CTRL_MMR_CFG0_IPC_CLR19 Register (Offset = 1CCh) [reset = 0h]

Acknowledge interprocessor communication interrupt to MAIN R5 cluster1 core3

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Table 14-4158. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 01CCh

Figure 14-2067. MAIN_CTRL_MMR_CFG0_IPC_CLR19 Name Register

31	30	29	28	27	26	25	24
IPC_CLR19_IPC_SRC_CLR							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
IPC_CLR19_IPC_SRC_CLR							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
IPC_CLR19_IPC_SRC_CLR							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
IPC_CLR19_IPC_SRC_CLR				RESERVED			IPC_CLR19_IPC_CLR
R/W1TC				NONE			R/W1TC
0h				0h			0h

Table 14-4159. MAIN_CTRL_MMR_CFG0_IPC_CLR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR19_IPC_SRC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR19_IPC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.13 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register

14.2.1.1.1.2.13.1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-4160. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1008h

Figure 14-2068. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-4161. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.14 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register

14.2.1.1.1.2.14.1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-4162. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 100Ch

Figure 14-2069. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-4163. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.15 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

14.2.1.1.1.2.15.1 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-4164. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1010h

Figure 14-2070. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>PROXY_ERR</td><td>KICK_ERR</td><td>ADDR_ERR</td><td>PROT_ERR</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-4165. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.16 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

14.2.1.1.1.2.16.1 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-4166. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1014h

Figure 14-2071. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-4167. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.17 MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register

14.2.1.1.1.2.17.1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-4168. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1018h

Figure 14-2072. MAIN_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-4169. MAIN_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.18 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

14.2.1.1.1.2.18.1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-4170. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 101Ch

Figure 14-2073. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-4171. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.19 MAIN_CTRL_MMR_CFG0_EOI Register

14.2.1.1.1.2.19.1 MAIN_CTRL_MMR_CFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-4172. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1020h

Figure 14-2074. MAIN_CTRL_MMR_CFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-4173. MAIN_CTRL_MMR_CFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.1.2.20 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register

14.2.1.1.1.2.20.1 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-4174. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1024h

Figure 14-2075. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-4175. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.1.2.21 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

14.2.1.1.1.2.21.1 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-4176. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1028h

Figure 14-2076. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-4177. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.1.2.22 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

14.2.1.1.1.2.22.1 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-4178. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 102Ch

Figure 14-2077. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 14-4179. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.1.2.23 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register

14.2.1.1.1.2.23.1 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-4180. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1030h

Figure 14-2078. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-4181. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.24 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

14.2.1.1.1.2.24.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4182. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1100h

Figure 14-2079. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-4183. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.25 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register

14.2.1.1.1.2.25.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register (Offset = 1108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4184. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1108h

Figure 14-2080. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4185. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.26 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register

14.2.1.1.1.2.26.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register (Offset = 110Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-4186. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 110Ch

Figure 14-2081. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3_READONLY							
R							
0h							

Table 14-4187. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.27 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register

14.2.1.1.1.2.27.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register (Offset = 1118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4188. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 1118h

Figure 14-2082. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R6_READONLY							
R							
0h							

Table 14-4189. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.28 MAIN_CTRL_MMR_CFG0_PID_PROXY Register

14.2.1.1.1.2.28.1 MAIN_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800215h]

PID register

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Table 14-4190. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 2000h

Figure 14-2083. MAIN_CTRL_MMR_CFG0_PID_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC_PROXY</td><td colspan="3">PID_MAJOR_PROXY</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM_PROXY</td><td colspan="6">PID_MINOR_PROXY</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-4191. MAIN_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.1.2.29 MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

14.2.1.1.1.2.29.1 MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 8000005Fh]

Indicates the MMR configuration

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Table 14-4192. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 2008h

Figure 14-2084. MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS_PROXY							
R							
5Fh							

Table 14-4193. MAIN_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	5Fh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.1.2.30 MAIN_CTRL_MMR_CFG0_IPC_SET_PROXY_j Register

14.2.1.1.1.2.30.1 MAIN_CTRL_MMR_CFG0_IPC_SET_PROXY_j Register (Offset = 2100h) [reset = 0h]

Generate interprocessor communication interrupt to C71x core0

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Table 14-4194. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 2100h + formula

Figure 14-2085. MAIN_CTRL_MMR_CFG0_IPC_SET_PROXY_j Name Register

31	30	29	28	27	26	25	24
IPC_SRC_SET_PROXY							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPC_SRC_SET_PROXY							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPC_SRC_SET_PROXY							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPC_SRC_SET_PROXY				RESERVED			IPC_SET_PROXY
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4195. MAIN_CTRL_MMR_CFG0_IPC_SET_PROXY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SRC_SET_PROXY	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.31 MAIN_CTRL_MMR_CFG0_IPC_SET16_PROXY Register

14.2.1.1.1.2.31.1 MAIN_CTRL_MMR_CFG0_IPC_SET16_PROXY Register (Offset = 2140h) [reset = 0h]

Generate interprocessor communication interrupt to MAIN R5 cluster0 core0

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Table 14-4196. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 2140h

Figure 14-2086. MAIN_CTRL_MMR_CFG0_IPC_SET16_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_SET16_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPC_SET16_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPC_SET16_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPC_SET16_IPC_SRC_SET_PROXY				RESERVED			IPC_SET16_IPC_SET_PROXY
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4197. MAIN_CTRL_MMR_CFG0_IPC_SET16_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET16_IPC_SRC_SET_PROXY	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET16_IPC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.32 MAIN_CTRL_MMR_CFG0_IPC_SET17_PROXY Register

14.2.1.1.1.2.32.1 MAIN_CTRL_MMR_CFG0_IPC_SET17_PROXY Register (Offset = 2144h) [reset = 0h]

Generate interprocessor communication interrupt to MAIN R5 cluster0 core1

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Table 14-4198. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 2144h

Figure 14-2087. MAIN_CTRL_MMR_CFG0_IPC_SET17_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_SET17_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
IPC_SET17_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
IPC_SET17_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
IPC_SET17_IPC_SRC_SET_PROXY				RESERVED			IPC_SET17_IPC_SET_PROXY
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4199. MAIN_CTRL_MMR_CFG0_IPC_SET17_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET17_IPC_SRC_SET_PROXY	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET17_IPC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.33 MAIN_CTRL_MMR_CFG0_IPC_SET18_PROXY Register

14.2.1.1.1.2.33.1 MAIN_CTRL_MMR_CFG0_IPC_SET18_PROXY Register (Offset = 2148h) [reset = 0h]

Generate interprocessor communication interrupt to MAIN R5 cluster1 core0

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Table 14-4200. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 2148h

Figure 14-2088. MAIN_CTRL_MMR_CFG0_IPC_SET18_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_SET18_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
IPC_SET18_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
IPC_SET18_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
IPC_SET18_IPC_SRC_SET_PROXY				RESERVED			IPC_SET18_IPC_SET_PROXY
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4201. MAIN_CTRL_MMR_CFG0_IPC_SET18_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET18_IPC_SRC_SET_PROXY	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET18_IPC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.34 MAIN_CTRL_MMR_CFG0_IPC_SET19_PROXY Register

14.2.1.1.1.2.34.1 MAIN_CTRL_MMR_CFG0_IPC_SET19_PROXY Register (Offset = 214Ch) [reset = 0h]

Generate interprocessor communication interrupt to MAIN R5 cluster1 core1

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Table 14-4202. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 214Ch

Figure 14-2089. MAIN_CTRL_MMR_CFG0_IPC_SET19_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_SET19_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPC_SET19_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPC_SET19_IPC_SRC_SET_PROXY							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPC_SET19_IPC_SRC_SET_PROXY				RESERVED			IPC_SET19_IPC_SET_PROXY
R/W1TS				NONE			R/W1TS
0h				0h			0h

Table 14-4203. MAIN_CTRL_MMR_CFG0_IPC_SET19_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET19_IPC_SRC_SET_PROXY	R/W1TS	0h	Read returns current value Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET19_IPC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.35 MAIN_CTRL_MMR_CFG0_IPC_CLR_PROXY_j Register

14.2.1.1.1.2.35.1 MAIN_CTRL_MMR_CFG0_IPC_CLR_PROXY_j Register (Offset = 2180h) [reset = 0h]

Acknowledge interprocessor communication interrupt to C71x core0

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Table 14-4204. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 2180h + formula

Figure 14-2090. MAIN_CTRL_MMR_CFG0_IPC_CLR_PROXY_j Name Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR_PROXY				RESERVED			IPC_CLR_PROXY
R/W1TC				NONE			R/W1TC
0h				0h			0h

Table 14-4205. MAIN_CTRL_MMR_CFG0_IPC_CLR_PROXY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SRC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.36 MAIN_CTRL_MMR_CFG0_IPC_CLR16_PROXY Register

14.2.1.1.1.2.36.1 MAIN_CTRL_MMR_CFG0_IPC_CLR16_PROXY Register (Offset = 21C0h) [reset = 0h]

Acknowledge interprocessor communication interrupt to MAIN R5 cluster0 core0

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Table 14-4206. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 21C0h

Figure 14-2091. MAIN_CTRL_MMR_CFG0_IPC_CLR16_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_CLR16_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_CLR16_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_CLR16_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_CLR16_IPC_SRC_CLR_PROXY</td><td colspan="3">RESERVED</td><td>IPC_CLR16_IPC_CLR_PROXY</td></tr>
<tr><td colspan="4">R/W1TC</td><td colspan="3">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-4207. MAIN_CTRL_MMR_CFG0_IPC_CLR16_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR16_IPC_SRC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR16_IPC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.37 MAIN_CTRL_MMR_CFG0_IPC_CLR17_PROXY Register

14.2.1.1.1.2.37.1 MAIN_CTRL_MMR_CFG0_IPC_CLR17_PROXY Register (Offset = 21C4h) [reset = 0h]

Acknowledge interprocessor communication interrupt to MAIN R5 cluster0 core1

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Table 14-4208. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 21C4h

Figure 14-2092. MAIN_CTRL_MMR_CFG0_IPC_CLR17_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_CLR17_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
IPC_CLR17_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
IPC_CLR17_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
IPC_CLR17_IPC_SRC_CLR_PROXY				RESERVED			IPC_CLR17_IPC_CLR_PROXY
R/W1TC				NONE			R/W1TC
0h				0h			0h

Table 14-4209. MAIN_CTRL_MMR_CFG0_IPC_CLR17_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR17_IPC_SRC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR17_IPC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.38 MAIN_CTRL_MMR_CFG0_IPC_CLR18_PROXY Register

14.2.1.1.1.2.38.1 MAIN_CTRL_MMR_CFG0_IPC_CLR18_PROXY Register (Offset = 21C8h) [reset = 0h]

Acknowledge interprocessor communication interrupt to MAIN R5 cluster1 core2

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Table 14-4210. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 21C8h

Figure 14-2093. MAIN_CTRL_MMR_CFG0_IPC_CLR18_PROXY Name Register

31	30	29	28	27	26	25	24
IPC_CLR18_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
IPC_CLR18_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
IPC_CLR18_IPC_SRC_CLR_PROXY							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
IPC_CLR18_IPC_SRC_CLR_PROXY				RESERVED			IPC_CLR18_IPC_CLR_PROXY
R/W1TC				NONE			R/W1TC
0h				0h			0h

Table 14-4211. MAIN_CTRL_MMR_CFG0_IPC_CLR18_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR18_IPC_SRC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR18_IPC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.39 MAIN_CTRL_MMR_CFG0_IPC_CLR19_PROXY Register

14.2.1.1.1.2.39.1 MAIN_CTRL_MMR_CFG0_IPC_CLR19_PROXY Register (Offset = 21CCh) [reset = 0h]

Acknowledge interprocessor communication interrupt to MAIN R5 cluster1 core3

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Table 14-4212. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 21CCh

Figure 14-2094. MAIN_CTRL_MMR_CFG0_IPC_CLR19_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_CLR19_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_CLR19_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_CLR19_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_CLR19_IPC_SRC_CLR_PROXY</td><td colspan="3">RESERVED</td><td>IPC_CLR19_IPC_CLR_PROXY</td></tr>
<tr><td colspan="4">R/W1TC</td><td colspan="3">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-4213. MAIN_CTRL_MMR_CFG0_IPC_CLR19_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR19_IPC_SRC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR19_IPC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.40 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

14.2.1.1.1.2.40.1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-4214. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3008h

Figure 14-2095. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-4215. MAIN_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.41 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

14.2.1.1.1.2.41.1 MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-4216. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 300Ch

Figure 14-2096. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-4217. MAIN_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.42 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

14.2.1.1.1.2.42.1 MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-4218. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3010h

Figure 14-2097. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-4219. MAIN_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.43 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

14.2.1.1.1.2.43.1 MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-4220. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3014h

Figure 14-2098. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-4221. MAIN_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.44 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

14.2.1.1.1.2.44.1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-4222. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3018h

Figure 14-2099. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-4223. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.45 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

14.2.1.1.1.2.45.1 MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-4224. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 301Ch

Figure 14-2100. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-4225. MAIN_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.46 MAIN_CTRL_MMR_CFG0_EOI_PROXY Register

14.2.1.1.1.2.46.1 MAIN_CTRL_MMR_CFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-4226. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3020h

Figure 14-2101. MAIN_CTRL_MMR_CFG0_EOI_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EOI_VECTOR_PROXY							
R/W							
0h							

Table 14-4227. MAIN_CTRL_MMR_CFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.1.2.47 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

14.2.1.1.1.2.47.1 MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-4228. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3024h

Figure 14-2102. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-4229. MAIN_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.1.2.48 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

14.2.1.1.1.2.48.1 MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-4230. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3028h

Figure 14-2103. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-4231. MAIN_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.1.2.49 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

14.2.1.1.1.2.49.1 MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-4232. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 302Ch

Figure 14-2104. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-4233. MAIN_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.1.2.50 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

14.2.1.1.1.2.50.1 MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-4234. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3030h

Figure 14-2105. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-4235. MAIN_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.1.2.51 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

14.2.1.1.1.2.51.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4236. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3100h

Figure 14-2106. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-4237. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.52 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register

14.2.1.1.1.2.52.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register (Offset = 3104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4238. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3104h

Figure 14-2107. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1							
R/W							
0h							

Table 14-4239. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.53 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register

14.2.1.1.1.2.53.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register (Offset = 3108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4240. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3108h

Figure 14-2108. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2							
R/W							
0h							

Table 14-4241. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.54 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register

14.2.1.1.1.2.54.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register (Offset = 310Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-4242. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 310Ch

Figure 14-2109. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3							
R/W							
0h							

Table 14-4243. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.55 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register

14.2.1.1.1.2.55.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register (Offset = 3110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4244. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3110h

Figure 14-2110. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4							
R/W							
0h							

Table 14-4245. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.56 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register

14.2.1.1.1.2.56.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register (Offset = 3114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4246. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3114h

Figure 14-2111. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5							
R/W							
0h							

Table 14-4247. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.57 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register

14.2.1.1.1.2.57.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register (Offset = 3118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-4248. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 3118h

Figure 14-2112. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R6							
R/W							
0h							

Table 14-4249. MAIN_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.58 MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register

14.2.1.1.1.2.58.1 MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register (Offset = 4044h) [reset = 2h]

Controls Ethernet Port1 operation

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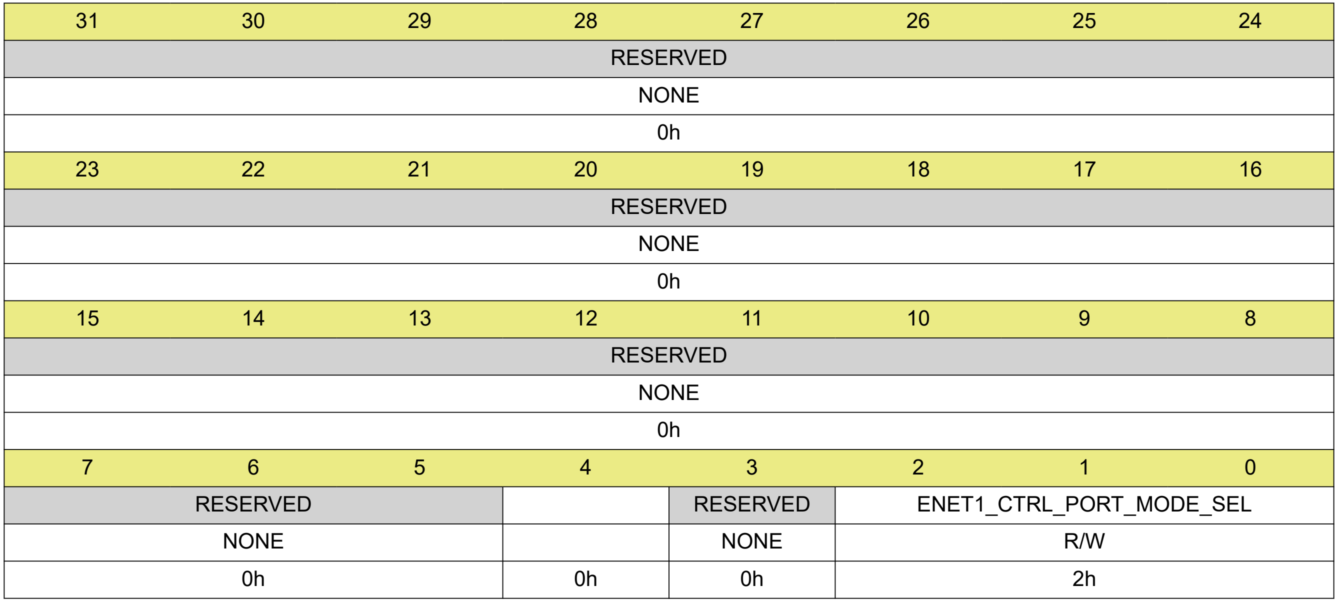
Table 14-4250. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4044h

Figure 14-2113. MAIN_CTRL_MMR_CFG0_ENET1_CTRL Name Register



31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	ENET1_CTRL_PORT_MODE_SEL		
NONE				NONE	R/W		
0h			0h	0h	2h		

Table 14-4251. MAIN_CTRL_MMR_CFG0_ENET1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET1_CTRL_PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port1 interface Field values (others are reserved): 3'b000 - GMII/MII (not supported) 3'b001 - RMII 3'b010 - RGMII 3'b011 - SGMII 3'b100 - QSGMII (not supported) 3'b101 - XFI (not supported) 3'b110 - QSGMII_SUB (not supported) 3'b111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.59 MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register

14.2.1.1.1.2.59.1 MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register (Offset = 4048h) [reset = 2h]

Controls Ethernet Port2 operation

Return to Summary Table

Table 14-4252. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4048h

Figure 14-2114. MAIN_CTRL_MMR_CFG0_ENET2_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td></td><td>RESERVED</td><td colspan="3">ENET2_CTRL_PORT_MODE_SEL</td></tr>
<tr><td colspan="3">NONE</td><td></td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
</table>

Table 14-4253. MAIN_CTRL_MMR_CFG0_ENET2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET2_CTRL_PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port2 interface Field values (others are reserved): 3'b000 - GMII/MII (not supported) 3'b001 - RMII 3'b010 - RGMII 3'b011 - SGMII 3'b100 - QSGMII (not supported) 3'b101 - XFI (not supported) 3'b110 - QSGMII_SUB (not supported) 3'b111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.60 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register

14.2.1.1.1.2.60.1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register (Offset = 4130h) [reset = 0h]

Controls Timebase Counter of EPWM Modules

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Table 14-4254. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4130h

Figure 14-2115. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM_TB_CLKEN_EPWM2_TB_CLKEN	EPWM_TB_CLKEN_EPWM1_TB_CLKEN	EPWM_TB_CLKEN_EPWM0_TB_CLKEN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-4255. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	EPWM_TB_CLKEN_EPWM2_TB_CLKEN	R/W	0h	Enabled Timebase Clock of EPWM2 When Set Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_EPWM1_TB_CLKEN	R/W	0h	EnablesTimebase Clock of EPWM1 When Set Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_EPWM0_TB_CLKEN	R/W	0h	EnablesTimebase Clock of EPWM0 When Set Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n

14.2.1.1.1.2.61 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register

14.2.1.1.1.2.61.1 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register (Offset = 4140h) [reset = 0h]

Controls EPWM0 Operation

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Table 14-4256. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4140h

Figure 14-2116. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">EPWM0_CTRL_SYNCIN_SEL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>EPWM0_CTRL_EALLOW</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4257. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM0_CTRL_SYNCIN_SEL	R/W	0h	Selects the source of the EPWM0 synchronization input Field values (others are reserved): 3'b000 - EPWM0_SYNCIN (Pin) undefined - undefined 3'b010 - TimeSync Intr Router outl.20 3'b011 - CPSW CPTS Compare Event Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM0_CTRL_EALLOW	R/W	0h	Enable write access to EPWM tripzone registers Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.62 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register

14.2.1.1.1.2.62.1 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register (Offset = 4144h) [reset = 0h]

Controls EPWM1 Operation

Return to Summary Table

Table 14-4258. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4144h

Figure 14-2117. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>EPWM1_CTRL_EALLOW</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4259. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM1_CTRL_EALLOW	R/W	0h	Enable write access to EPWM tripzone registers Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.63 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register

14.2.1.1.1.2.63.1 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register (Offset = 4148h) [reset = 0h]

Controls EPWM2 Operation

Return to Summary Table

Table 14-4260. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4148h

Figure 14-2118. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM2_CTRL_EALLOW	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4261. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM2_CTRL_EALLOW	R/W	0h	Enable write access to EPWM tripzone registers Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.64 MAIN_CTRL_MMR_CFG0_TIMER0_CTRL Register

14.2.1.1.1.2.64.1 MAIN_CTRL_MMR_CFG0_TIMER0_CTRL Register (Offset = 4200h) [reset = 0h]

Controls TIMER0 operation

Return to Summary Table

Table 14-4262. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4200h

Figure 14-2119. MAIN_CTRL_MMR_CFG0_TIMER0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER0_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4263. MAIN_CTRL_MMR_CFG0_TIMER0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER0_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER0 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.65 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register

14.2.1.1.1.2.65.1 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register (Offset = 4204h) [reset = 0h]

Controls TIMER1 operation

Return to Summary Table

Table 14-4264. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4204h

Figure 14-2120. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER1_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TIMER1_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4265. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER1_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER1 to TIMER0 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER1_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER1 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.66 MAIN_CTRL_MMR_CFG0_TIMER2_CTRL Register

14.2.1.1.1.2.66.1 MAIN_CTRL_MMR_CFG0_TIMER2_CTRL Register (Offset = 4208h) [reset = 0h]

Controls TIMER2 operation

Return to Summary Table

Table 14-4266. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4208h

Figure 14-2121. MAIN_CTRL_MMR_CFG0_TIMER2_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TIMER2_CTRL_CAP_SEL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4267. MAIN_CTRL_MMR_CFG0_TIMER2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER2_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER2 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.67 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register

14.2.1.1.1.2.67.1 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register (Offset = 420Ch) [reset = 0h]

Controls TIMER3 operation

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Table 14-4268. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 420Ch

Figure 14-2122. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>TIMER3_CTRL_CASCADE_EN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TIMER3_CTRL_CAP_SEL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4269. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER3_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER3 to TIMER2 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER3_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER3 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.68 MAIN_CTRL_MMR_CFG0_TIMER4_CTRL Register

14.2.1.1.1.2.68.1 MAIN_CTRL_MMR_CFG0_TIMER4_CTRL Register (Offset = 4210h) [reset = 0h]

Controls TIMER4 operation

Return to Summary Table

Table 14-4270. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4210h

Figure 14-2123. MAIN_CTRL_MMR_CFG0_TIMER4_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TIMER4_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4271. MAIN_CTRL_MMR_CFG0_TIMER4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER4_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER4 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.69 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register

14.2.1.1.1.2.69.1 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register (Offset = 4214h) [reset = 0h]

Controls TIMER5 operation

Return to Summary Table

Table 14-4272. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4214h

Figure 14-2124. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TIMER5_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TIMER5_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4273. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER5_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER5 to TIMER4 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER5_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER5 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.70 MAIN_CTRL_MMR_CFG0_TIMER6_CTRL Register

14.2.1.1.1.2.70.1 MAIN_CTRL_MMR_CFG0_TIMER6_CTRL Register (Offset = 4218h) [reset = 0h]

Controls TIMER6 operation

Return to Summary Table

Table 14-4274. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4218h

Figure 14-2125. MAIN_CTRL_MMR_CFG0_TIMER6_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER6_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4275. MAIN_CTRL_MMR_CFG0_TIMER6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER6_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER6 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.71 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register

14.2.1.1.1.2.71.1 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register (Offset = 421Ch) [reset = 0h]

Controls TIMER7 operation

Return to Summary Table

Table 14-4276. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 421Ch

Figure 14-2126. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							TIMER7_CTRL_CASCADE_EN
NONE							R/W
0h							0h

7	6	5	4	3	2	1	0
RESERVED					TIMER7_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4277. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER7_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER7 to TIMER6 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER7_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER7 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.72 MAIN_CTRL_MMR_CFG0_TIMER8_CTRL Register

14.2.1.1.1.2.72.1 MAIN_CTRL_MMR_CFG0_TIMER8_CTRL Register (Offset = 4220h) [reset = 0h]

Controls TIMER8 operation

Return to Summary Table

Table 14-4278. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4220h

Figure 14-2127. MAIN_CTRL_MMR_CFG0_TIMER8_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER8_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4279. MAIN_CTRL_MMR_CFG0_TIMER8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER8_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER8 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.73 MAIN_CTRL_MMR_CFG0_TIMER9_CTRL Register

14.2.1.1.1.2.73.1 MAIN_CTRL_MMR_CFG0_TIMER9_CTRL Register (Offset = 4224h) [reset = 0h]

Controls TIMER9 operation

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Table 14-4280. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4224h

Figure 14-2128. MAIN_CTRL_MMR_CFG0_TIMER9_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TIMER9_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TIMER9_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4281. MAIN_CTRL_MMR_CFG0_TIMER9_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER9_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER9 to TIMER8 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER9_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER9 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.74 MAIN_CTRL_MMR_CFG0_TIMER10_CTRL Register

14.2.1.1.1.2.74.1 MAIN_CTRL_MMR_CFG0_TIMER10_CTRL Register (Offset = 4228h) [reset = 0h]

Controls TIMER10 operation

Return to Summary Table

Table 14-4282. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4228h

Figure 14-2129. MAIN_CTRL_MMR_CFG0_TIMER10_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TIMER10_CTRL_CAP_SEL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4283. MAIN_CTRL_MMR_CFG0_TIMER10_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER10_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER10 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.75 MAIN_CTRL_MMR_CFG0_TIMER11_CTRL Register

14.2.1.1.1.2.75.1 MAIN_CTRL_MMR_CFG0_TIMER11_CTRL Register (Offset = 422Ch) [reset = 0h]

Controls TIMER11 operation

Return to Summary Table

Table 14-4284. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 422Ch

Figure 14-2130. MAIN_CTRL_MMR_CFG0_TIMER11_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER11_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TIMER11_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4285. MAIN_CTRL_MMR_CFG0_TIMER11_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER11_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER11 to TIMER10 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER11_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER11 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.76 MAIN_CTRL_MMR_CFG0_TIMER12_CTRL Register

14.2.1.1.1.2.76.1 MAIN_CTRL_MMR_CFG0_TIMER12_CTRL Register (Offset = 4230h) [reset = 0h]

Controls TIMER12 operation

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Table 14-4286. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4230h

Figure 14-2131. MAIN_CTRL_MMR_CFG0_TIMER12_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER12_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4287. MAIN_CTRL_MMR_CFG0_TIMER12_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER12_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER12 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.77 MAIN_CTRL_MMR_CFG0_TIMER13_CTRL Register

14.2.1.1.1.2.77.1 MAIN_CTRL_MMR_CFG0_TIMER13_CTRL Register (Offset = 4234h) [reset = 0h]

Controls TIMER13 operation

Return to Summary Table

Table 14-4288. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4234h

Figure 14-2132. MAIN_CTRL_MMR_CFG0_TIMER13_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER13_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TIMER13_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4289. MAIN_CTRL_MMR_CFG0_TIMER13_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER13_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER13 to TIMER12 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER13_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER13 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.78 MAIN_CTRL_MMR_CFG0_TIMER14_CTRL Register

14.2.1.1.1.2.78.1 MAIN_CTRL_MMR_CFG0_TIMER14_CTRL Register (Offset = 4238h) [reset = 0h]

Controls TIMER14 operation

Return to Summary Table

Table 14-4290. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4238h

Figure 14-2133. MAIN_CTRL_MMR_CFG0_TIMER14_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TIMER14_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4291. MAIN_CTRL_MMR_CFG0_TIMER14_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER14_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER14 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.79 MAIN_CTRL_MMR_CFG0_TIMER15_CTRL Register

14.2.1.1.1.2.79.1 MAIN_CTRL_MMR_CFG0_TIMER15_CTRL Register (Offset = 423Ch) [reset = 0h]

Controls TIMER15 operation

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Table 14-4292. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 423Ch

Figure 14-2134. MAIN_CTRL_MMR_CFG0_TIMER15_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TIMER15_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TIMER15_CTRL_CAP_SEL		
NONE					R/W		
0h					0h		

Table 14-4293. MAIN_CTRL_MMR_CFG0_TIMER15_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER15_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER15 to TIMER14 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER15_CTRL_CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER15 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.80 MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL Register

14.2.1.1.1.2.80.1 MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL Register (Offset = 4280h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4294. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4280h

Figure 14-2135. MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO0_CTRL_OUT_SEL			
NONE				R/W			
0h				0h			

Table 14-4295. MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO0_CTRL_OUT_SEL	R/W	0h	Selects the source of the TIMERIO0 output Field values (others are reserved): 4'b0000 - TIMERIO0 is driven by TIMER0 output 4'b0001 - TIMERIO0 is driven by TIMER1 output 4'b0010 - TIMERIO0 is driven by TIMER2 output 4'b0011 - TIMERIO0 is driven by TIMER3 output 4'b0100 - TIMERIO0 is driven by TIMER4 output 4'b0101 - TIMERIO0 is driven by TIMER5 output 4'b0110 - TIMERIO0 is driven by TIMER6 output 4'b0111 - TIMERIO0 is driven by TIMER7 output 4'b1000 - TIMERIO0 is driven by TIMER8 output 4'b1001 - TIMERIO0 is driven by TIMER9 output 4'b1010 - TIMERIO0 is driven by TIMER10 output 4'b1011 - TIMERIO0 is driven by TIMER11 output 4'b1100 - TIMERIO0 is driven by TIMER12 output 4'b1101 - TIMERIO0 is driven by TIMER13 output 4'b1110 - TIMERIO0 is driven by TIMER14 output 4'b1111 - TIMERIO0 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.81 MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL Register

14.2.1.1.1.2.81.1 MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL Register (Offset = 4284h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4296. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4284h

Figure 14-2136. MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO1_CTRL_OUT_SEL			
NONE				R/W			
0h				0h			

Table 14-4297. MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO1_CTRL_OUT_SEL	R/W	0h	Selects the source of the TIMERIO1 output Field values (others are reserved): 4'b0000 - TIMERIO1 is driven by TIMER0 output 4'b0001 - TIMERIO1 is driven by TIMER1 output 4'b0010 - TIMERIO1 is driven by TIMER2 output 4'b0011 - TIMERIO1 is driven by TIMER3 output 4'b0100 - TIMERIO1 is driven by TIMER4 output 4'b0101 - TIMERIO1 is driven by TIMER5 output 4'b0110 - TIMERIO1 is driven by TIMER6 output 4'b0111 - TIMERIO1 is driven by TIMER7 output 4'b1000 - TIMERIO1 is driven by TIMER8 output 4'b1001 - TIMERIO1 is driven by TIMER9 output 4'b1010 - TIMERIO1 is driven by TIMER10 output 4'b1011 - TIMERIO1 is driven by TIMER11 output 4'b1100 - TIMERIO1 is driven by TIMER12 output 4'b1101 - TIMERIO1 is driven by TIMER13 output 4'b1110 - TIMERIO1 is driven by TIMER14 output 4'b1111 - TIMERIO1 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.82 MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL Register

14.2.1.1.1.2.82.1 MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL Register (Offset = 4288h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4298. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4288h

Figure 14-2137. MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMERIO2_CTRL_OUT_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4299. MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO2_CTRL_OUT_SEL	R/W	0h	Selects the source of the TIMERIO2 output Field values (others are reserved): 4'b0000 - TIMERIO2 is driven by TIMER0 output 4'b0001 - TIMERIO2 is driven by TIMER1 output 4'b0010 - TIMERIO2 is driven by TIMER2 output 4'b0011 - TIMERIO2 is driven by TIMER3 output 4'b0100 - TIMERIO2 is driven by TIMER4 output 4'b0101 - TIMERIO2 is driven by TIMER5 output 4'b0110 - TIMERIO2 is driven by TIMER6 output 4'b0111 - TIMERIO2 is driven by TIMER7 output 4'b1000 - TIMERIO2 is driven by TIMER8 output 4'b1001 - TIMERIO2 is driven by TIMER9 output 4'b1010 - TIMERIO2 is driven by TIMER10 output 4'b1011 - TIMERIO2 is driven by TIMER11 output 4'b1100 - TIMERIO2 is driven by TIMER12 output 4'b1101 - TIMERIO2 is driven by TIMER13 output 4'b1110 - TIMERIO2 is driven by TIMER14 output 4'b1111 - TIMERIO2 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.83 MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL Register

14.2.1.1.1.2.83.1 MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL Register (Offset = 428Ch) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4300. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 428Ch

Figure 14-2138. MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO3_CTRL_OUT_SEL			
NONE				R/W			
0h				0h			

Table 14-4301. MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO3_CTRL_OUT_SEL	R/W	0h	Selects the source of the TIMERIO3 output Field values (others are reserved): 4'b0000 - TIMERIO3 is driven by TIMER0 output 4'b0001 - TIMERIO3 is driven by TIMER1 output 4'b0010 - TIMERIO3 is driven by TIMER2 output 4'b0011 - TIMERIO3 is driven by TIMER3 output 4'b0100 - TIMERIO3 is driven by TIMER4 output 4'b0101 - TIMERIO3 is driven by TIMER5 output 4'b0110 - TIMERIO3 is driven by TIMER6 output 4'b0111 - TIMERIO3 is driven by TIMER7 output 4'b1000 - TIMERIO3 is driven by TIMER8 output 4'b1001 - TIMERIO3 is driven by TIMER9 output 4'b1010 - TIMERIO3 is driven by TIMER10 output 4'b1011 - TIMERIO3 is driven by TIMER11 output 4'b1100 - TIMERIO3 is driven by TIMER12 output 4'b1101 - TIMERIO3 is driven by TIMER13 output 4'b1110 - TIMERIO3 is driven by TIMER14 output 4'b1111 - TIMERIO3 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.84 MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL Register

14.2.1.1.1.2.84.1 MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL Register (Offset = 4290h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4302. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4290h

Figure 14-2139. MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO4_CTRL_OUT_SEL			
NONE				R/W			
0h				0h			

Table 14-4303. MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO4_CTRL_OUT_SEL	R/W	0h	Selects the source of the TIMERIO4 output Field values (others are reserved): 4'b0000 - TIMERIO4 is driven by TIMER0 output 4'b0001 - TIMERIO4 is driven by TIMER1 output 4'b0010 - TIMERIO4 is driven by TIMER2 output 4'b0011 - TIMERIO4 is driven by TIMER3 output 4'b0100 - TIMERIO4 is driven by TIMER4 output 4'b0101 - TIMERIO4 is driven by TIMER5 output 4'b0110 - TIMERIO4 is driven by TIMER6 output 4'b0111 - TIMERIO4 is driven by TIMER7 output 4'b1000 - TIMERIO4 is driven by TIMER8 output 4'b1001 - TIMERIO4 is driven by TIMER9 output 4'b1010 - TIMERIO4 is driven by TIMER10 output 4'b1011 - TIMERIO4 is driven by TIMER11 output 4'b1100 - TIMERIO4 is driven by TIMER12 output 4'b1101 - TIMERIO4 is driven by TIMER13 output 4'b1110 - TIMERIO4 is driven by TIMER14 output 4'b1111 - TIMERIO4 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.85 MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL Register

14.2.1.1.1.2.85.1 MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL Register (Offset = 4294h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4304. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4294h

Figure 14-2140. MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO5_CTRL_OUT_SEL			
NONE				R/W			
0h				0h			

Table 14-4305. MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO5_CTRL_OUT_SEL	R/W	0h	Selects the source of the TIMERIO5 output Field values (others are reserved): 4'b0000 - TIMERIO5 is driven by TIMER0 output 4'b0001 - TIMERIO5 is driven by TIMER1 output 4'b0010 - TIMERIO5 is driven by TIMER2 output 4'b0011 - TIMERIO5 is driven by TIMER3 output 4'b0100 - TIMERIO5 is driven by TIMER4 output 4'b0101 - TIMERIO5 is driven by TIMER5 output 4'b0110 - TIMERIO5 is driven by TIMER6 output 4'b0111 - TIMERIO5 is driven by TIMER7 output 4'b1000 - TIMERIO5 is driven by TIMER8 output 4'b1001 - TIMERIO5 is driven by TIMER9 output 4'b1010 - TIMERIO5 is driven by TIMER10 output 4'b1011 - TIMERIO5 is driven by TIMER11 output 4'b1100 - TIMERIO5 is driven by TIMER12 output 4'b1101 - TIMERIO5 is driven by TIMER13 output 4'b1110 - TIMERIO5 is driven by TIMER14 output 4'b1111 - TIMERIO5 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.86 MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL Register

14.2.1.1.1.2.86.1 MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL Register (Offset = 4298h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4306. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4298h

Figure 14-2141. MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMERIO6_CTRL_OUT_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4307. MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO6_CTRL_OUT_SEL	R/W	0h	Selects the source of the TIMERIO6 output Field values (others are reserved): 4'b0000 - TIMERIO6 is driven by TIMER0 output 4'b0001 - TIMERIO6 is driven by TIMER1 output 4'b0010 - TIMERIO6 is driven by TIMER2 output 4'b0011 - TIMERIO6 is driven by TIMER3 output 4'b0100 - TIMERIO6 is driven by TIMER4 output 4'b0101 - TIMERIO6 is driven by TIMER5 output 4'b0110 - TIMERIO6 is driven by TIMER6 output 4'b0111 - TIMERIO6 is driven by TIMER7 output 4'b1000 - TIMERIO6 is driven by TIMER8 output 4'b1001 - TIMERIO6 is driven by TIMER9 output 4'b1010 - TIMERIO6 is driven by TIMER10 output 4'b1011 - TIMERIO6 is driven by TIMER11 output 4'b1100 - TIMERIO6 is driven by TIMER12 output 4'b1101 - TIMERIO6 is driven by TIMER13 output 4'b1110 - TIMERIO6 is driven by TIMER14 output 4'b1111 - TIMERIO6 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.87 MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL Register

14.2.1.1.1.2.87.1 MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL Register (Offset = 429Ch) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4308. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 429Ch

Figure 14-2142. MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMERIO7_CTRL_OUT_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4309. MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO7_CTRL_OUT_SEL	R/W	0h	Selects the source of the TIMERIO7 output Field values (others are reserved): 4'b0000 - TIMERIO7 is driven by TIMER0 output 4'b0001 - TIMERIO7 is driven by TIMER1 output 4'b0010 - TIMERIO7 is driven by TIMER2 output 4'b0011 - TIMERIO7 is driven by TIMER3 output 4'b0100 - TIMERIO7 is driven by TIMER4 output 4'b0101 - TIMERIO7 is driven by TIMER5 output 4'b0110 - TIMERIO7 is driven by TIMER6 output 4'b0111 - TIMERIO7 is driven by TIMER7 output 4'b1000 - TIMERIO7 is driven by TIMER8 output 4'b1001 - TIMERIO7 is driven by TIMER9 output 4'b1010 - TIMERIO7 is driven by TIMER10 output 4'b1011 - TIMERIO7 is driven by TIMER11 output 4'b1100 - TIMERIO7 is driven by TIMER12 output 4'b1101 - TIMERIO7 is driven by TIMER13 output 4'b1110 - TIMERIO7 is driven by TIMER14 output 4'b1111 - TIMERIO7 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.88 MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register

14.2.1.1.1.2.88.1 MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register (Offset = 4300h) [reset = 3F3Fh]

Controls Relaxed Ordering by OrderID for the C7xv0 L2 Memory from external accesses. Ordering of accesses to the same 4KB L2 Block is relaxed either between Reads (more strict) or Between both Reads and Writes (more relaxed)

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Table 14-4310. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4300h

Figure 14-2143. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
C7XV_CTRL0_ORD15	C7XV_CTRL0_ORD14	C7XV_CTRL0_ORD13	C7XV_CTRL0_ORD12	C7XV_CTRL0_ORD11	C7XV_CTRL0_ORD10	C7XV_CTRL0_ORD9	C7XV_CTRL0_ORD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
C7XV_CTRL0_ORD7	C7XV_CTRL0_ORD6	C7XV_CTRL0_ORD5	C7XV_CTRL0_ORD4	C7XV_CTRL0_ORD3	C7XV_CTRL0_ORD2	C7XV_CTRL0_ORD1	C7XV_CTRL0_ORD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h

Table 14-4311. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	C7XV_CTRL0_ORD15	R/W	0h	Ordering Rule for Order ID 15 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
14	C7XV_CTRL0_ORD14	R/W	0h	Ordering Rule for Order ID 14 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
13	C7XV_CTRL0_ORD13	R/W	1h	Ordering Rule for Order ID 13 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

Table 14-4311. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	C7XV_CTRL0_ORD12	R/W	1h	Ordering Rule for Order ID 12 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
11	C7XV_CTRL0_ORD11	R/W	1h	Ordering Rule for Order ID 11 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
10	C7XV_CTRL0_ORD10	R/W	1h	Ordering Rule for Order ID 10 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
9	C7XV_CTRL0_ORD9	R/W	1h	Ordering Rule for Order ID 9 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
8	C7XV_CTRL0_ORD8	R/W	1h	Ordering Rule for Order ID 8 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
7	C7XV_CTRL0_ORD7	R/W	0h	Ordering Rule for Order ID 7 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
6	C7XV_CTRL0_ORD6	R/W	0h	Ordering Rule for Order ID 6 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
5	C7XV_CTRL0_ORD5	R/W	1h	Ordering Rule for Order ID 5 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
4	C7XV_CTRL0_ORD4	R/W	1h	Ordering Rule for Order ID 4 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
3	C7XV_CTRL0_ORD3	R/W	1h	Ordering Rule for Order ID 3 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
2	C7XV_CTRL0_ORD2	R/W	1h	Ordering Rule for Order ID 2 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

Table 14-4311. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	C7XV_CTRL0_ORD1	R/W	1h	Ordering Rule for Order ID 1 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
0	C7XV_CTRL0_ORD0	R/W	1h	Ordering Rule for Order ID 0 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

14.2.1.1.1.2.89 MAIN_CTRL_MMR_CFG0_C7XV_CTRL1 Register

14.2.1.1.1.2.89.1 MAIN_CTRL_MMR_CFG0_C7XV_CTRL1 Register (Offset = 4308h) [reset = 3F3Fh]

Controls Relaxed Ordering by OrderID for the C7xv1 L2 Memory from external accesses. Ordering of accesses to the same 4KB L2 Block is relaxed either between Reads (more strict) or Between both Reads and Writes (more relaxed)

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Table 14-4312. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4308h

Figure 14-2144. MAIN_CTRL_MMR_CFG0_C7XV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
C7XV_CTRL1_ORD15	C7XV_CTRL1_ORD14	C7XV_CTRL1_ORD13	C7XV_CTRL1_ORD12	C7XV_CTRL1_ORD11	C7XV_CTRL1_ORD10	C7XV_CTRL1_ORD9	C7XV_CTRL1_ORD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
C7XV_CTRL1_ORD7	C7XV_CTRL1_ORD6	C7XV_CTRL1_ORD5	C7XV_CTRL1_ORD4	C7XV_CTRL1_ORD3	C7XV_CTRL1_ORD2	C7XV_CTRL1_ORD1	C7XV_CTRL1_ORD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h

Table 14-4313. MAIN_CTRL_MMR_CFG0_C7XV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	C7XV_CTRL1_ORD15	R/W	0h	Ordering Rule for Order ID 15 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
14	C7XV_CTRL1_ORD14	R/W	0h	Ordering Rule for Order ID 14 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
13	C7XV_CTRL1_ORD13	R/W	1h	Ordering Rule for Order ID 13 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

Table 14-4313. MAIN_CTRL_MMR_CFG0_C7XV_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	C7XV_CTRL1_ORD12	R/W	1h	Ordering Rule for Order ID 12 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
11	C7XV_CTRL1_ORD11	R/W	1h	Ordering Rule for Order ID 11 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
10	C7XV_CTRL1_ORD10	R/W	1h	Ordering Rule for Order ID 10 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
9	C7XV_CTRL1_ORD9	R/W	1h	Ordering Rule for Order ID 9 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
8	C7XV_CTRL1_ORD8	R/W	1h	Ordering Rule for Order ID 8 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
7	C7XV_CTRL1_ORD7	R/W	0h	Ordering Rule for Order ID 7 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
6	C7XV_CTRL1_ORD6	R/W	0h	Ordering Rule for Order ID 6 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
5	C7XV_CTRL1_ORD5	R/W	1h	Ordering Rule for Order ID 5 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
4	C7XV_CTRL1_ORD4	R/W	1h	Ordering Rule for Order ID 4 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
3	C7XV_CTRL1_ORD3	R/W	1h	Ordering Rule for Order ID 3 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
2	C7XV_CTRL1_ORD2	R/W	1h	Ordering Rule for Order ID 2 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

Table 14-4313. MAIN_CTRL_MMR_CFG0_C7XV_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	C7XV_CTRL1_ORD1	R/W	1h	Ordering Rule for Order ID 1 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
0	C7XV_CTRL1_ORD0	R/W	1h	Ordering Rule for Order ID 0 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

14.2.1.1.1.2.90 MAIN_CTRL_MMR_CFG0_EMMC0_STAT Register

14.2.1.1.1.2.90.1 MAIN_CTRL_MMR_CFG0_EMMC0_STAT Register (Offset = 44C0h) [reset = 0h]

For determining state of MMCSD 1.8V Signalling

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Table 14-4314. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 44C0h

Figure 14-2145. MAIN_CTRL_MMR_CFG0_EMMC0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							EMMC0_STAT_SIG1P8_EN
NONE							R
0h							X

Table 14-4315. MAIN_CTRL_MMR_CFG0_EMMC0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC0_STAT_SIG1P8_EN	R	X	Status of 1.8V Signal Activate from EMMC0 Module Field values (others are reserved): 1'b0 - DISABLE_1P8V_SIGNALLING 1'b1 - ENABLE_1P8V_SIGNALLING Reset Source: mod_g_rst_n

14.2.1.1.1.2.91 MAIN_CTRL_MMR_CFG0_ADC0_CTRL Register

14.2.1.1.1.2.91.1 MAIN_CTRL_MMR_CFG0_ADC0_CTRL Register (Offset = 44D0h) [reset = 0h]

Controls operation of ADC0

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Table 14-4316. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 44D0h

Figure 14-2146. MAIN_CTRL_MMR_CFG0_ADC0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							ADC0_CTRL_GPI_MODE_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ADC0_CTRL_TRIG_SEL				
NONE			R/W				
0h			0h				

Table 14-4317. MAIN_CTRL_MMR_CFG0_ADC0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ADC0_CTRL_GPI_MODE_EN	R/W	0h	Enables ADC0 data pins to be used as general purpose inputs when set. This signal is tied to the en_dig_test input of MCU_ADC0 Reset Source: mod_g_rst_n
15:5	RESERVED	NONE	0h	Reserved

Table 14-4317. MAIN_CTRL_MMR_CFG0_ADC0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ADC0_CTRL_TRIG_SEL	R/W	0h	Selects the source of the ADC hardware event trigger Field values (others are reserved): 5'b00000 - ADC_EXT_TRIGGER0 (Pin) 5'b00001 - 0 - Reserved 5'b00010 - EPWM SOCA_OUT 5'b00011 - EPWM SOCB_OUT 5'b00100 - 0 - Reserved 5'b00101 - 0 - Reserved 5'b00110 - 0 - Reserved 5'b00111 - 0 - Reserved 5'b01000 - 0 - Reserved 5'b01001 - 0 - Reserved 5'b01010 - 0 - Reserved 5'b01011 - 0 - Reserved 5'b01100 - 0 - Reserved 5'b01101 - 0 - Reserved 5'b01110 - WKUP_TIMER0 PWM 5'b01111 - WKUP_TIMER1 PWM 5'b10000 - TIMER0 PWM 5'b10001 - TIMER1 PWM 5'b10010 - TIMER2 PWM 5'b10011 - TIMER3 PWM 5'b10100 - TIMER4 PWM 5'b10101 - TIMER5 PWM 5'b10110 - TIMER6 PWM 5'b10111 - TIMER7 PWM 5'b11000 - TIMER8 PWM 5'b11001 - TIMER9 PWM 5'b11010 - TIMER10 PWM 5'b11011 - TIMER11 PWM 5'b11100 - TIMER12 PWM 5'b11101 - TIMER13_PWM 5'b11110 - TIMER14_pWM 5'b11111 - Timer15_PWM Reset Source: mod_g_rst_n

14.2.1.1.1.2.92 MAIN_CTRL_MMR_CFG0_ADC0_CAL Register

14.2.1.1.1.2.92.1 MAIN_CTRL_MMR_CFG0_ADC0_CAL Register (Offset = 44F0h) [reset = 0h]

Controls ADC0 calibration sequence (not used)

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Table 14-4318. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 44F0h

Figure 14-2147. MAIN_CTRL_MMR_CFG0_ADC0_CAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADC0_CAL_CAL_EN	ADC0_CAL_DIFF_CAL_EN	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
7	6	5	4	3	2	1	0
RESERVED			ADC0_CAL_CAL_CAP_SEL				
NONE			R/W				
0h			0h				

Table 14-4319. MAIN_CTRL_MMR_CFG0_ADC0_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	ADC0_CAL_CAL_EN	R/W	0h	Enable single-ended calibration Set to 1 to begin single-ended calibration Reset Source: mod_g_rst_n
14	ADC0_CAL_DIFF_CAL_EN	R/W	0h	Enable differential calibration Set to 1 to begin differential calibration Reset Source: mod_g_rst_n
13:5	RESERVED	NONE	0h	Reserved
4:0	ADC0_CAL_CAL_CAP_SEL	R/W	0h	Select capacitor for calibration Bits correspond to C5:C1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.93 MAIN_CTRL_MMR_CFG0_FSS0_CTRL0 Register

14.2.1.1.1.2.93.1 MAIN_CTRL_MMR_CFG0_FSS0_CTRL0 Register (Offset = 4700h) [reset = 0h]

Controls Flash boot region size for Flash Subsystem0

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Table 14-4320. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4700h

Figure 14-2148. MAIN_CTRL_MMR_CFG0_FSS0_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				FSS0_CTRL0_S0_BOOT_SEG			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
FSS0_CTRL0_S0_BOOT_SEG							
R/W							
0h							
7	6	5	4	3	2	1	0
FSS0_CTRL0_S0_BOOT_SEG							
R/W							
0h							

Table 14-4321. MAIN_CTRL_MMR_CFG0_FSS0_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	FSS0_CTRL0_S0_BOOT_SEG	R/W	0h	Selects the flash boot segment size Field values (others are reserved): 20'h00001 - 4 kB 20'h00002 - 8 kB 20'h00004 - 16 kB 20'h00008 - 32 kB 20'h00010 - 64 kB 20'h00020 - 128 kB 20'h00040 - 256 kB 20'h00080 - 512 kB 20'h00100 - 1 MB 20'h00200 - 2 MB 20'h00400 - 4 MB 20'h00800 - 8 MB 20'h01000 - 16 MB 20'h02000 - 32 MB 20'h04000 - 64 MB 20'h08000 - 128 MB 20'h10000 - 256 MB 20'h20000 - 512 MB 20'h40000 - 1 GB 20'h80000 - 2 GB Reset Source: mod_g_rst_n

14.2.1.1.1.2.94 MAIN_CTRL_MMR_CFG0_FSS0_CTRL1 Register

14.2.1.1.1.2.94.1 MAIN_CTRL_MMR_CFG0_FSS0_CTRL1 Register (Offset = 4704h) [reset = 0h]

Controls Flash boot region placement for Flash Subsystem0

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Table 14-4322. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4704h

Figure 14-2149. MAIN_CTRL_MMR_CFG0_FSS0_CTRL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FSS0_CTRL1_S0_BOOT_MASK</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FSS0_CTRL1_S0_BOOT_MASK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FSS0_CTRL1_S0_BOOT_MASK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4323. MAIN_CTRL_MMR_CFG0_FSS0_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	FSS0_CTRL1_S0_BOOT_MASK	R/W	0h	Determines which (upper 20) address bits to replace with boot_seg signals when accessing the Boot Region (Region 1) Reset Source: mod_g_rst_n

14.2.1.1.1.2.95 MAIN_CTRL_MMR_CFG0_FSS1_CTRL0 Register

14.2.1.1.1.2.95.1 MAIN_CTRL_MMR_CFG0_FSS1_CTRL0 Register (Offset = 4710h) [reset = 0h]

Controls Flash boot region size and placement for Flash Subsystem1

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Table 14-4324. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4710h

Figure 14-2150. MAIN_CTRL_MMR_CFG0_FSS1_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td></td></tr>
<tr><td colspan="7">NONE</td><td></td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6"></td></tr>
<tr><td colspan="2">NONE</td><td colspan="6"></td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>FSS1_CTRL0_S0_BOOT_SIZE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">FSS1_CTRL0_S0_BOOT_SEG</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-4325. MAIN_CTRL_MMR_CFG0_FSS1_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
23:22	RESERVED	NONE	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	FSS1_CTRL0_S0_BOOT_SIZE	R/W	0h	Selects the size of the boot block to be used for the S0 (OSPI1) flash interface Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	FSS1_CTRL0_S0_BOOT_SEG	R/W	0h	Selects the boot block to be used for the S0 (OSPI1) flash interface. If the s0_boot_size is 128 MB then only bits [4:0] of this field are used. Care must be taken to account for the address translation as to not fall off or wrap the address of the flash. (e.g. if both ECC and authentication are enabled for 64 MB boot, the highest valid block number is is 49, as sector 50 is only .2M Bytes in size.) Reset Source: mod_g_rst_n

14.2.1.1.1.2.96 MAIN_CTRL_MMR_CFG0_DCC_STAT Register

14.2.1.1.1.2.96.1 MAIN_CTRL_MMR_CFG0_DCC_STAT Register (Offset = 4750h) [reset = 0h]

Interrupt Status of Individual DCC Modules

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Table 14-4326. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4750h

Figure 14-2151. MAIN_CTRL_MMR_CFG0_DCC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						DCC_STAT_MCU_DCC1_INTR_DONE	DCC_STAT_MCU_DCC0_INTR_DONE
NONE						R	R
0h						X	X
15	14	13	12	11	10	9	8
RESERVED							DCC_STAT_DCC8_INTR_DONE
NONE							R
0h							X
7	6	5	4	3	2	1	0
DCC_STAT_DCC7_INTR_DONE	DCC_STAT_DCC6_INTR_DONE	DCC_STAT_DCC5_INTR_DONE	DCC_STAT_DCC4_INTR_DONE	DCC_STAT_DCC3_INTR_DONE	DCC_STAT_DCC2_INTR_DONE	DCC_STAT_DCC1_INTR_DONE	DCC_STAT_DCC0_INTR_DONE
R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X

Table 14-4327. MAIN_CTRL_MMR_CFG0_DCC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DCC_STAT_MCU_DCC1_INTR_DONE	R	X	MCU_DCC1 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
16	DCC_STAT_MCU_DCC0_INTR_DONE	R	X	MCU_DCC0 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	DCC_STAT_DCC8_INTR_DONE	R	X	DCC8 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n

Table 14-4327. MAIN_CTRL_MMR_CFG0_DCC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	DCC_STAT_DCC7_INTR_DONE	R	X	DCC7 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
6	DCC_STAT_DCC6_INTR_DONE	R	X	DCC6 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
5	DCC_STAT_DCC5_INTR_DONE	R	X	DCC5 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
4	DCC_STAT_DCC4_INTR_DONE	R	X	DCC4 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
3	DCC_STAT_DCC3_INTR_DONE	R	X	DCC3 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
2	DCC_STAT_DCC2_INTR_DONE	R	X	DCC2 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
1	DCC_STAT_DCC1_INTR_DONE	R	X	DCC1 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
0	DCC_STAT_DCC0_INTR_DONE	R	X	DCC0 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n

14.2.1.1.1.2.97 MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL Register

14.2.1.1.1.2.97.1 MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL Register (Offset = 4760h) [reset = 1h]

Controls operation of the RL2 Cache Controller for Main R5 Cluster0 Core0

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Table 14-4328. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4760h

Figure 14-2152. MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">R5SS0_CORE0_RL2_CTRL_RTXIP_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td></td></tr>
<tr><td colspan="7">NONE</td><td></td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
</table>

Table 14-4329. MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	R5SS0_CORE0_RL2_CTRL_RTXIP_SEL	R/W	0h	Selects R5SS0 Core 0 OSPI0 XIP realtime access mode When realtime accesses are enabled, read transactions take priority over write transactions. This prevents XIP delays when Flash RWW updates are active. Field values (others are reserved): 2'b00 - No realtime accesses 2'b01 - Realtime access on RL2 Flash read pending 2'b10 - All read accesses are realtime Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.98 MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL Register

14.2.1.1.1.2.98.1 MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL Register (Offset = 4764h) [reset = 1h]

Controls operation of the RL2 Cache Controller for Main R5 Cluster0 Core1. Note this register has no effect if Main R5 Cluster0 is operating in lockstep mode.

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Table 14-4330. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4764h

Figure 14-2153. MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">R5SS0_CORE1_RL2_CTRL_RTXIP_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td></td></tr>
<tr><td colspan="7">NONE</td><td></td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
</table>

Table 14-4331. MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	R5SS0_CORE1_RL2_CTRL_RTXIP_SEL	R/W	0h	Selects R5SS0 Core 1 OSPI0 XIP realtime access mode When realtime accesses are enabled, read transactions take priority over write transactions. This prevents XIP delays when Flash RWW updates are active. Field values (others are reserved): 2'b00 - No realtime accesses 2'b01 - Realtime access on RL2 Flash read pending 2'b10 - All read accesses are realtime Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.99 MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL Register

14.2.1.1.1.2.99.1 MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL Register (Offset = 4770h) [reset = 1h]

Controls operation of the RL2 Cache Controller for Main R5 Cluster1 Core0

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Table 14-4332. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4770h

Figure 14-2154. MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						R5SS1_CORE0_RL2_CTRL_RTXIP_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							1h

Table 14-4333. MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	R5SS1_CORE0_RL2_CTRL_RTXIP_SEL	R/W	0h	Selects R5SS1 Core 0 OSPI0 XIP realtime access mode When realtime accesses are enabled, read transactions take priority over write transactions. This prevents XIP delays when Flash RWW updates are active. Field values (others are reserved): 2'b00 - No realtime accesses 2'b01 - Realtime access on RL2 Flash read pending 2'b10 - All read accesses are realtime Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.100 MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL Register

14.2.1.1.1.2.100.1 MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL Register (Offset = 4774h) [reset = 1h]

Controls operation of the RL2 Cache Controller for Main R5 Cluster1 Core1. Note this register has no effect if Main R5 Cluster0 is operating in lockstep mode.

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Table 14-4334. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 4774h

Figure 14-2155. MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						R5SS1_CORE1_RL2_CTRL_RTXIP_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							1h

Table 14-4335. MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	R5SS1_CORE1_RL2_CTRL_RTXIP_SEL	R/W	0h	Selects R5SS1 Core 1 OSPI0 XIP realtime access mode When realtime accesses are enabled, read transactions take priority over write transactions. This prevents XIP delays when Flash RWW updates are active. Field values (others are reserved): 2'b00 - No realtime accesses 2'b01 - Realtime access on RL2 Flash read pending 2'b10 - All read accesses are realtime Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.101 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register

14.2.1.1.1.2.101.1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-4336. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 5008h

Figure 14-2156. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-4337. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.102 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register

14.2.1.1.1.2.102.1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-4338. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 500Ch

Figure 14-2157. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK1_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK1_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK1_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK1_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4339. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.103 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

14.2.1.1.1.2.103.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4340. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 5100h

Figure 14-2158. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-4341. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.104 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register

14.2.1.1.1.2.104.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4342. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 5108h

Figure 14-2159. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-4343. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.105 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

14.2.1.1.1.2.105.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-4344. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 510Ch

Figure 14-2160. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-4345. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.106 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

14.2.1.1.1.2.106.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4346. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 5110h

Figure 14-2161. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-4347. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.107 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register

14.2.1.1.1.2.107.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register (Offset = 5118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4348. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 5118h

Figure 14-2162. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6_READONLY							
R							
0h							

Table 14-4349. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.108 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register

14.2.1.1.1.2.108.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register (Offset = 5120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4350. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 5120h

Figure 14-2163. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8_READONLY							
R							
0h							

Table 14-4351. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.109 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register

14.2.1.1.1.2.109.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register (Offset = 5124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4352. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 5124h

Figure 14-2164. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9_READONLY							
R							
0h							

Table 14-4353. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.110 MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register

14.2.1.1.1.2.110.1 MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register (Offset = 6044h) [reset = 2h]

Controls Ethernet Port1 operation

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Table 14-4354. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6044h

Figure 14-2165. MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	ENET1_CTRL_PORT_MODE_SEL_PROXY		
NONE				NONE	R/W		
0h			0h	0h	2h		

Table 14-4355. MAIN_CTRL_MMR_CFG0_ENET1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET1_CTRL_PORT_MODE_SEL_PROXY	R/W	2h	Selects Ethernet switch Port1 interface Field values (others are reserved): 3'b000 - GMII/MII (not supported) 3'b001 - RMII 3'b010 - RGMII 3'b011 - SGMII 3'b100 - QSGMII (not supported) 3'b101 - XFI (not supported) 3'b110 - QSGMII_SUB (not supported) 3'b111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.111 MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register

14.2.1.1.1.2.111.1 MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register (Offset = 6048h) [reset = 2h]

Controls Ethernet Port2 operation

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Table 14-4356. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6048h

Figure 14-2166. MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	ENET2_CTRL_PORT_MODE_SEL_PROXY		
NONE				NONE	R/W		
0h			0h	0h	2h		

Table 14-4357. MAIN_CTRL_MMR_CFG0_ENET2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
3	RESERVED	NONE	0h	Reserved
2:0	ENET2_CTRL_PORT_MODE_SEL_PROXY	R/W	2h	Selects Ethernet switch Port2 interface Field values (others are reserved): 3'b000 - GMII/MII (not supported) 3'b001 - RMII 3'b010 - RGMII 3'b011 - SGMII 3'b100 - QSGMII (not supported) 3'b101 - XFI (not supported) 3'b110 - QSGMII_SUB (not supported) 3'b111 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.112 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register

14.2.1.1.1.2.112.1 MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register (Offset = 6130h) [reset = 0h]

Controls Timebase Counter of EPWM Modules

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Table 14-4358. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6130h

Figure 14-2167. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM_TB_CLKEN_EPWM2_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM1_TB_CLKEN_PROXY	EPWM_TB_CLKEN_EPWM0_TB_CLKEN_PROXY
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-4359. MAIN_CTRL_MMR_CFG0_EPWM_TB_CLKEN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	EPWM_TB_CLKEN_EPWM2_TB_CLKEN_PROXY	R/W	0h	Enabled Timebase Clock of EPWM2 When Set Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
1	EPWM_TB_CLKEN_EPWM1_TB_CLKEN_PROXY	R/W	0h	EnablesTimebase Clock of EPWM1 When Set Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
0	EPWM_TB_CLKEN_EPWM0_TB_CLKEN_PROXY	R/W	0h	EnablesTimebase Clock of EPWM0 When Set Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n

14.2.1.1.1.2.113 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register

14.2.1.1.1.2.113.1 MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register (Offset = 6140h) [reset = 0h]

Controls EPWM0 Operation

Return to Summary Table

Table 14-4360. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6140h

Figure 14-2168. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					EPWM0_CTRL_SYNCIN_SEL_PROXY		
NONE					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			EPWM0_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4361. MAIN_CTRL_MMR_CFG0_EPWM0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	EPWM0_CTRL_SYNCIN_SEL_PROXY	R/W	0h	Selects the source of the EPWM0 synchronization input Field values (others are reserved): 3'b000 - EPWM0_SYNCIN (Pin) undefined - undefined 3'b010 - TimeSync Intr Router outl.20 3'b011 - CPSW CPTS Compare Event Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	EPWM0_CTRL_EALLOW_PROXY	R/W	0h	Enable write access to EPWM tripzone registers Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.114 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register

14.2.1.1.1.2.114.1 MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register (Offset = 6144h) [reset = 0h]

Controls EPWM1 Operation

Return to Summary Table

Table 14-4362. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6144h

Figure 14-2169. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM1_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4363. MAIN_CTRL_MMR_CFG0_EPWM1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM1_CTRL_EALLOW_PROXY	R/W	0h	Enable write access to EPWM tripzone registers Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.115 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register

14.2.1.1.1.2.115.1 MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register (Offset = 6148h) [reset = 0h]

Controls EPWM2 Operation

Return to Summary Table

Table 14-4364. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6148h

Figure 14-2170. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EPWM2_CTRL_EALLOW_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4365. MAIN_CTRL_MMR_CFG0_EPWM2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EPWM2_CTRL_EALLOW_PROXY	R/W	0h	Enable write access to EPWM tripzone registers Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.116 MAIN_CTRL_MMR_CFG0_TIMER0_CTRL_PROXY Register

14.2.1.1.1.2.116.1 MAIN_CTRL_MMR_CFG0_TIMER0_CTRL_PROXY Register (Offset = 6200h) [reset = 0h]

Controls TIMER0 operation

Return to Summary Table

Table 14-4366. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6200h

Figure 14-2171. MAIN_CTRL_MMR_CFG0_TIMER0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER0_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4367. MAIN_CTRL_MMR_CFG0_TIMER0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER0_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER0 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.117 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register

14.2.1.1.1.2.117.1 MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register (Offset = 6204h) [reset = 0h]

Controls TIMER1 operation

Return to Summary Table

Table 14-4368. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6204h

Figure 14-2172. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER1_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TIMER1_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4369. MAIN_CTRL_MMR_CFG0_TIMER1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER1_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER1 to TIMER0 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER1_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER1 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.118 MAIN_CTRL_MMR_CFG0_TIMER2_CTRL_PROXY Register

14.2.1.1.1.2.118.1 MAIN_CTRL_MMR_CFG0_TIMER2_CTRL_PROXY Register (Offset = 6208h) [reset = 0h]

Controls TIMER2 operation

Return to Summary Table

Table 14-4370. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6208h

Figure 14-2173. MAIN_CTRL_MMR_CFG0_TIMER2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER2_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4371. MAIN_CTRL_MMR_CFG0_TIMER2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER2_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER2 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.119 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register

14.2.1.1.1.2.119.1 MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register (Offset = 620Ch) [reset = 0h]

Controls TIMER3 operation

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Table 14-4372. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 620Ch

Figure 14-2174. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER3_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TIMER3_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4373. MAIN_CTRL_MMR_CFG0_TIMER3_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER3_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER3 to TIMER2 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER3_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER3 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.120 MAIN_CTRL_MMR_CFG0_TIMER4_CTRL_PROXY Register

14.2.1.1.1.2.120.1 MAIN_CTRL_MMR_CFG0_TIMER4_CTRL_PROXY Register (Offset = 6210h) [reset = 0h]

Controls TIMER4 operation

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Table 14-4374. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6210h

Figure 14-2175. MAIN_CTRL_MMR_CFG0_TIMER4_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TIMER4_CTRL_CAP_SEL_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4375. MAIN_CTRL_MMR_CFG0_TIMER4_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER4_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER4 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.121 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register

14.2.1.1.1.2.121.1 MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register (Offset = 6214h) [reset = 0h]

Controls TIMER5 operation

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Table 14-4376. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6214h

Figure 14-2176. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>TIMER5_CTRL_CASCADE_EN_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TIMER5_CTRL_CAP_SEL_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4377. MAIN_CTRL_MMR_CFG0_TIMER5_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER5_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER5 to TIMER4 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER5_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER5 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.122 MAIN_CTRL_MMR_CFG0_TIMER6_CTRL_PROXY Register

14.2.1.1.1.2.122.1 MAIN_CTRL_MMR_CFG0_TIMER6_CTRL_PROXY Register (Offset = 6218h) [reset = 0h]

Controls TIMER6 operation

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Table 14-4378. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6218h

Figure 14-2177. MAIN_CTRL_MMR_CFG0_TIMER6_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER6_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4379. MAIN_CTRL_MMR_CFG0_TIMER6_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER6_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER6 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.123 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register

14.2.1.1.1.2.123.1 MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register (Offset = 621Ch) [reset = 0h]

Controls TIMER7 operation

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Table 14-4380. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 621Ch

Figure 14-2178. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER7_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TIMER7_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4381. MAIN_CTRL_MMR_CFG0_TIMER7_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER7_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER7 to TIMER6 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER7_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER7 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.124 MAIN_CTRL_MMR_CFG0_TIMER8_CTRL_PROXY Register

14.2.1.1.1.2.124.1 MAIN_CTRL_MMR_CFG0_TIMER8_CTRL_PROXY Register (Offset = 6220h) [reset = 0h]

Controls TIMER8 operation

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Table 14-4382. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6220h

Figure 14-2179. MAIN_CTRL_MMR_CFG0_TIMER8_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER8_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4383. MAIN_CTRL_MMR_CFG0_TIMER8_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER8_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER8 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.125 MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY Register

14.2.1.1.1.2.125.1 MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY Register (Offset = 6224h) [reset = 0h]

Controls TIMER9 operation

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Table 14-4384. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6224h

Figure 14-2180. MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TIMER9_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					TIMER9_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4385. MAIN_CTRL_MMR_CFG0_TIMER9_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER9_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER9 to TIMER8 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER9_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER9 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.126 MAIN_CTRL_MMR_CFG0_TIMER10_CTRL_PROXY Register

14.2.1.1.1.2.126.1 MAIN_CTRL_MMR_CFG0_TIMER10_CTRL_PROXY Register (Offset = 6228h) [reset = 0h]

Controls TIMER10 operation

Return to Summary Table

Table 14-4386. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6228h

Figure 14-2181. MAIN_CTRL_MMR_CFG0_TIMER10_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER10_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4387. MAIN_CTRL_MMR_CFG0_TIMER10_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER10_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER10 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.127 MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY Register

14.2.1.1.1.2.127.1 MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY Register (Offset = 622Ch) [reset = 0h]

Controls TIMER11 operation

Return to Summary Table

Table 14-4388. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 622Ch

Figure 14-2182. MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>TIMER11_CTRL_CASCADE_EN_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">TIMER11_CTRL_CAP_SEL_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4389. MAIN_CTRL_MMR_CFG0_TIMER11_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER11_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER11 to TIMER10 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER11_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER11 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.128 MAIN_CTRL_MMR_CFG0_TIMER12_CTRL_PROXY Register

14.2.1.1.1.2.128.1 MAIN_CTRL_MMR_CFG0_TIMER12_CTRL_PROXY Register (Offset = 6230h) [reset = 0h]

Controls TIMER12 operation

Return to Summary Table

Table 14-4390. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6230h

Figure 14-2183. MAIN_CTRL_MMR_CFG0_TIMER12_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER12_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4391. MAIN_CTRL_MMR_CFG0_TIMER12_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER12_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER12 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.129 MAIN_CTRL_MMR_CFG0_TIMER13_CTRL_PROXY Register

14.2.1.1.1.2.129.1 MAIN_CTRL_MMR_CFG0_TIMER13_CTRL_PROXY Register (Offset = 6234h) [reset = 0h]

Controls TIMER13 operation

Return to Summary Table

Table 14-4392. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6234h

Figure 14-2184. MAIN_CTRL_MMR_CFG0_TIMER13_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							TIMER13_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h

7	6	5	4	3	2	1	0
RESERVED					TIMER13_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4393. MAIN_CTRL_MMR_CFG0_TIMER13_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER13_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER13 to TIMER12 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER13_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER13 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.130 MAIN_CTRL_MMR_CFG0_TIMER14_CTRL_PROXY Register

14.2.1.1.1.2.130.1 MAIN_CTRL_MMR_CFG0_TIMER14_CTRL_PROXY Register (Offset = 6238h) [reset = 0h]

Controls TIMER14 operation

Return to Summary Table

Table 14-4394. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6238h

Figure 14-2185. MAIN_CTRL_MMR_CFG0_TIMER14_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TIMER14_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4395. MAIN_CTRL_MMR_CFG0_TIMER14_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TIMER14_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER14 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.131 MAIN_CTRL_MMR_CFG0_TIMER15_CTRL_PROXY Register

14.2.1.1.1.2.131.1 MAIN_CTRL_MMR_CFG0_TIMER15_CTRL_PROXY Register (Offset = 623Ch) [reset = 0h]

Controls TIMER15 operation

Return to Summary Table

Table 14-4396. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 623Ch

Figure 14-2186. MAIN_CTRL_MMR_CFG0_TIMER15_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TIMER15_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED					TIMER15_CTRL_CAP_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4397. MAIN_CTRL_MMR_CFG0_TIMER15_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TIMER15_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER15 to TIMER14 Field values (others are reserved): 1'b0 - Cascading disabled 1'b1 - Cascading enabled Reset Source: sys_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	TIMER15_CTRL_CAP_SEL_PROXY	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER15 is configured for capture operation. Field values (others are reserved): 3'b000 - Use TIMERIO0 pin 3'b001 - Use TIMERIO1 pin 3'b010 - Use TIMERIO2 pin 3'b011 - Use TIMERIO3 pin 3'b100 - Use TIMERIO4 pin 3'b101 - Use TIMERIO5 pin 3'b110 - Use TIMERIO6 pin 3'b111 - Use TIMERIO7 pin Reset Source: sys_por_rst_n

14.2.1.1.1.2.132 MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL_PROXY Register

14.2.1.1.1.2.132.1 MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL_PROXY Register (Offset = 6280h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4398. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6280h

Figure 14-2187. MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMERIO0_CTRL_OUT_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4399. MAIN_CTRL_MMR_CFG0_TIMERIO0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO0_CTRL_OUT_SEL_PROXY	R/W	0h	Selects the source of the TIMERIO0 output Field values (others are reserved): 4'b0000 - TIMERIO0 is driven by TIMER0 output 4'b0001 - TIMERIO0 is driven by TIMER1 output 4'b0010 - TIMERIO0 is driven by TIMER2 output 4'b0011 - TIMERIO0 is driven by TIMER3 output 4'b0100 - TIMERIO0 is driven by TIMER4 output 4'b0101 - TIMERIO0 is driven by TIMER5 output 4'b0110 - TIMERIO0 is driven by TIMER6 output 4'b0111 - TIMERIO0 is driven by TIMER7 output 4'b1000 - TIMERIO0 is driven by TIMER8 output 4'b1001 - TIMERIO0 is driven by TIMER9 output 4'b1010 - TIMERIO0 is driven by TIMER10 output 4'b1011 - TIMERIO0 is driven by TIMER11 output 4'b1100 - TIMERIO0 is driven by TIMER12 output 4'b1101 - TIMERIO0 is driven by TIMER13 output 4'b1110 - TIMERIO0 is driven by TIMER14 output 4'b1111 - TIMERIO0 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.133 MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL_PROXY Register

14.2.1.1.1.2.133.1 MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL_PROXY Register (Offset = 6284h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4400. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6284h

Figure 14-2188. MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO1_CTRL_OUT_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4401. MAIN_CTRL_MMR_CFG0_TIMERIO1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO1_CTRL_OUT_SEL_PROXY	R/W	0h	Selects the source of the TIMERIO1 output Field values (others are reserved): 4'b0000 - TIMERIO1 is driven by TIMER0 output 4'b0001 - TIMERIO1 is driven by TIMER1 output 4'b0010 - TIMERIO1 is driven by TIMER2 output 4'b0011 - TIMERIO1 is driven by TIMER3 output 4'b0100 - TIMERIO1 is driven by TIMER4 output 4'b0101 - TIMERIO1 is driven by TIMER5 output 4'b0110 - TIMERIO1 is driven by TIMER6 output 4'b0111 - TIMERIO1 is driven by TIMER7 output 4'b1000 - TIMERIO1 is driven by TIMER8 output 4'b1001 - TIMERIO1 is driven by TIMER9 output 4'b1010 - TIMERIO1 is driven by TIMER10 output 4'b1011 - TIMERIO1 is driven by TIMER11 output 4'b1100 - TIMERIO1 is driven by TIMER12 output 4'b1101 - TIMERIO1 is driven by TIMER13 output 4'b1110 - TIMERIO1 is driven by TIMER14 output 4'b1111 - TIMERIO1 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.134 MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL_PROXY Register

14.2.1.1.1.2.134.1 MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL_PROXY Register (Offset = 6288h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4402. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6288h

Figure 14-2189. MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO2_CTRL_OUT_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4403. MAIN_CTRL_MMR_CFG0_TIMERIO2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO2_CTRL_OUT_SEL_PROXY	R/W	0h	Selects the source of the TIMERIO2 output Field values (others are reserved): 4'b0000 - TIMERIO2 is driven by TIMER0 output 4'b0001 - TIMERIO2 is driven by TIMER1 output 4'b0010 - TIMERIO2 is driven by TIMER2 output 4'b0011 - TIMERIO2 is driven by TIMER3 output 4'b0100 - TIMERIO2 is driven by TIMER4 output 4'b0101 - TIMERIO2 is driven by TIMER5 output 4'b0110 - TIMERIO2 is driven by TIMER6 output 4'b0111 - TIMERIO2 is driven by TIMER7 output 4'b1000 - TIMERIO2 is driven by TIMER8 output 4'b1001 - TIMERIO2 is driven by TIMER9 output 4'b1010 - TIMERIO2 is driven by TIMER10 output 4'b1011 - TIMERIO2 is driven by TIMER11 output 4'b1100 - TIMERIO2 is driven by TIMER12 output 4'b1101 - TIMERIO2 is driven by TIMER13 output 4'b1110 - TIMERIO2 is driven by TIMER14 output 4'b1111 - TIMERIO2 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.135 MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL_PROXY Register

14.2.1.1.1.2.135.1 MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL_PROXY Register (Offset = 628Ch) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4404. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 628Ch

Figure 14-2190. MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO3_CTRL_OUT_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4405. MAIN_CTRL_MMR_CFG0_TIMERIO3_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO3_CTRL_OUT_SEL_PROXY	R/W	0h	Selects the source of the TIMERIO3 output Field values (others are reserved): 4'b0000 - TIMERIO3 is driven by TIMER0 output 4'b0001 - TIMERIO3 is driven by TIMER1 output 4'b0010 - TIMERIO3 is driven by TIMER2 output 4'b0011 - TIMERIO3 is driven by TIMER3 output 4'b0100 - TIMERIO3 is driven by TIMER4 output 4'b0101 - TIMERIO3 is driven by TIMER5 output 4'b0110 - TIMERIO3 is driven by TIMER6 output 4'b0111 - TIMERIO3 is driven by TIMER7 output 4'b1000 - TIMERIO3 is driven by TIMER8 output 4'b1001 - TIMERIO3 is driven by TIMER9 output 4'b1010 - TIMERIO3 is driven by TIMER10 output 4'b1011 - TIMERIO3 is driven by TIMER11 output 4'b1100 - TIMERIO3 is driven by TIMER12 output 4'b1101 - TIMERIO3 is driven by TIMER13 output 4'b1110 - TIMERIO3 is driven by TIMER14 output 4'b1111 - TIMERIO3 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.136 MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL_PROXY Register

14.2.1.1.1.2.136.1 MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL_PROXY Register (Offset = 6290h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4406. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6290h

Figure 14-2191. MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO4_CTRL_OUT_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4407. MAIN_CTRL_MMR_CFG0_TIMERIO4_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO4_CTRL_OUT_SEL_PROXY	R/W	0h	Selects the source of the TIMERIO4 output Field values (others are reserved): 4'b0000 - TIMERIO4 is driven by TIMER0 output 4'b0001 - TIMERIO4 is driven by TIMER1 output 4'b0010 - TIMERIO4 is driven by TIMER2 output 4'b0011 - TIMERIO4 is driven by TIMER3 output 4'b0100 - TIMERIO4 is driven by TIMER4 output 4'b0101 - TIMERIO4 is driven by TIMER5 output 4'b0110 - TIMERIO4 is driven by TIMER6 output 4'b0111 - TIMERIO4 is driven by TIMER7 output 4'b1000 - TIMERIO4 is driven by TIMER8 output 4'b1001 - TIMERIO4 is driven by TIMER9 output 4'b1010 - TIMERIO4 is driven by TIMER10 output 4'b1011 - TIMERIO4 is driven by TIMER11 output 4'b1100 - TIMERIO4 is driven by TIMER12 output 4'b1101 - TIMERIO4 is driven by TIMER13 output 4'b1110 - TIMERIO4 is driven by TIMER14 output 4'b1111 - TIMERIO4 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.137 MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL_PROXY Register

14.2.1.1.1.2.137.1 MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL_PROXY Register (Offset = 6294h) [reset = 0h]

Controls Timer IO muxing

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Table 14-4408. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6294h

Figure 14-2192. MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO5_CTRL_OUT_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4409. MAIN_CTRL_MMR_CFG0_TIMERIO5_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO5_CTRL_OUT_SEL_PROXY	R/W	0h	Selects the source of the TIMERIO5 output Field values (others are reserved): 4'b0000 - TIMERIO5 is driven by TIMER0 output 4'b0001 - TIMERIO5 is driven by TIMER1 output 4'b0010 - TIMERIO5 is driven by TIMER2 output 4'b0011 - TIMERIO5 is driven by TIMER3 output 4'b0100 - TIMERIO5 is driven by TIMER4 output 4'b0101 - TIMERIO5 is driven by TIMER5 output 4'b0110 - TIMERIO5 is driven by TIMER6 output 4'b0111 - TIMERIO5 is driven by TIMER7 output 4'b1000 - TIMERIO5 is driven by TIMER8 output 4'b1001 - TIMERIO5 is driven by TIMER9 output 4'b1010 - TIMERIO5 is driven by TIMER10 output 4'b1011 - TIMERIO5 is driven by TIMER11 output 4'b1100 - TIMERIO5 is driven by TIMER12 output 4'b1101 - TIMERIO5 is driven by TIMER13 output 4'b1110 - TIMERIO5 is driven by TIMER14 output 4'b1111 - TIMERIO5 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.138 MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL_PROXY Register

14.2.1.1.1.2.138.1 MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL_PROXY Register (Offset = 6298h) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4410. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6298h

Figure 14-2193. MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMERIO6_CTRL_OUT_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4411. MAIN_CTRL_MMR_CFG0_TIMERIO6_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO6_CTRL_OUT_SEL_PROXY	R/W	0h	Selects the source of the TIMERIO6 output Field values (others are reserved): 4'b0000 - TIMERIO6 is driven by TIMER0 output 4'b0001 - TIMERIO6 is driven by TIMER1 output 4'b0010 - TIMERIO6 is driven by TIMER2 output 4'b0011 - TIMERIO6 is driven by TIMER3 output 4'b0100 - TIMERIO6 is driven by TIMER4 output 4'b0101 - TIMERIO6 is driven by TIMER5 output 4'b0110 - TIMERIO6 is driven by TIMER6 output 4'b0111 - TIMERIO6 is driven by TIMER7 output 4'b1000 - TIMERIO6 is driven by TIMER8 output 4'b1001 - TIMERIO6 is driven by TIMER9 output 4'b1010 - TIMERIO6 is driven by TIMER10 output 4'b1011 - TIMERIO6 is driven by TIMER11 output 4'b1100 - TIMERIO6 is driven by TIMER12 output 4'b1101 - TIMERIO6 is driven by TIMER13 output 4'b1110 - TIMERIO6 is driven by TIMER14 output 4'b1111 - TIMERIO6 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.139 MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL_PROXY Register

14.2.1.1.1.2.139.1 MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL_PROXY Register (Offset = 629Ch) [reset = 0h]

Controls Timer IO muxing

Return to Summary Table

Table 14-4412. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 629Ch

Figure 14-2194. MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMERIO7_CTRL_OUT_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4413. MAIN_CTRL_MMR_CFG0_TIMERIO7_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMERIO7_CTRL_OUT_SEL_PROXY	R/W	0h	Selects the source of the TIMERIO7 output Field values (others are reserved): 4'b0000 - TIMERIO7 is driven by TIMER0 output 4'b0001 - TIMERIO7 is driven by TIMER1 output 4'b0010 - TIMERIO7 is driven by TIMER2 output 4'b0011 - TIMERIO7 is driven by TIMER3 output 4'b0100 - TIMERIO7 is driven by TIMER4 output 4'b0101 - TIMERIO7 is driven by TIMER5 output 4'b0110 - TIMERIO7 is driven by TIMER6 output 4'b0111 - TIMERIO7 is driven by TIMER7 output 4'b1000 - TIMERIO7 is driven by TIMER8 output 4'b1001 - TIMERIO7 is driven by TIMER9 output 4'b1010 - TIMERIO7 is driven by TIMER10 output 4'b1011 - TIMERIO7 is driven by TIMER11 output 4'b1100 - TIMERIO7 is driven by TIMER12 output 4'b1101 - TIMERIO7 is driven by TIMER13 output 4'b1110 - TIMERIO7 is driven by TIMER14 output 4'b1111 - TIMERIO7 is driven by TIMER15 output Reset Source: sys_por_rst_n

14.2.1.1.1.2.140 MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register

14.2.1.1.1.2.140.1 MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register (Offset = 6300h) [reset = 3F3Fh]

Controls Relaxed Ordering by OrderID for the C7xv0 L2 Memory from external accesses. Ordering of accesses to the same 4KB L2 Block is relaxed either between Reads (more strict) or Between both Reads and Writes (more relaxed)

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Table 14-4414. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6300h

Figure 14-2195. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
C7XV_CTRL0_ORD15_PROXY	C7XV_CTRL0_ORD14_PROXY	C7XV_CTRL0_ORD13_PROXY	C7XV_CTRL0_ORD12_PROXY	C7XV_CTRL0_ORD11_PROXY	C7XV_CTRL0_ORD10_PROXY	C7XV_CTRL0_ORD9_PROXY	C7XV_CTRL0_ORD8_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
C7XV_CTRL0_ORD7_PROXY	C7XV_CTRL0_ORD6_PROXY	C7XV_CTRL0_ORD5_PROXY	C7XV_CTRL0_ORD4_PROXY	C7XV_CTRL0_ORD3_PROXY	C7XV_CTRL0_ORD2_PROXY	C7XV_CTRL0_ORD1_PROXY	C7XV_CTRL0_ORD0_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h

Table 14-4415. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	C7XV_CTRL0_ORD15_PROXY	R/W	0h	Ordering Rule for Order ID 15 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
14	C7XV_CTRL0_ORD14_PROXY	R/W	0h	Ordering Rule for Order ID 14 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
13	C7XV_CTRL0_ORD13_PROXY	R/W	1h	Ordering Rule for Order ID 13 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

Table 14-4415. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	C7XV_CTRL0_ORD12_PROXY	R/W	1h	Ordering Rule for Order ID 12 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
11	C7XV_CTRL0_ORD11_PROXY	R/W	1h	Ordering Rule for Order ID 11 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
10	C7XV_CTRL0_ORD10_PROXY	R/W	1h	Ordering Rule for Order ID 10 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
9	C7XV_CTRL0_ORD9_PROXY	R/W	1h	Ordering Rule for Order ID 9 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
8	C7XV_CTRL0_ORD8_PROXY	R/W	1h	Ordering Rule for Order ID 8 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
7	C7XV_CTRL0_ORD7_PROXY	R/W	0h	Ordering Rule for Order ID 7 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
6	C7XV_CTRL0_ORD6_PROXY	R/W	0h	Ordering Rule for Order ID 6 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
5	C7XV_CTRL0_ORD5_PROXY	R/W	1h	Ordering Rule for Order ID 5 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
4	C7XV_CTRL0_ORD4_PROXY	R/W	1h	Ordering Rule for Order ID 4 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
3	C7XV_CTRL0_ORD3_PROXY	R/W	1h	Ordering Rule for Order ID 3 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
2	C7XV_CTRL0_ORD2_PROXY	R/W	1h	Ordering Rule for Order ID 2 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

Table 14-4415. MAIN_CTRL_MMR_CFG0_C7XV_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	C7XV_CTRL0_ORD1_PROXY	R/W	1h	Ordering Rule for Order ID 1 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
0	C7XV_CTRL0_ORD0_PROXY	R/W	1h	Ordering Rule for Order ID 0 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

14.2.1.1.1.2.141 MAIN_CTRL_MMR_CFG0_C7XV_CTRL1_PROXY Register

14.2.1.1.1.2.141.1 MAIN_CTRL_MMR_CFG0_C7XV_CTRL1_PROXY Register (Offset = 6308h) [reset = 3F3Fh]

Controls Relaxed Ordering by OrderID for the C7xv1 L2 Memory from external accesses. Ordering of accesses to the same 4KB L2 Block is relaxed either between Reads (more strict) or Between both Reads and Writes (more relaxed)

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Table 14-4416. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6308h

Figure 14-2196. MAIN_CTRL_MMR_CFG0_C7XV_CTRL1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
C7XV_CTRL1_ORD15_PROXY	C7XV_CTRL1_ORD14_PROXY	C7XV_CTRL1_ORD13_PROXY	C7XV_CTRL1_ORD12_PROXY	C7XV_CTRL1_ORD11_PROXY	C7XV_CTRL1_ORD10_PROXY	C7XV_CTRL1_ORD9_PROXY	C7XV_CTRL1_ORD8_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
C7XV_CTRL1_ORD7_PROXY	C7XV_CTRL1_ORD6_PROXY	C7XV_CTRL1_ORD5_PROXY	C7XV_CTRL1_ORD4_PROXY	C7XV_CTRL1_ORD3_PROXY	C7XV_CTRL1_ORD2_PROXY	C7XV_CTRL1_ORD1_PROXY	C7XV_CTRL1_ORD0_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	1h	1h	1h	1h	1h	1h

Table 14-4417. MAIN_CTRL_MMR_CFG0_C7XV_CTRL1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	C7XV_CTRL1_ORD15_PROXY	R/W	0h	Ordering Rule for Order ID 15 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
14	C7XV_CTRL1_ORD14_PROXY	R/W	0h	Ordering Rule for Order ID 14 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
13	C7XV_CTRL1_ORD13_PROXY	R/W	1h	Ordering Rule for Order ID 13 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

Table 14-4417. MAIN_CTRL_MMR_CFG0_C7XV_CTRL1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	C7XV_CTRL1_ORD12_PROXY	R/W	1h	Ordering Rule for Order ID 12 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
11	C7XV_CTRL1_ORD11_PROXY	R/W	1h	Ordering Rule for Order ID 11 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
10	C7XV_CTRL1_ORD10_PROXY	R/W	1h	Ordering Rule for Order ID 10 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
9	C7XV_CTRL1_ORD9_PROXY	R/W	1h	Ordering Rule for Order ID 9 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
8	C7XV_CTRL1_ORD8_PROXY	R/W	1h	Ordering Rule for Order ID 8 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
7	C7XV_CTRL1_ORD7_PROXY	R/W	0h	Ordering Rule for Order ID 7 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
6	C7XV_CTRL1_ORD6_PROXY	R/W	0h	Ordering Rule for Order ID 6 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
5	C7XV_CTRL1_ORD5_PROXY	R/W	1h	Ordering Rule for Order ID 5 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
4	C7XV_CTRL1_ORD4_PROXY	R/W	1h	Ordering Rule for Order ID 4 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
3	C7XV_CTRL1_ORD3_PROXY	R/W	1h	Ordering Rule for Order ID 3 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
2	C7XV_CTRL1_ORD2_PROXY	R/W	1h	Ordering Rule for Order ID 2 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

Table 14-4417. MAIN_CTRL_MMR_CFG0_C7XV_CTRL1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	C7XV_CTRL1_ORD1_PROXY	R/W	1h	Ordering Rule for Order ID 1 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n
0	C7XV_CTRL1_ORD0_PROXY	R/W	1h	Ordering Rule for Order ID 0 Field values (others are reserved): 1'b0 - RELAXED_READ 1'b1 - RELAXED_R_TO_W Reset Source: mod_por_rst_n

14.2.1.1.1.2.142 MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY Register

14.2.1.1.1.2.142.1 MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY Register (Offset = 64C0h) [reset = 0h]

For determining state of MMCSD 1.8V Signalling

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Table 14-4418. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 64C0h

Figure 14-2197. MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC0_STAT_SIG1P8_EN_PROXY
NONE							R
0h							X

Table 14-4419. MAIN_CTRL_MMR_CFG0_EMMC0_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EMMC0_STAT_SIG1P8_EN_PROXY	R	X	Status of 1.8V Signal Activate from EMMC0 Module Field values (others are reserved): 1'b0 - DISABLE_1P8V_SIGNALLING 1'b1 - ENABLE_1P8V_SIGNALLING Reset Source: mod_g_rst_n

14.2.1.1.1.2.143 MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Register

14.2.1.1.1.2.143.1 MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Register (Offset = 64D0h) [reset = 0h]

Controls operation of ADC0

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Table 14-4420. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 64D0h

Figure 14-2198. MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>ADC0_CTRL_GPI_MODE_EN_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ADC0_CTRL_TRIG_SEL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-4421. MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	ADC0_CTRL_GPI_MODE_EN_PROXY	R/W	0h	Enables ADC0 data pins to be used as general purpose inputs when set. This signal is tied to the en_dig_test input of MCU_ADC0 Reset Source: mod_g_rst_n
15:5	RESERVED	NONE	0h	Reserved

Table 14-4421. MAIN_CTRL_MMR_CFG0_ADC0_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ADC0_CTRL_TRIG_SEL_PROXY	R/W	0h	Selects the source of the ADC hardware event trigger Field values (others are reserved): 5'b00000 - ADC_EXT_TRIGGER0 (Pin) 5'b00001 - 0 - Reserved 5'b00010 - EPWM SOCA_OUT 5'b00011 - EPWM SOCB_OUT 5'b00100 - 0 - Reserved 5'b00101 - 0 - Reserved 5'b00110 - 0 - Reserved 5'b00111 - 0 - Reserved 5'b01000 - 0 - Reserved 5'b01001 - 0 - Reserved 5'b01010 - 0 - Reserved 5'b01011 - 0 - Reserved 5'b01100 - 0 - Reserved 5'b01101 - 0 - Reserved 5'b01110 - WKUP_TIMER0 PWM 5'b01111 - WKUP_TIMER1 PWM 5'b10000 - TIMER0 PWM 5'b10001 - TIMER1 PWM 5'b10010 - TIMER2 PWM 5'b10011 - TIMER3 PWM 5'b10100 - TIMER4 PWM 5'b10101 - TIMER5 PWM 5'b10110 - TIMER6 PWM 5'b10111 - TIMER7 PWM 5'b11000 - TIMER8 PWM 5'b11001 - TIMER9 PWM 5'b11010 - TIMER10 PWM 5'b11011 - TIMER11 PWM 5'b11100 - TIMER12 PWM 5'b11101 - TIMER13_PWM 5'b11110 - TIMER14_pWM 5'b11111 - Timer15_PWM Reset Source: mod_g_rst_n

14.2.1.1.1.2.144 MAIN_CTRL_MMR_CFG0_ADC0_CAL_PROXY Register

14.2.1.1.1.2.144.1 MAIN_CTRL_MMR_CFG0_ADC0_CAL_PROXY Register (Offset = 64F0h) [reset = 0h]

Controls ADC0 calibration sequence (not used)

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Table 14-4422. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 64F0h

Figure 14-2199. MAIN_CTRL_MMR_CFG0_ADC0_CAL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADC0_CAL_CAL_EN_PROXY	ADC0_CAL_DIFF_CAL_EN_PROXY	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
7	6	5	4	3	2	1	0
RESERVED			ADC0_CAL_CAL_CAP_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4423. MAIN_CTRL_MMR_CFG0_ADC0_CAL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	ADC0_CAL_CAL_EN_PROXY	R/W	0h	Enable single-ended calibration Set to 1 to begin single-ended calibration Reset Source: mod_g_rst_n
14	ADC0_CAL_DIFF_CAL_EN_PROXY	R/W	0h	Enable differential calibration Set to 1 to begin differential calibration Reset Source: mod_g_rst_n
13:5	RESERVED	NONE	0h	Reserved
4:0	ADC0_CAL_CAL_CAP_SEL_PROXY	R/W	0h	Select capacitor for calibration Bits correspond to C5:C1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.145 MAIN_CTRL_MMR_CFG0_FSS0_CTRL0_PROXY Register

14.2.1.1.1.2.145.1 MAIN_CTRL_MMR_CFG0_FSS0_CTRL0_PROXY Register (Offset = 6700h) [reset = 0h]

Controls Flash boot region size for Flash Subsystem0

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Table 14-4424. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6700h

Figure 14-2200. MAIN_CTRL_MMR_CFG0_FSS0_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				FSS0_CTRL0_S0_BOOT_SEG_PROXY			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
FSS0_CTRL0_S0_BOOT_SEG_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
FSS0_CTRL0_S0_BOOT_SEG_PROXY							
R/W							
0h							

Table 14-4425. MAIN_CTRL_MMR_CFG0_FSS0_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	FSS0_CTRL0_S0_BOOT_SEG_PROXY	R/W	0h	Selects the flash boot segment size Field values (others are reserved): 20'h00001 - 4 kB 20'h00002 - 8 kB 20'h00004 - 16 kB 20'h00008 - 32 kB 20'h00010 - 64 kB 20'h00020 - 128 kB 20'h00040 - 256 kB 20'h00080 - 512 kB 20'h00100 - 1 MB 20'h00200 - 2 MB 20'h00400 - 4 MB 20'h00800 - 8 MB 20'h01000 - 16 MB 20'h02000 - 32 MB 20'h04000 - 64 MB 20'h08000 - 128 MB 20'h10000 - 256 MB 20'h20000 - 512 MB 20'h40000 - 1 GB 20'h80000 - 2 GB Reset Source: mod_g_rst_n

14.2.1.1.1.2.146 MAIN_CTRL_MMR_CFG0_FSS0_CTRL1_PROXY Register

14.2.1.1.1.2.146.1 MAIN_CTRL_MMR_CFG0_FSS0_CTRL1_PROXY Register (Offset = 6704h) [reset = 0h]

Controls Flash boot region placement for Flash Subsystem0

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Table 14-4426. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6704h

Figure 14-2201. MAIN_CTRL_MMR_CFG0_FSS0_CTRL1_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FSS0_CTRL1_S0_BOOT_MASK_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FSS0_CTRL1_S0_BOOT_MASK_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FSS0_CTRL1_S0_BOOT_MASK_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4427. MAIN_CTRL_MMR_CFG0_FSS0_CTRL1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	FSS0_CTRL1_S0_BOOT_MASK_PROXY	R/W	0h	Determines which (upper 20) address bits to replace with boot_seg signals when accessing the Boot Region (Region 1) Reset Source: mod_g_rst_n

14.2.1.1.1.2.147 MAIN_CTRL_MMR_CFG0_FSS1_CTRL0_PROXY Register

14.2.1.1.1.2.147.1 MAIN_CTRL_MMR_CFG0_FSS1_CTRL0_PROXY Register (Offset = 6710h) [reset = 0h]

Controls Flash boot region size and placement for Flash Subsystem1

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Table 14-4428. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6710h

Figure 14-2202. MAIN_CTRL_MMR_CFG0_FSS1_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							FSS1_CTRL0_S0_BOOT_SIZE_PROXY
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		FSS1_CTRL0_S0_BOOT_SEG_PROXY					
NONE		R/W					
0h		0h					

Table 14-4429. MAIN_CTRL_MMR_CFG0_FSS1_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
23:22	RESERVED	NONE	0h	Reserved
15:9	RESERVED	NONE	0h	Reserved
8	FSS1_CTRL0_S0_BOOT_SIZE_PROXY	R/W	0h	Selects the size of the boot block to be used for the S0 (OSPI1) flash interface Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	FSS1_CTRL0_S0_BOOT_SEG_PROXY	R/W	0h	Selects the boot block to be used for the S0 (OSPI1) flash interface. If the s0_boot_size is 128 MB then only bits [4:0] of this field are used. Care must be taken to account for the address translation as to not fall off or wrap the address of the flash. (e.g. if both ECC and authentication are enabled for 64 MB boot, the highest valid block number is is 49, as sector 50 is only .2M Bytes in size.) Reset Source: mod_g_rst_n

14.2.1.1.1.2.148 MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register

14.2.1.1.1.2.148.1 MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register (Offset = 6750h) [reset = 0h]

Interrupt Status of Individual DCC Modules

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Table 14-4430. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6750h

Figure 14-2203. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						DCC_STAT_MCU_DCC1_INTR_DONE_PROXY	DCC_STAT_MCU_DCC0_INTR_DONE_PROXY
NONE						R	R
0h						X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							DCC_STAT_DCC8_INTR_DONE_PROXY
NONE							R
0h							X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCC_STAT_DCC7_INTR_DONE_PROXY	DCC_STAT_DCC6_INTR_DONE_PROXY	DCC_STAT_DCC5_INTR_DONE_PROXY	DCC_STAT_DCC4_INTR_DONE_PROXY	DCC_STAT_DCC3_INTR_DONE_PROXY	DCC_STAT_DCC2_INTR_DONE_PROXY	DCC_STAT_DCC1_INTR_DONE_PROXY	DCC_STAT_DCC0_INTR_DONE_PROXY
R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X

Table 14-4431. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DCC_STAT_MCU_DCC1_INTR_DONE_PROXY	R	X	MCU_DCC1 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
16	DCC_STAT_MCU_DCC0_INTR_DONE_PROXY	R	X	MCU_DCC0 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8	DCC_STAT_DCC8_INTR_DONE_PROXY	R	X	DCC8 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n

Table 14-4431. MAIN_CTRL_MMR_CFG0_DCC_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	DCC_STAT_DCC7_INTR_DONE_PROXY	R	X	DCC7 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
6	DCC_STAT_DCC6_INTR_DONE_PROXY	R	X	DCC6 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
5	DCC_STAT_DCC5_INTR_DONE_PROXY	R	X	DCC5 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
4	DCC_STAT_DCC4_INTR_DONE_PROXY	R	X	DCC4 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
3	DCC_STAT_DCC3_INTR_DONE_PROXY	R	X	DCC3 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
2	DCC_STAT_DCC2_INTR_DONE_PROXY	R	X	DCC2 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
1	DCC_STAT_DCC1_INTR_DONE_PROXY	R	X	DCC1 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n
0	DCC_STAT_DCC0_INTR_DONE_PROXY	R	X	DCC0 Done Interrupt Status Field values (others are reserved): 1'b0 - CLR 1'b1 - PEND Reset Source: mod_g_rst_n

14.2.1.1.1.2.149 MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL_PROXY Register

14.2.1.1.1.2.149.1 MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL_PROXY Register (Offset = 6760h) [reset = 1h]

Controls operation of the RL2 Cache Controller for Main R5 Cluster0 Core0

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Table 14-4432. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6760h

Figure 14-2204. MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						R5SS0_CORE0_RL2_CTRL_RTXIP_SEL_PROXY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							1h

Table 14-4433. MAIN_CTRL_MMR_CFG0_R5SS0_CORE0_RL2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	R5SS0_CORE0_RL2_CTRL_RTXIP_SEL_PROXY	R/W	0h	Selects R5SS0 Core 0 OSPI0 XIP realtime access mode When realtime accesses are enabled, read transactions take priority over write transactions. This prevents XIP delays when Flash RWW updates are active. Field values (others are reserved): 2'b00 - No realtime accesses 2'b01 - Realtime access on RL2 Flash read pending 2'b10 - All read accesses are realtime Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.150 MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL_PROXY Register

14.2.1.1.1.2.150.1 MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL_PROXY Register (Offset = 6764h) [reset = 1h]

Controls operation of the RL2 Cache Controller for Main R5 Cluster0 Core1. Note this register has no effect if Main R5 Cluster0 is operating in lockstep mode.

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Table 14-4434. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6764h

Figure 14-2205. MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						R5SS0_CORE1_RL2_CTRL_RTXIP_SEL_PROXY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							1h

Table 14-4435. MAIN_CTRL_MMR_CFG0_R5SS0_CORE1_RL2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	R5SS0_CORE1_RL2_CTRL_RTXIP_SEL_PROXY	R/W	0h	Selects R5SS0 Core 1 OSPI0 XIP realtime access mode When realtime accesses are enabled, read transactions take priority over write transactions. This prevents XIP delays when Flash RWW updates are active. Field values (others are reserved): 2'b00 - No realtime accesses 2'b01 - Realtime access on RL2 Flash read pending 2'b10 - All read accesses are realtime Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.151 MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL_PROXY Register

14.2.1.1.1.2.151.1 MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL_PROXY Register (Offset = 6770h) [reset = 1h]

Controls operation of the RL2 Cache Controller for Main R5 Cluster1 Core0

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Table 14-4436. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6770h

Figure 14-2206. MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						R5SS1_CORE0_RL2_CTRL_RTXIP_SEL_PROXY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							1h

Table 14-4437. MAIN_CTRL_MMR_CFG0_R5SS1_CORE0_RL2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	R5SS1_CORE0_RL2_CTRL_RTXIP_SEL_PROXY	R/W	0h	Selects R5SS1 Core 0 OSPI0 XIP realtime access mode When realtime accesses are enabled, read transactions take priority over write transactions. This prevents XIP delays when Flash RWW updates are active. Field values (others are reserved): 2'b00 - No realtime accesses 2'b01 - Realtime access on RL2 Flash read pending 2'b10 - All read accesses are realtime Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.152 MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL_PROXY Register

14.2.1.1.1.2.152.1 MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL_PROXY Register (Offset = 6774h) [reset = 1h]

Controls operation of the RL2 Cache Controller for Main R5 Cluster1 Core1. Note this register has no effect if Main R5 Cluster0 is operating in lockstep mode.

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Table 14-4438. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 6774h

Figure 14-2207. MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">R5SS1_CORE1_RL2_CTRL_RTXIP_SEL_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td></td></tr>
<tr><td colspan="7">NONE</td><td></td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
</table>

Table 14-4439. MAIN_CTRL_MMR_CFG0_R5SS1_CORE1_RL2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	R5SS1_CORE1_RL2_CTRL_RTXIP_SEL_PROXY	R/W	0h	Selects R5SS1 Core 1 OSPI0 XIP realtime access mode When realtime accesses are enabled, read transactions take priority over write transactions. This prevents XIP delays when Flash RWW updates are active. Field values (others are reserved): 2'b00 - No realtime accesses 2'b01 - Realtime access on RL2 Flash read pending 2'b10 - All read accesses are realtime Reset Source: mod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.153 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

14.2.1.1.1.2.153.1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-4440. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7008h

Figure 14-2208. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-4441. MAIN_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.154 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

14.2.1.1.1.2.154.1 MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-4442. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 700Ch

Figure 14-2209. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-4443. MAIN_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.155 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

14.2.1.1.1.2.155.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4444. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7100h

Figure 14-2210. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-4445. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.156 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

14.2.1.1.1.2.156.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4446. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7104h

Figure 14-2211. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-4447. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.157 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

14.2.1.1.1.2.157.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4448. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7108h

Figure 14-2212. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-4449. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.158 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

14.2.1.1.1.2.158.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-4450. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 710Ch

Figure 14-2213. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-4451. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.159 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

14.2.1.1.1.2.159.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4452. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7110h

Figure 14-2214. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-4453. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.160 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register

14.2.1.1.1.2.160.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4454. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7114h

Figure 14-2215. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4455. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.161 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register

14.2.1.1.1.2.161.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register (Offset = 7118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4456. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7118h

Figure 14-2216. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6							
R/W							
0h							

Table 14-4457. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.162 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register

14.2.1.1.1.2.162.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register (Offset = 711Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-4458. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 711Ch

Figure 14-2217. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7							
R/W							
0h							

Table 14-4459. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.163 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register

14.2.1.1.1.2.163.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register (Offset = 7120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4460. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7120h

Figure 14-2218. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8							
R/W							
0h							

Table 14-4461. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.164 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register

14.2.1.1.1.2.164.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register (Offset = 7124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4462. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7124h

Figure 14-2219. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4463. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.165 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register

14.2.1.1.1.2.165.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register (Offset = 7128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4464. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7128h

Figure 14-2220. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10							
R/W							
0h							

Table 14-4465. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.166 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register

14.2.1.1.1.2.166.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register (Offset = 712Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-4466. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 712Ch

Figure 14-2221. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11							
R/W							
0h							

Table 14-4467. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.167 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register

14.2.1.1.1.2.167.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register (Offset = 7130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4468. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7130h

Figure 14-2222. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12							
R/W							
0h							

Table 14-4469. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.168 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register

14.2.1.1.1.2.168.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register (Offset = 7134h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4470. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7134h

Figure 14-2223. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R13							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R13							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R13							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R13							
R/W							
0h							

Table 14-4471. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R13	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.169 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register

14.2.1.1.1.2.169.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register (Offset = 7138h) [reset = 0h]

Claim bits for Partition 1

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Table 14-4472. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 7138h

Figure 14-2224. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R14							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R14							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R14							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R14							
R/W							
0h							

Table 14-4473. MAIN_CTRL_MMR_CFG0_CLAIMREG_P1_R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R14	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.170 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register

14.2.1.1.1.2.170.1 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register (Offset = 8000h) [reset = 7h]

This register controls which internal clock is made observable on the OBSCLK0/1 output pins

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Table 14-4474. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8000h

Figure 14-2225. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							OBSCLK0_CTRL_OUT_MUX_SEL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							OBSCLK0_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
OBSCLK0_CTRL_CLK_DIV							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED			OBSCLK0_CTRL_CLK_SEL				
NONE			R/W				
0h			7h				

Table 14-4475. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	OBSCLK0_CTRL_OUT_MUX_SEL	R/W	0h	OBSCLK pin output mux selection. PLL4_REFCLK is the direct output from either HFOSC0 or HFOSC1. Field values (others are reserved): 1'b0 - Selects the output of the CLK_DIV_OUT clock mux 1'b1 - Select PLL4_REFCLK (clk_sel value must be 5'b11111) Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	OBSCLK0_CTRL_CLK_DIV_LD	R/W	0h	Load divisor value from clk_div field, when the bit is toggled from 0 to 1. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_por_rst_n
15:8	OBSCLK0_CTRL_CLK_DIV	R/W	0h	OBSCLK0 output divider. Sets divider to divide by clkdiv + 1. Divide by 1 to 256 are supported. After Writing to this field, the clk_div_ld field must be toggled. Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved

Table 14-4475. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	OBSCLK0_CTRL_CLK_SEL	R/W	7h	OBSCLK0 clock source selection. Selects the source of the clock to be divided by the OBSCLK0 divider. Field values (others are reserved): 5'b00000 - MAIN_PLL0_HSDIV0_CLKOUT 5'b00001 - MAIN_PLL1_HSDIV0_CLKOUT 5'b00010 - MAIN_PLL2_HSDIV0_CLKOUT 5'b00011 - MAIN_PLL4_HSDIV0_CLKOUT 5'b00100 - MAIN_PLL14_HSDIV0_CLKOUT 5'b00101 - CLK_12M_RC 5'b00110 - HFOSC0_CLKOUT_32K 5'b00111 - PLLCTRL_OBSCLK 5'b01000 - HFOSC0_CLKOUT 5'b01001 - CLK_32K_RC 5'b01010 - CPSW0_CPTS_GENF0 5'b01011 - CPSW0_CPTS_GENF1 5'b01100 - MCU_PLL0_HSDIV0_CLKOUT 5'b01101 - MAIN_PLL15_HSDIV0_CLKOUT undefined - undefined undefined - undefined undefined - undefined 5'b10000 - MAIN_SYSCLK0 5'b10001 - DEVICE_CLKOUT_32K undefined - undefined 5'b10011 - C7XV_CLK_DIV4 undefined - undefined undefined - undefined 5'b11111 - OFF (Must Select this option when out_mux_sel is set to PLL4_REFCLK) Reset Source: mod_por_rst_n

14.2.1.1.1.2.171 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register

14.2.1.1.1.2.171.1 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register (Offset = 8010h) [reset = 0h]

Enables and selects clock source of CPSW CLKOUT pin

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Table 14-4476. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8010h

Figure 14-2226. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED			CLKOUT_CTRL_CLK_SEL
NONE				NONE			R/W
0h			0h	0h			0h

Table 14-4477. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
3:1	RESERVED	NONE	0h	Reserved
0	CLKOUT_CTRL_CLK_SEL	R/W	0h	Selects CLKOUT clock source Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV1_CLKOUT / 5 1'b1 - MAIN_PLL2_HSDIV1_CLKOUT / 10 Reset Source: mod_g_rst_n

14.2.1.1.1.2.172 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register

14.2.1.1.1.2.172.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register (Offset = 8060h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL0

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Table 14-4478. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8060h

Figure 14-2227. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
MAIN_PLL0_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4479. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL0. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL0_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL0 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.173 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register

14.2.1.1.1.2.173.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register (Offset = 8064h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL1

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Table 14-4480. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8064h

Figure 14-2228. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL1_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-4481. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL1. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL1_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL1 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.174 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register

14.2.1.1.1.2.174.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register (Offset = 8068h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL2

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Table 14-4482. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8068h

Figure 14-2229. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL2_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-4483. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL2. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL2_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL2 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.175 MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL Register

14.2.1.1.1.2.175.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL Register (Offset = 8070h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL4

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Table 14-4484. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8070h

Figure 14-2230. MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>MAIN_PLL4_CLKSEL_BYPASS_SW_OVRD</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>MAIN_PLL4_CLKSEL_BYP_WARM_RST</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>MAIN_PLL4_CLKSEL_CLK_SEL</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4485. MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL4_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL4. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL4_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL4 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n

Table 14-4485. MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:5	RESERVED	NONE	0h	Reserved
4	MAIN_PLL4_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL4 1'b0 - Use HFOSC0_CLKOUT 1'b1 - Use HFOSC1_CLKOUT Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.176 MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL Register

14.2.1.1.1.2.176.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL Register (Offset = 807Ch) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL7

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Table 14-4486. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 807Ch

Figure 14-2231. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL7_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL7_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-4487. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL7_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL7. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL7_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL7 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.177 MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Register

14.2.1.1.1.2.177.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Register (Offset = 8098h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL14

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Table 14-4488. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8098h

Figure 14-2232. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Name Register

31	30	29	28	27	26	25	24
MAIN_PLL14_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL14_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4489. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL14_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL14. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL14_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL14 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n

Table 14-4489. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.178 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register

14.2.1.1.1.2.178.1 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register (Offset = 8140h) [reset = 7h]

Selects the CP Switch clock sources

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Table 14-4490. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8140h

Figure 14-2233. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CPSW_CLKSEL_CPTS_CLKSEL		
NONE					R/W		
0h					7h		

Table 14-4491. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPSW_CLKSEL_CPTS_CLKSEL	R/W	7h	Selects the clock source for the CPSW Ethernet switch Common Platform Time Stamp module Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV5_CLKOUT 3'b001 - MAIN_PLL0_HSDIV6_CLKOUT 3'b010 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 3'b011 - Reserved 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - EXT_REFCLK1 (Pin) 3'b110 - SERDES0_IP1_LN0_TXMCLK undefined - undefined 3'b111 - MAIN_SYSCLK0 Reset Source: mod_por_rst_n

14.2.1.1.1.2.179 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register

14.2.1.1.1.2.179.1 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register (Offset = 8160h) [reset = 0h]

Selects the functional clock source for 8-bit eMMC0

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Table 14-4492. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8160h

Figure 14-2234. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							EMMC0_CLKSEL_EMMCSD_IO_CLKLB_SEL
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							EMMC0_CLKSEL_EMMCSD_REFCLK_SEL
NONE							R/W
0h							0h

Table 14-4493. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC0_CLKSEL_EMMCSD_IO_CLKLB_SEL	R/W	0h	Selects IO Pad Loopback for the MMC Module Field values (others are reserved): 1'b0 - Loopback from Unbonded Pad MMCSD0_CLKLB 1'b1 - Loopback from IO Pin MMCSD0_CLK Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC0_CLKSEL_EMMCSD_REFCLK_SEL	R/W	0h	Selects the functional clock for the MMC Module Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV5_CLKOUT 1'b1 - MAIN_PLL2_HSDIV2_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.180 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register

14.2.1.1.1.2.180.1 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register (Offset = 81B0h) [reset = 0h]

Timer0 functional clock selection control

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Table 14-4494. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81B0h

Figure 14-2235. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER0_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4495. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER0_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.181 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register

14.2.1.1.1.2.181.1 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register (Offset = 81B4h) [reset = 0h]

Timer1 functional clock selection control

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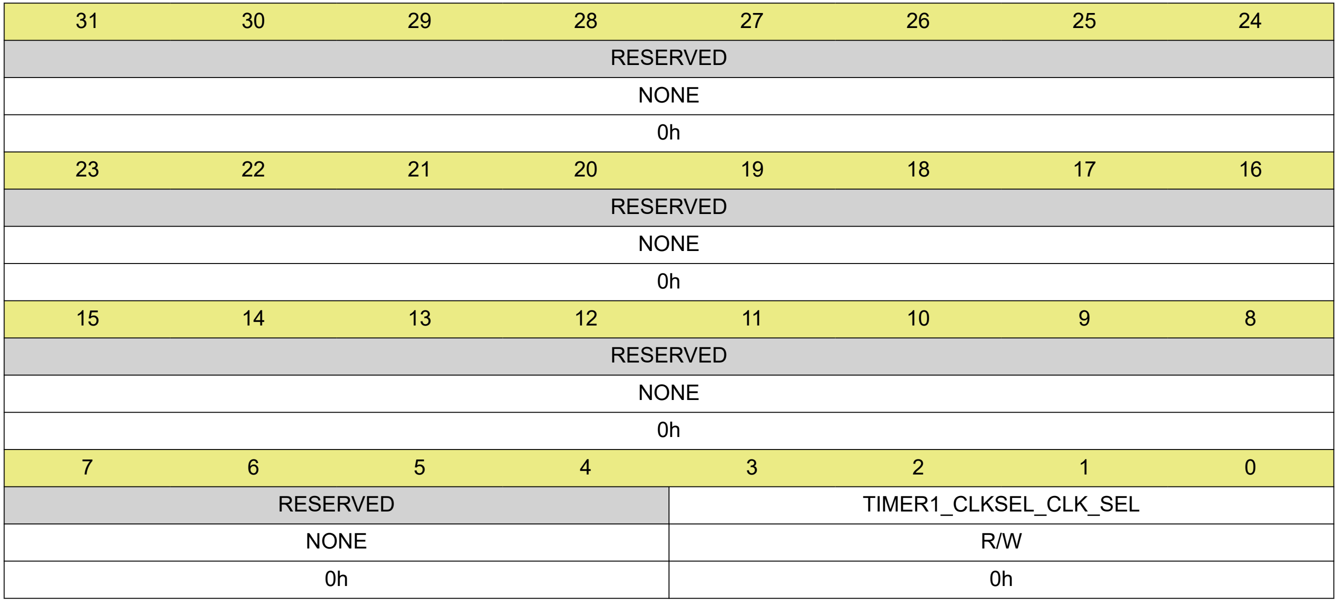
Table 14-4496. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81B4h

Figure 14-2236. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Name Register



31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER1_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4497. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER1_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.182 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register

14.2.1.1.1.2.182.1 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register (Offset = 81B8h) [reset = 0h]

Timer2 functional clock selection control

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Table 14-4498. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81B8h

Figure 14-2237. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER2_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4499. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER2_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.183 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register

14.2.1.1.1.2.183.1 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register (Offset = 81BCh) [reset = 0h]

Timer3 functional clock selection control

Return to Summary Table

Table 14-4500. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81BCh

Figure 14-2238. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER3_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4501. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER3_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.184 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register

14.2.1.1.1.2.184.1 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register (Offset = 81C0h) [reset = 0h]

Timer4 functional clock selection control

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Table 14-4502. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81C0h

Figure 14-2239. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER4_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4503. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER4_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.185 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register

14.2.1.1.1.2.185.1 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register (Offset = 81C4h) [reset = 0h]

Timer5 functional clock selection control

Return to Summary Table

Table 14-4504. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81C4h

Figure 14-2240. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMER5_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4505. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER5_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.186 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register

14.2.1.1.1.2.186.1 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register (Offset = 81C8h) [reset = 0h]

Timer6 functional clock selection control

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Table 14-4506. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81C8h

Figure 14-2241. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER6_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4507. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER6_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.187 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register

14.2.1.1.1.2.187.1 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register (Offset = 81CCh) [reset = 0h]

Timer7 functional clock selection control

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Table 14-4508. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81CCh

Figure 14-2242. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER7_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4509. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER7_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.188 MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL Register

14.2.1.1.1.2.188.1 MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL Register (Offset = 81D0h) [reset = 0h]

Timer8 functional clock selection control

Return to Summary Table

Table 14-4510. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81D0h

Figure 14-2243. MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER8_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4511. MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER8_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.189 MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL Register

14.2.1.1.1.2.189.1 MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL Register (Offset = 81D4h) [reset = 0h]

Timer9 functional clock selection control

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Table 14-4512. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81D4h

Figure 14-2244. MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER9_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4513. MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER9_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.190 MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL Register

14.2.1.1.1.2.190.1 MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL Register (Offset = 81D8h) [reset = 0h]

Timer10 functional clock selection control

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Table 14-4514. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81D8h

Figure 14-2245. MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER10_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4515. MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER10_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.191 MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL Register

14.2.1.1.1.2.191.1 MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL Register (Offset = 81DCh) [reset = 0h]

Timer11 functional clock selection control

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Table 14-4516. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81DCh

Figure 14-2246. MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER11_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4517. MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER11_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.192 MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL Register

14.2.1.1.1.2.192.1 MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL Register (Offset = 81E0h) [reset = 0h]

Timer12 functional clock selection control

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Table 14-4518. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81E0h

Figure 14-2247. MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER12_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4519. MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER12_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.193 MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL Register

14.2.1.1.1.2.193.1 MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL Register (Offset = 81E4h) [reset = 0h]

Timer13 functional clock selection control

Return to Summary Table

Table 14-4520. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81E4h

Figure 14-2248. MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER13_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4521. MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER13_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.194 MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL Register

14.2.1.1.1.2.194.1 MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL Register (Offset = 81E8h) [reset = 0h]

Timer14 functional clock selection control

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Table 14-4522. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81E8h

Figure 14-2249. MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER14_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4523. MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER14_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.195 MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL Register

14.2.1.1.1.2.195.1 MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL Register (Offset = 81ECh) [reset = 0h]

Timer15 functional clock selection control

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Table 14-4524. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 81ECh

Figure 14-2250. MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER15_CLKSEL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-4525. MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER15_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.196 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register

14.2.1.1.1.2.196.1 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register (Offset = 8200h) [reset = 0h]

SPI0 clock control

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Table 14-4526. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8200h

Figure 14-2251. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SPI0_CLKSEL_MSTR_LB_CLKSEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4527. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI0_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.197 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register

14.2.1.1.1.2.197.1 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register (Offset = 8204h) [reset = 0h]

SPI1 clock control

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Table 14-4528. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8204h

Figure 14-2252. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI1_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4529. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI1_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.198 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register

14.2.1.1.1.2.198.1 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register (Offset = 8208h) [reset = 0h]

SPI2 clock control

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Table 14-4530. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8208h

Figure 14-2253. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI2_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4531. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI2_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.199 MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL Register

14.2.1.1.1.2.199.1 MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL Register (Offset = 820Ch) [reset = 0h]

SPI3 clock control

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Table 14-4532. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 820Ch

Figure 14-2254. MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI3_CLKSEL_MSTR_LB_CLKSEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4533. MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI3_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.200 MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL Register

14.2.1.1.1.2.200.1 MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL Register (Offset = 8210h) [reset = 0h]

SPI4 clock control

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Table 14-4534. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8210h

Figure 14-2255. MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>SPI4_CLKSEL_MSTR_LB_CLKSEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4535. MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI4_CLKSEL_MSTR_LB_CLKSEL	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.201 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register

14.2.1.1.1.2.201.1 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register (Offset = 8240h) [reset = 3h]

Selects the clock divider of the USART0 functional clock

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Table 14-4536. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8240h

Figure 14-2256. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART0_CLK_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART0_CLK_CTRL_CLK_DIV</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-4537. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART0_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART0 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART0_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.202 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register

14.2.1.1.1.2.202.1 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register (Offset = 8244h) [reset = 3h]

Selects the clock divider of the USART1 functional clock

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Table 14-4538. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8244h

Figure 14-2257. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART1_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART1_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-4539. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART1_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART1 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART1_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.203 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register

14.2.1.1.1.2.203.1 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register (Offset = 8248h) [reset = 3h]

Selects the clock divider of the USART2 functional clock

Return to Summary Table

Table 14-4540. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8248h

Figure 14-2258. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART2_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART2_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-4541. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART2_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART2 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART2_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.204 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register

14.2.1.1.1.2.204.1 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register (Offset = 824Ch) [reset = 3h]

Selects the clock divider of the USART3 functional clock

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Table 14-4542. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 824Ch

Figure 14-2259. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART3_CLK_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART3_CLK_CTRL_CLK_DIV</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-4543. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART3_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART3 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART3_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.205 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register

14.2.1.1.1.2.205.1 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register (Offset = 8250h) [reset = 3h]

Selects the clock divider of the USART4 functional clock

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Table 14-4544. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8250h

Figure 14-2260. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART4_CLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART4_CLK_CTRL_CLK_DIV	
NONE						R/W	
0h						3h	

Table 14-4545. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART4_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART4 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART4_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.206 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register

14.2.1.1.1.2.206.1 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register (Offset = 8254h) [reset = 3h]

Selects the clock divider of the USART5 functional clock

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Table 14-4546. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8254h

Figure 14-2261. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART5_CLK_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART5_CLK_CTRL_CLK_DIV</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-4547. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART5_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART5 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART5_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.207 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register

14.2.1.1.1.2.207.1 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register (Offset = 8258h) [reset = 3h]

Selects the clock divider of the USART6 functional clock

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Table 14-4548. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8258h

Figure 14-2262. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART6_CLK_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART6_CLK_CTRL_CLK_DIV</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-4549. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART6_CLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART6 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART6_CLK_CTRL_CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.208 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register

14.2.1.1.1.2.208.1 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register (Offset = 8280h) [reset = 0h]

Selects the clock source for USART0 functional clock

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Table 14-4550. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8280h

Figure 14-2263. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART0_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-4551. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART0_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART0: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART0_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.209 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register

14.2.1.1.1.2.209.1 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register (Offset = 8284h) [reset = 0h]

Selects the clock source for USART1 functional clock

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Table 14-4552. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8284h

Figure 14-2264. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART1_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-4553. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART1_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART1: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART1_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.210 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register

14.2.1.1.1.2.210.1 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register (Offset = 8288h) [reset = 0h]

Selects the clock source for USART2 functional clock

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Table 14-4554. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8288h

Figure 14-2265. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART2_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-4555. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART2_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART2: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART2_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.211 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register

14.2.1.1.1.2.211.1 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register (Offset = 828Ch) [reset = 0h]

Selects the clock source for USART3 functional clock

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Table 14-4556. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 828Ch

Figure 14-2266. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART3_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-4557. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART3_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART3: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART3_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.212 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register

14.2.1.1.1.2.212.1 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register (Offset = 8290h) [reset = 0h]

Selects the clock source for USART4 functional clock

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Table 14-4558. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8290h

Figure 14-2267. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART4_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-4559. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART4_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART4: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART4_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.213 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register

14.2.1.1.1.2.213.1 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register (Offset = 8294h) [reset = 0h]

Selects the clock source for USART5 functional clock

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Table 14-4560. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8294h

Figure 14-2268. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART5_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-4561. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART5_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART5: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART5_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.214 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register

14.2.1.1.1.2.214.1 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register (Offset = 8298h) [reset = 0h]

Selects the clock source for USART6 functional clock

Return to Summary Table

Table 14-4562. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8298h

Figure 14-2269. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART6_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-4563. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART6_CLKSEL_CLK_SEL	R/W	0h	Selects the clock source for UART6: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART6_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.215 MAIN_CTRL_MMR_CFG0_ATL_CLKSEL Register

14.2.1.1.1.2.215.1 MAIN_CTRL_MMR_CFG0_ATL_CLKSEL Register (Offset = 82B0h) [reset = 0h]

Selects the source of ATL PCLK which drives ATL Measurement and Adjustment Logic

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Table 14-4564. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82B0h

Figure 14-2270. MAIN_CTRL_MMR_CFG0_ATL_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ATL_CLKSEL_PCLK_SEL		
NONE					R/W		
0h					0h		

Table 14-4565. MAIN_CTRL_MMR_CFG0_ATL_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ATL_CLKSEL_PCLK_SEL	R/W	0h	Selects the PCLK clock source Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b010 - MAIN_PLL2_HSDIV0_CLKOUT 3'b011 - MAIN_PLL4_HSDIV1_CLKOUT 3'b100 - MAIN_PLL0_HSDIV7_CLKOUT 3'b101 - MCU_EXT_REFCLK0 (Pin) 3'b110 - EXT_REFCLK1 (Pin) Reset Source: mod_g_rst_n

14.2.1.1.1.2.216 MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL Register

14.2.1.1.1.2.216.1 MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL Register (Offset = 82C0h) [reset = 0h]

Selects the word clock for the ATL channel0 Baseband Stream

Return to Summary Table

Table 14-4566. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82C0h

Figure 14-2271. MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_BWS0_SEL_WD_SEL			
NONE				R/W			
0h				0h			

Table 14-4567. MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_BWS0_SEL_WD_SEL	R/W	0h	BWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSR_IN 4'b0001 - MCASP1_AFSR_IN 4'b0010 - MCASP2_AFSR_IN 4'b0011 - MCASP3_AFSR_IN 4'b0100 - MCASP4_AFSR_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.217 MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL Register

14.2.1.1.1.2.217.1 MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL Register (Offset = 82C4h) [reset = 0h]

Selects the word clock for the ATL channel1 Baseband Stream

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Table 14-4568. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82C4h

Figure 14-2272. MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ATL_BWS1_SEL_WD_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4569. MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_BWS1_SEL_WD_SEL	R/W	0h	BWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSR_IN 4'b0001 - MCASP1_AFSR_IN 4'b0010 - MCASP2_AFSR_IN 4'b0011 - MCASP3_AFSR_IN 4'b0100 - MCASP4_AFSR_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.218 MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL Register

14.2.1.1.1.2.218.1 MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL Register (Offset = 82C8h) [reset = 0h]

Selects the word clock for the ATL channel2 Baseband Stream

Return to Summary Table

Table 14-4570. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82C8h

Figure 14-2273. MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_BWS2_SEL_WD_SEL			
NONE				R/W			
0h				0h			

Table 14-4571. MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_BWS2_SEL_WD_SEL	R/W	0h	BWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSR_IN 4'b0001 - MCASP1_AFSR_IN 4'b0010 - MCASP2_AFSR_IN 4'b0011 - MCASP3_AFSR_IN 4'b0100 - MCASP4_AFSR_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.219 MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL Register

14.2.1.1.1.2.219.1 MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL Register (Offset = 82CCh) [reset = 0h]

Selects the word clock for the ATL channel3 Baseband Stream

Return to Summary Table

Table 14-4572. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82CCh

Figure 14-2274. MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_BWS3_SEL_WD_SEL			
NONE				R/W			
0h				0h			

Table 14-4573. MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_BWS3_SEL_WD_SEL	R/W	0h	BWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSR_IN 4'b0001 - MCASP1_AFSR_IN 4'b0010 - MCASP2_AFSR_IN 4'b0011 - MCASP3_AFSR_IN 4'b0100 - MCASP4_AFSR_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.220 MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL Register

14.2.1.1.1.2.220.1 MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL Register (Offset = 82D0h) [reset = 0h]

Selects the word clock for the ATL channel0 Audio Stream

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Table 14-4574. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82D0h

Figure 14-2275. MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_AWS0_SEL_WD_SEL			
NONE				R/W			
0h				0h			

Table 14-4575. MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_AWS0_SEL_WD_SEL	R/W	0h	AWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSX_IN 4'b0001 - MCASP1_AFSX_IN 4'b0010 - MCASP2_AFSX_IN 4'b0011 - MCASP3_AFSX_IN 4'b0100 - MCASP4_AFSX_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.221 MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL Register

14.2.1.1.1.2.221.1 MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL Register (Offset = 82D4h) [reset = 0h]

Selects the word clock for the ATL channel1 Audio Stream

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Table 14-4576. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82D4h

Figure 14-2276. MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_AWS1_SEL_WD_SEL			
NONE				R/W			
0h				0h			

Table 14-4577. MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_AWS1_SEL_WD_SEL	R/W	0h	AWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSX_IN 4'b0001 - MCASP1_AFSX_IN 4'b0010 - MCASP2_AFSX_IN 4'b0011 - MCASP3_AFSX_IN 4'b0100 - MCASP4_AFSX_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.222 MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL Register

14.2.1.1.1.2.222.1 MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL Register (Offset = 82D8h) [reset = 0h]

Selects the word clock for the ATL channel2 Audio Stream

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Table 14-4578. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82D8h

Figure 14-2277. MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ATL_AWS2_SEL_WD_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4579. MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_AWS2_SEL_WD_SEL	R/W	0h	AWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSX_IN 4'b0001 - MCASP1_AFSX_IN 4'b0010 - MCASP2_AFSX_IN 4'b0011 - MCASP3_AFSX_IN 4'b0100 - MCASP4_AFSX_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.223 MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL Register

14.2.1.1.1.2.223.1 MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL Register (Offset = 82DCh) [reset = 0h]

Selects the word clock for the ATL channel3 Audio Stream

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Table 14-4580. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82DCh

Figure 14-2278. MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_AWS3_SEL_WD_SEL			
NONE				R/W			
0h				0h			

Table 14-4581. MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_AWS3_SEL_WD_SEL	R/W	0h	AWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSX_IN 4'b0001 - MCASP1_AFSX_IN 4'b0010 - MCASP2_AFSX_IN 4'b0011 - MCASP3_AFSX_IN 4'b0100 - MCASP4_AFSX_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.224 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Register

14.2.1.1.1.2.224.1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Register (Offset = 82E0h) [reset = Fh]

Selects the clock source for the AUDIO_EXT_REFCLK0 output, and direction.

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Table 14-4582. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82E0h

Figure 14-2279. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AUDIO_REFCLK0_CTRL_CLKOUT_EN	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				AUDIO_REFCLK0_CTRL_CLK_SEL			
NONE				R/W			
0h				Fh			

Table 14-4583. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK0_CTRL_CLKOUT_EN	R/W	0h	AUDIO_REFCLK 0 output enable Field values (others are reserved): 1'b0 - INPUT 1'b1 - OUTPUT Reset Source: mod_g_rst_n
14:4	RESERVED	NONE	0h	Reserved

Table 14-4583. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	AUDIO_REFCLK0_CTRL_CLK_SEL	R/W	Fh	Selects the source of AUDIO_REFCLK0 Field values (others are reserved): 4'b0000 - MCASP0_AHCLKR 4'b0001 - MCASP1_AHCLKR 4'b0010 - MCASP2_AHCLKR 4'b0011 - MCASP3_AHCLKR 4'b0100 - MCASP4_AHCLKR 4'b0101 - MCASP0_AHCLKX 4'b0110 - MCASP1_AHCLKX 4'b0111 - MCASP2_AHCLKX 4'b1000 - MCASP3_AHCLKX 4'b1001 - MCASP4_AHCLKX 4'b1010 - ATCLK0 4'b1011 - ATCLK1 4'b1100 - ATCLK2 4'b1101 - ATCLK3 4'b1110 - MAIN_PLL1_HSDIV6_CLKOUT undefined - undefined 4'b1111 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.225 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Register

14.2.1.1.1.2.225.1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Register (Offset = 82E4h) [reset = Fh]

Selects the clock source for the AUDIO_EXT_REFCLK0 output, and direction.

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Table 14-4584. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82E4h

Figure 14-2280. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>AUDIO_REFCLK1_CTRL_CLKOUT_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">AUDIO_REFCLK1_CTRL_CLK_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-4585. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK1_CTRL_CLKOUT_EN	R/W	0h	AUDIO_REFCLK 1 output enable Field values (others are reserved): 1'b0 - INPUT 1'b1 - OUTPUT Reset Source: mod_g_rst_n
14:4	RESERVED	NONE	0h	Reserved

Table 14-4585. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	AUDIO_REFCLK1_CTRL_CLK_SEL	R/W	Fh	Selects the source of AUDIO_REFCLK1 Field values (others are reserved): 4'b0000 - MCASP0_AHCLKR 4'b0001 - MCASP1_AHCLKR 4'b0010 - MCASP2_AHCLKR 4'b0011 - MCASP3_AHCLKR 4'b0100 - MCASP4_AHCLKR 4'b0101 - MCASP0_AHCLKX 4'b0110 - MCASP1_AHCLKX 4'b0111 - MCASP2_AHCLKX 4'b1000 - MCASP3_AHCLKX 4'b1001 - MCASP4_AHCLKX 4'b1010 - ATCLK0 4'b1011 - ATCLK1 4'b1100 - ATCLK2 4'b1101 - ATCLK3 4'b1110 - MAIN_PLL1_HSDIV6_CLKOUT undefined - undefined 4'b1111 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.226 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL Register

14.2.1.1.1.2.226.1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL Register (Offset = 82E8h) [reset = Fh]

Selects the clock source for the AUDIO_EXT_REFCLK0 output, and direction.

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Table 14-4586. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82E8h

Figure 14-2281. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>AUDIO_REFCLK2_CTRL_CLKOUT_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">AUDIO_REFCLK2_CTRL_CLK_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-4587. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK2_CTRL_CLKOUT_EN	R/W	0h	AUDIO_REFCLK 2 output enable Field values (others are reserved): 1'b0 - INPUT 1'b1 - OUTPUT Reset Source: mod_g_rst_n
14:4	RESERVED	NONE	0h	Reserved

Table 14-4587. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	AUDIO_REFCLK2_CTRL_CLK_SEL	R/W	Fh	Selects the source of AUDIO_REFCLK2 Field values (others are reserved): 4'b0000 - MCASP0_AHCLKR 4'b0001 - MCASP1_AHCLKR 4'b0010 - MCASP2_AHCLKR 4'b0011 - MCASP3_AHCLKR 4'b0100 - MCASP4_AHCLKR 4'b0101 - MCASP0_AHCLKX 4'b0110 - MCASP1_AHCLKX 4'b0111 - MCASP2_AHCLKX 4'b1000 - MCASP3_AHCLKX 4'b1001 - MCASP4_AHCLKX 4'b1010 - ATCLK0 4'b1011 - ATCLK1 4'b1100 - ATCLK2 4'b1101 - ATCLK3 4'b1110 - MAIN_PLL1_HSDIV6_CLKOUT undefined - undefined 4'b1111 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.227 MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL Register

14.2.1.1.1.2.227.1 MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL Register (Offset = 82F0h) [reset = 0h]

Selects additional divide value for the MAIN_PLL4 clock source to the ASRC RXSYNC and TXSYNC selection muxes

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Table 14-4588. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 82F0h

Figure 14-2282. MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>ASRC_SYNC_DIV_CTRL_CLK_DIV_LD</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ASRC_SYNC_DIV_CTRL_CLK_DIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4589. MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	ASRC_SYNC_DIV_CTRL_CLK_DIV_LD	R/W	0h	Load the divider value Writing 1 to this bit will generate a load pulse to load the clk_div divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	ASRC_SYNC_DIV_CTRL_CLK_DIV	R/W	0h	ASRC Sync divider value Divides MAIN_PLL4_HSDIV_CLKOUT3 by clkdiv+1. Supports divide by 1 to 16 (default to 1). To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.228 MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL Register

14.2.1.1.1.2.228.1 MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL Register (Offset = 8330h) [reset = 0h]

Selects the functional clock source for McASP0

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Table 14-4590. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8330h

Figure 14-2283. MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP0_CLKSEL_LOC_AUXCLK_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED					MCASP0_CLKSEL_AUXCLK_SEL		
NONE					R/W		
0h					0h		

Table 14-4591. MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP0_CLKSEL_LOC_AUXCLK_SEL	R/W	0h	Selects the local clock source to use for McASP0 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP0_CLKSEL_AUXCLK_SEL	R/W	0h	Selects the system AUXCLK input source for McASP0 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.229 MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL Register

14.2.1.1.1.2.229.1 MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL Register (Offset = 8334h) [reset = 0h]

Selects the functional clock source for McASP1

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Table 14-4592. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8334h

Figure 14-2284. MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						MCASP1_CLKSEL_LOC_AUXCLK_SEL	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
RESERVED					MCASP1_CLKSEL_AUXCLK_SEL		
NONE					R/W		
0h					0h		

Table 14-4593. MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP1_CLKSEL_LOC_AUXCLK_SEL	R/W	0h	Selects the local clock source to use for McASP1 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP1_CLKSEL_AUXCLK_SEL	R/W	0h	Selects the system AUXCLK input source for McASP1 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.230 MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL Register

14.2.1.1.1.2.230.1 MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL Register (Offset = 8338h) [reset = 0h]

Selects the functional clock source for McASP2

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Table 14-4594. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8338h

Figure 14-2285. MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MCASP2_CLKSEL_LOC_AUXCLK_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MCASP2_CLKSEL_AUXCLK_SEL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4595. MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP2_CLKSEL_LOC_AUXCLK_SEL	R/W	0h	Selects the local clock source to use for McASP2 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP2_CLKSEL_AUXCLK_SEL	R/W	0h	Selects the system AUXCLK input source for McASP2 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.231 MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL Register

14.2.1.1.1.2.231.1 MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL Register (Offset = 833Ch) [reset = 0h]

Selects the functional clock source for McASP3

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Table 14-4596. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 833Ch

Figure 14-2286. MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP3_CLKSEL_LOC_AUXCLK_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED					MCASP3_CLKSEL_AUXCLK_SEL		
NONE					R/W		
0h					0h		

Table 14-4597. MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP3_CLKSEL_LOC_AUXCLK_SEL	R/W	0h	Selects the local clock source to use for McASP3 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP3_CLKSEL_AUXCLK_SEL	R/W	0h	Selects the system AUXCLK input source for McASP3 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.232 MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL Register

14.2.1.1.1.2.232.1 MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL Register (Offset = 8340h) [reset = 0h]

Selects the functional clock source for McASP4

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Table 14-4598. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8340h

Figure 14-2287. MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						MCASP4_CLKSEL_LOC_AUXCLK_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MCASP4_CLKSEL_AUXCLK_SEL		
NONE					R/W		
0h					0h		

Table 14-4599. MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP4_CLKSEL_LOC_AUXCLK_SEL	R/W	0h	Selects the local clock source to use for McASP4 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP4_CLKSEL_AUXCLK_SEL	R/W	0h	Selects the system AUXCLK input source for McASP4 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.233 MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Register

14.2.1.1.1.2.233.1 MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Register (Offset = 8350h) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP0

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Table 14-4600. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8350h

Figure 14-2288. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCASP0_AHCLKSEL_AHCLKX_SEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCASP0_AHCLKSEL_AHCLKR_SEL			
NONE				R/W			
0h				0h			

Table 14-4601. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP0_AHCLKSEL_AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP0 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4601. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP0_AHCLKSEL_AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP0 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.234 MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Register

14.2.1.1.1.2.234.1 MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Register (Offset = 8354h) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP1

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Table 14-4602. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8354h

Figure 14-2289. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED				MCASP1_AHCLKSEL_AHCLKX_SEL			
NONE				R/W			
0h				0h			

7	6	5	4	3	2	1	0
RESERVED				MCASP1_AHCLKSEL_AHCLKR_SEL			
NONE				R/W			
0h				0h			

Table 14-4603. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP1_AHCLKSEL_AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP1 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4603. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP1_AHCLKSEL_AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP1 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.235 MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Register

14.2.1.1.1.2.235.1 MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Register (Offset = 8358h) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP2

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Table 14-4604. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8358h

Figure 14-2290. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MCASP2_AHCLKSEL_AHCLKX_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MCASP2_AHCLKSEL_AHCLKR_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4605. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP2_AHCLKSEL_AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP2 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4605. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP2_AHCLKSEL_AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP2 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.236 MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL Register

14.2.1.1.1.2.236.1 MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL Register (Offset = 835Ch) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP3

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Table 14-4606. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 835Ch

Figure 14-2291. MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCASP3_AHCLKSEL_AHCLKX_SEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MCASP3_AHCLKSEL_AHCLKR_SEL			
NONE				R/W			
0h				0h			

Table 14-4607. MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP3_AHCLKSEL_AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP3 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4607. MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP3_AHCLKSEL_AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP3 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.237 MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL Register

14.2.1.1.1.2.237.1 MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL Register (Offset = 8360h) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP4

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Table 14-4608. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8360h

Figure 14-2292. MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCASP4_AHCLKSEL_AHCLKX_SEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCASP4_AHCLKSEL_AHCLKR_SEL			
NONE				R/W			
0h				0h			

Table 14-4609. MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP4_AHCLKSEL_AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP4 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4609. MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP4_AHCLKSEL_AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP4 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.238 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register

14.2.1.1.1.2.238.1 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register (Offset = 8380h) [reset = 0h]

Windowed Watchdog WWD0 functional clock selection control

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Table 14-4610. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8380h

Figure 14-2293. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD0_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4611. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD0_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD0_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.239 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register

14.2.1.1.1.2.239.1 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register (Offset = 8384h) [reset = 0h]

Windowed Watchdog WWD1 functional clock selection control

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Table 14-4612. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8384h

Figure 14-2294. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD1_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED						WWD1_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4613. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD1_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD1_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD1_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.240 MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL Register

14.2.1.1.1.2.240.1 MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL Register (Offset = 8388h) [reset = 0h]

Windowed Watchdog WWD2 functional clock selection control

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Table 14-4614. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8388h

Figure 14-2295. MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD2_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD2_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4615. MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD2_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD2_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD2_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.241 MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL Register

14.2.1.1.1.2.241.1 MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL Register (Offset = 838Ch) [reset = 0h]

Windowed Watchdog WWD3 functional clock selection control

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Table 14-4616. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 838Ch

Figure 14-2296. MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD3_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD3_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4617. MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD3_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD3_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD3_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.242 MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL Register

14.2.1.1.1.2.242.1 MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL Register (Offset = 8390h) [reset = 0h]

Windowed Watchdog WWD4 functional clock selection control

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Table 14-4618. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8390h

Figure 14-2297. MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD4_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD4_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4619. MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD4_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD4_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD4_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.243 MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL Register

14.2.1.1.1.2.243.1 MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL Register (Offset = 8394h) [reset = 0h]

Windowed Watchdog WWD5 functional clock selection control

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Table 14-4620. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8394h

Figure 14-2298. MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL Name Register

31	30	29	28	27	26	25	24
WWD5_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD5_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4621. MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD5_CLKSEL_WRTLOCK	R/W	0h	When set, locks WWD5_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD5_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.244 MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL Register

14.2.1.1.1.2.244.1 MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL Register (Offset = 83E0h) [reset = 0h]

Performs glitchfree selection of the McASP0 functional clock

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Table 14-4622. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 83E0h

Figure 14-2299. MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCASP0_GF_CLK_SEL_AUXCLK_GF_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4623. MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP0_GF_CLK_SEL_AUXCLK_GF_SEL	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP0 based on MCASP0_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.245 MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL Register

14.2.1.1.1.2.245.1 MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL Register (Offset = 83E4h) [reset = 0h]

Performs glitchfree selection of the McASP1 functional clock

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Table 14-4624. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 83E4h

Figure 14-2300. MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCASP1_GF_CLK_SEL_AUXCLK_GF_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4625. MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP1_GF_CLK_SEL_AUXCLK_GF_SEL	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP1 based on MCASP1_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.246 MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL Register

14.2.1.1.1.2.246.1 MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL Register (Offset = 83E8h) [reset = 0h]

Performs glitchfree selection of the McASP2 functional clock

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Table 14-4626. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 83E8h

Figure 14-2301. MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCASP2_GF_CLK_SEL_AUXCLK_GF_SEL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4627. MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP2_GF_CLK_SEL_AUXCLK_GF_SEL	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP2 based on MCASP2_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.247 MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL Register

14.2.1.1.1.2.247.1 MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL Register (Offset = 83ECh) [reset = 0h]

Performs glitchfree selection of the McASP3 functional clock

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Table 14-4628. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 83ECh

Figure 14-2302. MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCASP3_GF_CLK_SEL_AUXCLK_GF_SEL</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4629. MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP3_GF_CLK_SEL_AUXCLK_GF_SEL	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP3 based on MCASP3_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.248 MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL Register

14.2.1.1.1.2.248.1 MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL Register (Offset = 83F0h) [reset = 0h]

Performs glitchfree selection of the McASP4 functional clock

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Table 14-4630. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 83F0h

Figure 14-2303. MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MCASP4_GF_CLK_SEL_AUXCLK_GF_SEL
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-4631. MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP4_GF_CLK_SEL_AUXCLK_GF_SEL	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP4 based on MCASP4_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.249 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register

14.2.1.1.1.2.249.1 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register (Offset = 8480h) [reset = 0h]

Controls the functional clock source for MCAN0

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Table 14-4632. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8480h

Figure 14-2304. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4633. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN0_CLKSEL_CLK_SEL	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.250 MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL Register

14.2.1.1.1.2.250.1 MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL Register (Offset = 8484h) [reset = 0h]

Controls the functional clock source for MCAN1

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Table 14-4634. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8484h

Figure 14-2305. MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN1_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4635. MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN1_CLKSEL_CLK_SEL	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.251 MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL Register

14.2.1.1.1.2.251.1 MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL Register (Offset = 8488h) [reset = 0h]

Controls the functional clock source for MCAN2

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Table 14-4636. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8488h

Figure 14-2306. MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MCAN2_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-4637. MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN2_CLKSEL_CLK_SEL	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.252 MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL Register

14.2.1.1.1.2.252.1 MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL Register (Offset = 848Ch) [reset = 0h]

Controls the functional clock source for MCAN3

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Table 14-4638. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 848Ch

Figure 14-2307. MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN3_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-4639. MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN3_CLKSEL_CLK_SEL	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.253 MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL Register

14.2.1.1.1.2.253.1 MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL Register (Offset = 8490h) [reset = 0h]

Controls the functional clock source for MCAN4

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Table 14-4640. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8490h

Figure 14-2308. MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MCAN4_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-4641. MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN4_CLKSEL_CLK_SEL	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.254 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL Register

14.2.1.1.1.2.254.1 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL Register (Offset = 84C0h) [reset = 0h]

Selects the source signal for the ASRC0 RXSYNC0 frame sync input

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Table 14-4642. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84C0h

Figure 14-2309. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED			ASRC0_RXSYNC0_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4643. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4643. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_RXSYNC0_SEL_SYNC_SEL	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.255 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL Register

14.2.1.1.1.2.255.1 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL Register (Offset = 84C4h) [reset = 0h]

Selects the source signal for the ASRC0 RXSYNC1 frame sync input

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Table 14-4644. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84C4h

Figure 14-2310. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_RXSYNC1_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4645. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4645. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_RXSYNC1_SEL_SYNC_SEL	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.256 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL Register

14.2.1.1.1.2.256.1 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL Register (Offset = 84C8h) [reset = 0h]

Selects the source signal for the ASRC0 RXSYNC2 frame sync input

Return to Summary Table

Table 14-4646. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84C8h

Figure 14-2311. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_RXSYNC2_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4647. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4647. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_RXSYNC2_SEL_SYNC_SEL	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.257 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL Register

14.2.1.1.1.2.257.1 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL Register (Offset = 84CCh) [reset = 0h]

Selects the source signal for the ASRC0 RXSYNC3 frame sync input

Return to Summary Table

Table 14-4648. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84CCh

Figure 14-2312. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_RXSYNC3_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4649. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4649. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_RXSYNC3_SEL_SYNC_SEL	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.258 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL Register

14.2.1.1.1.2.258.1 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL Register (Offset = 84D0h) [reset = 0h]

Selects the source signal for the ASRC1 RXSYNC0 frame sync input

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Table 14-4650. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84D0h

Figure 14-2313. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ASRC1_RXSYNC0_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4651. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4651. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_RXSYNC0_SEL_SYNC_SEL	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.259 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL Register

14.2.1.1.1.2.259.1 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL Register (Offset = 84D4h) [reset = 0h]

Selects the source signal for the ASRC1 RXSYNC1 frame sync input

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Table 14-4652. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84D4h

Figure 14-2314. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ASRC1_RXSYNC1_SEL_SYNC_SEL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-4653. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4653. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_RXSYNC1_SEL_SYNC_SEL	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.260 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL Register

14.2.1.1.1.2.260.1 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL Register (Offset = 84D8h) [reset = 0h]

Selects the source signal for the ASRC1 RXSYNC2 frame sync input

Return to Summary Table

Table 14-4654. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84D8h

Figure 14-2315. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_RXSYNC2_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4655. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4655. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_RXSYNC2_SEL_SYNC_SEL	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.261 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL Register

14.2.1.1.1.2.261.1 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL Register (Offset = 84DCh) [reset = 0h]

Selects the source signal for the ASRC1 RXSYNC3 frame sync input

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Table 14-4656. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84DCh

Figure 14-2316. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_RXSYNC3_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4657. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4657. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_RXSYNC3_SEL_SYNC_SEL	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.262 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL Register

14.2.1.1.1.2.262.1 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL Register (Offset = 84E0h) [reset = 0h]

Selects the source signal for the ASRC0 TXSYNC0 frame sync input

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Table 14-4658. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84E0h

Figure 14-2317. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_TXSYNC0_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4659. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4659. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_TXSYNC0_SEL_SYNC_SEL	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.263 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL Register

14.2.1.1.1.2.263.1 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL Register (Offset = 84E4h) [reset = 0h]

Selects the source signal for the ASRC0 TXSYNC1 frame sync input

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Table 14-4660. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84E4h

Figure 14-2318. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_TXSYNC1_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4661. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4661. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_TXSYNC1_SEL_SYNC_SEL	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.264 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL Register

14.2.1.1.1.2.264.1 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL Register (Offset = 84E8h) [reset = 0h]

Selects the source signal for the ASRC0 TXSYNC2 frame sync input

Return to Summary Table

Table 14-4662. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84E8h

Figure 14-2319. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_TXSYNC2_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4663. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4663. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_TXSYNC2_SEL_SYNC_SEL	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.265 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL Register

14.2.1.1.1.2.265.1 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL Register (Offset = 84ECh) [reset = 0h]

Selects the source signal for the ASRC0 TXSYNC3 frame sync input

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Table 14-4664. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84ECh

Figure 14-2320. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_TXSYNC3_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4665. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4665. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_TXSYNC3_SEL_SYNC_SEL	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.266 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL Register

14.2.1.1.1.2.266.1 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL Register (Offset = 84F0h) [reset = 0h]

Selects the source signal for the ASRC1 TXSYNC0 frame sync input

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Table 14-4666. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84F0h

Figure 14-2321. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_TXSYNC0_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4667. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4667. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_TXSYNC0_SEL_SYNC_SEL	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.267 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL Register

14.2.1.1.1.2.267.1 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL Register (Offset = 84F4h) [reset = 0h]

Selects the source signal for the ASRC1 TXSYNC1 frame sync input

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Table 14-4668. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84F4h

Figure 14-2322. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_TXSYNC1_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4669. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4669. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_TXSYNC1_SEL_SYNC_SEL	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.268 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL Register

14.2.1.1.1.2.268.1 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL Register (Offset = 84F8h) [reset = 0h]

Selects the source signal for the ASRC1 TXSYNC2 frame sync input

Return to Summary Table

Table 14-4670. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84F8h

Figure 14-2323. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_TXSYNC2_SEL_SYNC_SEL				
NONE			R/W				
0h			0h				

Table 14-4671. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4671. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_TXSYNC2_SEL_SYNC_SEL	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.269 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL Register

14.2.1.1.1.2.269.1 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL Register (Offset = 84FCh) [reset = 0h]

Selects the source signal for the ASRC1 TXSYNC3 frame sync input

Return to Summary Table

Table 14-4672. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 84FCh

Figure 14-2324. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ASRC1_TXSYNC3_SEL_SYNC_SEL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-4673. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4673. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_TXSYNC3_SEL_SYNC_SEL	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.270 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register

14.2.1.1.1.2.270.1 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register (Offset = 8500h) [reset = 0h]

Controls the OSPI loopback clock source

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Table 14-4674. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8500h

Figure 14-2325. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			OSPI0_CLKSEL_LOOPCLK_SEL	RESERVED			OSPI0_CLKSEL_CLK_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-4675. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	OSPI0_CLKSEL_LOOPCLK_SEL	R/W	0h	OSPI0 Loopback clock source Field values (others are reserved): 1'b0 - Board Level Loopback 1'b1 - Internal Loopback Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	OSPI0_CLKSEL_CLK_SEL	R/W	0h	OSPI0 reference clock selection Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV1_CLKOUT 1'b1 - MAIN_PLL1_HSDIV5_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.271 MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL Register

14.2.1.1.1.2.271.1 MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL Register (Offset = 8504h) [reset = 0h]

Controls the OSPI loopback clock source

Return to Summary Table

Table 14-4676. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8504h

Figure 14-2326. MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			OSPI1_CLKSEL_LOOPCLK_SEL	RESERVED			OSPI1_CLKSEL_CLK_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-4677. MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	OSPI1_CLKSEL_LOOPCLK_SEL	R/W	0h	OSPI1 Loopback clock source Field values (others are reserved): 1'b0 - Board Level Loopback 1'b1 - Internal Loopback Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	OSPI1_CLKSEL_CLK_SEL	R/W	0h	OSPI1 reference clock selection Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV1_CLKOUT 1'b1 - MAIN_PLL1_HSDIV5_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.272 MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL Register

14.2.1.1.1.2.272.1 MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL Register (Offset = 8510h) [reset = 0h]

Controls the functional clock source for the ADC0

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Table 14-4678. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8510h

Figure 14-2327. MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">ADC0_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-4679. MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ADC0_CLKSEL_CLK_SEL	R/W	0h	Selects the sampling clock source for ADC0 Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - HFOSC1_CLKOUT 2'b10 - MAIN_PLL1_HSDIV4_CLKOUT 2'b11 - EXT_REFCLK1 (Pin) Reset Source: mod_g_rst_n

14.2.1.1.1.2.273 MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL Register

14.2.1.1.1.2.273.1 MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL Register (Offset = 8580h) [reset = 0h]

Controls Main R5 Subsystem 0 clocking

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Table 14-4680. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8580h

Figure 14-2328. MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS0_CLKSEL_CORE_CLK_SEL
NONE							R/W
0h							0h

Table 14-4681. MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CLKSEL_CORE_CLK_SEL	R/W	0h	Selects R5SS core and interface clock rate Field values (others are reserved): 1'b0 - MAIN_PLL14_HSDIV_CLKOUT 1'b1 - MAIN_PLL14_HSDIV_CLKOUT / 2 (half speed) Reset Source: mod_g_rst_n

14.2.1.1.1.2.274 MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL Register

14.2.1.1.1.2.274.1 MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL Register (Offset = 8584h) [reset = 0h]

Controls Main R5 Subsystem 1 clocking

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Table 14-4682. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 8584h

Figure 14-2329. MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS1_CLKSEL_CORE_CLK_SEL
NONE							R/W
0h							0h

Table 14-4683. MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CLKSEL_CORE_CLK_SEL	R/W	0h	Selects R5SS core and interface clock rate Field values (others are reserved): 1'b0 - MAIN_PLL14_HSDIV_CLKOUT 1'b1 - MAIN_PLL14_HSDIV_CLKOUT / 2 (half speed) Reset Source: mod_g_rst_n

14.2.1.1.1.2.275 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register

14.2.1.1.1.2.275.1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

- KICK0 component

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Table 14-4684. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9008h

Figure 14-2330. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0							
R/W							
0h							

Table 14-4685. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.276 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register

14.2.1.1.1.2.276.1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

- KICK1 component

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Table 14-4686. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 900Ch

Figure 14-2331. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK2_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK2_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK2_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK2_KICK1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4687. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.277 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register

14.2.1.1.1.2.277.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register (Offset = 9100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4688. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9100h

Figure 14-2332. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0_READONLY							
R							
0h							

Table 14-4689. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.278 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register

14.2.1.1.1.2.278.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register (Offset = 9104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4690. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9104h

Figure 14-2333. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1_READONLY							
R							
0h							

Table 14-4691. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.279 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register

14.2.1.1.1.2.279.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register (Offset = 9108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4692. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9108h

Figure 14-2334. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R2_READONLY							
R							
0h							

Table 14-4693. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.280 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register

14.2.1.1.1.2.280.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register (Offset = 910Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-4694. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 910Ch

Figure 14-2335. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4695. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.281 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register

14.2.1.1.1.2.281.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register (Offset = 9110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4696. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9110h

Figure 14-2336. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4_READONLY							
R							
0h							

Table 14-4697. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.282 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register

14.2.1.1.1.2.282.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register (Offset = 9114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4698. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9114h

Figure 14-2337. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5_READONLY							
R							
0h							

Table 14-4699. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.283 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register

14.2.1.1.1.2.283.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register (Offset = 9118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4700. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9118h

Figure 14-2338. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6_READONLY							
R							
0h							

Table 14-4701. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.284 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register

14.2.1.1.1.2.284.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register (Offset = 911Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-4702. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 911Ch

Figure 14-2339. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P2_R7_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P2_R7_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P2_R7_READONLY							
R							
0h							

Table 14-4703. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.285 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register

14.2.1.1.1.2.285.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register (Offset = 9124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4704. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9124h

Figure 14-2340. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R9_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R9_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R9_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R9_READONLY							
R							
0h							

Table 14-4705. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.286 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register

14.2.1.1.1.2.286.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register (Offset = 9128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4706. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 9128h

Figure 14-2341. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R10_READONLY							
R							
0h							

Table 14-4707. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.287 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register

14.2.1.1.1.2.287.1 MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register (Offset = A000h) [reset = 7h]

This register controls which internal clock is made observable on the OBSCLK0/1 output pins

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Table 14-4708. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A000h

Figure 14-2342. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							OBSCLK0_CTRL_OUT_MUX_SEL_PROXY
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OBSCLK0_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OBSCLK0_CTRL_CLK_DIV_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			OBSCLK0_CTRL_CLK_SEL_PROXY				
NONE			R/W				
0h			7h				

Table 14-4709. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	OBSCLK0_CTRL_OUT_MUX_SEL_PROXY	R/W	0h	OBSCLK pin output mux selection. PLL4_REFCLK is the direct output from either HFOSC0 or HFOSC1. Field values (others are reserved): 1'b0 - Selects the output of the CLK_DIV_OUT clock mux 1'b1 - Select PLL4_REFCLK (clk_sel value must be 5'b11111) Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	OBSCLK0_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load divisor value from clk_div field, when the bit is toggled from 0 to 1. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_por_rst_n
15:8	OBSCLK0_CTRL_CLK_DIV_PROXY	R/W	0h	OBSCLK0 output divider. Sets divider to divide by clkdiv + 1. Divide by 1 to 256 are supported. After Writing to this field, the clk_div_ld field must be toggled. Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved

Table 14-4709. MAIN_CTRL_MMR_CFG0_OBSCLK0_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	OBSCLK0_CTRL_CLK_SEL_PROXY	R/W	7h	OBSCLK0 clock source selection. Selects the source of the clock to be divided by the OBSCLK0 divider. Field values (others are reserved): 5'b00000 - MAIN_PLL0_HSDIV0_CLKOUT 5'b00001 - MAIN_PLL1_HSDIV0_CLKOUT 5'b00010 - MAIN_PLL2_HSDIV0_CLKOUT 5'b00011 - MAIN_PLL4_HSDIV0_CLKOUT 5'b00100 - MAIN_PLL14_HSDIV0_CLKOUT 5'b00101 - CLK_12M_RC 5'b00110 - HFOSC0_CLKOUT_32K 5'b00111 - PLLCTRL_OBSCLK 5'b01000 - HFOSC0_CLKOUT 5'b01001 - CLK_32K_RC 5'b01010 - CPSW0_CPTS_GENF0 5'b01011 - CPSW0_CPTS_GENF1 5'b01100 - MCU_PLL0_HSDIV0_CLKOUT 5'b01101 - MAIN_PLL15_HSDIV0_CLKOUT undefined - undefined undefined - undefined undefined - undefined 5'b10000 - MAIN_SYSCLK0 5'b10001 - DEVICE_CLKOUT_32K undefined - undefined 5'b10011 - C7XV_CLK_DIV4 undefined - undefined undefined - undefined 5'b11111 - OFF (Must Select this option when out_mux_sel is set to PLL4_REFCLK) Reset Source: mod_por_rst_n

14.2.1.1.1.2.288 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register

14.2.1.1.1.2.288.1 MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register (Offset = A010h) [reset = 0h]

Enables and selects clock source of CPSW CLKOUT pin

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Table 14-4710. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A010h

Figure 14-2343. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td></td><td colspan="3">RESERVED</td><td>CLKOUT_CTRL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td></td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-4711. MAIN_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
3:1	RESERVED	NONE	0h	Reserved
0	CLKOUT_CTRL_CLK_SEL_PROXY	R/W	0h	Selects CLKOUT clock source Field values (others are reserved): 1'b0 - MAIN_PLL2_HSDIV1_CLKOUT / 5 1'b1 - MAIN_PLL2_HSDIV1_CLKOUT / 10 Reset Source: mod_g_rst_n

14.2.1.1.1.2.289 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register

14.2.1.1.1.2.289.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register (Offset = A060h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL0

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Table 14-4712. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A060h

Figure 14-2344. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAIN_PLL0_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-4713. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL0_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL0. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL0_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL0 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n

Table 14-4713. MAIN_CTRL_MMR_CFG0_MAIN_PLL0_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.290 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register

14.2.1.1.1.2.290.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register (Offset = A064h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL1

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Table 14-4714. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A064h

Figure 14-2345. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL1_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4715. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL1_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL1. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL1_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL1 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n

Table 14-4715. MAIN_CTRL_MMR_CFG0_MAIN_PLL1_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.291 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register

14.2.1.1.1.2.291.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register (Offset = A068h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL2

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Table 14-4716. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A068h

Figure 14-2346. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL2_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4717. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL2_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL2. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL2_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL2 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n

Table 14-4717. MAIN_CTRL_MMR_CFG0_MAIN_PLL2_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.292 MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL_PROXY Register

14.2.1.1.1.2.292.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL_PROXY Register (Offset = A070h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL4

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Table 14-4718. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A070h

Figure 14-2347. MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL4_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL4_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			MAIN_PLL4_CLKSEL_CLK_SEL_PROXY	RESERVED			
NONE			R/W	NONE			
0h			0h	0h			

Table 14-4719. MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL4_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL4. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved

Table 14-4719. MAIN_CTRL_MMR_CFG0_MAIN_PLL4_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	MAIN_PLL4_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL4 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n
22:5	RESERVED	NONE	0h	Reserved
4	MAIN_PLL4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for MAIN PLL4 1'b0 - Use HFOSC0_CLKOUT 1'b1 - Use HFOSC1_CLKOUT Reset Source: mod_g_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.293 MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Register

14.2.1.1.1.2.293.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Register (Offset = A07Ch) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL7

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Table 14-4720. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A07Ch

Figure 14-2348. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL7_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
MAIN_PLL7_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4721. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL7_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL7. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MAIN_PLL7_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL7 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n

Table 14-4721. MAIN_CTRL_MMR_CFG0_MAIN_PLL7_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.294 MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Register

14.2.1.1.1.2.294.1 MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Register (Offset = A098h) [reset = 800000h]

Controls the clock source for MAIN voltage domain PLL14

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Table 14-4722. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A098h

Figure 14-2349. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MAIN_PLL14_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MAIN_PLL14_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4723. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_PLL14_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL14. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable 1'b1 - Enable Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved

Table 14-4723. MAIN_CTRL_MMR_CFG0_MAIN_PLL14_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	MAIN_PLL14_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MAIN warm reset occurs and will keep MAIN PLL14 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: main_chip1_rst_n
22:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.295 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register

14.2.1.1.1.2.295.1 MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register (Offset = A140h) [reset = 7h]

Selects the CP Switch clock sources

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Table 14-4724. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A140h

Figure 14-2350. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CPSW_CLKSEL_CPTS_CLKSEL_PROXY		
NONE					R/W		
0h					7h		

Table 14-4725. MAIN_CTRL_MMR_CFG0_CPSW_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPSW_CLKSEL_CPTS_CLKSEL_PROXY	R/W	7h	Selects the clock source for the CPSW Ethernet switch Common Platform Time Stamp module Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV5_CLKOUT 3'b001 - MAIN_PLL0_HSDIV6_CLKOUT 3'b010 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 3'b011 - Reserved 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - EXT_REFCLK1 (Pin) 3'b110 - SERDES0_IP1_LN0_TXMCLK undefined - undefined 3'b111 - MAIN_SYSCLK0 Reset Source: mod_por_rst_n

14.2.1.1.1.2.296 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register

14.2.1.1.1.2.296.1 MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register (Offset = A160h) [reset = 0h]

Selects the functional clock source for 8-bit eMMC0

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Table 14-4726. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A160h

Figure 14-2351. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							EMMC0_CLKSEL_EMMCSD_IO_CLKLB_SEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EMMC0_CLKSEL_EMMCSD_REFCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-4727. MAIN_CTRL_MMR_CFG0_EMMC0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	EMMC0_CLKSEL_EMMCSD_IO_CLKLB_SEL_PROXY	R/W	0h	Selects IO Pad Loopback for the MMC Module Field values (others are reserved): 1'b0 - Loopback from Unbonded Pad MMCSD0_CLKLB 1'b1 - Loopback from IO Pin MMCSD0_CLK Reset Source: mod_g_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	EMMC0_CLKSEL_EMMCSD_REFCLK_SEL_PROXY	R/W	0h	Selects the functional clock for the MMC Module Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV5_CLKOUT 1'b1 - MAIN_PLL2_HSDIV2_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.297 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register

14.2.1.1.1.2.297.1 MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register (Offset = A1B0h) [reset = 0h]

Timer0 functional clock selection control

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Table 14-4728. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1B0h

Figure 14-2352. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMER0_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4729. MAIN_CTRL_MMR_CFG0_TIMER0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.298 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register

14.2.1.1.1.2.298.1 MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register (Offset = A1B4h) [reset = 0h]

Timer1 functional clock selection control

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Table 14-4730. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1B4h

Figure 14-2353. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER1_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4731. MAIN_CTRL_MMR_CFG0_TIMER1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.299 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register

14.2.1.1.1.2.299.1 MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register (Offset = A1B8h) [reset = 0h]

Timer2 functional clock selection control

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Table 14-4732. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1B8h

Figure 14-2354. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER2_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4733. MAIN_CTRL_MMR_CFG0_TIMER2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.300 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register

14.2.1.1.1.2.300.1 MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register (Offset = A1BCh) [reset = 0h]

Timer3 functional clock selection control

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Table 14-4734. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1BCh

Figure 14-2355. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER3_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4735. MAIN_CTRL_MMR_CFG0_TIMER3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.301 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register

14.2.1.1.1.2.301.1 MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register (Offset = A1C0h) [reset = 0h]

Timer4 functional clock selection control

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Table 14-4736. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1C0h

Figure 14-2356. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER4_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4737. MAIN_CTRL_MMR_CFG0_TIMER4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.302 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register

14.2.1.1.1.2.302.1 MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register (Offset = A1C4h) [reset = 0h]

Timer5 functional clock selection control

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Table 14-4738. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1C4h

Figure 14-2357. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TIMER5_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4739. MAIN_CTRL_MMR_CFG0_TIMER5_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER5_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.303 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register

14.2.1.1.1.2.303.1 MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register (Offset = A1C8h) [reset = 0h]

Timer6 functional clock selection control

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Table 14-4740. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1C8h

Figure 14-2358. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER6_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4741. MAIN_CTRL_MMR_CFG0_TIMER6_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER6_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.304 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register

14.2.1.1.1.2.304.1 MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register (Offset = A1CCh) [reset = 0h]

Timer7 functional clock selection control

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Table 14-4742. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1CCh

Figure 14-2359. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER7_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4743. MAIN_CTRL_MMR_CFG0_TIMER7_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER7_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.305 MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY Register

14.2.1.1.1.2.305.1 MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY Register (Offset = A1D0h) [reset = 0h]

Timer8 functional clock selection control

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Table 14-4744. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1D0h

Figure 14-2360. MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER8_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4745. MAIN_CTRL_MMR_CFG0_TIMER8_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER8_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.306 MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY Register

14.2.1.1.1.2.306.1 MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY Register (Offset = A1D4h) [reset = 0h]

Timer9 functional clock selection control

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Table 14-4746. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1D4h

Figure 14-2361. MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER9_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4747. MAIN_CTRL_MMR_CFG0_TIMER9_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER9_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.307 MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY Register

14.2.1.1.1.2.307.1 MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY Register (Offset = A1D8h) [reset = 0h]

Timer10 functional clock selection control

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Table 14-4748. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1D8h

Figure 14-2362. MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER10_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4749. MAIN_CTRL_MMR_CFG0_TIMER10_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER10_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.308 MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY Register

14.2.1.1.1.2.308.1 MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY Register (Offset = A1DCh) [reset = 0h]

Timer11 functional clock selection control

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Table 14-4750. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1DCh

Figure 14-2363. MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER11_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4751. MAIN_CTRL_MMR_CFG0_TIMER11_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER11_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.309 MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL_PROXY Register

14.2.1.1.1.2.309.1 MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL_PROXY Register (Offset = A1E0h) [reset = 0h]

Timer12 functional clock selection control

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Table 14-4752. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1E0h

Figure 14-2364. MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER12_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4753. MAIN_CTRL_MMR_CFG0_TIMER12_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER12_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.310 MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL_PROXY Register

14.2.1.1.1.2.310.1 MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL_PROXY Register (Offset = A1E4h) [reset = 0h]

Timer13 functional clock selection control

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Table 14-4754. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1E4h

Figure 14-2365. MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER13_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4755. MAIN_CTRL_MMR_CFG0_TIMER13_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER13_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.311 MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL_PROXY Register

14.2.1.1.1.2.311.1 MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL_PROXY Register (Offset = A1E8h) [reset = 0h]

Timer14 functional clock selection control

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Table 14-4756. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1E8h

Figure 14-2366. MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TIMER14_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4757. MAIN_CTRL_MMR_CFG0_TIMER14_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER14_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.312 MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL_PROXY Register

14.2.1.1.1.2.312.1 MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL_PROXY Register (Offset = A1ECh) [reset = 0h]

Timer15 functional clock selection control

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Table 14-4758. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A1ECh

Figure 14-2367. MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMER15_CLKSEL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4759. MAIN_CTRL_MMR_CFG0_TIMER15_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TIMER15_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select control. Field values (others are reserved): 4'b0000 - HFOSC0_CLKOUT 4'b0001 - DEVICE_CLKOUT_32K 4'b0010 - MAIN_PLL0_HSDIV7_CLKOUT 4'b0011 - CLK_12M_RC 4'b0100 - MCU_EXT_REFCLK0 (Pin) 4'b0101 - EXT_REFCLK1 (Pin) 4'b0110 - Reserved 4'b0111 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 4'b1000 - MAIN_PLL1_HSDIV3_CLKOUT 4'b1001 - MAIN_PLL2_HSDIV6_CLKOUT 4'b1010 - CPSW0_CPTS_GENF0 4'b1011 - CPSW0_CPTS_GENF1 4'b1100 - Reserved Reset Source: sys_por_rst_n

14.2.1.1.1.2.313 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register

14.2.1.1.1.2.313.1 MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register (Offset = A200h) [reset = 0h]

SPI0 clock control

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Table 14-4760. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A200h

Figure 14-2368. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4761. MAIN_CTRL_MMR_CFG0_SPI0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI0_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.314 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register

14.2.1.1.1.2.314.1 MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register (Offset = A204h) [reset = 0h]

SPI1 clock control

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Table 14-4762. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A204h

Figure 14-2369. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4763. MAIN_CTRL_MMR_CFG0_SPI1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI1_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.315 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register

14.2.1.1.1.2.315.1 MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register (Offset = A208h) [reset = 0h]

SPI2 clock control

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Table 14-4764. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A208h

Figure 14-2370. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							SPI2_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-4765. MAIN_CTRL_MMR_CFG0_SPI2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI2_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.316 MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY Register

14.2.1.1.1.2.316.1 MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY Register (Offset = A20Ch) [reset = 0h]

SPI3 clock control

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Table 14-4766. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A20Ch

Figure 14-2371. MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI3_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4767. MAIN_CTRL_MMR_CFG0_SPI3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI3_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.317 MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY Register

14.2.1.1.1.2.317.1 MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY Register (Offset = A210h) [reset = 0h]

SPI4 clock control

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Table 14-4768. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A210h

Figure 14-2372. MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							SPI4_CLKSEL_MSTR_LB_CLKSEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4769. MAIN_CTRL_MMR_CFG0_SPI4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	SPI4_CLKSEL_MSTR_LB_CLKSEL_PROXY	R/W	0h	Controller mode receive capture clock loopback selection Field values (others are reserved): 1'b0 - INTERNAL_LOOPBACK 1'b1 - EXTERNAL_LOOPBACK Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.318 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register

14.2.1.1.1.2.318.1 MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register (Offset = A240h) [reset = 3h]

Selects the clock divider of the USART0 functional clock

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Table 14-4770. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A240h

Figure 14-2373. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART0_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART0_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-4771. MAIN_CTRL_MMR_CFG0_USART0_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART0_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART0 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART0_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.319 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register

14.2.1.1.1.2.319.1 MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register (Offset = A244h) [reset = 3h]

Selects the clock divider of the USART1 functional clock

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Table 14-4772. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A244h

Figure 14-2374. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART1_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART1_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-4773. MAIN_CTRL_MMR_CFG0_USART1_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART1_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART1 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART1_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.320 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register

14.2.1.1.1.2.320.1 MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register (Offset = A248h) [reset = 3h]

Selects the clock divider of the USART2 functional clock

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Table 14-4774. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A248h

Figure 14-2375. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>USART2_CLK_CTRL_CLK_DIV_LD_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USART2_CLK_CTRL_CLK_DIV_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">3h</td></tr>
</table>

Table 14-4775. MAIN_CTRL_MMR_CFG0_USART2_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART2_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART2 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART2_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.321 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register

14.2.1.1.1.2.321.1 MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register (Offset = A24Ch) [reset = 3h]

Selects the clock divider of the USART3 functional clock

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Table 14-4776. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A24Ch

Figure 14-2376. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART3_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART3_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-4777. MAIN_CTRL_MMR_CFG0_USART3_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART3_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART3 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART3_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.322 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register

14.2.1.1.1.2.322.1 MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register (Offset = A250h) [reset = 3h]

Selects the clock divider of the USART4 functional clock

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Table 14-4778. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A250h

Figure 14-2377. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							USART4_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USART4_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-4779. MAIN_CTRL_MMR_CFG0_USART4_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART4_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART4 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART4_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.323 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register

14.2.1.1.1.2.323.1 MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register (Offset = A254h) [reset = 3h]

Selects the clock divider of the USART5 functional clock

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Table 14-4780. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A254h

Figure 14-2378. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							USART5_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						USART5_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-4781. MAIN_CTRL_MMR_CFG0_USART5_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART5_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART5 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART5_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.324 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register

14.2.1.1.1.2.324.1 MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register (Offset = A258h) [reset = 3h]

Selects the clock divider of the USART6 functional clock

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Table 14-4782. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A258h

Figure 14-2379. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							USART6_CLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						USART6_CLK_CTRL_CLK_DIV_PROXY	
NONE						R/W	
0h						3h	

Table 14-4783. MAIN_CTRL_MMR_CFG0_USART6_CLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	USART6_CLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART6 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
15:2	RESERVED	NONE	0h	Reserved
1:0	USART6_CLK_CTRL_CLK_DIV_PROXY	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Field values (others are reserved): 2'b00 - Divide by 1 2'b01 - Divide by 2 2'b10 - Divide by 3 2'b11 - Divide by 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.325 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register

14.2.1.1.1.2.325.1 MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register (Offset = A280h) [reset = 0h]

Selects the clock source for USART0 functional clock

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Table 14-4784. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A280h

Figure 14-2380. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART0_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-4785. MAIN_CTRL_MMR_CFG0_USART0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART0: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART0_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.326 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register

14.2.1.1.1.2.326.1 MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register (Offset = A284h) [reset = 0h]

Selects the clock source for USART1 functional clock

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Table 14-4786. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A284h

Figure 14-2381. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART1_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-4787. MAIN_CTRL_MMR_CFG0_USART1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART1: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART1_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.327 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register

14.2.1.1.1.2.327.1 MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register (Offset = A288h) [reset = 0h]

Selects the clock source for USART2 functional clock

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Table 14-4788. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A288h

Figure 14-2382. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							USART2_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-4789. MAIN_CTRL_MMR_CFG0_USART2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART2: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART2_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.328 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register

14.2.1.1.1.2.328.1 MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register (Offset = A28Ch) [reset = 0h]

Selects the clock source for USART3 functional clock

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Table 14-4790. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A28Ch

Figure 14-2383. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							USART3_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-4791. MAIN_CTRL_MMR_CFG0_USART3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART3: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART3_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.329 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register

14.2.1.1.1.2.329.1 MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register (Offset = A290h) [reset = 0h]

Selects the clock source for USART4 functional clock

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Table 14-4792. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A290h

Figure 14-2384. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							USART4_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-4793. MAIN_CTRL_MMR_CFG0_USART4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART4: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART4_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.330 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register

14.2.1.1.1.2.330.1 MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register (Offset = A294h) [reset = 0h]

Selects the clock source for USART5 functional clock

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Table 14-4794. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A294h

Figure 14-2385. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART5_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-4795. MAIN_CTRL_MMR_CFG0_USART5_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART5_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART5: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART5_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.331 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register

14.2.1.1.1.2.331.1 MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register (Offset = A298h) [reset = 0h]

Selects the clock source for USART6 functional clock

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Table 14-4796. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A298h

Figure 14-2386. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USART6_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-4797. MAIN_CTRL_MMR_CFG0_USART6_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USART6_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the clock source for UART6: Field values (others are reserved): 1'b0 - MAIN_PLL1_HSDIV0_CLKOUT Divider Output (See USART6_CLK_CTRL) 1'b1 - MAIN_PLL1_HSDIV1_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.332 MAIN_CTRL_MMR_CFG0_ATL_CLKSEL_PROXY Register

14.2.1.1.1.2.332.1 MAIN_CTRL_MMR_CFG0_ATL_CLKSEL_PROXY Register (Offset = A2B0h) [reset = 0h]

Selects the source of ATL PCLK which drives ATL Measurement and Adjustment Logic

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Table 14-4798. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2B0h

Figure 14-2387. MAIN_CTRL_MMR_CFG0_ATL_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ATL_CLKSEL_PCLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4799. MAIN_CTRL_MMR_CFG0_ATL_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ATL_CLKSEL_PCLK_SEL_PROXY	R/W	0h	Selects the PCLK clock source Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b010 - MAIN_PLL2_HSDIV0_CLKOUT 3'b011 - MAIN_PLL4_HSDIV1_CLKOUT 3'b100 - MAIN_PLL0_HSDIV7_CLKOUT 3'b101 - MCU_EXT_REFCLK0 (Pin) 3'b110 - EXT_REFCLK1 (Pin) Reset Source: mod_g_rst_n

14.2.1.1.1.2.333 MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL_PROXY Register

14.2.1.1.1.2.333.1 MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL_PROXY Register (Offset = A2C0h) [reset = 0h]

Selects the word clock for the ATL channel0 Baseband Stream

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Table 14-4800. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2C0h

Figure 14-2388. MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_BWS0_SEL_WD_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4801. MAIN_CTRL_MMR_CFG0_ATL_BWS0_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_BWS0_SEL_WD_SEL_PROXY	R/W	0h	BWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSR_IN 4'b0001 - MCASP1_AFSR_IN 4'b0010 - MCASP2_AFSR_IN 4'b0011 - MCASP3_AFSR_IN 4'b0100 - MCASP4_AFSR_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.334 MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL_PROXY Register

14.2.1.1.1.2.334.1 MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL_PROXY Register (Offset = A2C4h) [reset = 0h]

Selects the word clock for the ATL channel1 Baseband Stream

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Table 14-4802. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2C4h

Figure 14-2389. MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_BWS1_SEL_WD_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4803. MAIN_CTRL_MMR_CFG0_ATL_BWS1_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_BWS1_SEL_WD_SEL_PROXY	R/W	0h	BWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSR_IN 4'b0001 - MCASP1_AFSR_IN 4'b0010 - MCASP2_AFSR_IN 4'b0011 - MCASP3_AFSR_IN 4'b0100 - MCASP4_AFSR_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.335 MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL_PROXY Register

14.2.1.1.1.2.335.1 MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL_PROXY Register (Offset = A2C8h) [reset = 0h]

Selects the word clock for the ATL channel2 Baseband Stream

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Table 14-4804. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2C8h

Figure 14-2390. MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_BWS2_SEL_WD_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4805. MAIN_CTRL_MMR_CFG0_ATL_BWS2_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_BWS2_SEL_WD_SEL_PROXY	R/W	0h	BWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSR_IN 4'b0001 - MCASP1_AFSR_IN 4'b0010 - MCASP2_AFSR_IN 4'b0011 - MCASP3_AFSR_IN 4'b0100 - MCASP4_AFSR_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.336 MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL_PROXY Register

14.2.1.1.1.2.336.1 MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL_PROXY Register (Offset = A2CCh) [reset = 0h]

Selects the word clock for the ATL channel3 Baseband Stream

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Table 14-4806. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2CCh

Figure 14-2391. MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_BWS3_SEL_WD_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4807. MAIN_CTRL_MMR_CFG0_ATL_BWS3_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_BWS3_SEL_WD_SEL_PROXY	R/W	0h	BWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSR_IN 4'b0001 - MCASP1_AFSR_IN 4'b0010 - MCASP2_AFSR_IN 4'b0011 - MCASP3_AFSR_IN 4'b0100 - MCASP4_AFSR_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.337 MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL_PROXY Register

14.2.1.1.1.2.337.1 MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL_PROXY Register (Offset = A2D0h) [reset = 0h]

Selects the word clock for the ATL channel0 Audio Stream

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Table 14-4808. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2D0h

Figure 14-2392. MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_AWS0_SEL_WD_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4809. MAIN_CTRL_MMR_CFG0_ATL_AWS0_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_AWS0_SEL_WD_SEL_PROXY	R/W	0h	AWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSX_IN 4'b0001 - MCASP1_AFSX_IN 4'b0010 - MCASP2_AFSX_IN 4'b0011 - MCASP3_AFSX_IN 4'b0100 - MCASP4_AFSX_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.338 MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL_PROXY Register

14.2.1.1.1.2.338.1 MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL_PROXY Register (Offset = A2D4h) [reset = 0h]

Selects the word clock for the ATL channel1 Audio Stream

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Table 14-4810. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2D4h

Figure 14-2393. MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ATL_AWS1_SEL_WD_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-4811. MAIN_CTRL_MMR_CFG0_ATL_AWS1_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_AWS1_SEL_WD_SEL_PROXY	R/W	0h	AWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSX_IN 4'b0001 - MCASP1_AFSX_IN 4'b0010 - MCASP2_AFSX_IN 4'b0011 - MCASP3_AFSX_IN 4'b0100 - MCASP4_AFSX_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.339 MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL_PROXY Register

14.2.1.1.1.2.339.1 MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL_PROXY Register (Offset = A2D8h) [reset = 0h]

Selects the word clock for the ATL channel2 Audio Stream

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Table 14-4812. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2D8h

Figure 14-2394. MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ATL_AWS2_SEL_WD_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4813. MAIN_CTRL_MMR_CFG0_ATL_AWS2_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_AWS2_SEL_WD_SEL_PROXY	R/W	0h	AWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSX_IN 4'b0001 - MCASP1_AFSX_IN 4'b0010 - MCASP2_AFSX_IN 4'b0011 - MCASP3_AFSX_IN 4'b0100 - MCASP4_AFSX_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.340 MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL_PROXY Register

14.2.1.1.1.2.340.1 MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL_PROXY Register (Offset = A2DCh) [reset = 0h]

Selects the word clock for the ATL channel3 Audio Stream

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Table 14-4814. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2DCh

Figure 14-2395. MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATL_AWS3_SEL_WD_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4815. MAIN_CTRL_MMR_CFG0_ATL_AWS3_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ATL_AWS3_SEL_WD_SEL_PROXY	R/W	0h	AWS source signal Field values (others are reserved): 4'b0000 - MCASP0_AFSX_IN 4'b0001 - MCASP1_AFSX_IN 4'b0010 - MCASP2_AFSX_IN 4'b0011 - MCASP3_AFSX_IN 4'b0100 - MCASP4_AFSX_IN 4'b0101 - MCASP0_AFSX_IN 4'b0110 - MCASP1_AFSX_IN 4'b0111 - MCASP2_AFSX_IN 4'b1000 - MCASP3_AFSX_IN 4'b1001 - MCASP4_AFSX_IN 4'b1010 - AUDIO_EXT_REFCLK0_IN 4'b1011 - AUDIO_EXT_REFCLK1_IN 4'b1100 - AUDIO_EXT_REFCLK2_IN Reset Source: mod_g_rst_n

14.2.1.1.1.2.341 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Register

14.2.1.1.1.2.341.1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Register (Offset = A2E0h) [reset = Fh]

Selects the clock source for the AUDIO_EXT_REFCLK0 output, and direction.

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Table 14-4816. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2E0h

Figure 14-2396. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
AUDIO_REFCLK0_CTRL_CLKOUT_EN_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED				AUDIO_REFCLK0_CTRL_CLK_SEL_PROXY			
NONE				R/W			
0h				Fh			

Table 14-4817. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK0_CTRL_CLKOUT_EN_PROXY	R/W	0h	AUDIO_REFCLK 0 output enable Field values (others are reserved): 1'b0 - INPUT 1'b1 - OUTPUT Reset Source: mod_g_rst_n
14:4	RESERVED	NONE	0h	Reserved

Table 14-4817. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK0_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	AUDIO_REFCLK0_CTRL_CLK_SEL_PROXY	R/W	Fh	Selects the source of AUDIO_REFCLK0 Field values (others are reserved): 4'b0000 - MCASP0_AHCLKR 4'b0001 - MCASP1_AHCLKR 4'b0010 - MCASP2_AHCLKR 4'b0011 - MCASP3_AHCLKR 4'b0100 - MCASP4_AHCLKR 4'b0101 - MCASP0_AHCLKX 4'b0110 - MCASP1_AHCLKX 4'b0111 - MCASP2_AHCLKX 4'b1000 - MCASP3_AHCLKX 4'b1001 - MCASP4_AHCLKX 4'b1010 - ATCLK0 4'b1011 - ATCLK1 4'b1100 - ATCLK2 4'b1101 - ATCLK3 4'b1110 - MAIN_PLL1_HSDIV6_CLKOUT undefined - undefined 4'b1111 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.342 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Register

14.2.1.1.1.2.342.1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Register (Offset = A2E4h) [reset = Fh]

Selects the clock source for the AUDIO_EXT_REFCLK0 output, and direction.

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Table 14-4818. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2E4h

Figure 14-2397. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AUDIO_REFCLK1_CTRL_CLKOUT_EN_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				AUDIO_REFCLK1_CTRL_CLK_SEL_PROXY			
NONE				R/W			
0h				Fh			

Table 14-4819. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK1_CTRL_CLKOUT_EN_PROXY	R/W	0h	AUDIO_REFCLK 1 output enable Field values (others are reserved): 1'b0 - INPUT 1'b1 - OUTPUT Reset Source: mod_g_rst_n
14:4	RESERVED	NONE	0h	Reserved

Table 14-4819. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK1_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	AUDIO_REFCLK1_CTRL_CLK_SEL_PROXY	R/W	Fh	Selects the source of AUDIO_REFCLK1 Field values (others are reserved): 4'b0000 - MCASP0_AHCLKR 4'b0001 - MCASP1_AHCLKR 4'b0010 - MCASP2_AHCLKR 4'b0011 - MCASP3_AHCLKR 4'b0100 - MCASP4_AHCLKR 4'b0101 - MCASP0_AHCLKX 4'b0110 - MCASP1_AHCLKX 4'b0111 - MCASP2_AHCLKX 4'b1000 - MCASP3_AHCLKX 4'b1001 - MCASP4_AHCLKX 4'b1010 - ATCLK0 4'b1011 - ATCLK1 4'b1100 - ATCLK2 4'b1101 - ATCLK3 4'b1110 - MAIN_PLL1_HSDIV6_CLKOUT undefined - undefined 4'b1111 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.343 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL_PROXY Register

14.2.1.1.1.2.343.1 MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL_PROXY Register (Offset = A2E8h) [reset = Fh]

Selects the clock source for the AUDIO_EXT_REFCLK0 output, and direction.

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Table 14-4820. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2E8h

Figure 14-2398. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>AUDIO_REFCLK2_CTRL_CLKOUT_EN_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">AUDIO_REFCLK2_CTRL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-4821. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	AUDIO_REFCLK2_CTRL_CLKOUT_EN_PROXY	R/W	0h	AUDIO_REFCLK 2 output enable Field values (others are reserved): 1'b0 - INPUT 1'b1 - OUTPUT Reset Source: mod_g_rst_n
14:4	RESERVED	NONE	0h	Reserved

Table 14-4821. MAIN_CTRL_MMR_CFG0_AUDIO_REFCLK2_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	AUDIO_REFCLK2_CTRL_CLK_SEL_PROXY	R/W	Fh	Selects the source of AUDIO_REFCLK2 Field values (others are reserved): 4'b0000 - MCASP0_AHCLKR 4'b0001 - MCASP1_AHCLKR 4'b0010 - MCASP2_AHCLKR 4'b0011 - MCASP3_AHCLKR 4'b0100 - MCASP4_AHCLKR 4'b0101 - MCASP0_AHCLKX 4'b0110 - MCASP1_AHCLKX 4'b0111 - MCASP2_AHCLKX 4'b1000 - MCASP3_AHCLKX 4'b1001 - MCASP4_AHCLKX 4'b1010 - ATCLK0 4'b1011 - ATCLK1 4'b1100 - ATCLK2 4'b1101 - ATCLK3 4'b1110 - MAIN_PLL1_HSDIV6_CLKOUT undefined - undefined 4'b1111 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.344 MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL_PROXY Register

14.2.1.1.1.2.344.1 MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL_PROXY Register (Offset = A2F0h) [reset = 0h]

Selects additional divide value for the MAIN_PLL4 clock source to the ASRC RXSYNC and TXSYNC selection muxes

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Table 14-4822. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A2F0h

Figure 14-2399. MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ASRC_SYNC_DIV_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ASRC_SYNC_DIV_CTRL_CLK_DIV_PROXY			
NONE				R/W			
0h				0h			

Table 14-4823. MAIN_CTRL_MMR_CFG0_ASRC_SYNC_DIV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	ASRC_SYNC_DIV_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the divider value Writing 1 to this bit will generate a load pulse to load the clk_div divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	ASRC_SYNC_DIV_CTRL_CLK_DIV_PROXY	R/W	0h	ASRC Sync divider value Divides MAIN_PLL4_HSDIV_CLKOUT3 by clkdiv+1. Supports divide by 1 to 16 (default to 1). To load the new divider value the clk_div_ld bit must be cleared and then set to 1. Reset Source: mod_g_rst_n

14.2.1.1.1.2.345 MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY Register

14.2.1.1.1.2.345.1 MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY Register (Offset = A330h) [reset = 0h]

Selects the functional clock source for McASP0

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Table 14-4824. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A330h

Figure 14-2400. MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						MCASP0_CLKSEL_LOC_AUXCLK_SEL_PROXY	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MCASP0_CLKSEL_AUXCLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4825. MAIN_CTRL_MMR_CFG0_MCASP0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP0_CLKSEL_LOC_AUXCLK_SEL_PROXY	R/W	0h	Selects the local clock source to use for McASP0 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP0_CLKSEL_AUXCLK_SEL_PROXY	R/W	0h	Selects the system AUXCLK input source for McASP0 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.346 MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY Register

14.2.1.1.1.2.346.1 MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY Register (Offset = A334h) [reset = 0h]

Selects the functional clock source for McASP1

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Table 14-4826. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A334h

Figure 14-2401. MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MCASP1_CLKSEL_LOC_AUXCLK_SEL_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MCASP1_CLKSEL_AUXCLK_SEL_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4827. MAIN_CTRL_MMR_CFG0_MCASP1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP1_CLKSEL_LOC_AUXCLK_SEL_PROXY	R/W	0h	Selects the local clock source to use for McASP1 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP1_CLKSEL_AUXCLK_SEL_PROXY	R/W	0h	Selects the system AUXCLK input source for McASP1 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.347 MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY Register

14.2.1.1.1.2.347.1 MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY Register (Offset = A338h) [reset = 0h]

Selects the functional clock source for McASP2

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Table 14-4828. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A338h

Figure 14-2402. MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP2_CLKSEL_LOC_AUXCLK_SEL_PROXY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED					MCASP2_CLKSEL_AUXCLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4829. MAIN_CTRL_MMR_CFG0_MCASP2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP2_CLKSEL_LOC_AUXCLK_SEL_PROXY	R/W	0h	Selects the local clock source to use for McASP2 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP2_CLKSEL_AUXCLK_SEL_PROXY	R/W	0h	Selects the system AUXCLK input source for McASP2 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.348 MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL_PROXY Register

14.2.1.1.1.2.348.1 MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL_PROXY Register (Offset = A33Ch) [reset = 0h]

Selects the functional clock source for McASP3

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Table 14-4830. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A33Ch

Figure 14-2403. MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						MCASP3_CLKSEL_LOC_AUXCLK_SEL_PROXY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED					MCASP3_CLKSEL_AUXCLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-4831. MAIN_CTRL_MMR_CFG0_MCASP3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP3_CLKSEL_LOC_AUXCLK_SEL_PROXY	R/W	0h	Selects the local clock source to use for McASP3 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP3_CLKSEL_AUXCLK_SEL_PROXY	R/W	0h	Selects the system AUXCLK input source for McASP3 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.349 MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL_PROXY Register

14.2.1.1.1.2.349.1 MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL_PROXY Register (Offset = A340h) [reset = 0h]

Selects the functional clock source for McASP4

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Table 14-4832. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A340h

Figure 14-2404. MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MCASP4_CLKSEL_LOC_AUXCLK_SEL_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MCASP4_CLKSEL_AUXCLK_SEL_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-4833. MAIN_CTRL_MMR_CFG0_MCASP4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	MCASP4_CLKSEL_LOC_AUXCLK_SEL_PROXY	R/W	0h	Selects the local clock source to use for McASP4 AUXCLK Field values (others are reserved): 2'b00 - PLL4_REF_CLK (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b01 - PLL4_REF_CLK / 2 (as selected by MAIN_PLL4_CLKSEL_clk_sel) 2'b10 - MAIN_PLL4_HSDIV0_CLKOUT Reset Source: mod_g_rst_n
7:3	RESERVED	NONE	0h	Reserved
2:0	MCASP4_CLKSEL_AUXCLK_SEL_PROXY	R/W	0h	Selects the system AUXCLK input source for McASP4 Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV8_CLKOUT 3'b001 - MAIN_PLL1_HSDIV6_CLKOUT 3'b011 - AUDIO_EXT_REFCLK0 (Pin) 3'b100 - AUDIO_EXT_REFCLK1 (Pin) 3'b101 - AUDIO_EXT_REFCLK2 (Pin) 3'b110 - ATCLK0 3'b111 - ATCLK1 Reset Source: mod_g_rst_n

14.2.1.1.1.2.350 MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Register

14.2.1.1.1.2.350.1 MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Register (Offset = A350h) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP0

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Table 14-4834. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A350h

Figure 14-2405. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCASP0_AHCLKSEL_AHCLKX_SEL_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCASP0_AHCLKSEL_AHCLKR_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4835. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP0_AHCLKSEL_AHCLKX_SEL_PROXY	R/W	0h	Selects the AHCLKX input source for McASP0 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4835. MAIN_CTRL_MMR_CFG0_MCASP0_AHCLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP0_AHCLKSEL_AHCLKR_SEL_PROXY	R/W	0h	Selects the AHCLKR input source for McASP0 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.351 MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Register

14.2.1.1.1.2.351.1 MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Register (Offset = A354h) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP1

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Table 14-4836. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A354h

Figure 14-2406. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCASP1_AHCLKSEL_AHCLKX_SEL_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCASP1_AHCLKSEL_AHCLKR_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4837. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP1_AHCLKSEL_AHCLKX_SEL_PROXY	R/W	0h	Selects the AHCLKX input source for McASP1 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4837. MAIN_CTRL_MMR_CFG0_MCASP1_AHCLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP1_AHCLKSEL_AHCLKR_SEL_PROXY	R/W	0h	Selects the AHCLKR input source for McASP1 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.352 MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Register

14.2.1.1.1.2.352.1 MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Register (Offset = A358h) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP2

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Table 14-4838. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A358h

Figure 14-2407. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCASP2_AHCLKSEL_AHCLKX_SEL_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCASP2_AHCLKSEL_AHCLKR_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4839. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP2_AHCLKSEL_AHCLKX_SEL_PROXY	R/W	0h	Selects the AHCLKX input source for McASP2 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4839. MAIN_CTRL_MMR_CFG0_MCASP2_AHCLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP2_AHCLKSEL_AHCLKR_SEL_PROXY	R/W	0h	Selects the AHCLKR input source for McASP2 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.353 MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL_PROXY Register

14.2.1.1.1.2.353.1 MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL_PROXY Register (Offset = A35Ch) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP3

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Table 14-4840. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A35Ch

Figure 14-2408. MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCASP3_AHCLKSEL_AHCLKX_SEL_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCASP3_AHCLKSEL_AHCLKR_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4841. MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP3_AHCLKSEL_AHCLKX_SEL_PROXY	R/W	0h	Selects the AHCLKX input source for McASP3 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4841. MAIN_CTRL_MMR_CFG0_MCASP3_AHCLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP3_AHCLKSEL_AHCLKR_SEL_PROXY	R/W	0h	Selects the AHCLKR input source for McASP3 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.354 MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL_PROXY Register

14.2.1.1.1.2.354.1 MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL_PROXY Register (Offset = A360h) [reset = 0h]

Selects the AHCLKX and AHCLKR clock source for McASP4

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Table 14-4842. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A360h

Figure 14-2409. MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCASP4_AHCLKSEL_AHCLKX_SEL_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCASP4_AHCLKSEL_AHCLKR_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-4843. MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	MCASP4_AHCLKSEL_AHCLKX_SEL_PROXY	R/W	0h	Selects the AHCLKX input source for McASP4 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-4843. MAIN_CTRL_MMR_CFG0_MCASP4_AHCLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCASP4_AHCLKSEL_AHCLKR_SEL_PROXY	R/W	0h	Selects the AHCLKR input source for McASP4 Field values (others are reserved): 4'b0000 - EXT_REFCLK1 (Pin) 4'b0001 - HFOSC0_CLKOUT 4'b0010 - AUDIO_EXT_REFCLK0 (Pin) 4'b0011 - AUDIO_EXT_REFCLK1 (Pin) 4'b0100 - AUDIO_EXT_REFCLK2 (Pin) undefined - undefined 4'b0110 - MLB_IO_CLK undefined - undefined 4'b1000 - ATCLK0 4'b1001 - ATCLK1 4'b1010 - ATCLK2 4'b1011 - ATCLK3 4'b1100 - CPSW CPTS GENF0 4'b1101 - CPSW CPTS GENF0 Reset Source: mod_g_rst_n

14.2.1.1.1.2.355 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register

14.2.1.1.1.2.355.1 MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register (Offset = A380h) [reset = 0h]

Windowed Watchdog WWD0 functional clock selection control

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Table 14-4844. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A380h

Figure 14-2410. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD0_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4845. MAIN_CTRL_MMR_CFG0_WWD0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD0_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD0_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.356 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register

14.2.1.1.1.2.356.1 MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register (Offset = A384h) [reset = 0h]

Windowed Watchdog WWD1 functional clock selection control

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Table 14-4846. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A384h

Figure 14-2411. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD1_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD1_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4847. MAIN_CTRL_MMR_CFG0_WWD1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD1_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD1_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.357 MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY Register

14.2.1.1.1.2.357.1 MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY Register (Offset = A388h) [reset = 0h]

Windowed Watchdog WWD2 functional clock selection control

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Table 14-4848. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A388h

Figure 14-2412. MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD2_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD2_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4849. MAIN_CTRL_MMR_CFG0_WWD2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD2_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD2_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD2_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.358 MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY Register

14.2.1.1.1.2.358.1 MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY Register (Offset = A38Ch) [reset = 0h]

Windowed Watchdog WWD3 functional clock selection control

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Table 14-4850. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A38Ch

Figure 14-2413. MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD3_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WWD3_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4851. MAIN_CTRL_MMR_CFG0_WWD3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD3_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD3_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD3_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.359 MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY Register

14.2.1.1.1.2.359.1 MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY Register (Offset = A390h) [reset = 0h]

Windowed Watchdog WWD4 functional clock selection control

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Table 14-4852. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A390h

Figure 14-2414. MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
WWD4_CLKSEL_WRTLOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WWD4_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4853. MAIN_CTRL_MMR_CFG0_WWD4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD4_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD4_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD4_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.360 MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL_PROXY Register

14.2.1.1.1.2.360.1 MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL_PROXY Register (Offset = A394h) [reset = 0h]

Windowed Watchdog WWD5 functional clock selection control

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Table 14-4854. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A394h

Figure 14-2415. MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>WWD5_CLKSEL_WRTLOCK_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">WWD5_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-4855. MAIN_CTRL_MMR_CFG0_WWD5_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WWD5_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WWD5_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WWD5_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.1.2.361 MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL_PROXY Register

14.2.1.1.1.2.361.1 MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL_PROXY Register (Offset = A3E0h) [reset = 0h]

Performs glitchfree selection of the McASP0 functional clock

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Table 14-4856. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A3E0h

Figure 14-2416. MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MCASP0_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-4857. MAIN_CTRL_MMR_CFG0_MCASP0_GF_CLK_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP0_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP0 based on MCASP0_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.362 MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL_PROXY Register

14.2.1.1.1.2.362.1 MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL_PROXY Register (Offset = A3E4h) [reset = 0h]

Performs glitchfree selection of the McASP1 functional clock

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Table 14-4858. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A3E4h

Figure 14-2417. MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCASP1_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4859. MAIN_CTRL_MMR_CFG0_MCASP1_GF_CLK_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP1_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP1 based on MCASP1_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.363 MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL_PROXY Register

14.2.1.1.1.2.363.1 MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL_PROXY Register (Offset = A3E8h) [reset = 0h]

Performs glitchfree selection of the McASP2 functional clock

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Table 14-4860. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A3E8h

Figure 14-2418. MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>MCASP2_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4861. MAIN_CTRL_MMR_CFG0_MCASP2_GF_CLK_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP2_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP2 based on MCASP2_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.364 MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL_PROXY Register

14.2.1.1.1.2.364.1 MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL_PROXY Register (Offset = A3ECh) [reset = 0h]

Performs glitchfree selection of the McASP3 functional clock

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Table 14-4862. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A3ECh

Figure 14-2419. MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCASP3_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4863. MAIN_CTRL_MMR_CFG0_MCASP3_GF_CLK_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP3_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP3 based on MCASP3_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.365 MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL_PROXY Register

14.2.1.1.1.2.365.1 MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL_PROXY Register (Offset = A3F0h) [reset = 0h]

Performs glitchfree selection of the McASP4 functional clock

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Table 14-4864. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A3F0h

Figure 14-2420. MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCASP4_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-4865. MAIN_CTRL_MMR_CFG0_MCASP4_GF_CLK_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	MCASP4_GF_CLK_SEL_AUXCLK_GF_SEL_PROXY	R/W	0h	Provides glitch-free switching between the local and system AUXCLK source for McASP4 based on MCASP4_CLKSEL loc_auxclk_sel and auxclk_sel settings. Field values (others are reserved): 1'b0 - Use local AUXCLK source (as selected by loc_auxclk_sel bitfield) 1'b1 - Use system AUXCLK source (as selected by auxsel_sel bitfield) Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.1.2.366 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register

14.2.1.1.1.2.366.1 MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register (Offset = A480h) [reset = 0h]

Controls the functional clock source for MCAN0

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Table 14-4866. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A480h

Figure 14-2421. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4867. MAIN_CTRL_MMR_CFG0_MCAN0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN0_CLKSEL_CLK_SEL_PROXY	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.367 MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY Register

14.2.1.1.1.2.367.1 MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY Register (Offset = A484h) [reset = 0h]

Controls the functional clock source for MCAN1

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Table 14-4868. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A484h

Figure 14-2422. MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN1_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4869. MAIN_CTRL_MMR_CFG0_MCAN1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN1_CLKSEL_CLK_SEL_PROXY	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.368 MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL_PROXY Register

14.2.1.1.1.2.368.1 MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL_PROXY Register (Offset = A488h) [reset = 0h]

Controls the functional clock source for MCAN2

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Table 14-4870. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A488h

Figure 14-2423. MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MCAN2_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-4871. MAIN_CTRL_MMR_CFG0_MCAN2_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN2_CLKSEL_CLK_SEL_PROXY	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.369 MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL_PROXY Register

14.2.1.1.1.2.369.1 MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL_PROXY Register (Offset = A48Ch) [reset = 0h]

Controls the functional clock source for MCAN3

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Table 14-4872. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A48Ch

Figure 14-2424. MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN3_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4873. MAIN_CTRL_MMR_CFG0_MCAN3_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN3_CLKSEL_CLK_SEL_PROXY	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.370 MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL_PROXY Register

14.2.1.1.1.2.370.1 MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL_PROXY Register (Offset = A490h) [reset = 0h]

Controls the functional clock source for MCAN4

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Table 14-4874. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A490h

Figure 14-2425. MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MCAN4_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4875. MAIN_CTRL_MMR_CFG0_MCAN4_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	MCAN4_CLKSEL_CLK_SEL_PROXY	R/W	0h	MCAN functional clock selection Field values (others are reserved): 2'b00 - MAIN_PLL0_HSDIV4_CLKOUT 2'b01 - MCU_EXT_REFCLK0 (Pin) 2'b10 - EXT_REFCLK1 (Pin) 2'b11 - HFOSC0_CLKOUT Reset Source: sys_por_rst_n

14.2.1.1.1.2.371 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL_PROXY Register

14.2.1.1.1.2.371.1 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL_PROXY Register (Offset = A4C0h) [reset = 0h]

Selects the source signal for the ASRC0 RXSYNC0 frame sync input

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Table 14-4876. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4C0h

Figure 14-2426. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ASRC0_RXSYNC0_SEL_SYNC_SEL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-4877. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4877. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC0_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_RXSYNC0_SEL_SYNC_SEL_PROXY	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.372 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL_PROXY Register

14.2.1.1.1.2.372.1 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL_PROXY Register (Offset = A4C4h) [reset = 0h]

Selects the source signal for the ASRC0 RXSYNC1 frame sync input

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Table 14-4878. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4C4h

Figure 14-2427. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ASRC0_RXSYNC1_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4879. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4879. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC1_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_RXSYNC1_SEL_SYNC_SEL_PROXY	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.373 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL_PROXY Register

14.2.1.1.1.2.373.1 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL_PROXY Register (Offset = A4C8h) [reset = 0h]

Selects the source signal for the ASRC0 RXSYNC2 frame sync input

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Table 14-4880. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4C8h

Figure 14-2428. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_RXSYNC2_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4881. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4881. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC2_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_RXSYNC2_SEL_SYNC_SEL_PROXY	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.374 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL_PROXY Register

14.2.1.1.1.2.374.1 MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL_PROXY Register (Offset = A4CCh) [reset = 0h]

Selects the source signal for the ASRC0 RXSYNC3 frame sync input

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Table 14-4882. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4CCh

Figure 14-2429. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ASRC0_RXSYNC3_SEL_SYNC_SEL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-4883. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4883. MAIN_CTRL_MMR_CFG0_ASRC0_RXSYNC3_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_RXSYNC3_SEL_SYNC_SEL_PROXY	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.375 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL_PROXY Register

14.2.1.1.1.2.375.1 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL_PROXY Register (Offset = A4D0h) [reset = 0h]

Selects the source signal for the ASRC1 RXSYNC0 frame sync input

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Table 14-4884. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4D0h

Figure 14-2430. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_RXSYNC0_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4885. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4885. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC0_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_RXSYNC0_SEL_SYNC_SEL_PROXY	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.376 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL_PROXY Register

14.2.1.1.1.2.376.1 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL_PROXY Register (Offset = A4D4h) [reset = 0h]

Selects the source signal for the ASRC1 RXSYNC1 frame sync input

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Table 14-4886. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4D4h

Figure 14-2431. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_RXSYNC1_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4887. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4887. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC1_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_RXSYNC1_SEL_SYNC_SEL_PROXY	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.377 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL_PROXY Register

14.2.1.1.1.2.377.1 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL_PROXY Register (Offset = A4D8h) [reset = 0h]

Selects the source signal for the ASRC1 RXSYNC2 frame sync input

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Table 14-4888. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4D8h

Figure 14-2432. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ASRC1_RXSYNC2_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4889. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4889. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC2_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_RXSYNC2_SEL_SYNC_SEL_PROXY	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.378 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL_PROXY Register

14.2.1.1.1.2.378.1 MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL_PROXY Register (Offset = A4DCh) [reset = 0h]

Selects the source signal for the ASRC1 RXSYNC3 frame sync input

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Table 14-4890. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4DCh

Figure 14-2433. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_RXSYNC3_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4891. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4891. MAIN_CTRL_MMR_CFG0_ASRC1_RXSYNC3_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_RXSYNC3_SEL_SYNC_SEL_PROXY	R/W	0h	RXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSR Pin Input 5'b00001 - McASP1 AFSR Pin Input 5'b00010 - McASP2 AFSR Pin Input 5'b00011 - McASP3 AFSR Pin Input 5'b00100 - McASP4 AFSR Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.379 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL_PROXY Register

14.2.1.1.1.2.379.1 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL_PROXY Register (Offset = A4E0h) [reset = 0h]

Selects the source signal for the ASRC0 TXSYNC0 frame sync input

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Table 14-4892. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4E0h

Figure 14-2434. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ASRC0_TXSYNC0_SEL_SYNC_SEL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-4893. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4893. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC0_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_TXSYNC0_SEL_SYNC_SEL_PROXY	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.380 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL_PROXY Register

14.2.1.1.1.2.380.1 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL_PROXY Register (Offset = A4E4h) [reset = 0h]

Selects the source signal for the ASRC0 TXSYNC1 frame sync input

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Table 14-4894. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4E4h

Figure 14-2435. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_TXSYNC1_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4895. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4895. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC1_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_TXSYNC1_SEL_SYNC_SEL_PROXY	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.381 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL_PROXY Register

14.2.1.1.1.2.381.1 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL_PROXY Register (Offset = A4E8h) [reset = 0h]

Selects the source signal for the ASRC0 TXSYNC2 frame sync input

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Table 14-4896. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4E8h

Figure 14-2436. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ASRC0_TXSYNC2_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4897. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4897. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC2_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_TXSYNC2_SEL_SYNC_SEL_PROXY	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.382 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL_PROXY Register

14.2.1.1.1.2.382.1 MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL_PROXY Register (Offset = A4ECh) [reset = 0h]

Selects the source signal for the ASRC0 TXSYNC3 frame sync input

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Table 14-4898. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4ECh

Figure 14-2437. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC0_TXSYNC3_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4899. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4899. MAIN_CTRL_MMR_CFG0_ASRC0_TXSYNC3_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC0_TXSYNC3_SEL_SYNC_SEL_PROXY	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.383 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL_PROXY Register

14.2.1.1.1.2.383.1 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL_PROXY Register (Offset = A4F0h) [reset = 0h]

Selects the source signal for the ASRC1 TXSYNC0 frame sync input

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Table 14-4900. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4F0h

Figure 14-2438. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_TXSYNC0_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4901. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4901. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC0_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_TXSYNC0_SEL_SYNC_SEL_PROXY	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.384 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL_PROXY Register

14.2.1.1.1.2.384.1 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL_PROXY Register (Offset = A4F4h) [reset = 0h]

Selects the source signal for the ASRC1 TXSYNC1 frame sync input

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Table 14-4902. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4F4h

Figure 14-2439. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">ASRC1_TXSYNC1_SEL_SYNC_SEL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-4903. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4903. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC1_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_TXSYNC1_SEL_SYNC_SEL_PROXY	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.385 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL_PROXY Register

14.2.1.1.1.2.385.1 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL_PROXY Register (Offset = A4F8h) [reset = 0h]

Selects the source signal for the ASRC1 TXSYNC2 frame sync input

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Table 14-4904. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4F8h

Figure 14-2440. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_TXSYNC2_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4905. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4905. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC2_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_TXSYNC2_SEL_SYNC_SEL_PROXY	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.386 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL_PROXY Register

14.2.1.1.1.2.386.1 MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL_PROXY Register (Offset = A4FCh) [reset = 0h]

Selects the source signal for the ASRC1 TXSYNC3 frame sync input

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Table 14-4906. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A4FCh

Figure 14-2441. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			ASRC1_TXSYNC3_SEL_SYNC_SEL_PROXY				
NONE			R/W				
0h			0h				

Table 14-4907. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-4907. MAIN_CTRL_MMR_CFG0_ASRC1_TXSYNC3_SEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ASRC1_TXSYNC3_SEL_SYNC_SEL_PROXY	R/W	0h	TXSYNC source signal Field values (others are reserved): 5'b00000 - McASP0 AFSX Pin Input 5'b00001 - McASP1 AFSX Pin Input 5'b00010 - McASP2 AFSX Pin Input 5'b00011 - McASP3 AFSX Pin Input 5'b00100 - McASP4 AFSX Pin Input 5'b00101 - '0' - Reserved 5'b00110 - '0' - Reserved 5'b00111 - '0' - Reserved 5'b01000 - McASP0 AFSX Pin Input 5'b01001 - McASP1 AFSX Pin Input 5'b01010 - McASP2 AFSX Pin Input 5'b01011 - McASP3 AFSX Pin Input 5'b01100 - McASP4 AFSX Pin Input 5'b01101 - '0' - Reserved 5'b01110 - '0' - Reserved 5'b01111 - '0' - Reserved 5'b10000 - AUDIO_EXT_REFCLK0 Pin input 5'b10001 - AUDIO_EXT_REFCLK1 Pin input 5'b10010 - AUDIO_EXT_REFCLK2 Pin input 5'b10011 - '0' - Reserved 5'b10100 - ADC0_CLK 5'b10101 - MLB_IO_CLK 5'b10110 - MAIN_PLL4_HSDIV3_CLKOUT 5'b10111 - '0' - Reserved 5'b11000 - MCU_EXT_REFCLK0 Pin 5'b11001 - EXT_REFCLK1 Pin 5'b11010 - CPSW_CPTS_GENF0 5'b11011 - CPSW_CPTS_GENF1 5'b11100 - '0' - Reserved 5'b11101 - '0' - Reserved 5'b11110 - '0' - Reserved 5'b11111 - '0' - Reserved Reset Source: mod_g_rst_n

14.2.1.1.1.2.387 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register

14.2.1.1.1.2.387.1 MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register (Offset = A500h) [reset = 0h]

Controls the OSPI loopback clock source

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Table 14-4908. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A500h

Figure 14-2442. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			OSPI0_CLKSEL_LOOPCLK_SEL_PROXY	RESERVED			OSPI0_CLKSEL_CLK_SEL_PROXY
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-4909. MAIN_CTRL_MMR_CFG0_OSPI0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	OSPI0_CLKSEL_LOOPCLK_SEL_PROXY	R/W	0h	OSPI0 Loopback clock source Field values (others are reserved): 1'b0 - Board Level Loopback 1'b1 - Internal Loopback Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	OSPI0_CLKSEL_CLK_SEL_PROXY	R/W	0h	OSPI0 reference clock selection Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV1_CLKOUT 1'b1 - MAIN_PLL1_HSDIV5_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.388 MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL_PROXY Register

14.2.1.1.1.2.388.1 MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL_PROXY Register (Offset = A504h) [reset = 0h]

Controls the OSPI loopback clock source

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Table 14-4910. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A504h

Figure 14-2443. MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>OSPI1_CLKSEL_LOOPCLK_SEL_PROXY</td><td colspan="3">RESERVED</td><td>OSPI1_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-4911. MAIN_CTRL_MMR_CFG0_OSPI1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	OSPI1_CLKSEL_LOOPCLK_SEL_PROXY	R/W	0h	OSPI1 Loopback clock source Field values (others are reserved): 1'b0 - Board Level Loopback 1'b1 - Internal Loopback Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	OSPI1_CLKSEL_CLK_SEL_PROXY	R/W	0h	OSPI1 reference clock selection Field values (others are reserved): 1'b0 - MAIN_PLL0_HSDIV1_CLKOUT 1'b1 - MAIN_PLL1_HSDIV5_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.1.2.389 MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY Register

14.2.1.1.1.2.389.1 MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY Register (Offset = A510h) [reset = 0h]

Controls the functional clock source for the ADC0

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Table 14-4912. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A510h

Figure 14-2444. MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ADC0_CLKSEL_CLK_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-4913. MAIN_CTRL_MMR_CFG0_ADC0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ADC0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the sampling clock source for ADC0 Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - HFOSC1_CLKOUT 2'b10 - MAIN_PLL1_HSDIV4_CLKOUT 2'b11 - EXT_REFCLK1 (Pin) Reset Source: mod_g_rst_n

14.2.1.1.1.2.390 MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL_PROXY Register

14.2.1.1.1.2.390.1 MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL_PROXY Register (Offset = A580h) [reset = 0h]

Controls Main R5 Subsystem 0 clocking

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Table 14-4914. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A580h

Figure 14-2445. MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>R5SS0_CLKSEL_CORE_CLK_SEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-4915. MAIN_CTRL_MMR_CFG0_R5SS0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CLKSEL_CORE_CLK_SEL_PROXY	R/W	0h	Selects R5SS core and interface clock rate Field values (others are reserved): 1'b0 - MAIN_PLL14_HSDIV_CLKOUT 1'b1 - MAIN_PLL14_HSDIV_CLKOUT / 2 (half speed) Reset Source: mod_g_rst_n

14.2.1.1.1.2.391 MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL_PROXY Register

14.2.1.1.1.2.391.1 MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL_PROXY Register (Offset = A584h) [reset = 0h]

Controls Main R5 Subsystem 1 clocking

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Table 14-4916. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 A584h

Figure 14-2446. MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>R5SS1_CLKSEL_CORE_CLK_SEL_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-4917. MAIN_CTRL_MMR_CFG0_R5SS1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CLKSEL_CORE_CLK_SEL_PROXY	R/W	0h	Selects R5SS core and interface clock rate Field values (others are reserved): 1'b0 - MAIN_PLL14_HSDIV_CLKOUT 1'b1 - MAIN_PLL14_HSDIV_CLKOUT / 2 (half speed) Reset Source: mod_g_rst_n

14.2.1.1.1.2.392 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register

14.2.1.1.1.2.392.1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register (Offset = B008h) [reset = 0h]

- KICK0 component

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Table 14-4918. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B008h

Figure 14-2447. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0_PROXY							
R/W							
0h							

Table 14-4919. MAIN_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.393 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register

14.2.1.1.1.2.393.1 MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register (Offset = B00Ch) [reset = 0h]

- KICK1 component

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Table 14-4920. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B00Ch

Figure 14-2448. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK2_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK2_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK2_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK2_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4921. MAIN_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.394 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register

14.2.1.1.1.2.394.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register (Offset = B100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4922. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B100h

Figure 14-2449. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0							
R/W							
0h							

Table 14-4923. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.395 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register

14.2.1.1.1.2.395.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register (Offset = B104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4924. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B104h

Figure 14-2450. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1							
R/W							
0h							

Table 14-4925. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.396 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register

14.2.1.1.1.2.396.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register (Offset = B108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4926. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B108h

Figure 14-2451. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R2							
R/W							
0h							

Table 14-4927. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.397 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register

14.2.1.1.1.2.397.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register (Offset = B10Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-4928. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B10Ch

Figure 14-2452. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R3							
R/W							
0h							

Table 14-4929. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.398 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register

14.2.1.1.1.2.398.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register (Offset = B110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4930. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B110h

Figure 14-2453. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4							
R/W							
0h							

Table 14-4931. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.399 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register

14.2.1.1.1.2.399.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register (Offset = B114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4932. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B114h

Figure 14-2454. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5							
R/W							
0h							

Table 14-4933. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.400 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register

14.2.1.1.1.2.400.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register (Offset = B118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4934. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B118h

Figure 14-2455. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6							
R/W							
0h							

Table 14-4935. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.401 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register

14.2.1.1.1.2.401.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register (Offset = B11Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-4936. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B11Ch

Figure 14-2456. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7							
R/W							
0h							

Table 14-4937. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.402 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register

14.2.1.1.1.2.402.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register (Offset = B120h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4938. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B120h

Figure 14-2457. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R8							
R/W							
0h							

Table 14-4939. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R8	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.403 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register

14.2.1.1.1.2.403.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register (Offset = B124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4940. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B124h

Figure 14-2458. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4941. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.404 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register

14.2.1.1.1.2.404.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register (Offset = B128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-4942. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B128h

Figure 14-2459. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R10							
R/W							
0h							

Table 14-4943. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.405 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register

14.2.1.1.1.2.405.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register (Offset = B12Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-4944. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 B12Ch

Figure 14-2460. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R11							
R/W							
0h							

Table 14-4945. MAIN_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R11	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.1.2.406 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL Register

14.2.1.1.1.2.406.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL Register (Offset = C000h) [reset = 0h]

Configures and enables LBIST operation

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Table 14-4946. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C000h

Figure 14-2461. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_CTRL_BIST_RESET	RESERVED			R5SS0_LBIST_CTRL_BIST_RUN			
R/W	NONE			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS0_LBIST_CTRL_RUNBIST_MODE				RESERVED		R5SS0_LBIST_CTRL_DC_DEF	
R/W				NONE		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS0_LBIST_CTRL_LOAD_DIV	RESERVED		R5SS0_LBIST_CTRL_DIVIDE_RATIO				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-4947. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R5SS0_LBIST_CTRL_BIST_RESET	R/W	0h	Reset LBIST macro Reset Source: mod_g_rst_n
30:28	RESERVED	NONE	0h	Reserved
27:24	R5SS0_LBIST_CTRL_BIST_RUN	R/W	0h	Starts LBIST if all bits are 1 Reset Source: mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:12	R5SS0_LBIST_CTRL_RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1 Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:8	R5SS0_LBIST_CTRL_DC_DEF	R/W	0h	Clock delay after scan_enable switching Reset Source: mod_g_rst_n
7	R5SS0_LBIST_CTRL_LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1 Reset Source: mod_g_rst_n
6:5	RESERVED	NONE	0h	Reserved
4:0	R5SS0_LBIST_CTRL_DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio Reset Source: mod_g_rst_n

14.2.1.1.1.2.407 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT Register

14.2.1.1.1.2.407.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT Register (Offset = C004h) [reset = 0h]

Specifies the number of LBIST patterns to run

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Table 14-4948. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C004h

Figure 14-2462. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT Name Register

31	30	29	28	27	26	25	24
RESERVED		R5SS0_LBIST_PATCOUNT_STATIC_PC_DEF					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R5SS0_LBIST_PATCOUNT_STATIC_PC_DEF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				R5SS0_LBIST_PATCOUNT_SET_PC_DEF			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS0_LBIST_PATCOUNT_RESET_PC_DEF				R5SS0_LBIST_PATCOUNT_SCAN_PC_DEF			
R/W				R/W			
0h				0h			

Table 14-4949. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	R5SS0_LBIST_PATCOUNT_STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	R5SS0_LBIST_PATCOUNT_SET_PC_DEF	R/W	0h	Number of set patterns to run Reset Source: mod_g_rst_n
7:4	R5SS0_LBIST_PATCOUNT_RESET_PC_DEF	R/W	0h	Number of reset patterns to run Reset Source: mod_g_rst_n
3:0	R5SS0_LBIST_PATCOUNT_SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run Reset Source: mod_g_rst_n

14.2.1.1.1.2.408 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0 Register

14.2.1.1.1.2.408.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0 Register (Offset = C008h) [reset = 0h]

Specifies the 32 LSBs of the PRPG seed

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Table 14-4950. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C008h

Figure 14-2463. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0 Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS0_LBIST_SEED0_PRPG_DEF							
R/W							
0h							

Table 14-4951. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS0_LBIST_SEED0_PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0) Reset Source: mod_g_rst_n

14.2.1.1.1.2.409 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1 Register

14.2.1.1.1.2.409.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1 Register (Offset = C00Ch) [reset = 0h]

Specifies the 21 MSBs of the PRPG seed

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Table 14-4952. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C00Ch

Figure 14-2464. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">R5SS0_LBIST_SEED1_PRPG_DEF</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R5SS0_LBIST_SEED1_PRPG_DEF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R5SS0_LBIST_SEED1_PRPG_DEF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4953. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	R5SS0_LBIST_SEED1_PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32) Reset Source: mod_g_rst_n

14.2.1.1.1.2.410 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0 Register

14.2.1.1.1.2.410.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0 Register (Offset = C010h) [reset = 0h]

Spare LBIST control bits

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Table 14-4954. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C010h

Figure 14-2465. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0 Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_SPARE0_SPARE0							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS0_LBIST_SPARE0_SPARE0							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS0_LBIST_SPARE0_SPARE0							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS0_LBIST_SPARE0_SPARE0						R5SS0_LBIST_SPARE0_PBIST_SELFTEST_EN	R5SS0_LBIST_SPARE0_LBIST_SELFTEST_EN
R/W						R/W	R/W
0h						0h	0h

Table 14-4955. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	R5SS0_LBIST_SPARE0_SPARE0	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n
1	R5SS0_LBIST_SPARE0_PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control Reset Source: mod_g_rst_n
0	R5SS0_LBIST_SPARE0_LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control Reset Source: mod_g_rst_n

14.2.1.1.1.2.411 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1 Register

14.2.1.1.1.2.411.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1 Register (Offset = C014h) [reset = 0h]

Spare LBIST control bits

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Table 14-4956. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C014h

Figure 14-2466. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1 Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS0_LBIST_SPARE1_SPARE1							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS0_LBIST_SPARE1_SPARE1							
R/W							
0h							

Table 14-4957. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS0_LBIST_SPARE1_SPARE1	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.412 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT Register

14.2.1.1.1.2.412.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT Register (Offset = C018h) [reset = 0h]

Indicates LBIST status and provides MISR selection control

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Table 14-4958. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C018h

Figure 14-2467. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_STAT_BIST_DONE	RESERVED						
R	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS0_LBIST_STAT_BIST_RUNNING	RESERVED					R5SS0_LBIST_STAT_OUT_MUX_CTL	
R	NONE					R/W	
X	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS0_LBIST_STAT_MISR_MUX_CTL							
R/W							
0h							

Table 14-4959. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R5SS0_LBIST_STAT_BIST_DONE	R	X	LBIST is done Reset Source: mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	R5SS0_LBIST_STAT_BIST_RUNNING	R	X	LBIST is running Reset Source: mod_g_rst_n
14:10	RESERVED	NONE	0h	Reserved
9:8	R5SS0_LBIST_STAT_OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 00 - LBIST IP PID value 01 - LBIST CTRL ID value 1x - MISR value Reset Source: mod_g_rst_n
7:0	R5SS0_LBIST_STAT_MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR. Reset Source: mod_g_rst_n

14.2.1.1.1.2.413 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR Register

14.2.1.1.1.2.413.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR Register (Offset = C01Ch) [reset = 0h]

Contains LBIST MISR output value

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Table 14-4960. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C01Ch

Figure 14-2468. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_MISR_MISR_RESULT							
R							
X							
23	22	21	20	19	18	17	16
R5SS0_LBIST_MISR_MISR_RESULT							
R							
X							
15	14	13	12	11	10	9	8
R5SS0_LBIST_MISR_MISR_RESULT							
R							
X							
7	6	5	4	3	2	1	0
R5SS0_LBIST_MISR_MISR_RESULT							
R							
X							

Table 14-4961. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS0_LBIST_MISR_MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl Reset Source: mod_g_rst_n

14.2.1.1.1.2.414 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL Register

14.2.1.1.1.2.414.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL Register (Offset = C020h) [reset = 0h]

Configures and enables LBIST operation

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Table 14-4962. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C020h

Figure 14-2469. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_CTRL_BIST_RESET	RESERVED			R5SS1_LBIST_CTRL_BIST_RUN			
R/W	NONE			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS1_LBIST_CTRL_RUNBIST_MODE				RESERVED		R5SS1_LBIST_CTRL_DC_DEF	
R/W				NONE		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS1_LBIST_CTRL_LOAD_DIV	RESERVED		R5SS1_LBIST_CTRL_DIVIDE_RATIO				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-4963. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R5SS1_LBIST_CTRL_BIST_RESET	R/W	0h	Reset LBIST macro Reset Source: mod_g_rst_n
30:28	RESERVED	NONE	0h	Reserved
27:24	R5SS1_LBIST_CTRL_BIST_RUN	R/W	0h	Starts LBIST if all bits are 1 Reset Source: mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:12	R5SS1_LBIST_CTRL_RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1 Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:8	R5SS1_LBIST_CTRL_DC_DEF	R/W	0h	Clock delay after scan_enable switching Reset Source: mod_g_rst_n
7	R5SS1_LBIST_CTRL_LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1 Reset Source: mod_g_rst_n
6:5	RESERVED	NONE	0h	Reserved
4:0	R5SS1_LBIST_CTRL_DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio Reset Source: mod_g_rst_n

14.2.1.1.1.2.415 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT Register

14.2.1.1.1.2.415.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT Register (Offset = C024h) [reset = 0h]

Specifies the number of LBIST patterns to run

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Table 14-4964. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C024h

Figure 14-2470. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT Name Register

31	30	29	28	27	26	25	24
RESERVED		R5SS1_LBIST_PATCOUNT_STATIC_PC_DEF					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R5SS1_LBIST_PATCOUNT_STATIC_PC_DEF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				R5SS1_LBIST_PATCOUNT_SET_PC_DEF			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS1_LBIST_PATCOUNT_RESET_PC_DEF				R5SS1_LBIST_PATCOUNT_SCAN_PC_DEF			
R/W				R/W			
0h				0h			

Table 14-4965. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	R5SS1_LBIST_PATCOUNT_STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	R5SS1_LBIST_PATCOUNT_SET_PC_DEF	R/W	0h	Number of set patterns to run Reset Source: mod_g_rst_n
7:4	R5SS1_LBIST_PATCOUNT_RESET_PC_DEF	R/W	0h	Number of reset patterns to run Reset Source: mod_g_rst_n
3:0	R5SS1_LBIST_PATCOUNT_SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run Reset Source: mod_g_rst_n

14.2.1.1.1.2.416 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0 Register

14.2.1.1.1.2.416.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0 Register (Offset = C028h) [reset = 0h]

Specifies the 32 LSBs of the PRPG seed

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Table 14-4966. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C028h

Figure 14-2471. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0 Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS1_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS1_LBIST_SEED0_PRPG_DEF							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_LBIST_SEED0_PRPG_DEF							
R/W							
0h							

Table 14-4967. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS1_LBIST_SEED0_PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0) Reset Source: mod_g_rst_n

14.2.1.1.1.2.417 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1 Register

14.2.1.1.1.2.417.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1 Register (Offset = C02Ch) [reset = 0h]

Specifies the 21 MSBs of the PRPG seed

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Table 14-4968. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C02Ch

Figure 14-2472. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">R5SS1_LBIST_SEED1_PRPG_DEF</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R5SS1_LBIST_SEED1_PRPG_DEF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R5SS1_LBIST_SEED1_PRPG_DEF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4969. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	R5SS1_LBIST_SEED1_PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32) Reset Source: mod_g_rst_n

14.2.1.1.1.2.418 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0 Register

14.2.1.1.1.2.418.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0 Register (Offset = C030h) [reset = 0h]

Spare LBIST control bits

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Table 14-4970. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C030h

Figure 14-2473. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0 Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_SPARE0_SPARE0							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS1_LBIST_SPARE0_SPARE0							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS1_LBIST_SPARE0_SPARE0							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_LBIST_SPARE0_SPARE0						R5SS1_LBIST_SPARE0_PBIST_SELFTEST_EN	R5SS1_LBIST_SPARE0_LBIST_SELFTEST_EN
R/W						R/W	R/W
0h						0h	0h

Table 14-4971. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	R5SS1_LBIST_SPARE0_SPARE0	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n
1	R5SS1_LBIST_SPARE0_PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control Reset Source: mod_g_rst_n
0	R5SS1_LBIST_SPARE0_LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control Reset Source: mod_g_rst_n

14.2.1.1.1.2.419 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1 Register

14.2.1.1.1.2.419.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1 Register (Offset = C034h) [reset = 0h]

Spare LBIST control bits

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Table 14-4972. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C034h

Figure 14-2474. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1 Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_SPARE1_SPARE1							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS1_LBIST_SPARE1_SPARE1							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS1_LBIST_SPARE1_SPARE1							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_LBIST_SPARE1_SPARE1							
R/W							
0h							

Table 14-4973. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS1_LBIST_SPARE1_SPARE1	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.420 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT Register

14.2.1.1.1.2.420.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT Register (Offset = C038h) [reset = 0h]

Indicates LBIST status and provides MISR selection control

Return to Summary Table

Table 14-4974. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C038h

Figure 14-2475. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_STAT_BIST_DONE	RESERVED						
R	NONE						
X	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
R5SS1_LBIST_STAT_BIST_RUNNING	RESERVED					R5SS1_LBIST_STAT_OUT_MUX_CTL	
R	NONE					R/W	
X	0h					0h	
7	6	5	4	3	2	1	0
R5SS1_LBIST_STAT_MISR_MUX_CTL							
R/W							
0h							

Table 14-4975. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R5SS1_LBIST_STAT_BIST_DONE	R	X	LBIST is done Reset Source: mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	R5SS1_LBIST_STAT_BIST_RUNNING	R	X	LBIST is running Reset Source: mod_g_rst_n
14:10	RESERVED	NONE	0h	Reserved
9:8	R5SS1_LBIST_STAT_OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 00 - LBIST IP PID value 01 - LBIST CTRL ID value 1x - MISR value Reset Source: mod_g_rst_n
7:0	R5SS1_LBIST_STAT_MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR. Reset Source: mod_g_rst_n

14.2.1.1.1.2.421 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR Register

14.2.1.1.1.2.421.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR Register (Offset = C03Ch) [reset = 0h]

Contains LBIST MISR output value

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Table 14-4976. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C03Ch

Figure 14-2476. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_MISR_MISR_RESULT							
R							
X							
23	22	21	20	19	18	17	16
R5SS1_LBIST_MISR_MISR_RESULT							
R							
X							
15	14	13	12	11	10	9	8
R5SS1_LBIST_MISR_MISR_RESULT							
R							
X							
7	6	5	4	3	2	1	0
R5SS1_LBIST_MISR_MISR_RESULT							
R							
X							

Table 14-4977. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS1_LBIST_MISR_MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl Reset Source: mod_g_rst_n

14.2.1.1.1.2.422 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SIG Register

14.2.1.1.1.2.422.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SIG Register (Offset = C280h) [reset = 0h]

Contains expected MISR output value

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Table 14-4978. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C280h

Figure 14-2477. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SIG Name Register

31	30	29	28	27	26	25	24
X							
23	22	21	20	19	18	17	16
X							
15	14	13	12	11	10	9	8
X							
7	6	5	4	3	2	1	0
X							

14.2.1.1.1.2.423 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SIG Register

14.2.1.1.1.2.423.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SIG Register (Offset = C2A0h) [reset = 0h]

Contains expected MISR output value

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Table 14-4980. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 C2A0h

Figure 14-2478. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SIG Name Register

31	30	29	28	27	26	25	24
X							
23	22	21	20	19	18	17	16
X							
15	14	13	12	11	10	9	8
X							
7	6	5	4	3	2	1	0
X							

14.2.1.1.1.2.424 MAIN_CTRL_MMR_CFG0_LOCK3_KICK0 Register

14.2.1.1.1.2.424.1 MAIN_CTRL_MMR_CFG0_LOCK3_KICK0 Register (Offset = D008h) [reset = 0h]

- KICK0 component

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Table 14-4982. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 D008h

Figure 14-2479. MAIN_CTRL_MMR_CFG0_LOCK3_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0							
R/W							
0h							

Table 14-4983. MAIN_CTRL_MMR_CFG0_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.425 MAIN_CTRL_MMR_CFG0_LOCK3_KICK1 Register

14.2.1.1.1.2.425.1 MAIN_CTRL_MMR_CFG0_LOCK3_KICK1 Register (Offset = D00Ch) [reset = 0h]

- KICK1 component

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Table 14-4984. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 D00Ch

Figure 14-2480. MAIN_CTRL_MMR_CFG0_LOCK3_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1							
R/W							
0h							

Table 14-4985. MAIN_CTRL_MMR_CFG0_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.426 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register

14.2.1.1.1.2.426.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register (Offset = D100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-4986. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 D100h

Figure 14-2481. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0_READONLY							
R							
0h							

Table 14-4987. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.427 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register

14.2.1.1.1.2.427.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register (Offset = D114h) [reset = 0h]

Claim bits for Partition 3

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Table 14-4988. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 D114h

Figure 14-2482. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R5_READONLY							
R							
0h							

Table 14-4989. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R5_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.428 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL_PROXY Register

14.2.1.1.1.2.428.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL_PROXY Register (Offset = E000h) [reset = 0h]

Configures and enables LBIST operation

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Table 14-4990. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E000h

Figure 14-2483. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_CTRL_BIST_RESET_PROXY	RESERVED			R5SS0_LBIST_CTRL_BIST_RUN_PROXY			
R/W	NONE			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
R5SS0_LBIST_CTRL_RUNBIST_MODE_PROXY				RESERVED		R5SS0_LBIST_CTRL_DC_DEF_PROXY	
R/W				NONE		R/W	
0h				0h		0h	
7	6	5	4	3	2	1	0
R5SS0_LBIST_CTRL_LOAD_DIV_PROXY	RESERVED		R5SS0_LBIST_CTRL_DIVIDE_RATIO_PROXY				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-4991. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R5SS0_LBIST_CTRL_BIST_RESET_PROXY	R/W	0h	Reset LBIST macro Reset Source: mod_g_rst_n
30:28	RESERVED	NONE	0h	Reserved
27:24	R5SS0_LBIST_CTRL_BIST_RUN_PROXY	R/W	0h	Starts LBIST if all bits are 1 Reset Source: mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:12	R5SS0_LBIST_CTRL_RUNBIST_MODE_PROXY	R/W	0h	Runbist mode enable if all bits are 1 Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:8	R5SS0_LBIST_CTRL_DC_DEF_PROXY	R/W	0h	Clock delay after scan_enable switching Reset Source: mod_g_rst_n
7	R5SS0_LBIST_CTRL_LOAD_DIV_PROXY	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1 Reset Source: mod_g_rst_n
6:5	RESERVED	NONE	0h	Reserved

Table 14-4991. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	R5SS0_LBIST_CTRL_DIVIDE_RATIO_PROXY	R/W	0h	LBIST clock divide ratio Reset Source: mod_g_rst_n

14.2.1.1.1.2.429 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT_PROXY Register

14.2.1.1.1.2.429.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT_PROXY Register (Offset = E004h) [reset = 0h]

Specifies the number of LBIST patterns to run

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Table 14-4992. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E004h

Figure 14-2484. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED		R5SS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
R5SS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				R5SS0_LBIST_PATCOUNT_SET_PC_DEF_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
R5SS0_LBIST_PATCOUNT_RESET_PC_DEF_PROXY				R5SS0_LBIST_PATCOUNT_SCAN_PC_DEF_PROXY			
R/W				R/W			
0h				0h			

Table 14-4993. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_PATCOUNT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	R5SS0_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY	R/W	0h	Number of stuck-at patterns to run Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	R5SS0_LBIST_PATCOUNT_SET_PC_DEF_PROXY	R/W	0h	Number of set patterns to run Reset Source: mod_g_rst_n
7:4	R5SS0_LBIST_PATCOUNT_RESET_PC_DEF_PROXY	R/W	0h	Number of reset patterns to run Reset Source: mod_g_rst_n
3:0	R5SS0_LBIST_PATCOUNT_SCAN_PC_DEF_PROXY	R/W	0h	Number of chain test patterns to run Reset Source: mod_g_rst_n

14.2.1.1.1.2.430 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0_PROXY Register

14.2.1.1.1.2.430.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0_PROXY Register (Offset = E008h) [reset = 0h]

Specifies the 32 LSBs of the PRPG seed

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Table 14-4994. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E008h

Figure 14-2485. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS0_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS0_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS0_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							

Table 14-4995. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS0_LBIST_SEED0_PRPG_DEF_PROXY	R/W	0h	Initial seed for PRPG (bits 31:0) Reset Source: mod_g_rst_n

14.2.1.1.1.2.431 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1_PROXY Register

14.2.1.1.1.2.431.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1_PROXY Register (Offset = E00Ch) [reset = 0h]

Specifies the 21 MSBs of the PRPG seed

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Table 14-4996. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E00Ch

Figure 14-2486. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">R5SS0_LBIST_SEED1_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R5SS0_LBIST_SEED1_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R5SS0_LBIST_SEED1_PRPG_DEF_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-4997. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SEED1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	R5SS0_LBIST_SEED1_PRPG_DEF_PROXY	R/W	0h	Initial seed for PRPG (bits 52:32) Reset Source: mod_g_rst_n

14.2.1.1.1.2.432 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0_PROXY Register

14.2.1.1.1.2.432.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0_PROXY Register (Offset = E010h) [reset = 0h]

Spare LBIST control bits

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Table 14-4998. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E010h

Figure 14-2487. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS0_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS0_LBIST_SPARE0_SPARE0_PROXY						R5SS0_LBIST_SPARE0_PBIST_SELFTEST_EN_PROXY	R5SS0_LBIST_SPARE0_LBIST_SELFTEST_EN_PROXY
R/W						R/W	R/W
0h						0h	0h

Table 14-4999. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	R5SS0_LBIST_SPARE0_SPARE0_PROXY	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n
1	R5SS0_LBIST_SPARE0_PBIST_SELFTEST_EN_PROXY	R/W	0h	PBIST isolation control Reset Source: mod_g_rst_n
0	R5SS0_LBIST_SPARE0_LBIST_SELFTEST_EN_PROXY	R/W	0h	LBIST isolation control Reset Source: mod_g_rst_n

14.2.1.1.1.2.433 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1_PROXY Register

14.2.1.1.1.2.433.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1_PROXY Register (Offset = E014h) [reset = 0h]

Spare LBIST control bits

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Table 14-5000. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E014h

Figure 14-2488. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS0_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							

Table 14-5001. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SPARE1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS0_LBIST_SPARE1_SPARE1_PROXY	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.434 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT_PROXY Register

14.2.1.1.1.2.434.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT_PROXY Register (Offset = E018h) [reset = 0h]

Indicates LBIST status and provides MISR selection control

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Table 14-5002. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E018h

Figure 14-2489. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>R5SS0_LBIST_STAT_BIST_DONE_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>X</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>R5SS0_LBIST_STAT_BIST_RUNNING_PROXY</td><td colspan="5">RESERVED</td><td colspan="2">R5SS0_LBIST_STAT_OUT_MUX_CTL_PROXY</td></tr>
<tr><td>R</td><td colspan="5">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>X</td><td colspan="5">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R5SS0_LBIST_STAT_MISR_MUX_CTL_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5003. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R5SS0_LBIST_STAT_BIST_DONE_PROXY	R	X	LBIST is done Reset Source: mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	R5SS0_LBIST_STAT_BIST_RUNNING_PROXY	R	X	LBIST is running Reset Source: mod_g_rst_n
14:10	RESERVED	NONE	0h	Reserved
9:8	R5SS0_LBIST_STAT_OUT_MUX_CTL_PROXY	R/W	0h	Selects source of LBIST output 00 - LBIST IP PID value 01 - LBIST CTRL ID value 1x - MISR value Reset Source: mod_g_rst_n
7:0	R5SS0_LBIST_STAT_MISR_MUX_CTL_PROXY	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR. Reset Source: mod_g_rst_n

14.2.1.1.1.2.435 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR_PROXY Register

14.2.1.1.1.2.435.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR_PROXY Register (Offset = E01Ch) [reset = 0h]

Contains LBIST MISR output value

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Table 14-5004. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E01Ch

Figure 14-2490. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R5SS0_LBIST_MISR_MISR_RESULT_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R5SS0_LBIST_MISR_MISR_RESULT_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R5SS0_LBIST_MISR_MISR_RESULT_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R5SS0_LBIST_MISR_MISR_RESULT_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-5005. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_MISR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS0_LBIST_MISR_MISR_RESULT_PROXY	R	X	32-bits of MISR value selected by misr_mux_ctl Reset Source: mod_g_rst_n

14.2.1.1.1.2.436 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL_PROXY Register

14.2.1.1.1.2.436.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL_PROXY Register (Offset = E020h) [reset = 0h]

Configures and enables LBIST operation

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Table 14-5006. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E020h

Figure 14-2491. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_CTRL_BIST_RESET_PROXY	RESERVED			R5SS1_LBIST_CTRL_BIST_RUN_PROXY			
R/W	NONE			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS1_LBIST_CTRL_RUNBIST_MODE_PROXY				RESERVED		R5SS1_LBIST_CTRL_DC_DEF_PROXY	
R/W				NONE		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS1_LBIST_CTRL_LOAD_DIV_PROXY	RESERVED		R5SS1_LBIST_CTRL_DIVIDE_RATIO_PROXY				
R/W	NONE		R/W				
0h	0h		0h				

Table 14-5007. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R5SS1_LBIST_CTRL_BIST_RESET_PROXY	R/W	0h	Reset LBIST macro Reset Source: mod_g_rst_n
30:28	RESERVED	NONE	0h	Reserved
27:24	R5SS1_LBIST_CTRL_BIST_RUN_PROXY	R/W	0h	Starts LBIST if all bits are 1 Reset Source: mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:12	R5SS1_LBIST_CTRL_RUNBIST_MODE_PROXY	R/W	0h	Runbist mode enable if all bits are 1 Reset Source: mod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9:8	R5SS1_LBIST_CTRL_DC_DEF_PROXY	R/W	0h	Clock delay after scan_enable switching Reset Source: mod_g_rst_n
7	R5SS1_LBIST_CTRL_LOAD_DIV_PROXY	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1 Reset Source: mod_g_rst_n
6:5	RESERVED	NONE	0h	Reserved

Table 14-5007. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	R5SS1_LBIST_CTRL_DIVIDE_RATIO_PROXY	R/W	0h	LBIST clock divide ratio Reset Source: mod_g_rst_n

14.2.1.1.1.2.437 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT_PROXY Register

14.2.1.1.1.2.437.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT_PROXY Register (Offset = E024h) [reset = 0h]

Specifies the number of LBIST patterns to run

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Table 14-5008. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E024h

Figure 14-2492. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED		R5SS1_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R5SS1_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				R5SS1_LBIST_PATCOUNT_SET_PC_DEF_PROXY			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS1_LBIST_PATCOUNT_RESET_PC_DEF_PROXY				R5SS1_LBIST_PATCOUNT_SCAN_PC_DEF_PROXY			
R/W				R/W			
0h				0h			

Table 14-5009. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_PATCOUNT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:16	R5SS1_LBIST_PATCOUNT_STATIC_PC_DEF_PROXY	R/W	0h	Number of stuck-at patterns to run Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	R5SS1_LBIST_PATCOUNT_SET_PC_DEF_PROXY	R/W	0h	Number of set patterns to run Reset Source: mod_g_rst_n
7:4	R5SS1_LBIST_PATCOUNT_RESET_PC_DEF_PROXY	R/W	0h	Number of reset patterns to run Reset Source: mod_g_rst_n
3:0	R5SS1_LBIST_PATCOUNT_SCAN_PC_DEF_PROXY	R/W	0h	Number of chain test patterns to run Reset Source: mod_g_rst_n

14.2.1.1.1.2.438 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0_PROXY Register

14.2.1.1.1.2.438.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0_PROXY Register (Offset = E028h) [reset = 0h]

Specifies the 32 LSBs of the PRPG seed

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Table 14-5010. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E028h

Figure 14-2493. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS1_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS1_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_LBIST_SEED0_PRPG_DEF_PROXY							
R/W							
0h							

Table 14-5011. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS1_LBIST_SEED0_PRPG_DEF_PROXY	R/W	0h	Initial seed for PRPG (bits 31:0) Reset Source: mod_g_rst_n

14.2.1.1.1.2.439 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1_PROXY Register

14.2.1.1.1.2.439.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1_PROXY Register (Offset = E02Ch) [reset = 0h]

Specifies the 21 MSBs of the PRPG seed

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Table 14-5012. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E02Ch

Figure 14-2494. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			R5SS1_LBIST_SEED1_PRPG_DEF_PROXY				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
R5SS1_LBIST_SEED1_PRPG_DEF_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_LBIST_SEED1_PRPG_DEF_PROXY							
R/W							
0h							

Table 14-5013. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SEED1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	R5SS1_LBIST_SEED1_PRPG_DEF_PROXY	R/W	0h	Initial seed for PRPG (bits 52:32) Reset Source: mod_g_rst_n

14.2.1.1.1.2.440 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0_PROXY Register

14.2.1.1.1.2.440.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0_PROXY Register (Offset = E030h) [reset = 0h]

Spare LBIST control bits

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Table 14-5014. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E030h

Figure 14-2495. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS1_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS1_LBIST_SPARE0_SPARE0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_LBIST_SPARE0_SPARE0_PROXY						R5SS1_LBIST_SPARE0_PBIST_SELFTEST_EN_PROXY	R5SS1_LBIST_SPARE0_LBIST_SELFTEST_EN_PROXY
R/W						R/W	R/W
0h						0h	0h

Table 14-5015. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	R5SS1_LBIST_SPARE0_SPARE0_PROXY	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n
1	R5SS1_LBIST_SPARE0_PBIST_SELFTEST_EN_PROXY	R/W	0h	PBIST isolation control Reset Source: mod_g_rst_n
0	R5SS1_LBIST_SPARE0_LBIST_SELFTEST_EN_PROXY	R/W	0h	LBIST isolation control Reset Source: mod_g_rst_n

14.2.1.1.1.2.441 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1_PROXY Register

14.2.1.1.1.2.441.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1_PROXY Register (Offset = E034h) [reset = 0h]

Spare LBIST control bits

Return to Summary Table

Table 14-5016. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E034h

Figure 14-2496. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS1_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS1_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_LBIST_SPARE1_SPARE1_PROXY							
R/W							
0h							

Table 14-5017. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SPARE1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS1_LBIST_SPARE1_SPARE1_PROXY	R/W	0h	LBIST spare bits Reset Source: mod_g_rst_n

14.2.1.1.1.2.442 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT_PROXY Register

14.2.1.1.1.2.442.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT_PROXY Register (Offset = E038h) [reset = 0h]

Indicates LBIST status and provides MISR selection control

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Table 14-5018. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E038h

Figure 14-2497. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_STAT_BIST_DONE_PROXY	RESERVED						
R	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS1_LBIST_STAT_BIST_RUNNING_PROXY	RESERVED					R5SS1_LBIST_STAT_OUT_MUX_CTL_PROXY	
R	NONE					R/W	
X	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS1_LBIST_STAT_MISR_MUX_CTL_PROXY							
R/W							
0h							

Table 14-5019. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R5SS1_LBIST_STAT_BIST_DONE_PROXY	R	X	LBIST is done Reset Source: mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	R5SS1_LBIST_STAT_BIST_RUNNING_PROXY	R	X	LBIST is running Reset Source: mod_g_rst_n
14:10	RESERVED	NONE	0h	Reserved
9:8	R5SS1_LBIST_STAT_OUT_MUX_CTL_PROXY	R/W	0h	Selects source of LBIST output 00 - LBIST IP PID value 01 - LBIST CTRL ID value 1x - MISR value Reset Source: mod_g_rst_n
7:0	R5SS1_LBIST_STAT_MISR_MUX_CTL_PROXY	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR. Reset Source: mod_g_rst_n

14.2.1.1.1.2.443 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR_PROXY Register

14.2.1.1.1.2.443.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR_PROXY Register (Offset = E03Ch) [reset = 0h]

Contains LBIST MISR output value

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Table 14-5020. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E03Ch

Figure 14-2498. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR_PROXY Name Register

31	30	29	28	27	26	25	24
R5SS1_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
23	22	21	20	19	18	17	16
R5SS1_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
15	14	13	12	11	10	9	8
R5SS1_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							
7	6	5	4	3	2	1	0
R5SS1_LBIST_MISR_MISR_RESULT_PROXY							
R							
X							

Table 14-5021. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_MISR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5SS1_LBIST_MISR_MISR_RESULT_PROXY	R	X	32-bits of MISR value selected by misr_mux_ctl Reset Source: mod_g_rst_n

14.2.1.1.1.2.444 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SIG_PROXY Register

14.2.1.1.1.2.444.1 MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SIG_PROXY Register (Offset = E280h) [reset = 0h]

Contains expected MISR output value

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Table 14-5022. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E280h

Figure 14-2499. MAIN_CTRL_MMR_CFG0_R5SS0_LBIST_SIG_PROXY Name Register

31	30	29	28	27	26	25	24
X							
23	22	21	20	19	18	17	16
X							
15	14	13	12	11	10	9	8
X							
7	6	5	4	3	2	1	0
X							

14.2.1.1.1.2.445 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SIG_PROXY Register

14.2.1.1.1.2.445.1 MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SIG_PROXY Register (Offset = E2A0h) [reset = 0h]

Contains expected MISR output value

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Table 14-5024. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 E2A0h

Figure 14-2500. MAIN_CTRL_MMR_CFG0_R5SS1_LBIST_SIG_PROXY Name Register

31	30	29	28	27	26	25	24
X							
23	22	21	20	19	18	17	16
X							
15	14	13	12	11	10	9	8
X							
7	6	5	4	3	2	1	0
X							

14.2.1.1.1.2.446 MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register

14.2.1.1.1.2.446.1 MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register (Offset = F008h) [reset = 0h]

- KICK0 component

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Table 14-5026. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 F008h

Figure 14-2501. MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK3_KICK0_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK3_KICK0_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK3_KICK0_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK3_KICK0_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5027. MAIN_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.447 MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register

14.2.1.1.1.2.447.1 MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register (Offset = F00Ch) [reset = 0h]

- KICK1 component

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Table 14-5028. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 F00Ch

Figure 14-2502. MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1_PROXY							
R/W							
0h							

Table 14-5029. MAIN_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.1.2.448 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register

14.2.1.1.1.2.448.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register (Offset = F100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5030. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 F100h

Figure 14-2503. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5031. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.449 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register

14.2.1.1.1.2.449.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register (Offset = F104h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5032. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 F104h

Figure 14-2504. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5033. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R1	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.450 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register

14.2.1.1.1.2.450.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register (Offset = F108h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5034. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 F108h

Figure 14-2505. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R2							
R/W							
0h							

Table 14-5035. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R2	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.451 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register

14.2.1.1.1.2.451.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register (Offset = F10Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5036. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 F10Ch

Figure 14-2506. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R3							
R/W							
0h							

Table 14-5037. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R3	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.452 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register

14.2.1.1.1.2.452.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register (Offset = F110h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5038. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 F110h

Figure 14-2507. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R4							
R/W							
0h							

Table 14-5039. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R4	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.453 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register

14.2.1.1.1.2.453.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register (Offset = F114h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5040. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0010 F114h

Figure 14-2508. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P3_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5041. MAIN_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R5	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.1.2.454 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register

14.2.1.1.1.2.454.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register (Offset = 11128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5042. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 1128h

Figure 14-2509. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10_READONLY							
R							
0h							

Table 14-5043. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.455 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register

14.2.1.1.1.2.455.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register (Offset = 11138h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5044. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 1138h

Figure 14-2510. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R14_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R14_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R14_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R14_READONLY							
R							
0h							

Table 14-5045. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R14_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.456 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register

14.2.1.1.1.2.456.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register (Offset = 13100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5046. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3100h

Figure 14-2511. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0							
R/W							
0h							

Table 14-5047. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.457 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register

14.2.1.1.1.2.457.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register (Offset = 13104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5048. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3104h

Figure 14-2512. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1							
R/W							
0h							

Table 14-5049. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.458 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register

14.2.1.1.1.2.458.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register (Offset = 13108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5050. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3108h

Figure 14-2513. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2							
R/W							
0h							

Table 14-5051. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.459 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register

14.2.1.1.1.2.459.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register (Offset = 1310Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5052. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 310Ch

Figure 14-2514. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3							
R/W							
0h							

Table 14-5053. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.460 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register

14.2.1.1.1.2.460.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register (Offset = 13110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5054. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3110h

Figure 14-2515. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5055. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.461 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register

14.2.1.1.1.2.461.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register (Offset = 13114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5056. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3114h

Figure 14-2516. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5							
R/W							
0h							

Table 14-5057. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.462 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register

14.2.1.1.1.2.462.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register (Offset = 13118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5058. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3118h

Figure 14-2517. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6							
R/W							
0h							

Table 14-5059. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.463 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register

14.2.1.1.1.2.463.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register (Offset = 1311Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5060. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 311Ch

Figure 14-2518. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7							
R/W							
0h							

Table 14-5061. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.464 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register

14.2.1.1.1.2.464.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register (Offset = 13120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5062. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3120h

Figure 14-2519. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8							
R/W							
0h							

Table 14-5063. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.465 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register

14.2.1.1.1.2.465.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register (Offset = 13124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5064. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3124h

Figure 14-2520. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9							
R/W							
0h							

Table 14-5065. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.466 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register

14.2.1.1.1.2.466.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register (Offset = 13128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5066. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3128h

Figure 14-2521. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10							
R/W							
0h							

Table 14-5067. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.467 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register

14.2.1.1.1.2.467.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register (Offset = 1312Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5068. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 312Ch

Figure 14-2522. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R11							
R/W							
0h							

Table 14-5069. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R11	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.468 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register

14.2.1.1.1.2.468.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register (Offset = 13130h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5070. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3130h

Figure 14-2523. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R12							
R/W							
0h							

Table 14-5071. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R12	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.469 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register

14.2.1.1.1.2.469.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register (Offset = 13134h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5072. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3134h

Figure 14-2524. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R13							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R13							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R13							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R13							
R/W							
0h							

Table 14-5073. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R13	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.470 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register

14.2.1.1.1.2.470.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register (Offset = 13138h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5074. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 3138h

Figure 14-2525. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R14							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R14							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R14							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R14							
R/W							
0h							

Table 14-5075. MAIN_CTRL_MMR_CFG0_CLAIMREG_P4_R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R14	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.1.2.471 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register

14.2.1.1.1.2.471.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register (Offset = 1B100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5076. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B100h

Figure 14-2526. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0							
R/W							
0h							

Table 14-5077. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.472 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register

14.2.1.1.1.2.472.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register (Offset = 1B104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5078. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B104h

Figure 14-2527. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1							
R/W							
0h							

Table 14-5079. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.473 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register

14.2.1.1.1.2.473.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register (Offset = 1B108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5080. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B108h

Figure 14-2528. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2							
R/W							
0h							

Table 14-5081. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.474 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register

14.2.1.1.1.2.474.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register (Offset = 1B10Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-5082. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B10Ch

Figure 14-2529. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3							
R/W							
0h							

Table 14-5083. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.475 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register

14.2.1.1.1.2.475.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register (Offset = 1B110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5084. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B110h

Figure 14-2530. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4							
R/W							
0h							

Table 14-5085. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.476 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register

14.2.1.1.1.2.476.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register (Offset = 1B114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5086. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B114h

Figure 14-2531. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5							
R/W							
0h							

Table 14-5087. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.477 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register

14.2.1.1.1.2.477.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register (Offset = 1B118h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5088. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B118h

Figure 14-2532. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5089. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R6	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.478 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register

14.2.1.1.1.2.478.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register (Offset = 1B11Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-5090. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B11Ch

Figure 14-2533. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R7							
R/W							
0h							

Table 14-5091. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R7	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.1.2.479 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register

14.2.1.1.1.2.479.1 MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register (Offset = 1B120h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5092. Instance Table

Instance Name	Physical Address
MAIN_CTRL_MMR0	0011 B120h

Figure 14-2534. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R8							
R/W							
0h							

Table 14-5093. MAIN_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R8	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2 MCU_CTRL_MMR0

MCU_CTRL_MMR0

14.2.1.1.2.1 MCU_CTRL_MMR0 Summaries

MCU_CTRL_MMR0 Summaries

Table 14-5094. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
0h	32	MCU_CTRL_MMRCFG0_PID	0450 0000h
8h	32	MCU_CTRL_MMRCFG0_MMR_CFG1	0450 0008h
100h	32	MCU_CTRL_MMRCFG0_IPC_SET0	0450 0100h
180h	32	MCU_CTRL_MMRCFG0_IPC_CLR0	0450 0180h
270h	32	MCU_CTRL_MMRCFG0_CBA_ERR_STAT	0450 0270h
280h	32	MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT	0450 0280h
1008h	32	MCU_CTRL_MMRCFG0_LOCK0_KICK0	0450 1008h
100Ch	32	MCU_CTRL_MMRCFG0_LOCK0_KICK1	0450 100Ch
1010h	32	MCU_CTRL_MMRCFG0_INTR_RAW_STATUS	0450 1010h
1014h	32	MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR	0450 1014h
1018h	32	MCU_CTRL_MMRCFG0_INTR_ENABLE	0450 1018h
101Ch	32	MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR	0450 101Ch
1020h	32	MCU_CTRL_MMRCFG0_EOI	0450 1020h
1024h	32	MCU_CTRL_MMRCFG0_FAULT_ADDRESS	0450 1024h
1028h	32	MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS	0450 1028h
102Ch	32	MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS	0450 102Ch
1030h	32	MCU_CTRL_MMRCFG0_FAULT_CLEAR	0450 1030h
1100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY	0450 1100h
1108h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2_READONLY	0450 1108h
110Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3_READONLY	0450 110Ch
1110h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4_READONLY	0450 1110h
1114h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5_READONLY	0450 1114h
2000h	32	MCU_CTRL_MMRCFG0_PID_PROXY	0450 2000h
2008h	32	MCU_CTRL_MMRCFG0_MMR_CFG1_PROXY	0450 2008h
2100h	32	MCU_CTRL_MMRCFG0_IPC_SET0_PROXY	0450 2100h
2180h	32	MCU_CTRL_MMRCFG0_IPC_CLR0_PROXY	0450 2180h
2270h	32	MCU_CTRL_MMRCFG0_CBA_ERR_STAT_PROXY	0450 2270h
2280h	32	MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT_PROXY	0450 2280h
3008h	32	MCU_CTRL_MMRCFG0_LOCK0_KICK0_PROXY	0450 3008h
300Ch	32	MCU_CTRL_MMRCFG0_LOCK0_KICK1_PROXY	0450 300Ch
3010h	32	MCU_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY	0450 3010h
3014h	32	MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	0450 3014h
3018h	32	MCU_CTRL_MMRCFG0_INTR_ENABLE_PROXY	0450 3018h
301Ch	32	MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY	0450 301Ch
3020h	32	MCU_CTRL_MMRCFG0_EOI_PROXY	0450 3020h
3024h	32	MCU_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY	0450 3024h
3028h	32	MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY	0450 3028h
302Ch	32	MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY	0450 302Ch

Table 14-5094. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
3030h	32	MCU_CTRL_MMRCFG0_FAULT_CLEAR_PROXY	0450 3030h
3100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0	0450 3100h
3104h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R1	0450 3104h
3108h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2	0450 3108h
310Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3	0450 310Ch
3110h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4	0450 3110h
3114h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5	0450 3114h
4020h	32	MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL	0450 4020h
4084h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG1	0450 4084h
4088h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG2	0450 4088h
408Ch	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG3	0450 408Ch
4090h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG4	0450 4090h
4094h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG5	0450 4094h
4098h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG6	0450 4098h
40B0h	32	MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT	0450 40B0h
4604h	32	MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0	0450 4604h
4610h	32	MCU_CTRL_MMRCFG0_TOG_STAT	0450 4610h
5008h	32	MCU_CTRL_MMRCFG0_LOCK1_KICK0	0450 5008h
500Ch	32	MCU_CTRL_MMRCFG0_LOCK1_KICK1	0450 500Ch
5100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY	0450 5100h
5104h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY	0450 5104h
5108h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY	0450 5108h
6020h	32	MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL_PROXY	0450 6020h
6084h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG1_PROXY	0450 6084h
6088h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG2_PROXY	0450 6088h
608Ch	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG3_PROXY	0450 608Ch
6090h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG4_PROXY	0450 6090h
6094h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG5_PROXY	0450 6094h
6098h	32	MCU_CTRL_MMRCFG0_DBOUNCE_CFG6_PROXY	0450 6098h
60B0h	32	MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT_PROXY	0450 60B0h
6604h	32	MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0_PROXY	0450 6604h
6610h	32	MCU_CTRL_MMRCFG0_TOG_STAT_PROXY	0450 6610h
7008h	32	MCU_CTRL_MMRCFG0_LOCK1_KICK0_PROXY	0450 7008h
700Ch	32	MCU_CTRL_MMRCFG0_LOCK1_KICK1_PROXY	0450 700Ch
7100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0	0450 7100h
7104h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1	0450 7104h
7108h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2	0450 7108h
710Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R3	0450 710Ch
7110h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R4	0450 7110h
7114h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R5	0450 7114h
7118h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R6	0450 7118h
711Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R7	0450 711Ch
7120h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R8	0450 7120h
7124h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R9	0450 7124h
7128h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R10	0450 7128h
712Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R11	0450 712Ch

Table 14-5094. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
7130h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P1_R12	0450 7130h
8000h	32	MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL	0450 8000h
8010h	32	MCU_CTRL_MMRCFG0_HFOSC0_CTRL	0450 8010h
8014h	32	MCU_CTRL_MMRCFG0_HFOSC1_CTRL	0450 8014h
8020h	32	MCU_CTRL_MMRCFG0_HFOSC0_STAT	0450 8020h
8030h	32	MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL	0450 8030h
8038h	32	MCU_CTRL_MMRCFG0_LFXOSC_CTRL	0450 8038h
8050h	32	MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL	0450 8050h
8058h	32	MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL	0450 8058h
8070h	32	MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL	0450 8070h
9008h	32	MCU_CTRL_MMRCFG0_LOCK2_KICK0	0450 9008h
900Ch	32	MCU_CTRL_MMRCFG0_LOCK2_KICK1	0450 900Ch
9100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0_READONLY	0450 9100h
A000h	32	MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL_PROXY	0450 A000h
A010h	32	MCU_CTRL_MMRCFG0_HFOSC0_CTRL_PROXY	0450 A010h
A014h	32	MCU_CTRL_MMRCFG0_HFOSC1_CTRL_PROXY	0450 A014h
A020h	32	MCU_CTRL_MMRCFG0_HFOSC0_STAT_PROXY	0450 A020h
A030h	32	MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY	0450 A030h
A038h	32	MCU_CTRL_MMRCFG0_LFXOSC_CTRL_PROXY	0450 A038h
A050h	32	MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL_PROXY	0450 A050h
A058h	32	MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL_PROXY	0450 A058h
A070h	32	MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL_PROXY	0450 A070h
B008h	32	MCU_CTRL_MMRCFG0_LOCK2_KICK0_PROXY	0450 B008h
B00Ch	32	MCU_CTRL_MMRCFG0_LOCK2_KICK1_PROXY	0450 B00Ch
B100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0	0450 B100h
11008h	32	MCU_CTRL_MMRCFG0_LOCK4_KICK0	0451 1008h
1100Ch	32	MCU_CTRL_MMRCFG0_LOCK4_KICK1	0451 100Ch
13008h	32	MCU_CTRL_MMRCFG0_LOCK4_KICK0_PROXY	0451 3008h
1300Ch	32	MCU_CTRL_MMRCFG0_LOCK4_KICK1_PROXY	0451 300Ch
13100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R0	0451 3100h
13104h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R1	0451 3104h
13108h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R2	0451 3108h
1310Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R3	0451 310Ch
13110h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R4	0451 3110h
13114h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R5	0451 3114h
13118h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R6	0451 3118h
1311Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R7	0451 311Ch
13120h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R8	0451 3120h
13124h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R9	0451 3124h
13128h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R10	0451 3128h
1312Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R11	0451 312Ch
13130h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R12	0451 3130h
13134h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R13	0451 3134h
13138h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R14	0451 3138h

Table 14-5094. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
1313Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R15	0451 313Ch
13140h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R16	0451 3140h
13144h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R17	0451 3144h
13148h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R18	0451 3148h
1314Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P4_R19	0451 314Ch
18000h	32	MCU_CTRL_MMRCFG0_POR_CTRL	0451 8000h
18004h	32	MCU_CTRL_MMRCFG0_POR_STAT	0451 8004h
18110h	32	MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL	0451 8110h
18114h	32	MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL	0451 8114h
18118h	32	MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL	0451 8118h
1811Ch	32	MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL	0451 811Ch
18120h	32	MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL	0451 8120h
18124h	32	MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL	0451 8124h
18138h	32	MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL	0451 8138h
1813Ch	32	MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL	0451 813Ch
18140h	32	MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL	0451 8140h
18144h	32	MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL	0451 8144h
18148h	32	MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL	0451 8148h
1814Ch	32	MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL	0451 814Ch
18160h	32	MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL	0451 8160h
18170h	32	MCU_CTRL_MMRCFG0_RST_CTRL	0451 8170h
18174h	32	MCU_CTRL_MMRCFG0_RST_STAT	0451 8174h
18178h	32	MCU_CTRL_MMRCFG0_RST_SRC	0451 8178h
18190h	32	MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL	0451 8190h
181B0h	32	MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT	0451 81B0h
18200h	32	MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL	0451 8200h
18208h	32	MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL	0451 8208h
18280h	32	MCU_CTRL_MMRCFG0_CLKGATE_CTRL	0451 8280h
19008h	32	MCU_CTRL_MMRCFG0_LOCK6_KICK0	0451 9008h
1900Ch	32	MCU_CTRL_MMRCFG0_LOCK6_KICK1	0451 900Ch
19100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0_READONLY	0451 9100h
19108h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2_READONLY	0451 9108h
1910Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3_READONLY	0451 910Ch
19110h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4_READONLY	0451 9110h
19114h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5_READONLY	0451 9114h
1A000h	32	MCU_CTRL_MMRCFG0_POR_CTRL_PROXY	0451 A000h
1A004h	32	MCU_CTRL_MMRCFG0_POR_STAT_PROXY	0451 A004h
1A110h	32	MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL_PROXY	0451 A110h
1A114h	32	MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL_PROXY	0451 A114h
1A118h	32	MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL_PROXY	0451 A118h

Table 14-5094. MCU_CTRL_MMR_CFG0 Registers, Base Address=0450 0000h, Length=131072 (continued)

Offset	Length	Register Name	MCU_CTRL_MMR0 Physical Address
1A11Ch	32	MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL_PROXY	0451 A11Ch
1A120h	32	MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL_PROXY	0451 A120h
1A124h	32	MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL_PROXY	0451 A124h
1A138h	32	MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY	0451 A138h
1A13Ch	32	MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY	0451 A13Ch
1A140h	32	MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY	0451 A140h
1A144h	32	MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY	0451 A144h
1A148h	32	MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY	0451 A148h
1A14Ch	32	MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY	0451 A14Ch
1A160h	32	MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL_PROXY	0451 A160h
1A170h	32	MCU_CTRL_MMRCFG0_RST_CTRL_PROXY	0451 A170h
1A174h	32	MCU_CTRL_MMRCFG0_RST_STAT_PROXY	0451 A174h
1A178h	32	MCU_CTRL_MMRCFG0_RST_SRC_PROXY	0451 A178h
1A190h	32	MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL_PROXY	0451 A190h
1A1B0h	32	MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT_PROXY	0451 A1B0h
1A200h	32	MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL_PROXY	0451 A200h
1A208h	32	MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL_PROXY	0451 A208h
1A280h	32	MCU_CTRL_MMRCFG0_CLKGATE_CTRL_PROXY	0451 A280h
1B008h	32	MCU_CTRL_MMRCFG0_LOCK6_KICK0_PROXY	0451 B008h
1B00Ch	32	MCU_CTRL_MMRCFG0_LOCK6_KICK1_PROXY	0451 B00Ch
1B100h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0	0451 B100h
1B104h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R1	0451 B104h
1B108h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2	0451 B108h
1B10Ch	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3	0451 B10Ch
1B110h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4	0451 B110h
1B114h	32	MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5	0451 B114h

14.2.1.1.2.2 MCU_CTRL_MMR0 Registers

MCU_CTRL_MMR0 Registers

14.2.1.1.2.2.1 MCU_CTRL_MMRCFG0_PID Register

14.2.1.1.2.2.1.1 MCU_CTRL_MMRCFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-5095. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 0000h

Figure 14-2535. MCU_CTRL_MMRCFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-5096. MCU_CTRL_MMRCFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.2.2.2 MCU_CTRL_MMRCFG0_MMR_CFG1 Register

14.2.1.1.2.2.2.1 MCU_CTRL_MMRCFG0_MMR_CFG1 Register (Offset = 8h) [reset = 80000057h]

Indicates the MMR configuration

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Table 14-5097. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 0008h

Figure 14-2536. MCU_CTRL_MMRCFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
57h							

Table 14-5098. MCU_CTRL_MMRCFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	57h	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.2.2.3 MCU_CTRL_MMRCFG0_IPC_SET0 Register

14.2.1.1.2.2.3.1 MCU_CTRL_MMRCFG0_IPC_SET0 Register (Offset = 100h) [reset = 0h]

Generate interprocessor communication interrupt to Device Manager

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Table 14-5099. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 0100h

Figure 14-2537. MCU_CTRL_MMRCFG0_IPC_SET0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_SET0_IPC_SRC_SET</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_SET0_IPC_SRC_SET</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_SET0_IPC_SRC_SET</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_SET0_IPC_SRC_SET</td><td colspan="3">RESERVED</td><td>IPC_SET0_IPC_SET</td></tr>
<tr><td colspan="4">R/W1TS</td><td colspan="3">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-5100. MCU_CTRL_MMRCFG0_IPC_SET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET0_IPC_SRC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET0_IPC_SET	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.2.2.4 MCU_CTRL_MMRCFG0_IPC_CLR0 Register

14.2.1.1.2.2.4.1 MCU_CTRL_MMRCFG0_IPC_CLR0 Register (Offset = 180h) [reset = 0h]

Acknowledge interprocessor communication interrupt to Device Manager

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Table 14-5101. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 0180h

Figure 14-2538. MCU_CTRL_MMRCFG0_IPC_CLR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_CLR0_IPC_SRC_CLR</td><td colspan="3">RESERVED</td><td>IPC_CLR0_IPC_CLR</td></tr>
<tr><td colspan="4">R/W1TC</td><td colspan="3">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-5102. MCU_CTRL_MMRCFG0_IPC_CLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR0_IPC_SRC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR0_IPC_CLR	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.2.2.5 MCU_CTRL_MMRCFG0_CBA_ERR_STAT Register

14.2.1.1.2.2.5.1 MCU_CTRL_MMRCFG0_CBA_ERR_STAT Register (Offset = 270h) [reset = 0h]

Indicates addressing errors on the bus segments. Software can read this register upon receiving an mcu_cbass_err interrupt to determine the bus segment on which the error occurred.

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Table 14-5103. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 0270h

Figure 14-2539. MCU_CTRL_MMRCFG0_CBA_ERR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							CBA_ERR_STAT_WKUP_SAFE_CBA_ERR
NONE							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RESERVED			
NONE				NONE			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5104. MCU_CTRL_MMRCFG0_CBA_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR	R	0h	Access Error from Wkup Safe CBASS Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
19:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.6 MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT Register

14.2.1.1.2.2.6.1 MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT Register (Offset = 280h) [reset = 0h]

Indicates an SoC MMR module access error. Software can read this register upon receiving an soc_access_err interrupt to determine the MMR module(s) where the error occurred. Interrupt status registers within the indicated MMR will provide additional details on the type of error. The access error must be cleared within the MMR for the associated access_err_in bit to be cleared.

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Table 14-5105. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 0280h

Figure 14-2540. MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN9</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN8</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN4</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN3</td><td colspan="2">RESERVED</td><td>ACCESS_ERR_STAT_ACCESS_ERR_IN0</td></tr>
<tr><td colspan="3">NONE</td><td>R</td><td>R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-5106. MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ACCESS_ERR_STAT_ACCESS_ERR_IN9	R	0h	Access Error From MCU_PADCFG_CTRL0 MMR Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n
8	ACCESS_ERR_STAT_ACCESS_ERR_IN8	R	0h	Access Error From WKUP_CTRL_MMR1 Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	ACCESS_ERR_STAT_ACCESS_ERR_IN4	R	0h	Access Error From PADCFG_CTRL0 MMR Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n
3	ACCESS_ERR_STAT_ACCESS_ERR_IN3	R	0h	Access Error From CTRL_MMR0 Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved

Table 14-5106. MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ACCESS_ERR_STAT_ACCESS_ERR_IN0	R	0h	Access Error From WKUP_CTRL_MMR0 Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n

14.2.1.1.2.2.7 MCU_CTRL_MMRCFG0_LOCK0_KICK0 Register

14.2.1.1.2.2.7.1 MCU_CTRL_MMRCFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-5107. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1008h

Figure 14-2541. MCU_CTRL_MMRCFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-5108. MCU_CTRL_MMRCFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.8 MCU_CTRL_MMRCFG0_LOCK0_KICK1 Register

14.2.1.1.2.2.8.1 MCU_CTRL_MMRCFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-5109. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 100Ch

Figure 14-2542. MCU_CTRL_MMRCFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-5110. MCU_CTRL_MMRCFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.9 MCU_CTRL_MMRCFG0_INTR_RAW_STATUS Register

14.2.1.1.2.2.9.1 MCU_CTRL_MMRCFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-5111. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1010h

Figure 14-2543. MCU_CTRL_MMRCFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5112. MCU_CTRL_MMRCFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.10 MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register

14.2.1.1.2.2.10.1 MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-5113. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1014h

Figure 14-2544. MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5114. MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.11 MCU_CTRL_MMRCFG0_INTR_ENABLE Register

14.2.1.1.2.2.11.1 MCU_CTRL_MMRCFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-5115. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1018h

Figure 14-2545. MCU_CTRL_MMRCFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5116. MCU_CTRL_MMRCFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.12 MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register

14.2.1.1.2.2.12.1 MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-5117. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 101Ch

Figure 14-2546. MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5118. MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.13 MCU_CTRL_MMRCFG0_EOI Register

14.2.1.1.2.2.13.1 MCU_CTRL_MMRCFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-5119. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1020h

Figure 14-2547. MCU_CTRL_MMRCFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-5120. MCU_CTRL_MMRCFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.2.2.14 MCU_CTRL_MMRCFG0_FAULT_ADDRESS Register

14.2.1.1.2.2.14.1 MCU_CTRL_MMRCFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-5121. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1024h

Figure 14-2548. MCU_CTRL_MMRCFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FAULT_ADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FAULT_ADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FAULT_ADDR							
R							
0h							

Table 14-5122. MCU_CTRL_MMRCFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.2.2.15 MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register

14.2.1.1.2.2.15.1 MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-5123. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1028h

Figure 14-2549. MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-5124. MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.2.2.16 MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register

14.2.1.1.2.2.16.1 MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-5125. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 102Ch

Figure 14-2550. MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID</td><td colspan="4">FAULT_ROUTEID</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5126. MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.2.2.17 MCU_CTRL_MMRCFG0_FAULT_CLEAR Register

14.2.1.1.2.2.17.1 MCU_CTRL_MMRCFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-5127. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1030h

Figure 14-2551. MCU_CTRL_MMRCFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-5128. MCU_CTRL_MMRCFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.18 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register

14.2.1.1.2.2.18.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5129. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1100h

Figure 14-2552. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-5130. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.19 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2_READONLY Register

14.2.1.1.2.2.19.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2_READONLY Register (Offset = 1108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5131. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1108h

Figure 14-2553. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2_READONLY							
R							
0h							

Table 14-5132. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.20 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3_READONLY Register

14.2.1.1.2.2.20.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3_READONLY Register (Offset = 110Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-5133. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 110Ch

Figure 14-2554. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R3_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5134. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.21 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4_READONLY Register

14.2.1.1.2.2.21.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4_READONLY Register (Offset = 1110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5135. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1110h

Figure 14-2555. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4_READONLY							
R							
0h							

Table 14-5136. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.22 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5_READONLY Register

14.2.1.1.2.2.22.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5_READONLY Register (Offset = 1114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5137. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 1114h

Figure 14-2556. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5_READONLY							
R							
0h							

Table 14-5138. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.23 MCU_CTRL_MMRCFG0_PID_PROXY Register

14.2.1.1.2.2.23.1 MCU_CTRL_MMRCFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800215h]

PID register

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Table 14-5139. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 2000h

Figure 14-2557. MCU_CTRL_MMRCFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MSB16_PROXY							
R							
6180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		15h					

Table 14-5140. MCU_CTRL_MMRCFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.2.2.24 MCU_CTRL_MMRCFG0_MMR_CFG1_PROXY Register

14.2.1.1.2.2.24.1 MCU_CTRL_MMRCFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 80000057h]

Indicates the MMR configuration

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Table 14-5141. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 2008h

Figure 14-2558. MCU_CTRL_MMRCFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS_PROXY							
R							
57h							

Table 14-5142. MCU_CTRL_MMRCFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	57h	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.2.2.25 MCU_CTRL_MMRCFG0_IPC_SET0_PROXY Register

14.2.1.1.2.2.25.1 MCU_CTRL_MMRCFG0_IPC_SET0_PROXY Register (Offset = 2100h) [reset = 0h]

Generate interprocessor communication interrupt to Device Manager

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Table 14-5143. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 2100h

Figure 14-2559. MCU_CTRL_MMRCFG0_IPC_SET0_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_SET0_IPC_SRC_SET_PROXY</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_SET0_IPC_SRC_SET_PROXY</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_SET0_IPC_SRC_SET_PROXY</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_SET0_IPC_SRC_SET_PROXY</td><td colspan="3">RESERVED</td><td>IPC_SET0_IPC_SET_PROXY</td></tr>
<tr><td colspan="4">R/W1TS</td><td colspan="3">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-5144. MCU_CTRL_MMRCFG0_IPC_SET0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_SET0_IPC_SRC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_SET0_IPC_SET_PROXY	R/W1TS	0h	Read returns 0 Write: 0 - No effect 1 - Sets both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.2.2.26 MCU_CTRL_MMRCFG0_IPC_CLR0_PROXY Register

14.2.1.1.2.2.26.1 MCU_CTRL_MMRCFG0_IPC_CLR0_PROXY Register (Offset = 2180h) [reset = 0h]

Acknowledge interprocessor communication interrupt to Device Manager

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Table 14-5145. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 2180h

Figure 14-2560. MCU_CTRL_MMRCFG0_IPC_CLR0_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IPC_CLR0_IPC_SRC_CLR_PROXY</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IPC_CLR0_IPC_SRC_CLR_PROXY</td><td colspan="3">RESERVED</td><td>IPC_CLR0_IPC_CLR_PROXY</td></tr>
<tr><td colspan="4">R/W1TC</td><td colspan="3">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-5146. MCU_CTRL_MMRCFG0_IPC_CLR0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IPC_CLR0_IPC_SRC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	IPC_CLR0_IPC_CLR_PROXY	R/W1TC	0h	Read returns current value Write: 0 - No effect 1 - Clears both corresponding IPC_CLR and the IPC_SET bits Reset Source: mod_g_rst_n

14.2.1.1.2.2.27 MCU_CTRL_MMRCFG0_CBA_ERR_STAT_PROXY Register

14.2.1.1.2.2.27.1 MCU_CTRL_MMRCFG0_CBA_ERR_STAT_PROXY Register (Offset = 2270h) [reset = 0h]

Indicates addressing errors on the bus segments. Software can read this register upon receiving an mcu_cbass_err interrupt to determine the bus segment on which the error occurred.

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Table 14-5147. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 2270h

Figure 14-2561. MCU_CTRL_MMRCFG0_CBA_ERR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							CBA_ERR_STAT_WKUP_SAFE_CBA_ERR_PROXY
NONE							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
NONE				NONE			
0h			0h	0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5148. MCU_CTRL_MMRCFG0_CBA_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR_PROXY	R	0h	Access Error from Wkup Safe CBASS Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
19:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.28 MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT_PROXY Register

14.2.1.1.2.2.28.1 MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT_PROXY Register (Offset = 2280h) [reset = 0h]

Indicates an SoC MMR module access error. Software can read this register upon receiving an soc_access_err interrupt to determine the MMR module(s) where the error occurred. Interrupt status registers within the indicated MMR will provide additional details on the type of error. The access error must be cleared within the MMR for the associated access_err_in bit to be cleared.

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Table 14-5149. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 2280h

Figure 14-2562. MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						ACCESS_ERR_STAT_ACCESS_ERR_IN9_PROXY	ACCESS_ERR_STAT_ACCESS_ERR_IN8_PROXY
NONE						R	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ACCESS_ERR_STAT_ACCESS_ERR_IN4_PROXY	ACCESS_ERR_STAT_ACCESS_ERR_IN3_PROXY	RESERVED		ACCESS_ERR_STAT_ACCESS_ERR_IN0_PROXY
NONE			R	R	NONE		R
0h			0h	0h	0h		0h

Table 14-5150. MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ACCESS_ERR_STAT_ACCESS_ERR_IN9_PROXY	R	0h	Access Error From MCU_PADCFG_CTRL0 MMR Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n
8	ACCESS_ERR_STAT_ACCESS_ERR_IN8_PROXY	R	0h	Access Error From WKUP_CTRL_MMR1 Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	ACCESS_ERR_STAT_ACCESS_ERR_IN4_PROXY	R	0h	Access Error From PADCFG_CTRL0 MMR Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n

Table 14-5150. MCU_CTRL_MMRCFG0_ACCESS_ERR_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ACCESS_ERR_STAT_ACCESS_ERR_IN3_PROXY	R	0h	Access Error From CTRL_MMR0 Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	ACCESS_ERR_STAT_ACCESS_ERR_IN0_PROXY	R	0h	Access Error From WKUP_CTRL_MMR0 Field values (others are reserved): 1'b0 - NO_ERROR 1'b1 - ERROR Reset Source: mod_por_rst_n

14.2.1.1.2.2.29 MCU_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register

14.2.1.1.2.2.29.1 MCU_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-5151. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3008h

Figure 14-2563. MCU_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-5152. MCU_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.30 MCU_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register

14.2.1.1.2.2.30.1 MCU_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-5153. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 300Ch

Figure 14-2564. MCU_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-5154. MCU_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.31 MCU_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register

14.2.1.1.2.2.31.1 MCU_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-5155. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3010h

Figure 14-2565. MCU_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5156. MCU_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.32 MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

14.2.1.1.2.2.32.1 MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-5157. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3014h

Figure 14-2566. MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5158. MCU_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.33 MCU_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register

14.2.1.1.2.2.33.1 MCU_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-5159. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3018h

Figure 14-2567. MCU_CTRL_MMRCFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5160. MCU_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.34 MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register

14.2.1.1.2.2.34.1 MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-5161. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 301Ch

Figure 14-2568. MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5162. MCU_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.35 MCU_CTRL_MMRCFG0_EOI_PROXY Register

14.2.1.1.2.2.35.1 MCU_CTRL_MMRCFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-5163. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3020h

Figure 14-2569. MCU_CTRL_MMRCFG0_EOI_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EOI_VECTOR_PROXY							
R/W							
0h							

Table 14-5164. MCU_CTRL_MMRCFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.1.2.2.36 MCU_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register

14.2.1.1.2.2.36.1 MCU_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-5165. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3024h

Figure 14-2570. MCU_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-5166. MCU_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.2.2.37 MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register

14.2.1.1.2.2.37.1 MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-5167. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3028h

Figure 14-2571. MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-5168. MCU_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.2.2.38 MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register

14.2.1.1.2.2.38.1 MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-5169. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 302Ch

Figure 14-2572. MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-5170. MCU_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.2.2.39 MCU_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register

14.2.1.1.2.2.39.1 MCU_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-5171. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3030h

Figure 14-2573. MCU_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-5172. MCU_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.2.2.40 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register

14.2.1.1.2.2.40.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5173. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3100h

Figure 14-2574. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5174. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.41 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R1 Register

14.2.1.1.2.2.41.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R1 Register (Offset = 3104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5175. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3104h

Figure 14-2575. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5176. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.42 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2 Register

14.2.1.1.2.2.42.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2 Register (Offset = 3108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5177. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3108h

Figure 14-2576. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2							
R/W							
0h							

Table 14-5178. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.43 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3 Register

14.2.1.1.2.2.43.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3 Register (Offset = 310Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-5179. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 310Ch

Figure 14-2577. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3							
R/W							
0h							

Table 14-5180. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.44 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4 Register

14.2.1.1.2.2.44.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4 Register (Offset = 3110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5181. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3110h

Figure 14-2578. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4							
R/W							
0h							

Table 14-5182. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.45 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5 Register

14.2.1.1.2.2.45.1 MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5 Register (Offset = 3114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5183. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 3114h

Figure 14-2579. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5							
R/W							
0h							

Table 14-5184. MCU_CTRL_MMRCFG0_CLAIMREG_P0_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.2.2.46 MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL Register

14.2.1.1.2.2.46.1 MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL Register (Offset = 4020h) [reset = 0h]

Controls operation of the MCU_GPIO module

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Table 14-5185. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 4020h

Figure 14-2580. MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCU_GPIO_CTRL_WAKEN
NONE							R/W
0h							0h

Table 14-5186. MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_GPIO_CTRL_WAKEN	R/W	0h	Determines whether or not MCU_GPIO clock is stopped by its LPSC. Preventing the clock stop allows the MCU_GPIO to provide a wakeup event. Field values (others are reserved): 1'b0 - WAKEUP_DISABLED 1'b1 - WAKEUP_ENABLED Reset Source: mod_por_rst_n

14.2.1.1.2.2.47 MCU_CTRL_MMRCFG0_DBOUNCE_CFG1 Register

14.2.1.1.2.2.47.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG1 Register (Offset = 4084h) [reset = 0h]

Configures IO debounce selections

Return to Summary Table

Table 14-5187. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 4084h

Figure 14-2581. MCU_CTRL_MMRCFG0_DBOUNCE_CFG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">DBOUNCE_CFG1_DB_CFG</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-5188. MCU_CTRL_MMRCFG0_DBOUNCE_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5188. MCU_CTRL_MMRCFG0_DBOUNCE_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG1_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 1. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.48 MCU_CTRL_MMRCFG0_DBOUNCE_CFG2 Register

14.2.1.1.2.2.48.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG2 Register (Offset = 4088h) [reset = 0h]

Configures IO debounce selections

Return to Summary Table

Table 14-5189. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 4088h

Figure 14-2582. MCU_CTRL_MMRCFG0_DBOUNCE_CFG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG2_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-5190. MCU_CTRL_MMRCFG0_DBOUNCE_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5190. MCU_CTRL_MMRCFG0_DBOUNCE_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG2_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 2. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.49 MCU_CTRL_MMRCFG0_DBOUNCE_CFG3 Register

14.2.1.1.2.2.49.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG3 Register (Offset = 408Ch) [reset = 0h]

Configures IO debounce selections

Return to Summary Table

Table 14-5191. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 408Ch

Figure 14-2583. MCU_CTRL_MMRCFG0_DBOUNCE_CFG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">DBOUNCE_CFG3_DB_CFG</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-5192. MCU_CTRL_MMRCFG0_DBOUNCE_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5192. MCU_CTRL_MMRCFG0_DBOUNCE_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG3_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 3. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.50 MCU_CTRL_MMRCFG0_DBOUNCE_CFG4 Register

14.2.1.1.2.2.50.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG4 Register (Offset = 4090h) [reset = 0h]

Configures IO debounce selections

Return to Summary Table

Table 14-5193. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 4090h

Figure 14-2584. MCU_CTRL_MMRCFG0_DBOUNCE_CFG4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">DBOUNCE_CFG4_DB_CFG</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-5194. MCU_CTRL_MMRCFG0_DBOUNCE_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5194. MCU_CTRL_MMRCFG0_DBOUNCE_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG4_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 4. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.51 MCU_CTRL_MMRCFG0_DBOUNCE_CFG5 Register

14.2.1.1.2.2.51.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG5 Register (Offset = 4094h) [reset = 0h]

Configures IO debounce selections

Return to Summary Table

Table 14-5195. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 4094h

Figure 14-2585. MCU_CTRL_MMRCFG0_DBOUNCE_CFG5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">DBOUNCE_CFG5_DB_CFG</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-5196. MCU_CTRL_MMRCFG0_DBOUNCE_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5196. MCU_CTRL_MMRCFG0_DBOUNCE_CFG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG5_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 5. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.52 MCU_CTRL_MMRCFG0_DBOUNCE_CFG6 Register

14.2.1.1.2.2.52.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG6 Register (Offset = 4098h) [reset = 0h]

Configures IO debounce selections

Return to Summary Table

Table 14-5197. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 4098h

Figure 14-2586. MCU_CTRL_MMRCFG0_DBOUNCE_CFG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG6_DB_CFG					
NONE		R/W					
0h		0h					

Table 14-5198. MCU_CTRL_MMRCFG0_DBOUNCE_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5198. MCU_CTRL_MMRCFG0_DBOUNCE_CFG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG6_DB_CFG	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 6. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.53 MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT Register

14.2.1.1.2.2.53.1 MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT Register (Offset = 40B0h) [reset = 0h]

Reads returns the current value detected by the IO voltage mode circuit for each dual rail I/O Group.

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Table 14-5199. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 40B0h

Figure 14-2587. MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							IO_VOLTAGE_STAT_ENET
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED			IO_VOLTAGE_STAT_AUDIO	RESERVED		IO_VOLTAGE_STAT_MMC0	IO_VOLTAGE_STAT_GENERAL
NONE			R	NONE		R	R
0h			0h	0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED					IO_VOLTAGE_STAT_CANUART	IO_VOLTAGE_STAT_FLASH	IO_VOLTAGE_STAT_WKUP_MCU
NONE					R	R	R
0h					0h	0h	0h

Table 14-5200. MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	IO_VOLTAGE_STAT_ENET	R	0h	Detected voltage for the ENET I/O group (VDDSHV2) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
15:13	RESERVED	NONE	0h	Reserved
12	IO_VOLTAGE_STAT_AUDIO	R	0h	Detected voltage for the AUDIO I/O group (VDDSHV3) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
11:10	RESERVED	NONE	0h	Reserved
9	IO_VOLTAGE_STAT_MMC0	R	0h	Detected voltage for the MMC0 I/O group (VDDSHV4) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
8	IO_VOLTAGE_STAT_GENERAL	R	0h	Detected voltage for the General I/O group (VDDSHV0) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n

Table 14-5200. MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	IO_VOLTAGE_STAT_CANUART	R	0h	Detected voltage for the CANUART I/O group (VDDSHV_WKUP) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
1	IO_VOLTAGE_STAT_FLASH	R	0h	Detected voltage for the Flash I/O group (VDDSHV1) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
0	IO_VOLTAGE_STAT_WKUP_MCU	R	0h	Detected voltage for the WKUP_MCU I/O group (VDDSHV_MCU) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n

14.2.1.1.2.2.54 MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0 Register

14.2.1.1.2.2.54.1 MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0 Register (Offset = 4604h) [reset = 0h]

Controls the dm2ws WKUP_TIMEOUT0 gasket

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Table 14-5201. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 4604h

Figure 14-2588. MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0 Name Register

31	30	29	28	27	26	25	24
WKUP_MTOG_CTRL0_IDLE_STAT	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WKUP_MTOG_CTRL0_FORCE_TIMEOUT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WKUP_MTOG_CTRL0_TIMEOUT_EN	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					WKUP_MTOG_CTRL0_TIMEOUT_VAL		
NONE					R/W		
0h					0h		

Table 14-5202. MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_MTOG_CTRL0_IDLE_STAT	R	0h	Idle status When high, indicates MTOGundefined is idle. Field values (others are reserved): 1'b0 - BUSY 1'b1 - IDLE Reset Source: mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	WKUP_MTOG_CTRL0_FORCE_TIMEOUT	R/W	0h	Force Timout This is a fault tolerant bitfield. Forces a flush of the interface transactions. This bitfield is only relevant if timeout_en=1. After forcing a timeout by Writing the encoded value, the force_timeout and timeout_en bitfields mut be cleared to clear the timeout before re-enabling the gasket. Field values (others are reserved): 8'h00 - CLEAR_TIMEOUT 8'h95 - FORCE_TIMEOUT Reset Source: mod_g_rst_n
15	WKUP_MTOG_CTRL0_TIMEOUT_EN	R/W	0h	Timeout Gasket Enable Field values (others are reserved): 1'b0 - DISABLED (write 0 to clear the interrupt and reset the gasket counter) 1'b1 - ENABLED Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved

Table 14-5202. MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	WKUP_MTOG_CTRL0_TIMEOUT_VAL	R/W	0h	Gasket Timeout Value Selects the number of clock cycles before the interface is considered to have timed out Field values (others are reserved): 3'b000 - TO_1K_CYCLES 3'b001 - TO_4K_CYCLES 3'b010 - TO_16K_CYCLES 3'b011 - TO_64K_CYCLES 3'b100 - TO_256K_CYCLES 3'b101 - TO_1024K_CYCLES 3'b110 - TO_2048K_CYCLES 3'b111 - TO_4096K_CYCLES Reset Source: mod_g_rst_n

14.2.1.1.2.2.55 MCU_CTRL_MMRCFG0_TOG_STAT Register

14.2.1.1.2.2.55.1 MCU_CTRL_MMRCFG0_TOG_STAT Register (Offset = 4610h) [reset = 0h]

Contains the status of each Timeout Gasket, to be read in ISR to determine which timeout gasket caused an interrupt.

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Table 14-5203. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 4610h

Figure 14-2589. MCU_CTRL_MMRCFG0_TOG_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TOG_STAT_MST_TOG_STAT	
NONE						R	
0h						0h	

Table 14-5204. MCU_CTRL_MMRCFG0_TOG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	TOG_STAT_MST_TOG_STAT	R	0h	Error Status of Initiator Timeout Gaskets Field values (others are reserved): undefined - undefined undefined - undefined 2'b01 - RESERVED 2'b10 - WKUP_TIMEOUT0 undefined - undefined 2'b11 - RESERVED Reset Source: mod_g_rst_n

14.2.1.1.2.2.56 MCU_CTRL_MMRCFG0_LOCK1_KICK0 Register

14.2.1.1.2.2.56.1 MCU_CTRL_MMRCFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-5205. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 5008h

Figure 14-2590. MCU_CTRL_MMRCFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-5206. MCU_CTRL_MMRCFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.57 MCU_CTRL_MMRCFG0_LOCK1_KICK1 Register

14.2.1.1.2.2.57.1 MCU_CTRL_MMRCFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-5207. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 500Ch

Figure 14-2591. MCU_CTRL_MMRCFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-5208. MCU_CTRL_MMRCFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.58 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register

14.2.1.1.2.2.58.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5209. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 5100h

Figure 14-2592. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-5210. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.59 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register

14.2.1.1.2.2.59.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5211. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 5104h

Figure 14-2593. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R1_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5212. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.60 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY Register

14.2.1.1.2.2.60.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5213. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 5108h

Figure 14-2594. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2_READONLY							
R							
0h							

Table 14-5214. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.61 MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL_PROXY Register

14.2.1.1.2.2.61.1 MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL_PROXY Register (Offset = 6020h) [reset = 0h]

Controls operation of the MCU_GPIO module

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Table 14-5215. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 6020h

Figure 14-2595. MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MCU_GPIO_CTRL_WAKEN_PROXY
NONE							R/W
0h							0h

Table 14-5216. MCU_CTRL_MMRCFG0_MCU_GPIO_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MCU_GPIO_CTRL_WAKEN_PROXY	R/W	0h	Determines whether or not MCU_GPIO clock is stopped by its LPSC. Preventing the clock stop allows the MCU_GPIO to provide a wakeup event. Field values (others are reserved): 1'b0 - WAKEUP_DISABLED 1'b1 - WAKEUP_ENABLED Reset Source: mod_por_rst_n

14.2.1.1.2.2.62 MCU_CTRL_MMRCFG0_DBOUNCE_CFG1_PROXY Register

14.2.1.1.2.2.62.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG1_PROXY Register (Offset = 6084h) [reset = 0h]

Configures IO debounce selections

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Table 14-5217. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 6084h

Figure 14-2596. MCU_CTRL_MMRCFG0_DBOUNCE_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		DBOUNCE_CFG1_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5218. MCU_CTRL_MMRCFG0_DBOUNCE_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5218. MCU_CTRL_MMRCFG0_DBOUNCE_CFG1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG1_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 1. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.63 MCU_CTRL_MMRCFG0_DBOUNCE_CFG2_PROXY Register

14.2.1.1.2.2.63.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG2_PROXY Register (Offset = 6088h) [reset = 0h]

Configures IO debounce selections

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Table 14-5219. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 6088h

Figure 14-2597. MCU_CTRL_MMRCFG0_DBOUNCE_CFG2_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG2_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5220. MCU_CTRL_MMRCFG0_DBOUNCE_CFG2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5220. MCU_CTRL_MMRCFG0_DBOUNCE_CFG2_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG2_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 2. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.64 MCU_CTRL_MMRCFG0_DBOUNCE_CFG3_PROXY Register

14.2.1.1.2.2.64.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG3_PROXY Register (Offset = 608Ch) [reset = 0h]

Configures IO debounce selections

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Table 14-5221. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 608Ch

Figure 14-2598. MCU_CTRL_MMRCFG0_DBOUNCE_CFG3_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG3_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5222. MCU_CTRL_MMRCFG0_DBOUNCE_CFG3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5222. MCU_CTRL_MMRCFG0_DBOUNCE_CFG3_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG3_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 3. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.65 MCU_CTRL_MMRCFG0_DBOUNCE_CFG4_PROXY Register

14.2.1.1.2.2.65.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG4_PROXY Register (Offset = 6090h) [reset = 0h]

Configures IO debounce selections

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Table 14-5223. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 6090h

Figure 14-2599. MCU_CTRL_MMRCFG0_DBOUNCE_CFG4_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG4_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5224. MCU_CTRL_MMRCFG0_DBOUNCE_CFG4_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5224. MCU_CTRL_MMRCFG0_DBOUNCE_CFG4_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG4_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 4. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.66 MCU_CTRL_MMRCFG0_DBOUNCE_CFG5_PROXY Register

14.2.1.1.2.2.66.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG5_PROXY Register (Offset = 6094h) [reset = 0h]

Configures IO debounce selections

Return to Summary Table

Table 14-5225. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 6094h

Figure 14-2600. MCU_CTRL_MMRCFG0_DBOUNCE_CFG5_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG5_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5226. MCU_CTRL_MMRCFG0_DBOUNCE_CFG5_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5226. MCU_CTRL_MMRCFG0_DBOUNCE_CFG5_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG5_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 5. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.67 MCU_CTRL_MMRCFG0_DBOUNCE_CFG6_PROXY Register

14.2.1.1.2.2.67.1 MCU_CTRL_MMRCFG0_DBOUNCE_CFG6_PROXY Register (Offset = 6098h) [reset = 0h]

Configures IO debounce selections

Return to Summary Table

Table 14-5227. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 6098h

Figure 14-2601. MCU_CTRL_MMRCFG0_DBOUNCE_CFG6_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		DBOUNCE_CFG6_DB_CFG_PROXY					
NONE		R/W					
0h		0h					

Table 14-5228. MCU_CTRL_MMRCFG0_DBOUNCE_CFG6_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

Table 14-5228. MCU_CTRL_MMRCFG0_DBOUNCE_CFG6_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DBOUNCE_CFG6_DB_CFG_PROXY	R/W	0h	Configures the debounce period used for I/Os with PADCONFIGx_DEBOUNCE_SEL = 6. Debounce period is specified as a number of CLK0 or CLK1 clock cycles. For all inputs CLK0 is CLK_32K_RC and CLK1 is HFOSC0_CLKOUT. Field values (others are reserved): 6'b000000 - BYPASS 6'b000001 - DB_64_CLK0 6'b000010 - DB_96_CLK0 6'b000011 - DB_128_CLK0 6'b000100 - DB_160_CLK0 6'b000101 - DB_192_CLK0 6'b000110 - DB_224_CLK0 6'b000111 - DB_256_CLK0 6'b001000 - DB_288_CLK0 6'b001001 - DB_320_CLK0 6'b001010 - DB_352_CLK0 6'b001011 - DB_384_CLK0 6'b001100 - DB_416_CLK0 6'b001101 - DB_448_CLK0 6'b001110 - DB_480_CLK0 6'b001111 - DB_512_CLK0 6'b010000 - DB_544_CLK0 6'b010001 - DB_576_CLK0 6'b010010 - DB_608_CLK0 6'b010011 - DB_640_CLK0 6'b010100 - DB_672_CLK0 6'b010101 - DB_704_CLK0 6'b010110 - DB_512_CLK0 6'b010111 - DB_1024_CLK0 6'b011000 - DB_1536_CLK0 6'b011001 - DB_2048_CLK0 6'b011010 - DB_2560_CLK0 6'b011011 - DB_3072_CLK0 6'b011100 - DB_3584_CLK0 6'b011101 - DB_4096_CLK0 6'b011110 - DB_4608_CLK0 6'b011111 - DB_5120_CLK0 6'b100000 - DB_1_CLK1 6'b100001 - DB_2_CLK1 6'b100010 - DB_3_CLK1 6'b100011 - DB_4_CLK1 6'b100100 - DB_5_CLK1 6'b100101 - DB_6_CLK1 6'b100110 - DB_7_CLK1 6'b100111 - DB_8_CLK1 6'b101000 - DB_9_CLK1 6'b101001 - DB_10_CLK1 6'b101010 - DB_11_CLK1 6'b101011 - DB_12_CLK1 6'b101100 - DB_13_CLK1 6'b101101 - DB_14_CLK1 6'b101110 - DB_15_CLK1 6'b101111 - DB_16_CLK1 6'b110000 - DB_17_CLK1 6'b110001 - DB_18_CLK1 6'b110010 - DB_19_CLK1 6'b110011 - DB_20_CLK1 6'b110100 - DB_21_CLK1 6'b110101 - DB_22_CLK1 6'b110110 - DB_512_CLK1 6'b110111 - DB_1024_CLK1 6'b111000 - DB_1536_CLK1 6'b111001 - DB_2048_CLK1 6'b111010 - DB_2560_CLK1 6'b111011 - DB_3072_CLK1 6'b111100 - DB_3584_CLK1 6'b111101 - DB_4096_CLK1 6'b111110 - DB_4608_CLK1 6'b111111 - DB_5120_CLK1 Reset Source: mod_por_rst_n

14.2.1.1.2.2.68 MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT_PROXY Register

14.2.1.1.2.2.68.1 MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT_PROXY Register (Offset = 60B0h) [reset = 0h]

Reads returns the current value detected by the IO voltage mode circuit for each dual rail I/O Group.

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Table 14-5229. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 60B0h

Figure 14-2602. MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>IO_VOLTAGE_STAT_ENET_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>IO_VOLTAGE_STAT_AUDIO_PROXY</td><td colspan="2">RESERVED</td><td>IO_VOLTAGE_STAT_MMC0_PROXY</td><td>IO_VOLTAGE_STAT_GENERAL_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td>R</td><td colspan="2">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>IO_VOLTAGE_STAT_CANUART_PROXY</td><td>IO_VOLTAGE_STAT_FLASH_PROXY</td><td>IO_VOLTAGE_STAT_WKUP_MCU_PROXY</td></tr>
<tr><td colspan="5">NONE</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-5230. MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	IO_VOLTAGE_STAT_ENET_PROXY	R	0h	Detected voltage for the ENET I/O group (VDDSHV2) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
15:13	RESERVED	NONE	0h	Reserved
12	IO_VOLTAGE_STAT_AUDIO_PROXY	R	0h	Detected voltage for the AUDIO I/O group (VDDSHV3) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
11:10	RESERVED	NONE	0h	Reserved
9	IO_VOLTAGE_STAT_MMC0_PROXY	R	0h	Detected voltage for the MMC0 I/O group (VDDSHV4) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n

Table 14-5230. MCU_CTRL_MMRCFG0_IO_VOLTAGE_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	IO_VOLTAGE_STAT_GENERAL_PROXY	R	0h	Detected voltage for the General I/O group (VDDSHV0) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
7:3	RESERVED	NONE	0h	Reserved
2	IO_VOLTAGE_STAT_CANUART_PROXY	R	0h	Detected voltage for the CANUART I/O group (VDDSHV_WKUP) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
1	IO_VOLTAGE_STAT_FLASH_PROXY	R	0h	Detected voltage for the Flash I/O group (VDDSHV1) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n
0	IO_VOLTAGE_STAT_WKUP_MCU_PROXY	R	0h	Detected voltage for the WKUP_MCU I/O group (VDDSHV_MCU) Field values (others are reserved): 1'b0 - IOGROUP_3P3V 1'b1 - IOGROUP_1P8V Reset Source: mod_por_rst_n

14.2.1.1.2.2.69 MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0_PROXY Register

14.2.1.1.2.2.69.1 MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0_PROXY Register (Offset = 6604h) [reset = 0h]

Controls the dm2ws WKUP_TIMEOUT0 gasket

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Table 14-5231. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 6604h

Figure 14-2603. MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
WKUP_MTOG_CTRL0_IDLE_STAT_PROXY	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WKUP_MTOG_CTRL0_FORCE_TIMEOUT_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WKUP_MTOG_CTRL0_TIMEOUT_EN_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					WKUP_MTOG_CTRL0_TIMEOUT_VAL_PROXY		
NONE					R/W		
0h					0h		

Table 14-5232. MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_MTOG_CTRL0_IDLE_STAT_PROXY	R	0h	Idle status When high, indicates MTOGundefined is idle. Field values (others are reserved): 1'b0 - BUSY 1'b1 - IDLE Reset Source: mod_g_rst_n
30:24	RESERVED	NONE	0h	Reserved
23:16	WKUP_MTOG_CTRL0_FORCE_TIMEOUT_PROXY	R/W	0h	Force Timout This is a fault tolerant bitfield. Forces a flush of the interface transactions. This bitfield is only relevant if timeout_en=1. After forcing a timeout by Writing the encoded value, the force_timeout and timeout_en bitfields mut be cleared to clear the timeout before re-enabling the gasket. Field values (others are reserved): 8'h00 - CLEAR_TIMEOUT 8'h95 - FORCE_TIMEOUT Reset Source: mod_g_rst_n
15	WKUP_MTOG_CTRL0_TIMEOUT_EN_PROXY	R/W	0h	Timeout Gasket Enable Field values (others are reserved): 1'b0 - DISABLED (write 0 to clear the interrupt and reset the gasket counter) 1'b1 - ENABLED Reset Source: mod_g_rst_n
14:3	RESERVED	NONE	0h	Reserved

Table 14-5232. MCU_CTRL_MMRCFG0_WKUP_MTOG_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	WKUP_MTOG_CTRL0_TIMEOUT_VAL_PROXY	R/W	0h	Gasket Timeout Value Selects the number of clock cycles before the interface is considered to have timed out Field values (others are reserved): 3'b000 - TO_1K_CYCLES 3'b001 - TO_4K_CYCLES 3'b010 - TO_16K_CYCLES 3'b011 - TO_64K_CYCLES 3'b100 - TO_256K_CYCLES 3'b101 - TO_1024K_CYCLES 3'b110 - TO_2048K_CYCLES 3'b111 - TO_4096K_CYCLES Reset Source: mod_g_rst_n

14.2.1.1.2.2.70 MCU_CTRL_MMRCFG0_TOG_STAT_PROXY Register

14.2.1.1.2.2.70.1 MCU_CTRL_MMRCFG0_TOG_STAT_PROXY Register (Offset = 6610h) [reset = 0h]

Contains the status of each Timeout Gasket, to be read in ISR to determine which timeout gasket caused an interrupt.

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Table 14-5233. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 6610h

Figure 14-2604. MCU_CTRL_MMRCFG0_TOG_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TOG_STAT_MST_TOG_STAT_PROXY	
NONE						R	
0h						0h	

Table 14-5234. MCU_CTRL_MMRCFG0_TOG_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	TOG_STAT_MST_TOG_STAT_PROXY	R	0h	Error Status of Initiator Timeout Gaskets Field values (others are reserved): undefined - undefined undefined - undefined 2'b01 - RESERVED 2'b10 - WKUP_TIMEOUT0 undefined - undefined 2'b11 - RESERVED Reset Source: mod_g_rst_n

14.2.1.1.2.2.71 MCU_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register

14.2.1.1.2.2.71.1 MCU_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-5235. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7008h

Figure 14-2605. MCU_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-5236. MCU_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.72 MCU_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register

14.2.1.1.2.2.72.1 MCU_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-5237. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 700Ch

Figure 14-2606. MCU_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-5238. MCU_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.73 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register

14.2.1.1.2.2.73.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5239. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7100h

Figure 14-2607. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-5240. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.74 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register

14.2.1.1.2.2.74.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5241. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7104h

Figure 14-2608. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-5242. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.75 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2 Register

14.2.1.1.2.2.75.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5243. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7108h

Figure 14-2609. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5244. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.76 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R3 Register

14.2.1.1.2.2.76.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5245. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 710Ch

Figure 14-2610. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-5246. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.77 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R4 Register

14.2.1.1.2.2.77.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5247. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7110h

Figure 14-2611. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-5248. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.78 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R5 Register

14.2.1.1.2.2.78.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5249. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7114h

Figure 14-2612. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-5250. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.79 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R6 Register

14.2.1.1.2.2.79.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R6 Register (Offset = 7118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5251. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7118h

Figure 14-2613. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6							
R/W							
0h							

Table 14-5252. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.80 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R7 Register

14.2.1.1.2.2.80.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R7 Register (Offset = 711Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5253. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 711Ch

Figure 14-2614. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R7							
R/W							
0h							

Table 14-5254. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.81 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R8 Register

14.2.1.1.2.2.81.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R8 Register (Offset = 7120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5255. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7120h

Figure 14-2615. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8							
R/W							
0h							

Table 14-5256. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.82 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R9 Register

14.2.1.1.2.2.82.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R9 Register (Offset = 7124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5257. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7124h

Figure 14-2616. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9							
R/W							
0h							

Table 14-5258. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.83 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R10 Register

14.2.1.1.2.2.83.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R10 Register (Offset = 7128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5259. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7128h

Figure 14-2617. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10							
R/W							
0h							

Table 14-5260. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.84 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R11 Register

14.2.1.1.2.2.84.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R11 Register (Offset = 712Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5261. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 712Ch

Figure 14-2618. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R11							
R/W							
0h							

Table 14-5262. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.85 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R12 Register

14.2.1.1.2.2.85.1 MCU_CTRL_MMRCFG0_CLAIMREG_P1_R12 Register (Offset = 7130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5263. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 7130h

Figure 14-2619. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12							
R/W							
0h							

Table 14-5264. MCU_CTRL_MMRCFG0_CLAIMREG_P1_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.2.2.86 MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL Register

14.2.1.1.2.2.86.1 MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL Register (Offset = 8000h) [reset = 0h]

Controls which internal clock is made observable on the MCU_OBSCLK output pin

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Table 14-5265. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8000h

Figure 14-2620. MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							MCU_OBSCLK_CTRL_OUT_MUX_SEL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							MCU_OBSCLK_CTRL_CLK_DIV_LD
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				MCU_OBSCLK_CTRL_CLK_DIV			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCU_OBSCLK_CTRL_CLK_SEL			
NONE				R/W			
0h				0h			

Table 14-5266. MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MCU_OBSCLK_CTRL_OUT_MUX_SEL	R/W	0h	MCU_OBSCLK pin output mux selection. Note, HFOSC0_CLK is a direct output from the HFOSC0, distinct from HFOSC0_CLKOUT. Note, when HFOSC0_CLK is selected (1'b1) the MCU_OBSCLK_CTRL_clk_sel field must be programmed to 4'b0001. Field values (others are reserved): 1'b0 - CLK_DIV_OUT 1'b1 - HFOSC0_CLK (clk_sel must be OFF) Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MCU_OBSCLK_CTRL_CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_por_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	MCU_OBSCLK_CTRL_CLK_DIV	R/W	0h	MCU_OBSCLK pin clock selection output divider Output clock is divided by clk_div+1 Reset Source: mod_por_rst_n
7:4	RESERVED	NONE	0h	Reserved

Table 14-5266. MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MCU_OBSCLK_CTRL_CLK_SEL	R/W	0h	MCU_OBSCLK pin clock selection Field values (others are reserved): 4'b0000 - CLK_12M_RC 4'b0001 - OFF 4'b0010 - MCU_PLL0_HSDIV0_CLKOUT 4'b0011 - MCU_PLL0_HSDIV4_CLKOUT 4'b0100 - MCU_PLLCTRL_OBSCLK 4'b0101 - CLK_32K_RC 4'b0110 - HFOSC0_CLKOUT 4'b0111 - HFOSC0_CLKOUT_32K 4'b1000 - MCU_SYSCLK0 4'b1001 - DEVICE_CLKOUT_32K Reset Source: mod_por_rst_n

14.2.1.1.2.2.87 MCU_CTRL_MMRCFG0_HFOSC0_CTRL Register

14.2.1.1.2.2.87.1 MCU_CTRL_MMRCFG0_HFOSC0_CTRL Register (Offset = 8010h) [reset = 0h]

Controls the operation of oscillator 0

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Table 14-5267. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8010h

Figure 14-2621. MCU_CTRL_MMRCFG0_HFOSC0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HFOSC0_CTRL_PD_C	RESERVED		HFOSC0_CTRL_BP_C	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		0h	0h			

Table 14-5268. MCU_CTRL_MMRCFG0_HFOSC0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HFOSC0_CTRL_PD_C	R/W	0h	Oscillator powerdown control. When set, oscillator is disabled. Oscillator output is tristated if bp_c=0 Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - POWERDOWN Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	HFOSC0_CTRL_BP_C	R/W	0h	Must write '0' Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.88 MCU_CTRL_MMRCFG0_HFOSC1_CTRL Register

14.2.1.1.2.2.88.1 MCU_CTRL_MMRCFG0_HFOSC1_CTRL Register (Offset = 8014h) [reset = 80h]

Controls the operation of oscillator 1

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Table 14-5269. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8014h

Figure 14-2622. MCU_CTRL_MMRCFG0_HFOSC1_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>HFOSC1_CTRL_PD_C</td><td colspan="2">RESERVED</td><td>HFOSC1_CTRL_BP_C</td><td colspan="4">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="2">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td>1h</td><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5270. MCU_CTRL_MMRCFG0_HFOSC1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HFOSC1_CTRL_PD_C	R/W	1h	Oscillator powerdown control. When set, oscillator is disabled. Oscillator output is tristated if bp_c=0 Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - POWERDOWN Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	HFOSC1_CTRL_BP_C	R/W	0h	Must write '0' Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.89 MCU_CTRL_MMRCFG0_HFOSC0_STAT Register

14.2.1.1.2.2.89.1 MCU_CTRL_MMRCFG0_HFOSC0_STAT Register (Offset = 8020h) [reset = 0h]

Allows status of the HFOSC Power Down by DM to be read by Top Level.

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Table 14-5271. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8020h

Figure 14-2623. MCU_CTRL_MMRCFG0_HFOSC0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							0h

Table 14-5272. MCU_CTRL_MMRCFG0_HFOSC0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.90 MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL Register

14.2.1.1.2.2.90.1 MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL Register (Offset = 8030h) [reset = 805Eh]

Controls the HSDIV that generates a 32KHz RT clock from the HFOSC0 Crystal

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Table 14-5273. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8030h

Figure 14-2624. MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL Name Register

31	30	29	28	27	26	25	24
HFOSC0_CLKOUT_32K_CTRL_RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN	RESERVED						HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS
R/W	NONE						R/W
1h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HFOSC0_CLKOUT_32K_CTRL_HSDIV						
NONE	R/W						
0h	5Eh						

Table 14-5274. MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_CLKOUT_32K_CTRL_RESET	R/W	0h	Asynchronous Divider Reset. Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - RESET Reset Source: sys_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN	R/W	1h	HFOSC0_CLKOUT_32K output active Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: sys_por_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS	R/W	0h	HFOSC0_CLKOUT_32K Synchronize Disable This bit must be written 0. Field values (others are reserved): 1'b0 - NORMAL Reset Source: sys_por_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HFOSC0_CLKOUT_32K_CTRL_HSDIV	R/W	5Eh	HFOSC0_CLKOUT_32K divider: HFOSC0_CLKKOUT_32K Frequency = HFOSC0 Frequency / [8 * (hsdiv + 1)] Ex. HFOSC0 Frequency = 25MHz. hsdiv = 94 (Default) HFOSC0_CLKOUT_32K = 25MHz / (8 * (94+1)) = 26MHz / 760 = 32.894 kHz Reset Source: sys_por_rst_n

14.2.1.1.2.2.91 MCU_CTRL_MMRCFG0_LFXOSC_CTRL Register

14.2.1.1.2.2.91.1 MCU_CTRL_MMRCFG0_LFXOSC_CTRL Register (Offset = 8038h) [reset = 80h]

Controls the operation of the low frequency oscillator

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Table 14-5275. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8038h

Figure 14-2625. MCU_CTRL_MMRCFG0_LFXOSC_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LFXOSC_CTRL_PD_C	RESERVED		LFXOSC_CTRL_BP_C	RESERVED			
R/W	NONE		R/W	NONE			
1h	0h		0h	0h			

Table 14-5276. MCU_CTRL_MMRCFG0_LFXOSC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LFXOSC_CTRL_PD_C	R/W	1h	Oscillator powerdown control. When set, oscillator is disabled. Oscillator output is tristated if bp_c=0 Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - POWERDOWN Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	LFXOSC_CTRL_BP_C	R/W	0h	Oscillator bypass control. When set, oscillator is in bypass mode Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - BYPASS Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.92 MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL Register

14.2.1.1.2.2.92.1 MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL Register (Offset = 8050h) [reset = 800000h]

Controls the clock source for MCU PLL

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Table 14-5277. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8050h

Figure 14-2626. MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL Name Register

31	30	29	28	27	26	25	24
MCU_PLL_CLKSEL_BYPASS_SW_OVRD	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
MCU_PLL_CLKSEL_BYP_WARM_RST	RESERVED						
R/W	NONE						
1h	0h						

15	14	13	12	11	10	9	8
RESERVED							MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN
NONE							R/W
0h							0h

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5278. MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_PLL_CLKSEL_BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a mcu_reset_z for MCU_PLL0. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable Software control of exit from bypass mode 1'b1 - Enable Software control of exit from bypass mode Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MCU_PLL_CLKSEL_BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MCU warm reset occurs and will keep MCU_PLL0 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: mcu_chip1_rst_n
22:9	RESERVED	NONE	0h	Reserved

Table 14-5278. MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN	R/W	0h	When set, enables automatic switching of MCU_PLL0 clock source to CLK_12M_RC if HFOSC0 clock loss is detected Field values (others are reserved): 1'b0 - Disable clock source switching on clock loss 1'b1 - Enable clock source switching on clock loss Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.93 MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL Register

14.2.1.1.2.2.93.1 MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL Register (Offset = 8058h) [reset = 0h]

Selects which 32KHz Clock Source provides the 32KHz clock to the Device.

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Table 14-5279. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8058h

Figure 14-2627. MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DEVICE_CLKOUT_32K_CTRL_CLK_32K_RC_SEL	
NONE						R/W	
0h						0h	

Table 14-5280. MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	DEVICE_CLKOUT_32K_CTRL_CLK_32K_RC_SEL	R/W	0h	Selects the source of the device level 32KHz Clock Field values (others are reserved): 2'b00 - CLK_32K_RC 2'b01 - HFOSC0_CLKOUT_32K undefined - undefined 2'b11 - LFOSC0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.2.2.94 MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL Register

14.2.1.1.2.2.94.1 MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL Register (Offset = 8070h) [reset = 0h]

Controls the functional clock source for MCU_GPIO

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Table 14-5281. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 8070h

Figure 14-2628. MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h						0h	

Table 14-5282. MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.95 MCU_CTRL_MMRCFG0_LOCK2_KICK0 Register

14.2.1.1.2.2.95.1 MCU_CTRL_MMRCFG0_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

- KICK0 component

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Table 14-5283. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 9008h

Figure 14-2629. MCU_CTRL_MMRCFG0_LOCK2_KICK0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK2_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK2_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK2_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK2_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5284. MCU_CTRL_MMRCFG0_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.96 MCU_CTRL_MMRCFG0_LOCK2_KICK1 Register

14.2.1.1.2.2.96.1 MCU_CTRL_MMRCFG0_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

- KICK1 component

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Table 14-5285. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 900Ch

Figure 14-2630. MCU_CTRL_MMRCFG0_LOCK2_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1							
R/W							
0h							

Table 14-5286. MCU_CTRL_MMRCFG0_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.97 MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0_READONLY Register

14.2.1.1.2.2.97.1 MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0_READONLY Register (Offset = 9100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5287. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 9100h

Figure 14-2631. MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P2_R0_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P2_R0_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P2_R0_READONLY							
R							
0h							

Table 14-5288. MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.98 MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL_PROXY Register

14.2.1.1.2.2.98.1 MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL_PROXY Register (Offset = A000h) [reset = 0h]

Controls which internal clock is made observable on the MCU_OBSCLK output pin

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Table 14-5289. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A000h

Figure 14-2632. MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							MCU_OBSCLK_CTRL_OUT_MUX_SEL_PROXY
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							MCU_OBSCLK_CTRL_CLK_DIV_LD_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				MCU_OBSCLK_CTRL_CLK_DIV_PROXY			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				MCU_OBSCLK_CTRL_CLK_SEL_PROXY			
NONE				R/W			
0h				0h			

Table 14-5290. MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	MCU_OBSCLK_CTRL_OUT_MUX_SEL_PROXY	R/W	0h	MCU_OBSCLK pin output mux selection. Note, HFOSC0_CLK is a direct output from the HFOSC0, distinct from HFOSC0_CLKOUT. Note, when HFOSC0_CLK is selected (1'b1) the MCU_OBSCLK_CTRL_clk_sel field must be programmed to 4'b0001. Field values (others are reserved): 1'b0 - CLK_DIV_OUT 1'b1 - HFOSC0_CLK (clk_sel must be OFF) Reset Source: mod_por_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	MCU_OBSCLK_CTRL_CLK_DIV_LD_PROXY	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed. Field values (others are reserved): 1'b0 - READY 1'b1 - LOAD Reset Source: mod_por_rst_n
15:12	RESERVED	NONE	0h	Reserved

Table 14-5290. MCU_CTRL_MMRCFG0_MCU_OBSCLK_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	MCU_OBSCLK_CTRL_CLK_DIV_PROXY	R/W	0h	MCU_OBSCLK pin clock selection output divider Output clock is divided by clk_div+1 Reset Source: mod_por_rst_n
7:4	RESERVED	NONE	0h	Reserved
3:0	MCU_OBSCLK_CTRL_CLK_SEL_PROXY	R/W	0h	MCU_OBSCLK pin clock selection Field values (others are reserved): 4'b0000 - CLK_12M_RC 4'b0001 - OFF 4'b0010 - MCU_PLL0_HSDIV0_CLKOUT 4'b0011 - MCU_PLL0_HSDIV4_CLKOUT 4'b0100 - MCU_PLLCTRL_OBSCLK 4'b0101 - CLK_32K_RC 4'b0110 - HFOSC0_CLKOUT 4'b0111 - HFOSC0_CLKOUT_32K 4'b1000 - MCU_SYSCLK0 4'b1001 - DEVICE_CLKOUT_32K Reset Source: mod_por_rst_n

14.2.1.1.2.2.99 MCU_CTRL_MMRCFG0_HFOSC0_CTRL_PROXY Register

14.2.1.1.2.2.99.1 MCU_CTRL_MMRCFG0_HFOSC0_CTRL_PROXY Register (Offset = A010h) [reset = 0h]

Controls the operation of oscillator 0

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Table 14-5291. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A010h

Figure 14-2633. MCU_CTRL_MMRCFG0_HFOSC0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HFOSC0_CTRL_PD_C_PROXY	RESERVED		HFOSC0_CTRL_BP_C_PROXY	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		0h	0h			

Table 14-5292. MCU_CTRL_MMRCFG0_HFOSC0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HFOSC0_CTRL_PD_C_PROXY	R/W	0h	Oscillator powerdown control. When set, oscillator is disabled. Oscillator output is tristated if bp_c=0 Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - POWERDOWN Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	HFOSC0_CTRL_BP_C_PROXY	R/W	0h	Must write '0' Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.100 MCU_CTRL_MMRCFG0_HFOSC1_CTRL_PROXY Register

14.2.1.1.2.2.100.1 MCU_CTRL_MMRCFG0_HFOSC1_CTRL_PROXY Register (Offset = A014h) [reset = 80h]

Controls the operation of oscillator 1

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Table 14-5293. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A014h

Figure 14-2634. MCU_CTRL_MMRCFG0_HFOSC1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HFOSC1_CTRL_PD_C_PROXY	RESERVED		HFOSC1_CTRL_BP_C_PROXY	RESERVED			
R/W	NONE		R/W	NONE			
1h	0h		0h	0h			

Table 14-5294. MCU_CTRL_MMRCFG0_HFOSC1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HFOSC1_CTRL_PD_C_PROXY	R/W	1h	Oscillator powerdown control. When set, oscillator is disabled. Oscillator output is tristated if bp_c=0 Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - POWERDOWN Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	HFOSC1_CTRL_BP_C_PROXY	R/W	0h	Must write '0' Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.101 MCU_CTRL_MMRCFG0_HFOSC0_STAT_PROXY Register

14.2.1.1.2.2.101.1 MCU_CTRL_MMRCFG0_HFOSC0_STAT_PROXY Register (Offset = A020h) [reset = 0h]

Allows status of the HFOSC Power Down by DM to be read by Top Level.

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Table 14-5295. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A020h

Figure 14-2635. MCU_CTRL_MMRCFG0_HFOSC0_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							0h

Table 14-5296. MCU_CTRL_MMRCFG0_HFOSC0_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.102 MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register

14.2.1.1.2.2.102.1 MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register (Offset = A030h) [reset = 805Eh]

Controls the HSDIV that generates a 32KHz RT clock from the HFOSC0 Crystal

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Table 14-5297. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A030h

Figure 14-2636. MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
HFOSC0_CLKOUT_32K_CTRL_RESET_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN_PROXY	RESERVED						HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS_PROXY
R/W	NONE						R/W
1h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HFOSC0_CLKOUT_32K_CTRL_HSDIV_PROXY						
NONE	R/W						
0h	5Eh						

Table 14-5298. MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HFOSC0_CLKOUT_32K_CTRL_RESET_PROXY	R/W	0h	Asynchronous Divider Reset. Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - RESET Reset Source: sys_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	HFOSC0_CLKOUT_32K_CTRL_CLKOUT_EN_PROXY	R/W	1h	HFOSC0_CLKOUT_32K output active Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: sys_por_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	HFOSC0_CLKOUT_32K_CTRL_SYNC_DIS_PROXY	R/W	0h	HFOSC0_CLKOUT_32K Synchronize Disable This bit must be written 0. Field values (others are reserved): 1'b0 - NORMAL Reset Source: sys_por_rst_n
7	RESERVED	NONE	0h	Reserved

Table 14-5298. MCU_CTRL_MMRCFG0_HFOSC0_CLKOUT_32K_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	HFOSC0_CLKOUT_32K_CTRL_HSDIV_PROXY	R/W	5Eh	HFOSC0_CLKOUT_32K divider: HFOSC0_CLKKOUT_32K Frequency = HFOSC0 Frequency / [8 * (hsdiv + 1)] Ex. HFOSC0 Frequency = 25MHz. hsdiv = 94 (Default) HFOSC0_CLKOUT_32K = 25MHz / (8 * (94+1)) = 26MHz / 760 = 32.894 kHz Reset Source: sys_por_rst_n

14.2.1.1.2.2.103 MCU_CTRL_MMRCFG0_LFXOSC_CTRL_PROXY Register

14.2.1.1.2.2.103.1 MCU_CTRL_MMRCFG0_LFXOSC_CTRL_PROXY Register (Offset = A038h) [reset = 80h]

Controls the operation of the low frequency oscillator

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Table 14-5299. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A038h

Figure 14-2637. MCU_CTRL_MMRCFG0_LFXOSC_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LFXOSC_CTRL_PD_C_PROXY	RESERVED		LFXOSC_CTRL_BP_C_PROXY	RESERVED			
R/W	NONE		R/W	NONE			
1h	0h		0h	0h			

Table 14-5300. MCU_CTRL_MMRCFG0_LFXOSC_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LFXOSC_CTRL_PD_C_PROXY	R/W	1h	Oscillator powerdown control. When set, oscillator is disabled. Oscillator output is tristated if bp_c=0 Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - POWERDOWN Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	LFXOSC_CTRL_BP_C_PROXY	R/W	0h	Oscillator bypass control. When set, oscillator is in bypass mode Field values (others are reserved): 1'b0 - ACTIVE 1'b1 - BYPASS Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.104 MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL_PROXY Register

14.2.1.1.2.2.104.1 MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL_PROXY Register (Offset = A050h) [reset = 800000h]

Controls the clock source for MCU PLL

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Table 14-5301. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A050h

Figure 14-2638. MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
MCU_PLL_CLKSEL_BYPASS_SW_OVRD_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
MCU_PLL_CLKSEL_BYP_WARM_RST_PROXY	RESERVED						
R/W	NONE						
1h	0h						
15	14	13	12	11	10	9	8
RESERVED							MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5302. MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MCU_PLL_CLKSEL_BYPASS_SW_OVRD_PROXY	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a mcu_reset_z for MCU_PLL0. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode. Field values (others are reserved): 1'b0 - Disable Software control of exit from bypass mode 1'b1 - Enable Software control of exit from bypass mode Reset Source: sys_por_rst_n
30:24	RESERVED	NONE	0h	Reserved
23	MCU_PLL_CLKSEL_BYP_WARM_RST_PROXY	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1'b1 to enable bypass software override. This bit is set (1'b1) when a MCU warm reset occurs and will keep MCU_PLL0 in bypass mode after reset exit until cleared by software. Field values (others are reserved): 1'b0 - EXIT_BYPASS 1'b1 - MAINTAIN_BYPASS Reset Source: mcu_chip1_rst_n

Table 14-5302. MCU_CTRL_MMRCFG0_MCU_PLL_CLKSEL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:9	RESERVED	NONE	0h	Reserved
8	MCU_PLL_CLKSEL_CLKLOSS_SWTCH_EN_PROXY	R/W	0h	When set, enables automatic switching of MCU_PLL0 clock source to CLK_12M_RC if HFOSC0 clock loss is detected Field values (others are reserved): 1'b0 - Disable clock source switching on clock loss 1'b1 - Enable clock source switching on clock loss Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.105 MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL_PROXY Register

14.2.1.1.2.2.105.1 MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL_PROXY Register (Offset = A058h) [reset = 0h]

Selects which 32KHz Clock Source provides the 32KHz clock to the Device.

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Table 14-5303. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A058h

Figure 14-2639. MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DEVICE_CLKOUT_32K_CTRL_CLK_32K_RC_SEL_PROXY	
NONE						R/W	
0h						0h	

Table 14-5304. MCU_CTRL_MMRCFG0_DEVICE_CLKOUT_32K_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	DEVICE_CLKOUT_32K_CTRL_CLK_32K_RC_SEL_PROXY	R/W	0h	Selects the source of the device level 32KHz Clock Field values (others are reserved): 2'b00 - CLK_32K_RC 2'b01 - HFOSC0_CLKOUT_32K undefined - undefined 2'b11 - LFOSC0_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.2.2.106 MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL_PROXY Register

14.2.1.1.2.2.106.1 MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL_PROXY Register (Offset = A070h) [reset = 0h]

Controls the functional clock source for MCU_GPIO

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Table 14-5305. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 A070h

Figure 14-2640. MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h						0h	

Table 14-5306. MCU_CTRL_MMRCFG0_MCU_GPIO_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.107 MCU_CTRL_MMRCFG0_LOCK2_KICK0_PROXY Register

14.2.1.1.2.2.107.1 MCU_CTRL_MMRCFG0_LOCK2_KICK0_PROXY Register (Offset = B008h) [reset = 0h]

- KICK0 component

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Table 14-5307. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 B008h

Figure 14-2641. MCU_CTRL_MMRCFG0_LOCK2_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0_PROXY							
R/W							
0h							

Table 14-5308. MCU_CTRL_MMRCFG0_LOCK2_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.108 MCU_CTRL_MMRCFG0_LOCK2_KICK1_PROXY Register

14.2.1.1.2.2.108.1 MCU_CTRL_MMRCFG0_LOCK2_KICK1_PROXY Register (Offset = B00Ch) [reset = 0h]

- KICK1 component

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Table 14-5309. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 B00Ch

Figure 14-2642. MCU_CTRL_MMRCFG0_LOCK2_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1_PROXY							
R/W							
0h							

Table 14-5310. MCU_CTRL_MMRCFG0_LOCK2_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.109 MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0 Register

14.2.1.1.2.2.109.1 MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0 Register (Offset = B100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5311. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0450 B100h

Figure 14-2643. MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0							
R/W							
0h							

Table 14-5312. MCU_CTRL_MMRCFG0_CLAIMREG_P2_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.2.2.110 MCU_CTRL_MMRCFG0_LOCK4_KICK0 Register

14.2.1.1.2.2.110.1 MCU_CTRL_MMRCFG0_LOCK4_KICK0 Register (Offset = 11008h) [reset = 0h]

- KICK0 component

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Table 14-5313. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 1008h

Figure 14-2644. MCU_CTRL_MMRCFG0_LOCK4_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0							
R/W							
0h							

Table 14-5314. MCU_CTRL_MMRCFG0_LOCK4_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.111 MCU_CTRL_MMRCFG0_LOCK4_KICK1 Register

14.2.1.1.2.2.111.1 MCU_CTRL_MMRCFG0_LOCK4_KICK1 Register (Offset = 1100Ch) [reset = 0h]

- KICK1 component

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Table 14-5315. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 100Ch

Figure 14-2645. MCU_CTRL_MMRCFG0_LOCK4_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1							
R/W							
0h							

Table 14-5316. MCU_CTRL_MMRCFG0_LOCK4_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.112 MCU_CTRL_MMRCFG0_LOCK4_KICK0_PROXY Register

14.2.1.1.2.2.112.1 MCU_CTRL_MMRCFG0_LOCK4_KICK0_PROXY Register (Offset = 13008h) [reset = 0h]

- KICK0 component

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Table 14-5317. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3008h

Figure 14-2646. MCU_CTRL_MMRCFG0_LOCK4_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK0_PROXY							
R/W							
0h							

Table 14-5318. MCU_CTRL_MMRCFG0_LOCK4_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.113 MCU_CTRL_MMRCFG0_LOCK4_KICK1_PROXY Register

14.2.1.1.2.2.113.1 MCU_CTRL_MMRCFG0_LOCK4_KICK1_PROXY Register (Offset = 1300Ch) [reset = 0h]

- KICK1 component

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Table 14-5319. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 300Ch

Figure 14-2647. MCU_CTRL_MMRCFG0_LOCK4_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK4_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK4_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK4_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK4_KICK1_PROXY							
R/W							
0h							

Table 14-5320. MCU_CTRL_MMRCFG0_LOCK4_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK4_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.114 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R0 Register

14.2.1.1.2.2.114.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R0 Register (Offset = 13100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5321. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3100h

Figure 14-2648. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0							
R/W							
0h							

Table 14-5322. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.115 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R1 Register

14.2.1.1.2.2.115.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R1 Register (Offset = 13104h) [reset = 0h]

Claim bits for Partition 4

Return to Summary Table

Table 14-5323. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3104h

Figure 14-2649. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1							
R/W							
0h							

Table 14-5324. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.116 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R2 Register

14.2.1.1.2.2.116.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R2 Register (Offset = 13108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5325. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3108h

Figure 14-2650. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2							
R/W							
0h							

Table 14-5326. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.117 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R3 Register

14.2.1.1.2.2.117.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R3 Register (Offset = 1310Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5327. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 310Ch

Figure 14-2651. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3							
R/W							
0h							

Table 14-5328. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.118 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R4 Register

14.2.1.1.2.2.118.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R4 Register (Offset = 13110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5329. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3110h

Figure 14-2652. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4							
R/W							
0h							

Table 14-5330. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.119 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R5 Register

14.2.1.1.2.2.119.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R5 Register (Offset = 13114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5331. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3114h

Figure 14-2653. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5							
R/W							
0h							

Table 14-5332. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.120 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R6 Register

14.2.1.1.2.2.120.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R6 Register (Offset = 13118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5333. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3118h

Figure 14-2654. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6							
R/W							
0h							

Table 14-5334. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.121 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R7 Register

14.2.1.1.2.2.121.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R7 Register (Offset = 1311Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5335. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 311Ch

Figure 14-2655. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5336. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.122 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R8 Register

14.2.1.1.2.2.122.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R8 Register (Offset = 13120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5337. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3120h

Figure 14-2656. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8							
R/W							
0h							

Table 14-5338. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.123 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R9 Register

14.2.1.1.2.2.123.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R9 Register (Offset = 13124h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5339. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3124h

Figure 14-2657. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R9							
R/W							
0h							

Table 14-5340. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R9	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.124 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R10 Register

14.2.1.1.2.2.124.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R10 Register (Offset = 13128h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5341. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3128h

Figure 14-2658. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R10							
R/W							
0h							

Table 14-5342. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R10	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.125 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R11 Register

14.2.1.1.2.2.125.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R11 Register (Offset = 1312Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5343. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 312Ch

Figure 14-2659. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R11							
R/W							
0h							

Table 14-5344. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R11	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.126 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R12 Register

14.2.1.1.2.2.126.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R12 Register (Offset = 13130h) [reset = 0h]

Claim bits for Partition 4

Return to Summary Table

Table 14-5345. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3130h

Figure 14-2660. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R12							
R/W							
0h							

Table 14-5346. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R12	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.127 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R13 Register

14.2.1.1.2.2.127.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R13 Register (Offset = 13134h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5347. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3134h

Figure 14-2661. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R13 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R13							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R13							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R13							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R13							
R/W							
0h							

Table 14-5348. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R13	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.128 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R14 Register

14.2.1.1.2.2.128.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R14 Register (Offset = 13138h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5349. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3138h

Figure 14-2662. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R14 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R14							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R14							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R14							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R14							
R/W							
0h							

Table 14-5350. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R14	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.129 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R15 Register

14.2.1.1.2.2.129.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R15 Register (Offset = 1313Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5351. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 313Ch

Figure 14-2663. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R15 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R15							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R15							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R15							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R15							
R/W							
0h							

Table 14-5352. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R15	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.130 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R16 Register

14.2.1.1.2.2.130.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R16 Register (Offset = 13140h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5353. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3140h

Figure 14-2664. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R16 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R16							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R16							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R16							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R16							
R/W							
0h							

Table 14-5354. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R16	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.131 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R17 Register

14.2.1.1.2.2.131.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R17 Register (Offset = 13144h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5355. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3144h

Figure 14-2665. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R17 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R17							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R17							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R17							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R17							
R/W							
0h							

Table 14-5356. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R17	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.132 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R18 Register

14.2.1.1.2.2.132.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R18 Register (Offset = 13148h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5357. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 3148h

Figure 14-2666. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R18 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R18</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R18</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R18</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P4_R18</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5358. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R18	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.133 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R19 Register

14.2.1.1.2.2.133.1 MCU_CTRL_MMRCFG0_CLAIMREG_P4_R19 Register (Offset = 1314Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5359. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 314Ch

Figure 14-2667. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R19 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R19							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R19							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R19							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R19							
R/W							
0h							

Table 14-5360. MCU_CTRL_MMRCFG0_CLAIMREG_P4_R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R19	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.2.2.134 MCU_CTRL_MMRCFG0_POR_CTRL Register

14.2.1.1.2.2.134.1 MCU_CTRL_MMRCFG0_POR_CTRL Register (Offset = 18000h) [reset = 10h]

Configures POR module reset behavior and allows software to directly override POR comparator outputs.

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Table 14-5361. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8000h

Figure 14-2668. MCU_CTRL_MMRCFG0_POR_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED		POR_CTRL_OVRD_SET5	POR_CTRL_OVRD_SET4	POR_CTRL_OVRD_SET3	POR_CTRL_OVRD_SET2	POR_CTRL_OVRD_SET1	POR_CTRL_OVRD_SET0
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		POR_CTRL_OVRD5	POR_CTRL_OVRD4	POR_CTRL_OVRD3	POR_CTRL_OVRD2	POR_CTRL_OVRD1	POR_CTRL_OVRD0
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POR_CTRL_TRIM_SEL	RESERVED		POR_CTRL_MASK_HHV	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		1h	0h			

Table 14-5362. MCU_CTRL_MMRCFG0_POR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	POR_CTRL_OVRD_SET5	R/W	0h	Override value when override is active, for RESERVED output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
28	POR_CTRL_OVRD_SET4	R/W	0h	Override value when override is active, for POKLVB output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
27	POR_CTRL_OVRD_SET3	R/W	0h	Override value when override is active, for POKLVA output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
26	POR_CTRL_OVRD_SET2	R/W	0h	Override value when override is active, for POKHV output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n

Table 14-5362. MCU_CTRL_MMRCFG0_POR_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	POR_CTRL_OVRD_SET1	R/W	0h	Override value when override is active, for BGOK output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
24	POR_CTRL_OVRD_SET0	R/W	0h	Override value when override is active, for PORHV output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	POR_CTRL_OVRD5	R/W	0h	Enables override of RESERVED output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
20	POR_CTRL_OVRD4	R/W	0h	Enables override of POKLVB output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
19	POR_CTRL_OVRD3	R/W	0h	Enables override of POKLVA output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
18	POR_CTRL_OVRD2	R/W	0h	Enables override of POKHV output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
17	POR_CTRL_OVRD1	R/W	0h	Enables override of BGOK output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
16	POR_CTRL_OVRD0	R/W	0h	Enables override of PORHV output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
15:8	RESERVED	NONE	0h	Reserved
7	POR_CTRL_TRIM_SEL	R/W	0h	POR Trim Select - Fixed value or from POR_BANDGAP_CTRL and POR_POKxxx_CTRL registers MMRs Field values (others are reserved): 1'b0 - FIXED_TRIM 1'b1 - MMR_TRIM Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	POR_CTRL_MASK_HHV	R/W	1h	Mask HHV/SOC_PORz outputs when applying new trim values Field values (others are reserved): 1'b0 - UNMASK 1'b1 - MASK Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.135 MCU_CTRL_MMRCFG0_POR_STAT Register

14.2.1.1.2.2.135.1 MCU_CTRL_MMRCFG0_POR_STAT Register (Offset = 18004h) [reset = 0h]

Shows POR module status

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Table 14-5363. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8004h

Figure 14-2669. MCU_CTRL_MMRCFG0_POR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							POR_STAT_BGOK
NONE							R
0h							0h

7	6	5	4	3	2	1	0
RESERVED			POR_STAT_SOC_POR	RESERVED			
NONE			R	NONE			
0h			0h	0h			

Table 14-5364. MCU_CTRL_MMRCFG0_POR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	POR_STAT_BGOK	R	0h	Bandgap OK status Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - OK Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	POR_STAT_SOC_POR	R	0h	POR module status Field values (others are reserved): 1'b0 - POR_IS_ACTIVE 1'b1 - POR_IS_RESET Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.136 MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL Register

14.2.1.1.2.2.136.1 MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL Register (Offset = 18110h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDA_MCU 1P8 Under/Over Voltage Monitors in POR (POKHV, POKLVA)

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Table 14-5365. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8110h

Figure 14-2670. MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5366. MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_UV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.137 MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL Register

14.2.1.1.2.2.137.1 MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL Register (Offset = 18114h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDA_MCU 1P8 Under/Over Voltage Monitors in POR (POKHV, POKLVA)

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Table 14-5367. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8114h

Figure 14-2671. MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5368. MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_OV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.138 MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL Register

14.2.1.1.2.2.138.1 MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL Register (Offset = 18118h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDD_CORE Under/Over Voltage Monitors in POR (POKLVB) and POK_VDD_CORE_UV

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Table 14-5369. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8118h

Figure 14-2672. MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5370. MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_UV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.139 MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL Register

14.2.1.1.2.2.139.1 MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL Register (Offset = 1811Ch) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDD_CORE Under/Over Voltage Monitors in POR (POKLVB) and POK_VDD_CORE_UV

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Table 14-5371. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 811Ch

Figure 14-2673. MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5372. MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_OV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.140 MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL Register

14.2.1.1.2.2.140.1 MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL Register (Offset = 18120h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDR_CORE Under/Over Voltage Monitor

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Table 14-5373. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8120h

Figure 14-2674. MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5374. MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_UV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.141 MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL Register

14.2.1.1.2.2.141.1 MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL Register (Offset = 18124h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDR_CORE Under/Over Voltage Monitor

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Table 14-5375. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8124h

Figure 14-2675. MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDR_CORE_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5376. MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_OV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.142 MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register

14.2.1.1.2.2.142.1 MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register (Offset = 18138h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VMON_CAP_MCU_GENERAL Under/Over Voltage Monitor

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Table 14-5377. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8138h

Figure 14-2676. MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5378. MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.143 MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register

14.2.1.1.2.2.143.1 MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register (Offset = 1813Ch) [reset = 80000000h]

Hysterisis, Threshold, and Control of VMON_CAP_MCU_GENERAL Under/Over Voltage Monitor

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Table 14-5379. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 813Ch

Figure 14-2677. MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5380. MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.144 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register

14.2.1.1.2.2.144.1 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register (Offset = 18140h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDSHV_MAIN_1P8 Under/Over Voltage Monitor

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Table 14-5381. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8140h

Figure 14-2678. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5382. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.145 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register

14.2.1.1.2.2.145.1 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register (Offset = 18144h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDSHV_MAIN_1P8 Under/Over Voltage Monitor

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Table 14-5383. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8144h

Figure 14-2679. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5384. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.146 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register

14.2.1.1.2.2.146.1 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register (Offset = 18148h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDSHV_MAIN_3P3 Under/Over Voltage Monitor

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Table 14-5385. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8148h

Figure 14-2680. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5386. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.147 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register

14.2.1.1.2.2.147.1 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register (Offset = 1814Ch) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDSHV_MAIN_3P3 Under/Over Voltage Monitor

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Table 14-5387. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 814Ch

Figure 14-2681. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET							
R/W							
0h	0h						

Table 14-5388. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.148 MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL Register

14.2.1.1.2.2.148.1 MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL Register (Offset = 18160h) [reset = 80000000h]

Hysterisis and Control of VDDA_PMIC_IN Under/Over Voltage Monitor

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Table 14-5389. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8160h

Figure 14-2682. MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL Name Register

31	30	29	28	27	26	25	24
POK_VDDA_PMIC_IN_CTRL_HYST_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5390. MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_PMIC_IN_CTRL_HYST_EN	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n
14:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.149 MCU_CTRL_MMRCFG0_RST_CTRL Register

14.2.1.1.2.2.149.1 MCU_CTRL_MMRCFG0_RST_CTRL Register (Offset = 18170h) [reset = 420FFFh]

Controls Reset Assertion and Propogation

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Table 14-5391. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8170h

Figure 14-2683. MCU_CTRL_MMRCFG0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	RST_CTRL_DM_WDT_RST_EN_Z	RESERVED				RST_CTRL_MCU_ESM_ERROR_RST_EN_Z	RST_CTRL_SMS_COLD_RESET_EN_Z
NONE	R/W	NONE				R/W	R/W
0h	1h	0h			0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				RST_CTRL_SW_MCU_WARMRST			
NONE				R/W			
0h				Fh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Fh				Fh			

Table 14-5392. MCU_CTRL_MMRCFG0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	RST_CTRL_DM_WDT_RST_EN_Z	R/W	1h	Block Reset from DM WDT propogating to MCU domain Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: mcu_chip1_rst_n
21:19	RESERVED	NONE	0h	Reserved
17	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z	R/W	1h	Block Reset of MCU by ESM Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: mcu_chip1_rst_n
16	RST_CTRL_SMS_COLD_RESET_EN_Z	R/W	0h	Block Reset of MCU by SMS Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: mcu_chip1_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	RST_CTRL_SW_MCU_WARMRST	R/W	Fh	Causes full device Warm Reset. This is a fault tolerant bitfield. Automatically resets to 4'b1111 after write. Field values (others are reserved): 4'b0110 - FORCE_RESET 4'b1111 - INACTIVE Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.150 MCU_CTRL_MMRCFG0_RST_STAT Register

14.2.1.1.2.2.150.1 MCU_CTRL_MMRCFG0_RST_STAT Register (Offset = 18174h) [reset = 0h]

Reset Status

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Table 14-5393. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8174h

Figure 14-2684. MCU_CTRL_MMRCFG0_RST_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MAIN_RESETSTATZ
NONE							R
0h							0h

Table 14-5394. MCU_CTRL_MMRCFG0_RST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MAIN_RESETSTATZ	R	0h	Status of Main Domain Reset: Field values (others are reserved): 1'b0 - BLOCKED 1'b1 - PROPOGATE Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.151 MCU_CTRL_MMRCFG0_RST_SRC Register

14.2.1.1.2.2.151.1 MCU_CTRL_MMRCFG0_RST_SRC Register (Offset = 18178h) [reset = 0h]

Captures Reason for Warm and Main Domain Power On Resets

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Table 14-5395. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8178h

Figure 14-2685. MCU_CTRL_MMRCFG0_RST_SRC Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR	RST_SRC_MAIN_ESM_ERROR	RESERVED					
R/W1TC	R/W1TC	NONE					
0h	0h	0h				0h	0h

23	22	21	20	19	18	17	16
	RST_SRC_DM_WDT_RST			RESERVED			RST_SRC_SW_MCU_WARMRST
	R/W1TC			NONE			R/W1TC
0h	0h	0h	0h	0h			0h

15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST	RST_SRC_COLD_OUT_RST	RESERVED			RST_SRC_DEBUG_RST
NONE		R/W1TC	R/W1TC	NONE			R/W1TC
0h		0h	0h	0h			0h

7	6	5	4	3	2	1	0
RESERVED	RST_SRC_IPOR_WAKE	RESERVED	RST_SRC_THERMAL_RST	RESERVED		RESERVED	RST_SRC_MCU_RESET_PIN
NONE	R/W1TC	NONE	R/W1TC	NONE		NONE	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5396. MCU_CTRL_MMRCFG0_RST_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR	R/W1TC	0h	Reset Caused by MCU ESM Error. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
30	RST_SRC_MAIN_ESM_ERROR	R/W1TC	0h	Reset Caused by Main ESM Error. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
29:26	RESERVED	NONE	0h	Reserved
22	RST_SRC_DM_WDT_RST	R/W1TC	0h	Watchdog Initiated Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST	R/W1TC	0h	Software Warm Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-5396. MCU_CTRL_MMRCFG0_RST_SRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RST_SRC_WARM_OUT_RST	R/W1TC	0h	SMS Warm Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
12	RST_SRC_COLD_OUT_RST	R/W1TC	0h	When set, indicates that a DMSC Cold reset occurred and reset either main or mcu domains (or both). Write 1 to clear this bit. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST	R/W1TC	0h	Debug Subsystem Initiated Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
7	RESERVED	NONE	0h	Reserved
6	RST_SRC_IPOR_WAKE	R/W1TC	0h	Wake Event Monitor Internal Power On Reset. Write 1 to Clear Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: por_boot_cfg_rst_n
5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST	R/W1TC	0h	Thermal Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
3	RESERVED	NONE	0h	Reserved
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN	R/W1TC	0h	Reset Caused by MCU Reset Pin. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n

14.2.1.1.2.2.152 MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL Register

14.2.1.1.2.2.152.1 MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL Register (Offset = 18190h) [reset = 0h]

Controls the voltage glitch detector circuit monitoring the VDD_CORE voltage domain

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Table 14-5397. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8190h

Figure 14-2686. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL Name Register

31	30	29	28	27	26	25	24
VDD_CORE_GLDTC_CTRL_PWDB	VDD_CORE_GLDTC_CTRL_RSTB	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED					VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL					
NONE		R/W					
0h		0h					

Table 14-5398. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VDD_CORE_GLDTC_CTRL_PWDB	R/W	0h	Power down - active low. Field values (others are reserved): 1'b0 - PWRDN 1'b1 - PWRUP Reset Source: mcu_chip1_rst_n
30	VDD_CORE_GLDTC_CTRL_RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must be not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. Field values (others are reserved): 1'b0 - RESET 1'b1 - ACTIVE Reset Source: mcu_chip1_rst_n
29:19	RESERVED	NONE	0h	Reserved
18:16	VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL	R/W	0h	Selects the glitch detect low-pass filter bandwidth Field values (others are reserved): 3'b000 - BW_150KHz 3'b001 - BW_125KHz 3'b010 - BW_100KHz 3'b011 - BW_80KHz 3'b100 - BW_60KHz 3'b101 - BW_45KHz 3'b110 - BW_30KHz 3'b111 - BW_15KHz Reset Source: mcu_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-5398. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL	R/W	0h	Selects the high voltage glitch threshold as a percentage of the monitored voltage Field values (others are reserved): 6'b000000 - PCT_VDD_93P5 6'b000001 - PCT_VDD_94 6'b000010 - PCT_VDD_94P5 6'b000011 - PCT_VDD_95 6'b000100 - PCT_VDD_95P5 6'b000101 - PCT_VDD_96 6'b000110 - PCT_VDD_96P5 6'b000111 - PCT_VDD_97 6'b001000 - PCT_VDD_97P5 6'b001001 - PCT_VDD_98 6'b001010 - PCT_VDD_98P5 6'b001011 - PCT_VDD_99 6'b001100 - PCT_VDD_99P5 6'b001101 - PCT_VDD_100 6'b001110 - PCT_VDD_100P5 6'b001111 - PCT_VDD_101 6'b010000 - PCT_VDD_101P5 6'b010001 - PCT_VDD_102 6'b010010 - PCT_VDD_102P5 6'b010011 - PCT_VDD_103 6'b010100 - PCT_VDD_103P5 6'b010101 - PCT_VDD_104 6'b010110 - PCT_VDD_104P5 6'b010111 - PCT_VDD_105 6'b011000 - PCT_VDD_105P5 6'b011001 - PCT_VDD_106 6'b011010 - PCT_VDD_106P5 6'b011011 - PCT_VDD_107 6'b011100 - PCT_VDD_107P5 6'b011101 - PCT_VDD_108 6'b011110 - PCT_VDD_108P5 6'b011111 - PCT_VDD_109 6'b100000 - PCT_VDD_109P5 6'b100001 - PCT_VDD_110 6'b100010 - PCT_VDD_111 6'b100011 - PCT_VDD_112 6'b100100 - PCT_VDD_113 6'b100101 - PCT_VDD_114 6'b100110 - PCT_VDD_115 6'b100111 - PCT_VDD_116 6'b101000 - PCT_VDD_117 6'b101001 - PCT_VDD_118 6'b101010 - PCT_VDD_119 6'b101011 - PCT_VDD_120 6'b101100 - PCT_VDD_121 6'b101101 - PCT_VDD_122 6'b101110 - PCT_VDD_123 6'b101111 - PCT_VDD_124 6'b110000 - PCT_VDD_125 6'b110001 - PCT_VDD_126 6'b110010 - PCT_VDD_127 6'b110011 - PCT_VDD_128 6'b110100 - PCT_VDD_129 6'b110101 - PCT_VDD_130 6'b110110 - PCT_VDD_131 6'b110111 - PCT_VDD_132 6'b111000 - PCT_VDD_133 6'b111001 - PCT_VDD_134 6'b111010 - PCT_VDD_135 6'b111011 - PCT_VDD_136 6'b111100 - PCT_VDD_137 6'b111101 - PCT_VDD_138 6'b111110 - PCT_VDD_139 6'b111111 - PCT_VDD_140 Reset Source: mcu_chip1_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-5398. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL	R/W	0h	Selects the low voltage glitch threshold as a percentage of the monitored voltage Field values (others are reserved): 6'b000000 - PCT_VDD_106P5 6'b000001 - PCT_VDD_106 6'b000010 - PCT_VDD_105P5 6'b000011 - PCT_VDD_105 6'b000100 - PCT_VDD_104P5 6'b000101 - PCT_VDD_104 6'b000110 - PCT_VDD_103P5 6'b000111 - PCT_VDD_103 6'b001000 - PCT_VDD_102P5 6'b001001 - PCT_VDD_102 6'b001010 - PCT_VDD_101P5 6'b001011 - PCT_VDD_101 6'b001100 - PCT_VDD_100P5 6'b001101 - PCT_VDD_100 6'b001110 - PCT_VDD_99P5 6'b001111 - PCT_VDD_99 6'b010000 - PCT_VDD_98P5 6'b010001 - PCT_VDD_98 6'b010010 - PCT_VDD_97P5 6'b010011 - PCT_VDD_97 6'b010100 - PCT_VDD_96P5 6'b010101 - PCT_VDD_96 6'b010110 - PCT_VDD_95P5 6'b010111 - PCT_VDD_95 6'b011000 - PCT_VDD_94P5 6'b011001 - PCT_VDD_94 6'b011010 - PCT_VDD_93P5 6'b011011 - PCT_VDD_93 6'b011100 - PCT_VDD_92P5 6'b011101 - PCT_VDD_92 6'b011110 - PCT_VDD_91P5 6'b011111 - PCT_VDD_91 6'b100000 - PCT_VDD_90P5 6'b100001 - PCT_VDD_90 6'b100010 - PCT_VDD_89 6'b100011 - PCT_VDD_88 6'b100100 - PCT_VDD_87 6'b100101 - PCT_VDD_86 6'b100110 - PCT_VDD_85 6'b100111 - PCT_VDD_84 6'b101000 - PCT_VDD_83 6'b101001 - PCT_VDD_82 6'b101010 - PCT_VDD_81 6'b101011 - PCT_VDD_80 6'b101100 - PCT_VDD_79 6'b101101 - PCT_VDD_78 6'b101110 - PCT_VDD_77 6'b101111 - PCT_VDD_76 6'b110000 - PCT_VDD_75 6'b110001 - PCT_VDD_74 6'b110010 - PCT_VDD_73 6'b110011 - PCT_VDD_72 6'b110100 - PCT_VDD_71 6'b110101 - PCT_VDD_70 6'b110110 - PCT_VDD_69 6'b110111 - PCT_VDD_68 6'b111000 - PCT_VDD_67 6'b111001 - PCT_VDD_66 6'b111010 - PCT_VDD_65 6'b111011 - PCT_VDD_64 6'b111100 - PCT_VDD_63 6'b111101 - PCT_VDD_62 6'b111110 - PCT_VDD_61 6'b111111 - PCT_VDD_60 Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.153 MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT Register

14.2.1.1.2.2.153.1 MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT Register (Offset = 181B0h) [reset = 0h]

Shows the status of the voltage glitch detector circuit monitoring the VDD_CORE voltage domain

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Table 14-5399. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 81B0h

Figure 14-2687. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG
NONE							R
0h							0h

Table 14-5400. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG	R	0h	High voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. Field values (others are reserved): 1'b0 - HV_UNKNOWN (not detected) 1'b1 - HV_DETECTED Reset Source: mcu_chip1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG	R	0h	Low voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. Field values (others are reserved): 1'b0 - LV_UNKNOWN (not detected) 1'b1 - LV_DETECTED Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.154 MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL Register

14.2.1.1.2.2.154.1 MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL Register (Offset = 18200h) [reset = 2001Fh]

Configures PRG_PP_0 - Fixed POKs (In POR, POKSA, and POK_VDD_CORE_OV)

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Table 14-5401. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8200h

Figure 14-2688. MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PRG_PP_0_CTRL_DEGLITCH_SEL	
NONE						R/W	
0h						2h	
15	14	13	12	11	10	9	8
PRG_PP_0_CTRL_POK_EN_SEL	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN
NONE			R/W	R/W	R/W	R/W	R/W
0h			1h	1h	1h	1h	1h

Table 14-5402. MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_0_CTRL_DEGLITCH_SEL	R/W	2h	Deglitch period for PRG_PP1 POKs (microseconds) Field values (others are reserved): 2'b00 - DG_5_US 2'b01 - DG_10_US 2'b10 - DG_15_US 2'b11 - DG_20_US Reset Source: mod_por_rst_n
15	PRG_PP_0_CTRL_POK_EN_SEL	R/W	0h	Selects source of POK controls Field values (others are reserved): 1'b0 - TIEOFFS 1'b1 - PRG_PP0_CTRL_REG Reset Source: mod_por_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN	R/W	1h	Enable VDDA_PMIC_IN undervoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
3	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN	R/W	1h	Enable VDD_MCU overvoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n

Table 14-5402. MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN	R/W	1h	Enable VDD_MCU undervoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
1	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN	R/W	1h	Enable 1.8V VDDA_MCU overvoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
0	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN	R/W	1h	Enable 1.8V VDDA_MCU undervoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n

14.2.1.1.2.2.155 MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL Register

14.2.1.1.2.2.155.1 MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL Register (Offset = 18208h) [reset = 2007Fh]

Configures PRG_PP_1 - Ping-Pong Capable POKs

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Table 14-5403. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8208h

Figure 14-2689. MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PRG_PP_1_CTRL_POK_PP_EN	RESERVED	PRG_PP_1_CTRL_DEGLITCH_SEL	
NONE				R/W	NONE	R/W	
0h				0h	0h	2h	
15	14	13	12	11	10	9	8
PRG_PP_1_CTRL_POK_EN_SEL	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL			PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL
R/W	R/W	R/W	R/W	R/W			R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN			PRG_PP_1_CTRL_POK_VDDR_CORE_EN
NONE	R/W	R/W	R/W	R/W			R/W
0h	1h	1h	1h	1h	1h	1h	1h

Table 14-5404. MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	PRG_PP_1_CTRL_POK_PP_EN	R/W	0h	POK ping-pong enable. When set, POKs with their ov_sel option set to UV_OR_PINGPONG are automatically cycled between UV and OV detection (ping-pong). POKs with ov_sel selecting OV are unaffected by this bit. Field values (others are reserved): 1'b0 - UV_FIXED 1'b1 - UV_PINGPONG_OV Reset Source: mod_por_rst_n
18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_1_CTRL_DEGLITCH_SEL	R/W	2h	Deglitch period for PRG_PP1 POKs (microseconds) Field values (others are reserved): 2'b00 - DG_5_US 2'b01 - DG_10_US 2'b10 - DG_15_US 2'b11 - DG_20_US Reset Source: mod_por_rst_n
15	PRG_PP_1_CTRL_POK_EN_SEL	R/W	0h	Selects source of POK controls Field values (others are reserved): 1'b0 - TIEOFFS 1'b1 - PRG_PP0_CTRL_REG Reset Source: mod_por_rst_n

Table 14-5404. MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL	R/W	0h	POK_VDDS_DDRIO mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
13	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL	R/W	0h	POK_VDDSHV_MAIN_3P3 mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
12	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL	R/W	0h	POK_VDDSHV_MAIN_1P8 mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
11	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL	R/W	0h	POK_VMON_CAP_MCU_GENERAL mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
8	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL	R/W	0h	POK_VDDR_CORE mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
7	RESERVED	NONE	0h	Reserved
6	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN	R/W	1h	Enable POK_VDDS_DDRIO (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
5	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN	R/W	1h	Enable POK_VDDSHV_MAIN_3P3 (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
4	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN	R/W	1h	Enable POK_VDDSHV_MAIN_1P8 (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
3	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN	R/W	1h	Enable POK_VMON_CAP_MCU_GENERAL (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
0	PRG_PP_1_CTRL_POK_VDDR_CORE_EN	R/W	1h	Enable POK_VDDR_CORE (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n

14.2.1.1.2.2.156 MCU_CTRL_MMRCFG0_CLKGATE_CTRL Register

14.2.1.1.2.2.156.1 MCU_CTRL_MMRCFG0_CLKGATE_CTRL Register (Offset = 18280h) [reset = 0h]

Controls the power clock gating feature of MCU domain modules and busses

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Table 14-5405. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 8280h

Figure 14-2690. MCU_CTRL_MMRCFG0_CLKGATE_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>CLKGATE_CTRL_WKUP_SAFE_CBA_NOGATE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-5406. MCU_CTRL_MMRCFG0_CLKGATE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLKGATE_CTRL_WKUP_SAFE_CBA_NOGATE	R/W	0h	WKUP domain CBASS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

14.2.1.1.2.2.157 MCU_CTRL_MMRCFG0_LOCK6_KICK0 Register

14.2.1.1.2.2.157.1 MCU_CTRL_MMRCFG0_LOCK6_KICK0 Register (Offset = 19008h) [reset = 0h]

- KICK0 component

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Table 14-5407. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 9008h

Figure 14-2691. MCU_CTRL_MMRCFG0_LOCK6_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0							
R/W							
0h							

Table 14-5408. MCU_CTRL_MMRCFG0_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.158 MCU_CTRL_MMRCFG0_LOCK6_KICK1 Register

14.2.1.1.2.2.158.1 MCU_CTRL_MMRCFG0_LOCK6_KICK1 Register (Offset = 1900Ch) [reset = 0h]

- KICK1 component

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Table 14-5409. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 900Ch

Figure 14-2692. MCU_CTRL_MMRCFG0_LOCK6_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1							
R/W							
0h							

Table 14-5410. MCU_CTRL_MMRCFG0_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.159 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0_READONLY Register

14.2.1.1.2.2.159.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0_READONLY Register (Offset = 19100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5411. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 9100h

Figure 14-2693. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0_READONLY							
R							
0h							

Table 14-5412. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.160 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2_READONLY Register

14.2.1.1.2.2.160.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2_READONLY Register (Offset = 19108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5413. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 9108h

Figure 14-2694. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2_READONLY							
R							
0h							

Table 14-5414. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.161 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3_READONLY Register

14.2.1.1.2.2.161.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3_READONLY Register (Offset = 1910Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-5415. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 910Ch

Figure 14-2695. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3_READONLY							
R							
0h							

Table 14-5416. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.162 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4_READONLY Register

14.2.1.1.2.2.162.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4_READONLY Register (Offset = 19110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5417. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 9110h

Figure 14-2696. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4_READONLY							
R							
0h							

Table 14-5418. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.163 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5_READONLY Register

14.2.1.1.2.2.163.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5_READONLY Register (Offset = 19114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5419. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 9114h

Figure 14-2697. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5_READONLY							
R							
0h							

Table 14-5420. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.164 MCU_CTRL_MMRCFG0_POR_CTRL_PROXY Register

14.2.1.1.2.2.164.1 MCU_CTRL_MMRCFG0_POR_CTRL_PROXY Register (Offset = 1A000h) [reset = 10h]

Configures POR module reset behavior and allows software to directly override POR comparator outputs.

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Table 14-5421. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A000h

Figure 14-2698. MCU_CTRL_MMRCFG0_POR_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED		POR_CTRL_OVRD_SET5_PROXY	POR_CTRL_OVRD_SET4_PROXY	POR_CTRL_OVRD_SET3_PROXY	POR_CTRL_OVRD_SET2_PROXY	POR_CTRL_OVRD_SET1_PROXY	POR_CTRL_OVRD_SET0_PROXY
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED		POR_CTRL_OVRD5_PROXY	POR_CTRL_OVRD4_PROXY	POR_CTRL_OVRD3_PROXY	POR_CTRL_OVRD2_PROXY	POR_CTRL_OVRD1_PROXY	POR_CTRL_OVRD0_PROXY
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POR_CTRL_TRIM_SEL_PROXY	RESERVED		POR_CTRL_MASK_HHV_PROXY	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		1h	0h			

Table 14-5422. MCU_CTRL_MMRCFG0_POR_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	POR_CTRL_OVRD_SET5_PROXY	R/W	0h	Override value when override is active, for RESERVED output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
28	POR_CTRL_OVRD_SET4_PROXY	R/W	0h	Override value when override is active, for POKLVB output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
27	POR_CTRL_OVRD_SET3_PROXY	R/W	0h	Override value when override is active, for POKLVA output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
26	POR_CTRL_OVRD_SET2_PROXY	R/W	0h	Override value when override is active, for POKHV output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n

Table 14-5422. MCU_CTRL_MMRCFG0_POR_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	POR_CTRL_OVRD_SET1_PROXY	R/W	0h	Override value when override is active, for BGOK output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
24	POR_CTRL_OVRD_SET0_PROXY	R/W	0h	Override value when override is active, for PORHV output. Field values (others are reserved): 1'b0 - OVERRIDE_TO_0 1'b1 - OVERRIDE_TO_1 Reset Source: mod_por_rst_n
23:22	RESERVED	NONE	0h	Reserved
21	POR_CTRL_OVRD5_PROXY	R/W	0h	Enables override of RESERVED output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
20	POR_CTRL_OVRD4_PROXY	R/W	0h	Enables override of POKLVB output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
19	POR_CTRL_OVRD3_PROXY	R/W	0h	Enables override of POKLVA output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
18	POR_CTRL_OVRD2_PROXY	R/W	0h	Enables override of POKHV output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
17	POR_CTRL_OVRD1_PROXY	R/W	0h	Enables override of BGOK output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
16	POR_CTRL_OVRD0_PROXY	R/W	0h	Enables override of PORHV output Field values (others are reserved): 1'b0 - NORMAL_OPERATION 1'b1 - OVERRIDE_OUTPUT Reset Source: mod_por_rst_n
15:8	RESERVED	NONE	0h	Reserved
7	POR_CTRL_TRIM_SEL_PROXY	R/W	0h	POR Trim Select - Fixed value or from POR_BANDGAP_CTRL and POR_POKxxx_CTRL registers MMRs Field values (others are reserved): 1'b0 - FIXED_TRIM 1'b1 - MMR_TRIM Reset Source: mod_por_rst_n
6:5	RESERVED	NONE	0h	Reserved
4	POR_CTRL_MASK_HHV_PROXY	R/W	1h	Mask HHV/SOC_PORz outputs when applying new trim values Field values (others are reserved): 1'b0 - UNMASK 1'b1 - MASK Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.165 MCU_CTRL_MMRCFG0_POR_STAT_PROXY Register

14.2.1.1.2.2.165.1 MCU_CTRL_MMRCFG0_POR_STAT_PROXY Register (Offset = 1A004h) [reset = 0h]

Shows POR module status

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Table 14-5423. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A004h

Figure 14-2699. MCU_CTRL_MMRCFG0_POR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							POR_STAT_BGOK_PROXY
NONE							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			POR_STAT_SOC_POR_PROXY	RESERVED			
NONE			R	NONE			
0h			0h	0h			

Table 14-5424. MCU_CTRL_MMRCFG0_POR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	POR_STAT_BGOK_PROXY	R	0h	Bandgap OK status Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - OK Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	POR_STAT_SOC_POR_PROXY	R	0h	POR module status Field values (others are reserved): 1'b0 - POR_IS_ACTIVE 1'b1 - POR_IS_RESET Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.166 MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register

14.2.1.1.2.2.166.1 MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register (Offset = 1A110h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDA_MCU 1P8 Under/Over Voltage Monitors in POR (POKHV, POKLVA)

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Table 14-5425. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A110h

Figure 14-2700. MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5426. MCU_CTRL_MMRCFG0_POK_VDDA_MCU_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_UV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.167 MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register

14.2.1.1.2.2.167.1 MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register (Offset = 1A114h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDA_MCU 1P8 Under/Over Voltage Monitors in POR (POKHV, POKLVA)

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Table 14-5427. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A114h

Figure 14-2701. MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_MCU_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5428. MCU_CTRL_MMRCFG0_POK_VDDA_MCU_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_MCU_OV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDA_MCU_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.168 MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL_PROXY Register

14.2.1.1.2.2.168.1 MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL_PROXY Register (Offset = 1A118h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDD_CORE Under/Over Voltage Monitors in POR (POKLVB) and POK_VDD_CORE_UV

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Table 14-5429. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A118h

Figure 14-2702. MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5430. MCU_CTRL_MMRCFG0_POK_VDD_CORE_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_UV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.169 MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL_PROXY Register

14.2.1.1.2.2.169.1 MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL_PROXY Register (Offset = 1A11Ch) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDD_CORE Under/Over Voltage Monitors in POR (POKLVB) and POK_VDD_CORE_UV

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Table 14-5431. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A11Ch

Figure 14-2703. MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDD_CORE_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5432. MCU_CTRL_MMRCFG0_POK_VDD_CORE_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDD_CORE_OV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDD_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.170 MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register

14.2.1.1.2.2.170.1 MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register (Offset = 1A120h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDR_CORE Under/Over Voltage Monitor

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Table 14-5433. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A120h

Figure 14-2704. MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>POK_VDDR_CORE_UV_CTRL_HYST_EN_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET_PROXY</td><td colspan="7"></td></tr>
<tr><td>R/W</td><td colspan="7"></td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-5434. MCU_CTRL_MMRCFG0_POK_VDDR_CORE_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_UV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.171 MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register

14.2.1.1.2.2.171.1 MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register (Offset = 1A124h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDR_CORE Under/Over Voltage Monitor

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Table 14-5435. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A124h

Figure 14-2705. MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>POK_VDDR_CORE_OV_CTRL_HYST_EN_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET_PROXY</td><td colspan="7"></td></tr>
<tr><td>R/W</td><td colspan="7"></td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-5436. MCU_CTRL_MMRCFG0_POK_VDDR_CORE_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDR_CORE_OV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDR_CORE_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.172 MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register

14.2.1.1.2.2.172.1 MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register (Offset = 1A138h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VMON_CAP_MCU_GENERAL Under/Over Voltage Monitor

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Table 14-5437. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A138h

Figure 14-2706. MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5438. MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.173 MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register

14.2.1.1.2.2.173.1 MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register (Offset = 1A13Ch) [reset = 80000000h]

Hysterisis, Threshold, and Control of VMON_CAP_MCU_GENERAL Under/Over Voltage Monitor

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Table 14-5439. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A13Ch

Figure 14-2707. MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5440. MCU_CTRL_MMRCFG0_POK_VMON_CAP_MCU_GENERAL_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VMON_CAP_MCU_GENERAL_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.174 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register

14.2.1.1.2.2.174.1 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register (Offset = 1A140h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDSHV_MAIN_1P8 Under/Over Voltage Monitor

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Table 14-5441. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A140h

Figure 14-2708. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5442. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_UV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.175 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register

14.2.1.1.2.2.175.1 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register (Offset = 1A144h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDSHV_MAIN_1P8 Under/Over Voltage Monitor

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Table 14-5443. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A144h

Figure 14-2709. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5444. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_1P8_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_1P8_OV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_1P8_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.176 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register

14.2.1.1.2.2.176.1 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register (Offset = 1A148h) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDSHV_MAIN_3P3 Under/Over Voltage Monitor

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Table 14-5445. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A148h

Figure 14-2710. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5446. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_UV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_UV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_UV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.177 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register

14.2.1.1.2.2.177.1 MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register (Offset = 1A14Ch) [reset = 80000000h]

Hysterisis, Threshold, and Control of VDDSHV_MAIN_3P3 Under/Over Voltage Monitor

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Table 14-5447. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A14Ch

Figure 14-2711. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET_PROXY							
R/W							
0h	0h						

Table 14-5448. MCU_CTRL_MMRCFG0_POK_VDDSHV_MAIN_3P3_OV_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDSHV_MAIN_3P3_OV_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7	POK_VDDSHV_MAIN_3P3_OV_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n

14.2.1.1.2.2.178 MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register

14.2.1.1.2.2.178.1 MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register (Offset = 1A160h) [reset = 80000000h]

Hysterisis and Control of VDDA_PMIC_IN Under/Over Voltage Monitor

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Table 14-5449. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A160h

Figure 14-2712. MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
POK_VDDA_PMIC_IN_CTRL_HYST_EN_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5450. MCU_CTRL_MMRCFG0_POK_VDDA_PMIC_IN_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_VDDA_PMIC_IN_CTRL_HYST_EN_PROXY	R/W	1h	Enable POK hysteresis Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	POK_VDDA_PMIC_IN_CTRL_OVER_VOLT_DET_PROXY	R/W	0h	Over / under voltage detection mode Field values (others are reserved): 1'b0 - UNDERVOLTAGE_MODE 1'b1 - OVERVOLTAGE_MODE Reset Source: mod_por_rst_n
14:0	RESERVED	NONE	0h	Reserved

14.2.1.1.2.2.179 MCU_CTRL_MMRCFG0_RST_CTRL_PROXY Register

14.2.1.1.2.2.179.1 MCU_CTRL_MMRCFG0_RST_CTRL_PROXY Register (Offset = 1A170h) [reset = 420FFFh]

Controls Reset Assertion and Propogation

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Table 14-5451. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A170h

Figure 14-2713. MCU_CTRL_MMRCFG0_RST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	RST_CTRL_DM_WDT_RST_EN_Z_PROXY	RESERVED			RST_CTRL_MCU_RESET_ISO_DONE_Z_PROXY	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z_PROXY	RST_CTRL_SMS_COLD_RESET_EN_Z_PROXY
NONE	R/W	NONE			R/W	R/W	R/W
0h	1h	0h			0h	1h	0h
15	14	13	12	11	10	9	8
RESERVED				RST_CTRL_SW_MCU_WARMRST_PROXY			
NONE				R/W			
0h				Fh			
7	6	5	4	3	2	1	0
Fh				Fh			

Table 14-5452. MCU_CTRL_MMRCFG0_RST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	RST_CTRL_DM_WDT_RST_EN_Z_PROXY	R/W	1h	Block Reset from DM WDT propogating to MCU domain Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: mcu_chip1_rst_n
21:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MCU_RESET_ISO_DONE_Z_PROXY	R/W	0h	Block Main Domain Warm Reset MCU domain Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: mcu_chip1_rst_n
17	RST_CTRL_MCU_ESM_ERROR_RST_EN_Z_PROXY	R/W	1h	Block Reset of MCU by ESM Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: mcu_chip1_rst_n
16	RST_CTRL_SMS_COLD_RESET_EN_Z_PROXY	R/W	0h	Block Reset of MCU by SMS Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: mcu_chip1_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:8	RST_CTRL_SW_MCU_WARMRST_PROXY	R/W	Fh	Causes MAIN Domain Warm Reset. This is a fault tolerant bitfield. Automatically resets to 4'b1111 after write. Field values (others are reserved): 4'b0110 - FORCE_RESET 4'b1111 - INACTIVE Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.180 MCU_CTRL_MMRCFG0_RST_STAT_PROXY Register

14.2.1.1.2.2.180.1 MCU_CTRL_MMRCFG0_RST_STAT_PROXY Register (Offset = 1A174h) [reset = 0h]

Reset Status

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Table 14-5453. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A174h

Figure 14-2714. MCU_CTRL_MMRCFG0_RST_STAT_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>RST_STAT_MAIN_RESETSTATZ_PROXY</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-5454. MCU_CTRL_MMRCFG0_RST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MAIN_RESETSTATZ_PROXY	R	0h	Status of Main Domain Reset: Field values (others are reserved): 1'b0 - BLOCKED 1'b1 - PROPOGATE Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.181 MCU_CTRL_MMRCFG0_RST_SRC_PROXY Register

14.2.1.1.2.2.181.1 MCU_CTRL_MMRCFG0_RST_SRC_PROXY Register (Offset = 1A178h) [reset = 0h]

Captures Reason for Warm and Main Domain Power On Resets

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Table 14-5455. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A178h

Figure 14-2715. MCU_CTRL_MMRCFG0_RST_SRC_PROXY Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR_PROXY	RST_SRC_MAIN_ESM_ERROR_PROXY	RESERVED					
R/W1TC	R/W1TC	NONE					
0h	0h	0h				0h	0h

23	22	21	20	19	18	17	16
	RST_SRC_DM_WDT_RST_PROXY			RESERVED			RST_SRC_SW_MCU_WARMRST_PROXY
	R/W1TC			NONE			R/W1TC
0h	0h	0h	0h	0h			0h

15	14	13	12	11	10	9	8
RESERVED		RST_SRC_WARM_OUT_RST_PROXY	RST_SRC_COLD_OUT_RST_PROXY	RESERVED			RST_SRC_DEBUG_RST_PROXY
NONE		R/W1TC	R/W1TC	NONE			R/W1TC
0h		0h	0h	0h			0h

7	6	5	4	3	2	1	0
RESERVED	RST_SRC_IPOR_WAKE_PROXY	RESERVED	RST_SRC_THERMAL_RST_PROXY	RESERVED		RESERVED	RST_SRC_MCU_RESET_PIN_PROXY
NONE	R/W1TC	NONE	R/W1TC	NONE		NONE	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-5456. MCU_CTRL_MMRCFG0_RST_SRC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR_PROXY	R/W1TC	0h	Reset Caused by MCU ESM Error. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
30	RST_SRC_MAIN_ESM_ERROR_PROXY	R/W1TC	0h	Reset Caused by Main ESM Error. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
29:26	RESERVED	NONE	0h	Reserved
22	RST_SRC_DM_WDT_RST_PROXY	R/W1TC	0h	Watchdog Initiated Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST_PROXY	R/W1TC	0h	Software Warm Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-5456. MCU_CTRL_MMRCFG0_RST_SRC_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RST_SRC_WARM_OUT_RST_PROXY	R/W1TC	0h	SMS Warm Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
12	RST_SRC_COLD_OUT_RST_PROXY	R/W1TC	0h	When set, indicates that a DMSC Cold reset occurred and reset either main or mcu domains (or both). Write 1 to clear this bit. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST_PROXY	R/W1TC	0h	Debug Subsystem Initiated Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
7	RESERVED	NONE	0h	Reserved
6	RST_SRC_IPOR_WAKE_PROXY	R/W1TC	0h	Wake Event Monitor Internal Power On Reset. Write 1 to Clear Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: por_boot_cfg_rst_n
5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST_PROXY	R/W1TC	0h	Thermal Reset. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n
3	RESERVED	NONE	0h	Reserved
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN_PROXY	R/W1TC	0h	Reset Caused by MCU Reset Pin. Write 1 to Clear. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: mod_por_rst_n

14.2.1.1.2.2.182 MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL_PROXY Register

14.2.1.1.2.2.182.1 MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL_PROXY Register (Offset = 1A190h) [reset = 0h]

Controls the voltage glitch detector circuit monitoring the VDD_CORE voltage domain

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Table 14-5457. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A190h

Figure 14-2716. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
VDD_CORE_GLDTC_CTRL_PWDB_PROXY	VDD_CORE_GLDTC_CTRL_RSTB_PROXY	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED					VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL_PROXY		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL_PROXY					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED		VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL_PROXY					
NONE		R/W					
0h		0h					

Table 14-5458. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VDD_CORE_GLDTC_CTRL_PWDB_PROXY	R/W	0h	Power down - active low. Field values (others are reserved): 1'b0 - PWRDN 1'b1 - PWRUP Reset Source: mcu_chip1_rst_n
30	VDD_CORE_GLDTC_CTRL_RSTB_PROXY	R/W	0h	Reset - active low. To ensure proper operation, rstb must be not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. Field values (others are reserved): 1'b0 - RESET 1'b1 - ACTIVE Reset Source: mcu_chip1_rst_n
29:19	RESERVED	NONE	0h	Reserved
18:16	VDD_CORE_GLDTC_CTRL_LP_FILTER_SEL_PROXY	R/W	0h	Selects the glitch detect low-pass filter bandwidth Field values (others are reserved): 3'b000 - BW_150KHz 3'b001 - BW_125KHz 3'b010 - BW_100KHz 3'b011 - BW_80KHz 3'b100 - BW_60KHz 3'b101 - BW_45KHz 3'b110 - BW_30KHz 3'b111 - BW_15KHz Reset Source: mcu_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved

Table 14-5458. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	VDD_CORE_GLDTC_CTRL_THRESH_HI_SEL_PROXY	R/W	0h	Selects the high voltage glitch threshold as a percentage of the monitored voltage Field values (others are reserved): 6'b000000 - PCT_VDD_93P5 6'b000001 - PCT_VDD_94 6'b000010 - PCT_VDD_94P5 6'b000011 - PCT_VDD_95 6'b000100 - PCT_VDD_95P5 6'b000101 - PCT_VDD_96 6'b000110 - PCT_VDD_96P5 6'b000111 - PCT_VDD_97 6'b001000 - PCT_VDD_97P5 6'b001001 - PCT_VDD_98 6'b001010 - PCT_VDD_98P5 6'b001011 - PCT_VDD_99 6'b001100 - PCT_VDD_99P5 6'b001101 - PCT_VDD_100 6'b001110 - PCT_VDD_100P5 6'b001111 - PCT_VDD_101 6'b010000 - PCT_VDD_101P5 6'b010001 - PCT_VDD_102 6'b010010 - PCT_VDD_102P5 6'b010011 - PCT_VDD_103 6'b010100 - PCT_VDD_103P5 6'b010101 - PCT_VDD_104 6'b010110 - PCT_VDD_104P5 6'b010111 - PCT_VDD_105 6'b011000 - PCT_VDD_105P5 6'b011001 - PCT_VDD_106 6'b011010 - PCT_VDD_106P5 6'b011011 - PCT_VDD_107 6'b011100 - PCT_VDD_107P5 6'b011101 - PCT_VDD_108 6'b011110 - PCT_VDD_108P5 6'b011111 - PCT_VDD_109 6'b100000 - PCT_VDD_109P5 6'b100001 - PCT_VDD_110 6'b100010 - PCT_VDD_111 6'b100011 - PCT_VDD_112 6'b100100 - PCT_VDD_113 6'b100101 - PCT_VDD_114 6'b100110 - PCT_VDD_115 6'b100111 - PCT_VDD_116 6'b101000 - PCT_VDD_117 6'b101001 - PCT_VDD_118 6'b101010 - PCT_VDD_119 6'b101011 - PCT_VDD_120 6'b101100 - PCT_VDD_121 6'b101101 - PCT_VDD_122 6'b101110 - PCT_VDD_123 6'b101111 - PCT_VDD_124 6'b110000 - PCT_VDD_125 6'b110001 - PCT_VDD_126 6'b110010 - PCT_VDD_127 6'b110011 - PCT_VDD_128 6'b110100 - PCT_VDD_129 6'b110101 - PCT_VDD_130 6'b110110 - PCT_VDD_131 6'b110111 - PCT_VDD_132 6'b111000 - PCT_VDD_133 6'b111001 - PCT_VDD_134 6'b111010 - PCT_VDD_135 6'b111011 - PCT_VDD_136 6'b111100 - PCT_VDD_137 6'b111101 - PCT_VDD_138 6'b111110 - PCT_VDD_139 6'b111111 - PCT_VDD_140 Reset Source: mcu_chip1_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-5458. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VDD_CORE_GLDTC_CTRL_THRESH_LO_SEL_PROXY	R/W	0h	Selects the low voltage glitch threshold as a percentage of the monitored voltage Field values (others are reserved): 6'b000000 - PCT_VDD_106P5 6'b000001 - PCT_VDD_106 6'b000010 - PCT_VDD_105P5 6'b000011 - PCT_VDD_105 6'b000100 - PCT_VDD_104P5 6'b000101 - PCT_VDD_104 6'b000110 - PCT_VDD_103P5 6'b000111 - PCT_VDD_103 6'b001000 - PCT_VDD_102P5 6'b001001 - PCT_VDD_102 6'b001010 - PCT_VDD_101P5 6'b001011 - PCT_VDD_101 6'b001100 - PCT_VDD_100P5 6'b001101 - PCT_VDD_100 6'b001110 - PCT_VDD_99P5 6'b001111 - PCT_VDD_99 6'b010000 - PCT_VDD_98P5 6'b010001 - PCT_VDD_98 6'b010010 - PCT_VDD_97P5 6'b010011 - PCT_VDD_97 6'b010100 - PCT_VDD_96P5 6'b010101 - PCT_VDD_96 6'b010110 - PCT_VDD_95P5 6'b010111 - PCT_VDD_95 6'b011000 - PCT_VDD_94P5 6'b011001 - PCT_VDD_94 6'b011010 - PCT_VDD_93P5 6'b011011 - PCT_VDD_93 6'b011100 - PCT_VDD_92P5 6'b011101 - PCT_VDD_92 6'b011110 - PCT_VDD_91P5 6'b011111 - PCT_VDD_91 6'b100000 - PCT_VDD_90P5 6'b100001 - PCT_VDD_90 6'b100010 - PCT_VDD_89 6'b100011 - PCT_VDD_88 6'b100100 - PCT_VDD_87 6'b100101 - PCT_VDD_86 6'b100110 - PCT_VDD_85 6'b100111 - PCT_VDD_84 6'b101000 - PCT_VDD_83 6'b101001 - PCT_VDD_82 6'b101010 - PCT_VDD_81 6'b101011 - PCT_VDD_80 6'b101100 - PCT_VDD_79 6'b101101 - PCT_VDD_78 6'b101110 - PCT_VDD_77 6'b101111 - PCT_VDD_76 6'b110000 - PCT_VDD_75 6'b110001 - PCT_VDD_74 6'b110010 - PCT_VDD_73 6'b110011 - PCT_VDD_72 6'b110100 - PCT_VDD_71 6'b110101 - PCT_VDD_70 6'b110110 - PCT_VDD_69 6'b110111 - PCT_VDD_68 6'b111000 - PCT_VDD_67 6'b111001 - PCT_VDD_66 6'b111010 - PCT_VDD_65 6'b111011 - PCT_VDD_64 6'b111100 - PCT_VDD_63 6'b111101 - PCT_VDD_62 6'b111110 - PCT_VDD_61 6'b111111 - PCT_VDD_60 Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.183 MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT_PROXY Register

14.2.1.1.2.2.183.1 MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT_PROXY Register (Offset = 1A1B0h) [reset = 0h]

Shows the status of the voltage glitch detector circuit monitoring the VDD_CORE voltage domain

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Table 14-5459. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A1B0h

Figure 14-2717. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_PROXY
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED							VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_PROXY
NONE							R
0h							0h

Table 14-5460. MCU_CTRL_MMRCFG0_VDD_CORE_GLDTC_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_PROXY	R	0h	High voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. Field values (others are reserved): 1'b0 - HV_UNKNOWN (not detected) 1'b1 - HV_DETECTED Reset Source: mcu_chip1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_PROXY	R	0h	Low voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. Field values (others are reserved): 1'b0 - LV_UNKNOWN (not detected) 1'b1 - LV_DETECTED Reset Source: mcu_chip1_rst_n

14.2.1.1.2.2.184 MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL_PROXY Register

14.2.1.1.2.2.184.1 MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL_PROXY Register (Offset = 1A200h) [reset = 2001Fh]

Configures PRG_PP_0 - Fixed POKs (In POR, POKSA, and POK_VDD_CORE_OV)

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Table 14-5461. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A200h

Figure 14-2718. MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PRG_PP_0_CTRL_DEGLITCH_SEL_PROXY	
NONE						R/W	
0h						2h	
15	14	13	12	11	10	9	8
PRG_PP_0_CTRL_POK_EN_SEL_PROXY	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN_PROXY	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN_PROXY	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN_PROXY	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN_PROXY	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN_PROXY
NONE			R/W	R/W	R/W	R/W	R/W
0h			1h	1h	1h	1h	1h

Table 14-5462. MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_0_CTRL_DEGLITCH_SEL_PROXY	R/W	2h	Deglitch period for PRG_PP1 POKs (microseconds) Field values (others are reserved): 2'b00 - DG_5_US 2'b01 - DG_10_US 2'b10 - DG_15_US 2'b11 - DG_20_US Reset Source: mod_por_rst_n
15	PRG_PP_0_CTRL_POK_EN_SEL_PROXY	R/W	0h	Selects source of POK controls Field values (others are reserved): 1'b0 - TIEOFFS 1'b1 - PRG_PP0_CTRL_REG Reset Source: mod_por_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	PRG_PP_0_CTRL_POK_VDDA_PMIC_IN_UV_EN_PROXY	R/W	1h	Enable VDDA_PMIC_IN undervoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
3	PRG_PP_0_CTRL_POK_VDD_MCU_OV_EN_PROXY	R/W	1h	Enable VDD_MCU overvoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n

Table 14-5462. MCU_CTRL_MMRCFG0_PRG_PP_0_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PRG_PP_0_CTRL_POK_VDD_MCU_UV_EN_PROXY	R/W	1h	Enable VDD_MCU undervoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
1	PRG_PP_0_CTRL_POK_VDDA_MCU_OV_EN_PROXY	R/W	1h	Enable 1.8V VDDA_MCU overvoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
0	PRG_PP_0_CTRL_POK_VDDA_MCU_UV_EN_PROXY	R/W	1h	Enable 1.8V VDDA_MCU undervoltage POK detection Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n

14.2.1.1.2.2.185 MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL_PROXY Register

14.2.1.1.2.2.185.1 MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL_PROXY Register (Offset = 1A208h) [reset = 2007Fh]

Configures PRG_PP_1 - Ping-Pong Capable POKs

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Table 14-5463. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A208h

Figure 14-2719. MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED				PRG_PP_1_CTRL_POK_PP_EN_PROXY	RESERVED	PRG_PP_1_CTRL_DEGLITCH_SEL_PROXY	
NONE				R/W	NONE	R/W	
0h				0h	0h	2h	

15	14	13	12	11	10	9	8
PRG_PP_1_CTRL_POK_EN_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL_PROXY	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL_PROXY			PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL_PROXY
R/W	R/W	R/W	R/W	R/W			R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
RESERVED	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN_PROXY	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN_PROXY	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN_PROXY			PRG_PP_1_CTRL_POK_VDDR_CORE_EN_PROXY
NONE	R/W	R/W	R/W	R/W			R/W
0h	1h	1h	1h	1h	1h	1h	1h

Table 14-5464. MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	PRG_PP_1_CTRL_POK_PP_EN_PROXY	R/W	0h	POK ping-pong enable. When set, POKs with their ov_sel option set to UV_OR_PINGPONG are automatically cycled between UV and OV detection (ping-pong). POKs with ov_sel selecting OV are unaffected by this bit. Field values (others are reserved): 1'b0 - UV_FIXED 1'b1 - UV_PINGPONG_OV Reset Source: mod_por_rst_n
18	RESERVED	NONE	0h	Reserved
17:16	PRG_PP_1_CTRL_DEGLITCH_SEL_PROXY	R/W	2h	Deglitch period for PRG_PP1 POKs (microseconds) Field values (others are reserved): 2'b00 - DG_5_US 2'b01 - DG_10_US 2'b10 - DG_15_US 2'b11 - DG_20_US Reset Source: mod_por_rst_n

Table 14-5464. MCU_CTRL_MMRCFG0_PRG_PP_1_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PRG_PP_1_CTRL_POK_EN_SEL_PROXY	R/W	0h	Selects source of POK controls Field values (others are reserved): 1'b0 - TIEOFFS 1'b1 - PRG_PP0_CTRL_REG Reset Source: mod_por_rst_n
14	PRG_PP_1_CTRL_POK_VDDS_DDRIO_OV_SEL_PROXY	R/W	0h	POK_VDDS_DDRIO mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
13	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_OV_SEL_PROXY	R/W	0h	POK_VDDSHV_MAIN_3P3 mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
12	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_OV_SEL_PROXY	R/W	0h	POK_VDDSHV_MAIN_1P8 mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
11	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_OV_SEL_PROXY	R/W	0h	POK_VMON_CAP_MCU_GENERAL mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
8	PRG_PP_1_CTRL_POK_VDDR_CORE_OV_SEL_PROXY	R/W	0h	POK_VDDR_CORE mode (undervoltage/ping-pong or over-voltage) Field values (others are reserved): 1'b0 - UV_OR_PINGPONG 1'b1 - OV Reset Source: mod_por_rst_n
7	RESERVED	NONE	0h	Reserved
6	PRG_PP_1_CTRL_POK_VDDS_DDRIO_EN_PROXY	R/W	1h	Enable POK_VDDS_DDRIO (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
5	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_3P3_EN_PROXY	R/W	1h	Enable POK_VDDSHV_MAIN_3P3 (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
4	PRG_PP_1_CTRL_POK_VDDSHV_MAIN_1P8_EN_PROXY	R/W	1h	Enable POK_VDDSHV_MAIN_1P8 (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
3	PRG_PP_1_CTRL_POK_VMON_CAP_MCU_GENERAL_EN_PROXY	R/W	1h	Enable POK_VMON_CAP_MCU_GENERAL (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n
0	PRG_PP_1_CTRL_POK_VDDR_CORE_EN_PROXY	R/W	1h	Enable POK_VDDR_CORE (if pok_en_sel = 1): Field values (others are reserved): 1'b0 - Disabled 1'b1 - Enabled Reset Source: mod_por_rst_n

14.2.1.1.2.2.186 MCU_CTRL_MMRCFG0_CLKGATE_CTRL_PROXY Register

14.2.1.1.2.2.186.1 MCU_CTRL_MMRCFG0_CLKGATE_CTRL_PROXY Register (Offset = 1A280h) [reset = 0h]

Controls the power clock gating feature of MCU domain modules and busses

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Table 14-5465. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 A280h

Figure 14-2720. MCU_CTRL_MMRCFG0_CLKGATE_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLKGATE_CTRL_WKUP_SAFE_CBA_NOGATE_PROXY
NONE							R/W
0h							0h

Table 14-5466. MCU_CTRL_MMRCFG0_CLKGATE_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLKGATE_CTRL_WKUP_SAFE_CBA_NOGATE_PROXY	R/W	0h	WKUP domain CBASS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

14.2.1.1.2.2.187 MCU_CTRL_MMRCFG0_LOCK6_KICK0_PROXY Register

14.2.1.1.2.2.187.1 MCU_CTRL_MMRCFG0_LOCK6_KICK0_PROXY Register (Offset = 1B008h) [reset = 0h]

- KICK0 component

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Table 14-5467. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 B008h

Figure 14-2721. MCU_CTRL_MMRCFG0_LOCK6_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0_PROXY							
R/W							
0h							

Table 14-5468. MCU_CTRL_MMRCFG0_LOCK6_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.188 MCU_CTRL_MMRCFG0_LOCK6_KICK1_PROXY Register

14.2.1.1.2.2.188.1 MCU_CTRL_MMRCFG0_LOCK6_KICK1_PROXY Register (Offset = 1B00Ch) [reset = 0h]

- KICK1 component

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Table 14-5469. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 B00Ch

Figure 14-2722. MCU_CTRL_MMRCFG0_LOCK6_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1_PROXY							
R/W							
0h							

Table 14-5470. MCU_CTRL_MMRCFG0_LOCK6_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.2.2.189 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0 Register

14.2.1.1.2.2.189.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0 Register (Offset = 1B100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5471. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 B100h

Figure 14-2723. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0							
R/W							
0h							

Table 14-5472. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.190 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R1 Register

14.2.1.1.2.2.190.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R1 Register (Offset = 1B104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5473. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 B104h

Figure 14-2724. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1							
R/W							
0h							

Table 14-5474. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.191 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2 Register

14.2.1.1.2.2.191.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2 Register (Offset = 1B108h) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-5475. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 B108h

Figure 14-2725. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2							
R/W							
0h							

Table 14-5476. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.192 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3 Register

14.2.1.1.2.2.192.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3 Register (Offset = 1B10Ch) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-5477. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 B10Ch

Figure 14-2726. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5478. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.193 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4 Register

14.2.1.1.2.2.193.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4 Register (Offset = 1B110h) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-5479. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 B110h

Figure 14-2727. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4							
R/W							
0h							

Table 14-5480. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.2.2.194 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5 Register

14.2.1.1.2.2.194.1 MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5 Register (Offset = 1B114h) [reset = 0h]

Claim bits for Partition 6

Return to Summary Table

Table 14-5481. Instance Table

Instance Name	Physical Address
MCU_CTRL_MMR0	0451 B114h

Figure 14-2728. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5482. MCU_CTRL_MMRCFG0_CLAIMREG_P6_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3 WKUP_CTRL_MMR0

WKUP_CTRL_MMR0

14.2.1.1.3.1 WKUP_CTRL_MMR0 Summaries

WKUP_CTRL_MMR0 Summaries

Table 14-5483. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
0h	32	WKUP_CTRL_MMR_CFG0_PID	4300 0000h
8h	32	WKUP_CTRL_MMR_CFG0_MMR_CFG1	4300 0008h
14h	32	WKUP_CTRL_MMR_CFG0_JTAGID	4300 0014h
18h	32	WKUP_CTRL_MMR_CFG0_JTAG_USER_ID	4300 0018h
44h	32	WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS	4300 0044h
60h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0	4300 0060h
64h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1	4300 0064h
68h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2	4300 0068h
6Ch	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3	4300 006Ch
74h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5	4300 0074h
78h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6	4300 0078h
200h	32	WKUP_CTRL_MMR_CFG0_MAC_ID0	4300 0200h
204h	32	WKUP_CTRL_MMR_CFG0_MAC_ID1	4300 0204h
220h	32	WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0	4300 0220h
230h	32	WKUP_CTRL_MMR_CFG0_GP_SW0	4300 0230h
234h	32	WKUP_CTRL_MMR_CFG0_GP_SW1	4300 0234h
238h	32	WKUP_CTRL_MMR_CFG0_GP_SW2	4300 0238h
23Ch	32	WKUP_CTRL_MMR_CFG0_GP_SW3	4300 023Ch
270h	32	WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT	4300 0270h
280h	32	WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT	4300 0280h
1008h	32	WKUP_CTRL_MMR_CFG0_LOCK0_KICK0	4300 1008h
100Ch	32	WKUP_CTRL_MMR_CFG0_LOCK0_KICK1	4300 100Ch
1010h	32	WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS	4300 1010h
1014h	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR	4300 1014h
1018h	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLE	4300 1018h
101Ch	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR	4300 101Ch
1024h	32	WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS	4300 1024h
1028h	32	WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS	4300 1028h
102Ch	32	WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS	4300 102Ch
1030h	32	WKUP_CTRL_MMR_CFG0_FAULT_CLEAR	4300 1030h
1100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY	4300 1100h
1110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY	4300 1110h
1114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY	4300 1114h
2000h	32	WKUP_CTRL_MMR_CFG0_PID_PROXY	4300 2000h
2008h	32	WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY	4300 2008h
2044h	32	WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY	4300 2044h
2060h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY	4300 2060h

Table 14-5483. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
2064h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY	4300 2064h
2068h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY	4300 2068h
206Ch	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY	4300 206Ch
2074h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5_PROXY	4300 2074h
2078h	32	WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY	4300 2078h
2200h	32	WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY	4300 2200h
2204h	32	WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY	4300 2204h
2220h	32	WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY	4300 2220h
2230h	32	WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY	4300 2230h
2234h	32	WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY	4300 2234h
2238h	32	WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY	4300 2238h
223Ch	32	WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY	4300 223Ch
2270h	32	WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY	4300 2270h
2280h	32	WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY	4300 2280h
3008h	32	WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY	4300 3008h
300Ch	32	WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY	4300 300Ch
3010h	32	WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY	4300 3010h
3014h	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	4300 3014h
3018h	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY	4300 3018h
301Ch	32	WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY	4300 301Ch
3024h	32	WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY	4300 3024h
3028h	32	WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY	4300 3028h
302Ch	32	WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY	4300 302Ch
3030h	32	WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY	4300 3030h
3100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0	4300 3100h
3104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1	4300 3104h
3108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2	4300 3108h
310Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3	4300 310Ch
3110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4	4300 3110h
3114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5	4300 3114h
3118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6	4300 3118h
4008h	32	WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL	4300 4008h
41B4h	32	WKUP_CTRL_MMR_CFG0_SDIO0_CTRL	4300 41B4h
4204h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL	4300 4204h
42E0h	32	WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL	4300 42E0h
5008h	32	WKUP_CTRL_MMR_CFG0_LOCK1_KICK0	4300 5008h
500Ch	32	WKUP_CTRL_MMR_CFG0_LOCK1_KICK1	4300 500Ch
5100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY	4300 5100h
510Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY	4300 510Ch
5110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY	4300 5110h

Table 14-5483. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
5114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY	4300 5114h
5130h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY	4300 5130h
6008h	32	WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY	4300 6008h
61B4h	32	WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY	4300 61B4h
6204h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY	4300 6204h
62E0h	32	WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY	4300 62E0h
7008h	32	WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY	4300 7008h
700Ch	32	WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY	4300 700Ch
7100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0	4300 7100h
7104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1	4300 7104h
7108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2	4300 7108h
710Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3	4300 710Ch
7110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4	4300 7110h
7114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5	4300 7114h
7118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6	4300 7118h
711Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7	4300 711Ch
7120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8	4300 7120h
7124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9	4300 7124h
7128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10	4300 7128h
712Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11	4300 712Ch
7130h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12	4300 7130h
8010h	32	WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL	4300 8010h
8020h	32	WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL	4300 8020h
8030h	32	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL	4300 8030h
8190h	32	WKUP_CTRL_MMR_CFG0_USB0_CLKSEL	4300 8190h
81B0h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL	4300 81B0h
81B4h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL	4300 81B4h
8340h	32	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL	4300 8340h
8380h	32	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL	4300 8380h
8600h	32	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL	4300 8600h
9008h	32	WKUP_CTRL_MMR_CFG0_LOCK2_KICK0	4300 9008h
900Ch	32	WKUP_CTRL_MMR_CFG0_LOCK2_KICK1	4300 900Ch
9100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY	4300 9100h
910Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY	4300 910Ch
9118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY	4300 9118h
911Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY	4300 911Ch
9130h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY	4300 9130h
A010h	32	WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY	4300 A010h
A020h	32	WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY	4300 A020h
A030h	32	WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY	4300 A030h

Table 14-5483. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
A190h	32	WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY	4300 A190h
A1B0h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY	4300 A1B0h
A1B4h	32	WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY	4300 A1B4h
A340h	32	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY	4300 A340h
A380h	32	WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY	4300 A380h
A600h	32	WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY	4300 A600h
B008h	32	WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY	4300 B008h
B00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY	4300 B00Ch
B100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0	4300 B100h
B104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1	4300 B104h
B108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2	4300 B108h
B10Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3	4300 B10Ch
B110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4	4300 B110h
B114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5	4300 B114h
B118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6	4300 B118h
B11Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7	4300 B11Ch
B120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8	4300 B120h
B124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9	4300 B124h
B128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10	4300 B128h
B12Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11	4300 B12Ch
B130h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12	4300 B130h
C2C0h	32	WKUP_CTRL_MMR_CFG0_POST_STAT	4300 C2C0h
C400h	32	WKUP_CTRL_MMR_CFG0_PBIST_EN	4300 C400h
D008h	32	WKUP_CTRL_MMR_CFG0_LOCK3_KICK0	4300 D008h
D00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK3_KICK1	4300 D00Ch
D100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY	4300 D100h
D104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY	4300 D104h
D108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY	4300 D108h
D10Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY	4300 D10Ch
D110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY	4300 D110h
D114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY	4300 D114h
D118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY	4300 D118h
D11Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY	4300 D11Ch
D120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY	4300 D120h
E2C0h	32	WKUP_CTRL_MMR_CFG0_POST_STAT_PROXY	4300 E2C0h
E400h	32	WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY	4300 E400h

Table 14-5483. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
F008h	32	WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY	4300 F008h
F00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY	4300 F00Ch
F100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0	4300 F100h
F104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1	4300 F104h
F108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2	4300 F108h
F10Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3	4300 F10Ch
F110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4	4300 F110h
F114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5	4300 F114h
F118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6	4300 F118h
F11Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7	4300 F11Ch
F120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8	4300 F120h
11100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY	4301 1100h
11120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY	4301 1120h
13100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0	4301 3100h
13104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1	4301 3104h
13108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2	4301 3108h
1310Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3	4301 310Ch
13110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4	4301 3110h
13114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5	4301 3114h
13118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6	4301 3118h
1311Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7	4301 311Ch
13120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8	4301 3120h
18080h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_SYS	4301 8080h
18084h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0	4301 8084h
18088h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1	4301 8088h
18090h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC	4301 8090h
18098h	32	WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS	4301 8098h
18170h	32	WKUP_CTRL_MMR_CFG0_RST_CTRL	4301 8170h
18174h	32	WKUP_CTRL_MMR_CFG0_RST_STAT	4301 8174h
18178h	32	WKUP_CTRL_MMR_CFG0_RST_SRC	4301 8178h
1817Ch	32	WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD	4301 817Ch
18180h	32	WKUP_CTRL_MMR_CFG0_WKUP0_EN	4301 8180h
18280h	32	WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0	4301 8280h
18284h	32	WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1	4301 8284h
18300h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL	4301 8300h
18308h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0	4301 8308h
1830Ch	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1	4301 830Ch
18310h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE	4301 8310h
18318h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT	4301 8318h
18320h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_J	4301 8320h + formula
18340h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_J	4301 8340h + formula
18360h	32	WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL	4301 8360h

Table 14-5483. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
18364h	32	WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR	4301 8364h
18368h	32	WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT	4301 8368h
18380h	32	WKUP_CTRL_MMR_CFG0_RET_RAM_STAT	4301 8380h
18400h	32	WKUP_CTRL_MMR_CFG0_WFI_STATUS	4301 8400h
18420h	32	WKUP_CTRL_MMR_CFG0_DS_MAIN	4301 8420h
18440h	32	WKUP_CTRL_MMR_CFG0_DS_DM_RESET	4301 8440h
18460h	32	WKUP_CTRL_MMR_CFG0_DS_USB0_RESET	4301 8460h
184A0h	32	WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ	4301 84A0h
18500h	32	WKUP_CTRL_MMR_CFG0_DEVICE_TYPE	4301 8500h
19008h	32	WKUP_CTRL_MMR_CFG0_LOCK6_KICK0	4301 9008h
1900Ch	32	WKUP_CTRL_MMR_CFG0_LOCK6_KICK1	4301 900Ch
19100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY	4301 9100h
19104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY	4301 9104h
19108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY	4301 9108h
1910Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY	4301 910Ch
19110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY	4301 9110h
19114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY	4301 9114h
19118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY	4301 9118h
1911Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY	4301 911Ch
19120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY	4301 9120h
19124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY	4301 9124h
19128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY	4301 9128h
1A080h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY	4301 A080h
1A084h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY	4301 A084h
1A088h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY	4301 A088h
1A090h	32	WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY	4301 A090h
1A098h	32	WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY	4301 A098h
1A170h	32	WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY	4301 A170h
1A174h	32	WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY	4301 A174h
1A178h	32	WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY	4301 A178h
1A17Ch	32	WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY	4301 A17Ch
1A180h	32	WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY	4301 A180h
1A280h	32	WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY	4301 A280h
1A284h	32	WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY	4301 A284h
1A300h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY	4301 A300h
1A308h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY	4301 A308h

Table 14-5483. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
1A30Ch	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY	4301 A30Ch
1A310h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY	4301 A310h
1A318h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY	4301 A318h
1A320h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_J	4301 A320h + formula
1A340h	32	WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_J	4301 A340h + formula
1A360h	32	WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL_PROXY	4301 A360h
1A364h	32	WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR_PROXY	4301 A364h
1A368h	32	WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT_PROXY	4301 A368h
1A380h	32	WKUP_CTRL_MMR_CFG0_RET_RAM_STAT_PROXY	4301 A380h
1A400h	32	WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY	4301 A400h
1A420h	32	WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY	4301 A420h
1A440h	32	WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY	4301 A440h
1A460h	32	WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY	4301 A460h
1A4A0h	32	WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY	4301 A4A0h
1A500h	32	WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY	4301 A500h
1B008h	32	WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY	4301 B008h
1B00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY	4301 B00Ch
1B100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0	4301 B100h
1B104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1	4301 B104h
1B108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2	4301 B108h
1B10Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3	4301 B10Ch
1B110h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4	4301 B110h
1B114h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5	4301 B114h
1B118h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6	4301 B118h
1B11Ch	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7	4301 B11Ch
1B120h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8	4301 B120h
1B124h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9	4301 B124h
1B128h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10	4301 B128h
1D008h	32	WKUP_CTRL_MMR_CFG0_LOCK7_KICK0	4301 D008h
1D00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK7_KICK1	4301 D00Ch
1D100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY	4301 D100h
1D104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY	4301 D104h
1D108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY	4301 D108h
1F008h	32	WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY	4301 F008h
1F00Ch	32	WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY	4301 F00Ch
1F100h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0	4301 F100h
1F104h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1	4301 F104h

Table 14-5483. WKUP_CTRL_MMR_CFG0 Registers, Base Address=4300 0000h, Length=131072 (continued)

Offset	Length	Register Name	WKUP_CTRL_MMR0 Physical Address
1F108h	32	WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2	4301 F108h

14.2.1.1.3.2 WKUP_CTRL_MMR0 Registers

WKUP_CTRL_MMR0 Registers

14.2.1.1.3.2.1 WKUP_CTRL_MMR_CFG0_PID Register

14.2.1.1.3.2.1.1 WKUP_CTRL_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-5484. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0000h

Figure 14-2729. WKUP_CTRL_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM		PID_MINOR					
R		R					
0h		15h					

Table 14-5485. WKUP_CTRL_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.3.2.2 WKUP_CTRL_MMR_CFG0_MMR_CFG1 Register

14.2.1.1.3.2.2.1 WKUP_CTRL_MMR_CFG0_MMR_CFG1 Register (Offset = 8h) [reset = 800000DFh]

Indicates the MMR configuration

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Table 14-5486. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0008h

Figure 14-2730. WKUP_CTRL_MMR_CFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS							
R							
DFh							

Table 14-5487. WKUP_CTRL_MMR_CFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	DFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.3.2.3 WKUP_CTRL_MMR_CFG0_JTAGID Register

14.2.1.1.3.2.3.1 WKUP_CTRL_MMR_CFG0_JTAGID Register (Offset = 14h) [reset = BBAA02Fh]

The JTAGID register must be readable by the configuration bus so that this can be accessed via the JTAG and CPU. In Boundary Scan mode, this ID should also be readable with only TCLK present. This means without a valid CPU clock running and also implies that Fusefarm scan is not necessary. The partno and variant field inputs should be set in the top metal mask so that this may be changed if a future PG is necessary. All other fields may be hard coded.

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Table 14-5488. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0014h

Figure 14-2731. WKUP_CTRL_MMR_CFG0_JTAGID Name Register

31	30	29	28	27	26	25	24
JTAGID_VARIANT				JTAGID_PARTNO			
R				R			
0h				BBAAh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JTAGID_PARTNO							
R							
BBAAh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
JTAGID_PARTNO				JTAGID_MFG			
R				R			
BBAAh				17h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
JTAGID_MFG							JTAGID_LSB
R							R
17h							1h

Table 14-5489. WKUP_CTRL_MMR_CFG0_JTAGID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	JTAGID_VARIANT	R	0h	Used to indicate new PGs Reset Source: mod_por_rst_n
27:12	JTAGID_PARTNO	R	BBAAh	Part number for boundary scan Reset Source: mod_por_rst_n
11:1	JTAGID_MFG	R	17h	Indicates manufacturer Reset Source: mod_por_rst_n
0	JTAGID_LSB	R	1h	Always 1 Reset Source: mod_por_rst_n

14.2.1.1.3.2.4 WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register

14.2.1.1.3.2.4.1 WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register (Offset = 18h) [reset = 0h]

Additional fuse programmable device identifying information.

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Table 14-5490. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0018h

Figure 14-2732. WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Name Register

31	30	29	28	27	26	25	24
JTAG_USER_ID_USERCODE							
R							
X							
23	22	21	20	19	18	17	16
JTAG_USER_ID_USERCODE							
R							
X							
15	14	13	12	11	10	9	8
JTAG_USER_ID_USERCODE							
R							
X							
7	6	5	4	3	2	1	0
JTAG_USER_ID_USERCODE							
R							
X							

Table 14-5491. WKUP_CTRL_MMR_CFG0_JTAG_USER_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_USER_ID_USERCODE	R	X	Device information Reset Source: mod_por_rst_n

14.2.1.1.3.2.5 WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS Register

14.2.1.1.3.2.5.1 WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS Register (Offset = 44h) [reset = 0h]

Used by ROM to mark the progress of the boot operation

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Table 14-5492. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0044h

Figure 14-2733. WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BOOT_PROGRESS_PROGRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BOOT_PROGRESS_PROGRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BOOT_PROGRESS_PROGRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BOOT_PROGRESS_PROGRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5493. WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BOOT_PROGRESS_PROGRESS	R/W	0h	Written by ROM to indicate boot progression. Values and their meaning are determined by the ROM. Reset Source: mod_por_rst_n

14.2.1.1.3.2.6 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register

14.2.1.1.3.2.6.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register (Offset = 60h) [reset = 0h]

Indicates enabled Main Domain processing elements on the device

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Table 14-5494. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0060h

Figure 14-2734. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				DEVICE_FEATURE0_R5FSS1_CORE1	DEVICE_FEATURE0_R5FSS1_CORE0	DEVICE_FEATURE0_R5FSS0_CORE1	DEVICE_FEATURE0_R5FSS0_CORE0
NONE				R	R	R	R
0h				X	X	X	X
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5495. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	DEVICE_FEATURE0_R5FSS1_CORE1	R	X	Main R5FSS1 dual/single core support Field values (others are reserved): 1'b0 - Single core 1'b1 - Dual core Reset Source: mod_por_rst_n
18	DEVICE_FEATURE0_R5FSS1_CORE0	R	X	Main R5SS1 avalability Field values (others are reserved): 1'b0 - Cluster not available 1'b1 - Cluster available Reset Source: mod_por_rst_n
17	DEVICE_FEATURE0_R5FSS0_CORE1	R	X	Main R5FSS0 dual/single core support Field values (others are reserved): 1'b0 - Single core 1'b1 - Dual core Reset Source: mod_por_rst_n
16	DEVICE_FEATURE0_R5FSS0_CORE0	R	X	Main R5SS0 avalability Field values (others are reserved): 1'b0 - Cluster not available 1'b1 - Cluster available Reset Source: mod_por_rst_n

Table 14-5495. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.7 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Register

14.2.1.1.3.2.7.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Register (Offset = 64h) [reset = 0h]

Indicates enabled Main Domain DSP processing elements on the device

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Table 14-5496. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0064h

Figure 14-2735. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED						DEVICE_FEATURE1_C7X_CORE1	DEVICE_FEATURE1_C7X_CORE0
NONE						R	R
0h						X	X

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5497. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DEVICE_FEATURE1_C7X_CORE1	R	X	C7x1 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
16	DEVICE_FEATURE1_C7X_CORE0	R	X	C7x0 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.8 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register

14.2.1.1.3.2.8.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register (Offset = 68h) [reset = 0h]

Indicates enabled interface elements on the device

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Table 14-5498. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0068h

Figure 14-2736. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td>DEVICE_FEATURE2_CRYPTO_SM_EN</td><td>DEVICE_FEATURE2_CRYPTO_PKA_EN</td><td>DEVICE_FEATURE2_CRYPTO_ENCR_EN</td><td>DEVICE_FEATURE2_CRYPTO_SHA_EN</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>DEVICE_FEATURE2_AES_AUTH_EN</td><td colspan="6">RESERVED</td><td>DEVICE_FEATURE2_MCAN_FD_MODE</td></tr>
<tr><td>R</td><td colspan="6">NONE</td><td>R</td></tr>
<tr><td>X</td><td colspan="6">0h</td><td>X</td></tr>
</table>

Table 14-5499. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	DEVICE_FEATURE2_CRYPTO_SM_EN	R	X	Crypto Module SM2, SM3, SM4 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
10	DEVICE_FEATURE2_CRYPTO_PKA_EN	R	X	Crypto Module PKA Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
9	DEVICE_FEATURE2_CRYPTO_ENCR_EN	R	X	Crypto Module AES/3DES/DBRG Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

Table 14-5499. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DEVICE_FEATURE2_CRYPTO_SHA_EN	R	X	Crypto Module SHA/MD5 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
7	DEVICE_FEATURE2_AES_AUTH_EN	R	X	AES authentication availability in FlashSS and SMS Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE2_MCAN_FD_MODE	R	X	FD mode availability (applies to all MCAN instances) Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

14.2.1.1.3.2.9 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3 Register

14.2.1.1.3.2.9.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3 Register (Offset = 6Ch) [reset = 0h]

Indicates enabled processing element features on the device

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Table 14-5500. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 006Ch

Figure 14-2737. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DEVICE_FEATURE3_MMA1_PRESENT	DEVICE_FEATURE3_MMA0_PRESENT
NONE						R	R
0h						X	X

Table 14-5501. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DEVICE_FEATURE3_MMA1_PRESENT	R	X	C7x1 MMA Feature Availability Reset Source: mod_por_rst_n
0	DEVICE_FEATURE3_MMA0_PRESENT	R	X	C7x0 MMA Feature Availability Reset Source: mod_por_rst_n

14.2.1.1.3.2.10 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5 Register

14.2.1.1.3.2.10.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5 Register (Offset = 74h) [reset = 0h]

Indicates enabled interface elements on the device

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Table 14-5502. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0074h

Figure 14-2738. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DEVICE_FEATURE5_MCAN4	DEVICE_FEATURE5_MCAN3	DEVICE_FEATURE5_MCAN2	DEVICE_FEATURE5_MCAN1	DEVICE_FEATURE5_MCAN0
NONE			R	R	R	R	R
0h			X	X	X	X	X

Table 14-5503. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DEVICE_FEATURE5_MCAN4	R	X	MCAN4 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
3	DEVICE_FEATURE5_MCAN3	R	X	MCAN3 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
2	DEVICE_FEATURE5_MCAN2	R	X	MCAN2 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
1	DEVICE_FEATURE5_MCAN1	R	X	MCAN1 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

Table 14-5503. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DEVICE_FEATURE5_MCAN0	R	X	MCAN0 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

14.2.1.1.3.2.11 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register

14.2.1.1.3.2.11.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register (Offset = 78h) [reset = 0h]

Indicates enabled interface elements on the device

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Table 14-5504. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0078h

Figure 14-2739. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
X	X	X	X	X	X	X	X
15	14	13	12	11	10	9	8
RESERVED					DEVICE_FEATURE6_ASRC1	DEVICE_FEATURE6_ASRC0	RESERVED
NONE					R	R	NONE
0h					X	X	0h
7	6	5	4	3	2	1	0
DEVICE_FEATURE6_ATL	DEVICE_FEATURE6_MLB	DEVICE_FEATURE6_SA3_UL	RESERVED				
R	R	R	NONE				
X	X	X	0h				

Table 14-5505. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
15:11	RESERVED	NONE	0h	Reserved
10	DEVICE_FEATURE6_ASRC1	R	X	ASRC1 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
9	DEVICE_FEATURE6_ASRC0	R	X	ASRC0 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
8	RESERVED	NONE	0h	Reserved
7	DEVICE_FEATURE6_ATL	R	X	Audio Tracking Logic Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
6	DEVICE_FEATURE6_MLB	R	X	Medis Local Bus Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

Table 14-5505. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DEVICE_FEATURE6_SA3_UL	R	X	SA3SS domain security accelerator availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.12 WKUP_CTRL_MMR_CFG0_MAC_ID0 Register

14.2.1.1.3.2.12.1 WKUP_CTRL_MMR_CFG0_MAC_ID0 Register (Offset = 200h) [reset = 0h]

Ethernet MAC address lower 32-bits

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Table 14-5506. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0200h

Figure 14-2740. WKUP_CTRL_MMR_CFG0_MAC_ID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MAC_ID0_MACID_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MAC_ID0_MACID_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MAC_ID0_MACID_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MAC_ID0_MACID_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-5507. WKUP_CTRL_MMR_CFG0_MAC_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAC_ID0_MACID_LO	R/W	X	32 lsbs of MAC address Reset Source: mod_g_rst_n

14.2.1.1.3.2.13 WKUP_CTRL_MMR_CFG0_MAC_ID1 Register

14.2.1.1.3.2.13.1 WKUP_CTRL_MMR_CFG0_MAC_ID1 Register (Offset = 204h) [reset = 0h]

Ethernet MAC address upper 16-bits

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Table 14-5508. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0204h

Figure 14-2741. WKUP_CTRL_MMR_CFG0_MAC_ID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ID1_MACID_HI							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID1_MACID_HI							
R/W							
X							

Table 14-5509. WKUP_CTRL_MMR_CFG0_MAC_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAC_ID1_MACID_HI	R/W	X	16 msbs of MAC address Reset Source: mod_g_rst_n

14.2.1.1.3.2.14 WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register

14.2.1.1.3.2.14.1 WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register (Offset = 220h) [reset = 61650451h]

USB device and vendor ID register 0 (ROM Writes)

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Table 14-5510. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0220h

Figure 14-2742. WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0 Name Register

31	30	29	28	27	26	25	24
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
23	22	21	20	19	18	17	16
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
15	14	13	12	11	10	9	8
USB_DEVICE_ID0_ID0							
R/W							
61650451h							
7	6	5	4	3	2	1	0
USB_DEVICE_ID0_ID0							
R/W							
61650451h							

Table 14-5511. WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USB_DEVICE_ID0_ID0	R/W	61650451h	ROM writes 32-bit Value from Customer OTP to Here Reset Source: mod_g_rst_n

14.2.1.1.3.2.15 WKUP_CTRL_MMR_CFG0_GP_SW0 Register

14.2.1.1.3.2.15.1 WKUP_CTRL_MMR_CFG0_GP_SW0 Register (Offset = 230h) [reset = 0h]

Allocated for customer use - Ex. Storage of PID/VID, Model #, Etc.

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Table 14-5512. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0230h

Figure 14-2743. WKUP_CTRL_MMR_CFG0_GP_SW0 Name Register

31	30	29	28	27	26	25	24
GP_SW0_VAL							
R							
X							
23	22	21	20	19	18	17	16
GP_SW0_VAL							
R							
X							
15	14	13	12	11	10	9	8
GP_SW0_VAL							
R							
X							
7	6	5	4	3	2	1	0
GP_SW0_VAL							
R							
X							

Table 14-5513. WKUP_CTRL_MMR_CFG0_GP_SW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GP_SW0_VAL	R	X	general purpose value Reset Source: mod_por_rst_n

14.2.1.1.3.2.16 WKUP_CTRL_MMR_CFG0_GP_SW1 Register

14.2.1.1.3.2.16.1 WKUP_CTRL_MMR_CFG0_GP_SW1 Register (Offset = 234h) [reset = 0h]

Allocated for customer use - Ex. Storage of PID/VID, Model #, Etc.

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Table 14-5514. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0234h

Figure 14-2744. WKUP_CTRL_MMR_CFG0_GP_SW1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GP_SW1_VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GP_SW1_VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GP_SW1_VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GP_SW1_VAL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-5515. WKUP_CTRL_MMR_CFG0_GP_SW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GP_SW1_VAL	R	X	general purpose value Reset Source: mod_por_rst_n

14.2.1.1.3.2.17 WKUP_CTRL_MMR_CFG0_GP_SW2 Register

14.2.1.1.3.2.17.1 WKUP_CTRL_MMR_CFG0_GP_SW2 Register (Offset = 238h) [reset = 0h]

Allocated for customer use - Ex. Storage of PID/VID, Model #, Etc.

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Table 14-5516. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0238h

Figure 14-2745. WKUP_CTRL_MMR_CFG0_GP_SW2 Name Register

31	30	29	28	27	26	25	24
GP_SW2_VAL							
R							
X							
23	22	21	20	19	18	17	16
GP_SW2_VAL							
R							
X							
15	14	13	12	11	10	9	8
GP_SW2_VAL							
R							
X							
7	6	5	4	3	2	1	0
GP_SW2_VAL							
R							
X							

Table 14-5517. WKUP_CTRL_MMR_CFG0_GP_SW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GP_SW2_VAL	R	X	general purpose value Reset Source: mod_por_rst_n

14.2.1.1.3.2.18 WKUP_CTRL_MMR_CFG0_GP_SW3 Register

14.2.1.1.3.2.18.1 WKUP_CTRL_MMR_CFG0_GP_SW3 Register (Offset = 23Ch) [reset = 0h]

Allocated for customer use - Ex. Storage of PID/VID, Model #, Etc.

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Table 14-5518. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 023Ch

Figure 14-2746. WKUP_CTRL_MMR_CFG0_GP_SW3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				GP_SW3_VAL			
NONE				R			
0h				X			

Table 14-5519. WKUP_CTRL_MMR_CFG0_GP_SW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	GP_SW3_VAL	R	X	general purpose value Reset Source: mod_por_rst_n

14.2.1.1.3.2.19 WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Register

14.2.1.1.3.2.19.1 WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Register (Offset = 270h) [reset = 0h]

Provides Aggregated, Read Only status of bus address error interrupts reported by CBASS components.. Processors on the SoC read this MMR to determine which CBASS components require service. Actual service of CBASS interrupts must be handled through each CBASS component.

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Table 14-5520. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0270h

Figure 14-2747. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Name Register

31	30	29	28	27	26	25	24
CBA_ERR_STAT_DBG_CBA_ERR	RESERVED					CBA_ERR_STAT_WKUP_DM_CBA_ERR	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR
R	NONE					R	R
X	0h					X	X
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						CBA_ERR_STAT_MAIN_MEM_CBA_ERR	CBA_ERR_STAT_MAIN_AUDIO_CBA_ERR
NONE						R	R
0h						X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		CBA_ERR_STAT_MAIN_IPCSS_CBA_ERR	RESERVED	CBA_ERR_STAT_MAIN_MISC_PERI_CBA_ERR	RESERVED		
NONE		R	NONE	R	NONE		
0h		X	0h	X	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CBA_ERR_STAT_MAIN_FW_CBA_ERR	CBA_ERR_STAT_MAIN_DATA_CBA_ERR	CBA_ERR_STAT_MAIN_CENTRAL_CBA_ERR	RESERVED		CBA_ERR_STAT_MAIN_INFRA_CBA_ERR
NONE		R	R	R	NONE		R
0h		X	X	X	0h		X

Table 14-5521. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CBA_ERR_STAT_DBG_CBA_ERR	R	X	Access Error from Main Debug CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	CBA_ERR_STAT_WKUP_DM_CBA_ERR	R	X	Access Error from Wkup Device Manager CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n

Table 14-5521. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR	R	X	Access Error from Wkup Safe CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17	CBA_ERR_STAT_MAIN_MEM_CBA_ERR	R	X	Access Error from Main MEM CBASS Reset Source: mod_g_rst_n
16	CBA_ERR_STAT_MAIN_AUDIO_CBA_ERR	R	X	Access Error from Main Audio CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	CBA_ERR_STAT_MAIN_IPCSS_CBA_ERR	R	X	Access Error from Main IPCSS CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
12	RESERVED	NONE	0h	Reserved
11	CBA_ERR_STAT_MAIN_MISC_PERI_CBA_ERR	R	X	Access Errror from Main Misc. Peripheral CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
10:6	RESERVED	NONE	0h	Reserved
5	CBA_ERR_STAT_MAIN_FW_CBA_ERR	R	X	Access Error from Main Firewall CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
4	CBA_ERR_STAT_MAIN_DATA_CBA_ERR	R	X	Access Error from Main Data CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
3	CBA_ERR_STAT_MAIN_CENTRAL_CBA_ERR	R	X	Access Error from Main Central CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	CBA_ERR_STAT_MAIN_INFRA_CBA_ERR	R	X	Access Error from Main Infrastructure CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n

14.2.1.1.3.2.20 WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register

14.2.1.1.3.2.20.1 WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register (Offset = 280h) [reset = 0h]

Provides Aggregated, Read Only status of access error interrupts reported by MMR components.. Processors on the SoC read this MMR to determine which MMR components require service. Actual service of MMR interrupts must be handled through each MMR component.

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Table 14-5522. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 0280h

Figure 14-2748. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ACCESS_ERR_STAT_ACCESS_ERR_IN9	ACCESS_ERR_STAT_ACCESS_ERR_IN8
NONE						R	R
0h						X	X
7	6	5	4	3	2	1	0
RESERVED			ACCESS_ERR_STAT_ACCESS_ERR_IN4	ACCESS_ERR_STAT_ACCESS_ERR_IN3	RESERVED		ACCESS_ERR_STAT_ACCESS_ERR_IN0
NONE			R	R	NONE		R
0h			X	X	0h		X

Table 14-5523. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ACCESS_ERR_STAT_ACCESS_ERR_IN9	R	X	Access Error Detected in MCU PadCfg MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n
8	ACCESS_ERR_STAT_ACCESS_ERR_IN8	R	X	Access Error Detected in MCU Ctrl MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	ACCESS_ERR_STAT_ACCESS_ERR_IN4	R	X	Access Error Detected in MAIN PadCfg MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n

Table 14-5523. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ACCESS_ERR_STAT_ACCESS_ERR_IN3	R	X	Access Error Detected in MAIN Ctrl MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	ACCESS_ERR_STAT_ACCESS_ERR_IN0	R	X	Access Error Detected in WKUP Ctrl MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n

14.2.1.1.3.2.21 WKUP_CTRL_MMR_CFG0_LOCK0_KICK0 Register

14.2.1.1.3.2.21.1 WKUP_CTRL_MMR_CFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-5524. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1008h

Figure 14-2749. WKUP_CTRL_MMR_CFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-5525. WKUP_CTRL_MMR_CFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.22 WKUP_CTRL_MMR_CFG0_LOCK0_KICK1 Register

14.2.1.1.3.2.22.1 WKUP_CTRL_MMR_CFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-5526. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 100Ch

Figure 14-2750. WKUP_CTRL_MMR_CFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-5527. WKUP_CTRL_MMR_CFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.23 WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS Register

14.2.1.1.3.2.23.1 WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-5528. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1010h

Figure 14-2751. WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5529. WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.24 WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register

14.2.1.1.3.2.24.1 WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-5530. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1014h

Figure 14-2752. WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5531. WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.25 WKUP_CTRL_MMR_CFG0_INTR_ENABLE Register

14.2.1.1.3.2.25.1 WKUP_CTRL_MMR_CFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-5532. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1018h

Figure 14-2753. WKUP_CTRL_MMR_CFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5533. WKUP_CTRL_MMR_CFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.26 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register

14.2.1.1.3.2.26.1 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-5534. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 101Ch

Figure 14-2754. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5535. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.27 WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS Register

14.2.1.1.3.2.27.1 WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-5536. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1024h

Figure 14-2755. WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-5537. WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.3.2.28 WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register

14.2.1.1.3.2.28.1 WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-5538. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1028h

Figure 14-2756. WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-5539. WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.3.2.29 WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register

14.2.1.1.3.2.29.1 WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-5540. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 102Ch

Figure 14-2757. WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID</td><td colspan="4">FAULT_ROUTEID</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5541. WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.3.2.30 WKUP_CTRL_MMR_CFG0_FAULT_CLEAR Register

14.2.1.1.3.2.30.1 WKUP_CTRL_MMR_CFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-5542. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1030h

Figure 14-2758. WKUP_CTRL_MMR_CFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-5543. WKUP_CTRL_MMR_CFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.31 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register

14.2.1.1.3.2.31.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5544. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1100h

Figure 14-2759. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-5545. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.32 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register

14.2.1.1.3.2.32.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register (Offset = 1110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5546. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1110h

Figure 14-2760. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P0_R4_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5547. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.33 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register

14.2.1.1.3.2.33.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register (Offset = 1114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5548. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 1114h

Figure 14-2761. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5_READONLY							
R							
0h							

Table 14-5549. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.34 WKUP_CTRL_MMR_CFG0_PID_PROXY Register

14.2.1.1.3.2.34.1 WKUP_CTRL_MMR_CFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800215h]

PID register

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Table 14-5550. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2000h

Figure 14-2762. WKUP_CTRL_MMR_CFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MSB16_PROXY							
R							
6180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		15h					

Table 14-5551. WKUP_CTRL_MMR_CFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	15h	Reset Source: mod_g_rst_n

14.2.1.1.3.2.35 WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register

14.2.1.1.3.2.35.1 WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 800000DFh]

Indicates the MMR configuration

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Table 14-5552. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2008h

Figure 14-2763. WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS_PROXY							
R							
DFh							

Table 14-5553. WKUP_CTRL_MMR_CFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	DFh	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.1.3.2.36 WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register

14.2.1.1.3.2.36.1 WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register (Offset = 2044h) [reset = 0h]

Used by ROM to mark the progress of the boot operation

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Table 14-5554. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2044h

Figure 14-2764. WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Name Register

31	30	29	28	27	26	25	24
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
BOOT_PROGRESS_PROGRESS_PROXY							
R/W							
0h							

Table 14-5555. WKUP_CTRL_MMR_CFG0_BOOT_PROGRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BOOT_PROGRESS_PROGRESS_PROXY	R/W	0h	Written by ROM to indicate boot progression. Values and their meaning are determined by the ROM. Reset Source: mod_por_rst_n

14.2.1.1.3.2.37 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register

14.2.1.1.3.2.37.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register (Offset = 2060h) [reset = 0h]

Indicates enabled Main Domain processing elements on the device

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Table 14-5556. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2060h

Figure 14-2765. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				DEVICE_FEATURE0_R5FSS1_CORE1_PROXY	DEVICE_FEATURE0_R5FSS1_CORE0_PROXY	DEVICE_FEATURE0_R5FSS0_CORE1_PROXY	DEVICE_FEATURE0_R5FSS0_CORE0_PROXY
NONE				R	R	R	R
0h				X	X	X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5557. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	DEVICE_FEATURE0_R5FSS1_CORE1_PROXY	R	X	Main R5FSS1 dual/single core support Field values (others are reserved): 1'b0 - Single core 1'b1 - Dual core Reset Source: mod_por_rst_n
18	DEVICE_FEATURE0_R5FSS1_CORE0_PROXY	R	X	Main R5SS1 avalability Field values (others are reserved): 1'b0 - Cluster not available 1'b1 - Cluster available Reset Source: mod_por_rst_n
17	DEVICE_FEATURE0_R5FSS0_CORE1_PROXY	R	X	Main R5FSS0 dual/single core support Field values (others are reserved): 1'b0 - Single core 1'b1 - Dual core Reset Source: mod_por_rst_n

Table 14-5557. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	DEVICE_FEATURE0_R5FSS0_CORE0_PROXY	R	X	Main R5SS0 avalability Field values (others are reserved): 1'b0 - Cluster not available 1'b1 - Cluster available Reset Source: mod_por_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.38 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Register

14.2.1.1.3.2.38.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Register (Offset = 2064h) [reset = 0h]

Indicates enabled Main Domain DSP processing elements on the device

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Table 14-5558. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2064h

Figure 14-2766. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						DEVICE_FEATURE1_C7X_CORE1_PROXY	DEVICE_FEATURE1_C7X_CORE0_PROXY
NONE						R	R
0h						X	X
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5559. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	DEVICE_FEATURE1_C7X_CORE1_PROXY	R	X	C7x1 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
16	DEVICE_FEATURE1_C7X_CORE0_PROXY	R	X	C7x0 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.39 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register

14.2.1.1.3.2.39.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register (Offset = 2068h) [reset = 0h]

Indicates enabled interface elements on the device

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Table 14-5560. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2068h

Figure 14-2767. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				DEVICE_FEATURE2_CRYPTO_SM_EN_PROXY	DEVICE_FEATURE2_CRYPTO_PKA_EN_PROXY	DEVICE_FEATURE2_CRYPTO_ENCR_EN_PROXY	DEVICE_FEATURE2_CRYPTO_SHA_EN_PROXY
NONE				R	R	R	R
0h				X	X	X	X
7	6	5	4	3	2	1	0
DEVICE_FEATURE2_AES_AUTH_EN_PROXY	RESERVED						DEVICE_FEATURE2_MCAN_FD_MODE_PROXY
R	NONE						R
X	0h						X

Table 14-5561. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	DEVICE_FEATURE2_CRYPTO_SM_EN_PROXY	R	X	Crypto Module SM2, SM3, SM4 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
10	DEVICE_FEATURE2_CRYPTO_PKA_EN_PROXY	R	X	Crypto Module PKA Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
9	DEVICE_FEATURE2_CRYPTO_ENCR_EN_PROXY	R	X	Crypto Module AES/3DES/DBRG Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

Table 14-5561. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE2_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DEVICE_FEATURE2_CRYPTO_SHA_EN_PROXY	R	X	Crypto Module SHA/MD5 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
7	DEVICE_FEATURE2_AES_AUTH_EN_PROXY	R	X	AES authentication availability in FlashSS and SMS Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
6:1	RESERVED	NONE	0h	Reserved
0	DEVICE_FEATURE2_MCAN_FD_MODE_PROXY	R	X	FD mode availability (applies to all MCAN instances) Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

14.2.1.1.3.2.40 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY Register

14.2.1.1.3.2.40.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY Register (Offset = 206Ch) [reset = 0h]

Indicates enabled processing element features on the device

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Table 14-5562. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 206Ch

Figure 14-2768. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						DEVICE_FEATURE3_MMA1_PRESENT_PROXY	DEVICE_FEATURE3_MMA0_PRESENT_PROXY
NONE						R	R
0h						X	X

Table 14-5563. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DEVICE_FEATURE3_MMA1_PRESENT_PROXY	R	X	C7x1 MMA Feature Availability Reset Source: mod_por_rst_n
0	DEVICE_FEATURE3_MMA0_PRESENT_PROXY	R	X	C7x0 MMA Feature Availability Reset Source: mod_por_rst_n

14.2.1.1.3.2.41 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5_PROXY Register

14.2.1.1.3.2.41.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5_PROXY Register (Offset = 2074h) [reset = 0h]

Indicates enabled interface elements on the device

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Table 14-5564. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2074h

Figure 14-2769. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED			DEVICE_FEATURE5_MCAN4_PROXY	DEVICE_FEATURE5_MCAN3_PROXY	DEVICE_FEATURE5_MCAN2_PROXY	DEVICE_FEATURE5_MCAN1_PROXY	DEVICE_FEATURE5_MCAN0_PROXY
NONE			R	R	R	R	R
0h			X	X	X	X	X

Table 14-5565. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DEVICE_FEATURE5_MCAN4_PROXY	R	X	MCAN4 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
3	DEVICE_FEATURE5_MCAN3_PROXY	R	X	MCAN3 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
2	DEVICE_FEATURE5_MCAN2_PROXY	R	X	MCAN2 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
1	DEVICE_FEATURE5_MCAN1_PROXY	R	X	MCAN1 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

Table 14-5565. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE5_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DEVICE_FEATURE5_MCAN0_PROXY	R	X	MCAN0 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

14.2.1.1.3.2.42 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register

14.2.1.1.3.2.42.1 WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register (Offset = 2078h) [reset = 0h]

Indicates enabled interface elements on the device

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Table 14-5566. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2078h

Figure 14-2770. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
X	X	X	X	X	X	X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					DEVICE_FEATURE6_ASRC1_PROXY	DEVICE_FEATURE6_ASRC0_PROXY	RESERVED
NONE					R	R	NONE
0h					X	X	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEVICE_FEATURE6_ATL_PROXY	DEVICE_FEATURE6_MLB_PROXY	DEVICE_FEATURE6_SA3_UL_PROXY	RESERVED				
R	R	R	NONE				
X	X	X	0h				

Table 14-5567. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
15:11	RESERVED	NONE	0h	Reserved
10	DEVICE_FEATURE6_ASRC1_PROXY	R	X	ASRC1 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
9	DEVICE_FEATURE6_ASRC0_PROXY	R	X	ASRC0 Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
8	RESERVED	NONE	0h	Reserved
7	DEVICE_FEATURE6_ATL_PROXY	R	X	Audio Tracking Logic Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n

Table 14-5567. WKUP_CTRL_MMR_CFG0_DEVICE_FEATURE6_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DEVICE_FEATURE6_MLB_PROXY	R	X	Medis Local Bus Availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
5	DEVICE_FEATURE6_SA3_UL_PROXY	R	X	SA3SS domain security accelerator availability Field values (others are reserved): 1'b0 - Not available 1'b1 - Available Reset Source: mod_por_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.43 WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY Register

14.2.1.1.3.2.43.1 WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY Register (Offset = 2200h) [reset = 0h]

Ethernet MAC address lower 32-bits

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Table 14-5568. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2200h

Figure 14-2771. WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY Name Register

31	30	29	28	27	26	25	24
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
23	22	21	20	19	18	17	16
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
15	14	13	12	11	10	9	8
MAC_ID0_MACID_LO_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID0_MACID_LO_PROXY							
R/W							
X							

Table 14-5569. WKUP_CTRL_MMR_CFG0_MAC_ID0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAC_ID0_MACID_LO_PROXY	R/W	X	32 lsbs of MAC address Reset Source: mod_g_rst_n

14.2.1.1.3.2.44 WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY Register

14.2.1.1.3.2.44.1 WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY Register (Offset = 2204h) [reset = 0h]

Ethernet MAC address upper 16-bits

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Table 14-5570. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2204h

Figure 14-2772. WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ID1_MACID_HI_PROXY							
R/W							
X							
7	6	5	4	3	2	1	0
MAC_ID1_MACID_HI_PROXY							
R/W							
X							

Table 14-5571. WKUP_CTRL_MMR_CFG0_MAC_ID1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAC_ID1_MACID_HI_PROXY	R/W	X	16 msbs of MAC address Reset Source: mod_g_rst_n

14.2.1.1.3.2.45 WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register

14.2.1.1.3.2.45.1 WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register (Offset = 2220h) [reset = 61650451h]

USB device and vendor ID register 0 (ROM Writes)

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Table 14-5572. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2220h

Figure 14-2773. WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Name Register

31	30	29	28	27	26	25	24
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
23	22	21	20	19	18	17	16
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
15	14	13	12	11	10	9	8
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							
7	6	5	4	3	2	1	0
USB_DEVICE_ID0_ID0_PROXY							
R/W							
61650451h							

Table 14-5573. WKUP_CTRL_MMR_CFG0_USB_DEVICE_ID0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USB_DEVICE_ID0_ID0_PROXY	R/W	61650451h	ROM writes 32-bit Value from Customer OTP to Here Reset Source: mod_g_rst_n

14.2.1.1.3.2.46 WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY Register

14.2.1.1.3.2.46.1 WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY Register (Offset = 2230h) [reset = 0h]

Allocated for customer use - Ex. Storage of PID/VID, Model #, Etc.

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Table 14-5574. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2230h

Figure 14-2774. WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY Name Register

31	30	29	28	27	26	25	24
GP_SW0_VAL_PROXY							
R							
X							
23	22	21	20	19	18	17	16
GP_SW0_VAL_PROXY							
R							
X							
15	14	13	12	11	10	9	8
GP_SW0_VAL_PROXY							
R							
X							
7	6	5	4	3	2	1	0
GP_SW0_VAL_PROXY							
R							
X							

Table 14-5575. WKUP_CTRL_MMR_CFG0_GP_SW0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GP_SW0_VAL_PROXY	R	X	general purpose value Reset Source: mod_por_rst_n

14.2.1.1.3.2.47 WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY Register

14.2.1.1.3.2.47.1 WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY Register (Offset = 2234h) [reset = 0h]

Allocated for customer use - Ex. Storage of PID/VID, Model #, Etc.

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Table 14-5576. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2234h

Figure 14-2775. WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY Name Register

31	30	29	28	27	26	25	24
GP_SW1_VAL_PROXY							
R							
X							
23	22	21	20	19	18	17	16
GP_SW1_VAL_PROXY							
R							
X							
15	14	13	12	11	10	9	8
GP_SW1_VAL_PROXY							
R							
X							
7	6	5	4	3	2	1	0
GP_SW1_VAL_PROXY							
R							
X							

Table 14-5577. WKUP_CTRL_MMR_CFG0_GP_SW1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GP_SW1_VAL_PROXY	R	X	general purpose value Reset Source: mod_por_rst_n

14.2.1.1.3.2.48 WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY Register

14.2.1.1.3.2.48.1 WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY Register (Offset = 2238h) [reset = 0h]

Allocated for customer use - Ex. Storage of PID/VID, Model #, Etc.

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Table 14-5578. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2238h

Figure 14-2776. WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY Name Register

31	30	29	28	27	26	25	24
GP_SW2_VAL_PROXY							
R							
X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GP_SW2_VAL_PROXY							
R							
X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GP_SW2_VAL_PROXY							
R							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GP_SW2_VAL_PROXY							
R							
X							

Table 14-5579. WKUP_CTRL_MMR_CFG0_GP_SW2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GP_SW2_VAL_PROXY	R	X	general purpose value Reset Source: mod_por_rst_n

14.2.1.1.3.2.49 WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY Register

14.2.1.1.3.2.49.1 WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY Register (Offset = 223Ch) [reset = 0h]

Allocated for customer use - Ex. Storage of PID/VID, Model #, Etc.

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Table 14-5580. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 223Ch

Figure 14-2777. WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				GP_SW3_VAL_PROXY			
NONE				R			
0h				X			

Table 14-5581. WKUP_CTRL_MMR_CFG0_GP_SW3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	GP_SW3_VAL_PROXY	R	X	general purpose value Reset Source: mod_por_rst_n

14.2.1.1.3.2.50 WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register

14.2.1.1.3.2.50.1 WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register (Offset = 2270h) [reset = 0h]

Provides Aggregated, Read Only status of bus address error interrupts reported by CBASS components.. Processors on the SoC read this MMR to determine which CBASS components require service. Actual service of CBASS interrupts must be handled through each CBASS component.

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Table 14-5582. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2270h

Figure 14-2778. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
CBA_ERR_STAT_DBG_CBA_ERR_PROXY	RESERVED					CBA_ERR_STAT_WKUP_DM_CBA_ERR_PROXY	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR_PROXY
R	NONE					R	R
X	0h					X	X

23	22	21	20	19	18	17	16
RESERVED						CBA_ERR_STAT_MAIN_MEM_CBA_ERR_PROXY	CBA_ERR_STAT_MAIN_AUDIO_CBA_ERR_PROXY
NONE						R	R
0h						X	X

15	14	13	12	11	10	9	8
RESERVED		CBA_ERR_STAT_MAIN_IPCSS_CBA_ERR_PROXY	RESERVED	CBA_ERR_STAT_MAIN_MISC_PERI_CBA_ERR_PROXY	RESERVED		
NONE		R	NONE	R	NONE		
0h		X	0h	X	0h		

7	6	5	4	3	2	1	0
RESERVED		CBA_ERR_STAT_MAIN_FW_CBA_ERR_PROXY	CBA_ERR_STAT_MAIN_DATA_CBA_ERR_PROXY	CBA_ERR_STAT_MAIN_CENTRAL_CBA_ERR_PROXY	RESERVED		CBA_ERR_STAT_MAIN_INFRA_CBA_ERR_PROXY
NONE		R	R	R	NONE		R
0h		X	X	X	0h		X

Table 14-5583. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CBA_ERR_STAT_DBG_CBA_ERR_PROXY	R	X	Access Error from Main Debug CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	CBA_ERR_STAT_WKUP_DM_CBA_ERR_PROXY	R	X	Access Error from Wkup Device Manager CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n

Table 14-5583. WKUP_CTRL_MMR_CFG0_CBA_ERR_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CBA_ERR_STAT_WKUP_SAFE_CBA_ERR_PROXY	R	X	Access Error from Wkup Safe CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
23:18	RESERVED	NONE	0h	Reserved
17	CBA_ERR_STAT_MAIN_MEM_CBA_ERR_PROXY	R	X	Access Error from Main MEM CBASS Reset Source: mod_g_rst_n
16	CBA_ERR_STAT_MAIN_AUDIO_CBA_ERR_PROXY	R	X	Access Error from Main Audio CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	CBA_ERR_STAT_MAIN_IPCSS_CBA_ERR_PROXY	R	X	Access Error from Main IPCSS CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
12	RESERVED	NONE	0h	Reserved
11	CBA_ERR_STAT_MAIN_MISC_PERI_CBA_ERR_PROXY	R	X	Access Errror from Main Misc. Peripheral CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
10:6	RESERVED	NONE	0h	Reserved
5	CBA_ERR_STAT_MAIN_FW_CBA_ERR_PROXY	R	X	Access Error from Main Firewall CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
4	CBA_ERR_STAT_MAIN_DATA_CBA_ERR_PROXY	R	X	Access Error from Main Data CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
3	CBA_ERR_STAT_MAIN_CENTRAL_CBA_ERR_PROXY	R	X	Access Error from Main Central CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	CBA_ERR_STAT_MAIN_INFRA_CBA_ERR_PROXY	R	X	Access Error from Main Infrastructure CBASS Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n

14.2.1.1.3.2.51 WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register

14.2.1.1.3.2.51.1 WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register (Offset = 2280h) [reset = 0h]

Provides Aggregated, Read Only status of access error interrupts reported by MMR components.. Processors on the SoC read this MMR to determine which MMR components require service. Actual service of MMR interrupts must be handled through each MMR component.

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Table 14-5584. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 2280h

Figure 14-2779. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ACCESS_ERR_STAT_ACCESS_ERR_IN9_PROXY	ACCESS_ERR_STAT_ACCESS_ERR_IN8_PROXY
NONE						R	R
0h						X	X
7	6	5	4	3	2	1	0
RESERVED			ACCESS_ERR_STAT_ACCESS_ERR_IN4_PROXY	ACCESS_ERR_STAT_ACCESS_ERR_IN3_PROXY	RESERVED		ACCESS_ERR_STAT_ACCESS_ERR_IN0_PROXY
NONE			R	R	NONE		R
0h			X	X	0h		X

Table 14-5585. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ACCESS_ERR_STAT_ACCESS_ERR_IN9_PROXY	R	X	Access Error Detected in MCU PadCfg MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n
8	ACCESS_ERR_STAT_ACCESS_ERR_IN8_PROXY	R	X	Access Error Detected in MCU Ctrl MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved

Table 14-5585. WKUP_CTRL_MMR_CFG0_ACCESS_ERR_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ACCESS_ERR_STAT_ACCESS_ERR_IN4_PROXY	R	X	Access Error Detected in MAIN PadCfg MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n
3	ACCESS_ERR_STAT_ACCESS_ERR_IN3_PROXY	R	X	Access Error Detected in MAIN Ctrl MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n
2:1	RESERVED	NONE	0h	Reserved
0	ACCESS_ERR_STAT_ACCESS_ERR_IN0_PROXY	R	X	Access Error Detected in WKUP Ctrl MMR Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_por_rst_n

14.2.1.1.3.2.52 WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register

14.2.1.1.3.2.52.1 WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-5586. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3008h

Figure 14-2780. WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-5587. WKUP_CTRL_MMR_CFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.53 WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register

14.2.1.1.3.2.53.1 WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-5588. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 300Ch

Figure 14-2781. WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-5589. WKUP_CTRL_MMR_CFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.54 WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register

14.2.1.1.3.2.54.1 WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-5590. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3010h

Figure 14-2782. WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5591. WKUP_CTRL_MMR_CFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.55 WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

14.2.1.1.3.2.55.1 WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-5592. Instance Table

Instance Name	**Physical Address**
WKUP_CTRL_MMR0	4300 3014h

Figure 14-2783. WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5593. WKUP_CTRL_MMR_CFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.56 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register

14.2.1.1.3.2.56.1 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-5594. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3018h

Figure 14-2784. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-5595. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.57 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register

14.2.1.1.3.2.57.1 WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-5596. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 301Ch

Figure 14-2785. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-5597. WKUP_CTRL_MMR_CFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.58 WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register

14.2.1.1.3.2.58.1 WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-5598. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3024h

Figure 14-2786. WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-5599. WKUP_CTRL_MMR_CFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.1.3.2.59 WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register

14.2.1.1.3.2.59.1 WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-5600. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3028h

Figure 14-2787. WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-5601. WKUP_CTRL_MMR_CFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.1.3.2.60 WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register

14.2.1.1.3.2.60.1 WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-5602. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 302Ch

Figure 14-2788. WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID_PROXY</td><td colspan="4">FAULT_ROUTEID_PROXY</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5603. WKUP_CTRL_MMR_CFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.1.3.2.61 WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register

14.2.1.1.3.2.61.1 WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-5604. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3030h

Figure 14-2789. WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-5605. WKUP_CTRL_MMR_CFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.1.3.2.62 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register

14.2.1.1.3.2.62.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5606. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3100h

Figure 14-2790. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-5607. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.63 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register

14.2.1.1.3.2.63.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register (Offset = 3104h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5608. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3104h

Figure 14-2791. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R1							
R/W							
0h							

Table 14-5609. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R1	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.64 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register

14.2.1.1.3.2.64.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register (Offset = 3108h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5610. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3108h

Figure 14-2792. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R2							
R/W							
0h							

Table 14-5611. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R2	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.65 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register

14.2.1.1.3.2.65.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register (Offset = 310Ch) [reset = 0h]

Claim bits for Partition 0

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Table 14-5612. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 310Ch

Figure 14-2793. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R3							
R/W							
0h							

Table 14-5613. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R3	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.66 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register

14.2.1.1.3.2.66.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register (Offset = 3110h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5614. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3110h

Figure 14-2794. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R4							
R/W							
0h							

Table 14-5615. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R4	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.67 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register

14.2.1.1.3.2.67.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register (Offset = 3114h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5616. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3114h

Figure 14-2795. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R5							
R/W							
0h							

Table 14-5617. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R5	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.68 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register

14.2.1.1.3.2.68.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register (Offset = 3118h) [reset = 0h]

Claim bits for Partition 0

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Table 14-5618. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 3118h

Figure 14-2796. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R6							
R/W							
0h							

Table 14-5619. WKUP_CTRL_MMR_CFG0_CLAIMREG_P0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R6	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.69 WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Register

14.2.1.1.3.2.69.1 WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Register (Offset = 4008h) [reset = 80000006h]

Configures the USB0 Phy operation

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Table 14-5620. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 4008h

Figure 14-2797. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Name Register

31	30	29	28	27	26	25	24
USB0_PHY_CTRL_CORE_VOLTAGE	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				USB0_PHY_CTRL_PLL_REF_SEL			
NONE				R/W			
0h				6h			

Table 14-5621. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	USB0_PHY_CTRL_CORE_VOLTAGE	R/W	1h	Selects the USB PHY Core Voltage Option: 0.85V or 0.75/0.80V Field values (others are reserved): 1'b0 - V_0P85 1'b1 - V_0P75_0P80 Reset Source: mod_g_rst_n
30:4	RESERVED	NONE	0h	Reserved

Table 14-5621. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	USB0_PHY_CTRL_PLL_REF_SEL	R/W	6h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should be set to match the frequency of the USB0 input clock, as selected by the USB0_CLKSEL register Field values (others are reserved): 4'b0000 - MHZ_9P6 4'b0001 - MHZ_10 4'b0010 - MHZ_12 4'b0011 - MHZ_19P2 4'b0100 - MHZ_20 4'b0101 - MHZ_24 4'b0110 - MHZ_25 4'b0111 - MHZ_26 4'b1000 - MHZ_38P4 4'b1001 - MHZ_40 4'b1010 - MHZ_48 4'b1011 - MHZ_50 4'b1100 - MHZ_52 Reset Source: mod_g_rst_n

14.2.1.1.3.2.70 WKUP_CTRL_MMR_CFG0_SDIO0_CTRL Register

14.2.1.1.3.2.70.1 WKUP_CTRL_MMR_CFG0_SDIO0_CTRL Register (Offset = 41B4h) [reset = 0h]

Controls drive strength of MMC0 SDIO mode pins

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Table 14-5622. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 41B4h

Figure 14-2798. WKUP_CTRL_MMR_CFG0_SDIO0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO0_CTRL_DRV_STR				
NONE			R/W				
0h			X				

Table 14-5623. WKUP_CTRL_MMR_CFG0_SDIO0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO0_CTRL_DRV_STR	R/W	X	Selects the SDIO pin drive strength. The default value trims the buffers for ~40 ohms. For options other than the Reset/Default 40 ohm, the register value should be modified as follows: 40 ohms - Default Value 33 ohms - Default Value + 5 50 ohms - Default Value -5 66 ohms - Default Value -10 Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.3.2.71 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL Register

14.2.1.1.3.2.71.1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL Register (Offset = 4204h) [reset = 0h]

Controls TIMER1 operation

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Table 14-5624. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 4204h

Figure 14-2799. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							WKUP_TIMER1_CTRL_CASCADE_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5625. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	WKUP_TIMER1_CTRL_CASCADE_EN	R/W	0h	Enables cascading of TIMER1 to TIMER0 Field values (others are reserved): 1'b0 - CASCADE_DISABLED 1'b1 - CASCADE_ENABLED Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.72 WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL Register

14.2.1.1.3.2.72.1 WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL Register (Offset = 42E0h) [reset = 0h]

Controls I2C0 operation for open drain I/Os

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Table 14-5626. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 42E0h

Figure 14-2800. WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_I2C0_CTRL_HS_MCS_EN
NONE							R/W
0h							0h

Table 14-5627. WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_I2C0_CTRL_HS_MCS_EN	R/W	0h	HS Mode controller current source enable. When set, enables the current-source pull-up on the SCL output. Only one controller on the I2C bus should enable SCL current sourcing. Field values (others are reserved): 1'b0 - HS_MCS_INACTIVE 1'b1 - HS_MCS_ACTIVE Reset Source: mod_g_rst_n

14.2.1.1.3.2.73 WKUP_CTRL_MMR_CFG0_LOCK1_KICK0 Register

14.2.1.1.3.2.73.1 WKUP_CTRL_MMR_CFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-5628. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 5008h

Figure 14-2801. WKUP_CTRL_MMR_CFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-5629. WKUP_CTRL_MMR_CFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.74 WKUP_CTRL_MMR_CFG0_LOCK1_KICK1 Register

14.2.1.1.3.2.74.1 WKUP_CTRL_MMR_CFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-5630. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 500Ch

Figure 14-2802. WKUP_CTRL_MMR_CFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-5631. WKUP_CTRL_MMR_CFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.75 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register

14.2.1.1.3.2.75.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5632. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 5100h

Figure 14-2803. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-5633. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.76 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register

14.2.1.1.3.2.76.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5634. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 510Ch

Figure 14-2804. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-5635. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.77 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register

14.2.1.1.3.2.77.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5636. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 5110h

Figure 14-2805. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-5637. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.78 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register

14.2.1.1.3.2.78.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register (Offset = 5114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5638. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 5114h

Figure 14-2806. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R5_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5639. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.79 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register

14.2.1.1.3.2.79.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register (Offset = 5130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5640. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 5130h

Figure 14-2807. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R12_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R12_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R12_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R12_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5641. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.80 WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register

14.2.1.1.3.2.80.1 WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register (Offset = 6008h) [reset = 80000006h]

Configures the USB0 Phy operation

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Table 14-5642. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 6008h

Figure 14-2808. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
USB0_PHY_CTRL_CORE_VOLTAGE_PROXY	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				USB0_PHY_CTRL_PLL_REF_SEL_PROXY			
NONE				R/W			
0h				6h			

Table 14-5643. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	USB0_PHY_CTRL_CORE_VOLTAGE_PROXY	R/W	1h	Selects the USB PHY Core Voltage Option: 0.85V or 0.75/0.80V Field values (others are reserved): 1'b0 - V_0P85 1'b1 - V_0P75_0P80 Reset Source: mod_g_rst_n
30:4	RESERVED	NONE	0h	Reserved

Table 14-5643. WKUP_CTRL_MMR_CFG0_USB0_PHY_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	USB0_PHY_CTRL_PLL_ REF_SEL_PROXY	R/W	6h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value should be set to match the frequency of the USB0 input clock, as selected by the USB0_CLKSEL register Field values (others are reserved): 4'b0000 - MHZ_9P6 4'b0001 - MHZ_10 4'b0010 - MHZ_12 4'b0011 - MHZ_19P2 4'b0100 - MHZ_20 4'b0101 - MHZ_24 4'b0110 - MHZ_25 4'b0111 - MHZ_26 4'b1000 - MHZ_38P4 4'b1001 - MHZ_40 4'b1010 - MHZ_48 4'b1011 - MHZ_50 4'b1100 - MHZ_52 Reset Source: mod_g_rst_n

14.2.1.1.3.2.81 WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY Register

14.2.1.1.3.2.81.1 WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY Register (Offset = 61B4h) [reset = 0h]

Controls drive strength of MMC0 SDIO mode pins

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Table 14-5644. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 61B4h

Figure 14-2809. WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SDIO0_CTRL_DRV_STR_PROXY				
NONE			R/W				
0h			X				

Table 14-5645. WKUP_CTRL_MMR_CFG0_SDIO0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	SDIO0_CTRL_DRV_STR_PROXY	R/W	X	Selects the SDIO pin drive strength. The default value trims the buffers for ~40 ohms. For options other than the Reset/Default 40 ohm, the register value should be modified as follows: 40 ohms - Default Value 33 ohms - Default Value + 5 50 ohms - Default Value -5 66 ohms - Default Value -10 Note: Values other than the reset value may invalidate the datasheet timing parameters and therefore should not be used. Reset Source: mod_por_rst_n

14.2.1.1.3.2.82 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY Register

14.2.1.1.3.2.82.1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY Register (Offset = 6204h) [reset = 0h]

Controls TIMER1 operation

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Table 14-5646. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 6204h

Figure 14-2810. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							WKUP_TIMER1_CTRL_CASCADE_EN_PROXY
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5647. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	WKUP_TIMER1_CTRL_CASCADE_EN_PROXY	R/W	0h	Enables cascading of TIMER1 to TIMER0 Field values (others are reserved): 1'b0 - CASCADE_DISABLED 1'b1 - CASCADE_ENABLED Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.83 WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY Register

14.2.1.1.3.2.83.1 WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY Register (Offset = 62E0h) [reset = 0h]

Controls I2C0 operation for open drain I/Os

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Table 14-5648. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 62E0h

Figure 14-2811. WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_I2C0_CTRL_HS_MCS_EN_PROXY
NONE							R/W
0h							0h

Table 14-5649. WKUP_CTRL_MMR_CFG0_WKUP_I2C0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_I2C0_CTRL_HS_MCS_EN_PROXY	R/W	0h	HS Mode controller current source enable. When set, enables the current-source pull-up on the SCL output. Only one controller on the I2C bus should enable SCL current sourcing. Field values (others are reserved): 1'b0 - HS_MCS_INACTIVE 1'b1 - HS_MCS_ACTIVE Reset Source: mod_g_rst_n

14.2.1.1.3.2.84 WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register

14.2.1.1.3.2.84.1 WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-5650. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7008h

Figure 14-2812. WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-5651. WKUP_CTRL_MMR_CFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.85 WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register

14.2.1.1.3.2.85.1 WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-5652. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 700Ch

Figure 14-2813. WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-5653. WKUP_CTRL_MMR_CFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.86 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register

14.2.1.1.3.2.86.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5654. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7100h

Figure 14-2814. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-5655. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.87 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register

14.2.1.1.3.2.87.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5656. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7104h

Figure 14-2815. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-5657. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.88 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register

14.2.1.1.3.2.88.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5658. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7108h

Figure 14-2816. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-5659. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.89 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register

14.2.1.1.3.2.89.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5660. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 710Ch

Figure 14-2817. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5661. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.90 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register

14.2.1.1.3.2.90.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5662. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7110h

Figure 14-2818. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-5663. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.91 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register

14.2.1.1.3.2.91.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5664. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7114h

Figure 14-2819. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-5665. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.92 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register

14.2.1.1.3.2.92.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register (Offset = 7118h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5666. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7118h

Figure 14-2820. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R6							
R/W							
0h							

Table 14-5667. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R6	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.93 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register

14.2.1.1.3.2.93.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register (Offset = 711Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5668. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 711Ch

Figure 14-2821. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5669. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R7	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.94 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register

14.2.1.1.3.2.94.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register (Offset = 7120h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5670. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7120h

Figure 14-2822. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R8							
R/W							
0h							

Table 14-5671. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R8	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.95 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register

14.2.1.1.3.2.95.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register (Offset = 7124h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5672. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7124h

Figure 14-2823. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R9							
R/W							
0h							

Table 14-5673. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R9	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.96 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register

14.2.1.1.3.2.96.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register (Offset = 7128h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5674. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7128h

Figure 14-2824. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R10							
R/W							
0h							

Table 14-5675. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R10	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.97 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register

14.2.1.1.3.2.97.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register (Offset = 712Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-5676. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 712Ch

Figure 14-2825. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5677. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R11	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.98 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register

14.2.1.1.3.2.98.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register (Offset = 7130h) [reset = 0h]

Claim bits for Partition 1

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Table 14-5678. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 7130h

Figure 14-2826. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R12							
R/W							
0h							

Table 14-5679. WKUP_CTRL_MMR_CFG0_CLAIMREG_P1_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R12	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.1.3.2.99 WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL Register

14.2.1.1.3.2.99.1 WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL Register (Offset = 8010h) [reset = 0h]

Selects the functional clock source for the WKUP Domain

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Table 14-5680. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 8010h

Figure 14-2827. WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							WKUP_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5681. WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_CLKSEL_CLK_SEL	R/W	0h	Selects Clock Source for Wakeup Domain (Device Manager and Peripherals) Field values (others are reserved): 1'b0 - CPU_MAIN_PLL15_HSDIV2_CLKOUT__PERIPHERALS_MAIN_PLL15_HSDIV0_CLKOUT 1'b0 - MAIN_PLL15_HSDIV0_CLKOUT0 (HSM_DM_CLK) 1'b1 - CPU_AND_PERIPHERALS_MCU_PLL0_HSDIV0_CLKOUT 1'b1 - MCU_PLL0_HSDIV0_CKLOUT (MCU_SYSCLK0) Reset Source: mod_g_rst_n

14.2.1.1.3.2.100 WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL Register

14.2.1.1.3.2.100.1 WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL Register (Offset = 8020h) [reset = 0h]

Enables and selects clock source of WKUP_CLKOUT pin

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Table 14-5682. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 8020h

Figure 14-2828. WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							CLKOUT_CTRL_OUT_MUX_SEL
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLKOUT_CTRL_WKUP_CLKOUT_SEL		
NONE					R/W		
0h					0h		

Table 14-5683. WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CLKOUT_CTRL_OUT_MUX_SEL	R/W	0h	WKUP CLKOUT (Pin) pin output mux selection. HFOSC0_CLK is a direct output from the HFOSC0 Field values (others are reserved): 1'b0 - CLK_DIV_OUT 1'b1 - HFOSC0_CLK (clk_sel must be DRIVE_LOW) Reset Source: mod_por_rst_n
23:3	RESERVED	NONE	0h	Reserved
2:0	CLKOUT_CTRL_WKUP_CLKOUT_SEL	R/W	0h	Controls WKUP CLKOUT MUX for WKUP_CLKOUT0 Pin Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT_SERDES 3'b000 - DRIVE_LOW 3'b001 - LFOSC0_CLKOUT 3'b010 - MAIN_PLL0_HSDIV2_CLKOUT 3'b011 - MAIN_PLL1_HSDIV2_CLKOUT 3'b100 - MAIN_PLL2_HSDIV9_CLKOUT 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CLK_12M_RC 3'b111 - HFOSC0_CLKOUT Reset Source: mod_por_rst_n

14.2.1.1.3.2.101 WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL Register

14.2.1.1.3.2.101.1 WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL Register (Offset = 8030h) [reset = 1h]

Selects the timebase clock source for the Global Timebase Counter

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Table 14-5684. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 8030h

Figure 14-2829. WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_GTC_CLKSEL_CLK_SEL		
NONE					R/W		
0h					1h		

Table 14-5685. WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_GTC_CLKSEL_CLK_SEL	R/W	1h	Selects the GTC timebase clock source Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV5_CLKOUT 3'b001 - MAIN_PLL0_HSDIV6_CLKOUT 3'b010 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 3'b011 - Reserved '0' 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - EXT_REFCLK1 (Pin) 3'b110 - MCU_SYSCLK0_DIV2 3'b110 - MCU_SYSCLK0/2 3'b111 - MAIN_SYSCLK0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.102 WKUP_CTRL_MMR_CFG0_USB0_CLKSEL Register

14.2.1.1.3.2.102.1 WKUP_CTRL_MMR_CFG0_USB0_CLKSEL Register (Offset = 8190h) [reset = 0h]

Selects the functional clock sources for USB0

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Table 14-5686. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 8190h

Figure 14-2830. WKUP_CTRL_MMR_CFG0_USB0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USB0_CLKSEL_REFCLK_SEL
NONE							R/W
0h							0h

Table 14-5687. WKUP_CTRL_MMR_CFG0_USB0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USB0_CLKSEL_REFCLK_SEL	R/W	0h	Selects the clock source for the USB0 ref_clk. Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - MAIN_PLL0_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.3.2.103 WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL Register

14.2.1.1.3.2.103.1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL Register (Offset = 81B0h) [reset = 0h]

Timer0 functional clock selection control

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Table 14-5688. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 81B0h

Figure 14-2831. WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_TIMER0_CLKSEL_CLK_SEL		
NONE					R/W		
0h					0h		

Table 14-5689. WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_TIMER0_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - DM_CLK/2 3'b001 - DM_CLK/4 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW0_CPTS_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.3.2.104 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL Register

14.2.1.1.3.2.104.1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL Register (Offset = 81B4h) [reset = 0h]

Timer1 functional clock selection control

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Table 14-5690. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 81B4h

Figure 14-2832. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">WKUP_TIMER1_CLKSEL_CLK_SEL</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-5691. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_TIMER1_CLKSEL_CLK_SEL	R/W	0h	Timer functional clock input select mux control Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - DM_CLK/2 3'b001 - DM_CLK/4 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW0_CPTS_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.3.2.105 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL Register

14.2.1.1.3.2.105.1 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL Register (Offset = 8340h) [reset = 0h]

RM WWDT Clock Manager Control Register

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Table 14-5692. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 8340h

Figure 14-2833. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">WKUP_WWD0_CTRL_WWD_STOP</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-5693. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	WKUP_WWD0_CTRL_WWD_STOP	R/W	0h	Controls Clocks to the WWD Watchdog Counter Field values (others are reserved): 4'b0000 - WWD Counter Running 4'b1010 - WWD Counter Stopped Reset Source: mod_g_rst_n

14.2.1.1.3.2.106 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL Register

14.2.1.1.3.2.106.1 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL Register (Offset = 8380h) [reset = 0h]

RM WWDT Clock Manager Clock Selection Register

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Table 14-5694. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 8380h

Figure 14-2834. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL Name Register

31	30	29	28	27	26	25	24
WKUP_WWD0_CLKSEL_WRTLOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						WKUP_WWD0_CLKSEL_CLK_SEL	
NONE						R/W	
0h						0h	

Table 14-5695. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_WWD0_CLKSEL_WRTLOCK	R/W	0h	When set, locks WKUP_WWD0_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WKUP_WWD0_CLKSEL_CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.3.2.107 WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL Register

14.2.1.1.3.2.107.1 WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL Register (Offset = 8600h) [reset = 0h]

Controls the functional source clock for RTC

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Table 14-5696. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 8600h

Figure 14-2835. WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_RTC_CLKSEL_CLK_SEL
NONE							R/W
0h							0h

Table 14-5697. WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_RTC_CLKSEL_CLK_SEL	R/W	0h	Selects the source of the RTC functional clock Field values (others are reserved): 1'b0 - DEVICE_CLKOUT_32K 1'b1 - CLK_32K_RC Reset Source: mod_por_rst_n

14.2.1.1.3.2.108 WKUP_CTRL_MMR_CFG0_LOCK2_KICK0 Register

14.2.1.1.3.2.108.1 WKUP_CTRL_MMR_CFG0_LOCK2_KICK0 Register (Offset = 9008h) [reset = 0h]

- KICK0 component

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Table 14-5698. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 9008h

Figure 14-2836. WKUP_CTRL_MMR_CFG0_LOCK2_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0							
R/W							
0h							

Table 14-5699. WKUP_CTRL_MMR_CFG0_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.109 WKUP_CTRL_MMR_CFG0_LOCK2_KICK1 Register

14.2.1.1.3.2.109.1 WKUP_CTRL_MMR_CFG0_LOCK2_KICK1 Register (Offset = 900Ch) [reset = 0h]

- KICK1 component

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Table 14-5700. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 900Ch

Figure 14-2837. WKUP_CTRL_MMR_CFG0_LOCK2_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK1							
R/W							
0h							

Table 14-5701. WKUP_CTRL_MMR_CFG0_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.110 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register

14.2.1.1.3.2.110.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register (Offset = 9100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5702. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 9100h

Figure 14-2838. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R0_READONLY							
R							
0h							

Table 14-5703. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.111 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register

14.2.1.1.3.2.111.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register (Offset = 910Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5704. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 910Ch

Figure 14-2839. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R3_READONLY							
R							
0h							

Table 14-5705. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.112 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register

14.2.1.1.3.2.112.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register (Offset = 9118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5706. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 9118h

Figure 14-2840. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6_READONLY							
R							
0h							

Table 14-5707. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.113 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register

14.2.1.1.3.2.113.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register (Offset = 911Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5708. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 911Ch

Figure 14-2841. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7_READONLY							
R							
0h							

Table 14-5709. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.114 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY Register

14.2.1.1.3.2.114.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY Register (Offset = 9130h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5710. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 9130h

Figure 14-2842. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R12_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R12_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R12_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R12_READONLY							
R							
0h							

Table 14-5711. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R12_READONLY	R	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.115 WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY Register

14.2.1.1.3.2.115.1 WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY Register (Offset = A010h) [reset = 0h]

Selects the functional clock source for the WKUP Domain

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Table 14-5712. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A010h

Figure 14-2843. WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5713. WKUP_CTRL_MMR_CFG0_WKUP_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects Clock Source for Wakeup Domain (Device Manager and Peripherals) Field values (others are reserved): 1'b0 - CPU_MAIN_PLL15_HSDIV2_CLKOUT__PERIPHERALS_MAIN_PLL15_HSDIV0_CLKOUT 1'b0 - MAIN_PLL15_HSDIV0_CLKOUT0 (HSM_DM_CLK) 1'b1 - CPU_AND_PERIPHERALS_MCU_PLL0_HSDIV0_CLKOUT 1'b1 - MCU_PLL0_HSDIV0_CKLOUT (MCU_SYSCLK0) Reset Source: mod_g_rst_n

14.2.1.1.3.2.116 WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register

14.2.1.1.3.2.116.1 WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register (Offset = A020h) [reset = 0h]

Enables and selects clock source of WKUP_CLKOUT pin

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Table 14-5714. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A020h

Figure 14-2844. WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							CLKOUT_CTRL_OUT_MUX_SEL_PROXY
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CLKOUT_CTRL_WKUP_CLKOUT_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-5715. WKUP_CTRL_MMR_CFG0_CLKOUT_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CLKOUT_CTRL_OUT_MUX_SEL_PROXY	R/W	0h	WKUP CLKOUT (Pin) pin output mux selection. HFOSC0_CLK is a direct output from the HFOSC0 Field values (others are reserved): 1'b0 - CLK_DIV_OUT 1'b1 - HFOSC0_CLK (clk_sel must be DRIVE_LOW) Reset Source: mod_por_rst_n
23:3	RESERVED	NONE	0h	Reserved
2:0	CLKOUT_CTRL_WKUP_CLKOUT_SEL_PROXY	R/W	0h	Controls WKUP CLKOUT MUX for WKUP_CLKOUT0 Pin Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT_SERDES 3'b000 - DRIVE_LOW 3'b001 - LFOSC0_CLKOUT 3'b010 - MAIN_PLL0_HSDIV2_CLKOUT 3'b011 - MAIN_PLL1_HSDIV2_CLKOUT 3'b100 - MAIN_PLL2_HSDIV9_CLKOUT 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CLK_12M_RC 3'b111 - HFOSC0_CLKOUT Reset Source: mod_por_rst_n

14.2.1.1.3.2.117 WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY Register

14.2.1.1.3.2.117.1 WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY Register (Offset = A030h) [reset = 1h]

Selects the timebase clock source for the Global Timebase Counter

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Table 14-5716. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A030h

Figure 14-2845. WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_GTC_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					1h		

Table 14-5717. WKUP_CTRL_MMR_CFG0_WKUP_GTC_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_GTC_CLKSEL_CLK_SEL_PROXY	R/W	1h	Selects the GTC timebase clock source Field values (others are reserved): 3'b000 - MAIN_PLL2_HSDIV5_CLKOUT 3'b001 - MAIN_PLL0_HSDIV6_CLKOUT 3'b010 - CP_GEMAC_CPTS0_RFT_CLK (Pin) 3'b011 - Reserved '0' 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - EXT_REFCLK1 (Pin) 3'b110 - MCU_SYSCLK0_DIV2 3'b110 - MCU_SYSCLK0/2 3'b111 - MAIN_SYSCLK0 Reset Source: mod_g_rst_n

14.2.1.1.3.2.118 WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register

14.2.1.1.3.2.118.1 WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register (Offset = A190h) [reset = 0h]

Selects the functional clock sources for USB0

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Table 14-5718. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A190h

Figure 14-2846. WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							USB0_CLKSEL_REFCLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5719. WKUP_CTRL_MMR_CFG0_USB0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	USB0_CLKSEL_REFCLK_SEL_PROXY	R/W	0h	Selects the clock source for the USB0 ref_clk. Field values (others are reserved): 1'b0 - HFOSC0_CLKOUT 1'b1 - MAIN_PLL0_HSDIV8_CLKOUT Reset Source: mod_g_rst_n

14.2.1.1.3.2.119 WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY Register

14.2.1.1.3.2.119.1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY Register (Offset = A1B0h) [reset = 0h]

Timer0 functional clock selection control

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Table 14-5720. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A1B0h

Figure 14-2847. WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_TIMER0_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-5721. WKUP_CTRL_MMR_CFG0_WKUP_TIMER0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_TIMER0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - DM_CLK/2 3'b001 - DM_CLK/4 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW0_CPTS_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.3.2.120 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY Register

14.2.1.1.3.2.120.1 WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY Register (Offset = A1B4h) [reset = 0h]

Timer1 functional clock selection control

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Table 14-5722. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A1B4h

Figure 14-2848. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WKUP_TIMER1_CLKSEL_CLK_SEL_PROXY		
NONE					R/W		
0h					0h		

Table 14-5723. WKUP_CTRL_MMR_CFG0_WKUP_TIMER1_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WKUP_TIMER1_CLKSEL_CLK_SEL_PROXY	R/W	0h	Timer functional clock input select mux control Field values (others are reserved): 3'b000 - HFOSC0_CLKOUT 3'b001 - DM_CLK/2 3'b001 - DM_CLK/4 3'b010 - CLK_12M_RC 3'b011 - MCU_PLL0_HSDIV5_CLKOUT 3'b100 - MCU_EXT_REFCLK0 (Pin) 3'b101 - DEVICE_CLKOUT_32K 3'b110 - CPSW0_CPTS_GENF0 3'b111 - CLK_32K_RC Reset Source: sys_por_rst_n

14.2.1.1.3.2.121 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY Register

14.2.1.1.3.2.121.1 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY Register (Offset = A340h) [reset = 0h]

RM WWDT Clock Manager Control Register

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Table 14-5724. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A340h

Figure 14-2849. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				WKUP_WWD0_CTRL_WWD_STOP_PROXY			
NONE				R/W			
0h				0h			

Table 14-5725. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	WKUP_WWD0_CTRL_WWD_STOP_PROXY	R/W	0h	Controls Clocks to the WWD Watchdog Counter Field values (others are reserved): 4'b0000 - WWD Counter Running 4'b1010 - WWD Counter Stopped Reset Source: mod_g_rst_n

14.2.1.1.3.2.122 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY Register

14.2.1.1.3.2.122.1 WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY Register (Offset = A380h) [reset = 0h]

RM WWDT Clock Manager Clock Selection Register

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Table 14-5726. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A380h

Figure 14-2850. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>WKUP_WWD0_CLKSEL_WRTLOCK_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">WKUP_WWD0_CLKSEL_CLK_SEL_PROXY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-5727. WKUP_CTRL_MMR_CFG0_WKUP_WWD0_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WKUP_WWD0_CLKSEL_WRTLOCK_PROXY	R/W	0h	When set, locks WKUP_WWD0_CLKSEL from further writes until the next module reset. Field values (others are reserved): 1'b0 - UNLOCKED 1'b1 - LOCKED Reset Source: mod_g_rst_n
30:2	RESERVED	NONE	0h	Reserved
1:0	WKUP_WWD0_CLKSEL_CLK_SEL_PROXY	R/W	0h	Windowed watchdog timer functional clock input select mux control Field values (others are reserved): 2'b00 - HFOSC0_CLKOUT 2'b01 - DEVICE_CLKOUT_32K 2'b10 - CLK_12M_RC 2'b11 - CLK_32K Reset Source: mod_g_rst_n

14.2.1.1.3.2.123 WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY Register

14.2.1.1.3.2.123.1 WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY Register (Offset = A600h) [reset = 0h]

Controls the functional source clock for RTC

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Table 14-5728. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 A600h

Figure 14-2851. WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WKUP_RTC_CLKSEL_CLK_SEL_PROXY
NONE							R/W
0h							0h

Table 14-5729. WKUP_CTRL_MMR_CFG0_WKUP_RTC_CLKSEL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	WKUP_RTC_CLKSEL_CLK_SEL_PROXY	R/W	0h	Selects the source of the RTC functional clock Field values (others are reserved): 1'b0 - DEVICE_CLKOUT_32K 1'b1 - CLK_32K_RC Reset Source: mod_por_rst_n

14.2.1.1.3.2.124 WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register

14.2.1.1.3.2.124.1 WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register (Offset = B008h) [reset = 0h]

- KICK0 component

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Table 14-5730. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B008h

Figure 14-2852. WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK2_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK2_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK2_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK2_KICK0_PROXY							
R/W							
0h							

Table 14-5731. WKUP_CTRL_MMR_CFG0_LOCK2_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.125 WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register

14.2.1.1.3.2.125.1 WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register (Offset = B00Ch) [reset = 0h]

- KICK1 component

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Table 14-5732. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B00Ch

Figure 14-2853. WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK2_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK2_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK2_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK2_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5733. WKUP_CTRL_MMR_CFG0_LOCK2_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK2_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.126 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register

14.2.1.1.3.2.126.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register (Offset = B100h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5734. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B100h

Figure 14-2854. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P2_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5735. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R0	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.127 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register

14.2.1.1.3.2.127.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register (Offset = B104h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5736. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B104h

Figure 14-2855. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R1							
R/W							
0h							

Table 14-5737. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R1	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.128 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register

14.2.1.1.3.2.128.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register (Offset = B108h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5738. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B108h

Figure 14-2856. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R2							
R/W							
0h							

Table 14-5739. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R2	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.129 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register

14.2.1.1.3.2.129.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register (Offset = B10Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5740. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B10Ch

Figure 14-2857. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R3							
R/W							
0h							

Table 14-5741. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R3	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.130 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register

14.2.1.1.3.2.130.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register (Offset = B110h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5742. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B110h

Figure 14-2858. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R4							
R/W							
0h							

Table 14-5743. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R4	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.131 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register

14.2.1.1.3.2.131.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register (Offset = B114h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5744. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B114h

Figure 14-2859. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R5							
R/W							
0h							

Table 14-5745. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R5	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.132 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register

14.2.1.1.3.2.132.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register (Offset = B118h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5746. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B118h

Figure 14-2860. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R6							
R/W							
0h							

Table 14-5747. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R6	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.133 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register

14.2.1.1.3.2.133.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register (Offset = B11Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5748. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B11Ch

Figure 14-2861. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R7							
R/W							
0h							

Table 14-5749. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R7	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.134 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register

14.2.1.1.3.2.134.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register (Offset = B120h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5750. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B120h

Figure 14-2862. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R8							
R/W							
0h							

Table 14-5751. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R8	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.135 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register

14.2.1.1.3.2.135.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register (Offset = B124h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5752. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B124h

Figure 14-2863. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R9							
R/W							
0h							

Table 14-5753. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R9	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.136 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register

14.2.1.1.3.2.136.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register (Offset = B128h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5754. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B128h

Figure 14-2864. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R10							
R/W							
0h							

Table 14-5755. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R10	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.137 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register

14.2.1.1.3.2.137.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register (Offset = B12Ch) [reset = 0h]

Claim bits for Partition 2

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Table 14-5756. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B12Ch

Figure 14-2865. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R11							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R11							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R11							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R11							
R/W							
0h							

Table 14-5757. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R11	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.138 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12 Register

14.2.1.1.3.2.138.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12 Register (Offset = B130h) [reset = 0h]

Claim bits for Partition 2

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Table 14-5758. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 B130h

Figure 14-2866. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P2_R12							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P2_R12							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P2_R12							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P2_R12							
R/W							
0h							

Table 14-5759. WKUP_CTRL_MMR_CFG0_CLAIMREG_P2_R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P2_R12	R/W	0h	Claim bits for Partition 2 Reset Source: mod_g_rst_n

14.2.1.1.3.2.139 WKUP_CTRL_MMR_CFG0_POST_STAT Register

14.2.1.1.3.2.139.1 WKUP_CTRL_MMR_CFG0_POST_STAT Register (Offset = C2C0h) [reset = 0h]

Contains the result of power-on self tests.

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Table 14-5760. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 C2C0h

Figure 14-2867. WKUP_CTRL_MMR_CFG0_POST_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						POST_STAT_FPOST_PLL_LOCK_TIMEOUT	POST_STAT_FPOST_PLL_LOCKLOSS
NONE						R	R
0h						X	X
15	14	13	12	11	10	9	8
POST_STAT_POST_PBIST_FAIL	RESERVED					POST_STAT_POST_PBIST_TIMEOUT	POST_STAT_POST_PBIST_DONE
R	NONE					R	R
X	0h					X	X
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5761. WKUP_CTRL_MMR_CFG0_POST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	POST_STAT_FPOST_PLL_LOCK_TIMEOUT	R	X	Differentiates between Fast POST and Slow POST. Fast POST is initiated after the PLL locks using the settings in the POST_CFG MMR. Otherwise, if the PLL lock times out, Slow POST is initated at the PLL reference clock rate. Field values (others are reserved): 1'b0 - FAST_POST 1'b1 - SLOW_POST Reset Source: mod_por_rst_n
16	POST_STAT_FPOST_PLL_LOCKLOSS	R	X	Indicates that POST exited with a PLL Lockloss Error Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - EXITED_ON_LOCK_LOSS Reset Source: mod_por_rst_n
15	POST_STAT_POST_PBIST_FAIL	R	X	POST PBIST failed Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - FAIL Reset Source: mod_por_rst_n
14:10	RESERVED	NONE	0h	Reserved

Table 14-5761. WKUP_CTRL_MMR_CFG0_POST_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	POST_STAT_POST_PBIST_TIMEOUT	R	X	POST PBIST timed out Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - TIMEOUT Reset Source: mod_por_rst_n
8	POST_STAT_POST_PBIST_DONE	R	X	POST PBIST done Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DONE Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.140 WKUP_CTRL_MMR_CFG0_PBIST_EN Register

14.2.1.1.3.2.140.1 WKUP_CTRL_MMR_CFG0_PBIST_EN Register (Offset = C400h) [reset = 0h]

Enables PBIST Config Modes access to memories

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Table 14-5762. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 C400h

Figure 14-2868. WKUP_CTRL_MMR_CFG0_PBIST_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		PBIST_EN_MAIN_R5SS1	PBIST_EN_MAIN_R5SS0	RESERVED		PBIST_EN_AASRC1	PBIST_EN_AASRC0
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	0h	0h		0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PBIST_EN_USB0	RESERVED			PBIST_EN_EMMC0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-5763. WKUP_CTRL_MMR_CFG0_PBIST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21	PBIST_EN_MAIN_R5SS1	R/W	0h	Enables PBIST Access to Main R5SS1 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n
20	PBIST_EN_MAIN_R5SS0	R/W	0h	Enables PBIST Access to Main R5SS0 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n
19:18	RESERVED	NONE	0h	Reserved
17	PBIST_EN_AASRC1	R/W	0h	Enables PBIST Access to AASRC1 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n
16	PBIST_EN_AASRC0	R/W	0h	Enables PBIST Access to AASRC0 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n

Table 14-5763. WKUP_CTRL_MMR_CFG0_PBIST_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:5	RESERVED	NONE	0h	Reserved
4	PBIST_EN_USB0	R/W	0h	Enables PBIST Access to USB0 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	PBIST_EN_EMMC0	R/W	0h	Enables PBIST Access to MMC0 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n

14.2.1.1.3.2.141 WKUP_CTRL_MMR_CFG0_LOCK3_KICK0 Register

14.2.1.1.3.2.141.1 WKUP_CTRL_MMR_CFG0_LOCK3_KICK0 Register (Offset = D008h) [reset = 0h]

- KICK0 component

Return to Summary Table

Table 14-5764. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D008h

Figure 14-2869. WKUP_CTRL_MMR_CFG0_LOCK3_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0							
R/W							
0h							

Table 14-5765. WKUP_CTRL_MMR_CFG0_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.142 WKUP_CTRL_MMR_CFG0_LOCK3_KICK1 Register

14.2.1.1.3.2.142.1 WKUP_CTRL_MMR_CFG0_LOCK3_KICK1 Register (Offset = D00Ch) [reset = 0h]

- KICK1 component

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Table 14-5766. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D00Ch

Figure 14-2870. WKUP_CTRL_MMR_CFG0_LOCK3_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK1							
R/W							
0h							

Table 14-5767. WKUP_CTRL_MMR_CFG0_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.143 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register

14.2.1.1.3.2.143.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register (Offset = D100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5768. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D100h

Figure 14-2871. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0_READONLY							
R							
0h							

Table 14-5769. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.144 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register

14.2.1.1.3.2.144.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register (Offset = D104h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5770. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D104h

Figure 14-2872. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R1_READONLY							
R							
0h							

Table 14-5771. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R1_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.145 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register

14.2.1.1.3.2.145.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register (Offset = D108h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5772. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D108h

Figure 14-2873. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R2_READONLY							
R							
0h							

Table 14-5773. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R2_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.146 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register

14.2.1.1.3.2.146.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register (Offset = D10Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5774. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D10Ch

Figure 14-2874. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R3_READONLY							
R							
0h							

Table 14-5775. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R3_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.147 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register

14.2.1.1.3.2.147.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register (Offset = D110h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5776. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D110h

Figure 14-2875. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R4_READONLY							
R							
0h							

Table 14-5777. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R4_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.148 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register

14.2.1.1.3.2.148.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register (Offset = D114h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5778. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D114h

Figure 14-2876. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R5_READONLY							
R							
0h							

Table 14-5779. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R5_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.149 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register

14.2.1.1.3.2.149.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register (Offset = D118h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5780. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D118h

Figure 14-2877. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R6_READONLY							
R							
0h							

Table 14-5781. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R6_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.150 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register

14.2.1.1.3.2.150.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register (Offset = D11Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5782. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D11Ch

Figure 14-2878. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R7_READONLY							
R							
0h							

Table 14-5783. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R7_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.151 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register

14.2.1.1.3.2.151.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register (Offset = D120h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5784. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 D120h

Figure 14-2879. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R8_READONLY							
R							
0h							

Table 14-5785. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R8_READONLY	R	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.152 WKUP_CTRL_MMR_CFG0_POST_STAT_PROXY Register

14.2.1.1.3.2.152.1 WKUP_CTRL_MMR_CFG0_POST_STAT_PROXY Register (Offset = E2C0h) [reset = 0h]

Contains the result of power-on self tests.

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Table 14-5786. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 E2C0h

Figure 14-2880. WKUP_CTRL_MMR_CFG0_POST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						POST_STAT_FPOST_PLL_LOCK_TIMEOUT_PROXY	POST_STAT_FPOST_PLL_LOCKLOSS_PROXY
NONE						R	R
0h						X	X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POST_STAT_POST_PBIST_FAIL_PROXY	RESERVED					POST_STAT_POST_PBIST_TIMEOUT_PROXY	POST_STAT_POST_PBIST_DONE_PROXY
R	NONE					R	R
X	0h					X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-5787. WKUP_CTRL_MMR_CFG0_POST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	POST_STAT_FPOST_PLL_LOCK_TIMEOUT_PROXY	R	X	Differentiates between Fast POST and Slow POST. Fast POST is initiated after the PLL locks using the settings in the POST_CFG MMR. Otherwise, if the PLL lock times out, Slow POST is initated at the PLL reference clock rate. Field values (others are reserved): 1'b0 - FAST_POST 1'b1 - SLOW_POST Reset Source: mod_por_rst_n
16	POST_STAT_FPOST_PLL_LOCKLOSS_PROXY	R	X	Indicates that POST exited with a PLL Lockloss Error Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - EXITED_ON_LOCK_LOSS Reset Source: mod_por_rst_n
15	POST_STAT_POST_PBIST_FAIL_PROXY	R	X	POST PBIST failed Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - FAIL Reset Source: mod_por_rst_n

Table 14-5787. WKUP_CTRL_MMR_CFG0_POST_STAT_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:10	RESERVED	NONE	0h	Reserved
9	POST_STAT_POST_PBIST_TIMEOUT_PROXY	R	X	POST PBIST timed out Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - TIMEOUT Reset Source: mod_por_rst_n
8	POST_STAT_POST_PBIST_DONE_PROXY	R	X	POST PBIST done Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DONE Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.153 WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Register

14.2.1.1.3.2.153.1 WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Register (Offset = E400h) [reset = 0h]

Enables PBIST Config Modes access to memories

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Table 14-5788. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 E400h

Figure 14-2881. WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td>PBIST_EN_MAIN_R5SS1_PROXY</td><td>PBIST_EN_MAIN_R5SS0_PROXY</td><td colspan="2">RESERVED</td><td>PBIST_EN_AASRC1_PROXY</td><td>PBIST_EN_AASRC0_PROXY</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="2">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>PBIST_EN_USB0_PROXY</td><td colspan="3">RESERVED</td><td>PBIST_EN_EMMC0_PROXY</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-5789. WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21	PBIST_EN_MAIN_R5SS1_PROXY	R/W	0h	Enables PBIST Access to Main R5SS1 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n
20	PBIST_EN_MAIN_R5SS0_PROXY	R/W	0h	Enables PBIST Access to Main R5SS0 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n
19:18	RESERVED	NONE	0h	Reserved
17	PBIST_EN_AASRC1_PROXY	R/W	0h	Enables PBIST Access to AASRC1 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n

Table 14-5789. WKUP_CTRL_MMR_CFG0_PBIST_EN_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PBIST_EN_AASRC0_PROXY	R/W	0h	Enables PBIST Access to AASRC0 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n
15:5	RESERVED	NONE	0h	Reserved
4	PBIST_EN_USB0_PROXY	R/W	0h	Enables PBIST Access to USB0 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	PBIST_EN_EMMC0_PROXY	R/W	0h	Enables PBIST Access to MMC0 Memories Field values (others are reserved): 1'b0 - DISABLE 1'b1 - ENABLE Reset Source: mod_g_rst_n

14.2.1.1.3.2.154 WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register

14.2.1.1.3.2.154.1 WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register (Offset = F008h) [reset = 0h]

- KICK0 component

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Table 14-5790. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F008h

Figure 14-2882. WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK3_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK3_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK3_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK3_KICK0_PROXY							
R/W							
0h							

Table 14-5791. WKUP_CTRL_MMR_CFG0_LOCK3_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.155 WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register

14.2.1.1.3.2.155.1 WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register (Offset = F00Ch) [reset = 0h]

- KICK1 component

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Table 14-5792. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F00Ch

Figure 14-2883. WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK3_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK3_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK3_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK3_KICK1_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5793. WKUP_CTRL_MMR_CFG0_LOCK3_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK3_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.156 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register

14.2.1.1.3.2.156.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register (Offset = F100h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5794. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F100h

Figure 14-2884. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R0							
R/W							
0h							

Table 14-5795. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R0	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.157 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register

14.2.1.1.3.2.157.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register (Offset = F104h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5796. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F104h

Figure 14-2885. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R1							
R/W							
0h							

Table 14-5797. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R1	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.158 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register

14.2.1.1.3.2.158.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register (Offset = F108h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5798. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F108h

Figure 14-2886. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R2							
R/W							
0h							

Table 14-5799. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R2	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.159 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register

14.2.1.1.3.2.159.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register (Offset = F10Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5800. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F10Ch

Figure 14-2887. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R3							
R/W							
0h							

Table 14-5801. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R3	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.160 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register

14.2.1.1.3.2.160.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register (Offset = F110h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5802. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F110h

Figure 14-2888. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R4							
R/W							
0h							

Table 14-5803. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R4	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.161 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register

14.2.1.1.3.2.161.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register (Offset = F114h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5804. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F114h

Figure 14-2889. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R5							
R/W							
0h							

Table 14-5805. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R5	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.162 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register

14.2.1.1.3.2.162.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register (Offset = F118h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5806. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F118h

Figure 14-2890. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R6							
R/W							
0h							

Table 14-5807. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R6	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.163 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register

14.2.1.1.3.2.163.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register (Offset = F11Ch) [reset = 0h]

Claim bits for Partition 3

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Table 14-5808. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F11Ch

Figure 14-2891. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R7							
R/W							
0h							

Table 14-5809. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R7	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.164 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register

14.2.1.1.3.2.164.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register (Offset = F120h) [reset = 0h]

Claim bits for Partition 3

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Table 14-5810. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4300 F120h

Figure 14-2892. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P3_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P3_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P3_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P3_R8							
R/W							
0h							

Table 14-5811. WKUP_CTRL_MMR_CFG0_CLAIMREG_P3_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P3_R8	R/W	0h	Claim bits for Partition 3 Reset Source: mod_g_rst_n

14.2.1.1.3.2.165 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register

14.2.1.1.3.2.165.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register (Offset = 11100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5812. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 1100h

Figure 14-2893. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0_READONLY							
R							
0h							

Table 14-5813. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.166 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register

14.2.1.1.3.2.166.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register (Offset = 11120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5814. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 1120h

Figure 14-2894. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8_READONLY							
R							
0h							

Table 14-5815. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8_READONLY	R	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.167 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register

14.2.1.1.3.2.167.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register (Offset = 13100h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5816. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 3100h

Figure 14-2895. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R0							
R/W							
0h							

Table 14-5817. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R0	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.168 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register

14.2.1.1.3.2.168.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register (Offset = 13104h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5818. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 3104h

Figure 14-2896. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R1							
R/W							
0h							

Table 14-5819. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R1	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.169 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register

14.2.1.1.3.2.169.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register (Offset = 13108h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5820. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 3108h

Figure 14-2897. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R2							
R/W							
0h							

Table 14-5821. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R2	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.170 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register

14.2.1.1.3.2.170.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register (Offset = 1310Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5822. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 310Ch

Figure 14-2898. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R3							
R/W							
0h							

Table 14-5823. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R3	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.171 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register

14.2.1.1.3.2.171.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register (Offset = 13110h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5824. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 3110h

Figure 14-2899. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R4							
R/W							
0h							

Table 14-5825. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R4	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.172 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register

14.2.1.1.3.2.172.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register (Offset = 13114h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5826. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 3114h

Figure 14-2900. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R5							
R/W							
0h							

Table 14-5827. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R5	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.173 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register

14.2.1.1.3.2.173.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register (Offset = 13118h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5828. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 3118h

Figure 14-2901. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R6							
R/W							
0h							

Table 14-5829. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R6	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.174 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register

14.2.1.1.3.2.174.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register (Offset = 1311Ch) [reset = 0h]

Claim bits for Partition 4

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Table 14-5830. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 311Ch

Figure 14-2902. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R7							
R/W							
0h							

Table 14-5831. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R7	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.175 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register

14.2.1.1.3.2.175.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register (Offset = 13120h) [reset = 0h]

Claim bits for Partition 4

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Table 14-5832. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 3120h

Figure 14-2903. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P4_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P4_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P4_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P4_R8							
R/W							
0h							

Table 14-5833. WKUP_CTRL_MMR_CFG0_CLAIMREG_P4_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P4_R8	R/W	0h	Claim bits for Partition 4 Reset Source: mod_g_rst_n

14.2.1.1.3.2.176 WKUP_CTRL_MMR_CFG0_PMCTRL_SYS Register

14.2.1.1.3.2.176.1 WKUP_CTRL_MMR_CFG0_PMCTRL_SYS Register (Offset = 18080h) [reset = 10h]

Controls operation of the PMIC_LPM_EN pin

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Table 14-5834. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8080h

Figure 14-2904. WKUP_CTRL_MMR_CFG0_PMCTRL_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PMCTRL_SYS_PMIC_EN_WE	PMCTRL_SYS_PMIC_EN	PMCTRL_SYS_LPM_EN_WE	PMCTRL_SYS_LPM_EN		
NONE		R/W	R/W	R/W	R/W		
0h		0h	1h	0h	0h		

Table 14-5835. WKUP_CTRL_MMR_CFG0_PMCTRL_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	PMCTRL_SYS_PMIC_EN_WE	R/W	0h	Unused Field - Value is Don't Care Reset Source: mod_g_rst_n
4	PMCTRL_SYS_PMIC_EN	R/W	1h	Controls state of PMIC_LPM_EN_OUT when LPM_EN[2:0] is 000 Reset Source: mod_g_rst_n
3	PMCTRL_SYS_LPM_EN_WE	R/W	0h	Unused Field - Value is Don't Care Reset Source: mod_g_rst_n
2:0	PMCTRL_SYS_LPM_EN	R/W	0h	Controls whether PMIC_LPM_EN_OUT is driven by the pmic_en bit. Field values (others are reserved): 3'b000 - PMIC_LPM_EN_OUT controlled by pmic_en bit. Reset Source: mod_g_rst_n

14.2.1.1.3.2.177 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Register

14.2.1.1.3.2.177.1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Register (Offset = 18084h) [reset = 0h]

This register is writable only when LOCK6-KICK0:1 are unlocked

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Table 14-5836. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8084h

Figure 14-2905. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Name Register

31	30	29	28	27	26	25	24
RESERVED						PMCTRL_IO_0_IO_ISO_STATUS_0	PMCTRL_IO_0_IO_ISO_CTRL_0
NONE						R	R/W
0h						X	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PMCTRL_IO_0_GLOBAL_WUEN_0
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PMCTRL_IO_0_WUCLK_STATUS_0	PMCTRL_IO_0_WUCLK_CTRL_0
NONE						R	R/W
0h						X	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PMCTRL_IO_0_ISOBYPASS_OVR_0	PMCTRL_IO_0_IO_ON_STATUS_0	PMCTRL_IO_0_ISOOVR_EXTEND_0	RESERVED		PMCTRL_IO_0_ISOCLK_STATUS_0	PMCTRL_IO_0_ISOCLK_OVRD_0
NONE	R/W	R	R/W	NONE		R	R/W
0h	0h	X	0h	0h		X	0h

Table 14-5837. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	PMCTRL_IO_0_IO_ISO_STATUS_0	R	X	IO ISO Status. Read 0: IO isolation not active. Read 1: IO isolation active. Reflects value of SMS input port io_isoack coming back from IO pad ring. Reset Source: mod_g_rst_n
24	PMCTRL_IO_0_IO_ISO_CTRL_0	R/W	0h	IO ISO control. Writing this bit to 1 will kick off IO isolation. Reset Source: mod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PMCTRL_IO_0_GLOBAL_WUEN_0	R/W	0h	Global IO wakeup enable. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Io Logiclogic. 0:All individual IO WUEN are gated in the IO logic (override to 0). 1: All individual IO WUEN from control module are going to IOs. Map to SMS input port io_globalwkupen Reset Source: mod_g_rst_n

Table 14-5837. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:10	RESERVED	NONE	0h	Reserved
9	PMCTRL_IO_0_WUCLK_STATUS_0	R	X	Reflects value of DM input port io_wuclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
8	PMCTRL_IO_0_WUCLK_CTRL_0	R/W	0h	Direct control on WUCLKIN signal to IO pad ring.0:WUCLKIN signal is driven to 0.IO wakeup daisy chain is functional as well as IO whose wakeup feature is enabled. 1:WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs. Reset Source: mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	PMCTRL_IO_0_ISOBYPASS_OVR_0	R/W	0h	This MMR bit drives directly DM output port io_isobypassundefined. Reset Source: mod_g_rst_n
5	PMCTRL_IO_0_IO_ON_STATUS_0	R	X	Gives the functional status of the IO ring. Read 0: Part or all of the IOs are not in the ON state that is are in isolation state. Read 1: All IOs are in the ON state. io_on_status = assign 1 if (io_iso == 0 & io_isoack==0 & io_iso_clk == 0 & io_isoclk_ack = 0) else 0; Reset Source: mod_g_rst_n
4	PMCTRL_IO_0_ISOOVR_EXTEND_0	R/W	0h	This drives the SOC chain ISO-OVERRIDE global control. This bit drives directly the DM output port io_isoovrundefined. At the SOC level it is used to enable when 1 or gate-off when 0, the individual ISOOR for each IO. This operates as a global enable/disable for the individual IOs.Control for IO isolation extension. '0' IO isolation is not extended. Transition happens as soon as automatic restore is completed. '1' IO isolation is extended. The IOs whose ISOOVR bits have been individually set in their PADCFG MMRs will all get its IO isolation extended beyond the point when the initial IO daisy chain isolation is released. Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PMCTRL_IO_0_ISOCLK_STATUS_0	R	X	Reflects value of DM input port io_isoclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
0	PMCTRL_IO_0_ISOCLK_OVRD_0	R/W	0h	Override control on ISOCLKIN signal to IO pad ring. When not overridden this signal is controlled by hardware only. 0 ISOCLKIN signal is not override. 1 ISOCLKIN signal is overridden to active value ('1'). Reset Source: mod_g_rst_n

14.2.1.1.3.2.178 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Register

14.2.1.1.3.2.178.1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Register (Offset = 18088h) [reset = 0h]

This register is writable only when LOCK6-KICK0:1 are unlocked

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Table 14-5838. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8088h

Figure 14-2906. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">PMCTRL_IO_1_RESERVED4</td><td>PMCTRL_IO_1_IO_ISO_STATUS_1</td><td>PMCTRL_IO_1_IO_ISO_CTRL_1</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="6">X</td><td>X</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>PMCTRL_IO_1_GLOBAL_WUEN_1</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>PMCTRL_IO_1_WUCLK_STATUS_1</td><td>PMCTRL_IO_1_WUCLK_CTRL_1</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>PMCTRL_IO_1_ISOBYPASS_OVR_1</td><td>PMCTRL_IO_1_IO_ON_STATUS_1</td><td>PMCTRL_IO_1_ISOOVR_EXTEND_1</td><td colspan="2">RESERVED</td><td>PMCTRL_IO_1_ISOCLK_STATUS_1</td><td>PMCTRL_IO_1_ISOCLK_OVRD_1</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R</td><td>R/W</td><td colspan="2">NONE</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>X</td><td>0h</td><td colspan="2">0h</td><td>X</td><td>0h</td></tr>
</table>

Table 14-5839. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	PMCTRL_IO_1_RESERVED4	R	X	reserved
25	PMCTRL_IO_1_IO_ISO_STATUS_1	R	X	IO ISO Status. Read 0: IO isolation not active. Read 1: IO isolation active. Reflects value of DM input port io_isoack coming back from IO pad ring. Reset Source: mod_g_rst_n
24	PMCTRL_IO_1_IO_ISO_CTRL_1	R/W	0h	IO ISO control. Writing this bit to 1 will kick off IO isolation. Reset Source: mod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved
16	PMCTRL_IO_1_GLOBAL_WUEN_1	R/W	0h	Global IO wakeup enable. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Spinner logic. 0:All individual IO WUEN are gated in the Spinner logic (override to 0). 1: All individual IO WUEN from control module are going to Ios. Map to DM input port io_globalwkupen Reset Source: mod_g_rst_n

Table 14-5839. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:10	RESERVED	NONE	0h	Reserved
9	PMCTRL_IO_1_WUCLK_STATUS_1	R	X	Reflects value of DM input port io_wuclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
8	PMCTRL_IO_1_WUCLK_CTRL_1	R/W	0h	Direct control on WUCLKIN signal to IO pad ring.0:WUCLKIN signal is driven to 0.IO wakeup daisy chain is functional as well as IO whose wakeup feature is enabled. 1:WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs. Reset Source: mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	PMCTRL_IO_1_ISOBYPASS_OVR_1	R/W	0h	This MMR bit drives directly DM output port io_isobypassundefined. Reset Source: mod_g_rst_n
5	PMCTRL_IO_1_IO_ON_STATUS_1	R	X	Gives the functional status of the IO ring. Read 0: Part or all of the Ios are not in the ON state that is are in isolation state. Read 1: All Ios are in the ON state. io_on_status = assign 1 if (io_iso == 0 & io_isoack==0 & io_iso_clk == 0 & io_isoclk_ack = 0) else 0; Reset Source: mod_g_rst_n
4	PMCTRL_IO_1_ISOOVR_EXTEND_1	R/W	0h	This drives the SOC chain ISO-OVERRIDE global control. This bit drives directly the DM output port io_isoovrundefined. At the SOC level it is used to enable when 1 or gate-off when 0, the individual ISOOR for each IO. This operates as a global enable/disable for the individual IOs.Control for IO isolation extension. '0' IO isolation is not extended. Transition happens as soon as automatic restore is completed. '1' IO isolation is extended. The IOs whose ISOOVR bits have been individually set in their PADCFG MMRs will all get its IO isolation extended beyond the point when the initial IO daisy chain isolation is released. Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PMCTRL_IO_1_ISOCLK_STATUS_1	R	X	Reflects value of DM input port io_isoclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
0	PMCTRL_IO_1_ISOCLK_OVRD_1	R/W	0h	Override control on ISOCLKIN signal to IO pad ring. When not overridden this signal is controlled by hardware only. 0 ISOCLKIN signal is not override. 1 ISOCLKIN signal is overridden to active value ('1'). Reset Source: mod_g_rst_n

14.2.1.1.3.2.179 WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC Register

14.2.1.1.3.2.179.1 WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC Register (Offset = 18090h) [reset = BC00h]

This register is writable only when LOCK6-KICK0:1 are unlocked

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Table 14-5840. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8090h

Figure 14-2907. WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC Name Register

31	30	29	28	27	26	25	24
PMCTRL_MOSC_OSC_CG_ON_WFI	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PMCTRL_MOSC_SETUP_TIME			
NONE				R/W			
0h				BC00h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMCTRL_MOSC_SETUP_TIME							
R/W							
BC00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMCTRL_MOSC_SETUP_TIME							
R/W							
BC00h							

Table 14-5841. WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PMCTRL_MOSC_OSC_CG_ON_WFI	R/W	0h	To clock gate the main HFOSC, DM sets this bit then enters the WFI state at which time the HFOSC will be gated. Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:0	PMCTRL_MOSC_SETUP_TIME	R/W	BC00h	Number of HFOSC clock cycles before HFOSC clock is ungated to the SOC (allows the HFOSC time to stabilize after starting up, before the SOC is clocked). Reset Source: mod_g_rst_n

14.2.1.1.3.2.180 WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS Register

14.2.1.1.3.2.180.1 WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS Register (Offset = 18098h) [reset = 0h]

Reflects the progress of the request to clock-gate HFOSC via MMR PMCTRL_MOSCundefined.

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Table 14-5842. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8098h

Figure 14-2908. WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PM_MISC_STATUS_OSC_CG_STAT	
NONE						R	
0h						X	

Table 14-5843. WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PM_MISC_STATUS_OSC_CG_STAT	R	X	HFOSC Clock Gating State Field values (others are reserved): 2'b00 - HFOSC_OFF 2'b01 - HFOSC_OFF2ON (transition state) 2'b10 - HFOSC_ON2OFF (transition state) 2'b11 - HFOSC_ON Reset Source: mod_g_rst_n

14.2.1.1.3.2.181 WKUP_CTRL_MMR_CFG0_RST_CTRL Register

14.2.1.1.3.2.181.1 WKUP_CTRL_MMR_CFG0_RST_CTRL Register (Offset = 18170h) [reset = 200FFh]

Controls Reset Assertion and Propogation

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Table 14-5844. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8170h

Figure 14-2909. WKUP_CTRL_MMR_CFG0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					RST_CTRL_MAIN_RESET_ISO_DONE_Z	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z	RST_CTRL_SMS_COLD_RESET_EN_Z
NONE					R/W	R/W	R/W
0h					0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Fh				Fh			

Table 14-5845. WKUP_CTRL_MMR_CFG0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MAIN_RESET_ISO_DONE_Z	R/W	0h	Blocks Main Domain Warm Reset. Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: main_chip1_rst_n
17	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z	R/W	1h	Block Reset of Main by ESM Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: main_chip1_rst_n
16	RST_CTRL_SMS_COLD_RESET_EN_Z	R/W	0h	Block Reset of Main by SMS Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: main_chip1_rst_n
15:8	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.182 WKUP_CTRL_MMR_CFG0_RST_STAT Register

14.2.1.1.3.2.182.1 WKUP_CTRL_MMR_CFG0_RST_STAT Register (Offset = 18174h) [reset = 0h]

Reset Status

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Table 14-5846. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8174h

Figure 14-2910. WKUP_CTRL_MMR_CFG0_RST_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MCU_RESET_ISO_DONE_Z
NONE							R
0h							X

Table 14-5847. WKUP_CTRL_MMR_CFG0_RST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MCU_RESET_ISO_DONE_Z	R	X	Indicates MCU Domain is in Reset Isolation When Active (Low) Field values (others are reserved): 1'b0 - ISOLATION 1'b1 - PASS_THROUGH Reset Source: main_chip1_rst_n

14.2.1.1.3.2.183 WKUP_CTRL_MMR_CFG0_RST_SRC Register

14.2.1.1.3.2.183.1 WKUP_CTRL_MMR_CFG0_RST_SRC Register (Offset = 18178h) [reset = 0h]

Captures Reason for Warm and Main Domain Power On Resets Read Only Mirror of MCU CTRL MMR version. Clearing these bits must be done through the MCU CTRL MMR.

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Table 14-5848. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8178h

Figure 14-2911. WKUP_CTRL_MMR_CFG0_RST_SRC Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR	RST_SRC_MAIN_ESM_ERROR	RESERVED					
R	R	NONE					
X	X	0h				X	X
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	RST_SRC_DM_WDT_RST			RESERVED			RST_SRC_SW_MCU_WARMRST
NONE	R			NONE			R
0h	X	X	X	0h			X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		RST_SRC_WARM_OUT_RST	RST_SRC_COLD_OUT_RST	RESERVED			RST_SRC_DEBUG_RST
NONE		R	R	NONE			R
0h		X	X	0h			X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RST_SRC_IPOR_WAKE	RESERVED	RST_SRC_THERMAL_RST	RESERVED		RESERVED	RST_SRC_MCU_RESET_PIN
NONE	R	NONE	R	NONE		NONE	R
0h	X	0h	X	0h	X	0h	X

Table 14-5849. WKUP_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR	R	X	Reset Caused by MCU ESM Error. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
30	RST_SRC_MAIN_ESM_ERROR	R	X	Reset Caused by Main ESM Error. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
29:26	RESERVED	NONE	0h	Reserved
23	RESERVED	NONE	0h	Reserved
22	RST_SRC_DM_WDT_RST	R	X	Watchdog Initiated Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n

Table 14-5849. WKUP_CTRL_MMR_CFG0_RST_SRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST	R	X	Software Warm Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST	R	X	SMS Warm Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
12	RST_SRC_COLD_OUT_RST	R	X	SMS Cold Reset. When set, indicates that a SMS Cold reset occurred and reset either MAIN or MCU domains (or both). Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST	R	X	Debug Subsystem Initiated Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
7	RESERVED	NONE	0h	Reserved
6	RST_SRC_IPOR_WAKE	R	X	Wake Event Monitor Internal Power On Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST	R	X	Thermal Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
3	RESERVED	NONE	0h	Reserved
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN	R	X	Rest Caused by MCU Reset Pin. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n

14.2.1.1.3.2.184 WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD Register

14.2.1.1.3.2.184.1 WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD Register (Offset = 1817Ch) [reset = 0h]

Read Only Mirror of MCU CTRL MMR version. After an MCU_PORz reset this bit field resets to 0x00000000. While this bit field remains 0x00000000 any warm reset from the Main Domain also propagates through the MCU domain. If the application does not require reset isolation of the MCU domain, it may leave this bit field with a value of 0x00000000. If the application does require reset isolation of the MCU domain after the initial boot, then the R5FSS CPU must write a nonzero value to the magic word. The actual value is left to software and different values may be used to convey information, but in order to isolate the MCU domain from all Main domain warm reset sources that trigger main_resetz, the value must be non-zero. If the value is nonzero and one of the Main domain warm reset sources triggers main_resetz occurs in the main domain, the R5FSS will not be reset. The Main domain bootloader must read this value to determine that the R5FSS is already initialized, and has configured reset isolation. The Main domain bootloader then also skips any initialization steps involving bootstrapping the R5FSS as it is is already running. Note that MCU_PORz reset is never blocked by a nonzero magic word.

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Table 14-5850. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 817Ch

Figure 14-2912. WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD							
R							
X							

Table 14-5851. WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD	R	X	Magic Word Indicating Status of MCU Subsystem Boot Reset Source: main_chip1_rst_n

14.2.1.1.3.2.185 WKUP_CTRL_MMR_CFG0_WKUP0_EN Register

14.2.1.1.3.2.185.1 WKUP_CTRL_MMR_CFG0_WKUP0_EN Register (Offset = 18180h) [reset = 0h]

Selects active wake-up sources

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Table 14-5852. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8180h

Figure 14-2913. WKUP_CTRL_MMR_CFG0_WKUP0_EN Name Register

31	30	29	28	27	26	25	24
WKUP0_EN_WKUPEN							
R/W							
0h							
23	22	21	20	19	18	17	16
WKUP0_EN_WKUPEN							
R/W							
0h							
15	14	13	12	11	10	9	8
WKUP0_EN_WKUPEN							
R/W							
0h							
7	6	5	4	3	2	1	0
WKUP0_EN_WKUPEN							
R/W							
0h							

Table 14-5853. WKUP_CTRL_MMR_CFG0_WKUP0_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WKUP0_EN_WKUPEN	R/W	0h	Enables Wakeup from on-chip sources. In addition to values listed, any OR combination of the values is also valid. Field values (others are reserved): 32'h00000001 - WKUP_I2C0 32'h00000002 - WKUP_USART0 32'h00000004 - MCU_GPIO0 32'h00000008 - DEBUG undefined - undefined 32'h00000020 - WKUP_TIMER0 32'h00000040 - WKUP_TIMER1 32'h00000080 - WKUP_RTC 32'h00000100 - MAIN_RESET_REQz 32'h00000200 - USB0_IN_BAND undefined - undefined 32'h00010000 - MAIN_IO_DAISY_CHAIN 32'h00020000 - MCU_IO_DAISY_CHAIN 32'h00040000 - CANUART_IO_DAISY_CHAIN Reset Source: mod_g_rst_n

14.2.1.1.3.2.186 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register

14.2.1.1.3.2.186.1 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register (Offset = 18280h) [reset = 100Eh]

Controls the power clock gating feature of modules and busses

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Table 14-5854. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8280h

Figure 14-2914. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Name Register

31	30	29	28	27	26	25	24
CLKGATE_CTRL0_MAIN_SMS_NOGATE	RESERVED	CLKGATE_CTRL0_MAIN_SA3SS_NOGATE	CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE	CLKGATE_CTRL0_MAIN_R5SS1_NOGATE	CLKGATE_CTRL0_MAIN_R5SS0_NOGATE	RESERVED	CLKGATE_CTRL0_MAIN_PDMA7_NOGATE
R/W	NONE	R/W	R/W	R/W	R/W	NONE	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLKGATE_CTRL0_MAIN_PDMA6_NOGATE	CLKGATE_CTRL0_MAIN_PDMA5_NOGATE	CLKGATE_CTRL0_MAIN_PDMA4_NOGATE	CLKGATE_CTRL0_MAIN_PDMA3_NOGATE	CLKGATE_CTRL0_MAIN_PDMA2_NOGATE	CLKGATE_CTRL0_MAIN_PDMA1_NOGATE	CLKGATE_CTRL0_MAIN_PDMA0_NOGATE	CLKGATE_CTRL0_MAIN_DMSS_NOGATE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	CLKGATE_CTRL0_MAIN_AUDIO_CBA_NOGATE	CLKGATE_CTRL0_MAIN_IPCSS_CBA_NOGATE	CLKGATE_CTRL0_MAIN_MEM_CBA_NOGATE	CLKGATE_CTRL0_MAIN_MISC_PERI_CBA_NOGATE	RESERVED		
NONE	R/W	R/W	R/W	R/W	NONE		
0h	0h	0h	1h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE	CLKGATE_CTRL0_MAIN_DATA_CBA_NOGATE	CLKGATE_CTRL0_MAIN_CENTRAL_CBA_NOGATE	CLKGATE_CTRL0_WKUP_DM_PWR_NOGATE	CLKGATE_CTRL0_WKUP_DM_CBA_NOGATE	CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	1h	1h	1h	0h

Table 14-5855. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLKGATE_CTRL0_MAIN_SMS_NOGATE	R/W	0h	MAIN domain SMS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
30	RESERVED	NONE	0h	Reserved
29	CLKGATE_CTRL0_MAIN_SA3SS_NOGATE	R/W	0h	MAIN domain SA3SS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

Table 14-5855. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE	R/W	0h	MAIN domain Debug CBASS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
27	CLKGATE_CTRL0_MAIN_R5SS1_NOGATE	R/W	0h	MAIN domain R5SS1 auto clock gate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
26	CLKGATE_CTRL0_MAIN_R5SS0_NOGATE	R/W	0h	MAIN domain R5SS0 auto clock gate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
25	RESERVED	NONE	0h	Reserved
24	CLKGATE_CTRL0_MAIN_PDMA7_NOGATE	R/W	0h	MAIN domain PDMA7 (ASRC11) auto clock gate on idle disable. Field values (others are reserved): 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
23	CLKGATE_CTRL0_MAIN_PDMA6_NOGATE	R/W	0h	MAIN domain PDMA6 (ASRC0) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled 1'b0 - Auto clock gating enabled Reset Source: mod_por_rst_n
22	CLKGATE_CTRL0_MAIN_PDMA5_NOGATE	R/W	0h	MAIN domain PDMA5 (ADC) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
21	CLKGATE_CTRL0_MAIN_PDMA4_NOGATE	R/W	0h	MAIN domain PDMA4 (SPI/MCAN 1) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
20	CLKGATE_CTRL0_MAIN_PDMA3_NOGATE	R/W	0h	MAIN domain PDMA3 (McASP1) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
19	CLKGATE_CTRL0_MAIN_PDMA2_NOGATE	R/W	0h	MAIN domain PDMA2 (McASP0) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
18	CLKGATE_CTRL0_MAIN_PDMA1_NOGATE	R/W	0h	MAIN domain PDMA1 (UART) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
17	CLKGATE_CTRL0_MAIN_PDMA0_NOGATE	R/W	0h	MAIN domain PDMA0 (SPI/MCAN 0) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

Table 14-5855. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CLKGATE_CTRL0_MAIN_DMSS_NOGATE	R/W	0h	MAIN domain DMSS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
15	RESERVED	NONE	0h	Reserved
14	CLKGATE_CTRL0_MAIN_AUDIO_CBA_NOGATE	R/W	0h	MAIN domain Infrastructure bus (AUDIO) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
13	CLKGATE_CTRL0_MAIN_IPCSS_CBA_NOGATE	R/W	0h	MAIN domain Infrastructure CBASS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
12	CLKGATE_CTRL0_MAIN_MEM_CBA_NOGATE	R/W	1h	MAIN domain infrastructure bus (MEM) auto cloclk gate on idle disable Reset Source: mod_por_rst_n
11	CLKGATE_CTRL0_MAIN_MISC_PERI_CBA_NOGATE	R/W	0h	MAIN domain Infrastructure bus (Misc Peripheral) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
10:6	RESERVED	NONE	0h	Reserved
5	CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE	R/W	0h	MAIN domain data bus auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
4	CLKGATE_CTRL0_MAIN_DATA_CBA_NOGATE	R/W	0h	MAIN domain data bus auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
3	CLKGATE_CTRL0_MAIN_CENTRAL_CBA_NOGATE	R/W	1h	WKUP domain Infrastructure ECC aggregator auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
2	CLKGATE_CTRL0_WKUP_DM_PWR_NOGATE	R/W	1h	WKUP domain Device Manager auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
1	CLKGATE_CTRL0_WKUP_DM_CBA_NOGATE	R/W	1h	WKUP domain device manager CBA auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

Table 14-5855. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE	R/W	0h	MAIN domain Infrastructure bus auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

14.2.1.1.3.2.187 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Register

14.2.1.1.3.2.187.1 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Register (Offset = 18284h) [reset = 3F000000h]

Controls the power clock gating feature of modules and busses

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Table 14-5856. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8284h

Figure 14-2915. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED		CLKGATE_CTRL1_RAM5_NOGATE	CLKGATE_CTRL1_RAM4_NOGATE	CLKGATE_CTRL1_RAM3_NOGATE	CLKGATE_CTRL1_RAM2_NOGATE	CLKGATE_CTRL1_RAM1_NOGATE	CLKGATE_CTRL1_RAM0_NOGATE
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		1h	1h	1h	1h	1h	1h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			CLKGATE_CTRL1_C7X_1_NOGATE	CLKGATE_CTRL1_C7X_0_NOGATE	RESERVED		
NONE			R/W	R/W	NONE		
0h			0h	0h	0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5857. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	CLKGATE_CTRL1_RAM5_NOGATE	R/W	1h	MAIN SRAM bank 5 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
28	CLKGATE_CTRL1_RAM4_NOGATE	R/W	1h	MAIN SRAM bank 4 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
27	CLKGATE_CTRL1_RAM3_NOGATE	R/W	1h	MAIN SRAM bank 5 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

Table 14-5857. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	CLKGATE_CTRL1_RAM2_NOGATE	R/W	1h	MAIN SRAM bank 2 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
25	CLKGATE_CTRL1_RAM1_NOGATE	R/W	1h	MAIN SRAM bank 1 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
24	CLKGATE_CTRL1_RAM0_NOGATE	R/W	1h	MAIN SRAM bank 0 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
23:13	RESERVED	NONE	0h	Reserved
12	CLKGATE_CTRL1_C7X_1_NOGATE	R/W	0h	C7x_1 auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
11	CLKGATE_CTRL1_C7X_0_NOGATE	R/W	0h	C7x_0 auto clock gate on idle disable. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.188 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL Register

14.2.1.1.3.2.188.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL Register (Offset = 18300h) [reset = 0h]

Controls the operation of IO wakeup on the CANUART pins.

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Table 14-5858. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8300h

Figure 14-2916. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_CTRL_MW							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CANUART_WAKE_CTRL_MW							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CANUART_WAKE_CTRL_MW							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CANUART_WAKE_CTRL_MW							CANUART_WAKE_CTRL_MW_LOAD_EN
R/W							R/W
0h							0h

Table 14-5859. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CANUART_WAKE_CTRL_MW	R/W	0h	CANUART IO magic word. The lower 23 bits determine if the device enters CANUART IO isolation when mw_load_en is set. If the lower 23 bits match the ACTIVATE value (0x5AAAAA), then CANUART IO Isolation is entered, any other value will prevent entry. The upper 8 bits of this register are software defined and do not determine whether or not CANUART IO isolation is entered. Field values (others are reserved): 31'h005AAAAA - ACTIVATE 31'h00000000 - DEACTIVATE Reset Source: mcu_chip1_rst_n
0	CANUART_WAKE_CTRL_MW_LOAD_EN	R/W	0h	Magic word load enable Setting this bit loads and locks the mw field for CANUART IO isolation. If the mw field matches ACTIVATE, CANUART IO Isolation is initiated. Field values (others are reserved): 1'b0 - UNLOCK 1'b1 - LOCK_AND_LOAD Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.189 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0 Register

14.2.1.1.3.2.189.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0 Register (Offset = 18308h) [reset = 0h]

Provides the status of CANUART_WAKE control bits. These bits come from the daisy-chain wakeup logic and maintain their value across core powerdown if isolation is activated.

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Table 14-5860. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8308h

Figure 14-2917. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CANUART_WAKE_STAT0_MW_STAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CANUART_WAKE_STAT0_MW_STAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CANUART_WAKE_STAT0_MW_STAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">CANUART_WAKE_STAT0_MW_STAT</td><td>CANUART_WAKE_STAT0_MW_LOAD_STAT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">X</td><td>X</td></tr>
</table>

Table 14-5861. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CANUART_WAKE_STAT0_MW_STAT	R	X	CANUART magic word status Indicates the latched value of the mw field. Reset Source: mod_por_rst_n
0	CANUART_WAKE_STAT0_MW_LOAD_STAT	R	X	Magic word load status. Indicates the latched value of the mw_load_en bit Reset Source: mod_por_rst_n

14.2.1.1.3.2.190 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1 Register

14.2.1.1.3.2.190.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1 Register (Offset = 1830Ch) [reset = 0h]

Provides CANUART IO isolation status. These bits come from the daisy-chain wakeup logic and maintain their value across core powerdown if isolation is activated

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Table 14-5862. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 830Ch

Figure 14-2918. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CANUART_WAKE_STAT1_CANUART_IO_MODE
NONE							R
0h							X

Table 14-5863. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CANUART_WAKE_STAT1_CANUART_IO_MODE	R	X	Indicates if CANUART IO wakeup mode is enabled. Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVATED Reset Source: mod_por_rst_n

14.2.1.1.3.2.191 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE Register

14.2.1.1.3.2.191.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE Register (Offset = 18310h) [reset = 0h]

CANUART IO Domain OFF Mode Magic Word Register

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Table 14-5864. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8310h

Figure 14-2919. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_OFF_MODE_MW							
R/W							
0h							
23	22	21	20	19	18	17	16
CANUART_WAKE_OFF_MODE_MW							
R/W							
0h							
15	14	13	12	11	10	9	8
CANUART_WAKE_OFF_MODE_MW							
R/W							
0h							
7	6	5	4	3	2	1	0
CANUART_WAKE_OFF_MODE_MW							
R/W							
0h							

Table 14-5865. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CANUART_WAKE_OFF_MODE_MW	R/W	0h	magic word Reset Source: mod_por_rst_n

14.2.1.1.3.2.192 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT Register

14.2.1.1.3.2.192.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT Register (Offset = 18318h) [reset = 0h]

CANUART IO Domain OFF Mode Magic Word Register

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Table 14-5866. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8318h

Figure 14-2920. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CANUART_WAKE_OFF_MODE_STAT_MW</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CANUART_WAKE_OFF_MODE_STAT_MW</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CANUART_WAKE_OFF_MODE_STAT_MW</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CANUART_WAKE_OFF_MODE_STAT_MW</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-5867. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CANUART_WAKE_OFF_MODE_STAT_MW	R	X	returned magic word Reset Source: mod_por_rst_n

14.2.1.1.3.2.193 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_j Register

14.2.1.1.3.2.193.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_j Register (Offset = 18320h) [reset = 0h]

CAN_UART IO Domain Resume Key Value Register

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Table 14-5868. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8320h + formula

Figure 14-2921. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_j Name Register

31	30	29	28	27	26	25	24
KEYVAL							
R/W							
0h							
23	22	21	20	19	18	17	16
KEYVAL							
R/W							
0h							
15	14	13	12	11	10	9	8
KEYVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
KEYVAL							
R/W							
0h							

Table 14-5869. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEYVAL	R/W	0h	key value Reset Source: mod_por_rst_n

14.2.1.1.3.2.194 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_j Register

14.2.1.1.3.2.194.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_j Register (Offset = 18340h) [reset = 0h]

CAN_UART IO Domain Resume Key Value Register

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Table 14-5870. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8340h + formula

Figure 14-2922. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_j Name Register

31	30	29	28	27	26	25	24
KEYVAL							
R							
X							
23	22	21	20	19	18	17	16
KEYVAL							
R							
X							
15	14	13	12	11	10	9	8
KEYVAL							
R							
X							
7	6	5	4	3	2	1	0
KEYVAL							
R							
X							

Table 14-5871. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEYVAL	R	X	returned key value Reset Source: mod_por_rst_n

14.2.1.1.3.2.195 WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL Register

14.2.1.1.3.2.195.1 WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL Register (Offset = 18360h) [reset = 0h]

Controls monitoring of wake events during IO retention entry/exit

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Table 14-5872. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8360h

Figure 14-2923. WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL Name Register

31	30	29	28	27	26	25	24
WAKE_EVT_MON_CTRL_WAKE_TIMEOUT_DIS	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							WAKE_EVT_MON_CTRL_CLR_WAKE_EVT
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							WAKE_EVT_MON_CTRL_EN_WAKE_EVT_MON
NONE							R/W
0h							0h

Table 14-5873. WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WAKE_EVT_MON_CTRL_WAKE_TIMEOUT_DIS	R/W	0h	Disable wakeup event timeout window. Field values (others are reserved): 1'b0 - An Internal POR is generated when a wakeup event is detected by the IORET entry/exit wakeup event monitor before the Immediate Wakeup Timeout window expiration 1'b1 - The immediate wakeup timeout window is disabled. Reset Source: mod_por_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	WAKE_EVT_MON_CTRL_CLR_WAKE_EVT	R/W	0h	Clear wakeup events. Write 1 to clear all wakeup events. Read always returns 0. Field values (others are reserved): 1'b0 - Read value. Writing 0 has no effect 1'b1 - Clear all wake events Reset Source: mod_por_rst_n
15:1	RESERVED	NONE	0h	Reserved

Table 14-5873. WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAKE_EVT_MON_CTRL_EN_WAKE_EVT_MON	R/W	0h	Enable wakeup event monitoring. Field values (others are reserved): 1'b0 - All IORET entry/exit wakeup event monitoring is disabled 1'b1 - Enable wakeup event monitoring during IORET entry/exit. The pins to be monitored are determined by the corresponding PADCONFIG register settings Reset Source: mod_por_rst_n

14.2.1.1.3.2.196 WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR Register

14.2.1.1.3.2.196.1 WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR Register (Offset = 18364h) [reset = 20h]

Determines how long the IPOR generated by IORET entry/exit wakeup monitoring will be asserted

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Table 14-5874. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8364h

Figure 14-2924. WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INTRN_POR_DUR_IPOR_LEN							
R/W							
20h							

Table 14-5875. WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTRN_POR_DUR_IPOR_LEN	R/W	20h	Specifies the number of HFOSC0 clock cycles to assert IPORz (low) when the wake monitoring logic detects a wakeup event. This value must exceed the minimum PORz period for the device with stable power supplies and reference clocks (1200 ns) Reset Source: mod_por_rst_n

14.2.1.1.3.2.197 WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT Register

14.2.1.1.3.2.197.1 WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT Register (Offset = 18368h) [reset = EAh]

Determines the length of the timing window during which a monitored wakeup event will generate an IPOR. This ensures wakeup events occurring soon after PMIC_EN deactivation but before IORET state entry are recognized. After this window has expired, the external PMIC is expected to generate a POR based on PMIC_EN activation. The ImmediateWakeup Timeout window is disabled (no IPOR generated) if the wake_timeout_dis in WAKE_EVT_MON_CTRL is 1.

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Table 14-5876. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8368h

Figure 14-2925. WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IMMED_WAKE_TIMEOUT_TIMEOUT_LENGTH							
R/W							
EAh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IMMED_WAKE_TIMEOUT_TIMEOUT_LENGTH							
R/W							
EAh							

Table 14-5877. WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	IMMED_WAKE_TIMEOUT_TIMEOUT_LENGTH	R/W	EAh	Specifies the number of HFOSC0 clock cycles during which wake monitoring logic will issue an internal POR. This timeout value must exceed the PMIC glitch filtering window for its PMIC_EN input. (Default value is 9 s at 26 MHz HFOSC0) Reset Source: mod_por_rst_n

14.2.1.1.3.2.198 WKUP_CTRL_MMR_CFG0_RET_RAM_STAT Register

14.2.1.1.3.2.198.1 WKUP_CTRL_MMR_CFG0_RET_RAM_STAT Register (Offset = 18380h) [reset = 0h]

Shows the Retention RAM Status

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Table 14-5878. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8380h

Figure 14-2926. WKUP_CTRL_MMR_CFG0_RET_RAM_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h						X	
15	14	13	12	11	10	9	8
	RESERVED						RET_RAM_STAT_ISOLATED
	NONE						R
X	0h						X
7	6	5	4	3	2	1	0
RESERVED							RET_RAM_STAT_BUSY
NONE							R
0h							X

Table 14-5879. WKUP_CTRL_MMR_CFG0_RET_RAM_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
14:9	RESERVED	NONE	0h	Reserved
8	RET_RAM_STAT_ISOLATED	R	X	Indicates Retention RAM isolation state (when busy=0) Field values (others are reserved): 1'b0 - RAM is not isolated 1'b1 - RAM is isolated Reset Source: mod_por_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	RET_RAM_STAT_BUSY	R	X	Indicates that Retention RAM state is transitioning. The RAM must not be accessed or the isolation powerdown sequence continued while busy=1 Field values (others are reserved): 1'b0 - RAM is in isolation state indicated by the isolated bit 1'b1 - RAM isolation state is transitioning - do not access Reset Source: mod_por_rst_n

14.2.1.1.3.2.199 WKUP_CTRL_MMR_CFG0_WFI_STATUS Register

14.2.1.1.3.2.199.1 WKUP_CTRL_MMR_CFG0_WFI_STATUS Register (Offset = 18400h) [reset = 0h]

Allows inspection of WFI Status of all CPU Cores

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Table 14-5880. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8400h

Figure 14-2927. WKUP_CTRL_MMR_CFG0_WFI_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							WFI_STATUS_MAIN_R5FSS1_CORE1_WFI
NONE							R
0h							X
7	6	5	4	3	2	1	0
WFI_STATUS_MAIN_R5FSS1_CORE0_WFI	WFI_STATUS_MAIN_R5FSS0_CORE1_WFI	WFI_STATUS_MAIN_R5FSS0_CORE0_WFI	RESERVED	WFI_STATUS_SMS_CPU1_WFI	WFI_STATUS_SMS_CPU0_WFI	RESERVED	WFI_STATUS_WKUP_R5F_WFI
R	R	R	NONE	R	R	NONE	R
X	X	X	0h	X	X	0h	X

Table 14-5881. WKUP_CTRL_MMR_CFG0_WFI_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	WFI_STATUS_MAIN_R5FSS1_CORE1_WFI	R	X	WFI status of MAIN Cortex R5F_1 Core 1 (only valid when core is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
7	WFI_STATUS_MAIN_R5FSS1_CORE0_WFI	R	X	WFI status of MAIN Cortex R5F_1 Core 0 (only valid when core is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
6	WFI_STATUS_MAIN_R5FSS0_CORE1_WFI	R	X	WFI status of MAIN Cortex R5F_0 Core 0 (only valid when core is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n

Table 14-5881. WKUP_CTRL_MMR_CFG0_WFI_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	WFI_STATUS_MAIN_R5FSS0_CORE0_WFI	R	X	WFI status of MAIN Cortex R5F_0 Core 0 (only valid when core is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
4	RESERVED	NONE	0h	Reserved
3	WFI_STATUS_SMS_CPU1_WFI	R	X	WFI status of SMS Cortex M4F1 (only valid when CPU is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
2	WFI_STATUS_SMS_CPU0_WFI	R	X	WFI status of SMS Cortex M4F0 (only valid when CPU is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	WFI_STATUS_WKUP_R5F_WFI	R	X	WFI status of Device Manager Cortex R5F (only valid when CPU is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n

14.2.1.1.3.2.200 WKUP_CTRL_MMR_CFG0_DS_MAIN Register

14.2.1.1.3.2.200.1 WKUP_CTRL_MMR_CFG0_DS_MAIN Register (Offset = 18420h) [reset = Fh]

Reset Control and Main Power Domain Control

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Table 14-5882. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8420h

Figure 14-2928. WKUP_CTRL_MMR_CFG0_DS_MAIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DS_MAIN_POR_PDOFF			
NONE				R/W			
0h				Fh			

Table 14-5883. WKUP_CTRL_MMR_CFG0_DS_MAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_MAIN_POR_PDOFF	R/W	Fh	Signal Puts main SMS, DebugSS and MainIP Power Domains into Power Off state, and asserts Main Power On Reset. Field values (others are reserved): 4'b0110 - Off 4'b1111 - On Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.201 WKUP_CTRL_MMR_CFG0_DS_DM_RESET Register

14.2.1.1.3.2.201.1 WKUP_CTRL_MMR_CFG0_DS_DM_RESET Register (Offset = 18440h) [reset = Fh]

Reset Isolation for the Device Manager

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Table 14-5884. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8440h

Figure 14-2929. WKUP_CTRL_MMR_CFG0_DS_DM_RESET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_DM_RESET_MASK			
NONE				R/W			
0h				Fh			

Table 14-5885. WKUP_CTRL_MMR_CFG0_DS_DM_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_DM_RESET_MASK	R/W	Fh	Signal used to mask main domain resets from Device Manager / Wakeup and MCU Ips Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.202 WKUP_CTRL_MMR_CFG0_DS_USB0_RESET Register

14.2.1.1.3.2.202.1 WKUP_CTRL_MMR_CFG0_DS_USB0_RESET Register (Offset = 18460h) [reset = Fh]

Reset Isolation for the USB0 Subsystem

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Table 14-5886. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8460h

Figure 14-2930. WKUP_CTRL_MMR_CFG0_DS_USB0_RESET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_USB0_RESET_MASK			
NONE				R/W			
0h				Fh			

Table 14-5887. WKUP_CTRL_MMR_CFG0_DS_USB0_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_USB0_RESET_MASK	R/W	Fh	Signal used to block reset to the USBSS0 Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.203 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ Register

14.2.1.1.3.2.203.1 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ Register (Offset = 184A0h) [reset = 0h]

Initiate Clockstop Request Sequence on WKUP Peripherals Activated in DM_CLKSTOP_EN

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Table 14-5888. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 84A0h

Figure 14-2931. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DM_GRP_CLKSTOP_REQ_REQ
NONE							R/W
0h							0h

Table 14-5889. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DM_GRP_CLKSTOP_REQ_REQ	R/W	0h	Controls Assertion of Clockstop Request to IPs participating in Clockstop Req Group Field values (others are reserved): 1'b0 - DEASSERT_REQ 1'b1 - ASSERT_REQ Reset Source: mod_por_rst_n

14.2.1.1.3.2.204 WKUP_CTRL_MMR_CFG0_DEVICE_TYPE Register

14.2.1.1.3.2.204.1 WKUP_CTRL_MMR_CFG0_DEVICE_TYPE Register (Offset = 18500h) [reset = 0h]

Device Type as Decoded by SMS

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Table 14-5890. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 8500h

Figure 14-2932. WKUP_CTRL_MMR_CFG0_DEVICE_TYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEVICE_TYPE_SMS_DEV_TYPE							
R							
X				X			

Table 14-5891. WKUP_CTRL_MMR_CFG0_DEVICE_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DEVICE_TYPE_SMS_DEV_TYPE	R	X	Type of device reported by SMS. Values not listed should be interpreted as BAD. Field values (others are reserved): 4'b0101 - DT_TEST 4'b1001 - DT_EMU 4'b1010 - DT_HS 4'b0011 - DT_GP Reset Source: mod_por_rst_n

14.2.1.1.3.2.205 WKUP_CTRL_MMR_CFG0_LOCK6_KICK0 Register

14.2.1.1.3.2.205.1 WKUP_CTRL_MMR_CFG0_LOCK6_KICK0 Register (Offset = 19008h) [reset = 0h]

- KICK0 component

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Table 14-5892. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9008h

Figure 14-2933. WKUP_CTRL_MMR_CFG0_LOCK6_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0							
R/W							
0h							

Table 14-5893. WKUP_CTRL_MMR_CFG0_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.206 WKUP_CTRL_MMR_CFG0_LOCK6_KICK1 Register

14.2.1.1.3.2.206.1 WKUP_CTRL_MMR_CFG0_LOCK6_KICK1 Register (Offset = 1900Ch) [reset = 0h]

- KICK1 component

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Table 14-5894. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 900Ch

Figure 14-2934. WKUP_CTRL_MMR_CFG0_LOCK6_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1							
R/W							
0h							

Table 14-5895. WKUP_CTRL_MMR_CFG0_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.207 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register

14.2.1.1.3.2.207.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register (Offset = 19100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5896. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9100h

Figure 14-2935. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R0_READONLY							
R							
0h							

Table 14-5897. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.208 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register

14.2.1.1.3.2.208.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register (Offset = 19104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5898. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9104h

Figure 14-2936. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1_READONLY							
R							
0h							

Table 14-5899. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.209 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register

14.2.1.1.3.2.209.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register (Offset = 19108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5900. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9108h

Figure 14-2937. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2_READONLY							
R							
0h							

Table 14-5901. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.210 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register

14.2.1.1.3.2.210.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register (Offset = 1910Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-5902. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 910Ch

Figure 14-2938. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3_READONLY							
R							
0h							

Table 14-5903. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.211 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register

14.2.1.1.3.2.211.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register (Offset = 19110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5904. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9110h

Figure 14-2939. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4_READONLY							
R							
0h							

Table 14-5905. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.212 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register

14.2.1.1.3.2.212.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register (Offset = 19114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5906. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9114h

Figure 14-2940. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5_READONLY							
R							
0h							

Table 14-5907. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.213 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register

14.2.1.1.3.2.213.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register (Offset = 19118h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5908. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9118h

Figure 14-2941. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R6_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R6_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R6_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R6_READONLY							
R							
0h							

Table 14-5909. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R6_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.214 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register

14.2.1.1.3.2.214.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register (Offset = 1911Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-5910. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 911Ch

Figure 14-2942. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R7_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R7_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R7_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R7_READONLY							
R							
0h							

Table 14-5911. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R7_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.215 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register

14.2.1.1.3.2.215.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register (Offset = 19120h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5912. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9120h

Figure 14-2943. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R8_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R8_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R8_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R8_READONLY							
R							
0h							

Table 14-5913. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R8_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.216 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY Register

14.2.1.1.3.2.216.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY Register (Offset = 19124h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5914. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9124h

Figure 14-2944. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R9_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R9_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R9_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R9_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5915. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R9_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.217 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY Register

14.2.1.1.3.2.217.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY Register (Offset = 19128h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5916. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 9128h

Figure 14-2945. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R10_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R10_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R10_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R10_READONLY							
R							
0h							

Table 14-5917. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R10_READONLY	R	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.218 WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY Register

14.2.1.1.3.2.218.1 WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY Register (Offset = 1A080h) [reset = 10h]

Controls operation of the PMIC_LPM_EN pin

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Table 14-5918. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A080h

Figure 14-2946. WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PMCTRL_SYS_PMIC_EN_WE_PROXY	PMCTRL_SYS_PMIC_EN_PROXY	PMCTRL_SYS_LPM_EN_WE_PROXY	PMCTRL_SYS_LPM_EN_PROXY		
NONE		R/W	R/W	R/W	R/W		
0h		0h	1h	0h	0h		

Table 14-5919. WKUP_CTRL_MMR_CFG0_PMCTRL_SYS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	PMCTRL_SYS_PMIC_EN_WE_PROXY	R/W	0h	Unused Field - Value is Don't Care Reset Source: mod_g_rst_n
4	PMCTRL_SYS_PMIC_EN_PROXY	R/W	1h	Controls state of PMIC_LPM_EN_OUT when LPM_EN[2:0] is 000 Reset Source: mod_g_rst_n
3	PMCTRL_SYS_LPM_EN_WE_PROXY	R/W	0h	Unused Field - Value is Don't Care Reset Source: mod_g_rst_n
2:0	PMCTRL_SYS_LPM_EN_PROXY	R/W	0h	Controls whether PMIC_LPM_EN_OUT is driven by the pmic_en bit. Field values (others are reserved): 3'b000 - PMIC_LPM_EN_OUT controlled by pmic_en bit. Reset Source: mod_g_rst_n

14.2.1.1.3.2.219 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Register

14.2.1.1.3.2.219.1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Register (Offset = 1A084h) [reset = 0h]

This register is writable only when LOCK6-KICK0:1 are unlocked

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Table 14-5920. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A084h

Figure 14-2947. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED						PMCTRL_IO_0_IO_ISO_STATUS_0_PROXY	PMCTRL_IO_0_IO_ISO_CTRL_0_PROXY
NONE						R	R/W
0h						X	0h
23	22	21	20	19	18	17	16
RESERVED							PMCTRL_IO_0_GLOBAL_WUEN_0_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED						PMCTRL_IO_0_WUCLK_STATUS_0_PROXY	PMCTRL_IO_0_WUCLK_CTRL_0_PROXY
NONE						R	R/W
0h						X	0h
7	6	5	4	3	2	1	0
RESERVED	PMCTRL_IO_0_ISOBYPASS_OVR_0_PROXY	PMCTRL_IO_0_IO_ON_STATUS_0_PROXY	PMCTRL_IO_0_ISOOVR_EXTEND_0_PROXY	RESERVED		PMCTRL_IO_0_ISOCLK_STATUS_0_PROXY	PMCTRL_IO_0_ISOCLK_OVRD_0_PROXY
NONE	R/W	R	R/W	NONE		R	R/W
0h	0h	X	0h	0h		X	0h

Table 14-5921. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	PMCTRL_IO_0_IO_ISO_STATUS_0_PROXY	R	X	IO ISO Status. Read 0: IO isolation not active. Read 1: IO isolation active. Reflects value of SMS input port io_isoack coming back from IO pad ring. Reset Source: mod_g_rst_n
24	PMCTRL_IO_0_IO_ISO_CTRL_0_PROXY	R/W	0h	IO ISO control. Writing this bit to 1 will kick off IO isolation. Reset Source: mod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved

Table 14-5921. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PMCTRL_IO_0_GLOBAL_WUEN_0_PROXY	R/W	0h	Global IO wakeup enable. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Io Logiclogic. 0:All individual IO WUEN are gated in the IO logic (override to 0). 1: All individual IO WUEN from control module are going to IOs. Map to SMS input port io_globalwkupen Reset Source: mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	PMCTRL_IO_0_WUCLK_STATUS_0_PROXY	R	X	Reflects value of DM input port io_wuclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
8	PMCTRL_IO_0_WUCLK_CTRL_0_PROXY	R/W	0h	Direct control on WUCLKIN signal to IO pad ring.0:WUCLKIN signal is driven to 0.IO wakeup daisy chain is functional as well as IO whose wakeup feature is enabled. 1:WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs. Reset Source: mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	PMCTRL_IO_0_ISOBYPASS_OVR_0_PROXY	R/W	0h	This MMR bit drives directly DM output port io_isobypassundefined. Reset Source: mod_g_rst_n
5	PMCTRL_IO_0_IO_ON_STATUS_0_PROXY	R	X	Gives the functional status of the IO ring. Read 0: Part or all of the IOs are not in the ON state that is are in isolation state. Read 1: All IOs are in the ON state. io_on_status = assign 1 if (io_iso == 0 & io_isoack==0 & io_iso_clk == 0 & io_isoclk_ack = 0) else 0; Reset Source: mod_g_rst_n
4	PMCTRL_IO_0_ISOOVR_EXTEND_0_PROXY	R/W	0h	This drives the SOC chain ISO-OVERRIDE global control. This bit drives directly the DM output port io_isoovrundefined. At the SOC level it is used to enable when 1 or gate-off when 0, the individual ISOOR for each IO. This operates as a global enable/disable for the individual IOs.Control for IO isolation extension. '0' IO isolation is not extended. Transition happens as soon as automatic restore is completed. '1' IO isolation is extended. The IOs whose ISOOVR bits have been individually set in their PADCFG MMRs will all get its IO isolation extended beyond the point when the initial IO daisy chain isolation is released. Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PMCTRL_IO_0_ISOCLK_STATUS_0_PROXY	R	X	Reflects value of DM input port io_isoclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
0	PMCTRL_IO_0_ISOCLK_OVRD_0_PROXY	R/W	0h	Override control on ISOCLKIN signal to IO pad ring. When not overridden this signal is controlled by hardware only. 0 ISOCLKIN signal is not override. 1 ISOCLKIN signal is overridden to active value ('1'). Reset Source: mod_g_rst_n

14.2.1.1.3.2.220 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Register

14.2.1.1.3.2.220.1 WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Register (Offset = 1A088h) [reset = 0h]

This register is writable only when LOCK6-KICK0:1 are unlocked

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Table 14-5922. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A088h

Figure 14-2948. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Name Register

31	30	29	28	27	26	25	24
PMCTRL_IO_1_RESERVED4_PROXY						PMCTRL_IO_1_IO_ISO_STATUS_1_PROXY	PMCTRL_IO_1_IO_ISO_CTRL_1_PROXY
R						R	R/W
X						X	0h

23	22	21	20	19	18	17	16
RESERVED							PMCTRL_IO_1_GLOBAL_WUEN_1_PROXY
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED						PMCTRL_IO_1_WUCLK_STATUS_1_PROXY	PMCTRL_IO_1_WUCLK_CTRL_1_PROXY
NONE						R	R/W
0h						X	0h

7	6	5	4	3	2	1	0
RESERVED	PMCTRL_IO_1_ISOBYPASS_OVR_1_PROXY	PMCTRL_IO_1_IO_ON_STATUS_1_PROXY	PMCTRL_IO_1_ISOOVR_EXTEND_1_PROXY	RESERVED		PMCTRL_IO_1_ISOCLK_STATUS_1_PROXY	PMCTRL_IO_1_ISOCLK_OVRD_1_PROXY
NONE	R/W	R	R/W	NONE		R	R/W
0h	0h	X	0h	0h		X	0h

Table 14-5923. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	PMCTRL_IO_1_RESERVED4_PROXY	R	X	reserved
25	PMCTRL_IO_1_IO_ISO_STATUS_1_PROXY	R	X	IO ISO Status. Read 0: IO isolation not active. Read 1: IO isolation active. Reflects value of DM input port io_isoack coming back from IO pad ring. Reset Source: mod_g_rst_n
24	PMCTRL_IO_1_IO_ISO_CTRL_1_PROXY	R/W	0h	IO ISO control. Writing this bit to 1 will kick off IO isolation. Reset Source: mod_g_rst_n
23:17	RESERVED	NONE	0h	Reserved

Table 14-5923. WKUP_CTRL_MMR_CFG0_PMCTRL_IO_1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PMCTRL_IO_1_GLOBAL_WUEN_1_PROXY	R/W	0h	Global IO wakeup enable. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Spinner logic. 0:All individual IO WUEN are gated in the Spinner logic (override to 0). 1: All individual IO WUEN from control module are going to Ios. Map to DM input port io_globalwkupen Reset Source: mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
9	PMCTRL_IO_1_WUCLK_STATUS_1_PROXY	R	X	Reflects value of DM input port io_wuclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
8	PMCTRL_IO_1_WUCLK_CTRL_1_PROXY	R/W	0h	Direct control on WUCLKIN signal to IO pad ring.0:WUCLKIN signal is driven to 0.IO wakeup daisy chain is functional as well as IO whose wakeup feature is enabled. 1:WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs. Reset Source: mod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6	PMCTRL_IO_1_ISOBYPASS_OVR_1_PROXY	R/W	0h	This MMR bit drives directly DM output port io_isobypassundefined. Reset Source: mod_g_rst_n
5	PMCTRL_IO_1_IO_ON_STATUS_1_PROXY	R	X	Gives the functional status of the IO ring. Read 0: Part or all of the Ios are not in the ON state that is are in isolation state. Read 1: All Ios are in the ON state. io_on_status = assign 1 if (io_iso == 0 & io_isoack==0 & io_iso_clk == 0 & io_isoclk_ack = 0) else 0; Reset Source: mod_g_rst_n
4	PMCTRL_IO_1_ISOOVR_EXTEND_1_PROXY	R/W	0h	This drives the SOC chain ISO-OVERRIDE global control. This bit drives directly the DM output port io_isoovrundefined. At the SOC level it is used to enable when 1 or gate-off when 0, the individual ISOOR for each IO. This operates as a global enable/disable for the individual IOs.Control for IO isolation extension. '0' IO isolation is not extended. Transition happens as soon as automatic restore is completed. '1' IO isolation is extended. The IOs whose ISOOVR bits have been individually set in their PADCFG MMRs will all get its IO isolation extended beyond the point when the initial IO daisy chain isolation is released. Reset Source: mod_g_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	PMCTRL_IO_1_ISOCLK_STATUS_1_PROXY	R	X	Reflects value of DM input port io_isoclkack coming back from IO pad ring. Reset Source: mod_g_rst_n
0	PMCTRL_IO_1_ISOCLK_OVRD_1_PROXY	R/W	0h	Override control on ISOCLKIN signal to IO pad ring. When not overridden this signal is controlled by hardware only. 0 ISOCLKIN signal is not override. 1 ISOCLKIN signal is overridden to active value ('1'). Reset Source: mod_g_rst_n

14.2.1.1.3.2.221 WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY Register

14.2.1.1.3.2.221.1 WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY Register (Offset = 1A090h) [reset = BC00h]

This register is writable only when LOCK6-KICK0:1 are unlocked

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Table 14-5924. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A090h

Figure 14-2949. WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY Name Register

31	30	29	28	27	26	25	24
PMCTRL_MOSC_OSC_CG_ON_WFI_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PMCTRL_MOSC_SETUP_TIME_PROXY			
NONE				R/W			
0h				BC00h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMCTRL_MOSC_SETUP_TIME_PROXY							
R/W							
BC00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMCTRL_MOSC_SETUP_TIME_PROXY							
R/W							
BC00h							

Table 14-5925. WKUP_CTRL_MMR_CFG0_PMCTRL_MOSC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PMCTRL_MOSC_OSC_CG_ON_WFI_PROXY	R/W	0h	To clock gate the main HFOSC, DM sets this bit then enters the WFI state at which time the HFOSC will be gated. Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVE Reset Source: mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:0	PMCTRL_MOSC_SETUP_TIME_PROXY	R/W	BC00h	Number of HFOSC clock cycles before HFOSC clock is ungated to the SOC (allows the HFOSC time to stabilize after starting up, before the SOC is clocked). Reset Source: mod_g_rst_n

14.2.1.1.3.2.222 WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY Register

14.2.1.1.3.2.222.1 WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY Register (Offset = 1A098h) [reset = 0h]

Reflects the progress of the request to clock-gate HFOSC via MMR PMCTRL_MOSCundefined.

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Table 14-5926. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A098h

Figure 14-2950. WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PM_MISC_STATUS_OSC_CG_STAT_PROXY	
NONE						R	
0h						X	

Table 14-5927. WKUP_CTRL_MMR_CFG0_PM_MISC_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PM_MISC_STATUS_OSC_CG_STAT_PROXY	R	X	HFOSC Clock Gating State Field values (others are reserved): 2'b00 - HFOSC_OFF 2'b01 - HFOSC_OFF2ON (transition state) 2'b10 - HFOSC_ON2OFF (transition state) 2'b11 - HFOSC_ON Reset Source: mod_g_rst_n

14.2.1.1.3.2.223 WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Register

14.2.1.1.3.2.223.1 WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Register (Offset = 1A170h) [reset = 200FFh]

Controls Reset Assertion and Propogation

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Table 14-5928. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A170h

Figure 14-2951. WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					RST_CTRL_MAIN_RESET_ISO_DONE_Z_PROXY	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z_PROXY	RST_CTRL_SMS_COLD_RESET_EN_Z_PROXY
NONE					R/W	R/W	R/W
0h					0h	1h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
Fh				Fh			

Table 14-5929. WKUP_CTRL_MMR_CFG0_RST_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	RST_CTRL_MAIN_RESET_ISO_DONE_Z_PROXY	R/W	0h	Blocks Main Domain Warm Reset. Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: main_chip1_rst_n
17	RST_CTRL_MAIN_ESM_ERROR_RST_EN_Z_PROXY	R/W	1h	Block Reset of Main by ESM Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: main_chip1_rst_n
16	RST_CTRL_SMS_COLD_RESET_EN_Z_PROXY	R/W	0h	Block Reset of Main by SMS Field values (others are reserved): 1'b0 - PROPOGATE 1'b1 - BLOCK Reset Source: main_chip1_rst_n
15:8	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.224 WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY Register

14.2.1.1.3.2.224.1 WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY Register (Offset = 1A174h) [reset = 0h]

Reset Status

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Table 14-5930. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A174h

Figure 14-2952. WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RST_STAT_MCU_RESET_ISO_DONE_Z_PROXY
NONE							R
0h							X

Table 14-5931. WKUP_CTRL_MMR_CFG0_RST_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RST_STAT_MCU_RESET_ISO_DONE_Z_PROXY	R	X	Indicates MCU Domain is in Reset Isolation When Active (Low) Field values (others are reserved): 1'b0 - ISOLATION 1'b1 - PASS_THROUGH Reset Source: main_chip1_rst_n

14.2.1.1.3.2.225 WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Register

14.2.1.1.3.2.225.1 WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Register (Offset = 1A178h) [reset = 0h]

Captures Reason for Warm and Main Domain Power On Resets Read Only Mirror of MCU CTRL MMR version. Clearing these bits must be done through the MCU CTRL MMR.

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Table 14-5932. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A178h

Figure 14-2953. WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Name Register

31	30	29	28	27	26	25	24
RST_SRC_SAFETY_ERROR_PROXY	RST_SRC_MAIN_ESM_ERROR_PROXY	RESERVED					
R	R	NONE					
X	X	0h				X	X
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	RST_SRC_DM_WDT_RST_PROXY			RESERVED			RST_SRC_SW_MCU_WARMRST_PROXY
NONE	R			NONE			R
0h	X	X	X	0h			X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		RST_SRC_WARM_OUT_RST_PROXY	RST_SRC_COLD_OUT_RST_PROXY	RESERVED			RST_SRC_DEBUG_RST_PROXY
NONE		R	R	NONE			R
0h		X	X	0h			X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RST_SRC_IPOR_WAKE_PROXY	RESERVED	RST_SRC_THERMAL_RST_PROXY	RESERVED		RESERVED	RST_SRC_MCU_RESET_PIN_PROXY
NONE	R	NONE	R	NONE		NONE	R
0h	X	0h	X	0h	X	0h	X

Table 14-5933. WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RST_SRC_SAFETY_ERROR_PROXY	R	X	Reset Caused by MCU ESM Error. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
30	RST_SRC_MAIN_ESM_ERROR_PROXY	R	X	Reset Caused by Main ESM Error. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
29:26	RESERVED	NONE	0h	Reserved
23	RESERVED	NONE	0h	Reserved

Table 14-5933. WKUP_CTRL_MMR_CFG0_RST_SRC_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RST_SRC_DM_WDT_RST_PROXY	R	X	Watchdog Initiated Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
19:17	RESERVED	NONE	0h	Reserved
16	RST_SRC_SW_MCU_WARMRST_PROXY	R	X	Software Warm Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	RST_SRC_WARM_OUT_RST_PROXY	R	X	SMS Warm Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
12	RST_SRC_COLD_OUT_RST_PROXY	R	X	SMS Cold Reset. When set, indicates that a SMS Cold reset occurred and reset either MAIN or MCU domains (or both). Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	RST_SRC_DEBUG_RST_PROXY	R	X	Debug Subsystem Initiated Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
7	RESERVED	NONE	0h	Reserved
6	RST_SRC_IPOR_WAKE_PROXY	R	X	Wake Event Monitor Internal Power On Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
5	RESERVED	NONE	0h	Reserved
4	RST_SRC_THERMAL_RST_PROXY	R	X	Thermal Reset. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n
3	RESERVED	NONE	0h	Reserved
1	RESERVED	NONE	0h	Reserved
0	RST_SRC_MCU_RESET_PIN_PROXY	R	X	Rest Caused by MCU Reset Pin. Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - DETECTED Reset Source: main_chip1_rst_n

14.2.1.1.3.2.226 WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register

14.2.1.1.3.2.226.1 WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register (Offset = 1A17Ch) [reset = 0h]

Read Only Mirror of MCU CTRL MMR version. After an MCU_PORz reset this bit field resets to 0x00000000. While this bit field remains 0x00000000 any warm reset from the Main Domain also propagates through the MCU domain. If the application does not require reset isolation of the MCU domain, it may leave this bit field with a value of 0x00000000. If the application does require reset isolation of the MCU domain after the initial boot, then the R5FSS CPU must write a nonzero value to the magic word. The actual value is left to software and different values may be used to convey information, but in order to isolate the MCU domain from all Main domain warm reset sources that trigger main_resetz, the value must be non-zero. If the value is nonzero and one of the Main domain warm reset sources triggers main_resetz occurs in the main domain, the R5FSS will not be reset. The Main domain bootloader must read this value to determine that the R5FSS is already initialized, and has configured reset isolation. The Main domain bootloader then also skips any initialization steps involving bootstrapping the R5FSS as it is is already running. Note that MCU_PORz reset is never blocked by a nonzero magic word.

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Table 14-5934. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A17Ch

Figure 14-2954. WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Name Register

31	30	29	28	27	26	25	24
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
23	22	21	20	19	18	17	16
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
15	14	13	12	11	10	9	8
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							
7	6	5	4	3	2	1	0
RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY							
R							
X							

Table 14-5935. WKUP_CTRL_MMR_CFG0_RST_MAGIC_WORD_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RST_MAGIC_WORD_MCU_MAGIC_WORD_PROXY	R	X	Magic Word Indicating Status of MCU Subsystem Boot Reset Source: main_chip1_rst_n

14.2.1.1.3.2.227 WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY Register

14.2.1.1.3.2.227.1 WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY Register (Offset = 1A180h) [reset = 0h]

Selects active wake-up sources

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Table 14-5936. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A180h

Figure 14-2955. WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY Name Register

31	30	29	28	27	26	25	24
WKUP0_EN_WKUPEN_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
WKUP0_EN_WKUPEN_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
WKUP0_EN_WKUPEN_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
WKUP0_EN_WKUPEN_PROXY							
R/W							
0h							

Table 14-5937. WKUP_CTRL_MMR_CFG0_WKUP0_EN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WKUP0_EN_WKUPEN_PROXY	R/W	0h	Enables Wakeup from on-chip sources. In addition to values listed, any OR combination of the values is also valid. Field values (others are reserved): 32'h00000001 - WKUP_I2C0 32'h00000002 - WKUP_USART0 32'h00000004 - MCU_GPIO0 32'h00000008 - DEBUG undefined - undefined 32'h00000020 - WKUP_TIMER0 32'h00000040 - WKUP_TIMER1 32'h00000080 - WKUP_RTC 32'h00000100 - MAIN_RESET_REQz 32'h00000200 - USB0_IN_BAND undefined - undefined 32'h00010000 - MAIN_IO_DAISY_CHAIN 32'h00020000 - MCU_IO_DAISY_CHAIN 32'h00040000 - CANUART_IO_DAISY_CHAIN Reset Source: mod_g_rst_n

14.2.1.1.3.2.228 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register

14.2.1.1.3.2.228.1 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register (Offset = 1A280h) [reset = 100Eh]

Controls the power clock gating feature of modules and busses

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Table 14-5938. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A280h

Figure 14-2956. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Name Register

31	30	29	28	27	26	25	24
CLKGATE_CTRL0_MAIN_SMS_NOGATE_PROXY	RESERVED	CLKGATE_CTRL0_MAIN_SA3SS_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_R5SS1_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_R5SS0_NOGATE_PROXY	RESERVED	CLKGATE_CTRL0_MAIN_PDMA7_NOGATE_PROXY
R/W	NONE	R/W	R/W	R/W	R/W	NONE	R/W
0h	0h	0h	0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
CLKGATE_CTRL0_MAIN_PDMA6_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_PDMA5_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_PDMA4_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_PDMA3_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_PDMA2_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_PDMA1_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_PDMA0_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_DMSS_NOGATE_PROXY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
RESERVED	CLKGATE_CTRL0_MAIN_AUDIO_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_IPCSS_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_MEM_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_MISC_PERI_CBA_NOGATE_PROXY	RESERVED		
NONE	R/W	R/W	R/W	R/W	NONE		
0h	0h	0h	1h	0h	0h		

7	6	5	4	3	2	1	0
RESERVED		CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_DATA_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_CENTRAL_CBA_NOGATE_PROXY	CLKGATE_CTRL0_WKUP_DM_PWR_NOGATE_PROXY	CLKGATE_CTRL0_WKUP_DM_CBA_NOGATE_PROXY	CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE_PROXY
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	1h	1h	1h	0h

Table 14-5939. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLKGATE_CTRL0_MAIN_SMS_NOGATE_PROXY	R/W	0h	MAIN domain SMS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
30	RESERVED	NONE	0h	Reserved
29	CLKGATE_CTRL0_MAIN_SA3SS_NOGATE_PROXY	R/W	0h	MAIN domain SA3SS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

Table 14-5939. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	CLKGATE_CTRL0_MAIN_DBG_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Debug CBASS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
27	CLKGATE_CTRL0_MAIN_R5SS1_NOGATE_PROXY	R/W	0h	MAIN domain R5SS1 auto clock gate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
26	CLKGATE_CTRL0_MAIN_R5SS0_NOGATE_PROXY	R/W	0h	MAIN domain R5SS0 auto clock gate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
25	RESERVED	NONE	0h	Reserved
24	CLKGATE_CTRL0_MAIN_PDMA7_NOGATE_PROXY	R/W	0h	MAIN domain PDMA7 (ASRC11) auto clock gate on idle disable. Field values (others are reserved): 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
23	CLKGATE_CTRL0_MAIN_PDMA6_NOGATE_PROXY	R/W	0h	MAIN domain PDMA6 (ASRC0) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled 1'b0 - Auto clock gating enabled Reset Source: mod_por_rst_n
22	CLKGATE_CTRL0_MAIN_PDMA5_NOGATE_PROXY	R/W	0h	MAIN domain PDMA5 (ADC) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
21	CLKGATE_CTRL0_MAIN_PDMA4_NOGATE_PROXY	R/W	0h	MAIN domain PDMA4 (SPI/MCAN 1) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
20	CLKGATE_CTRL0_MAIN_PDMA3_NOGATE_PROXY	R/W	0h	MAIN domain PDMA3 (McASP1) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
19	CLKGATE_CTRL0_MAIN_PDMA2_NOGATE_PROXY	R/W	0h	MAIN domain PDMA2 (McASP0) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
18	CLKGATE_CTRL0_MAIN_PDMA1_NOGATE_PROXY	R/W	0h	MAIN domain PDMA1 (UART) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
17	CLKGATE_CTRL0_MAIN_PDMA0_NOGATE_PROXY	R/W	0h	MAIN domain PDMA0 (SPI/MCAN 0) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

Table 14-5939. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CLKGATE_CTRL0_MAIN_DMSS_NOGATE_PROXY	R/W	0h	MAIN domain DMSS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
15	RESERVED	NONE	0h	Reserved
14	CLKGATE_CTRL0_MAIN_AUDIO_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Infrastructure bus (AUDIO) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
13	CLKGATE_CTRL0_MAIN_IPCSS_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Infrastructure CBASS auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
12	CLKGATE_CTRL0_MAIN_MEM_CBA_NOGATE_PROXY	R/W	1h	MAIN domain infrastructure bus (MEM) auto cloclk gate on idle disable Reset Source: mod_por_rst_n
11	CLKGATE_CTRL0_MAIN_MISC_PERI_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Infrastructure bus (Misc Peripheral) auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
10:6	RESERVED	NONE	0h	Reserved
5	CLKGATE_CTRL0_MAIN_FW_CBA_NOGATE_PROXY	R/W	0h	MAIN domain data bus auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
4	CLKGATE_CTRL0_MAIN_DATA_CBA_NOGATE_PROXY	R/W	0h	MAIN domain data bus auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
3	CLKGATE_CTRL0_MAIN_CENTRAL_CBA_NOGATE_PROXY	R/W	1h	WKUP domain Infrastructure ECC aggregator auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
2	CLKGATE_CTRL0_WKUP_DM_PWR_NOGATE_PROXY	R/W	1h	WKUP domain Device Manager auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
1	CLKGATE_CTRL0_WKUP_DM_CBA_NOGATE_PROXY	R/W	1h	WKUP domain device manager CBA auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

Table 14-5939. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLKGATE_CTRL0_MAIN_INFRA_CBA_NOGATE_PROXY	R/W	0h	MAIN domain Infrastructure bus auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

14.2.1.1.3.2.229 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Register

14.2.1.1.3.2.229.1 WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Register (Offset = 1A284h) [reset = 3F000000h]

Controls the power clock gating feature of modules and busses

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Table 14-5940. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A284h

Figure 14-2957. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED		CLKGATE_CTRL1_RAM5_NOGATE_PROXY	CLKGATE_CTRL1_RAM4_NOGATE_PROXY	CLKGATE_CTRL1_RAM3_NOGATE_PROXY	CLKGATE_CTRL1_RAM2_NOGATE_PROXY	CLKGATE_CTRL1_RAM1_NOGATE_PROXY	CLKGATE_CTRL1_RAM0_NOGATE_PROXY
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		1h	1h	1h	1h	1h	1h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			CLKGATE_CTRL1_C7X_1_NOGATE_PROXY	CLKGATE_CTRL1_C7X_0_NOGATE_PROXY	RESERVED		
NONE			R/W	R/W	NONE		
0h			0h	0h	0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-5941. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	CLKGATE_CTRL1_RAM5_NOGATE_PROXY	R/W	1h	MAIN SRAM bank 5 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
28	CLKGATE_CTRL1_RAM4_NOGATE_PROXY	R/W	1h	MAIN SRAM bank 4 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
27	CLKGATE_CTRL1_RAM3_NOGATE_PROXY	R/W	1h	MAIN SRAM bank 5 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n

Table 14-5941. WKUP_CTRL_MMR_CFG0_CLKGATE_CTRL1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	CLKGATE_CTRL1_RAM2_NOGATE_PROXY	R/W	1h	MAIN SRAM bank 2 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
25	CLKGATE_CTRL1_RAM1_NOGATE_PROXY	R/W	1h	MAIN SRAM bank 1 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
24	CLKGATE_CTRL1_RAM0_NOGATE_PROXY	R/W	1h	MAIN SRAM bank 0 auto clockgate on idle disable Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
23:13	RESERVED	NONE	0h	Reserved
12	CLKGATE_CTRL1_C7X_1_NOGATE_PROXY	R/W	0h	C7x_1 auto clock gate on idle disable. Field values (others are reserved): 1'b0 - Auto clock gating enabled 1'b1 - Auto clock gating disabled Reset Source: mod_por_rst_n
11	CLKGATE_CTRL1_C7X_0_NOGATE_PROXY	R/W	0h	C7x_0 auto clock gate on idle disable. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.1.3.2.230 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY Register

14.2.1.1.3.2.230.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY Register (Offset = 1A300h) [reset = 0h]

Controls the operation of IO wakeup on the CANUART pins.

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Table 14-5942. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A300h

Figure 14-2958. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_CTRL_MW_PROXY							
R/W							
0h							

23	22	21	20	19	18	17	16
CANUART_WAKE_CTRL_MW_PROXY							
R/W							
0h							

15	14	13	12	11	10	9	8
CANUART_WAKE_CTRL_MW_PROXY							
R/W							
0h							

7	6	5	4	3	2	1	0
CANUART_WAKE_CTRL_MW_PROXY							CANUART_WAKE_CTRL_MW_LOAD_EN_PROXY
R/W							R/W
0h							0h

Table 14-5943. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CANUART_WAKE_CTRL_MW_PROXY	R/W	0h	CANUART IO magic word. The lower 23 bits determine if the device enters CANUART IO isolation when mw_load_en is set. If the lower 23 bits match the ACTIVATE value (0x5AAAAA), then CANUART IO Isolation is entered, any other value will prevent entry. The upper 8 bits of this register are software defined and do not determine whether or not CANUART IO isolation is entered. Field values (others are reserved): 31'h005AAAAA - ACTIVATE 31'h00000000 - DEACTIVATE Reset Source: mcu_chip1_rst_n
0	CANUART_WAKE_CTRL_MW_LOAD_EN_PROXY	R/W	0h	Magic word load enable Setting this bit loads and locks the mw field for CANUART IO isolation. If the mw field matches ACTIVATE, CANUART IO Isolation is initiated. Field values (others are reserved): 1'b0 - UNLOCK 1'b1 - LOCK_AND_LOAD Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.231 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY Register

14.2.1.1.3.2.231.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY Register (Offset = 1A308h) [reset = 0h]

Provides the status of CANUART_WAKE control bits. These bits come from the daisy-chain wakeup logic and maintain their value across core powerdown if isolation is activated.

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Table 14-5944. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A308h

Figure 14-2959. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_STAT0_MW_STAT_PROXY							
R							
X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CANUART_WAKE_STAT0_MW_STAT_PROXY							
R							
X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CANUART_WAKE_STAT0_MW_STAT_PROXY							
R							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CANUART_WAKE_STAT0_MW_STAT_PROXY							CANUART_WAKE_STAT0_MW_LOAD_STAT_PROXY
R							R
X							X

Table 14-5945. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CANUART_WAKE_STAT0_MW_STAT_PROXY	R	X	CANUART magic word status Indicates the latched value of the mw field. Reset Source: mod_por_rst_n
0	CANUART_WAKE_STAT0_MW_LOAD_STAT_PROXY	R	X	Magic word load status. Indicates the latched value of the mw_load_en bit Reset Source: mod_por_rst_n

14.2.1.1.3.2.232 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY Register

14.2.1.1.3.2.232.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY Register (Offset = 1A30Ch) [reset = 0h]

Provides CANUART IO isolation status. These bits come from the daisy-chain wakeup logic and maintain their value across core powerdown if isolation is activated

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Table 14-5946. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A30Ch

Figure 14-2960. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CANUART_WAKE_STAT1_CANUART_IO_MODE_PROXY
NONE							R
0h							X

Table 14-5947. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_STAT1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CANUART_WAKE_STAT1_CANUART_IO_MODE_PROXY	R	X	Indicates if CANUART IO wakeup mode is enabled. Field values (others are reserved): 1'b0 - INACTIVE 1'b1 - ACTIVATED Reset Source: mod_por_rst_n

14.2.1.1.3.2.233 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY Register

14.2.1.1.3.2.233.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY Register (Offset = 1A310h) [reset = 0h]

CANUART IO Domain OFF Mode Magic Word Register

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Table 14-5948. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A310h

Figure 14-2961. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_OFF_MODE_MW_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
CANUART_WAKE_OFF_MODE_MW_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
CANUART_WAKE_OFF_MODE_MW_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
CANUART_WAKE_OFF_MODE_MW_PROXY							
R/W							
0h							

Table 14-5949. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CANUART_WAKE_OFF_MODE_MW_PROXY	R/W	0h	magic word Reset Source: mod_por_rst_n

14.2.1.1.3.2.234 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY Register

14.2.1.1.3.2.234.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY Register (Offset = 1A318h) [reset = 0h]

CANUART IO Domain OFF Mode Magic Word Register

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Table 14-5950. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A318h

Figure 14-2962. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
CANUART_WAKE_OFF_MODE_STAT_MW_PROXY							
R							
X							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CANUART_WAKE_OFF_MODE_STAT_MW_PROXY							
R							
X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CANUART_WAKE_OFF_MODE_STAT_MW_PROXY							
R							
X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CANUART_WAKE_OFF_MODE_STAT_MW_PROXY							
R							
X							

Table 14-5951. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_OFF_MODE_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CANUART_WAKE_OFF_MODE_STAT_MW_PROXY	R	X	returned magic word Reset Source: mod_por_rst_n

14.2.1.1.3.2.235 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_j Register

14.2.1.1.3.2.235.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_j Register (Offset = 1A320h) [reset = 0h]

CAN_UART IO Domain Resume Key Value Register

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Table 14-5952. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A320h + formula

Figure 14-2963. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_j Name Register

31	30	29	28	27	26	25	24
KEYVAL_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEYVAL_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEYVAL_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEYVAL_PROXY							
R/W							
0h							

Table 14-5953. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_PROXY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEYVAL_PROXY	R/W	0h	key value Reset Source: mod_por_rst_n

14.2.1.1.3.2.236 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_j Register

14.2.1.1.3.2.236.1 WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_j Register (Offset = 1A340h) [reset = 0h]

CAN_UART IO Domain Resume Key Value Register

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Table 14-5954. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A340h + formula

Figure 14-2964. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_j Name Register

31	30	29	28	27	26	25	24
KEYVAL_PROXY							
R							
X							
23	22	21	20	19	18	17	16
KEYVAL_PROXY							
R							
X							
15	14	13	12	11	10	9	8
KEYVAL_PROXY							
R							
X							
7	6	5	4	3	2	1	0
KEYVAL_PROXY							
R							
X							

Table 14-5955. WKUP_CTRL_MMR_CFG0_CANUART_WAKE_RESUME_KEY_STAT_PROXY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KEYVAL_PROXY	R	X	returned key value Reset Source: mod_por_rst_n

14.2.1.1.3.2.237 WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL_PROXY Register

14.2.1.1.3.2.237.1 WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL_PROXY Register (Offset = 1A360h) [reset = 0h]

Controls monitoring of wake events during IO retention entry/exit

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Table 14-5956. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A360h

Figure 14-2965. WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL_PROXY Name Register

31	30	29	28	27	26	25	24
WAKE_EVT_MON_CTRL_WAKE_TIMEOUT_DIS_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							WAKE_EVT_MON_CTRL_CLR_WAKE_EVT_PROXY
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							WAKE_EVT_MON_CTRL_EN_WAKE_EVT_MON_PROXY
NONE							R/W
0h							0h

Table 14-5957. WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WAKE_EVT_MON_CTRL_WAKE_TIMEOUT_DIS_PROXY	R/W	0h	Disable wakeup event timeout window. Field values (others are reserved): 1'b0 - An Internal POR is generated when a wakeup event is detected by the IORET entry/exit wakeup event monitor before the Immediate Wakeup Timeout window expiration 1'b1 - The immediate wakeup timeout window is disabled. Reset Source: mod_por_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	WAKE_EVT_MON_CTRL_CLR_WAKE_EVT_PROXY	R/W	0h	Clear wakeup events. Write 1 to clear all wakeup events. Read always returns 0. Field values (others are reserved): 1'b0 - Read value. Writing 0 has no effect 1'b1 - Clear all wake events Reset Source: mod_por_rst_n
15:1	RESERVED	NONE	0h	Reserved

Table 14-5957. WKUP_CTRL_MMR_CFG0_WAKE_EVT_MON_CTRL_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAKE_EVT_MON_CTRL_EN_WAKE_EVT_MON_PROXY	R/W	0h	Enable wakeup event monitoring. Field values (others are reserved): 1'b0 - All IORET entry/exit wakeup event monitoring is disabled 1'b1 - Enable wakeup event monitoring during IORET entry/exit. The pins to be monitored are determined by the corresponding PADCONFIG register settings Reset Source: mod_por_rst_n

14.2.1.1.3.2.238 WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR_PROXY Register

14.2.1.1.3.2.238.1 WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR_PROXY Register (Offset = 1A364h) [reset = 20h]

Determines how long the IPOR generated by IORET entry/exit wakeup monitoring will be asserted

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Table 14-5958. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A364h

Figure 14-2966. WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTRN_POR_DUR_IPOR_LEN_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">20h</td></tr>
</table>

Table 14-5959. WKUP_CTRL_MMR_CFG0_INTRN_POR_DUR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTRN_POR_DUR_IPOR_LEN_PROXY	R/W	20h	Specifies the number of HFOSC0 clock cycles to assert IPORz (low) when the wake monitoring logic detects a wakeup event. This value must exceed the minimum PORz period for the device with stable power supplies and reference clocks (1200 ns) Reset Source: mod_por_rst_n

14.2.1.1.3.2.239 WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT_PROXY Register

14.2.1.1.3.2.239.1 WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT_PROXY Register (Offset = 1A368h) [reset = EAh]

Determines the length of the timing window during which a monitored wakeup event will generate an IPOR. This ensures wakeup events occurring soon after PMIC_EN deactivation but before IORET state entry are recognized. After this window has expired, the external PMIC is expected to generate a POR based on PMIC_EN activation. The ImmediateWakeup Timeout window is disabled (no IPOR generated) if the wake_timeout_dis in WAKE_EVT_MON_CTRL is 1.

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Table 14-5960. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A368h

Figure 14-2967. WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IMMED_WAKE_TIMEOUT_TIMEOUT_LENGTH_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">EAh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IMMED_WAKE_TIMEOUT_TIMEOUT_LENGTH_PROXY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">EAh</td></tr>
</table>

Table 14-5961. WKUP_CTRL_MMR_CFG0_IMMED_WAKE_TIMEOUT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	IMMED_WAKE_TIMEOUT_TIMEOUT_LENGTH_PROXY	R/W	EAh	Specifies the number of HFOSC0 clock cycles during which wake monitoring logic will issue an internal POR. This timeout value must exceed the PMIC glitch filtering window for its PMIC_EN input. (Default value is 9 s at 26 MHz HFOSC0) Reset Source: mod_por_rst_n

14.2.1.1.3.2.240 WKUP_CTRL_MMR_CFG0_RET_RAM_STAT_PROXY Register

14.2.1.1.3.2.240.1 WKUP_CTRL_MMR_CFG0_RET_RAM_STAT_PROXY Register (Offset = 1A380h) [reset = 0h]

Shows the Retention RAM Status

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Table 14-5962. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A380h

Figure 14-2968. WKUP_CTRL_MMR_CFG0_RET_RAM_STAT_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h						X	
15	14	13	12	11	10	9	8
	RESERVED						RET_RAM_STAT_ISOLATED_PROXY
	NONE						R
X	0h						X
7	6	5	4	3	2	1	0
RESERVED							RET_RAM_STAT_BUSY_PROXY
NONE							R
0h							X

Table 14-5963. WKUP_CTRL_MMR_CFG0_RET_RAM_STAT_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
14:9	RESERVED	NONE	0h	Reserved
8	RET_RAM_STAT_ISOLATED_PROXY	R	X	Indicates Retention RAM isolation state (when busy=0) Field values (others are reserved): 1'b0 - RAM is not isolated 1'b1 - RAM is isolated Reset Source: mod_por_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	RET_RAM_STAT_BUSY_PROXY	R	X	Indicates that Retention RAM state is transitioning. The RAM must not be accessed or the isolation powerdown sequence continued while busy=1 Field values (others are reserved): 1'b0 - RAM is in isolation state indicated by the isolated bit 1'b1 - RAM isolation state is transitioning - do not access Reset Source: mod_por_rst_n

14.2.1.1.3.2.241 WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Register

14.2.1.1.3.2.241.1 WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Register (Offset = 1A400h) [reset = 0h]

Allows inspection of WFI Status of all CPU Cores

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Table 14-5964. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A400h

Figure 14-2969. WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							WFI_STATUS_MAIN_R5FSS1_CORE1_WFI_PROXY
NONE							R
0h							X
7	6	5	4	3	2	1	0
WFI_STATUS_MAIN_R5FSS1_CORE0_WFI_PROXY	WFI_STATUS_MAIN_R5FSS0_CORE1_WFI_PROXY	WFI_STATUS_MAIN_R5FSS0_CORE0_WFI_PROXY	RESERVED	WFI_STATUS_SMS_CPU1_WFI_PROXY	WFI_STATUS_SMS_CPU0_WFI_PROXY	RESERVED	WFI_STATUS_WKUP_R5F_WFI_PROXY
R	R	R	NONE	R	R	NONE	R
X	X	X	0h	X	X	0h	X

Table 14-5965. WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	WFI_STATUS_MAIN_R5FSS1_CORE1_WFI_PROXY	R	X	WFI status of MAIN Cortex R5F_1 Core 1 (only valid when core is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
7	WFI_STATUS_MAIN_R5FSS1_CORE0_WFI_PROXY	R	X	WFI status of MAIN Cortex R5F_1 Core 0 (only valid when core is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n

Table 14-5965. WKUP_CTRL_MMR_CFG0_WFI_STATUS_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	WFI_STATUS_MAIN_R5FSS0_CORE1_WFI_PROXY	R	X	WFI status of MAIN Cortex R5F_0 Core 0 (only valid when core is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
5	WFI_STATUS_MAIN_R5FSS0_CORE0_WFI_PROXY	R	X	WFI status of MAIN Cortex R5F_0 Core 0 (only valid when core is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
4	RESERVED	NONE	0h	Reserved
3	WFI_STATUS_SMS_CPU1_WFI_PROXY	R	X	WFI status of SMS Cortex M4F1 (only valid when CPU is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
2	WFI_STATUS_SMS_CPU0_WFI_PROXY	R	X	WFI status of SMS Cortex M4F0 (only valid when CPU is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n
1	RESERVED	NONE	0h	Reserved
0	WFI_STATUS_WKUP_R5F_WFI_PROXY	R	X	WFI status of Device Manager Cortex R5F (only valid when CPU is out of reset) Field values (others are reserved): 1'b0 - UNKNOWN 1'b1 - WFI_ACTIVE Reset Source: mod_por_rst_n

14.2.1.1.3.2.242 WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY Register

14.2.1.1.3.2.242.1 WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY Register (Offset = 1A420h) [reset = Fh]

Reset Control and Main Power Domain Control

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Table 14-5966. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A420h

Figure 14-2970. WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_MAIN_POR_PDOFF_PROXY			
NONE				R/W			
0h				Fh			

Table 14-5967. WKUP_CTRL_MMR_CFG0_DS_MAIN_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_MAIN_POR_PDOFF_PROXY	R/W	Fh	Signal Puts main SMS, DebugSS and MainIP Power Domains into Power Off state, and asserts Main Power On Reset. Field values (others are reserved): 4'b0110 - Off 4'b1111 - On Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.243 WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY Register

14.2.1.1.3.2.243.1 WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY Register (Offset = 1A440h) [reset = Fh]

Reset Isolation for the Device Manager

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Table 14-5968. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A440h

Figure 14-2971. WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">DS_DM_RESET_MASK_PROXY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">Fh</td></tr>
</table>

Table 14-5969. WKUP_CTRL_MMR_CFG0_DS_DM_RESET_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_DM_RESET_MASK_PROXY	R/W	Fh	Signal used to mask main domain resets from Device Manager / Wakeup and MCU Ips Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.244 WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY Register

14.2.1.1.3.2.244.1 WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY Register (Offset = 1A460h) [reset = Fh]

Reset Isolation for the USB0 Subsystem

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Table 14-5970. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A460h

Figure 14-2972. WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DS_USB0_RESET_MASK_PROXY			
NONE				R/W			
0h				Fh			

Table 14-5971. WKUP_CTRL_MMR_CFG0_DS_USB0_RESET_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DS_USB0_RESET_MASK_PROXY	R/W	Fh	Signal used to block reset to the USBSS0 Field values (others are reserved): 4'b0110 - Masked 4'b1111 - UnMasked Reset Source: mcu_chip1_rst_n

14.2.1.1.3.2.245 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY Register

14.2.1.1.3.2.245.1 WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY Register (Offset = 1A4A0h) [reset = 0h]

Initiate Clockstop Request Sequence on WKUP Peripherals Activated in DM_CLKSTOP_EN

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Table 14-5972. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A4A0h

Figure 14-2973. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DM_GRP_CLKSTOP_REQ_REQ_PROXY
NONE							R/W
0h							0h

Table 14-5973. WKUP_CTRL_MMR_CFG0_DM_GRP_CLKSTOP_REQ_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DM_GRP_CLKSTOP_REQ_REQ_PROXY	R/W	0h	Controls Assertion of Clockstop Request to IPs participating in Clockstop Req Group Field values (others are reserved): 1'b0 - DEASSERT_REQ 1'b1 - ASSERT_REQ Reset Source: mod_por_rst_n

14.2.1.1.3.2.246 WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY Register

14.2.1.1.3.2.246.1 WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY Register (Offset = 1A500h) [reset = 0h]

Device Type as Decoded by SMS

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Table 14-5974. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 A500h

Figure 14-2974. WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEVICE_TYPE_SMS_DEV_TYPE_PROXY							
R							
X				X			

Table 14-5975. WKUP_CTRL_MMR_CFG0_DEVICE_TYPE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DEVICE_TYPE_SMS_DEV_TYPE_PROXY	R	X	Type of device reported by SMS. Values not listed should be interpreted as BAD. Field values (others are reserved): 4'b0101 - DT_TEST 4'b1001 - DT_EMU 4'b1010 - DT_HS 4'b0011 - DT_GP Reset Source: mod_por_rst_n

14.2.1.1.3.2.247 WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register

14.2.1.1.3.2.247.1 WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register (Offset = 1B008h) [reset = 0h]

- KICK0 component

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Table 14-5976. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B008h

Figure 14-2975. WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK0_PROXY							
R/W							
0h							

Table 14-5977. WKUP_CTRL_MMR_CFG0_LOCK6_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.248 WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register

14.2.1.1.3.2.248.1 WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register (Offset = 1B00Ch) [reset = 0h]

- KICK1 component

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Table 14-5978. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B00Ch

Figure 14-2976. WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK6_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK6_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK6_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK6_KICK1_PROXY							
R/W							
0h							

Table 14-5979. WKUP_CTRL_MMR_CFG0_LOCK6_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK6_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.249 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register

14.2.1.1.3.2.249.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register (Offset = 1B100h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5980. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B100h

Figure 14-2977. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P6_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-5981. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R0	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.250 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register

14.2.1.1.3.2.250.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register (Offset = 1B104h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5982. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B104h

Figure 14-2978. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R1							
R/W							
0h							

Table 14-5983. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R1	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.251 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register

14.2.1.1.3.2.251.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register (Offset = 1B108h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5984. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B108h

Figure 14-2979. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R2							
R/W							
0h							

Table 14-5985. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R2	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.252 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register

14.2.1.1.3.2.252.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register (Offset = 1B10Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-5986. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B10Ch

Figure 14-2980. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R3							
R/W							
0h							

Table 14-5987. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R3	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.253 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register

14.2.1.1.3.2.253.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register (Offset = 1B110h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5988. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B110h

Figure 14-2981. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R4							
R/W							
0h							

Table 14-5989. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R4	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.254 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register

14.2.1.1.3.2.254.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register (Offset = 1B114h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5990. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B114h

Figure 14-2982. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R5							
R/W							
0h							

Table 14-5991. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R5	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.255 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register

14.2.1.1.3.2.255.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register (Offset = 1B118h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5992. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B118h

Figure 14-2983. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R6							
R/W							
0h							

Table 14-5993. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R6	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.256 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register

14.2.1.1.3.2.256.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register (Offset = 1B11Ch) [reset = 0h]

Claim bits for Partition 6

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Table 14-5994. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B11Ch

Figure 14-2984. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R7							
R/W							
0h							

Table 14-5995. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R7	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.257 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register

14.2.1.1.3.2.257.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register (Offset = 1B120h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5996. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B120h

Figure 14-2985. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R8							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R8							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R8							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R8							
R/W							
0h							

Table 14-5997. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R8	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.258 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9 Register

14.2.1.1.3.2.258.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9 Register (Offset = 1B124h) [reset = 0h]

Claim bits for Partition 6

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Table 14-5998. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B124h

Figure 14-2986. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R9							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R9							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R9							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R9							
R/W							
0h							

Table 14-5999. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R9	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.259 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10 Register

14.2.1.1.3.2.259.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10 Register (Offset = 1B128h) [reset = 0h]

Claim bits for Partition 6

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Table 14-6000. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 B128h

Figure 14-2987. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P6_R10							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P6_R10							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P6_R10							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P6_R10							
R/W							
0h							

Table 14-6001. WKUP_CTRL_MMR_CFG0_CLAIMREG_P6_R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P6_R10	R/W	0h	Claim bits for Partition 6 Reset Source: mod_g_rst_n

14.2.1.1.3.2.260 WKUP_CTRL_MMR_CFG0_LOCK7_KICK0 Register

14.2.1.1.3.2.260.1 WKUP_CTRL_MMR_CFG0_LOCK7_KICK0 Register (Offset = 1D008h) [reset = 0h]

- KICK0 component

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Table 14-6002. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 D008h

Figure 14-2988. WKUP_CTRL_MMR_CFG0_LOCK7_KICK0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK7_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK7_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK7_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK7_KICK0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6003. WKUP_CTRL_MMR_CFG0_LOCK7_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK7_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.261 WKUP_CTRL_MMR_CFG0_LOCK7_KICK1 Register

14.2.1.1.3.2.261.1 WKUP_CTRL_MMR_CFG0_LOCK7_KICK1 Register (Offset = 1D00Ch) [reset = 0h]

- KICK1 component

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Table 14-6004. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 D00Ch

Figure 14-2989. WKUP_CTRL_MMR_CFG0_LOCK7_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK7_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK7_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK7_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK7_KICK1							
R/W							
0h							

Table 14-6005. WKUP_CTRL_MMR_CFG0_LOCK7_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK7_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.262 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY Register

14.2.1.1.3.2.262.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY Register (Offset = 1D100h) [reset = 0h]

Claim bits for Partition 7

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Table 14-6006. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 D100h

Figure 14-2990. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6007. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R0_READONLY	R	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.263 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY Register

14.2.1.1.3.2.263.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY Register (Offset = 1D104h) [reset = 0h]

Claim bits for Partition 7

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Table 14-6008. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 D104h

Figure 14-2991. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P7_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P7_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P7_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P7_R1_READONLY							
R							
0h							

Table 14-6009. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R1_READONLY	R	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.264 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY Register

14.2.1.1.3.2.264.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY Register (Offset = 1D108h) [reset = 0h]

Claim bits for Partition 7

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Table 14-6010. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 D108h

Figure 14-2992. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P7_R2_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P7_R2_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P7_R2_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P7_R2_READONLY							
R							
0h							

Table 14-6011. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R2_READONLY	R	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.265 WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY Register

14.2.1.1.3.2.265.1 WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY Register (Offset = 1F008h) [reset = 0h]

- KICK0 component

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Table 14-6012. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 F008h

Figure 14-2993. WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK7_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK7_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK7_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK7_KICK0_PROXY							
R/W							
0h							

Table 14-6013. WKUP_CTRL_MMR_CFG0_LOCK7_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK7_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.266 WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY Register

14.2.1.1.3.2.266.1 WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY Register (Offset = 1F00Ch) [reset = 0h]

- KICK1 component

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Table 14-6014. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 F00Ch

Figure 14-2994. WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK7_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK7_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK7_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK7_KICK1_PROXY							
R/W							
0h							

Table 14-6015. WKUP_CTRL_MMR_CFG0_LOCK7_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK7_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.1.3.2.267 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0 Register

14.2.1.1.3.2.267.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0 Register (Offset = 1F100h) [reset = 0h]

Claim bits for Partition 7

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Table 14-6016. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 F100h

Figure 14-2995. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6017. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R0	R/W	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.268 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1 Register

14.2.1.1.3.2.268.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1 Register (Offset = 1F104h) [reset = 0h]

Claim bits for Partition 7

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Table 14-6018. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 F104h

Figure 14-2996. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P7_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P7_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P7_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P7_R1							
R/W							
0h							

Table 14-6019. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R1	R/W	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.1.3.2.269 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2 Register

14.2.1.1.3.2.269.1 WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2 Register (Offset = 1F108h) [reset = 0h]

Claim bits for Partition 7

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Table 14-6020. Instance Table

Instance Name	Physical Address
WKUP_CTRL_MMR0	4301 F108h

Figure 14-2997. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P7_R2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6021. WKUP_CTRL_MMR_CFG0_CLAIMREG_P7_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P7_R2	R/W	0h	Claim bits for Partition 7 Reset Source: mod_g_rst_n

14.2.1.2 Pad Configuration Registers

14.2.1.2.1 Pad Configuration Register Functional Description

The pad configuration registers are used to configure most of the device pads. Each pad configuration registers is associated only with one pad and has bits as described in the below table.

Table 14-6022. Description Of The Pad Configuration Register Bits

Bit	Field	Type	Reset	Description
31	LOCK	R/W	(1)	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes
30	WKUP_EVT	R/W	(1)	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin
29	WKUP_EN	R/W	(1)	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled

Table 14-6022. Description Of The Pad Configuration Register Bits (continued)

Bit	Field	Type	Reset	Description
28	DS_PULLTYPE_SEL	R/W	(1)	Deep Sleep pull-up/down selection 0 - Offmode pulldown selected 1 - Offmode pullup selected
27	DS_PULLUD_EN	R/W	(1)	Deep Sleep pull-up/down enable (active low) 0 - Pullup / pulldown is enabled 1 - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	(1)	Deep Sleep output value 0 - Output value is 0 1 - Output value is 1
25	DSOUT_DIS	R/W	(1)	Deep Sleep output disable 0 - Output enabled 1 - Output disabled
24	DS_EN	R/W	(1)	Deep Sleep override control 0 - IO keeps its previous state when Deep Sleep mode is active 1 - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	(1)	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed
22	ISO_OVR	R/W	(1)	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden
21	TX_DIS (3)	R/W	(1)	Driver Disable 0 - Driver is enabled 1 - Driver is disabled
20 - 19	DRV_STR (4)	R/W	(1)	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) 0 - Default 1 - Reserved 2 - Reserved 3 - Reserved
18	RXACTIVE (5)	R/W	(1)	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled
17	PULLTYPESEL (2)	R/W	(1)	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected
16	PULLUDEN(2)	R/W	(1)	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	(1)	Enable pad Deep Sleep controls by overriding DMSC gating 0 - Deep Sleep pad controls are gated by the DMSC 1 - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	(1)	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled
13 - 11	DEBOUNCE_SEL	R/W	(1)	Selects the debouce period for the pad.
10 - 9	RESERVED	R/W	0	Reserved

Table 14-6022. Description Of The Pad Configuration Register Bits (continued)

Bit	Field	Type	Reset	Description
8	WK_LVL_POL	R/W	(1)	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup
7	WK_LVL_EN	R/W	(1)	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed)
6 - 4	RESERVED	R/W	0	Reserved
3 - 0	MUXMODE	R/W	(1)	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15

(1) See *Pad Configuration Registers* for reset values for Pad Configuration registers.
(2) These bits do not apply to "I2C OD FS" buffer types as these IOs do not have internal pull registers.
(3) To prevent unwanted glitches, software should disable the output driver by setting the TX_DIS bit before writing a new MUXMODE value. Once the new MUXMODE value is written, the TX_DIS bit can be reset in order to re-enable the pin driver.
(4) Use of settings other than the reset value could invalidate datasheet timings.
(5) The RXACTIVE bit must never be set without a valid logic state being sourced to the pin associated with the respective PADCONFIG register. This is very important since a floating input may damage the device.

14.2.1.2.1.1 PADCFG_CTRL

PADCFG_CTRL

14.2.1.2.1.1.1 PADCFG_CTRL Summaries

PADCFG_CTRL Summaries

Table 14-6023. MCU_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=0408 0000h, Length=32768

Offset	Length	Register Name	MCU_PADCFG_CTRL0 Physical Address
0h	32	MCU_PADCFG_CTRL_MMRCFG0_PID	0408 0000h
4h	32	MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0	0408 0004h
8h	32	MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1	0408 0008h
1008h	32	MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0	0408 1008h
100Ch	32	MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1	0408 100Ch
1010h	32	MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS	0408 1010h
1014h	32	MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR	0408 1014h
1018h	32	MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE	0408 1018h
101Ch	32	MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR	0408 101Ch
1020h	32	MCU_PADCFG_CTRL_MMRCFG0_EOI	0408 1020h
1024h	32	MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS	0408 1024h
1028h	32	MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS	0408 1028h
102Ch	32	MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS	0408 102Ch
1030h	32	MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR	0408 1030h
1100h	32	MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY	0408 1100h
2000h	32	MCU_PADCFG_CTRL_MMRCFG0_PID_PROXY	0408 2000h
2004h	32	MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY	0408 2004h
2008h	32	MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY	0408 2008h
3008h	32	MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY	0408 3008h
300Ch	32	MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY	0408 300Ch
3010h	32	MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY	0408 3010h
3014h	32	MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	0408 3014h
3018h	32	MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY	0408 3018h
301Ch	32	MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY	0408 301Ch
3020h	32	MCU_PADCFG_CTRL_MMRCFG0_EOI_PROXY	0408 3020h
3024h	32	MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY	0408 3024h
3028h	32	MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY	0408 3028h
302Ch	32	MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY	0408 302Ch
3030h	32	MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY	0408 3030h
3100h	32	MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0	0408 3100h

Table 14-6023. MCU_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=0408 0000h, Length=32768 (continued)

Offset	Length	Register Name	MCU_PADCFG_CTRL0 Physical Address
4000h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0	0408 4000h
4004h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1	0408 4004h
4008h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2	0408 4008h
400Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3	0408 400Ch
4010h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4	0408 4010h
4014h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5	0408 4014h
4018h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6	0408 4018h
401Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7	0408 401Ch
4020h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8	0408 4020h
4024h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9	0408 4024h
4028h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10	0408 4028h
402Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11	0408 402Ch
4030h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12	0408 4030h
4034h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13	0408 4034h
4038h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14	0408 4038h
403Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15	0408 403Ch
4040h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16	0408 4040h
404Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19	0408 404Ch
4050h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20	0408 4050h
4054h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21	0408 4054h
4058h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22	0408 4058h
405Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23	0408 405Ch
4060h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24	0408 4060h
4064h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25	0408 4064h
4068h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26	0408 4068h
406Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27	0408 406Ch
4070h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28	0408 4070h
4074h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29	0408 4074h
4078h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30	0408 4078h
407Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31	0408 407Ch
4080h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32	0408 4080h
4084h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33	0408 4084h
5008h	32	MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0	0408 5008h
500Ch	32	MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1	0408 500Ch
5100h	32	MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY	0408 5100h
5104h	32	MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY	0408 5104h
6000h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY	0408 6000h
6004h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY	0408 6004h
6008h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY	0408 6008h
600Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY	0408 600Ch
6010h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY	0408 6010h

Table 14-6023. MCU_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=0408 0000h, Length=32768 (continued)

Offset	Length	Register Name	MCU_PADCFG_CTRL0 Physical Address
6014h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY	0408 6014h
6018h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY	0408 6018h
601Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY	0408 601Ch
6020h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY	0408 6020h
6024h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY	0408 6024h
6028h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY	0408 6028h
602Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY	0408 602Ch
6030h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY	0408 6030h
6034h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY	0408 6034h
6038h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY	0408 6038h
603Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY	0408 603Ch
6040h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY	0408 6040h
604Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY	0408 604Ch
6050h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY	0408 6050h
6054h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY	0408 6054h
6058h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY	0408 6058h
605Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY	0408 605Ch
6060h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY	0408 6060h
6064h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY	0408 6064h
6068h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY	0408 6068h
606Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY	0408 606Ch
6070h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY	0408 6070h
6074h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY	0408 6074h
6078h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY	0408 6078h
607Ch	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY	0408 607Ch
6080h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32_PROXY	0408 6080h
6084h	32	MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY	0408 6084h

Table 14-6023. MCU_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=0408 0000h, Length=32768 (continued)

Offset	Length	Register Name	MCU_PADCFG_CTRL0 Physical Address
7008h	32	MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY	0408 7008h
700Ch	32	MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY	0408 700Ch
7100h	32	MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0	0408 7100h
7104h	32	MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1	0408 7104h

14.2.1.2.1.1.2 PADCFG_CTRL Registers

PADCFG_CTRL Registers

14.2.1.2.1.1.2.1 MCU_PADCFG_CTRL_MMRCFG0_PID Register

14.2.1.2.1.1.2.1.1 MCU_PADCFG_CTRL_MMRCFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-6024. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 0000h

Figure 14-2998. MCU_PADCFG_CTRL_MMRCFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-6025. MCU_PADCFG_CTRL_MMRCFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.2 MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0 Register

14.2.1.2.1.1.2.2.1 MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0 Register (Offset = 4h) [reset = 10000000h]

Indicates the version of the CFG used to create the MMR Module

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Table 14-6026. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 0004h

Figure 14-2999. MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MMR_CFG0_CFG_REV</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MMR_CFG0_CFG_REV</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MMR_CFG0_SPEC_REV</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MMR_CFG0_SPEC_REV</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6027. MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV	R	0h	Minor spec-only revision. Deprecated. Was intended to reflect non-RTL updates in the printed Spec but this can't be reflected in the MMR read value without an RTL change when post RTL descriptions are pushed into the VPS. Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.3 MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1 Register

14.2.1.2.1.1.2.3.1 MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1 Register (Offset = 8h) [reset = 80000003h]

Indicates the MMR configuration

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Table 14-6028. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 0008h

Figure 14-3000. MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MMR_CFG1_PARTITIONS							
R							
3h							

Table 14-6029. MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	3h	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.4 MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0 Register

14.2.1.2.1.1.2.4.1 MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-6030. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1008h

Figure 14-3001. MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-6031. MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.5 MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1 Register

14.2.1.2.1.1.2.5.1 MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-6032. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 100Ch

Figure 14-3002. MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-6033. MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.6 MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS Register

14.2.1.2.1.1.2.6.1 MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-6034. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1010h

Figure 14-3003. MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6035. MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.7 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register

14.2.1.2.1.1.2.7.1 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-6036. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1014h

Figure 14-3004. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6037. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.8 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE Register

14.2.1.2.1.1.2.8.1 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-6038. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1018h

Figure 14-3005. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6039. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.9 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register

14.2.1.2.1.1.2.9.1 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-6040. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 101Ch

Figure 14-3006. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6041. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.10 MCU_PADCFG_CTRL_MMRCFG0_EOI Register

14.2.1.2.1.1.2.10.1 MCU_PADCFG_CTRL_MMRCFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-6042. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1020h

Figure 14-3007. MCU_PADCFG_CTRL_MMRCFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-6043. MCU_PADCFG_CTRL_MMRCFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.11 MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS Register

14.2.1.2.1.1.2.11.1 MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-6044. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1024h

Figure 14-3008. MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-6045. MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.12 MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register

14.2.1.2.1.1.2.12.1 MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-6046. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1028h

Figure 14-3009. MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-6047. MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.13 MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register

14.2.1.2.1.1.2.13.1 MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-6048. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 102Ch

Figure 14-3010. MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID</td><td colspan="4">FAULT_ROUTEID</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6049. MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.14 MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR Register

14.2.1.2.1.1.2.14.1 MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-6050. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1030h

Figure 14-3011. MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-6051. MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.15 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register

14.2.1.2.1.1.2.15.1 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-6052. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 1100h

Figure 14-3012. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-6053. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.16 MCU_PADCFG_CTRL_MMRCFG0_PID_PROXY Register

14.2.1.2.1.1.2.16.1 MCU_PADCFG_CTRL_MMRCFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800215h]

PID register

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Table 14-6054. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 2000h

Figure 14-3013. MCU_PADCFG_CTRL_MMRCFG0_PID_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16_PROXY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC_PROXY</td><td colspan="3">PID_MAJOR_PROXY</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM_PROXY</td><td colspan="6">PID_MINOR_PROXY</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-6055. MCU_PADCFG_CTRL_MMRCFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	15h	Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.17 MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY Register

14.2.1.2.1.1.2.17.1 MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY Register (Offset = 2004h) [reset = 10000000h]

Indicates the version of the CFG used to create the MMR Module

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Table 14-6056. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 2004h

Figure 14-3014. MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MMR_CFG0_SPEC_REV_PROXY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG0_SPEC_REV_PROXY							
R							
0h							

Table 14-6057. MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV_PROXY	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV_PROXY	R	0h	Minor spec-only revision. Deprecated. Was intended to reflect non-RTL updates in the printed Spec but this can't be reflected in the MMR read value without an RTL change when post RTL descriptions are pushed into the VPS. Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.18 MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY Register

14.2.1.2.1.1.2.18.1 MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 80000003h]

Indicates the MMR configuration

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Table 14-6058. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 2008h

Figure 14-3015. MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS_PROXY							
R							
3h							

Table 14-6059. MCU_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	3h	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.19 MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register

14.2.1.2.1.1.2.19.1 MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-6060. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3008h

Figure 14-3016. MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-6061. MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.20 MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register

14.2.1.2.1.1.2.20.1 MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-6062. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 300Ch

Figure 14-3017. MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-6063. MCU_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.21 MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register

14.2.1.2.1.1.2.21.1 MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-6064. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3010h

Figure 14-3018. MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6065. MCU_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.22 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

14.2.1.2.1.1.2.22.1 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-6066. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3014h

Figure 14-3019. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6067. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.23 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register

14.2.1.2.1.1.2.23.1 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-6068. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3018h

Figure 14-3020. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6069. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.24 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register

14.2.1.2.1.1.2.24.1 MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-6070. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 301Ch

Figure 14-3021. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6071. MCU_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.25 MCU_PADCFG_CTRL_MMRCFG0_EOI_PROXY Register

14.2.1.2.1.1.2.25.1 MCU_PADCFG_CTRL_MMRCFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-6072. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3020h

Figure 14-3022. MCU_PADCFG_CTRL_MMRCFG0_EOI_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR_PROXY							
R/W							
0h							

Table 14-6073. MCU_PADCFG_CTRL_MMRCFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.26 MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register

14.2.1.2.1.1.2.26.1 MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-6074. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3024h

Figure 14-3023. MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-6075. MCU_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.27 MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register

14.2.1.2.1.1.2.27.1 MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-6076. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3028h

Figure 14-3024. MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-6077. MCU_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.28 MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register

14.2.1.2.1.1.2.28.1 MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-6078. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 302Ch

Figure 14-3025. MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-6079. MCU_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.29 MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register

14.2.1.2.1.1.2.29.1 MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-6080. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3030h

Figure 14-3026. MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-6081. MCU_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.30 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register

14.2.1.2.1.1.2.30.1 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-6082. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 3100h

Figure 14-3027. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-6083. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.31 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Register

14.2.1.2.1.1.2.31.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Register (Offset = 4000h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6084. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4000h

Figure 14-3028. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Name Register

31	30	29	28	27	26	25	24
PADCONFIG0_LOCK	PADCONFIG0_WKUP_EVT	PADCONFIG0_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG0_ISO_BYP	PADCONFIG0_ISO_OVR	PADCONFIG0_TX_DIS	PADCONFIG0_DRV_STR		PADCONFIG0_RXACTIVE	PADCONFIG0_PULLTYPESEL	PADCONFIG0_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG0_ST_EN	PADCONFIG0_DEBOUNCE_SEL			RESERVED		PADCONFIG0_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG0_WK_LVL_EN	RESERVED			PADCONFIG0_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6085. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG0_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG0_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG0_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG0_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG0_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG0_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6085. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG0_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG0_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG0_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG0_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG0_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG0_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG0_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG0_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG0_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.32 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Register

14.2.1.2.1.1.2.32.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Register (Offset = 4004h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6086. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4004h

Figure 14-3029. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Name Register

31	30	29	28	27	26	25	24
PADCONFIG1_LOCK	PADCONFIG1_WKUP_EVT	PADCONFIG1_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG1_ISO_BYP	PADCONFIG1_ISO_OVR	PADCONFIG1_TX_DIS	PADCONFIG1_DRV_STR		PADCONFIG1_RXACTIVE	PADCONFIG1_PULLTYPESEL	PADCONFIG1_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG1_ST_EN	PADCONFIG1_DEBOUNCE_SEL			RESERVED		PADCONFIG1_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG1_WK_LVL_EN	RESERVED			PADCONFIG1_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6087. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG1_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG1_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG1_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG1_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG1_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG1_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6087. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG1_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG1_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG1_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG1_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG1_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG1_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG1_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG1_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG1_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.33 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Register

14.2.1.2.1.1.2.33.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Register (Offset = 4008h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6088. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4008h

Figure 14-3030. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Name Register

31	30	29	28	27	26	25	24
PADCONFIG2_LOCK	PADCONFIG2_WKUP_EVT	PADCONFIG2_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG2_ISO_BYP	PADCONFIG2_ISO_OVR	PADCONFIG2_TX_DIS	PADCONFIG2_DRV_STR		PADCONFIG2_RXACTIVE	PADCONFIG2_PULLTYPESEL	PADCONFIG2_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG2_ST_EN	PADCONFIG2_DEBOUNCE_SEL			RESERVED		PADCONFIG2_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG2_WK_LVL_EN	RESERVED			PADCONFIG2_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6089. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG2_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG2_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG2_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG2_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG2_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG2_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6089. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG2_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG2_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG2_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG2_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG2_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG2_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG2_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG2_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG2_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.34 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Register

14.2.1.2.1.1.2.34.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Register (Offset = 400Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6090. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 400Ch

Figure 14-3031. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Name Register

31	30	29	28	27	26	25	24
PADCONFIG3_LOCK	PADCONFIG3_WKUP_EVT	PADCONFIG3_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG3_ISO_BYP	PADCONFIG3_ISO_OVR	PADCONFIG3_TX_DIS	PADCONFIG3_DRV_STR		PADCONFIG3_RXACTIVE	PADCONFIG3_PULLTYPESEL	PADCONFIG3_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG3_ST_EN	PADCONFIG3_DEBOUNCE_SEL			RESERVED		PADCONFIG3_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG3_WK_LVL_EN	RESERVED			PADCONFIG3_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6091. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG3_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG3_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG3_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG3_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG3_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG3_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6091. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG3_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG3_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG3_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG3_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG3_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG3_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG3_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG3_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG3_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.35 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Register

14.2.1.2.1.1.2.35.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Register (Offset = 4010h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6092. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4010h

Figure 14-3032. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Name Register

31	30	29	28	27	26	25	24
PADCONFIG4_LOCK	PADCONFIG4_WKUP_EVT	PADCONFIG4_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG4_ISO_BYP	PADCONFIG4_ISO_OVR	PADCONFIG4_TX_DIS	PADCONFIG4_DRV_STR		PADCONFIG4_RXACTIVE	PADCONFIG4_PULLTYPESEL	PADCONFIG4_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG4_ST_EN	PADCONFIG4_DEBOUNCE_SEL			RESERVED		PADCONFIG4_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG4_WK_LVL_EN	RESERVED			PADCONFIG4_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6093. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG4_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG4_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG4_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG4_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG4_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG4_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6093. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG4_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG4_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG4_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG4_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG4_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG4_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG4_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG4_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG4_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.36 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Register

14.2.1.2.1.1.2.36.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Register (Offset = 4014h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6094. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4014h

Figure 14-3033. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Name Register

31	30	29	28	27	26	25	24
PADCONFIG5_LOCK	PADCONFIG5_WKUP_EVT	PADCONFIG5_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG5_ISO_BYP	PADCONFIG5_ISO_OVR	PADCONFIG5_TX_DIS	PADCONFIG5_DRV_STR		PADCONFIG5_RXACTIVE	PADCONFIG5_PULLTYPESEL	PADCONFIG5_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG5_ST_EN	PADCONFIG5_DEBOUNCE_SEL			RESERVED		PADCONFIG5_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG5_WK_LVL_EN	RESERVED			PADCONFIG5_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6095. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG5_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG5_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG5_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG5_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG5_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG5_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6095. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG5_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG5_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG5_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG5_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG5_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG5_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG5_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG5_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG5_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.37 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Register

14.2.1.2.1.1.2.37.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Register (Offset = 4018h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6096. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4018h

Figure 14-3034. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Name Register

31	30	29	28	27	26	25	24
PADCONFIG6_LOCK	PADCONFIG6_WKUP_EVT	PADCONFIG6_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG6_ISO_BYP	PADCONFIG6_ISO_OVR	PADCONFIG6_TX_DIS	PADCONFIG6_DRV_STR		PADCONFIG6_RXACTIVE	PADCONFIG6_PULLTYPESEL	PADCONFIG6_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG6_ST_EN	PADCONFIG6_DEBOUNCE_SEL			RESERVED		PADCONFIG6_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG6_WK_LVL_EN	RESERVED			PADCONFIG6_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6097. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG6_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG6_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG6_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG6_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG6_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG6_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6097. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG6_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG6_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG6_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG6_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG6_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG6_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG6_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG6_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG6_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.38 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Register

14.2.1.2.1.1.2.38.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Register (Offset = 401Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6098. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 401Ch

Figure 14-3035. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Name Register

31	30	29	28	27	26	25	24
PADCONFIG7_LOCK	PADCONFIG7_WKUP_EVT	PADCONFIG7_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG7_ISO_BYP	PADCONFIG7_ISO_OVR	PADCONFIG7_TX_DIS	PADCONFIG7_DRV_STR		PADCONFIG7_RXACTIVE	PADCONFIG7_PULLTYPESEL	PADCONFIG7_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG7_ST_EN	PADCONFIG7_DEBOUNCE_SEL			RESERVED		PADCONFIG7_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG7_WK_LVL_EN	RESERVED			PADCONFIG7_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6099. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG7_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG7_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG7_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG7_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG7_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG7_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6099. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG7_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG7_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG7_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG7_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG7_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG7_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG7_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG7_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG7_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.39 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Register

14.2.1.2.1.1.2.39.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Register (Offset = 4020h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6100. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4020h

Figure 14-3036. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Name Register

31	30	29	28	27	26	25	24
PADCONFIG8_LOCK	PADCONFIG8_WKUP_EVT	PADCONFIG8_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG8_ISO_BYP	PADCONFIG8_ISO_OVR	PADCONFIG8_TX_DIS	PADCONFIG8_DRV_STR		PADCONFIG8_RXACTIVE	PADCONFIG8_PULLTYPESEL	PADCONFIG8_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG8_ST_EN	PADCONFIG8_DEBOUNCE_SEL			RESERVED		PADCONFIG8_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG8_WK_LVL_EN	RESERVED			PADCONFIG8_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6101. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG8_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG8_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG8_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG8_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG8_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG8_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6101. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG8_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG8_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG8_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG8_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG8_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG8_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG8_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG8_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG8_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.40 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Register

14.2.1.2.1.1.2.40.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Register (Offset = 4024h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6102. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4024h

Figure 14-3037. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Name Register

31	30	29	28	27	26	25	24
PADCONFIG9_LOCK	PADCONFIG9_WKUP_EVT	PADCONFIG9_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG9_ISO_BYP	PADCONFIG9_ISO_OVR	PADCONFIG9_TX_DIS	PADCONFIG9_DRV_STR		PADCONFIG9_RXACTIVE	PADCONFIG9_PULLTYPESEL	PADCONFIG9_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG9_ST_EN	PADCONFIG9_DEBOUNCE_SEL			RESERVED		PADCONFIG9_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG9_WK_LVL_EN	RESERVED			PADCONFIG9_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6103. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG9_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG9_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG9_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG9_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG9_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG9_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6103. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG9_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG9_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG9_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG9_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG9_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG9_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG9_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG9_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG9_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.41 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Register

14.2.1.2.1.1.2.41.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Register (Offset = 4028h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6104. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4028h

Figure 14-3038. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Name Register

31	30	29	28	27	26	25	24
PADCONFIG10_LOCK	PADCONFIG10_WKUP_EVT	PADCONFIG10_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG10_ISO_BYP	PADCONFIG10_ISO_OVR	PADCONFIG10_TX_DIS	PADCONFIG10_DRV_STR		PADCONFIG10_RXACTIVE	PADCONFIG10_PULLTYPESEL	PADCONFIG10_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG10_ST_EN	PADCONFIG10_DEBOUNCE_SEL			RESERVED		PADCONFIG10_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG10_WK_LVL_EN	RESERVED			PADCONFIG10_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6105. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG10_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG10_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG10_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG10_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG10_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG10_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6105. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG10_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG10_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG10_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG10_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG10_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG10_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG10_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG10_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG10_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.42 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Register

14.2.1.2.1.1.2.42.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Register (Offset = 402Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6106. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 402Ch

Figure 14-3039. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Name Register

31	30	29	28	27	26	25	24
PADCONFIG11_LOCK	PADCONFIG11_WKUP_EVT	PADCONFIG11_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG11_ISO_BYP	PADCONFIG11_ISO_OVR	PADCONFIG11_TX_DIS	PADCONFIG11_DRV_STR		PADCONFIG11_RXACTIVE	PADCONFIG11_PULLTYPESEL	PADCONFIG11_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG11_ST_EN	PADCONFIG11_DEBOUNCE_SEL			RESERVED		PADCONFIG11_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG11_WK_LVL_EN	RESERVED			PADCONFIG11_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6107. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG11_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG11_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG11_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG11_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG11_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG11_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6107. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG11_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG11_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG11_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG11_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG11_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG11_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG11_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG11_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG11_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.43 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Register

14.2.1.2.1.1.2.43.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Register (Offset = 4030h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6108. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4030h

Figure 14-3040. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Name Register

31	30	29	28	27	26	25	24
PADCONFIG12_LOCK	PADCONFIG12_WKUP_EVT	PADCONFIG12_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG12_ISO_BYP	PADCONFIG12_ISO_OVR	PADCONFIG12_TX_DIS	PADCONFIG12_DRV_STR		PADCONFIG12_RXACTIVE	PADCONFIG12_PULLTYPESEL	PADCONFIG12_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG12_ST_EN	PADCONFIG12_DEBOUNCE_SEL			RESERVED		PADCONFIG12_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG12_WK_LVL_EN	RESERVED			PADCONFIG12_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6109. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG12_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG12_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG12_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG12_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG12_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG12_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6109. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG12_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG12_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG12_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG12_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG12_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG12_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG12_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG12_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG12_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.44 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Register

14.2.1.2.1.1.2.44.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Register (Offset = 4034h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6110. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4034h

Figure 14-3041. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Name Register

31	30	29	28	27	26	25	24
PADCONFIG13_LOCK	PADCONFIG13_WKUP_EVT	PADCONFIG13_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG13_ISO_BYP	PADCONFIG13_ISO_OVR	PADCONFIG13_TX_DIS	PADCONFIG13_DRV_STR		PADCONFIG13_RXACTIVE	PADCONFIG13_PULLTYPESEL	PADCONFIG13_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG13_ST_EN	PADCONFIG13_DEBOUNCE_SEL			RESERVED		PADCONFIG13_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG13_WK_LVL_EN	RESERVED			PADCONFIG13_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6111. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG13_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG13_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG13_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG13_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG13_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG13_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6111. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG13_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG13_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG13_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG13_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG13_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG13_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG13_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG13_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG13_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.45 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Register

14.2.1.2.1.1.2.45.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Register (Offset = 4038h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6112. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4038h

Figure 14-3042. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Name Register

31	30	29	28	27	26	25	24
PADCONFIG14_LOCK	PADCONFIG14_WKUP_EVT	PADCONFIG14_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG14_ISO_BYP	PADCONFIG14_ISO_OVR	PADCONFIG14_TX_DIS	PADCONFIG14_DRV_STR		PADCONFIG14_RXACTIVE	PADCONFIG14_PULLTYPESEL	PADCONFIG14_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG14_ST_EN	PADCONFIG14_DEBOUNCE_SEL			RESERVED		PADCONFIG14_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG14_WK_LVL_EN	RESERVED			PADCONFIG14_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6113. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG14_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG14_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG14_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG14_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG14_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG14_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6113. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG14_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG14_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG14_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG14_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG14_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG14_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG14_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG14_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG14_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.46 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Register

14.2.1.2.1.1.2.46.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Register (Offset = 403Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6114. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 403Ch

Figure 14-3043. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Name Register

31	30	29	28	27	26	25	24
PADCONFIG15_LOCK	PADCONFIG15_WKUP_EVT	PADCONFIG15_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG15_ISO_BYP	PADCONFIG15_ISO_OVR	PADCONFIG15_TX_DIS	PADCONFIG15_DRV_STR		PADCONFIG15_RXACTIVE	PADCONFIG15_PULLTYPESEL	PADCONFIG15_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG15_ST_EN	PADCONFIG15_DEBOUNCE_SEL			RESERVED		PADCONFIG15_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG15_WK_LVL_EN	RESERVED			PADCONFIG15_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6115. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG15_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG15_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG15_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG15_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG15_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG15_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6115. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG15_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG15_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG15_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG15_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG15_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG15_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG15_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG15_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG15_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.47 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Register

14.2.1.2.1.1.2.47.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Register (Offset = 4040h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6116. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4040h

Figure 14-3044. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Name Register

31	30	29	28	27	26	25	24
PADCONFIG16_LOCK	PADCONFIG16_WKUP_EVT	PADCONFIG16_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG16_ISO_BYP	PADCONFIG16_ISO_OVR	PADCONFIG16_TX_DIS	PADCONFIG16_DRV_STR		PADCONFIG16_RXACTIVE	PADCONFIG16_PULLTYPESEL	PADCONFIG16_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG16_ST_EN	PADCONFIG16_DEBOUNCE_SEL			RESERVED		PADCONFIG16_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG16_WK_LVL_EN	RESERVED			PADCONFIG16_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6117. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG16_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG16_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG16_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG16_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG16_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG16_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6117. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG16_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG16_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG16_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG16_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG16_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG16_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG16_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG16_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG16_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.48 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Register

14.2.1.2.1.1.2.48.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Register (Offset = 404Ch) [reset = 8054007h]

Register to control pin configuration and muxing

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Table 14-6118. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 404Ch

Figure 14-3045. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Name Register

31	30	29	28	27	26	25	24
PADCONFIG19_LOCK	PADCONFIG19_WKUP_EVT	PADCONFIG19_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG19_ISO_BYP	PADCONFIG19_ISO_OVR	PADCONFIG19_TX_DIS	PADCONFIG19_DRV_STR		PADCONFIG19_RXACTIVE	PADCONFIG19_PULLTYPESEL	PADCONFIG19_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG19_ST_EN	PADCONFIG19_DEBOUNCE_SEL			RESERVED		PADCONFIG19_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG19_WK_LVL_EN	RESERVED			PADCONFIG19_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6119. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG19_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG19_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG19_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG19_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG19_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG19_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6119. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG19_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG19_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG19_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG19_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG19_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG19_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG19_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG19_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG19_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.49 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Register

14.2.1.2.1.1.2.49.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Register (Offset = 4050h) [reset = 8054007h]

Register to control pin configuration and muxing

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Table 14-6120. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4050h

Figure 14-3046. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Name Register

31	30	29	28	27	26	25	24
PADCONFIG20_LOCK	PADCONFIG20_WKUP_EVT	PADCONFIG20_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG20_ISO_BYP	PADCONFIG20_ISO_OVR	PADCONFIG20_TX_DIS	PADCONFIG20_DRV_STR		PADCONFIG20_RXACTIVE	PADCONFIG20_PULLTYPESEL	PADCONFIG20_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG20_ST_EN	PADCONFIG20_DEBOUNCE_SEL			RESERVED		PADCONFIG20_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG20_WK_LVL_EN	RESERVED			PADCONFIG20_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6121. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG20_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG20_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG20_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG20_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG20_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG20_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6121. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG20_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG20_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG20_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG20_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG20_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG20_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG20_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG20_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG20_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.50 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Register

14.2.1.2.1.1.2.50.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Register (Offset = 4054h) [reset = 10264000h]

Register to control pin configuration and muxing

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Table 14-6122. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4054h

Figure 14-3047. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Name Register

31	30	29	28	27	26	25	24
PADCONFIG21_LOCK	PADCONFIG21_WKUP_EVT	PADCONFIG21_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	1h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG21_ISO_BYP	PADCONFIG21_ISO_OVR	PADCONFIG21_TX_DIS	PADCONFIG21_DRV_STR		PADCONFIG21_RXACTIVE	PADCONFIG21_PULLTYPESEL	PADCONFIG21_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	14	13	12	11	10	9	8
	PADCONFIG21_ST_EN	PADCONFIG21_DEBOUNCE_SEL			RESERVED		PADCONFIG21_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG21_WK_LVL_EN	RESERVED			PADCONFIG21_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6123. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG21_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG21_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG21_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG21_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG21_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG21_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6123. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG21_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG21_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG21_PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG21_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG21_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG21_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG21_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG21_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG21_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.51 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Register

14.2.1.2.1.1.2.51.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Register (Offset = 4058h) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6124. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4058h

Figure 14-3048. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Name Register

31	30	29	28	27	26	25	24
PADCONFIG22_LOCK	PADCONFIG22_WKUP_EVT	PADCONFIG22_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG22_ISO_BYP	PADCONFIG22_ISO_OVR	PADCONFIG22_TX_DIS	PADCONFIG22_DRV_STR		PADCONFIG22_RXACTIVE	PADCONFIG22_PULLTYPESEL	PADCONFIG22_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG22_ST_EN	PADCONFIG22_DEBOUNCE_SEL			RESERVED		PADCONFIG22_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG22_WK_LVL_EN	RESERVED			PADCONFIG22_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6125. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG22_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG22_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG22_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG22_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG22_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG22_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6125. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG22_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG22_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG22_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG22_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG22_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG22_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG22_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG22_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG22_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.52 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Register

14.2.1.2.1.1.2.52.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Register (Offset = 405Ch) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6126. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 405Ch

Figure 14-3049. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Name Register

31	30	29	28	27	26	25	24
PADCONFIG23_LOCK	PADCONFIG23_WKUP_EVT	PADCONFIG23_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG23_ISO_BYP	PADCONFIG23_ISO_OVR	PADCONFIG23_TX_DIS	PADCONFIG23_DRV_STR		PADCONFIG23_RXACTIVE	PADCONFIG23_PULLTYPESEL	PADCONFIG23_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG23_ST_EN	PADCONFIG23_DEBOUNCE_SEL			RESERVED		PADCONFIG23_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG23_WK_LVL_EN	RESERVED			PADCONFIG23_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6127. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG23_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG23_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG23_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG23_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG23_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG23_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6127. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG23_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG23_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG23_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG23_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG23_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG23_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG23_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG23_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG23_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.53 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Register

14.2.1.2.1.1.2.53.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Register (Offset = 4060h) [reset = 44000h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6128. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4060h

Figure 14-3050. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG24_LOCK</td><td>PADCONFIG24_WKUP_EVT</td><td>PADCONFIG24_WKUP_EN</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG24_ISO_BYP</td><td>PADCONFIG24_ISO_OVR</td><td>PADCONFIG24_TX_DIS</td><td colspan="2">PADCONFIG24_DRV_STR</td><td>PADCONFIG24_RXACTIVE</td><td>PADCONFIG24_PULLTYPESEL</td><td>PADCONFIG24_PULLUDEN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>1h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG24_ST_EN</td><td colspan="3">PADCONFIG24_DEBOUNCE_SEL</td><td colspan="2">RESERVED</td><td>PADCONFIG24_WK_LVL_POL</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG24_WK_LVL_EN</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG24_MUXMODE</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6129. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG24_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG24_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG24_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG24_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG24_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG24_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6129. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG24_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG24_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG24_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG24_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG24_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG24_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG24_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG24_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG24_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.54 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Register

14.2.1.2.1.1.2.54.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Register (Offset = 4064h) [reset = 8264000h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6130. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4064h

Figure 14-3051. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Name Register

31	30	29	28	27	26	25	24
PADCONFIG25_LOCK	PADCONFIG25_WKUP_EVT	PADCONFIG25_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG25_ISO_BYP	PADCONFIG25_ISO_OVR	PADCONFIG25_TX_DIS	PADCONFIG25_DRV_STR		PADCONFIG25_RXACTIVE	PADCONFIG25_PULLTYPESEL	PADCONFIG25_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG25_ST_EN	PADCONFIG25_DEBOUNCE_SEL			RESERVED		PADCONFIG25_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG25_WK_LVL_EN	RESERVED			PADCONFIG25_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6131. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG25_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG25_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG25_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG25_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG25_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG25_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6131. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG25_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG25_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG25_PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG25_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG25_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG25_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG25_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG25_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG25_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.55 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Register

14.2.1.2.1.1.2.55.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Register (Offset = 4068h) [reset = 8244000h]

Register to control pin configuration and muxing

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Table 14-6132. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4068h

Figure 14-3052. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Name Register

31	30	29	28	27	26	25	24
PADCONFIG26_LOCK	PADCONFIG26_WKUP_EVT	PADCONFIG26_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG26_ISO_BYP	PADCONFIG26_ISO_OVR	PADCONFIG26_TX_DIS	PADCONFIG26_DRV_STR		PADCONFIG26_RXACTIVE	PADCONFIG26_PULLTYPESEL	PADCONFIG26_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG26_ST_EN	PADCONFIG26_DEBOUNCE_SEL			RESERVED		PADCONFIG26_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG26_WK_LVL_EN	RESERVED			PADCONFIG26_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6133. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG26_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG26_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG26_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG26_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG26_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG26_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6133. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG26_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG26_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG26_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG26_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG26_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG26_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG26_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG26_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG26_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.56 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Register

14.2.1.2.1.1.2.56.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Register (Offset = 406Ch) [reset = 8264000h]

Register to control pin configuration and muxing

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Table 14-6134. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 406Ch

Figure 14-3053. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Name Register

31	30	29	28	27	26	25	24
PADCONFIG27_LOCK	PADCONFIG27_WKUP_EVT	PADCONFIG27_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG27_ISO_BYP	PADCONFIG27_ISO_OVR	PADCONFIG27_TX_DIS	PADCONFIG27_DRV_STR		PADCONFIG27_RXACTIVE	PADCONFIG27_PULLTYPESEL	PADCONFIG27_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	14	13	12	11	10	9	8
	PADCONFIG27_ST_EN	PADCONFIG27_DEBOUNCE_SEL			RESERVED		PADCONFIG27_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG27_WK_LVL_EN	RESERVED			PADCONFIG27_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6135. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG27_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG27_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG27_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG27_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG27_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG27_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6135. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG27_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG27_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG27_PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG27_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG27_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG27_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG27_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG27_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG27_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.57 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Register

14.2.1.2.1.1.2.57.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Register (Offset = 4070h) [reset = 8024000h]

Register to control pin configuration and muxing

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Table 14-6136. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4070h

Figure 14-3054. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Name Register

31	30	29	28	27	26	25	24
PADCONFIG28_LOCK	PADCONFIG28_WKUP_EVT	PADCONFIG28_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG28_ISO_BYP	PADCONFIG28_ISO_OVR	PADCONFIG28_TX_DIS	PADCONFIG28_DRV_STR		PADCONFIG28_RXACTIVE	PADCONFIG28_PULLTYPESEL	PADCONFIG28_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	1h	0h
15	14	13	12	11	10	9	8
	PADCONFIG28_ST_EN	PADCONFIG28_DEBOUNCE_SEL			RESERVED		PADCONFIG28_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG28_WK_LVL_EN	RESERVED			PADCONFIG28_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6137. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG28_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG28_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG28_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG28_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG28_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG28_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6137. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG28_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG28_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG28_PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG28_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG28_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG28_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG28_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG28_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG28_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.58 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Register

14.2.1.2.1.1.2.58.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Register (Offset = 4074h) [reset = 8264000h]

Register to control pin configuration and muxing

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Table 14-6138. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4074h

Figure 14-3055. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Name Register

31	30	29	28	27	26	25	24
PADCONFIG29_LOCK	PADCONFIG29_WKUP_EVT	PADCONFIG29_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG29_ISO_BYP	PADCONFIG29_ISO_OVR	PADCONFIG29_TX_DIS	PADCONFIG29_DRV_STR		PADCONFIG29_RXACTIVE	PADCONFIG29_PULLTYPESEL	PADCONFIG29_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG29_ST_EN	PADCONFIG29_DEBOUNCE_SEL			RESERVED		PADCONFIG29_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG29_WK_LVL_EN	RESERVED			PADCONFIG29_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6139. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG29_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG29_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG29_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG29_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG29_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG29_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6139. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG29_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG29_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG29_PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG29_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG29_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG29_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG29_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG29_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG29_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.59 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Register

14.2.1.2.1.1.2.59.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Register (Offset = 4078h) [reset = 10264000h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6140. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4078h

Figure 14-3056. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Name Register

31	30	29	28	27	26	25	24
PADCONFIG30_LOCK	PADCONFIG30_WKUP_EVT	PADCONFIG30_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	1h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG30_ISO_BYP	PADCONFIG30_ISO_OVR	PADCONFIG30_TX_DIS	PADCONFIG30_DRV_STR		PADCONFIG30_RXACTIVE	PADCONFIG30_PULLTYPESEL	PADCONFIG30_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG30_ST_EN	PADCONFIG30_DEBOUNCE_SEL			RESERVED		PADCONFIG30_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG30_WK_LVL_EN	RESERVED			PADCONFIG30_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6141. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG30_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG30_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG30_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG30_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG30_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG30_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6141. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG30_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG30_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG30_PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG30_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG30_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG30_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG30_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG30_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG30_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.60 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Register

14.2.1.2.1.1.2.60.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Register (Offset = 407Ch) [reset = 10264000h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6142. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 407Ch

Figure 14-3057. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Name Register

31	30	29	28	27	26	25	24
PADCONFIG31_LOCK	PADCONFIG31_WKUP_EVT	PADCONFIG31_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	1h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG31_ISO_BYP	PADCONFIG31_ISO_OVR	PADCONFIG31_TX_DIS	PADCONFIG31_DRV_STR		PADCONFIG31_RXACTIVE	PADCONFIG31_PULLTYPESEL	PADCONFIG31_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG31_ST_EN	PADCONFIG31_DEBOUNCE_SEL			RESERVED		PADCONFIG31_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG31_WK_LVL_EN	RESERVED			PADCONFIG31_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6143. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG31_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG31_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG31_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG31_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG31_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG31_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6143. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG31_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG31_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG31_PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG31_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG31_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG31_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG31_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG31_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG31_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.61 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32 Register

14.2.1.2.1.1.2.61.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32 Register (Offset = 4080h) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6144. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4080h

Figure 14-3058. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32 Name Register

31	30	29	28	27	26	25	24
PADCONFIG32_LOCK	PADCONFIG32_WKUP_EVT	PADCONFIG32_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG32_ISO_BYP	PADCONFIG32_ISO_OVR	PADCONFIG32_TX_DIS	PADCONFIG32_DRV_STR		PADCONFIG32_RXACTIVE	PADCONFIG32_PULLTYPESEL	PADCONFIG32_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG32_ST_EN	PADCONFIG32_DEBOUNCE_SEL			RESERVED		PADCONFIG32_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG32_WK_LVL_EN	RESERVED			PADCONFIG32_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6145. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG32_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG32_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG32_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG32_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG32_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG32_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6145. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG32_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG32_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG32_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG32_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG32_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG32_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG32_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG32_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG32_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.62 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Register

14.2.1.2.1.1.2.62.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Register (Offset = 4084h) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6146. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 4084h

Figure 14-3059. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Name Register

31	30	29	28	27	26	25	24
PADCONFIG33_LOCK	PADCONFIG33_WKUP_EVT	PADCONFIG33_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG33_ISO_BYP	PADCONFIG33_ISO_OVR	PADCONFIG33_TX_DIS	PADCONFIG33_DRV_STR		PADCONFIG33_RXACTIVE	PADCONFIG33_PULLTYPESEL	PADCONFIG33_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG33_ST_EN	PADCONFIG33_DEBOUNCE_SEL			RESERVED		PADCONFIG33_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG33_WK_LVL_EN	RESERVED			PADCONFIG33_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6147. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG33_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG33_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG33_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG33_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG33_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG33_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6147. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG33_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG33_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG33_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG33_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG33_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG33_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG33_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG33_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG33_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.63 MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0 Register

14.2.1.2.1.1.2.63.1 MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-6148. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 5008h

Figure 14-3060. MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-6149. MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.64 MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1 Register

14.2.1.2.1.1.2.64.1 MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-6150. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 500Ch

Figure 14-3061. MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-6151. MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.65 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register

14.2.1.2.1.1.2.65.1 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6152. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 5100h

Figure 14-3062. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R0_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6153. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.66 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register

14.2.1.2.1.1.2.66.1 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6154. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 5104h

Figure 14-3063. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-6155. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.67 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Register

14.2.1.2.1.1.2.67.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Register (Offset = 6000h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6156. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6000h

Figure 14-3064. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG0_LOCK_PROXY	PADCONFIG0_WKUP_EVT_PROXY	PADCONFIG0_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG0_ISO_BYP_PROXY	PADCONFIG0_ISO_OVR_PROXY	PADCONFIG0_TX_DIS_PROXY	PADCONFIG0_DRV_STR_PROXY		PADCONFIG0_RXACTIVE_PROXY	PADCONFIG0_PULLTYPESEL_PROXY	PADCONFIG0_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG0_ST_EN_PROXY	PADCONFIG0_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG0_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG0_WK_LVL_EN_PROXY	RESERVED			PADCONFIG0_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6157. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG0_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG0_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG0_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG0_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG0_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6157. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG0_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG0_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG0_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG0_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG0_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG0_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG0_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG0_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG0_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG0_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.68 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Register

14.2.1.2.1.1.2.68.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Register (Offset = 6004h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6158. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6004h

Figure 14-3065. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG1_LOCK_PROXY	PADCONFIG1_WKUP_EVT_PROXY	PADCONFIG1_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG1_ISO_BYP_PROXY	PADCONFIG1_ISO_OVR_PROXY	PADCONFIG1_TX_DIS_PROXY	PADCONFIG1_DRV_STR_PROXY		PADCONFIG1_RXACTIVE_PROXY	PADCONFIG1_PULLTYPESEL_PROXY	PADCONFIG1_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG1_ST_EN_PROXY	PADCONFIG1_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG1_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG1_WK_LVL_EN_PROXY	RESERVED			PADCONFIG1_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6159. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG1_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG1_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG1_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG1_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG1_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6159. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG1_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG1_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG1_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG1_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG1_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG1_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG1_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG1_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG1_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG1_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.69 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Register

14.2.1.2.1.1.2.69.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Register (Offset = 6008h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6160. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6008h

Figure 14-3066. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG2_LOCK_PROXY	PADCONFIG2_WKUP_EVT_PROXY	PADCONFIG2_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG2_ISO_BYP_PROXY	PADCONFIG2_ISO_OVR_PROXY	PADCONFIG2_TX_DIS_PROXY	PADCONFIG2_DRV_STR_PROXY		PADCONFIG2_RXACTIVE_PROXY	PADCONFIG2_PULLTYPESEL_PROXY	PADCONFIG2_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG2_ST_EN_PROXY	PADCONFIG2_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG2_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG2_WK_LVL_EN_PROXY	RESERVED			PADCONFIG2_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6161. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG2_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG2_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG2_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG2_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG2_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6161. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG2_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG2_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG2_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG2_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG2_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG2_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG2_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG2_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG2_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG2_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.70 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Register

14.2.1.2.1.1.2.70.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Register (Offset = 600Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6162. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 600Ch

Figure 14-3067. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG3_LOCK_PROXY	PADCONFIG3_WKUP_EVT_PROXY	PADCONFIG3_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG3_ISO_BYP_PROXY	PADCONFIG3_ISO_OVR_PROXY	PADCONFIG3_TX_DIS_PROXY	PADCONFIG3_DRV_STR_PROXY		PADCONFIG3_RXACTIVE_PROXY	PADCONFIG3_PULLTYPESEL_PROXY	PADCONFIG3_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG3_ST_EN_PROXY	PADCONFIG3_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG3_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG3_WK_LVL_EN_PROXY	RESERVED			PADCONFIG3_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6163. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG3_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG3_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG3_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG3_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG3_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6163. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG3_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG3_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG3_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG3_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG3_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG3_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG3_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG3_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG3_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG3_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.71 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Register

14.2.1.2.1.1.2.71.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Register (Offset = 6010h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6164. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6010h

Figure 14-3068. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG4_LOCK_PROXY	PADCONFIG4_WKUP_EVT_PROXY	PADCONFIG4_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG4_ISO_BYP_PROXY	PADCONFIG4_ISO_OVR_PROXY	PADCONFIG4_TX_DIS_PROXY	PADCONFIG4_DRV_STR_PROXY		PADCONFIG4_RXACTIVE_PROXY	PADCONFIG4_PULLTYPESEL_PROXY	PADCONFIG4_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG4_ST_EN_PROXY	PADCONFIG4_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG4_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG4_WK_LVL_EN_PROXY	RESERVED			PADCONFIG4_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6165. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG4_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG4_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG4_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG4_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG4_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6165. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG4_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG4_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG4_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG4_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG4_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG4_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG4_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG4_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG4_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG4_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.72 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Register

14.2.1.2.1.1.2.72.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Register (Offset = 6014h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6166. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6014h

Figure 14-3069. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG5_LOCK_PROXY	PADCONFIG5_WKUP_EVT_PROXY	PADCONFIG5_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG5_ISO_BYP_PROXY	PADCONFIG5_ISO_OVR_PROXY	PADCONFIG5_TX_DIS_PROXY	PADCONFIG5_DRV_STR_PROXY		PADCONFIG5_RXACTIVE_PROXY	PADCONFIG5_PULLTYPESEL_PROXY	PADCONFIG5_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG5_ST_EN_PROXY	PADCONFIG5_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG5_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG5_WK_LVL_EN_PROXY	RESERVED			PADCONFIG5_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6167. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG5_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG5_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG5_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG5_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG5_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6167. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG5_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG5_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG5_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG5_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG5_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG5_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG5_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG5_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG5_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG5_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.73 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Register

14.2.1.2.1.1.2.73.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Register (Offset = 6018h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6168. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6018h

Figure 14-3070. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG6_LOCK_PROXY	PADCONFIG6_WKUP_EVT_PROXY	PADCONFIG6_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG6_ISO_BYP_PROXY	PADCONFIG6_ISO_OVR_PROXY	PADCONFIG6_TX_DIS_PROXY	PADCONFIG6_DRV_STR_PROXY		PADCONFIG6_RXACTIVE_PROXY	PADCONFIG6_PULLTYPESEL_PROXY	PADCONFIG6_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG6_ST_EN_PROXY	PADCONFIG6_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG6_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG6_WK_LVL_EN_PROXY	RESERVED			PADCONFIG6_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6169. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG6_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG6_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG6_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG6_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG6_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6169. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG6_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG6_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG6_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG6_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG6_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG6_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG6_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG6_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG6_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG6_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.74 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Register

14.2.1.2.1.1.2.74.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Register (Offset = 601Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6170. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 601Ch

Figure 14-3071. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG7_LOCK_PROXY	PADCONFIG7_WKUP_EVT_PROXY	PADCONFIG7_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG7_ISO_BYP_PROXY	PADCONFIG7_ISO_OVR_PROXY	PADCONFIG7_TX_DIS_PROXY	PADCONFIG7_DRV_STR_PROXY		PADCONFIG7_RXACTIVE_PROXY	PADCONFIG7_PULLTYPESEL_PROXY	PADCONFIG7_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG7_ST_EN_PROXY	PADCONFIG7_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG7_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG7_WK_LVL_EN_PROXY	RESERVED			PADCONFIG7_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6171. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG7_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG7_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG7_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG7_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG7_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6171. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG7_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG7_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG7_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG7_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG7_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG7_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG7_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG7_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG7_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG7_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.75 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Register

14.2.1.2.1.1.2.75.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Register (Offset = 6020h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6172. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6020h

Figure 14-3072. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG8_LOCK_PROXY	PADCONFIG8_WKUP_EVT_PROXY	PADCONFIG8_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG8_ISO_BYP_PROXY	PADCONFIG8_ISO_OVR_PROXY	PADCONFIG8_TX_DIS_PROXY	PADCONFIG8_DRV_STR_PROXY		PADCONFIG8_RXACTIVE_PROXY	PADCONFIG8_PULLTYPESEL_PROXY	PADCONFIG8_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG8_ST_EN_PROXY	PADCONFIG8_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG8_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG8_WK_LVL_EN_PROXY	RESERVED			PADCONFIG8_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6173. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG8_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG8_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG8_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG8_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG8_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6173. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG8_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG8_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG8_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG8_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG8_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG8_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG8_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG8_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG8_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG8_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.76 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Register

14.2.1.2.1.1.2.76.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Register (Offset = 6024h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6174. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6024h

Figure 14-3073. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG9_LOCK_PROXY	PADCONFIG9_WKUP_EVT_PROXY	PADCONFIG9_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG9_ISO_BYP_PROXY	PADCONFIG9_ISO_OVR_PROXY	PADCONFIG9_TX_DIS_PROXY	PADCONFIG9_DRV_STR_PROXY		PADCONFIG9_RXACTIVE_PROXY	PADCONFIG9_PULLTYPESEL_PROXY	PADCONFIG9_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG9_ST_EN_PROXY	PADCONFIG9_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG9_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG9_WK_LVL_EN_PROXY	RESERVED			PADCONFIG9_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6175. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG9_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG9_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG9_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG9_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG9_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6175. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG9_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG9_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG9_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG9_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG9_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG9_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG9_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG9_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG9_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG9_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.77 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Register

14.2.1.2.1.1.2.77.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Register (Offset = 6028h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6176. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6028h

Figure 14-3074. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG10_LOCK_PROXY	PADCONFIG10_WKUP_EVT_PROXY	PADCONFIG10_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG10_ISO_BYP_PROXY	PADCONFIG10_ISO_OVR_PROXY	PADCONFIG10_TX_DIS_PROXY	PADCONFIG10_DRV_STR_PROXY		PADCONFIG10_RXACTIVE_PROXY	PADCONFIG10_PULLTYPESEL_PROXY	PADCONFIG10_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG10_ST_EN_PROXY	PADCONFIG10_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG10_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG10_WK_LVL_EN_PROXY	RESERVED			PADCONFIG10_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6177. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG10_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG10_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG10_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG10_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG10_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6177. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG10_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG10_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG10_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG10_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG10_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG10_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG10_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG10_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG10_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG10_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.78 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Register

14.2.1.2.1.1.2.78.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Register (Offset = 602Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6178. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 602Ch

Figure 14-3075. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG11_LOCK_PROXY	PADCONFIG11_WKUP_EVT_PROXY	PADCONFIG11_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG11_ISO_BYP_PROXY	PADCONFIG11_ISO_OVR_PROXY	PADCONFIG11_TX_DIS_PROXY	PADCONFIG11_DRV_STR_PROXY		PADCONFIG11_RXACTIVE_PROXY	PADCONFIG11_PULLTYPESEL_PROXY	PADCONFIG11_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG11_ST_EN_PROXY	PADCONFIG11_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG11_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG11_WK_LVL_EN_PROXY	RESERVED			PADCONFIG11_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6179. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG11_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG11_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG11_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG11_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG11_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6179. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG11_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG11_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG11_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG11_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG11_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG11_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG11_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG11_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG11_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG11_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.79 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Register

14.2.1.2.1.1.2.79.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Register (Offset = 6030h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6180. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6030h

Figure 14-3076. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG12_LOCK_PROXY	PADCONFIG12_WKUP_EVT_PROXY	PADCONFIG12_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG12_ISO_BYP_PROXY	PADCONFIG12_ISO_OVR_PROXY	PADCONFIG12_TX_DIS_PROXY	PADCONFIG12_DRV_STR_PROXY		PADCONFIG12_RXACTIVE_PROXY	PADCONFIG12_PULLTYPESEL_PROXY	PADCONFIG12_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG12_ST_EN_PROXY	PADCONFIG12_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG12_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG12_WK_LVL_EN_PROXY	RESERVED			PADCONFIG12_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6181. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG12_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG12_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG12_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG12_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG12_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6181. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG12_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG12_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG12_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG12_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG12_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG12_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG12_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG12_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG12_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG12_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.80 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Register

14.2.1.2.1.1.2.80.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Register (Offset = 6034h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6182. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6034h

Figure 14-3077. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG13_LOCK_PROXY	PADCONFIG13_WKUP_EVT_PROXY	PADCONFIG13_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG13_ISO_BYP_PROXY	PADCONFIG13_ISO_OVR_PROXY	PADCONFIG13_TX_DIS_PROXY	PADCONFIG13_DRV_STR_PROXY		PADCONFIG13_RXACTIVE_PROXY	PADCONFIG13_PULLTYPESEL_PROXY	PADCONFIG13_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG13_ST_EN_PROXY	PADCONFIG13_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG13_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG13_WK_LVL_EN_PROXY	RESERVED			PADCONFIG13_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6183. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG13_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG13_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG13_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG13_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG13_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6183. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG13_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG13_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG13_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG13_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG13_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG13_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG13_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG13_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG13_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG13_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.81 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Register

14.2.1.2.1.1.2.81.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Register (Offset = 6038h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6184. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6038h

Figure 14-3078. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG14_LOCK_PROXY	PADCONFIG14_WKUP_EVT_PROXY	PADCONFIG14_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG14_ISO_BYP_PROXY	PADCONFIG14_ISO_OVR_PROXY	PADCONFIG14_TX_DIS_PROXY	PADCONFIG14_DRV_STR_PROXY		PADCONFIG14_RXACTIVE_PROXY	PADCONFIG14_PULLTYPESEL_PROXY	PADCONFIG14_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG14_ST_EN_PROXY	PADCONFIG14_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG14_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG14_WK_LVL_EN_PROXY	RESERVED			PADCONFIG14_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6185. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG14_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG14_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG14_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG14_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG14_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6185. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG14_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG14_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG14_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG14_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG14_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG14_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG14_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG14_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG14_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG14_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.82 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Register

14.2.1.2.1.1.2.82.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Register (Offset = 603Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6186. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 603Ch

Figure 14-3079. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG15_LOCK_PROXY	PADCONFIG15_WKUP_EVT_PROXY	PADCONFIG15_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG15_ISO_BYP_PROXY	PADCONFIG15_ISO_OVR_PROXY	PADCONFIG15_TX_DIS_PROXY	PADCONFIG15_DRV_STR_PROXY		PADCONFIG15_RXACTIVE_PROXY	PADCONFIG15_PULLTYPESEL_PROXY	PADCONFIG15_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG15_ST_EN_PROXY	PADCONFIG15_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG15_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG15_WK_LVL_EN_PROXY	RESERVED			PADCONFIG15_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6187. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG15_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG15_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG15_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG15_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG15_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6187. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG15_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG15_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG15_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG15_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG15_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG15_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG15_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG15_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG15_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG15_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.83 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Register

14.2.1.2.1.1.2.83.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Register (Offset = 6040h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6188. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6040h

Figure 14-3080. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG16_LOCK_PROXY	PADCONFIG16_WKUP_EVT_PROXY	PADCONFIG16_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG16_ISO_BYP_PROXY	PADCONFIG16_ISO_OVR_PROXY	PADCONFIG16_TX_DIS_PROXY	PADCONFIG16_DRV_STR_PROXY		PADCONFIG16_RXACTIVE_PROXY	PADCONFIG16_PULLTYPESEL_PROXY	PADCONFIG16_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG16_ST_EN_PROXY	PADCONFIG16_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG16_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG16_WK_LVL_EN_PROXY	RESERVED			PADCONFIG16_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6189. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG16_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG16_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG16_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG16_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG16_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6189. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG16_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG16_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG16_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG16_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG16_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG16_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG16_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG16_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG16_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG16_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.84 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Register

14.2.1.2.1.1.2.84.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Register (Offset = 604Ch) [reset = 8054007h]

Register to control pin configuration and muxing

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Table 14-6190. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 604Ch

Figure 14-3081. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG19_LOCK_PROXY	PADCONFIG19_WKUP_EVT_PROXY	PADCONFIG19_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG19_ISO_BYP_PROXY	PADCONFIG19_ISO_OVR_PROXY	PADCONFIG19_TX_DIS_PROXY	PADCONFIG19_DRV_STR_PROXY		PADCONFIG19_RXACTIVE_PROXY	PADCONFIG19_PULLTYPESEL_PROXY	PADCONFIG19_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG19_ST_EN_PROXY	PADCONFIG19_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG19_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG19_WK_LVL_EN_PROXY	RESERVED			PADCONFIG19_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6191. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG19_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG19_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG19_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG19_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG19_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6191. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG19_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG19_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG19_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG19_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG19_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG19_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG19_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG19_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG19_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG19_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.85 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Register

14.2.1.2.1.1.2.85.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Register (Offset = 6050h) [reset = 8054007h]

Register to control pin configuration and muxing

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Table 14-6192. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6050h

Figure 14-3082. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG20_LOCK_PROXY	PADCONFIG20_WKUP_EVT_PROXY	PADCONFIG20_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG20_ISO_BYP_PROXY	PADCONFIG20_ISO_OVR_PROXY	PADCONFIG20_TX_DIS_PROXY	PADCONFIG20_DRV_STR_PROXY		PADCONFIG20_RXACTIVE_PROXY	PADCONFIG20_PULLTYPESEL_PROXY	PADCONFIG20_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG20_ST_EN_PROXY	PADCONFIG20_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG20_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG20_WK_LVL_EN_PROXY	RESERVED			PADCONFIG20_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6193. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG20_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG20_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG20_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG20_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG20_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6193. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG20_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG20_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG20_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG20_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG20_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG20_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG20_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG20_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG20_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG20_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.86 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Register

14.2.1.2.1.1.2.86.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Register (Offset = 6054h) [reset = 10264000h]

Register to control pin configuration and muxing

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Table 14-6194. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6054h

Figure 14-3083. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG21_LOCK_PROXY	PADCONFIG21_WKUP_EVT_PROXY	PADCONFIG21_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	1h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG21_ISO_BYP_PROXY	PADCONFIG21_ISO_OVR_PROXY	PADCONFIG21_TX_DIS_PROXY	PADCONFIG21_DRV_STR_PROXY		PADCONFIG21_RXACTIVE_PROXY	PADCONFIG21_PULLTYPESEL_PROXY	PADCONFIG21_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG21_ST_EN_PROXY	PADCONFIG21_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG21_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG21_WK_LVL_EN_PROXY	RESERVED			PADCONFIG21_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6195. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG21_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG21_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG21_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG21_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG21_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6195. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG21_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG21_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG21_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG21_PULLTYPESEL_PROXY	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG21_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG21_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG21_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG21_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG21_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG21_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.87 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Register

14.2.1.2.1.1.2.87.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Register (Offset = 6058h) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6196. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6058h

Figure 14-3084. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG22_LOCK_PROXY	PADCONFIG22_WKUP_EVT_PROXY	PADCONFIG22_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG22_ISO_BYP_PROXY	PADCONFIG22_ISO_OVR_PROXY	PADCONFIG22_TX_DIS_PROXY	PADCONFIG22_DRV_STR_PROXY		PADCONFIG22_RXACTIVE_PROXY	PADCONFIG22_PULLTYPESEL_PROXY	PADCONFIG22_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG22_ST_EN_PROXY	PADCONFIG22_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG22_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG22_WK_LVL_EN_PROXY	RESERVED			PADCONFIG22_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6197. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG22_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG22_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG22_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG22_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG22_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6197. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG22_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG22_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG22_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG22_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG22_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG22_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG22_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG22_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG22_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG22_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.88 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Register

14.2.1.2.1.1.2.88.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Register (Offset = 605Ch) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6198. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 605Ch

Figure 14-3085. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG23_LOCK_PROXY	PADCONFIG23_WKUP_EVT_PROXY	PADCONFIG23_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG23_ISO_BYP_PROXY	PADCONFIG23_ISO_OVR_PROXY	PADCONFIG23_TX_DIS_PROXY	PADCONFIG23_DRV_STR_PROXY		PADCONFIG23_RXACTIVE_PROXY	PADCONFIG23_PULLTYPESEL_PROXY	PADCONFIG23_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG23_ST_EN_PROXY	PADCONFIG23_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG23_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG23_WK_LVL_EN_PROXY	RESERVED			PADCONFIG23_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6199. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG23_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG23_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG23_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG23_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG23_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6199. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG23_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG23_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG23_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG23_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG23_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG23_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG23_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG23_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG23_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG23_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.89 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Register

14.2.1.2.1.1.2.89.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Register (Offset = 6060h) [reset = 44000h]

Register to control pin configuration and muxing

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Table 14-6200. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6060h

Figure 14-3086. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG24_LOCK_PROXY	PADCONFIG24_WKUP_EVT_PROXY	PADCONFIG24_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG24_ISO_BYP_PROXY	PADCONFIG24_ISO_OVR_PROXY	PADCONFIG24_TX_DIS_PROXY	PADCONFIG24_DRV_STR_PROXY		PADCONFIG24_RXACTIVE_PROXY	PADCONFIG24_PULLTYPESEL_PROXY	PADCONFIG24_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		1h	0h	0h

15	14	13	12	11	10	9	8
	PADCONFIG24_ST_EN_PROXY	PADCONFIG24_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG24_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG24_WK_LVL_EN_PROXY	RESERVED			PADCONFIG24_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6201. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG24_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG24_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG24_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG24_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG24_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6201. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG24_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG24_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG24_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG24_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG24_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG24_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG24_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG24_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG24_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG24_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.90 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Register

14.2.1.2.1.1.2.90.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Register (Offset = 6064h) [reset = 8264000h]

Register to control pin configuration and muxing

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Table 14-6202. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6064h

Figure 14-3087. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG25_LOCK_PROXY	PADCONFIG25_WKUP_EVT_PROXY	PADCONFIG25_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG25_ISO_BYP_PROXY	PADCONFIG25_ISO_OVR_PROXY	PADCONFIG25_TX_DIS_PROXY	PADCONFIG25_DRV_STR_PROXY		PADCONFIG25_RXACTIVE_PROXY	PADCONFIG25_PULLTYPESEL_PROXY	PADCONFIG25_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG25_ST_EN_PROXY	PADCONFIG25_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG25_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG25_WK_LVL_EN_PROXY	RESERVED			PADCONFIG25_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6203. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG25_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG25_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG25_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG25_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG25_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6203. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG25_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG25_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG25_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG25_PULLTYPESEL_PROXY	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG25_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG25_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG25_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG25_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG25_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG25_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.91 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Register

14.2.1.2.1.1.2.91.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Register (Offset = 6068h) [reset = 8244000h]

Register to control pin configuration and muxing

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Table 14-6204. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6068h

Figure 14-3088. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG26_LOCK_PROXY	PADCONFIG26_WKUP_EVT_PROXY	PADCONFIG26_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG26_ISO_BYP_PROXY	PADCONFIG26_ISO_OVR_PROXY	PADCONFIG26_TX_DIS_PROXY	PADCONFIG26_DRV_STR_PROXY		PADCONFIG26_RXACTIVE_PROXY	PADCONFIG26_PULLTYPESEL_PROXY	PADCONFIG26_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	0h
15	14	13	12	11	10	9	8
	PADCONFIG26_ST_EN_PROXY	PADCONFIG26_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG26_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG26_WK_LVL_EN_PROXY	RESERVED			PADCONFIG26_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6205. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG26_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG26_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG26_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG26_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG26_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6205. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG26_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG26_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG26_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG26_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG26_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG26_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG26_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG26_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG26_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG26_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.92 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Register

14.2.1.2.1.1.2.92.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Register (Offset = 606Ch) [reset = 8264000h]

Register to control pin configuration and muxing

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Table 14-6206. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 606Ch

Figure 14-3089. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG27_LOCK_PROXY	PADCONFIG27_WKUP_EVT_PROXY	PADCONFIG27_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG27_ISO_BYP_PROXY	PADCONFIG27_ISO_OVR_PROXY	PADCONFIG27_TX_DIS_PROXY	PADCONFIG27_DRV_STR_PROXY		PADCONFIG27_RXACTIVE_PROXY	PADCONFIG27_PULLTYPESEL_PROXY	PADCONFIG27_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	14	13	12	11	10	9	8
	PADCONFIG27_ST_EN_PROXY	PADCONFIG27_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG27_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG27_WK_LVL_EN_PROXY	RESERVED			PADCONFIG27_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6207. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG27_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG27_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG27_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG27_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG27_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6207. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG27_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG27_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG27_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG27_PULLTYPESEL_PROXY	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG27_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG27_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG27_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG27_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG27_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG27_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.93 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Register

14.2.1.2.1.1.2.93.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Register (Offset = 6070h) [reset = 8024000h]

Register to control pin configuration and muxing

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Table 14-6208. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6070h

Figure 14-3090. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG28_LOCK_PROXY	PADCONFIG28_WKUP_EVT_PROXY	PADCONFIG28_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG28_ISO_BYP_PROXY	PADCONFIG28_ISO_OVR_PROXY	PADCONFIG28_TX_DIS_PROXY	PADCONFIG28_DRV_STR_PROXY		PADCONFIG28_RXACTIVE_PROXY	PADCONFIG28_PULLTYPESEL_PROXY	PADCONFIG28_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG28_ST_EN_PROXY	PADCONFIG28_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG28_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG28_WK_LVL_EN_PROXY	RESERVED			PADCONFIG28_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6209. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG28_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG28_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG28_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG28_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG28_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6209. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG28_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG28_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG28_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG28_PULLTYPESEL_PROXY	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG28_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG28_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG28_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG28_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG28_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG28_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.94 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Register

14.2.1.2.1.1.2.94.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Register (Offset = 6074h) [reset = 8264000h]

Register to control pin configuration and muxing

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Table 14-6210. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6074h

Figure 14-3091. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG29_LOCK_PROXY	PADCONFIG29_WKUP_EVT_PROXY	PADCONFIG29_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG29_ISO_BYP_PROXY	PADCONFIG29_ISO_OVR_PROXY	PADCONFIG29_TX_DIS_PROXY	PADCONFIG29_DRV_STR_PROXY		PADCONFIG29_RXACTIVE_PROXY	PADCONFIG29_PULLTYPESEL_PROXY	PADCONFIG29_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG29_ST_EN_PROXY	PADCONFIG29_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG29_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG29_WK_LVL_EN_PROXY	RESERVED			PADCONFIG29_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6211. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG29_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG29_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG29_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG29_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG29_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6211. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG29_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG29_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG29_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG29_PULLTYPESEL_PROXY	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG29_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG29_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG29_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG29_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG29_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG29_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.95 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Register

14.2.1.2.1.1.2.95.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Register (Offset = 6078h) [reset = 10264000h]

Register to control pin configuration and muxing

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Table 14-6212. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6078h

Figure 14-3092. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG30_LOCK_PROXY</td><td>PADCONFIG30_WKUP_EVT_PROXY</td><td>PADCONFIG30_WKUP_EN_PROXY</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG30_ISO_BYP_PROXY</td><td>PADCONFIG30_ISO_OVR_PROXY</td><td>PADCONFIG30_TX_DIS_PROXY</td><td colspan="2">PADCONFIG30_DRV_STR_PROXY</td><td>PADCONFIG30_RXACTIVE_PROXY</td><td>PADCONFIG30_PULLTYPESEL_PROXY</td><td>PADCONFIG30_PULLUDEN_PROXY</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>1h</td><td>1h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG30_ST_EN_PROXY</td><td colspan="3">PADCONFIG30_DEBOUNCE_SEL_PROXY</td><td colspan="2">RESERVED</td><td>PADCONFIG30_WK_LVL_POL_PROXY</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG30_WK_LVL_EN_PROXY</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG30_MUXMODE_PROXY</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-6213. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG30_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG30_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG30_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG30_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG30_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6213. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG30_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG30_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG30_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG30_PULLTYPESEL_PROXY	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG30_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG30_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG30_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG30_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG30_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG30_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.96 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Register

14.2.1.2.1.1.2.96.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Register (Offset = 607Ch) [reset = 10264000h]

Register to control pin configuration and muxing

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Table 14-6214. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 607Ch

Figure 14-3093. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG31_LOCK_PROXY	PADCONFIG31_WKUP_EVT_PROXY	PADCONFIG31_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	1h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG31_ISO_BYP_PROXY	PADCONFIG31_ISO_OVR_PROXY	PADCONFIG31_TX_DIS_PROXY	PADCONFIG31_DRV_STR_PROXY		PADCONFIG31_RXACTIVE_PROXY	PADCONFIG31_PULLTYPESEL_PROXY	PADCONFIG31_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG31_ST_EN_PROXY	PADCONFIG31_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG31_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG31_WK_LVL_EN_PROXY	RESERVED			PADCONFIG31_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6215. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG31_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG31_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG31_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG31_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG31_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6215. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG31_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG31_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG31_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG31_PULLTYPESEL_PROXY	R/W	1h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG31_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG31_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG31_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG31_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG31_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG31_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.97 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32_PROXY Register

14.2.1.2.1.1.2.97.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32_PROXY Register (Offset = 6080h) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6216. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6080h

Figure 14-3094. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG32_LOCK_PROXY	PADCONFIG32_WKUP_EVT_PROXY	PADCONFIG32_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG32_ISO_BYP_PROXY	PADCONFIG32_ISO_OVR_PROXY	PADCONFIG32_TX_DIS_PROXY	PADCONFIG32_DRV_STR_PROXY		PADCONFIG32_RXACTIVE_PROXY	PADCONFIG32_PULLTYPESEL_PROXY	PADCONFIG32_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG32_ST_EN_PROXY	PADCONFIG32_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG32_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG32_WK_LVL_EN_PROXY	RESERVED			PADCONFIG32_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6217. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG32_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG32_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG32_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG32_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG32_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6217. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG32_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG32_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG32_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG32_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG32_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG32_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG32_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG32_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG32_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG32_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG32_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.98 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Register

14.2.1.2.1.1.2.98.1 MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Register (Offset = 6084h) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6218. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 6084h

Figure 14-3095. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG33_LOCK_PROXY	PADCONFIG33_WKUP_EVT_PROXY	PADCONFIG33_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG33_ISO_BYP_PROXY	PADCONFIG33_ISO_OVR_PROXY	PADCONFIG33_TX_DIS_PROXY	PADCONFIG33_DRV_STR_PROXY		PADCONFIG33_RXACTIVE_PROXY	PADCONFIG33_PULLTYPESEL_PROXY	PADCONFIG33_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG33_ST_EN_PROXY	PADCONFIG33_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG33_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG33_WK_LVL_EN_PROXY	RESERVED			PADCONFIG33_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6219. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG33_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG33_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG33_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG33_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG33_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6219. MCU_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG33_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG33_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG33_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG33_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG33_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG33_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG33_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Field values (others are reserved): 3'b000 - No debounce enabled 3'b001 - Use DBOUNCE_CFG1 register value 3'b010 - Use DBOUNCE_CFG2 register value 3'b011 - Use DBOUNCE_CFG3 register value 3'b100 - Use DBOUNCE_CFG4 register value 3'b101 - Use DBOUNCE_CFG5 register value 3'b110 - Use DBOUNCE_CFG6 register value 3'b'111 - Reserved Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG33_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG33_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG33_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'h0 - Mux Mode 0 4'h1 - Mux Mode 1 4'h2 - Mux Mode 2 4'h3 - Mux Mode 3 4'h4 - Mux Mode 4 4'h5 - Mux Mode 5 4'h6 - Mux Mode 6 4'h7 - Mux Mode 7 4'h8 - Mux Mode 8 4'h9 - Mux Mode 9 4'hA - Mux Mode 10 4'hB - Mux Mode 11 4'hC - Mux Mode 12 4'hD - Mux Mode 13 4'hE - Mux Mode 14 4'hF - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.1.2.99 MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register

14.2.1.2.1.1.2.99.1 MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-6220. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 7008h

Figure 14-3096. MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-6221. MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.100 MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register

14.2.1.2.1.1.2.100.1 MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-6222. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 700Ch

Figure 14-3097. MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-6223. MCU_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.101 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register

14.2.1.2.1.1.2.101.1 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6224. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 7100h

Figure 14-3098. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-6225. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.1.2.102 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register

14.2.1.2.1.1.2.102.1 MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6226. Instance Table

Instance Name	Physical Address
MCU_PADCFG_CTRL0	0408 7104h

Figure 14-3099. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-6227. MCU_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2 PADCFG_CTRL

PADCFG_CTRL

14.2.1.2.1.2.1 PADCFG_CTRL Summaries

PADCFG_CTRL Summaries

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PID	000F 0000h
4h	32	MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0	000F 0004h
8h	32	MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1	000F 0008h
1008h	32	MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0	000F 1008h
100Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1	000F 100Ch
1010h	32	MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS	000F 1010h
1014h	32	MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR	000F 1014h
1018h	32	MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE	000F 1018h
101Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR	000F 101Ch
1020h	32	MAIN_PADCFG_CTRL_MMRCFG0_EOI	000F 1020h
1024h	32	MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS	000F 1024h
1028h	32	MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS	000F 1028h
102Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS	000F 102Ch
1030h	32	MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR	000F 1030h
1100h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY	000F 1100h
2000h	32	MAIN_PADCFG_CTRL_MMRCFG0_PID_PROXY	000F 2000h
2004h	32	MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY	000F 2004h
2008h	32	MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY	000F 2008h
3008h	32	MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY	000F 3008h
300Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY	000F 300Ch
3010h	32	MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY	000F 3010h
3014h	32	MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY	000F 3014h
3018h	32	MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY	000F 3018h
301Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY	000F 301Ch
3020h	32	MAIN_PADCFG_CTRL_MMRCFG0_EOI_PROXY	000F 3020h
3024h	32	MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY	000F 3024h
3028h	32	MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY	000F 3028h
302Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY	000F 302Ch
3030h	32	MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY	000F 3030h
3100h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0	000F 3100h

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
4000h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0	000F 4000h
4004h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1	000F 4004h
4008h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2	000F 4008h
400Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3	000F 400Ch
4010h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4	000F 4010h
4014h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5	000F 4014h
4018h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6	000F 4018h
401Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7	000F 401Ch
4020h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8	000F 4020h
4024h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9	000F 4024h
4028h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10	000F 4028h
402Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11	000F 402Ch
4030h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12	000F 4030h
4034h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13	000F 4034h
4038h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14	000F 4038h
403Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15	000F 403Ch
4040h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16	000F 4040h
4044h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17	000F 4044h
4048h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18	000F 4048h
404Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19	000F 404Ch
4050h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20	000F 4050h
4054h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21	000F 4054h
4058h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22	000F 4058h
405Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23	000F 405Ch
4060h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24	000F 4060h
4064h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25	000F 4064h
4068h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26	000F 4068h
406Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27	000F 406Ch
4070h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28	000F 4070h
4074h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29	000F 4074h
4078h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30	000F 4078h
407Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31	000F 407Ch
4084h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33	000F 4084h
4088h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34	000F 4088h
408Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35	000F 408Ch
4090h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36	000F 4090h
4094h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37	000F 4094h
4098h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38	000F 4098h
409Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39	000F 409Ch
40A0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40	000F 40A0h
40A4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41	000F 40A4h
40A8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42	000F 40A8h
40ACh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43	000F 40ACh
40B0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44	000F 40B0h
40B4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45	000F 40B4h
40B8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46	000F 40B8h

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
40BCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47	000F 40BCh
40C0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48	000F 40C0h
40C4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49	000F 40C4h
40C8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50	000F 40C8h
40CCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51	000F 40CCh
40D0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52	000F 40D0h
40D4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53	000F 40D4h
40E0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56	000F 40E0h
40E4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57	000F 40E4h
40E8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58	000F 40E8h
40ECh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59	000F 40ECh
40F0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60	000F 40F0h
40FCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63	000F 40FCh
4100h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64	000F 4100h
4104h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65	000F 4104h
4108h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66	000F 4108h
410Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67	000F 410Ch
4110h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68	000F 4110h
4114h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69	000F 4114h
4118h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70	000F 4118h
411Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71	000F 411Ch
4120h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72	000F 4120h
4124h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73	000F 4124h
4128h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74	000F 4128h
412Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75	000F 412Ch
4130h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76	000F 4130h
4134h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77	000F 4134h
4138h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78	000F 4138h
413Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79	000F 413Ch
4140h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80	000F 4140h
4144h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81	000F 4144h
4148h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82	000F 4148h
414Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83	000F 414Ch
4150h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84	000F 4150h
4154h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85	000F 4154h
4158h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86	000F 4158h
415Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87	000F 415Ch
4160h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88	000F 4160h
4164h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89	000F 4164h
4168h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90	000F 4168h
416Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91	000F 416Ch
4170h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92	000F 4170h
4174h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93	000F 4174h
4178h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94	000F 4178h
417Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95	000F 417Ch
4180h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96	000F 4180h

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
4184h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97	000F 4184h
4188h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98	000F 4188h
418Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99	000F 418Ch
4190h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100	000F 4190h
4194h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101	000F 4194h
4198h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102	000F 4198h
419Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103	000F 419Ch
41A0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104	000F 41A0h
41A4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105	000F 41A4h
41A8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106	000F 41A8h
41ACh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107	000F 41ACh
41B0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108	000F 41B0h
41B4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109	000F 41B4h
41B8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110	000F 41B8h
41BCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111	000F 41BCh
41C0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112	000F 41C0h
41C4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113	000F 41C4h
41C8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114	000F 41C8h
41CCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115	000F 41CCh
41D0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116	000F 41D0h
41D4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117	000F 41D4h
41D8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118	000F 41D8h
41DCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119	000F 41DCh
41E0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120	000F 41E0h
41E4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121	000F 41E4h
41E8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122	000F 41E8h
41ECh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123	000F 41ECh
41F0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124	000F 41F0h
41F4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125	000F 41F4h
41F8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126	000F 41F8h
41FCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127	000F 41FCh
4200h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128	000F 4200h
4204h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129	000F 4204h
4208h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130	000F 4208h
420Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131	000F 420Ch
4210h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132	000F 4210h
4214h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133	000F 4214h
4218h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134	000F 4218h
421Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135	000F 421Ch
4220h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136	000F 4220h
4224h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137	000F 4224h
4228h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138	000F 4228h
422Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139	000F 422Ch
4230h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140	000F 4230h
4234h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141	000F 4234h
423Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143	000F 423Ch

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
4240h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144	000F 4240h
4244h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145	000F 4244h
424Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147	000F 424Ch
4254h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149	000F 4254h
42ACh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171	000F 42ACh
42B0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172	000F 42B0h
42B4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173	000F 42B4h
42B8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174	000F 42B8h
42BCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175	000F 42BCh
42C0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176	000F 42C0h
42C4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177	000F 42C4h
42C8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178	000F 42C8h
42CCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179	000F 42CCh
42D0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180	000F 42D0h
42D4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181	000F 42D4h
42D8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182	000F 42D8h
42DCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183	000F 42DCh
5008h	32	MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0	000F 5008h
500Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1	000F 500Ch
5100h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY	000F 5100h
5104h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY	000F 5104h
5108h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY	000F 5108h
510Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3_READONLY	000F 510Ch
5110h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4_READONLY	000F 5110h
5114h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5_READONLY	000F 5114h
6000h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY	000F 6000h
6004h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY	000F 6004h
6008h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY	000F 6008h
600Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY	000F 600Ch
6010h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY	000F 6010h
6014h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY	000F 6014h
6018h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY	000F 6018h
601Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY	000F 601Ch
6020h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY	000F 6020h
6024h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY	000F 6024h

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
6028h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY	000F 6028h
602Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY	000F 602Ch
6030h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY	000F 6030h
6034h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY	000F 6034h
6038h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY	000F 6038h
603Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY	000F 603Ch
6040h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY	000F 6040h
6044h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17_PROXY	000F 6044h
6048h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18_PROXY	000F 6048h
604Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY	000F 604Ch
6050h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY	000F 6050h
6054h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY	000F 6054h
6058h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY	000F 6058h
605Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY	000F 605Ch
6060h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY	000F 6060h
6064h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY	000F 6064h
6068h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY	000F 6068h
606Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY	000F 606Ch
6070h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY	000F 6070h
6074h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY	000F 6074h
6078h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY	000F 6078h
607Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY	000F 607Ch
6084h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY	000F 6084h
6088h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34_PROXY	000F 6088h
608Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35_PROXY	000F 608Ch
6090h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36_PROXY	000F 6090h
6094h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37_PROXY	000F 6094h

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
6098h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38_PROXY	000F 6098h
609Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39_PROXY	000F 609Ch
60A0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40_PROXY	000F 60A0h
60A4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41_PROXY	000F 60A4h
60A8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42_PROXY	000F 60A8h
60ACh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43_PROXY	000F 60ACh
60B0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44_PROXY	000F 60B0h
60B4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45_PROXY	000F 60B4h
60B8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46_PROXY	000F 60B8h
60BCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47_PROXY	000F 60BCh
60C0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48_PROXY	000F 60C0h
60C4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49_PROXY	000F 60C4h
60C8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50_PROXY	000F 60C8h
60CCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51_PROXY	000F 60CCh
60D0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52_PROXY	000F 60D0h
60D4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53_PROXY	000F 60D4h
60E0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56_PROXY	000F 60E0h
60E4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57_PROXY	000F 60E4h
60E8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58_PROXY	000F 60E8h
60ECh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59_PROXY	000F 60ECh
60F0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60_PROXY	000F 60F0h
60FCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63_PROXY	000F 60FCh
6100h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64_PROXY	000F 6100h
6104h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65_PROXY	000F 6104h
6108h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66_PROXY	000F 6108h
610Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67_PROXY	000F 610Ch
6110h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68_PROXY	000F 6110h

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
6114h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69_PROXY	000F 6114h
6118h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70_PROXY	000F 6118h
611Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71_PROXY	000F 611Ch
6120h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72_PROXY	000F 6120h
6124h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73_PROXY	000F 6124h
6128h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74_PROXY	000F 6128h
612Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75_PROXY	000F 612Ch
6130h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76_PROXY	000F 6130h
6134h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77_PROXY	000F 6134h
6138h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78_PROXY	000F 6138h
613Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79_PROXY	000F 613Ch
6140h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80_PROXY	000F 6140h
6144h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81_PROXY	000F 6144h
6148h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82_PROXY	000F 6148h
614Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83_PROXY	000F 614Ch
6150h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84_PROXY	000F 6150h
6154h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85_PROXY	000F 6154h
6158h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86_PROXY	000F 6158h
615Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87_PROXY	000F 615Ch
6160h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88_PROXY	000F 6160h
6164h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89_PROXY	000F 6164h
6168h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90_PROXY	000F 6168h
616Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91_PROXY	000F 616Ch
6170h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92_PROXY	000F 6170h
6174h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93_PROXY	000F 6174h
6178h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94_PROXY	000F 6178h
617Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95_PROXY	000F 617Ch

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
6180h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96_PROXY	000F 6180h
6184h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97_PROXY	000F 6184h
6188h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98_PROXY	000F 6188h
618Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99_PROXY	000F 618Ch
6190h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100_PROXY	000F 6190h
6194h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101_PROXY	000F 6194h
6198h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102_PROXY	000F 6198h
619Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103_PROXY	000F 619Ch
61A0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104_PROXY	000F 61A0h
61A4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105_PROXY	000F 61A4h
61A8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106_PROXY	000F 61A8h
61ACh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107_PROXY	000F 61ACh
61B0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108_PROXY	000F 61B0h
61B4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109_PROXY	000F 61B4h
61B8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110_PROXY	000F 61B8h
61BCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111_PROXY	000F 61BCh
61C0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112_PROXY	000F 61C0h
61C4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113_PROXY	000F 61C4h
61C8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114_PROXY	000F 61C8h
61CCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115_PROXY	000F 61CCh
61D0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116_PROXY	000F 61D0h
61D4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117_PROXY	000F 61D4h
61D8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118_PROXY	000F 61D8h
61DCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119_PROXY	000F 61DCh
61E0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120_PROXY	000F 61E0h
61E4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121_PROXY	000F 61E4h
61E8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122_PROXY	000F 61E8h

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
61ECh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123_PROXY	000F 61ECh
61F0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124_PROXY	000F 61F0h
61F4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125_PROXY	000F 61F4h
61F8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126_PROXY	000F 61F8h
61FCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127_PROXY	000F 61FCh
6200h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128_PROXY	000F 6200h
6204h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129_PROXY	000F 6204h
6208h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130_PROXY	000F 6208h
620Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131_PROXY	000F 620Ch
6210h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132_PROXY	000F 6210h
6214h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133_PROXY	000F 6214h
6218h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134_PROXY	000F 6218h
621Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135_PROXY	000F 621Ch
6220h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136_PROXY	000F 6220h
6224h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137_PROXY	000F 6224h
6228h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138_PROXY	000F 6228h
622Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139_PROXY	000F 622Ch
6230h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140_PROXY	000F 6230h
6234h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141_PROXY	000F 6234h
623Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143_PROXY	000F 623Ch
6240h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144_PROXY	000F 6240h
6244h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145_PROXY	000F 6244h
624Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147_PROXY	000F 624Ch
6254h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149_PROXY	000F 6254h
62ACh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171_PROXY	000F 62ACh
62B0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172_PROXY	000F 62B0h
62B4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173_PROXY	000F 62B4h

Table 14-6228. MAIN_PADCFG_CTRL_MMR_CFG0 Registers, Base Address=000F 0000h, Length=32768 (continued)

Offset	Length	Register Name	PADCFG_CTRL0 Physical Address
62B8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174_PROXY	000F 62B8h
62BCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175_PROXY	000F 62BCh
62C0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176_PROXY	000F 62C0h
62C4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177_PROXY	000F 62C4h
62C8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178_PROXY	000F 62C8h
62CCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179_PROXY	000F 62CCh
62D0h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180_PROXY	000F 62D0h
62D4h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181_PROXY	000F 62D4h
62D8h	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182_PROXY	000F 62D8h
62DCh	32	MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183_PROXY	000F 62DCh
7008h	32	MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY	000F 7008h
700Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY	000F 700Ch
7100h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0	000F 7100h
7104h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1	000F 7104h
7108h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2	000F 7108h
710Ch	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3	000F 710Ch
7110h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4	000F 7110h
7114h	32	MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5	000F 7114h

14.2.1.2.1.2.2 PADCFG_CTRL Registers

PADCFG_CTRL Registers

14.2.1.2.1.2.2.1 MAIN_PADCFG_CTRL_MMRCFG0_PID Register

14.2.1.2.1.2.2.1.1 MAIN_PADCFG_CTRL_MMRCFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-6229. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 0000h

Figure 14-3100. MAIN_PADCFG_CTRL_MMRCFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MSB16							
R							
6180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PID_CUSTOM		PID_MINOR					
R		R					
0h		15h					

Table 14-6230. MAIN_PADCFG_CTRL_MMRCFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.2 MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0 Register

14.2.1.2.1.2.2.2.1 MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0 Register (Offset = 4h) [reset = 10000000h]

Indicates the version of the CFG used to create the MMR Module

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Table 14-6231. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 0004h

Figure 14-3101. MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0 Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV							
R							
1000h							
23	22	21	20	19	18	17	16
MMR_CFG0_CFG_REV							
R							
1000h							
15	14	13	12	11	10	9	8
MMR_CFG0_SPEC_REV							
R							
0h							
7	6	5	4	3	2	1	0
MMR_CFG0_SPEC_REV							
R							
0h							

Table 14-6232. MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV	R	0h	Minor spec-only revision. Deprecated. Was intended to reflect non-RTL updates in the printed Spec but this can't be reflected in the MMR read value without an RTL change when post RTL descriptions are pushed into the VPS. Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.3 MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1 Register

14.2.1.2.1.2.2.3.1 MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1 Register (Offset = 8h) [reset = 80000003h]

Indicates the MMR configuration

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Table 14-6233. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 0008h

Figure 14-3102. MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1 Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS							
R							
3h							

Table 14-6234. MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS	R	3h	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.4 MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0 Register

14.2.1.2.1.2.2.4.1 MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component

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Table 14-6235. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1008h

Figure 14-3103. MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 14-6236. MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.5 MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1 Register

14.2.1.2.1.2.2.5.1 MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component

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Table 14-6237. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 100Ch

Figure 14-3104. MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 14-6238. MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.6 MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS Register

14.2.1.2.1.2.2.6.1 MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-6239. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1010h

Figure 14-3105. MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6240. MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.7 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register

14.2.1.2.1.2.2.7.1 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-6241. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1014h

Figure 14-3106. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6242. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.8 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE Register

14.2.1.2.1.2.2.8.1 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register

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Table 14-6243. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1018h

Figure 14-3107. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6244. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.9 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register

14.2.1.2.1.2.2.9.1 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-6245. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 101Ch

Figure 14-3108. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6246. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.10 MAIN_PADCFG_CTRL_MMRCFG0_EOI Register

14.2.1.2.1.2.2.10.1 MAIN_PADCFG_CTRL_MMRCFG0_EOI Register (Offset = 1020h) [reset = 0h]

EOI register

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Table 14-6247. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1020h

Figure 14-3109. MAIN_PADCFG_CTRL_MMRCFG0_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 14-6248. MAIN_PADCFG_CTRL_MMRCFG0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.11 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS Register

14.2.1.2.1.2.2.11.1 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register

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Table 14-6249. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1024h

Figure 14-3110. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 14-6250. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.12 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register

14.2.1.2.1.2.2.12.1 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register

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Table 14-6251. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1028h

Figure 14-3111. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 14-6252. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.13 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register

14.2.1.2.1.2.2.13.1 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-6253. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 102Ch

Figure 14-3112. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID</td><td colspan="4">FAULT_ROUTEID</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6254. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.14 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR Register

14.2.1.2.1.2.2.14.1 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register

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Table 14-6255. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1030h

Figure 14-3113. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 14-6256. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.15 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register

14.2.1.2.1.2.2.15.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register (Offset = 1100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-6257. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 1100h

Figure 14-3114. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0_READONLY							
R							
0h							

Table 14-6258. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0_READONLY	R	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.16 MAIN_PADCFG_CTRL_MMRCFG0_PID_PROXY Register

14.2.1.2.1.2.2.16.1 MAIN_PADCFG_CTRL_MMRCFG0_PID_PROXY Register (Offset = 2000h) [reset = 61800215h]

PID register

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Table 14-6259. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 2000h

Figure 14-3115. MAIN_PADCFG_CTRL_MMRCFG0_PID_PROXY Name Register

31	30	29	28	27	26	25	24
PID_MSB16_PROXY							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16_PROXY							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC_PROXY					PID_MAJOR_PROXY		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM_PROXY		PID_MINOR_PROXY					
R		R					
0h		15h					

Table 14-6260. MAIN_PADCFG_CTRL_MMRCFG0_PID_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16_PROXY	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC_PROXY	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR_PROXY	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM_PROXY	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR_PROXY	R	15h	Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.17 MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY Register

14.2.1.2.1.2.2.17.1 MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY Register (Offset = 2004h) [reset = 10000000h]

Indicates the version of the CFG used to create the MMR Module

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Table 14-6261. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 2004h

Figure 14-3116. MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MMR_CFG0_CFG_REV_PROXY							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MMR_CFG0_SPEC_REV_PROXY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG0_SPEC_REV_PROXY							
R							
0h							

Table 14-6262. MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MMR_CFG0_CFG_REV_PROXY	R	1000h	Major configuration release Reset Source: mod_por_rst_n
15:0	MMR_CFG0_SPEC_REV_PROXY	R	0h	Minor spec-only revision. Deprecated. Was intended to reflect non-RTL updates in the printed Spec but this can't be reflected in the MMR read value without an RTL change when post RTL descriptions are pushed into the VPS. Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.18 MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY Register

14.2.1.2.1.2.2.18.1 MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY Register (Offset = 2008h) [reset = 80000003h]

Indicates the MMR configuration

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Table 14-6263. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 2008h

Figure 14-3117. MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY Name Register

31	30	29	28	27	26	25	24
MMR_CFG1_PROXY_EN_PROXY	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_CFG1_PARTITIONS_PROXY							
R							
3h							

Table 14-6264. MAIN_PADCFG_CTRL_MMRCFG0_MMR_CFG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MMR_CFG1_PROXY_EN_PROXY	R	1h	Proxy addressing enabled Reset Source: mod_por_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	MMR_CFG1_PARTITIONS_PROXY	R	3h	Indicates present partitions Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.19 MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register

14.2.1.2.1.2.2.19.1 MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register (Offset = 3008h) [reset = 0h]

- KICK0 component

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Table 14-6265. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3008h

Figure 14-3118. MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0_PROXY							
R/W							
0h							

Table 14-6266. MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.20 MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register

14.2.1.2.1.2.2.20.1 MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register (Offset = 300Ch) [reset = 0h]

- KICK1 component

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Table 14-6267. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 300Ch

Figure 14-3119. MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1_PROXY							
R/W							
0h							

Table 14-6268. MAIN_PADCFG_CTRL_MMRCFG0_LOCK0_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.21 MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register

14.2.1.2.1.2.2.21.1 MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register (Offset = 3010h) [reset = 0h]

Interrupt Raw Status/Set Register

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Table 14-6269. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3010h

Figure 14-3120. MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_PROXY	KICK_ERR_PROXY	ADDR_ERR_PROXY	PROT_ERR_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6270. MAIN_PADCFG_CTRL_MMRCFG0_INTR_RAW_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_PROXY	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_PROXY	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_PROXY	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_PROXY	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.22 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register

14.2.1.2.1.2.2.22.1 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register (Offset = 3014h) [reset = 0h]

Interrupt Enabled Status/Clear register

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Table 14-6271. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3014h

Figure 14-3121. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR_PROXY	ENABLED_KICK_ERR_PROXY	ENABLED_ADDR_ERR_PROXY	ENABLED_PROT_ERR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6272. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLED_STATUS_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR_PROXY	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR_PROXY	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR_PROXY	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR_PROXY	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.23 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register

14.2.1.2.1.2.2.23.1 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register (Offset = 3018h) [reset = 0h]

Interrupt Enable register

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Table 14-6273. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3018h

Figure 14-3122. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_PROXY	KICK_ERR_EN_PROXY	ADDR_ERR_EN_PROXY	PROT_ERR_EN_PROXY
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-6274. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_PROXY	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_PROXY	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_PROXY	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_PROXY	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.24 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register

14.2.1.2.1.2.2.24.1 MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register (Offset = 301Ch) [reset = 0h]

Interrupt Enable Clear register

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Table 14-6275. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 301Ch

Figure 14-3123. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR_PROXY	KICK_ERR_EN_CLR_PROXY	ADDR_ERR_EN_CLR_PROXY	PROT_ERR_EN_CLR_PROXY
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-6276. MAIN_PADCFG_CTRL_MMRCFG0_INTR_ENABLE_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR_PROXY	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR_PROXY	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR_PROXY	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR_PROXY	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.25 MAIN_PADCFG_CTRL_MMRCFG0_EOI_PROXY Register

14.2.1.2.1.2.2.25.1 MAIN_PADCFG_CTRL_MMRCFG0_EOI_PROXY Register (Offset = 3020h) [reset = 0h]

EOI register

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Table 14-6277. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3020h

Figure 14-3124. MAIN_PADCFG_CTRL_MMRCFG0_EOI_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR_PROXY							
R/W							
0h							

Table 14-6278. MAIN_PADCFG_CTRL_MMRCFG0_EOI_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR_PROXY	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.26 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register

14.2.1.2.1.2.2.26.1 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register (Offset = 3024h) [reset = 0h]

Fault Address register

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Table 14-6279. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3024h

Figure 14-3125. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR_PROXY							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR_PROXY							
R							
0h							

Table 14-6280. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ADDRESS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR_PROXY	R	0h	Fault Address. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.27 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register

14.2.1.2.1.2.2.27.1 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register (Offset = 3028h) [reset = 0h]

Fault Type Status register

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Table 14-6281. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3028h

Figure 14-3126. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS_PROXY	FAULT_TYPE_PROXY					
NONE	R	R					
0h	0h	0h					

Table 14-6282. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_TYPE_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS_PROXY	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE_PROXY	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.28 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register

14.2.1.2.1.2.2.28.1 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register (Offset = 302Ch) [reset = 0h]

Fault Attribute Status register

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Table 14-6283. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 302Ch

Figure 14-3127. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Name Register

31	30	29	28	27	26	25	24
FAULT_XID_PROXY							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID_PROXY				FAULT_ROUTEID_PROXY			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID_PROXY							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID_PROXY							
R							
0h							

Table 14-6284. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_ATTR_STATUS_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID_PROXY	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID_PROXY	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID_PROXY	R	0h	Privilege ID. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.29 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register

14.2.1.2.1.2.2.29.1 MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register (Offset = 3030h) [reset = 0h]

Fault Clear register

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Table 14-6285. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3030h

Figure 14-3128. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR_PROXY
NONE							W
0h							0h

Table 14-6286. MAIN_PADCFG_CTRL_MMRCFG0_FAULT_CLEAR_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR_PROXY	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.30 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register

14.2.1.2.1.2.2.30.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register (Offset = 3100h) [reset = 0h]

Claim bits for Partition 0

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Table 14-6287. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 3100h

Figure 14-3129. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P0_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P0_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P0_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P0_R0							
R/W							
0h							

Table 14-6288. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P0_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P0_R0	R/W	0h	Claim bits for Partition 0 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.31 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Register

14.2.1.2.1.2.2.31.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Register (Offset = 4000h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6289. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4000h

Figure 14-3130. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Name Register

31	30	29	28	27	26	25	24
PADCONFIG0_LOCK	PADCONFIG0_WKUP_EVT	PADCONFIG0_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG0_ISO_BYP	PADCONFIG0_ISO_OVR	PADCONFIG0_TX_DIS	PADCONFIG0_DRV_STR		PADCONFIG0_RXACTIVE	PADCONFIG0_PULLTYPESEL	PADCONFIG0_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG0_ST_EN	PADCONFIG0_DEBOUNCE_SEL			RESERVED		PADCONFIG0_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG0_WK_LVL_EN	RESERVED			PADCONFIG0_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6290. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG0_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG0_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG0_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG0_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG0_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG0_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6290. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG0_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG0_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG0_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG0_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG0_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG0_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG0_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG0_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG0_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.32 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Register

14.2.1.2.1.2.2.32.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Register (Offset = 4004h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6291. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4004h

Figure 14-3131. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Name Register

31	30	29	28	27	26	25	24
PADCONFIG1_LOCK	PADCONFIG1_WKUP_EVT	PADCONFIG1_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG1_ISO_BYP	PADCONFIG1_ISO_OVR	PADCONFIG1_TX_DIS	PADCONFIG1_DRV_STR		PADCONFIG1_RXACTIVE	PADCONFIG1_PULLTYPESEL	PADCONFIG1_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG1_ST_EN	PADCONFIG1_DEBOUNCE_SEL			RESERVED		PADCONFIG1_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG1_WK_LVL_EN	RESERVED			PADCONFIG1_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6292. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG1_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG1_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG1_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG1_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG1_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG1_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6292. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG1_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG1_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG1_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG1_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG1_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG1_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG1_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG1_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG1_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.33 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Register

14.2.1.2.1.2.2.33.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Register (Offset = 4008h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6293. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4008h

Figure 14-3132. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Name Register

31	30	29	28	27	26	25	24
PADCONFIG2_LOCK	PADCONFIG2_WKUP_EVT	PADCONFIG2_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG2_ISO_BYP	PADCONFIG2_ISO_OVR	PADCONFIG2_TX_DIS	PADCONFIG2_DRV_STR		PADCONFIG2_RXACTIVE	PADCONFIG2_PULLTYPESEL	PADCONFIG2_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG2_ST_EN	PADCONFIG2_DEBOUNCE_SEL			RESERVED		PADCONFIG2_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG2_WK_LVL_EN	RESERVED			PADCONFIG2_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6294. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG2_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG2_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG2_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG2_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG2_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG2_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6294. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG2_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG2_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG2_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG2_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG2_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG2_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG2_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG2_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG2_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.34 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Register

14.2.1.2.1.2.2.34.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Register (Offset = 400Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6295. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 400Ch

Figure 14-3133. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Name Register

31	30	29	28	27	26	25	24
PADCONFIG3_LOCK	PADCONFIG3_WKUP_EVT	PADCONFIG3_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG3_ISO_BYP	PADCONFIG3_ISO_OVR	PADCONFIG3_TX_DIS	PADCONFIG3_DRV_STR		PADCONFIG3_RXACTIVE	PADCONFIG3_PULLTYPESEL	PADCONFIG3_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG3_ST_EN	PADCONFIG3_DEBOUNCE_SEL			RESERVED		PADCONFIG3_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG3_WK_LVL_EN	RESERVED			PADCONFIG3_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6296. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG3_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG3_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG3_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG3_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG3_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG3_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6296. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG3_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG3_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG3_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG3_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG3_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG3_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG3_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG3_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG3_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.35 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Register

14.2.1.2.1.2.2.35.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Register (Offset = 4010h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6297. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4010h

Figure 14-3134. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Name Register

31	30	29	28	27	26	25	24
PADCONFIG4_LOCK	PADCONFIG4_WKUP_EVT	PADCONFIG4_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG4_ISO_BYP	PADCONFIG4_ISO_OVR	PADCONFIG4_TX_DIS	PADCONFIG4_DRV_STR		PADCONFIG4_RXACTIVE	PADCONFIG4_PULLTYPESEL	PADCONFIG4_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG4_ST_EN	PADCONFIG4_DEBOUNCE_SEL			RESERVED		PADCONFIG4_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG4_WK_LVL_EN	RESERVED			PADCONFIG4_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6298. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG4_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG4_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG4_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG4_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG4_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG4_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6298. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG4_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG4_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG4_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG4_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG4_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG4_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG4_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG4_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG4_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.36 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Register

14.2.1.2.1.2.2.36.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Register (Offset = 4014h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6299. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4014h

Figure 14-3135. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Name Register

31	30	29	28	27	26	25	24
PADCONFIG5_LOCK	PADCONFIG5_WKUP_EVT	PADCONFIG5_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG5_ISO_BYP	PADCONFIG5_ISO_OVR	PADCONFIG5_TX_DIS	PADCONFIG5_DRV_STR		PADCONFIG5_RXACTIVE	PADCONFIG5_PULLTYPESEL	PADCONFIG5_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG5_ST_EN	PADCONFIG5_DEBOUNCE_SEL			RESERVED		PADCONFIG5_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG5_WK_LVL_EN	RESERVED			PADCONFIG5_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6300. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG5_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG5_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG5_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG5_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG5_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG5_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6300. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG5_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG5_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG5_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG5_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG5_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG5_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG5_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG5_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG5_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.37 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Register

14.2.1.2.1.2.2.37.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Register (Offset = 4018h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6301. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4018h

Figure 14-3136. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Name Register

31	30	29	28	27	26	25	24
PADCONFIG6_LOCK	PADCONFIG6_WKUP_EVT	PADCONFIG6_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG6_ISO_BYP	PADCONFIG6_ISO_OVR	PADCONFIG6_TX_DIS	PADCONFIG6_DRV_STR		PADCONFIG6_RXACTIVE	PADCONFIG6_PULLTYPESEL	PADCONFIG6_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG6_ST_EN	PADCONFIG6_DEBOUNCE_SEL			RESERVED		PADCONFIG6_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG6_WK_LVL_EN	RESERVED			PADCONFIG6_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6302. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG6_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG6_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG6_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG6_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG6_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG6_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6302. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG6_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG6_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG6_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG6_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG6_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG6_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG6_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG6_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG6_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.38 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Register

14.2.1.2.1.2.2.38.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Register (Offset = 401Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6303. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 401Ch

Figure 14-3137. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Name Register

31	30	29	28	27	26	25	24
PADCONFIG7_LOCK	PADCONFIG7_WKUP_EVT	PADCONFIG7_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG7_ISO_BYP	PADCONFIG7_ISO_OVR	PADCONFIG7_TX_DIS	PADCONFIG7_DRV_STR		PADCONFIG7_RXACTIVE	PADCONFIG7_PULLTYPESEL	PADCONFIG7_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG7_ST_EN	PADCONFIG7_DEBOUNCE_SEL			RESERVED		PADCONFIG7_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG7_WK_LVL_EN	RESERVED			PADCONFIG7_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6304. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG7_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG7_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG7_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG7_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG7_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG7_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6304. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG7_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG7_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG7_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG7_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG7_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG7_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG7_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG7_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG7_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.39 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Register

14.2.1.2.1.2.2.39.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Register (Offset = 4020h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6305. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4020h

Figure 14-3138. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Name Register

31	30	29	28	27	26	25	24
PADCONFIG8_LOCK	PADCONFIG8_WKUP_EVT	PADCONFIG8_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG8_ISO_BYP	PADCONFIG8_ISO_OVR	PADCONFIG8_TX_DIS	PADCONFIG8_DRV_STR		PADCONFIG8_RXACTIVE	PADCONFIG8_PULLTYPESEL	PADCONFIG8_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG8_ST_EN	PADCONFIG8_DEBOUNCE_SEL			RESERVED		PADCONFIG8_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG8_WK_LVL_EN	RESERVED			PADCONFIG8_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6306. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG8_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG8_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG8_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG8_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG8_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG8_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6306. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG8_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG8_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG8_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG8_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG8_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG8_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG8_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG8_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG8_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.40 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Register

14.2.1.2.1.2.2.40.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Register (Offset = 4024h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6307. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4024h

Figure 14-3139. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Name Register

31	30	29	28	27	26	25	24
PADCONFIG9_LOCK	PADCONFIG9_WKUP_EVT	PADCONFIG9_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG9_ISO_BYP	PADCONFIG9_ISO_OVR	PADCONFIG9_TX_DIS	PADCONFIG9_DRV_STR		PADCONFIG9_RXACTIVE	PADCONFIG9_PULLTYPESEL	PADCONFIG9_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG9_ST_EN	PADCONFIG9_DEBOUNCE_SEL			RESERVED		PADCONFIG9_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG9_WK_LVL_EN	RESERVED			PADCONFIG9_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6308. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG9_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG9_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG9_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG9_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG9_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG9_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6308. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG9_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG9_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG9_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG9_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG9_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG9_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG9_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG9_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG9_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.41 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Register

14.2.1.2.1.2.2.41.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Register (Offset = 4028h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6309. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4028h

Figure 14-3140. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Name Register

31	30	29	28	27	26	25	24
PADCONFIG10_LOCK	PADCONFIG10_WKUP_EVT	PADCONFIG10_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG10_ISO_BYP	PADCONFIG10_ISO_OVR	PADCONFIG10_TX_DIS	PADCONFIG10_DRV_STR		PADCONFIG10_RXACTIVE	PADCONFIG10_PULLTYPESEL	PADCONFIG10_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG10_ST_EN	PADCONFIG10_DEBOUNCE_SEL			RESERVED		PADCONFIG10_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG10_WK_LVL_EN	RESERVED			PADCONFIG10_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6310. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG10_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG10_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG10_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG10_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG10_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG10_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6310. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG10_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG10_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG10_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG10_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG10_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG10_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG10_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG10_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG10_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.42 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Register

14.2.1.2.1.2.2.42.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Register (Offset = 402Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6311. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 402Ch

Figure 14-3141. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Name Register

31	30	29	28	27	26	25	24
PADCONFIG11_LOCK	PADCONFIG11_WKUP_EVT	PADCONFIG11_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG11_ISO_BYP	PADCONFIG11_ISO_OVR	PADCONFIG11_TX_DIS	PADCONFIG11_DRV_STR		PADCONFIG11_RXACTIVE	PADCONFIG11_PULLTYPESEL	PADCONFIG11_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG11_ST_EN	PADCONFIG11_DEBOUNCE_SEL			RESERVED		PADCONFIG11_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG11_WK_LVL_EN	RESERVED			PADCONFIG11_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6312. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG11_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG11_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG11_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG11_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG11_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG11_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6312. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG11_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG11_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG11_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG11_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG11_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG11_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG11_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG11_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG11_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.43 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Register

14.2.1.2.1.2.2.43.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Register (Offset = 4030h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6313. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4030h

Figure 14-3142. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Name Register

31	30	29	28	27	26	25	24
PADCONFIG12_LOCK	PADCONFIG12_WKUP_EVT	PADCONFIG12_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG12_ISO_BYP	PADCONFIG12_ISO_OVR	PADCONFIG12_TX_DIS	PADCONFIG12_DRV_STR		PADCONFIG12_RXACTIVE	PADCONFIG12_PULLTYPESEL	PADCONFIG12_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG12_ST_EN	PADCONFIG12_DEBOUNCE_SEL			RESERVED		PADCONFIG12_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG12_WK_LVL_EN	RESERVED			PADCONFIG12_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6314. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG12_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG12_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG12_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG12_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG12_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG12_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6314. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG12_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG12_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG12_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG12_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG12_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG12_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG12_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG12_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG12_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.44 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Register

14.2.1.2.1.2.2.44.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Register (Offset = 4034h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6315. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4034h

Figure 14-3143. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Name Register

31	30	29	28	27	26	25	24
PADCONFIG13_LOCK	PADCONFIG13_WKUP_EVT	PADCONFIG13_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG13_ISO_BYP	PADCONFIG13_ISO_OVR	PADCONFIG13_TX_DIS	PADCONFIG13_DRV_STR		PADCONFIG13_RXACTIVE	PADCONFIG13_PULLTYPESEL	PADCONFIG13_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG13_ST_EN	PADCONFIG13_DEBOUNCE_SEL			RESERVED		PADCONFIG13_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG13_WK_LVL_EN	RESERVED			PADCONFIG13_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6316. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG13_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG13_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG13_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG13_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG13_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG13_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6316. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG13_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG13_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG13_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG13_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG13_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG13_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG13_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG13_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG13_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.45 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Register

14.2.1.2.1.2.2.45.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Register (Offset = 4038h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6317. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4038h

Figure 14-3144. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Name Register

31	30	29	28	27	26	25	24
PADCONFIG14_LOCK	PADCONFIG14_WKUP_EVT	PADCONFIG14_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG14_ISO_BYP	PADCONFIG14_ISO_OVR	PADCONFIG14_TX_DIS	PADCONFIG14_DRV_STR		PADCONFIG14_RXACTIVE	PADCONFIG14_PULLTYPESEL	PADCONFIG14_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG14_ST_EN	PADCONFIG14_DEBOUNCE_SEL			RESERVED		PADCONFIG14_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG14_WK_LVL_EN	RESERVED			PADCONFIG14_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6318. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG14_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG14_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG14_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG14_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG14_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG14_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6318. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG14_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG14_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG14_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG14_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG14_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG14_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG14_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG14_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG14_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.46 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Register

14.2.1.2.1.2.2.46.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Register (Offset = 403Ch) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6319. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 403Ch

Figure 14-3145. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Name Register

31	30	29	28	27	26	25	24
PADCONFIG15_LOCK	PADCONFIG15_WKUP_EVT	PADCONFIG15_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG15_ISO_BYP	PADCONFIG15_ISO_OVR	PADCONFIG15_TX_DIS	PADCONFIG15_DRV_STR		PADCONFIG15_RXACTIVE	PADCONFIG15_PULLTYPESEL	PADCONFIG15_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG15_ST_EN	PADCONFIG15_DEBOUNCE_SEL			RESERVED		PADCONFIG15_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG15_WK_LVL_EN	RESERVED			PADCONFIG15_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6320. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG15_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG15_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG15_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG15_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG15_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG15_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6320. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG15_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG15_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG15_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG15_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG15_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG15_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG15_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG15_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG15_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.47 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Register

14.2.1.2.1.2.2.47.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Register (Offset = 4040h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6321. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4040h

Figure 14-3146. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Name Register

31	30	29	28	27	26	25	24
PADCONFIG16_LOCK	PADCONFIG16_WKUP_EVT	PADCONFIG16_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG16_ISO_BYP	PADCONFIG16_ISO_OVR	PADCONFIG16_TX_DIS	PADCONFIG16_DRV_STR		PADCONFIG16_RXACTIVE	PADCONFIG16_PULLTYPESEL	PADCONFIG16_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG16_ST_EN	PADCONFIG16_DEBOUNCE_SEL			RESERVED		PADCONFIG16_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG16_WK_LVL_EN	RESERVED			PADCONFIG16_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6322. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG16_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG16_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG16_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG16_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG16_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG16_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6322. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG16_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG16_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG16_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG16_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG16_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG16_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG16_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG16_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG16_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.48 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17 Register

14.2.1.2.1.2.2.48.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17 Register (Offset = 4044h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6323. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4044h

Figure 14-3147. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17 Name Register

31	30	29	28	27	26	25	24
PADCONFIG17_LOCK	PADCONFIG17_WKUP_EVT	PADCONFIG17_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG17_ISO_BYP	PADCONFIG17_ISO_OVR	PADCONFIG17_TX_DIS	PADCONFIG17_DRV_STR		PADCONFIG17_RXACTIVE	PADCONFIG17_PULLTYPESEL	PADCONFIG17_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG17_ST_EN	PADCONFIG17_DEBOUNCE_SEL			RESERVED		PADCONFIG17_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG17_WK_LVL_EN	RESERVED			PADCONFIG17_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6324. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG17_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG17_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG17_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG17_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG17_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG17_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6324. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG17_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG17_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG17_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG17_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG17_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG17_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG17_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG17_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG17_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.49 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18 Register

14.2.1.2.1.2.2.49.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18 Register (Offset = 4048h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6325. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4048h

Figure 14-3148. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18 Name Register

31	30	29	28	27	26	25	24
PADCONFIG18_LOCK	PADCONFIG18_WKUP_EVT	PADCONFIG18_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG18_ISO_BYP	PADCONFIG18_ISO_OVR	PADCONFIG18_TX_DIS	PADCONFIG18_DRV_STR		PADCONFIG18_RXACTIVE	PADCONFIG18_PULLTYPESEL	PADCONFIG18_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG18_ST_EN	PADCONFIG18_DEBOUNCE_SEL			RESERVED		PADCONFIG18_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG18_WK_LVL_EN	RESERVED			PADCONFIG18_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6326. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG18_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG18_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG18_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG18_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG18_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG18_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6326. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG18_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG18_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG18_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG18_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG18_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG18_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG18_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG18_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG18_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.50 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Register

14.2.1.2.1.2.2.50.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Register (Offset = 404Ch) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6327. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 404Ch

Figure 14-3149. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Name Register

31	30	29	28	27	26	25	24
PADCONFIG19_LOCK	PADCONFIG19_WKUP_EVT	PADCONFIG19_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG19_ISO_BYP	PADCONFIG19_ISO_OVR	PADCONFIG19_TX_DIS	PADCONFIG19_DRV_STR		PADCONFIG19_RXACTIVE	PADCONFIG19_PULLTYPESEL	PADCONFIG19_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG19_ST_EN	PADCONFIG19_DEBOUNCE_SEL			RESERVED		PADCONFIG19_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG19_WK_LVL_EN	RESERVED			PADCONFIG19_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6328. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG19_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG19_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG19_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG19_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG19_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG19_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6328. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG19_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG19_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG19_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG19_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG19_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG19_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG19_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG19_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG19_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.51 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Register

14.2.1.2.1.2.2.51.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Register (Offset = 4050h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6329. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4050h

Figure 14-3150. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Name Register

31	30	29	28	27	26	25	24
PADCONFIG20_LOCK	PADCONFIG20_WKUP_EVT	PADCONFIG20_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG20_ISO_BYP	PADCONFIG20_ISO_OVR	PADCONFIG20_TX_DIS	PADCONFIG20_DRV_STR		PADCONFIG20_RXACTIVE	PADCONFIG20_PULLTYPESEL	PADCONFIG20_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG20_ST_EN	PADCONFIG20_DEBOUNCE_SEL			RESERVED		PADCONFIG20_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG20_WK_LVL_EN	RESERVED			PADCONFIG20_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6330. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG20_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG20_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG20_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG20_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG20_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG20_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6330. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG20_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG20_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG20_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG20_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG20_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG20_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG20_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG20_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG20_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.52 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Register

14.2.1.2.1.2.2.52.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Register (Offset = 4054h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6331. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4054h

Figure 14-3151. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Name Register

31	30	29	28	27	26	25	24
PADCONFIG21_LOCK	PADCONFIG21_WKUP_EVT	PADCONFIG21_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG21_ISO_BYP	PADCONFIG21_ISO_OVR	PADCONFIG21_TX_DIS	PADCONFIG21_DRV_STR		PADCONFIG21_RXACTIVE	PADCONFIG21_PULLTYPESEL	PADCONFIG21_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG21_ST_EN	PADCONFIG21_DEBOUNCE_SEL			RESERVED		PADCONFIG21_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG21_WK_LVL_EN	RESERVED			PADCONFIG21_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6332. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG21_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG21_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG21_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG21_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG21_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG21_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6332. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG21_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG21_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG21_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG21_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG21_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG21_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG21_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG21_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG21_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.53 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Register

14.2.1.2.1.2.2.53.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Register (Offset = 4058h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6333. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4058h

Figure 14-3152. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Name Register

31	30	29	28	27	26	25	24
PADCONFIG22_LOCK	PADCONFIG22_WKUP_EVT	PADCONFIG22_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG22_ISO_BYP	PADCONFIG22_ISO_OVR	PADCONFIG22_TX_DIS	PADCONFIG22_DRV_STR		PADCONFIG22_RXACTIVE	PADCONFIG22_PULLTYPESEL	PADCONFIG22_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG22_ST_EN	PADCONFIG22_DEBOUNCE_SEL			RESERVED		PADCONFIG22_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG22_WK_LVL_EN	RESERVED			PADCONFIG22_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6334. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG22_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG22_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG22_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG22_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG22_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG22_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6334. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG22_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG22_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG22_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG22_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG22_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG22_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG22_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG22_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG22_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.54 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Register

14.2.1.2.1.2.2.54.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Register (Offset = 405Ch) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6335. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 405Ch

Figure 14-3153. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Name Register

31	30	29	28	27	26	25	24
PADCONFIG23_LOCK	PADCONFIG23_WKUP_EVT	PADCONFIG23_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG23_ISO_BYP	PADCONFIG23_ISO_OVR	PADCONFIG23_TX_DIS	PADCONFIG23_DRV_STR		PADCONFIG23_RXACTIVE	PADCONFIG23_PULLTYPESEL	PADCONFIG23_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG23_ST_EN	PADCONFIG23_DEBOUNCE_SEL			RESERVED		PADCONFIG23_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG23_WK_LVL_EN	RESERVED			PADCONFIG23_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6336. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG23_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG23_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG23_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG23_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG23_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG23_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6336. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG23_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG23_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG23_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG23_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG23_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG23_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG23_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG23_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG23_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.55 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Register

14.2.1.2.1.2.2.55.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Register (Offset = 4060h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6337. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4060h

Figure 14-3154. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Name Register

31	30	29	28	27	26	25	24
PADCONFIG24_LOCK	PADCONFIG24_WKUP_EVT	PADCONFIG24_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG24_ISO_BYP	PADCONFIG24_ISO_OVR	PADCONFIG24_TX_DIS	PADCONFIG24_DRV_STR		PADCONFIG24_RXACTIVE	PADCONFIG24_PULLTYPESEL	PADCONFIG24_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG24_ST_EN	PADCONFIG24_DEBOUNCE_SEL			RESERVED		PADCONFIG24_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG24_WK_LVL_EN	RESERVED			PADCONFIG24_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6338. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG24_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG24_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG24_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG24_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG24_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG24_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6338. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG24_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG24_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG24_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG24_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG24_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG24_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG24_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG24_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG24_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.56 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Register

14.2.1.2.1.2.2.56.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Register (Offset = 4064h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6339. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4064h

Figure 14-3155. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Name Register

31	30	29	28	27	26	25	24
PADCONFIG25_LOCK	PADCONFIG25_WKUP_EVT	PADCONFIG25_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG25_ISO_BYP	PADCONFIG25_ISO_OVR	PADCONFIG25_TX_DIS	PADCONFIG25_DRV_STR		PADCONFIG25_RXACTIVE	PADCONFIG25_PULLTYPESEL	PADCONFIG25_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG25_ST_EN	PADCONFIG25_DEBOUNCE_SEL			RESERVED		PADCONFIG25_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG25_WK_LVL_EN	RESERVED			PADCONFIG25_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6340. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG25_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG25_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG25_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG25_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG25_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG25_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6340. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG25_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG25_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG25_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG25_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG25_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG25_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG25_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG25_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG25_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.57 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Register

14.2.1.2.1.2.2.57.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Register (Offset = 4068h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6341. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4068h

Figure 14-3156. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Name Register

31	30	29	28	27	26	25	24
PADCONFIG26_LOCK	PADCONFIG26_WKUP_EVT	PADCONFIG26_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG26_ISO_BYP	PADCONFIG26_ISO_OVR	PADCONFIG26_TX_DIS	PADCONFIG26_DRV_STR		PADCONFIG26_RXACTIVE	PADCONFIG26_PULLTYPESEL	PADCONFIG26_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG26_ST_EN	PADCONFIG26_DEBOUNCE_SEL			RESERVED		PADCONFIG26_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG26_WK_LVL_EN	RESERVED			PADCONFIG26_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6342. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG26_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG26_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG26_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG26_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG26_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG26_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6342. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG26_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG26_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG26_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG26_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG26_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG26_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG26_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG26_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG26_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.58 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Register

14.2.1.2.1.2.2.58.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Register (Offset = 406Ch) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6343. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 406Ch

Figure 14-3157. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Name Register

31	30	29	28	27	26	25	24
PADCONFIG27_LOCK	PADCONFIG27_WKUP_EVT	PADCONFIG27_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG27_ISO_BYP	PADCONFIG27_ISO_OVR	PADCONFIG27_TX_DIS	PADCONFIG27_DRV_STR		PADCONFIG27_RXACTIVE	PADCONFIG27_PULLTYPESEL	PADCONFIG27_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG27_ST_EN	PADCONFIG27_DEBOUNCE_SEL			RESERVED		PADCONFIG27_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG27_WK_LVL_EN	RESERVED			PADCONFIG27_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6344. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG27_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG27_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG27_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG27_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG27_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG27_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6344. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG27_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG27_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG27_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG27_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG27_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG27_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG27_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG27_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG27_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.59 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Register

14.2.1.2.1.2.2.59.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Register (Offset = 4070h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6345. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4070h

Figure 14-3158. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Name Register

31	30	29	28	27	26	25	24
PADCONFIG28_LOCK	PADCONFIG28_WKUP_EVT	PADCONFIG28_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG28_ISO_BYP	PADCONFIG28_ISO_OVR	PADCONFIG28_TX_DIS	PADCONFIG28_DRV_STR		PADCONFIG28_RXACTIVE	PADCONFIG28_PULLTYPESEL	PADCONFIG28_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG28_ST_EN	PADCONFIG28_DEBOUNCE_SEL			RESERVED		PADCONFIG28_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG28_WK_LVL_EN	RESERVED			PADCONFIG28_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6346. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG28_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG28_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG28_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG28_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG28_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG28_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6346. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG28_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG28_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG28_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG28_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG28_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG28_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG28_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG28_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG28_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.60 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Register

14.2.1.2.1.2.2.60.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Register (Offset = 4074h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6347. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4074h

Figure 14-3159. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Name Register

31	30	29	28	27	26	25	24
PADCONFIG29_LOCK	PADCONFIG29_WKUP_EVT	PADCONFIG29_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG29_ISO_BYP	PADCONFIG29_ISO_OVR	PADCONFIG29_TX_DIS	PADCONFIG29_DRV_STR		PADCONFIG29_RXACTIVE	PADCONFIG29_PULLTYPESEL	PADCONFIG29_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG29_ST_EN	PADCONFIG29_DEBOUNCE_SEL			RESERVED		PADCONFIG29_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG29_WK_LVL_EN	RESERVED				PADCONFIG29_MUXMODE		
R/W	NONE				R/W		
0h	0h				7h		

Table 14-6348. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG29_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG29_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG29_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG29_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG29_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG29_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6348. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG29_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG29_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG29_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG29_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG29_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG29_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG29_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG29_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG29_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.61 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Register

14.2.1.2.1.2.2.61.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Register (Offset = 4078h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6349. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4078h

Figure 14-3160. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Name Register

31	30	29	28	27	26	25	24
PADCONFIG30_LOCK	PADCONFIG30_WKUP_EVT	PADCONFIG30_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG30_ISO_BYP	PADCONFIG30_ISO_OVR	PADCONFIG30_TX_DIS	PADCONFIG30_DRV_STR		PADCONFIG30_RXACTIVE	PADCONFIG30_PULLTYPESEL	PADCONFIG30_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG30_ST_EN	PADCONFIG30_DEBOUNCE_SEL			RESERVED		PADCONFIG30_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG30_WK_LVL_EN	RESERVED			PADCONFIG30_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6350. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG30_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG30_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG30_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG30_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG30_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG30_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6350. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG30_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG30_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG30_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG30_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG30_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG30_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG30_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG30_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG30_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.62 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Register

14.2.1.2.1.2.2.62.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Register (Offset = 407Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6351. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 407Ch

Figure 14-3161. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Name Register

31	30	29	28	27	26	25	24
PADCONFIG31_LOCK	PADCONFIG31_WKUP_EVT	PADCONFIG31_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG31_ISO_BYP	PADCONFIG31_ISO_OVR	PADCONFIG31_TX_DIS	PADCONFIG31_DRV_STR		PADCONFIG31_RXACTIVE	PADCONFIG31_PULLTYPESEL	PADCONFIG31_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG31_ST_EN	PADCONFIG31_DEBOUNCE_SEL			RESERVED		PADCONFIG31_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG31_WK_LVL_EN	RESERVED			PADCONFIG31_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6352. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG31_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG31_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG31_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG31_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG31_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG31_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6352. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG31_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG31_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG31_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG31_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG31_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG31_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG31_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG31_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG31_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.63 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Register

14.2.1.2.1.2.2.63.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Register (Offset = 4084h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6353. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4084h

Figure 14-3162. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG33_LOCK</td><td>PADCONFIG33_WKUP_EVT</td><td>PADCONFIG33_WKUP_EN</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG33_ISO_BYP</td><td>PADCONFIG33_ISO_OVR</td><td>PADCONFIG33_TX_DIS</td><td colspan="2">PADCONFIG33_DRV_STR</td><td>PADCONFIG33_RXACTIVE</td><td>PADCONFIG33_PULLTYPESEL</td><td>PADCONFIG33_PULLUDEN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG33_ST_EN</td><td colspan="3">PADCONFIG33_DEBOUNCE_SEL</td><td colspan="2">RESERVED</td><td>PADCONFIG33_WK_LVL_POL</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG33_WK_LVL_EN</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG33_MUXMODE</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-6354. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG33_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG33_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG33_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG33_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG33_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG33_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6354. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG33_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG33_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG33_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG33_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG33_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG33_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG33_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG33_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG33_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.64 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34 Register

14.2.1.2.1.2.2.64.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34 Register (Offset = 4088h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6355. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4088h

Figure 14-3163. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34 Name Register

31	30	29	28	27	26	25	24
PADCONFIG34_LOCK	PADCONFIG34_WKUP_EVT	PADCONFIG34_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG34_ISO_BYP	PADCONFIG34_ISO_OVR	PADCONFIG34_TX_DIS	PADCONFIG34_DRV_STR		PADCONFIG34_RXACTIVE	PADCONFIG34_PULLTYPESEL	PADCONFIG34_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG34_ST_EN	PADCONFIG34_DEBOUNCE_SEL			RESERVED		PADCONFIG34_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG34_WK_LVL_EN	RESERVED			PADCONFIG34_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6356. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG34_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG34_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG34_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG34_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG34_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG34_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6356. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG34_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG34_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG34_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG34_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG34_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG34_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG34_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG34_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG34_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.65 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35 Register

14.2.1.2.1.2.2.65.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35 Register (Offset = 408Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6357. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 408Ch

Figure 14-3164. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35 Name Register

31	30	29	28	27	26	25	24
PADCONFIG35_LOCK	PADCONFIG35_WKUP_EVT	PADCONFIG35_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG35_ISO_BYP	PADCONFIG35_ISO_OVR	PADCONFIG35_TX_DIS	PADCONFIG35_DRV_STR		PADCONFIG35_RXACTIVE	PADCONFIG35_PULLTYPESEL	PADCONFIG35_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG35_ST_EN	PADCONFIG35_DEBOUNCE_SEL			RESERVED		PADCONFIG35_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG35_WK_LVL_EN	RESERVED			PADCONFIG35_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6358. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG35_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG35_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG35_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG35_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG35_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG35_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6358. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG35_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG35_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG35_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG35_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG35_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG35_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG35_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG35_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG35_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.66 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36 Register

14.2.1.2.1.2.2.66.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36 Register (Offset = 4090h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6359. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4090h

Figure 14-3165. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36 Name Register

31	30	29	28	27	26	25	24
PADCONFIG36_LOCK	PADCONFIG36_WKUP_EVT	PADCONFIG36_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG36_ISO_BYP	PADCONFIG36_ISO_OVR	PADCONFIG36_TX_DIS	PADCONFIG36_DRV_STR		PADCONFIG36_RXACTIVE	PADCONFIG36_PULLTYPESEL	PADCONFIG36_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG36_ST_EN	PADCONFIG36_DEBOUNCE_SEL			RESERVED		PADCONFIG36_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG36_WK_LVL_EN	RESERVED			PADCONFIG36_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6360. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG36_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG36_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG36_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG36_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG36_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG36_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6360. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG36_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG36_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG36_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG36_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG36_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG36_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG36_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG36_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG36_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.67 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37 Register

14.2.1.2.1.2.2.67.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37 Register (Offset = 4094h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6361. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4094h

Figure 14-3166. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37 Name Register

31	30	29	28	27	26	25	24
PADCONFIG37_LOCK	PADCONFIG37_WKUP_EVT	PADCONFIG37_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG37_ISO_BYP	PADCONFIG37_ISO_OVR	PADCONFIG37_TX_DIS	PADCONFIG37_DRV_STR		PADCONFIG37_RXACTIVE	PADCONFIG37_PULLTYPESEL	PADCONFIG37_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG37_ST_EN	PADCONFIG37_DEBOUNCE_SEL			RESERVED		PADCONFIG37_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG37_WK_LVL_EN	RESERVED			PADCONFIG37_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6362. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG37_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG37_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG37_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG37_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG37_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG37_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6362. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG37_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG37_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG37_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG37_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG37_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG37_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG37_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG37_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG37_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.68 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38 Register

14.2.1.2.1.2.2.68.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38 Register (Offset = 4098h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6363. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4098h

Figure 14-3167. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38 Name Register

31	30	29	28	27	26	25	24
PADCONFIG38_LOCK	PADCONFIG38_WKUP_EVT	PADCONFIG38_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG38_ISO_BYP	PADCONFIG38_ISO_OVR	PADCONFIG38_TX_DIS	PADCONFIG38_DRV_STR		PADCONFIG38_RXACTIVE	PADCONFIG38_PULLTYPESEL	PADCONFIG38_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG38_ST_EN	PADCONFIG38_DEBOUNCE_SEL			RESERVED		PADCONFIG38_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG38_WK_LVL_EN	RESERVED			PADCONFIG38_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6364. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG38_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG38_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG38_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG38_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG38_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG38_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6364. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG38_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG38_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG38_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG38_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG38_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG38_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG38_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG38_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG38_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.69 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39 Register

14.2.1.2.1.2.2.69.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39 Register (Offset = 409Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6365. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 409Ch

Figure 14-3168. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39 Name Register

31	30	29	28	27	26	25	24
PADCONFIG39_LOCK	PADCONFIG39_WKUP_EVT	PADCONFIG39_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG39_ISO_BYP	PADCONFIG39_ISO_OVR	PADCONFIG39_TX_DIS	PADCONFIG39_DRV_STR		PADCONFIG39_RXACTIVE	PADCONFIG39_PULLTYPESEL	PADCONFIG39_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG39_ST_EN	PADCONFIG39_DEBOUNCE_SEL			RESERVED		PADCONFIG39_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG39_WK_LVL_EN	RESERVED			PADCONFIG39_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6366. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG39_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG39_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG39_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG39_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG39_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG39_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6366. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG39_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG39_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG39_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG39_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG39_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG39_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG39_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG39_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG39_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.70 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40 Register

14.2.1.2.1.2.2.70.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40 Register (Offset = 40A0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6367. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40A0h

Figure 14-3169. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40 Name Register

31	30	29	28	27	26	25	24
PADCONFIG40_LOCK	PADCONFIG40_WKUP_EVT	PADCONFIG40_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG40_ISO_BYP	PADCONFIG40_ISO_OVR	PADCONFIG40_TX_DIS	PADCONFIG40_DRV_STR		PADCONFIG40_RXACTIVE	PADCONFIG40_PULLTYPESEL	PADCONFIG40_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG40_ST_EN	PADCONFIG40_DEBOUNCE_SEL			RESERVED		PADCONFIG40_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG40_WK_LVL_EN	RESERVED			PADCONFIG40_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6368. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG40_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG40_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG40_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG40_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG40_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG40_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6368. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG40_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG40_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG40_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG40_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG40_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG40_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG40_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG40_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG40_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.71 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41 Register

14.2.1.2.1.2.2.71.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41 Register (Offset = 40A4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6369. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40A4h

Figure 14-3170. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41 Name Register

31	30	29	28	27	26	25	24
PADCONFIG41_LOCK	PADCONFIG41_WKUP_EVT	PADCONFIG41_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG41_ISO_BYP	PADCONFIG41_ISO_OVR	PADCONFIG41_TX_DIS	PADCONFIG41_DRV_STR		PADCONFIG41_RXACTIVE	PADCONFIG41_PULLTYPESEL	PADCONFIG41_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG41_ST_EN	PADCONFIG41_DEBOUNCE_SEL			RESERVED		PADCONFIG41_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG41_WK_LVL_EN	RESERVED			PADCONFIG41_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6370. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG41_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG41_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG41_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG41_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG41_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG41_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6370. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG41_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG41_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG41_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG41_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG41_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG41_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG41_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG41_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG41_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.72 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42 Register

14.2.1.2.1.2.2.72.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42 Register (Offset = 40A8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6371. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40A8h

Figure 14-3171. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42 Name Register

31	30	29	28	27	26	25	24
PADCONFIG42_LOCK	PADCONFIG42_WKUP_EVT	PADCONFIG42_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG42_ISO_BYP	PADCONFIG42_ISO_OVR	PADCONFIG42_TX_DIS	PADCONFIG42_DRV_STR		PADCONFIG42_RXACTIVE	PADCONFIG42_PULLTYPESEL	PADCONFIG42_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG42_ST_EN	PADCONFIG42_DEBOUNCE_SEL			RESERVED		PADCONFIG42_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG42_WK_LVL_EN	RESERVED			PADCONFIG42_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6372. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG42_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG42_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG42_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG42_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG42_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG42_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6372. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG42_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG42_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG42_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG42_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG42_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG42_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG42_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG42_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG42_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.73 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43 Register

14.2.1.2.1.2.2.73.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43 Register (Offset = 40ACh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6373. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40ACh

Figure 14-3172. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43 Name Register

31	30	29	28	27	26	25	24
PADCONFIG43_LOCK	PADCONFIG43_WKUP_EVT	PADCONFIG43_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG43_ISO_BYP	PADCONFIG43_ISO_OVR	PADCONFIG43_TX_DIS	PADCONFIG43_DRV_STR		PADCONFIG43_RXACTIVE	PADCONFIG43_PULLTYPESEL	PADCONFIG43_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG43_ST_EN	PADCONFIG43_DEBOUNCE_SEL			RESERVED		PADCONFIG43_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG43_WK_LVL_EN	RESERVED			PADCONFIG43_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6374. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG43_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG43_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG43_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG43_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG43_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG43_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6374. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG43_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG43_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG43_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG43_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG43_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG43_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG43_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG43_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG43_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.74 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44 Register

14.2.1.2.1.2.2.74.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44 Register (Offset = 40B0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6375. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40B0h

Figure 14-3173. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44 Name Register

31	30	29	28	27	26	25	24
PADCONFIG44_LOCK	PADCONFIG44_WKUP_EVT	PADCONFIG44_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG44_ISO_BYP	PADCONFIG44_ISO_OVR	PADCONFIG44_TX_DIS	PADCONFIG44_DRV_STR		PADCONFIG44_RXACTIVE	PADCONFIG44_PULLTYPESEL	PADCONFIG44_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG44_ST_EN	PADCONFIG44_DEBOUNCE_SEL			RESERVED		PADCONFIG44_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG44_WK_LVL_EN	RESERVED			PADCONFIG44_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6376. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG44_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG44_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG44_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG44_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG44_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG44_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6376. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG44_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG44_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG44_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG44_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG44_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG44_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG44_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG44_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG44_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.75 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45 Register

14.2.1.2.1.2.2.75.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45 Register (Offset = 40B4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6377. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40B4h

Figure 14-3174. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45 Name Register

31	30	29	28	27	26	25	24
PADCONFIG45_LOCK	PADCONFIG45_WKUP_EVT	PADCONFIG45_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG45_ISO_BYP	PADCONFIG45_ISO_OVR	PADCONFIG45_TX_DIS	PADCONFIG45_DRV_STR		PADCONFIG45_RXACTIVE	PADCONFIG45_PULLTYPESEL	PADCONFIG45_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG45_ST_EN	PADCONFIG45_DEBOUNCE_SEL			RESERVED		PADCONFIG45_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG45_WK_LVL_EN	RESERVED			PADCONFIG45_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6378. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG45_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG45_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG45_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG45_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG45_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG45_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6378. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG45_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG45_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG45_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG45_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG45_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG45_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG45_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG45_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG45_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.76 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46 Register

14.2.1.2.1.2.2.76.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46 Register (Offset = 40B8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6379. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40B8h

Figure 14-3175. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46 Name Register

31	30	29	28	27	26	25	24
PADCONFIG46_LOCK	PADCONFIG46_WKUP_EVT	PADCONFIG46_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG46_ISO_BYP	PADCONFIG46_ISO_OVR	PADCONFIG46_TX_DIS	PADCONFIG46_DRV_STR		PADCONFIG46_RXACTIVE	PADCONFIG46_PULLTYPESEL	PADCONFIG46_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG46_ST_EN	PADCONFIG46_DEBOUNCE_SEL			RESERVED		PADCONFIG46_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG46_WK_LVL_EN	RESERVED			PADCONFIG46_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6380. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG46_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG46_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG46_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG46_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG46_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG46_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6380. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG46_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG46_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG46_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG46_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG46_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG46_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG46_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG46_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG46_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.77 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47 Register

14.2.1.2.1.2.2.77.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47 Register (Offset = 40BCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6381. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40BCh

Figure 14-3176. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47 Name Register

31	30	29	28	27	26	25	24
PADCONFIG47_LOCK	PADCONFIG47_WKUP_EVT	PADCONFIG47_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG47_ISO_BYP	PADCONFIG47_ISO_OVR	PADCONFIG47_TX_DIS	PADCONFIG47_DRV_STR		PADCONFIG47_RXACTIVE	PADCONFIG47_PULLTYPESEL	PADCONFIG47_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG47_ST_EN	PADCONFIG47_DEBOUNCE_SEL			RESERVED		PADCONFIG47_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG47_WK_LVL_EN	RESERVED			PADCONFIG47_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6382. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG47_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG47_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG47_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG47_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG47_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG47_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6382. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG47_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG47_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG47_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG47_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG47_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG47_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG47_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG47_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG47_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.78 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48 Register

14.2.1.2.1.2.2.78.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48 Register (Offset = 40C0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6383. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40C0h

Figure 14-3177. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48 Name Register

31	30	29	28	27	26	25	24
PADCONFIG48_LOCK	PADCONFIG48_WKUP_EVT	PADCONFIG48_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG48_ISO_BYP	PADCONFIG48_ISO_OVR	PADCONFIG48_TX_DIS	PADCONFIG48_DRV_STR		PADCONFIG48_RXACTIVE	PADCONFIG48_PULLTYPESEL	PADCONFIG48_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG48_ST_EN	PADCONFIG48_DEBOUNCE_SEL			RESERVED		PADCONFIG48_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG48_WK_LVL_EN	RESERVED			PADCONFIG48_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6384. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG48_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG48_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG48_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG48_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG48_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG48_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6384. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG48_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG48_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG48_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG48_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG48_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG48_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG48_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG48_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG48_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.79 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49 Register

14.2.1.2.1.2.2.79.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49 Register (Offset = 40C4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6385. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40C4h

Figure 14-3178. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49 Name Register

31	30	29	28	27	26	25	24
PADCONFIG49_LOCK	PADCONFIG49_WKUP_EVT	PADCONFIG49_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG49_ISO_BYP	PADCONFIG49_ISO_OVR	PADCONFIG49_TX_DIS	PADCONFIG49_DRV_STR		PADCONFIG49_RXACTIVE	PADCONFIG49_PULLTYPESEL	PADCONFIG49_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG49_ST_EN	PADCONFIG49_DEBOUNCE_SEL			RESERVED		PADCONFIG49_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG49_WK_LVL_EN	RESERVED			PADCONFIG49_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6386. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG49_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG49_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG49_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG49_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG49_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG49_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6386. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG49_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG49_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG49_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG49_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG49_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG49_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG49_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG49_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG49_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.80 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50 Register

14.2.1.2.1.2.2.80.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50 Register (Offset = 40C8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6387. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40C8h

Figure 14-3179. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50 Name Register

31	30	29	28	27	26	25	24
PADCONFIG50_LOCK	PADCONFIG50_WKUP_EVT	PADCONFIG50_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG50_ISO_BYP	PADCONFIG50_ISO_OVR	PADCONFIG50_TX_DIS	PADCONFIG50_DRV_STR		PADCONFIG50_RXACTIVE	PADCONFIG50_PULLTYPESEL	PADCONFIG50_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG50_ST_EN	PADCONFIG50_DEBOUNCE_SEL			RESERVED		PADCONFIG50_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG50_WK_LVL_EN	RESERVED			PADCONFIG50_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6388. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG50_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG50_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG50_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG50_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG50_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG50_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6388. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG50_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG50_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG50_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG50_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG50_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG50_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG50_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG50_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG50_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.81 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51 Register

14.2.1.2.1.2.2.81.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51 Register (Offset = 40CCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6389. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40CCh

Figure 14-3180. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51 Name Register

31	30	29	28	27	26	25	24
PADCONFIG51_LOCK	PADCONFIG51_WKUP_EVT	PADCONFIG51_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG51_ISO_BYP	PADCONFIG51_ISO_OVR	PADCONFIG51_TX_DIS	PADCONFIG51_DRV_STR		PADCONFIG51_RXACTIVE	PADCONFIG51_PULLTYPESEL	PADCONFIG51_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG51_ST_EN	PADCONFIG51_DEBOUNCE_SEL			RESERVED		PADCONFIG51_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG51_WK_LVL_EN	RESERVED			PADCONFIG51_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6390. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG51_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG51_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG51_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG51_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG51_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG51_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6390. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG51_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG51_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG51_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG51_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG51_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG51_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG51_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG51_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG51_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.82 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52 Register

14.2.1.2.1.2.2.82.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52 Register (Offset = 40D0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6391. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40D0h

Figure 14-3181. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52 Name Register

31	30	29	28	27	26	25	24
PADCONFIG52_LOCK	PADCONFIG52_WKUP_EVT	PADCONFIG52_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG52_ISO_BYP	PADCONFIG52_ISO_OVR	PADCONFIG52_TX_DIS	PADCONFIG52_DRV_STR		PADCONFIG52_RXACTIVE	PADCONFIG52_PULLTYPESEL	PADCONFIG52_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG52_ST_EN	PADCONFIG52_DEBOUNCE_SEL			RESERVED		PADCONFIG52_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG52_WK_LVL_EN	RESERVED			PADCONFIG52_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6392. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG52_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG52_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG52_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG52_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG52_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG52_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6392. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG52_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG52_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG52_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG52_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG52_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG52_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG52_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG52_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG52_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.83 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53 Register

14.2.1.2.1.2.2.83.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53 Register (Offset = 40D4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6393. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40D4h

Figure 14-3182. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53 Name Register

31	30	29	28	27	26	25	24
PADCONFIG53_LOCK	PADCONFIG53_WKUP_EVT	PADCONFIG53_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG53_ISO_BYP	PADCONFIG53_ISO_OVR	PADCONFIG53_TX_DIS	PADCONFIG53_DRV_STR		PADCONFIG53_RXACTIVE	PADCONFIG53_PULLTYPESEL	PADCONFIG53_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG53_ST_EN	PADCONFIG53_DEBOUNCE_SEL			RESERVED		PADCONFIG53_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG53_WK_LVL_EN	RESERVED			PADCONFIG53_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6394. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG53_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG53_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG53_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG53_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG53_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG53_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6394. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG53_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG53_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG53_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG53_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG53_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG53_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG53_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG53_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG53_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.84 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56 Register

14.2.1.2.1.2.2.84.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56 Register (Offset = 40E0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6395. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40E0h

Figure 14-3183. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56 Name Register

31	30	29	28	27	26	25	24
PADCONFIG56_LOCK	PADCONFIG56_WKUP_EVT	PADCONFIG56_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG56_ISO_BYP	PADCONFIG56_ISO_OVR	PADCONFIG56_TX_DIS	PADCONFIG56_DRV_STR		PADCONFIG56_RXACTIVE	PADCONFIG56_PULLTYPESEL	PADCONFIG56_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG56_ST_EN	PADCONFIG56_DEBOUNCE_SEL			RESERVED		PADCONFIG56_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG56_WK_LVL_EN	RESERVED			PADCONFIG56_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6396. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG56_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG56_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG56_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG56_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG56_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG56_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6396. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG56_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG56_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG56_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG56_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG56_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG56_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG56_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG56_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG56_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.85 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57 Register

14.2.1.2.1.2.2.85.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57 Register (Offset = 40E4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6397. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40E4h

Figure 14-3184. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57 Name Register

31	30	29	28	27	26	25	24
PADCONFIG57_LOCK	PADCONFIG57_WKUP_EVT	PADCONFIG57_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG57_ISO_BYP	PADCONFIG57_ISO_OVR	PADCONFIG57_TX_DIS	PADCONFIG57_DRV_STR		PADCONFIG57_RXACTIVE	PADCONFIG57_PULLTYPESEL	PADCONFIG57_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG57_ST_EN	PADCONFIG57_DEBOUNCE_SEL			RESERVED		PADCONFIG57_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG57_WK_LVL_EN	RESERVED			PADCONFIG57_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6398. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG57_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG57_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG57_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG57_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG57_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG57_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6398. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG57_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG57_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG57_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG57_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG57_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG57_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG57_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG57_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG57_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.86 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58 Register

14.2.1.2.1.2.2.86.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58 Register (Offset = 40E8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6399. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40E8h

Figure 14-3185. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58 Name Register

31	30	29	28	27	26	25	24
PADCONFIG58_LOCK	PADCONFIG58_WKUP_EVT	PADCONFIG58_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG58_ISO_BYP	PADCONFIG58_ISO_OVR	PADCONFIG58_TX_DIS	PADCONFIG58_DRV_STR		PADCONFIG58_RXACTIVE	PADCONFIG58_PULLTYPESEL	PADCONFIG58_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG58_ST_EN	PADCONFIG58_DEBOUNCE_SEL			RESERVED		PADCONFIG58_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG58_WK_LVL_EN	RESERVED			PADCONFIG58_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6400. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG58_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG58_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG58_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG58_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG58_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG58_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6400. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG58_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG58_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG58_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG58_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG58_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG58_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG58_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG58_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG58_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.87 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59 Register

14.2.1.2.1.2.2.87.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59 Register (Offset = 40ECh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6401. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40ECh

Figure 14-3186. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59 Name Register

31	30	29	28	27	26	25	24
PADCONFIG59_LOCK	PADCONFIG59_WKUP_EVT	PADCONFIG59_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG59_ISO_BYP	PADCONFIG59_ISO_OVR	PADCONFIG59_TX_DIS	PADCONFIG59_DRV_STR		PADCONFIG59_RXACTIVE	PADCONFIG59_PULLTYPESEL	PADCONFIG59_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG59_ST_EN	PADCONFIG59_DEBOUNCE_SEL			RESERVED		PADCONFIG59_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG59_WK_LVL_EN	RESERVED			PADCONFIG59_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6402. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG59_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG59_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG59_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG59_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG59_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG59_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6402. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG59_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG59_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG59_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG59_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG59_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG59_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG59_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG59_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG59_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.88 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60 Register

14.2.1.2.1.2.2.88.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60 Register (Offset = 40F0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6403. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40F0h

Figure 14-3187. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60 Name Register

31	30	29	28	27	26	25	24
PADCONFIG60_LOCK	PADCONFIG60_WKUP_EVT	PADCONFIG60_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG60_ISO_BYP	PADCONFIG60_ISO_OVR	PADCONFIG60_TX_DIS	PADCONFIG60_DRV_STR		PADCONFIG60_RXACTIVE	PADCONFIG60_PULLTYPESEL	PADCONFIG60_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG60_ST_EN	PADCONFIG60_DEBOUNCE_SEL			RESERVED		PADCONFIG60_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG60_WK_LVL_EN	RESERVED			PADCONFIG60_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6404. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG60_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG60_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG60_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG60_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG60_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG60_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6404. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG60_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG60_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG60_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG60_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG60_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG60_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG60_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG60_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG60_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.89 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63 Register

14.2.1.2.1.2.2.89.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63 Register (Offset = 40FCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6405. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 40FCh

Figure 14-3188. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63 Name Register

31	30	29	28	27	26	25	24
PADCONFIG63_LOCK	PADCONFIG63_WKUP_EVT	PADCONFIG63_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG63_ISO_BYP	PADCONFIG63_ISO_OVR	PADCONFIG63_TX_DIS	PADCONFIG63_DRV_STR		PADCONFIG63_RXACTIVE	PADCONFIG63_PULLTYPESEL	PADCONFIG63_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG63_ST_EN	PADCONFIG63_DEBOUNCE_SEL			RESERVED		PADCONFIG63_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG63_WK_LVL_EN	RESERVED			PADCONFIG63_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6406. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG63_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG63_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG63_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG63_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG63_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG63_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6406. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG63_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG63_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG63_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG63_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG63_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG63_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG63_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG63_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG63_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.90 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64 Register

14.2.1.2.1.2.2.90.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64 Register (Offset = 4100h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6407. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4100h

Figure 14-3189. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64 Name Register

31	30	29	28	27	26	25	24
PADCONFIG64_LOCK	PADCONFIG64_WKUP_EVT	PADCONFIG64_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG64_ISO_BYP	PADCONFIG64_ISO_OVR	PADCONFIG64_TX_DIS	PADCONFIG64_DRV_STR		PADCONFIG64_RXACTIVE	PADCONFIG64_PULLTYPESEL	PADCONFIG64_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG64_ST_EN	PADCONFIG64_DEBOUNCE_SEL			RESERVED		PADCONFIG64_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG64_WK_LVL_EN	RESERVED			PADCONFIG64_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6408. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG64_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG64_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG64_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG64_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG64_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG64_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6408. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG64_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG64_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG64_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG64_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG64_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG64_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG64_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG64_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG64_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.91 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65 Register

14.2.1.2.1.2.2.91.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65 Register (Offset = 4104h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6409. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4104h

Figure 14-3190. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65 Name Register

31	30	29	28	27	26	25	24
PADCONFIG65_LOCK	PADCONFIG65_WKUP_EVT	PADCONFIG65_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG65_ISO_BYP	PADCONFIG65_ISO_OVR	PADCONFIG65_TX_DIS	PADCONFIG65_DRV_STR		PADCONFIG65_RXACTIVE	PADCONFIG65_PULLTYPESEL	PADCONFIG65_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG65_ST_EN	PADCONFIG65_DEBOUNCE_SEL			RESERVED		PADCONFIG65_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG65_WK_LVL_EN	RESERVED			PADCONFIG65_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6410. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG65_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG65_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG65_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG65_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG65_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG65_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6410. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG65_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG65_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG65_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG65_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG65_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG65_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG65_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG65_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG65_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.92 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66 Register

14.2.1.2.1.2.2.92.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66 Register (Offset = 4108h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6411. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4108h

Figure 14-3191. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66 Name Register

31	30	29	28	27	26	25	24
PADCONFIG66_LOCK	PADCONFIG66_WKUP_EVT	PADCONFIG66_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG66_ISO_BYP	PADCONFIG66_ISO_OVR	PADCONFIG66_TX_DIS	PADCONFIG66_DRV_STR		PADCONFIG66_RXACTIVE	PADCONFIG66_PULLTYPESEL	PADCONFIG66_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG66_ST_EN	PADCONFIG66_DEBOUNCE_SEL			RESERVED		PADCONFIG66_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG66_WK_LVL_EN	RESERVED			PADCONFIG66_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6412. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG66_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG66_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG66_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG66_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG66_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG66_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6412. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG66_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG66_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG66_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG66_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG66_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG66_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG66_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG66_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG66_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.93 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67 Register

14.2.1.2.1.2.2.93.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67 Register (Offset = 410Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6413. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 410Ch

Figure 14-3192. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67 Name Register

31	30	29	28	27	26	25	24
PADCONFIG67_LOCK	PADCONFIG67_WKUP_EVT	PADCONFIG67_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG67_ISO_BYP	PADCONFIG67_ISO_OVR	PADCONFIG67_TX_DIS	PADCONFIG67_DRV_STR		PADCONFIG67_RXACTIVE	PADCONFIG67_PULLTYPESEL	PADCONFIG67_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG67_ST_EN	PADCONFIG67_DEBOUNCE_SEL			RESERVED		PADCONFIG67_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG67_WK_LVL_EN	RESERVED			PADCONFIG67_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6414. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG67_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG67_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG67_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG67_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG67_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG67_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6414. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG67_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG67_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG67_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG67_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG67_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG67_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG67_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG67_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG67_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.94 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68 Register

14.2.1.2.1.2.2.94.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68 Register (Offset = 4110h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6415. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4110h

Figure 14-3193. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68 Name Register

31	30	29	28	27	26	25	24
PADCONFIG68_LOCK	PADCONFIG68_WKUP_EVT	PADCONFIG68_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG68_ISO_BYP	PADCONFIG68_ISO_OVR	PADCONFIG68_TX_DIS	PADCONFIG68_DRV_STR		PADCONFIG68_RXACTIVE	PADCONFIG68_PULLTYPESEL	PADCONFIG68_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG68_ST_EN	PADCONFIG68_DEBOUNCE_SEL			RESERVED		PADCONFIG68_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG68_WK_LVL_EN	RESERVED			PADCONFIG68_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6416. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG68_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG68_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG68_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG68_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG68_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG68_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6416. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG68_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG68_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG68_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG68_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG68_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG68_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG68_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG68_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG68_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.95 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69 Register

14.2.1.2.1.2.2.95.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69 Register (Offset = 4114h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6417. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4114h

Figure 14-3194. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69 Name Register

31	30	29	28	27	26	25	24
PADCONFIG69_LOCK	PADCONFIG69_WKUP_EVT	PADCONFIG69_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG69_ISO_BYP	PADCONFIG69_ISO_OVR	PADCONFIG69_TX_DIS	PADCONFIG69_DRV_STR		PADCONFIG69_RXACTIVE	PADCONFIG69_PULLTYPESEL	PADCONFIG69_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG69_ST_EN	PADCONFIG69_DEBOUNCE_SEL			RESERVED		PADCONFIG69_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG69_WK_LVL_EN	RESERVED			PADCONFIG69_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6418. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG69_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG69_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG69_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG69_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG69_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG69_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6418. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG69_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG69_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG69_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG69_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG69_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG69_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG69_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG69_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG69_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.96 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70 Register

14.2.1.2.1.2.2.96.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70 Register (Offset = 4118h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6419. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4118h

Figure 14-3195. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70 Name Register

31	30	29	28	27	26	25	24
PADCONFIG70_LOCK	PADCONFIG70_WKUP_EVT	PADCONFIG70_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG70_ISO_BYP	PADCONFIG70_ISO_OVR	PADCONFIG70_TX_DIS	PADCONFIG70_DRV_STR		PADCONFIG70_RXACTIVE	PADCONFIG70_PULLTYPESEL	PADCONFIG70_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG70_ST_EN	PADCONFIG70_DEBOUNCE_SEL			RESERVED		PADCONFIG70_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG70_WK_LVL_EN	RESERVED			PADCONFIG70_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6420. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG70_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG70_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG70_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG70_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG70_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG70_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6420. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG70_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG70_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG70_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG70_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG70_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG70_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG70_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG70_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG70_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.97 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71 Register

14.2.1.2.1.2.2.97.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71 Register (Offset = 411Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6421. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 411Ch

Figure 14-3196. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71 Name Register

31	30	29	28	27	26	25	24
PADCONFIG71_LOCK	PADCONFIG71_WKUP_EVT	PADCONFIG71_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG71_ISO_BYP	PADCONFIG71_ISO_OVR	PADCONFIG71_TX_DIS	PADCONFIG71_DRV_STR		PADCONFIG71_RXACTIVE	PADCONFIG71_PULLTYPESEL	PADCONFIG71_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG71_ST_EN	PADCONFIG71_DEBOUNCE_SEL			RESERVED		PADCONFIG71_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG71_WK_LVL_EN	RESERVED			PADCONFIG71_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6422. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG71_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG71_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG71_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG71_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG71_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG71_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6422. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG71_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG71_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG71_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG71_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG71_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG71_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG71_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG71_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG71_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.98 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72 Register

14.2.1.2.1.2.2.98.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72 Register (Offset = 4120h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6423. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4120h

Figure 14-3197. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72 Name Register

31	30	29	28	27	26	25	24
PADCONFIG72_LOCK	PADCONFIG72_WKUP_EVT	PADCONFIG72_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG72_ISO_BYP	PADCONFIG72_ISO_OVR	PADCONFIG72_TX_DIS	PADCONFIG72_DRV_STR		PADCONFIG72_RXACTIVE	PADCONFIG72_PULLTYPESEL	PADCONFIG72_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG72_ST_EN	PADCONFIG72_DEBOUNCE_SEL			RESERVED		PADCONFIG72_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG72_WK_LVL_EN	RESERVED			PADCONFIG72_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6424. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG72_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG72_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG72_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG72_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG72_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG72_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6424. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG72_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG72_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG72_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG72_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG72_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG72_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG72_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG72_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG72_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.99 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73 Register

14.2.1.2.1.2.2.99.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73 Register (Offset = 4124h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6425. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4124h

Figure 14-3198. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73 Name Register

31	30	29	28	27	26	25	24
PADCONFIG73_LOCK	PADCONFIG73_WKUP_EVT	PADCONFIG73_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG73_ISO_BYP	PADCONFIG73_ISO_OVR	PADCONFIG73_TX_DIS	PADCONFIG73_DRV_STR		PADCONFIG73_RXACTIVE	PADCONFIG73_PULLTYPESEL	PADCONFIG73_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG73_ST_EN	PADCONFIG73_DEBOUNCE_SEL			RESERVED		PADCONFIG73_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG73_WK_LVL_EN	RESERVED			PADCONFIG73_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6426. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG73_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG73_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG73_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG73_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG73_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG73_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6426. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG73_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG73_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG73_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG73_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG73_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG73_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG73_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG73_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG73_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.100 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74 Register

14.2.1.2.1.2.2.100.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74 Register (Offset = 4128h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6427. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4128h

Figure 14-3199. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74 Name Register

31	30	29	28	27	26	25	24
PADCONFIG74_LOCK	PADCONFIG74_WKUP_EVT	PADCONFIG74_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG74_ISO_BYP	PADCONFIG74_ISO_OVR	PADCONFIG74_TX_DIS	PADCONFIG74_DRV_STR		PADCONFIG74_RXACTIVE	PADCONFIG74_PULLTYPESEL	PADCONFIG74_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG74_ST_EN	PADCONFIG74_DEBOUNCE_SEL			RESERVED		PADCONFIG74_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG74_WK_LVL_EN	RESERVED			PADCONFIG74_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6428. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG74_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG74_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG74_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG74_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG74_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG74_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6428. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG74_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG74_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG74_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG74_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG74_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG74_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG74_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG74_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG74_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.101 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75 Register

14.2.1.2.1.2.2.101.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75 Register (Offset = 412Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6429. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 412Ch

Figure 14-3200. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75 Name Register

31	30	29	28	27	26	25	24
PADCONFIG75_LOCK	PADCONFIG75_WKUP_EVT	PADCONFIG75_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG75_ISO_BYP	PADCONFIG75_ISO_OVR	PADCONFIG75_TX_DIS	PADCONFIG75_DRV_STR		PADCONFIG75_RXACTIVE	PADCONFIG75_PULLTYPESEL	PADCONFIG75_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG75_ST_EN	PADCONFIG75_DEBOUNCE_SEL			RESERVED		PADCONFIG75_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG75_WK_LVL_EN	RESERVED			PADCONFIG75_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6430. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG75_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG75_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG75_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG75_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG75_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG75_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6430. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG75_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG75_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG75_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG75_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG75_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG75_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG75_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG75_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG75_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.102 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76 Register

14.2.1.2.1.2.2.102.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76 Register (Offset = 4130h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6431. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4130h

Figure 14-3201. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG76_LOCK</td><td>PADCONFIG76_WKUP_EVT</td><td>PADCONFIG76_WKUP_EN</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG76_ISO_BYP</td><td>PADCONFIG76_ISO_OVR</td><td>PADCONFIG76_TX_DIS</td><td colspan="2">PADCONFIG76_DRV_STR</td><td>PADCONFIG76_RXACTIVE</td><td>PADCONFIG76_PULLTYPESEL</td><td>PADCONFIG76_PULLUDEN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG76_ST_EN</td><td colspan="3">PADCONFIG76_DEBOUNCE_SEL</td><td colspan="2">RESERVED</td><td>PADCONFIG76_WK_LVL_POL</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG76_WK_LVL_EN</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG76_MUXMODE</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-6432. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG76_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG76_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG76_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG76_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG76_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG76_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6432. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG76_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG76_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG76_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG76_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG76_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG76_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG76_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG76_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG76_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.103 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77 Register

14.2.1.2.1.2.2.103.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77 Register (Offset = 4134h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6433. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4134h

Figure 14-3202. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77 Name Register

31	30	29	28	27	26	25	24
PADCONFIG77_LOCK	PADCONFIG77_WKUP_EVT	PADCONFIG77_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG77_ISO_BYP	PADCONFIG77_ISO_OVR	PADCONFIG77_TX_DIS	PADCONFIG77_DRV_STR		PADCONFIG77_RXACTIVE	PADCONFIG77_PULLTYPESEL	PADCONFIG77_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG77_ST_EN	PADCONFIG77_DEBOUNCE_SEL			RESERVED		PADCONFIG77_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG77_WK_LVL_EN	RESERVED			PADCONFIG77_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6434. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG77_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG77_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG77_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG77_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG77_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG77_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6434. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG77_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG77_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG77_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG77_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG77_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG77_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG77_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG77_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG77_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.104 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78 Register

14.2.1.2.1.2.2.104.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78 Register (Offset = 4138h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6435. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4138h

Figure 14-3203. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78 Name Register

31	30	29	28	27	26	25	24
PADCONFIG78_LOCK	PADCONFIG78_WKUP_EVT	PADCONFIG78_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG78_ISO_BYP	PADCONFIG78_ISO_OVR	PADCONFIG78_TX_DIS	PADCONFIG78_DRV_STR		PADCONFIG78_RXACTIVE	PADCONFIG78_PULLTYPESEL	PADCONFIG78_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG78_ST_EN	PADCONFIG78_DEBOUNCE_SEL			RESERVED		PADCONFIG78_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG78_WK_LVL_EN	RESERVED			PADCONFIG78_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6436. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG78_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG78_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG78_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG78_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG78_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG78_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6436. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG78_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG78_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG78_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG78_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG78_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG78_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG78_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG78_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG78_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.105 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79 Register

14.2.1.2.1.2.2.105.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79 Register (Offset = 413Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6437. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 413Ch

Figure 14-3204. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79 Name Register

31	30	29	28	27	26	25	24
PADCONFIG79_LOCK	PADCONFIG79_WKUP_EVT	PADCONFIG79_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG79_ISO_BYP	PADCONFIG79_ISO_OVR	PADCONFIG79_TX_DIS	PADCONFIG79_DRV_STR		PADCONFIG79_RXACTIVE	PADCONFIG79_PULLTYPESEL	PADCONFIG79_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG79_ST_EN	PADCONFIG79_DEBOUNCE_SEL			RESERVED		PADCONFIG79_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG79_WK_LVL_EN	RESERVED			PADCONFIG79_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6438. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG79_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG79_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG79_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG79_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG79_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG79_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6438. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG79_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG79_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG79_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG79_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG79_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG79_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG79_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG79_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG79_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.106 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80 Register

14.2.1.2.1.2.2.106.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80 Register (Offset = 4140h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6439. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4140h

Figure 14-3205. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80 Name Register

31	30	29	28	27	26	25	24
PADCONFIG80_LOCK	PADCONFIG80_WKUP_EVT	PADCONFIG80_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG80_ISO_BYP	PADCONFIG80_ISO_OVR	PADCONFIG80_TX_DIS	PADCONFIG80_DRV_STR		PADCONFIG80_RXACTIVE	PADCONFIG80_PULLTYPESEL	PADCONFIG80_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG80_ST_EN	PADCONFIG80_DEBOUNCE_SEL			RESERVED		PADCONFIG80_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG80_WK_LVL_EN	RESERVED			PADCONFIG80_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6440. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG80_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG80_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG80_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG80_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG80_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG80_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6440. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG80_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG80_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG80_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG80_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG80_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG80_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG80_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG80_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG80_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.107 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81 Register

14.2.1.2.1.2.2.107.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81 Register (Offset = 4144h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6441. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4144h

Figure 14-3206. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81 Name Register

31	30	29	28	27	26	25	24
PADCONFIG81_LOCK	PADCONFIG81_WKUP_EVT	PADCONFIG81_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG81_ISO_BYP	PADCONFIG81_ISO_OVR	PADCONFIG81_TX_DIS	PADCONFIG81_DRV_STR		PADCONFIG81_RXACTIVE	PADCONFIG81_PULLTYPESEL	PADCONFIG81_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG81_ST_EN	PADCONFIG81_DEBOUNCE_SEL			RESERVED		PADCONFIG81_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG81_WK_LVL_EN	RESERVED			PADCONFIG81_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6442. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG81_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG81_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG81_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG81_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG81_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG81_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6442. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG81_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG81_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG81_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG81_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG81_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG81_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG81_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG81_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG81_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.108 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82 Register

14.2.1.2.1.2.2.108.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82 Register (Offset = 4148h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6443. Instance Table

Instance Name	**Physical Address**
PADCFG_CTRL0	000F 4148h

Figure 14-3207. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82 Name Register

31	30	29	28	27	26	25	24
PADCONFIG82_LOCK	PADCONFIG82_WKUP_EVT	PADCONFIG82_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG82_ISO_BYP	PADCONFIG82_ISO_OVR	PADCONFIG82_TX_DIS	PADCONFIG82_DRV_STR		PADCONFIG82_RXACTIVE	PADCONFIG82_PULLTYPESEL	PADCONFIG82_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG82_ST_EN	PADCONFIG82_DEBOUNCE_SEL			RESERVED		PADCONFIG82_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG82_WK_LVL_EN	RESERVED			PADCONFIG82_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6444. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG82_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG82_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG82_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG82_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG82_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG82_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6444. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG82_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG82_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG82_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG82_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG82_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG82_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG82_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG82_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG82_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.109 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83 Register

14.2.1.2.1.2.2.109.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83 Register (Offset = 414Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6445. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 414Ch

Figure 14-3208. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83 Name Register

31	30	29	28	27	26	25	24
PADCONFIG83_LOCK	PADCONFIG83_WKUP_EVT	PADCONFIG83_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG83_ISO_BYP	PADCONFIG83_ISO_OVR	PADCONFIG83_TX_DIS	PADCONFIG83_DRV_STR		PADCONFIG83_RXACTIVE	PADCONFIG83_PULLTYPESEL	PADCONFIG83_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG83_ST_EN	PADCONFIG83_DEBOUNCE_SEL			RESERVED		PADCONFIG83_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG83_WK_LVL_EN	RESERVED			PADCONFIG83_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6446. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG83_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG83_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG83_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG83_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG83_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG83_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6446. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG83_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG83_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG83_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG83_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG83_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG83_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG83_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG83_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG83_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.110 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84 Register

14.2.1.2.1.2.2.110.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84 Register (Offset = 4150h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6447. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4150h

Figure 14-3209. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84 Name Register

31	30	29	28	27	26	25	24
PADCONFIG84_LOCK	PADCONFIG84_WKUP_EVT	PADCONFIG84_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG84_ISO_BYP	PADCONFIG84_ISO_OVR	PADCONFIG84_TX_DIS	PADCONFIG84_DRV_STR		PADCONFIG84_RXACTIVE	PADCONFIG84_PULLTYPESEL	PADCONFIG84_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG84_ST_EN	PADCONFIG84_DEBOUNCE_SEL			RESERVED		PADCONFIG84_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG84_WK_LVL_EN	RESERVED			PADCONFIG84_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6448. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG84_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG84_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG84_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG84_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG84_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG84_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6448. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG84_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG84_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG84_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG84_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG84_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG84_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG84_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG84_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG84_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.111 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85 Register

14.2.1.2.1.2.2.111.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85 Register (Offset = 4154h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6449. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4154h

Figure 14-3210. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85 Name Register

31	30	29	28	27	26	25	24
PADCONFIG85_LOCK	PADCONFIG85_WKUP_EVT	PADCONFIG85_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG85_ISO_BYP	PADCONFIG85_ISO_OVR	PADCONFIG85_TX_DIS	PADCONFIG85_DRV_STR		PADCONFIG85_RXACTIVE	PADCONFIG85_PULLTYPESEL	PADCONFIG85_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG85_ST_EN	PADCONFIG85_DEBOUNCE_SEL			RESERVED		PADCONFIG85_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG85_WK_LVL_EN	RESERVED			PADCONFIG85_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6450. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG85_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG85_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG85_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG85_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG85_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG85_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6450. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG85_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG85_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG85_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG85_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG85_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG85_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG85_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG85_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG85_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.112 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86 Register

14.2.1.2.1.2.2.112.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86 Register (Offset = 4158h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6451. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4158h

Figure 14-3211. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86 Name Register

31	30	29	28	27	26	25	24
PADCONFIG86_LOCK	PADCONFIG86_WKUP_EVT	PADCONFIG86_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG86_ISO_BYP	PADCONFIG86_ISO_OVR	PADCONFIG86_TX_DIS	PADCONFIG86_DRV_STR		PADCONFIG86_RXACTIVE	PADCONFIG86_PULLTYPESEL	PADCONFIG86_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG86_ST_EN	PADCONFIG86_DEBOUNCE_SEL			RESERVED		PADCONFIG86_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG86_WK_LVL_EN	RESERVED			PADCONFIG86_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6452. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG86_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG86_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG86_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG86_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG86_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG86_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6452. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG86_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG86_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG86_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG86_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG86_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG86_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG86_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG86_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG86_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.113 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87 Register

14.2.1.2.1.2.2.113.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87 Register (Offset = 415Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6453. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 415Ch

Figure 14-3212. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87 Name Register

31	30	29	28	27	26	25	24
PADCONFIG87_LOCK	PADCONFIG87_WKUP_EVT	PADCONFIG87_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG87_ISO_BYP	PADCONFIG87_ISO_OVR	PADCONFIG87_TX_DIS	PADCONFIG87_DRV_STR		PADCONFIG87_RXACTIVE	PADCONFIG87_PULLTYPESEL	PADCONFIG87_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG87_ST_EN	PADCONFIG87_DEBOUNCE_SEL			RESERVED		PADCONFIG87_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG87_WK_LVL_EN	RESERVED			PADCONFIG87_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6454. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG87_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG87_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG87_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG87_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG87_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG87_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6454. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG87_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG87_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG87_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG87_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG87_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG87_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG87_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG87_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG87_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.114 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88 Register

14.2.1.2.1.2.2.114.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88 Register (Offset = 4160h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6455. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4160h

Figure 14-3213. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88 Name Register

31	30	29	28	27	26	25	24
PADCONFIG88_LOCK	PADCONFIG88_WKUP_EVT	PADCONFIG88_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG88_ISO_BYP	PADCONFIG88_ISO_OVR	PADCONFIG88_TX_DIS	PADCONFIG88_DRV_STR		PADCONFIG88_RXACTIVE	PADCONFIG88_PULLTYPESEL	PADCONFIG88_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG88_ST_EN	PADCONFIG88_DEBOUNCE_SEL			RESERVED		PADCONFIG88_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG88_WK_LVL_EN	RESERVED			PADCONFIG88_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6456. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG88_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG88_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG88_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG88_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG88_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG88_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6456. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG88_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG88_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG88_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG88_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG88_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG88_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG88_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG88_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG88_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.115 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89 Register

14.2.1.2.1.2.2.115.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89 Register (Offset = 4164h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6457. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4164h

Figure 14-3214. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89 Name Register

31	30	29	28	27	26	25	24
PADCONFIG89_LOCK	PADCONFIG89_WKUP_EVT	PADCONFIG89_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG89_ISO_BYP	PADCONFIG89_ISO_OVR	PADCONFIG89_TX_DIS	PADCONFIG89_DRV_STR		PADCONFIG89_RXACTIVE	PADCONFIG89_PULLTYPESEL	PADCONFIG89_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG89_ST_EN	PADCONFIG89_DEBOUNCE_SEL			RESERVED		PADCONFIG89_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG89_WK_LVL_EN	RESERVED			PADCONFIG89_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6458. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG89_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG89_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG89_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG89_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG89_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG89_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6458. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG89_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG89_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG89_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG89_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG89_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG89_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG89_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG89_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG89_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.116 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90 Register

14.2.1.2.1.2.2.116.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90 Register (Offset = 4168h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6459. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4168h

Figure 14-3215. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90 Name Register

31	30	29	28	27	26	25	24
PADCONFIG90_LOCK	PADCONFIG90_WKUP_EVT	PADCONFIG90_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG90_ISO_BYP	PADCONFIG90_ISO_OVR	PADCONFIG90_TX_DIS	PADCONFIG90_DRV_STR		PADCONFIG90_RXACTIVE	PADCONFIG90_PULLTYPESEL	PADCONFIG90_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG90_ST_EN	PADCONFIG90_DEBOUNCE_SEL			RESERVED		PADCONFIG90_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG90_WK_LVL_EN	RESERVED			PADCONFIG90_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6460. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG90_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG90_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG90_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG90_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG90_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG90_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6460. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG90_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG90_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG90_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG90_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG90_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG90_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG90_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG90_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG90_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.117 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91 Register

14.2.1.2.1.2.2.117.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91 Register (Offset = 416Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6461. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 416Ch

Figure 14-3216. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91 Name Register

31	30	29	28	27	26	25	24
PADCONFIG91_LOCK	PADCONFIG91_WKUP_EVT	PADCONFIG91_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG91_ISO_BYP	PADCONFIG91_ISO_OVR	PADCONFIG91_TX_DIS	PADCONFIG91_DRV_STR		PADCONFIG91_RXACTIVE	PADCONFIG91_PULLTYPESEL	PADCONFIG91_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG91_ST_EN	PADCONFIG91_DEBOUNCE_SEL			RESERVED		PADCONFIG91_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG91_WK_LVL_EN	RESERVED			PADCONFIG91_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6462. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG91_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG91_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG91_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG91_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG91_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG91_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6462. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG91_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG91_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG91_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG91_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG91_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG91_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG91_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG91_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG91_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.118 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92 Register

14.2.1.2.1.2.2.118.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92 Register (Offset = 4170h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6463. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4170h

Figure 14-3217. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92 Name Register

31	30	29	28	27	26	25	24
PADCONFIG92_LOCK	PADCONFIG92_WKUP_EVT	PADCONFIG92_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG92_ISO_BYP	PADCONFIG92_ISO_OVR	PADCONFIG92_TX_DIS	PADCONFIG92_DRV_STR		PADCONFIG92_RXACTIVE	PADCONFIG92_PULLTYPESEL	PADCONFIG92_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG92_ST_EN	PADCONFIG92_DEBOUNCE_SEL			RESERVED		PADCONFIG92_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG92_WK_LVL_EN	RESERVED			PADCONFIG92_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6464. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG92_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG92_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG92_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG92_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG92_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG92_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6464. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG92_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG92_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG92_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG92_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG92_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG92_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG92_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG92_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG92_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.119 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93 Register

14.2.1.2.1.2.2.119.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93 Register (Offset = 4174h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6465. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4174h

Figure 14-3218. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG93_LOCK</td><td>PADCONFIG93_WKUP_EVT</td><td>PADCONFIG93_WKUP_EN</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG93_ISO_BYP</td><td>PADCONFIG93_ISO_OVR</td><td>PADCONFIG93_TX_DIS</td><td colspan="2">PADCONFIG93_DRV_STR</td><td>PADCONFIG93_RXACTIVE</td><td>PADCONFIG93_PULLTYPESEL</td><td>PADCONFIG93_PULLUDEN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG93_ST_EN</td><td colspan="3">PADCONFIG93_DEBOUNCE_SEL</td><td colspan="2">RESERVED</td><td>PADCONFIG93_WK_LVL_POL</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG93_WK_LVL_EN</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG93_MUXMODE</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-6466. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG93_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG93_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG93_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG93_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG93_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG93_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6466. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG93_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG93_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG93_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG93_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG93_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG93_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG93_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG93_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG93_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.120 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94 Register

14.2.1.2.1.2.2.120.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94 Register (Offset = 4178h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6467. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4178h

Figure 14-3219. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94 Name Register

31	30	29	28	27	26	25	24
PADCONFIG94_LOCK	PADCONFIG94_WKUP_EVT	PADCONFIG94_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG94_ISO_BYP	PADCONFIG94_ISO_OVR	PADCONFIG94_TX_DIS	PADCONFIG94_DRV_STR		PADCONFIG94_RXACTIVE	PADCONFIG94_PULLTYPESEL	PADCONFIG94_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG94_ST_EN	PADCONFIG94_DEBOUNCE_SEL			RESERVED		PADCONFIG94_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG94_WK_LVL_EN	RESERVED			PADCONFIG94_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6468. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG94_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG94_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG94_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG94_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG94_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG94_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6468. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG94_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG94_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG94_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG94_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG94_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG94_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG94_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG94_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG94_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.121 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95 Register

14.2.1.2.1.2.2.121.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95 Register (Offset = 417Ch) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6469. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 417Ch

Figure 14-3220. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95 Name Register

31	30	29	28	27	26	25	24
PADCONFIG95_LOCK	PADCONFIG95_WKUP_EVT	PADCONFIG95_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG95_ISO_BYP	PADCONFIG95_ISO_OVR	PADCONFIG95_TX_DIS	PADCONFIG95_DRV_STR		PADCONFIG95_RXACTIVE	PADCONFIG95_PULLTYPESEL	PADCONFIG95_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG95_ST_EN	PADCONFIG95_DEBOUNCE_SEL			RESERVED		PADCONFIG95_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG95_WK_LVL_EN	RESERVED			PADCONFIG95_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6470. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG95_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG95_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG95_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG95_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG95_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG95_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6470. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG95_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG95_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG95_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG95_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG95_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG95_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG95_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG95_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG95_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.122 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96 Register

14.2.1.2.1.2.2.122.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96 Register (Offset = 4180h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6471. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4180h

Figure 14-3221. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG96_LOCK</td><td>PADCONFIG96_WKUP_EVT</td><td>PADCONFIG96_WKUP_EN</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG96_ISO_BYP</td><td>PADCONFIG96_ISO_OVR</td><td>PADCONFIG96_TX_DIS</td><td colspan="2">PADCONFIG96_DRV_STR</td><td>PADCONFIG96_RXACTIVE</td><td>PADCONFIG96_PULLTYPESEL</td><td>PADCONFIG96_PULLUDEN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG96_ST_EN</td><td colspan="3">PADCONFIG96_DEBOUNCE_SEL</td><td colspan="2">RESERVED</td><td>PADCONFIG96_WK_LVL_POL</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG96_WK_LVL_EN</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG96_MUXMODE</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-6472. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG96_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG96_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG96_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG96_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG96_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG96_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6472. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG96_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG96_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG96_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG96_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG96_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG96_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG96_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG96_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG96_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.123 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97 Register

14.2.1.2.1.2.2.123.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97 Register (Offset = 4184h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6473. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4184h

Figure 14-3222. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97 Name Register

31	30	29	28	27	26	25	24
PADCONFIG97_LOCK	PADCONFIG97_WKUP_EVT	PADCONFIG97_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG97_ISO_BYP	PADCONFIG97_ISO_OVR	PADCONFIG97_TX_DIS	PADCONFIG97_DRV_STR		PADCONFIG97_RXACTIVE	PADCONFIG97_PULLTYPESEL	PADCONFIG97_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG97_ST_EN	PADCONFIG97_DEBOUNCE_SEL			RESERVED		PADCONFIG97_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG97_WK_LVL_EN	RESERVED			PADCONFIG97_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6474. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG97_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG97_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG97_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG97_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG97_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG97_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6474. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG97_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG97_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG97_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG97_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG97_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG97_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG97_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG97_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG97_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.124 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98 Register

14.2.1.2.1.2.2.124.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98 Register (Offset = 4188h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6475. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4188h

Figure 14-3223. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98 Name Register

31	30	29	28	27	26	25	24
PADCONFIG98_LOCK	PADCONFIG98_WKUP_EVT	PADCONFIG98_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG98_ISO_BYP	PADCONFIG98_ISO_OVR	PADCONFIG98_TX_DIS	PADCONFIG98_DRV_STR		PADCONFIG98_RXACTIVE	PADCONFIG98_PULLTYPESEL	PADCONFIG98_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG98_ST_EN	PADCONFIG98_DEBOUNCE_SEL			RESERVED		PADCONFIG98_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG98_WK_LVL_EN	RESERVED			PADCONFIG98_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6476. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG98_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG98_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG98_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG98_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG98_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG98_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6476. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG98_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG98_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG98_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG98_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG98_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG98_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG98_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG98_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG98_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.125 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99 Register

14.2.1.2.1.2.2.125.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99 Register (Offset = 418Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6477. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 418Ch

Figure 14-3224. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99 Name Register

31	30	29	28	27	26	25	24
PADCONFIG99_LOCK	PADCONFIG99_WKUP_EVT	PADCONFIG99_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG99_ISO_BYP	PADCONFIG99_ISO_OVR	PADCONFIG99_TX_DIS	PADCONFIG99_DRV_STR		PADCONFIG99_RXACTIVE	PADCONFIG99_PULLTYPESEL	PADCONFIG99_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG99_ST_EN	PADCONFIG99_DEBOUNCE_SEL			RESERVED		PADCONFIG99_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG99_WK_LVL_EN	RESERVED			PADCONFIG99_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6478. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG99_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG99_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG99_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG99_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG99_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n
21	PADCONFIG99_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n

Table 14-6478. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	PADCONFIG99_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG99_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG99_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG99_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG99_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG99_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG99_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG99_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG99_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.126 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100 Register

14.2.1.2.1.2.2.126.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100 Register (Offset = 4190h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6479. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4190h

Figure 14-3225. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100 Name Register

31	30	29	28	27	26	25	24
PADCONFIG100_LOCK	PADCONFIG100_WKUP_EVT	PADCONFIG100_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG100_ISO_BYP	PADCONFIG100_ISO_OVR	PADCONFIG100_TX_DIS	PADCONFIG100_DRV_STR		PADCONFIG100_RXACTIVE	PADCONFIG100_PULLTYPESEL	PADCONFIG100_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG100_ST_EN	PADCONFIG100_DEBOUNCE_SEL			RESERVED		PADCONFIG100_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG100_WK_LVL_EN	RESERVED			PADCONFIG100_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6480. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG100_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG100_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG100_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG100_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG100_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6480. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG100_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG100_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG100_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG100_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG100_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG100_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG100_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG100_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG100_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG100_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.127 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101 Register

14.2.1.2.1.2.2.127.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101 Register (Offset = 4194h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6481. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4194h

Figure 14-3226. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101 Name Register

31	30	29	28	27	26	25	24
PADCONFIG101_LOCK	PADCONFIG101_WKUP_EVT	PADCONFIG101_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG101_ISO_BYP	PADCONFIG101_ISO_OVR	PADCONFIG101_TX_DIS	PADCONFIG101_DRV_STR		PADCONFIG101_RXACTIVE	PADCONFIG101_PULLTYPESEL	PADCONFIG101_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG101_ST_EN	PADCONFIG101_DEBOUNCE_SEL			RESERVED		PADCONFIG101_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG101_WK_LVL_EN	RESERVED			PADCONFIG101_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6482. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG101_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG101_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG101_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG101_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG101_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6482. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG101_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG101_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG101_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG101_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG101_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG101_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG101_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG101_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG101_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG101_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.128 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102 Register

14.2.1.2.1.2.2.128.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102 Register (Offset = 4198h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6483. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4198h

Figure 14-3227. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102 Name Register

31	30	29	28	27	26	25	24
PADCONFIG102_LOCK	PADCONFIG102_WKUP_EVT	PADCONFIG102_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG102_ISO_BYP	PADCONFIG102_ISO_OVR	PADCONFIG102_TX_DIS	PADCONFIG102_DRV_STR		PADCONFIG102_RXACTIVE	PADCONFIG102_PULLTYPESEL	PADCONFIG102_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG102_ST_EN	PADCONFIG102_DEBOUNCE_SEL			RESERVED		PADCONFIG102_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG102_WK_LVL_EN	RESERVED			PADCONFIG102_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6484. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG102_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG102_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG102_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG102_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG102_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6484. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG102_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG102_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG102_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG102_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG102_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG102_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG102_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG102_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG102_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG102_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.129 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103 Register

14.2.1.2.1.2.2.129.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103 Register (Offset = 419Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6485. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 419Ch

Figure 14-3228. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103 Name Register

31	30	29	28	27	26	25	24
PADCONFIG103_LOCK	PADCONFIG103_WKUP_EVT	PADCONFIG103_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG103_ISO_BYP	PADCONFIG103_ISO_OVR	PADCONFIG103_TX_DIS	PADCONFIG103_DRV_STR		PADCONFIG103_RXACTIVE	PADCONFIG103_PULLTYPESEL	PADCONFIG103_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG103_ST_EN	PADCONFIG103_DEBOUNCE_SEL			RESERVED		PADCONFIG103_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG103_WK_LVL_EN	RESERVED			PADCONFIG103_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6486. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG103_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG103_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG103_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG103_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG103_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6486. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG103_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG103_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG103_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG103_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG103_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG103_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG103_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG103_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG103_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG103_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.130 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104 Register

14.2.1.2.1.2.2.130.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104 Register (Offset = 41A0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6487. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41A0h

Figure 14-3229. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104 Name Register

31	30	29	28	27	26	25	24
PADCONFIG104_LOCK	PADCONFIG104_WKUP_EVT	PADCONFIG104_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG104_ISO_BYP	PADCONFIG104_ISO_OVR	PADCONFIG104_TX_DIS	PADCONFIG104_DRV_STR		PADCONFIG104_RXACTIVE	PADCONFIG104_PULLTYPESEL	PADCONFIG104_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG104_ST_EN	PADCONFIG104_DEBOUNCE_SEL			RESERVED		PADCONFIG104_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG104_WK_LVL_EN	RESERVED			PADCONFIG104_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6488. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG104_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG104_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG104_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG104_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG104_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6488. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG104_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG104_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG104_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG104_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG104_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG104_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG104_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG104_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG104_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG104_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.131 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105 Register

14.2.1.2.1.2.2.131.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105 Register (Offset = 41A4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6489. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41A4h

Figure 14-3230. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105 Name Register

31	30	29	28	27	26	25	24
PADCONFIG105_LOCK	PADCONFIG105_WKUP_EVT	PADCONFIG105_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG105_ISO_BYP	PADCONFIG105_ISO_OVR	PADCONFIG105_TX_DIS	PADCONFIG105_DRV_STR		PADCONFIG105_RXACTIVE	PADCONFIG105_PULLTYPESEL	PADCONFIG105_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG105_ST_EN	PADCONFIG105_DEBOUNCE_SEL			RESERVED		PADCONFIG105_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG105_WK_LVL_EN	RESERVED			PADCONFIG105_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6490. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG105_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG105_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG105_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG105_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG105_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6490. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG105_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG105_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG105_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG105_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG105_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG105_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG105_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG105_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG105_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG105_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.132 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106 Register

14.2.1.2.1.2.2.132.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106 Register (Offset = 41A8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6491. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41A8h

Figure 14-3231. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106 Name Register

31	30	29	28	27	26	25	24
PADCONFIG106_LOCK	PADCONFIG106_WKUP_EVT	PADCONFIG106_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG106_ISO_BYP	PADCONFIG106_ISO_OVR	PADCONFIG106_TX_DIS	PADCONFIG106_DRV_STR		PADCONFIG106_RXACTIVE	PADCONFIG106_PULLTYPESEL	PADCONFIG106_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG106_ST_EN	PADCONFIG106_DEBOUNCE_SEL			RESERVED		PADCONFIG106_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG106_WK_LVL_EN	RESERVED			PADCONFIG106_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6492. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG106_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG106_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG106_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG106_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG106_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6492. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG106_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG106_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG106_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG106_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG106_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG106_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG106_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG106_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG106_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG106_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.133 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107 Register

14.2.1.2.1.2.2.133.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107 Register (Offset = 41ACh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6493. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41ACh

Figure 14-3232. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107 Name Register

31	30	29	28	27	26	25	24
PADCONFIG107_LOCK	PADCONFIG107_WKUP_EVT	PADCONFIG107_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG107_ISO_BYP	PADCONFIG107_ISO_OVR	PADCONFIG107_TX_DIS	PADCONFIG107_DRV_STR		PADCONFIG107_RXACTIVE	PADCONFIG107_PULLTYPESEL	PADCONFIG107_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG107_ST_EN	PADCONFIG107_DEBOUNCE_SEL			RESERVED		PADCONFIG107_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG107_WK_LVL_EN	RESERVED			PADCONFIG107_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6494. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG107_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG107_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG107_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG107_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG107_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6494. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG107_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG107_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG107_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG107_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG107_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG107_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG107_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG107_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG107_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG107_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.134 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108 Register

14.2.1.2.1.2.2.134.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108 Register (Offset = 41B0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6495. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41B0h

Figure 14-3233. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108 Name Register

31	30	29	28	27	26	25	24
PADCONFIG108_LOCK	PADCONFIG108_WKUP_EVT	PADCONFIG108_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG108_ISO_BYP	PADCONFIG108_ISO_OVR	PADCONFIG108_TX_DIS	PADCONFIG108_DRV_STR		PADCONFIG108_RXACTIVE	PADCONFIG108_PULLTYPESEL	PADCONFIG108_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG108_ST_EN	PADCONFIG108_DEBOUNCE_SEL			RESERVED		PADCONFIG108_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG108_WK_LVL_EN	RESERVED			PADCONFIG108_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6496. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG108_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG108_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG108_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG108_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG108_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6496. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG108_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG108_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG108_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG108_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG108_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG108_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG108_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG108_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG108_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG108_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.135 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109 Register

14.2.1.2.1.2.2.135.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109 Register (Offset = 41B4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6497. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41B4h

Figure 14-3234. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109 Name Register

31	30	29	28	27	26	25	24
PADCONFIG109_LOCK	PADCONFIG109_WKUP_EVT	PADCONFIG109_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG109_ISO_BYP	PADCONFIG109_ISO_OVR	PADCONFIG109_TX_DIS	PADCONFIG109_DRV_STR		PADCONFIG109_RXACTIVE	PADCONFIG109_PULLTYPESEL	PADCONFIG109_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG109_ST_EN	PADCONFIG109_DEBOUNCE_SEL			RESERVED		PADCONFIG109_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG109_WK_LVL_EN	RESERVED			PADCONFIG109_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6498. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG109_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG109_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG109_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG109_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG109_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6498. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG109_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG109_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG109_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG109_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG109_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG109_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG109_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG109_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG109_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG109_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.136 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110 Register

14.2.1.2.1.2.2.136.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110 Register (Offset = 41B8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6499. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41B8h

Figure 14-3235. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110 Name Register

31	30	29	28	27	26	25	24
PADCONFIG110_LOCK	PADCONFIG110_WKUP_EVT	PADCONFIG110_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG110_ISO_BYP	PADCONFIG110_ISO_OVR	PADCONFIG110_TX_DIS	PADCONFIG110_DRV_STR		PADCONFIG110_RXACTIVE	PADCONFIG110_PULLTYPESEL	PADCONFIG110_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG110_ST_EN	PADCONFIG110_DEBOUNCE_SEL			RESERVED		PADCONFIG110_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG110_WK_LVL_EN	RESERVED			PADCONFIG110_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6500. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG110_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG110_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG110_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG110_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG110_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6500. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG110_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG110_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG110_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG110_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG110_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG110_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG110_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG110_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG110_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG110_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.137 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111 Register

14.2.1.2.1.2.2.137.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111 Register (Offset = 41BCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6501. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41BCh

Figure 14-3236. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111 Name Register

31	30	29	28	27	26	25	24
PADCONFIG111_LOCK	PADCONFIG111_WKUP_EVT	PADCONFIG111_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG111_ISO_BYP	PADCONFIG111_ISO_OVR	PADCONFIG111_TX_DIS	PADCONFIG111_DRV_STR		PADCONFIG111_RXACTIVE	PADCONFIG111_PULLTYPESEL	PADCONFIG111_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG111_ST_EN	PADCONFIG111_DEBOUNCE_SEL			RESERVED		PADCONFIG111_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG111_WK_LVL_EN	RESERVED			PADCONFIG111_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6502. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG111_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG111_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG111_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG111_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG111_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6502. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG111_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG111_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG111_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG111_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG111_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG111_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG111_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG111_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG111_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG111_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.138 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112 Register

14.2.1.2.1.2.2.138.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112 Register (Offset = 41C0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6503. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41C0h

Figure 14-3237. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112 Name Register

31	30	29	28	27	26	25	24
PADCONFIG112_LOCK	PADCONFIG112_WKUP_EVT	PADCONFIG112_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG112_ISO_BYP	PADCONFIG112_ISO_OVR	PADCONFIG112_TX_DIS	PADCONFIG112_DRV_STR		PADCONFIG112_RXACTIVE	PADCONFIG112_PULLTYPESEL	PADCONFIG112_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG112_ST_EN	PADCONFIG112_DEBOUNCE_SEL			RESERVED		PADCONFIG112_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG112_WK_LVL_EN	RESERVED			PADCONFIG112_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6504. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG112_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG112_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG112_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG112_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG112_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6504. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG112_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG112_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG112_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG112_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG112_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG112_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG112_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG112_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG112_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG112_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.139 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113 Register

14.2.1.2.1.2.2.139.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113 Register (Offset = 41C4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6505. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41C4h

Figure 14-3238. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113 Name Register

31	30	29	28	27	26	25	24
PADCONFIG113_LOCK	PADCONFIG113_WKUP_EVT	PADCONFIG113_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG113_ISO_BYP	PADCONFIG113_ISO_OVR	PADCONFIG113_TX_DIS	PADCONFIG113_DRV_STR		PADCONFIG113_RXACTIVE	PADCONFIG113_PULLTYPESEL	PADCONFIG113_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG113_ST_EN	PADCONFIG113_DEBOUNCE_SEL			RESERVED		PADCONFIG113_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG113_WK_LVL_EN	RESERVED			PADCONFIG113_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6506. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG113_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG113_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG113_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG113_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG113_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6506. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG113_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG113_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG113_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG113_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG113_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG113_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG113_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG113_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG113_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG113_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.140 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114 Register

14.2.1.2.1.2.2.140.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114 Register (Offset = 41C8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6507. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41C8h

Figure 14-3239. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114 Name Register

31	30	29	28	27	26	25	24
PADCONFIG114_LOCK	PADCONFIG114_WKUP_EVT	PADCONFIG114_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG114_ISO_BYP	PADCONFIG114_ISO_OVR	PADCONFIG114_TX_DIS	PADCONFIG114_DRV_STR		PADCONFIG114_RXACTIVE	PADCONFIG114_PULLTYPESEL	PADCONFIG114_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG114_ST_EN	PADCONFIG114_DEBOUNCE_SEL			RESERVED		PADCONFIG114_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG114_WK_LVL_EN	RESERVED			PADCONFIG114_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6508. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG114_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG114_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG114_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG114_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG114_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6508. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG114_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG114_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG114_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG114_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG114_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG114_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG114_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG114_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG114_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG114_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.141 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115 Register

14.2.1.2.1.2.2.141.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115 Register (Offset = 41CCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6509. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41CCh

Figure 14-3240. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115 Name Register

31	30	29	28	27	26	25	24
PADCONFIG115_LOCK	PADCONFIG115_WKUP_EVT	PADCONFIG115_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG115_ISO_BYP	PADCONFIG115_ISO_OVR	PADCONFIG115_TX_DIS	PADCONFIG115_DRV_STR		PADCONFIG115_RXACTIVE	PADCONFIG115_PULLTYPESEL	PADCONFIG115_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG115_ST_EN	PADCONFIG115_DEBOUNCE_SEL			RESERVED		PADCONFIG115_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG115_WK_LVL_EN	RESERVED			PADCONFIG115_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6510. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG115_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG115_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG115_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG115_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG115_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6510. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG115_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG115_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG115_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG115_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG115_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG115_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG115_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG115_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG115_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG115_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.142 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116 Register

14.2.1.2.1.2.2.142.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116 Register (Offset = 41D0h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6511. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41D0h

Figure 14-3241. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116 Name Register

31	30	29	28	27	26	25	24
PADCONFIG116_LOCK	PADCONFIG116_WKUP_EVT	PADCONFIG116_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG116_ISO_BYP	PADCONFIG116_ISO_OVR	PADCONFIG116_TX_DIS	PADCONFIG116_DRV_STR		PADCONFIG116_RXACTIVE	PADCONFIG116_PULLTYPESEL	PADCONFIG116_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG116_ST_EN	PADCONFIG116_DEBOUNCE_SEL			RESERVED		PADCONFIG116_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG116_WK_LVL_EN	RESERVED			PADCONFIG116_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6512. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG116_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG116_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG116_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG116_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG116_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6512. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG116_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG116_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG116_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG116_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG116_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG116_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG116_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG116_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG116_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG116_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.143 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117 Register

14.2.1.2.1.2.2.143.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117 Register (Offset = 41D4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6513. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41D4h

Figure 14-3242. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117 Name Register

31	30	29	28	27	26	25	24
PADCONFIG117_LOCK	PADCONFIG117_WKUP_EVT	PADCONFIG117_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG117_ISO_BYP	PADCONFIG117_ISO_OVR	PADCONFIG117_TX_DIS	PADCONFIG117_DRV_STR		PADCONFIG117_RXACTIVE	PADCONFIG117_PULLTYPESEL	PADCONFIG117_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG117_ST_EN	PADCONFIG117_DEBOUNCE_SEL			RESERVED		PADCONFIG117_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG117_WK_LVL_EN	RESERVED			PADCONFIG117_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6514. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG117_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG117_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG117_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG117_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG117_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6514. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG117_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG117_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG117_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG117_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG117_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG117_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG117_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG117_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG117_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG117_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.144 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118 Register

14.2.1.2.1.2.2.144.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118 Register (Offset = 41D8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6515. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41D8h

Figure 14-3243. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118 Name Register

31	30	29	28	27	26	25	24
PADCONFIG118_LOCK	PADCONFIG118_WKUP_EVT	PADCONFIG118_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG118_ISO_BYP	PADCONFIG118_ISO_OVR	PADCONFIG118_TX_DIS	PADCONFIG118_DRV_STR		PADCONFIG118_RXACTIVE	PADCONFIG118_PULLTYPESEL	PADCONFIG118_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG118_ST_EN	PADCONFIG118_DEBOUNCE_SEL			RESERVED		PADCONFIG118_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG118_WK_LVL_EN	RESERVED			PADCONFIG118_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6516. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG118_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG118_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG118_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG118_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG118_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6516. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG118_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG118_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG118_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG118_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG118_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG118_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG118_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG118_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG118_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG118_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.145 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119 Register

14.2.1.2.1.2.2.145.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119 Register (Offset = 41DCh) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6517. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41DCh

Figure 14-3244. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG119_LOCK</td><td>PADCONFIG119_WKUP_EVT</td><td>PADCONFIG119_WKUP_EN</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG119_ISO_BYP</td><td>PADCONFIG119_ISO_OVR</td><td>PADCONFIG119_TX_DIS</td><td colspan="2">PADCONFIG119_DRV_STR</td><td>PADCONFIG119_RXACTIVE</td><td>PADCONFIG119_PULLTYPESEL</td><td>PADCONFIG119_PULLUDEN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG119_ST_EN</td><td colspan="3">PADCONFIG119_DEBOUNCE_SEL</td><td colspan="2">RESERVED</td><td>PADCONFIG119_WK_LVL_POL</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG119_WK_LVL_EN</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG119_MUXMODE</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-6518. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG119_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG119_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG119_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG119_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG119_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6518. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG119_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG119_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG119_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG119_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG119_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG119_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG119_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG119_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG119_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG119_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.146 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120 Register

14.2.1.2.1.2.2.146.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120 Register (Offset = 41E0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6519. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41E0h

Figure 14-3245. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120 Name Register

31	30	29	28	27	26	25	24
PADCONFIG120_LOCK	PADCONFIG120_WKUP_EVT	PADCONFIG120_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG120_ISO_BYP	PADCONFIG120_ISO_OVR	PADCONFIG120_TX_DIS	PADCONFIG120_DRV_STR		PADCONFIG120_RXACTIVE	PADCONFIG120_PULLTYPESEL	PADCONFIG120_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG120_ST_EN	PADCONFIG120_DEBOUNCE_SEL			RESERVED		PADCONFIG120_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG120_WK_LVL_EN	RESERVED			PADCONFIG120_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6520. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG120_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG120_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG120_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG120_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG120_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6520. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG120_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG120_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG120_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG120_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG120_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG120_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG120_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG120_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG120_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG120_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.147 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121 Register

14.2.1.2.1.2.2.147.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121 Register (Offset = 41E4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6521. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41E4h

Figure 14-3246. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG121_LOCK</td><td>PADCONFIG121_WKUP_EVT</td><td>PADCONFIG121_WKUP_EN</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG121_ISO_BYP</td><td>PADCONFIG121_ISO_OVR</td><td>PADCONFIG121_TX_DIS</td><td colspan="2">PADCONFIG121_DRV_STR</td><td>PADCONFIG121_RXACTIVE</td><td>PADCONFIG121_PULLTYPESEL</td><td>PADCONFIG121_PULLUDEN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG121_ST_EN</td><td colspan="3">PADCONFIG121_DEBOUNCE_SEL</td><td colspan="2">RESERVED</td><td>PADCONFIG121_WK_LVL_POL</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG121_WK_LVL_EN</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG121_MUXMODE</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-6522. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG121_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG121_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG121_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG121_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG121_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6522. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG121_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG121_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG121_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG121_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG121_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG121_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG121_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG121_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG121_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG121_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.148 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122 Register

14.2.1.2.1.2.2.148.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122 Register (Offset = 41E8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6523. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41E8h

Figure 14-3247. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122 Name Register

31	30	29	28	27	26	25	24
PADCONFIG122_LOCK	PADCONFIG122_WKUP_EVT	PADCONFIG122_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG122_ISO_BYP	PADCONFIG122_ISO_OVR	PADCONFIG122_TX_DIS	PADCONFIG122_DRV_STR		PADCONFIG122_RXACTIVE	PADCONFIG122_PULLTYPESEL	PADCONFIG122_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG122_ST_EN	PADCONFIG122_DEBOUNCE_SEL			RESERVED		PADCONFIG122_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG122_WK_LVL_EN	RESERVED			PADCONFIG122_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6524. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG122_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG122_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG122_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG122_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG122_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6524. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG122_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG122_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG122_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG122_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG122_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG122_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG122_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG122_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG122_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG122_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.149 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123 Register

14.2.1.2.1.2.2.149.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123 Register (Offset = 41ECh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6525. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41ECh

Figure 14-3248. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123 Name Register

31	30	29	28	27	26	25	24
PADCONFIG123_LOCK	PADCONFIG123_WKUP_EVT	PADCONFIG123_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG123_ISO_BYP	PADCONFIG123_ISO_OVR	PADCONFIG123_TX_DIS	PADCONFIG123_DRV_STR		PADCONFIG123_RXACTIVE	PADCONFIG123_PULLTYPESEL	PADCONFIG123_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG123_ST_EN	PADCONFIG123_DEBOUNCE_SEL			RESERVED		PADCONFIG123_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG123_WK_LVL_EN	RESERVED			PADCONFIG123_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6526. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG123_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG123_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG123_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG123_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG123_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6526. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG123_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG123_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG123_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG123_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG123_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG123_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG123_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG123_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG123_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG123_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.150 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124 Register

14.2.1.2.1.2.2.150.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124 Register (Offset = 41F0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6527. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41F0h

Figure 14-3249. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124 Name Register

31	30	29	28	27	26	25	24
PADCONFIG124_LOCK	PADCONFIG124_WKUP_EVT	PADCONFIG124_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG124_ISO_BYP	PADCONFIG124_ISO_OVR	PADCONFIG124_TX_DIS	PADCONFIG124_DRV_STR		PADCONFIG124_RXACTIVE	PADCONFIG124_PULLTYPESEL	PADCONFIG124_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG124_ST_EN	PADCONFIG124_DEBOUNCE_SEL			RESERVED		PADCONFIG124_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG124_WK_LVL_EN	RESERVED			PADCONFIG124_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6528. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG124_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG124_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG124_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG124_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG124_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6528. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG124_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG124_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG124_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG124_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG124_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG124_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG124_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG124_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG124_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG124_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.151 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125 Register

14.2.1.2.1.2.2.151.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125 Register (Offset = 41F4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6529. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41F4h

Figure 14-3250. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125 Name Register

31	30	29	28	27	26	25	24
PADCONFIG125_LOCK	PADCONFIG125_WKUP_EVT	PADCONFIG125_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG125_ISO_BYP	PADCONFIG125_ISO_OVR	PADCONFIG125_TX_DIS	PADCONFIG125_DRV_STR		PADCONFIG125_RXACTIVE	PADCONFIG125_PULLTYPESEL	PADCONFIG125_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG125_ST_EN	PADCONFIG125_DEBOUNCE_SEL			RESERVED		PADCONFIG125_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG125_WK_LVL_EN	RESERVED			PADCONFIG125_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6530. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG125_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG125_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG125_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG125_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG125_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6530. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG125_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG125_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG125_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG125_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG125_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG125_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG125_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG125_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG125_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG125_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.152 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126 Register

14.2.1.2.1.2.2.152.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126 Register (Offset = 41F8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6531. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41F8h

Figure 14-3251. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126 Name Register

31	30	29	28	27	26	25	24
PADCONFIG126_LOCK	PADCONFIG126_WKUP_EVT	PADCONFIG126_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG126_ISO_BYP	PADCONFIG126_ISO_OVR	PADCONFIG126_TX_DIS	PADCONFIG126_DRV_STR		PADCONFIG126_RXACTIVE	PADCONFIG126_PULLTYPESEL	PADCONFIG126_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG126_ST_EN	PADCONFIG126_DEBOUNCE_SEL			RESERVED		PADCONFIG126_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG126_WK_LVL_EN	RESERVED			PADCONFIG126_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6532. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG126_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG126_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG126_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG126_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG126_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6532. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG126_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG126_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG126_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG126_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG126_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG126_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG126_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG126_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG126_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG126_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.153 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127 Register

14.2.1.2.1.2.2.153.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127 Register (Offset = 41FCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6533. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 41FCh

Figure 14-3252. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127 Name Register

31	30	29	28	27	26	25	24
PADCONFIG127_LOCK	PADCONFIG127_WKUP_EVT	PADCONFIG127_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG127_ISO_BYP	PADCONFIG127_ISO_OVR	PADCONFIG127_TX_DIS	PADCONFIG127_DRV_STR		PADCONFIG127_RXACTIVE	PADCONFIG127_PULLTYPESEL	PADCONFIG127_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG127_ST_EN	PADCONFIG127_DEBOUNCE_SEL			RESERVED		PADCONFIG127_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG127_WK_LVL_EN	RESERVED			PADCONFIG127_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6534. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG127_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG127_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG127_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG127_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG127_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6534. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG127_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG127_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG127_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG127_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG127_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG127_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG127_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG127_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG127_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG127_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.154 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128 Register

14.2.1.2.1.2.2.154.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128 Register (Offset = 4200h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6535. Instance Table

Instance Name	**Physical Address**
PADCFG_CTRL0	000F 4200h

Figure 14-3253. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128 Name Register

31	30	29	28	27	26	25	24
PADCONFIG128_LOCK	PADCONFIG128_WKUP_EVT	PADCONFIG128_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG128_ISO_BYP	PADCONFIG128_ISO_OVR	PADCONFIG128_TX_DIS	PADCONFIG128_DRV_STR		PADCONFIG128_RXACTIVE	PADCONFIG128_PULLTYPESEL	PADCONFIG128_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG128_ST_EN	PADCONFIG128_DEBOUNCE_SEL			RESERVED		PADCONFIG128_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG128_WK_LVL_EN	RESERVED			PADCONFIG128_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6536. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG128_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG128_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG128_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG128_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG128_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6536. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG128_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG128_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG128_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG128_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG128_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG128_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG128_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG128_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG128_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG128_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.155 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129 Register

14.2.1.2.1.2.2.155.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129 Register (Offset = 4204h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6537. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4204h

Figure 14-3254. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129 Name Register

31	30	29	28	27	26	25	24
PADCONFIG129_LOCK	PADCONFIG129_WKUP_EVT	PADCONFIG129_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG129_ISO_BYP	PADCONFIG129_ISO_OVR	PADCONFIG129_TX_DIS	PADCONFIG129_DRV_STR		PADCONFIG129_RXACTIVE	PADCONFIG129_PULLTYPESEL	PADCONFIG129_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG129_ST_EN	PADCONFIG129_DEBOUNCE_SEL			RESERVED		PADCONFIG129_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG129_WK_LVL_EN	RESERVED			PADCONFIG129_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6538. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG129_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG129_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG129_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG129_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG129_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6538. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG129_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG129_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG129_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG129_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG129_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG129_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG129_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG129_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG129_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG129_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.156 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130 Register

14.2.1.2.1.2.2.156.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130 Register (Offset = 4208h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6539. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4208h

Figure 14-3255. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130 Name Register

31	30	29	28	27	26	25	24
PADCONFIG130_LOCK	PADCONFIG130_WKUP_EVT	PADCONFIG130_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG130_ISO_BYP	PADCONFIG130_ISO_OVR	PADCONFIG130_TX_DIS	PADCONFIG130_DRV_STR		PADCONFIG130_RXACTIVE	PADCONFIG130_PULLTYPESEL	PADCONFIG130_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG130_ST_EN	PADCONFIG130_DEBOUNCE_SEL			RESERVED		PADCONFIG130_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG130_WK_LVL_EN	RESERVED			PADCONFIG130_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6540. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG130_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG130_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG130_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG130_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG130_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6540. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG130_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG130_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG130_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG130_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG130_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG130_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG130_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG130_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG130_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG130_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.157 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131 Register

14.2.1.2.1.2.2.157.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131 Register (Offset = 420Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6541. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 420Ch

Figure 14-3256. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131 Name Register

31	30	29	28	27	26	25	24
PADCONFIG131_LOCK	PADCONFIG131_WKUP_EVT	PADCONFIG131_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG131_ISO_BYP	PADCONFIG131_ISO_OVR	PADCONFIG131_TX_DIS	PADCONFIG131_DRV_STR		PADCONFIG131_RXACTIVE	PADCONFIG131_PULLTYPESEL	PADCONFIG131_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG131_ST_EN	PADCONFIG131_DEBOUNCE_SEL			RESERVED		PADCONFIG131_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG131_WK_LVL_EN	RESERVED			PADCONFIG131_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6542. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG131_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG131_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG131_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG131_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG131_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6542. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG131_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG131_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG131_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG131_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG131_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG131_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG131_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG131_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG131_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG131_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.158 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132 Register

14.2.1.2.1.2.2.158.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132 Register (Offset = 4210h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6543. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4210h

Figure 14-3257. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132 Name Register

31	30	29	28	27	26	25	24
PADCONFIG132_LOCK	PADCONFIG132_WKUP_EVT	PADCONFIG132_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG132_ISO_BYP	PADCONFIG132_ISO_OVR	PADCONFIG132_TX_DIS	PADCONFIG132_DRV_STR		PADCONFIG132_RXACTIVE	PADCONFIG132_PULLTYPESEL	PADCONFIG132_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG132_ST_EN	PADCONFIG132_DEBOUNCE_SEL			RESERVED		PADCONFIG132_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG132_WK_LVL_EN	RESERVED			PADCONFIG132_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6544. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG132_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG132_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG132_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG132_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG132_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6544. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG132_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG132_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG132_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG132_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG132_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG132_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG132_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG132_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG132_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG132_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.159 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133 Register

14.2.1.2.1.2.2.159.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133 Register (Offset = 4214h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6545. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4214h

Figure 14-3258. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133 Name Register

31	30	29	28	27	26	25	24
PADCONFIG133_LOCK	PADCONFIG133_WKUP_EVT	PADCONFIG133_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG133_ISO_BYP	PADCONFIG133_ISO_OVR	PADCONFIG133_TX_DIS	PADCONFIG133_DRV_STR		PADCONFIG133_RXACTIVE	PADCONFIG133_PULLTYPESEL	PADCONFIG133_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG133_ST_EN	PADCONFIG133_DEBOUNCE_SEL			RESERVED		PADCONFIG133_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG133_WK_LVL_EN	RESERVED			PADCONFIG133_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6546. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG133_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG133_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG133_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG133_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG133_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6546. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG133_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG133_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG133_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG133_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG133_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG133_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG133_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG133_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG133_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG133_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.160 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134 Register

14.2.1.2.1.2.2.160.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134 Register (Offset = 4218h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6547. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4218h

Figure 14-3259. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134 Name Register

31	30	29	28	27	26	25	24
PADCONFIG134_LOCK	PADCONFIG134_WKUP_EVT	PADCONFIG134_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG134_ISO_BYP	PADCONFIG134_ISO_OVR	PADCONFIG134_TX_DIS	PADCONFIG134_DRV_STR		PADCONFIG134_RXACTIVE	PADCONFIG134_PULLTYPESEL	PADCONFIG134_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG134_ST_EN	PADCONFIG134_DEBOUNCE_SEL			RESERVED		PADCONFIG134_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG134_WK_LVL_EN	RESERVED			PADCONFIG134_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6548. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG134_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG134_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG134_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG134_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG134_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6548. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG134_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG134_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG134_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG134_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG134_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG134_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG134_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG134_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG134_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG134_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.161 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135 Register

14.2.1.2.1.2.2.161.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135 Register (Offset = 421Ch) [reset = 8054000h]

Register to control pin configuration and muxing

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Table 14-6549. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 421Ch

Figure 14-3260. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135 Name Register

31	30	29	28	27	26	25	24
PADCONFIG135_LOCK	PADCONFIG135_WKUP_EVT	PADCONFIG135_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG135_ISO_BYP	PADCONFIG135_ISO_OVR	PADCONFIG135_TX_DIS	PADCONFIG135_DRV_STR		PADCONFIG135_RXACTIVE	PADCONFIG135_PULLTYPESEL	PADCONFIG135_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG135_ST_EN	PADCONFIG135_DEBOUNCE_SEL			RESERVED		PADCONFIG135_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG135_WK_LVL_EN	RESERVED			PADCONFIG135_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6550. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG135_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG135_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG135_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG135_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG135_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6550. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG135_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG135_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG135_RXACTIVE	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG135_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG135_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG135_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG135_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG135_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG135_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG135_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.162 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136 Register

14.2.1.2.1.2.2.162.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136 Register (Offset = 4220h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6551. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4220h

Figure 14-3261. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136 Name Register

31	30	29	28	27	26	25	24
PADCONFIG136_LOCK	PADCONFIG136_WKUP_EVT	PADCONFIG136_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG136_ISO_BYP	PADCONFIG136_ISO_OVR	PADCONFIG136_TX_DIS	PADCONFIG136_DRV_STR		PADCONFIG136_RXACTIVE	PADCONFIG136_PULLTYPESEL	PADCONFIG136_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG136_ST_EN	PADCONFIG136_DEBOUNCE_SEL			RESERVED		PADCONFIG136_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG136_WK_LVL_EN	RESERVED			PADCONFIG136_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6552. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG136_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG136_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG136_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG136_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG136_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6552. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG136_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG136_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG136_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG136_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG136_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG136_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG136_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG136_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG136_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG136_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.163 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137 Register

14.2.1.2.1.2.2.163.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137 Register (Offset = 4224h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6553. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4224h

Figure 14-3262. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137 Name Register

31	30	29	28	27	26	25	24
PADCONFIG137_LOCK	PADCONFIG137_WKUP_EVT	PADCONFIG137_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG137_ISO_BYP	PADCONFIG137_ISO_OVR	PADCONFIG137_TX_DIS	PADCONFIG137_DRV_STR		PADCONFIG137_RXACTIVE	PADCONFIG137_PULLTYPESEL	PADCONFIG137_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG137_ST_EN	PADCONFIG137_DEBOUNCE_SEL			RESERVED		PADCONFIG137_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG137_WK_LVL_EN	RESERVED			PADCONFIG137_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6554. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG137_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG137_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG137_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG137_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG137_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6554. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG137_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG137_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG137_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG137_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG137_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG137_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG137_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG137_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG137_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG137_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.164 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138 Register

14.2.1.2.1.2.2.164.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138 Register (Offset = 4228h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6555. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4228h

Figure 14-3263. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138 Name Register

31	30	29	28	27	26	25	24
PADCONFIG138_LOCK	PADCONFIG138_WKUP_EVT	PADCONFIG138_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG138_ISO_BYP	PADCONFIG138_ISO_OVR	PADCONFIG138_TX_DIS	PADCONFIG138_DRV_STR		PADCONFIG138_RXACTIVE	PADCONFIG138_PULLTYPESEL	PADCONFIG138_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG138_ST_EN	PADCONFIG138_DEBOUNCE_SEL			RESERVED		PADCONFIG138_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG138_WK_LVL_EN	RESERVED			PADCONFIG138_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6556. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG138_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG138_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG138_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG138_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG138_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6556. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG138_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG138_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG138_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG138_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG138_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG138_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG138_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG138_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG138_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG138_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.165 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139 Register

14.2.1.2.1.2.2.165.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139 Register (Offset = 422Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6557. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 422Ch

Figure 14-3264. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139 Name Register

31	30	29	28	27	26	25	24
PADCONFIG139_LOCK	PADCONFIG139_WKUP_EVT	PADCONFIG139_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG139_ISO_BYP	PADCONFIG139_ISO_OVR	PADCONFIG139_TX_DIS	PADCONFIG139_DRV_STR		PADCONFIG139_RXACTIVE	PADCONFIG139_PULLTYPESEL	PADCONFIG139_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG139_ST_EN	PADCONFIG139_DEBOUNCE_SEL			RESERVED		PADCONFIG139_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG139_WK_LVL_EN	RESERVED			PADCONFIG139_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6558. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG139_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG139_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG139_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG139_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG139_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6558. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG139_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG139_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG139_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG139_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG139_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG139_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG139_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG139_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG139_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG139_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.166 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140 Register

14.2.1.2.1.2.2.166.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140 Register (Offset = 4230h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6559. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4230h

Figure 14-3265. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140 Name Register

31	30	29	28	27	26	25	24
PADCONFIG140_LOCK	PADCONFIG140_WKUP_EVT	PADCONFIG140_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG140_ISO_BYP	PADCONFIG140_ISO_OVR	PADCONFIG140_TX_DIS	PADCONFIG140_DRV_STR		PADCONFIG140_RXACTIVE	PADCONFIG140_PULLTYPESEL	PADCONFIG140_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG140_ST_EN	PADCONFIG140_DEBOUNCE_SEL			RESERVED		PADCONFIG140_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG140_WK_LVL_EN	RESERVED			PADCONFIG140_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6560. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG140_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG140_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG140_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG140_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG140_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6560. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG140_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG140_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG140_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG140_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG140_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG140_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG140_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG140_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG140_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG140_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.167 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141 Register

14.2.1.2.1.2.2.167.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141 Register (Offset = 4234h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6561. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4234h

Figure 14-3266. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141 Name Register

31	30	29	28	27	26	25	24
PADCONFIG141_LOCK	PADCONFIG141_WKUP_EVT	PADCONFIG141_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG141_ISO_BYP	PADCONFIG141_ISO_OVR	PADCONFIG141_TX_DIS	PADCONFIG141_DRV_STR		PADCONFIG141_RXACTIVE	PADCONFIG141_PULLTYPESEL	PADCONFIG141_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG141_ST_EN	PADCONFIG141_DEBOUNCE_SEL			RESERVED		PADCONFIG141_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG141_WK_LVL_EN	RESERVED			PADCONFIG141_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6562. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG141_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG141_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG141_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG141_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG141_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6562. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG141_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG141_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG141_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG141_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG141_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG141_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG141_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG141_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG141_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG141_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.168 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143 Register

14.2.1.2.1.2.2.168.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143 Register (Offset = 423Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6563. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 423Ch

Figure 14-3267. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143 Name Register

31	30	29	28	27	26	25	24
PADCONFIG143_LOCK	PADCONFIG143_WKUP_EVT	PADCONFIG143_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG143_ISO_BYP	PADCONFIG143_ISO_OVR	PADCONFIG143_TX_DIS	PADCONFIG143_DRV_STR		PADCONFIG143_RXACTIVE	PADCONFIG143_PULLTYPESEL	PADCONFIG143_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG143_ST_EN	PADCONFIG143_DEBOUNCE_SEL			RESERVED		PADCONFIG143_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG143_WK_LVL_EN	RESERVED			PADCONFIG143_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6564. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG143_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG143_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG143_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG143_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG143_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6564. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG143_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG143_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG143_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG143_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG143_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG143_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG143_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG143_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG143_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG143_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.169 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144 Register

14.2.1.2.1.2.2.169.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144 Register (Offset = 4240h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6565. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4240h

Figure 14-3268. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144 Name Register

31	30	29	28	27	26	25	24
PADCONFIG144_LOCK	PADCONFIG144_WKUP_EVT	PADCONFIG144_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG144_ISO_BYP	PADCONFIG144_ISO_OVR	PADCONFIG144_TX_DIS	PADCONFIG144_DRV_STR		PADCONFIG144_RXACTIVE	PADCONFIG144_PULLTYPESEL	PADCONFIG144_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG144_ST_EN	PADCONFIG144_DEBOUNCE_SEL			RESERVED		PADCONFIG144_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG144_WK_LVL_EN	RESERVED			PADCONFIG144_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6566. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG144_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG144_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG144_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG144_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG144_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6566. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG144_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG144_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG144_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG144_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG144_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG144_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG144_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG144_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG144_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG144_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.170 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145 Register

14.2.1.2.1.2.2.170.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145 Register (Offset = 4244h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6567. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4244h

Figure 14-3269. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145 Name Register

31	30	29	28	27	26	25	24
PADCONFIG145_LOCK	PADCONFIG145_WKUP_EVT	PADCONFIG145_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG145_ISO_BYP	PADCONFIG145_ISO_OVR	PADCONFIG145_TX_DIS	PADCONFIG145_DRV_STR		PADCONFIG145_RXACTIVE	PADCONFIG145_PULLTYPESEL	PADCONFIG145_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG145_ST_EN	PADCONFIG145_DEBOUNCE_SEL			RESERVED		PADCONFIG145_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG145_WK_LVL_EN	RESERVED			PADCONFIG145_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6568. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG145_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG145_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG145_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG145_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG145_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6568. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG145_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG145_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG145_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG145_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG145_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG145_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG145_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG145_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG145_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG145_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.171 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147 Register

14.2.1.2.1.2.2.171.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147 Register (Offset = 424Ch) [reset = 8014000h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6569. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 424Ch

Figure 14-3270. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147 Name Register

31	30	29	28	27	26	25	24
PADCONFIG147_LOCK	PADCONFIG147_WKUP_EVT	PADCONFIG147_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG147_ISO_BYP	PADCONFIG147_ISO_OVR	PADCONFIG147_TX_DIS	PADCONFIG147_DRV_STR		PADCONFIG147_RXACTIVE	PADCONFIG147_PULLTYPESEL	PADCONFIG147_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG147_ST_EN	PADCONFIG147_DEBOUNCE_SEL			RESERVED		PADCONFIG147_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG147_WK_LVL_EN	RESERVED			PADCONFIG147_MUXMODE			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6570. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG147_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG147_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG147_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG147_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG147_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6570. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG147_TX_DIS	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG147_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG147_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG147_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG147_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG147_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG147_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG147_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG147_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG147_MUXMODE	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.172 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149 Register

14.2.1.2.1.2.2.172.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149 Register (Offset = 4254h) [reset = 204007h]

Register to control pin configuration and muxing

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Table 14-6571. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 4254h

Figure 14-3271. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149 Name Register

31	30	29	28	27	26	25	24
PADCONFIG149_LOCK	PADCONFIG149_WKUP_EVT	PADCONFIG149_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG149_ISO_BYP	PADCONFIG149_ISO_OVR	PADCONFIG149_TX_DIS	PADCONFIG149_DRV_STR		PADCONFIG149_RXACTIVE	PADCONFIG149_PULLTYPESEL	PADCONFIG149_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG149_ST_EN	PADCONFIG149_DEBOUNCE_SEL			RESERVED		PADCONFIG149_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG149_WK_LVL_EN	RESERVED			PADCONFIG149_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6572. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG149_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG149_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG149_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG149_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG149_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6572. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG149_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG149_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG149_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG149_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG149_PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG149_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG149_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG149_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG149_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG149_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.173 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171 Register

14.2.1.2.1.2.2.173.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171 Register (Offset = 42ACh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6573. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42ACh

Figure 14-3272. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171 Name Register

31	30	29	28	27	26	25	24
PADCONFIG171_LOCK	PADCONFIG171_WKUP_EVT	PADCONFIG171_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG171_ISO_BYP	PADCONFIG171_ISO_OVR	PADCONFIG171_TX_DIS	PADCONFIG171_DRV_STR		PADCONFIG171_RXACTIVE	PADCONFIG171_PULLTYPESEL	PADCONFIG171_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG171_ST_EN	PADCONFIG171_DEBOUNCE_SEL			RESERVED		PADCONFIG171_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG171_WK_LVL_EN	RESERVED			PADCONFIG171_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6574. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG171_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG171_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG171_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG171_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG171_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6574. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG171_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG171_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG171_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG171_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG171_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG171_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG171_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG171_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG171_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG171_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.174 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172 Register

14.2.1.2.1.2.2.174.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172 Register (Offset = 42B0h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6575. Instance Table

Instance Name	**Physical Address**
PADCFG_CTRL0	000F 42B0h

Figure 14-3273. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172 Name Register

31	30	29	28	27	26	25	24
PADCONFIG172_LOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PADCONFIG172_DEBOUNCE_SEL			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6576. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG172_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG172_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.175 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173 Register

14.2.1.2.1.2.2.175.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173 Register (Offset = 42B4h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6577. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42B4h

Figure 14-3274. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173 Name Register

31	30	29	28	27	26	25	24
PADCONFIG173_LOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PADCONFIG173_DEBOUNCE_SEL			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6578. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG173_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG173_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.176 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174 Register

14.2.1.2.1.2.2.176.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174 Register (Offset = 42B8h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6579. Instance Table

Instance Name	**Physical Address**
PADCFG_CTRL0	000F 42B8h

Figure 14-3275. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG174_LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="3">PADCONFIG174_DEBOUNCE_SEL</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="2">NONE</td><td colspan="3">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6580. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG174_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG174_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.177 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175 Register

14.2.1.2.1.2.2.177.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175 Register (Offset = 42BCh) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6581. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42BCh

Figure 14-3276. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175 Name Register

31	30	29	28	27	26	25	24
PADCONFIG175_LOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PADCONFIG175_DEBOUNCE_SEL			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6582. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG175_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG175_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.178 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176 Register

14.2.1.2.1.2.2.178.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176 Register (Offset = 42C0h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6583. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42C0h

Figure 14-3277. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176 Name Register

31	30	29	28	27	26	25	24
PADCONFIG176_LOCK	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PADCONFIG176_DEBOUNCE_SEL			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6584. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG176_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG176_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.179 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177 Register

14.2.1.2.1.2.2.179.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177 Register (Offset = 42C4h) [reset = 0h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6585. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42C4h

Figure 14-3278. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG177_LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="3">PADCONFIG177_DEBOUNCE_SEL</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="2">NONE</td><td colspan="3">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6586. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG177_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG177_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.180 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178 Register

14.2.1.2.1.2.2.180.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178 Register (Offset = 42C8h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6587. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42C8h

Figure 14-3279. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178 Name Register

31	30	29	28	27	26	25	24
PADCONFIG178_LOCK	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PADCONFIG178_DEBOUNCE_SEL			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-6588. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG178_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG178_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.181 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179 Register

14.2.1.2.1.2.2.181.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179 Register (Offset = 42CCh) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6589. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42CCh

Figure 14-3280. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG179_LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="3">PADCONFIG179_DEBOUNCE_SEL</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="2">NONE</td><td colspan="3">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6590. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG179_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG179_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.182 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180 Register

14.2.1.2.1.2.2.182.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180 Register (Offset = 42D0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6591. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42D0h

Figure 14-3281. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180 Name Register

31	30	29	28	27	26	25	24
PADCONFIG180_LOCK	PADCONFIG180_WKUP_EVT	PADCONFIG180_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG180_ISO_BYP	PADCONFIG180_ISO_OVR	PADCONFIG180_TX_DIS	PADCONFIG180_DRV_STR		PADCONFIG180_RXACTIVE	PADCONFIG180_PULLTYPESEL	PADCONFIG180_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG180_ST_EN	PADCONFIG180_DEBOUNCE_SEL			RESERVED		PADCONFIG180_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG180_WK_LVL_EN	RESERVED			PADCONFIG180_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6592. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG180_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG180_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG180_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG180_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG180_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6592. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG180_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG180_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG180_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG180_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG180_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG180_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG180_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG180_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG180_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG180_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.183 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181 Register

14.2.1.2.1.2.2.183.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181 Register (Offset = 42D4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6593. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42D4h

Figure 14-3282. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181 Name Register

31	30	29	28	27	26	25	24
PADCONFIG181_LOCK	PADCONFIG181_WKUP_EVT	PADCONFIG181_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG181_ISO_BYP	PADCONFIG181_ISO_OVR	PADCONFIG181_TX_DIS	PADCONFIG181_DRV_STR		PADCONFIG181_RXACTIVE	PADCONFIG181_PULLTYPESEL	PADCONFIG181_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG181_ST_EN	PADCONFIG181_DEBOUNCE_SEL			RESERVED		PADCONFIG181_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG181_WK_LVL_EN	RESERVED			PADCONFIG181_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6594. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG181_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG181_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG181_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG181_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG181_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6594. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG181_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG181_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG181_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG181_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG181_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG181_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG181_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG181_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG181_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG181_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.184 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182 Register

14.2.1.2.1.2.2.184.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182 Register (Offset = 42D8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6595. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42D8h

Figure 14-3283. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182 Name Register

31	30	29	28	27	26	25	24
PADCONFIG182_LOCK	PADCONFIG182_WKUP_EVT	PADCONFIG182_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG182_ISO_BYP	PADCONFIG182_ISO_OVR	PADCONFIG182_TX_DIS	PADCONFIG182_DRV_STR		PADCONFIG182_RXACTIVE	PADCONFIG182_PULLTYPESEL	PADCONFIG182_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG182_ST_EN	PADCONFIG182_DEBOUNCE_SEL			RESERVED		PADCONFIG182_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG182_WK_LVL_EN	RESERVED			PADCONFIG182_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6596. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG182_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG182_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG182_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG182_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG182_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6596. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG182_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG182_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG182_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG182_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG182_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG182_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG182_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG182_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG182_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG182_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.185 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183 Register

14.2.1.2.1.2.2.185.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183 Register (Offset = 42DCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6597. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 42DCh

Figure 14-3284. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183 Name Register

31	30	29	28	27	26	25	24
PADCONFIG183_LOCK	PADCONFIG183_WKUP_EVT	PADCONFIG183_WKUP_EN					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG183_ISO_BYP	PADCONFIG183_ISO_OVR	PADCONFIG183_TX_DIS	PADCONFIG183_DRV_STR		PADCONFIG183_RXACTIVE	PADCONFIG183_PULLTYPESEL	PADCONFIG183_PULLUDEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG183_ST_EN	PADCONFIG183_DEBOUNCE_SEL			RESERVED		PADCONFIG183_WK_LVL_POL
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG183_WK_LVL_EN	RESERVED			PADCONFIG183_MUXMODE			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6598. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG183_LOCK	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG183_WKUP_EVT	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG183_WKUP_EN	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG183_ISO_BYP	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG183_ISO_OVR	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6598. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG183_TX_DIS	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG183_DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG183_RXACTIVE	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG183_PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG183_PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG183_ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG183_DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG183_WK_LVL_POL	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG183_WK_LVL_EN	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG183_MUXMODE	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.186 MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0 Register

14.2.1.2.1.2.2.186.1 MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0 Register (Offset = 5008h) [reset = 0h]

- KICK0 component

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Table 14-6599. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 5008h

Figure 14-3285. MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0							
R/W							
0h							

Table 14-6600. MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.187 MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1 Register

14.2.1.2.1.2.2.187.1 MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1 Register (Offset = 500Ch) [reset = 0h]

- KICK1 component

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Table 14-6601. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 500Ch

Figure 14-3286. MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK1							
R/W							
0h							

Table 14-6602. MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.188 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register

14.2.1.2.1.2.2.188.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register (Offset = 5100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6603. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 5100h

Figure 14-3287. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0_READONLY							
R							
0h							

Table 14-6604. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.189 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register

14.2.1.2.1.2.2.189.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register (Offset = 5104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6605. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 5104h

Figure 14-3288. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R1_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R1_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R1_READONLY							
R							
0h							

Table 14-6606. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.190 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY Register

14.2.1.2.1.2.2.190.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY Register (Offset = 5108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6607. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 5108h

Figure 14-3289. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLAIMREG_P1_R2_READONLY</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6608. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.191 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3_READONLY Register

14.2.1.2.1.2.2.191.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3_READONLY Register (Offset = 510Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-6609. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 510Ch

Figure 14-3290. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3_READONLY							
R							
0h							

Table 14-6610. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.192 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4_READONLY Register

14.2.1.2.1.2.2.192.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4_READONLY Register (Offset = 5110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6611. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 5110h

Figure 14-3291. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4_READONLY							
R							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4_READONLY							
R							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4_READONLY							
R							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4_READONLY							
R							
0h							

Table 14-6612. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.193 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5_READONLY Register

14.2.1.2.1.2.2.193.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5_READONLY Register (Offset = 5114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6613. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 5114h

Figure 14-3292. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5_READONLY Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5_READONLY							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P1_R5_READONLY							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P1_R5_READONLY							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P1_R5_READONLY							
R							
0h							

Table 14-6614. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5_READONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5_READONLY	R	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.194 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Register

14.2.1.2.1.2.2.194.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Register (Offset = 6000h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6615. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6000h

Figure 14-3293. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG0_LOCK_PROXY	PADCONFIG0_WKUP_EVT_PROXY	PADCONFIG0_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG0_ISO_BYP_PROXY	PADCONFIG0_ISO_OVR_PROXY	PADCONFIG0_TX_DIS_PROXY	PADCONFIG0_DRV_STR_PROXY		PADCONFIG0_RXACTIVE_PROXY	PADCONFIG0_PULLTYPESEL_PROXY	PADCONFIG0_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG0_ST_EN_PROXY	PADCONFIG0_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG0_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG0_WK_LVL_EN_PROXY	RESERVED			PADCONFIG0_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6616. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG0_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG0_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG0_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG0_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG0_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6616. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG0_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG0_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG0_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG0_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG0_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG0_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG0_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG0_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG0_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG0_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG0_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.195 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Register

14.2.1.2.1.2.2.195.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Register (Offset = 6004h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6617. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6004h

Figure 14-3294. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG1_LOCK_PROXY	PADCONFIG1_WKUP_EVT_PROXY	PADCONFIG1_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG1_ISO_BYP_PROXY	PADCONFIG1_ISO_OVR_PROXY	PADCONFIG1_TX_DIS_PROXY	PADCONFIG1_DRV_STR_PROXY		PADCONFIG1_RXACTIVE_PROXY	PADCONFIG1_PULLTYPESEL_PROXY	PADCONFIG1_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG1_ST_EN_PROXY	PADCONFIG1_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG1_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG1_WK_LVL_EN_PROXY	RESERVED			PADCONFIG1_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6618. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG1_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG1_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG1_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG1_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG1_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6618. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG1_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG1_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG1_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG1_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG1_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG1_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG1_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG1_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG1_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG1_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG1_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.196 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Register

14.2.1.2.1.2.2.196.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Register (Offset = 6008h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6619. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6008h

Figure 14-3295. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG2_LOCK_PROXY	PADCONFIG2_WKUP_EVT_PROXY	PADCONFIG2_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG2_ISO_BYP_PROXY	PADCONFIG2_ISO_OVR_PROXY	PADCONFIG2_TX_DIS_PROXY	PADCONFIG2_DRV_STR_PROXY		PADCONFIG2_RXACTIVE_PROXY	PADCONFIG2_PULLTYPESEL_PROXY	PADCONFIG2_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG2_ST_EN_PROXY	PADCONFIG2_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG2_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG2_WK_LVL_EN_PROXY	RESERVED			PADCONFIG2_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6620. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG2_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG2_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG2_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG2_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG2_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6620. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG2_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG2_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG2_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG2_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG2_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG2_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG2_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG2_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG2_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG2_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG2_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.197 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Register

14.2.1.2.1.2.2.197.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Register (Offset = 600Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6621. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 600Ch

Figure 14-3296. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG3_LOCK_PROXY	PADCONFIG3_WKUP_EVT_PROXY	PADCONFIG3_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG3_ISO_BYP_PROXY	PADCONFIG3_ISO_OVR_PROXY	PADCONFIG3_TX_DIS_PROXY	PADCONFIG3_DRV_STR_PROXY		PADCONFIG3_RXACTIVE_PROXY	PADCONFIG3_PULLTYPESEL_PROXY	PADCONFIG3_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG3_ST_EN_PROXY	PADCONFIG3_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG3_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG3_WK_LVL_EN_PROXY	RESERVED			PADCONFIG3_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6622. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG3_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG3_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG3_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG3_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG3_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6622. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG3_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG3_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG3_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG3_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG3_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG3_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG3_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG3_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG3_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG3_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG3_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.198 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Register

14.2.1.2.1.2.2.198.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Register (Offset = 6010h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6623. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6010h

Figure 14-3297. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG4_LOCK_PROXY	PADCONFIG4_WKUP_EVT_PROXY	PADCONFIG4_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG4_ISO_BYP_PROXY	PADCONFIG4_ISO_OVR_PROXY	PADCONFIG4_TX_DIS_PROXY	PADCONFIG4_DRV_STR_PROXY		PADCONFIG4_RXACTIVE_PROXY	PADCONFIG4_PULLTYPESEL_PROXY	PADCONFIG4_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG4_ST_EN_PROXY	PADCONFIG4_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG4_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG4_WK_LVL_EN_PROXY	RESERVED			PADCONFIG4_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6624. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG4_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG4_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG4_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG4_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG4_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6624. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG4_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG4_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG4_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG4_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG4_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG4_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG4_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG4_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG4_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG4_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG4_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.199 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Register

14.2.1.2.1.2.2.199.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Register (Offset = 6014h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6625. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6014h

Figure 14-3298. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG5_LOCK_PROXY	PADCONFIG5_WKUP_EVT_PROXY	PADCONFIG5_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG5_ISO_BYP_PROXY	PADCONFIG5_ISO_OVR_PROXY	PADCONFIG5_TX_DIS_PROXY	PADCONFIG5_DRV_STR_PROXY		PADCONFIG5_RXACTIVE_PROXY	PADCONFIG5_PULLTYPESEL_PROXY	PADCONFIG5_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG5_ST_EN_PROXY	PADCONFIG5_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG5_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG5_WK_LVL_EN_PROXY	RESERVED			PADCONFIG5_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6626. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG5_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG5_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG5_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG5_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG5_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6626. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG5_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG5_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG5_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG5_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG5_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG5_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG5_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG5_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG5_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG5_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG5_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.200 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Register

14.2.1.2.1.2.2.200.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Register (Offset = 6018h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6627. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6018h

Figure 14-3299. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG6_LOCK_PROXY	PADCONFIG6_WKUP_EVT_PROXY	PADCONFIG6_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG6_ISO_BYP_PROXY	PADCONFIG6_ISO_OVR_PROXY	PADCONFIG6_TX_DIS_PROXY	PADCONFIG6_DRV_STR_PROXY		PADCONFIG6_RXACTIVE_PROXY	PADCONFIG6_PULLTYPESEL_PROXY	PADCONFIG6_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG6_ST_EN_PROXY	PADCONFIG6_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG6_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG6_WK_LVL_EN_PROXY	RESERVED			PADCONFIG6_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6628. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG6_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG6_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG6_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG6_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG6_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6628. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG6_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG6_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG6_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG6_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG6_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG6_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG6_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG6_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG6_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG6_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG6_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.201 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Register

14.2.1.2.1.2.2.201.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Register (Offset = 601Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6629. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 601Ch

Figure 14-3300. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG7_LOCK_PROXY	PADCONFIG7_WKUP_EVT_PROXY	PADCONFIG7_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG7_ISO_BYP_PROXY	PADCONFIG7_ISO_OVR_PROXY	PADCONFIG7_TX_DIS_PROXY	PADCONFIG7_DRV_STR_PROXY		PADCONFIG7_RXACTIVE_PROXY	PADCONFIG7_PULLTYPESEL_PROXY	PADCONFIG7_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG7_ST_EN_PROXY	PADCONFIG7_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG7_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG7_WK_LVL_EN_PROXY	RESERVED			PADCONFIG7_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6630. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG7_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG7_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG7_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG7_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG7_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6630. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG7_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG7_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG7_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG7_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG7_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG7_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG7_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG7_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG7_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG7_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG7_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.202 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Register

14.2.1.2.1.2.2.202.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Register (Offset = 6020h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6631. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6020h

Figure 14-3301. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG8_LOCK_PROXY	PADCONFIG8_WKUP_EVT_PROXY	PADCONFIG8_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG8_ISO_BYP_PROXY	PADCONFIG8_ISO_OVR_PROXY	PADCONFIG8_TX_DIS_PROXY	PADCONFIG8_DRV_STR_PROXY		PADCONFIG8_RXACTIVE_PROXY	PADCONFIG8_PULLTYPESEL_PROXY	PADCONFIG8_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG8_ST_EN_PROXY	PADCONFIG8_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG8_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG8_WK_LVL_EN_PROXY	RESERVED			PADCONFIG8_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6632. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG8_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG8_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG8_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG8_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG8_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6632. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG8_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG8_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG8_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG8_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG8_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG8_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG8_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG8_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG8_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG8_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG8_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.203 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Register

14.2.1.2.1.2.2.203.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Register (Offset = 6024h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6633. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6024h

Figure 14-3302. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG9_LOCK_PROXY	PADCONFIG9_WKUP_EVT_PROXY	PADCONFIG9_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG9_ISO_BYP_PROXY	PADCONFIG9_ISO_OVR_PROXY	PADCONFIG9_TX_DIS_PROXY	PADCONFIG9_DRV_STR_PROXY		PADCONFIG9_RXACTIVE_PROXY	PADCONFIG9_PULLTYPESEL_PROXY	PADCONFIG9_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG9_ST_EN_PROXY	PADCONFIG9_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG9_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG9_WK_LVL_EN_PROXY	RESERVED			PADCONFIG9_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6634. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG9_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG9_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG9_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG9_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG9_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6634. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG9_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG9_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG9_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG9_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG9_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG9_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG9_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG9_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG9_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG9_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG9_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.204 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Register

14.2.1.2.1.2.2.204.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Register (Offset = 6028h) [reset = 8214007h]

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Table 14-6635. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6028h

Figure 14-3303. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG10_LOCK_PROXY	PADCONFIG10_WKUP_EVT_PROXY	PADCONFIG10_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG10_ISO_BYP_PROXY	PADCONFIG10_ISO_OVR_PROXY	PADCONFIG10_TX_DIS_PROXY	PADCONFIG10_DRV_STR_PROXY		PADCONFIG10_RXACTIVE_PROXY	PADCONFIG10_PULLTYPESEL_PROXY	PADCONFIG10_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG10_ST_EN_PROXY	PADCONFIG10_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG10_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG10_WK_LVL_EN_PROXY	RESERVED			PADCONFIG10_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6636. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG10_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG10_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG10_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG10_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG10_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6636. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG10_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG10_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG10_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG10_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG10_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG10_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG10_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG10_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG10_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG10_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG10_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.205 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Register

14.2.1.2.1.2.2.205.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Register (Offset = 602Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6637. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 602Ch

Figure 14-3304. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG11_LOCK_PROXY	PADCONFIG11_WKUP_EVT_PROXY	PADCONFIG11_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG11_ISO_BYP_PROXY	PADCONFIG11_ISO_OVR_PROXY	PADCONFIG11_TX_DIS_PROXY	PADCONFIG11_DRV_STR_PROXY		PADCONFIG11_RXACTIVE_PROXY	PADCONFIG11_PULLTYPESEL_PROXY	PADCONFIG11_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG11_ST_EN_PROXY	PADCONFIG11_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG11_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG11_WK_LVL_EN_PROXY	RESERVED			PADCONFIG11_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6638. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG11_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG11_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG11_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG11_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG11_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6638. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG11_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG11_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG11_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG11_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG11_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG11_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG11_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG11_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG11_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG11_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG11_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.206 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Register

14.2.1.2.1.2.2.206.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Register (Offset = 6030h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6639. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6030h

Figure 14-3305. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG12_LOCK_PROXY	PADCONFIG12_WKUP_EVT_PROXY	PADCONFIG12_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG12_ISO_BYP_PROXY	PADCONFIG12_ISO_OVR_PROXY	PADCONFIG12_TX_DIS_PROXY	PADCONFIG12_DRV_STR_PROXY		PADCONFIG12_RXACTIVE_PROXY	PADCONFIG12_PULLTYPESEL_PROXY	PADCONFIG12_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG12_ST_EN_PROXY	PADCONFIG12_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG12_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG12_WK_LVL_EN_PROXY	RESERVED			PADCONFIG12_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6640. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG12_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG12_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG12_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG12_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG12_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6640. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG12_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG12_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG12_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG12_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG12_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG12_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG12_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG12_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG12_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG12_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG12_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.207 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Register

14.2.1.2.1.2.2.207.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Register (Offset = 6034h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6641. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6034h

Figure 14-3306. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG13_LOCK_PROXY	PADCONFIG13_WKUP_EVT_PROXY	PADCONFIG13_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG13_ISO_BYP_PROXY	PADCONFIG13_ISO_OVR_PROXY	PADCONFIG13_TX_DIS_PROXY	PADCONFIG13_DRV_STR_PROXY		PADCONFIG13_RXACTIVE_PROXY	PADCONFIG13_PULLTYPESEL_PROXY	PADCONFIG13_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG13_ST_EN_PROXY	PADCONFIG13_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG13_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG13_WK_LVL_EN_PROXY	RESERVED			PADCONFIG13_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6642. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG13_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG13_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG13_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG13_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG13_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6642. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG13_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG13_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG13_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG13_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG13_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG13_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG13_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG13_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG13_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG13_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG13_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.208 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Register

14.2.1.2.1.2.2.208.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Register (Offset = 6038h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6643. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6038h

Figure 14-3307. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG14_LOCK_PROXY	PADCONFIG14_WKUP_EVT_PROXY	PADCONFIG14_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG14_ISO_BYP_PROXY	PADCONFIG14_ISO_OVR_PROXY	PADCONFIG14_TX_DIS_PROXY	PADCONFIG14_DRV_STR_PROXY		PADCONFIG14_RXACTIVE_PROXY	PADCONFIG14_PULLTYPESEL_PROXY	PADCONFIG14_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG14_ST_EN_PROXY	PADCONFIG14_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG14_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG14_WK_LVL_EN_PROXY	RESERVED			PADCONFIG14_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6644. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG14_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG14_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG14_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG14_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG14_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6644. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG14_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG14_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG14_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG14_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG14_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG14_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG14_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG14_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG14_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG14_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG14_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.209 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Register

14.2.1.2.1.2.2.209.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Register (Offset = 603Ch) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6645. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 603Ch

Figure 14-3308. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG15_LOCK_PROXY	PADCONFIG15_WKUP_EVT_PROXY	PADCONFIG15_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG15_ISO_BYP_PROXY	PADCONFIG15_ISO_OVR_PROXY	PADCONFIG15_TX_DIS_PROXY	PADCONFIG15_DRV_STR_PROXY		PADCONFIG15_RXACTIVE_PROXY	PADCONFIG15_PULLTYPESEL_PROXY	PADCONFIG15_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG15_ST_EN_PROXY	PADCONFIG15_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG15_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG15_WK_LVL_EN_PROXY	RESERVED			PADCONFIG15_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6646. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG15_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG15_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG15_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG15_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG15_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6646. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG15_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG15_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG15_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG15_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG15_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG15_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG15_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG15_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG15_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG15_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG15_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.210 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Register

14.2.1.2.1.2.2.210.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Register (Offset = 6040h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6647. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6040h

Figure 14-3309. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG16_LOCK_PROXY	PADCONFIG16_WKUP_EVT_PROXY	PADCONFIG16_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG16_ISO_BYP_PROXY	PADCONFIG16_ISO_OVR_PROXY	PADCONFIG16_TX_DIS_PROXY	PADCONFIG16_DRV_STR_PROXY		PADCONFIG16_RXACTIVE_PROXY	PADCONFIG16_PULLTYPESEL_PROXY	PADCONFIG16_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG16_ST_EN_PROXY	PADCONFIG16_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG16_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG16_WK_LVL_EN_PROXY	RESERVED			PADCONFIG16_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6648. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG16_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG16_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG16_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG16_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG16_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6648. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG16_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG16_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG16_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG16_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG16_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG16_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG16_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG16_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG16_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG16_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG16_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.211 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17_PROXY Register

14.2.1.2.1.2.2.211.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17_PROXY Register (Offset = 6044h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6649. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6044h

Figure 14-3310. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG17_LOCK_PROXY	PADCONFIG17_WKUP_EVT_PROXY	PADCONFIG17_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG17_ISO_BYP_PROXY	PADCONFIG17_ISO_OVR_PROXY	PADCONFIG17_TX_DIS_PROXY	PADCONFIG17_DRV_STR_PROXY		PADCONFIG17_RXACTIVE_PROXY	PADCONFIG17_PULLTYPESEL_PROXY	PADCONFIG17_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG17_ST_EN_PROXY	PADCONFIG17_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG17_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG17_WK_LVL_EN_PROXY	RESERVED			PADCONFIG17_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6650. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG17_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG17_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG17_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG17_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG17_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6650. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG17_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG17_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG17_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG17_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG17_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG17_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG17_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG17_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG17_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG17_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG17_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.212 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18_PROXY Register

14.2.1.2.1.2.2.212.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18_PROXY Register (Offset = 6048h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6651. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6048h

Figure 14-3311. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG18_LOCK_PROXY	PADCONFIG18_WKUP_EVT_PROXY	PADCONFIG18_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG18_ISO_BYP_PROXY	PADCONFIG18_ISO_OVR_PROXY	PADCONFIG18_TX_DIS_PROXY	PADCONFIG18_DRV_STR_PROXY		PADCONFIG18_RXACTIVE_PROXY	PADCONFIG18_PULLTYPESEL_PROXY	PADCONFIG18_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG18_ST_EN_PROXY	PADCONFIG18_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG18_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG18_WK_LVL_EN_PROXY	RESERVED			PADCONFIG18_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6652. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG18_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG18_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG18_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG18_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG18_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6652. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG18_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG18_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG18_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG18_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG18_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG18_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG18_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG18_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG18_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG18_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG18_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.213 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Register

14.2.1.2.1.2.2.213.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Register (Offset = 604Ch) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6653. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 604Ch

Figure 14-3312. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG19_LOCK_PROXY	PADCONFIG19_WKUP_EVT_PROXY	PADCONFIG19_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG19_ISO_BYP_PROXY	PADCONFIG19_ISO_OVR_PROXY	PADCONFIG19_TX_DIS_PROXY	PADCONFIG19_DRV_STR_PROXY		PADCONFIG19_RXACTIVE_PROXY	PADCONFIG19_PULLTYPESEL_PROXY	PADCONFIG19_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG19_ST_EN_PROXY	PADCONFIG19_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG19_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG19_WK_LVL_EN_PROXY	RESERVED			PADCONFIG19_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6654. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG19_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG19_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG19_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG19_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG19_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6654. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG19_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG19_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG19_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG19_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG19_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG19_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG19_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG19_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG19_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG19_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG19_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.214 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Register

14.2.1.2.1.2.2.214.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Register (Offset = 6050h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6655. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6050h

Figure 14-3313. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG20_LOCK_PROXY	PADCONFIG20_WKUP_EVT_PROXY	PADCONFIG20_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG20_ISO_BYP_PROXY	PADCONFIG20_ISO_OVR_PROXY	PADCONFIG20_TX_DIS_PROXY	PADCONFIG20_DRV_STR_PROXY		PADCONFIG20_RXACTIVE_PROXY	PADCONFIG20_PULLTYPESEL_PROXY	PADCONFIG20_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG20_ST_EN_PROXY	PADCONFIG20_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG20_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG20_WK_LVL_EN_PROXY	RESERVED			PADCONFIG20_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6656. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG20_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG20_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG20_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG20_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG20_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6656. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG20_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG20_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG20_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG20_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG20_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG20_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG20_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG20_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG20_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG20_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG20_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.215 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Register

14.2.1.2.1.2.2.215.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Register (Offset = 6054h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6657. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6054h

Figure 14-3314. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG21_LOCK_PROXY	PADCONFIG21_WKUP_EVT_PROXY	PADCONFIG21_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG21_ISO_BYP_PROXY	PADCONFIG21_ISO_OVR_PROXY	PADCONFIG21_TX_DIS_PROXY	PADCONFIG21_DRV_STR_PROXY		PADCONFIG21_RXACTIVE_PROXY	PADCONFIG21_PULLTYPESEL_PROXY	PADCONFIG21_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG21_ST_EN_PROXY	PADCONFIG21_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG21_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG21_WK_LVL_EN_PROXY	RESERVED			PADCONFIG21_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6658. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG21_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG21_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG21_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG21_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG21_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6658. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG21_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG21_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG21_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG21_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG21_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG21_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG21_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG21_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG21_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG21_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG21_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.216 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Register

14.2.1.2.1.2.2.216.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Register (Offset = 6058h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6659. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6058h

Figure 14-3315. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG22_LOCK_PROXY	PADCONFIG22_WKUP_EVT_PROXY	PADCONFIG22_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG22_ISO_BYP_PROXY	PADCONFIG22_ISO_OVR_PROXY	PADCONFIG22_TX_DIS_PROXY	PADCONFIG22_DRV_STR_PROXY		PADCONFIG22_RXACTIVE_PROXY	PADCONFIG22_PULLTYPESEL_PROXY	PADCONFIG22_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG22_ST_EN_PROXY	PADCONFIG22_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG22_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG22_WK_LVL_EN_PROXY	RESERVED			PADCONFIG22_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6660. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG22_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG22_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG22_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG22_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG22_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6660. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG22_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG22_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG22_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG22_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG22_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG22_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG22_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG22_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG22_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG22_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG22_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.217 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Register

14.2.1.2.1.2.2.217.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Register (Offset = 605Ch) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6661. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 605Ch

Figure 14-3316. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG23_LOCK_PROXY	PADCONFIG23_WKUP_EVT_PROXY	PADCONFIG23_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG23_ISO_BYP_PROXY	PADCONFIG23_ISO_OVR_PROXY	PADCONFIG23_TX_DIS_PROXY	PADCONFIG23_DRV_STR_PROXY		PADCONFIG23_RXACTIVE_PROXY	PADCONFIG23_PULLTYPESEL_PROXY	PADCONFIG23_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG23_ST_EN_PROXY	PADCONFIG23_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG23_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG23_WK_LVL_EN_PROXY	RESERVED			PADCONFIG23_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6662. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG23_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG23_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG23_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG23_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG23_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6662. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG23_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG23_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG23_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG23_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG23_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG23_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG23_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG23_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG23_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG23_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG23_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.218 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Register

14.2.1.2.1.2.2.218.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Register (Offset = 6060h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6663. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6060h

Figure 14-3317. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG24_LOCK_PROXY	PADCONFIG24_WKUP_EVT_PROXY	PADCONFIG24_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG24_ISO_BYP_PROXY	PADCONFIG24_ISO_OVR_PROXY	PADCONFIG24_TX_DIS_PROXY	PADCONFIG24_DRV_STR_PROXY		PADCONFIG24_RXACTIVE_PROXY	PADCONFIG24_PULLTYPESEL_PROXY	PADCONFIG24_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG24_ST_EN_PROXY	PADCONFIG24_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG24_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG24_WK_LVL_EN_PROXY	RESERVED			PADCONFIG24_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6664. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG24_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG24_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG24_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG24_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG24_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6664. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG24_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG24_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG24_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG24_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG24_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG24_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG24_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG24_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG24_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG24_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG24_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.219 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Register

14.2.1.2.1.2.2.219.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Register (Offset = 6064h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6665. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6064h

Figure 14-3318. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG25_LOCK_PROXY	PADCONFIG25_WKUP_EVT_PROXY	PADCONFIG25_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG25_ISO_BYP_PROXY	PADCONFIG25_ISO_OVR_PROXY	PADCONFIG25_TX_DIS_PROXY	PADCONFIG25_DRV_STR_PROXY		PADCONFIG25_RXACTIVE_PROXY	PADCONFIG25_PULLTYPESEL_PROXY	PADCONFIG25_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG25_ST_EN_PROXY	PADCONFIG25_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG25_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG25_WK_LVL_EN_PROXY	RESERVED			PADCONFIG25_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6666. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG25_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG25_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG25_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG25_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG25_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6666. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG25_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG25_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG25_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG25_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG25_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG25_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG25_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG25_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG25_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG25_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG25_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.220 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Register

14.2.1.2.1.2.2.220.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Register (Offset = 6068h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6667. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6068h

Figure 14-3319. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG26_LOCK_PROXY	PADCONFIG26_WKUP_EVT_PROXY	PADCONFIG26_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG26_ISO_BYP_PROXY	PADCONFIG26_ISO_OVR_PROXY	PADCONFIG26_TX_DIS_PROXY	PADCONFIG26_DRV_STR_PROXY		PADCONFIG26_RXACTIVE_PROXY	PADCONFIG26_PULLTYPESEL_PROXY	PADCONFIG26_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG26_ST_EN_PROXY	PADCONFIG26_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG26_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG26_WK_LVL_EN_PROXY	RESERVED			PADCONFIG26_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6668. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG26_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG26_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG26_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG26_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG26_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6668. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG26_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG26_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG26_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG26_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG26_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG26_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG26_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG26_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG26_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG26_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG26_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.221 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Register

14.2.1.2.1.2.2.221.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Register (Offset = 606Ch) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6669. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 606Ch

Figure 14-3320. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG27_LOCK_PROXY	PADCONFIG27_WKUP_EVT_PROXY	PADCONFIG27_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG27_ISO_BYP_PROXY	PADCONFIG27_ISO_OVR_PROXY	PADCONFIG27_TX_DIS_PROXY	PADCONFIG27_DRV_STR_PROXY		PADCONFIG27_RXACTIVE_PROXY	PADCONFIG27_PULLTYPESEL_PROXY	PADCONFIG27_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG27_ST_EN_PROXY	PADCONFIG27_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG27_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG27_WK_LVL_EN_PROXY	RESERVED			PADCONFIG27_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6670. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG27_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG27_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG27_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG27_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG27_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6670. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG27_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG27_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG27_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG27_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG27_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG27_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG27_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG27_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG27_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG27_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG27_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.222 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Register

14.2.1.2.1.2.2.222.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Register (Offset = 6070h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6671. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6070h

Figure 14-3321. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG28_LOCK_PROXY	PADCONFIG28_WKUP_EVT_PROXY	PADCONFIG28_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG28_ISO_BYP_PROXY	PADCONFIG28_ISO_OVR_PROXY	PADCONFIG28_TX_DIS_PROXY	PADCONFIG28_DRV_STR_PROXY		PADCONFIG28_RXACTIVE_PROXY	PADCONFIG28_PULLTYPESEL_PROXY	PADCONFIG28_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG28_ST_EN_PROXY	PADCONFIG28_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG28_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG28_WK_LVL_EN_PROXY	RESERVED			PADCONFIG28_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6672. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG28_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG28_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG28_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG28_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG28_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6672. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG28_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG28_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG28_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG28_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG28_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG28_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG28_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG28_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG28_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG28_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG28_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.223 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Register

14.2.1.2.1.2.2.223.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Register (Offset = 6074h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6673. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6074h

Figure 14-3322. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG29_LOCK_PROXY	PADCONFIG29_WKUP_EVT_PROXY	PADCONFIG29_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG29_ISO_BYP_PROXY	PADCONFIG29_ISO_OVR_PROXY	PADCONFIG29_TX_DIS_PROXY	PADCONFIG29_DRV_STR_PROXY		PADCONFIG29_RXACTIVE_PROXY	PADCONFIG29_PULLTYPESEL_PROXY	PADCONFIG29_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG29_ST_EN_PROXY	PADCONFIG29_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG29_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG29_WK_LVL_EN_PROXY	RESERVED			PADCONFIG29_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6674. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG29_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG29_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG29_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG29_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG29_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6674. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG29_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG29_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG29_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG29_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG29_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG29_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG29_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG29_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG29_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG29_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG29_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.224 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Register

14.2.1.2.1.2.2.224.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Register (Offset = 6078h) [reset = 8254007h]

Register to control pin configuration and muxing

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Table 14-6675. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6078h

Figure 14-3323. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG30_LOCK_PROXY	PADCONFIG30_WKUP_EVT_PROXY	PADCONFIG30_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG30_ISO_BYP_PROXY	PADCONFIG30_ISO_OVR_PROXY	PADCONFIG30_TX_DIS_PROXY	PADCONFIG30_DRV_STR_PROXY		PADCONFIG30_RXACTIVE_PROXY	PADCONFIG30_PULLTYPESEL_PROXY	PADCONFIG30_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		1h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG30_ST_EN_PROXY	PADCONFIG30_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG30_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG30_WK_LVL_EN_PROXY	RESERVED			PADCONFIG30_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6676. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG30_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG30_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG30_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG30_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG30_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6676. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG30_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG30_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG30_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG30_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG30_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG30_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG30_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG30_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG30_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG30_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG30_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.225 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Register

14.2.1.2.1.2.2.225.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Register (Offset = 607Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6677. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 607Ch

Figure 14-3324. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG31_LOCK_PROXY	PADCONFIG31_WKUP_EVT_PROXY	PADCONFIG31_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG31_ISO_BYP_PROXY	PADCONFIG31_ISO_OVR_PROXY	PADCONFIG31_TX_DIS_PROXY	PADCONFIG31_DRV_STR_PROXY		PADCONFIG31_RXACTIVE_PROXY	PADCONFIG31_PULLTYPESEL_PROXY	PADCONFIG31_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG31_ST_EN_PROXY	PADCONFIG31_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG31_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG31_WK_LVL_EN_PROXY	RESERVED			PADCONFIG31_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6678. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG31_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG31_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG31_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG31_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG31_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6678. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG31_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG31_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG31_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG31_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG31_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG31_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG31_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG31_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG31_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG31_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG31_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.226 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Register

14.2.1.2.1.2.2.226.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Register (Offset = 6084h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6679. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6084h

Figure 14-3325. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG33_LOCK_PROXY	PADCONFIG33_WKUP_EVT_PROXY	PADCONFIG33_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG33_ISO_BYP_PROXY	PADCONFIG33_ISO_OVR_PROXY	PADCONFIG33_TX_DIS_PROXY	PADCONFIG33_DRV_STR_PROXY		PADCONFIG33_RXACTIVE_PROXY	PADCONFIG33_PULLTYPESEL_PROXY	PADCONFIG33_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG33_ST_EN_PROXY	PADCONFIG33_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG33_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG33_WK_LVL_EN_PROXY	RESERVED			PADCONFIG33_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6680. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG33_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG33_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG33_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG33_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG33_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6680. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG33_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG33_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG33_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG33_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG33_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG33_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG33_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG33_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG33_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG33_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG33_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.227 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34_PROXY Register

14.2.1.2.1.2.2.227.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34_PROXY Register (Offset = 6088h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6681. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6088h

Figure 14-3326. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG34_LOCK_PROXY	PADCONFIG34_WKUP_EVT_PROXY	PADCONFIG34_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG34_ISO_BYP_PROXY	PADCONFIG34_ISO_OVR_PROXY	PADCONFIG34_TX_DIS_PROXY	PADCONFIG34_DRV_STR_PROXY		PADCONFIG34_RXACTIVE_PROXY	PADCONFIG34_PULLTYPESEL_PROXY	PADCONFIG34_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG34_ST_EN_PROXY	PADCONFIG34_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG34_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG34_WK_LVL_EN_PROXY	RESERVED			PADCONFIG34_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6682. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG34_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG34_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG34_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG34_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG34_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6682. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG34_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG34_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG34_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG34_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG34_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG34_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG34_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG34_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG34_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG34_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG34_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.228 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35_PROXY Register

14.2.1.2.1.2.2.228.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35_PROXY Register (Offset = 608Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6683. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 608Ch

Figure 14-3327. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG35_LOCK_PROXY	PADCONFIG35_WKUP_EVT_PROXY	PADCONFIG35_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG35_ISO_BYP_PROXY	PADCONFIG35_ISO_OVR_PROXY	PADCONFIG35_TX_DIS_PROXY	PADCONFIG35_DRV_STR_PROXY		PADCONFIG35_RXACTIVE_PROXY	PADCONFIG35_PULLTYPESEL_PROXY	PADCONFIG35_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG35_ST_EN_PROXY	PADCONFIG35_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG35_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG35_WK_LVL_EN_PROXY	RESERVED			PADCONFIG35_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6684. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG35_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG35_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG35_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG35_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG35_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6684. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG35_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG35_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG35_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG35_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG35_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG35_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG35_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG35_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG35_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG35_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG35_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.229 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36_PROXY Register

14.2.1.2.1.2.2.229.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36_PROXY Register (Offset = 6090h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6685. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6090h

Figure 14-3328. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG36_LOCK_PROXY	PADCONFIG36_WKUP_EVT_PROXY	PADCONFIG36_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG36_ISO_BYP_PROXY	PADCONFIG36_ISO_OVR_PROXY	PADCONFIG36_TX_DIS_PROXY	PADCONFIG36_DRV_STR_PROXY		PADCONFIG36_RXACTIVE_PROXY	PADCONFIG36_PULLTYPESEL_PROXY	PADCONFIG36_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG36_ST_EN_PROXY	PADCONFIG36_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG36_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG36_WK_LVL_EN_PROXY	RESERVED			PADCONFIG36_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6686. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG36_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG36_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG36_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG36_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG36_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6686. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG36_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG36_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG36_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG36_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG36_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG36_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG36_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG36_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG36_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG36_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG36_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.230 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37_PROXY Register

14.2.1.2.1.2.2.230.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37_PROXY Register (Offset = 6094h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6687. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6094h

Figure 14-3329. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG37_LOCK_PROXY	PADCONFIG37_WKUP_EVT_PROXY	PADCONFIG37_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG37_ISO_BYP_PROXY	PADCONFIG37_ISO_OVR_PROXY	PADCONFIG37_TX_DIS_PROXY	PADCONFIG37_DRV_STR_PROXY		PADCONFIG37_RXACTIVE_PROXY	PADCONFIG37_PULLTYPESEL_PROXY	PADCONFIG37_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG37_ST_EN_PROXY	PADCONFIG37_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG37_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG37_WK_LVL_EN_PROXY	RESERVED			PADCONFIG37_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6688. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG37_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG37_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG37_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG37_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG37_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6688. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG37_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG37_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG37_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG37_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG37_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG37_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG37_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG37_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG37_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG37_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG37_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.231 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38_PROXY Register

14.2.1.2.1.2.2.231.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38_PROXY Register (Offset = 6098h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6689. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6098h

Figure 14-3330. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG38_LOCK_PROXY	PADCONFIG38_WKUP_EVT_PROXY	PADCONFIG38_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG38_ISO_BYP_PROXY	PADCONFIG38_ISO_OVR_PROXY	PADCONFIG38_TX_DIS_PROXY	PADCONFIG38_DRV_STR_PROXY		PADCONFIG38_RXACTIVE_PROXY	PADCONFIG38_PULLTYPESEL_PROXY	PADCONFIG38_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG38_ST_EN_PROXY	PADCONFIG38_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG38_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG38_WK_LVL_EN_PROXY	RESERVED			PADCONFIG38_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6690. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG38_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG38_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG38_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG38_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG38_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6690. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG38_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG38_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG38_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG38_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG38_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG38_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG38_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG38_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG38_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG38_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG38_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.232 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39_PROXY Register

14.2.1.2.1.2.2.232.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39_PROXY Register (Offset = 609Ch) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6691. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 609Ch

Figure 14-3331. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG39_LOCK_PROXY	PADCONFIG39_WKUP_EVT_PROXY	PADCONFIG39_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG39_ISO_BYP_PROXY	PADCONFIG39_ISO_OVR_PROXY	PADCONFIG39_TX_DIS_PROXY	PADCONFIG39_DRV_STR_PROXY		PADCONFIG39_RXACTIVE_PROXY	PADCONFIG39_PULLTYPESEL_PROXY	PADCONFIG39_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG39_ST_EN_PROXY	PADCONFIG39_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG39_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG39_WK_LVL_EN_PROXY	RESERVED			PADCONFIG39_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6692. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG39_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG39_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG39_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG39_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG39_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6692. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG39_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG39_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG39_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG39_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG39_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG39_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG39_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG39_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG39_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG39_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG39_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.233 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40_PROXY Register

14.2.1.2.1.2.2.233.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40_PROXY Register (Offset = 60A0h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6693. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60A0h

Figure 14-3332. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG40_LOCK_PROXY</td><td>PADCONFIG40_WKUP_EVT_PROXY</td><td>PADCONFIG40_WKUP_EN_PROXY</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG40_ISO_BYP_PROXY</td><td>PADCONFIG40_ISO_OVR_PROXY</td><td>PADCONFIG40_TX_DIS_PROXY</td><td colspan="2">PADCONFIG40_DRV_STR_PROXY</td><td>PADCONFIG40_RXACTIVE_PROXY</td><td>PADCONFIG40_PULLTYPESEL_PROXY</td><td>PADCONFIG40_PULLUDEN_PROXY</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG40_ST_EN_PROXY</td><td colspan="3">PADCONFIG40_DEBOUNCE_SEL_PROXY</td><td colspan="2">RESERVED</td><td>PADCONFIG40_WK_LVL_POL_PROXY</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG40_WK_LVL_EN_PROXY</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG40_MUXMODE_PROXY</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-6694. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG40_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG40_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG40_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG40_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG40_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6694. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG40_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG40_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG40_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG40_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG40_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG40_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG40_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG40_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG40_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG40_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG40_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.234 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41_PROXY Register

14.2.1.2.1.2.2.234.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41_PROXY Register (Offset = 60A4h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6695. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60A4h

Figure 14-3333. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG41_LOCK_PROXY	PADCONFIG41_WKUP_EVT_PROXY	PADCONFIG41_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG41_ISO_BYP_PROXY	PADCONFIG41_ISO_OVR_PROXY	PADCONFIG41_TX_DIS_PROXY	PADCONFIG41_DRV_STR_PROXY		PADCONFIG41_RXACTIVE_PROXY	PADCONFIG41_PULLTYPESEL_PROXY	PADCONFIG41_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG41_ST_EN_PROXY	PADCONFIG41_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG41_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG41_WK_LVL_EN_PROXY	RESERVED			PADCONFIG41_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6696. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG41_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG41_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG41_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG41_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG41_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6696. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG41_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG41_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG41_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG41_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG41_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG41_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG41_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG41_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG41_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG41_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG41_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.235 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42_PROXY Register

14.2.1.2.1.2.2.235.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42_PROXY Register (Offset = 60A8h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6697. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60A8h

Figure 14-3334. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG42_LOCK_PROXY	PADCONFIG42_WKUP_EVT_PROXY	PADCONFIG42_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG42_ISO_BYP_PROXY	PADCONFIG42_ISO_OVR_PROXY	PADCONFIG42_TX_DIS_PROXY	PADCONFIG42_DRV_STR_PROXY		PADCONFIG42_RXACTIVE_PROXY	PADCONFIG42_PULLTYPESEL_PROXY	PADCONFIG42_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG42_ST_EN_PROXY	PADCONFIG42_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG42_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG42_WK_LVL_EN_PROXY	RESERVED			PADCONFIG42_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6698. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG42_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG42_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG42_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG42_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG42_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6698. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG42_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG42_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG42_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG42_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG42_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG42_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG42_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG42_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG42_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG42_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG42_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.236 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43_PROXY Register

14.2.1.2.1.2.2.236.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43_PROXY Register (Offset = 60ACh) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6699. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60ACh

Figure 14-3335. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG43_LOCK_PROXY	PADCONFIG43_WKUP_EVT_PROXY	PADCONFIG43_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG43_ISO_BYP_PROXY	PADCONFIG43_ISO_OVR_PROXY	PADCONFIG43_TX_DIS_PROXY	PADCONFIG43_DRV_STR_PROXY		PADCONFIG43_RXACTIVE_PROXY	PADCONFIG43_PULLTYPESEL_PROXY	PADCONFIG43_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG43_ST_EN_PROXY	PADCONFIG43_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG43_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG43_WK_LVL_EN_PROXY	RESERVED			PADCONFIG43_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6700. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG43_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG43_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG43_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG43_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG43_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6700. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG43_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG43_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG43_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG43_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG43_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG43_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG43_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG43_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG43_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG43_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG43_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.237 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44_PROXY Register

14.2.1.2.1.2.2.237.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44_PROXY Register (Offset = 60B0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6701. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60B0h

Figure 14-3336. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG44_LOCK_PROXY	PADCONFIG44_WKUP_EVT_PROXY	PADCONFIG44_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG44_ISO_BYP_PROXY	PADCONFIG44_ISO_OVR_PROXY	PADCONFIG44_TX_DIS_PROXY	PADCONFIG44_DRV_STR_PROXY		PADCONFIG44_RXACTIVE_PROXY	PADCONFIG44_PULLTYPESEL_PROXY	PADCONFIG44_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG44_ST_EN_PROXY	PADCONFIG44_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG44_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG44_WK_LVL_EN_PROXY	RESERVED			PADCONFIG44_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6702. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG44_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG44_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG44_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG44_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG44_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6702. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG44_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG44_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG44_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG44_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG44_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG44_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG44_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG44_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG44_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG44_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG44_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.238 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45_PROXY Register

14.2.1.2.1.2.2.238.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45_PROXY Register (Offset = 60B4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6703. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60B4h

Figure 14-3337. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG45_LOCK_PROXY	PADCONFIG45_WKUP_EVT_PROXY	PADCONFIG45_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG45_ISO_BYP_PROXY	PADCONFIG45_ISO_OVR_PROXY	PADCONFIG45_TX_DIS_PROXY	PADCONFIG45_DRV_STR_PROXY		PADCONFIG45_RXACTIVE_PROXY	PADCONFIG45_PULLTYPESEL_PROXY	PADCONFIG45_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG45_ST_EN_PROXY	PADCONFIG45_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG45_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG45_WK_LVL_EN_PROXY	RESERVED			PADCONFIG45_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6704. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG45_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG45_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG45_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG45_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG45_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6704. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG45_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG45_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG45_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG45_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG45_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG45_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG45_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG45_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG45_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG45_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG45_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.239 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46_PROXY Register

14.2.1.2.1.2.2.239.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46_PROXY Register (Offset = 60B8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6705. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60B8h

Figure 14-3338. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG46_LOCK_PROXY	PADCONFIG46_WKUP_EVT_PROXY	PADCONFIG46_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG46_ISO_BYP_PROXY	PADCONFIG46_ISO_OVR_PROXY	PADCONFIG46_TX_DIS_PROXY	PADCONFIG46_DRV_STR_PROXY		PADCONFIG46_RXACTIVE_PROXY	PADCONFIG46_PULLTYPESEL_PROXY	PADCONFIG46_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG46_ST_EN_PROXY	PADCONFIG46_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG46_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG46_WK_LVL_EN_PROXY	RESERVED			PADCONFIG46_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6706. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG46_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG46_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG46_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG46_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG46_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6706. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG46_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG46_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG46_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG46_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG46_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG46_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG46_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG46_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG46_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG46_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG46_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.240 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47_PROXY Register

14.2.1.2.1.2.2.240.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47_PROXY Register (Offset = 60BCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6707. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60BCh

Figure 14-3339. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG47_LOCK_PROXY	PADCONFIG47_WKUP_EVT_PROXY	PADCONFIG47_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG47_ISO_BYP_PROXY	PADCONFIG47_ISO_OVR_PROXY	PADCONFIG47_TX_DIS_PROXY	PADCONFIG47_DRV_STR_PROXY		PADCONFIG47_RXACTIVE_PROXY	PADCONFIG47_PULLTYPESEL_PROXY	PADCONFIG47_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG47_ST_EN_PROXY	PADCONFIG47_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG47_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG47_WK_LVL_EN_PROXY	RESERVED			PADCONFIG47_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6708. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG47_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG47_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG47_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG47_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG47_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6708. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG47_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG47_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG47_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG47_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG47_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG47_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG47_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG47_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG47_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG47_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG47_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.241 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48_PROXY Register

14.2.1.2.1.2.2.241.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48_PROXY Register (Offset = 60C0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6709. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60C0h

Figure 14-3340. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG48_LOCK_PROXY	PADCONFIG48_WKUP_EVT_PROXY	PADCONFIG48_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG48_ISO_BYP_PROXY	PADCONFIG48_ISO_OVR_PROXY	PADCONFIG48_TX_DIS_PROXY	PADCONFIG48_DRV_STR_PROXY		PADCONFIG48_RXACTIVE_PROXY	PADCONFIG48_PULLTYPESEL_PROXY	PADCONFIG48_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG48_ST_EN_PROXY	PADCONFIG48_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG48_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG48_WK_LVL_EN_PROXY	RESERVED			PADCONFIG48_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6710. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG48_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG48_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG48_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG48_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG48_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6710. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG48_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG48_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG48_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG48_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG48_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG48_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG48_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG48_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG48_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG48_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG48_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.242 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49_PROXY Register

14.2.1.2.1.2.2.242.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49_PROXY Register (Offset = 60C4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6711. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60C4h

Figure 14-3341. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG49_LOCK_PROXY	PADCONFIG49_WKUP_EVT_PROXY	PADCONFIG49_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG49_ISO_BYP_PROXY	PADCONFIG49_ISO_OVR_PROXY	PADCONFIG49_TX_DIS_PROXY	PADCONFIG49_DRV_STR_PROXY		PADCONFIG49_RXACTIVE_PROXY	PADCONFIG49_PULLTYPESEL_PROXY	PADCONFIG49_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG49_ST_EN_PROXY	PADCONFIG49_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG49_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG49_WK_LVL_EN_PROXY	RESERVED			PADCONFIG49_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6712. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG49_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG49_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG49_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG49_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG49_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6712. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG49_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG49_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG49_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG49_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG49_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG49_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG49_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG49_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG49_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG49_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG49_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.243 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50_PROXY Register

14.2.1.2.1.2.2.243.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50_PROXY Register (Offset = 60C8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6713. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60C8h

Figure 14-3342. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG50_LOCK_PROXY	PADCONFIG50_WKUP_EVT_PROXY	PADCONFIG50_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG50_ISO_BYP_PROXY	PADCONFIG50_ISO_OVR_PROXY	PADCONFIG50_TX_DIS_PROXY	PADCONFIG50_DRV_STR_PROXY		PADCONFIG50_RXACTIVE_PROXY	PADCONFIG50_PULLTYPESEL_PROXY	PADCONFIG50_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG50_ST_EN_PROXY	PADCONFIG50_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG50_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG50_WK_LVL_EN_PROXY	RESERVED			PADCONFIG50_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6714. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG50_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG50_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG50_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG50_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG50_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6714. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG50_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG50_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG50_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG50_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG50_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG50_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG50_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG50_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG50_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG50_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG50_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.244 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51_PROXY Register

14.2.1.2.1.2.2.244.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51_PROXY Register (Offset = 60CCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6715. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60CCh

Figure 14-3343. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG51_LOCK_PROXY	PADCONFIG51_WKUP_EVT_PROXY	PADCONFIG51_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG51_ISO_BYP_PROXY	PADCONFIG51_ISO_OVR_PROXY	PADCONFIG51_TX_DIS_PROXY	PADCONFIG51_DRV_STR_PROXY		PADCONFIG51_RXACTIVE_PROXY	PADCONFIG51_PULLTYPESEL_PROXY	PADCONFIG51_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG51_ST_EN_PROXY	PADCONFIG51_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG51_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG51_WK_LVL_EN_PROXY	RESERVED			PADCONFIG51_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6716. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG51_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG51_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG51_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG51_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG51_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6716. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG51_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG51_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG51_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG51_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG51_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG51_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG51_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG51_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG51_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG51_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG51_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.245 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52_PROXY Register

14.2.1.2.1.2.2.245.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52_PROXY Register (Offset = 60D0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6717. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60D0h

Figure 14-3344. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG52_LOCK_PROXY	PADCONFIG52_WKUP_EVT_PROXY	PADCONFIG52_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG52_ISO_BYP_PROXY	PADCONFIG52_ISO_OVR_PROXY	PADCONFIG52_TX_DIS_PROXY	PADCONFIG52_DRV_STR_PROXY		PADCONFIG52_RXACTIVE_PROXY	PADCONFIG52_PULLTYPESEL_PROXY	PADCONFIG52_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG52_ST_EN_PROXY	PADCONFIG52_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG52_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG52_WK_LVL_EN_PROXY	RESERVED			PADCONFIG52_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6718. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG52_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG52_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG52_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG52_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG52_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6718. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG52_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG52_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG52_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG52_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG52_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG52_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG52_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG52_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG52_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG52_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG52_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.246 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53_PROXY Register

14.2.1.2.1.2.2.246.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53_PROXY Register (Offset = 60D4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6719. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60D4h

Figure 14-3345. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG53_LOCK_PROXY	PADCONFIG53_WKUP_EVT_PROXY	PADCONFIG53_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG53_ISO_BYP_PROXY	PADCONFIG53_ISO_OVR_PROXY	PADCONFIG53_TX_DIS_PROXY	PADCONFIG53_DRV_STR_PROXY		PADCONFIG53_RXACTIVE_PROXY	PADCONFIG53_PULLTYPESEL_PROXY	PADCONFIG53_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG53_ST_EN_PROXY	PADCONFIG53_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG53_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG53_WK_LVL_EN_PROXY	RESERVED			PADCONFIG53_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6720. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG53_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG53_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG53_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG53_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG53_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6720. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG53_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG53_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG53_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG53_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG53_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG53_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG53_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG53_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG53_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG53_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG53_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.247 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56_PROXY Register

14.2.1.2.1.2.2.247.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56_PROXY Register (Offset = 60E0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6721. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60E0h

Figure 14-3346. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG56_LOCK_PROXY	PADCONFIG56_WKUP_EVT_PROXY	PADCONFIG56_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG56_ISO_BYP_PROXY	PADCONFIG56_ISO_OVR_PROXY	PADCONFIG56_TX_DIS_PROXY	PADCONFIG56_DRV_STR_PROXY		PADCONFIG56_RXACTIVE_PROXY	PADCONFIG56_PULLTYPESEL_PROXY	PADCONFIG56_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG56_ST_EN_PROXY	PADCONFIG56_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG56_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG56_WK_LVL_EN_PROXY	RESERVED			PADCONFIG56_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6722. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG56_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG56_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG56_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG56_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG56_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6722. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG56_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG56_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG56_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG56_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG56_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG56_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG56_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG56_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG56_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG56_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG56_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.248 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57_PROXY Register

14.2.1.2.1.2.2.248.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57_PROXY Register (Offset = 60E4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6723. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60E4h

Figure 14-3347. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG57_LOCK_PROXY	PADCONFIG57_WKUP_EVT_PROXY	PADCONFIG57_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG57_ISO_BYP_PROXY	PADCONFIG57_ISO_OVR_PROXY	PADCONFIG57_TX_DIS_PROXY	PADCONFIG57_DRV_STR_PROXY		PADCONFIG57_RXACTIVE_PROXY	PADCONFIG57_PULLTYPESEL_PROXY	PADCONFIG57_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG57_ST_EN_PROXY	PADCONFIG57_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG57_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG57_WK_LVL_EN_PROXY	RESERVED			PADCONFIG57_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6724. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG57_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG57_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG57_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG57_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG57_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6724. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG57_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG57_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG57_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG57_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG57_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG57_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG57_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG57_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG57_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG57_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG57_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.249 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58_PROXY Register

14.2.1.2.1.2.2.249.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58_PROXY Register (Offset = 60E8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6725. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60E8h

Figure 14-3348. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG58_LOCK_PROXY	PADCONFIG58_WKUP_EVT_PROXY	PADCONFIG58_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG58_ISO_BYP_PROXY	PADCONFIG58_ISO_OVR_PROXY	PADCONFIG58_TX_DIS_PROXY	PADCONFIG58_DRV_STR_PROXY		PADCONFIG58_RXACTIVE_PROXY	PADCONFIG58_PULLTYPESEL_PROXY	PADCONFIG58_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG58_ST_EN_PROXY	PADCONFIG58_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG58_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG58_WK_LVL_EN_PROXY	RESERVED			PADCONFIG58_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6726. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG58_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG58_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG58_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG58_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG58_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6726. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG58_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG58_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG58_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG58_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG58_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG58_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG58_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG58_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG58_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG58_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG58_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.250 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59_PROXY Register

14.2.1.2.1.2.2.250.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59_PROXY Register (Offset = 60ECh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6727. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60ECh

Figure 14-3349. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG59_LOCK_PROXY	PADCONFIG59_WKUP_EVT_PROXY	PADCONFIG59_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG59_ISO_BYP_PROXY	PADCONFIG59_ISO_OVR_PROXY	PADCONFIG59_TX_DIS_PROXY	PADCONFIG59_DRV_STR_PROXY		PADCONFIG59_RXACTIVE_PROXY	PADCONFIG59_PULLTYPESEL_PROXY	PADCONFIG59_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG59_ST_EN_PROXY	PADCONFIG59_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG59_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG59_WK_LVL_EN_PROXY	RESERVED			PADCONFIG59_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6728. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG59_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG59_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG59_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG59_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG59_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6728. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG59_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG59_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG59_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG59_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG59_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG59_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG59_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG59_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG59_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG59_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG59_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.251 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60_PROXY Register

14.2.1.2.1.2.2.251.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60_PROXY Register (Offset = 60F0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6729. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60F0h

Figure 14-3350. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG60_LOCK_PROXY	PADCONFIG60_WKUP_EVT_PROXY	PADCONFIG60_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG60_ISO_BYP_PROXY	PADCONFIG60_ISO_OVR_PROXY	PADCONFIG60_TX_DIS_PROXY	PADCONFIG60_DRV_STR_PROXY		PADCONFIG60_RXACTIVE_PROXY	PADCONFIG60_PULLTYPESEL_PROXY	PADCONFIG60_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG60_ST_EN_PROXY	PADCONFIG60_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG60_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG60_WK_LVL_EN_PROXY	RESERVED			PADCONFIG60_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6730. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG60_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG60_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG60_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG60_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG60_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6730. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG60_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG60_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG60_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG60_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG60_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG60_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG60_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG60_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG60_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG60_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG60_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.252 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63_PROXY Register

14.2.1.2.1.2.2.252.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63_PROXY Register (Offset = 60FCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6731. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 60FCh

Figure 14-3351. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG63_LOCK_PROXY	PADCONFIG63_WKUP_EVT_PROXY	PADCONFIG63_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG63_ISO_BYP_PROXY	PADCONFIG63_ISO_OVR_PROXY	PADCONFIG63_TX_DIS_PROXY	PADCONFIG63_DRV_STR_PROXY		PADCONFIG63_RXACTIVE_PROXY	PADCONFIG63_PULLTYPESEL_PROXY	PADCONFIG63_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG63_ST_EN_PROXY	PADCONFIG63_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG63_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG63_WK_LVL_EN_PROXY	RESERVED			PADCONFIG63_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6732. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG63_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG63_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG63_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG63_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG63_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6732. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG63_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG63_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG63_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG63_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG63_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG63_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG63_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG63_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG63_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG63_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG63_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.253 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64_PROXY Register

14.2.1.2.1.2.2.253.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64_PROXY Register (Offset = 6100h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6733. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6100h

Figure 14-3352. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG64_LOCK_PROXY	PADCONFIG64_WKUP_EVT_PROXY	PADCONFIG64_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG64_ISO_BYP_PROXY	PADCONFIG64_ISO_OVR_PROXY	PADCONFIG64_TX_DIS_PROXY	PADCONFIG64_DRV_STR_PROXY		PADCONFIG64_RXACTIVE_PROXY	PADCONFIG64_PULLTYPESEL_PROXY	PADCONFIG64_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG64_ST_EN_PROXY	PADCONFIG64_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG64_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG64_WK_LVL_EN_PROXY	RESERVED			PADCONFIG64_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6734. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG64_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG64_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG64_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG64_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG64_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6734. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG64_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG64_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG64_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG64_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG64_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG64_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG64_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG64_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG64_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG64_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG64_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.254 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65_PROXY Register

14.2.1.2.1.2.2.254.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65_PROXY Register (Offset = 6104h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6735. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6104h

Figure 14-3353. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG65_LOCK_PROXY	PADCONFIG65_WKUP_EVT_PROXY	PADCONFIG65_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG65_ISO_BYP_PROXY	PADCONFIG65_ISO_OVR_PROXY	PADCONFIG65_TX_DIS_PROXY	PADCONFIG65_DRV_STR_PROXY		PADCONFIG65_RXACTIVE_PROXY	PADCONFIG65_PULLTYPESEL_PROXY	PADCONFIG65_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG65_ST_EN_PROXY	PADCONFIG65_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG65_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG65_WK_LVL_EN_PROXY	RESERVED			PADCONFIG65_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6736. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG65_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG65_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG65_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG65_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG65_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6736. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG65_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG65_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG65_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG65_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG65_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG65_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG65_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG65_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG65_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG65_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG65_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.255 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66_PROXY Register

14.2.1.2.1.2.2.255.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66_PROXY Register (Offset = 6108h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6737. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6108h

Figure 14-3354. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG66_LOCK_PROXY	PADCONFIG66_WKUP_EVT_PROXY	PADCONFIG66_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG66_ISO_BYP_PROXY	PADCONFIG66_ISO_OVR_PROXY	PADCONFIG66_TX_DIS_PROXY	PADCONFIG66_DRV_STR_PROXY		PADCONFIG66_RXACTIVE_PROXY	PADCONFIG66_PULLTYPESEL_PROXY	PADCONFIG66_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG66_ST_EN_PROXY	PADCONFIG66_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG66_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG66_WK_LVL_EN_PROXY	RESERVED			PADCONFIG66_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6738. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG66_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG66_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG66_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG66_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG66_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6738. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG66_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG66_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG66_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG66_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG66_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG66_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG66_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG66_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG66_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG66_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG66_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.256 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67_PROXY Register

14.2.1.2.1.2.2.256.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67_PROXY Register (Offset = 610Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6739. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 610Ch

Figure 14-3355. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG67_LOCK_PROXY	PADCONFIG67_WKUP_EVT_PROXY	PADCONFIG67_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG67_ISO_BYP_PROXY	PADCONFIG67_ISO_OVR_PROXY	PADCONFIG67_TX_DIS_PROXY	PADCONFIG67_DRV_STR_PROXY		PADCONFIG67_RXACTIVE_PROXY	PADCONFIG67_PULLTYPESEL_PROXY	PADCONFIG67_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG67_ST_EN_PROXY	PADCONFIG67_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG67_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG67_WK_LVL_EN_PROXY	RESERVED			PADCONFIG67_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6740. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG67_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG67_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG67_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG67_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG67_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6740. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG67_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG67_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG67_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG67_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG67_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG67_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG67_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG67_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG67_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG67_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG67_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.257 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68_PROXY Register

14.2.1.2.1.2.2.257.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68_PROXY Register (Offset = 6110h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6741. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6110h

Figure 14-3356. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG68_LOCK_PROXY	PADCONFIG68_WKUP_EVT_PROXY	PADCONFIG68_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG68_ISO_BYP_PROXY	PADCONFIG68_ISO_OVR_PROXY	PADCONFIG68_TX_DIS_PROXY	PADCONFIG68_DRV_STR_PROXY		PADCONFIG68_RXACTIVE_PROXY	PADCONFIG68_PULLTYPESEL_PROXY	PADCONFIG68_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG68_ST_EN_PROXY	PADCONFIG68_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG68_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG68_WK_LVL_EN_PROXY	RESERVED			PADCONFIG68_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6742. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG68_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG68_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG68_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG68_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG68_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6742. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG68_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG68_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG68_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG68_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG68_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG68_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG68_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG68_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG68_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG68_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG68_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.258 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69_PROXY Register

14.2.1.2.1.2.2.258.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69_PROXY Register (Offset = 6114h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6743. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6114h

Figure 14-3357. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG69_LOCK_PROXY	PADCONFIG69_WKUP_EVT_PROXY	PADCONFIG69_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG69_ISO_BYP_PROXY	PADCONFIG69_ISO_OVR_PROXY	PADCONFIG69_TX_DIS_PROXY	PADCONFIG69_DRV_STR_PROXY		PADCONFIG69_RXACTIVE_PROXY	PADCONFIG69_PULLTYPESEL_PROXY	PADCONFIG69_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG69_ST_EN_PROXY	PADCONFIG69_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG69_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG69_WK_LVL_EN_PROXY	RESERVED			PADCONFIG69_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6744. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG69_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG69_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG69_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG69_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG69_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6744. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG69_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG69_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG69_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG69_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG69_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG69_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG69_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG69_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG69_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG69_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG69_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.259 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70_PROXY Register

14.2.1.2.1.2.2.259.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70_PROXY Register (Offset = 6118h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6745. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6118h

Figure 14-3358. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG70_LOCK_PROXY	PADCONFIG70_WKUP_EVT_PROXY	PADCONFIG70_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG70_ISO_BYP_PROXY	PADCONFIG70_ISO_OVR_PROXY	PADCONFIG70_TX_DIS_PROXY	PADCONFIG70_DRV_STR_PROXY		PADCONFIG70_RXACTIVE_PROXY	PADCONFIG70_PULLTYPESEL_PROXY	PADCONFIG70_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG70_ST_EN_PROXY	PADCONFIG70_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG70_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG70_WK_LVL_EN_PROXY	RESERVED			PADCONFIG70_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6746. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG70_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG70_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG70_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG70_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG70_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6746. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG70_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG70_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG70_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG70_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG70_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG70_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG70_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG70_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG70_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG70_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG70_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.260 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71_PROXY Register

14.2.1.2.1.2.2.260.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71_PROXY Register (Offset = 611Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6747. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 611Ch

Figure 14-3359. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG71_LOCK_PROXY	PADCONFIG71_WKUP_EVT_PROXY	PADCONFIG71_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG71_ISO_BYP_PROXY	PADCONFIG71_ISO_OVR_PROXY	PADCONFIG71_TX_DIS_PROXY	PADCONFIG71_DRV_STR_PROXY		PADCONFIG71_RXACTIVE_PROXY	PADCONFIG71_PULLTYPESEL_PROXY	PADCONFIG71_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG71_ST_EN_PROXY	PADCONFIG71_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG71_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG71_WK_LVL_EN_PROXY	RESERVED			PADCONFIG71_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6748. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG71_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG71_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG71_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG71_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG71_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6748. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG71_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG71_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG71_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG71_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG71_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG71_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG71_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG71_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG71_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG71_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG71_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.261 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72_PROXY Register

14.2.1.2.1.2.2.261.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72_PROXY Register (Offset = 6120h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6749. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6120h

Figure 14-3360. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG72_LOCK_PROXY	PADCONFIG72_WKUP_EVT_PROXY	PADCONFIG72_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG72_ISO_BYP_PROXY	PADCONFIG72_ISO_OVR_PROXY	PADCONFIG72_TX_DIS_PROXY	PADCONFIG72_DRV_STR_PROXY		PADCONFIG72_RXACTIVE_PROXY	PADCONFIG72_PULLTYPESEL_PROXY	PADCONFIG72_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG72_ST_EN_PROXY	PADCONFIG72_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG72_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG72_WK_LVL_EN_PROXY	RESERVED			PADCONFIG72_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6750. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG72_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG72_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG72_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG72_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG72_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6750. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG72_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG72_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG72_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG72_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG72_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG72_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG72_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG72_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG72_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG72_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG72_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.262 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73_PROXY Register

14.2.1.2.1.2.2.262.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73_PROXY Register (Offset = 6124h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6751. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6124h

Figure 14-3361. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG73_LOCK_PROXY	PADCONFIG73_WKUP_EVT_PROXY	PADCONFIG73_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG73_ISO_BYP_PROXY	PADCONFIG73_ISO_OVR_PROXY	PADCONFIG73_TX_DIS_PROXY	PADCONFIG73_DRV_STR_PROXY		PADCONFIG73_RXACTIVE_PROXY	PADCONFIG73_PULLTYPESEL_PROXY	PADCONFIG73_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG73_ST_EN_PROXY	PADCONFIG73_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG73_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG73_WK_LVL_EN_PROXY	RESERVED			PADCONFIG73_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6752. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG73_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG73_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG73_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG73_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG73_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6752. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG73_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG73_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG73_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG73_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG73_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG73_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG73_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG73_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG73_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG73_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG73_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.263 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74_PROXY Register

14.2.1.2.1.2.2.263.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74_PROXY Register (Offset = 6128h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6753. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6128h

Figure 14-3362. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG74_LOCK_PROXY	PADCONFIG74_WKUP_EVT_PROXY	PADCONFIG74_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG74_ISO_BYP_PROXY	PADCONFIG74_ISO_OVR_PROXY	PADCONFIG74_TX_DIS_PROXY	PADCONFIG74_DRV_STR_PROXY		PADCONFIG74_RXACTIVE_PROXY	PADCONFIG74_PULLTYPESEL_PROXY	PADCONFIG74_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG74_ST_EN_PROXY	PADCONFIG74_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG74_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG74_WK_LVL_EN_PROXY	RESERVED			PADCONFIG74_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6754. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG74_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG74_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG74_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG74_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG74_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6754. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG74_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG74_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG74_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG74_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG74_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG74_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG74_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG74_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG74_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG74_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG74_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.264 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75_PROXY Register

14.2.1.2.1.2.2.264.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75_PROXY Register (Offset = 612Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6755. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 612Ch

Figure 14-3363. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG75_LOCK_PROXY	PADCONFIG75_WKUP_EVT_PROXY	PADCONFIG75_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG75_ISO_BYP_PROXY	PADCONFIG75_ISO_OVR_PROXY	PADCONFIG75_TX_DIS_PROXY	PADCONFIG75_DRV_STR_PROXY		PADCONFIG75_RXACTIVE_PROXY	PADCONFIG75_PULLTYPESEL_PROXY	PADCONFIG75_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG75_ST_EN_PROXY	PADCONFIG75_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG75_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG75_WK_LVL_EN_PROXY	RESERVED			PADCONFIG75_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6756. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG75_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG75_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG75_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG75_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG75_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6756. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG75_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG75_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG75_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG75_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG75_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG75_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG75_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG75_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG75_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG75_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG75_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.265 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76_PROXY Register

14.2.1.2.1.2.2.265.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76_PROXY Register (Offset = 6130h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6757. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6130h

Figure 14-3364. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG76_LOCK_PROXY	PADCONFIG76_WKUP_EVT_PROXY	PADCONFIG76_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG76_ISO_BYP_PROXY	PADCONFIG76_ISO_OVR_PROXY	PADCONFIG76_TX_DIS_PROXY	PADCONFIG76_DRV_STR_PROXY		PADCONFIG76_RXACTIVE_PROXY	PADCONFIG76_PULLTYPESEL_PROXY	PADCONFIG76_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG76_ST_EN_PROXY	PADCONFIG76_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG76_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG76_WK_LVL_EN_PROXY	RESERVED			PADCONFIG76_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6758. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG76_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG76_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG76_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG76_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG76_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6758. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG76_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG76_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG76_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG76_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG76_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG76_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG76_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG76_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG76_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG76_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG76_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.266 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77_PROXY Register

14.2.1.2.1.2.2.266.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77_PROXY Register (Offset = 6134h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6759. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6134h

Figure 14-3365. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG77_LOCK_PROXY	PADCONFIG77_WKUP_EVT_PROXY	PADCONFIG77_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG77_ISO_BYP_PROXY	PADCONFIG77_ISO_OVR_PROXY	PADCONFIG77_TX_DIS_PROXY	PADCONFIG77_DRV_STR_PROXY		PADCONFIG77_RXACTIVE_PROXY	PADCONFIG77_PULLTYPESEL_PROXY	PADCONFIG77_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG77_ST_EN_PROXY	PADCONFIG77_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG77_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG77_WK_LVL_EN_PROXY	RESERVED			PADCONFIG77_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6760. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG77_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG77_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG77_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG77_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG77_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6760. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG77_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG77_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG77_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG77_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG77_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG77_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG77_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG77_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG77_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG77_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG77_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.267 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78_PROXY Register

14.2.1.2.1.2.2.267.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78_PROXY Register (Offset = 6138h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6761. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6138h

Figure 14-3366. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG78_LOCK_PROXY	PADCONFIG78_WKUP_EVT_PROXY	PADCONFIG78_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG78_ISO_BYP_PROXY	PADCONFIG78_ISO_OVR_PROXY	PADCONFIG78_TX_DIS_PROXY	PADCONFIG78_DRV_STR_PROXY		PADCONFIG78_RXACTIVE_PROXY	PADCONFIG78_PULLTYPESEL_PROXY	PADCONFIG78_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG78_ST_EN_PROXY	PADCONFIG78_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG78_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG78_WK_LVL_EN_PROXY	RESERVED			PADCONFIG78_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6762. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG78_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG78_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG78_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG78_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG78_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6762. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG78_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG78_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG78_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG78_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG78_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG78_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG78_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG78_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG78_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG78_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG78_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.268 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79_PROXY Register

14.2.1.2.1.2.2.268.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79_PROXY Register (Offset = 613Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6763. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 613Ch

Figure 14-3367. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG79_LOCK_PROXY	PADCONFIG79_WKUP_EVT_PROXY	PADCONFIG79_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG79_ISO_BYP_PROXY	PADCONFIG79_ISO_OVR_PROXY	PADCONFIG79_TX_DIS_PROXY	PADCONFIG79_DRV_STR_PROXY		PADCONFIG79_RXACTIVE_PROXY	PADCONFIG79_PULLTYPESEL_PROXY	PADCONFIG79_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG79_ST_EN_PROXY	PADCONFIG79_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG79_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG79_WK_LVL_EN_PROXY	RESERVED			PADCONFIG79_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6764. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG79_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG79_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG79_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG79_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG79_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6764. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG79_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG79_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG79_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG79_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG79_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG79_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG79_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG79_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG79_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG79_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG79_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.269 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80_PROXY Register

14.2.1.2.1.2.2.269.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80_PROXY Register (Offset = 6140h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6765. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6140h

Figure 14-3368. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG80_LOCK_PROXY	PADCONFIG80_WKUP_EVT_PROXY	PADCONFIG80_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG80_ISO_BYP_PROXY	PADCONFIG80_ISO_OVR_PROXY	PADCONFIG80_TX_DIS_PROXY	PADCONFIG80_DRV_STR_PROXY		PADCONFIG80_RXACTIVE_PROXY	PADCONFIG80_PULLTYPESEL_PROXY	PADCONFIG80_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG80_ST_EN_PROXY	PADCONFIG80_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG80_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG80_WK_LVL_EN_PROXY	RESERVED			PADCONFIG80_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6766. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG80_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG80_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG80_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG80_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG80_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6766. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG80_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG80_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG80_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG80_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG80_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG80_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG80_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG80_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG80_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG80_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG80_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.270 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81_PROXY Register

14.2.1.2.1.2.2.270.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81_PROXY Register (Offset = 6144h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6767. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6144h

Figure 14-3369. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG81_LOCK_PROXY	PADCONFIG81_WKUP_EVT_PROXY	PADCONFIG81_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG81_ISO_BYP_PROXY	PADCONFIG81_ISO_OVR_PROXY	PADCONFIG81_TX_DIS_PROXY	PADCONFIG81_DRV_STR_PROXY		PADCONFIG81_RXACTIVE_PROXY	PADCONFIG81_PULLTYPESEL_PROXY	PADCONFIG81_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG81_ST_EN_PROXY	PADCONFIG81_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG81_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG81_WK_LVL_EN_PROXY	RESERVED			PADCONFIG81_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6768. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG81_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG81_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG81_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG81_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG81_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6768. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG81_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG81_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG81_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG81_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG81_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG81_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG81_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG81_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG81_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG81_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG81_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.271 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82_PROXY Register

14.2.1.2.1.2.2.271.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82_PROXY Register (Offset = 6148h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6769. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6148h

Figure 14-3370. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG82_LOCK_PROXY	PADCONFIG82_WKUP_EVT_PROXY	PADCONFIG82_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG82_ISO_BYP_PROXY	PADCONFIG82_ISO_OVR_PROXY	PADCONFIG82_TX_DIS_PROXY	PADCONFIG82_DRV_STR_PROXY		PADCONFIG82_RXACTIVE_PROXY	PADCONFIG82_PULLTYPESEL_PROXY	PADCONFIG82_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG82_ST_EN_PROXY	PADCONFIG82_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG82_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG82_WK_LVL_EN_PROXY	RESERVED			PADCONFIG82_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6770. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG82_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG82_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG82_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG82_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG82_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6770. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG82_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG82_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG82_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG82_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG82_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG82_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG82_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG82_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG82_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG82_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG82_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.272 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83_PROXY Register

14.2.1.2.1.2.2.272.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83_PROXY Register (Offset = 614Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6771. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 614Ch

Figure 14-3371. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG83_LOCK_PROXY	PADCONFIG83_WKUP_EVT_PROXY	PADCONFIG83_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG83_ISO_BYP_PROXY	PADCONFIG83_ISO_OVR_PROXY	PADCONFIG83_TX_DIS_PROXY	PADCONFIG83_DRV_STR_PROXY		PADCONFIG83_RXACTIVE_PROXY	PADCONFIG83_PULLTYPESEL_PROXY	PADCONFIG83_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG83_ST_EN_PROXY	PADCONFIG83_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG83_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG83_WK_LVL_EN_PROXY	RESERVED			PADCONFIG83_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6772. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG83_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG83_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG83_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG83_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG83_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6772. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG83_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG83_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG83_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG83_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG83_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG83_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG83_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG83_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG83_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG83_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG83_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.273 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84_PROXY Register

14.2.1.2.1.2.2.273.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84_PROXY Register (Offset = 6150h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6773. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6150h

Figure 14-3372. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG84_LOCK_PROXY	PADCONFIG84_WKUP_EVT_PROXY	PADCONFIG84_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG84_ISO_BYP_PROXY	PADCONFIG84_ISO_OVR_PROXY	PADCONFIG84_TX_DIS_PROXY	PADCONFIG84_DRV_STR_PROXY		PADCONFIG84_RXACTIVE_PROXY	PADCONFIG84_PULLTYPESEL_PROXY	PADCONFIG84_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG84_ST_EN_PROXY	PADCONFIG84_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG84_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG84_WK_LVL_EN_PROXY	RESERVED			PADCONFIG84_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6774. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG84_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG84_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG84_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG84_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG84_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6774. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG84_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG84_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG84_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG84_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG84_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG84_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG84_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG84_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG84_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG84_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG84_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.274 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85_PROXY Register

14.2.1.2.1.2.2.274.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85_PROXY Register (Offset = 6154h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6775. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6154h

Figure 14-3373. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG85_LOCK_PROXY	PADCONFIG85_WKUP_EVT_PROXY	PADCONFIG85_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG85_ISO_BYP_PROXY	PADCONFIG85_ISO_OVR_PROXY	PADCONFIG85_TX_DIS_PROXY	PADCONFIG85_DRV_STR_PROXY		PADCONFIG85_RXACTIVE_PROXY	PADCONFIG85_PULLTYPESEL_PROXY	PADCONFIG85_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG85_ST_EN_PROXY	PADCONFIG85_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG85_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG85_WK_LVL_EN_PROXY	RESERVED			PADCONFIG85_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6776. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG85_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG85_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG85_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG85_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG85_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6776. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG85_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG85_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG85_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG85_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG85_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG85_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG85_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG85_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG85_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG85_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG85_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.275 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86_PROXY Register

14.2.1.2.1.2.2.275.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86_PROXY Register (Offset = 6158h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6777. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6158h

Figure 14-3374. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG86_LOCK_PROXY	PADCONFIG86_WKUP_EVT_PROXY	PADCONFIG86_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG86_ISO_BYP_PROXY	PADCONFIG86_ISO_OVR_PROXY	PADCONFIG86_TX_DIS_PROXY	PADCONFIG86_DRV_STR_PROXY		PADCONFIG86_RXACTIVE_PROXY	PADCONFIG86_PULLTYPESEL_PROXY	PADCONFIG86_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG86_ST_EN_PROXY	PADCONFIG86_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG86_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG86_WK_LVL_EN_PROXY	RESERVED			PADCONFIG86_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6778. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG86_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG86_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG86_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG86_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG86_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6778. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG86_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG86_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG86_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG86_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG86_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG86_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG86_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG86_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG86_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG86_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG86_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.276 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87_PROXY Register

14.2.1.2.1.2.2.276.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87_PROXY Register (Offset = 615Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6779. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 615Ch

Figure 14-3375. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG87_LOCK_PROXY	PADCONFIG87_WKUP_EVT_PROXY	PADCONFIG87_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG87_ISO_BYP_PROXY	PADCONFIG87_ISO_OVR_PROXY	PADCONFIG87_TX_DIS_PROXY	PADCONFIG87_DRV_STR_PROXY		PADCONFIG87_RXACTIVE_PROXY	PADCONFIG87_PULLTYPESEL_PROXY	PADCONFIG87_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG87_ST_EN_PROXY	PADCONFIG87_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG87_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG87_WK_LVL_EN_PROXY	RESERVED			PADCONFIG87_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6780. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG87_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG87_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG87_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG87_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG87_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6780. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG87_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG87_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG87_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG87_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG87_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG87_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG87_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG87_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG87_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG87_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG87_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.277 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88_PROXY Register

14.2.1.2.1.2.2.277.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88_PROXY Register (Offset = 6160h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6781. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6160h

Figure 14-3376. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG88_LOCK_PROXY	PADCONFIG88_WKUP_EVT_PROXY	PADCONFIG88_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG88_ISO_BYP_PROXY	PADCONFIG88_ISO_OVR_PROXY	PADCONFIG88_TX_DIS_PROXY	PADCONFIG88_DRV_STR_PROXY		PADCONFIG88_RXACTIVE_PROXY	PADCONFIG88_PULLTYPESEL_PROXY	PADCONFIG88_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG88_ST_EN_PROXY	PADCONFIG88_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG88_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG88_WK_LVL_EN_PROXY	RESERVED			PADCONFIG88_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6782. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG88_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG88_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG88_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG88_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG88_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6782. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG88_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG88_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG88_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG88_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG88_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG88_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG88_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG88_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG88_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG88_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG88_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.278 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89_PROXY Register

14.2.1.2.1.2.2.278.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89_PROXY Register (Offset = 6164h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6783. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6164h

Figure 14-3377. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG89_LOCK_PROXY	PADCONFIG89_WKUP_EVT_PROXY	PADCONFIG89_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG89_ISO_BYP_PROXY	PADCONFIG89_ISO_OVR_PROXY	PADCONFIG89_TX_DIS_PROXY	PADCONFIG89_DRV_STR_PROXY		PADCONFIG89_RXACTIVE_PROXY	PADCONFIG89_PULLTYPESEL_PROXY	PADCONFIG89_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG89_ST_EN_PROXY	PADCONFIG89_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG89_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG89_WK_LVL_EN_PROXY	RESERVED			PADCONFIG89_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6784. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG89_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG89_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG89_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG89_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG89_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6784. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG89_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG89_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG89_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG89_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG89_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG89_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG89_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG89_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG89_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG89_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG89_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.279 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90_PROXY Register

14.2.1.2.1.2.2.279.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90_PROXY Register (Offset = 6168h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6785. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6168h

Figure 14-3378. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG90_LOCK_PROXY	PADCONFIG90_WKUP_EVT_PROXY	PADCONFIG90_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG90_ISO_BYP_PROXY	PADCONFIG90_ISO_OVR_PROXY	PADCONFIG90_TX_DIS_PROXY	PADCONFIG90_DRV_STR_PROXY		PADCONFIG90_RXACTIVE_PROXY	PADCONFIG90_PULLTYPESEL_PROXY	PADCONFIG90_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG90_ST_EN_PROXY	PADCONFIG90_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG90_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG90_WK_LVL_EN_PROXY	RESERVED			PADCONFIG90_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6786. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG90_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG90_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG90_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG90_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG90_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6786. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG90_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG90_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG90_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG90_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG90_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG90_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG90_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG90_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG90_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG90_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG90_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.280 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91_PROXY Register

14.2.1.2.1.2.2.280.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91_PROXY Register (Offset = 616Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6787. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 616Ch

Figure 14-3379. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG91_LOCK_PROXY	PADCONFIG91_WKUP_EVT_PROXY	PADCONFIG91_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG91_ISO_BYP_PROXY	PADCONFIG91_ISO_OVR_PROXY	PADCONFIG91_TX_DIS_PROXY	PADCONFIG91_DRV_STR_PROXY		PADCONFIG91_RXACTIVE_PROXY	PADCONFIG91_PULLTYPESEL_PROXY	PADCONFIG91_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG91_ST_EN_PROXY	PADCONFIG91_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG91_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG91_WK_LVL_EN_PROXY	RESERVED			PADCONFIG91_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6788. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG91_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG91_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG91_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG91_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG91_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6788. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG91_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG91_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG91_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG91_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG91_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG91_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG91_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG91_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG91_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG91_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG91_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.281 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92_PROXY Register

14.2.1.2.1.2.2.281.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92_PROXY Register (Offset = 6170h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6789. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6170h

Figure 14-3380. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG92_LOCK_PROXY	PADCONFIG92_WKUP_EVT_PROXY	PADCONFIG92_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG92_ISO_BYP_PROXY	PADCONFIG92_ISO_OVR_PROXY	PADCONFIG92_TX_DIS_PROXY	PADCONFIG92_DRV_STR_PROXY		PADCONFIG92_RXACTIVE_PROXY	PADCONFIG92_PULLTYPESEL_PROXY	PADCONFIG92_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG92_ST_EN_PROXY	PADCONFIG92_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG92_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG92_WK_LVL_EN_PROXY	RESERVED			PADCONFIG92_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6790. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG92_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG92_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG92_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG92_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG92_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6790. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG92_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG92_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG92_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG92_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG92_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG92_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG92_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG92_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG92_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG92_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG92_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.282 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93_PROXY Register

14.2.1.2.1.2.2.282.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93_PROXY Register (Offset = 6174h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6791. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6174h

Figure 14-3381. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG93_LOCK_PROXY	PADCONFIG93_WKUP_EVT_PROXY	PADCONFIG93_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG93_ISO_BYP_PROXY	PADCONFIG93_ISO_OVR_PROXY	PADCONFIG93_TX_DIS_PROXY	PADCONFIG93_DRV_STR_PROXY		PADCONFIG93_RXACTIVE_PROXY	PADCONFIG93_PULLTYPESEL_PROXY	PADCONFIG93_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG93_ST_EN_PROXY	PADCONFIG93_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG93_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG93_WK_LVL_EN_PROXY	RESERVED			PADCONFIG93_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6792. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG93_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG93_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG93_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG93_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG93_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6792. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG93_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG93_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG93_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG93_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG93_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG93_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG93_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG93_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG93_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG93_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG93_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.283 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94_PROXY Register

14.2.1.2.1.2.2.283.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94_PROXY Register (Offset = 6178h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6793. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6178h

Figure 14-3382. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG94_LOCK_PROXY	PADCONFIG94_WKUP_EVT_PROXY	PADCONFIG94_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG94_ISO_BYP_PROXY	PADCONFIG94_ISO_OVR_PROXY	PADCONFIG94_TX_DIS_PROXY	PADCONFIG94_DRV_STR_PROXY		PADCONFIG94_RXACTIVE_PROXY	PADCONFIG94_PULLTYPESEL_PROXY	PADCONFIG94_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG94_ST_EN_PROXY	PADCONFIG94_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG94_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG94_WK_LVL_EN_PROXY	RESERVED			PADCONFIG94_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6794. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG94_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG94_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG94_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG94_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG94_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6794. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG94_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG94_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG94_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG94_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG94_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG94_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG94_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG94_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG94_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG94_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG94_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.284 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95_PROXY Register

14.2.1.2.1.2.2.284.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95_PROXY Register (Offset = 617Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6795. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 617Ch

Figure 14-3383. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG95_LOCK_PROXY	PADCONFIG95_WKUP_EVT_PROXY	PADCONFIG95_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG95_ISO_BYP_PROXY	PADCONFIG95_ISO_OVR_PROXY	PADCONFIG95_TX_DIS_PROXY	PADCONFIG95_DRV_STR_PROXY		PADCONFIG95_RXACTIVE_PROXY	PADCONFIG95_PULLTYPESEL_PROXY	PADCONFIG95_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG95_ST_EN_PROXY	PADCONFIG95_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG95_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG95_WK_LVL_EN_PROXY	RESERVED			PADCONFIG95_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6796. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG95_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG95_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG95_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG95_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG95_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6796. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG95_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG95_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG95_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG95_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG95_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG95_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG95_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG95_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG95_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG95_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG95_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.285 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96_PROXY Register

14.2.1.2.1.2.2.285.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96_PROXY Register (Offset = 6180h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6797. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6180h

Figure 14-3384. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG96_LOCK_PROXY	PADCONFIG96_WKUP_EVT_PROXY	PADCONFIG96_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG96_ISO_BYP_PROXY	PADCONFIG96_ISO_OVR_PROXY	PADCONFIG96_TX_DIS_PROXY	PADCONFIG96_DRV_STR_PROXY		PADCONFIG96_RXACTIVE_PROXY	PADCONFIG96_PULLTYPESEL_PROXY	PADCONFIG96_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG96_ST_EN_PROXY	PADCONFIG96_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG96_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG96_WK_LVL_EN_PROXY	RESERVED			PADCONFIG96_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6798. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG96_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG96_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG96_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG96_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG96_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6798. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG96_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG96_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG96_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG96_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG96_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG96_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG96_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG96_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG96_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG96_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG96_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.286 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97_PROXY Register

14.2.1.2.1.2.2.286.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97_PROXY Register (Offset = 6184h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6799. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6184h

Figure 14-3385. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG97_LOCK_PROXY	PADCONFIG97_WKUP_EVT_PROXY	PADCONFIG97_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG97_ISO_BYP_PROXY	PADCONFIG97_ISO_OVR_PROXY	PADCONFIG97_TX_DIS_PROXY	PADCONFIG97_DRV_STR_PROXY		PADCONFIG97_RXACTIVE_PROXY	PADCONFIG97_PULLTYPESEL_PROXY	PADCONFIG97_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG97_ST_EN_PROXY	PADCONFIG97_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG97_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG97_WK_LVL_EN_PROXY	RESERVED			PADCONFIG97_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6800. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG97_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG97_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG97_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG97_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG97_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6800. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG97_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG97_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG97_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG97_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG97_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG97_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG97_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG97_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG97_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG97_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG97_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.287 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98_PROXY Register

14.2.1.2.1.2.2.287.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98_PROXY Register (Offset = 6188h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6801. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6188h

Figure 14-3386. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG98_LOCK_PROXY	PADCONFIG98_WKUP_EVT_PROXY	PADCONFIG98_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG98_ISO_BYP_PROXY	PADCONFIG98_ISO_OVR_PROXY	PADCONFIG98_TX_DIS_PROXY	PADCONFIG98_DRV_STR_PROXY		PADCONFIG98_RXACTIVE_PROXY	PADCONFIG98_PULLTYPESEL_PROXY	PADCONFIG98_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG98_ST_EN_PROXY	PADCONFIG98_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG98_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG98_WK_LVL_EN_PROXY	RESERVED			PADCONFIG98_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6802. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG98_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG98_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG98_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG98_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG98_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6802. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG98_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG98_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG98_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG98_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG98_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG98_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG98_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG98_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG98_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG98_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG98_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.288 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99_PROXY Register

14.2.1.2.1.2.2.288.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99_PROXY Register (Offset = 618Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6803. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 618Ch

Figure 14-3387. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG99_LOCK_PROXY	PADCONFIG99_WKUP_EVT_PROXY	PADCONFIG99_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG99_ISO_BYP_PROXY	PADCONFIG99_ISO_OVR_PROXY	PADCONFIG99_TX_DIS_PROXY	PADCONFIG99_DRV_STR_PROXY		PADCONFIG99_RXACTIVE_PROXY	PADCONFIG99_PULLTYPESEL_PROXY	PADCONFIG99_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG99_ST_EN_PROXY	PADCONFIG99_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG99_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG99_WK_LVL_EN_PROXY	RESERVED			PADCONFIG99_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6804. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG99_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG99_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG99_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG99_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG99_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6804. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG99_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG99_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG99_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG99_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG99_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG99_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG99_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG99_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG99_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG99_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG99_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.289 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100_PROXY Register

14.2.1.2.1.2.2.289.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100_PROXY Register (Offset = 6190h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6805. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6190h

Figure 14-3388. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG100_LOCK_PROXY	PADCONFIG100_WKUP_EVT_PROXY	PADCONFIG100_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG100_ISO_BYP_PROXY	PADCONFIG100_ISO_OVR_PROXY	PADCONFIG100_TX_DIS_PROXY	PADCONFIG100_DRV_STR_PROXY		PADCONFIG100_RXACTIVE_PROXY	PADCONFIG100_PULLTYPESEL_PROXY	PADCONFIG100_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG100_ST_EN_PROXY	PADCONFIG100_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG100_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG100_WK_LVL_EN_PROXY	RESERVED			PADCONFIG100_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6806. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG100_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG100_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG100_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG100_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG100_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6806. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG100_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG100_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG100_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG100_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG100_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG100_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG100_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG100_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG100_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG100_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG100_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.290 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101_PROXY Register

14.2.1.2.1.2.2.290.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101_PROXY Register (Offset = 6194h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6807. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6194h

Figure 14-3389. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG101_LOCK_PROXY	PADCONFIG101_WKUP_EVT_PROXY	PADCONFIG101_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG101_ISO_BYP_PROXY	PADCONFIG101_ISO_OVR_PROXY	PADCONFIG101_TX_DIS_PROXY	PADCONFIG101_DRV_STR_PROXY		PADCONFIG101_RXACTIVE_PROXY	PADCONFIG101_PULLTYPESEL_PROXY	PADCONFIG101_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG101_ST_EN_PROXY	PADCONFIG101_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG101_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG101_WK_LVL_EN_PROXY	RESERVED			PADCONFIG101_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6808. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG101_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG101_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG101_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG101_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG101_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6808. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG101_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG101_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG101_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG101_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG101_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG101_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG101_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG101_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG101_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG101_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG101_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.291 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102_PROXY Register

14.2.1.2.1.2.2.291.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102_PROXY Register (Offset = 6198h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6809. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6198h

Figure 14-3390. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG102_LOCK_PROXY	PADCONFIG102_WKUP_EVT_PROXY	PADCONFIG102_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG102_ISO_BYP_PROXY	PADCONFIG102_ISO_OVR_PROXY	PADCONFIG102_TX_DIS_PROXY	PADCONFIG102_DRV_STR_PROXY		PADCONFIG102_RXACTIVE_PROXY	PADCONFIG102_PULLTYPESEL_PROXY	PADCONFIG102_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG102_ST_EN_PROXY	PADCONFIG102_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG102_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG102_WK_LVL_EN_PROXY	RESERVED			PADCONFIG102_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6810. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG102_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG102_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG102_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG102_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG102_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6810. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG102_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG102_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG102_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG102_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG102_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG102_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG102_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG102_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG102_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG102_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG102_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.292 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103_PROXY Register

14.2.1.2.1.2.2.292.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103_PROXY Register (Offset = 619Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6811. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 619Ch

Figure 14-3391. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG103_LOCK_PROXY	PADCONFIG103_WKUP_EVT_PROXY	PADCONFIG103_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG103_ISO_BYP_PROXY	PADCONFIG103_ISO_OVR_PROXY	PADCONFIG103_TX_DIS_PROXY	PADCONFIG103_DRV_STR_PROXY		PADCONFIG103_RXACTIVE_PROXY	PADCONFIG103_PULLTYPESEL_PROXY	PADCONFIG103_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG103_ST_EN_PROXY	PADCONFIG103_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG103_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG103_WK_LVL_EN_PROXY	RESERVED			PADCONFIG103_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6812. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG103_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG103_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG103_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG103_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG103_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6812. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG103_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG103_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG103_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG103_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG103_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG103_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG103_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG103_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG103_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG103_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG103_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.293 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104_PROXY Register

14.2.1.2.1.2.2.293.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104_PROXY Register (Offset = 61A0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6813. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61A0h

Figure 14-3392. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG104_LOCK_PROXY	PADCONFIG104_WKUP_EVT_PROXY	PADCONFIG104_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG104_ISO_BYP_PROXY	PADCONFIG104_ISO_OVR_PROXY	PADCONFIG104_TX_DIS_PROXY	PADCONFIG104_DRV_STR_PROXY		PADCONFIG104_RXACTIVE_PROXY	PADCONFIG104_PULLTYPESEL_PROXY	PADCONFIG104_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG104_ST_EN_PROXY	PADCONFIG104_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG104_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG104_WK_LVL_EN_PROXY	RESERVED			PADCONFIG104_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6814. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG104_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG104_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG104_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG104_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG104_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6814. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG104_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG104_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG104_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG104_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG104_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG104_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG104_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG104_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG104_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG104_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG104_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.294 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105_PROXY Register

14.2.1.2.1.2.2.294.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105_PROXY Register (Offset = 61A4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6815. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61A4h

Figure 14-3393. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG105_LOCK_PROXY	PADCONFIG105_WKUP_EVT_PROXY	PADCONFIG105_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG105_ISO_BYP_PROXY	PADCONFIG105_ISO_OVR_PROXY	PADCONFIG105_TX_DIS_PROXY	PADCONFIG105_DRV_STR_PROXY		PADCONFIG105_RXACTIVE_PROXY	PADCONFIG105_PULLTYPESEL_PROXY	PADCONFIG105_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG105_ST_EN_PROXY	PADCONFIG105_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG105_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG105_WK_LVL_EN_PROXY	RESERVED			PADCONFIG105_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6816. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG105_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG105_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG105_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG105_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG105_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6816. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG105_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG105_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG105_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG105_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG105_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG105_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG105_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG105_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG105_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG105_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG105_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.295 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106_PROXY Register

14.2.1.2.1.2.2.295.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106_PROXY Register (Offset = 61A8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6817. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61A8h

Figure 14-3394. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG106_LOCK_PROXY	PADCONFIG106_WKUP_EVT_PROXY	PADCONFIG106_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG106_ISO_BYP_PROXY	PADCONFIG106_ISO_OVR_PROXY	PADCONFIG106_TX_DIS_PROXY	PADCONFIG106_DRV_STR_PROXY		PADCONFIG106_RXACTIVE_PROXY	PADCONFIG106_PULLTYPESEL_PROXY	PADCONFIG106_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG106_ST_EN_PROXY	PADCONFIG106_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG106_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG106_WK_LVL_EN_PROXY	RESERVED			PADCONFIG106_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6818. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG106_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG106_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG106_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG106_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG106_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6818. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG106_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG106_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG106_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG106_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG106_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG106_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG106_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG106_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG106_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG106_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG106_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.296 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107_PROXY Register

14.2.1.2.1.2.2.296.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107_PROXY Register (Offset = 61ACh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6819. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61ACh

Figure 14-3395. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG107_LOCK_PROXY	PADCONFIG107_WKUP_EVT_PROXY	PADCONFIG107_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG107_ISO_BYP_PROXY	PADCONFIG107_ISO_OVR_PROXY	PADCONFIG107_TX_DIS_PROXY	PADCONFIG107_DRV_STR_PROXY		PADCONFIG107_RXACTIVE_PROXY	PADCONFIG107_PULLTYPESEL_PROXY	PADCONFIG107_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG107_ST_EN_PROXY	PADCONFIG107_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG107_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG107_WK_LVL_EN_PROXY	RESERVED			PADCONFIG107_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6820. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG107_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG107_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG107_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG107_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG107_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6820. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG107_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG107_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG107_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG107_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG107_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG107_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG107_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG107_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG107_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG107_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG107_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.297 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108_PROXY Register

14.2.1.2.1.2.2.297.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108_PROXY Register (Offset = 61B0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6821. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61B0h

Figure 14-3396. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG108_LOCK_PROXY	PADCONFIG108_WKUP_EVT_PROXY	PADCONFIG108_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h

23	22	21	20	19	18	17	16
PADCONFIG108_ISO_BYP_PROXY	PADCONFIG108_ISO_OVR_PROXY	PADCONFIG108_TX_DIS_PROXY	PADCONFIG108_DRV_STR_PROXY		PADCONFIG108_RXACTIVE_PROXY	PADCONFIG108_PULLTYPESEL_PROXY	PADCONFIG108_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h

15	14	13	12	11	10	9	8
	PADCONFIG108_ST_EN_PROXY	PADCONFIG108_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG108_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h

7	6	5	4	3	2	1	0
PADCONFIG108_WK_LVL_EN_PROXY	RESERVED			PADCONFIG108_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6822. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG108_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG108_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG108_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG108_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG108_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6822. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG108_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG108_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG108_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG108_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG108_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG108_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG108_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG108_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG108_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG108_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG108_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.298 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109_PROXY Register

14.2.1.2.1.2.2.298.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109_PROXY Register (Offset = 61B4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6823. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61B4h

Figure 14-3397. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG109_LOCK_PROXY	PADCONFIG109_WKUP_EVT_PROXY	PADCONFIG109_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG109_ISO_BYP_PROXY	PADCONFIG109_ISO_OVR_PROXY	PADCONFIG109_TX_DIS_PROXY	PADCONFIG109_DRV_STR_PROXY		PADCONFIG109_RXACTIVE_PROXY	PADCONFIG109_PULLTYPESEL_PROXY	PADCONFIG109_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG109_ST_EN_PROXY	PADCONFIG109_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG109_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG109_WK_LVL_EN_PROXY	RESERVED			PADCONFIG109_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6824. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG109_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG109_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG109_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG109_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG109_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6824. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG109_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG109_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG109_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG109_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG109_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG109_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG109_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG109_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG109_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG109_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG109_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.299 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110_PROXY Register

14.2.1.2.1.2.2.299.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110_PROXY Register (Offset = 61B8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6825. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61B8h

Figure 14-3398. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG110_LOCK_PROXY	PADCONFIG110_WKUP_EVT_PROXY	PADCONFIG110_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG110_ISO_BYP_PROXY	PADCONFIG110_ISO_OVR_PROXY	PADCONFIG110_TX_DIS_PROXY	PADCONFIG110_DRV_STR_PROXY		PADCONFIG110_RXACTIVE_PROXY	PADCONFIG110_PULLTYPESEL_PROXY	PADCONFIG110_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG110_ST_EN_PROXY	PADCONFIG110_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG110_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG110_WK_LVL_EN_PROXY	RESERVED			PADCONFIG110_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6826. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG110_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG110_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG110_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG110_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG110_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6826. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG110_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG110_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG110_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG110_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG110_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG110_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG110_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG110_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG110_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG110_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG110_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.300 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111_PROXY Register

14.2.1.2.1.2.2.300.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111_PROXY Register (Offset = 61BCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6827. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61BCh

Figure 14-3399. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG111_LOCK_PROXY	PADCONFIG111_WKUP_EVT_PROXY	PADCONFIG111_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG111_ISO_BYP_PROXY	PADCONFIG111_ISO_OVR_PROXY	PADCONFIG111_TX_DIS_PROXY	PADCONFIG111_DRV_STR_PROXY		PADCONFIG111_RXACTIVE_PROXY	PADCONFIG111_PULLTYPESEL_PROXY	PADCONFIG111_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG111_ST_EN_PROXY	PADCONFIG111_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG111_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG111_WK_LVL_EN_PROXY	RESERVED			PADCONFIG111_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6828. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG111_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG111_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG111_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG111_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG111_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6828. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG111_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG111_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG111_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG111_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG111_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG111_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG111_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG111_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG111_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG111_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG111_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.301 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112_PROXY Register

14.2.1.2.1.2.2.301.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112_PROXY Register (Offset = 61C0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6829. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61C0h

Figure 14-3400. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG112_LOCK_PROXY	PADCONFIG112_WKUP_EVT_PROXY	PADCONFIG112_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG112_ISO_BYP_PROXY	PADCONFIG112_ISO_OVR_PROXY	PADCONFIG112_TX_DIS_PROXY	PADCONFIG112_DRV_STR_PROXY		PADCONFIG112_RXACTIVE_PROXY	PADCONFIG112_PULLTYPESEL_PROXY	PADCONFIG112_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG112_ST_EN_PROXY	PADCONFIG112_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG112_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG112_WK_LVL_EN_PROXY	RESERVED			PADCONFIG112_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6830. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG112_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG112_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG112_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG112_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG112_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6830. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG112_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG112_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG112_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG112_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG112_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG112_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG112_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG112_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG112_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG112_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG112_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.302 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113_PROXY Register

14.2.1.2.1.2.2.302.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113_PROXY Register (Offset = 61C4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6831. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61C4h

Figure 14-3401. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG113_LOCK_PROXY	PADCONFIG113_WKUP_EVT_PROXY	PADCONFIG113_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG113_ISO_BYP_PROXY	PADCONFIG113_ISO_OVR_PROXY	PADCONFIG113_TX_DIS_PROXY	PADCONFIG113_DRV_STR_PROXY		PADCONFIG113_RXACTIVE_PROXY	PADCONFIG113_PULLTYPESEL_PROXY	PADCONFIG113_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG113_ST_EN_PROXY	PADCONFIG113_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG113_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG113_WK_LVL_EN_PROXY	RESERVED			PADCONFIG113_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6832. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG113_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG113_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG113_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG113_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG113_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6832. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG113_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG113_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG113_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG113_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG113_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG113_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG113_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG113_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG113_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG113_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG113_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.303 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114_PROXY Register

14.2.1.2.1.2.2.303.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114_PROXY Register (Offset = 61C8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6833. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61C8h

Figure 14-3402. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG114_LOCK_PROXY	PADCONFIG114_WKUP_EVT_PROXY	PADCONFIG114_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG114_ISO_BYP_PROXY	PADCONFIG114_ISO_OVR_PROXY	PADCONFIG114_TX_DIS_PROXY	PADCONFIG114_DRV_STR_PROXY		PADCONFIG114_RXACTIVE_PROXY	PADCONFIG114_PULLTYPESEL_PROXY	PADCONFIG114_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG114_ST_EN_PROXY	PADCONFIG114_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG114_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG114_WK_LVL_EN_PROXY	RESERVED			PADCONFIG114_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6834. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG114_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG114_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG114_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG114_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG114_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6834. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG114_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG114_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG114_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG114_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG114_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG114_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG114_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG114_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG114_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG114_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG114_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.304 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115_PROXY Register

14.2.1.2.1.2.2.304.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115_PROXY Register (Offset = 61CCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6835. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61CCh

Figure 14-3403. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG115_LOCK_PROXY	PADCONFIG115_WKUP_EVT_PROXY	PADCONFIG115_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG115_ISO_BYP_PROXY	PADCONFIG115_ISO_OVR_PROXY	PADCONFIG115_TX_DIS_PROXY	PADCONFIG115_DRV_STR_PROXY		PADCONFIG115_RXACTIVE_PROXY	PADCONFIG115_PULLTYPESEL_PROXY	PADCONFIG115_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG115_ST_EN_PROXY	PADCONFIG115_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG115_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG115_WK_LVL_EN_PROXY	RESERVED			PADCONFIG115_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6836. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG115_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG115_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG115_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG115_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG115_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6836. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG115_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG115_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG115_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG115_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG115_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG115_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG115_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG115_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG115_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG115_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG115_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.305 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116_PROXY Register

14.2.1.2.1.2.2.305.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116_PROXY Register (Offset = 61D0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6837. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61D0h

Figure 14-3404. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG116_LOCK_PROXY	PADCONFIG116_WKUP_EVT_PROXY	PADCONFIG116_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG116_ISO_BYP_PROXY	PADCONFIG116_ISO_OVR_PROXY	PADCONFIG116_TX_DIS_PROXY	PADCONFIG116_DRV_STR_PROXY		PADCONFIG116_RXACTIVE_PROXY	PADCONFIG116_PULLTYPESEL_PROXY	PADCONFIG116_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG116_ST_EN_PROXY	PADCONFIG116_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG116_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG116_WK_LVL_EN_PROXY	RESERVED			PADCONFIG116_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6838. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG116_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG116_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG116_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG116_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG116_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6838. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG116_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG116_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG116_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG116_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG116_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG116_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG116_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG116_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG116_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG116_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG116_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.306 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117_PROXY Register

14.2.1.2.1.2.2.306.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117_PROXY Register (Offset = 61D4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6839. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61D4h

Figure 14-3405. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG117_LOCK_PROXY	PADCONFIG117_WKUP_EVT_PROXY	PADCONFIG117_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG117_ISO_BYP_PROXY	PADCONFIG117_ISO_OVR_PROXY	PADCONFIG117_TX_DIS_PROXY	PADCONFIG117_DRV_STR_PROXY		PADCONFIG117_RXACTIVE_PROXY	PADCONFIG117_PULLTYPESEL_PROXY	PADCONFIG117_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG117_ST_EN_PROXY	PADCONFIG117_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG117_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG117_WK_LVL_EN_PROXY	RESERVED			PADCONFIG117_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6840. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG117_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG117_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG117_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG117_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG117_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6840. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG117_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG117_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG117_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG117_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG117_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG117_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG117_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG117_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG117_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG117_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG117_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.307 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118_PROXY Register

14.2.1.2.1.2.2.307.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118_PROXY Register (Offset = 61D8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6841. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61D8h

Figure 14-3406. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG118_LOCK_PROXY	PADCONFIG118_WKUP_EVT_PROXY	PADCONFIG118_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG118_ISO_BYP_PROXY	PADCONFIG118_ISO_OVR_PROXY	PADCONFIG118_TX_DIS_PROXY	PADCONFIG118_DRV_STR_PROXY		PADCONFIG118_RXACTIVE_PROXY	PADCONFIG118_PULLTYPESEL_PROXY	PADCONFIG118_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG118_ST_EN_PROXY	PADCONFIG118_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG118_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG118_WK_LVL_EN_PROXY	RESERVED			PADCONFIG118_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6842. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG118_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG118_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG118_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG118_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG118_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6842. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG118_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG118_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG118_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG118_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG118_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG118_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG118_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG118_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG118_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG118_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG118_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.308 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119_PROXY Register

14.2.1.2.1.2.2.308.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119_PROXY Register (Offset = 61DCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6843. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61DCh

Figure 14-3407. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG119_LOCK_PROXY	PADCONFIG119_WKUP_EVT_PROXY	PADCONFIG119_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG119_ISO_BYP_PROXY	PADCONFIG119_ISO_OVR_PROXY	PADCONFIG119_TX_DIS_PROXY	PADCONFIG119_DRV_STR_PROXY		PADCONFIG119_RXACTIVE_PROXY	PADCONFIG119_PULLTYPESEL_PROXY	PADCONFIG119_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG119_ST_EN_PROXY	PADCONFIG119_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG119_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG119_WK_LVL_EN_PROXY	RESERVED			PADCONFIG119_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6844. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG119_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG119_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG119_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG119_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG119_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6844. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG119_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG119_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG119_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG119_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG119_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG119_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG119_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG119_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG119_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG119_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG119_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.309 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120_PROXY Register

14.2.1.2.1.2.2.309.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120_PROXY Register (Offset = 61E0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6845. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61E0h

Figure 14-3408. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG120_LOCK_PROXY	PADCONFIG120_WKUP_EVT_PROXY	PADCONFIG120_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG120_ISO_BYP_PROXY	PADCONFIG120_ISO_OVR_PROXY	PADCONFIG120_TX_DIS_PROXY	PADCONFIG120_DRV_STR_PROXY		PADCONFIG120_RXACTIVE_PROXY	PADCONFIG120_PULLTYPESEL_PROXY	PADCONFIG120_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG120_ST_EN_PROXY	PADCONFIG120_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG120_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG120_WK_LVL_EN_PROXY	RESERVED			PADCONFIG120_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6846. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG120_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG120_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG120_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG120_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG120_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6846. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG120_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG120_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG120_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG120_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG120_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG120_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG120_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG120_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG120_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG120_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG120_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.310 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121_PROXY Register

14.2.1.2.1.2.2.310.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121_PROXY Register (Offset = 61E4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6847. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61E4h

Figure 14-3409. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG121_LOCK_PROXY	PADCONFIG121_WKUP_EVT_PROXY	PADCONFIG121_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG121_ISO_BYP_PROXY	PADCONFIG121_ISO_OVR_PROXY	PADCONFIG121_TX_DIS_PROXY	PADCONFIG121_DRV_STR_PROXY		PADCONFIG121_RXACTIVE_PROXY	PADCONFIG121_PULLTYPESEL_PROXY	PADCONFIG121_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG121_ST_EN_PROXY	PADCONFIG121_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG121_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG121_WK_LVL_EN_PROXY	RESERVED			PADCONFIG121_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6848. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG121_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG121_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG121_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG121_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG121_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6848. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG121_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG121_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG121_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG121_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG121_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG121_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG121_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG121_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG121_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG121_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG121_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.311 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122_PROXY Register

14.2.1.2.1.2.2.311.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122_PROXY Register (Offset = 61E8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6849. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61E8h

Figure 14-3410. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG122_LOCK_PROXY	PADCONFIG122_WKUP_EVT_PROXY	PADCONFIG122_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG122_ISO_BYP_PROXY	PADCONFIG122_ISO_OVR_PROXY	PADCONFIG122_TX_DIS_PROXY	PADCONFIG122_DRV_STR_PROXY		PADCONFIG122_RXACTIVE_PROXY	PADCONFIG122_PULLTYPESEL_PROXY	PADCONFIG122_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG122_ST_EN_PROXY	PADCONFIG122_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG122_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG122_WK_LVL_EN_PROXY	RESERVED			PADCONFIG122_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6850. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG122_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG122_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG122_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG122_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG122_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6850. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG122_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG122_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG122_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG122_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG122_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG122_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG122_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG122_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG122_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG122_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG122_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.312 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123_PROXY Register

14.2.1.2.1.2.2.312.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123_PROXY Register (Offset = 61ECh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6851. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61ECh

Figure 14-3411. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG123_LOCK_PROXY	PADCONFIG123_WKUP_EVT_PROXY	PADCONFIG123_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG123_ISO_BYP_PROXY	PADCONFIG123_ISO_OVR_PROXY	PADCONFIG123_TX_DIS_PROXY	PADCONFIG123_DRV_STR_PROXY		PADCONFIG123_RXACTIVE_PROXY	PADCONFIG123_PULLTYPESEL_PROXY	PADCONFIG123_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG123_ST_EN_PROXY	PADCONFIG123_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG123_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG123_WK_LVL_EN_PROXY	RESERVED			PADCONFIG123_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6852. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG123_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG123_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG123_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG123_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG123_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6852. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG123_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG123_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG123_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG123_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG123_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG123_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG123_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG123_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG123_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG123_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG123_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.313 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124_PROXY Register

14.2.1.2.1.2.2.313.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124_PROXY Register (Offset = 61F0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6853. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61F0h

Figure 14-3412. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG124_LOCK_PROXY	PADCONFIG124_WKUP_EVT_PROXY	PADCONFIG124_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG124_ISO_BYP_PROXY	PADCONFIG124_ISO_OVR_PROXY	PADCONFIG124_TX_DIS_PROXY	PADCONFIG124_DRV_STR_PROXY		PADCONFIG124_RXACTIVE_PROXY	PADCONFIG124_PULLTYPESEL_PROXY	PADCONFIG124_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG124_ST_EN_PROXY	PADCONFIG124_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG124_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG124_WK_LVL_EN_PROXY	RESERVED			PADCONFIG124_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6854. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG124_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG124_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG124_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG124_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG124_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6854. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG124_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG124_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG124_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG124_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG124_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG124_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG124_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG124_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG124_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG124_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG124_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.314 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125_PROXY Register

14.2.1.2.1.2.2.314.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125_PROXY Register (Offset = 61F4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6855. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61F4h

Figure 14-3413. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG125_LOCK_PROXY	PADCONFIG125_WKUP_EVT_PROXY	PADCONFIG125_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG125_ISO_BYP_PROXY	PADCONFIG125_ISO_OVR_PROXY	PADCONFIG125_TX_DIS_PROXY	PADCONFIG125_DRV_STR_PROXY		PADCONFIG125_RXACTIVE_PROXY	PADCONFIG125_PULLTYPESEL_PROXY	PADCONFIG125_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG125_ST_EN_PROXY	PADCONFIG125_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG125_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG125_WK_LVL_EN_PROXY	RESERVED			PADCONFIG125_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6856. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG125_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG125_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG125_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG125_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG125_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6856. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG125_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG125_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG125_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG125_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG125_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG125_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG125_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG125_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG125_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG125_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG125_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.315 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126_PROXY Register

14.2.1.2.1.2.2.315.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126_PROXY Register (Offset = 61F8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6857. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61F8h

Figure 14-3414. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG126_LOCK_PROXY	PADCONFIG126_WKUP_EVT_PROXY	PADCONFIG126_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG126_ISO_BYP_PROXY	PADCONFIG126_ISO_OVR_PROXY	PADCONFIG126_TX_DIS_PROXY	PADCONFIG126_DRV_STR_PROXY		PADCONFIG126_RXACTIVE_PROXY	PADCONFIG126_PULLTYPESEL_PROXY	PADCONFIG126_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG126_ST_EN_PROXY	PADCONFIG126_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG126_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG126_WK_LVL_EN_PROXY	RESERVED			PADCONFIG126_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6858. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG126_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG126_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG126_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG126_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG126_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6858. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG126_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG126_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG126_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG126_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG126_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG126_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG126_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG126_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG126_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG126_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG126_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.316 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127_PROXY Register

14.2.1.2.1.2.2.316.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127_PROXY Register (Offset = 61FCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6859. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 61FCh

Figure 14-3415. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG127_LOCK_PROXY	PADCONFIG127_WKUP_EVT_PROXY	PADCONFIG127_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG127_ISO_BYP_PROXY	PADCONFIG127_ISO_OVR_PROXY	PADCONFIG127_TX_DIS_PROXY	PADCONFIG127_DRV_STR_PROXY		PADCONFIG127_RXACTIVE_PROXY	PADCONFIG127_PULLTYPESEL_PROXY	PADCONFIG127_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG127_ST_EN_PROXY	PADCONFIG127_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG127_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG127_WK_LVL_EN_PROXY	RESERVED			PADCONFIG127_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6860. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG127_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG127_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG127_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG127_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG127_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6860. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG127_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG127_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG127_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG127_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG127_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG127_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG127_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG127_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG127_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG127_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG127_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.317 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128_PROXY Register

14.2.1.2.1.2.2.317.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128_PROXY Register (Offset = 6200h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6861. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6200h

Figure 14-3416. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG128_LOCK_PROXY	PADCONFIG128_WKUP_EVT_PROXY	PADCONFIG128_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG128_ISO_BYP_PROXY	PADCONFIG128_ISO_OVR_PROXY	PADCONFIG128_TX_DIS_PROXY	PADCONFIG128_DRV_STR_PROXY		PADCONFIG128_RXACTIVE_PROXY	PADCONFIG128_PULLTYPESEL_PROXY	PADCONFIG128_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG128_ST_EN_PROXY	PADCONFIG128_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG128_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG128_WK_LVL_EN_PROXY	RESERVED			PADCONFIG128_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6862. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG128_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG128_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG128_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG128_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG128_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6862. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG128_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG128_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG128_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG128_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG128_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG128_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG128_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG128_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG128_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG128_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG128_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.318 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129_PROXY Register

14.2.1.2.1.2.2.318.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129_PROXY Register (Offset = 6204h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6863. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6204h

Figure 14-3417. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG129_LOCK_PROXY	PADCONFIG129_WKUP_EVT_PROXY	PADCONFIG129_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG129_ISO_BYP_PROXY	PADCONFIG129_ISO_OVR_PROXY	PADCONFIG129_TX_DIS_PROXY	PADCONFIG129_DRV_STR_PROXY		PADCONFIG129_RXACTIVE_PROXY	PADCONFIG129_PULLTYPESEL_PROXY	PADCONFIG129_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG129_ST_EN_PROXY	PADCONFIG129_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG129_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG129_WK_LVL_EN_PROXY	RESERVED			PADCONFIG129_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6864. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG129_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG129_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG129_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG129_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG129_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6864. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG129_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG129_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG129_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG129_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG129_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG129_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG129_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG129_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG129_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG129_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG129_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.319 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130_PROXY Register

14.2.1.2.1.2.2.319.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130_PROXY Register (Offset = 6208h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6865. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6208h

Figure 14-3418. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG130_LOCK_PROXY</td><td>PADCONFIG130_WKUP_EVT_PROXY</td><td>PADCONFIG130_WKUP_EN_PROXY</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PADCONFIG130_ISO_BYP_PROXY</td><td>PADCONFIG130_ISO_OVR_PROXY</td><td>PADCONFIG130_TX_DIS_PROXY</td><td colspan="2">PADCONFIG130_DRV_STR_PROXY</td><td>PADCONFIG130_RXACTIVE_PROXY</td><td>PADCONFIG130_PULLTYPESEL_PROXY</td><td>PADCONFIG130_PULLUDEN_PROXY</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td></td><td>PADCONFIG130_ST_EN_PROXY</td><td colspan="3">PADCONFIG130_DEBOUNCE_SEL_PROXY</td><td colspan="2">RESERVED</td><td>PADCONFIG130_WK_LVL_POL_PROXY</td></tr>
<tr><td></td><td>R/W</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td>1h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PADCONFIG130_WK_LVL_EN_PROXY</td><td colspan="3">RESERVED</td><td colspan="4">PADCONFIG130_MUXMODE_PROXY</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">7h</td></tr>
</table>

Table 14-6866. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG130_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG130_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG130_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG130_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG130_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6866. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG130_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG130_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG130_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG130_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG130_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG130_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG130_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG130_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG130_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG130_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG130_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.320 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131_PROXY Register

14.2.1.2.1.2.2.320.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131_PROXY Register (Offset = 620Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6867. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 620Ch

Figure 14-3419. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG131_LOCK_PROXY	PADCONFIG131_WKUP_EVT_PROXY	PADCONFIG131_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG131_ISO_BYP_PROXY	PADCONFIG131_ISO_OVR_PROXY	PADCONFIG131_TX_DIS_PROXY	PADCONFIG131_DRV_STR_PROXY		PADCONFIG131_RXACTIVE_PROXY	PADCONFIG131_PULLTYPESEL_PROXY	PADCONFIG131_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG131_ST_EN_PROXY	PADCONFIG131_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG131_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG131_WK_LVL_EN_PROXY	RESERVED			PADCONFIG131_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6868. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG131_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG131_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG131_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG131_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG131_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6868. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG131_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG131_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG131_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG131_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG131_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG131_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG131_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG131_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG131_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG131_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG131_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.321 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132_PROXY Register

14.2.1.2.1.2.2.321.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132_PROXY Register (Offset = 6210h) [reset = 8214007h]

Register to control pin configuration and muxing

Return to Summary Table

Table 14-6869. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6210h

Figure 14-3420. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG132_LOCK_PROXY	PADCONFIG132_WKUP_EVT_PROXY	PADCONFIG132_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG132_ISO_BYP_PROXY	PADCONFIG132_ISO_OVR_PROXY	PADCONFIG132_TX_DIS_PROXY	PADCONFIG132_DRV_STR_PROXY		PADCONFIG132_RXACTIVE_PROXY	PADCONFIG132_PULLTYPESEL_PROXY	PADCONFIG132_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG132_ST_EN_PROXY	PADCONFIG132_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG132_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG132_WK_LVL_EN_PROXY	RESERVED			PADCONFIG132_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6870. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG132_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG132_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG132_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG132_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG132_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6870. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG132_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG132_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG132_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG132_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG132_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG132_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG132_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG132_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG132_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG132_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG132_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.322 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133_PROXY Register

14.2.1.2.1.2.2.322.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133_PROXY Register (Offset = 6214h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6871. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6214h

Figure 14-3421. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG133_LOCK_PROXY	PADCONFIG133_WKUP_EVT_PROXY	PADCONFIG133_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG133_ISO_BYP_PROXY	PADCONFIG133_ISO_OVR_PROXY	PADCONFIG133_TX_DIS_PROXY	PADCONFIG133_DRV_STR_PROXY		PADCONFIG133_RXACTIVE_PROXY	PADCONFIG133_PULLTYPESEL_PROXY	PADCONFIG133_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG133_ST_EN_PROXY	PADCONFIG133_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG133_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG133_WK_LVL_EN_PROXY	RESERVED			PADCONFIG133_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6872. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG133_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG133_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG133_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG133_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG133_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6872. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG133_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG133_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG133_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG133_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG133_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG133_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG133_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG133_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG133_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG133_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG133_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.323 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134_PROXY Register

14.2.1.2.1.2.2.323.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134_PROXY Register (Offset = 6218h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6873. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6218h

Figure 14-3422. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG134_LOCK_PROXY	PADCONFIG134_WKUP_EVT_PROXY	PADCONFIG134_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG134_ISO_BYP_PROXY	PADCONFIG134_ISO_OVR_PROXY	PADCONFIG134_TX_DIS_PROXY	PADCONFIG134_DRV_STR_PROXY		PADCONFIG134_RXACTIVE_PROXY	PADCONFIG134_PULLTYPESEL_PROXY	PADCONFIG134_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG134_ST_EN_PROXY	PADCONFIG134_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG134_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG134_WK_LVL_EN_PROXY	RESERVED			PADCONFIG134_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6874. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG134_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG134_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG134_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG134_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG134_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6874. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG134_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG134_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG134_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG134_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG134_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG134_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG134_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG134_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG134_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG134_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG134_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.324 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135_PROXY Register

14.2.1.2.1.2.2.324.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135_PROXY Register (Offset = 621Ch) [reset = 8054000h]

Register to control pin configuration and muxing

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Table 14-6875. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 621Ch

Figure 14-3423. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG135_LOCK_PROXY	PADCONFIG135_WKUP_EVT_PROXY	PADCONFIG135_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG135_ISO_BYP_PROXY	PADCONFIG135_ISO_OVR_PROXY	PADCONFIG135_TX_DIS_PROXY	PADCONFIG135_DRV_STR_PROXY		PADCONFIG135_RXACTIVE_PROXY	PADCONFIG135_PULLTYPESEL_PROXY	PADCONFIG135_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		1h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG135_ST_EN_PROXY	PADCONFIG135_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG135_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG135_WK_LVL_EN_PROXY	RESERVED			PADCONFIG135_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6876. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG135_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG135_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG135_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG135_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG135_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6876. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG135_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG135_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG135_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG135_RXACTIVE_PROXY	R/W	1h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG135_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG135_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG135_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG135_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG135_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG135_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG135_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.325 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136_PROXY Register

14.2.1.2.1.2.2.325.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136_PROXY Register (Offset = 6220h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6877. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6220h

Figure 14-3424. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG136_LOCK_PROXY	PADCONFIG136_WKUP_EVT_PROXY	PADCONFIG136_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG136_ISO_BYP_PROXY	PADCONFIG136_ISO_OVR_PROXY	PADCONFIG136_TX_DIS_PROXY	PADCONFIG136_DRV_STR_PROXY		PADCONFIG136_RXACTIVE_PROXY	PADCONFIG136_PULLTYPESEL_PROXY	PADCONFIG136_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG136_ST_EN_PROXY	PADCONFIG136_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG136_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG136_WK_LVL_EN_PROXY	RESERVED			PADCONFIG136_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6878. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG136_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG136_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG136_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG136_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG136_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6878. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG136_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG136_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG136_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG136_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG136_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG136_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG136_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG136_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG136_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG136_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG136_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.326 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137_PROXY Register

14.2.1.2.1.2.2.326.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137_PROXY Register (Offset = 6224h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6879. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6224h

Figure 14-3425. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG137_LOCK_PROXY	PADCONFIG137_WKUP_EVT_PROXY	PADCONFIG137_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG137_ISO_BYP_PROXY	PADCONFIG137_ISO_OVR_PROXY	PADCONFIG137_TX_DIS_PROXY	PADCONFIG137_DRV_STR_PROXY		PADCONFIG137_RXACTIVE_PROXY	PADCONFIG137_PULLTYPESEL_PROXY	PADCONFIG137_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG137_ST_EN_PROXY	PADCONFIG137_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG137_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG137_WK_LVL_EN_PROXY	RESERVED			PADCONFIG137_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6880. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG137_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG137_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG137_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG137_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG137_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6880. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG137_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG137_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG137_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG137_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG137_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG137_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG137_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG137_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG137_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG137_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG137_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.327 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138_PROXY Register

14.2.1.2.1.2.2.327.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138_PROXY Register (Offset = 6228h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6881. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6228h

Figure 14-3426. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG138_LOCK_PROXY	PADCONFIG138_WKUP_EVT_PROXY	PADCONFIG138_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG138_ISO_BYP_PROXY	PADCONFIG138_ISO_OVR_PROXY	PADCONFIG138_TX_DIS_PROXY	PADCONFIG138_DRV_STR_PROXY		PADCONFIG138_RXACTIVE_PROXY	PADCONFIG138_PULLTYPESEL_PROXY	PADCONFIG138_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG138_ST_EN_PROXY	PADCONFIG138_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG138_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG138_WK_LVL_EN_PROXY	RESERVED			PADCONFIG138_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6882. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG138_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG138_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG138_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG138_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG138_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6882. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG138_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG138_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG138_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG138_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG138_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG138_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG138_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG138_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG138_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG138_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG138_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.328 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139_PROXY Register

14.2.1.2.1.2.2.328.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139_PROXY Register (Offset = 622Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6883. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 622Ch

Figure 14-3427. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG139_LOCK_PROXY	PADCONFIG139_WKUP_EVT_PROXY	PADCONFIG139_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG139_ISO_BYP_PROXY	PADCONFIG139_ISO_OVR_PROXY	PADCONFIG139_TX_DIS_PROXY	PADCONFIG139_DRV_STR_PROXY		PADCONFIG139_RXACTIVE_PROXY	PADCONFIG139_PULLTYPESEL_PROXY	PADCONFIG139_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG139_ST_EN_PROXY	PADCONFIG139_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG139_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG139_WK_LVL_EN_PROXY	RESERVED			PADCONFIG139_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6884. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG139_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG139_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG139_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG139_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG139_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6884. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG139_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG139_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG139_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG139_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG139_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG139_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG139_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG139_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG139_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG139_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG139_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.329 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140_PROXY Register

14.2.1.2.1.2.2.329.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140_PROXY Register (Offset = 6230h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6885. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6230h

Figure 14-3428. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG140_LOCK_PROXY	PADCONFIG140_WKUP_EVT_PROXY	PADCONFIG140_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG140_ISO_BYP_PROXY	PADCONFIG140_ISO_OVR_PROXY	PADCONFIG140_TX_DIS_PROXY	PADCONFIG140_DRV_STR_PROXY		PADCONFIG140_RXACTIVE_PROXY	PADCONFIG140_PULLTYPESEL_PROXY	PADCONFIG140_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG140_ST_EN_PROXY	PADCONFIG140_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG140_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG140_WK_LVL_EN_PROXY	RESERVED			PADCONFIG140_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6886. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG140_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG140_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG140_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG140_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG140_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6886. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG140_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG140_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG140_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG140_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG140_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG140_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG140_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG140_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG140_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG140_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG140_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.330 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141_PROXY Register

14.2.1.2.1.2.2.330.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141_PROXY Register (Offset = 6234h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6887. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6234h

Figure 14-3429. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG141_LOCK_PROXY	PADCONFIG141_WKUP_EVT_PROXY	PADCONFIG141_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG141_ISO_BYP_PROXY	PADCONFIG141_ISO_OVR_PROXY	PADCONFIG141_TX_DIS_PROXY	PADCONFIG141_DRV_STR_PROXY		PADCONFIG141_RXACTIVE_PROXY	PADCONFIG141_PULLTYPESEL_PROXY	PADCONFIG141_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG141_ST_EN_PROXY	PADCONFIG141_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG141_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG141_WK_LVL_EN_PROXY	RESERVED			PADCONFIG141_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6888. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG141_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG141_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG141_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG141_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG141_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6888. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG141_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG141_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG141_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG141_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG141_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG141_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG141_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG141_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG141_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG141_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG141_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.331 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143_PROXY Register

14.2.1.2.1.2.2.331.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143_PROXY Register (Offset = 623Ch) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6889. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 623Ch

Figure 14-3430. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG143_LOCK_PROXY	PADCONFIG143_WKUP_EVT_PROXY	PADCONFIG143_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG143_ISO_BYP_PROXY	PADCONFIG143_ISO_OVR_PROXY	PADCONFIG143_TX_DIS_PROXY	PADCONFIG143_DRV_STR_PROXY		PADCONFIG143_RXACTIVE_PROXY	PADCONFIG143_PULLTYPESEL_PROXY	PADCONFIG143_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG143_ST_EN_PROXY	PADCONFIG143_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG143_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG143_WK_LVL_EN_PROXY	RESERVED			PADCONFIG143_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6890. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG143_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG143_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG143_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG143_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG143_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6890. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG143_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG143_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG143_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG143_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG143_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG143_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG143_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG143_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG143_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG143_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG143_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.332 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144_PROXY Register

14.2.1.2.1.2.2.332.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144_PROXY Register (Offset = 6240h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6891. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6240h

Figure 14-3431. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG144_LOCK_PROXY	PADCONFIG144_WKUP_EVT_PROXY	PADCONFIG144_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG144_ISO_BYP_PROXY	PADCONFIG144_ISO_OVR_PROXY	PADCONFIG144_TX_DIS_PROXY	PADCONFIG144_DRV_STR_PROXY		PADCONFIG144_RXACTIVE_PROXY	PADCONFIG144_PULLTYPESEL_PROXY	PADCONFIG144_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG144_ST_EN_PROXY	PADCONFIG144_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG144_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG144_WK_LVL_EN_PROXY	RESERVED				PADCONFIG144_MUXMODE_PROXY		
R/W	NONE				R/W		
0h	0h				7h		

Table 14-6892. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG144_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG144_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG144_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG144_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG144_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6892. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG144_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG144_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG144_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG144_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG144_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG144_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG144_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG144_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG144_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG144_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG144_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.333 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145_PROXY Register

14.2.1.2.1.2.2.333.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145_PROXY Register (Offset = 6244h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6893. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6244h

Figure 14-3432. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG145_LOCK_PROXY	PADCONFIG145_WKUP_EVT_PROXY	PADCONFIG145_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG145_ISO_BYP_PROXY	PADCONFIG145_ISO_OVR_PROXY	PADCONFIG145_TX_DIS_PROXY	PADCONFIG145_DRV_STR_PROXY		PADCONFIG145_RXACTIVE_PROXY	PADCONFIG145_PULLTYPESEL_PROXY	PADCONFIG145_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	14	13	12	11	10	9	8
	PADCONFIG145_ST_EN_PROXY	PADCONFIG145_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG145_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG145_WK_LVL_EN_PROXY	RESERVED			PADCONFIG145_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6894. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG145_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG145_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG145_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG145_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG145_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6894. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG145_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG145_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG145_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG145_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG145_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG145_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG145_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG145_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG145_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG145_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG145_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.334 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147_PROXY Register

14.2.1.2.1.2.2.334.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147_PROXY Register (Offset = 624Ch) [reset = 8014000h]

Register to control pin configuration and muxing

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Table 14-6895. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 624Ch

Figure 14-3433. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG147_LOCK_PROXY	PADCONFIG147_WKUP_EVT_PROXY	PADCONFIG147_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG147_ISO_BYP_PROXY	PADCONFIG147_ISO_OVR_PROXY	PADCONFIG147_TX_DIS_PROXY	PADCONFIG147_DRV_STR_PROXY		PADCONFIG147_RXACTIVE_PROXY	PADCONFIG147_PULLTYPESEL_PROXY	PADCONFIG147_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG147_ST_EN_PROXY	PADCONFIG147_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG147_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG147_WK_LVL_EN_PROXY	RESERVED			PADCONFIG147_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-6896. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG147_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG147_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG147_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG147_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG147_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6896. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG147_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG147_TX_DIS_PROXY	R/W	0h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG147_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG147_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG147_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG147_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG147_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG147_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG147_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG147_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG147_MUXMODE_PROXY	R/W	0h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.335 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149_PROXY Register

14.2.1.2.1.2.2.335.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149_PROXY Register (Offset = 6254h) [reset = 204007h]

Register to control pin configuration and muxing

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Table 14-6897. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 6254h

Figure 14-3434. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG149_LOCK_PROXY	PADCONFIG149_WKUP_EVT_PROXY	PADCONFIG149_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
PADCONFIG149_ISO_BYP_PROXY	PADCONFIG149_ISO_OVR_PROXY	PADCONFIG149_TX_DIS_PROXY	PADCONFIG149_DRV_STR_PROXY		PADCONFIG149_RXACTIVE_PROXY	PADCONFIG149_PULLTYPESEL_PROXY	PADCONFIG149_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
	PADCONFIG149_ST_EN_PROXY	PADCONFIG149_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG149_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	6	5	4	3	2	1	0
PADCONFIG149_WK_LVL_EN_PROXY	RESERVED			PADCONFIG149_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6898. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG149_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG149_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG149_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG149_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG149_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6898. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG149_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG149_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG149_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG149_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG149_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG149_PULLUDEN_PROXY	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG149_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG149_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG149_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG149_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG149_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.336 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171_PROXY Register

14.2.1.2.1.2.2.336.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171_PROXY Register (Offset = 62ACh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6899. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62ACh

Figure 14-3435. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG171_LOCK_PROXY	PADCONFIG171_WKUP_EVT_PROXY	PADCONFIG171_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG171_ISO_BYP_PROXY	PADCONFIG171_ISO_OVR_PROXY	PADCONFIG171_TX_DIS_PROXY	PADCONFIG171_DRV_STR_PROXY		PADCONFIG171_RXACTIVE_PROXY	PADCONFIG171_PULLTYPESEL_PROXY	PADCONFIG171_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG171_ST_EN_PROXY	PADCONFIG171_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG171_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG171_WK_LVL_EN_PROXY	RESERVED			PADCONFIG171_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6900. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG171_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG171_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG171_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG171_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG171_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6900. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG171_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG171_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG171_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG171_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG171_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG171_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG171_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG171_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG171_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG171_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG171_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.337 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172_PROXY Register

14.2.1.2.1.2.2.337.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172_PROXY Register (Offset = 62B0h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6901. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62B0h

Figure 14-3436. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG172_LOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PADCONFIG172_DEBOUNCE_SEL_PROXY			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6902. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG172_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG172_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG172_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.338 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173_PROXY Register

14.2.1.2.1.2.2.338.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173_PROXY Register (Offset = 62B4h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6903. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62B4h

Figure 14-3437. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG173_LOCK_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="3">PADCONFIG173_DEBOUNCE_SEL_PROXY</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="2">NONE</td><td colspan="3">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6904. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG173_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG173_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG173_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.339 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174_PROXY Register

14.2.1.2.1.2.2.339.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174_PROXY Register (Offset = 62B8h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6905. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62B8h

Figure 14-3438. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG174_LOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PADCONFIG174_DEBOUNCE_SEL_PROXY			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6906. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG174_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG174_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG174_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.340 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175_PROXY Register

14.2.1.2.1.2.2.340.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175_PROXY Register (Offset = 62BCh) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6907. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62BCh

Figure 14-3439. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG175_LOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PADCONFIG175_DEBOUNCE_SEL_PROXY			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6908. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG175_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG175_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG175_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.341 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176_PROXY Register

14.2.1.2.1.2.2.341.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176_PROXY Register (Offset = 62C0h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6909. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62C0h

Figure 14-3440. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176_PROXY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PADCONFIG176_LOCK_PROXY</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="3">PADCONFIG176_DEBOUNCE_SEL_PROXY</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="2">NONE</td><td colspan="3">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6910. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG176_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG176_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG176_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.342 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177_PROXY Register

14.2.1.2.1.2.2.342.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177_PROXY Register (Offset = 62C4h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6911. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62C4h

Figure 14-3441. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG177_LOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PADCONFIG177_DEBOUNCE_SEL_PROXY			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-6912. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG177_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG177_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG177_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.343 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178_PROXY Register

14.2.1.2.1.2.2.343.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178_PROXY Register (Offset = 62C8h) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6913. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62C8h

Figure 14-3442. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG178_LOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		PADCONFIG178_DEBOUNCE_SEL_PROXY			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-6914. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG178_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG178_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG178_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.344 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179_PROXY Register

14.2.1.2.1.2.2.344.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179_PROXY Register (Offset = 62CCh) [reset = 0h]

Register to control pin configuration and muxing

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Table 14-6915. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62CCh

Figure 14-3443. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG179_LOCK_PROXY	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PADCONFIG179_DEBOUNCE_SEL_PROXY			RESERVED		
NONE		R/W			NONE		
0h		0h			0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6916. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG179_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG179_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30:14	RESERVED	NONE	0h	Reserved
13:11	PADCONFIG179_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:0	RESERVED	NONE	0h	Reserved

14.2.1.2.1.2.2.345 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180_PROXY Register

14.2.1.2.1.2.2.345.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180_PROXY Register (Offset = 62D0h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6917. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62D0h

Figure 14-3444. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG180_LOCK_PROXY	PADCONFIG180_WKUP_EVT_PROXY	PADCONFIG180_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG180_ISO_BYP_PROXY	PADCONFIG180_ISO_OVR_PROXY	PADCONFIG180_TX_DIS_PROXY	PADCONFIG180_DRV_STR_PROXY		PADCONFIG180_RXACTIVE_PROXY	PADCONFIG180_PULLTYPESEL_PROXY	PADCONFIG180_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG180_ST_EN_PROXY	PADCONFIG180_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG180_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG180_WK_LVL_EN_PROXY	RESERVED			PADCONFIG180_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6918. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG180_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG180_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG180_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG180_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG180_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6918. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG180_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG180_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG180_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG180_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG180_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG180_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG180_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG180_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG180_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG180_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG180_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.346 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181_PROXY Register

14.2.1.2.1.2.2.346.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181_PROXY Register (Offset = 62D4h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6919. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62D4h

Figure 14-3445. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG181_LOCK_PROXY	PADCONFIG181_WKUP_EVT_PROXY	PADCONFIG181_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG181_ISO_BYP_PROXY	PADCONFIG181_ISO_OVR_PROXY	PADCONFIG181_TX_DIS_PROXY	PADCONFIG181_DRV_STR_PROXY		PADCONFIG181_RXACTIVE_PROXY	PADCONFIG181_PULLTYPESEL_PROXY	PADCONFIG181_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG181_ST_EN_PROXY	PADCONFIG181_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG181_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG181_WK_LVL_EN_PROXY	RESERVED			PADCONFIG181_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6920. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG181_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG181_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG181_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG181_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG181_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6920. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG181_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG181_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG181_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG181_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG181_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG181_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG181_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG181_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG181_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG181_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG181_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.347 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182_PROXY Register

14.2.1.2.1.2.2.347.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182_PROXY Register (Offset = 62D8h) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6921. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62D8h

Figure 14-3446. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG182_LOCK_PROXY	PADCONFIG182_WKUP_EVT_PROXY	PADCONFIG182_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG182_ISO_BYP_PROXY	PADCONFIG182_ISO_OVR_PROXY	PADCONFIG182_TX_DIS_PROXY	PADCONFIG182_DRV_STR_PROXY		PADCONFIG182_RXACTIVE_PROXY	PADCONFIG182_PULLTYPESEL_PROXY	PADCONFIG182_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG182_ST_EN_PROXY	PADCONFIG182_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG182_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG182_WK_LVL_EN_PROXY	RESERVED			PADCONFIG182_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6922. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG182_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG182_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG182_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG182_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG182_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6922. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG182_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG182_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG182_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG182_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG182_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG182_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG182_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG182_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG182_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG182_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG182_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.348 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183_PROXY Register

14.2.1.2.1.2.2.348.1 MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183_PROXY Register (Offset = 62DCh) [reset = 8214007h]

Register to control pin configuration and muxing

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Table 14-6923. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 62DCh

Figure 14-3447. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183_PROXY Name Register

31	30	29	28	27	26	25	24
PADCONFIG183_LOCK_PROXY	PADCONFIG183_WKUP_EVT_PROXY	PADCONFIG183_WKUP_EN_PROXY					
R/W	R	R/W					
0h	0h	0h	0h	1h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PADCONFIG183_ISO_BYP_PROXY	PADCONFIG183_ISO_OVR_PROXY	PADCONFIG183_TX_DIS_PROXY	PADCONFIG183_DRV_STR_PROXY		PADCONFIG183_RXACTIVE_PROXY	PADCONFIG183_PULLTYPESEL_PROXY	PADCONFIG183_PULLUDEN_PROXY
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	1h	0h		0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PADCONFIG183_ST_EN_PROXY	PADCONFIG183_DEBOUNCE_SEL_PROXY			RESERVED		PADCONFIG183_WK_LVL_POL_PROXY
	R/W	R/W			NONE		R/W
0h	1h	0h			0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PADCONFIG183_WK_LVL_EN_PROXY	RESERVED			PADCONFIG183_MUXMODE_PROXY			
R/W	NONE			R/W			
0h	0h			7h			

Table 14-6924. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PADCONFIG183_LOCK_PROXY	R/W	0h	Lock 0 - Padconfig register is unlocked 1 - Padconfig register is locked from further writes Reset Source: mod_por_rst_n
30	PADCONFIG183_WKUP_EVT_PROXY	R	0h	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin Reset Source: mod_por_rst_n
29	PADCONFIG183_WKUP_EN_PROXY	R/W	0h	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled Reset Source: mod_por_rst_n
23	PADCONFIG183_ISO_BYP_PROXY	R/W	0h	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed Reset Source: mod_por_rst_n
22	PADCONFIG183_ISO_OVR_PROXY	R/W	0h	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden Reset Source: mod_por_rst_n

Table 14-6924. MAIN_PADCFG_CTRL_MMRCFG0_PADCONFIG183_PROXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PADCONFIG183_TX_DIS_PROXY	R/W	1h	Driver Disable 0 - Driver is enabled 1 - Driver is disabled Reset Source: mod_por_rst_n
20:19	PADCONFIG183_DRV_STR_PROXY	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types) Reset Source: mod_por_rst_n
18	PADCONFIG183_RXACTIVE_PROXY	R/W	0h	Input enable for the Pad 0 - Receiver disabled 1 - Receiver enabled Reset Source: mod_por_rst_n
17	PADCONFIG183_PULLTYPESEL_PROXY	R/W	0h	Pad Pullup / Pulldown type selection 0 - Pulldown selected 1 - Pullup selected Reset Source: mod_por_rst_n
16	PADCONFIG183_PULLUDEN_PROXY	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0 - Pullup / Pulldown enabled 1 - Pullup / Pulldown disabled Reset Source: mod_por_rst_n
14	PADCONFIG183_ST_EN_PROXY	R/W	1h	Receiver Schmitt Trigger enable 0 - Schmitt trigger input disabled 1 - Schmitt trigger input enabled Reset Source: mod_por_rst_n
13:11	PADCONFIG183_DEBOUNCE_SEL_PROXY	R/W	0h	Selects the debouce period for the pad. Reset Source: mod_por_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	PADCONFIG183_WK_LVL_POL_PROXY	R/W	0h	Level Sensitive Wakeup Polarity This bit is not relevant unless wk_lvl_en is set to 1'b1. 0 - Low. A low (0) value on the pin causes a wakeup 1 - High. A high (1) value on the pin causes a wakeup Reset Source: mod_por_rst_n
7	PADCONFIG183_WK_LVL_EN_PROXY	R/W	0h	Level Sensitive Wakeup Enable 0 - Disabled. Wakeup is triggered by change of the pin input value 1 - Enabled. Wakeup is triggered when the pin matches the value specified by wk_lvl_pol. The chosen polarity must be maintained. (e.g. until wakeup completion is confirmed) Reset Source: mod_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	PADCONFIG183_MUXMODE_PROXY	R/W	7h	Pad functional signal mux selection Field values (others are reserved): 4'b0000 - Mux Mode 0 4'b0001 - Mux Mode 1 4'b0010 - Mux Mode 2 4'b0011 - Mux Mode 3 4'b0100 - Mux Mode 4 4'b0101 - Mux Mode 5 4'b0110 - Mux Mode 6 4'b0111 - Mux Mode 7 4'b1000 - Mux Mode 8 4'b1001 - Mux Mode 9 4'b1010 - Mux Mode 10 4'b1011 - Mux Mode 11 4'b1100 - Mux Mode 12 4'b1101 - Mux Mode 13 4'b1110 - Mux Mode 14 4'b1111 - Mux Mode 15 Reset Source: mod_por_rst_n

14.2.1.2.1.2.2.349 MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register

14.2.1.2.1.2.2.349.1 MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register (Offset = 7008h) [reset = 0h]

- KICK0 component

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Table 14-6925. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 7008h

Figure 14-3448. MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK0_PROXY							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK1_KICK0_PROXY							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK1_KICK0_PROXY							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK1_KICK0_PROXY							
R/W							
0h							

Table 14-6926. MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK0_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK0_PROXY	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.350 MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register

14.2.1.2.1.2.2.350.1 MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register (Offset = 700Ch) [reset = 0h]

- KICK1 component

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Table 14-6927. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 700Ch

Figure 14-3449. MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Name Register

31	30	29	28	27	26	25	24
LOCK1_KICK1_PROXY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCK1_KICK1_PROXY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK1_KICK1_PROXY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK1_KICK1_PROXY							
R/W							
0h							

Table 14-6928. MAIN_PADCFG_CTRL_MMRCFG0_LOCK1_KICK1_PROXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK1_KICK1_PROXY	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.351 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register

14.2.1.2.1.2.2.351.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register (Offset = 7100h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6929. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 7100h

Figure 14-3450. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R0							
R/W							
0h							

Table 14-6930. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R0	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.352 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register

14.2.1.2.1.2.2.352.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register (Offset = 7104h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6931. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 7104h

Figure 14-3451. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLAIMREG_P1_R1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLAIMREG_P1_R1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLAIMREG_P1_R1							
R/W							
0h							

Table 14-6932. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R1	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.353 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2 Register

14.2.1.2.1.2.2.353.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2 Register (Offset = 7108h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6933. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 7108h

Figure 14-3452. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R2							
R/W							
0h							

Table 14-6934. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R2	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.354 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3 Register

14.2.1.2.1.2.2.354.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3 Register (Offset = 710Ch) [reset = 0h]

Claim bits for Partition 1

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Table 14-6935. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 710Ch

Figure 14-3453. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R3							
R/W							
0h							

Table 14-6936. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R3	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.355 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4 Register

14.2.1.2.1.2.2.355.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4 Register (Offset = 7110h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6937. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 7110h

Figure 14-3454. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R4							
R/W							
0h							

Table 14-6938. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R4	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.2.1.2.2.356 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5 Register

14.2.1.2.1.2.2.356.1 MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5 Register (Offset = 7114h) [reset = 0h]

Claim bits for Partition 1

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Table 14-6939. Instance Table

Instance Name	Physical Address
PADCFG_CTRL0	000F 7114h

Figure 14-3455. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5 Name Register

31	30	29	28	27	26	25	24
CLAIMREG_P1_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAIMREG_P1_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAIMREG_P1_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAIMREG_P1_R5							
R/W							
0h							

Table 14-6940. MAIN_PADCFG_CTRL_MMRCFG0_CLAIMREG_P1_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAIMREG_P1_R5	R/W	0h	Claim bits for Partition 1 Reset Source: mod_g_rst_n

14.2.1.3 Security Control Registers

14.2.1.3.1 MAIN_SEC_MMR

MAIN_SEC_MMR

14.2.1.3.1.1 MAIN_SEC_MMR Summaries

MAIN_SEC_MMR Summaries

Table 14-6941. MAIN_SEC_MMR_CFG2 Registers, Base Address=4590 0000h, Length=65536

Offset	Length	Register Name	MAIN_SEC_MMR0 Physical Address
0h	32	MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG	4590 0000h
40h	32	MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG	4590 0040h
1000h	32	MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG	4590 1000h
1040h	32	MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG	4590 1040h
D000h	32	MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG	4590 D000h
E000h	32	MAIN_SEC_MMR_CFG2_CLSTR14_CORE0_DBG_CFG	4590 E000h

Table 14-6942. MAIN_SEC_MMR_CFG0 Registers, Base Address=45A0 0000h, Length=65536

Offset	Length	Register Name	MAIN_SEC_MMR0 Physical Address
0h	32	MAIN_SEC_MMR_CFG0_PID	45A0 0000h
20h	32	MAIN_SEC_MMR_CFG0_CLSTR0_DEF	45A0 0020h
40h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CFG	45A0 0040h
80h	32	MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL	45A0 0080h
90h	32	MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT	45A0 0090h
100h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG	45A0 0100h
110h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO	45A0 0110h
114h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI	45A0 0114h
120h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL	45A0 0120h
130h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT	45A0 0130h
180h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG	45A0 0180h
190h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO	45A0 0190h
194h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI	45A0 0194h
1A0h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL	45A0 01A0h
1B0h	32	MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT	45A0 01B0h
1020h	32	MAIN_SEC_MMR_CFG0_CLSTR1_DEF	45A0 1020h
1040h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CFG	45A0 1040h
1080h	32	MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL	45A0 1080h
1090h	32	MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT	45A0 1090h
1100h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG	45A0 1100h
1110h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO	45A0 1110h
1114h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI	45A0 1114h
1120h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL	45A0 1120h
1130h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT	45A0 1130h
1180h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG	45A0 1180h
1190h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO	45A0 1190h

Table 14-6942. MAIN_SEC_MMR_CFG0 Registers, Base Address=45A0 0000h, Length=65536 (continued)

Offset	Length	Register Name	MAIN_SEC_MMR0 Physical Address
1194h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI	45A0 1194h
11A0h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL	45A0 11A0h
11B0h	32	MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT	45A0 11B0h
D020h	32	MAIN_SEC_MMR_CFG0_CLSTR13_DEF	45A0 D020h
D040h	32	MAIN_SEC_MMR_CFG0_CLSTR13_CFG	45A0 D040h
D090h	32	MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT	45A0 D090h
D110h	32	MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO	45A0 D110h
D114h	32	MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI	45A0 D114h
E020h	32	MAIN_SEC_MMR_CFG0_CLSTR14_DEF	45A0 E020h
E040h	32	MAIN_SEC_MMR_CFG0_CLSTR14_CFG	45A0 E040h
E090h	32	MAIN_SEC_MMR_CFG0_CLSTR14_PMSTAT	45A0 E090h
E110h	32	MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_LO	45A0 E110h
E114h	32	MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_HI	45A0 E114h

14.2.1.3.1.2 MAIN_SEC_MMR Registers

MAIN_SEC_MMR Registers

14.2.1.3.1.2.1 MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register

14.2.1.3.1.2.1.1 MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register (Offset = 0h) [reset = AA00h]

Configures debug operation for R5FSS0 Core0

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Table 14-6943. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	4590 0000h

Figure 14-3456. MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_DBG_CFG_DBGEN				CLSTR0_CORE0_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6944. MAIN_SEC_MMR_CFG2_CLSTR0_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR0_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
11:8	CLSTR0_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.2 MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Register

14.2.1.3.1.2.2.1 MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Register (Offset = 40h) [reset = AA00h]

Configures debug operation for R5FSS0 Core1

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Table 14-6945. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	4590 0040h

Figure 14-3457. MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">CLSTR0_CORE1_DBG_CFG_DBGEN</td><td colspan="4">CLSTR0_CORE1_DBG_CFG_NIDEN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Ah</td><td colspan="4">Ah</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-6946. MAIN_SEC_MMR_CFG2_CLSTR0_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR0_CORE1_DBG_CFG_DBGEN	R/W	Ah	Core1 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
11:8	CLSTR0_CORE1_DBG_CFG_NIDEN	R/W	Ah	Core1 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.3 MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG Register

14.2.1.3.1.2.3.1 MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG Register (Offset = 1000h) [reset = AA00h]

Configures debug operation for R5FSS1 Core0

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Table 14-6947. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	4590 1000h

Figure 14-3458. MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE0_DBG_CFG_DBGEN				CLSTR1_CORE0_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6948. MAIN_SEC_MMR_CFG2_CLSTR1_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR1_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
11:8	CLSTR1_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.4 MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG Register

14.2.1.3.1.2.4.1 MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG Register (Offset = 1040h) [reset = AA00h]

Configures debug operation for R5FSS1 Core1

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Table 14-6949. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	4590 1040h

Figure 14-3459. MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE1_DBG_CFG_DBGEN				CLSTR1_CORE1_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-6950. MAIN_SEC_MMR_CFG2_CLSTR1_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR1_CORE1_DBG_CFG_DBGEN	R/W	Ah	Core1 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
11:8	CLSTR1_CORE1_DBG_CFG_NIDEN	R/W	Ah	Core1 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.5 MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG Register

14.2.1.3.1.2.5.1 MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG Register (Offset = D000h) [reset = AAh]

Configures debug operation for C7x 0

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Table 14-6951. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	4590 D000h

Figure 14-3460. MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR13_CORE0_DBG_CFG_SPNIDEN				CLSTR13_CORE0_DBG_CFG_SPIDEN			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
CLSTR13_CORE0_DBG_CFG_NIDEN				CLSTR13_CORE0_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-6952. MAIN_SEC_MMR_CFG2_CLSTR13_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR13_CORE0_DBG_CFG_SPNIDEN	R	0h	Core0 Secure Non-invasive debug enable. 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
11:8	CLSTR13_CORE0_DBG_CFG_SPIDEN	R	0h	Core0 Secure Invasive debug enable. 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
7:4	CLSTR13_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
3:0	CLSTR13_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n

14.2.1.3.1.2.6 MAIN_SEC_MMR_CFG2_CLSTR14_CORE0_DBG_CFG Register

14.2.1.3.1.2.6.1 MAIN_SEC_MMR_CFG2_CLSTR14_CORE0_DBG_CFG Register (Offset = E000h) [reset = AAh]

Configures debug operation for C7x 1

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Table 14-6953. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	4590 E000h

Figure 14-3461. MAIN_SEC_MMR_CFG2_CLSTR14_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR14_CORE0_DBG_CFG_SPNIDEN				CLSTR14_CORE0_DBG_CFG_SPIDEN			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
CLSTR14_CORE0_DBG_CFG_NIDEN				CLSTR14_CORE0_DBG_CFG_DBGEN			
R/W				R/W			
Ah				Ah			

Table 14-6954. MAIN_SEC_MMR_CFG2_CLSTR14_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR14_CORE0_DBG_CFG_SPNIDEN	R	0h	Core0 Secure Non-invasive debug enable. 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
11:8	CLSTR14_CORE0_DBG_CFG_SPIDEN	R	0h	Core0 Secure Invasive debug enable. 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
7:4	CLSTR14_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
3:0	CLSTR14_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n

14.2.1.3.1.2.7 MAIN_SEC_MMR_CFG0_PID Register

14.2.1.3.1.2.7.1 MAIN_SEC_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-6955. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0000h

Figure 14-3462. MAIN_SEC_MMR_CFG0_PID Name Register

31	30	29	28	27	26	25	24
PID_MSB16							
R							
6180h							
23	22	21	20	19	18	17	16
PID_MSB16							
R							
6180h							
15	14	13	12	11	10	9	8
PID_MISC					PID_MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
PID_CUSTOM		PID_MINOR					
R		R					
0h		15h					

Table 14-6956. MAIN_SEC_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.3.1.2.8 MAIN_SEC_MMR_CFG0_CLSTR0_DEF Register

14.2.1.3.1.2.8.1 MAIN_SEC_MMR_CFG0_CLSTR0_DEF Register (Offset = 20h) [reset = 2FF10h]

Defines the type of the processor cluster

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Table 14-6957. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0020h

Figure 14-3463. MAIN_SEC_MMR_CFG0_CLSTR0_DEF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">CLSTR0_DEF_CORE_NUM</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLSTR0_DEF_DSP_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLSTR0_DEF_ARM_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-6958. MAIN_SEC_MMR_CFG0_CLSTR0_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR0_DEF_CORE_NUM	R	2h	Number of cores in cluster 001 - Single Core 010 - Dual Core 100 - Quad Core Reset Source: mod_g_rst_n
15:8	CLSTR0_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'h10 - AC7x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR0_DEF_ARM_CORE_TYPE	R	10h	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.3.1.2.9 MAIN_SEC_MMR_CFG0_CLSTR0_CFG Register

14.2.1.3.1.2.9.1 MAIN_SEC_MMR_CFG0_CLSTR0_CFG Register (Offset = 40h) [reset = 0h]

Configures cluster level characteristics

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Table 14-6959. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0040h

Figure 14-3464. MAIN_SEC_MMR_CFG0_CLSTR0_CFG Name Register

31	30	29	28	27	26	25	24
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CLSTR0_CFG_SINGLE_CORE_ONLY	CLSTR0_CFG_SINGLE_CORE	CLSTR0_CFG_MEM_INIT_DIS	CLSTR0_CFG_LOCKSTEP_EN	CLSTR0_CFG_DBG_NO_CLKSTOP	CLSTR0_CFG_TEINIT	CLSTR0_CFG_LOCKSTEP
	R	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6960. MAIN_SEC_MMR_CFG0_CLSTR0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
6	CLSTR0_CFG_SINGLE_CORE_ONLY	R	0h	Single / Dual Core Custer Support: 0 = Both Dual and Single Core are supported 1 = Only Single Core Mode is Supported Reset Source: sys_por_rst_n
5	CLSTR0_CFG_SINGLE_CORE	R/W	0h	Single / Dual Core Mode: 0 = Both Cores are activate 1 = Only Core0 is active. Reset Source: sys_por_rst_n
4	CLSTR0_CFG_MEM_INIT_DIS	R/W	0h	Disables SRAM initialization (TCM, Cache Tags, etc) at reset Initialization must be performed for proper initial ECC initialization. The mem_init_dis value must be selected prior to R5 reset assertion. 1'b0 - Perform memory initialization 1'b1 - Disable memory initialization Reset Source: mod_g_rst_n
3	CLSTR0_CFG_LOCKSTEP_EN	R	0h	Lockstep enable. Indicates if R5 lockstep operation is supported on the device Reset Source: sys_por_rst_n
2	CLSTR0_CFG_DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior 0 - CPU clocks stopped and nCLOCKSTOPPED asserted in standby mode 1 - CPU clocks not stopped in standby mode Reset Source: sys_por_rst_n
1	CLSTR0_CFG_TEINIT	R/W	0h	Exception handling state at reset: 0 - ARM mode 1 - Thumb mode CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n

Table 14-6960. MAIN_SEC_MMR_CFG0_CLSTR0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLSTR0_CFG_LOCKSTEP	R/W	0h	When set, Core0 and Core1 operate in lockstep mode. Can only be changed if lockstep operation is supported as indicated by CLSTR0_CFG_lockstep_en = 1. If CLSTR0_CFG_lockstep_en = 0, lockstep is not supported, this bit will be read only with a value of 0. Reset Source: sys_por_rst_n

14.2.1.3.1.2.10 MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL Register

14.2.1.3.1.2.10.1 MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL Register (Offset = 80h) [reset = 0h]

Configures Cluster overall power state

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Table 14-6961. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0080h

Figure 14-3465. MAIN_SEC_MMR_CFG0_CLSTR0_PMCTRL Name Register

31	30	29	28	27	26	25	24
0h							
23	22	21	20	19	18	17	16
0h							
15	14	13	12	11	10	9	8
0h							
7	6	5	4	3	2	1	0
0h							

14.2.1.3.1.2.11 MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT Register

14.2.1.3.1.2.11.1 MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT Register (Offset = 90h) [reset = 0h]

Shows Cluster overall power status

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Table 14-6962. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0090h

Figure 14-3466. MAIN_SEC_MMR_CFG0_CLSTR0_PMSTAT Name Register

31	30	29	28	27	26	25	24
0h							
23	22	21	20	19	18	17	16
0h							
15	14	13	12	11	10	9	8
0h							
7	6	5	4	3	2	1	0
0h							

14.2.1.3.1.2.12 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register

14.2.1.3.1.2.12.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register (Offset = 100h) [reset = 880h]

Configures the TCM and interrupt operation of R5 Core0

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Table 14-6963. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0100h

Figure 14-3467. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR0_CORE0_CFG_NMFI_EN	RESERVED			CLSTR0_CORE0_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR0_CORE0_CFG_BTCM_EN	RESERVED			CLSTR0_CORE0_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-6964. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR0_CORE0_CFG_NMFI_EN	R/W	0h	Enable Core0 Non-Maskable Fast Interrupts CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR0_CORE0_CFG_TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator 0 - BTCM located at address 0x0 1 - ATCM located at address 0x0 CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR0_CORE0_CFG_BTCM_EN	R/W	1h	Enable Core0 BTCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE0_CFG_ATCM_EN	R/W	0h	Enable Core0 ATCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.13 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register

14.2.1.3.1.2.13.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register (Offset = 110h) [reset = 200h]

Contains the lower 32 bits of the boot vector location for R5 Core0. Bits 4:0 are not used and are always 0.

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Table 14-6965. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0110h

Figure 14-3468. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	22	21	20	19	18	17	16
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	6	5	4	3	2	1	0
CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-6966. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR0_CORE0_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.14 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register

14.2.1.3.1.2.14.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register (Offset = 114h) [reset = 0h]

Contains the lower 16 bits of the boot vector location for R5 Core0

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Table 14-6967. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0114h

Figure 14-3469. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-6968. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR0_CORE0_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.3.1.2.15 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register

14.2.1.3.1.2.15.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register (Offset = 120h) [reset = 0h]

Configures Cluster Core0 power state

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Table 14-6969. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0120h

Figure 14-3470. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLSTR0_CORE0_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-6970. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR0_CORE0_PMCTRL_CORE_HALT	R/W	0h	Halt Core0 Field values (others are reserved): 1'b0 - Core0 is held waiting to begin execution after reset 1'b1 - Core0 is released for execution after reset Reset Source: sys_por_rst_n

14.2.1.3.1.2.16 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register

14.2.1.3.1.2.16.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register (Offset = 130h) [reset = 0h]

Shows Cluster Core0 power status

Return to Summary Table

Table 14-6971. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0130h

Figure 14-3471. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLSTR0_CORE0_PMSTAT_CLK_GATE	RESERVED	CLSTR0_CORE0_PMSTAT_WFE	CLSTR0_CORE0_PMSTAT_WFI
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-6972. MAIN_SEC_MMR_CFG0_CLSTR0_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE0_PMSTAT_CLK_GATE	R	0h	Core0 Clocked stopped due to WFI or WFE state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR0_CORE0_PMSTAT_WFE	R	0h	Core0 WFE When 0, indicates that Core0 is in the WFE state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n
0	CLSTR0_CORE0_PMSTAT_WFI	R	0h	Core0 WFI When 0, indicates that Core0 is in the WFI state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n

14.2.1.3.1.2.17 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG Register

14.2.1.3.1.2.17.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG Register (Offset = 180h) [reset = 880h]

Configures the TCM and interrupt operation of R5 Core1

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Table 14-6973. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0180h

Figure 14-3472. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE1_CFG_NMFI_EN	RESERVED			CLSTR0_CORE1_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	6	5	4	3	2	1	0
CLSTR0_CORE1_CFG_BTCM_EN	RESERVED			CLSTR0_CORE1_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-6974. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR0_CORE1_CFG_NMFI_EN	R/W	0h	Enable Core1 Non-Maskable Fast Interrupts CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR0_CORE1_CFG_TCM_RSTBASE	R/W	1h	Core1 A/BTCM Reset Base Address Indicator 0 - BTCM located at address 0x0 1 - ATCM located at address 0x0 CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR0_CORE1_CFG_BTCM_EN	R/W	1h	Enable Core1 BTCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE1_CFG_ATCM_EN	R/W	0h	Enable Core1 ATCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.18 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO Register

14.2.1.3.1.2.18.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO Register (Offset = 190h) [reset = 200h]

Contains the lower 32 bits of the boot vector location for R5 Core1. Bits 4:0 are not used and are always 0.

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Table 14-6975. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0190h

Figure 14-3473. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	22	21	20	19	18	17	16
CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	14	13	12	11	10	9	8
CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	6	5	4	3	2	1	0
CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-6976. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR0_CORE1_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.19 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI Register

14.2.1.3.1.2.19.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI Register (Offset = 194h) [reset = 0h]

Contains the lower 16 bits of the boot vector location for R5 Core1

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Table 14-6977. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 0194h

Figure 14-3474. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR0_CORE1_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR0_CORE1_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-6978. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR0_CORE1_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.3.1.2.20 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL Register

14.2.1.3.1.2.20.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL Register (Offset = 1A0h) [reset = 0h]

Configures Cluster Core1 power state

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Table 14-6979. Instance Table

Instance Name	**Physical Address**
MAIN_SEC_MMR0	45A0 01A0h

Figure 14-3475. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLSTR0_CORE1_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-6980. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR0_CORE1_PMCTRL_CORE_HALT	R/W	0h	Halt Core1 Field values (others are reserved): 1'b0 - Core1 is held waiting to begin execution after reset 1'b1 - Core1 is released for execution after reset Reset Source: sys_por_rst_n

14.2.1.3.1.2.21 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT Register

14.2.1.3.1.2.21.1 MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT Register (Offset = 1B0h) [reset = 0h]

Shows Cluster Core1 power status

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Table 14-6981. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 01B0h

Figure 14-3476. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>CLSTR0_CORE1_PMSTAT_CLK_GATE</td><td>RESERVED</td><td>CLSTR0_CORE1_PMSTAT_WFE</td><td>CLSTR0_CORE1_PMSTAT_WFI</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td>NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-6982. MAIN_SEC_MMR_CFG0_CLSTR0_CORE1_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR0_CORE1_PMSTAT_CLK_GATE	R	0h	Core1 Clocked stopped due to WFI or WFE state Note: Bit value is invalid when Core1 is in reset Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR0_CORE1_PMSTAT_WFE	R	0h	Core1 WFE When 0, indicates that Core1 is in the WFE state Note: Bit value is invalid when Core1 is in reset Reset Source: mod_g_rst_n
0	CLSTR0_CORE1_PMSTAT_WFI	R	0h	Core1 WFI When 0, indicates that Core1 is in the WFI state Note: Bit value is invalid when Core1 is in reset Reset Source: mod_g_rst_n

14.2.1.3.1.2.22 MAIN_SEC_MMR_CFG0_CLSTR1_DEF Register

14.2.1.3.1.2.22.1 MAIN_SEC_MMR_CFG0_CLSTR1_DEF Register (Offset = 1020h) [reset = 2FF10h]

Defines the type of the processor cluster

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Table 14-6983. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1020h

Figure 14-3477. MAIN_SEC_MMR_CFG0_CLSTR1_DEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					CLSTR1_DEF_CORE_NUM		
NONE					R		
0h					2h		
15	14	13	12	11	10	9	8
CLSTR1_DEF_DSP_CORE_TYPE							
R							
FFh							
7	6	5	4	3	2	1	0
CLSTR1_DEF_ARM_CORE_TYPE							
R							
10h							

Table 14-6984. MAIN_SEC_MMR_CFG0_CLSTR1_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR1_DEF_CORE_NUM	R	2h	Number of cores in cluster 001 - Single Core 010 - Dual Core 100 - Quad Core Reset Source: mod_g_rst_n
15:8	CLSTR1_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'h10 - AC7x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR1_DEF_ARM_CORE_TYPE	R	10h	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.3.1.2.23 MAIN_SEC_MMR_CFG0_CLSTR1_CFG Register

14.2.1.3.1.2.23.1 MAIN_SEC_MMR_CFG0_CLSTR1_CFG Register (Offset = 1040h) [reset = 0h]

Configures cluster level characteristics

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Table 14-6985. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1040h

Figure 14-3478. MAIN_SEC_MMR_CFG0_CLSTR1_CFG Name Register

31	30	29	28	27	26	25	24
0h							

23	22	21	20	19	18	17	16
0h							

15	14	13	12	11	10	9	8
0h							

7	6	5	4	3	2	1	0
	CLSTR1_CFG_SINGLE_CORE_ONLY	CLSTR1_CFG_SINGLE_CORE	CLSTR1_CFG_MEM_INIT_DIS	CLSTR1_CFG_LOCKSTEP_EN	CLSTR1_CFG_DBG_NO_CLKSTOP	CLSTR1_CFG_TEINIT	CLSTR1_CFG_LOCKSTEP
	R	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-6986. MAIN_SEC_MMR_CFG0_CLSTR1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
6	CLSTR1_CFG_SINGLE_CORE_ONLY	R	0h	Single / Dual Core Custer Support: 0 = Both Dual and Single Core are supported 1 = Only Single Core Mode is Supported Reset Source: sys_por_rst_n
5	CLSTR1_CFG_SINGLE_CORE	R/W	0h	Single / Dual Core Mode: 0 = Both Cores are activate 1 = Only Core0 is active. Reset Source: sys_por_rst_n
4	CLSTR1_CFG_MEM_INIT_DIS	R/W	0h	Disables SRAM initialization (TCM, Cache Tags, etc) at reset Initialization must be performed for proper initial ECC initialization. The mem_init_dis value must be selected prior to R5 reset assertion. 1'b0 - Perform memory initialization 1'b1 - Disable memory initialization Reset Source: mod_g_rst_n
3	CLSTR1_CFG_LOCKSTEP_EN	R	0h	Lockstep enable. Indicates if R5 lockstep operation is supported on the device Reset Source: sys_por_rst_n
2	CLSTR1_CFG_DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior 0 - CPU clocks stopped and nCLOCKSTOPPED asserted in standby mode 1 - CPU clocks not stopped in standby mode Reset Source: sys_por_rst_n
1	CLSTR1_CFG_TEINIT	R/W	0h	Exception handling state at reset: 0 - ARM mode 1 - Thumb mode CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n

Table 14-6986. MAIN_SEC_MMR_CFG0_CLSTR1_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLSTR1_CFG_LOCKSTEP	R/W	0h	When set, Core0 and Core1 operate in lockstep mode. Can only be changed if lockstep operation is supported as indicated by CLSTR1_CFG_lockstep_en = 1. If CLSTR1_CFG_lockstep_en = 0, lockstep is not supported, this bit will be read only with a value of 0. Reset Source: sys_por_rst_n

14.2.1.3.1.2.24 MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL Register

14.2.1.3.1.2.24.1 MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL Register (Offset = 1080h) [reset = 0h]

Configures Cluster overall power state

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Table 14-6987. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1080h

Figure 14-3479. MAIN_SEC_MMR_CFG0_CLSTR1_PMCTRL Name Register

31	30	29	28	27	26	25	24
0h							
23	22	21	20	19	18	17	16
0h							
15	14	13	12	11	10	9	8
0h							
7	6	5	4	3	2	1	0
0h							

14.2.1.3.1.2.25 MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT Register

14.2.1.3.1.2.25.1 MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT Register (Offset = 1090h) [reset = 0h]

Shows Cluster overall power status

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Table 14-6988. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1090h

Figure 14-3480. MAIN_SEC_MMR_CFG0_CLSTR1_PMSTAT Name Register

31	30	29	28	27	26	25	24
0h							
23	22	21	20	19	18	17	16
0h							
15	14	13	12	11	10	9	8
0h							
7	6	5	4	3	2	1	0
0h							

14.2.1.3.1.2.26 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG Register

14.2.1.3.1.2.26.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG Register (Offset = 1100h) [reset = 880h]

Configures the TCM and interrupt operation of R5 Core0

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Table 14-6989. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1100h

Figure 14-3481. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLSTR1_CORE0_CFG_NMFI_EN</td><td colspan="3">RESERVED</td><td>CLSTR1_CORE0_CFG_TCM_RSTBASE</td><td colspan="3">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>1h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CLSTR1_CORE0_CFG_BTCM_EN</td><td colspan="3">RESERVED</td><td>CLSTR1_CORE0_CFG_ATCM_EN</td><td colspan="3">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td></tr>
<tr><td>1h</td><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-6990. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR1_CORE0_CFG_NMFI_EN	R/W	0h	Enable Core0 Non-Maskable Fast Interrupts CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR1_CORE0_CFG_TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator 0 - BTCM located at address 0x0 1 - ATCM located at address 0x0 CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR1_CORE0_CFG_BTCM_EN	R/W	1h	Enable Core0 BTCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3	CLSTR1_CORE0_CFG_ATCM_EN	R/W	0h	Enable Core0 ATCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.27 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO Register

14.2.1.3.1.2.27.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO Register (Offset = 1110h) [reset = 200h]

Contains the lower 32 bits of the boot vector location for R5 Core0. Bits 4:0 are not used and are always 0.

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Table 14-6991. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1110h

Figure 14-3482. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-6992. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR1_CORE0_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.28 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI Register

14.2.1.3.1.2.28.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI Register (Offset = 1114h) [reset = 0h]

Contains the lower 16 bits of the boot vector location for R5 Core0

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Table 14-6993. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1114h

Figure 14-3483. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR1_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-6994. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR1_CORE0_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.3.1.2.29 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL Register

14.2.1.3.1.2.29.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL Register (Offset = 1120h) [reset = 0h]

Configures Cluster Core0 power state

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Table 14-6995. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1120h

Figure 14-3484. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLSTR1_CORE0_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-6996. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR1_CORE0_PMCTRL_CORE_HALT	R/W	0h	Halt Core0 Field values (others are reserved): 1'b0 - Core0 is held waiting to begin execution after reset 1'b1 - Core0 is released for execution after reset Reset Source: sys_por_rst_n

14.2.1.3.1.2.30 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT Register

14.2.1.3.1.2.30.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT Register (Offset = 1130h) [reset = 0h]

Shows Cluster Core0 power status

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Table 14-6997. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1130h

Figure 14-3485. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLSTR1_CORE0_PMSTAT_CLK_GATE	RESERVED	CLSTR1_CORE0_PMSTAT_WFE	CLSTR1_CORE0_PMSTAT_WFI
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-6998. MAIN_SEC_MMR_CFG0_CLSTR1_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR1_CORE0_PMSTAT_CLK_GATE	R	0h	Core0 Clocked stopped due to WFI or WFE state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR1_CORE0_PMSTAT_WFE	R	0h	Core0 WFE When 0, indicates that Core0 is in the WFE state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n
0	CLSTR1_CORE0_PMSTAT_WFI	R	0h	Core0 WFI When 0, indicates that Core0 is in the WFI state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n

14.2.1.3.1.2.31 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG Register

14.2.1.3.1.2.31.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG Register (Offset = 1180h) [reset = 880h]

Configures the TCM and interrupt operation of R5 Core1

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Table 14-6999. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1180h

Figure 14-3486. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE1_CFG_NMFI_EN	RESERVED			CLSTR1_CORE1_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	6	5	4	3	2	1	0
CLSTR1_CORE1_CFG_BTCM_EN	RESERVED			CLSTR1_CORE1_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-7000. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR1_CORE1_CFG_NMFI_EN	R/W	0h	Enable Core1 Non-Maskable Fast Interrupts CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR1_CORE1_CFG_TCM_RSTBASE	R/W	1h	Core1 A/BTCM Reset Base Address Indicator 0 - BTCM located at address 0x0 1 - ATCM located at address 0x0 CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR1_CORE1_CFG_BTCM_EN	R/W	1h	Enable Core1 BTCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved
3	CLSTR1_CORE1_CFG_ATCM_EN	R/W	0h	Enable Core1 ATCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.32 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO Register

14.2.1.3.1.2.32.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO Register (Offset = 1190h) [reset = 200h]

Contains the lower 32 bits of the boot vector location for R5 Core1. Bits 4:0 are not used and are always 0.

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Table 14-7001. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1190h

Figure 14-3487. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-7002. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR1_CORE1_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.3.1.2.33 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI Register

14.2.1.3.1.2.33.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI Register (Offset = 1194h) [reset = 0h]

Contains the lower 16 bits of the boot vector location for R5 Core1

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Table 14-7003. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 1194h

Figure 14-3488. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR1_CORE1_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR1_CORE1_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-7004. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR1_CORE1_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.3.1.2.34 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL Register

14.2.1.3.1.2.34.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL Register (Offset = 11A0h) [reset = 0h]

Configures Cluster Core1 power state

Return to Summary Table

Table 14-7005. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 11A0h

Figure 14-3489. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLSTR1_CORE1_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-7006. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR1_CORE1_PMCTRL_CORE_HALT	R/W	0h	Halt Core1 Field values (others are reserved): 1'b0 - Core1 is held waiting to begin execution after reset 1'b1 - Core1 is released for execution after reset Reset Source: sys_por_rst_n

14.2.1.3.1.2.35 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT Register

14.2.1.3.1.2.35.1 MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT Register (Offset = 11B0h) [reset = 0h]

Shows Cluster Core1 power status

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Table 14-7007. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 11B0h

Figure 14-3490. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLSTR1_CORE1_PMSTAT_CLK_GATE	RESERVED	CLSTR1_CORE1_PMSTAT_WFE	CLSTR1_CORE1_PMSTAT_WFI
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-7008. MAIN_SEC_MMR_CFG0_CLSTR1_CORE1_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR1_CORE1_PMSTAT_CLK_GATE	R	0h	Core1 Clocked stopped due to WFI or WFE state Note: Bit value is invalid when Core1 is in reset Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR1_CORE1_PMSTAT_WFE	R	0h	Core1 WFE When 0, indicates that Core1 is in the WFE state Note: Bit value is invalid when Core1 is in reset Reset Source: mod_g_rst_n
0	CLSTR1_CORE1_PMSTAT_WFI	R	0h	Core1 WFI When 0, indicates that Core1 is in the WFI state Note: Bit value is invalid when Core1 is in reset Reset Source: mod_g_rst_n

14.2.1.3.1.2.36 MAIN_SEC_MMR_CFG0_CLSTR13_DEF Register

14.2.1.3.1.2.36.1 MAIN_SEC_MMR_CFG0_CLSTR13_DEF Register (Offset = D020h) [reset = 10FFh]

Defines the type of the processor cluster

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Table 14-7009. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 D020h

Figure 14-3491. MAIN_SEC_MMR_CFG0_CLSTR13_DEF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">CLSTR13_DEF_CORE_NUM</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLSTR13_DEF_DSP_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLSTR13_DEF_ARM_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
</table>

Table 14-7010. MAIN_SEC_MMR_CFG0_CLSTR13_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR13_DEF_CORE_NUM	R	0h	Number of cores in cluster 000 - Single Core 001 - Dual Core 010 - Quad Core Reset Source: mod_g_rst_n
15:8	CLSTR13_DEF_DSP_CORE_TYPE	R	10h	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'h10 - AC7x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR13_DEF_ARM_CORE_TYPE	R	FFh	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.3.1.2.37 MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register

14.2.1.3.1.2.37.1 MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register (Offset = D040h) [reset = 4454h]

Configures cluster level characteristics

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Table 14-7011. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 D040h

Figure 14-3492. MAIN_SEC_MMR_CFG0_CLSTR13_CFG Name Register

31	30	29	28	27	26	25	24
CLSTR13_CONFIG0_ENDIAN	CLSTR13_CONFIG0_CPU_SYS_RISCV_MODE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED					CLSTR13_CONFIG0_EL2SIZE		
NONE					R		
0h				0h	0h		

15	14	13	12	11	10	9	8
CLSTR13_CONFIG0_L2SIZE					CLSTR13_CONFIG0_L1DSIZE		CLSTR13_CONFIG0_L1PSIZE
R					R		R
8h					2h		0h

7	6	5	4	3	2	1	0
CLSTR13_CONFIG0_L1PSIZE	CLSTR13_CONFIG0_VWIDTH		CLSTR13_CONFIG0_RISCV	CLSTR13_CONFIG0_MMA		CLSTR13_CONFIG0_CPU	
R	R		R	R		R	
0h	2h		1h	1h		0h	

Table 14-7012. MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLSTR13_CONFIG0_ENDIAN	R/W	0h	Reset value of Endian control. 0 - Little Endian 1 - Big Endian Reset Source: mod_g_rst_n
30	CLSTR13_CONFIG0_CPU_SYS_RISCV_MODE	R/W	0h	Activates CPU Booting in RiscV Mode 0 - Boot in C7x ISA Mode 1 - Boot in RiscV ISA Mode Reset Source: mod_g_rst_n
29:20	RESERVED	NONE	0h	Reserved
18:16	CLSTR13_CONFIG0_EL2SIZE	R	0h	EL2 Size Field values (others are reserved): 3'b000 - None 3'b001 - 1 MB 3'b010 - 1.5 MB 3'b011 - 2 MB 3'b100 - 2.5 MB 3'b101 - 3 MB 3'b110 - 3.5MB 3'b111 - 4 Mb Reset Source: mod_g_rst_n
15:11	CLSTR13_CONFIG0_L2SIZE	R	8h	L2 Size Field values (others are reserved): 5'b00000 - None 5'b00001 - 512 KB 5'b00010 - 768 KB 5'b00011 - 1 MB 5'b00100 - 1.25 MB 5'b00101 - 1.5 MB 5'b00110 - 1.75 MB 5'b00111 - 2 MB 5'b01000 - 2.25 MB 5'b01001 - 2.5 MB 5'b01010 - 2.75 MB 5'b01011 - 3 MB 5'b00100 - 3.25 MB 5'b01101 - 3.5 MB 5'b01110 - 3.75 MB 5'b01111 - 4 MB 5'b10000 - 4.5 MB 5'b10001 - 5 MB 5'b10010 - 5.5 MB 5'b10011 - 6 MB 5'b10100 - 6.5 MB 5'b10101 - 7 MB 5'b10110 - 7.5 MB 5'b10111 - 8 MB Reset Source: mod_g_rst_n

Table 14-7012. MAIN_SEC_MMR_CFG0_CLSTR13_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:9	CLSTR13_CONFIG0_L1DSIZE	R	2h	L1D Cache Size Field values (others are reserved): 2'b00 - 32 KB 2'b01 - 48 KB 2'b10 - 64 KB 2'b11 - 128 KB Reset Source: mod_g_rst_n
8:7	CLSTR13_CONFIG0_L1PSIZE	R	0h	L1P Cache Size Field values (others are reserved): 2'b00 - 32 KB 2'b01 - 48 KB 2'b10 - 64 KB 2'b11 - 128 KB Reset Source: mod_g_rst_n
6:5	CLSTR13_CONFIG0_VWIDTH	R	2h	Vector Width Field values (others are reserved): 2'b00 - 64 bit 2'b01 - 128 bit 2'b10 - 256 bit 2'b11 - 512 bit Reset Source: mod_g_rst_n
4	CLSTR13_CONFIG0_RISCV	R	1h	RISCV ISA Support Field values (others are reserved): 1'b0 - Not Supported 1'b1 - Supported Reset Source: mod_g_rst_n
3:2	CLSTR13_CONFIG0_MMA	R	1h	MMA Type Field values (others are reserved): 2'b00 - Reserved 2'b01 - Reserved 2'b10 - MMA2 2'b11 - MMA2p1 Reset Source: mod_g_rst_n
1:0	CLSTR13_CONFIG0_CPU	R	0h	CPU Type Field values (others are reserved): 2'b00 - Reserved 2'b01 - Reserved 2'b10 - Reserved 2'b11 - AC72 R10 Reset Source: mod_g_rst_n

14.2.1.3.1.2.38 MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Register

14.2.1.3.1.2.38.1 MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Register (Offset = D090h) [reset = 0h]

Contains Idle Status for C7x DSP Cluster

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Table 14-7013. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 D090h

Figure 14-3493. MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							CLSTR13_PM_STATUS_DSP_IDLE_STAT16
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CLSTR13_PM_STATUS_DSP_IDLE_STAT8
NONE							R
0h						0h	0h
7	6	5	4	3	2	1	0
CLSTR13_PM_STATUS_DSP_IDLE_STAT7	CLSTR13_PM_STATUS_DSP_IDLE_STAT6	CLSTR13_PM_STATUS_DSP_IDLE_STAT5	CLSTR13_PM_STATUS_DSP_IDLE_STAT4	CLSTR13_PM_STATUS_DSP_IDLE_STAT3	CLSTR13_PM_STATUS_DSP_IDLE_STAT2	CLSTR13_PM_STATUS_DSP_IDLE_STAT1	CLSTR13_PM_STATUS_DSP_IDLE_STAT0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7014. MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	CLSTR13_PM_STATUS_DSP_IDLE_STAT16	R	0h	C7x PBIST Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
8	CLSTR13_PM_STATUS_DSP_IDLE_STAT8	R	0h	C7x DRU Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
7	CLSTR13_PM_STATUS_DSP_IDLE_STAT7	R	0h	C7x L2 Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
6	CLSTR13_PM_STATUS_DSP_IDLE_STAT6	R	0h	C7x Debug Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
5	CLSTR13_PM_STATUS_DSP_IDLE_STAT5	R	0h	C7x SE Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n

Table 14-7014. MAIN_SEC_MMR_CFG0_CLSTR13_PMSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CLSTR13_PM_STATUS_DSP_IDLE_STAT4	R	0h	C7x DMC Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
3	CLSTR13_PM_STATUS_DSP_IDLE_STAT3	R	0h	C7x PMC Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
2	CLSTR13_PM_STATUS_DSP_IDLE_STAT2	R	0h	C7x CPU Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
1	CLSTR13_PM_STATUS_DSP_IDLE_STAT1	R	0h	C7x Core LPSC Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
0	CLSTR13_PM_STATUS_DSP_IDLE_STAT0	R	0h	Composite Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n

14.2.1.3.1.2.39 MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO Register

14.2.1.3.1.2.39.1 MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO Register (Offset = D110h) [reset = 0h]

Contains Bits [33:2] of the Boot Vector for C7x DSP

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Table 14-7015. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 D110h

Figure 14-3494. MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-7016. MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR13_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO	R/W	0h	Reset Vector Base Address 33:2 for C7x Reset Source: mod_g_rst_n

14.2.1.3.1.2.40 MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI Register

14.2.1.3.1.2.40.1 MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI Register (Offset = D114h) [reset = 0h]

Contains Bits [35:34] of the Boot Vector for C7x DSP

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Table 14-7017. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 D114h

Figure 14-3495. MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CLSTR13_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	
NONE						R/W	
0h						0h	

Table 14-7018. MAIN_SEC_MMR_CFG0_CLSTR13_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR13_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	R/W	0h	Reset Vector Base Address 35:34 for C7x Reset Source: mod_g_rst_n

14.2.1.3.1.2.41 MAIN_SEC_MMR_CFG0_CLSTR14_DEF Register

14.2.1.3.1.2.41.1 MAIN_SEC_MMR_CFG0_CLSTR14_DEF Register (Offset = E020h) [reset = 10FFh]

Defines the type of the processor cluster

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Table 14-7019. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 E020h

Figure 14-3496. MAIN_SEC_MMR_CFG0_CLSTR14_DEF Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">CLSTR14_DEF_CORE_NUM</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLSTR14_DEF_DSP_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLSTR14_DEF_ARM_CORE_TYPE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
</table>

Table 14-7020. MAIN_SEC_MMR_CFG0_CLSTR14_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	CLSTR14_DEF_CORE_NUM	R	0h	Number of cores in cluster 000 - Single Core 001 - Dual Core 010 - Quad Core Reset Source: mod_g_rst_n
15:8	CLSTR14_DEF_DSP_CORE_TYPE	R	10h	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'h10 - AC7x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR14_DEF_ARM_CORE_TYPE	R	FFh	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.3.1.2.42 MAIN_SEC_MMR_CFG0_CLSTR14_CFG Register

14.2.1.3.1.2.42.1 MAIN_SEC_MMR_CFG0_CLSTR14_CFG Register (Offset = E040h) [reset = 4454h]

Configures cluster level characteristics

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Table 14-7021. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 E040h

Figure 14-3497. MAIN_SEC_MMR_CFG0_CLSTR14_CFG Name Register

31	30	29	28	27	26	25	24
CLSTR14_CONFIG0_ENDIAN	CLSTR14_CONFIG0_CPU_SYS_RISCV_MODE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED					CLSTR14_CONFIG0_EL2SIZE		
NONE					R		
0h				0h	0h		
15	14	13	12	11	10	9	8
CLSTR14_CONFIG0_L2SIZE					CLSTR14_CONFIG0_L1DSIZE		CLSTR14_CONFIG0_L1PSIZE
R					R		R
8h					2h		0h
7	6	5	4	3	2	1	0
CLSTR14_CONFIG0_L1PSIZE	CLSTR14_CONFIG0_VWIDTH		CLSTR14_CONFIG0_RISCV	CLSTR14_CONFIG0_MMA		CLSTR14_CONFIG0_CPU	
R	R		R	R		R	
0h	2h		1h	1h		0h	

Table 14-7022. MAIN_SEC_MMR_CFG0_CLSTR14_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLSTR14_CONFIG0_ENDIAN	R/W	0h	Reset value of Endian control. 0 - Little Endian 1 - Big Endian Reset Source: mod_g_rst_n
30	CLSTR14_CONFIG0_CPU_SYS_RISCV_MODE	R/W	0h	Activates CPU Booting in RiscV Mode 0 - Boot in C7x ISA Mode 1 - Boot in RiscV ISA Mode Reset Source: mod_g_rst_n
29:20	RESERVED	NONE	0h	Reserved
18:16	CLSTR14_CONFIG0_EL2SIZE	R	0h	EL2 Size Field values (others are reserved): 3'b000 - None 3'b001 - 1 MB 3'b010 - 1.5 MB 3'b011 - 2 MB 3'b100 - 2.5 MB 3'b101 - 3 MB 3'b110 - 3.5MB 3'b111 - 4 Mb Reset Source: mod_g_rst_n
15:11	CLSTR14_CONFIG0_L2SIZE	R	8h	L2 Size Field values (others are reserved): 5'b00000 - None 5'b00001 - 512 KB 5'b00010 - 768 KB 5'b00011 - 1 MB 5'b00100 - 1.25 MB 5'b00101 - 1.5 MB 5'b00110 - 1.75 MB 5'b00111 - 2 MB 5'b01000 - 2.25 MB 5'b01001 - 2.5 MB 5'b01010 - 2.75 MB 5'b01011 - 3 MB 5'b00100 - 3.25 MB 5'b01101 - 3.5 MB 5'b01110 - 3.75 MB 5'b01111 - 4 MB 5'b10000 - 4.5 MB 5'b10001 - 5 MB 5'b10010 - 5.5 MB 5'b10011 - 6 MB 5'b10100 - 6.5 MB 5'b10101 - 7 MB 5'b10110 - 7.5 MB 5'b10111 - 8 MB Reset Source: mod_g_rst_n

Table 14-7022. MAIN_SEC_MMR_CFG0_CLSTR14_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:9	CLSTR14_CONFIG0_L1DSIZE	R	2h	L1D Cache Size Field values (others are reserved): 2'b00 - 32 KB 2'b01 - 48 KB 2'b10 - 64 KB 2'b11 - 128 KB Reset Source: mod_g_rst_n
8:7	CLSTR14_CONFIG0_L1PSIZE	R	0h	L1P Cache Size Field values (others are reserved): 2'b00 - 32 KB 2'b01 - 48 KB 2'b10 - 64 KB 2'b11 - 128 KB Reset Source: mod_g_rst_n
6:5	CLSTR14_CONFIG0_VWIDTH	R	2h	Vector Width Field values (others are reserved): 2'b00 - 64 bit 2'b01 - 128 bit 2'b10 - 256 bit 2'b11 - 512 bit Reset Source: mod_g_rst_n
4	CLSTR14_CONFIG0_RISCV	R	1h	RISCV ISA Support Field values (others are reserved): 1'b0 - Not Supported 1'b1 - Supported Reset Source: mod_g_rst_n
3:2	CLSTR14_CONFIG0_MMA	R	1h	MMA Type Field values (others are reserved): 2'b00 - Reserved 2'b01 - Reserved 2'b10 - MMA2 2'b11 - MMA2p1 Reset Source: mod_g_rst_n
1:0	CLSTR14_CONFIG0_CPU	R	0h	CPU Type Field values (others are reserved): 2'b00 - Reserved 2'b01 - Reserved 2'b10 - Reserved 2'b11 - AC72 R10 Reset Source: mod_g_rst_n

14.2.1.3.1.2.43 MAIN_SEC_MMR_CFG0_CLSTR14_PMSTAT Register

14.2.1.3.1.2.43.1 MAIN_SEC_MMR_CFG0_CLSTR14_PMSTAT Register (Offset = E090h) [reset = 0h]

Contains Idle Status for C7x DSP Cluster

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Table 14-7023. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 E090h

Figure 14-3498. MAIN_SEC_MMR_CFG0_CLSTR14_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							CLSTR14_PM_STATUS_DSP_IDLE_STAT16
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CLSTR14_PM_STATUS_DSP_IDLE_STAT8
NONE							R
0h						0h	0h
7	6	5	4	3	2	1	0
CLSTR14_PM_STATUS_DSP_IDLE_STAT7	CLSTR14_PM_STATUS_DSP_IDLE_STAT6	CLSTR14_PM_STATUS_DSP_IDLE_STAT5	CLSTR14_PM_STATUS_DSP_IDLE_STAT4	CLSTR14_PM_STATUS_DSP_IDLE_STAT3	CLSTR14_PM_STATUS_DSP_IDLE_STAT2	CLSTR14_PM_STATUS_DSP_IDLE_STAT1	CLSTR14_PM_STATUS_DSP_IDLE_STAT0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7024. MAIN_SEC_MMR_CFG0_CLSTR14_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	CLSTR14_PM_STATUS_DSP_IDLE_STAT16	R	0h	C7x PBIST Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
15:10	RESERVED	NONE	0h	Reserved
8	CLSTR14_PM_STATUS_DSP_IDLE_STAT8	R	0h	C7x DRU Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
7	CLSTR14_PM_STATUS_DSP_IDLE_STAT7	R	0h	C7x L2 Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
6	CLSTR14_PM_STATUS_DSP_IDLE_STAT6	R	0h	C7x Debug Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
5	CLSTR14_PM_STATUS_DSP_IDLE_STAT5	R	0h	C7x SE Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n

Table 14-7024. MAIN_SEC_MMR_CFG0_CLSTR14_PMSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CLSTR14_PM_STATUS_DSP_IDLE_STAT4	R	0h	C7x DMC Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
3	CLSTR14_PM_STATUS_DSP_IDLE_STAT3	R	0h	C7x PMC Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
2	CLSTR14_PM_STATUS_DSP_IDLE_STAT2	R	0h	C7x CPU Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
1	CLSTR14_PM_STATUS_DSP_IDLE_STAT1	R	0h	C7x Core LPSC Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n
0	CLSTR14_PM_STATUS_DSP_IDLE_STAT0	R	0h	Composite Idle Status Field values (others are reserved): 1'b0 - Idle 1'b1 - Not Idle Reset Source: mod_g_rst_n

14.2.1.3.1.2.44 MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_LO Register

14.2.1.3.1.2.44.1 MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_LO Register (Offset = E110h) [reset = 0h]

Contains Bits [33:2] of the Boot Vector for C7x DSP

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Table 14-7025. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 E110h

Figure 14-3499. MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR14_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
CLSTR14_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
CLSTR14_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR14_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO							
R/W							
0h							

Table 14-7026. MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLSTR14_RST_VEC_LO_CORE0_RESET_BASE_VECTOR_LO	R/W	0h	Reset Vector Base Address 33:2 for C7x Reset Source: mod_g_rst_n

14.2.1.3.1.2.45 MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_HI Register

14.2.1.3.1.2.45.1 MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_HI Register (Offset = E114h) [reset = 0h]

Contains Bits [35:34] of the Boot Vector for C7x DSP

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Table 14-7027. Instance Table

Instance Name	Physical Address
MAIN_SEC_MMR0	45A0 E114h

Figure 14-3500. MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CLSTR14_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	
NONE						R/W	
0h						0h	

Table 14-7028. MAIN_SEC_MMR_CFG0_CLSTR14_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CLSTR14_RST_VEC_HI_CORE0_RESET_BASE_VECTOR_HI	R/W	0h	Reset Vector Base Address 35:34 for C7x Reset Source: mod_g_rst_n

14.2.1.3.2 WKUP_SEC_MMR

WKUP_SEC_MMR

14.2.1.3.2.1 WKUP_SEC_MMR Summaries

WKUP_SEC_MMR Summaries

Table 14-7029. WKUP_SEC_MMR_CFG2 Registers, Base Address=4592 0000h, Length=131072

Offset	Length	Register Name	WKUP_WKUP_SEC_MMR0 Physical Address
1C000h	32	WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG	4593 C000h
1C040h	32	WKUP_SEC_MMR_CFG2_CLSTR28_CORE1_DBG_CFG	4593 C040h

Table 14-7030. WKUP_SEC_MMR_CFG0 Registers, Base Address=45A2 0000h, Length=131072

Offset	Length	Register Name	WKUP_WKUP_SEC_MMR0 Physical Address
0h	32	WKUP_SEC_MMR_CFG0_PID	45A2 0000h
1C020h	32	WKUP_SEC_MMR_CFG0_CLSTR28_DEF	45A3 C020h
1C040h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CFG	45A3 C040h
1C080h	32	WKUP_SEC_MMR_CFG0_CLSTR28_PMCTRL	45A3 C080h
1C090h	32	WKUP_SEC_MMR_CFG0_CLSTR28_PMSTAT	45A3 C090h
1C100h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG	45A3 C100h
1C110h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO	45A3 C110h
1C114h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI	45A3 C114h
1C120h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL	45A3 C120h
1C130h	32	WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT	45A3 C130h

14.2.1.3.2.2 WKUP_SEC_MMR Registers

WKUP_SEC_MMR Registers

14.2.1.3.2.2.1 WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG Register

14.2.1.3.2.2.1.1 WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG Register (Offset = 1C000h) [reset = AA00h]

Configures debug operation for R5FSS28 Core0

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Table 14-7031. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	4593 C000h

Figure 14-3501. WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR28_CORE0_DBG_CFG_DBGEN				CLSTR28_CORE0_DBG_CFG_NIDEN			
R/W				R/W			
Ah				Ah			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7032. WKUP_SEC_MMR_CFG2_CLSTR28_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	CLSTR28_CORE0_DBG_CFG_DBGEN	R/W	Ah	Core0 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
11:8	CLSTR28_CORE0_DBG_CFG_NIDEN	R/W	Ah	Core0 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable 4'b1010 - Enabled others - Disabled Reset Source: sys_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.1.3.2.2.2 WKUP_SEC_MMR_CFG2_CLSTR28_CORE1_DBG_CFG Register

14.2.1.3.2.2.2.1 WKUP_SEC_MMR_CFG2_CLSTR28_CORE1_DBG_CFG Register (Offset = 1C040h) [reset = 0h]

Configures debug operation for R5FSS28 Core1

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Table 14-7033. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	4593 C040h

Figure 14-3502. WKUP_SEC_MMR_CFG2_CLSTR28_CORE1_DBG_CFG Name Register

31	30	29	28	27	26	25	24
0h							
23	22	21	20	19	18	17	16
0h							
15	14	13	12	11	10	9	8
0h							
7	6	5	4	3	2	1	0
0h							

14.2.1.3.2.2.3 WKUP_SEC_MMR_CFG0_PID Register

14.2.1.3.2.2.3.1 WKUP_SEC_MMR_CFG0_PID Register (Offset = 0h) [reset = 61800215h]

PID register

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Table 14-7035. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A2 0000h

Figure 14-3503. WKUP_SEC_MMR_CFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">15h</td></tr>
</table>

Table 14-7036. WKUP_SEC_MMR_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

14.2.1.3.2.2.4 WKUP_SEC_MMR_CFG0_CLSTR28_DEF Register

14.2.1.3.2.2.4.1 WKUP_SEC_MMR_CFG0_CLSTR28_DEF Register (Offset = 1C020h) [reset = 1FF10h]

Defines the type of the processor cluster

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Table 14-7037. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C020h

Figure 14-3504. WKUP_SEC_MMR_CFG0_CLSTR28_DEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						CLSTR28_DEF_CORE_NUM	
NONE						R	
0h						1h	
15	14	13	12	11	10	9	8
CLSTR28_DEF_DSP_CORE_TYPE							
R							
FFh							
7	6	5	4	3	2	1	0
CLSTR28_DEF_ARM_CORE_TYPE							
R							
10h							

Table 14-7038. WKUP_SEC_MMR_CFG0_CLSTR28_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	CLSTR28_DEF_CORE_NUM	R	1h	Number of cores in cluster 001 - Single Core 010 - Dual Core Reset Source: mod_g_rst_n
15:8	CLSTR28_DEF_DSP_CORE_TYPE	R	FFh	DSP core type configuration Field values (others are reserved): 8'h00 - C7x 8'h01 - C6x 8'hFF - Not DSP Reset Source: mod_g_rst_n
7:0	CLSTR28_DEF_ARM_CORE_TYPE	R	10h	ARM core type configuration Field values (others are reserved): 8'h00 - A53 8'h01 - A57 8'h10 - R5 8'h11 - M4F 8'hFF - Not ARM Reset Source: mod_g_rst_n

14.2.1.3.2.2.5 WKUP_SEC_MMR_CFG0_CLSTR28_CFG Register

14.2.1.3.2.2.5.1 WKUP_SEC_MMR_CFG0_CLSTR28_CFG Register (Offset = 1C040h) [reset = 60h]

Configures cluster level characteristics

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Table 14-7039. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C040h

Figure 14-3505. WKUP_SEC_MMR_CFG0_CLSTR28_CFG Name Register

31	30	29	28	27	26	25	24
0h							
23	22	21	20	19	18	17	16
0h							
15	14	13	12	11	10	9	8
0h							
7	6	5	4	3	2	1	0
	CLSTR28_CFG_SINGLE_CORE_ONLY	CLSTR28_CFG_SINGLE_CORE	CLSTR28_CFG_MEM_INIT_DIS	CLSTR28_CFG_LOCKSTEP_EN	CLSTR28_CFG_DBG_NO_CLKSTOP	CLSTR28_CFG_TEINIT	CLSTR28_CFG_LOCKSTEP
	R	R	R/W	R	R/W	R/W	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-7040. WKUP_SEC_MMR_CFG0_CLSTR28_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
6	CLSTR28_CFG_SINGLE_CORE_ONLY	R	1h	Single / Dual CPU Mode Supported: 0 = Both Dual and Single Core are supported 1 = Only Single Core Mode is Supported Reset Source: sys_por_rst_n
5	CLSTR28_CFG_SINGLE_CORE	R	1h	Single / Dual CPU Mode: 0 = Unsupported on this device 1 = Only CPU0 is active. Reset Source: sys_por_rst_n
4	CLSTR28_CFG_MEM_INIT_DIS	R/W	0h	Disables SRAM initialization (TCM, Cache Tags, etc) at reset Initialization must be performed for proper initial ECC initialization. The mem_init_dis value must be selected prior to R5 reset assertion. 1'b0 - Perform memory initialization 1'b1 - Disable memory initialization Reset Source: mod_g_rst_n
3	CLSTR28_CFG_LOCKSTEP_EN	R	0h	Lockstep Not Supported Reset Source: sys_por_rst_n
2	CLSTR28_CFG_DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior 0 - CPU clocks stopped and nCLOCKSTOPPED asserted in standby mode 1 - CPU clocks not stopped in standby mode Reset Source: sys_por_rst_n
1	CLSTR28_CFG_TEINIT	R/W	0h	Exception handling state at reset: 0 - ARM mode 1 - Thumb mode CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n

Table 14-7040. WKUP_SEC_MMR_CFG0_CLSTR28_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLSTR28_CFG_LOCKSTEP	R	0h	Lockstep Not Supported Reset Source: sys_por_rst_n

14.2.1.3.2.2.6 WKUP_SEC_MMR_CFG0_CLSTR28_PMCTRL Register

14.2.1.3.2.2.6.1 WKUP_SEC_MMR_CFG0_CLSTR28_PMCTRL Register (Offset = 1C080h) [reset = 0h]

Configures Cluster overall power state

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Table 14-7041. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C080h

Figure 14-3506. WKUP_SEC_MMR_CFG0_CLSTR28_PMCTRL Name Register

31	30	29	28	27	26	25	24
0h							
23	22	21	20	19	18	17	16
0h							
15	14	13	12	11	10	9	8
0h							
7	6	5	4	3	2	1	0
0h							

14.2.1.3.2.2.7 WKUP_SEC_MMR_CFG0_CLSTR28_PMSTAT Register

14.2.1.3.2.2.7.1 WKUP_SEC_MMR_CFG0_CLSTR28_PMSTAT Register (Offset = 1C090h) [reset = 0h]

Shows Cluster overall power status

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Table 14-7043. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C090h

Figure 14-3507. WKUP_SEC_MMR_CFG0_CLSTR28_PMSTAT Name Register

31	30	29	28	27	26	25	24
0h							
23	22	21	20	19	18	17	16
0h							
15	14	13	12	11	10	9	8
0h							
7	6	5	4	3	2	1	0
0h							

14.2.1.3.2.2.8 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Register

14.2.1.3.2.2.8.1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Register (Offset = 1C100h) [reset = 880h]

Configures the TCM and interrupt operation of R5 Core0

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Table 14-7045. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C100h

Figure 14-3508. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLSTR28_CORE0_CFG_NMFI_EN	RESERVED			CLSTR28_CORE0_CFG_TCM_RSTBASE	RESERVED		
R/W	NONE			R/W	NONE		
0h	0h			1h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLSTR28_CORE0_CFG_BTCM_EN	RESERVED			CLSTR28_CORE0_CFG_ATCM_EN	RESERVED		
R/W	NONE			R/W	NONE		
1h	0h			0h	0h		

Table 14-7046. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	CLSTR28_CORE0_CFG_NMFI_EN	R/W	0h	Enable Core0 Non-Maskable Fast Interrupts CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
14:12	RESERVED	NONE	0h	Reserved
11	CLSTR28_CORE0_CFG_TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator 0 - BTCM located at address 0x0 1 - ATCM located at address 0x0 CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
10:8	RESERVED	NONE	0h	Reserved
7	CLSTR28_CORE0_CFG_BTCM_EN	R/W	1h	Enable Core0 BTCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
6:4	RESERVED	NONE	0h	Reserved

Table 14-7046. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CLSTR28_CORE0_CFG_ATCM_EN	R/W	0h	Enable Core0 ATCM RAM at reset CAUTION: This bit must not be modified if R5F core has been released from reset. Reset Source: sys_por_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.2.1.3.2.2.9 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO Register

14.2.1.3.2.2.9.1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO Register (Offset = 1C110h) [reset = 200h]

Contains the lower 32 bits of the boot vector location for R5 Core0. Bits 4:0 are not used and are always 0.

Return to Summary Table

Table 14-7047. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C110h

Figure 14-3509. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO Name Register

31	30	29	28	27	26	25	24
CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
23	22	21	20	19	18	17	16
CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
15	14	13	12	11	10	9	8
CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR							
R/W							
4h							
7	6	5	4	3	2	1	0
CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR	RESERVED						
R/W	NONE						
4h	0h						

Table 14-7048. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	CLSTR28_CORE0_BOOTVECT_LO_VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0. Reset Source: sys_por_rst_n
6:0	RESERVED	NONE	0h	Reserved

14.2.1.3.2.2.10 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI Register

14.2.1.3.2.2.10.1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI Register (Offset = 1C114h) [reset = 0h]

Contains the lower 16 bits of the boot vector location for R5 Core0

Return to Summary Table

Table 14-7049. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C114h

Figure 14-3510. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLSTR28_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
CLSTR28_CORE0_BOOTVECT_HI_VECT_ADDR							
R/W							
0h							

Table 14-7050. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLSTR28_CORE0_BOOTVECT_HI_VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32]. Reset Source: sys_por_rst_n

14.2.1.3.2.2.11 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL Register

14.2.1.3.2.2.11.1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL Register (Offset = 1C120h) [reset = 0h]

Configures Cluster Core0 power state

Return to Summary Table

Table 14-7051. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C120h

Figure 14-3511. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CLSTR28_CORE0_PMCTRL_CORE_HALT
NONE							R/W
0h							0h

Table 14-7052. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CLSTR28_CORE0_PMCTRL_CORE_HALT	R/W	0h	Halt Core0 Field values (others are reserved): 1'b0 - CPU is held waiting to begin execution after reset is released 1'b1 - CPU is released to execute Reset Source: sys_por_rst_n

14.2.1.3.2.2.12 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT Register

14.2.1.3.2.2.12.1 WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT Register (Offset = 1C130h) [reset = 0h]

Shows Cluster Core0 power status

Return to Summary Table

Table 14-7053. Instance Table

Instance Name	Physical Address
WKUP_WKUP_SEC_MMR0	45A3 C130h

Figure 14-3512. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLSTR28_CORE0_PMSTAT_CLK_GATE	RESERVED	CLSTR28_CORE0_PMSTAT_WFE	CLSTR28_CORE0_PMSTAT_WFI
NONE				R	NONE	R	R
0h				X	0h	X	X

Table 14-7054. WKUP_SEC_MMR_CFG0_CLSTR28_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CLSTR28_CORE0_PMSTAT_CLK_GATE	R	X	Core0 Clocked stopped due to WFI or WFE state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n
2	RESERVED	NONE	0h	Reserved
1	CLSTR28_CORE0_PMSTAT_WFE	R	X	Core0 WFE When 0, indicates that Core0 is in the WFE state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n
0	CLSTR28_CORE0_PMSTAT_WFI	R	X	Core0 WFI When 0, indicates that Core0 is in the WFI state Note: Bit value is invalid when Core0 is in reset Reset Source: mod_g_rst_n

14.2.2 Power Registers

14.2.2.1 PSC

PSC

14.2.2.1.1 PSC Summaries

PSC Summaries

Table 14-7055. PSC Registers, Base Address=0400 0000h, Length=4096

Offset	Length	Register Name	WKUP_PSC0 Physical Address
0h	32	PSC_PID	0400 0000h
14h	32	PSC_GBLSTAT	0400 0014h
18h	32	PSC_INTEVAL	0400 0018h
40h	32	PSC_MERRPR	0400 0040h
50h	32	PSC_MERRCR	0400 0050h
60h	32	PSC_PERRPR	0400 0060h
68h	32	PSC_PERRCR	0400 0068h
70h	32	PSC_EPCPR	0400 0070h
78h	32	PSC_EPCCR	0400 0078h
100h	32	PSC_RAILSTAT	0400 0100h
104h	32	PSC_RAILCTL	0400 0104h
108h	32	PSC_RAILSEL	0400 0108h
120h	32	PSC_PTCMD	0400 0120h
128h	32	PSC_PTSTAT	0400 0128h
200h	32	PSC_PDSTAT_J	0400 0200h + formula
300h	32	PSC_PDCTL_J	0400 0300h + formula
400h	32	PSC_PDCFG_J	0400 0400h + formula
600h	32	PSC_MDCFG_J	0400 0600h + formula
800h	32	PSC_MDSTAT_J	0400 0800h + formula
A00h	32	PSC_MDCTL_J	0400 0A00h + formula

14.2.2.1.2 PSC Registers

PSC Registers

14.2.2.1.2.1 PSC_PID Register

14.2.2.1.2.1.1 PSC_PID Register (Offset = 0h) [reset = 44820200h]

The peripheral identification register is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect) meaning that the values within this register should be hard-coded with the appropriate values and must not change from their hard-coded values.

Return to Summary Table

Table 14-7056. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0000h

Figure 14-3513. PSC_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">0h</td><td colspan="4">482h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">482h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-7057. PSC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: chip_rst.chip_1_rst_n
29:28	BU	R	0h	Business Unit Reset Source: chip_rst.chip_1_rst_n
27:16	FUNC	R	482h	Module ID Reset Source: chip_rst.chip_1_rst_n
15:11	RTL	R	0h	RTL revision. Will vary depending on release Reset Source: chip_rst.chip_1_rst_n
10:8	MAJOR	R	2h	Major revision Reset Source: chip_rst.chip_1_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: chip_rst.chip_1_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.2 PSC_GBLSTAT Register

14.2.2.1.2.2.1 PSC_GBLSTAT Register (Offset = 14h) [reset = 0h]

This register shows the PSC global status.

Return to Summary Table

Table 14-7058. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0014h

Figure 14-3514. PSC_GBLSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED				EF_SMRFLEX			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EF_SMRFLEX							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							OVRIDE
NONE							R
0h							0h

Table 14-7059. PSC_GBLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	EF_SMRFLEX	R	0h	Smart reflex class0 bits Reset Source: chip_rst.chip_1_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	OVRIDE	R	0h	PSC Override Status Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.3 PSC_INTEVAL Register

14.2.2.1.2.3.1 PSC_INTEVAL Register (Offset = 18h) [reset = 0h]

This register has no storage. Read from this register returns 0.

Return to Summary Table

Table 14-7060. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0018h

Figure 14-3515. PSC_INTEVAL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td>GOSET</td><td>EPCSET</td><td>ERRSET</td><td>RESERVED</td></tr>
<tr><td colspan="4">NONE</td><td>W</td><td>W</td><td>W</td><td>NONE</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>EPCEV</td><td>ERREV</td><td>ALLEV</td></tr>
<tr><td colspan="5">NONE</td><td>W</td><td>W</td><td>W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7061. PSC_INTEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GOSET	W	0h	GOSTAT Interrupt Set Reset Source: chip_rst.chip_1_rst_n
18	EPCSET	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
17	ERRSET	W	0h	Combined Interrupt Set Reset Source: chip_rst.chip_1_rst_n
16:3	RESERVED	NONE	0h	Reserved
2	EPCEV	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
1	ERREV	W	0h	Re_evaluate Error Interrupt Reset Source: chip_rst.chip_1_rst_n
0	ALLEV	W	0h	Re_evaluate combined PSC interrupt Reset Source: chip_rst.chip_1_rst_n 0 Write of 0 has no effect 1 Re-evaluate the combined PSC interrupt PSC_ALLINT

14.2.2.1.2.4 PSC_MERRPR Register

14.2.2.1.2.4.1 PSC_MERRPR Register (Offset = 40h) [reset = 0h]

This register records pending error conditions for all modules. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Table 14-7062. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0040h

Figure 14-3516. PSC_MERRPR Name Register

31	30	29	28	27	26	25	24
M							
R							
0h							
23	22	21	20	19	18	17	16
M							
R							
0h							
15	14	13	12	11	10	9	8
M							
R							
0h							
7	6	5	4	3	2	1	0
M							
R							
0h							

Table 14-7063. PSC_MERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	R	0h	Records pending error conditions. Each bit n represents a module. Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.5 PSC_MERRCR Register

14.2.2.1.2.5.1 PSC_MERRCR Register (Offset = 50h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Table 14-7064. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0050h

Figure 14-3517. PSC_MERRCR Name Register

31	30	29	28	27	26	25	24
M							
W1TC							
0h							
23	22	21	20	19	18	17	16
M							
W1TC							
0h							
15	14	13	12	11	10	9	8
M							
W1TC							
0h							
7	6	5	4	3	2	1	0
M							
W1TC							
0h							

Table 14-7065. PSC_MERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	W1TC	0h	Write of 1 clears the corresponding MERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.6 PSC_PERRPR Register

14.2.2.1.2.6.1 PSC_PERRPR Register (Offset = 60h) [reset = 0h]

This register records pending error conditions for each power domain. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7066. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0060h

Figure 14-3518. PSC_PERRPR Name Register

31	30	29	28	27	26	25	24
P							
R							
0h							
23	22	21	20	19	18	17	16
P							
R							
0h							
15	14	13	12	11	10	9	8
P							
R							
0h							
7	6	5	4	3	2	1	0
P							
R							
0h							

Table 14-7067. PSC_PERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R	0h	Power Domain n Error Condition. Each bit n represents a power domain. Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.7 PSC_PERRCR Register

14.2.2.1.2.7.1 PSC_PERRCR Register (Offset = 68h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7068. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0068h

Figure 14-3519. PSC_PERRCR Name Register

31	30	29	28	27	26	25	24
P							
W1TC							
0h							
23	22	21	20	19	18	17	16
P							
W1TC							
0h							
15	14	13	12	11	10	9	8
P							
W1TC							
0h							
7	6	5	4	3	2	1	0
P							
W1TC							
0h							

Table 14-7069. PSC_PERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	W1TC	0h	Write of 1 clears the corresponding PERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.8 PSC_EPCPR Register

14.2.2.1.2.8.1 PSC_EPCPR Register (Offset = 70h) [reset = 0h]

This register records pending external power control conditions. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7070. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0070h

Figure 14-3520. PSC_EPCPR Name Register

31	30	29	28	27	26	25	24
EPC							
R							
0h							
23	22	21	20	19	18	17	16
EPC							
R							
0h							
15	14	13	12	11	10	9	8
EPC							
R							
0h							
7	6	5	4	3	2	1	0
EPC							
R							
0h							

Table 14-7071. PSC_EPCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	R	0h	External Power Control Intervention Request for Power Domain n Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.9 PSC_EPCCR Register

14.2.2.1.2.9.1 PSC_EPCCR Register (Offset = 78h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7072. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0078h

Figure 14-3521. PSC_EPCCR Name Register

31	30	29	28	27	26	25	24
EPC							
W1TC							
0h							
23	22	21	20	19	18	17	16
EPC							
W1TC							
0h							
15	14	13	12	11	10	9	8
EPC							
W1TC							
0h							
7	6	5	4	3	2	1	0
EPC							
W1TC							
0h							

Table 14-7073. PSC_EPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	W1TC	0h	Write of 1 clears the corresponding EPCPR bit Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.10 PSC_RAILSTAT Register

14.2.2.1.2.10.1 PSC_RAILSTAT Register (Offset = 100h) [reset = 0h]

This register is a read-only and shows the current rail requestor whose request is being granted and the current value of the counter associated with this requestor.

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Table 14-7074. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0100h

Figure 14-3522. PSC_RAILSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">RAILNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RAILCNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7075. PSC_RAILSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	RAILNUM	R	0h	Indicates Current Rail Requestor being processed by GPSC Reset Source: chip_rst.chip_1_rst_n
23:8	RESERVED	NONE	0h	Reserved
7:0	RAILCNT	R	0h	Indicates the current rail counter value Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.11 PSC_RAILCTL Register

14.2.2.1.2.11.1 PSC_RAILCTL Register (Offset = 104h) [reset = 0h]

This register is user programmable. It holds the counter values for rail counter. User can select one of the two counter values to be used for each power domain (see RAILSEL register).

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Table 14-7076. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0104h

Figure 14-3523. PSC_RAILCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RAILCTR1							
R/W							
X							
7	6	5	4	3	2	1	0
RAILCTR0							
R/W							
X							

Table 14-7077. PSC_RAILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RAILCTR1	R/W	X	Rail Counter Value 1 Reset Source: chip_rst.chip_1_rst_n
7:0	RAILCTR0	R/W	X	Rail Counter Value 0 Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.12 PSC_RAILSEL Register

14.2.2.1.2.12.1 PSC_RAILSEL Register (Offset = 108h) [reset = 0h]

User can use this register to select the counter value (RAILCTL) for each power domain.

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Table 14-7078. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0108h

Figure 14-3524. PSC_RAILSEL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">P</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">P</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">P</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">P</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-7079. PSC_RAILSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R/W	X	Rail Counter Select for Power Domain Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.13 PSC_PTCMD Register

14.2.2.1.2.13.1 PSC_PTCMD Register (Offset = 120h) [reset = 0h]

This is a pseudo-command register with no actual storage. Reads return 0. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7080. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0120h

Figure 14-3525. PSC_PTCMD Name Register

31	30	29	28	27	26	25	24
GO							
W1TS							
0h							
23	22	21	20	19	18	17	16
GO							
W1TS							
0h							
15	14	13	12	11	10	9	8
GO							
W1TS							
0h							
7	6	5	4	3	2	1	0
GO							
W1TS							
0h							

Table 14-7081. PSC_PTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GO	W1TS	0h	Power Domain n GO Transition Reset Source: chip_rst.chip_1_rst_n 0 Write of 0 has no effect 1 Sets corresponding PTSTAT.GOSTAT field which causes PSC hardware to evaluate PDCTL.NEXT and MDCTL.NEXT for this domain.

14.2.2.1.2.14 PSC_PTSTAT Register

14.2.2.1.2.14.1 PSC_PTSTAT Register (Offset = 128h) [reset = 0h]

This is a status register. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7082. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0128h

Figure 14-3526. PSC_PTSTAT Name Register

31	30	29	28	27	26	25	24
GOSTAT							
R							
0h							
23	22	21	20	19	18	17	16
GOSTAT							
R							
0h							
15	14	13	12	11	10	9	8
GOSTAT							
R							
0h							
7	6	5	4	3	2	1	0
GOSTAT							
R							
0h							

Table 14-7083. PSC_PTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GOSTAT	R	0h	Power Domain n Transition Command Status Reset Source: chip_rst.chip_1_rst_n 0 No transitions in progress in Power Domain 1 Power Domain Transition in progress. Either the power domain is transitioning, or modules on this domain are transitioning.

14.2.2.1.2.15 PSC_PDSTAT_j Register

14.2.2.1.2.15.1 PSC_PDSTAT_j Register (Offset = 200h) [reset = 0h]

This is a status register. One register per power domain. Each register contains the status for the given power domain.

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Table 14-7084. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0200h + formula

Figure 14-3527. PSC_PDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				EMUIHB	PWRBAD	PORDONE	PORZ
NONE				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			STATE				
NONE			R				
0h			0h				

Table 14-7085. PSC_PDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	EMUIHB	R	0h	Emulation Alters Domain State Reset Source: chip_rst.chip_1_rst_n
10	PWRBAD	R	0h	Power Bad error Reset Source: chip_rst.chip_1_rst_n
9	PORDONE	R	0h	POR Done Input Status Reset Source: chip_rst.chip_1_rst_n
8	PORZ	R	0h	PORz output actual status Reset Source: chip_rst.chip_1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	STATE	R	0h	Current Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 `Power domain is off` 1 `Power domain is on`

14.2.2.1.2.16 PSC_PDCTL_j Register

14.2.2.1.2.16.1 PSC_PDCTL_j Register (Offset = 300h) [reset = 0h]

This is a control register. One register per power domain.

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Table 14-7086. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0300h + formula

Figure 14-3528. PSC_PDCTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>FORCE</td><td>RESERVED</td><td>PWRSW</td><td>ISO</td><td colspan="4">RESERVED</td></tr>
<tr><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">WAKECNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">PDMODE</td><td colspan="2">RESERVED</td><td>EMUIHBIE</td><td>EPCGOOD</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="2">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>NEXT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7087. PSC_PDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit Reset Source: chip_rst.chip_1_rst_n
30	RESERVED	NONE	0h	Reserved
29	PWRSW	R/W	0h	Power shorting Switch Control Reset Source: chip_rst.chip_1_rst_n
28	ISO	R/W	0h	Isolation Cell control Reset Source: chip_rst.chip_1_rst_n
27:24	RESERVED	NONE	0h	Reserved
23:16	WAKECNT	R/W	0h	RAM wake count delay value Reset Source: chip_rst.chip_1_rst_n
15	RESERVED	NONE	0h	Reserved
14:12	PDMODE	R/W	0h	Power Down mode Reset Source: chip_rst.chip_1_rst_n 0 `Core Off, RAM Array Off, RAM Periphery Off` 8 `Core Retention, RAM Array Off, RAM Periphery Off` 9 `Core Retention, RAM Array Retention, RAM Periphery Off` 10 `Core On, RAM Array Retention, RAM Periphery Off` 11 `Core On, RAM Array Retention, RAM Periphery On` 15 `Core On, RAM Array On, RAM Periphery On`

Table 14-7087. PSC_PDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	RESERVED	NONE	0h	Reserved
9	EMUIHBIE	R/W	0h	Emulation alters domain state Reset Source: chip_rst.chip_1_rst_n 0 `Not enabled` 1 `Interrupt enabled`
8	EPCGOOD	R/W	0h	External Power Control Power Good Indication Reset Source: chip_rst.chip_1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	NEXT	R/W	0h	User_Desired Next Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 `Off` 1 `On`

14.2.2.1.2.17 PSC_PDCFG_j Register

14.2.2.1.2.17.1 PSC_PDCFG_j Register (Offset = 400h) [reset = 0h]

This is a status register. It shows PSC settings for easy debug.

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Table 14-7088. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0400h + formula

Figure 14-3529. PSC_PDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ICEPICK	RESERVED	MEMSLPKWK	ALWAYSON
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-7089. PSC_PDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

3	ICEPICK	R	0h	Icepick support
				Reset Source: chip_rst.chip_1_rst_n
				`0 This domain does not have IcePick support`
				`1 This domain has IcePick support because one or more of its LPSCs have IcePick support`

2	RESERVED	NONE	0h	Reserved
1	MEMSLPKWK	R	0h	Memory sleep-wake domain Reset Source: chip_rst.chip_1_rst_n

0	ALWAYSON	R	0h	Always on power domain
				Reset Source: chip_rst.chip_1_rst_n
				`0 This domain is not an AlwaysON power domain`
				`1 This domain is an AlwaysON power domain`

14.2.2.1.2.18 PSC_MDCFG_j Register

14.2.2.1.2.18.1 PSC_MDCFG_j Register (Offset = 600h) [reset = 0h]

This is a constant register showing some PSC settings for easy debug. This register is read only.

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Table 14-7090. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0600h + formula

Figure 14-3530. PSC_MDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PWRDOM				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
AUTOONLY	RESETISO	NEXTLOCK	ASYNC	ICEPICK	PERMDIS	PLLHANDSHAKE	NUMSCRDISBALE
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NUMSCRDISBALE		NUMCLKEN			NUMCLK		
R		R			R		
0h		0h			0h		

Table 14-7091. PSC_MDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PWRDOM	R	0h	Indicates which power domain this module belongs to Reset Source: chip_rst.chip_1_rst_n
15	AUTOONLY	R	0h	0: This LPSC supports all modes, 1: This LPSC supports Enable, AutoSleep or AutoWake only Reset Source: chip_rst.chip_1_rst_n
14	RESETISO	R	0h	0: This LPSC does not support Reset Isolation, 1: This LPSC supports Reset Isolation Reset Source: chip_rst.chip_1_rst_n
13	NEXTLOCK	R	0h	0: MDCTL.NEXT field is writable, 1: MDCTL.NEXT field is locked Reset Source: chip_rst.chip_1_rst_n
12	ASYNC	R	0h	Async Lpsc Reset Source: chip_rst.chip_1_rst_n
11	ICEPICK	R	0h	IcePick support Reset Source: chip_rst.chip_1_rst_n
10	PERMDIS	R	0h	Permanently disable Reset Source: chip_rst.chip_1_rst_n
9	PLLHANDSHAKE	R	0h	RTL parameter PLL_HANDSHAKE Reset Source: chip_rst.chip_1_rst_n

Table 14-7091. PSC_MDCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:6	NUMSCRDISBALE	R	0h	Number of PWR_SCR_DISABLE interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
5:3	NUMCLKEN	R	0h	Number of PWR_CLK_EN interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
2:0	NUMCLK	R	0h	Number of PWR_CLKSTOP interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n

14.2.2.1.2.19 PSC_MDSTAT_j Register

14.2.2.1.2.19.1 PSC_MDSTAT_j Register (Offset = 800h) [reset = 0h]

This register shows the status of each module. Requires one register per module on the device.

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Table 14-7092. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0800h + formula

Figure 14-3531. PSC_MDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EMUIHB	EMURST
NONE						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED			MCKOUT	MRSTDONE	MRSTZ	LRSTDONE	LRSTZ
NONE			R	R	R	R	R
0h			0h	X	X	X	X
7	6	5	4	3	2	1	0
RESERVED		STATE					
NONE		R					
0h		X					

Table 14-7093. PSC_MDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved

17	EMUIHB	R	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active.
				Reset Source: chip_rst.chip_1_rst_n
				`0 No emulation altering user-desired module state`
				`1 Emulation alters user-desired module state`

16	EMURST	R	0h	Emulation Alters Reset
				Reset Source: chip_rst.chip_1_rst_n
				`0 No emulation altering user-desired reset`
				`1 Emulation has altered module reset to be different from what user desires`

15:13	RESERVED	NONE	0h	Reserved

12	MCKOUT	R	0h	Actual modclk output to module
				Reset Source: chip_rst.chip_1_rst_n
				`0 modclk gated`
				`1 modclk on`

11	MRSTDONE	R	X	Module reset initialization done status
				Reset Source: chip_rst.chip_1_rst_n
				`0 module reset initialization not done`
				`1 module reset initialization done`

Table 14-7093. PSC_MDSTAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MRSTZ	R	X	Module reset actual status Reset Source: chip_rst.chip_1_rst_n 0 module reset modrst_po* asserted 1 module reset modrst_po* de-asserted
9	LRSTDONE	R	X	Module local reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 local reset initialization not done 1 local reset initialization done
8	LRSTZ	R	X	Module local reset actual status Reset Source: chip_rst.chip_1_rst_n 0 local reset mod_lrst_po* asserted 1 local reset mod_lrst_po* de-asserted
7:6	RESERVED	NONE	0h	Reserved
5:0	STATE	R	X	These bits indicate the current module state Values 0x0 - 0x5 = Key States Values 0x21 - 0x2B = Transitional States Other Values = Reserved Reset Source: chip_rst.chip_1_rst_n 4 AutoSleep 5 AutoWake 2 Disable 3 Enable 0 SwRstDisable 1 SyncRst 33 Disable Clk On 34 Disable In-Prog (waiting for clkstop_ack = 1) 35 Retry Disable (new vbus_req, retry--give clkstop_req = 1 again) 36 Enable In-Prog 37 Sleep In-Prog 38 ClockOn (from SwRstDisable to SyncRst) 39 ClockOff (from SyncRst to SwRstDisable) 40 ClockOn (from Disable to DisableClkOn) 41 ClockOff (from DisableClkOn to Disable) 42 ClockOn (from AutoSleep/Wake to Sleep In-Prog) 43 ClockOff (from DisableClkOn or Sleep In-Prog to AutoSleep/Wake) Others Reserved

14.2.2.1.2.20 PSC_MDCTL_j Register

14.2.2.1.2.20.1 PSC_MDCTL_j Register (Offset = A00h) [reset = 0h]

This register provides specific control for the individual module. One register per module on the device.

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Table 14-7094. Instance Table

Instance Name	Physical Address
WKUP_PSC0	0400 0A00h + formula

Figure 14-3532. PSC_MDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED						
R/W	NONE						
X	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			RESETISO	BLKCHIP1RST	EMUIHBIE	EMURSTIE	LRSTZ
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			NEXT				
NONE			R/W				
0h			0h				

Table 14-7095. PSC_MDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description

31	FORCE	R/W	X	Force Bit
				Reset Source: chip_rst.chip_1_rst_n
				`0 No force`
				`1 Force`

30:13	RESERVED	NONE	0h	Reserved

12	RESETISO	R/W	0h	Reset Isolation
				Reset Source: chip_rst.chip_1_rst_n
				`0 No reset isolation`
				`1 Enable reset isolation`

11	BLKCHIP1RST	R/W	0h	Block Chip_1_Reset Reset Source: chip_rst.chip_1_rst_n

10	EMUIHBIE	R/W	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active.
				Reset Source: chip_rst.chip_1_rst_n
				`0 Not enabled`
				`1 Interrupt enabled`

9	EMURSTIE	R/W	0h	Emulation Alter Reset Interrupt Enable
				Reset Source: chip_rst.chip_1_rst_n
				`0 Not enabled`
				`1 Interrupt enabled`

Table 14-7095. PSC_MDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

8	LRSTZ	R/W	0h	Module local reset control
				Reset Source: chip_rst.chip_1_rst_n
				`0` `assert local reset`
				`1` `de-assert local reset`

7:5	RESERVED	NONE	0h	Reserved

4:0	NEXT	R/W	0h	Module Next State
				Only key states can be selected in this field.
				If a Reserved value is programmed into MDCTL.NEXT, hardware will internally force the state to SwRstDisable.
				If MDCFG.PERMDIS = 1, the module must remain in SwRstDisable after hardware places it in SwRstDisable state. The user is allowed to write this field but hardware ignores this field and always passes along MDCTL.NEXT = SwRstDisable.
				Reset Source: chip_rst.chip_1_rst_n
				`4` `AutoSleep`
				`5` `AutoWake`
				`2` `Disable`
				`3` `Enable`
				`0` `SwRstDisable`
				`1` `SyncRst`
				`Others` `Reserved`

14.2.2.2 PSC

PSC

14.2.2.2.1 PSC Summaries

PSC Summaries

Table 14-7096. PSC Registers, Base Address=0040 0000h, Length=4096

Offset	Length	Register Name	MAIN_PSC0 Physical Address
0h	32	PSC_PID	0040 0000h
14h	32	PSC_GBLSTAT	0040 0014h
18h	32	PSC_INTEVAL	0040 0018h
40h	32	PSC_MERRPR_J	0040 0040h + formula
50h	32	PSC_MERRCR_J	0040 0050h + formula
60h	32	PSC_PERRPR	0040 0060h
68h	32	PSC_PERRCR	0040 0068h
70h	32	PSC_EPCPR	0040 0070h
78h	32	PSC_EPCCR	0040 0078h
100h	32	PSC_RAILSTAT	0040 0100h
104h	32	PSC_RAILCTL	0040 0104h
108h	32	PSC_RAILSEL	0040 0108h
120h	32	PSC_PTCMD	0040 0120h
128h	32	PSC_PTSTAT	0040 0128h
200h	32	PSC_PDSTAT_J	0040 0200h + formula
300h	32	PSC_PDCTL_J	0040 0300h + formula
400h	32	PSC_PDCFG_J	0040 0400h + formula
600h	32	PSC_MDCFG_J	0040 0600h + formula
800h	32	PSC_MDSTAT_J	0040 0800h + formula
A00h	32	PSC_MDCTL_J	0040 0A00h + formula

14.2.2.2.2 PSC Registers

PSC Registers

14.2.2.2.2.1 PSC_PID Register

14.2.2.2.2.1.1 PSC_PID Register (Offset = 0h) [reset = 44820200h]

The peripheral identification register is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect) meaning that the values within this register should be hard-coded with the appropriate values and must not change from their hard-coded values.

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Table 14-7097. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0000h

Figure 14-3533. PSC_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		0h		482h			
23	22	21	20	19	18	17	16
FUNC							
R							
482h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-7098. PSC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: chip_rst.chip_1_rst_n
29:28	BU	R	0h	Business Unit Reset Source: chip_rst.chip_1_rst_n
27:16	FUNC	R	482h	Module ID Reset Source: chip_rst.chip_1_rst_n
15:11	RTL	R	0h	RTL revision. Will vary depending on release Reset Source: chip_rst.chip_1_rst_n
10:8	MAJOR	R	2h	Major revision Reset Source: chip_rst.chip_1_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: chip_rst.chip_1_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.2 PSC_GBLSTAT Register

14.2.2.2.2.2.1 PSC_GBLSTAT Register (Offset = 14h) [reset = 0h]

This register shows the PSC global status.

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Table 14-7099. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0014h

Figure 14-3534. PSC_GBLSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED				EF_SMRFLEX			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
EF_SMRFLEX							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							OVRIDE
NONE							R
0h							0h

Table 14-7100. PSC_GBLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	EF_SMRFLEX	R	0h	Smart reflex class0 bits Reset Source: chip_rst.chip_1_rst_n
15:1	RESERVED	NONE	0h	Reserved
0	OVRIDE	R	0h	PSC Override Status Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.3 PSC_INTEVAL Register

14.2.2.2.2.3.1 PSC_INTEVAL Register (Offset = 18h) [reset = 0h]

This register has no storage. Read from this register returns 0.

Return to Summary Table

Table 14-7101. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0018h

Figure 14-3535. PSC_INTEVAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				GOSET	EPCSET	ERRSET	RESERVED
NONE				W	W	W	NONE
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPCEV	ERREV	ALLEV
NONE					W	W	W
0h					0h	0h	0h

Table 14-7102. PSC_INTEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GOSET	W	0h	GOSTAT Interrupt Set Reset Source: chip_rst.chip_1_rst_n
18	EPCSET	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
17	ERRSET	W	0h	Combined Interrupt Set Reset Source: chip_rst.chip_1_rst_n
16:3	RESERVED	NONE	0h	Reserved
2	EPCEV	W	0h	External Power Control Interrupt Set Reset Source: chip_rst.chip_1_rst_n
1	ERREV	W	0h	Re_evaluate Error Interrupt Reset Source: chip_rst.chip_1_rst_n

0	ALLEV	W	0h	Re_evaluate combined PSC interrupt
				Reset Source: chip_rst.chip_1_rst_n
				`0 Write of 0 has no effect`
				`1 Re-evaluate the combined PSC interrupt PSC_ALLINT`

14.2.2.2.2.4 PSC_MERRPR_j Register

14.2.2.2.2.4.1 PSC_MERRPR_j Register (Offset = 40h) [reset = 0h]

This register records pending error conditions for all modules. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Table 14-7103. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0040h + formula

Figure 14-3536. PSC_MERRPR_j Name Register

31	30	29	28	27	26	25	24
M							
R							
0h							
23	22	21	20	19	18	17	16
M							
R							
0h							
15	14	13	12	11	10	9	8
M							
R							
0h							
7	6	5	4	3	2	1	0
M							
R							
0h							

Table 14-7104. PSC_MERRPR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	R	0h	Records pending error conditions. Each bit n represents a module. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.5 PSC_MERRCR_j Register

14.2.2.2.2.5.1 PSC_MERRCR_j Register (Offset = 50h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Return to Summary Table

Table 14-7105. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0050h + formula

Figure 14-3537. PSC_MERRCR_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">M</td></tr>
<tr><td colspan="8">W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">M</td></tr>
<tr><td colspan="8">W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">M</td></tr>
<tr><td colspan="8">W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">M</td></tr>
<tr><td colspan="8">W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7106. PSC_MERRCR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	M	W1TC	0h	Write of 1 clears the corresponding MERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.6 PSC_PERRPR Register

14.2.2.2.2.6.1 PSC_PERRPR Register (Offset = 60h) [reset = 0h]

This register records pending error conditions for each power domain. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7107. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0060h

Figure 14-3538. PSC_PERRPR Name Register

31	30	29	28	27	26	25	24
P							
R							
0h							
23	22	21	20	19	18	17	16
P							
R							
0h							
15	14	13	12	11	10	9	8
P							
R							
0h							
7	6	5	4	3	2	1	0
P							
R							
0h							

Table 14-7108. PSC_PERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R	0h	Power Domain n Error Condition. Each bit n represents a power domain. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.7 PSC_PERRCR Register

14.2.2.2.2.7.1 PSC_PERRCR Register (Offset = 68h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Return to Summary Table

Table 14-7109. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0068h

Figure 14-3539. PSC_PERRCR Name Register

31	30	29	28	27	26	25	24
P							
W1TC							
0h							
23	22	21	20	19	18	17	16
P							
W1TC							
0h							
15	14	13	12	11	10	9	8
P							
W1TC							
0h							
7	6	5	4	3	2	1	0
P							
W1TC							
0h							

Table 14-7110. PSC_PERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	W1TC	0h	Write of 1 clears the corresponding PERRPR bit. Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.8 PSC_EPCPR Register

14.2.2.2.2.8.1 PSC_EPCPR Register (Offset = 70h) [reset = 0h]

This register records pending external power control conditions. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7111. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0070h

Figure 14-3540. PSC_EPCPR Name Register

31	30	29	28	27	26	25	24
EPC							
R							
0h							
23	22	21	20	19	18	17	16
EPC							
R							
0h							
15	14	13	12	11	10	9	8
EPC							
R							
0h							
7	6	5	4	3	2	1	0
EPC							
R							
0h							

Table 14-7112. PSC_EPCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	R	0h	External Power Control Intervention Request for Power Domain n Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.9 PSC_EPCCR Register

14.2.2.2.2.9.1 PSC_EPCCR Register (Offset = 78h) [reset = 0h]

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7113. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0078h

Figure 14-3541. PSC_EPCCR Name Register

31	30	29	28	27	26	25	24
EPC							
W1TC							
0h							
23	22	21	20	19	18	17	16
EPC							
W1TC							
0h							
15	14	13	12	11	10	9	8
EPC							
W1TC							
0h							
7	6	5	4	3	2	1	0
EPC							
W1TC							
0h							

Table 14-7114. PSC_EPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPC	W1TC	0h	Write of 1 clears the corresponding EPCPR bit Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.10 PSC_RAILSTAT Register

14.2.2.2.2.10.1 PSC_RAILSTAT Register (Offset = 100h) [reset = 0h]

This register is a read-only and shows the current rail requestor whose request is being granted and the current value of the counter associated with this requestor.

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Table 14-7115. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0100h

Figure 14-3542. PSC_RAILSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED			RAILNUM				
NONE			R				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RAILCNT							
R							
0h							

Table 14-7116. PSC_RAILSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	RAILNUM	R	0h	Indicates Current Rail Requestor being processed by GPSC Reset Source: chip_rst.chip_1_rst_n
23:8	RESERVED	NONE	0h	Reserved
7:0	RAILCNT	R	0h	Indicates the current rail counter value Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.11 PSC_RAILCTL Register

14.2.2.2.2.11.1 PSC_RAILCTL Register (Offset = 104h) [reset = 0h]

This register is user programmable. It holds the counter values for rail counter. User can select one of the two counter values to be used for each power domain (see RAILSEL register).

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Table 14-7117. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0104h

Figure 14-3543. PSC_RAILCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RAILCTR1							
R/W							
X							
7	6	5	4	3	2	1	0
RAILCTR0							
R/W							
X							

Table 14-7118. PSC_RAILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RAILCTR1	R/W	X	Rail Counter Value 1 Reset Source: chip_rst.chip_1_rst_n
7:0	RAILCTR0	R/W	X	Rail Counter Value 0 Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.12 PSC_RAILSEL Register

14.2.2.2.2.12.1 PSC_RAILSEL Register (Offset = 108h) [reset = 0h]

User can use this register to select the counter value (RAILCTL) for each power domain.

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Table 14-7119. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0108h

Figure 14-3544. PSC_RAILSEL Name Register

31	30	29	28	27	26	25	24
P							
R/W							
X							
23	22	21	20	19	18	17	16
P							
R/W							
X							
15	14	13	12	11	10	9	8
P							
R/W							
X							
7	6	5	4	3	2	1	0
P							
R/W							
X							

Table 14-7120. PSC_RAILSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	P	R/W	X	Rail Counter Select for Power Domain Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.13 PSC_PTCMD Register

14.2.2.2.2.13.1 PSC_PTCMD Register (Offset = 120h) [reset = 0h]

This is a pseudo-command register with no actual storage. Reads return 0. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7121. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0120h

Figure 14-3545. PSC_PTCMD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GO</td></tr>
<tr><td colspan="8">W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GO</td></tr>
<tr><td colspan="8">W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GO</td></tr>
<tr><td colspan="8">W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GO</td></tr>
<tr><td colspan="8">W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7122. PSC_PTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GO	W1TS	0h	Power Domain n GO Transition Reset Source: chip_rst.chip_1_rst_n 0 `Write of 0 has no effect` 1 `Sets corresponding PTSTAT.GOSTAT field which causes PSC hardware to evaluate PDCTL.NEXT and MDCTL.NEXT for this domain.`

14.2.2.2.2.14 PSC_PTSTAT Register

14.2.2.2.2.14.1 PSC_PTSTAT Register (Offset = 128h) [reset = 0h]

This is a status register. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

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Table 14-7123. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0128h

Figure 14-3546. PSC_PTSTAT Name Register

31	30	29	28	27	26	25	24
GOSTAT							
R							
0h							
23	22	21	20	19	18	17	16
GOSTAT							
R							
0h							
15	14	13	12	11	10	9	8
GOSTAT							
R							
0h							
7	6	5	4	3	2	1	0
GOSTAT							
R							
0h							

Table 14-7124. PSC_PTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GOSTAT	R	0h	Power Domain n Transition Command Status Reset Source: chip_rst.chip_1_rst_n 0 No transitions in progress in Power Domain 1 Power Domain Transition in progress. Either the power domain is transitioning, or modules on this domain are transitioning.

14.2.2.2.2.15 PSC_PDSTAT_j Register

14.2.2.2.2.15.1 PSC_PDSTAT_j Register (Offset = 200h) [reset = 0h]

This is a status register. One register per power domain. Each register contains the status for the given power domain.

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Table 14-7125. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0200h + formula

Figure 14-3547. PSC_PDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				EMUIHB	PWRBAD	PORDONE	PORZ
NONE				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			STATE				
NONE			R				
0h			0h				

Table 14-7126. PSC_PDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	EMUIHB	R	0h	Emulation Alters Domain State Reset Source: chip_rst.chip_1_rst_n
10	PWRBAD	R	0h	Power Bad error Reset Source: chip_rst.chip_1_rst_n
9	PORDONE	R	0h	POR Done Input Status Reset Source: chip_rst.chip_1_rst_n
8	PORZ	R	0h	PORz output actual status Reset Source: chip_rst.chip_1_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	STATE	R	0h	Current Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 Power domain is off 1 Power domain is on

14.2.2.2.2.16 PSC_PDCTL_j Register

14.2.2.2.2.16.1 PSC_PDCTL_j Register (Offset = 300h) [reset = 0h]

This is a control register. One register per power domain.

Return to Summary Table

Table 14-7127. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0300h + formula

Figure 14-3548. PSC_PDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED	PWRSW	ISO	RESERVED			
R/W	NONE	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
WAKECNT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED	PDMODE			RESERVED		EMUIHBIE	EPCGOOD
NONE	R/W			NONE		R/W	R/W
0h	0h			0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED							NEXT
NONE							R/W
0h							0h

Table 14-7128. PSC_PDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit Reset Source: chip_rst.chip_1_rst_n
30	RESERVED	NONE	0h	Reserved
29	PWRSW	R/W	0h	Power shorting Switch Control Reset Source: chip_rst.chip_1_rst_n
28	ISO	R/W	0h	Isolation Cell control Reset Source: chip_rst.chip_1_rst_n
27:24	RESERVED	NONE	0h	Reserved
23:16	WAKECNT	R/W	0h	RAM wake count delay value Reset Source: chip_rst.chip_1_rst_n
15	RESERVED	NONE	0h	Reserved
14:12	PDMODE	R/W	0h	Power Down mode Reset Source: chip_rst.chip_1_rst_n 0 `Core Off, RAM Array Off, RAM Periphery Off` 8 `Core Retention, RAM Array Off, RAM Periphery Off` 9 `Core Retention, RAM Array Retention, RAM Periphery Off` 10 `Core On, RAM Array Retention, RAM Periphery Off` 11 `Core On, RAM Array Retention, RAM Periphery On` 15 `Core On, RAM Array On, RAM Periphery On`

Table 14-7128. PSC_PDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	RESERVED	NONE	0h	Reserved
9	EMUIHBIE	R/W	0h	Emulation alters domain state Reset Source: chip_rst.chip_1_rst_n 0 `Not enabled` 1 `Interrupt enabled`
8	EPCGOOD	R/W	0h	External Power Control Power Good Indication Reset Source: chip_rst.chip_1_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	NEXT	R/W	0h	User_Desired Next Power Domain State Reset Source: chip_rst.chip_1_rst_n 0 `Off` 1 `On`

14.2.2.2.2.17 PSC_PDCFG_j Register

14.2.2.2.2.17.1 PSC_PDCFG_j Register (Offset = 400h) [reset = 0h]

This is a status register. It shows PSC settings for easy debug.

Return to Summary Table

Table 14-7129. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0400h + formula

Figure 14-3549. PSC_PDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				ICEPICK	RESERVED	MEMSLPKWK	ALWAYSON
NONE				R	NONE	R	R
0h				0h	0h	0h	0h

Table 14-7130. PSC_PDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

3	ICEPICK	R	0h	Icepick support
				Reset Source: chip_rst.chip_1_rst_n
				`0 This domain does not have IcePick support`
				`1 This domain has IcePick support because one or more of its LPSCs have IcePick support`

2	RESERVED	NONE	0h	Reserved
1	MEMSLPKWK	R	0h	Memory sleep-wake domain Reset Source: chip_rst.chip_1_rst_n

0	ALWAYSON	R	0h	Always on power domain
				Reset Source: chip_rst.chip_1_rst_n
				`0 This domain is not an AlwaysON power domain`
				`1 This domain is an AlwaysON power domain`

14.2.2.2.2.18 PSC_MDCFG_j Register

14.2.2.2.2.18.1 PSC_MDCFG_j Register (Offset = 600h) [reset = 0h]

This is a constant register showing some PSC settings for easy debug. This register is read only.

Return to Summary Table

Table 14-7131. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0600h + formula

Figure 14-3550. PSC_MDCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PWRDOM				
NONE			R				
0h			0h				
15	14	13	12	11	10	9	8
AUTOONLY	RESETISO	NEXTLOCK	ASYNC	ICEPICK	PERMDIS	PLLHANDSHAKE	NUMSCRDISBALE
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NUMSCRDISBALE		NUMCLKEN			NUMCLK		
R		R			R		
0h		0h			0h		

Table 14-7132. PSC_MDCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:16	PWRDOM	R	0h	Indicates which power domain this module belongs to Reset Source: chip_rst.chip_1_rst_n
15	AUTOONLY	R	0h	0: This LPSC supports all modes, 1: This LPSC supports Enable, AutoSleep or AutoWake only Reset Source: chip_rst.chip_1_rst_n
14	RESETISO	R	0h	0: This LPSC does not support Reset Isolation, 1: This LPSC supports Reset Isolation Reset Source: chip_rst.chip_1_rst_n
13	NEXTLOCK	R	0h	0: MDCTL.NEXT field is writable, 1: MDCTL.NEXT field is locked Reset Source: chip_rst.chip_1_rst_n
12	ASYNC	R	0h	Async Lpsc Reset Source: chip_rst.chip_1_rst_n
11	ICEPICK	R	0h	IcePick support Reset Source: chip_rst.chip_1_rst_n
10	PERMDIS	R	0h	Permanently disable Reset Source: chip_rst.chip_1_rst_n
9	PLLHANDSHAKE	R	0h	RTL parameter PLL_HANDSHAKE Reset Source: chip_rst.chip_1_rst_n

Table 14-7132. PSC_MDCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:6	NUMSCRDISBALE	R	0h	Number of PWR_SCR_DISABLE interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
5:3	NUMCLKEN	R	0h	Number of PWR_CLK_EN interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n
2:0	NUMCLK	R	0h	Number of PWR_CLKSTOP interfaces required on LPSC Reset Source: chip_rst.chip_1_rst_n

14.2.2.2.2.19 PSC_MDSTAT_j Register

14.2.2.2.2.19.1 PSC_MDSTAT_j Register (Offset = 800h) [reset = 0h]

This register shows the status of each module. Requires one register per module on the device.

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Table 14-7133. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0800h + formula

Figure 14-3551. PSC_MDSTAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EMUIHB	EMURST
NONE						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED			MCKOUT	MRSTDONE	MRSTZ	LRSTDONE	LRSTZ
NONE			R	R	R	R	R
0h			0h	X	X	X	X
7	6	5	4	3	2	1	0
RESERVED		STATE					
NONE		R					
0h		X					

Table 14-7134. PSC_MDSTAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EMUIHB	R	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. Reset Source: chip_rst.chip_1_rst_n 0 `No emulation altering user-desired module state` 1 `Emulation alters user-desired module state`
16	EMURST	R	0h	Emulation Alters Reset Reset Source: chip_rst.chip_1_rst_n 0 `No emulation altering user-desired reset` 1 `Emulation has altered module reset to be different from what user desires`
15:13	RESERVED	NONE	0h	Reserved
12	MCKOUT	R	0h	Actual modclk output to module Reset Source: chip_rst.chip_1_rst_n 0 `modclk gated` 1 `modclk on`
11	MRSTDONE	R	X	Module reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 `module reset initialization not done` 1 `module reset initialization done`

Table 14-7134. PSC_MDSTAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MRSTZ	R	X	Module reset actual status Reset Source: chip_rst.chip_1_rst_n 0 module reset modrst_po* asserted 1 module reset modrst_po* de-asserted
9	LRSTDONE	R	X	Module local reset initialization done status Reset Source: chip_rst.chip_1_rst_n 0 local reset initialization not done 1 local reset initialization done
8	LRSTZ	R	X	Module local reset actual status Reset Source: chip_rst.chip_1_rst_n 0 local reset mod_lrst_po* asserted 1 local reset mod_lrst_po* de-asserted
7:6	RESERVED	NONE	0h	Reserved
5:0	STATE	R	X	These bits indicate the current module state Values 0x0 - 0x5 = Key States Values 0x21 - 0x2B = Transitional States Other Values = Reserved Reset Source: chip_rst.chip_1_rst_n 4 AutoSleep 5 AutoWake 2 Disable 3 Enable 0 SwRstDisable 1 SyncRst 33 Disable Clk On 34 Disable In-Prog (waiting for clkstop_ack = 1) 35 Retry Disable (new vbus_req, retry--give clkstop_req = 1 again) 36 Enable In-Prog 37 Sleep In-Prog 38 ClockOn (from SwRstDisable to SyncRst) 39 ClockOff (from SyncRst to SwRstDisable) 40 ClockOn (from Disable to DisableClkOn) 41 ClockOff (from DisableClkOn to Disable) 42 ClockOn (from AutoSleep/Wake to Sleep In-Prog) 43 ClockOff (from DisableClkOn or Sleep In-Prog to AutoSleep/Wake) Others Reserved

14.2.2.2.2.20 PSC_MDCTL_j Register

14.2.2.2.2.20.1 PSC_MDCTL_j Register (Offset = A00h) [reset = 0h]

This register provides specific control for the individual module. One register per module on the device.

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Table 14-7135. Instance Table

Instance Name	Physical Address
MAIN_PSC0	0040 0A00h + formula

Figure 14-3552. PSC_MDCTL_j Name Register

31	30	29	28	27	26	25	24
FORCE	RESERVED						
R/W	NONE						
X	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			RESETISO	BLKCHIP1RST	EMUIHBIE	EMURSTIE	LRSTZ
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			NEXT				
NONE			R/W				
0h			0h				

Table 14-7136. PSC_MDCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description

31	FORCE	R/W	X	Force Bit
				Reset Source: chip_rst.chip_1_rst_n
				`0 No force`
				`1 Force`

30:13	RESERVED	NONE	0h	Reserved

12	RESETISO	R/W	0h	Reset Isolation
				Reset Source: chip_rst.chip_1_rst_n
				`0 No reset isolation`
				`1 Enable reset isolation`

11	BLKCHIP1RST	R/W	0h	Block Chip_1_Reset Reset Source: chip_rst.chip_1_rst_n

10	EMUIHBIE	R/W	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active.
				Reset Source: chip_rst.chip_1_rst_n
				`0 Not enabled`
				`1 Interrupt enabled`

9	EMURSTIE	R/W	0h	Emulation Alter Reset Interrupt Enable
				Reset Source: chip_rst.chip_1_rst_n
				`0 Not enabled`
				`1 Interrupt enabled`

Table 14-7136. PSC_MDCTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	LRSTZ	R/W	0h	Module local reset control Reset Source: chip_rst.chip_1_rst_n 0 assert local reset 1 de-assert local reset
7:5	RESERVED	NONE	0h	Reserved
4:0	NEXT	R/W	0h	Module Next State Only key states can be selected in this field. If a Reserved value is programmed into MDCTL.NEXT, hardware will internally force the state to SwRstDisable. If MDCFG.PERMDIS = 1, the module must remain in SwRstDisable after hardware places it in SwRstDisable state. The user is allowed to write this field but hardware ignores this field and always passes along MDCTL.NEXT = SwRstDisable. Reset Source: chip_rst.chip_1_rst_n 4 AutoSleep 5 AutoWake 2 Disable 3 Enable 0 SwRstDisable 1 SyncRst Others Reserved

14.2.2.3 VTM

VTM

14.2.2.3.1 VTM Summaries

VTM Summaries

Table 14-7137. VTM_CFG1 Registers, Base Address=00B0 0000h, Length=1024

Offset	Length	Register Name	WKUP_VTM0 Physical Address
0h	32	VTM_CFG1_PID	00B0 0000h
4h	32	VTM_CFG1_DEVINFO_PWR0	00B0 0004h
204h	32	VTM_CFG1_GT_TH1_INT_RAW_STAT_SET	00B0 0204h
208h	32	VTM_CFG1_GT_TH1_INT_EN_STAT_CLR	00B0 0208h
214h	32	VTM_CFG1_GT_TH1_INT_EN_SET	00B0 0214h
218h	32	VTM_CFG1_GT_TH1_INT_EN_CLR	00B0 0218h
224h	32	VTM_CFG1_GT_TH2_INT_RAW_STAT_SET	00B0 0224h
228h	32	VTM_CFG1_GT_TH2_INT_EN_STAT_CLR	00B0 0228h
234h	32	VTM_CFG1_GT_TH2_INT_EN_SET	00B0 0234h
238h	32	VTM_CFG1_GT_TH2_INT_EN_CLR	00B0 0238h
244h	32	VTM_CFG1_LT_TH0_INT_RAW_STAT_SET	00B0 0244h
248h	32	VTM_CFG1_LT_TH0_INT_EN_STAT_CLR	00B0 0248h
254h	32	VTM_CFG1_LT_TH0_INT_EN_SET	00B0 0254h
258h	32	VTM_CFG1_LT_TH0_INT_EN_CLR	00B0 0258h
100h	32	VTM_CFG1_VD_DEVINFO_J	00B0 0100h + formula
104h	32	VTM_CFG1_VD_OPPVID_J	00B0 0104h + formula
108h	32	VTM_CFG1_VD_EVT_STAT_J	00B0 0108h + formula
10Ch	32	VTM_CFG1_VD_EVT_SET_J	00B0 010Ch + formula
110h	32	VTM_CFG1_VD_EVT_CLR_J	00B0 0110h + formula
300h	32	VTM_CFG1_TMPSENS_CTRL_J	00B0 0300h + formula
308h	32	VTM_CFG1_TMPSENS_STAT_J	00B0 0308h + formula
30Ch	32	VTM_CFG1_TMPSENS_TH_J	00B0 030Ch + formula
310h	32	VTM_CFG1_TMPSENS_TH2_J	00B0 0310h + formula

Table 14-7138. VTM_CFG2 Registers, Base Address=00B0 1000h, Length=1024

Offset	Length	Register Name	WKUP_VTM0 Physical Address
Ch	32	VTM_CFG2_MISC_CTRL	00B0 100Ch
10h	32	VTM_CFG2_MISC_CTRL2	00B0 1010h
300h	32	VTM_CFG2_TMPSENS_CTRL_J	00B0 1300h + formula
304h	32	VTM_CFG2_TMPSENS_TRIM_J	00B0 1304h + formula

Table 14-7139. ECC_AGGR Registers, Base Address=00B0 2000h, Length=1024

Offset	Length	Register Name	WKUP_VTM0 Physical Address
0h	32	ECC_AGGR_REV	00B0 2000h
8h	32	ECC_AGGR_VECTOR	00B0 2008h
Ch	32	ECC_AGGR_STAT	00B0 200Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	00B0 2010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	00B0 203Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	00B0 2040h

Table 14-7139. ECC_AGGR Registers, Base Address=00B0 2000h, Length=1024 (continued)

Offset	Length	Register Name	WKUP_VTM0 Physical Address
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	00B0 2080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	00B0 20C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	00B0 213Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	00B0 2140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	00B0 2180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	00B0 21C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	00B0 2200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	00B0 2204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	00B0 2208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	00B0 220Ch

14.2.2.3.2 VTM Registers

VTM Registers

14.2.2.3.2.1 VTM_CFG1_PID Register

14.2.2.3.2.1.1 VTM_CFG1_PID Register (Offset = 0h) [reset = 661B8901h]

VTM Peripheral Identification Register

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Table 14-7140. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0000h

Figure 14-3553. VTM_CFG1_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		61Bh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
61Bh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_RTL					X_MAJOR		
R					R		
11h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		Y_MINOR					
R		R					
0h		1h					

Table 14-7141. VTM_CFG1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: mod_g_rst_n
29:28	BU	R	2h	Business unit - Processors Reset Source: mod_g_rst_n
27:16	FUNC	R	61Bh	Module functional identifier - CTRL MMR Reset Source: mod_g_rst_n
15:11	R_RTL	R	11h	RTL revision number - actual value determined by RTL Reset Source: mod_g_rst_n
10:8	X_MAJOR	R	1h	Major revision number - actual value determined by RTL Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom revision number - actual value determined by RTL Reset Source: mod_g_rst_n
5:0	Y_MINOR	R	1h	Minor revision number - actual value determined by RTL Reset Source: mod_g_rst_n

14.2.2.3.2.2 VTM_CFG1_DEVINFO_PWR0 Register

14.2.2.3.2.2.1 VTM_CFG1_DEVINFO_PWR0 Register (Offset = 4h) [reset = 0h]

Device specific voltage domain and temp sensor information register.

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Table 14-7142. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0004h

Figure 14-3554. VTM_CFG1_DEVINFO_PWR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				VTM_VD_MAP			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED			VD_RTC	RESERVED			
NONE			R	NONE			
0h			0h	0h			
7	6	5	4	3	2	1	0
TMPSENS_CT				CVD_CT			
R				R			
0h				0h			

Table 14-7143. VTM_CFG1_DEVINFO_PWR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	VTM_VD_MAP	R	0h	Core voltage domain, cVD, global mapping 4-bit code, in the context of this SOC. It shows in which cVD this VTM is instantiated/placed. This field indicates in which core voltage domain, cVD, has been physically placed this VTM. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff, d_vtm_vd_map. Reset Source: mod_g_rst_n
15:13	RESERVED	NONE	0h	Reserved
12	VD_RTC	R	0h	RTC voltage domain presence. 0: There is NO VD_RTC in this SOC. 1: There is a VD_RTC in this SOC. Reset value is a VTM tieoff, d_vd_rtc. Reset Source: mod_g_rst_n
11:8	RESERVED	NONE	0h	Reserved
7:4	TMPSENS_CT	R	0h	Number of temperature sensors associated with this VTM. Valid values are 4'h0 - 4'h8. 0x0: NO temp-sensor associated to this VTM. 0x8: 8 temp-sensors associated to this VTM. 0x9 to 0xF: invalid values. Reset value is a VTM tieoff, d_vtm_tmpsens_ct. Reset Source: mod_g_rst_n

Table 14-7143. VTM_CFG1_DEVINFO_PWR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CVD_CT	R	0h	Number of core voltage domains in device. VD0 is always allocated to VD_RTC, if it exists, and VD1 always to VD_WKUP. The maximum number of cVDs in an SOC is 15, 0xF. Reset value is a VTM tieoff, d_device_cvd_ct. Reset Source: mod_g_rst_n

14.2.2.3.2.3 VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register

14.2.2.3.2.3.1 VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register (Offset = 204h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7144. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0204h

Figure 14-3555. VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INT_VD</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7145. VTM_CFG1_GT_TH1_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the pending stats regardless of the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.3.2.4 VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register

14.2.2.3.2.4.1 VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register (Offset = 208h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt GT_TH1 per voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7146. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0208h

Figure 14-3556. VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7147. VTM_CFG1_GT_TH1_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt masked pending bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status that includes the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.3.2.5 VTM_CFG1_GT_TH1_INT_EN_SET Register

14.2.2.3.2.5.1 VTM_CFG1_GT_TH1_INT_EN_SET Register (Offset = 214h) [reset = 0h]

Enable set MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7148. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0214h

Figure 14-3557. VTM_CFG1_GT_TH1_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7149. VTM_CFG1_GT_TH1_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.3.2.6 VTM_CFG1_GT_TH1_INT_EN_CLR Register

14.2.2.3.2.6.1 VTM_CFG1_GT_TH1_INT_EN_CLR Register (Offset = 218h) [reset = 0h]

Enable clear MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH1_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7150. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0218h

Figure 14-3558. VTM_CFG1_GT_TH1_INT_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7151. VTM_CFG1_GT_TH1_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.3.2.7 VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register

14.2.2.3.2.7.1 VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register (Offset = 224h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7152. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0224h

Figure 14-3559. VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7153. VTM_CFG1_GT_TH2_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the pending status regardless of the enable setting. Reset Source: mod_g_rst_n

14.2.2.3.2.8 VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register

14.2.2.3.2.8.1 VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register (Offset = 228h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt GT_TH2 per voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7154. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0228h

Figure 14-3560. VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7155. VTM_CFG1_GT_TH2_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enabled pending bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status including the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.3.2.9 VTM_CFG1_GT_TH2_INT_EN_SET Register

14.2.2.3.2.9.1 VTM_CFG1_GT_TH2_INT_EN_SET Register (Offset = 234h) [reset = 0h]

Enable set MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7156. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0234h

Figure 14-3561. VTM_CFG1_GT_TH2_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7157. VTM_CFG1_GT_TH2_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.3.2.10 VTM_CFG1_GT_TH2_INT_EN_CLR Register

14.2.2.3.2.10.1 VTM_CFG1_GT_TH2_INT_EN_CLR Register (Offset = 238h) [reset = 0h]

Enable clear MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_GT_TH2_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7158. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0238h

Figure 14-3562. VTM_CFG1_GT_TH2_INT_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7159. VTM_CFG1_GT_TH2_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.3.2.11 VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register

14.2.2.3.2.11.1 VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register (Offset = 244h) [reset = 0h]

Interrupt RAW event status and set MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7160. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0244h

Figure 14-3563. VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7161. VTM_CFG1_LT_TH0_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt pending bit set for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the raw pending status regardless of the corresponding enable setting. Reset Source: mod_g_rst_n

14.2.2.3.2.12 VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register

14.2.2.3.2.12.1 VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register (Offset = 248h) [reset = 0h]

Enabled interrupt event status and clear MMR for interrupt LT_TH0 per voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/ mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

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Table 14-7162. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0248h

Figure 14-3564. VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7163. VTM_CFG1_LT_TH0_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enabled pending status bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status that factors in the corresponding enable along with the pending status. Reset Source: mod_g_rst_n

14.2.2.3.2.13 VTM_CFG1_LT_TH0_INT_EN_SET Register

14.2.2.3.2.13.1 VTM_CFG1_LT_TH0_INT_EN_SET Register (Offset = 254h) [reset = 0h]

Enable set MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7164. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0254h

Figure 14-3565. VTM_CFG1_LT_TH0_INT_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TS							
0h							

Table 14-7165. VTM_CFG1_LT_TH0_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TS	0h	Interrupt enable bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.3.2.14 VTM_CFG1_LT_TH0_INT_EN_CLR Register

14.2.2.3.2.14.1 VTM_CFG1_LT_TH0_INT_EN_CLR Register (Offset = 258h) [reset = 0h]

Enable clear MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, VTM_LT_TH0_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7166. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0258h

Figure 14-3566. VTM_CFG1_LT_TH0_INT_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INT_VD							
R/W1TC							
0h							

Table 14-7167. VTM_CFG1_LT_TH0_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INT_VD	R/W1TC	0h	Interrupt enable bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings. Reset Source: mod_g_rst_n

14.2.2.3.2.15 VTM_CFG1_VD_DEVINFO_J Register

14.2.2.3.2.15.1 VTM_CFG1_VD_DEVINFO_J Register (Offset = 100h) [reset = 0h]

Voltage domain a information register. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

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Table 14-7168. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0100h + formula

Figure 14-3567. VTM_CFG1_VD_DEVINFO_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>AVS0_SUP</td><td colspan="4">VD_MAP</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7169. VTM_CFG1_VD_DEVINFO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	AVS0_SUP	R/W	0h	Indicates VD0 AVS class0 support. Indicates if the cVD associated with this VTM's VD MMR supports AVS-Class0: 0: No AVS-Class0. 1: Supports-AVS-Class0. Reset value is from e-fuse at module (POR) reset, efuse_vd[j]_avs_sup. Reset Source: mod_g_rst_n
11:8	VD_MAP	R	0h	Indicates the core voltage domain mapping of VTM VD. Device specific field. This field indicates to which SOC cVD is this VD of this VTM map to. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff, d_vd[j]_vd_map_ipcfg (technically a direct connection, not latched, so reset agnostic). Reset Source: mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.3.2.16 VTM_CFG1_VD_OPPVID_J Register

14.2.2.3.2.16.1 VTM_CFG1_VD_OPPVID_J Register (Offset = 104h) [reset = 0h]

Voltage domain a VID actual code used as reference by Firmware to set the various voltage domain supply voltages. Reset defaults are sourced from efuse for each OPP. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

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Table 14-7170. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0104h + formula

Figure 14-3568. VTM_CFG1_VD_OPPVID_j Name Register

31	30	29	28	27	26	25	24
OPP_3							
R/W							
0h							
23	22	21	20	19	18	17	16
OPP_2							
R/W							
0h							
15	14	13	12	11	10	9	8
OPP_1							
R/W							
0h							
7	6	5	4	3	2	1	0
OPP_0							
R/W							
0h							

Table 14-7171. VTM_CFG1_VD_OPPVID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	OPP_3	R/W	0h	OPP 3 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_3. Reset Source: mod_por_rst_n
23:16	OPP_2	R/W	0h	OPP 2 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_2. Reset Source: mod_por_rst_n
15:8	OPP_1	R/W	0h	OPP 1 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_1. Reset Source: mod_por_rst_n

Table 14-7171. VTM_CFG1_VD_OPPVID_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	OPP_0	R/W	0h	OPP 0 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SOC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[j]_opp_0. Reset Source: mod_por_rst_n

14.2.2.3.2.17 VTM_CFG1_VD_EVT_STAT_J Register

14.2.2.3.2.17.1 VTM_CFG1_VD_EVT_STAT_J Register (Offset = 108h) [reset = 0h]

Voltage domain a event and control status register.

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Table 14-7172. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0108h + formula

Figure 14-3569. VTM_CFG1_VD_EVT_STAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					LT_TH0_ALERT	GT_TH2_ALERT	GT_TH1_ALERT
NONE					R	R	R
0h					0h	0h	0h

Table 14-7173. VTM_CFG1_VD_EVT_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LT_TH0_ALERT	R	0h	This bit reflects the status of the TH0 undertemp alert resulting from the OR of all the similar alerts produced by the temp sensors selected by VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. Reset Source: mod_g_rst_n
1	GT_TH2_ALERT	R	0h	This bit reflects the status of the merged temperature alert resulting from the combination of all the similar alerts produced by the temp-monitors selected as showed in field VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. This field shows the actual present level of the resulting OR function of the combined selected signals. Reset Source: mod_g_rst_n
0	GT_TH1_ALERT	R	0h	This bit reflects the status of the merged temperature alert resulting from the OR of all the similar alerts produced by the temp-monitors selected as showed in field VTM_VD[j]_EVT_SEL_SET.tsens_evt_sel. This field shows the actual present value of the resulting OR function of the combined selected signals. Reset Source: mod_g_rst_n

14.2.2.3.2.18 VTM_CFG1_VD_EVT_SET_J Register

14.2.2.3.2.18.1 VTM_CFG1_VD_EVT_SET_J Register (Offset = 10Ch) [reset = 0h]

Voltage domain a event select and control set register. NOTE: This MMR and the companion MMR VTM_VD[a]_EVT_SEL_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7174. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 010Ch + formula

Figure 14-3570. VTM_CFG1_VD_EVT_SET_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TSENS_EVT_SEL							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7175. VTM_CFG1_VD_EVT_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TSENS_EVT_SEL	R/W1TS	0h	In this field we select which of the event contributions of the 8-maximum possible temp-monitors controlled by this VTM will contribute to generate the merged event/alerts of this VD. Any combination of them could be selected and varies between SOCs and VDs. Eg: 0x00 : No temp-monitor event contributes to generate the temperature events of this VD. 0x06: Temp-monitors[2,1] contribute to generate the temperature events of this VD. ... 0xFF: All 8 temp-monitors contribute to generate the temperature events of this VD. 0: Writing 0 to this field produces no effect. 1: Writing 1 to any of the bits in this field sets to 1 the corresponding bit in that field. Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.2.3.2.19 VTM_CFG1_VD_EVT_CLR_J Register

14.2.2.3.2.19.1 VTM_CFG1_VD_EVT_CLR_J Register (Offset = 110h) [reset = 0h]

Voltage domain a event select and control clear register. NOTE: This MMR and the companion MMR VTM_VD[a]_EVT_SEL_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

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Table 14-7176. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0110h + formula

Figure 14-3571. VTM_CFG1_VD_EVT_CLR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TSENS_EVT_SEL							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-7177. VTM_CFG1_VD_EVT_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TSENS_EVT_SEL	R/W1TC	0h	In this field we select which of the event contributions of the 8-maximum possible temp-monitors controlled by this VTM will contribute to generate the merged event/alerts of this VD. Any combination of them could be selected and varies between SOCs and VDs. Eg: 0x00 : No temp-monitor event contributes to generate the temperature events of this VD. 0x06: Temp-monitors[2,1] contribute to generate the temperature events of this VD. ... 0xFF: All 8 temp-monitors contribute to generate the temperature events of this VD. 0: Writing 0 to this field produces no effect. 1: Writing 1 to any of the bits in this field clears, = 0, the corresponding bit in that field. Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.2.2.3.2.20 VTM_CFG1_TMPSENS_CTRL_J Register

14.2.2.3.2.20.1 VTM_CFG1_TMPSENS_CTRL_J Register (Offset = 300h) [reset = 0h]

Temperature Sensor Band-gap control register for sensor j.

Return to Summary Table

Table 14-7178. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0300h + formula

Figure 14-3572. VTM_CFG1_TMPSENS_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					LT_TH0_EN	GT_TH2_EN	GT_TH1_EN
NONE					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7179. VTM_CFG1_TMPSENS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	LT_TH0_EN	R/W	0h	Enable under-threshold0 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is < value set for threshold point 0. Reset value is POR only. Reset Source: mod_por_rst_n
9	GT_TH2_EN	R/W	0h	Enable over-threshold2 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is > value set for threshold point 2. Reset value is POR only. Reset Source: mod_por_rst_n
8	GT_TH1_EN	R/W	0h	Enable over-threshold1 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is > value set for threshold point 1. Reset value is POR only. Reset Source: mod_por_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.2.2.3.2.21 VTM_CFG1_TMPSENS_STAT_J Register

14.2.2.3.2.21.1 VTM_CFG1_TMPSENS_STAT_J Register (Offset = 308h) [reset = 0h]

Temperature Sensor Band-gap Status register for sensor j.

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Table 14-7180. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0308h + formula

Figure 14-3573. VTM_CFG1_TMPSENS_STAT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				VD_MAP			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
MAXT_OUTRG_ALERT	LT_TH0_ALERT	GT_TH2_ALERT	GT_TH1_ALERT	EOC_FC_UPDATE	DATA_VALID	DATA_OUT	
R	R	R	R	R	R	R	
0h	0h	0h	0h	0h	0h	0h	
7	6	5	4	3	2	1	0
DATA_OUT							
R							
0h							

Table 14-7181. VTM_CFG1_TMPSENS_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	VD_MAP	R	0h	Indicates the core voltage domain placement of the temp sensor. Device specific field. This field indicates in which core voltage domain, cVD, has been physically placed the temp-monitor. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SOCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SOCs, 0x4-0xE = Mapping varies between SOCs, 0xF = not implemented. Reset value is a VTM tieoff at POR, d_VTM_TMPSENS[j]_STAT_vd_map_ipcfg. Reset Source: mod_por_rst_n
15	MAXT_OUTRG_ALERT	R	0h	This bit will be driven to a level 1 for a given temperature monitor if it has its corresponding bit maxt_outrg_en = 1, and the temperature reading is reporting to be outside the max temperature supported, temp > programmed value. The level of this signal is a reflection, with some clock delays, of the temperature code reading. This is NOT an sticky bit. Reset value is POR only. Reset Source: mod_por_rst_n
14	LT_TH0_ALERT	R	0h	This field reflects the status of the lt_th0_alert comparator result during continuous mode. The control MMR field lt_th0_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n

Table 14-7181. VTM_CFG1_TMPSENS_STAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	GT_TH2_ALERT	R	0h	This field reflects the status of the gt_th2_alert comparator result during continuous mode. The control MMR field gt_th2_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n
12	GT_TH1_ALERT	R	0h	This field reflects the status of the gt_th1_alert comparator result during continuous mode. The control MMR field gt_th1_en = 1 is required for this field to become 1. Reset value is at POR or clrz. Reset Source: mod_por_rst_n
11	EOC_FC_UPDATE	R	0h	First time end of conversion. This field is reset to 0 every time VTM.por_rst_n or VTM_TMPSENS[j]_CTRL.clrz are active, or when continuous mode is deasserted. This bit will be set to 1 after the first time after reset release that data_valid transitions from 0 to 1, and remain at 1 until next time either of por_rst_n or VTM_TMPSENS[j]_CTRL.clrz are active, or when continuous mode is deasserted. Reset value is at POR or VTM_TMPSENS[j]_CTRL.clrz, or continuous mode deassertion. Reset Source: mod_por_rst_n
10	DATA_VALID	R	0h	Data_valid signal value from sensor: ADC End of Conversion. End of conversion indicated by 0 to 1 transition. When high data_out(9:0) out of the temp-monitor is valid. This field doesn't reflect the instantaneous output from the temp-monitor. This field gets latched/ updated in this VTM register when the data_valid value from temp-monitor toggles. Note the data_valid sensor output is asserted for only a short time window (on the order of a few clock cycles). Reset value is at POR or VTM_TMPSENS[j]_CTRL.clrz. Reset Source: mod_por_rst_n
9:0	DATA_OUT	R	0h	Data_out signal value from sensor: Temperature data from the ADC in monitor. Valid after VTM_TMPSENS[j]_STAT.eoc_fc_update = 1. This value will be latched in this VTM register every time monitor output data_valid transitions from 0 to 1 (specifically one vbus cycle after data_valid asserts). Reset value is POR only. Reset Source: mod_por_rst_n

14.2.2.3.2.22 VTM_CFG1_TMPSENS_TH_J Register

14.2.2.3.2.22.1 VTM_CFG1_TMPSENS_TH_J Register (Offset = 30Ch) [reset = 0h]

Temperature Sensor Band-gap Threshold register for sensor j.

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Table 14-7182. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 030Ch + formula

Figure 14-3574. VTM_CFG1_TMPSENS_TH_j Name Register

31	30	29	28	27	26	25	24
RESERVED						TH1_VAL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
TH1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED						TH0_VAL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TH0_VAL							
R/W							
0h							

Table 14-7183. VTM_CFG1_TMPSENS_TH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	TH1_VAL	R/W	0h	Threshold point-1, thpt1, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is > th1_val[9:0] and gt_th1_en=1, that will cause the VTM to set the gt_th1_alert output. Once the current temp reading =< th1_val[9:0] then gt_th1_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	TH0_VAL	R/W	0h	Threshold point-0, thpt0, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is < th0_val[9:0] and lt_th0_en=1, that will cause the VTM to set the lt_th0_alert output. Once the current temp reading => th0_val[9:0] then lt_th0_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n

14.2.2.3.2.23 VTM_CFG1_TMPSENS_TH2_J Register

14.2.2.3.2.23.1 VTM_CFG1_TMPSENS_TH2_J Register (Offset = 310h) [reset = 0h]

Temperature Sensor Band-gap Threshold register 2 for sensor j.

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Table 14-7184. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 0310h + formula

Figure 14-3575. VTM_CFG1_TMPSENS_TH2_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TH2_VAL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TH2_VAL							
R/W							
0h							

Table 14-7185. VTM_CFG1_TMPSENS_TH2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TH2_VAL	R/W	0h	Threshold point-2, thpt2, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is > th2_val[9:0] and gt_th2_en=1, that will cause the VTM to set the gt_th2_alert output. Once the current temp reading =< th2_val[9:0] then gt_th2_alert output will go to 0. Reset value is at POR only. Reset Source: mod_por_rst_n

14.2.2.3.2.24 VTM_CFG2_MISC_CTRL Register

14.2.2.3.2.24.1 VTM_CFG2_MISC_CTRL Register (Offset = Ch) [reset = 0h]

VTM miscellaneous control bits.

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Table 14-7186. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 100Ch

Figure 14-3576. VTM_CFG2_MISC_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ANY_MAXT_OUTRG_ALERT_EN
NONE							R/W
0h							0h

Table 14-7187. VTM_CFG2_MISC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ANY_MAXT_OUTRG_ALERT_EN	R/W	0h	This bit when enabled will cause the VTM's output therm_maxtemp_outrange_alert to be driven high, if any of the sources for the maxt_outrg_alert, is set high. Whenever all the maxt_outrg_alert enabled sensor alerts, out of the 8 possible are back to 0 then the output, therm_maxtemp_outrange_alert, will also return to 0. Reset is at POR only. Reset Source: mod_por_rst_n

14.2.2.3.2.25 VTM_CFG2_MISC_CTRL2 Register

14.2.2.3.2.25.1 VTM_CFG2_MISC_CTRL2 Register (Offset = 10h) [reset = 0h]

VTM miscellaneous control bits.

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Table 14-7188. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 1010h

Figure 14-3577. VTM_CFG2_MISC_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESERVED						MAXT_OUTRG_ALERT_THR0	
NONE						R/W	
0h						0h	

23	22	21	20	19	18	17	16
MAXT_OUTRG_ALERT_THR0							
R/W							
0h							

15	14	13	12	11	10	9	8
RESERVED						MAXT_OUTRG_ALERT_THR	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
MAXT_OUTRG_ALERT_THR							
R/W							
0h							

Table 14-7189. VTM_CFG2_MISC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	MAXT_OUTRG_ALERT_THR0	R/W	0h	This defines the global max temperature out of range safe sample value. If the alert is enabled globally and for the sensor and the sensor reads a value <= this value then the alert is cleared after being triggered. This safe threshold defines at what temp the alert can be cleared. Reset is at POR only. Reset Source: mod_por_rst_n
15:10	RESERVED	NONE	0h	Reserved
9:0	MAXT_OUTRG_ALERT_THR	R/W	0h	This defines the global max temperature out of range sample value. If the alert is enabled globally and for the sensor and the sensor reads a value >= this value then the alert is triggered. Reset is at POR only. Reset Source: mod_por_rst_n

14.2.2.3.2.26 VTM_CFG2_TMPSENS_CTRL_J Register

14.2.2.3.2.26.1 VTM_CFG2_TMPSENS_CTRL_J Register (Offset = 300h) [reset = 40h]

Temperature Sensor Band-gap control register for sensor j.

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Table 14-7190. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 1300h + formula

Figure 14-3578. VTM_CFG2_TMPSENS_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MAXT_OUTRG_EN	RESERVED		
NONE				R/W	NONE		
0h				0h	0h		
7	6	5	4	3	2	1	0
RESERVED	CLRZ	SOC	CONT	RESERVED			
NONE	R/W	R/W	R/W	NONE			
0h	1h	0h	0h	0h			

Table 14-7191. VTM_CFG2_TMPSENS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	MAXT_OUTRG_EN	R/W	0h	Enable out-of-range event. This bit enables generation of the alert in case the given temperature sensors generates a temp code above a programmed max. 0 = Don't generate alert. 1 = Generate alert. Reset value is POR only. Reset Source: mod_por_rst_n
10:7	RESERVED	NONE	0h	Reserved
6	CLRZ	R/W	1h	Temp-Monitor control: 0 = Reset all Temp-monitor digital outputs. 1 = Allow operation of sensor. Reset value is POR only. Reset Source: mod_por_rst_n
5	SOC	R/W	0h	Temp-Monitor control: ADC Start of Conversion. A transition from 0 to 1 starts a new ADC conversion cycle. The bit with automatically clear when the conversion has completed. This mode is not valid when already in continuous mode. Reset value is POR only. Reset Source: mod_por_rst_n
4	CONT	R/W	0h	Temp-Monitor control: ADC Continuous mode. Setting this mode enables the VTM to continuously monitor the sensor automatically. Each sample period the sensor will be accessed and the results captured. Reset value is POR only. Reset Source: mod_por_rst_n
3:0	RESERVED	NONE	0h	Reserved

14.2.2.3.2.27 VTM_CFG2_TMPSENS_TRIM_J Register

14.2.2.3.2.27.1 VTM_CFG2_TMPSENS_TRIM_J Register (Offset = 304h) [reset = 0h]

Temperature Sensor Band-gap trim values register for sensor j. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

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Table 14-7192. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 1304h + formula

Figure 14-3579. VTM_CFG2_TMPSENS_TRIM_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TRIMO					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
RESERVED			TRIMG				
NONE			R/W				
0h			0h				

Table 14-7193. VTM_CFG2_TMPSENS_TRIM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	TRIMO	R/W	0h	Trim offset bits in the temp sensor. Reset value is from e-fuse at POR, efuse_tmpsens[j]_trimo. Reset Source: mod_por_rst_n
7:5	RESERVED	NONE	0h	Reserved
4:0	TRIMG	R/W	0h	Trim gain bits in the temp sensor. Reset value is from e-fuse at POR, efuse_tmpsens[j]_trimg. Reset Source: mod_por_rst_n

14.2.2.3.2.28 ECC_AGGR_REV Register

14.2.2.3.2.28.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-7194. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2000h

Figure 14-3580. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-7195. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.2.2.3.2.29 ECC_AGGR_VECTOR Register

14.2.2.3.2.29.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-7196. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2008h

Figure 14-3581. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7197. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.2.2.3.2.30 ECC_AGGR_STAT Register

14.2.2.3.2.30.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

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Table 14-7198. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 200Ch

Figure 14-3582. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					4h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
4h							

Table 14-7199. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.2.2.3.2.31 ECC_AGGR_RESERVED_SVBUS_J Register

14.2.2.3.2.31.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-7200. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2010h + formula

Figure 14-3583. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-7201. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.2.2.3.2.32 ECC_AGGR_SEC_EOI_REG Register

14.2.2.3.2.32.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-7202. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 203Ch

Figure 14-3584. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7203. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.2.2.3.2.33 ECC_AGGR_SEC_STATUS_REG0 Register

14.2.2.3.2.33.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7204. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2040h

Figure 14-3585. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	ECCAGG_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7205. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend

14.2.2.3.2.34 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.2.2.3.2.34.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7206. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2080h

Figure 14-3586. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	ECCAGG_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7207. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend

14.2.2.3.2.35 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.2.2.3.2.35.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7208. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 20C0h

Figure 14-3587. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-7209. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend

14.2.2.3.2.36 ECC_AGGR_DED_EOI_REG Register

14.2.2.3.2.36.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-7210. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 213Ch

Figure 14-3588. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7211. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.2.2.3.2.37 ECC_AGGR_DED_STATUS_REG0 Register

14.2.2.3.2.37.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7212. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2140h

Figure 14-3589. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	ECCAGG_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7213. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend

14.2.2.3.2.38 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.2.2.3.2.38.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7214. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2180h

Figure 14-3590. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET</td><td>K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET</td><td>K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET</td><td>ECCAGG_ENABLE_SET</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7215. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend

14.2.2.3.2.39 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.2.2.3.2.39.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7216. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 21C0h

Figure 14-3591. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-7217. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend

14.2.2.3.2.40 ECC_AGGR_AGGR_ENABLE_SET Register

14.2.2.3.2.40.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-7218. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2200h

Figure 14-3592. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-7219. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.2.2.3.2.41 ECC_AGGR_AGGR_ENABLE_CLR Register

14.2.2.3.2.41.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-7220. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2204h

Figure 14-3593. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-7221. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.2.2.3.2.42 ECC_AGGR_AGGR_STATUS_SET Register

14.2.2.3.2.42.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-7222. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 2208h

Figure 14-3594. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-7223. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.2.2.3.2.43 ECC_AGGR_AGGR_STATUS_CLR Register

14.2.2.3.2.43.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-7224. Instance Table

Instance Name	Physical Address
WKUP_VTM0	00B0 220Ch

Figure 14-3595. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-7225. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.2.3 Clocking Registers

14.2.3.1 PLL

PLL

14.2.3.1.1 PLL Summaries

PLL Summaries

Table 14-7226. MAIN_PLL_MMR_CFG Registers, Base Address=0068 0000h, Length=65536

Offset	Length	Register Name	PLL0 Physical Address
0h	32	MAIN_PLL_MMRCFG_PLL0_PID	0068 0000h
8h	32	MAIN_PLL_MMRCFG_PLL0_CFG	0068 0008h
10h	32	MAIN_PLL_MMRCFG_PLL0_LOCKKEY0	0068 0010h
14h	32	MAIN_PLL_MMRCFG_PLL0_LOCKKEY1	0068 0014h
20h	32	MAIN_PLL_MMRCFG_PLL0_CTRL	0068 0020h
24h	32	MAIN_PLL_MMRCFG_PLL0_STAT	0068 0024h
30h	32	MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL0	0068 0030h
34h	32	MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL1	0068 0034h
38h	32	MAIN_PLL_MMRCFG_PLL0_DIV_CTRL	0068 0038h
40h	32	MAIN_PLL_MMRCFG_PLL0_SS_CTRL	0068 0040h
44h	32	MAIN_PLL_MMRCFG_PLL0_SS_SPREAD	0068 0044h
60h	32	MAIN_PLL_MMRCFG_PLL0_CAL_CTRL	0068 0060h
64h	32	MAIN_PLL_MMRCFG_PLL0_CAL_STAT	0068 0064h
80h	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL0	0068 0080h
84h	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL1	0068 0084h
88h	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL2	0068 0088h
8Ch	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL3	0068 008Ch
90h	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL4	0068 0090h
94h	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL5	0068 0094h
98h	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL6	0068 0098h
9Ch	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL7	0068 009Ch
A0h	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL8	0068 00A0h
A4h	32	MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL9	0068 00A4h
1000h	32	MAIN_PLL_MMRCFG_PLL1_PID	0068 1000h
1008h	32	MAIN_PLL_MMRCFG_PLL1_CFG	0068 1008h
1010h	32	MAIN_PLL_MMRCFG_PLL1_LOCKKEY0	0068 1010h
1014h	32	MAIN_PLL_MMRCFG_PLL1_LOCKKEY1	0068 1014h
1020h	32	MAIN_PLL_MMRCFG_PLL1_CTRL	0068 1020h
1024h	32	MAIN_PLL_MMRCFG_PLL1_STAT	0068 1024h
1030h	32	MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL0	0068 1030h
1034h	32	MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL1	0068 1034h
1038h	32	MAIN_PLL_MMRCFG_PLL1_DIV_CTRL	0068 1038h
1040h	32	MAIN_PLL_MMRCFG_PLL1_SS_CTRL	0068 1040h
1044h	32	MAIN_PLL_MMRCFG_PLL1_SS_SPREAD	0068 1044h
1060h	32	MAIN_PLL_MMRCFG_PLL1_CAL_CTRL	0068 1060h
1064h	32	MAIN_PLL_MMRCFG_PLL1_CAL_STAT	0068 1064h
1080h	32	MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL0	0068 1080h
1084h	32	MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL1	0068 1084h
1088h	32	MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL2	0068 1088h
108Ch	32	MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL3	0068 108Ch

Table 14-7226. MAIN_PLL_MMR_CFG Registers, Base Address=0068 0000h, Length=65536 (continued)

Offset	Length	Register Name	PLL0 Physical Address
1090h	32	MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL4	0068 1090h
1094h	32	MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL5	0068 1094h
1098h	32	MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL6	0068 1098h
2000h	32	MAIN_PLL_MMRCFG_PLL2_PID	0068 2000h
2008h	32	MAIN_PLL_MMRCFG_PLL2_CFG	0068 2008h
2010h	32	MAIN_PLL_MMRCFG_PLL2_LOCKKEY0	0068 2010h
2014h	32	MAIN_PLL_MMRCFG_PLL2_LOCKKEY1	0068 2014h
2020h	32	MAIN_PLL_MMRCFG_PLL2_CTRL	0068 2020h
2024h	32	MAIN_PLL_MMRCFG_PLL2_STAT	0068 2024h
2030h	32	MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL0	0068 2030h
2034h	32	MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL1	0068 2034h
2038h	32	MAIN_PLL_MMRCFG_PLL2_DIV_CTRL	0068 2038h
2040h	32	MAIN_PLL_MMRCFG_PLL2_SS_CTRL	0068 2040h
2044h	32	MAIN_PLL_MMRCFG_PLL2_SS_SPREAD	0068 2044h
2060h	32	MAIN_PLL_MMRCFG_PLL2_CAL_CTRL	0068 2060h
2064h	32	MAIN_PLL_MMRCFG_PLL2_CAL_STAT	0068 2064h
2080h	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL0	0068 2080h
2084h	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL1	0068 2084h
2088h	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL2	0068 2088h
208Ch	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL3	0068 208Ch
2090h	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL4	0068 2090h
2094h	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL5	0068 2094h
2098h	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL6	0068 2098h
209Ch	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL7	0068 209Ch
20A0h	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL8	0068 20A0h
20A4h	32	MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL9	0068 20A4h
4000h	32	MAIN_PLL_MMRCFG_PLL4_PID	0068 4000h
4008h	32	MAIN_PLL_MMRCFG_PLL4_CFG	0068 4008h
4010h	32	MAIN_PLL_MMRCFG_PLL4_LOCKKEY0	0068 4010h
4014h	32	MAIN_PLL_MMRCFG_PLL4_LOCKKEY1	0068 4014h
4020h	32	MAIN_PLL_MMRCFG_PLL4_CTRL	0068 4020h
4024h	32	MAIN_PLL_MMRCFG_PLL4_STAT	0068 4024h
4030h	32	MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL0	0068 4030h
4034h	32	MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL1	0068 4034h
4038h	32	MAIN_PLL_MMRCFG_PLL4_DIV_CTRL	0068 4038h
4040h	32	MAIN_PLL_MMRCFG_PLL4_SS_CTRL	0068 4040h
4044h	32	MAIN_PLL_MMRCFG_PLL4_SS_SPREAD	0068 4044h
4060h	32	MAIN_PLL_MMRCFG_PLL4_CAL_CTRL	0068 4060h
4064h	32	MAIN_PLL_MMRCFG_PLL4_CAL_STAT	0068 4064h
4080h	32	MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL0	0068 4080h
4084h	32	MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL1	0068 4084h
4088h	32	MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL2	0068 4088h
408Ch	32	MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL3	0068 408Ch
7000h	32	MAIN_PLL_MMRCFG_PLL7_PID	0068 7000h
7008h	32	MAIN_PLL_MMRCFG_PLL7_CFG	0068 7008h
7010h	32	MAIN_PLL_MMRCFG_PLL7_LOCKKEY0	0068 7010h
7014h	32	MAIN_PLL_MMRCFG_PLL7_LOCKKEY1	0068 7014h

Table 14-7226. MAIN_PLL_MMR_CFG Registers, Base Address=0068 0000h, Length=65536 (continued)

Offset	Length	Register Name	PLL0 Physical Address
7020h	32	MAIN_PLL_MMRCFG_PLL7_CTRL	0068 7020h
7024h	32	MAIN_PLL_MMRCFG_PLL7_STAT	0068 7024h
7030h	32	MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL0	0068 7030h
7034h	32	MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL1	0068 7034h
7038h	32	MAIN_PLL_MMRCFG_PLL7_DIV_CTRL	0068 7038h
7040h	32	MAIN_PLL_MMRCFG_PLL7_SS_CTRL	0068 7040h
7044h	32	MAIN_PLL_MMRCFG_PLL7_SS_SPREAD	0068 7044h
7060h	32	MAIN_PLL_MMRCFG_PLL7_CAL_CTRL	0068 7060h
7064h	32	MAIN_PLL_MMRCFG_PLL7_CAL_STAT	0068 7064h
7080h	32	MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL0	0068 7080h
7084h	32	MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL1	0068 7084h
E000h	32	MAIN_PLL_MMRCFG_PLL14_PID	0068 E000h
E008h	32	MAIN_PLL_MMRCFG_PLL14_CFG	0068 E008h
E010h	32	MAIN_PLL_MMRCFG_PLL14_LOCKKEY0	0068 E010h
E014h	32	MAIN_PLL_MMRCFG_PLL14_LOCKKEY1	0068 E014h
E020h	32	MAIN_PLL_MMRCFG_PLL14_CTRL	0068 E020h
E024h	32	MAIN_PLL_MMRCFG_PLL14_STAT	0068 E024h
E030h	32	MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL0	0068 E030h
E034h	32	MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL1	0068 E034h
E038h	32	MAIN_PLL_MMRCFG_PLL14_DIV_CTRL	0068 E038h
E040h	32	MAIN_PLL_MMRCFG_PLL14_SS_CTRL	0068 E040h
E044h	32	MAIN_PLL_MMRCFG_PLL14_SS_SPREAD	0068 E044h
E060h	32	MAIN_PLL_MMRCFG_PLL14_CAL_CTRL	0068 E060h
E064h	32	MAIN_PLL_MMRCFG_PLL14_CAL_STAT	0068 E064h
E080h	32	MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL0	0068 E080h
E084h	32	MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL1	0068 E084h
F000h	32	MAIN_PLL_MMRCFG_PLL15_PID	0068 F000h
F008h	32	MAIN_PLL_MMRCFG_PLL15_CFG	0068 F008h
F010h	32	MAIN_PLL_MMRCFG_PLL15_LOCKKEY0	0068 F010h
F014h	32	MAIN_PLL_MMRCFG_PLL15_LOCKKEY1	0068 F014h
F020h	32	MAIN_PLL_MMRCFG_PLL15_CTRL	0068 F020h
F024h	32	MAIN_PLL_MMRCFG_PLL15_STAT	0068 F024h
F030h	32	MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL0	0068 F030h
F034h	32	MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL1	0068 F034h
F038h	32	MAIN_PLL_MMRCFG_PLL15_DIV_CTRL	0068 F038h
F040h	32	MAIN_PLL_MMRCFG_PLL15_SS_CTRL	0068 F040h
F044h	32	MAIN_PLL_MMRCFG_PLL15_SS_SPREAD	0068 F044h
F060h	32	MAIN_PLL_MMRCFG_PLL15_CAL_CTRL	0068 F060h
F064h	32	MAIN_PLL_MMRCFG_PLL15_CAL_STAT	0068 F064h
F080h	32	MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL0	0068 F080h
F084h	32	MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL1	0068 F084h
F088h	32	MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL2	0068 F088h
F08Ch	32	MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL3	0068 F08Ch

14.2.3.1.2 PLL Registers

PLL Registers

14.2.3.1.2.1 MAIN_PLL_MMRCFG_PLL0_PID Register

14.2.3.1.2.1.1 MAIN_PLL_MMRCFG_PLL0_PID Register (Offset = 0h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-7227. Instance Table

Instance Name	Physical Address
PLL0	0068 0000h

Figure 14-3596. MAIN_PLL_MMRCFG_PLL0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">MISC</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">2h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-7228. MAIN_PLL_MMRCFG_PLL0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.2.2 MAIN_PLL_MMRCFG_PLL0_CFG Register

14.2.3.1.2.2.1 MAIN_PLL_MMRCFG_PLL0_CFG Register (Offset = 8h) [reset = 3FF0801h]

pll MMR Configuration

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Table 14-7229. Instance Table

Instance Name	Physical Address
PLL0	0068 0008h

Figure 14-3597. MAIN_PLL_MMRCFG_PLL0_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-7230. MAIN_PLL_MMRCFG_PLL0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.2.3 MAIN_PLL_MMRCFG_PLL0_LOCKKEY0 Register

14.2.3.1.2.3.1 MAIN_PLL_MMRCFG_PLL0_LOCKKEY0 Register (Offset = 10h) [reset = 0h]

PLL0_LOCKKEY0 - PLL0 Lock Key 0 Register

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Table 14-7231. Instance Table

Instance Name	Physical Address
PLL0	0068 0010h

Figure 14-3598. MAIN_PLL_MMRCFG_PLL0_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7232. MAIN_PLL_MMRCFG_PLL0_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.2.4 MAIN_PLL_MMRCFG_PLL0_LOCKKEY1 Register

14.2.3.1.2.4.1 MAIN_PLL_MMRCFG_PLL0_LOCKKEY1 Register (Offset = 14h) [reset = 0h]

PLL0_LOCKKEY1 - PLL0 Lock Key 1 RegisterAddr

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Table 14-7233. Instance Table

Instance Name	Physical Address
PLL0	0068 0014h

Figure 14-3599. MAIN_PLL_MMRCFG_PLL0_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7234. MAIN_PLL_MMRCFG_PLL0_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n

14.2.3.1.2.5 MAIN_PLL_MMRCFG_PLL0_CTRL Register

14.2.3.1.2.5.1 MAIN_PLL_MMRCFG_PLL0_CTRL Register (Offset = 20h) [reset = 80010011h]

PLL0_CTRL - PLL0 Control

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Table 14-7235. Instance Table

Instance Name	Physical Address
PLL0	0068 0020h

Figure 14-3600. MAIN_PLL_MMRCFG_PLL0_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7236. MAIN_PLL_MMRCFG_PLL0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-7236. MAIN_PLL_MMRCFG_PLL0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.6 MAIN_PLL_MMRCFG_PLL0_STAT Register

14.2.3.1.2.6.1 MAIN_PLL_MMRCFG_PLL0_STAT Register (Offset = 24h) [reset = 0h]

PLL0_STAT - PLL0 Status

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Table 14-7237. Instance Table

Instance Name	Physical Address
PLL0	0068 0024h

Figure 14-3601. MAIN_PLL_MMRCFG_PLL0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7238. MAIN_PLL_MMRCFG_PLL0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.2.7 MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL0 Register

14.2.3.1.2.7.1 MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL0 Register (Offset = 30h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL0 Frequency Control 0 Register

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Table 14-7239. Instance Table

Instance Name	Physical Address
PLL0	0068 0030h

Figure 14-3602. MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7240. MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.2.8 MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL1 Register

14.2.3.1.2.8.1 MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL1 Register (Offset = 34h) [reset = 0h]

PLL0_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-7241. Instance Table

Instance Name	Physical Address
PLL0	0068 0034h

Figure 14-3603. MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7242. MAIN_PLL_MMRCFG_PLL0_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.9 MAIN_PLL_MMRCFG_PLL0_DIV_CTRL Register

14.2.3.1.2.9.1 MAIN_PLL_MMRCFG_PLL0_DIV_CTRL Register (Offset = 38h) [reset = 1020001h]

PLL0_DIV_CTRL - PLL0 Output Clock Divider Register

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Table 14-7243. Instance Table

Instance Name	Physical Address
PLL0	0068 0038h

Figure 14-3604. MAIN_PLL_MMRCFG_PLL0_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7244. MAIN_PLL_MMRCFG_PLL0_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.10 MAIN_PLL_MMRCFG_PLL0_SS_CTRL Register

14.2.3.1.2.10.1 MAIN_PLL_MMRCFG_PLL0_SS_CTRL Register (Offset = 40h) [reset = 80000000h]

PLL_SS_CTRL register for pll0

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Table 14-7245. Instance Table

Instance Name	Physical Address
PLL0	0068 0040h

Figure 14-3605. MAIN_PLL_MMRCFG_PLL0_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7246. MAIN_PLL_MMRCFG_PLL0_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7246. MAIN_PLL_MMRCFG_PLL0_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.2.11 MAIN_PLL_MMRCFG_PLL0_SS_SPREAD Register

14.2.3.1.2.11.1 MAIN_PLL_MMRCFG_PLL0_SS_SPREAD Register (Offset = 44h) [reset = 10001h]

PLL_SS_SPREAD register for pll0

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Table 14-7247. Instance Table

Instance Name	Physical Address
PLL0	0068 0044h

Figure 14-3606. MAIN_PLL_MMRCFG_PLL0_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7248. MAIN_PLL_MMRCFG_PLL0_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.2.12 MAIN_PLL_MMRCFG_PLL0_CAL_CTRL Register

14.2.3.1.2.12.1 MAIN_PLL_MMRCFG_PLL0_CAL_CTRL Register (Offset = 60h) [reset = 20000h]

PLL0_CAL_CTRL - PLL0 Calibration Control Register

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Table 14-7249. Instance Table

Instance Name	Physical Address
PLL0	0068 0060h

Figure 14-3607. MAIN_PLL_MMRCFG_PLL0_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7250. MAIN_PLL_MMRCFG_PLL0_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7250. MAIN_PLL_MMRCFG_PLL0_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.2.13 MAIN_PLL_MMRCFG_PLL0_CAL_STAT Register

14.2.3.1.2.13.1 MAIN_PLL_MMRCFG_PLL0_CAL_STAT Register (Offset = 64h) [reset = 0h]

PLL0_CAL_STAT - PLL0 Calibration Status Register

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Table 14-7251. Instance Table

Instance Name	Physical Address
PLL0	0068 0064h

Figure 14-3608. MAIN_PLL_MMRCFG_PLL0_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7252. MAIN_PLL_MMRCFG_PLL0_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.2.14 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL0 Register

14.2.3.1.2.14.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL0 Register (Offset = 80h) [reset = 0h]

HSDIV_CTRL0 register for pll0

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Table 14-7253. Instance Table

Instance Name	Physical Address
PLL0	0068 0080h

Figure 14-3609. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7254. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.15 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL1 Register

14.2.3.1.2.15.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL1 Register (Offset = 84h) [reset = 0h]

HSDIV_CTRL1 register for pll0

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Table 14-7255. Instance Table

Instance Name	Physical Address
PLL0	0068 0084h

Figure 14-3610. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7256. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.16 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL2 Register

14.2.3.1.2.16.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL2 Register (Offset = 88h) [reset = 0h]

HSDIV_CTRL2 register for pll0

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Table 14-7257. Instance Table

Instance Name	Physical Address
PLL0	0068 0088h

Figure 14-3611. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7258. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.17 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL3 Register

14.2.3.1.2.17.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL3 Register (Offset = 8Ch) [reset = 0h]

HSDIV_CTRL3 register for pll0

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Table 14-7259. Instance Table

Instance Name	Physical Address
PLL0	0068 008Ch

Figure 14-3612. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7260. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.18 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL4 Register

14.2.3.1.2.18.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL4 Register (Offset = 90h) [reset = 0h]

HSDIV_CTRL4 register for pll0

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Table 14-7261. Instance Table

Instance Name	Physical Address
PLL0	0068 0090h

Figure 14-3613. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7262. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.19 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL5 Register

14.2.3.1.2.19.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL5 Register (Offset = 94h) [reset = 0h]

HSDIV_CTRL5 register for pll0

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Table 14-7263. Instance Table

Instance Name	Physical Address
PLL0	0068 0094h

Figure 14-3614. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7264. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.20 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL6 Register

14.2.3.1.2.20.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL6 Register (Offset = 98h) [reset = 0h]

HSDIV_CTRL6 register for pll0

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Table 14-7265. Instance Table

Instance Name	Physical Address
PLL0	0068 0098h

Figure 14-3615. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7266. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.21 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL7 Register

14.2.3.1.2.21.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL7 Register (Offset = 9Ch) [reset = 0h]

HSDIV_CTRL7 register for pll0

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Table 14-7267. Instance Table

Instance Name	Physical Address
PLL0	0068 009Ch

Figure 14-3616. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL7 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7268. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.22 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL8 Register

14.2.3.1.2.22.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL8 Register (Offset = A0h) [reset = 0h]

HSDIV_CTRL8 register for pll0

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Table 14-7269. Instance Table

Instance Name	Physical Address
PLL0	0068 00A0h

Figure 14-3617. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-7270. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.23 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL9 Register

14.2.3.1.2.23.1 MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL9 Register (Offset = A4h) [reset = 0h]

HSDIV_CTRL9 register for pll0

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Table 14-7271. Instance Table

Instance Name	**Physical Address**
PLL0	0068 00A4h

Figure 14-3618. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL9 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7272. MAIN_PLL_MMRCFG_PLL0_HSDIV_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.24 MAIN_PLL_MMRCFG_PLL1_PID Register

14.2.3.1.2.24.1 MAIN_PLL_MMRCFG_PLL1_PID Register (Offset = 1000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-7273. Instance Table

Instance Name	Physical Address
PLL0	0068 1000h

Figure 14-3619. MAIN_PLL_MMRCFG_PLL1_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7274. MAIN_PLL_MMRCFG_PLL1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.2.25 MAIN_PLL_MMRCFG_PLL1_CFG Register

14.2.3.1.2.25.1 MAIN_PLL_MMRCFG_PLL1_CFG Register (Offset = 1008h) [reset = 7F0801h]

pll MMR Configuration

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Table 14-7275. Instance Table

Instance Name	Physical Address
PLL0	0068 1008h

Figure 14-3620. MAIN_PLL_MMRCFG_PLL1_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
7Fh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HSDIV_PRSNT							
R							
7Fh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-7276. MAIN_PLL_MMRCFG_PLL1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	7Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.2.26 MAIN_PLL_MMRCFG_PLL1_LOCKKEY0 Register

14.2.3.1.2.26.1 MAIN_PLL_MMRCFG_PLL1_LOCKKEY0 Register (Offset = 1010h) [reset = 0h]

PLL1_LOCKKEY0 - PLL1 Lock Key 0 Register

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Table 14-7277. Instance Table

Instance Name	Physical Address
PLL0	0068 1010h

Figure 14-3621. MAIN_PLL_MMRCFG_PLL1_LOCKKEY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">KEY</td><td>UNLOCKED</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7278. MAIN_PLL_MMRCFG_PLL1_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.2.27 MAIN_PLL_MMRCFG_PLL1_LOCKKEY1 Register

14.2.3.1.2.27.1 MAIN_PLL_MMRCFG_PLL1_LOCKKEY1 Register (Offset = 1014h) [reset = 0h]

PLL1_LOCKKEY1 - PLL1 Lock Key 1 RegisterAddr

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Table 14-7279. Instance Table

Instance Name	Physical Address
PLL0	0068 1014h

Figure 14-3622. MAIN_PLL_MMRCFG_PLL1_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7280. MAIN_PLL_MMRCFG_PLL1_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers Reset Source: srst_n

14.2.3.1.2.28 MAIN_PLL_MMRCFG_PLL1_CTRL Register

14.2.3.1.2.28.1 MAIN_PLL_MMRCFG_PLL1_CTRL Register (Offset = 1020h) [reset = 80010011h]

PLL1_CTRL - PLL1 Control

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Table 14-7281. Instance Table

Instance Name	Physical Address
PLL0	0068 1020h

Figure 14-3623. MAIN_PLL_MMRCFG_PLL1_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						

23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h

15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7282. MAIN_PLL_MMRCFG_PLL1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-7282. MAIN_PLL_MMRCFG_PLL1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.29 MAIN_PLL_MMRCFG_PLL1_STAT Register

14.2.3.1.2.29.1 MAIN_PLL_MMRCFG_PLL1_STAT Register (Offset = 1024h) [reset = 0h]

PLL1_STAT - PLL1 Status

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Table 14-7283. Instance Table

Instance Name	Physical Address
PLL0	0068 1024h

Figure 14-3624. MAIN_PLL_MMRCFG_PLL1_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7284. MAIN_PLL_MMRCFG_PLL1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.2.30 MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL0 Register

14.2.3.1.2.30.1 MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL0 Register (Offset = 1030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL1 Frequency Control 1 Register

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Table 14-7285. Instance Table

Instance Name	Physical Address
PLL0	0068 1030h

Figure 14-3625. MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7286. MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.2.31 MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL1 Register

14.2.3.1.2.31.1 MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL1 Register (Offset = 1034h) [reset = 0h]

PLL1_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-7287. Instance Table

Instance Name	Physical Address
PLL0	0068 1034h

Figure 14-3626. MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7288. MAIN_PLL_MMRCFG_PLL1_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.32 MAIN_PLL_MMRCFG_PLL1_DIV_CTRL Register

14.2.3.1.2.32.1 MAIN_PLL_MMRCFG_PLL1_DIV_CTRL Register (Offset = 1038h) [reset = 1020001h]

PLL1_DIV_CTRL - PLL1 Output Clock Divider Register

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Table 14-7289. Instance Table

Instance Name	Physical Address
PLL0	0068 1038h

Figure 14-3627. MAIN_PLL_MMRCFG_PLL1_DIV_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">POST_DIV2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">POST_DIV1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">REF_DIV</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-7290. MAIN_PLL_MMRCFG_PLL1_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.33 MAIN_PLL_MMRCFG_PLL1_SS_CTRL Register

14.2.3.1.2.33.1 MAIN_PLL_MMRCFG_PLL1_SS_CTRL Register (Offset = 1040h) [reset = 80000000h]

PLL_SS_CTRL register for pll1

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Table 14-7291. Instance Table

Instance Name	Physical Address
PLL0	0068 1040h

Figure 14-3628. MAIN_PLL_MMRCFG_PLL1_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7292. MAIN_PLL_MMRCFG_PLL1_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7292. MAIN_PLL_MMRCFG_PLL1_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.2.34 MAIN_PLL_MMRCFG_PLL1_SS_SPREAD Register

14.2.3.1.2.34.1 MAIN_PLL_MMRCFG_PLL1_SS_SPREAD Register (Offset = 1044h) [reset = 10001h]

PLL_SS_SPREAD register for pll1

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Table 14-7293. Instance Table

Instance Name	Physical Address
PLL0	0068 1044h

Figure 14-3629. MAIN_PLL_MMRCFG_PLL1_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7294. MAIN_PLL_MMRCFG_PLL1_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.2.35 MAIN_PLL_MMRCFG_PLL1_CAL_CTRL Register

14.2.3.1.2.35.1 MAIN_PLL_MMRCFG_PLL1_CAL_CTRL Register (Offset = 1060h) [reset = 20000h]

PLL1_CAL_CTRL - PLL1 Calibration Control Register

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Table 14-7295. Instance Table

Instance Name	Physical Address
PLL0	0068 1060h

Figure 14-3630. MAIN_PLL_MMRCFG_PLL1_CAL_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>FAST_CAL</td><td>RESERVED</td><td colspan="3">CAL_CNT</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CAL_BYP</td><td colspan="3">RESERVED</td><td colspan="4">CAL_IN</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_IN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7296. MAIN_PLL_MMRCFG_PLL1_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7296. MAIN_PLL_MMRCFG_PLL1_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.2.36 MAIN_PLL_MMRCFG_PLL1_CAL_STAT Register

14.2.3.1.2.36.1 MAIN_PLL_MMRCFG_PLL1_CAL_STAT Register (Offset = 1064h) [reset = 0h]

PLL1_CAL_STAT - PLL1 Calibration Status Register

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Table 14-7297. Instance Table

Instance Name	Physical Address
PLL0	0068 1064h

Figure 14-3631. MAIN_PLL_MMRCFG_PLL1_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7298. MAIN_PLL_MMRCFG_PLL1_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.2.37 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL0 Register

14.2.3.1.2.37.1 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL0 Register (Offset = 1080h) [reset = 0h]

HSDIV_CTRL0 register for pll1

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Table 14-7299. Instance Table

Instance Name	Physical Address
PLL0	0068 1080h

Figure 14-3632. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7300. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.38 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL1 Register

14.2.3.1.2.38.1 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL1 Register (Offset = 1084h) [reset = 0h]

HSDIV_CTRL1 register for pll1

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Table 14-7301. Instance Table

Instance Name	Physical Address
PLL0	0068 1084h

Figure 14-3633. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7302. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.39 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL2 Register

14.2.3.1.2.39.1 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL2 Register (Offset = 1088h) [reset = 0h]

HSDIV_CTRL2 register for pll1

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Table 14-7303. Instance Table

Instance Name	Physical Address
PLL0	0068 1088h

Figure 14-3634. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7304. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.40 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL3 Register

14.2.3.1.2.40.1 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL3 Register (Offset = 108Ch) [reset = 0h]

HSDIV_CTRL3 register for pll1

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Table 14-7305. Instance Table

Instance Name	Physical Address
PLL0	0068 108Ch

Figure 14-3635. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7306. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.41 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL4 Register

14.2.3.1.2.41.1 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL4 Register (Offset = 1090h) [reset = 0h]

HSDIV_CTRL4 register for pll1

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Table 14-7307. Instance Table

Instance Name	Physical Address
PLL0	0068 1090h

Figure 14-3636. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7308. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.42 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL5 Register

14.2.3.1.2.42.1 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL5 Register (Offset = 1094h) [reset = 0h]

HSDIV_CTRL5 register for pll1

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Table 14-7309. Instance Table

Instance Name	Physical Address
PLL0	0068 1094h

Figure 14-3637. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7310. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.43 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL6 Register

14.2.3.1.2.43.1 MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL6 Register (Offset = 1098h) [reset = 0h]

HSDIV_CTRL6 register for pll1

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Table 14-7311. Instance Table

Instance Name	Physical Address
PLL0	0068 1098h

Figure 14-3638. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-7312. MAIN_PLL_MMRCFG_PLL1_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.44 MAIN_PLL_MMRCFG_PLL2_PID Register

14.2.3.1.2.44.1 MAIN_PLL_MMRCFG_PLL2_PID Register (Offset = 2000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-7313. Instance Table

Instance Name	Physical Address
PLL0	0068 2000h

Figure 14-3639. MAIN_PLL_MMRCFG_PLL2_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7314. MAIN_PLL_MMRCFG_PLL2_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.2.45 MAIN_PLL_MMRCFG_PLL2_CFG Register

14.2.3.1.2.45.1 MAIN_PLL_MMRCFG_PLL2_CFG Register (Offset = 2008h) [reset = 3FF0801h]

pll MMR Configuration

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Table 14-7315. Instance Table

Instance Name	Physical Address
PLL0	0068 2008h

Figure 14-3640. MAIN_PLL_MMRCFG_PLL2_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-7316. MAIN_PLL_MMRCFG_PLL2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.2.46 MAIN_PLL_MMRCFG_PLL2_LOCKKEY0 Register

14.2.3.1.2.46.1 MAIN_PLL_MMRCFG_PLL2_LOCKKEY0 Register (Offset = 2010h) [reset = 0h]

PLL2_LOCKKEY0 - PLL2 Lock Key 0 Register

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Table 14-7317. Instance Table

Instance Name	Physical Address
PLL0	0068 2010h

Figure 14-3641. MAIN_PLL_MMRCFG_PLL2_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7318. MAIN_PLL_MMRCFG_PLL2_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.2.47 MAIN_PLL_MMRCFG_PLL2_LOCKKEY1 Register

14.2.3.1.2.47.1 MAIN_PLL_MMRCFG_PLL2_LOCKKEY1 Register (Offset = 2014h) [reset = 0h]

PLL2_LOCKKEY1 - PLL2 Lock Key 1 RegisterAddr

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Table 14-7319. Instance Table

Instance Name	Physical Address
PLL0	0068 2014h

Figure 14-3642. MAIN_PLL_MMRCFG_PLL2_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7320. MAIN_PLL_MMRCFG_PLL2_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers Reset Source: srst_n

14.2.3.1.2.48 MAIN_PLL_MMRCFG_PLL2_CTRL Register

14.2.3.1.2.48.1 MAIN_PLL_MMRCFG_PLL2_CTRL Register (Offset = 2020h) [reset = 80010011h]

PLL2_CTRL - PLL2 Control

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Table 14-7321. Instance Table

Instance Name	Physical Address
PLL0	0068 2020h

Figure 14-3643. MAIN_PLL_MMRCFG_PLL2_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7322. MAIN_PLL_MMRCFG_PLL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-7322. MAIN_PLL_MMRCFG_PLL2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.49 MAIN_PLL_MMRCFG_PLL2_STAT Register

14.2.3.1.2.49.1 MAIN_PLL_MMRCFG_PLL2_STAT Register (Offset = 2024h) [reset = 0h]

PLL2_STAT - PLL2 Status

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Table 14-7323. Instance Table

Instance Name	Physical Address
PLL0	0068 2024h

Figure 14-3644. MAIN_PLL_MMRCFG_PLL2_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7324. MAIN_PLL_MMRCFG_PLL2_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.2.50 MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL0 Register

14.2.3.1.2.50.1 MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL0 Register (Offset = 2030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL2 Frequency Control 2 Register

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Table 14-7325. Instance Table

Instance Name	Physical Address
PLL0	0068 2030h

Figure 14-3645. MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FB_DIV_INT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_INT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-7326. MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.2.51 MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL1 Register

14.2.3.1.2.51.1 MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL1 Register (Offset = 2034h) [reset = 0h]

PLL2_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-7327. Instance Table

Instance Name	Physical Address
PLL0	0068 2034h

Figure 14-3646. MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FB_DIV_FRAC							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FB_DIV_FRAC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FB_DIV_FRAC							
R/W							
0h							

Table 14-7328. MAIN_PLL_MMRCFG_PLL2_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.52 MAIN_PLL_MMRCFG_PLL2_DIV_CTRL Register

14.2.3.1.2.52.1 MAIN_PLL_MMRCFG_PLL2_DIV_CTRL Register (Offset = 2038h) [reset = 1020001h]

PLL2_DIV_CTRL - PLL2 Output Clock Divider Register

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Table 14-7329. Instance Table

Instance Name	Physical Address
PLL0	0068 2038h

Figure 14-3647. MAIN_PLL_MMRCFG_PLL2_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7330. MAIN_PLL_MMRCFG_PLL2_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.53 MAIN_PLL_MMRCFG_PLL2_SS_CTRL Register

14.2.3.1.2.53.1 MAIN_PLL_MMRCFG_PLL2_SS_CTRL Register (Offset = 2040h) [reset = 80000000h]

PLL_SS_CTRL register for pll2

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Table 14-7331. Instance Table

Instance Name	Physical Address
PLL0	0068 2040h

Figure 14-3648. MAIN_PLL_MMRCFG_PLL2_SS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="5">RESERVED</td><td colspan="2">WV_TBLE_MAXADDR</td></tr>
<tr><td>R/W</td><td colspan="5">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>1h</td><td colspan="5">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WV_TBLE_MAXADDR</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">NONE</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>DOWNSPREAD_EN</td><td colspan="3">RESERVED</td><td>WAVE_SEL</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-7332. MAIN_PLL_MMRCFG_PLL2_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7332. MAIN_PLL_MMRCFG_PLL2_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.2.54 MAIN_PLL_MMRCFG_PLL2_SS_SPREAD Register

14.2.3.1.2.54.1 MAIN_PLL_MMRCFG_PLL2_SS_SPREAD Register (Offset = 2044h) [reset = 10001h]

PLL_SS_SPREAD register for pll2

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Table 14-7333. Instance Table

Instance Name	Physical Address
PLL0	0068 2044h

Figure 14-3649. MAIN_PLL_MMRCFG_PLL2_SS_SPREAD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MOD_DIV</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">SPREAD</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1h</td></tr>
</table>

Table 14-7334. MAIN_PLL_MMRCFG_PLL2_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.2.55 MAIN_PLL_MMRCFG_PLL2_CAL_CTRL Register

14.2.3.1.2.55.1 MAIN_PLL_MMRCFG_PLL2_CAL_CTRL Register (Offset = 2060h) [reset = 20000h]

PLL2_CAL_CTRL - PLL2 Calibration Control Register

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Table 14-7335. Instance Table

Instance Name	Physical Address
PLL0	0068 2060h

Figure 14-3650. MAIN_PLL_MMRCFG_PLL2_CAL_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>FAST_CAL</td><td>RESERVED</td><td colspan="3">CAL_CNT</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CAL_BYP</td><td colspan="3">RESERVED</td><td colspan="4">CAL_IN</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_IN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7336. MAIN_PLL_MMRCFG_PLL2_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7336. MAIN_PLL_MMRCFG_PLL2_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.2.56 MAIN_PLL_MMRCFG_PLL2_CAL_STAT Register

14.2.3.1.2.56.1 MAIN_PLL_MMRCFG_PLL2_CAL_STAT Register (Offset = 2064h) [reset = 0h]

PLL2_CAL_STAT - PLL2 Calibration Status Register

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Table 14-7337. Instance Table

Instance Name	Physical Address
PLL0	0068 2064h

Figure 14-3651. MAIN_PLL_MMRCFG_PLL2_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7338. MAIN_PLL_MMRCFG_PLL2_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.2.57 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL0 Register

14.2.3.1.2.57.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL0 Register (Offset = 2080h) [reset = 0h]

HSDIV_CTRL0 register for pll2

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Table 14-7339. Instance Table

Instance Name	Physical Address
PLL0	0068 2080h

Figure 14-3652. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-7340. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.58 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL1 Register

14.2.3.1.2.58.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL1 Register (Offset = 2084h) [reset = 0h]

HSDIV_CTRL1 register for pll2

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Table 14-7341. Instance Table

Instance Name	Physical Address
PLL0	0068 2084h

Figure 14-3653. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7342. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.59 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL2 Register

14.2.3.1.2.59.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL2 Register (Offset = 2088h) [reset = 0h]

HSDIV_CTRL2 register for pll2

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Table 14-7343. Instance Table

Instance Name	Physical Address
PLL0	0068 2088h

Figure 14-3654. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7344. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.60 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL3 Register

14.2.3.1.2.60.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL3 Register (Offset = 208Ch) [reset = 0h]

HSDIV_CTRL3 register for pll2

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Table 14-7345. Instance Table

Instance Name	Physical Address
PLL0	0068 208Ch

Figure 14-3655. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7346. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.61 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL4 Register

14.2.3.1.2.61.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL4 Register (Offset = 2090h) [reset = 0h]

HSDIV_CTRL4 register for pll2

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Table 14-7347. Instance Table

Instance Name	Physical Address
PLL0	0068 2090h

Figure 14-3656. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7348. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.62 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL5 Register

14.2.3.1.2.62.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL5 Register (Offset = 2094h) [reset = 0h]

HSDIV_CTRL5 register for pll2

Return to Summary Table

Table 14-7349. Instance Table

Instance Name	Physical Address
PLL0	0068 2094h

Figure 14-3657. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7350. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.63 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL6 Register

14.2.3.1.2.63.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL6 Register (Offset = 2098h) [reset = 0h]

HSDIV_CTRL6 register for pll2

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Table 14-7351. Instance Table

Instance Name	Physical Address
PLL0	0068 2098h

Figure 14-3658. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7352. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.64 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL7 Register

14.2.3.1.2.64.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL7 Register (Offset = 209Ch) [reset = 0h]

HSDIV_CTRL7 register for pll2

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Table 14-7353. Instance Table

Instance Name	Physical Address
PLL0	0068 209Ch

Figure 14-3659. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL7 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7354. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.65 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL8 Register

14.2.3.1.2.65.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL8 Register (Offset = 20A0h) [reset = 0h]

HSDIV_CTRL8 register for pll2

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Table 14-7355. Instance Table

Instance Name	Physical Address
PLL0	0068 20A0h

Figure 14-3660. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-7356. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.66 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL9 Register

14.2.3.1.2.66.1 MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL9 Register (Offset = 20A4h) [reset = 0h]

HSDIV_CTRL9 register for pll2

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Table 14-7357. Instance Table

Instance Name	Physical Address
PLL0	0068 20A4h

Figure 14-3661. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL9 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7358. MAIN_PLL_MMRCFG_PLL2_HSDIV_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.67 MAIN_PLL_MMRCFG_PLL4_PID Register

14.2.3.1.2.67.1 MAIN_PLL_MMRCFG_PLL4_PID Register (Offset = 4000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-7359. Instance Table

Instance Name	Physical Address
PLL0	0068 4000h

Figure 14-3662. MAIN_PLL_MMRCFG_PLL4_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			

23	22	21	20	19	18	17	16
MODULE							
R							
180h							

15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		

7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7360. MAIN_PLL_MMRCFG_PLL4_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.2.68 MAIN_PLL_MMRCFG_PLL4_CFG Register

14.2.3.1.2.68.1 MAIN_PLL_MMRCFG_PLL4_CFG Register (Offset = 4008h) [reset = F0801h]

pll MMR Configuration

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Table 14-7361. Instance Table

Instance Name	Physical Address
PLL0	0068 4008h

Figure 14-3663. MAIN_PLL_MMRCFG_PLL4_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-7362. MAIN_PLL_MMRCFG_PLL4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.2.69 MAIN_PLL_MMRCFG_PLL4_LOCKKEY0 Register

14.2.3.1.2.69.1 MAIN_PLL_MMRCFG_PLL4_LOCKKEY0 Register (Offset = 4010h) [reset = 0h]

PLL4_LOCKKEY0 - PLL4 Lock Key 0 Register

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Table 14-7363. Instance Table

Instance Name	Physical Address
PLL0	0068 4010h

Figure 14-3664. MAIN_PLL_MMRCFG_PLL4_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7364. MAIN_PLL_MMRCFG_PLL4_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition4 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.2.70 MAIN_PLL_MMRCFG_PLL4_LOCKKEY1 Register

14.2.3.1.2.70.1 MAIN_PLL_MMRCFG_PLL4_LOCKKEY1 Register (Offset = 4014h) [reset = 0h]

PLL4_LOCKKEY1 - PLL4 Lock Key 1 RegisterAddr

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Table 14-7365. Instance Table

Instance Name	Physical Address
PLL0	0068 4014h

Figure 14-3665. MAIN_PLL_MMRCFG_PLL4_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7366. MAIN_PLL_MMRCFG_PLL4_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition4 registers Reset Source: srst_n

14.2.3.1.2.71 MAIN_PLL_MMRCFG_PLL4_CTRL Register

14.2.3.1.2.71.1 MAIN_PLL_MMRCFG_PLL4_CTRL Register (Offset = 4020h) [reset = 80010011h]

PLL4_CTRL - PLL4 Control

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Table 14-7367. Instance Table

Instance Name	Physical Address
PLL0	0068 4020h

Figure 14-3666. MAIN_PLL_MMRCFG_PLL4_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7368. MAIN_PLL_MMRCFG_PLL4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-7368. MAIN_PLL_MMRCFG_PLL4_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.72 MAIN_PLL_MMRCFG_PLL4_STAT Register

14.2.3.1.2.72.1 MAIN_PLL_MMRCFG_PLL4_STAT Register (Offset = 4024h) [reset = 0h]

PLL4_STAT - PLL4 Status

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Table 14-7369. Instance Table

Instance Name	Physical Address
PLL0	0068 4024h

Figure 14-3667. MAIN_PLL_MMRCFG_PLL4_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7370. MAIN_PLL_MMRCFG_PLL4_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.2.73 MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL0 Register

14.2.3.1.2.73.1 MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL0 Register (Offset = 4030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL4 Frequency Control 4 Register

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Table 14-7371. Instance Table

Instance Name	Physical Address
PLL0	0068 4030h

Figure 14-3668. MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7372. MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.2.74 MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL1 Register

14.2.3.1.2.74.1 MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL1 Register (Offset = 4034h) [reset = 0h]

PLL4_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-7373. Instance Table

Instance Name	Physical Address
PLL0	0068 4034h

Figure 14-3669. MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7374. MAIN_PLL_MMRCFG_PLL4_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.75 MAIN_PLL_MMRCFG_PLL4_DIV_CTRL Register

14.2.3.1.2.75.1 MAIN_PLL_MMRCFG_PLL4_DIV_CTRL Register (Offset = 4038h) [reset = 1020001h]

PLL4_DIV_CTRL - PLL4 Output Clock Divider Register

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Table 14-7375. Instance Table

Instance Name	Physical Address
PLL0	0068 4038h

Figure 14-3670. MAIN_PLL_MMRCFG_PLL4_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7376. MAIN_PLL_MMRCFG_PLL4_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.76 MAIN_PLL_MMRCFG_PLL4_SS_CTRL Register

14.2.3.1.2.76.1 MAIN_PLL_MMRCFG_PLL4_SS_CTRL Register (Offset = 4040h) [reset = 80000000h]

PLL_SS_CTRL register for pll4

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Table 14-7377. Instance Table

Instance Name	Physical Address
PLL0	0068 4040h

Figure 14-3671. MAIN_PLL_MMRCFG_PLL4_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	

23	22	21	20	19	18	17	16
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	

15	14	13	12	11	10	9	8
RESET	RESERVED						
R/W	NONE						
0h	0h						

7	6	5	4	3	2	1	0
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7378. MAIN_PLL_MMRCFG_PLL4_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7378. MAIN_PLL_MMRCFG_PLL4_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.2.77 MAIN_PLL_MMRCFG_PLL4_SS_SPREAD Register

14.2.3.1.2.77.1 MAIN_PLL_MMRCFG_PLL4_SS_SPREAD Register (Offset = 4044h) [reset = 10001h]

PLL_SS_SPREAD register for pll4

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Table 14-7379. Instance Table

Instance Name	Physical Address
PLL0	0068 4044h

Figure 14-3672. MAIN_PLL_MMRCFG_PLL4_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7380. MAIN_PLL_MMRCFG_PLL4_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.2.78 MAIN_PLL_MMRCFG_PLL4_CAL_CTRL Register

14.2.3.1.2.78.1 MAIN_PLL_MMRCFG_PLL4_CAL_CTRL Register (Offset = 4060h) [reset = 20000h]

PLL4_CAL_CTRL - PLL4 Calibration Control Register

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Table 14-7381. Instance Table

Instance Name	Physical Address
PLL0	0068 4060h

Figure 14-3673. MAIN_PLL_MMRCFG_PLL4_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7382. MAIN_PLL_MMRCFG_PLL4_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7382. MAIN_PLL_MMRCFG_PLL4_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.2.79 MAIN_PLL_MMRCFG_PLL4_CAL_STAT Register

14.2.3.1.2.79.1 MAIN_PLL_MMRCFG_PLL4_CAL_STAT Register (Offset = 4064h) [reset = 0h]

PLL4_CAL_STAT - PLL4 Calibration Status Register

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Table 14-7383. Instance Table

Instance Name	Physical Address
PLL0	0068 4064h

Figure 14-3674. MAIN_PLL_MMRCFG_PLL4_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7384. MAIN_PLL_MMRCFG_PLL4_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.2.80 MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL0 Register

14.2.3.1.2.80.1 MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL0 Register (Offset = 4080h) [reset = 0h]

HSDIV_CTRL0 register for pll4

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Table 14-7385. Instance Table

Instance Name	Physical Address
PLL0	0068 4080h

Figure 14-3675. MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7386. MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.81 MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL1 Register

14.2.3.1.2.81.1 MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL1 Register (Offset = 4084h) [reset = 0h]

HSDIV_CTRL1 register for pll4

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Table 14-7387. Instance Table

Instance Name	Physical Address
PLL0	0068 4084h

Figure 14-3676. MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7388. MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.82 MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL2 Register

14.2.3.1.2.82.1 MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL2 Register (Offset = 4088h) [reset = 0h]

HSDIV_CTRL2 register for pll4

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Table 14-7389. Instance Table

Instance Name	Physical Address
PLL0	0068 4088h

Figure 14-3677. MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7390. MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.83 MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL3 Register

14.2.3.1.2.83.1 MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL3 Register (Offset = 408Ch) [reset = 0h]

HSDIV_CTRL3 register for pll4

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Table 14-7391. Instance Table

Instance Name	Physical Address
PLL0	0068 408Ch

Figure 14-3678. MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7392. MAIN_PLL_MMRCFG_PLL4_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.84 MAIN_PLL_MMRCFG_PLL7_PID Register

14.2.3.1.2.84.1 MAIN_PLL_MMRCFG_PLL7_PID Register (Offset = 7000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-7393. Instance Table

Instance Name	Physical Address
PLL0	0068 7000h

Figure 14-3679. MAIN_PLL_MMRCFG_PLL7_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7394. MAIN_PLL_MMRCFG_PLL7_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.2.85 MAIN_PLL_MMRCFG_PLL7_CFG Register

14.2.3.1.2.85.1 MAIN_PLL_MMRCFG_PLL7_CFG Register (Offset = 7008h) [reset = 30801h]

pll MMR Configuration

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Table 14-7395. Instance Table

Instance Name	Physical Address
PLL0	0068 7008h

Figure 14-3680. MAIN_PLL_MMRCFG_PLL7_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
3h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HSDIV_PRSNT							
R							
3h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-7396. MAIN_PLL_MMRCFG_PLL7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.2.86 MAIN_PLL_MMRCFG_PLL7_LOCKKEY0 Register

14.2.3.1.2.86.1 MAIN_PLL_MMRCFG_PLL7_LOCKKEY0 Register (Offset = 7010h) [reset = 0h]

PLL7_LOCKKEY0 - PLL7 Lock Key 0 Register

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Table 14-7397. Instance Table

Instance Name	Physical Address
PLL0	0068 7010h

Figure 14-3681. MAIN_PLL_MMRCFG_PLL7_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7398. MAIN_PLL_MMRCFG_PLL7_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition7 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.2.87 MAIN_PLL_MMRCFG_PLL7_LOCKKEY1 Register

14.2.3.1.2.87.1 MAIN_PLL_MMRCFG_PLL7_LOCKKEY1 Register (Offset = 7014h) [reset = 0h]

PLL7_LOCKKEY1 - PLL7 Lock Key 1 RegisterAddr

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Table 14-7399. Instance Table

Instance Name	Physical Address
PLL0	0068 7014h

Figure 14-3682. MAIN_PLL_MMRCFG_PLL7_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7400. MAIN_PLL_MMRCFG_PLL7_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition7 registers Reset Source: srst_n

14.2.3.1.2.88 MAIN_PLL_MMRCFG_PLL7_CTRL Register

14.2.3.1.2.88.1 MAIN_PLL_MMRCFG_PLL7_CTRL Register (Offset = 7020h) [reset = 80010011h]

PLL7_CTRL - PLL7 Control

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Table 14-7401. Instance Table

Instance Name	Physical Address
PLL0	0068 7020h

Figure 14-3683. MAIN_PLL_MMRCFG_PLL7_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>BYP_ON_LOCKLOSS</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>PLL_EN</td><td colspan="6">RESERVED</td><td>INTL_BYP_EN</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>CLK_4PH_EN</td><td>CLK_POSTDIV_EN</td><td colspan="2">RESERVED</td><td>DSM_EN</td><td>DAC_EN</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="2">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-7402. MAIN_PLL_MMRCFG_PLL7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-7402. MAIN_PLL_MMRCFG_PLL7_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.89 MAIN_PLL_MMRCFG_PLL7_STAT Register

14.2.3.1.2.89.1 MAIN_PLL_MMRCFG_PLL7_STAT Register (Offset = 7024h) [reset = 0h]

PLL7_STAT - PLL7 Status

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Table 14-7403. Instance Table

Instance Name	Physical Address
PLL0	0068 7024h

Figure 14-3684. MAIN_PLL_MMRCFG_PLL7_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7404. MAIN_PLL_MMRCFG_PLL7_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.2.90 MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL0 Register

14.2.3.1.2.90.1 MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL0 Register (Offset = 7030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL7 Frequency Control 7 Register

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Table 14-7405. Instance Table

Instance Name	Physical Address
PLL0	0068 7030h

Figure 14-3685. MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7406. MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.2.91 MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL1 Register

14.2.3.1.2.91.1 MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL1 Register (Offset = 7034h) [reset = 0h]

PLL7_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-7407. Instance Table

Instance Name	Physical Address
PLL0	0068 7034h

Figure 14-3686. MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7408. MAIN_PLL_MMRCFG_PLL7_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.92 MAIN_PLL_MMRCFG_PLL7_DIV_CTRL Register

14.2.3.1.2.92.1 MAIN_PLL_MMRCFG_PLL7_DIV_CTRL Register (Offset = 7038h) [reset = 1020001h]

PLL7_DIV_CTRL - PLL7 Output Clock Divider Register

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Table 14-7409. Instance Table

Instance Name	Physical Address
PLL0	0068 7038h

Figure 14-3687. MAIN_PLL_MMRCFG_PLL7_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7410. MAIN_PLL_MMRCFG_PLL7_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.93 MAIN_PLL_MMRCFG_PLL7_SS_CTRL Register

14.2.3.1.2.93.1 MAIN_PLL_MMRCFG_PLL7_SS_CTRL Register (Offset = 7040h) [reset = 80000000h]

PLL_SS_CTRL register for pll7

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Table 14-7411. Instance Table

Instance Name	Physical Address
PLL0	0068 7040h

Figure 14-3688. MAIN_PLL_MMRCFG_PLL7_SS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="5">RESERVED</td><td colspan="2">WV_TBLE_MAXADDR</td></tr>
<tr><td>R/W</td><td colspan="5">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>1h</td><td colspan="5">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WV_TBLE_MAXADDR</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">NONE</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>DOWNSPREAD_EN</td><td colspan="3">RESERVED</td><td>WAVE_SEL</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-7412. MAIN_PLL_MMRCFG_PLL7_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7412. MAIN_PLL_MMRCFG_PLL7_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.2.94 MAIN_PLL_MMRCFG_PLL7_SS_SPREAD Register

14.2.3.1.2.94.1 MAIN_PLL_MMRCFG_PLL7_SS_SPREAD Register (Offset = 7044h) [reset = 10001h]

PLL_SS_SPREAD register for pll7

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Table 14-7413. Instance Table

Instance Name	Physical Address
PLL0	0068 7044h

Figure 14-3689. MAIN_PLL_MMRCFG_PLL7_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7414. MAIN_PLL_MMRCFG_PLL7_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.2.95 MAIN_PLL_MMRCFG_PLL7_CAL_CTRL Register

14.2.3.1.2.95.1 MAIN_PLL_MMRCFG_PLL7_CAL_CTRL Register (Offset = 7060h) [reset = 20000h]

PLL7_CAL_CTRL - PLL7 Calibration Control Register

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Table 14-7415. Instance Table

Instance Name	Physical Address
PLL0	0068 7060h

Figure 14-3690. MAIN_PLL_MMRCFG_PLL7_CAL_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>FAST_CAL</td><td>RESERVED</td><td colspan="3">CAL_CNT</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CAL_BYP</td><td colspan="3">RESERVED</td><td colspan="4">CAL_IN</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_IN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7416. MAIN_PLL_MMRCFG_PLL7_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7416. MAIN_PLL_MMRCFG_PLL7_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.2.96 MAIN_PLL_MMRCFG_PLL7_CAL_STAT Register

14.2.3.1.2.96.1 MAIN_PLL_MMRCFG_PLL7_CAL_STAT Register (Offset = 7064h) [reset = 0h]

PLL7_CAL_STAT - PLL7 Calibration Status Register

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Table 14-7417. Instance Table

Instance Name	Physical Address
PLL0	0068 7064h

Figure 14-3691. MAIN_PLL_MMRCFG_PLL7_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7418. MAIN_PLL_MMRCFG_PLL7_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.2.97 MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL0 Register

14.2.3.1.2.97.1 MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL0 Register (Offset = 7080h) [reset = 0h]

HSDIV_CTRL0 register for pll7

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Table 14-7419. Instance Table

Instance Name	Physical Address
PLL0	0068 7080h

Figure 14-3692. MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7420. MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.98 MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL1 Register

14.2.3.1.2.98.1 MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL1 Register (Offset = 7084h) [reset = 0h]

HSDIV_CTRL1 register for pll7

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Table 14-7421. Instance Table

Instance Name	Physical Address
PLL0	0068 7084h

Figure 14-3693. MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7422. MAIN_PLL_MMRCFG_PLL7_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.99 MAIN_PLL_MMRCFG_PLL14_PID Register

14.2.3.1.2.99.1 MAIN_PLL_MMRCFG_PLL14_PID Register (Offset = E000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-7423. Instance Table

Instance Name	Physical Address
PLL0	0068 E000h

Figure 14-3694. MAIN_PLL_MMRCFG_PLL14_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	22	21	20	19	18	17	16
MODULE							
R							
180h							
15	14	13	12	11	10	9	8
MISC					MAJOR		
R					R		
2h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7424. MAIN_PLL_MMRCFG_PLL14_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.2.100 MAIN_PLL_MMRCFG_PLL14_CFG Register

14.2.3.1.2.100.1 MAIN_PLL_MMRCFG_PLL14_CFG Register (Offset = E008h) [reset = 30801h]

pll MMR Configuration

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Table 14-7425. Instance Table

Instance Name	Physical Address
PLL0	0068 E008h

Figure 14-3695. MAIN_PLL_MMRCFG_PLL14_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-7426. MAIN_PLL_MMRCFG_PLL14_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.2.101 MAIN_PLL_MMRCFG_PLL14_LOCKKEY0 Register

14.2.3.1.2.101.1 MAIN_PLL_MMRCFG_PLL14_LOCKKEY0 Register (Offset = E010h) [reset = 0h]

PLL14_LOCKKEY0 - PLL14 Lock Key 0 Register

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Table 14-7427. Instance Table

Instance Name	Physical Address
PLL0	0068 E010h

Figure 14-3696. MAIN_PLL_MMRCFG_PLL14_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7428. MAIN_PLL_MMRCFG_PLL14_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition14 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.2.102 MAIN_PLL_MMRCFG_PLL14_LOCKKEY1 Register

14.2.3.1.2.102.1 MAIN_PLL_MMRCFG_PLL14_LOCKKEY1 Register (Offset = E014h) [reset = 0h]

PLL14_LOCKKEY1 - PLL14 Lock Key 1 RegisterAddr

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Table 14-7429. Instance Table

Instance Name	Physical Address
PLL0	0068 E014h

Figure 14-3697. MAIN_PLL_MMRCFG_PLL14_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7430. MAIN_PLL_MMRCFG_PLL14_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition14 registers Reset Source: srst_n

14.2.3.1.2.103 MAIN_PLL_MMRCFG_PLL14_CTRL Register

14.2.3.1.2.103.1 MAIN_PLL_MMRCFG_PLL14_CTRL Register (Offset = E020h) [reset = 80010011h]

PLL14_CTRL - PLL14 Control

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Table 14-7431. Instance Table

Instance Name	Physical Address
PLL0	0068 E020h

Figure 14-3698. MAIN_PLL_MMRCFG_PLL14_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7432. MAIN_PLL_MMRCFG_PLL14_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-7432. MAIN_PLL_MMRCFG_PLL14_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.104 MAIN_PLL_MMRCFG_PLL14_STAT Register

14.2.3.1.2.104.1 MAIN_PLL_MMRCFG_PLL14_STAT Register (Offset = E024h) [reset = 0h]

PLL14_STAT - PLL14 Status

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Table 14-7433. Instance Table

Instance Name	Physical Address
PLL0	0068 E024h

Figure 14-3699. MAIN_PLL_MMRCFG_PLL14_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LOCK</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7434. MAIN_PLL_MMRCFG_PLL14_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.2.105 MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL0 Register

14.2.3.1.2.105.1 MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL0 Register (Offset = E030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL14 Frequency Control 14 Register

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Table 14-7435. Instance Table

Instance Name	Physical Address
PLL0	0068 E030h

Figure 14-3700. MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7436. MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.2.106 MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL1 Register

14.2.3.1.2.106.1 MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL1 Register (Offset = E034h) [reset = 0h]

PLL14_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-7437. Instance Table

Instance Name	Physical Address
PLL0	0068 E034h

Figure 14-3701. MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7438. MAIN_PLL_MMRCFG_PLL14_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.107 MAIN_PLL_MMRCFG_PLL14_DIV_CTRL Register

14.2.3.1.2.107.1 MAIN_PLL_MMRCFG_PLL14_DIV_CTRL Register (Offset = E038h) [reset = 1020001h]

PLL14_DIV_CTRL - PLL14 Output Clock Divider Register

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Table 14-7439. Instance Table

Instance Name	Physical Address
PLL0	0068 E038h

Figure 14-3702. MAIN_PLL_MMRCFG_PLL14_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	22	21	20	19	18	17	16
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7440. MAIN_PLL_MMRCFG_PLL14_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.108 MAIN_PLL_MMRCFG_PLL14_SS_CTRL Register

14.2.3.1.2.108.1 MAIN_PLL_MMRCFG_PLL14_SS_CTRL Register (Offset = E040h) [reset = 80000000h]

PLL_SS_CTRL register for pll14

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Table 14-7441. Instance Table

Instance Name	**Physical Address**
PLL0	0068 E040h

Figure 14-3703. MAIN_PLL_MMRCFG_PLL14_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7442. MAIN_PLL_MMRCFG_PLL14_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7442. MAIN_PLL_MMRCFG_PLL14_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.2.109 MAIN_PLL_MMRCFG_PLL14_SS_SPREAD Register

14.2.3.1.2.109.1 MAIN_PLL_MMRCFG_PLL14_SS_SPREAD Register (Offset = E044h) [reset = 10001h]

PLL_SS_SPREAD register for pll14

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Table 14-7443. Instance Table

Instance Name	Physical Address
PLL0	0068 E044h

Figure 14-3704. MAIN_PLL_MMRCFG_PLL14_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7444. MAIN_PLL_MMRCFG_PLL14_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.2.110 MAIN_PLL_MMRCFG_PLL14_CAL_CTRL Register

14.2.3.1.2.110.1 MAIN_PLL_MMRCFG_PLL14_CAL_CTRL Register (Offset = E060h) [reset = 20000h]

PLL14_CAL_CTRL - PLL14 Calibration Control Register

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Table 14-7445. Instance Table

Instance Name	Physical Address
PLL0	0068 E060h

Figure 14-3705. MAIN_PLL_MMRCFG_PLL14_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7446. MAIN_PLL_MMRCFG_PLL14_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7446. MAIN_PLL_MMRCFG_PLL14_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.2.111 MAIN_PLL_MMRCFG_PLL14_CAL_STAT Register

14.2.3.1.2.111.1 MAIN_PLL_MMRCFG_PLL14_CAL_STAT Register (Offset = E064h) [reset = 0h]

PLL14_CAL_STAT - PLL14 Calibration Status Register

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Table 14-7447. Instance Table

Instance Name	Physical Address
PLL0	0068 E064h

Figure 14-3706. MAIN_PLL_MMRCFG_PLL14_CAL_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">LOCK_CNT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CAL_OUT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_OUT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7448. MAIN_PLL_MMRCFG_PLL14_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.2.112 MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL0 Register

14.2.3.1.2.112.1 MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL0 Register (Offset = E080h) [reset = 0h]

HSDIV_CTRL0 register for pll14

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Table 14-7449. Instance Table

Instance Name	Physical Address
PLL0	0068 E080h

Figure 14-3707. MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7450. MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.113 MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL1 Register

14.2.3.1.2.113.1 MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL1 Register (Offset = E084h) [reset = 0h]

HSDIV_CTRL1 register for pll14

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Table 14-7451. Instance Table

Instance Name	Physical Address
PLL0	0068 E084h

Figure 14-3708. MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7452. MAIN_PLL_MMRCFG_PLL14_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.114 MAIN_PLL_MMRCFG_PLL15_PID Register

14.2.3.1.2.114.1 MAIN_PLL_MMRCFG_PLL15_PID Register (Offset = F000h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-7453. Instance Table

Instance Name	Physical Address
PLL0	0068 F000h

Figure 14-3709. MAIN_PLL_MMRCFG_PLL15_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE			
R		R		R			
1h		2h		180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE							
R							
180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MISC					MAJOR		
R					R		
2h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-7454. MAIN_PLL_MMRCFG_PLL15_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.1.2.115 MAIN_PLL_MMRCFG_PLL15_CFG Register

14.2.3.1.2.115.1 MAIN_PLL_MMRCFG_PLL15_CFG Register (Offset = F008h) [reset = F0801h]

pll MMR Configuration

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Table 14-7455. Instance Table

Instance Name	Physical Address
PLL0	0068 F008h

Figure 14-3710. MAIN_PLL_MMRCFG_PLL15_CFG Name Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R							
Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R							
Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
NONE			R		NONE		R
0h			1h		0h		0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
NONE						R	
0h						1h	

Table 14-7456. MAIN_PLL_MMRCFG_PLL15_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.1.2.116 MAIN_PLL_MMRCFG_PLL15_LOCKKEY0 Register

14.2.3.1.2.116.1 MAIN_PLL_MMRCFG_PLL15_LOCKKEY0 Register (Offset = F010h) [reset = 0h]

PLL15_LOCKKEY0 - PLL15 Lock Key 0 Register

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Table 14-7457. Instance Table

Instance Name	Physical Address
PLL0	0068 F010h

Figure 14-3711. MAIN_PLL_MMRCFG_PLL15_LOCKKEY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">KEY</td><td>UNLOCKED</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7458. MAIN_PLL_MMRCFG_PLL15_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition15 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.1.2.117 MAIN_PLL_MMRCFG_PLL15_LOCKKEY1 Register

14.2.3.1.2.117.1 MAIN_PLL_MMRCFG_PLL15_LOCKKEY1 Register (Offset = F014h) [reset = 0h]

PLL15_LOCKKEY1 - PLL15 Lock Key 1 RegisterAddr

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Table 14-7459. Instance Table

Instance Name	Physical Address
PLL0	0068 F014h

Figure 14-3712. MAIN_PLL_MMRCFG_PLL15_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKKEY1_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKKEY1_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7460. MAIN_PLL_MMRCFG_PLL15_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition15 registers Reset Source: srst_n

14.2.3.1.2.118 MAIN_PLL_MMRCFG_PLL15_CTRL Register

14.2.3.1.2.118.1 MAIN_PLL_MMRCFG_PLL15_CTRL Register (Offset = F020h) [reset = 80010011h]

PLL15_CTRL - PLL15 Control

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Table 14-7461. Instance Table

Instance Name	Physical Address
PLL0	0068 F020h

Figure 14-3713. MAIN_PLL_MMRCFG_PLL15_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							BYP_ON_LOCKLOSS
NONE							R/W
0h							1h
15	14	13	12	11	10	9	8
PLL_EN	RESERVED						INTL_BYP_EN
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
NONE		R/W	R/W	NONE		R/W	R/W
0h		0h	1h	0h		0h	1h

Table 14-7462. MAIN_PLL_MMRCFG_PLL15_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-7462. MAIN_PLL_MMRCFG_PLL15_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.119 MAIN_PLL_MMRCFG_PLL15_STAT Register

14.2.3.1.2.119.1 MAIN_PLL_MMRCFG_PLL15_STAT Register (Offset = F024h) [reset = 0h]

PLL15_STAT - PLL15 Status

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Table 14-7463. Instance Table

Instance Name	**Physical Address**
PLL0	0068 F024h

Figure 14-3714. MAIN_PLL_MMRCFG_PLL15_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7464. MAIN_PLL_MMRCFG_PLL15_STAT Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.1.2.120 MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL0 Register

14.2.3.1.2.120.1 MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL0 Register (Offset = F030h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL15 Frequency Control 15 Register

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Table 14-7465. Instance Table

Instance Name	Physical Address
PLL0	0068 F030h

Figure 14-3715. MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FB_DIV_INT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_INT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-7466. MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.1.2.121 MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL1 Register

14.2.3.1.2.121.1 MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL1 Register (Offset = F034h) [reset = 0h]

PLL15_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-7467. Instance Table

Instance Name	Physical Address
PLL0	0068 F034h

Figure 14-3716. MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FB_DIV_FRAC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7468. MAIN_PLL_MMRCFG_PLL15_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.1.2.122 MAIN_PLL_MMRCFG_PLL15_DIV_CTRL Register

14.2.3.1.2.122.1 MAIN_PLL_MMRCFG_PLL15_DIV_CTRL Register (Offset = F038h) [reset = 1020001h]

PLL15_DIV_CTRL - PLL15 Output Clock Divider Register

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Table 14-7469. Instance Table

Instance Name	Physical Address
PLL0	0068 F038h

Figure 14-3717. MAIN_PLL_MMRCFG_PLL15_DIV_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">POST_DIV2</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">POST_DIV1</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">REF_DIV</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-7470. MAIN_PLL_MMRCFG_PLL15_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.123 MAIN_PLL_MMRCFG_PLL15_SS_CTRL Register

14.2.3.1.2.123.1 MAIN_PLL_MMRCFG_PLL15_SS_CTRL Register (Offset = F040h) [reset = 80000000h]

PLL_SS_CTRL register for pll15

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Table 14-7471. Instance Table

Instance Name	Physical Address
PLL0	0068 F040h

Figure 14-3718. MAIN_PLL_MMRCFG_PLL15_SS_CTRL Name Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W	NONE					R/W	
1h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W						NONE	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 14-7472. MAIN_PLL_MMRCFG_PLL15_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7472. MAIN_PLL_MMRCFG_PLL15_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.1.2.124 MAIN_PLL_MMRCFG_PLL15_SS_SPREAD Register

14.2.3.1.2.124.1 MAIN_PLL_MMRCFG_PLL15_SS_SPREAD Register (Offset = F044h) [reset = 10001h]

PLL_SS_SPREAD register for pll15

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Table 14-7473. Instance Table

Instance Name	Physical Address
PLL0	0068 F044h

Figure 14-3719. MAIN_PLL_MMRCFG_PLL15_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7474. MAIN_PLL_MMRCFG_PLL15_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.1.2.125 MAIN_PLL_MMRCFG_PLL15_CAL_CTRL Register

14.2.3.1.2.125.1 MAIN_PLL_MMRCFG_PLL15_CAL_CTRL Register (Offset = F060h) [reset = 20000h]

PLL15_CAL_CTRL - PLL15 Calibration Control Register

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Table 14-7475. Instance Table

Instance Name	Physical Address
PLL0	0068 F060h

Figure 14-3720. MAIN_PLL_MMRCFG_PLL15_CAL_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>FAST_CAL</td><td>RESERVED</td><td colspan="3">CAL_CNT</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CAL_BYP</td><td colspan="3">RESERVED</td><td colspan="4">CAL_IN</td></tr>
<tr><td>R/W</td><td colspan="3">NONE</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_IN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7476. MAIN_PLL_MMRCFG_PLL15_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7476. MAIN_PLL_MMRCFG_PLL15_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.1.2.126 MAIN_PLL_MMRCFG_PLL15_CAL_STAT Register

14.2.3.1.2.126.1 MAIN_PLL_MMRCFG_PLL15_CAL_STAT Register (Offset = F064h) [reset = 0h]

PLL15_CAL_STAT - PLL15 Calibration Status Register

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Table 14-7477. Instance Table

Instance Name	Physical Address
PLL0	0068 F064h

Figure 14-3721. MAIN_PLL_MMRCFG_PLL15_CAL_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAL_LOCK</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">LOCK_CNT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CAL_OUT</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAL_OUT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7478. MAIN_PLL_MMRCFG_PLL15_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.1.2.127 MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL0 Register

14.2.3.1.2.127.1 MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL0 Register (Offset = F080h) [reset = 8000h]

HSDIV_CTRL0 register for pll15

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Table 14-7479. Instance Table

Instance Name	Physical Address
PLL0	0068 F080h

Figure 14-3722. MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
1h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7480. MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	1h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.128 MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL1 Register

14.2.3.1.2.128.1 MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL1 Register (Offset = F084h) [reset = 8000h]

HSDIV_CTRL1 register for pll15

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Table 14-7481. Instance Table

Instance Name	Physical Address
PLL0	0068 F084h

Figure 14-3723. MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
1h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7482. MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	1h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.129 MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL2 Register

14.2.3.1.2.129.1 MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL2 Register (Offset = F088h) [reset = 8000h]

HSDIV_CTRL2 register for pll15

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Table 14-7483. Instance Table

Instance Name	Physical Address
PLL0	0068 F088h

Figure 14-3724. MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
1h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7484. MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	1h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.1.2.130 MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL3 Register

14.2.3.1.2.130.1 MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL3 Register (Offset = F08Ch) [reset = 0h]

HSDIV_CTRL3 register for pll15

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Table 14-7485. Instance Table

Instance Name	Physical Address
PLL0	0068 F08Ch

Figure 14-3725. MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL3 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7486. MAIN_PLL_MMRCFG_PLL15_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2 PLL

PLL

14.2.3.2.1 PLL Summaries

PLL Summaries

Table 14-7487. MCU_PLL_MMR_CFG Registers, Base Address=0404 0000h, Length=4096

Offset	Length	Register Name	MCU_PLL0 Physical Address
0h	32	MCU_PLL_MMRCFG_PLL0_PID	0404 0000h
8h	32	MCU_PLL_MMRCFG_PLL0_CFG	0404 0008h
10h	32	MCU_PLL_MMRCFG_PLL0_LOCKKEY0	0404 0010h
14h	32	MCU_PLL_MMRCFG_PLL0_LOCKKEY1	0404 0014h
20h	32	MCU_PLL_MMRCFG_PLL0_CTRL	0404 0020h
24h	32	MCU_PLL_MMRCFG_PLL0_STAT	0404 0024h
30h	32	MCU_PLL_MMRCFG_PLL0_FREQ_CTRL0	0404 0030h
34h	32	MCU_PLL_MMRCFG_PLL0_FREQ_CTRL1	0404 0034h
38h	32	MCU_PLL_MMRCFG_PLL0_DIV_CTRL	0404 0038h
40h	32	MCU_PLL_MMRCFG_PLL0_SS_CTRL	0404 0040h
44h	32	MCU_PLL_MMRCFG_PLL0_SS_SPREAD	0404 0044h
60h	32	MCU_PLL_MMRCFG_PLL0_CAL_CTRL	0404 0060h
64h	32	MCU_PLL_MMRCFG_PLL0_CAL_STAT	0404 0064h
80h	32	MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL0	0404 0080h
84h	32	MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL1	0404 0084h
88h	32	MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL2	0404 0088h
8Ch	32	MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL3	0404 008Ch
90h	32	MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL4	0404 0090h
94h	32	MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL5	0404 0094h
98h	32	MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL6	0404 0098h

14.2.3.2.2 PLL Registers

PLL Registers

14.2.3.2.2.1 MCU_PLL_MMRCFG_PLL0_PID Register

14.2.3.2.2.1.1 MCU_PLL_MMRCFG_PLL0_PID Register (Offset = 0h) [reset = 61801001h]

Peripheral Identification Register

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Table 14-7488. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0000h

Figure 14-3726. MCU_PLL_MMRCFG_PLL0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">MISC</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">2h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-7489. MCU_PLL_MMRCFG_PLL0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID follows new scheme Reset Source: sys_por_arst_rst_n
29:28	BU	R	2h	Business Unit - Processors Reset Source: sys_por_arst_rst_n
27:16	MODULE	R	180h	Module functional identifier Reset Source: sys_por_arst_rst_n
15:11	MISC	R	2h	Misc revision number Reset Source: sys_por_arst_rst_n
10:8	MAJOR	R	0h	Major revision number Reset Source: sys_por_arst_rst_n
7:6	CUSTOM	R	0h	custom revision number Reset Source: sys_por_arst_rst_n
5:0	MINOR	R	1h	Minor revision number Reset Source: sys_por_arst_rst_n

14.2.3.2.2.2 MCU_PLL_MMRCFG_PLL0_CFG Register

14.2.3.2.2.2.1 MCU_PLL_MMRCFG_PLL0_CFG Register (Offset = 8h) [reset = 7F0801h]

pll MMR Configuration

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Table 14-7490. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0008h

Figure 14-3727. MCU_PLL_MMRCFG_PLL0_CFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7Fh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">HSDIV_PRSNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7Fh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="2">SSM_TYPE</td><td colspan="2">RESERVED</td><td>SSM_WVTBL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="2">R</td><td colspan="2">NONE</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td colspan="2">1h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PLL_TYPE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">1h</td></tr>
</table>

Table 14-7491. MCU_PLL_MMRCFG_PLL0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HSDIV_PRSNT	R	7Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV[4:0] are connected the PLL FOUTVCO output clock and HSDIV[15:5] are connected to the PLL FOUTPOSTDIV output clock Reset Source: sys_por_arst_rst_n
15:13	RESERVED	NONE	0h	Reserved
12:11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved Reset Source: sys_por_arst_rst_n
10:9	RESERVED	NONE	0h	Reserved
8	SSM_WVTBL	R	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present Reset Source: sys_por_arst_rst_n
7:2	RESERVED	NONE	0h	Reserved
1:0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL Reset Source: sys_por_arst_rst_n

14.2.3.2.2.3 MCU_PLL_MMRCFG_PLL0_LOCKKEY0 Register

14.2.3.2.2.3.1 MCU_PLL_MMRCFG_PLL0_LOCKKEY0 Register (Offset = 10h) [reset = 0h]

PLL0_LOCKKEY0 - PLL0 Lock Key 0 Register

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Table 14-7492. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0010h

Figure 14-3728. MCU_PLL_MMRCFG_PLL0_LOCKKEY0 Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W							R
0h							0h

Table 14-7493. MCU_PLL_MMRCFG_PLL0_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for Writing. Reset Source: srst_n

14.2.3.2.2.4 MCU_PLL_MMRCFG_PLL0_LOCKKEY1 Register

14.2.3.2.2.4.1 MCU_PLL_MMRCFG_PLL0_LOCKKEY1 Register (Offset = 14h) [reset = 0h]

PLL0_LOCKKEY1 - PLL0 Lock Key 1 RegisterAddr

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Table 14-7494. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0014h

Figure 14-3729. MCU_PLL_MMRCFG_PLL0_LOCKKEY1 Name Register

31	30	29	28	27	26	25	24
LOCKKEY1_VAL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOCKKEY1_VAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCKKEY1_VAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCKKEY1_VAL							
R/W							
0h							

Table 14-7495. MCU_PLL_MMRCFG_PLL0_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers Reset Source: srst_n

14.2.3.2.2.5 MCU_PLL_MMRCFG_PLL0_CTRL Register

14.2.3.2.2.5.1 MCU_PLL_MMRCFG_PLL0_CTRL Register (Offset = 20h) [reset = 80010011h]

PLL0_CTRL - PLL0 Control

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Table 14-7496. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0020h

Figure 14-3730. MCU_PLL_MMRCFG_PLL0_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>BYP_ON_LOCKLOSS</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>PLL_EN</td><td colspan="6">RESERVED</td><td>INTL_BYP_EN</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>CLK_4PH_EN</td><td>CLK_POSTDIV_EN</td><td colspan="2">RESERVED</td><td>DSM_EN</td><td>DAC_EN</td></tr>
<tr><td colspan="2">NONE</td><td>R/W</td><td>R/W</td><td colspan="2">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>1h</td><td colspan="2">0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-7497. MCU_PLL_MMRCFG_PLL0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The bypass_en bit should be set prior tomaking any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs Reset Source: sys_por_arst_rst_n
30:17	RESERVED	NONE	0h	Reserved
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock Reset Source: sys_por_arst_rst_n
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the outputclocks during switching. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock Reset Source: sys_por_arst_rst_n
7:6	RESERVED	NONE	0h	Reserved

Table 14-7497. MCU_PLL_MMRCFG_PLL0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. This bit is ignored if clk_postdiv_en=0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled. Reset Source: sys_por_arst_rst_n
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled. Reset Source: sys_por_arst_rst_n
3:2	RESERVED	NONE	0h	Reserved
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled (use integer divide mode) 1'b1 - Delta-Sigma modulator is enabled (use fractional divide mode) Reset Source: sys_por_arst_rst_n
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function (DAC is always disabled) in integer divide mode (when dsm_en=0) 1'b0 - Fractional NC DAC is disabled (for Test modes only) 1'b1 - Fractional NC DAC is enabled (ignored in integer divide mode) Reset Source: sys_por_arst_rst_n

14.2.3.2.2.6 MCU_PLL_MMRCFG_PLL0_STAT Register

14.2.3.2.2.6.1 MCU_PLL_MMRCFG_PLL0_STAT Register (Offset = 24h) [reset = 0h]

PLL0_STAT - PLL0 Status

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Table 14-7498. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0024h

Figure 14-3731. MCU_PLL_MMRCFG_PLL0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
NONE							R
0h							0h

Table 14-7499. MCU_PLL_MMRCFG_PLL0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL_bypass_en bit 1'b0 - PLL is not locked 1'b1 - PLL is locked Reset Source: sys_por_arst_rst_n

14.2.3.2.2.7 MCU_PLL_MMRCFG_PLL0_FREQ_CTRL0 Register

14.2.3.2.2.7.1 MCU_PLL_MMRCFG_PLL0_FREQ_CTRL0 Register (Offset = 30h) [reset = 10h]

PLL0_FREQ_CTRL0 - PLL0 Frequency Control 0 Register

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Table 14-7500. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0030h

Figure 14-3732. MCU_PLL_MMRCFG_PLL0_FREQ_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FB_DIV_INT			
NONE				R/W			
0h				10h			
7	6	5	4	3	2	1	0
FB_DIV_INT							
R/W							
10h							

Table 14-7501. MCU_PLL_MMRCFG_PLL0_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	FB_DIV_INT	R/W	10h	PLL feedback divider (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h010 - Divide by 16 12'h011 - Divide by 17 : 12'h140 - Divide by 320 : 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported Reset Source: sys_por_arst_rst_n

14.2.3.2.2.8 MCU_PLL_MMRCFG_PLL0_FREQ_CTRL1 Register

14.2.3.2.2.8.1 MCU_PLL_MMRCFG_PLL0_FREQ_CTRL1 Register (Offset = 34h) [reset = 0h]

PLL0_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

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Table 14-7502. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0034h

Figure 14-3733. MCU_PLL_MMRCFG_PLL0_FREQ_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FB_DIV_FRAC							
R/W							
0h							
15	14	13	12	11	10	9	8
FB_DIV_FRAC							
R/W							
0h							
7	6	5	4	3	2	1	0
FB_DIV_FRAC							
R/W							
0h							

Table 14-7503. MCU_PLL_MMRCFG_PLL0_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	FB_DIV_FRAC	R/W	0h	PLL feedback divider (fractional portion) Supports values of 0 to 0.999999940395. The total feedback divide value is (fb_div_int + fb_div_frac / (2^24)) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^24)) 24'h000002 - .000000119209 (2/(2^24)) : 24'h800000 - .500000000000 : 24'hFFFFFF - .999999940395 (1677215/(2^24)) Reset Source: sys_por_arst_rst_n

14.2.3.2.2.9 MCU_PLL_MMRCFG_PLL0_DIV_CTRL Register

14.2.3.2.2.9.1 MCU_PLL_MMRCFG_PLL0_DIV_CTRL Register (Offset = 38h) [reset = 1020001h]

PLL0_DIV_CTRL - PLL0 Output Clock Divider Register

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Table 14-7504. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0038h

Figure 14-3734. MCU_PLL_MMRCFG_PLL0_DIV_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					POST_DIV2		
NONE					R/W		
0h					1h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					POST_DIV1		
NONE					R/W		
0h					2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		REF_DIV					
NONE		R/W					
0h		1h					

Table 14-7505. MCU_PLL_MMRCFG_PLL0_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7 Reset Source: sys_por_arst_rst_n
23:19	RESERVED	NONE	0h	Reserved
18:16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, post_div1 must always be programmed to a value equal to or greater that post_div2. Supports values of 1-7i Field values (Others are reserved): 3'b000 - Reserved (do not use) 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7 Reset Source: sys_por_arst_rst_n
15:6	RESERVED	NONE	0h	Reserved
5:0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved /(do not use/) 6'b000001 - Divide by 1 6'b000010 - Divide by 2 : 6'b111111 - Divide by 63 Reset Source: sys_por_arst_rst_n

14.2.3.2.2.10 MCU_PLL_MMRCFG_PLL0_SS_CTRL Register

14.2.3.2.2.10.1 MCU_PLL_MMRCFG_PLL0_SS_CTRL Register (Offset = 40h) [reset = 80000000h]

PLL_SS_CTRL register for pll0

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Table 14-7506. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0040h

Figure 14-3735. MCU_PLL_MMRCFG_PLL0_SS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>BYPASS_EN</td><td colspan="5">RESERVED</td><td colspan="2">WV_TBLE_MAXADDR</td></tr>
<tr><td>R/W</td><td colspan="5">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>1h</td><td colspan="5">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WV_TBLE_MAXADDR</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">NONE</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>DOWNSPREAD_EN</td><td colspan="3">RESERVED</td><td>WAVE_SEL</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-7507. MCU_PLL_MMRCFG_PLL0_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency Reset Source: sys_por_arst_rst_n
30:26	RESERVED	NONE	0h	Reserved
25:18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLL_CFG_ssm_wvtbl = 0 Reset Source: sys_por_arst_rst_n
17:16	RESERVED	NONE	0h	Reserved
15	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in reset Reset Source: sys_por_arst_rst_n
14:5	RESERVED	NONE	0h	Reserved
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread Reset Source: sys_por_arst_rst_n
3:1	RESERVED	NONE	0h	Reserved

Table 14-7507. MCU_PLL_MMRCFG_PLL0_SS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLL_CFG_ssm_wvtbl = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table Reset Source: sys_por_arst_rst_n

14.2.3.2.2.11 MCU_PLL_MMRCFG_PLL0_SS_SPREAD Register

14.2.3.2.2.11.1 MCU_PLL_MMRCFG_PLL0_SS_SPREAD Register (Offset = 44h) [reset = 10001h]

PLL_SS_SPREAD register for pll0

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Table 14-7508. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0044h

Figure 14-3736. MCU_PLL_MMRCFG_PLL0_SS_SPREAD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				MOD_DIV			
NONE				R/W			
0h				1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			SPREAD				
NONE			R/W				
0h			1h				

Table 14-7509. MCU_PLL_MMRCFG_PLL0_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-15 Reset Source: sys_por_arst_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1% Reset Source: sys_por_arst_rst_n

14.2.3.2.2.12 MCU_PLL_MMRCFG_PLL0_CAL_CTRL Register

14.2.3.2.2.12.1 MCU_PLL_MMRCFG_PLL0_CAL_CTRL Register (Offset = 60h) [reset = 20000h]

PLL0_CAL_CTRL - PLL0 Calibration Control Register

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Table 14-7510. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0060h

Figure 14-3737. MCU_PLL_MMRCFG_PLL0_CAL_CTRL Name Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
NONE			R/W	NONE	R/W		
0h			0h	0h	2h		
15	14	13	12	11	10	9	8
CAL_BYP	RESERVED			CAL_IN			
R/W	NONE			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
CAL_IN							
R/W							
0h							

Table 14-7511. MCU_PLL_MMRCFG_PLL0_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input Reset Source: sys_por_arst_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known Reset Source: sys_por_arst_rst_n
19	RESERVED	NONE	0h	Reserved
18:16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt Reset Source: sys_por_arst_rst_n
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction Reset Source: sys_por_arst_rst_n
14:12	RESERVED	NONE	0h	Reserved

Table 14-7511. MCU_PLL_MMRCFG_PLL0_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset. Reset Source: sys_por_arst_rst_n

14.2.3.2.2.13 MCU_PLL_MMRCFG_PLL0_CAL_STAT Register

14.2.3.2.2.13.1 MCU_PLL_MMRCFG_PLL0_CAL_STAT Register (Offset = 64h) [reset = 0h]

PLL0_CAL_STAT - PLL0 Calibration Status Register

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Table 14-7512. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0064h

Figure 14-3738. MCU_PLL_MMRCFG_PLL0_CAL_STAT Name Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				LOCK_CNT			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CAL_OUT			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
CAL_OUT							
R							
0h							

Table 14-7513. MCU_PLL_MMRCFG_PLL0_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	LOCK_CNT	R	0h	Reserved for future use Reset Source: sys_por_arst_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in[11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration Reset Source: sys_por_arst_rst_n

14.2.3.2.2.14 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL0 Register

14.2.3.2.2.14.1 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL0 Register (Offset = 80h) [reset = 0h]

HSDIV_CTRL0 register for pll0

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Table 14-7514. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0080h

Figure 14-3739. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7515. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.2.15 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL1 Register

14.2.3.2.2.15.1 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL1 Register (Offset = 84h) [reset = 0h]

HSDIV_CTRL1 register for pll0

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Table 14-7516. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0084h

Figure 14-3740. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7517. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.2.16 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL2 Register

14.2.3.2.2.16.1 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL2 Register (Offset = 88h) [reset = 0h]

HSDIV_CTRL2 register for pll0

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Table 14-7518. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0088h

Figure 14-3741. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7519. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.2.17 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL3 Register

14.2.3.2.2.17.1 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL3 Register (Offset = 8Ch) [reset = 0h]

HSDIV_CTRL3 register for pll0

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Table 14-7520. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 008Ch

Figure 14-3742. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CLKOUT_EN</td><td colspan="6">RESERVED</td><td>SYNC_DIS</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="7">HSDIV</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-7521. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.2.18 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL4 Register

14.2.3.2.2.18.1 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL4 Register (Offset = 90h) [reset = 0h]

HSDIV_CTRL4 register for pll0

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Table 14-7522. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0090h

Figure 14-3743. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL4 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7523. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.2.19 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL5 Register

14.2.3.2.2.19.1 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL5 Register (Offset = 94h) [reset = 0h]

HSDIV_CTRL5 register for pll0

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Table 14-7524. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0094h

Figure 14-3744. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL5 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7525. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.2.2.20 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL6 Register

14.2.3.2.2.20.1 MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL6 Register (Offset = 98h) [reset = 0h]

HSDIV_CTRL6 register for pll0

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Table 14-7526. Instance Table

Instance Name	Physical Address
MCU_PLL0	0404 0098h

Figure 14-3745. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL6 Name Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
NONE	R/W						
0h	0h						

Table 14-7527. MCU_PLL_MMRCFG_PLL0_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	SSM reset. When set to 1 the SSM modulator is in resetl Reset Source: sys_por_arst_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1 Reset Source: sys_por_arst_rst_n
14:9	RESERVED	NONE	0h	Reserved
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 0 - Changes to DIV value synchronized to prevent glitches 1 - Changes are asynchronous Reset Source: sys_por_arst_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127 Reset Source: sys_por_arst_rst_n

14.2.3.3 TIMESYNC_EVENT_INTROUTER

TIMESYNC_EVENT_INTROUTER

14.2.3.3.1 TIMESYNC_EVENT_INTROUTER Summaries

TIMESYNC_EVENT_INTROUTER Summaries

Table 14-7528. INTR_ROUTER_CFG Registers, Base Address=00A4 0000h, Length=1024

Offset	Length	Register Name	TIMESYNC_EVENT_INTROUTER0 Physical Address
0h	32	INTR_ROUTER_CFG_PID	00A4 0000h
4h	32	INTR_ROUTER_CFG_MUXCNTL_J	00A4 0004h + formula

14.2.3.3.2 TIMESYNC_EVENT_INTROUTER Registers

TIMESYNC_EVENT_INTROUTER Registers

14.2.3.3.2.1 INTR_ROUTER_CFG_PID Register

14.2.3.3.2.1.1 INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Identification register

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Table 14-7529. Instance Table

Instance Name	Physical Address
TIMESYNC_EVENT_INTROUTER0	00A4 0000h

Figure 14-3746. INTR_ROUTER_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
694h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLVER					MAJREV		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-7530. INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	Business Unit Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

14.2.3.3.2.2 INTR_ROUTER_CFG_MUXCNTL_J Register

14.2.3.3.2.2.1 INTR_ROUTER_CFG_MUXCNTL_J Register (Offset = 4h) [reset = 0h]

Interrupt mux control register

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Table 14-7531. Instance Table

Instance Name	Physical Address
TIMESYNC_EVENT_INTROUTER0	00A4 0004h + formula

Figure 14-3747. INTR_ROUTER_CFG_MUXCNTL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							INT_ENABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			MUX_CNTL				
NONE			R/W				
0h			0h				

Table 14-7532. INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

14.3 Processors and Accelerators Registers

14.3.1 R5FSS Registers

14.3.1.1 R5FSS_COMMON0

R5FSS_COMMON0

14.3.1.1.1 R5FSS_COMMON0 Summaries

R5FSS_COMMON0 Summaries

Table 14-7533. ECC_AGGR Registers, Base Address=3F00 D000h, Length=1024

Offset	Length	Register Name	WKUP_R5FSS0_COMMON0 Physical Address
0h	32	ECC_AGGR_REV	3F00 D000h
8h	32	ECC_AGGR_VECTOR	3F00 D008h
Ch	32	ECC_AGGR_STAT	3F00 D00Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	3F00 D010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	3F00 D03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	3F00 D040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	3F00 D080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	3F00 D0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	3F00 D13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	3F00 D140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	3F00 D180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	3F00 D1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	3F00 D200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	3F00 D204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	3F00 D208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	3F00 D20Ch

14.3.1.1.2 R5FSS_COMMON0 Registers

R5FSS_COMMON0 Registers

14.3.1.1.2.1 ECC_AGGR_REV Register

14.3.1.1.2.1.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-7534. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D000h

Figure 14-3748. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
5h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-7535. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.1.1.2.2 ECC_AGGR_VECTOR Register

14.3.1.1.2.2.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-7536. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D008h

Figure 14-3749. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-7537. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.1.1.2.3 ECC_AGGR_STAT Register

14.3.1.1.2.3.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1Dh]

Misc Status

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Table 14-7538. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D00Ch

Figure 14-3750. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Dh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Dh							

Table 14-7539. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Dh	Indicates the number of RAMS serviced by the ECC aggregator

14.3.1.1.2.4 ECC_AGGR_RESERVED_SVBUS_J Register

14.3.1.1.2.4.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-7540. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D010h + formula

Figure 14-3751. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-7541. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.1.1.2.5 ECC_AGGR_SEC_EOI_REG Register

14.3.1.1.2.5.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-7542. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D03Ch

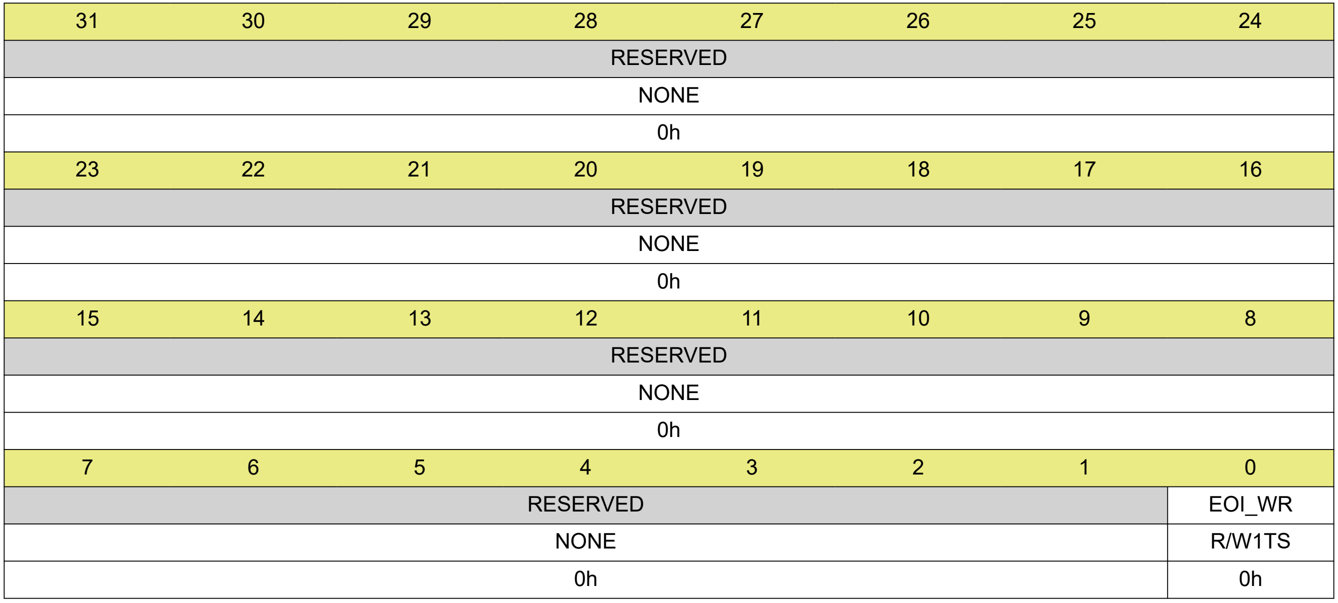

Figure 14-3752. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7543. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

14.3.1.1.2.6.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7544. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D040h

Figure 14-3753. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7545. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend

Table 14-7545. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.1.1.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.3.1.1.2.7.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7546. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D080h

Figure 14-3754. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7547. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend

Table 14-7547. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.1.1.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.3.1.1.2.8.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7548. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D0C0h

Figure 14-3755. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7549. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend

Table 14-7549. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.1.1.2.9 ECC_AGGR_DED_EOI_REG Register

14.3.1.1.2.9.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-7550. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D13Ch

Figure 14-3756. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-7551. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.1.1.2.10 ECC_AGGR_DED_STATUS_REG0 Register

14.3.1.1.2.10.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-7552. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D140h

Figure 14-3757. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7553. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend

Table 14-7553. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

14.3.1.1.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.3.1.1.2.11.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-7554. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D180h

Figure 14-3758. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7555. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend

Table 14-7555. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

14.3.1.1.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.3.1.1.2.12.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-7556. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D1C0h

Figure 14-3759. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7557. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_AXI2VBUSM_MEM_MST_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_axi2vbusm_mem_mst_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend

Table 14-7557. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

14.3.1.1.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

14.3.1.1.2.13.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-7558. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D200h

Figure 14-3760. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-7559. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.1.1.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

14.3.1.1.2.14.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-7560. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D204h

Figure 14-3761. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7561. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.1.1.2.15 ECC_AGGR_AGGR_STATUS_SET Register

14.3.1.1.2.15.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-7562. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D208h

Figure 14-3762. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-7563. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.1.1.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

14.3.1.1.2.16.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-7564. Instance Table

Instance Name	Physical Address
WKUP_R5FSS0_COMMON0	3F00 D20Ch

Figure 14-3763. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-7565. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.1.2 R5FSS_COMMON0

R5FSS_COMMON0

14.3.1.2.1 R5FSS_COMMON0 Summaries

R5FSS_COMMON0 Summaries

Table 14-7566. R5FSS_COMMON0_COMPARE_CFG Registers, Base Address=05B0 0000h, Length=256

Offset	Length	Register Name	R5FSS0_COMMON0 Physical Address	R5FSS1_COMMON0 Physical Address
0h	32	R5FSS_COMMON0_COMPARE_CFG_CCMSR1	05B0 0000h	05B2 0000h
4h	32	R5FSS_COMMON0_COMPARE_CFG_CCMKEYR1	05B0 0004h	05B2 0004h
8h	32	R5FSS_COMMON0_COMPARE_CFG_CCMSR2	05B0 0008h	05B2 0008h
Ch	32	R5FSS_COMMON0_COMPARE_CFG_CCMKEYR2	05B0 000Ch	05B2 000Ch
10h	32	R5FSS_COMMON0_COMPARE_CFG_CCMSR3	05B0 0010h	05B2 0010h
14h	32	R5FSS_COMMON0_COMPARE_CFG_CCMKEYR3	05B0 0014h	05B2 0014h
18h	32	R5FSS_COMMON0_COMPARE_CFG_CCMPOLCNTRL	05B0 0018h	05B2 0018h

Table 14-7567. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS Registers, Base Address=05B0 1000h, Length=256

Offset	Length	Register Name	R5FSS0_COMMON0 Physical Address	R5FSS1_COMMON0 Physical Address	WKUP_R5FSS0_COMMON0 Physical Address
0h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR	05B0 1000h	05B2 1000h	3C01 8000h
4h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS	05B0 1004h	05B2 1004h	3C01 8004h
8h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS	05B0 1008h	05B2 1008h	3C01 8008h
Ch	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS	05B0 100Ch	05B2 100Ch	3C01 800Ch
10h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS	05B0 1010h	05B2 1010h	3C01 8010h
14h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS	05B0 1014h	05B2 1014h	3C01 8014h
18h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET	05B0 1018h	05B2 1018h	3C01 8018h
1Ch	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR	05B0 101Ch	05B2 101Ch	3C01 801Ch

Table 14-7567. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS Registers, Base Address=05B0 1000h, Length=256 (continued)

Offset	Length	Register Name	R5FSS0_COMMON0 Physical Address	R5FSS1_COMMON0 Physical Address	WKUP_R5FSS0_COMMON0 Physical Address
20h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET	05B0 1020h	05B2 1020h	3C01 8020h
24h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR	05B0 1024h	05B2 1024h	3C01 8024h
40h	32	R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID	05B0 1040h	05B2 1040h	3C01 8040h

14.3.1.2.2 R5FSS_COMMON0 Registers

R5FSS_COMMON0 Registers

14.3.1.2.2.1 R5FSS_COMMON0_COMPARE_CFG_CCMSR1 Register

14.3.1.2.2.1.1 R5FSS_COMMON0_COMPARE_CFG_CCMSR1 Register (Offset = 0h) [reset = 0h]

Shows the Error and Self test Status of the CPU CPU Compare block.

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Table 14-7568. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 0000h
R5FSS1_COMMON0	05B2 0000h

Figure 14-3764. R5FSS_COMMON0_COMPARE_CFG_CCMSR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED2</td><td>CMPE1</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED1</td><td>STC1</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED0</td><td>STET1</td><td>STE1</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7569. R5FSS_COMMON0_COMPARE_CFG_CCMSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED2	R	0h	This is the Reserved field
16	CMPE1	R/W	0h	This is the CMPE1 field Reset Source: mod_g_rst_n
15:9	RESERVED1	R	0h	This is the Reserved field
8	STC1	R	0h	This is the STC1 field Reset Source: mod_g_rst_n
7:2	RESERVED0	R	0h	This is the Reserved field
1	STET1	R	0h	This is the STET1 field Reset Source: mod_g_rst_n
0	STE1	R	0h	This is the STE1 field Reset Source: mod_g_rst_n

14.3.1.2.2.2 R5FSS_COMMON0_COMPARE_CFG_CCMKEYR1 Register

14.3.1.2.2.2.1 R5FSS_COMMON0_COMPARE_CFG_CCMKEYR1 Register (Offset = 4h) [reset = 0h]

Selects Operating mode of CPU Compare block.

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Table 14-7570. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 0004h
R5FSS1_COMMON0	05B2 0004h

Figure 14-3765. R5FSS_COMMON0_COMPARE_CFG_CCMKEYR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MKEY1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7571. R5FSS_COMMON0_COMPARE_CFG_CCMKEYR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	This is the Reserved field
3:0	MKEY1	R/W	0h	This is the MKEY1 field Reset Source: mod_g_rst_n

14.3.1.2.2.3 R5FSS_COMMON0_COMPARE_CFG_CCMSR2 Register

14.3.1.2.2.3.1 R5FSS_COMMON0_COMPARE_CFG_CCMSR2 Register (Offset = 8h) [reset = 0h]

Shows the Error and Self test Status of the CPU CPU Compare block.

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Table 14-7572. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 0008h
R5FSS1_COMMON0	05B2 0008h

Figure 14-3766. R5FSS_COMMON0_COMPARE_CFG_CCMSR2 Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED2							CMPE2
R							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED1							STC2
R							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED0						STET2	STE2
R						R	R
0h						0h	0h

Table 14-7573. R5FSS_COMMON0_COMPARE_CFG_CCMSR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED2	R	0h	This is the Reserved field
16	CMPE2	R/W	0h	This is the CMPE2 field Reset Source: mod_g_rst_n
15:9	RESERVED1	R	0h	This is the Reserved field
8	STC2	R	0h	This is the STC2 field Reset Source: mod_g_rst_n
7:2	RESERVED0	R	0h	This is the Reserved field
1	STET2	R	0h	This is the STET2 field Reset Source: mod_g_rst_n
0	STE2	R	0h	This is the STE2 field Reset Source: mod_g_rst_n

14.3.1.2.2.4 R5FSS_COMMON0_COMPARE_CFG_CCMKEYR2 Register

14.3.1.2.2.4.1 R5FSS_COMMON0_COMPARE_CFG_CCMKEYR2 Register (Offset = Ch) [reset = 0h]

Selects Operating mode of CPU Compare block.

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Table 14-7574. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 000Ch
R5FSS1_COMMON0	05B2 000Ch

Figure 14-3767. R5FSS_COMMON0_COMPARE_CFG_CCMKEYR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				MKEY2			
R				R/W			
0h				0h			

Table 14-7575. R5FSS_COMMON0_COMPARE_CFG_CCMKEYR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	This is the Reserved field
3:0	MKEY2	R/W	0h	This is the MKEY2 field Reset Source: mod_g_rst_n

14.3.1.2.2.5 R5FSS_COMMON0_COMPARE_CFG_CCMSR3 Register

14.3.1.2.2.5.1 R5FSS_COMMON0_COMPARE_CFG_CCMSR3 Register (Offset = 10h) [reset = 0h]

Shows the Error and Self test Status of the CPU CPU Compare block.

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Table 14-7576. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 0010h
R5FSS1_COMMON0	05B2 0010h

Figure 14-3768. R5FSS_COMMON0_COMPARE_CFG_CCMSR3 Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED2							CMPE3
R							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED1							STC3
R							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED0						STET3	STE3
R						R	R
0h						0h	0h

Table 14-7577. R5FSS_COMMON0_COMPARE_CFG_CCMSR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED2	R	0h	This is the Reserved field
16	CMPE3	R/W	0h	This is the CMPE3 field Reset Source: mod_g_rst_n
15:9	RESERVED1	R	0h	This is the Reserved field
8	STC3	R	0h	This is the STC3 field Reset Source: mod_g_rst_n
7:2	RESERVED0	R	0h	This is the Reserved field
1	STET3	R	0h	This is the STET3 field Reset Source: mod_g_rst_n
0	STE3	R	0h	This is the STE3 field Reset Source: mod_g_rst_n

14.3.1.2.2.6 R5FSS_COMMON0_COMPARE_CFG_CCMKEYR3 Register

14.3.1.2.2.6.1 R5FSS_COMMON0_COMPARE_CFG_CCMKEYR3 Register (Offset = 14h) [reset = 0h]

Selects Operating mode of CPU Compare block.

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Table 14-7578. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 0014h
R5FSS1_COMMON0	05B2 0014h

Figure 14-3769. R5FSS_COMMON0_COMPARE_CFG_CCMKEYR3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				MKEY3			
R				R/W			
0h				0h			

Table 14-7579. R5FSS_COMMON0_COMPARE_CFG_CCMKEYR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	This is the Reserved field
3:0	MKEY3	R/W	0h	This is the MKEY3 field Reset Source: mod_g_rst_n

14.3.1.2.2.7 R5FSS_COMMON0_COMPARE_CFG_CCMPOLCNTRL Register

14.3.1.2.2.7.1 R5FSS_COMMON0_COMPARE_CFG_CCMPOLCNTRL Register (Offset = 18h) [reset = 0h]

Selects Operating mode of CPU Compare block.

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Table 14-7580. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 0018h
R5FSS1_COMMON0	05B2 0018h

Figure 14-3770. R5FSS_COMMON0_COMPARE_CFG_CCMPOLCNTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
POL_INV							
R/W							
0h							

Table 14-7581. R5FSS_COMMON0_COMPARE_CFG_CCMPOLCNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	This is the Reserved field
7:0	POL_INV	R/W	0h	This is the Polarity Inversion field Reset Source: mod_g_rst_n

14.3.1.2.2.8 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register

14.3.1.2.2.8.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register (Offset = 0h) [reset = 0h]

This register contains config bits to enable or disable change requests added to the IP

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Table 14-7582. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1000h
R5FSS1_COMMON0	05B2 1000h
WKUP_R5FSS0_COMMON0	3C01 8000h

Figure 14-3771. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							COMBINE_TCM_LOCKSTEP_MODE
NONE							R/W
0h							0h

Table 14-7583. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_DISABLE_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	COMBINE_TCM_LOCKSTEP_MODE	R/W	0h	this bit disables the CR logic to combine TCM in lockstep mode Reset Source: mod_g_rst_n

14.3.1.2.2.9 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register

14.3.1.2.2.9.1

R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register (Offset = 4h) [reset = 0h]

Status bits showing the PULSAR CPU0 EVNT_BUS single bit error counters

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Table 14-7584. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1004h
R5FSS1_COMMON0	05B2 1004h
WKUP_R5FSS0_COMMON0	3C01 8004h

Figure 14-3772. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EVNT_BUS8	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
EVNT_BUS7		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-7585. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	EVNT_BUS8	R	0h	Status bits showing the PULSAR CPU0 EVNT 8 single bit error counter. Reset Source: mod_g_rst_n
15:14	EVNT_BUS7	R	0h	Status bits showing the PULSAR CPU0 EVNT 7 single bit error counter. Reset Source: mod_g_rst_n
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU0 EVNT 6 single bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU0 EVNT 5 single bit error counter. Reset Source: mod_g_rst_n

Table 14-7585. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU0 EVNT 4 single bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU0 EVNT 3 single bit error counter. Reset Source: mod_g_rst_n
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU0 EVNT 2 single bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU0 EVNT 1 single bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU0 EVNT 0 single bit error counter. Reset Source: mod_g_rst_n

14.3.1.2.2.10 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register

14.3.1.2.2.10.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register (Offset = 8h) [reset = 0h]

Status bits showing the PULSAR CPU1 EVNT_BUS single bit error counters

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Table 14-7586. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1008h
R5FSS1_COMMON0	05B2 1008h
WKUP_R5FSS0_COMMON0	3C01 8008h

Figure 14-3773. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EVNT_BUS8	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
EVNT_BUS7		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
R		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-7587. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:16	EVNT_BUS8	R	0h	Status bits showing the PULSAR CPU1 EVNT 8 single bit error counter. Reset Source: mod_g_rst_n
15:14	EVNT_BUS7	R	0h	Status bits showing the PULSAR CPU1 EVNT 7 single bit error counter. Reset Source: mod_g_rst_n
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU1 EVNT 6 single bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU1 EVNT 5 single bit error counter. Reset Source: mod_g_rst_n

Table 14-7587. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_SB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU1 EVNT 4 single bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU1 EVNT 3 single bit error counter. Reset Source: mod_g_rst_n
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU1 EVNT 2 single bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU1 EVNT 1 single bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU1 EVNT 0 single bit error counter. Reset Source: mod_g_rst_n

14.3.1.2.2.11 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register

14.3.1.2.2.11.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register (Offset = Ch) [reset = 0h]

Status bits showing the PULSAR CPU0 EVNT_BUS multi bit error counters

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Table 14-7588. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 100Ch
R5FSS1_COMMON0	05B2 100Ch
WKUP_R5FSS0_COMMON0	3C01 800Ch

Figure 14-3774. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
NONE		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-7589. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU0 EVNT 6 multi bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU0 EVNT 5 multi bit error counter. Reset Source: mod_g_rst_n
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU0 EVNT 4 multi bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU0 EVNT 3 multi bit error counter. Reset Source: mod_g_rst_n

Table 14-7589. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU0_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU0 EVNT 2 multi bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU0 EVNT 1 multi bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU0 EVNT 0 multi bit error counter. Reset Source: mod_g_rst_n

14.3.1.2.2.12 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register

14.3.1.2.2.12.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register (Offset = 10h) [reset = 0h]

Status bits showing the PULSAR CPU1 EVNT_BUS multi bit error counters

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Table 14-7590. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1010h
R5FSS1_COMMON0	05B2 1010h
WKUP_R5FSS0_COMMON0	3C01 8010h

Figure 14-3775. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		EVNT_BUS6		EVNT_BUS5		EVNT_BUS4	
NONE		R		R		R	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
EVNT_BUS3		EVNT_BUS2		EVNT_BUS1		EVNT_BUS0	
R		R		R		R	
0h		0h		0h		0h	

Table 14-7591. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	EVNT_BUS6	R	0h	Status bits showing the PULSAR CPU1 EVNT 6 multi bit error counter. Reset Source: mod_g_rst_n
11:10	EVNT_BUS5	R	0h	Status bits showing the PULSAR CPU1 EVNT 5 multi bit error counter. Reset Source: mod_g_rst_n
9:8	EVNT_BUS4	R	0h	Status bits showing the PULSAR CPU1 EVNT 4 multi bit error counter. Reset Source: mod_g_rst_n
7:6	EVNT_BUS3	R	0h	Status bits showing the PULSAR CPU1 EVNT 3 multi bit error counter. Reset Source: mod_g_rst_n

Table 14-7591. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_CPU1_EVNT_BUS_MB_ERR_CNT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	EVNT_BUS2	R	0h	Status bits showing the PULSAR CPU1 EVNT 2 multi bit error counter. Reset Source: mod_g_rst_n
3:2	EVNT_BUS1	R	0h	Status bits showing the PULSAR CPU1 EVNT 1 multi bit error counter. Reset Source: mod_g_rst_n
1:0	EVNT_BUS0	R	0h	Status bits showing the PULSAR CPU1 EVNT 0 multi bit error counter. Reset Source: mod_g_rst_n

14.3.1.2.2.13 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register

14.3.1.2.2.13.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register (Offset = 14h) [reset = 0h]

ESM status bits for the PULSAR EVNT BUS

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Table 14-7592. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1014h
R5FSS1_COMMON0	05B2 1014h
WKUP_R5FSS0_COMMON0	3C01 8014h

Figure 14-3776. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-7593. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R	0h	ESM status of CPU1 multiple bit errors on EVNT BUS Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R	0h	ESM status of CPU1 single bit errors on EVNT BUS Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R	0h	ESM status of CPU0 multiple bit errors on EVNT BUS Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R	0h	ESM status of CPU0 single bit errors on EVNT BUS Reset Source: mod_g_rst_n

14.3.1.2.2.14 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register

14.3.1.2.2.14.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register (Offset = 18h) [reset = 0h]

SET the PULSAR EVNT BUS ESM events

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Table 14-7594. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1018h
R5FSS1_COMMON0	05B2 1018h
WKUP_R5FSS0_COMMON0	3C01 8018h

Figure 14-3777. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7595. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TS	0h	SET CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TS	0h	SET CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TS	0h	SET CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TS	0h	SET CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.1.2.2.15 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register

14.3.1.2.2.15.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register (Offset = 1Ch) [reset = 0h]

RESET the PULSAR EVNT BUS ESM events

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Table 14-7596. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 101Ch
R5FSS1_COMMON0	05B2 101Ch
WKUP_R5FSS0_COMMON0	3C01 801Ch

Figure 14-3778. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Name Register

31	30	29	28	27	26	25	24
CPU1_EB6_MULTIPLE_BIT_ERROR	CPU1_EB5_MULTIPLE_BIT_ERROR	CPU1_EB4_MULTIPLE_BIT_ERROR	CPU1_EB3_MULTIPLE_BIT_ERROR	CPU1_EB2_MULTIPLE_BIT_ERROR	CPU1_EB1_MULTIPLE_BIT_ERROR	CPU1_EB0_MULTIPLE_BIT_ERROR	CPU1_EB8_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CPU1_EB7_SINGLE_BIT_ERROR	CPU1_EB6_SINGLE_BIT_ERROR	CPU1_EB5_SINGLE_BIT_ERROR	CPU1_EB4_SINGLE_BIT_ERROR	CPU1_EB3_SINGLE_BIT_ERROR	CPU1_EB2_SINGLE_BIT_ERROR	CPU1_EB1_SINGLE_BIT_ERROR	CPU1_EB0_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_EB6_MULTIPLE_BIT_ERROR	CPU0_EB5_MULTIPLE_BIT_ERROR	CPU0_EB4_MULTIPLE_BIT_ERROR	CPU0_EB3_MULTIPLE_BIT_ERROR	CPU0_EB2_MULTIPLE_BIT_ERROR	CPU0_EB1_MULTIPLE_BIT_ERROR	CPU0_EB0_MULTIPLE_BIT_ERROR	CPU0_EB8_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_EB7_SINGLE_BIT_ERROR	CPU0_EB6_SINGLE_BIT_ERROR	CPU0_EB5_SINGLE_BIT_ERROR	CPU0_EB4_SINGLE_BIT_ERROR	CPU0_EB3_SINGLE_BIT_ERROR	CPU0_EB2_SINGLE_BIT_ERROR	CPU0_EB1_SINGLE_BIT_ERROR	CPU0_EB0_SINGLE_BIT_ERROR
R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD	R/W1TD
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7597. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPU1_EB6_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 31 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
30	CPU1_EB5_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 30 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
29	CPU1_EB4_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 29 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
28	CPU1_EB3_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 28 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n

Table 14-7597. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CPU1_EB2_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 27 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
26	CPU1_EB1_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 26 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
25	CPU1_EB0_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 25 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
24	CPU1_EB8_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 24 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
23	CPU1_EB7_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 23 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
22	CPU1_EB6_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 22 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
21	CPU1_EB5_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 21 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
20	CPU1_EB4_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 20 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
19	CPU1_EB3_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 19 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
18	CPU1_EB2_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 18 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
17	CPU1_EB1_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 17 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
16	CPU1_EB0_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU1 Event Bus 16 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
15	CPU0_EB6_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 15 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
14	CPU0_EB5_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 14 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
13	CPU0_EB4_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 13 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
12	CPU0_EB3_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 12 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
11	CPU0_EB2_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 11 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
10	CPU0_EB1_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 10 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
9	CPU0_EB0_MULTIPLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 9 MULTIPLE BIT Error Counter Reset Source: mod_g_rst_n
8	CPU0_EB8_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 8 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
7	CPU0_EB7_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 7 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
6	CPU0_EB6_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 6 SINGLE BIT Error Counter Reset Source: mod_g_rst_n

Table 14-7597. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_ESM_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CPU0_EB5_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 5 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
4	CPU0_EB4_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 4 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
3	CPU0_EB3_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 3 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
2	CPU0_EB2_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 2 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
1	CPU0_EB1_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 1 SINGLE BIT Error Counter Reset Source: mod_g_rst_n
0	CPU0_EB0_SINGLE_BIT_ERROR	R/W1TD	0h	Decrement CPU0 Event Bus 0 SINGLE BIT Error Counter Reset Source: mod_g_rst_n

14.3.1.2.2.16 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register

14.3.1.2.2.16.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register (Offset = 20h) [reset = 0h]

MASK the PULSAR EVNT BUS ESM events

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Table 14-7598. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1020h
R5FSS1_COMMON0	05B2 1020h
WKUP_R5FSS0_COMMON0	3C01 8020h

Figure 14-3779. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-7599. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TS	0h	MASK CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TS	0h	MASK CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TS	0h	MASK CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TS	0h	MASK CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.1.2.2.17 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register

14.3.1.2.2.17.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register (Offset = 24h) [reset = 0h]

UNMASK the PULSAR EVNT BUS ESM events

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Table 14-7600. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1024h
R5FSS1_COMMON0	05B2 1024h
WKUP_R5FSS0_COMMON0	3C01 8024h

Figure 14-3780. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPU1_MULTIPLE_BIT_ERROR	CPU1_SINGLE_BIT_ERROR	CPU0_MULTIPLE_BIT_ERROR	CPU0_SINGLE_BIT_ERROR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-7601. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVNT_BUS_MASK_ESM_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPU1_MULTIPLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU1 multiple bit errors ESM event Reset Source: mod_g_rst_n
2	CPU1_SINGLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU1 single bit errors ESM event Reset Source: mod_g_rst_n
1	CPU0_MULTIPLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU0 multiple bit error ESM event Reset Source: mod_g_rst_n
0	CPU0_SINGLE_BIT_ERROR	R/W1TC	0h	UNMASK CPU0 single bit error ESM event Reset Source: mod_g_rst_n

14.3.1.2.2.18 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register

14.3.1.2.2.18.1 R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register (Offset = 40h) [reset = 60800103h]

Module ID register

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Table 14-7602. Instance Table

Instance Name	Physical Address
R5FSS0_COMMON0	05B0 1040h
R5FSS1_COMMON0	05B2 1040h
WKUP_R5FSS0_COMMON0	3C01 8040h

Figure 14-3781. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6080h							
23	22	21	20	19	18	17	16
MODID							
R							
6080h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
0h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		3h					

Table 14-7603. R5FSS_COMMON0_EVNT_BUS_VBUSP_MMRS_PULSAR_EVT_BUS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6080h	Module ID field Reset Source: mod_g_rst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release Reset Source: mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	REVMIN	R	3h	Minor revision Reset Source: mod_g_rst_n

14.3.1.3 rl2_of_cba4

rl2_of_cba4

14.3.1.3.1 rl2_of_cba4 Summaries

rl2_of_cba4 Summaries

Table 14-7604. RL2_OF_CBA4 Registers, Base Address=2500 0000h, Length=1024

Offset	Length	Register Name	RL2_0 Physical Address	RL2_0 Physical Address	RL2_2 Physical Address
0h	32	RL2_OF_CBA4_MOD_VER	2500 0000h	2500 1000h	2500 2000h
4h	32	RL2_OF_CBA4_L2_CTRL	2500 0004h	2500 1004h	2500 2004h
8h	32	RL2_OF_CBA4_L2_STS	2500 0008h	2500 1008h	2500 2008h
10h	32	RL2_OF_CBA4_L2_LO_LSW	2500 0010h	2500 1010h	2500 2010h
14h	32	RL2_OF_CBA4_L2_LO_MSW	2500 0014h	2500 1014h	2500 2014h
18h	32	RL2_OF_CBA4_L2_HI	2500 0018h	2500 1018h	2500 2018h
1Ch	32	RL2_OF_CBA4_L2_HI_MSW	2500 001Ch	2500 101Ch	2500 201Ch
78h	32	RL2_OF_CBA4_L2HC	2500 0078h	2500 1078h	2500 2078h
7Ch	32	RL2_OF_CBA4_L2MC	2500 007Ch	2500 107Ch	2500 207Ch
80h	32	RL2_OF_CBA4_IRQSTATUS_RAW	2500 0080h	2500 1080h	2500 2080h
84h	32	RL2_OF_CBA4_IRQSTATUS_MSK	2500 0084h	2500 1084h	2500 2084h
88h	32	RL2_OF_CBA4_IRQENABLE_SET	2500 0088h	2500 1088h	2500 2088h
8Ch	32	RL2_OF_CBA4_IRQENABLE_CLR	2500 008Ch	2500 108Ch	2500 208Ch
104h	32	RL2_OF_CBA4_FLC_CFG	2500 0104h	2500 1104h	2500 2104h
108h	32	RL2_OF_CBA4_FLC_STS	2500 0108h	2500 1108h	2500 2108h
110h	32	RL2_OF_CBA4_FLC_DBG0	2500 0110h	2500 1110h	2500 2110h
114h	32	RL2_OF_CBA4_FLC_DBG1	2500 0114h	2500 1114h	2500 2114h
118h	32	RL2_OF_CBA4_FLC_DBG2	2500 0118h	2500 1118h	2500 2118h
204h	32	RL2_OF_CBA4_RAT_CFG	2500 0204h	2500 1204h	2500 2204h
300h	32	RL2_OF_CBA4_TRK0_LO	2500 0300h	2500 1300h	2500 2300h
304h	32	RL2_OF_CBA4_TRK0_LO_MSW	2500 0304h	2500 1304h	2500 2304h
308h	32	RL2_OF_CBA4_TRK0_HI	2500 0308h	2500 1308h	2500 2308h
30Ch	32	RL2_OF_CBA4_TRK0_HI_MSW	2500 030Ch	2500 130Ch	2500 230Ch
310h	32	RL2_OF_CBA4_TRK0_CTL	2500 0310h	2500 1310h	2500 2310h
20h	32	RL2_OF_CBA4_REM_ADR	2500 0020h + formula	2500 1020h + formula	2500 2020h + formula
24h	32	RL2_OF_CBA4_REM_ADR_MSW	2500 0024h + formula	2500 1024h + formula	2500 2024h + formula
28h	32	RL2_OF_CBA4_REM_LEN	2500 0028h + formula	2500 1028h + formula	2500 2028h + formula
120h	32	RL2_OF_CBA4_FLC_LO_J	2500 0120h + formula	2500 1120h + formula	2500 2120h + formula
124h	32	RL2_OF_CBA4_FLC_LO_MSW_J	2500 0124h + formula	2500 1124h + formula	2500 2124h + formula
128h	32	RL2_OF_CBA4_FLC_HI_J	2500 0128h + formula	2500 1128h + formula	2500 2128h + formula
12Ch	32	RL2_OF_CBA4_FLC_HI_MSW_J	2500 012Ch + formula	2500 112Ch + formula	2500 212Ch + formula
130h	32	RL2_OF_CBA4_FLC_RA_J	2500 0130h + formula	2500 1130h + formula	2500 2130h + formula
134h	32	RL2_OF_CBA4_FLC_RA_MSW_J	2500 0134h + formula	2500 1134h + formula	2500 2134h + formula
138h	32	RL2_OF_CBA4_FLC_CTL_J	2500 0138h + formula	2500 1138h + formula	2500 2138h + formula

Table 14-7605. RL2_OF_CBA4 Registers, Base Address=2500 0000h, Length=1024

Offset	Length	Register Name	RL2_3 Physical Address
0h	32	RL2_OF_CBA4_MOD_VER	2500 3000h
4h	32	RL2_OF_CBA4_L2_CTRL	2500 3004h

Table 14-7605. RL2_OF_CBA4 Registers, Base Address=2500 0000h, Length=1024 (continued)

Offset	Length	Register Name	RL2_3 Physical Address
8h	32	RL2_OF_CBA4_L2_STS	2500 3008h
10h	32	RL2_OF_CBA4_L2_LO_LSW	2500 3010h
14h	32	RL2_OF_CBA4_L2_LO_MSW	2500 3014h
18h	32	RL2_OF_CBA4_L2_HI	2500 3018h
1Ch	32	RL2_OF_CBA4_L2_HI_MSW	2500 301Ch
78h	32	RL2_OF_CBA4_L2HC	2500 3078h
7Ch	32	RL2_OF_CBA4_L2MC	2500 307Ch
80h	32	RL2_OF_CBA4_IRQSTATUS_RAW	2500 3080h
84h	32	RL2_OF_CBA4_IRQSTATUS_MSK	2500 3084h
88h	32	RL2_OF_CBA4_IRQENABLE_SET	2500 3088h
8Ch	32	RL2_OF_CBA4_IRQENABLE_CLR	2500 308Ch
104h	32	RL2_OF_CBA4_FLC_CFG	2500 3104h
108h	32	RL2_OF_CBA4_FLC_STS	2500 3108h
110h	32	RL2_OF_CBA4_FLC_DBG0	2500 3110h
114h	32	RL2_OF_CBA4_FLC_DBG1	2500 3114h
118h	32	RL2_OF_CBA4_FLC_DBG2	2500 3118h
204h	32	RL2_OF_CBA4_RAT_CFG	2500 3204h
300h	32	RL2_OF_CBA4_TRK0_LO	2500 3300h
304h	32	RL2_OF_CBA4_TRK0_LO_MSW	2500 3304h
308h	32	RL2_OF_CBA4_TRK0_HI	2500 3308h
30Ch	32	RL2_OF_CBA4_TRK0_HI_MSW	2500 330Ch
310h	32	RL2_OF_CBA4_TRK0_CTL	2500 3310h
20h	32	RL2_OF_CBA4_REM_ADR	2500 3020h + formula
24h	32	RL2_OF_CBA4_REM_ADR_MSW	2500 3024h + formula
28h	32	RL2_OF_CBA4_REM_LEN	2500 3028h + formula
120h	32	RL2_OF_CBA4_FLC_LO_J	2500 3120h + formula
124h	32	RL2_OF_CBA4_FLC_LO_MSW_J	2500 3124h + formula
128h	32	RL2_OF_CBA4_FLC_HI_J	2500 3128h + formula
12Ch	32	RL2_OF_CBA4_FLC_HI_MSW_J	2500 312Ch + formula
130h	32	RL2_OF_CBA4_FLC_RA_J	2500 3130h + formula
134h	32	RL2_OF_CBA4_FLC_RA_MSW_J	2500 3134h + formula
138h	32	RL2_OF_CBA4_FLC_CTL_J	2500 3138h + formula

14.3.1.3.2 rl2_of_cba4 Registers

rl2_of_cba4 Registers

14.3.1.3.2.1 RL2_OF_CBA4_MOD_VER Register

14.3.1.3.2.1.1 RL2_OF_CBA4_MOD_VER Register (Offset = 0h) [reset = 68840100h]

The Module and Version Register identifies the module identifier and revision of the RL2 module.

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Table 14-7606. Instance Table

Instance Name	Physical Address
RL2_0	2500 0000h
RL2_0	2500 1000h
RL2_2	2500 2000h
RL2_3	2500 3000h

Figure 14-3782. RL2_OF_CBA4_MOD_VER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">884h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">884h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VERSION</td><td colspan="3">MAJOR_REVISION</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM_REVISION</td><td colspan="6">MINOR_REVISION</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-7607. RL2_OF_CBA4_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Module Scheme
29:28	BU	R	2h	Module Business Unit
27:16	MODULE_ID	R	884h	RL2 module ID.
15:11	RTL_VERSION	R	0h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	0h	Minor Revision.

14.3.1.3.2.2 RL2_OF_CBA4_L2_CTRL Register

14.3.1.3.2.2.1 RL2_OF_CBA4_L2_CTRL Register (Offset = 4h) [reset = 0h]

The control register defines the size of the remote cache data storage memory to use and whether the L2 is enabled.

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Table 14-7608. Instance Table

Instance Name	Physical Address
RL2_0	2500 0004h
RL2_0	2500 1004h
RL2_2	2500 2004h
RL2_3	2500 3004h

Figure 14-3783. RL2_OF_CBA4_L2_CTRL Name Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SIZE		
NONE					R/W		
0h					0h		

Table 14-7609. RL2_OF_CBA4_L2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	The ~ienable field determines whether the L2 is enabled or not. Setting the enable from a 0 to 1 restarts the cache 0: Disabled 1: Enabled
30:3	RESERVED	NONE	0h	Reserved
2:0	SIZE	R/W	0h	The ~isize field determines the size of the remote cache data storage memory that is currently active. This field can be change dynamically, but will cause the entire cache to be invalidated when inflight transactions have completed. Changing the ~isize while ~ienable is already a '1' will restart the cache. 0: 8KB 1: 16KB 2: 32KB 3: 64KB 4: 128KB 5: 256KB (Dual Mode) Note: Setting this field to an invalid value will result in the field being set to '0'. The remote address range registers must be setup correctly to ensure it has sufficient memory for the selected size.

14.3.1.3.2.3 RL2_OF_CBA4_L2_STS Register

14.3.1.3.2.3.1 RL2_OF_CBA4_L2_STS Register (Offset = 8h) [reset = 0h]

The Status register displays the state of the RL2 module

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Table 14-7610. Instance Table

Instance Name	Physical Address
RL2_0	2500 0008h
RL2_0	2500 1008h
RL2_2	2500 2008h
RL2_3	2500 3008h

Figure 14-3784. RL2_OF_CBA4_L2_STS Name Register

31	30	29	28	27	26	25	24
OK_TO_GO	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7611. RL2_OF_CBA4_L2_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OK_TO_GO	R	0h	The ~iok_to_go status bit indicates the Tag/LRU Ram has been initialized and the cache is in an operable state.
30:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.4 RL2_OF_CBA4_L2_LO_LSW Register

14.3.1.3.2.4.1 RL2_OF_CBA4_L2_LO_LSW Register (Offset = 10h) [reset = 0h]

The L2 Low address Least Significant word defines the least significant portion of the low cache address. The RL2 cache can cache a range of 1 to 16MB of cache as defined by L2_LO>=CachedRange<=L2_HI. This register is write protected when ~ienable is set.

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Table 14-7612. Instance Table

Instance Name	Physical Address
RL2_0	2500 0010h
RL2_0	2500 1010h
RL2_2	2500 2010h
RL2_3	2500 3010h

Figure 14-3785. RL2_OF_CBA4_L2_LO_LSW Name Register

31	30	29	28	27	26	25	24
ADDRESS_LO_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS_LO_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS_LO_LSW					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7613. RL2_OF_CBA4_L2_LO_LSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	ADDRESS_LO_LSW	R/W	0h	The ~iaddress_lo_lsw defines the L2 low address[31:11] for the RL2 to cache. The remaining bits 10:0 are assumed to be zero.
10:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.5 RL2_OF_CBA4_L2_LO_MSW Register

14.3.1.3.2.5.1 RL2_OF_CBA4_L2_LO_MSW Register (Offset = 14h) [reset = 0h]

The L2 Low address Most Significant word defines the most significant portion of the low cache address. The RL2 cache can cache a range of 1 to 16MB of cache as defined by L2_LO>=CachedRange<=L2_HI. This register is write protected when ~ienable is set.

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Table 14-7614. Instance Table

Instance Name	Physical Address
RL2_0	2500 0014h
RL2_0	2500 1014h
RL2_2	2500 2014h
RL2_3	2500 3014h

Figure 14-3786. RL2_OF_CBA4_L2_LO_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDRESS_LO_MSW							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS_LO_MSW							
R/W							
0h							

Table 14-7615. RL2_OF_CBA4_L2_LO_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDRESS_LO_MSW	R/W	0h	The ~iaddress_lo_msw defines the L2 low address[47:32] for the RL2 to cache.

14.3.1.3.2.6 RL2_OF_CBA4_L2_HI Register

14.3.1.3.2.6.1 RL2_OF_CBA4_L2_HI Register (Offset = 18h) [reset = 0h]

The L2 High address Least Significant word defines the least significant portion of the high cache address. The RL2 cache can cache a range of 1 to 16MB of cache as defined by L2_LO>=CachedRange<=L2_HI. This register is write protected when ~ienable is set.

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Table 14-7616. Instance Table

Instance Name	Physical Address
RL2_0	2500 0018h
RL2_0	2500 1018h
RL2_2	2500 2018h
RL2_3	2500 3018h

Figure 14-3787. RL2_OF_CBA4_L2_HI Name Register

31	30	29	28	27	26	25	24
ADDRESS_HI_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS_HI_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS_HI_LSW					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7617. RL2_OF_CBA4_L2_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	ADDRESS_HI_LSW	R/W	0h	The ~iaddress_hi_lsw defines the high address[31:11] for the RL2 to cache. The remaining bits 10:0 are assumed to be ones.
10:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.7 RL2_OF_CBA4_L2_HI_MSW Register

14.3.1.3.2.7.1 RL2_OF_CBA4_L2_HI_MSW Register (Offset = 1Ch) [reset = 0h]

The L2 Hi address Most Significant word defines the most significant portion of the high cache address. The RL2 cache can cache a range of 1 to 16MB of cache as defined by L2_LO>=CachedRange<=L2_HI. This register is write protected when ~ienable is set.

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Table 14-7618. Instance Table

Instance Name	Physical Address
RL2_0	2500 001Ch
RL2_0	2500 101Ch
RL2_2	2500 201Ch
RL2_3	2500 301Ch

Figure 14-3788. RL2_OF_CBA4_L2_HI_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDRESS_HI_MSW							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDRESS_HI_MSW							
R/W							
0h							

Table 14-7619. RL2_OF_CBA4_L2_HI_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDRESS_HI_MSW	R/W	0h	The ~iaddress_lo_msw defines the L2 hi address[47:32] for the RL2 to cache.

14.3.1.3.2.8 RL2_OF_CBA4_L2HC Register

14.3.1.3.2.8.1 RL2_OF_CBA4_L2HC Register (Offset = 78h) [reset = 0h]

The L2 HIT Counter register holds the number of L2 Hits to the Remote data storage memory.

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Table 14-7620. Instance Table

Instance Name	Physical Address
RL2_0	2500 0078h
RL2_0	2500 1078h
RL2_2	2500 2078h
RL2_3	2500 3078h

Figure 14-3789. RL2_OF_CBA4_L2HC Name Register

31	30	29	28	27	26	25	24
HIT							
R/W							
0h							
23	22	21	20	19	18	17	16
HIT							
R/W							
0h							
15	14	13	12	11	10	9	8
HIT							
R/W							
0h							
7	6	5	4	3	2	1	0
HIT							
R/W							
0h							

Table 14-7621. RL2_OF_CBA4_L2HC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HIT	R/W	0h	The ~ihit Counts the number of hits to the L2 cache. Writing to this register will set the value written or restarting the cache will clear its contents. This field does not roll over, it will stop counting at all ones.

14.3.1.3.2.9 RL2_OF_CBA4_L2MC Register

14.3.1.3.2.9.1 RL2_OF_CBA4_L2MC Register (Offset = 7Ch) [reset = 0h]

The L2 MISS Counter register holds the number of L2 Misses to the Remote data storage memory.

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Table 14-7622. Instance Table

Instance Name	Physical Address
RL2_0	2500 007Ch
RL2_0	2500 107Ch
RL2_2	2500 207Ch
RL2_3	2500 307Ch

Figure 14-3790. RL2_OF_CBA4_L2MC Name Register

31	30	29	28	27	26	25	24
MISS							
R/W							
0h							
23	22	21	20	19	18	17	16
MISS							
R/W							
0h							
15	14	13	12	11	10	9	8
MISS							
R/W							
0h							
7	6	5	4	3	2	1	0
MISS							
R/W							
0h							

Table 14-7623. RL2_OF_CBA4_L2MC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MISS	R/W	0h	The ~imiss Counts the number of misses to the L2 cache. Writing to this register will set the value written or restarting the cache will clear its contents. This field does not roll over, it will stop counting at all ones.

14.3.1.3.2.10 RL2_OF_CBA4_IRQSTATUS_RAW Register

14.3.1.3.2.10.1 RL2_OF_CBA4_IRQSTATUS_RAW Register (Offset = 80h) [reset = 0h]

The Interrupt Raw Status Register holds the raw status of the FLC/RL2 status/error interrupts.

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Table 14-7624. Instance Table

Instance Name	Physical Address
RL2_0	2500 0080h
RL2_0	2500 1080h
RL2_2	2500 2080h
RL2_3	2500 3080h

Figure 14-3791. RL2_OF_CBA4_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			FLC_DON	FLC_WRERR	FLC_RDERR	WR_HIT	WR_ERR
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 14-7625. RL2_OF_CBA4_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	FLC_DON	R/W1TS	0h	The ~iflc_don bit indicates a FLC has completed the transfer to the FLC range. Write 1 to set the ~iflc_don status for diagnostic purposes. Writing a 0 has no effect.
3	FLC_WRERR	R/W1TS	0h	The ~iflc_wrerr bit indicates a write error from FLC remote range has occurred and the FLC is logically disabled while this bit is a '1'. Write 1 to set the ~iflc_wrerr status for diagnostic purposes. Writing a 0 has no effect.
2	FLC_RDERR	R/W1TS	0h	The ~iflc_rderr bit indicates a read error from FLC range has occurred and the FLC is logically disabled while this bit is a '1'. Write 1 to set the ~iflc_rderr status for diagnostic purposes. Writing a 0 has no effect.
1	WR_HIT	R/W1TS	0h	The ~iwr_hit bit indicates a write to the cacheable range has occurred potentially causing a coherency issue and the RL2 is logically disabled while this bit is a '1'. Write 1 to set the ~iwr_hit status for diagnostic purposes. Writing a 0 has no effect.
0	WR_ERR	R/W1TS	0h	The ~iwr_err bit indicates a write error has occurred to the remote cache data storage memory and the RL2 is logically disabled while this bit is a '1'. Write 1 to set the ~iwr_err status for diagnostic purposes. Writing a 0 has no effect.

14.3.1.3.2.11 RL2_OF_CBA4_IRQSTATUS_MSK Register

14.3.1.3.2.11.1 RL2_OF_CBA4_IRQSTATUS_MSK Register (Offset = 84h) [reset = 0h]

The Interrupt Masked Status Register holds the masked status for the FLC/RL2 status/error interrupts. Writing to this register will EOI the interrupt, that is if another interrupt is pending, a new pulse interrupt will be generated.

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Table 14-7626. Instance Table

Instance Name	Physical Address
RL2_0	2500 0084h
RL2_0	2500 1084h
RL2_2	2500 2084h
RL2_3	2500 3084h

Figure 14-3792. RL2_OF_CBA4_IRQSTATUS_MSK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			FLC_DON	FLC_WRERR	FLC_RDERR	WR_HIT	WR_ERR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-7627. RL2_OF_CBA4_IRQSTATUS_MSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	FLC_DON	R/W1TC	0h	The ~iflc_don bit indicates a FLC has completed the transfer to the FLC range. Write 1 to clear the ~iflc_don status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.
3	FLC_WRERR	R/W1TC	0h	The ~iflc_wrerr bit indicates a write error from FLC range has occurred and the FLC is logically disabled while this bit is a '1'. Write 1 to clear the ~iflc_wrerr status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.
2	FLC_RDERR	R/W1TC	0h	The ~iflc_rderr bit indicates a read error from FLC range has occurred and the FLC is logically disabled while this bit is a '1'. Write 1 to clear the ~iflc_rderr status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.
1	WR_HIT	R/W1TC	0h	The ~iwr_hit bit indicates a write to the cacheable range has occurred potentially causing a coherency issue and the RL2 is logically disabled while this bit is a '1'. Write 1 to clear the ~iwr_hit status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.

Table 14-7627. RL2_OF_CBA4_IRQSTATUS_MSK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WR_ERR	R/W1TC	0h	The ~iwr_err bit indicates a write error has occurred to the remote cache data storage memory and the RL2 is logically disabled while this bit is a '1'. Write 1 to clear the ~iwr_err status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.

14.3.1.3.2.12 RL2_OF_CBA4_IRQENABLE_SET Register

14.3.1.3.2.12.1 RL2_OF_CBA4_IRQENABLE_SET Register (Offset = 88h) [reset = 0h]

The Interrupt Enable Set Register holds the interrupt enable status of the FLC/RL2 status/error interrupts.

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Table 14-7628. Instance Table

Instance Name	Physical Address
RL2_0	2500 0088h
RL2_0	2500 1088h
RL2_2	2500 2088h
RL2_3	2500 3088h

Figure 14-3793. RL2_OF_CBA4_IRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EN_FLC_DON	EN_FLC_WRERR	EN_FLC_RDERR	EN_WR_HIT	EN_WR_ERR
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 14-7629. RL2_OF_CBA4_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EN_FLC_DON	R/W1TS	0h	Interrupt Enable Set for ~ien_flc_don status bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
3	EN_FLC_WRERR	R/W1TS	0h	Interrupt Enable Set for ~ien_flc_wrerr error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
2	EN_FLC_RDERR	R/W1TS	0h	Interrupt Enable Set for ~ien_flc_rderr error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
1	EN_WR_HIT	R/W1TS	0h	Interrupt Enable Set for ~iwr_hit error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
0	EN_WR_ERR	R/W1TS	0h	Interrupt Enable Set for ~iwr_err error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

14.3.1.3.2.13 RL2_OF_CBA4_IRQENABLE_CLR Register

14.3.1.3.2.13.1 RL2_OF_CBA4_IRQENABLE_CLR Register (Offset = 8Ch) [reset = 0h]

The Interrupt Enable Clear Register holds the interrupt enable status of the FLC/RL2 status/error interrupts.

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Table 14-7630. Instance Table

Instance Name	Physical Address
RL2_0	2500 008Ch
RL2_0	2500 108Ch
RL2_2	2500 208Ch
RL2_3	2500 308Ch

Figure 14-3794. RL2_OF_CBA4_IRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EN_FLC_DON	EN_FLC_WRERR	EN_FLC_RDERR	EN_WR_HIT	EN_WR_ERR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-7631. RL2_OF_CBA4_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EN_FLC_DON	R/W1TC	0h	Interrupt Enable Clear for ~iflc_don status bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
3	EN_FLC_WRERR	R/W1TC	0h	Interrupt Enable Clear for ~iflc_wrerr error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
2	EN_FLC_RDERR	R/W1TC	0h	Interrupt Enable Clear for ~iflc_rderr error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
1	EN_WR_HIT	R/W1TC	0h	Interrupt Enable Clear for ~iwr_hit error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
0	EN_WR_ERR	R/W1TC	0h	Interrupt Enable Clear for ~iwr_err error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

14.3.1.3.2.14 RL2_OF_CBA4_FLC_CFG Register

14.3.1.3.2.14.1 RL2_OF_CBA4_FLC_CFG Register (Offset = 104h) [reset = 504h]

The FLC Config Register contains the configuration values for the FLC.

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Table 14-7632. Instance Table

Instance Name	Physical Address
RL2_0	2500 0104h
RL2_0	2500 1104h
RL2_2	2500 2104h
RL2_3	2500 3104h

Figure 14-3795. RL2_OF_CBA4_FLC_CFG Name Register

31	30	29	28	27	26	25	24
FIFO_BYPASS	RESERVED				FLC_EXCNT		
R/W	NONE				R/W		
0h	0h				0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ASMNUM							
R							
5h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RANGES							
R							
4h							

Table 14-7633. RL2_OF_CBA4_FLC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FIFO_BYPASS	R/W	0h	Setting this bit will cause the write to remote memory for a cache miss or FLC return to forces stalls on the read returns if any other data phase for a cache miss or FLC return is received. This can cause stalls on the write to force stalls on the read.
30:27	RESERVED	NONE	0h	Reserved
26:24	FLC_EXCNT	R/W	0h	The number of extra requests the FLC can send. The maximum value is 4 anything greater will default to 4. This value + 1 is the number of Reassembly Buffers used for FLC so if cache misses needed to be supported this value should be set to 4 or lower. The number of cache misses that will be allowed to be outstanding while FLC is running will be 5 - (FLC_EXCNT + 1).
23:16	RESERVED	NONE	0h	Reserved
15:8	ASMNUM	R	5h	Number of Reassembly Buffer supported
7:0	RANGES	R	4h	Number of FLC ranges supported

14.3.1.3.2.15 RL2_OF_CBA4_FLC_STS Register

14.3.1.3.2.15.1 RL2_OF_CBA4_FLC_STS Register (Offset = 108h) [reset = 0h]

The FLC Status Register will indicate the state of the FLC completion.

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Table 14-7634. Instance Table

Instance Name	Physical Address
RL2_0	2500 0108h
RL2_0	2500 1108h
RL2_2	2500 2108h
RL2_3	2500 3108h

Figure 14-3796. RL2_OF_CBA4_FLC_STS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CPYCMP</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7635. RL2_OF_CBA4_FLC_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CPYCMP	R	0h	The ~icpycmp indicates which FLC range is complete. Each bit index indicates the FLC range is complete.

14.3.1.3.2.16 RL2_OF_CBA4_FLC_DBG0 Register

14.3.1.3.2.16.1 RL2_OF_CBA4_FLC_DBG0 Register (Offset = 110h) [reset = 0h]

The FLC Debug 0 Register holds the debug state of the FLC.

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Table 14-7636. Instance Table

Instance Name	Physical Address
RL2_0	2500 0110h
RL2_0	2500 1110h
RL2_2	2500 2110h
RL2_3	2500 3110h

Figure 14-3797. RL2_OF_CBA4_FLC_DBG0 Name Register

31	30	29	28	27	26	25	24
FLCIF	RESERVED				FLC_OUT_CNT		
R	NONE				R		
0h	0h				0h		
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CURFLC	
NONE						R	
0h						0h	

Table 14-7637. RL2_OF_CBA4_FLC_DBG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FLCIF	R	0h	The ~iflcif indicates a FLC operation is in flight.
30:27	RESERVED	NONE	0h	Reserved
26:24	FLC_OUT_CNT	R	0h	The number of read requests the FLC operation has in flight.
23:2	RESERVED	NONE	0h	Reserved
1:0	CURFLC	R	0h	The ~icurflc indicates which FLC range is in flight.

14.3.1.3.2.17 RL2_OF_CBA4_FLC_DBG1 Register

14.3.1.3.2.17.1 RL2_OF_CBA4_FLC_DBG1 Register (Offset = 114h) [reset = 0h]

The FLC Debug 1 Register holds the debug address of the FLC.

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Table 14-7638. Instance Table

Instance Name	Physical Address
RL2_0	2500 0114h
RL2_0	2500 1114h
RL2_2	2500 2114h
RL2_3	2500 3114h

Figure 14-3798. RL2_OF_CBA4_FLC_DBG1 Name Register

31	30	29	28	27	26	25	24
FLCADR_LO							
R							
0h							
23	22	21	20	19	18	17	16
FLCADR_LO							
R							
0h							
15	14	13	12	11	10	9	8
FLCADR_LO							
R							
0h							
7	6	5	4	3	2	1	0
FLCADR_LO							
R							
0h							

Table 14-7639. RL2_OF_CBA4_FLC_DBG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FLCADR_LO	R	0h	The ~iflcadr indicates the next FLC address to be processed if still in flight. That is all addresses less than this address have been transferred. This address is used for FLC hit when the particular FLC range is in flight. That is FLC_LO?>=FLCrange<~iflc_dbg1.flcadr would result in a hit. This address will match the last FLC transferred FLC_HI? when no FLC ranges are in flight.

14.3.1.3.2.18 RL2_OF_CBA4_FLC_DBG2 Register

14.3.1.3.2.18.1 RL2_OF_CBA4_FLC_DBG2 Register (Offset = 118h) [reset = 0h]

The FLC Debug 2 Register holds the upper portion of the debug address of the FLC.

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Table 14-7640. Instance Table

Instance Name	Physical Address
RL2_0	2500 0118h
RL2_0	2500 1118h
RL2_2	2500 2118h
RL2_3	2500 3118h

Figure 14-3799. RL2_OF_CBA4_FLC_DBG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
FLCADR_HI							
R							
0h							
7	6	5	4	3	2	1	0
FLCADR_HI							
R							
0h							

Table 14-7641. RL2_OF_CBA4_FLC_DBG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	FLCADR_HI	R	0h	The ~iflcadr indicates the next FLC address to be processed if still in flight. That is all addresses less than this address have been transferred. This address is used for FLC hit when the particular FLC range is in flight. That is FLC_LO?>=FLCrange<~iflc_dbg1.flcadr would result in a hit. This address will match the last FLC transferred FLC_HI? when no FLC ranges are in flight.

14.3.1.3.2.19 RL2_OF_CBA4_RAT_CFG Register

14.3.1.3.2.19.1 RL2_OF_CBA4_RAT_CFG Register (Offset = 204h) [reset = 200000h]

The RAT Config Register contains the configuration values for the RAT.

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Table 14-7642. Instance Table

Instance Name	Physical Address
RL2_0	2500 0204h
RL2_0	2500 1204h
RL2_2	2500 2204h
RL2_3	2500 3204h

Figure 14-3800. RL2_OF_CBA4_RAT_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
ADDR_WIDTH							
R							
20h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REGIONS							
R							
0h							

Table 14-7643. RL2_OF_CBA4_RAT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	ADDR_WIDTH	R	20h	Number of address bits
15:8	RESERVED	NONE	0h	Reserved
7:0	REGIONS	R	0h	Number of regions

14.3.1.3.2.20 RL2_OF_CBA4_TRK0_LO Register

14.3.1.3.2.20.1 RL2_OF_CBA4_TRK0_LO Register (Offset = 300h) [reset = 0h]

The Track Low 0 address defines the Track lo address for Track range 0. The Track range is defined by TRK_LO0>=TRKrange<TRK_HI0, if a read is in this range then while it is outstanding the trk0_active pin will be asserted. This register is write protected when ~trk_ifenable0 is set.

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Table 14-7644. Instance Table

Instance Name	Physical Address
RL2_0	2500 0300h
RL2_0	2500 1300h
RL2_2	2500 2300h
RL2_3	2500 3300h

Figure 14-3801. RL2_OF_CBA4_TRK0_LO Name Register

31	30	29	28	27	26	25	24
TRK0_ADR_LO_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
TRK0_ADR_LO_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
TRK0_ADR_LO_LSW				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7645. RL2_OF_CBA4_TRK0_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	TRK0_ADR_LO_LSW	R/W	0h	The ~trk0_adr_lo defines the TRK low address[31:12] for the Tracking function. The remaining bits 11:0 are assumed to be zero.
11:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.21 RL2_OF_CBA4_TRK0_LO_MSW Register

14.3.1.3.2.21.1 RL2_OF_CBA4_TRK0_LO_MSW Register (Offset = 304h) [reset = 0h]

The Track Low 0 address defines the Track lo address for Track range 0. The Track range is defined by TRK_LO0>=TRKrange<TRK_HI0, if a read is in this range then while it is outstanding the trk0_active pin will be asserted. This register is write protected when ~trk_ifenable0 is set.

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Table 14-7646. Instance Table

Instance Name	Physical Address
RL2_0	2500 0304h
RL2_0	2500 1304h
RL2_2	2500 2304h
RL2_3	2500 3304h

Figure 14-3802. RL2_OF_CBA4_TRK0_LO_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TRK0_ADR_LO_MSW							
R/W							
0h							
7	6	5	4	3	2	1	0
TRK0_ADR_LO_MSW							
R/W							
0h							

Table 14-7647. RL2_OF_CBA4_TRK0_LO_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TRK0_ADR_LO_MSW	R/W	0h	The ~iadr0_lo defines the TRK low address[47:32] for the Tracking Function

14.3.1.3.2.22 RL2_OF_CBA4_TRK0_HI Register

14.3.1.3.2.22.1 RL2_OF_CBA4_TRK0_HI Register (Offset = 308h) [reset = 0h]

The Track High 0 address defines the Track High address for Track range 0. The Track range is defined by TRK_LO0>=TRKrange<TRK_HI0, if a read is in this range then while it is outstanding the trk0_active pin will be asserted. This register is write protected when ~trk_ifenable0 is set.

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Table 14-7648. Instance Table

Instance Name	Physical Address
RL2_0	2500 0308h
RL2_0	2500 1308h
RL2_2	2500 2308h
RL2_3	2500 3308h

Figure 14-3803. RL2_OF_CBA4_TRK0_HI Name Register

31	30	29	28	27	26	25	24
TRK0_ADR_HI_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
TRK0_ADR_HI_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
TRK0_ADR_HI_LSW				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7649. RL2_OF_CBA4_TRK0_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	TRK0_ADR_HI_LSW	R/W	0h	The ~trk0_hi defines the TRK low address[31:12] for the Tracking function. The remaining bits 11:0 are assumed to be zero.
11:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.23 RL2_OF_CBA4_TRK0_HI_MSW Register

14.3.1.3.2.23.1 RL2_OF_CBA4_TRK0_HI_MSW Register (Offset = 30Ch) [reset = 0h]

The Track Hi 0 address defines the Track hi address for Track range 0. The Track range is defined by TRK_LO0>=TRKrange<TRK_HI0, if a read is in this range then while it is outstanding the trk0_active pin will be asserted. This register is write protected when ~trk_ifenable0 is set.

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Table 14-7650. Instance Table

Instance Name	Physical Address
RL2_0	2500 030Ch
RL2_0	2500 130Ch
RL2_2	2500 230Ch
RL2_3	2500 330Ch

Figure 14-3804. RL2_OF_CBA4_TRK0_HI_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TRK0_ADR_HI_MSW							
R/W							
0h							
7	6	5	4	3	2	1	0
TRK0_ADR_HI_MSW							
R/W							
0h							

Table 14-7651. RL2_OF_CBA4_TRK0_HI_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TRK0_ADR_HI_MSW	R/W	0h	The ~iadr0_lo defines the TRK low address[47:32] for the Tracking Function

14.3.1.3.2.24 RL2_OF_CBA4_TRK0_CTL Register

14.3.1.3.2.24.1 RL2_OF_CBA4_TRK0_CTL Register (Offset = 310h) [reset = 0h]

The Track Control 0 enables the given range TRK_LO0>=TRKrange<TRK_HI0 to generate the output on trk0_active pin.

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Table 14-7652. Instance Table

Instance Name	Physical Address
RL2_0	2500 0310h
RL2_0	2500 1310h
RL2_2	2500 2310h
RL2_3	2500 3310h

Figure 14-3805. RL2_OF_CBA4_TRK0_CTL Name Register

31	30	29	28	27	26	25	24
TRK0_FENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-7653. RL2_OF_CBA4_TRK0_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK0_FENABLE	R/W	0h	The ~ifenable0 enables the TRL_LO0>=TRKrange<TRK_HI0 to assert the output pin trk0_active. if the ~ifenable0 is set to zero, the range is disabled and the output will remain low.
30:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.25 RL2_OF_CBA4_REM_ADR Register

14.3.1.3.2.25.1 RL2_OF_CBA4_REM_ADR Register (Offset = 20h) [reset = 0h]

The REMote 'n' Address Least Significant word defines the least significant portion of the Remote address for remote cache data storage memory 0. The RL2 cache use up to three remote cache data storage memory ranges to place the L2 data within. The length of these ranges must be greater or equal to the size specified. This register is write protected when ~ienable is set.

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Table 14-7654. Instance Table

Instance Name	Physical Address
RL2_0	2500 0020h + formula
RL2_0	2500 1020h + formula
RL2_2	2500 2020h + formula
RL2_3	2500 3020h + formula

Figure 14-3806. RL2_OF_CBA4_REM_ADR Name Register

31	30	29	28	27	26	25	24
ADR_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
ADR_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
ADR_LSW					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7655. RL2_OF_CBA4_REM_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	ADR_LSW	R/W	0h	The ~irem0_adr_lsw defines the LSW of the remote cache data storage memory address[31:11] range 'n' for the RL2 to use for the cache. The remaining bits 10:0 are assumed to be zero.
10:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.26 RL2_OF_CBA4_REM_ADR_MSW Register

14.3.1.3.2.26.1 RL2_OF_CBA4_REM_ADR_MSW Register (Offset = 24h) [reset = 0h]

The REMote 'n' Address Most Significant word defines the Most significant portion of the Remote address for remote cache data storage memory 0. The RL2 cache use up to three remote cache data storage memory ranges to place the L2 data within. The length of these ranges must be greater or equal to the size specified. This register is write protected when ~ienable is set.

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Table 14-7656. Instance Table

Instance Name	Physical Address
RL2_0	2500 0024h + formula
RL2_0	2500 1024h + formula
RL2_2	2500 2024h + formula
RL2_3	2500 3024h + formula

Figure 14-3807. RL2_OF_CBA4_REM_ADR_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADR_MSW							
R/W							
0h							
7	6	5	4	3	2	1	0
ADR_MSW							
R/W							
0h							

Table 14-7657. RL2_OF_CBA4_REM_ADR_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADR_MSW	R/W	0h	The ~irem0_adr_lsw defines the LSW of the remote cache data storage memory address[47:32] range 'n' for the RL2 to use for the cache.

14.3.1.3.2.27 RL2_OF_CBA4_REM_LEN Register

14.3.1.3.2.27.1 RL2_OF_CBA4_REM_LEN Register (Offset = 28h) [reset = 0h]

The Remote 'n' length defines the amount of remote cache data storage memory in 64 byte aligned quanta used starting from the REMote 'n' Address. The RL2 consumes remote cache data storage memory ranges in numeric order. Range 0 is consumed prior to range 1, etc. This register is write protected when ~ienable is set.

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Table 14-7658. Instance Table

Instance Name	Physical Address
RL2_0	2500 0028h + formula
RL2_0	2500 1028h + formula
RL2_2	2500 2028h + formula
RL2_3	2500 3028h + formula

Figure 14-3808. RL2_OF_CBA4_REM_LEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					LEN		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
LEN							
R/W							
0h							
7	6	5	4	3	2	1	0
LEN		RESERVED					
R/W		NONE					
0h		0h					

Table 14-7659. RL2_OF_CBA4_REM_LEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:6	LEN	R/W	0h	The ~irem0_len field specifies the length of the remote cache data storage memory 'n' to use for the RL2 cache in 64 byte quanta, That is the number of bytes specified in the remote cache data storage memory range 'n' is (~irem0_len X 64). Note: Any value greater than 4096 assumes 4096
5:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.28 RL2_OF_CBA4_FLC_LO_J Register

14.3.1.3.2.28.1 RL2_OF_CBA4_FLC_LO_J Register (Offset = 120h) [reset = 0h]

The FLC Low 'n' address defines the FLC lo address for FLC range 0. The FLC range is defined by FLC_LO0>=FLCrange<FLC_HI0. This register is write protected when ~ifenable0 is set.

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Table 14-7660. Instance Table

Instance Name	Physical Address
RL2_0	2500 0120h + formula
RL2_0	2500 1120h + formula
RL2_2	2500 2120h + formula
RL2_3	2500 3120h + formula

Figure 14-3809. RL2_OF_CBA4_FLC_LO_j Name Register

31	30	29	28	27	26	25	24
ADR_LO_LSW							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADR_LO_LSW							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADR_LO_LSW				RESERVED			
R/W				NONE			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-7661. RL2_OF_CBA4_FLC_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	ADR_LO_LSW	R/W	0h	The ~iadr0_lo defines the FLC low address[31:12] for the FLC to copy. The remaining bits 11:0 are assumed to be zero.
11:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.29 RL2_OF_CBA4_FLC_LO_MSW_J Register

14.3.1.3.2.29.1 RL2_OF_CBA4_FLC_LO_MSW_J Register (Offset = 124h) [reset = 0h]

The FLC Low 'n' address defines the FLC lo address for FLC range 0. The FLC range is defined by FLC_LO0>=FLCrange<FLC_HI0. This register is write protected when ~ifenable0 is set.

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Table 14-7662. Instance Table

Instance Name	Physical Address
RL2_0	2500 0124h + formula
RL2_0	2500 1124h + formula
RL2_2	2500 2124h + formula
RL2_3	2500 3124h + formula

Figure 14-3810. RL2_OF_CBA4_FLC_LO_MSW_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADR_LO_MSW							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADR_LO_MSW							
R/W							
0h							

Table 14-7663. RL2_OF_CBA4_FLC_LO_MSW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADR_LO_MSW	R/W	0h	The ~iadr0_lo defines the FLC low address[47:32] for the FLC to copy.

14.3.1.3.2.30 RL2_OF_CBA4_FLC_HI_J Register

14.3.1.3.2.30.1 RL2_OF_CBA4_FLC_HI_J Register (Offset = 128h) [reset = 0h]

The FLC High 'n' address defines the FLC high address for FLC range 0. The FLC range is defined by FLC_LO0>=FLCrange<FLC_HI0. This register is write protected when ~ifenable0 is set.

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Table 14-7664. Instance Table

Instance Name	Physical Address
RL2_0	2500 0128h + formula
RL2_0	2500 1128h + formula
RL2_2	2500 2128h + formula
RL2_3	2500 3128h + formula

Figure 14-3811. RL2_OF_CBA4_FLC_HI_j Name Register

31	30	29	28	27	26	25	24
ADR_HI_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
ADR_HI_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
ADR_HI_LSW				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7665. RL2_OF_CBA4_FLC_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	ADR_HI_LSW	R/W	0h	The ~iadr0_hi defines the FLC high address[31:12] for the FLC to copy. The remaining bits 11:0 are assumed to be ones.
11:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.31 RL2_OF_CBA4_FLC_HI_MSW_J Register

14.3.1.3.2.31.1 RL2_OF_CBA4_FLC_HI_MSW_J Register (Offset = 12Ch) [reset = 0h]

The FLC High 'n' address defines the FLC high address for FLC range 0. The FLC range is defined by FLC_LO0>=FLCrange<FLC_HI0. This register is write protected when ~ifenable0 is set.

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Table 14-7666. Instance Table

Instance Name	Physical Address
RL2_0	2500 012Ch + formula
RL2_0	2500 112Ch + formula
RL2_2	2500 212Ch + formula
RL2_3	2500 312Ch + formula

Figure 14-3812. RL2_OF_CBA4_FLC_HI_MSW_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADR_HI_MSW							
R/W							
0h							
7	6	5	4	3	2	1	0
ADR_HI_MSW							
R/W							
0h							

Table 14-7667. RL2_OF_CBA4_FLC_HI_MSW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADR_HI_MSW	R/W	0h	The ~iadr0_lo defines the FLC Hi address[47:32] for the FLC to copy.

14.3.1.3.2.32 RL2_OF_CBA4_FLC_RA_J Register

14.3.1.3.2.32.1 RL2_OF_CBA4_FLC_RA_J Register (Offset = 130h) [reset = 0h]

The FLC Remote Address 'n' specifies the SRAM location base address the FLC will copy slow Flash data to the SRAM. That is the SRAM is acting like a block cache for a slow device.

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Table 14-7668. Instance Table

Instance Name	Physical Address
RL2_0	2500 0130h + formula
RL2_0	2500 1130h + formula
RL2_2	2500 2130h + formula
RL2_3	2500 3130h + formula

Figure 14-3813. RL2_OF_CBA4_FLC_RA_j Name Register

31	30	29	28	27	26	25	24
RADR_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
RADR_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
RADR_LSW				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7669. RL2_OF_CBA4_FLC_RA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RADR_LSW	R/W	0h	The ~iradr0 specifies the remote SRAM address for FLC data to be copied. The SRAM must be large enough for the specified range.
11:0	RESERVED	NONE	0h	Reserved

14.3.1.3.2.33 RL2_OF_CBA4_FLC_RA_MSW_J Register

14.3.1.3.2.33.1 RL2_OF_CBA4_FLC_RA_MSW_J Register (Offset = 134h) [reset = 0h]

The FLC Remote Address 'n' specifies the SRAM location base address the FLC will copy slow Flash data to the SRAM. That is the SRAM is acting like a block cache for a slow device.

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Table 14-7670. Instance Table

Instance Name	Physical Address
RL2_0	2500 0134h + formula
RL2_0	2500 1134h + formula
RL2_2	2500 2134h + formula
RL2_3	2500 3134h + formula

Figure 14-3814. RL2_OF_CBA4_FLC_RA_MSW_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RADR_MSW							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RADR_MSW							
R/W							
0h							

Table 14-7671. RL2_OF_CBA4_FLC_RA_MSW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RADR_MSW	R/W	0h	The ~iradr0 specifies the remote SRAM address for FLC data to be copied. This defines FLC0_RA address47:32] The SRAM must be large enough for the specified range.

14.3.1.3.2.34 RL2_OF_CBA4_FLC_CTL_J Register

14.3.1.3.2.34.1 RL2_OF_CBA4_FLC_CTL_J Register (Offset = 138h) [reset = 0h]

The FLC Control 'n' enables the given range FLC_LO0>=FLCrange<FLC_HI0 to be copied to the FLC_RA0 SRAM memory.

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Table 14-7672. Instance Table

Instance Name	Physical Address
RL2_0	2500 0138h + formula
RL2_0	2500 1138h + formula
RL2_2	2500 2138h + formula
RL2_3	2500 3138h + formula

Figure 14-3815. RL2_OF_CBA4_FLC_CTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>FENABLE</td><td colspan="2">RESERVED</td><td>FCOPIED</td><td colspan="4">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="2">NONE</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7673. RL2_OF_CBA4_FLC_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FENABLE	R/W	0h	The ~ifenable0 enables the FLC_LO0>=FLCrange<FLC_HI0 to be copied. if the ~ifenable0 is set to zero, the range is disabled and commands forwarded directly without change.
30:29	RESERVED	NONE	0h	Reserved
28	FCOPIED	R/W	0h	The ~ifcopied0 bit indicates the FLC range has already been copied to the ~iradr0 address so a transfer is not required. Setting this bit at the same cycle or prior to setting the ~ifenable will prevent the FLC transfer but enable the mapping.
27:0	RESERVED	NONE	0h	Reserved

14.3.2 DSP (C7x256v) Registers

14.3.2.1 C7X256V_CLEC

C7X256V_CLEC

14.3.2.1.1 C7X256V_CLEC Summaries

C7X256V_CLEC Summaries

Table 14-7674. CLEC_EVT Registers, Base Address=7D20 0000h, Length=1048576

Offset	Length	Register Name	C7X256V1_CLEC Physical Address
0h	32	CLEC_EVT_GLOBAL_PID	7D20 0000h + formula
C000h	32	CLEC_EVT_GLOBAL_GELRS	7D20 C000h + formula
D000h	32	CLEC_EVT_GLOBAL_GELRNS	7D20 D000h + formula
80000h	32	CLEC_EVT_CFG_MRR_J	7D28 0000h + formula
80004h	32	CLEC_EVT_CFG_ESR_J	7D28 0004h + formula
80008h	32	CLEC_EVT_CFG_ECR_J	7D28 0008h + formula
A000h	32	CLEC_EVT_GLOBAL_SET_FLAG_EFR_J	7D20 A000h + formula
B000h	32	CLEC_EVT_GLOBAL_DROP_FLAG_EDR_J	7D20 B000h + formula

14.3.2.1.2 C7X256V_CLEC Registers

C7X256V_CLEC Registers

14.3.2.1.2.1 CLEC_EVT_GLOBAL_PID Register

14.3.2.1.2.1.1 CLEC_EVT_GLOBAL_PID Register (Offset = 0h) [reset = 60100100h]

Revision parameters

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Table 14-7675. Instance Table

Instance Name	Physical Address
C7X256V1_CLEC	7D20 0000h + formula

Figure 14-3816. CLEC_EVT_GLOBAL_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		10h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAX		
R					R		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-7676. CLEC_EVT_GLOBAL_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: mod_g_rst_n
29:28	BU	R	2h	Scheme Reset Source: mod_g_rst_n
27:16	MODULE_ID	R	10h	Module ID Reset Source: mod_g_rst_n
15:11	REVRTL	R	0h	RTL version Reset Source: mod_g_rst_n
10:8	REVMAX	R	1h	Major version Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom version Reset Source: mod_g_rst_n
5:0	REVMIN	R	0h	Minor version Reset Source: mod_g_rst_n

14.3.2.1.2.2 CLEC_EVT_GLOBAL_GELRS Register

14.3.2.1.2.2.1 CLEC_EVT_GLOBAL_GELRS Register (Offset = C000h) [reset = 0h]

Event Lock reg for secure claim

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Table 14-7677. Instance Table

Instance Name	Physical Address
C7X256V1_CLEC	7D20 C000h + formula

Figure 14-3817. CLEC_EVT_GLOBAL_GELRS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LOCK</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7678. CLEC_EVT_GLOBAL_GELRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved
0	LOCK	R/W	0h	GELRS.LOCK - event lock register for secure claim Reset Source: mod_g_rst_n

14.3.2.1.2.3 CLEC_EVT_GLOBAL_GELRNS Register

14.3.2.1.2.3.1 CLEC_EVT_GLOBAL_GELRNS Register (Offset = D000h) [reset = 0h]

Event Lock reg for non-secure claim

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Table 14-7679. Instance Table

Instance Name	Physical Address
C7X256V1_CLEC	7D20 D000h + formula

Figure 14-3818. CLEC_EVT_GLOBAL_GELRNS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R							R/W
0h							0h

Table 14-7680. CLEC_EVT_GLOBAL_GELRNS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved
0	LOCK	R/W	0h	GELRNS.LOCK - event lock register for non-secure claim Reset Source: mod_g_rst_n

14.3.2.1.2.4 CLEC_EVT_CFG_MRR_J Register

14.3.2.1.2.4.1 CLEC_EVT_CFG_MRR_J Register (Offset = 80000h) [reset = 1010000h]

Map and routing register

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Table 14-7681. Instance Table

Instance Name	Physical Address
C7X256V1_CLEC	7D28 0000h + formula

Figure 14-3819. CLEC_EVT_CFG_MRR_j Name Register

31	30	29	28	27	26	25	24
S	ESE	RSVD3				EVTPF	IS_LVL
R/W	R/W	R				R	R/W
0h	0h	0h				0h	1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD2		RTMAP					
R		R/W					
0h		1h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXT_EVTNUM							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD0		C7X_EVTNUM					
R		R/W					
0h		0h					

Table 14-7682. CLEC_EVT_CFG_MRR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	S	R/W	0h	MRR.S - reserved, not used for AM62A since CPU doesn't support secure mode Reset Source: mod_g_rst_n
30	ESE	R/W	0h	MRR.ESE - Event-Send enable. Controls whether CLEC sends this event when ESR is written or Event occurred on interrupt line Reset Source: mod_g_rst_n
29:26	RSVD3	R	0h	Reserved Reset Source: mod_g_rst_n
25	EVTPF	R	0h	MRR.EPF - same value as EFR, read only pending status of all events regardless of they are enabled or disabled, for pulse events this flag is cleared as soon as event is sent, for level events this flag is cleared when input event is deasserted, writing 1 to ECR_n register also clears this bit in case of pending pulse event Reset Source: mod_g_rst_n
24	IS_LVL	R/W	1h	MRR.IS_LVL - Indicate that input event is level or pulse, event handling is different based on whether event is level or pulse Reset Source: mod_g_rst_n
23:22	RSVD2	R	0h	Reserved Reset Source: mod_g_rst_n

Table 14-7682. CLEC_EVT_CFG_MRR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:16	RTMAP	R/W	1h	MRR.RTMAP - If Bit [16] = 1 Send to None, If Bit [17] = 1 and bit [16] = 0 Send to System, If [16] = 0 and [17] = 0 send to [21:18] Corepac encoded value - value 1 and 0xF are valid since there is only one CPU Reset Source: mod_g_rst_n
15:8	EXT_EVTNUM	R/W	0h	MRR.EXT_EVTNUM - encoded external event number, event 0- 63 SOC events, 64-95 DRU events, event 128 ARM event others are reserved for AM62A Reset Source: mod_g_rst_n
7:6	RSVD0	R	0h	Reserved Reset Source: mod_g_rst_n
5:0	C7X_EVTNUM	R/W	0h	MRR.C7x_EVTNUM - C7x event number to send when this event is triggered Reset Source: mod_g_rst_n

14.3.2.1.2.5 CLEC_EVT_CFG_ESR_J Register

14.3.2.1.2.5.1 CLEC_EVT_CFG_ESR_J Register (Offset = 80004h) [reset = 0h]

Event send reg

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Table 14-7683. Instance Table

Instance Name	Physical Address
C7X256V1_CLEC	7D28 0004h + formula

Figure 14-3820. CLEC_EVT_CFG_ESR_j Name Register

31	30	29	28	27	26	25	24
ESR_N							
W							
0h							
23	22	21	20	19	18	17	16
ESR_N							
W							
0h							
15	14	13	12	11	10	9	8
ESR_N							
W							
0h							
7	6	5	4	3	2	1	0
ESR_N							
W							
0h							

Table 14-7684. CLEC_EVT_CFG_ESR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ESR_N	W	0h	ESR.ESR_n sends event number n if it is enabled, address offset 0x010000 * n + 0x03000 Reset Source: mod_g_rst_n

14.3.2.1.2.6 CLEC_EVT_CFG_ECR_J Register

14.3.2.1.2.6.1 CLEC_EVT_CFG_ECR_J Register (Offset = 80008h) [reset = 0h]

Event clear reg

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Table 14-7685. Instance Table

Instance Name	Physical Address
C7X256V1_CLEC	7D28 0008h + formula

Figure 14-3821. CLEC_EVT_CFG_ECR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
W							
0h							
7	6	5	4	3	2	1	0
RESERVED						ECR_PFLAG	ECR_FLAG
W						W	W
0h						0h	0h

Table 14-7686. CLEC_EVT_CFG_ECR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	W	0h	Reserved
1	ECR_PFLAG	W	0h	ECR.EDR_Clear - clears EDR flag bit when 2 is written Reset Source: mod_g_rst_n
0	ECR_FLAG	W	0h	ECR.EFR_Clear - clears EFR flag bit when 1 is written, also clears corresponding SOC level event if sent to system on SOCinterrupt port Reset Source: mod_g_rst_n

14.3.2.1.2.7 CLEC_EVT_GLOBAL_SET_FLAG_EFR_J Register

14.3.2.1.2.7.1 CLEC_EVT_GLOBAL_SET_FLAG_EFR_J Register (Offset = A000h) [reset = 0h]

CLEC event flags

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Table 14-7687. Instance Table

Instance Name	Physical Address
C7X256V1_CLEC	7D20 A000h + formula

Figure 14-3822. CLEC_EVT_GLOBAL_SET_FLAG_EFR_j Name Register

31	30	29	28	27	26	25	24
EVNTFR							
R							
0h							
23	22	21	20	19	18	17	16
EVNTFR							
R							
0h							
15	14	13	12	11	10	9	8
EVNTFR							
R							
0h							
7	6	5	4	3	2	1	0
EVNTFR							
R							
0h							

Table 14-7688. CLEC_EVT_GLOBAL_SET_FLAG_EFR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EVNTFR	R	0h	event flag register, read only pending status of all events regardless of they are enabled or disabled, for pulse events this flag is cleared as soon as event is sent, for level events this flag is cleared when input event is deasserted, writing 1 to ECR_n register also clears this bit in case of pending pulse event, description in spec section 4.2.2 Reset Source: mod_g_rst_n

14.3.2.1.2.8 CLEC_EVT_GLOBAL_DROP_FLAG_EDR_J Register

14.3.2.1.2.8.1 CLEC_EVT_GLOBAL_DROP_FLAG_EDR_J Register (Offset = B000h) [reset = 0h]

CLEC dropped event flags

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Table 14-7689. Instance Table

Instance Name	Physical Address
C7X256V1_CLEC	7D20 B000h + formula

Figure 14-3823. CLEC_EVT_GLOBAL_DROP_FLAG_EDR_j Name Register

31	30	29	28	27	26	25	24
EVNTDR							
R							
0h							
23	22	21	20	19	18	17	16
EVNTDR							
R							
0h							
15	14	13	12	11	10	9	8
EVNTDR							
R							
0h							
7	6	5	4	3	2	1	0
EVNTDR							
R							
0h							

Table 14-7690. CLEC_EVT_GLOBAL_DROP_FLAG_EDR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EVNTDR	R	0h	dropped event flags, for input events which are pulse if events are sent back back and second event gets dropped since first event still in the pending event queue, this bit gets set indicating that an event has been dropped, it also generates dropped event interrupt, description in spec section 4.2.3 Reset Source: mod_g_rst_n

14.3.2.2 C7X256V_CORE0

C7X256V_CORE0

14.3.2.2.1 C7X256V_CORE0 Summaries

C7X256V_CORE0 Summaries

Table 14-7691. DRU_ATOMIC Registers, Base Address=7D48 0000h, Length=131072

Offset	Length	Register Name	C7X256V1_CORE0 Physical Address
0h	64	DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD0_1_J	7D48 0000h + formula
8h	64	DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD2_3_J	7D48 0008h + formula
10h	64	DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD4_5_J	7D48 0010h + formula
18h	64	DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD6_7_J	7D48 0018h + formula
20h	64	DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD8_9_J	7D48 0020h + formula
28h	64	DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD10_11_J	7D48 0028h + formula
30h	64	DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD12_13_J	7D48 0030h + formula
38h	64	DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD14_15_J	7D48 0038h + formula
40h	64	DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD0_1_J_K	7D48 0040h + formula
48h	64	DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD2_3_J_K	7D48 0048h + formula
50h	64	DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD4_5_J_K	7D48 0050h + formula
58h	64	DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD6_7_J_K	7D48 0058h + formula
60h	64	DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD8_9_J_K	7D48 0060h + formula
68h	64	DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD10_11_J_K	7D48 0068h + formula
70h	64	DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD12_13_J_K	7D48 0070h + formula
78h	64	DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD14_15_J_K	7D48 0078h + formula

Table 14-7692. DRU_CHCORE Registers, Base Address=7D4A 0000h, Length=131072

Offset	Length	Register Name	C7X256V1_CORE0 Physical Address
0h	64	DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD0_1_J_K	7D4A 0000h + formula
8h	64	DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD2_3_J_K	7D4A 0008h + formula
10h	64	DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD4_5_J_K	7D4A 0010h + formula
18h	64	DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD6_7_J_K	7D4A 0018h + formula
20h	64	DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD8_9_J_K	7D4A 0020h + formula

Table 14-7692. DRU_CHCORE Registers, Base Address=7D4A 0000h, Length=131072 (continued)

Offset	Length	Register Name	C7X256V1_CORE0 Physical Address
28h	64	DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD10_11_J_K	7D4A 0028h + formula
30h	64	DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD12_13_J_K	7D4A 0030h + formula
38h	64	DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD14_15_J_K	7D4A 0038h + formula

14.3.2.2.2 C7X256V_CORE0 Registers

C7X256V_CORE0 Registers

14.3.2.2.2.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD0_1_J Register

14.3.2.2.2.1.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD0_1_J Register (Offset = 0h) [reset = 0h]

The first TR submission word

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Table 14-7693. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0000h + formula

Figure 14-3824. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD0_1_j Name Register

63	62	61	60	59	58	57	48
ICNT1							
R							
0h							
55	54	53	52	51	50	49	48
ICNT1							
R							
0h							
47	46	45	44	43	42	41	40
ICNT0							
R							
0h							
39	38	37	36	35	34	33	32
ICNT0							
R							
0h							
15	14	13	12	11	10	9	8
FLAGS							
R							
0h							
7	6	5	4	3	2	1	0
FLAGS							
R							
0h							

Table 14-7694. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD0_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	ICNT1	R	0h	Lines in a transfer
47:32	ICNT0	R	0h	Bytes in a transfer
31:0	FLAGS	R	0h	Flags for the operation and type of descriptor

14.3.2.2.2.2 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD2_3_J Register

14.3.2.2.2.2.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD2_3_J Register (Offset = 8h) [reset = 0h]

The second TR submission word

Return to Summary Table

Table 14-7695. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0008h + formula

Figure 14-3825. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD2_3_j Name Register

63	62	61	60	59	58	57	48
RSVD							
R							
0h							
55	54	53	52	51	50	49	48
RSVD							
R							
0h							
47	46	45	44	43	42	41	40
SRC_ADDR							
R							
0h							
39	38	37	36	35	34	33	32
SRC_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
SRC_ADDR							
R							
0h							

Table 14-7696. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD2_3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RSVD	R	0h	Reserved
47:0	SRC_ADDR	R	0h	Source transfer address virtual or physical allowed

14.3.2.2.2.3 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD4_5_J Register

14.3.2.2.2.3.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD4_5_J Register (Offset = 10h) [reset = 0h]

The third TR submission word

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Table 14-7697. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0010h + formula

Figure 14-3826. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD4_5_j Name Register

63	62	61	60	59	58	57	48
ICNT3							
R							
0h							
55	54	53	52	51	50	49	48
ICNT3							
R							
0h							
47	46	45	44	43	42	41	40
ICNT2							
R							
0h							
39	38	37	36	35	34	33	32
ICNT2							
R							
0h							
15	14	13	12	11	10	9	8
DIM1							
R							
0h							
7	6	5	4	3	2	1	0
DIM1							
R							
0h							

Table 14-7698. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD4_5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	ICNT3	R	0h	The size of the 4th loop in the TR transfer
47:32	ICNT2	R	0h	The size of the 3rd loop in the TR transfer
31:0	DIM1	R	0h	The first dimension width of the source data

14.3.2.2.2.4 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD6_7_J Register

14.3.2.2.2.4.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD6_7_J Register (Offset = 18h) [reset = 0h]

The fourth TR submission word

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Table 14-7699. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0018h + formula

Figure 14-3827. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD6_7_j Name Register

63	62	61	60	59	58	57	48
DIM3							
R							
0h							
55	54	53	52	51	50	49	48
DIM3							
R							
0h							
47	46	45	44	43	42	41	40
DIM3							
R							
0h							
39	38	37	36	35	34	33	32
DIM3							
R							
0h							
15	14	13	12	11	10	9	8
DIM2							
R							
0h							
7	6	5	4	3	2	1	0
DIM2							
R							
0h							

Table 14-7700. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD6_7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DIM3	R	0h	The third dimension width of the source data
31:0	DIM2	R	0h	The second dimension width of the source data

14.3.2.2.2.5 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD8_9_J Register

14.3.2.2.2.5.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD8_9_J Register (Offset = 20h) [reset = 0h]

The fifth TR submission word

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Table 14-7701. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0020h + formula

Figure 14-3828. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD8_9_j Name Register

63	62	61	60	59	58	57	48
DDIM1							
R							
0h							
55	54	53	52	51	50	49	48
DDIM1							
R							
0h							
47	46	45	44	43	42	41	40
DDIM1							
R							
0h							
39	38	37	36	35	34	33	32
DDIM1							
R							
0h							
15	14	13	12	11	10	9	8
FMTFLAGS							
R							
0h							
7	6	5	4	3	2	1	0
FMTFLAGS							
R							
0h							

Table 14-7702. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD8_9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DDIM1	R	0h	The first dimension width of the destination data
31:0	FMTFLAGS	R	0h	The data formatting flags to be used for the TR

14.3.2.2.2.6 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD10_11_J Register

14.3.2.2.2.6.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD10_11_J Register (Offset = 28h) [reset = 0h]

The sixth TR submission word

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Table 14-7703. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0028h + formula

Figure 14-3829. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD10_11_j Name Register

63	62	61	60	59	58	57	48
RSVD							
R							
0h							
55	54	53	52	51	50	49	48
RSVD							
R							
0h							
47	46	45	44	43	42	41	40
DADDR							
R							
0h							
39	38	37	36	35	34	33	32
DADDR							
R							
0h							
15	14	13	12	11	10	9	8
DADDR							
R							
0h							
7	6	5	4	3	2	1	0
DADDR							
R							
0h							

Table 14-7704. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD10_11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RSVD	R	0h	Reserved
47:0	DADDR	R	0h	Destination transfer address virtual or physical allowed

14.3.2.2.2.7 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD12_13_J Register

14.3.2.2.2.7.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD12_13_J Register (Offset = 30h) [reset = 0h]

The seventh TR submission word

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Table 14-7705. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0030h + formula

Figure 14-3830. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD12_13_j Name Register

63	62	61	60	59	58	57	48
DDIM3							
R							
0h							
55	54	53	52	51	50	49	48
DDIM3							
R							
0h							
47	46	45	44	43	42	41	40
DDIM3							
R							
0h							
39	38	37	36	35	34	33	32
DDIM3							
R							
0h							
15	14	13	12	11	10	9	8
DDIM2							
R							
0h							
7	6	5	4	3	2	1	0
DDIM2							
R							
0h							

Table 14-7706. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD12_13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DDIM3	R	0h	The third dimension width of the destination data
31:0	DDIM2	R	0h	The second dimension width of the destination data

14.3.2.2.2.8 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD14_15_J Register

14.3.2.2.2.8.1 DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD14_15_J Register (Offset = 38h) [reset = 0h]

The eight TR submission word

Return to Summary Table

Table 14-7707. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0038h + formula

Figure 14-3831. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD14_15_j Name Register

63	62	61	60	59	58	57	48
DICNT3							
R							
0h							
55	54	53	52	51	50	49	48
DICNT3							
R							
0h							
47	46	45	44	43	42	41	40
DICNT2							
R							
0h							
39	38	37	36	35	34	33	32
DICNT2							
R							
0h							
15	14	13	12	11	10	9	8
DICNT0							
R							
0h							
7	6	5	4	3	2	1	0
DICNT0							
R							
0h							

Table 14-7708. DRU_ATOMIC_CHATOMIC_DEBUG_ATOMIC_SUBMIT_CURR_TR_WORD14_15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	DICNT3	R	0h	The fourth count of the destination if different than the source
47:32	DICNT2	R	0h	The third count of the destination if different than the source
31:16	DICNT1	R	0h	The second innermost count of the destination if different than the source
15:0	DICNT0	R	0h	The innermost count of the destination if different than the source

14.3.2.2.2.9 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD0_1_J_K Register

14.3.2.2.2.9.1 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD0_1_J_K Register (Offset = 40h) [reset = 0h]

The first TR submission word

Return to Summary Table

Table 14-7709. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0040h + formula

Figure 14-3832. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD0_1_j_k Name Register

63	62	61	60	59	58	57	48
ICNT1							
R							
0h							
55	54	53	52	51	50	49	48
ICNT1							
R							
0h							
47	46	45	44	43	42	41	40
ICNT0							
R							
0h							
39	38	37	36	35	34	33	32
ICNT0							
R							
0h							
15	14	13	12	11	10	9	8
FLAGS							
R							
0h							
7	6	5	4	3	2	1	0
FLAGS							
R							
0h							

Table 14-7710. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD0_1_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	ICNT1	R	0h	Lines in a transfer
47:32	ICNT0	R	0h	Bytes in a transfer
31:0	FLAGS	R	0h	Flags for the operation and type of descriptor

14.3.2.2.2.10 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD2_3_J_K Register

14.3.2.2.2.10.1 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD2_3_J_K Register (Offset = 48h) [reset = 0h]

The second TR submission word

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Table 14-7711. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0048h + formula

Figure 14-3833. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD2_3_j_k Name Register

63	62	61	60	59	58	57	48
RSVD							
R							
0h							
55	54	53	52	51	50	49	48
RSVD							
R							
0h							
47	46	45	44	43	42	41	40
SRC_ADDR							
R							
0h							
39	38	37	36	35	34	33	32
SRC_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
SRC_ADDR							
R							
0h							

Table 14-7712. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD2_3_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RSVD	R	0h	Reserved
47:0	SRC_ADDR	R	0h	Source transfer address virtual or physical allowed

14.3.2.2.2.11 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD4_5_J_K Register

14.3.2.2.2.11.1 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD4_5_J_K Register (Offset = 50h) [reset = 0h]

The third TR submission word

Return to Summary Table

Table 14-7713. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0050h + formula

Figure 14-3834. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD4_5_j_k Name Register

63	62	61	60	59	58	57	48
ICNT3							
R							
0h							
55	54	53	52	51	50	49	48
ICNT3							
R							
0h							
47	46	45	44	43	42	41	40
ICNT2							
R							
0h							
39	38	37	36	35	34	33	32
ICNT2							
R							
0h							
15	14	13	12	11	10	9	8
DIM1							
R							
0h							
7	6	5	4	3	2	1	0
DIM1							
R							
0h							

Table 14-7714. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD4_5_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	ICNT3	R	0h	The size of the 4th loop in the TR transfer
47:32	ICNT2	R	0h	The size of the 3rd loop in the TR transfer
31:0	DIM1	R	0h	The first dimension width of the source data

14.3.2.2.2.12 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD6_7_J_K Register

14.3.2.2.2.12.1 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD6_7_J_K Register (Offset = 58h) [reset = 0h]

The fourth TR submission word

Return to Summary Table

Table 14-7715. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0058h + formula

Figure 14-3835. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD6_7_j_k Name Register

63	62	61	60	59	58	57	48
DIM3							
R							
0h							
55	54	53	52	51	50	49	48
DIM3							
R							
0h							
47	46	45	44	43	42	41	40
DIM3							
R							
0h							
39	38	37	36	35	34	33	32
DIM3							
R							
0h							
15	14	13	12	11	10	9	8
DIM2							
R							
0h							
7	6	5	4	3	2	1	0
DIM2							
R							
0h							

Table 14-7716. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD6_7_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DIM3	R	0h	The third dimension width of the source data
31:0	DIM2	R	0h	The second dimension width of the source data

14.3.2.2.2.13 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD8_9_J_K Register

14.3.2.2.2.13.1 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD8_9_J_K Register (Offset = 60h) [reset = 0h]

The fifth TR submission word

Return to Summary Table

Table 14-7717. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0060h + formula

Figure 14-3836. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD8_9_j_k Name Register

63	62	61	60	59	58	57	48
DDIM1							
R							
0h							
55	54	53	52	51	50	49	48
DDIM1							
R							
0h							
47	46	45	44	43	42	41	40
DDIM1							
R							
0h							
39	38	37	36	35	34	33	32
DDIM1							
R							
0h							
15	14	13	12	11	10	9	8
FMTFLAGS							
R							
0h							
7	6	5	4	3	2	1	0
FMTFLAGS							
R							
0h							

Table 14-7718. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD8_9_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DDIM1	R	0h	The first dimension width of the destination data
31:0	FMTFLAGS	R	0h	The data formatting flags to be used for the TR

14.3.2.2.2.14 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD10_11_J_K Register

14.3.2.2.2.14.1 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD10_11_J_K Register (Offset = 68h) [reset = 0h]

The sixth TR submission word

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Table 14-7719. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0068h + formula

Figure 14-3837. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD10_11_j_k Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">DADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">DADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7720. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD10_11_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RSVD	R	0h	Reserved
47:0	DADDR	R	0h	Destination transfer address virtual or physical allowed

14.3.2.2.2.15 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD12_13_J_K Register

14.3.2.2.2.15.1 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD12_13_J_K Register (Offset = 70h) [reset = 0h]

The seventh TR submission word

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Table 14-7721. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0070h + formula

Figure 14-3838. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD12_13_j_k Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">DDIM3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">DDIM3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">DDIM3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">DDIM3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DDIM2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DDIM2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7722. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD12_13_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DDIM3	R	0h	The third dimension width of the destination data
31:0	DDIM2	R	0h	The second dimension width of the destination data

14.3.2.2.2.16 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD14_15_J_K Register

14.3.2.2.2.16.1 DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD14_15_J_K Register (Offset = 78h) [reset = 0h]

The eight TR submission word

Return to Summary Table

Table 14-7723. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D48 0078h + formula

Figure 14-3839. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD14_15_j_k Name Register

63	62	61	60	59	58	57	48
DICNT3							
R							
0h							
55	54	53	52	51	50	49	48
DICNT3							
R							
0h							
47	46	45	44	43	42	41	40
DICNT2							
R							
0h							
39	38	37	36	35	34	33	32
DICNT2							
R							
0h							
15	14	13	12	11	10	9	8
DICNT0							
R							
0h							
7	6	5	4	3	2	1	0
DICNT0							
R							
0h							

Table 14-7724. DRU_ATOMIC_CHATOMIC_DEBUG_DEBUG_NEXT_TR_WORD14_15_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	DICNT3	R	0h	The fourth count of the destination if different than the source
47:32	DICNT2	R	0h	The third count of the destination if different than the source
31:16	DICNT1	R	0h	The second innermost count of the destination if different than the source
15:0	DICNT0	R	0h	The innermost count of the destination if different than the source

14.3.2.2.2.17 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD0_1_J_K Register

14.3.2.2.2.17.1 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD0_1_J_K Register (Offset = 0h) [reset = 0h]

The first TR submission word

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Table 14-7725. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D4A 0000h + formula

Figure 14-3840. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD0_1_j_k Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">ICNT1</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">ICNT1</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">ICNT0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">ICNT0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FLAGS</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FLAGS</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7726. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD0_1_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	ICNT1	W	0h	Lines in a transfer
47:32	ICNT0	W	0h	Bytes in a transfer
31:0	FLAGS	W	0h	Flags for the operation and type of descriptor

14.3.2.2.2.18 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD2_3_J_K Register

14.3.2.2.2.18.1 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD2_3_J_K Register (Offset = 8h) [reset = 0h]

The second TR submission word

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Table 14-7727. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D4A 0008h + formula

Figure 14-3841. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD2_3_j_k Name Register

63	62	61	60	59	58	57	48
RSVD							
0h							
55	54	53	52	51	50	49	48
RSVD							
0h							
47	46	45	44	43	42	41	40
SRC_ADDR							
W							
0h							
39	38	37	36	35	34	33	32
SRC_ADDR							
W							
0h							
15	14	13	12	11	10	9	8
SRC_ADDR							
W							
0h							
7	6	5	4	3	2	1	0
SRC_ADDR							
W							
0h							

Table 14-7728. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD2_3_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RSVD		0h	Reserved
47:0	SRC_ADDR	W	0h	Source transfer address virtual or physical allowed

14.3.2.2.2.19 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD4_5_J_K Register

14.3.2.2.2.19.1 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD4_5_J_K Register (Offset = 10h) [reset = 0h]

The third TR submission word

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Table 14-7729. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D4A 0010h + formula

Figure 14-3842. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD4_5_j_k Name Register

63	62	61	60	59	58	57	48
ICNT3							
W							
0h							
55	54	53	52	51	50	49	48
ICNT3							
W							
0h							
47	46	45	44	43	42	41	40
ICNT2							
W							
0h							
39	38	37	36	35	34	33	32
ICNT2							
W							
0h							
15	14	13	12	11	10	9	8
DIM1							
W							
0h							
7	6	5	4	3	2	1	0
DIM1							
W							
0h							

Table 14-7730. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD4_5_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	ICNT3	W	0h	The size of the 4th loop in the TR transfer
47:32	ICNT2	W	0h	The size of the 3rd loop in the TR transfer
31:0	DIM1	W	0h	The first dimension width of the source data

14.3.2.2.2.20 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD6_7_J_K Register

14.3.2.2.2.20.1 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD6_7_J_K Register (Offset = 18h) [reset = 0h]

The fourth TR submission word

Return to Summary Table

Table 14-7731. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D4A 0018h + formula

Figure 14-3843. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD6_7_j_k Name Register

63	62	61	60	59	58	57	48
DIM3							
W							
0h							
55	54	53	52	51	50	49	48
DIM3							
W							
0h							
47	46	45	44	43	42	41	40
DIM3							
W							
0h							
39	38	37	36	35	34	33	32
DIM3							
W							
0h							
15	14	13	12	11	10	9	8
DIM2							
W							
0h							
7	6	5	4	3	2	1	0
DIM2							
W							
0h							

Table 14-7732. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD6_7_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DIM3	W	0h	The third dimension width of the source data
31:0	DIM2	W	0h	The second dimension width of the source data

14.3.2.2.2.21 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD8_9_J_K Register

14.3.2.2.2.21.1 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD8_9_J_K Register (Offset = 20h) [reset = 0h]

The fifth TR submission word

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Table 14-7733. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D4A 0020h + formula

Figure 14-3844. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD8_9_j_k Name Register

63	62	61	60	59	58	57	48
DDIM1							
W							
0h							
55	54	53	52	51	50	49	48
DDIM1							
W							
0h							
47	46	45	44	43	42	41	40
DDIM1							
W							
0h							
39	38	37	36	35	34	33	32
DDIM1							
W							
0h							
15	14	13	12	11	10	9	8
FMTFLAGS							
W							
0h							
7	6	5	4	3	2	1	0
FMTFLAGS							
W							
0h							

Table 14-7734. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD8_9_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DDIM1	W	0h	The first dimension width of the destination data
31:0	FMTFLAGS	W	0h	The data formatting flags to be used for the TR

14.3.2.2.2.22 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD10_11_J_K Register

14.3.2.2.2.22.1 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD10_11_J_K Register (Offset = 28h) [reset = 0h]

The sixth TR submission word

Return to Summary Table

Table 14-7735. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D4A 0028h + formula

Figure 14-3845. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD10_11_j_k Name Register

63	62	61	60	59	58	57	48
RSVD							
0h							
55	54	53	52	51	50	49	48
RSVD							
0h							
47	46	45	44	43	42	41	40
DADDR							
W							
0h							
39	38	37	36	35	34	33	32
DADDR							
W							
0h							
15	14	13	12	11	10	9	8
DADDR							
W							
0h							
7	6	5	4	3	2	1	0
DADDR							
W							
0h							

Table 14-7736. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD10_11_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RSVD		0h	Reserved
47:0	DADDR	W	0h	Destination transfer address virtual or physical allowed

14.3.2.2.2.23 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD12_13_J_K Register

14.3.2.2.2.23.1 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD12_13_J_K Register (Offset = 30h) [reset = 0h]

The seventh TR submission word

Return to Summary Table

Table 14-7737. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D4A 0030h + formula

Figure 14-3846. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD12_13_j_k Name Register

63	62	61	60	59	58	57	48
DDIM3							
W							
0h							
55	54	53	52	51	50	49	48
DDIM3							
W							
0h							
47	46	45	44	43	42	41	40
DDIM3							
W							
0h							
39	38	37	36	35	34	33	32
DDIM3							
W							
0h							
15	14	13	12	11	10	9	8
DDIM2							
W							
0h							
7	6	5	4	3	2	1	0
DDIM2							
W							
0h							

Table 14-7738. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD12_13_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	DDIM3	W	0h	The third dimension width of the destination data
31:0	DDIM2	W	0h	The second dimension width of the destination data

14.3.2.2.2.24 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD14_15_J_K Register

14.3.2.2.2.24.1 DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD14_15_J_K Register (Offset = 38h) [reset = 0h]

The eight TR submission word

Return to Summary Table

Table 14-7739. Instance Table

Instance Name	Physical Address
C7X256V1_CORE0	7D4A 0038h + formula

Figure 14-3847. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD14_15_j_k Name Register

63	62	61	60	59	58	57	48
DICNT3							
W							
0h							
55	54	53	52	51	50	49	48
DICNT3							
W							
0h							
47	46	45	44	43	42	41	40
DICNT2							
W							
0h							
39	38	37	36	35	34	33	32
DICNT2							
W							
0h							
15	14	13	12	11	10	9	8
DICNT0							
W							
0h							
7	6	5	4	3	2	1	0
DICNT0							
W							
0h							

Table 14-7740. DRU_CHCORE_CHCORE_CORE_SUBMIT_WORD14_15_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	DICNT3	W	0h	The fourth count of the destination if different than the source
47:32	DICNT2	W	0h	The third count of the destination if different than the source
31:16	DICNT1	W	0h	The second innermost count of the destination if different than the source
15:0	DICNT0	W	0h	The innermost count of the destination if different than the source

14.3.2.3 C7X256V_DEBUG

C7X256V_DEBUG

14.3.2.3.1 C7X256V_DEBUG Summaries

C7X256V_DEBUG Summaries

Table 14-7741. THINMAN_REG Registers, Base Address=0007 3400 0000h, Length=8192

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address	C7X256V1_DEBUG Physical Address
0h	32	THINMAN_REG_DBG_CAP	0007 3400 0000h	0007 3800 0000h
4h	32	THINMAN_REG_DBG_PID	0007 3400 0004h	0007 3800 0004h
10h	32	THINMAN_REG_DBG_CNTL	0007 3400 0010h	0007 3800 0010h
14h	32	THINMAN_REG_DBG_STAT	0007 3400 0014h	0007 3800 0014h
18h	32	THINMAN_REG_DBG_OWN	0007 3400 0018h	0007 3800 0018h
20h	32	THINMAN_REG_DBG_INDRCT_CAP0	0007 3400 0020h	0007 3800 0020h
24h	32	THINMAN_REG_DBG_INDRCT_CAP1	0007 3400 0024h	0007 3800 0024h
30h	32	THINMAN_REG_DBG_INDRCT_CNTL	0007 3400 0030h	0007 3800 0030h
34h	32	THINMAN_REG_DBG_INDRCT_CTXT0	0007 3400 0034h	0007 3800 0034h
38h	32	THINMAN_REG_DBG_INDRCT_CTXT1	0007 3400 0038h	0007 3800 0038h
3Ch	32	THINMAN_REG_DBG_INDRCT_CTXT2	0007 3400 003Ch	0007 3800 003Ch
40h	32	THINMAN_REG_DBG_INDRCT_ADDR0	0007 3400 0040h	0007 3800 0040h
44h	32	THINMAN_REG_DBG_INDRCT_ADDR1	0007 3400 0044h	0007 3800 0044h
48h	32	THINMAN_REG_DBG_INDRCT_DATA0	0007 3400 0048h	0007 3800 0048h
4Ch	32	THINMAN_REG_DBG_INDRCT_DATA1	0007 3400 004Ch	0007 3800 004Ch
100h	32	THINMAN_REG_DBG_HWBP_0_CNTL	0007 3400 0100h	0007 3800 0100h
108h	32	THINMAN_REG_DBG_HWBP_0_CTXT0	0007 3400 0108h	0007 3800 0108h
10Ch	32	THINMAN_REG_DBG_HWBP_0_CTXT1	0007 3400 010Ch	0007 3800 010Ch
110h	32	THINMAN_REG_DBG_HWBP_0_CTXT2	0007 3400 0110h	0007 3800 0110h
118h	32	THINMAN_REG_DBG_HWBP_0_ADDR0	0007 3400 0118h	0007 3800 0118h
11Ch	32	THINMAN_REG_DBG_HWBP_0_ADDR1	0007 3400 011Ch	0007 3800 011Ch
120h	32	THINMAN_REG_DBG_HWBP_0_AMASK0	0007 3400 0120h	0007 3800 0120h
124h	32	THINMAN_REG_DBG_HWBP_0_AMASK1	0007 3400 0124h	0007 3800 0124h
180h	32	THINMAN_REG_DBG_HWBP_1_CNTL	0007 3400 0180h	0007 3800 0180h
188h	32	THINMAN_REG_DBG_HWBP_1_CTXT0	0007 3400 0188h	0007 3800 0188h
18Ch	32	THINMAN_REG_DBG_HWBP_1_CTXT1	0007 3400 018Ch	0007 3800 018Ch
190h	32	THINMAN_REG_DBG_HWBP_1_CTXT2	0007 3400 0190h	0007 3800 0190h
198h	32	THINMAN_REG_DBG_HWBP_1_ADDR0	0007 3400 0198h	0007 3800 0198h
19Ch	32	THINMAN_REG_DBG_HWBP_1_ADDR1	0007 3400 019Ch	0007 3800 019Ch
1A0h	32	THINMAN_REG_DBG_HWBP_1_AMASK0	0007 3400 01A0h	0007 3800 01A0h
1A4h	32	THINMAN_REG_DBG_HWBP_1_AMASK1	0007 3400 01A4h	0007 3800 01A4h
200h	32	THINMAN_REG_DBG_HWBP_2_CNTL	0007 3400 0200h	0007 3800 0200h
208h	32	THINMAN_REG_DBG_HWBP_2_CTXT0	0007 3400 0208h	0007 3800 0208h
20Ch	32	THINMAN_REG_DBG_HWBP_2_CTXT1	0007 3400 020Ch	0007 3800 020Ch
210h	32	THINMAN_REG_DBG_HWBP_2_CTXT2	0007 3400 0210h	0007 3800 0210h
218h	32	THINMAN_REG_DBG_HWBP_2_ADDR0	0007 3400 0218h	0007 3800 0218h
21Ch	32	THINMAN_REG_DBG_HWBP_2_ADDR1	0007 3400 021Ch	0007 3800 021Ch
220h	32	THINMAN_REG_DBG_HWBP_2_AMASK0	0007 3400 0220h	0007 3800 0220h
224h	32	THINMAN_REG_DBG_HWBP_2_AMASK1	0007 3400 0224h	0007 3800 0224h

Table 14-7741. THINMAN_REG Registers, Base Address=0007 3400 0000h, Length=8192 (continued)

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address	C7X256V1_DEBUG Physical Address
280h	32	THINMAN_REG_DBG_HWBP_3_CNTL	0007 3400 0280h	0007 3800 0280h
288h	32	THINMAN_REG_DBG_HWBP_3_CTXT0	0007 3400 0288h	0007 3800 0288h
28Ch	32	THINMAN_REG_DBG_HWBP_3_CTXT1	0007 3400 028Ch	0007 3800 028Ch
290h	32	THINMAN_REG_DBG_HWBP_3_CTXT2	0007 3400 0290h	0007 3800 0290h
298h	32	THINMAN_REG_DBG_HWBP_3_ADDR0	0007 3400 0298h	0007 3800 0298h
29Ch	32	THINMAN_REG_DBG_HWBP_3_ADDR1	0007 3400 029Ch	0007 3800 029Ch
2A0h	32	THINMAN_REG_DBG_HWBP_3_AMASK0	0007 3400 02A0h	0007 3800 02A0h
2A4h	32	THINMAN_REG_DBG_HWBP_3_AMASK1	0007 3400 02A4h	0007 3800 02A4h
300h	32	THINMAN_REG_DBG_HWWP_0_CNTL	0007 3400 0300h	0007 3800 0300h
308h	32	THINMAN_REG_DBG_HWWP_0_CTXT0	0007 3400 0308h	0007 3800 0308h
30Ch	32	THINMAN_REG_DBG_HWWP_0_CTXT1	0007 3400 030Ch	0007 3800 030Ch
310h	32	THINMAN_REG_DBG_HWWP_0_CTXT2	0007 3400 0310h	0007 3800 0310h
318h	32	THINMAN_REG_DBG_HWWP_0_ADDR0	0007 3400 0318h	0007 3800 0318h
31Ch	32	THINMAN_REG_DBG_HWWP_0_ADDR1	0007 3400 031Ch	0007 3800 031Ch
320h	32	THINMAN_REG_DBG_HWWP_0_AMASK0	0007 3400 0320h	0007 3800 0320h
324h	32	THINMAN_REG_DBG_HWWP_0_AMASK1	0007 3400 0324h	0007 3800 0324h

Table 14-7742. COLUMBO_COLUMBO_REG Registers, Base Address=0007 3400 1000h, Length=8192

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address	C7X256V1_DEBUG Physical Address
0h	32	COLUMBO_COLUMBO_REG_AET_PID	0007 3400 1000h	0007 3800 1000h
4h	32	COLUMBO_COLUMBO_REG_AET_OWN	0007 3400 1004h	0007 3800 1004h
8h	32	COLUMBO_COLUMBO_REG_AET_STAT	0007 3400 1008h	0007 3800 1008h
10h	32	COLUMBO_COLUMBO_REG_AET_EVT	0007 3400 1010h	0007 3800 1010h
14h	32	COLUMBO_COLUMBO_REG_AET_PC_0	0007 3400 1014h	0007 3800 1014h
18h	32	COLUMBO_COLUMBO_REG_AET_PC_1	0007 3400 1018h	0007 3800 1018h
20h	32	COLUMBO_COLUMBO_REG_IAR_ADD	0007 3400 1020h	0007 3800 1020h
24h	32	COLUMBO_COLUMBO_REG_IAR_DAT	0007 3400 1024h	0007 3800 1024h

Table 14-7743. MATLOCK_REG Registers, Base Address=0007 3400 2000h, Length=8192

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address	C7X256V1_DEBUG Physical Address
0h	32	MATLOCK_REG_TRC_ID	0007 3400 2000h	0007 3800 2000h
4h	32	MATLOCK_REG_TRC_OWN	0007 3400 2004h	0007 3800 2004h
8h	32	MATLOCK_REG_TRC_CNTL	0007 3400 2008h	0007 3800 2008h
Ch	32	MATLOCK_REG_TRC_PER_CNT	0007 3400 200Ch	0007 3800 200Ch
10h	32	MATLOCK_REG_TRC_STAT	0007 3400 2010h	0007 3800 2010h
14h	32	MATLOCK_REG_TRC_TRIG0_CNTL_STAT	0007 3400 2014h	0007 3800 2014h
18h	32	MATLOCK_REG_TRC_TRIG1_CNTL_STAT	0007 3400 2018h	0007 3800 2018h
1Ch	32	MATLOCK_REG_TRC_TIMESTAMP_CNT_REG0	0007 3400 201Ch	0007 3800 201Ch
20h	32	MATLOCK_REG_TRC_TIMESTAMP_CNT_REG1	0007 3400 2020h	0007 3800 2020h
24h	32	MATLOCK_REG_TRC_EXPT_CNTL	0007 3400 2024h	0007 3800 2024h
28h	32	MATLOCK_REG_TRC_EXPT_STAT	0007 3400 2028h	0007 3800 2028h
2Ch	32	MATLOCK_REG_TRC_EXPT_ATID	0007 3400 202Ch	0007 3800 202Ch

Table 14-7744. CSCTI Registers, Base Address=0007 3400 3000h, Length=4096

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address	C7X256V0_DEBUG Physical Address	C7X256V0_DEBUG Physical Address
0h	32	CSCTI_CTICONTROL	0007 3400 3000h	0007 3400 A000h	0007 3400 B000h
10h	32	CSCTI_CTIINTACK	0007 3400 3010h	0007 3400 A010h	0007 3400 B010h
14h	32	CSCTI_CTIAPPSET	0007 3400 3014h	0007 3400 A014h	0007 3400 B014h
18h	32	CSCTI_CTIAPPCLR	0007 3400 3018h	0007 3400 A018h	0007 3400 B018h
1Ch	32	CSCTI_CTIAPPPULSE	0007 3400 301Ch	0007 3400 A01Ch	0007 3400 B01Ch
20h	32	CSCTI_CTIINEN0	0007 3400 3020h	0007 3400 A020h	0007 3400 B020h
24h	32	CSCTI_CTIINEN1	0007 3400 3024h	0007 3400 A024h	0007 3400 B024h
28h	32	CSCTI_CTIINEN2	0007 3400 3028h	0007 3400 A028h	0007 3400 B028h
2Ch	32	CSCTI_CTIINEN3	0007 3400 302Ch	0007 3400 A02Ch	0007 3400 B02Ch
30h	32	CSCTI_CTIINEN4	0007 3400 3030h	0007 3400 A030h	0007 3400 B030h
34h	32	CSCTI_CTIINEN5	0007 3400 3034h	0007 3400 A034h	0007 3400 B034h
38h	32	CSCTI_CTIINEN6	0007 3400 3038h	0007 3400 A038h	0007 3400 B038h
3Ch	32	CSCTI_CTIINEN7	0007 3400 303Ch	0007 3400 A03Ch	0007 3400 B03Ch
A0h	32	CSCTI_CTIOUTEN0	0007 3400 30A0h	0007 3400 A0A0h	0007 3400 B0A0h
A4h	32	CSCTI_CTIOUTEN1	0007 3400 30A4h	0007 3400 A0A4h	0007 3400 B0A4h
A8h	32	CSCTI_CTIOUTEN2	0007 3400 30A8h	0007 3400 A0A8h	0007 3400 B0A8h
ACh	32	CSCTI_CTIOUTEN3	0007 3400 30ACh	0007 3400 A0ACh	0007 3400 B0ACh
B0h	32	CSCTI_CTIOUTEN4	0007 3400 30B0h	0007 3400 A0B0h	0007 3400 B0B0h
B4h	32	CSCTI_CTIOUTEN5	0007 3400 30B4h	0007 3400 A0B4h	0007 3400 B0B4h
B8h	32	CSCTI_CTIOUTEN6	0007 3400 30B8h	0007 3400 A0B8h	0007 3400 B0B8h
BCh	32	CSCTI_CTIOUTEN7	0007 3400 30BCh	0007 3400 A0BCh	0007 3400 B0BCh
130h	32	CSCTI_CTITRIGINSTATUS	0007 3400 3130h	0007 3400 A130h	0007 3400 B130h
134h	32	CSCTI_CTITRIGOUTSTATUS	0007 3400 3134h	0007 3400 A134h	0007 3400 B134h
138h	32	CSCTI_CTICHINSTATUS	0007 3400 3138h	0007 3400 A138h	0007 3400 B138h
13Ch	32	CSCTI_CTICHOUTSTATUS	0007 3400 313Ch	0007 3400 A13Ch	0007 3400 B13Ch
140h	32	CSCTI_CTIGATE	0007 3400 3140h	0007 3400 A140h	0007 3400 B140h
144h	32	CSCTI_ASICCTL	0007 3400 3144h	0007 3400 A144h	0007 3400 B144h
EDCh	32	CSCTI_ITCHINACK	0007 3400 3EDCh	0007 3400 AEDCh	0007 3400 BEDCh
EE0h	32	CSCTI_ITTRIGINACK	0007 3400 3EE0h	0007 3400 AEE0h	0007 3400 BEE0h
EE4h	32	CSCTI_ITCHOUT	0007 3400 3EE4h	0007 3400 AEE4h	0007 3400 BEE4h
EE8h	32	CSCTI_ITTRIGOUT	0007 3400 3EE8h	0007 3400 AEE8h	0007 3400 BEE8h
EECh	32	CSCTI_ITCHOUTACK	0007 3400 3EECh	0007 3400 AEECh	0007 3400 BEECh
EF0h	32	CSCTI_ITTRIGOUTACK	0007 3400 3EF0h	0007 3400 AEF0h	0007 3400 BEF0h
EF4h	32	CSCTI_ITCHIN	0007 3400 3EF4h	0007 3400 AEF4h	0007 3400 BEF4h
EF8h	32	CSCTI_ITTRIGIN	0007 3400 3EF8h	0007 3400 AEF8h	0007 3400 BEF8h
F00h	32	CSCTI_ITCTRL	0007 3400 3F00h	0007 3400 AF00h	0007 3400 BF00h
FA0h	32	CSCTI_CLAIMSET	0007 3400 3FA0h	0007 3400 AFA0h	0007 3400 BFA0h
FA4h	32	CSCTI_CLAIMCLR	0007 3400 3FA4h	0007 3400 AFA4h	0007 3400 BFA4h
FB0h	32	CSCTI_LOCKACCESS	0007 3400 3FB0h	0007 3400 AFB0h	0007 3400 BFB0h
FB4h	32	CSCTI_LOCKSTATUS	0007 3400 3FB4h	0007 3400 AFB4h	0007 3400 BFB4h
FB8h	32	CSCTI_AUTHSTATUS	0007 3400 3FB8h	0007 3400 AFB8h	0007 3400 BFB8h
FC8h	32	CSCTI_DEVID	0007 3400 3FC8h	0007 3400 AFC8h	0007 3400 BFC8h
FCCh	32	CSCTI_DEVTYPE	0007 3400 3FCCh	0007 3400 AFCCh	0007 3400 BFCCh
FD0h	32	CSCTI_PERIPHID4	0007 3400 3FD0h	0007 3400 AFD0h	0007 3400 BFD0h
FE0h	32	CSCTI_PERIPHID0	0007 3400 3FE0h	0007 3400 AFE0h	0007 3400 BFE0h

Table 14-7744. CSCTI Registers, Base Address=0007 3400 3000h, Length=4096 (continued)

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address	C7X256V0_DEBUG Physical Address	C7X256V0_DEBUG Physical Address
FE4h	32	CSCTI_PERIPHID1	0007 3400 3FE4h	0007 3400 AFE4h	0007 3400 BFE4h
FE8h	32	CSCTI_PERIPHID2	0007 3400 3FE8h	0007 3400 AFE8h	0007 3400 BFE8h
FECh	32	CSCTI_PERIPHID3	0007 3400 3FECh	0007 3400 AFECh	0007 3400 BFECh
FF0h	32	CSCTI_COMPID0	0007 3400 3FF0h	0007 3400 AFF0h	0007 3400 BFF0h
FF4h	32	CSCTI_COMPID1	0007 3400 3FF4h	0007 3400 AFF4h	0007 3400 BFF4h
FF8h	32	CSCTI_COMPID2	0007 3400 3FF8h	0007 3400 AFF8h	0007 3400 BFF8h
FFCh	32	CSCTI_COMPID3	0007 3400 3FFCh	0007 3400 AFFCh	0007 3400 BFFCh

Table 14-7745. CSCTI Registers, Base Address=0007 3400 3000h, Length=4096

Offset	Length	Register Name	C7X256V1_DEBUG Physical Address	C7X256V1_DEBUG Physical Address	C7X256V1_DEBUG Physical Address
0h	32	CSCTI_CTICONTROL	0007 3800 3000h	0007 3800 A000h	0007 3800 B000h
10h	32	CSCTI_CTIINTACK	0007 3800 3010h	0007 3800 A010h	0007 3800 B010h
14h	32	CSCTI_CTIAPPSET	0007 3800 3014h	0007 3800 A014h	0007 3800 B014h
18h	32	CSCTI_CTIAPPCLR	0007 3800 3018h	0007 3800 A018h	0007 3800 B018h
1Ch	32	CSCTI_CTIAPPPULSE	0007 3800 301Ch	0007 3800 A01Ch	0007 3800 B01Ch
20h	32	CSCTI_CTIINEN0	0007 3800 3020h	0007 3800 A020h	0007 3800 B020h
24h	32	CSCTI_CTIINEN1	0007 3800 3024h	0007 3800 A024h	0007 3800 B024h
28h	32	CSCTI_CTIINEN2	0007 3800 3028h	0007 3800 A028h	0007 3800 B028h
2Ch	32	CSCTI_CTIINEN3	0007 3800 302Ch	0007 3800 A02Ch	0007 3800 B02Ch
30h	32	CSCTI_CTIINEN4	0007 3800 3030h	0007 3800 A030h	0007 3800 B030h
34h	32	CSCTI_CTIINEN5	0007 3800 3034h	0007 3800 A034h	0007 3800 B034h
38h	32	CSCTI_CTIINEN6	0007 3800 3038h	0007 3800 A038h	0007 3800 B038h
3Ch	32	CSCTI_CTIINEN7	0007 3800 303Ch	0007 3800 A03Ch	0007 3800 B03Ch
A0h	32	CSCTI_CTIOUTEN0	0007 3800 30A0h	0007 3800 A0A0h	0007 3800 B0A0h
A4h	32	CSCTI_CTIOUTEN1	0007 3800 30A4h	0007 3800 A0A4h	0007 3800 B0A4h
A8h	32	CSCTI_CTIOUTEN2	0007 3800 30A8h	0007 3800 A0A8h	0007 3800 B0A8h
ACh	32	CSCTI_CTIOUTEN3	0007 3800 30ACh	0007 3800 A0ACh	0007 3800 B0ACh
B0h	32	CSCTI_CTIOUTEN4	0007 3800 30B0h	0007 3800 A0B0h	0007 3800 B0B0h
B4h	32	CSCTI_CTIOUTEN5	0007 3800 30B4h	0007 3800 A0B4h	0007 3800 B0B4h
B8h	32	CSCTI_CTIOUTEN6	0007 3800 30B8h	0007 3800 A0B8h	0007 3800 B0B8h
BCh	32	CSCTI_CTIOUTEN7	0007 3800 30BCh	0007 3800 A0BCh	0007 3800 B0BCh
130h	32	CSCTI_CTITRIGINSTATUS	0007 3800 3130h	0007 3800 A130h	0007 3800 B130h
134h	32	CSCTI_CTITRIGOUTSTATUS	0007 3800 3134h	0007 3800 A134h	0007 3800 B134h
138h	32	CSCTI_CTICHINSTATUS	0007 3800 3138h	0007 3800 A138h	0007 3800 B138h
13Ch	32	CSCTI_CTICHOUTSTATUS	0007 3800 313Ch	0007 3800 A13Ch	0007 3800 B13Ch
140h	32	CSCTI_CTIGATE	0007 3800 3140h	0007 3800 A140h	0007 3800 B140h
144h	32	CSCTI_ASICCTL	0007 3800 3144h	0007 3800 A144h	0007 3800 B144h
EDCh	32	CSCTI_ITCHINACK	0007 3800 3EDCh	0007 3800 AEDCh	0007 3800 BEDCh
EE0h	32	CSCTI_ITTRIGINACK	0007 3800 3EE0h	0007 3800 AEE0h	0007 3800 BEE0h
EE4h	32	CSCTI_ITCHOUT	0007 3800 3EE4h	0007 3800 AEE4h	0007 3800 BEE4h
EE8h	32	CSCTI_ITTRIGOUT	0007 3800 3EE8h	0007 3800 AEE8h	0007 3800 BEE8h
EECh	32	CSCTI_ITCHOUTACK	0007 3800 3EECh	0007 3800 AEECh	0007 3800 BEECh
EF0h	32	CSCTI_ITTRIGOUTACK	0007 3800 3EF0h	0007 3800 AEF0h	0007 3800 BEF0h
EF4h	32	CSCTI_ITCHIN	0007 3800 3EF4h	0007 3800 AEF4h	0007 3800 BEF4h
EF8h	32	CSCTI_ITTRIGIN	0007 3800 3EF8h	0007 3800 AEF8h	0007 3800 BEF8h

Table 14-7745. CSCTI Registers, Base Address=0007 3400 3000h, Length=4096 (continued)

Offset	Length	Register Name	C7X256V1_DEBUG Physical Address	C7X256V1_DEBUG Physical Address	C7X256V1_DEBUG Physical Address
F00h	32	CSCTI_ITCTRL	0007 3800 3F00h	0007 3800 AF00h	0007 3800 BF00h
FA0h	32	CSCTI_CLAIMSET	0007 3800 3FA0h	0007 3800 AFA0h	0007 3800 BFA0h
FA4h	32	CSCTI_CLAIMCLR	0007 3800 3FA4h	0007 3800 AFA4h	0007 3800 BFA4h
FB0h	32	CSCTI_LOCKACCESS	0007 3800 3FB0h	0007 3800 AFB0h	0007 3800 BFB0h
FB4h	32	CSCTI_LOCKSTATUS	0007 3800 3FB4h	0007 3800 AFB4h	0007 3800 BFB4h
FB8h	32	CSCTI_AUTHSTATUS	0007 3800 3FB8h	0007 3800 AFB8h	0007 3800 BFB8h
FC8h	32	CSCTI_DEVID	0007 3800 3FC8h	0007 3800 AFC8h	0007 3800 BFC8h
FCCh	32	CSCTI_DEVTYPE	0007 3800 3FCCh	0007 3800 AFCCh	0007 3800 BFCCh
FD0h	32	CSCTI_PERIPHID4	0007 3800 3FD0h	0007 3800 AFD0h	0007 3800 BFD0h
FE0h	32	CSCTI_PERIPHID0	0007 3800 3FE0h	0007 3800 AFE0h	0007 3800 BFE0h
FE4h	32	CSCTI_PERIPHID1	0007 3800 3FE4h	0007 3800 AFE4h	0007 3800 BFE4h
FE8h	32	CSCTI_PERIPHID2	0007 3800 3FE8h	0007 3800 AFE8h	0007 3800 BFE8h
FECh	32	CSCTI_PERIPHID3	0007 3800 3FECh	0007 3800 AFECh	0007 3800 BFECh
FF0h	32	CSCTI_COMPID0	0007 3800 3FF0h	0007 3800 AFF0h	0007 3800 BFF0h
FF4h	32	CSCTI_COMPID1	0007 3800 3FF4h	0007 3800 AFF4h	0007 3800 BFF4h
FF8h	32	CSCTI_COMPID2	0007 3800 3FF8h	0007 3800 AFF8h	0007 3800 BFF8h
FFCh	32	CSCTI_COMPID3	0007 3800 3FFCh	0007 3800 AFFCh	0007 3800 BFFCh

Table 14-7746. CTSET2_CFG Registers, Base Address=0007 3400 8000h, Length=8192

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address
0h	32	CTSET2_CFG_CTSETID	0007 3400 8000h
10h	32	CTSET2_CFG_CTSETSYSCFG	0007 3400 8010h
14h	32	CTSET2_CFG_SETSTR	0007 3400 8014h
18h	32	CTSET2_CFG_DBGTIMELOW	0007 3400 8018h
1Ch	32	CTSET2_CFG_DBGTIMEHI	0007 3400 801Ch
24h	32	CTSET2_CFG_CTSETCFG	0007 3400 8024h
28h	32	CTSET2_CFG_SETSPLREG	0007 3400 8028h
30h	32	CTSET2_CFG_SETEVTENBL1	0007 3400 8030h
34h	32	CTSET2_CFG_SETEVTENBL2	0007 3400 8034h
38h	32	CTSET2_CFG_SETEVTENBL3	0007 3400 8038h
3Ch	32	CTSET2_CFG_SETEVTENBL4	0007 3400 803Ch
40h	32	CTSET2_CFG_SETEVTENBL5	0007 3400 8040h
44h	32	CTSET2_CFG_SETEVTENBL6	0007 3400 8044h
48h	32	CTSET2_CFG_SETEVTENBL7	0007 3400 8048h
4Ch	32	CTSET2_CFG_SETEVTENBL8	0007 3400 804Ch
50h	32	CTSET2_CFG_SETMSTID	0007 3400 8050h
800h	32	CTSET2_CFG_CTCNTL	0007 3400 8800h
804h	32	CTSET2_CFG_CTNUMDBG	0007 3400 8804h
808h	32	CTSET2_CFG_CTUSERACCCTL	0007 3400 8808h
820h	32	CTSET2_CFG_CTSTMCNTL	0007 3400 8820h
824h	32	CTSET2_CFG_CTSTMMSTID	0007 3400 8824h
828h	32	CTSET2_CFG_CTSTMINTVL	0007 3400 8828h
82Ch	32	CTSET2_CFG_CTSTMSEL0	0007 3400 882Ch
830h	32	CTSET2_CFG_CTSTMSEL1	0007 3400 8830h
8A0h	32	CTSET2_CFG_CTDBGSGL0	0007 3400 88A0h
8A4h	32	CTSET2_CFG_CTDBGSGL1	0007 3400 88A4h

Table 14-7746. CTSET2_CFG Registers, Base Address=0007 3400 8000h, Length=8192 (continued)

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address
8A8h	32	CTSET2_CFG_CTDBGSGL2	0007 3400 88A8h
8ACh	32	CTSET2_CFG_CTDBGSGL3	0007 3400 88ACh
8B0h	32	CTSET2_CFG_CTDBGSGL4	0007 3400 88B0h
8B4h	32	CTSET2_CFG_CTDBGSGL5	0007 3400 88B4h
8B8h	32	CTSET2_CFG_CTDBGSGL6	0007 3400 88B8h
8BCh	32	CTSET2_CFG_CTDBGSGL7	0007 3400 88BCh
9F0h	32	CTSET2_CFG_CTGNBL0	0007 3400 89F0h
9F4h	32	CTSET2_CFG_CTGNBL1	0007 3400 89F4h
9F8h	32	CTSET2_CFG_CTGRST0	0007 3400 89F8h
9FCh	32	CTSET2_CFG_CTGRST1	0007 3400 89FCh
A00h	32	CTSET2_CFG_CTCR0	0007 3400 8A00h
A04h	32	CTSET2_CFG_CTCR1	0007 3400 8A04h
A08h	32	CTSET2_CFG_CTCR2	0007 3400 8A08h
A0Ch	32	CTSET2_CFG_CTCR3	0007 3400 8A0Ch
A10h	32	CTSET2_CFG_CTCR4	0007 3400 8A10h
A14h	32	CTSET2_CFG_CTCR5	0007 3400 8A14h
A18h	32	CTSET2_CFG_CTCR6	0007 3400 8A18h
A1Ch	32	CTSET2_CFG_CTCR7	0007 3400 8A1Ch
A20h	32	CTSET2_CFG_CTCR8	0007 3400 8A20h
A24h	32	CTSET2_CFG_CTCR9	0007 3400 8A24h
A28h	32	CTSET2_CFG_CTCR10	0007 3400 8A28h
A2Ch	32	CTSET2_CFG_CTCR11	0007 3400 8A2Ch
A30h	32	CTSET2_CFG_CTCR12	0007 3400 8A30h
A34h	32	CTSET2_CFG_CTCR13	0007 3400 8A34h
A38h	32	CTSET2_CFG_CTCR14	0007 3400 8A38h
A3Ch	32	CTSET2_CFG_CTCR15	0007 3400 8A3Ch
A40h	32	CTSET2_CFG_CTCR16	0007 3400 8A40h
A44h	32	CTSET2_CFG_CTCR17	0007 3400 8A44h
A48h	32	CTSET2_CFG_CTCR18	0007 3400 8A48h
A4Ch	32	CTSET2_CFG_CTCR19	0007 3400 8A4Ch
A50h	32	CTSET2_CFG_CTCR20	0007 3400 8A50h
A54h	32	CTSET2_CFG_CTCR21	0007 3400 8A54h
A58h	32	CTSET2_CFG_CTCR22	0007 3400 8A58h
A5Ch	32	CTSET2_CFG_CTCR23	0007 3400 8A5Ch
A60h	32	CTSET2_CFG_CTCR24	0007 3400 8A60h
A64h	32	CTSET2_CFG_CTCR25	0007 3400 8A64h
A68h	32	CTSET2_CFG_CTCR26	0007 3400 8A68h
A6Ch	32	CTSET2_CFG_CTCR27	0007 3400 8A6Ch
A70h	32	CTSET2_CFG_CTCR28	0007 3400 8A70h
A74h	32	CTSET2_CFG_CTCR29	0007 3400 8A74h
A78h	32	CTSET2_CFG_CTCR30	0007 3400 8A78h
A7Ch	32	CTSET2_CFG_CTCR31	0007 3400 8A7Ch
A80h	32	CTSET2_CFG_CTOWN0	0007 3400 8A80h
A84h	32	CTSET2_CFG_CTOWN1	0007 3400 8A84h
A88h	32	CTSET2_CFG_CTOWN2	0007 3400 8A88h
A8Ch	32	CTSET2_CFG_CTOWN3	0007 3400 8A8Ch
A90h	32	CTSET2_CFG_CTOWN4	0007 3400 8A90h

Table 14-7746. CTSET2_CFG Registers, Base Address=0007 3400 8000h, Length=8192 (continued)

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address
A94h	32	CTSET2_CFG_CTOWN5	0007 3400 8A94h
A98h	32	CTSET2_CFG_CTOWN6	0007 3400 8A98h
A9Ch	32	CTSET2_CFG_CTOWN7	0007 3400 8A9Ch
AA0h	32	CTSET2_CFG_CTOWN8	0007 3400 8AA0h
AA4h	32	CTSET2_CFG_CTOWN9	0007 3400 8AA4h
AA8h	32	CTSET2_CFG_CTOWN10	0007 3400 8AA8h
AACh	32	CTSET2_CFG_CTOWN11	0007 3400 8AACh
AB0h	32	CTSET2_CFG_CTOWN12	0007 3400 8AB0h
AB4h	32	CTSET2_CFG_CTOWN13	0007 3400 8AB4h
AB8h	32	CTSET2_CFG_CTOWN14	0007 3400 8AB8h
ABCh	32	CTSET2_CFG_CTOWN15	0007 3400 8ABCh
AC0h	32	CTSET2_CFG_CTOWN16	0007 3400 8AC0h
AC4h	32	CTSET2_CFG_CTOWN17	0007 3400 8AC4h
AC8h	32	CTSET2_CFG_CTOWN18	0007 3400 8AC8h
ACCh	32	CTSET2_CFG_CTOWN19	0007 3400 8ACCh
AD0h	32	CTSET2_CFG_CTOWN20	0007 3400 8AD0h
AD4h	32	CTSET2_CFG_CTOWN21	0007 3400 8AD4h
AD8h	32	CTSET2_CFG_CTOWN22	0007 3400 8AD8h
ADCh	32	CTSET2_CFG_CTOWN23	0007 3400 8ADCh
AE0h	32	CTSET2_CFG_CTOWN24	0007 3400 8AE0h
AE4h	32	CTSET2_CFG_CTOWN25	0007 3400 8AE4h
AE8h	32	CTSET2_CFG_CTOWN26	0007 3400 8AE8h
AECh	32	CTSET2_CFG_CTOWN27	0007 3400 8AECh
AF0h	32	CTSET2_CFG_CTOWN28	0007 3400 8AF0h
AF4h	32	CTSET2_CFG_CTOWN29	0007 3400 8AF4h
AF8h	32	CTSET2_CFG_CTOWN30	0007 3400 8AF8h
AFCh	32	CTSET2_CFG_CTOWN31	0007 3400 8AFCh
B00h	32	CTSET2_CFG_CTFILT0	0007 3400 8B00h
B04h	32	CTSET2_CFG_CTFILT1	0007 3400 8B04h
B08h	32	CTSET2_CFG_CTFILT2	0007 3400 8B08h
B0Ch	32	CTSET2_CFG_CTFILT3	0007 3400 8B0Ch
B10h	32	CTSET2_CFG_CTFILT4	0007 3400 8B10h
B14h	32	CTSET2_CFG_CTFILT5	0007 3400 8B14h
B18h	32	CTSET2_CFG_CTFILT6	0007 3400 8B18h
B1Ch	32	CTSET2_CFG_CTFILT7	0007 3400 8B1Ch
B20h	32	CTSET2_CFG_CTFILT8	0007 3400 8B20h
B24h	32	CTSET2_CFG_CTFILT9	0007 3400 8B24h
B28h	32	CTSET2_CFG_CTFILT10	0007 3400 8B28h
B2Ch	32	CTSET2_CFG_CTFILT11	0007 3400 8B2Ch
B30h	32	CTSET2_CFG_CTFILT12	0007 3400 8B30h
B34h	32	CTSET2_CFG_CTFILT13	0007 3400 8B34h
B38h	32	CTSET2_CFG_CTFILT14	0007 3400 8B38h
B3Ch	32	CTSET2_CFG_CTFILT15	0007 3400 8B3Ch
B40h	32	CTSET2_CFG_CTFILT16	0007 3400 8B40h
B44h	32	CTSET2_CFG_CTFILT17	0007 3400 8B44h
B48h	32	CTSET2_CFG_CTFILT18	0007 3400 8B48h
B4Ch	32	CTSET2_CFG_CTFILT19	0007 3400 8B4Ch

Table 14-7746. CTSET2_CFG Registers, Base Address=0007 3400 8000h, Length=8192 (continued)

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address
B50h	32	CTSET2_CFG_CTFILT20	0007 3400 8B50h
B54h	32	CTSET2_CFG_CTFILT21	0007 3400 8B54h
B58h	32	CTSET2_CFG_CTFILT22	0007 3400 8B58h
B5Ch	32	CTSET2_CFG_CTFILT23	0007 3400 8B5Ch
B60h	32	CTSET2_CFG_CTFILT24	0007 3400 8B60h
B64h	32	CTSET2_CFG_CTFILT25	0007 3400 8B64h
B68h	32	CTSET2_CFG_CTFILT26	0007 3400 8B68h
B6Ch	32	CTSET2_CFG_CTFILT27	0007 3400 8B6Ch
B70h	32	CTSET2_CFG_CTFILT28	0007 3400 8B70h
B74h	32	CTSET2_CFG_CTFILT29	0007 3400 8B74h
B78h	32	CTSET2_CFG_CTFILT30	0007 3400 8B78h
B7Ch	32	CTSET2_CFG_CTFILT31	0007 3400 8B7Ch
B80h	32	CTSET2_CFG_CTCNTR0	0007 3400 8B80h
B84h	32	CTSET2_CFG_CTCNTR1	0007 3400 8B84h
B88h	32	CTSET2_CFG_CTCNTR2	0007 3400 8B88h
B8Ch	32	CTSET2_CFG_CTCNTR3	0007 3400 8B8Ch
B90h	32	CTSET2_CFG_CTCNTR4	0007 3400 8B90h
B94h	32	CTSET2_CFG_CTCNTR5	0007 3400 8B94h
B98h	32	CTSET2_CFG_CTCNTR6	0007 3400 8B98h
B9Ch	32	CTSET2_CFG_CTCNTR7	0007 3400 8B9Ch
BA0h	32	CTSET2_CFG_CTCNTR8	0007 3400 8BA0h
BA4h	32	CTSET2_CFG_CTCNTR9	0007 3400 8BA4h
BA8h	32	CTSET2_CFG_CTCNTR10	0007 3400 8BA8h
BACh	32	CTSET2_CFG_CTCNTR11	0007 3400 8BACh
BB0h	32	CTSET2_CFG_CTCNTR12	0007 3400 8BB0h
BB4h	32	CTSET2_CFG_CTCNTR13	0007 3400 8BB4h
BB8h	32	CTSET2_CFG_CTCNTR14	0007 3400 8BB8h
BBCh	32	CTSET2_CFG_CTCNTR15	0007 3400 8BBCh
BC0h	32	CTSET2_CFG_CTCNTR16	0007 3400 8BC0h
BC4h	32	CTSET2_CFG_CTCNTR17	0007 3400 8BC4h
BC8h	32	CTSET2_CFG_CTCNTR18	0007 3400 8BC8h
BCCh	32	CTSET2_CFG_CTCNTR19	0007 3400 8BCCh
BD0h	32	CTSET2_CFG_CTCNTR20	0007 3400 8BD0h
BD4h	32	CTSET2_CFG_CTCNTR21	0007 3400 8BD4h
BD8h	32	CTSET2_CFG_CTCNTR22	0007 3400 8BD8h
BDCh	32	CTSET2_CFG_CTCNTR23	0007 3400 8BDCh
BE0h	32	CTSET2_CFG_CTCNTR24	0007 3400 8BE0h
BE4h	32	CTSET2_CFG_CTCNTR25	0007 3400 8BE4h
BE8h	32	CTSET2_CFG_CTCNTR26	0007 3400 8BE8h
BECh	32	CTSET2_CFG_CTCNTR27	0007 3400 8BECh
BF0h	32	CTSET2_CFG_CTCNTR28	0007 3400 8BF0h
BF4h	32	CTSET2_CFG_CTCNTR29	0007 3400 8BF4h
BF8h	32	CTSET2_CFG_CTCNTR30	0007 3400 8BF8h
BFCh	32	CTSET2_CFG_CTCNTR31	0007 3400 8BFCh
C00h	32	CTSET2_CFG_CT_EOI	0007 3400 8C00h
C04h	32	CTSET2_CFG_CTIRQSTAT_RAW	0007 3400 8C04h
C08h	32	CTSET2_CFG_CTIRQSTAT	0007 3400 8C08h

Table 14-7746. CTSET2_CFG Registers, Base Address=0007 3400 8000h, Length=8192 (continued)

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address
C0Ch	32	CTSET2_CFG_CTIRQENABLE_SET	0007 3400 8C0Ch
C10h	32	CTSET2_CFG_CTIRQENABLE_CLR	0007 3400 8C10h
1800h	32	CTSET2_CFG_STPTCR	0007 3400 9800h
1804h	32	CTSET2_CFG_STPTID	0007 3400 9804h
1810h	32	CTSET2_CFG_STPASYNC	0007 3400 9810h
1814h	32	CTSET2_CFG_STPFFCR	0007 3400 9814h
1818h	32	CTSET2_CFG_STPFEAT1	0007 3400 9818h

Table 14-7747. C7X256V_DEBUG_DBG_AGR0_MMR Registers, Base Address=0007 3404 0000h, Length=256

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address	C7X256V1_DEBUG Physical Address
0h	32	C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_ID	0007 3404 0000h	0007 3804 0000h
4h	32	C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_CNTL	0007 3404 0004h	0007 3804 0004h
8h	32	C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_OWN	0007 3404 0008h	0007 3804 0008h
20h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT0	0007 3404 0020h	0007 3804 0020h
24h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR0	0007 3404 0024h	0007 3804 0024h
28h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA0	0007 3404 0028h	0007 3804 0028h
30h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT1	0007 3404 0030h	0007 3804 0030h
34h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR1	0007 3404 0034h	0007 3804 0034h
38h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA1	0007 3404 0038h	0007 3804 0038h
40h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT2	0007 3404 0040h	0007 3804 0040h
44h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR2	0007 3404 0044h	0007 3804 0044h
48h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA2	0007 3404 0048h	0007 3804 0048h
50h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT3	0007 3404 0050h	0007 3804 0050h
54h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR3	0007 3404 0054h	0007 3804 0054h
58h	32	C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA3	0007 3404 0058h	0007 3804 0058h

Table 14-7748. C7X256V_DEBUG_DBG_AGR0_MEM_CFG Registers, Base Address=0007 3404 0100h, Length=256

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address
0h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL	0007 3404 0100h
4h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID	0007 3404 0104h
10h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL	0007 3404 0110h

Table 14-7748. C7X256V_DEBUG_DBG_AGR0_MEM_CFG Registers, Base Address=0007 3404 0100h, Length=256 (continued)

Offset	Length	Register Name	C7X256V0_DEBUG Physical Address
14h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL	0007 3404 0114h
18h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES	0007 3404 0118h

14.3.2.3.2 C7X256V_DEBUG Registers

C7X256V_DEBUG Registers

14.3.2.3.2.1 THINMAN_REG_DBG_CAP Register

14.3.2.3.2.1.1 THINMAN_REG_DBG_CAP Register (Offset = 0h) [reset = DEC01440h]

Debug Capabilities Register This register is used by debug software to determine which debug modules are present and how many instances of each module exist.

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Table 14-7749. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0000h
C7X256V1_DEBUG	0007 3800 0000h

Figure 14-3848. THINMAN_REG_DBG_CAP Name Register

31	30	29	28	27	26	25	24
DBG_EM_SUP	DBG_RT_INT_SUP	DBG_WP_DATA_SUP	DBG_OWN_SUP	DBG_INDIRECT_SUP	DBG_SWBP_SUP	DBG_RESET_SUP	SYS_EXE_REQ
R	R	R	R	R	R	R	R
1h	1h	0h	1h	1h	1h	1h	0h
23	22	21	20	19	18	17	16
TRIG_OUTPUT	TRIG_INPUT	TRIG_CHNS		NUM_CNTRS			
R	R	R		R			
1h	1h	0h		0h			
15	14	13	12	11	10	9	8
NUM_WPS				NUM_BPS			
R				R			
1h				4h			
7	6	5	4	3	2	1	0
REV_MAJ				REV_MIN			
R				R			
4h				0h			

Table 14-7750. THINMAN_REG_DBG_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBG_EM_SUP	R	1h	EM Mode Support
30	DBG_RT_INT_SUP	R	1h	RT Mode Support
29	DBG_WP_DATA_SUP	R	0h	WP Data Qualification Support
28	DBG_OWN_SUP	R	1h	Ownership Support
27	DBG_INDIRECT_SUP	R	1h	Indirect Debug Memory Port Support
26	DBG_SWBP_SUP	R	1h	SWBP Support
25	DBG_RESET_SUP	R	1h	CPU Reset Support
24	SYS_EXE_REQ	R	0h	IDLE Status and Control
23	TRIG_OUTPUT	R	1h	Trigger Output
22	TRIG_INPUT	R	1h	Trigger Input
21:20	TRIG_CHNS	R	0h	Number of Trigger Channels Supported
19:16	NUM_CNTRS	R	0h	Number of Counters Implemented
15:12	NUM_WPS	R	1h	Number of HWWP modules implemented
11:8	NUM_BPS	R	4h	Number of HWBP modules implemented
7:4	REV_MAJ	R	4h	The Major Revision number of this module
3:0	REV_MIN	R	0h	The Minor Revision number of this module The first minor revision will be 0000b

14.3.2.3.2.2 THINMAN_REG_DBG_PID Register

14.3.2.3.2.2.1 THINMAN_REG_DBG_PID Register (Offset = 4h) [reset = 62020400h]

ThinMan Peripheral Identification Register This register is used to identify this implementation of ThinMan.

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Table 14-7751. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0004h
C7X256V1_DEBUG	0007 3800 0004h

Figure 14-3849. THINMAN_REG_DBG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BUSINESS_UNIT		FUNC			
R		R		R			
1h		2h		202h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
202h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
0h					4h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-7752. THINMAN_REG_DBG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Defines the scheme
29:28	BUSINESS_UNIT	R	2h	Business Unit
27:16	FUNC	R	202h	Functional Group
15:11	RTL	R	0h	RTL Revision
10:8	MAJOR	R	4h	Major Revision
7:6	CUSTOM	R	0h	Custom Field
5:0	MINOR	R	0h	Minor Revision

14.3.2.3.2.3 THINMAN_REG_DBG_CNTL Register

14.3.2.3.2.3.1 THINMAN_REG_DBG_CNTL Register (Offset = 10h) [reset = 200h]

Debug Control Register This register is used by debug software to control all of the basic debug functions.

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Table 14-7753. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0010h
C7X256V1_DEBUG	0007 3800 0010h

Figure 14-3850. THINMAN_REG_DBG_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED_3	CANCEL_EXE	RESERVED_2				RESET_REQ	RESERVED
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED		EXE_IGNORE_DBGM	EXE_IGNORE_HPI	EXT_HALT_EN	EXT_RUN_EN	EXT_DBG_EN	AETBP_EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	1h	0h
7	6	5	4	3	2	1	0
SINGLE_STEP_TYPE	HWBP_EN	SWBP_EN	SINGLE_STEP_EN	EXMODE		HALT_LD	HALT
R/W	R/W	R/W	R/W	R/W		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-7754. THINMAN_REG_DBG_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_3	R/W	0h	reserved
30	CANCEL_EXE	R/W	0h	Cancel Execution Control Request This bit is used to cancel an execution control request
29:26	RESERVED_2	R/W	0h	reserved
25	RESET_REQ	R/W	0h	CPU Reset Request
24:14	RESERVED	R/W	0h	reserved
13	EXE_IGNORE_DBGM	R/W	0h	Ignore DBGM When Halting This bit is used to grant privileges to ignore the DBGM flag when servicing an execution control command that halts code execution
12	EXE_IGNORE_HPI	R/W	0h	Ignore HPI This bit determines if execution requests issued via DBG_CNTL will honor or ignore HPI state
11	EXT_HALT_EN	R/W	0h	Enable for External Debug Halt Trigger This bit enables the use of the external debug halt trigger [dbg_halt_req] to support halting the CPU
10	EXT_RUN_EN	R/W	0h	Enable for External Debug Run Trigger This bit enables the use of the external debug run trigger [dbg_run_req] to support running the CPU
9	EXT_DBG_EN	R/W	1h	Enable for External Debug Enable This bit enables allows the use of the external debug enable qualifier [dbg_enable] to support debug when coming out of a non-functional state

Table 14-7754. THINMAN_REG_DBG_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	AETBP_EN	R/W	0h	AET Generated Breakpoint Halt Enable This bit enables halting on the AET imprecise breakpoint debug event
7	SINGLE_STEP_TYPE	R/W	0h	Single Step Type This bit defines the interrupt behavior while single-stepping
6	HWBP_EN	R/W	0h	Hardware Breakpoint Halt Enable NOTE: Each hardware breakpoint resource also has a local enable
5	SWBP_EN	R/W	0h	Software Breakpoint Halt Enable This bit enables halting on software breakpoint detection NOTE: If a SWBP opcode is fetched when this enable bit is not set then it is executed as a NOP
4	SINGLE_STEP_EN	R/W	0h	Single Step Execution Enable This bit enables single step operation NOTE: See DBG_CNTL:SINGLE_STEP_TYPE for additional information
3:2	EXMODE	R/W	0h	Execution Mode This bit controls the setting of the execution mode
1	HALT_LD	R/W	0h	Global Debug Run Control Load This bit determines if a DBG_CNTL register write can update the HALT field This bit is simply an enable during writes, has no storage, and is always read as zero
0	HALT	R/W	0h	Global Debug Run Control This bit controls the global execution state This bit will be read as being set upon entry to HALTED state due to the halted state being entered because of a debug event

14.3.2.3.2.4 THINMAN_REG_DBG_STAT Register

14.3.2.3.2.4.1 THINMAN_REG_DBG_STAT Register (Offset = 14h) [reset = 0h]

Debug Status Register This register provides all the required system state to the debug tools.

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Table 14-7755. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0014h
C7X256V1_DEBUG	0007 3800 0014h

Figure 14-3851. THINMAN_REG_DBG_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_4		STAT_READY	STAT_EXT_RUN_SEEN	STAT_EXT_HALT_SEEN	STAT_EXT_ENABLE	STAT_IDS	RESERVED_3
R/W		R/W	R/W	R/W	R	R	R/W
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESET_OCC	RESET_ACTIVE	CLOCK_ACTIVE	IDLE_ACTIVE	STAT_NIPERM	STAT_IPERM	STAT_PRIV_HPI	STAT_PRIV_DBGM
R/W	R	R/W	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HALT_IN_IDS	HALT_AETBP	HALT_EXT_HALT	HALT_USER	HALT_STEP	HALT_CPU_RESET	HALT_HWBP	HALT_SWBP
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2		CANCEL_IAP	CANCEL_EXE	RESTART	RESERVED	EXE_STAT	NEW_HALT
R/W		R/W	R/W	R/W	R/W	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-7756. THINMAN_REG_DBG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_4	R/W	0h	reserved
29	STAT_READY	R/W	0h	Ready Status Continuously Inactive [sticky] This bit indicates the ready status of the CPU and is used to detect a CPU hang condition It is a sticky bit A simultaneous set and clear condition causes the bit to be set
28	STAT_EXT_RUN_SEEN	R/W	0h	External Run Trigger Status This bit indicates that a qualified external run trigger was detected since the last time it was cleared It is a sticky bit A simultaneous set and clear condition causes the bit to be set
27	STAT_EXT_HALT_SEEN	R/W	0h	External Halt Trigger Status This bit indicates that a qualified external halt trigger was detected since the last time it was cleared It is a sticky bit A simultaneous set and clear condition causes the bit to be set
26	STAT_EXT_ENABLE	R	0h	External Debug Enable Qualifier Status This bit indicates the state of the external debug enable qualifier
25	STAT_IDS	R	0h	State of the Interrupt During Suspend CPU State This bit indicates that an interrupt during suspend [IDS] is being serviced by the CPU
24	RESERVED_3	R/W	0h	reserved

Table 14-7756. THINMAN_REG_DBG_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	RESET_OCC	R/W	0h	CPU Reset Occurred [sticky] This bit is used to determine if the CPU reset has been active at least one clock since the last time it was cleared This is a sticky bit A simultaneous set and clear condition causes the bit to be set NOTE: This register has no reset value, instead it is affected by the occurrence of a CPU reset
22	RESET_ACTIVE	R	0h	CPU Reset Status This bit indicates the reset state of the CPU core
21	CLOCK_ACTIVE	R/W	0h	CPU Clocks Active [sticky] This is a sticky bit which is set when a rising edge is seen on the CPUs functional clock This is a sticky bit A simultaneous set and clear condition causes the bit to be set
20	IDLE_ACTIVE	R	0h	CPU is IDLE This bit indicates the idle state of the CPU core
19	STAT_NIPERM	R	0h	State of Non-Invasive Permissions This bit indicates whether the next execute packet has Non-Invasive Permissions It is used to detect that the CPU is executing code that is not allotted Non-Invasive Debug Permissions
18	STAT_IPERM	R	0h	State of Invasive Permissions This bit indicates whether the next execute packet has Invasive Permissions It is used to detect that the CPU is executing secure code and can not be debugged
17	STAT_PRIV_HPI	R	0h	State of the HPI Privilege Window This bit indicates that a high priority interrupt has been taken but has not yet been completed
16	STAT_PRIV_DBGM	R	0h	State of the DBGM Privilege Window This bit reflects the state of the DBGM privilege window
15	HALT_IN_IDS	R	0h	Execution Halted within an Interrupt During Suspend [IDS] This bit indicates that the CPU has halted while executing an IDS
14	HALT_AETBP	R	0h	Execution Halted Due to an AET generated breakpoint This bit indicates that an AET-generated breakpoint has halted code execution
13	HALT_EXT_HALT	R	0h	Execution Halted Due to an external debug halt request
12	HALT_USER	R	0h	Execution Halted Due to a application update of the HALT bit
11	HALT_STEP	R	0h	Execution Halted Due to a Single Step This bit indicates that the halt occurred due to the completion of a single step operation
10	HALT_CPU_RESET	R	0h	Execution Halted Due to CPU Reset or a halt request made during CPU Reset
9	HALT_HWBP	R	0h	Execution Halted Due to a Hardware Breakpoint This bit indicates that the halt occurred due to the detection of a hardware breakpoint
8	HALT_SWBP	R	0h	Execution Halted Due to a SWBP This bit indicates that the halt occurred due to a software breakpoint being detected
7:6	RESERVED_2	R/W	0h	reserved
5	CANCEL_IAP	R/W	0h	Indirect Access Port Request Canceled This bit indicates that an IAP read or write request has been canceled [eg due to Port Reset, CPU Reset, New debug context] since the last time it was cleared It is a sticky bit A simultaneous set and clear condition causes the bit to be set
4	CANCEL_EXE	R/W	0h	Debug Command Request Canceled This bit indicates that a debug request has been canceled [by a NEW_HALT or by DBG_CNTL:CANCEL_EXE while a previously issued command was pending] since the last time it was cleared It is a sticky bit A simultaneous set and clear condition causes the bit to be set
3	RESTART	R/W	0h	Execution Restart This bit indicates that the core execution resumed due to a debug command since the last time it was cleared It is a sticky bit A simultaneous set and clear condition causes the bit to be set
2	RESERVED	R/W	0h	reserved
1	EXE_STAT	R	0h	Execution State This bit indicates the execution status of the CPU
0	NEW_HALT	R	0h	Debug Context Status This bit indicates that the processor has halted at a new location [or debug context] relative to the previously active debug location

14.3.2.3.2.5 THINMAN_REG_DBG_OWN Register

14.3.2.3.2.5.1 THINMAN_REG_DBG_OWN Register (Offset = 18h) [reset = 0h]

Ownership Control and Status Register

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Table 14-7757. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0018h
C7X256V1_DEBUG	0007 3800 0018h

Figure 14-3852. THINMAN_REG_DBG_OWN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					OWN		CLAIM
R/W					R/W		R/W
0h					0h		0h

Table 14-7758. THINMAN_REG_DBG_OWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R/W	0h	reserved
2:1	OWN	R/W	0h	The Ownership State
0	CLAIM	R/W	0h	This bit is used to obtain exclusive ownership of the debug module for either the debug initiator or the application initiator Reads will always return 0 If the current state is NOT_OWNED o A debugger-initiated write of 1 will claim the module for use by the debugger initiator o An application-initiated write of 1 will claim the module for use by the application initiator If the current state is DBG_OWNED o A debugger-initiated write of 0 will release ownership o A debugger-initiated write of 1 has no effect o Application writes have no effect If the current state is APP_OWNED o An application-initiated write of 0 will release ownership o A debugger-initiated write of 0 will release ownership o A write of 1 has not effect

14.3.2.3.2.6 THINMAN_REG_DBG_INDRCT_CAP0 Register

14.3.2.3.2.6.1 THINMAN_REG_DBG_INDRCT_CAP0 Register (Offset = 20h) [reset = 1200012h]

Indirect Access Port Capabilities Register

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Table 14-7759. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0020h
C7X256V1_DEBUG	0007 3800 0020h

Figure 14-3853. THINMAN_REG_DBG_INDRCT_CAP0 Name Register

31	30	29	28	27	26	25	24
PAGE3_DATA_SIZE				PAGE3_ADDR_SIZE			
R				R			
0h				1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PAGE2_DATA_SIZE				PAGE2_ADDR_SIZE			
R				R			
2h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PAGE1_DATA_SIZE				PAGE1_ADDR_SIZE			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAGE0_DATA_SIZE				PAGE0_ADDR_SIZE			
R				R			
1h				2h			

Table 14-7760. THINMAN_REG_DBG_INDRCT_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PAGE3_DATA_SIZE	R	0h	Page 3 is not implemented
27:24	PAGE3_ADDR_SIZE	R	1h	Page 3 is not implemented
23:20	PAGE2_DATA_SIZE	R	2h	Page 2 Data Size : CPU Registers
19:16	PAGE2_ADDR_SIZE	R	0h	Page 2 Address Size : CPU Registers
15:12	PAGE1_DATA_SIZE	R	0h	Page 1 is not implemented
11:8	PAGE1_ADDR_SIZE	R	0h	Page 1 is not implemented
7:4	PAGE0_DATA_SIZE	R	1h	Page 0 Data Size : Memory [Virtual]
3:0	PAGE0_ADDR_SIZE	R	2h	Page 0 Address Size : Memory [Virtual]

14.3.2.3.2.7 THINMAN_REG_DBG_INDRCT_CAP1 Register

14.3.2.3.2.7.1 THINMAN_REG_DBG_INDRCT_CAP1 Register (Offset = 24h) [reset = 0h]

Indirect Access Port Capabilities Register for Pages 4 - 7

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Table 14-7761. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0024h
C7X256V1_DEBUG	0007 3800 0024h

Figure 14-3854. THINMAN_REG_DBG_INDRCT_CAP1 Name Register

31	30	29	28	27	26	25	24
PAGE7_DATA_SIZE				PAGE7_ADDR_SIZE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
PAGE6_DATA_SIZE				PAGE6_ADDR_SIZE			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
PAGE5_DATA_SIZE				PAGE5_ADDR_SIZE			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
PAGE4_DATA_SIZE				PAGE4_ADDR_SIZE			
R				R			
0h				0h			

Table 14-7762. THINMAN_REG_DBG_INDRCT_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PAGE7_DATA_SIZE	R	0h	Page 7 is not implemented
27:24	PAGE7_ADDR_SIZE	R	0h	Page 7 is not implemented
23:20	PAGE6_DATA_SIZE	R	0h	Page 6 is not implemented
19:16	PAGE6_ADDR_SIZE	R	0h	Page 6 is not implemented
15:12	PAGE5_DATA_SIZE	R	0h	Page 5 is not implemented
11:8	PAGE5_ADDR_SIZE	R	0h	Page 5 is not implemented
7:4	PAGE4_DATA_SIZE	R	0h	Page 4 is not implemented
3:0	PAGE4_ADDR_SIZE	R	0h	Page 4 is not implemented

14.3.2.3.2.8 THINMAN_REG_DBG_INDRCT_CNTL Register

14.3.2.3.2.8.1 THINMAN_REG_DBG_INDRCT_CNTL Register (Offset = 30h) [reset = 20080000h]

Indirect Memory Control and Status Register This register is used to control the behavior of the indirect memory controller.

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Table 14-7763. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0030h
C7X256V1_DEBUG	0007 3800 0030h

Figure 14-3855. THINMAN_REG_DBG_INDRCT_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED		MEM_RESET_PORT	RESERVED	MEM_ACC_CODE			
NONE		R/W	NONE	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MEM_ERR_CODE				MEM_BUS_STAT	MEM_ERR_OVERRUN	MEM_PORT_STAT	
R				R	R	R	
0h				1h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MEM_QUAL_PSTMTRM	MEM_QUAL_VMID	MEM_QUAL_PROC	MEM_QUAL_DCTXT	RESERVED	MEM_ACC_SIZE		
R/W	R/W	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	MEM_PAGE			MEM_IGNORE_CTXT	MEM_IGNORE_DBGM	MEM_ADDR_INC	MEM_RW
NONE	R/W			R/W	R/W	R/W	R/W
0h	0h			0h	0h	0h	0h

Table 14-7764. THINMAN_REG_DBG_INDRCT_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	MEM_RESET_PORT	R/W	1h	Port Reset
28	RESERVED	NONE	0h	Reserved
27:24	MEM_ACC_CODE	R	0h	Indicates the access code returned for the last read transaction
23:20	MEM_ERR_CODE	R	0h	Indicates the bus error code returned for a transaction This field indicates the memory access error code returned by the subsystem interconnect The first non-zero error is captured and held until it is cleared by a port reset
19	MEM_BUS_STAT	R	1h	Indicates the bus status [ready state] of the processor interface selected by MEM_PAGE This bit indicates the current availability state [the bus ready value] for the interface selected by MEM_PAGE It is used by the debug agent to determine if the interface is in a hung state
18	MEM_ERR_OVERRUN	R	0h	Indicates the state of the access port This field indicates that the settings of the indirect access port [control, context, data, or address] registers have changed before a previous access completed Once it is set to 1 it stays asserted until it is cleared by a port reset

Table 14-7764. THINMAN_REG_DBG_INDRCT_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	MEM_PORT_STAT	R	0h	Pending Memory Request Completed This bit indicates the status of the memory port
15	MEM_QUAL_PSTMTRM	R/W	0h	Post Mortem Qualification This bit controls if a memory access is submitted as part of a postmortem analysis acitivty This bit will be set only when normal debug initiated accesses are no longer possible due to a system crash When set, the CPU will service an indirect access port request independent of all other memory qualifiers or normally required architectural state dependencies
14	MEM_QUAL_VMID	R/W	0h	VMID Qualification This bit controls if a VMID context match is required of accesses submitted by the indirect controller The VMID reference is programmed using DBG_INDRCT_CTXT2
13	MEM_QUAL_PROC	R/W	0h	Processor State Qualification Enable This bit controls if a processor state match is required of accesses submitted by the indirect controller The processor states of interest are programmed using DBG_INDRCT_CTXT2
12	MEM_QUAL_DCTXT	R/W	0h	Debug Context Qualification Enable This bit controls if a DCTXT context match is required of accesses submitted by the indirect controller The DCTXT reference and mask are programmed using DBG_INDRCT_CTXT0 and DBG_INDRCT_CTXT1
11	RESERVED	NONE	0h	Reserved
10:8	MEM_ACC_SIZE	R/W	0h	Access size of the next transaction
7	RESERVED	NONE	0h	Reserved
6:4	MEM_PAGE	R/W	0h	Page designator for the next access This bit defines the page index of the memory page targeted for subsequent transactions The parameters of the pages supported in the system are available in the DBG_INDRCT_CAP register
3	MEM_IGNORE_CTXT	R/W	0h	Ignore Context This bit determines whether memory/register accesses through the indirect controller will honor or ignore IDS and debug context changes
2	MEM_IGNORE_DBGM	R/W	0h	Ignore DBGM When Halting This bit is used to grant privileges to ignore the DBGM flag when servicing a request to access memory or registers via the Indirect Access Port
1	MEM_ADDR_INC	R/W	0h	Auto increment on each access This bit determines if the address used for the memory access auto-increments For read transactions, the auto-increment occurs when the previous value is read from the data registers This will automatically launch another read transaction from the new address For write transactions, the auto-increment occurs when the write completes A new write is not launched until new data is written into the data registers The auto-increment feature is disabled on any error [the bit stays set] and is not re-enabled until the error is cleared
0	MEM_RW	R/W	0h	R/W Control for next accesses This bit determines if the port is executing read or write operations

14.3.2.3.2.9 THINMAN_REG_DBG_INDRCT_CTXT0 Register

14.3.2.3.2.9.1 THINMAN_REG_DBG_INDRCT_CTXT0 Register (Offset = 34h) [reset = 0h]

Indirect Memory Context ID Register 0 This register is used to designate the desired debug context of accesses initiated via the indirect access port mechanism. Context ID Register 0 holds the reference value for the CPU register DBGCTXT. When enabled (via DBG_INDRCT_CNTL::MEM_QUAL_DCTXT) this register is used in conjunction with DBG_INDRCT_CTXT1 and the state of the CPU register DBGCTXT to determine if the debug context criteria for an indirect access port access is met.

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Table 14-7765. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0034h
C7X256V1_DEBUG	0007 3800 0034h

Figure 14-3856. THINMAN_REG_DBG_INDRCT_CTXT0 Name Register

31	30	29	28	27	26	25	24
DBGCTXT_MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGCTXT_MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGCTXT_MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGCTXT_MASK							
R/W							
0h							

Table 14-7766. THINMAN_REG_DBG_INDRCT_CTXT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGCTXT_MASK	R/W	0h	This field is used to define the context qualification mask associated with DBG_INDRCT_CTXT0 An asserted bit means the corresponding DBGCTXT_REF bit is compared

14.3.2.3.2.10 THINMAN_REG_DBG_INDRCT_CTXT1 Register

14.3.2.3.2.10.1 THINMAN_REG_DBG_INDRCT_CTXT1 Register (Offset = 38h) [reset = 0h]

Indirect Memory Context ID Register 1 This register is used to designate the desired debug context of accesses initiated via the indirect access port mechanism. Context ID Register 1 holds the MASK value for DBG_INDRCT_CTXT0.

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Table 14-7767. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0038h
C7X256V1_DEBUG	0007 3800 0038h

Figure 14-3857. THINMAN_REG_DBG_INDRCT_CTXT1 Name Register

31	30	29	28	27	26	25	24
DBGCTXT_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGCTXT_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGCTXT_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGCTXT_REF							
R/W							
0h							

Table 14-7768. THINMAN_REG_DBG_INDRCT_CTXT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGCTXT_REF	R/W	0h	When used, this field is initialized with the DBGCTXT reference value

14.3.2.3.2.11 THINMAN_REG_DBG_INDRCT_CTXT2 Register

14.3.2.3.2.11.1 THINMAN_REG_DBG_INDRCT_CTXT2 Register (Offset = 3Ch) [reset = 0h]

Indirect Memory Context ID Register 2 This register is used to designate the desired debug context of accesses initiated via the indirect access port mechanism. Context ID Register 2 holds the context criteria for processor operating modes and the VMID. When enabled (via DBG_INDRCT_CNTL::MEM_QUAL_PROC and DBG_INDRCT_CNTL::MEM_QUAL_VMID) this register is used, in conjunction with current CPU state and VMID settings, to determine if the debug context criteria for an indirect access port access is met.

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Table 14-7769. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 003Ch
C7X256V1_DEBUG	0007 3800 003Ch

Figure 14-3858. THINMAN_REG_DBG_INDRCT_CTXT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		PROC_REF					
NONE		R/W					
0h		0h					
7	6	5	4	3	2	1	0
VMID_REF							
R/W							
0h							

Table 14-7770. THINMAN_REG_DBG_INDRCT_CTXT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	PROC_REF	R/W	0h	Processor Mode Reference When enabled, this bit-field controls which processor modes the associated hardware breakpoint is active for -----0 : Inactive during Non-Root User -----1 : Active during Non-Root User ----0- : Inactive during Non-Root Supervisor ----1- : Active during Non-Root Supervisor ---0-- : Inactive during Root User ---1-- : Active during Root User --0--- : Inactive during Root Supervisor --1--- : Active during Root Supervisor -0---- : Inactive during Secure User -1---- : Active during Secure User 0----- : Inactive during Secure Supervisor 1----- : Active during Secure Supervisor
7:0	VMID_REF	R/W	0h	When used, this field is initialized with the VMID reference

14.3.2.3.2.12 THINMAN_REG_DBG_INDRCT_ADDR0 Register

14.3.2.3.2.12.1 THINMAN_REG_DBG_INDRCT_ADDR0 Register (Offset = 40h) [reset = 0h]

Indirect Memory Address Register 0

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Table 14-7771. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0040h
C7X256V1_DEBUG	0007 3800 0040h

Figure 14-3859. THINMAN_REG_DBG_INDRCT_ADDR0 Name Register

31	30	29	28	27	26	25	24
ADDR0							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR0							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR0							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR0							
R/W							
0h							

Table 14-7772. THINMAN_REG_DBG_INDRCT_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR0	R/W	0h	Low order address bits for designating the target of an indirect debug access This bit field holds the 32 LSBs of the address of an indirect debug port transaction If the port is set for auto-incrementing addresses [DBG_INDRCT_CNTL:MEM_INC_ADDR = 1], this field will be incremented by the access size each time a transaction completes

14.3.2.3.2.13 THINMAN_REG_DBG_INDRCT_ADDR1 Register

14.3.2.3.2.13.1 THINMAN_REG_DBG_INDRCT_ADDR1 Register (Offset = 44h) [reset = 0h]

Indirect Memory Address Register 1

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Table 14-7773. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0044h
C7X256V1_DEBUG	0007 3800 0044h

Figure 14-3860. THINMAN_REG_DBG_INDRCT_ADDR1 Name Register

31	30	29	28	27	26	25	24
ADDR1							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR1							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR1							
R/W							
0h							

Table 14-7774. THINMAN_REG_DBG_INDRCT_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR1	R/W	0h	High order address bits for designating the target of an indirect debug access This bit field holds the 32 MSBs of the address of an indirect debug port transaction If the port is set for auto-incrementing addresses [DBG_INDRCT_CNTL:MEM_INC_ADDR = 1], this field will be incremented by one when the DBG_INDRCT_ADDR0 rolls over

14.3.2.3.2.14 THINMAN_REG_DBG_INDRCT_DATA0 Register

14.3.2.3.2.14.1 THINMAN_REG_DBG_INDRCT_DATA0 Register (Offset = 48h) [reset = 0h]

Indirect Memory Data Register 0 Data is packed using little endian byte numbering

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Table 14-7775. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0048h
C7X256V1_DEBUG	0007 3800 0048h

Figure 14-3861. THINMAN_REG_DBG_INDRCT_DATA0 Name Register

31	30	29	28	27	26	25	24
DATA0							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA0							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA0							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA0							
R/W							
0h							

Table 14-7776. THINMAN_REG_DBG_INDRCT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA0	R/W	0h	Data bits of the read or write transaction This bit field holds bits 31:00 of the data of an indirect debug port transaction If Writing data: This register must be written after the address registers If Reading data This register will have valid read data when the transaction is complete [MEM_PORT_STAT == 10b]

14.3.2.3.2.15 THINMAN_REG_DBG_INDRCT_DATA1 Register

14.3.2.3.2.15.1 THINMAN_REG_DBG_INDRCT_DATA1 Register (Offset = 4Ch) [reset = 0h]

Indirect Memory Data Register 1 Data is packed using little endian byte numbering

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Table 14-7777. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 004Ch
C7X256V1_DEBUG	0007 3800 004Ch

Figure 14-3862. THINMAN_REG_DBG_INDRCT_DATA1 Name Register

31	30	29	28	27	26	25	24
DATA1							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA1							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA1							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA1							
R/W							
0h							

Table 14-7778. THINMAN_REG_DBG_INDRCT_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA1	R/W	0h	Data bits of the read or write transaction This bit field holds bits 63:32 of the data of an indirect debug port transaction If Writing data: This register must be written after the address registers If Reading data This register will have valid read data when the transaction is complete [MEM_PORT_STAT == 10b]

14.3.2.3.2.16 THINMAN_REG_DBG_HWBP_0_CNTL Register

14.3.2.3.2.16.1 THINMAN_REG_DBG_HWBP_0_CNTL Register (Offset = 100h) [reset = 800h]

Hardware Breakpoint 0 Control Register This is the control and status register for hardware breakpoint resources.

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Table 14-7779. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0100h
C7X256V1_DEBUG	0007 3800 0100h

Figure 14-3863. THINMAN_REG_DBG_HWBP_0_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			COUNT	COUNT_SUP	RESERVED	CRIT_PROC	CRIT_VMID
NONE			R/W	R	NONE	R/W	R/W
0h			0h	1h	0h	0h	0h
7	6	5	4	3	2	1	0
CRIT_DCTXT	RESERVED	CRIT_ADDR	RESERVED	TRIGGERED	AET_EVT	HALT	ENABLE
R/W	NONE	R/W	NONE	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7780. THINMAN_REG_DBG_HWBP_0_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	COUNT	R/W	0h	When implemented, this 20-bit count field defines the number of times an instruction address match is detected before the trigger is generated Writing n causes this hardware breakpoint resource to generate a trigger upon the [n+1]th occurrence of an instruction address match When set to 0 this hardware breakpoint resource will halt on the first occurrence of an instruction address match Reads return the current value of the supporting occurrence counter
11	COUNT_SUP	R	1h	This bit defines whether this hardware breakpoint resource supports occurrence detection via the COUNT bit-field This bit is set by implementation
10	RESERVED	NONE	0h	Reserved
9	CRIT_PROC	R/W	0h	This bit designates if the processor state match criteria is used to determine a comparison match
8	CRIT_VMID	R/W	0h	This bit designates if the VMID match criteria is used to determine a comparison match
7	CRIT_DCTXT	R/W	0h	This bit designates if the debug context match criteria is used to determine a comparison match
6	RESERVED	NONE	0h	Reserved
5	CRIT_ADDR	R/W	0h	This bit designates if the address comparison criteria is used to determine a comparison match

Table 14-7780. THINMAN_REG_DBG_HWBP_0_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	NONE	0h	Reserved
3	TRIGGERED	R/W	0h	This bit indicates that the trigger condition has been met since the last time this bit was cleared
2	AET_EVT	R/W	0h	This bit configures the module to generate an AET event when triggered
1	HALT	R/W	0h	This bit configures the module to halt the processor when triggered
0	ENABLE	R/W	0h	This is the local enable for the hardware breakpoint module

14.3.2.3.2.17 THINMAN_REG_DBG_HWBP_0_CTXT0 Register

14.3.2.3.2.17.1 THINMAN_REG_DBG_HWBP_0_CTXT0 Register (Offset = 108h) [reset = 0h]

Hardware Breakpoint Context ID Register 0 This register is used to designate the desired context of the HWBP.

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Table 14-7781. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0108h
C7X256V1_DEBUG	0007 3800 0108h

Figure 14-3864. THINMAN_REG_DBG_HWBP_0_CTXT0 Name Register

31	30	29	28	27	26	25	24
DBGCTXT_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGCTXT_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGCTXT_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGCTXT_REF							
R/W							
0h							

Table 14-7782. THINMAN_REG_DBG_HWBP_0_CTXT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGCTXT_REF	R/W	0h	When used, this field is initialized with the DBGCTXT reference value

14.3.2.3.2.18 THINMAN_REG_DBG_HWBP_0_CTXT1 Register

14.3.2.3.2.18.1 THINMAN_REG_DBG_HWBP_0_CTXT1 Register (Offset = 10Ch) [reset = 0h]

Hardware Breakpoint Context ID Register 1 This register is used to designate the desired context of the HWBP.

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Table 14-7783. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 010Ch
C7X256V1_DEBUG	0007 3800 010Ch

Figure 14-3865. THINMAN_REG_DBG_HWBP_0_CTXT1 Name Register

31	30	29	28	27	26	25	24
CONTEXT_IDMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXT_IDMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXT_IDMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXT_IDMASK							
R/W							
0h							

Table 14-7784. THINMAN_REG_DBG_HWBP_0_CTXT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXT_IDMASK	R/W	0h	This field is used to define the context qualification mask associated with DBG_HWBP_0_ID0 An asserted bit means the corresponding CONTEXT_ID bit is compared

14.3.2.3.2.19 THINMAN_REG_DBG_HWBP_0_CTXT2 Register

14.3.2.3.2.19.1 THINMAN_REG_DBG_HWBP_0_CTXT2 Register (Offset = 110h) [reset = 0h]

Hardware Breakpoint Context ID Register 2 This register is used to designate the desired context of the HWBP.

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Table 14-7785. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0110h
C7X256V1_DEBUG	0007 3800 0110h

Figure 14-3866. THINMAN_REG_DBG_HWBP_0_CTXT2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PROC_REF</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VMID_REF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7786. THINMAN_REG_DBG_HWBP_0_CTXT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PROC_REF	R/W	0h	Processor Mode Reference When enabled, this bit-field controls which processor modes the associated hardware breakpoint is active for -----0 : Inactive during Non-Root User -----1 : Active during Non-Root User ----0- : Inactive during Non-Root Supervisor ----1- : Active during Non-Root Supervisor ---0-- : Inactive during Root User ---1-- : Active during Root User --0--- : Inactive during Root Supervisor --1--- : Active during Root Supervisor -0---- : Inactive during Secure User -1---- : Active during Secure User 0----- : Inactive during Secure Supervisor 1----- : Active during Secure Supervisor
15:8	VMID_REF	R/W	0h	When used, this field is initialized with the VMID reference
7:0	RESERVED	NONE	0h	Reserved

14.3.2.3.2.20 THINMAN_REG_DBG_HWBP_0_ADDR0 Register

14.3.2.3.2.20.1 THINMAN_REG_DBG_HWBP_0_ADDR0 Register (Offset = 118h) [reset = 0h]

Hardware Breakpoint Address Register 0 This register is used to designate bits [31:2] of the execute packet address that this hardware breakpoint resource is detecting.

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Table 14-7787. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0118h
C7X256V1_DEBUG	0007 3800 0118h

Figure 14-3867. THINMAN_REG_DBG_HWBP_0_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">ADDR0</td><td>RESERVED</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7788. THINMAN_REG_DBG_HWBP_0_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ADDR0	R/W	0h	Program Address Reference [31:2] This field is initialized with the most significant 30-bits of the least significant 32-bits of the execute packet in which this hardware breakpoint resource is detecting
0	RESERVED	R/W	0h	reserved

14.3.2.3.2.21 THINMAN_REG_DBG_HWBP_0_ADDR1 Register

14.3.2.3.2.21.1 THINMAN_REG_DBG_HWBP_0_ADDR1 Register (Offset = 11Ch) [reset = 0h]

Hardware Breakpoint Address Register 1 This register is used to designate bits [63:32] of the execute packet address that this hardware breakpoint resource is detecting.

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Table 14-7789. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 011Ch
C7X256V1_DEBUG	0007 3800 011Ch

Figure 14-3868. THINMAN_REG_DBG_HWBP_0_ADDR1 Name Register

31	30	29	28	27	26	25	24
ADDR1							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR1							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR1							
R/W							
0h							

Table 14-7790. THINMAN_REG_DBG_HWBP_0_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR1	R/W	0h	Program Address Reference [63:32] This field is initialized with the most significant 32-bits of a 64-bit address corresponding to the execute packet in which this hardware breakpoint resource is detecting

14.3.2.3.2.22 THINMAN_REG_DBG_HWBP_0_AMASK0 Register

14.3.2.3.2.22.1 THINMAN_REG_DBG_HWBP_0_AMASK0 Register (Offset = 120h) [reset = FFFFFFFEh]

Hardware Breakpoint Address Mask Register 0 This register designates the LS 32-bits of the address qualifier mask

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Table 14-7791. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0120h
C7X256V1_DEBUG	0007 3800 0120h

Figure 14-3869. THINMAN_REG_DBG_HWBP_0_AMASK0 Name Register

31	30	29	28	27	26	25	24
AMASK0							
R/W							
7FFFFFFFh							
23	22	21	20	19	18	17	16
AMASK0							
R/W							
7FFFFFFFh							
15	14	13	12	11	10	9	8
AMASK0							
R/W							
7FFFFFFFh							
7	6	5	4	3	2	1	0
AMASK0							RESERVED
R/W							R/W
7FFFFFFFh							0h

Table 14-7792. THINMAN_REG_DBG_HWBP_0_AMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	AMASK0	R/W	7FFFFFFFh	Program Address Reference [63:32] This field is initialized with the most significant 32-bits of a 64-bit address corresponding to the execute packet in which this hardware breakpoint resource is detecting
0	RESERVED	R/W	0h	reserved

14.3.2.3.2.23 THINMAN_REG_DBG_HWBP_0_AMASK1 Register

14.3.2.3.2.23.1 THINMAN_REG_DBG_HWBP_0_AMASK1 Register (Offset = 124h) [reset = FFFFFFFFh]

Hardware Breakpoint Address Mask Register 1 This register designates the MS 32-bits of the address qualifier mask.

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Table 14-7793. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0124h
C7X256V1_DEBUG	0007 3800 0124h

Figure 14-3870. THINMAN_REG_DBG_HWBP_0_AMASK1 Name Register

31	30	29	28	27	26	25	24
AMASK1							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
AMASK1							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
AMASK1							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
AMASK1							
R/W							
FFFFFFFFh							

Table 14-7794. THINMAN_REG_DBG_HWBP_0_AMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AMASK1	R/W	FFFFFFFFh	Program Address Mask [63:32] This field is used as an address qualification mask for this hardware breakpoint resource An asserted bit means the corresponding address bit is compared

14.3.2.3.2.24 THINMAN_REG_DBG_HWBP_1_CNTL Register

14.3.2.3.2.24.1 THINMAN_REG_DBG_HWBP_1_CNTL Register (Offset = 180h) [reset = 0h]

Hardware Breakpoint 0 Control Register This is the control and status register for hardware breakpoint resources.

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Table 14-7795. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0180h
C7X256V1_DEBUG	0007 3800 0180h

Figure 14-3871. THINMAN_REG_DBG_HWBP_1_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			COUNT	COUNT_SUP	RESERVED	CRIT_PROC	CRIT_VMID
NONE			R/W	R	NONE	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CRIT_DCTXT	RESERVED	CRIT_ADDR	RESERVED	TRIGGERED	AET_EVT	HALT	ENABLE
R/W	NONE	R/W	NONE	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7796. THINMAN_REG_DBG_HWBP_1_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	COUNT	R/W	0h	When implemented, this 20-bit count field defines the number of times an instruction address match is detected before the trigger is generated Writing n causes this hardware breakpoint resource to generate a trigger upon the [n+1]th occurrence of an instruction address match When set to 0 this hardware breakpoint resource will halt on the first occurrence of an instruction address match Reads return the current value of the supporting occurrence counter
11	COUNT_SUP	R	0h	This bit defines whether this hardware breakpoint resource supports occurrence detection via the COUNT bit-field This bit is set by implementation
10	RESERVED	NONE	0h	Reserved
9	CRIT_PROC	R/W	0h	This bit designates if the processor state match criteria is used to determine a comparison match
8	CRIT_VMID	R/W	0h	This bit designates if the VMID match criteria is used to determine a comparison match
7	CRIT_DCTXT	R/W	0h	This bit designates if the debug context match criteria is used to determine a comparison match
6	RESERVED	NONE	0h	Reserved
5	CRIT_ADDR	R/W	0h	This bit designates if the address comparison criteria is used to determine a comparison match

Table 14-7796. THINMAN_REG_DBG_HWBP_1_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	NONE	0h	Reserved
3	TRIGGERED	R/W	0h	This bit indicates that the trigger condition has been met since the last time this bit was cleared
2	AET_EVT	R/W	0h	This bit configures the module to generate an AET event when triggered
1	HALT	R/W	0h	This bit configures the module to halt the processor when triggered
0	ENABLE	R/W	0h	This is the local enable for the hardware breakpoint module

14.3.2.3.2.25 THINMAN_REG_DBG_HWBP_1_CTXT0 Register

14.3.2.3.2.25.1 THINMAN_REG_DBG_HWBP_1_CTXT0 Register (Offset = 188h) [reset = 0h]

Hardware Breakpoint Context ID Register 0 This register is used to designate the desired context of the HWBP.

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Table 14-7797. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0188h
C7X256V1_DEBUG	0007 3800 0188h

Figure 14-3872. THINMAN_REG_DBG_HWBP_1_CTXT0 Name Register

31	30	29	28	27	26	25	24
DBGCTXT_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGCTXT_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGCTXT_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGCTXT_REF							
R/W							
0h							

Table 14-7798. THINMAN_REG_DBG_HWBP_1_CTXT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGCTXT_REF	R/W	0h	When used, this field is initialized with the DBGCTXT reference value

14.3.2.3.2.26 THINMAN_REG_DBG_HWBP_1_CTXT1 Register

14.3.2.3.2.26.1 THINMAN_REG_DBG_HWBP_1_CTXT1 Register (Offset = 18Ch) [reset = 0h]

Hardware Breakpoint Context ID Register 1 This register is used to designate the desired context of the HWBP.

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Table 14-7799. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 018Ch
C7X256V1_DEBUG	0007 3800 018Ch

Figure 14-3873. THINMAN_REG_DBG_HWBP_1_CTXT1 Name Register

31	30	29	28	27	26	25	24
CONTEXT_IDMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXT_IDMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXT_IDMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXT_IDMASK							
R/W							
0h							

Table 14-7800. THINMAN_REG_DBG_HWBP_1_CTXT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXT_IDMASK	R/W	0h	This field is used to define the context qualification mask associated with DBG_HWBP_0_ID0 An asserted bit means the corresponding CONTEXT_ID bit is compared

14.3.2.3.2.27 THINMAN_REG_DBG_HWBP_1_CTXT2 Register

14.3.2.3.2.27.1 THINMAN_REG_DBG_HWBP_1_CTXT2 Register (Offset = 190h) [reset = 0h]

Hardware Breakpoint Context ID Register 2 This register is used to designate the desired context of the HWBP.

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Table 14-7801. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0190h
C7X256V1_DEBUG	0007 3800 0190h

Figure 14-3874. THINMAN_REG_DBG_HWBP_1_CTXT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		PROC_REF					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
VMID_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7802. THINMAN_REG_DBG_HWBP_1_CTXT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PROC_REF	R/W	0h	Processor Mode Reference When enabled, this bit-field controls which processor modes the associated hardware breakpoint is active for -----0 : Inactive during Non-Root User -----1 : Active during Non-Root User ----0- : Inactive during Non-Root Supervisor ----1- : Active during Non-Root Supervisor ---0-- : Inactive during Root User ---1-- : Active during Root User --0--- : Inactive during Root Supervisor --1--- : Active during Root Supervisor -0---- : Inactive during Secure User -1---- : Active during Secure User 0----- : Inactive during Secure Supervisor 1----- : Active during Secure Supervisor
15:8	VMID_REF	R/W	0h	When used, this field is initialized with the VMID reference
7:0	RESERVED	NONE	0h	Reserved

14.3.2.3.2.28 THINMAN_REG_DBG_HWBP_1_ADDR0 Register

14.3.2.3.2.28.1 THINMAN_REG_DBG_HWBP_1_ADDR0 Register (Offset = 198h) [reset = 0h]

Hardware Breakpoint Address Register 0 This register is used to designate bits [31:2] of the execute packet address that this hardware breakpoint resource is detecting.

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Table 14-7803. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0198h
C7X256V1_DEBUG	0007 3800 0198h

Figure 14-3875. THINMAN_REG_DBG_HWBP_1_ADDR0 Name Register

31	30	29	28	27	26	25	24
ADDR0							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR0							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR0							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR0							RESERVED
R/W							R/W
0h							0h

Table 14-7804. THINMAN_REG_DBG_HWBP_1_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ADDR0	R/W	0h	Program Address Reference [31:2] This field is initialized with the most significant 30-bits of the least significant 32-bits of the execute packet in which this hardware breakpoint resource is detecting
0	RESERVED	R/W	0h	reserved

14.3.2.3.2.29 THINMAN_REG_DBG_HWBP_1_ADDR1 Register

14.3.2.3.2.29.1 THINMAN_REG_DBG_HWBP_1_ADDR1 Register (Offset = 19Ch) [reset = 0h]

Hardware Breakpoint Address Register 1 This register is used to designate bits [63:32] of the execute packet address that this hardware breakpoint resource is detecting.

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Table 14-7805. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 019Ch
C7X256V1_DEBUG	0007 3800 019Ch

Figure 14-3876. THINMAN_REG_DBG_HWBP_1_ADDR1 Name Register

31	30	29	28	27	26	25	24
ADDR1							
R/W							
0h							

23	22	21	20	19	18	17	16
ADDR1							
R/W							
0h							

15	14	13	12	11	10	9	8
ADDR1							
R/W							
0h							

7	6	5	4	3	2	1	0
ADDR1							
R/W							
0h							

Table 14-7806. THINMAN_REG_DBG_HWBP_1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR1	R/W	0h	Program Address Reference [63:32] This field is initialized with the most significant 32-bits of a 64-bit address corresponding to the execute packet in which this hardware breakpoint resource is detecting

14.3.2.3.2.30 THINMAN_REG_DBG_HWBP_1_AMASK0 Register

14.3.2.3.2.30.1 THINMAN_REG_DBG_HWBP_1_AMASK0 Register (Offset = 1A0h) [reset = FFFFFFFEh]

Hardware Breakpoint Address Mask Register 0 This register designates the LS 32-bits of the address qualifier mask

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Table 14-7807. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 01A0h
C7X256V1_DEBUG	0007 3800 01A0h

Figure 14-3877. THINMAN_REG_DBG_HWBP_1_AMASK0 Name Register

31	30	29	28	27	26	25	24
AMASK0							
R/W							
7FFFFFFFh							
23	22	21	20	19	18	17	16
AMASK0							
R/W							
7FFFFFFFh							
15	14	13	12	11	10	9	8
AMASK0							
R/W							
7FFFFFFFh							
7	6	5	4	3	2	1	0
AMASK0							RESERVED
R/W							R/W
7FFFFFFFh							0h

Table 14-7808. THINMAN_REG_DBG_HWBP_1_AMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	AMASK0	R/W	7FFFFFFFh	Program Address Reference [63:32] This field is initialized with the most significant 32-bits of a 64-bit address corresponding to the execute packet in which this hardware breakpoint resource is detecting
0	RESERVED	R/W	0h	reserved

14.3.2.3.2.31 THINMAN_REG_DBG_HWBP_1_AMASK1 Register

14.3.2.3.2.31.1 THINMAN_REG_DBG_HWBP_1_AMASK1 Register (Offset = 1A4h) [reset = FFFFFFFFh]

Hardware Breakpoint Address Mask Register 1 This register designates the MS 32-bits of the address qualifier mask.

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Table 14-7809. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 01A4h
C7X256V1_DEBUG	0007 3800 01A4h

Figure 14-3878. THINMAN_REG_DBG_HWBP_1_AMASK1 Name Register

31	30	29	28	27	26	25	24
AMASK1							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
AMASK1							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
AMASK1							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
AMASK1							
R/W							
FFFFFFFFh							

Table 14-7810. THINMAN_REG_DBG_HWBP_1_AMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AMASK1	R/W	FFFFFFFFh	Program Address Mask [63:32] This field is used as an address qualification mask for this hardware breakpoint resource An asserted bit means the corresponding address bit is compared

14.3.2.3.2.32 THINMAN_REG_DBG_HWBP_2_CNTL Register

14.3.2.3.2.32.1 THINMAN_REG_DBG_HWBP_2_CNTL Register (Offset = 200h) [reset = 0h]

Hardware Breakpoint 0 Control Register This is the control and status register for hardware breakpoint resources.

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Table 14-7811. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0200h
C7X256V1_DEBUG	0007 3800 0200h

Figure 14-3879. THINMAN_REG_DBG_HWBP_2_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			COUNT	COUNT_SUP	RESERVED	CRIT_PROC	CRIT_VMID
NONE			R/W	R	NONE	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CRIT_DCTXT	RESERVED	CRIT_ADDR	RESERVED	TRIGGERED	AET_EVT	HALT	ENABLE
R/W	NONE	R/W	NONE	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7812. THINMAN_REG_DBG_HWBP_2_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	COUNT	R/W	0h	When implemented, this 20-bit count field defines the number of times an instruction address match is detected before the trigger is generated Writing n causes this hardware breakpoint resource to generate a trigger upon the [n+1]th occurrence of an instruction address match When set to 0 this hardware breakpoint resource will halt on the first occurrence of an instruction address match Reads return the current value of the supporting occurrence counter
11	COUNT_SUP	R	0h	This bit defines whether this hardware breakpoint resource supports occurrence detection via the COUNT bit-field This bit is set by implementation
10	RESERVED	NONE	0h	Reserved
9	CRIT_PROC	R/W	0h	This bit designates if the processor state match criteria is used to determine a comparison match
8	CRIT_VMID	R/W	0h	This bit designates if the VMID match criteria is used to determine a comparison match
7	CRIT_DCTXT	R/W	0h	This bit designates if the debug context match criteria is used to determine a comparison match
6	RESERVED	NONE	0h	Reserved
5	CRIT_ADDR	R/W	0h	This bit designates if the address comparison criteria is used to determine a comparison match

Table 14-7812. THINMAN_REG_DBG_HWBP_2_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	NONE	0h	Reserved
3	TRIGGERED	R/W	0h	This bit indicates that the trigger condition has been met since the last time this bit was cleared
2	AET_EVT	R/W	0h	This bit configures the module to generate an AET event when triggered
1	HALT	R/W	0h	This bit configures the module to halt the processor when triggered
0	ENABLE	R/W	0h	This is the local enable for the hardware breakpoint module

14.3.2.3.2.33 THINMAN_REG_DBG_HWBP_2_CTXT0 Register

14.3.2.3.2.33.1 THINMAN_REG_DBG_HWBP_2_CTXT0 Register (Offset = 208h) [reset = 0h]

Hardware Breakpoint Context ID Register 1 This register is used to designate the desired context of the HWBP.

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Table 14-7813. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0208h
C7X256V1_DEBUG	0007 3800 0208h

Figure 14-3880. THINMAN_REG_DBG_HWBP_2_CTXT0 Name Register

31	30	29	28	27	26	25	24
DBGCTXT_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGCTXT_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGCTXT_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGCTXT_REF							
R/W							
0h							

Table 14-7814. THINMAN_REG_DBG_HWBP_2_CTXT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGCTXT_REF	R/W	0h	When used, this field is initialized with the DBGCTXT reference value

14.3.2.3.2.34 THINMAN_REG_DBG_HWBP_2_CTXT1 Register

14.3.2.3.2.34.1 THINMAN_REG_DBG_HWBP_2_CTXT1 Register (Offset = 20Ch) [reset = 0h]

Hardware Breakpoint Context ID Register 1 This register is used to designate the desired context of the HWBP.

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Table 14-7815. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 020Ch
C7X256V1_DEBUG	0007 3800 020Ch

Figure 14-3881. THINMAN_REG_DBG_HWBP_2_CTXT1 Name Register

31	30	29	28	27	26	25	24
CONTEXT_IDMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXT_IDMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXT_IDMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXT_IDMASK							
R/W							
0h							

Table 14-7816. THINMAN_REG_DBG_HWBP_2_CTXT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXT_IDMASK	R/W	0h	This field is used to define the context qualification mask associated with DBG_HWBP_0_ID0 An asserted bit means the corresponding CONTEXT_ID bit is compared

14.3.2.3.2.35 THINMAN_REG_DBG_HWBP_2_CTXT2 Register

14.3.2.3.2.35.1 THINMAN_REG_DBG_HWBP_2_CTXT2 Register (Offset = 210h) [reset = 0h]

Hardware Breakpoint Context ID Register 2 This register is used to designate the desired context of the HWBP.

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Table 14-7817. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0210h
C7X256V1_DEBUG	0007 3800 0210h

Figure 14-3882. THINMAN_REG_DBG_HWBP_2_CTXT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED		PROC_REF					
NONE		R/W					
0h		0h					

15	14	13	12	11	10	9	8
VMID_REF							
R/W							
0h							

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-7818. THINMAN_REG_DBG_HWBP_2_CTXT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PROC_REF	R/W	0h	Processor Mode Reference When enabled, this bit-field controls which processor modes the associated hardware breakpoint is active for -----0 : Inactive during Non-Root User -----1 : Active during Non-Root User ----0- : Inactive during Non-Root Supervisor ----1- : Active during Non-Root Supervisor ---0-- : Inactive during Root User ---1-- : Active during Root User --0--- : Inactive during Root Supervisor --1--- : Active during Root Supervisor -0---- : Inactive during Secure User -1---- : Active during Secure User 0----- : Inactive during Secure Supervisor 1----- : Active during Secure Supervisor
15:8	VMID_REF	R/W	0h	When used, this field is initialized with the VMID reference
7:0	RESERVED	NONE	0h	Reserved

14.3.2.3.2.36 THINMAN_REG_DBG_HWBP_2_ADDR0 Register

14.3.2.3.2.36.1 THINMAN_REG_DBG_HWBP_2_ADDR0 Register (Offset = 218h) [reset = 0h]

Hardware Breakpoint Address Register 0 This register is used to designate bits [31:2] of the execute packet address that this hardware breakpoint resource is detecting.

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Table 14-7819. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0218h
C7X256V1_DEBUG	0007 3800 0218h

Figure 14-3883. THINMAN_REG_DBG_HWBP_2_ADDR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">ADDR0</td><td>RESERVED</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7820. THINMAN_REG_DBG_HWBP_2_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ADDR0	R/W	0h	Program Address Reference [31:2] This field is initialized with the most significant 30-bits of the least significant 32-bits of the execute packet in which this hardware breakpoint resource is detecting
0	RESERVED	R/W	0h	reserved

14.3.2.3.2.37 THINMAN_REG_DBG_HWBP_2_ADDR1 Register

14.3.2.3.2.37.1 THINMAN_REG_DBG_HWBP_2_ADDR1 Register (Offset = 21Ch) [reset = 0h]

Hardware Breakpoint Address Register 1 This register is used to designate bits [63:32] of the execute packet address that this hardware breakpoint resource is detecting.

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Table 14-7821. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 021Ch
C7X256V1_DEBUG	0007 3800 021Ch

Figure 14-3884. THINMAN_REG_DBG_HWBP_2_ADDR1 Name Register

31	30	29	28	27	26	25	24
ADDR1							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR1							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR1							
R/W							
0h							

Table 14-7822. THINMAN_REG_DBG_HWBP_2_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR1	R/W	0h	Program Address Reference [63:32] This field is initialized with the most significant 32-bits of a 64-bit address corresponding to the execute packet in which this hardware breakpoint resource is detecting

14.3.2.3.2.38 THINMAN_REG_DBG_HWBP_2_AMASK0 Register

14.3.2.3.2.38.1 THINMAN_REG_DBG_HWBP_2_AMASK0 Register (Offset = 220h) [reset = FFFFFFFEh]

Hardware Breakpoint Address Mask Register 0 This register designates the LS 32-bits of the address qualifier mask

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Table 14-7823. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0220h
C7X256V1_DEBUG	0007 3800 0220h

Figure 14-3885. THINMAN_REG_DBG_HWBP_2_AMASK0 Name Register

31	30	29	28	27	26	25	24
AMASK0							
R/W							
7FFFFFFFh							
23	22	21	20	19	18	17	16
AMASK0							
R/W							
7FFFFFFFh							
15	14	13	12	11	10	9	8
AMASK0							
R/W							
7FFFFFFFh							
7	6	5	4	3	2	1	0
AMASK0							RESERVED
R/W							R/W
7FFFFFFFh							0h

Table 14-7824. THINMAN_REG_DBG_HWBP_2_AMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	AMASK0	R/W	7FFFFFFFh	Program Address Reference [63:32] This field is initialized with the most significant 32-bits of a 64-bit address corresponding to the execute packet in which this hardware breakpoint resource is detecting
0	RESERVED	R/W	0h	reserved

14.3.2.3.2.39 THINMAN_REG_DBG_HWBP_2_AMASK1 Register

14.3.2.3.2.39.1 THINMAN_REG_DBG_HWBP_2_AMASK1 Register (Offset = 224h) [reset = FFFFFFFFh]

Hardware Breakpoint Address Mask Register 1 This register designates the MS 32-bits of the address qualifier mask.

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Table 14-7825. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0224h
C7X256V1_DEBUG	0007 3800 0224h

Figure 14-3886. THINMAN_REG_DBG_HWBP_2_AMASK1 Name Register

31	30	29	28	27	26	25	24
AMASK1							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
AMASK1							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
AMASK1							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
AMASK1							
R/W							
FFFFFFFFh							

Table 14-7826. THINMAN_REG_DBG_HWBP_2_AMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AMASK1	R/W	FFFFFFFFh	Program Address Mask [63:32] This field is used as an address qualification mask for this hardware breakpoint resource An asserted bit means the corresponding address bit is compared

14.3.2.3.2.40 THINMAN_REG_DBG_HWBP_3_CNTL Register

14.3.2.3.2.40.1 THINMAN_REG_DBG_HWBP_3_CNTL Register (Offset = 280h) [reset = 0h]

Hardware Breakpoint 0 Control Register This is the control and status register for hardware breakpoint resources.

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Table 14-7827. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0280h
C7X256V1_DEBUG	0007 3800 0280h

Figure 14-3887. THINMAN_REG_DBG_HWBP_3_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			COUNT	COUNT_SUP	RESERVED	CRIT_PROC	CRIT_VMID
NONE			R/W	R	NONE	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CRIT_DCTXT	RESERVED	CRIT_ADDR	RESERVED	TRIGGERED	AET_EVT	HALT	ENABLE
R/W	NONE	R/W	NONE	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7828. THINMAN_REG_DBG_HWBP_3_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	COUNT	R/W	0h	When implemented, this 20-bit count field defines the number of times an instruction address match is detected before the trigger is generated Writing n causes this hardware breakpoint resource to generate a trigger upon the [n+1]th occurrence of an instruction address match When set to 0 this hardware breakpoint resource will halt on the first occurrence of an instruction address match Reads return the current value of the supporting occurrence counter
11	COUNT_SUP	R	0h	This bit defines whether this hardware breakpoint resource supports occurrence detection via the COUNT bit-field This bit is set by implementation
10	RESERVED	NONE	0h	Reserved
9	CRIT_PROC	R/W	0h	This bit designates if the processor state match criteria is used to determine a comparison match
8	CRIT_VMID	R/W	0h	This bit designates if the VMID match criteria is used to determine a comparison match
7	CRIT_DCTXT	R/W	0h	This bit designates if the debug context match criteria is used to determine a comparison match
6	RESERVED	NONE	0h	Reserved
5	CRIT_ADDR	R/W	0h	This bit designates if the address comparison criteria is used to determine a comparison match

Table 14-7828. THINMAN_REG_DBG_HWBP_3_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	NONE	0h	Reserved
3	TRIGGERED	R/W	0h	This bit indicates that the trigger condition has been met since the last time this bit was cleared
2	AET_EVT	R/W	0h	This bit configures the module to generate an AET event when triggered
1	HALT	R/W	0h	This bit configures the module to halt the processor when triggered
0	ENABLE	R/W	0h	This is the local enable for the hardware breakpoint module

14.3.2.3.2.41 THINMAN_REG_DBG_HWBP_3_CTXT0 Register

14.3.2.3.2.41.1 THINMAN_REG_DBG_HWBP_3_CTXT0 Register (Offset = 288h) [reset = 0h]

Hardware Breakpoint Context ID Register 0 This register is used to designate the desired context of the HWBP.

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Table 14-7829. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0288h
C7X256V1_DEBUG	0007 3800 0288h

Figure 14-3888. THINMAN_REG_DBG_HWBP_3_CTXT0 Name Register

31	30	29	28	27	26	25	24
DBGCTXT_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGCTXT_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGCTXT_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGCTXT_REF							
R/W							
0h							

Table 14-7830. THINMAN_REG_DBG_HWBP_3_CTXT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGCTXT_REF	R/W	0h	When used, this field is initialized with the DBGCTXT reference value

14.3.2.3.2.42 THINMAN_REG_DBG_HWBP_3_CTXT1 Register

14.3.2.3.2.42.1 THINMAN_REG_DBG_HWBP_3_CTXT1 Register (Offset = 28Ch) [reset = 0h]

Hardware Breakpoint Context ID Register 1 This register is used to designate the desired context of the HWBP.

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Table 14-7831. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 028Ch
C7X256V1_DEBUG	0007 3800 028Ch

Figure 14-3889. THINMAN_REG_DBG_HWBP_3_CTXT1 Name Register

31	30	29	28	27	26	25	24
CONTEXT_IDMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXT_IDMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXT_IDMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXT_IDMASK							
R/W							
0h							

Table 14-7832. THINMAN_REG_DBG_HWBP_3_CTXT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXT_IDMASK	R/W	0h	This field is used to define the context qualification mask associated with DBG_HWBP_0_ID0 An asserted bit means the corresponding CONTEXT_ID bit is compared

14.3.2.3.2.43 THINMAN_REG_DBG_HWBP_3_CTXT2 Register

14.3.2.3.2.43.1 THINMAN_REG_DBG_HWBP_3_CTXT2 Register (Offset = 290h) [reset = 0h]

Hardware Breakpoint Context ID Register 2 This register is used to designate the desired context of the HWBP.

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Table 14-7833. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0290h
C7X256V1_DEBUG	0007 3800 0290h

Figure 14-3890. THINMAN_REG_DBG_HWBP_3_CTXT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		PROC_REF					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VMID_REF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-7834. THINMAN_REG_DBG_HWBP_3_CTXT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PROC_REF	R/W	0h	Processor Mode Reference When enabled, this bit-field controls which processor modes the associated hardware breakpoint is active for -----0 : Inactive during Non-Root User -----1 : Active during Non-Root User ----0- : Inactive during Non-Root Supervisor ----1- : Active during Non-Root Supervisor ---0-- : Inactive during Root User ---1-- : Active during Root User --0--- : Inactive during Root Supervisor --1--- : Active during Root Supervisor -0---- : Inactive during Secure User -1---- : Active during Secure User 0----- : Inactive during Secure Supervisor 1----- : Active during Secure Supervisor
15:8	VMID_REF	R/W	0h	When used, this field is initialized with the VMID reference
7:0	RESERVED	NONE	0h	Reserved

14.3.2.3.2.44 THINMAN_REG_DBG_HWBP_3_ADDR0 Register

14.3.2.3.2.44.1 THINMAN_REG_DBG_HWBP_3_ADDR0 Register (Offset = 298h) [reset = 0h]

Hardware Breakpoint Address Register 0 This register is used to designate bits [31:2] of the execute packet address that this hardware breakpoint resource is detecting.

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Table 14-7835. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0298h
C7X256V1_DEBUG	0007 3800 0298h

Figure 14-3891. THINMAN_REG_DBG_HWBP_3_ADDR0 Name Register

31	30	29	28	27	26	25	24
ADDR0							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR0							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR0							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR0							RESERVED
R/W							R/W
0h							0h

Table 14-7836. THINMAN_REG_DBG_HWBP_3_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	ADDR0	R/W	0h	Program Address Reference [31:2] This field is initialized with the most significant 30-bits of the least significant 32-bits of the execute packet in which this hardware breakpoint resource is detecting
0	RESERVED	R/W	0h	reserved

14.3.2.3.2.45 THINMAN_REG_DBG_HWBP_3_ADDR1 Register

14.3.2.3.2.45.1 THINMAN_REG_DBG_HWBP_3_ADDR1 Register (Offset = 29Ch) [reset = 0h]

Hardware Breakpoint Address Register 1 This register is used to designate bits [63:32] of the execute packet address that this hardware breakpoint resource is detecting.

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Table 14-7837. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 029Ch
C7X256V1_DEBUG	0007 3800 029Ch

Figure 14-3892. THINMAN_REG_DBG_HWBP_3_ADDR1 Name Register

31	30	29	28	27	26	25	24
ADDR1							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR1							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR1							
R/W							
0h							

Table 14-7838. THINMAN_REG_DBG_HWBP_3_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR1	R/W	0h	Program Address Reference [63:32] This field is initialized with the most significant 32-bits of a 64-bit address corresponding to the execute packet in which this hardware breakpoint resource is detecting

14.3.2.3.2.46 THINMAN_REG_DBG_HWBP_3_AMASK0 Register

14.3.2.3.2.46.1 THINMAN_REG_DBG_HWBP_3_AMASK0 Register (Offset = 2A0h) [reset = FFFFFFFEh]

Hardware Breakpoint Address Mask Register 0 This register designates the LS 32-bits of the address qualifier mask

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Table 14-7839. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 02A0h
C7X256V1_DEBUG	0007 3800 02A0h

Figure 14-3893. THINMAN_REG_DBG_HWBP_3_AMASK0 Name Register

31	30	29	28	27	26	25	24
AMASK0							
R/W							
7FFFFFFFh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AMASK0							
R/W							
7FFFFFFFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AMASK0							
R/W							
7FFFFFFFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AMASK0							RESERVED
R/W							R/W
7FFFFFFFh							0h

Table 14-7840. THINMAN_REG_DBG_HWBP_3_AMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	AMASK0	R/W	7FFFFFFFh	Program Address Reference [63:32] This field is initialized with the most significant 32-bits of a 64-bit address corresponding to the execute packet in which this hardware breakpoint resource is detecting
0	RESERVED	R/W	0h	reserved

14.3.2.3.2.47 THINMAN_REG_DBG_HWBP_3_AMASK1 Register

14.3.2.3.2.47.1 THINMAN_REG_DBG_HWBP_3_AMASK1 Register (Offset = 2A4h) [reset = FFFFFFFFh]

Hardware Breakpoint Address Mask Register 1 This register designates the MS 32-bits of the address qualifier mask.

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Table 14-7841. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 02A4h
C7X256V1_DEBUG	0007 3800 02A4h

Figure 14-3894. THINMAN_REG_DBG_HWBP_3_AMASK1 Name Register

31	30	29	28	27	26	25	24
AMASK1							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
AMASK1							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
AMASK1							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
AMASK1							
R/W							
FFFFFFFFh							

Table 14-7842. THINMAN_REG_DBG_HWBP_3_AMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AMASK1	R/W	FFFFFFFFh	Program Address Mask [63:32] This field is used as an address qualification mask for this hardware breakpoint resource An asserted bit means the corresponding address bit is compared

14.3.2.3.2.48 THINMAN_REG_DBG_HWWP_0_CNTL Register

14.3.2.3.2.48.1 THINMAN_REG_DBG_HWWP_0_CNTL Register (Offset = 300h) [reset = 0h]

Hardware Watchpoint Control Register This is the control and status register for hardware watchpoint resource.

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Table 14-7843. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0300h
C7X256V1_DEBUG	0007 3800 0300h

Figure 14-3895. THINMAN_REG_DBG_HWWP_0_CNTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>MANUAL</td><td colspan="7">RESERVED_4</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED_4</td><td>CRIT_ADDR_WR</td><td>CRIT_ADDR_RD</td><td>RESERVED_3</td><td colspan="3">CRIT_ADDR_SIZE</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">CRIT_ADDR_SIZE</td><td>CRIT_PROC</td><td>CRIT_VMID</td><td>CRIT_DCTXT</td><td>CRIT_ADDR</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED_2</td><td>CONDITION</td><td>TRIGGERED</td><td>INTEREST</td><td>RESERVED</td><td>ENABLE</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7844. THINMAN_REG_DBG_HWWP_0_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUAL	R/W	0h	This bitfield provides a manual override to the generation of the hardware watchpoint trigger When set, the hardware watchpoint is continuously triggered
30:22	RESERVED_4	R/W	0h	reserved
21	CRIT_ADDR_WR	R/W	0h	This bitfield configures if data write requests [stores] are monitored to determine a comparison match when the address comparison criteria is enabled
20	CRIT_ADDR_RD	R/W	0h	This bitfield configures if data read requests [loads] are monitored to determine a comparison match when the address comparison criteria is enabled
19	RESERVED_3	R/W	0h	reserved
18:12	CRIT_ADDR_SIZE	R/W	0h	This bitfield configures the size of the access used to determine a comparison match when the address comparison criteria is enabled ------0 : 8 bit accesses are not considered ------1 : 8 bit accesses are considered -----0- : 16-bit accesses are not considered -----1- : 16-bit accesses are considered ----0-- : 32-bit accesses are not considered ----1-- : 32-bit accesses are considered ---0--- : 64-bit accesses are not considered ---1--- : 64-bit accesses are considered --0---- : 128-bit accesses are not considered --1---- : 128-bit accesses are considered -0----- : 256-bit accesses are not considered -1----- : 256-bit accesses are considered 0------ : 512-bit accesses are not considered 1------ : 512-bit accesses are considered

Table 14-7844. THINMAN_REG_DBG_HWWP_0_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CRIT_PROC	R/W	0h	This bit designates if the processor state match criteria is used to determine a comparison match
10	CRIT_VMID	R/W	0h	This bit designates if the VMID match criteria is used to determine a comparison match
9	CRIT_DCTXT	R/W	0h	This bit designates if the debug context match criteria is used to determine a comparison match
8	CRIT_ADDR	R/W	0h	This bit designates if the address comparison criteria is used to determine a comparison match
7:5	RESERVED_2	R/W	0h	reserved
4	CONDITION	R/W	0h	This bit defines the trigger condition that results in the generation of a trigger
3	TRIGGERED	R/W	0h	This bit indicates that the trigger condition has been met since the last time this bit was cleared
2	INTEREST	R/W	0h	This bit configures the module to generate an AET event when triggered
1	RESERVED	R/W	0h	reserved
0	ENABLE	R/W	0h	This is the local enable for the hardware watchpoint module

14.3.2.3.2.49 THINMAN_REG_DBG_HWWP_0_CTXT0 Register

14.3.2.3.2.49.1 THINMAN_REG_DBG_HWWP_0_CTXT0 Register (Offset = 308h) [reset = 0h]

Hardware Watchpoint Context ID Register 0 This register is used to designate the desired context of the HWWP.

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Table 14-7845. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0308h
C7X256V1_DEBUG	0007 3800 0308h

Figure 14-3896. THINMAN_REG_DBG_HWWP_0_CTXT0 Name Register

31	30	29	28	27	26	25	24
DBGCTXT_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGCTXT_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGCTXT_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGCTXT_REF							
R/W							
0h							

Table 14-7846. THINMAN_REG_DBG_HWWP_0_CTXT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGCTXT_REF	R/W	0h	When used, this field is initialized with the DBGCTXT reference value

14.3.2.3.2.50 THINMAN_REG_DBG_HWWP_0_CTXT1 Register

14.3.2.3.2.50.1 THINMAN_REG_DBG_HWWP_0_CTXT1 Register (Offset = 30Ch) [reset = 0h]

Hardware Watchpoint Context ID Register 1 This register is used to designate the desired context of the HWWP.

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Table 14-7847. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 030Ch
C7X256V1_DEBUG	0007 3800 030Ch

Figure 14-3897. THINMAN_REG_DBG_HWWP_0_CTXT1 Name Register

31	30	29	28	27	26	25	24
CONTEXT_IDMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTEXT_IDMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTEXT_IDMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTEXT_IDMASK							
R/W							
0h							

Table 14-7848. THINMAN_REG_DBG_HWWP_0_CTXT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTEXT_IDMASK	R/W	0h	This field is used to define the context qualification mask associated with DBG_HWWP_0_ID0 An asserted bit means the corresponding CONTEXT_ID bit is compared

14.3.2.3.2.51 THINMAN_REG_DBG_HWWP_0_CTXT2 Register

14.3.2.3.2.51.1 THINMAN_REG_DBG_HWWP_0_CTXT2 Register (Offset = 310h) [reset = 0h]

Hardware Watchpoint Context ID Register 2 This register is used to designate the desired context of the HWWP.

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Table 14-7849. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0310h
C7X256V1_DEBUG	0007 3800 0310h

Figure 14-3898. THINMAN_REG_DBG_HWWP_0_CTXT2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">PROC_REF</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VMID_REF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7850. THINMAN_REG_DBG_HWWP_0_CTXT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	PROC_REF	R/W	0h	Processor Mode Reference When enabled, this bit-field controls which processor modes the associated hardware breakpoint is active for -----0 : Inactive during Non-Root User -----1 : Active during Non-Root User ----0- : Inactive during Non-Root Supervisor ----1- : Active during Non-Root Supervisor ---0-- : Inactive during Root User ---1-- : Active during Root User --0--- : Inactive during Root Supervisor --1--- : Active during Root Supervisor -0---- : Inactive during Secure User -1---- : Active during Secure User 0----- : Inactive during Secure Supervisor 1----- : Active during Secure Supervisor
15:8	VMID_REF	R/W	0h	When used, this field is initialized with the VMID reference
7:0	RESERVED	NONE	0h	Reserved

14.3.2.3.2.52 THINMAN_REG_DBG_HWWP_0_ADDR0 Register

14.3.2.3.2.52.1 THINMAN_REG_DBG_HWWP_0_ADDR0 Register (Offset = 318h) [reset = 0h]

Hardware Watchpoint Address Register 0 This register is used to designate bits [31:0] of the address that this hardware watchpoint resource is detecting

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Table 14-7851. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0318h
C7X256V1_DEBUG	0007 3800 0318h

Figure 14-3899. THINMAN_REG_DBG_HWWP_0_ADDR0 Name Register

31	30	29	28	27	26	25	24
ADDR0							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR0							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR0							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR0							
R/W							
0h							

Table 14-7852. THINMAN_REG_DBG_HWWP_0_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR0	R/W	0h	Address Reference [31:0] This field is initialized with the the least significant 32-bits of the address that this hardware watchpoint resource is detecting

14.3.2.3.2.53 THINMAN_REG_DBG_HWWP_0_ADDR1 Register

14.3.2.3.2.53.1 THINMAN_REG_DBG_HWWP_0_ADDR1 Register (Offset = 31Ch) [reset = 0h]

Hardware Watchpoint Address Register 1 This register is used to designate bits [63:32] of the address that this hardware watchpoint resource is detecting.

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Table 14-7853. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 031Ch
C7X256V1_DEBUG	0007 3800 031Ch

Figure 14-3900. THINMAN_REG_DBG_HWWP_0_ADDR1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7854. THINMAN_REG_DBG_HWWP_0_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR1	R/W	0h	Address Reference [63:32] This field is initialized with the the most significant 32-bits of the address that this hardware watchpoint resource is detecting

14.3.2.3.2.54 THINMAN_REG_DBG_HWWP_0_AMASK0 Register

14.3.2.3.2.54.1 THINMAN_REG_DBG_HWWP_0_AMASK0 Register (Offset = 320h) [reset = FFFFFFFFh]

Hardware Breakpoint Watchpoint Mask Register 0 This register designates the LS 32-bits of the address qualifier mask

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Table 14-7855. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0320h
C7X256V1_DEBUG	0007 3800 0320h

Figure 14-3901. THINMAN_REG_DBG_HWWP_0_AMASK0 Name Register

31	30	29	28	27	26	25	24
AMASK0							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
AMASK0							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
AMASK0							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
AMASK0							
R/W							
FFFFFFFFh							

Table 14-7856. THINMAN_REG_DBG_HWWP_0_AMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AMASK0	R/W	FFFFFFFFh	Address Mask [31:2] This field is used as an address qualification mask for this hardware watchpoint resource An asserted bit means the corresponding address bit is compared

14.3.2.3.2.55 THINMAN_REG_DBG_HWWP_0_AMASK1 Register

14.3.2.3.2.55.1 THINMAN_REG_DBG_HWWP_0_AMASK1 Register (Offset = 324h) [reset = FFFFFFFFh]

Hardware Watchpoint Address Mask Register 1 This register designates the MS 32-bits of the address qualifier m

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Table 14-7857. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 0324h
C7X256V1_DEBUG	0007 3800 0324h

Figure 14-3902. THINMAN_REG_DBG_HWWP_0_AMASK1 Name Register

31	30	29	28	27	26	25	24
AMASK1							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
AMASK1							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
AMASK1							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
AMASK1							
R/W							
FFFFFFFFh							

Table 14-7858. THINMAN_REG_DBG_HWWP_0_AMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AMASK1	R/W	FFFFFFFFh	Address Mask [63:32] This field is used as an address qualification mask for this hardware watchpoint resource An asserted bit means the corresponding address bit is compared

14.3.2.3.2.56 COLUMBO_COLUMBO_REG_AET_PID Register

14.3.2.3.2.56.1 COLUMBO_COLUMBO_REG_AET_PID Register (Offset = 0h) [reset = 62000100h]

This register is used to identify this implementation of AET

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Table 14-7859. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 1000h
C7X256V1_DEBUG	0007 3800 1000h

Figure 14-3903. COLUMBO_COLUMBO_REG_AET_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BUSINESS_UNIT</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">200h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">200h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-7860. COLUMBO_COLUMBO_REG_AET_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Defines the scheme Reads return 01b
29:28	BUSINESS_UNIT	R	2h	Business Unit Reads return 10b
27:16	FUNC	R	200h	Functional Group 0x200 is reserved for AET
15:11	RTL	R	0h	RTL Revision This value is implementation defined
10:8	MAJOR	R	1h	Major Revision
7:6	CUSTOM	R/W	0h	Custom Field Reads return 0x0
5:0	MINOR	R	0h	Minor Revision Reads return 0x0

14.3.2.3.2.57 COLUMBO_COLUMBO_REG_AET_OWN Register

14.3.2.3.2.57.1 COLUMBO_COLUMBO_REG_AET_OWN Register (Offset = 4h) [reset = 0h]

Ownership Control and Status Register

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Table 14-7861. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 1004h
C7X256V1_DEBUG	0007 3800 1004h

Figure 14-3904. COLUMBO_COLUMBO_REG_AET_OWN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					OWN		CLAIM
R/W					R		R/W
0h					0h		0h

Table 14-7862. COLUMBO_COLUMBO_REG_AET_OWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R/W	0h	reserved
2:1	OWN	R	0h	The Ownership State
0	CLAIM	R/W	0h	This bit is used to obtain exclusive ownership of the debug module for either the debug initiator or the application initiator Reads will always return 0 If the current state is NOT_OWNED o A debugger-initiated write of 1 will claim the module for use by the debugger initiator o An application-initiated write of 1 will claim the module for use by the application initiator If the current state is DBG_OWNED o A debugger-initiated write of 0 will release ownership o A debugger-initiated write of 1 has no effect o Application writes have no effect If the current state is APP_OWNED o An application-initiated write of 0 will release ownership o A debugger-initiated write of 0 will release ownership o A write of 1 has not effect

14.3.2.3.2.58 COLUMBO_COLUMBO_REG_AET_STAT Register

14.3.2.3.2.58.1 COLUMBO_COLUMBO_REG_AET_STAT Register (Offset = 8h) [reset = 0h]

AET Status Register This register provides access to AET Status

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Table 14-7863. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 1008h
C7X256V1_DEBUG	0007 3800 1008h

Figure 14-3905. COLUMBO_COLUMBO_REG_AET_STAT Name Register

31	30	29	28	27	26	25	24
BEND	TEND	RESERVED_3		UDF			
R	R	R/W		R			
0h	0h	0h		0h			
23	22	21	20	19	18	17	16
TRIG	REND	RESERVED_2					
R	R	R/W					
0h	0h	0h					
15	14	13	12	11	10	9	8
RESERVED_2						SMM	ST
R/W						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
ST			RESERVED				
R			R/W				
0h			0h				

Table 14-7864. COLUMBO_COLUMBO_REG_AET_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BEND	R	0h	A status bit set to a one by a qualified version of trigger that stops the CPU [qualified by FUNC_CNTL:BPE, FUNC_CNTL:BPC, and CPU State] Reset to a zero by Writing a one to IAR_ADD:RBEND A simultaneous set and reset condition causes the bit to be set Read 0: Indicates that a breakpoint trigger has not been generated recently Read 1: Indicates that a breakpoint trigger was recently encountered
30	TEND	R	0h	Trace End Status A status bit set to a one by the trace end trigger Reset to a zero by a Writing a one to IAR_ADD:RTEND A simultaneous set and reset condition causes the bit to be set Read 0: Indicates that a trace end trigger has not been generated recently Read 1: Indicates that a trace end trigger was recently encountered
29:28	RESERVED_3	R/W	0h	reserved

Table 14-7864. COLUMBO_COLUMBO_REG_AET_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:24	UDF	R	0h	Counter Underflow Status The meaning of this field depend on the counter operating mode Generic Operating Mode This flag is set to a one when the counter specified by the index n is directed to count past zero to the maximum counter value Reset to a zero by Writing a one to IAR_ADD:RUDF[n] or by disabling the counter A simultaneous set and reset condition causes this bit to be set Watermark Operating Mode The UDF[n] flag is set to a one when the counter specified by the index n is directed to count past zero to the maximum counter value Reset to a zero by Writing a one to IAR_ADD:RUDF[n] or by disabling the counter A simultaneous set and reset condition causes this bit to be set The UDF[n+1] flag is set to a one when a watermark window is terminated [eg end trigger is acted on] Reset to a zero by a Writing a one to IAR_ADD:RUDF[n+1] or by disabling the counter A simultaneous set and reset condition causes this bit to be set
23	TRIG	R	0h	Trace Trigger A status bit set to one by the trace trigger Reset to a zero by Writing a one to IAR_ADD:RTEND A simultaneous set and reset condition causes this bit to be set
22	REND	R	0h	AET Interrupt Status A status bit set to a one by a qualified version of the CPU_INT trigger [qualified by FUNC_CNTL:RIE, FUNC_CNTL:RIC, and CPU State] Reset to a zero by Writing a one to IAR_ADD:RREND A simultaneous set and reset condition causes this bit to be set
21:10	RESERVED_2	R/W	0h	reserved
9	SMM	R	0h	State Machine Mode This bit shadows the FUNC_CNTL:SMM bit-field
8:5	ST	R	0h	State Machine Current State SMM ST Encoding - 0000 State Machine not enabled 0 0001 State 0 0 0010 State 1 0 0100 State 2 0 1000 State 3 1 --01 State 0 [Machine 0] 1 --10 State 1 [Machine 0] 1 01-- State 0 [Machine 1] 1 10-- State 1 [Machine 1]
4:0	RESERVED	R/W	0h	reserved

14.3.2.3.2.59 COLUMBO_COLUMBO_REG_AET_EVT Register

14.3.2.3.2.59.1 COLUMBO_COLUMBO_REG_AET_EVT Register (Offset = 10h) [reset = 0h]

AET Event Register This register exposes the state of various internal AET events.

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Table 14-7865. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 1010h
C7X256V1_DEBUG	0007 3800 1010h

Figure 14-3906. COLUMBO_COLUMBO_REG_AET_EVT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>CAP_SRC</td><td colspan="4">CSE</td><td colspan="2">RESERVED_2</td><td>CCE</td></tr>
<tr><td>R/W</td><td colspan="4">R</td><td colspan="2">R/W</td><td>R</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">CCE</td><td>RESERVED</td><td colspan="4">CAE</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CBE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CBE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7866. COLUMBO_COLUMBO_REG_AET_EVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAP_SRC	R/W	0h	AET_EVT Capture Source This bitfield defines the behavior of the AET_EVT:CSE, AET_EVT:CCE, AET_EVT:CAE, and AET_PC registers 0: The AET_EVT Read Register will be frozen on BEND [CPU halt trigger event] 1: The AET_EVT Read Register will be frozen on REND [CPU_INT trigger event] Software shall only change CAP_SRC while BEND=0 and REND=0 Changing CAP_SRC at any other time will result in undefined behavior
30:27	CSE	R	0h	Captured State Events The state events recorded are the events that existed when the CAP_SRC programmed trigger event was created This register is loaded continuously when the trigger event is in the inactive state ---0b : State Event S0 is inactive ---1b : State Event S0 is active --0-b : State Event S1 is inactive --1-b : State Event S1 is active -0--b : State Event S2 is inactive -1--b : State Event S2 is active 0---b : State Event S3 is inactive 1---b : State Event S3 is active
26:25	RESERVED_2	R/W	0h	reserved
24:21	CCE	R	0h	Captured Counter Events The counter events recorded are the events that existed when the CAP_SRC programmed trigger event was created This register is loaded continuously when the trigger event is in the inactive state 0-00b : Watermark Instance 0 Counter Event is inactive 0-01b : Watermark Instance 0 Counter Event is active --1-b : Reserved for future use 000-b : Watermark Instance 1 Counter Event is inactive 010-b : Watermark Instance 1 Counter Event is active 1---b : Reserved for future use
20	RESERVED	R/W	0h	reserved

Table 14-7866. COLUMBO_COLUMBO_REG_AET_EVT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	CAE	R	0h	Captured Auxiliary Events The auxiliarly events recorded are the events that existed when the CAP_SRC programmed trigger event was created This register is loaded continuously when the trigger event is in the inactive state CAE[n] = 0 : AUX_EVT[n] is inactive CAE[n] = 1 : AUX _EVT[n] is active
15:0	CBE	R	0h	Captured Bus Events The counter events recorded are the events that existed when the CAP_SRC programmed trigger event was created This register is loaded continuously when the trigger event is in the inactive state CBE[n] = 0 : BUS_EVT[n] is inactive CBE[n] = 1 : BUS_EVT[n] is active

14.3.2.3.2.60 COLUMBO_COLUMBO_REG_AET_PC_0 Register

14.3.2.3.2.60.1 COLUMBO_COLUMBO_REG_AET_PC_0 Register (Offset = 14h) [reset = 0h]

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Table 14-7867. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 1014h
C7X256V1_DEBUG	0007 3800 1014h

Figure 14-3907. COLUMBO_COLUMBO_REG_AET_PC_0 Name Register

31	30	29	28	27	26	25	24
CPC							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CPC							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPC							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPC							CAP_SRC
R							R/W
0h							0h

Table 14-7868. COLUMBO_COLUMBO_REG_AET_PC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	CPC	R	0h	Captured PC[31:01] The PC is recorded when the trigger event specified by AET_PC_0:CAP_SRC occurs The recorded PC is the state of the PC that caused or was present when the conditions were suitable for the trigger event to be set This register is loaded continuously when the trigger event is in the inactive state Software shall only change CAP_SRC while BEND=0 and REND=0 Changing CAP_SRC at any other time will result in undefined behavior
0	CAP_SRC	R/W	0h	AET_PC Capture Source Write 0: The contents of AET_PC will be frozen on BEND [CPU_HALT trigger event] Write 1: The contents of AET_PC will be frozen on REND [CPU_INT trigger event]

14.3.2.3.2.61 COLUMBO_COLUMBO_REG_AET_PC_1 Register

14.3.2.3.2.61.1 COLUMBO_COLUMBO_REG_AET_PC_1 Register (Offset = 18h) [reset = 0h]

AET PC Part 1 Read Register This register exposes bits 63-32 of the PC captured as a result of a trigger event specified in AET_PC_0:CAP_SRC.

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Table 14-7869. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 1018h
C7X256V1_DEBUG	0007 3800 1018h

Figure 14-3908. COLUMBO_COLUMBO_REG_AET_PC_1 Name Register

31	30	29	28	27	26	25	24
CPC							
R							
0h							
23	22	21	20	19	18	17	16
CPC							
R							
0h							
15	14	13	12	11	10	9	8
CPC							
R							
0h							
7	6	5	4	3	2	1	0
CPC							
R							
0h							

Table 14-7870. COLUMBO_COLUMBO_REG_AET_PC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPC	R	0h	Captured PC[63:32] The PC is recorded when the trigger event specified by AET_PC:CAP_SRC occurs The recorded PC is the state of the PC that caused or was present when the conditions were suitable for the trigger event to be set This register is loaded continuously when the trigger event is in the inactive state

14.3.2.3.2.62 COLUMBO_COLUMBO_REG_IAR_ADD Register

14.3.2.3.2.62.1 COLUMBO_COLUMBO_REG_IAR_ADD Register (Offset = 20h) [reset = 0h]

Captured PC[63:32] The PC is recorded when the trigger event specified by AET_PC:CAP_SRC occurs. The recorded PC is the state of the PC that caused or was present when the conditions were suitable for the trigger event to be set. This register is loaded continuously when the trigger event is in the inactive state.

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Table 14-7871. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 1020h
C7X256V1_DEBUG	0007 3800 1020h

Figure 14-3909. COLUMBO_COLUMBO_REG_IAR_ADD Name Register

31	30	29	28	27	26	25	24
RBEND	RTEND	RESERVED_2		RUDF			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
23	22	21	20	19	18	17	16
STRIG	STEND	RREND	RESERVED				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				
15	14	13	12	11	10	9	8
RESERVED						ADRS	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
ADRS							
R/W							
0h							

Table 14-7872. COLUMBO_COLUMBO_REG_IAR_ADD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RBEND	R/W	0h	Reset Breakpoint End Status Software reset for AET_STAT:BEND status This bit has no memory so writes of 1 are self-clearing Reads : always return 0 Write 0 : No action Write 1 : Resets AET_STAT:BEND to a zero
30	RTEND	R/W	0h	Reset Trace End Status Software reset for AET_STAT:TEND and AET_STAT:TRIG status This bit has no memory so writes of 1 are self-clearing Reads : always return 0 Write 0 : No action Write 1 : Resets AET_STAT:TEND and AET_STAT:TRIG to a zero
29:28	RESERVED_2	R/W	0h	reserved
27:24	RUDF	R/W	0h	Reset Counter Underflow Status Software reset for AET_STAT:UDF[n] status This bit has no memory so writes of 1 are self-clearing Reads : always return 0 Write 0 to bit n : No action Write 1 to bit n : Resets AET_STAT:UDF[n] to a zero
23	STRIG	R/W	0h	Set Trace Trigger Software set for TRACE_TRIG trigger This bit has no memory so writes of 1 are self-clearing Reads : always return 0 Write 0 : No action Write 1 : Generates a TRACE_TRIG trigger
22	STEND	R/W	0h	Set Trace End Software set for TRACE_END trigger This bit has no memory so writes of 1 are self-clearing Reads : always return 0 Write 0 : No action Write 1 : Generates a TRACE_END trigger

Table 14-7872. COLUMBO_COLUMBO_REG_IAR_ADD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	RREND	R/W	0h	Reset AET Interrupt Status Software reset for AET_STAT:REND status This bit has no memory so writes of 1 are self-clearing Reads : always return 0 Write 0 : No action Write 1 : Resets AET_STAT:REND to a zero
20:10	RESERVED	R/W	0h	reserved
9:0	ADRS	R/W	0h	This 10-bit value creates the indirect register address

14.3.2.3.2.63 COLUMBO_COLUMBO_REG_IAR_DAT Register

14.3.2.3.2.63.1 COLUMBO_COLUMBO_REG_IAR_DAT Register (Offset = 24h) [reset = 0h]

IAR Data Register This register allows the reading and writing of indirect register values

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Table 14-7873. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 1024h
C7X256V1_DEBUG	0007 3800 1024h

Figure 14-3910. COLUMBO_COLUMBO_REG_IAR_DAT Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-7874. COLUMBO_COLUMBO_REG_IAR_DAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Indirectly Addressable Read Register Data Reads : return the value of the register referenced by IAR_ADD:ADDRS[9:0] Writes : initialize the register referenced by IAR_ADD:ADDRS[9:0] with the value contained here

14.3.2.3.2.64 MATLOCK_REG_TRC_ID Register

14.3.2.3.2.64.1 MATLOCK_REG_TRC_ID Register (Offset = 0h) [reset = 62010800h]

Trace ID Register

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Table 14-7875. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2000h
C7X256V1_DEBUG	0007 3800 2000h

Figure 14-3911. MATLOCK_REG_TRC_ID Name Register

31	30	29	28	27	26	25	24
SCHEME		BUSINESS_UNIT		RESERVED	FUNC		
R		R		R/W	R		
1h		2h		0h	201h		

23	22	21	20	19	18	17	16
FUNC							
R							
201h							

15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
1h					0h		

7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-7876. MATLOCK_REG_TRC_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Defines the scheme Reads return 01b
29:28	BUSINESS_UNIT	R	2h	Business Unit Reads return 10b
27	RESERVED	R/W	0h	reserved
26:16	FUNC	R	201h	Functional Group 0x201 is reserved for C71 Trace Reads return 0x201
15:11	RTL	R	1h	RTL Revision This value is implementation defined
10:8	MAJOR	R	0h	Major Revision This is the first major revision of Trace Reads return 0x0
7:6	CUSTOM	R	0h	Custom Field Reads return 0x0
5:0	MINOR	R	0h	Minor Revision Reads return 0x0

14.3.2.3.2.65 MATLOCK_REG_TRC_OWN Register

14.3.2.3.2.65.1 MATLOCK_REG_TRC_OWN Register (Offset = 4h) [reset = 0h]

Trace Ownership Control Register The Trace Ownership Control Register must be configured before any other trace subsystem resources can be programmed

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Table 14-7877. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2004h
C7X256V1_DEBUG	0007 3800 2004h

Figure 14-3912. MATLOCK_REG_TRC_OWN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED					OWN		CLAIM
R/W					R		R/W
0h					0h		0h

Table 14-7878. MATLOCK_REG_TRC_OWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R/W	0h	reserved
2:1	OWN	R	0h	The Ownership State
0	CLAIM	R/W	0h	This bit is used to obtain exclusive ownership of the debug module for either the debug initiator or the application initiator Reads will always return 0 If the current state is NOT_OWNED o A debugger-initiated write of 1 will claim the module for use by the debugger initiator o An application-initiated write of 1 will claim the module for use by the application initiator If the current state is DBG_OWNED o A debugger-initiated write of 0 will release ownership o A debugger-initiated write of 1 has no effect o Application writes have no effect If the current state is APP_OWNED o An application-initiated write of 0 will release ownership o A debugger-initiated write of 0 will release ownership o A write of 1 has not effect

14.3.2.3.2.66 MATLOCK_REG_TRC_CNTL Register

14.3.2.3.2.66.1 MATLOCK_REG_TRC_CNTL Register (Offset = 8h) [reset = 0h]

Trace Control Register

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Table 14-7879. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2008h
C7X256V1_DEBUG	0007 3800 2008h

Figure 14-3913. MATLOCK_REG_TRC_CNTL Name Register

31	30	29	28	27	26	25	24
TCO		CPTM			TRIG_CHN_ENABLE	DLOST_CLR	PLOST_CLR
R/W		R/W			R/W	R/W	R/W
0h		0h			0h	0h	0h
23	22	21	20	19	18	17	16
TLOST_CLR	CONT_ENABLE				CIDS	CEMU	DBGM_SD
R/W	R/W				R/W	R/W	R/W
0h	0h				0h	0h	0h
15	14	13	12	11	10	9	8
STALL_EN	HPI_MASK	CDAT	AEG_ACTIVE		GLOBAL_TIME_EN		
R/W	R/W	R/W	R/W		R/W		
0h	0h	0h	0h		0h		
7	6	5	4	3	2	1	0
GLOBAL_TIME_EN	STREAM_EN					BRANCH_RBROADCAST	TCOMP_DISABLE
R/W	R/W					R/W	R/W
0h	0h					0h	0h

Table 14-7880. MATLOCK_REG_TRC_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	TCO	R/W	0h	Last Stall Standing Timing Compression Scheme
29:27	CPTM	R/W	0h	Event Profiling Trace Mode These bits identify the mode in which trace is operating When an event profiling mode is configured this is equivalent to an enable to allow the data trace stream to be used for collection of event trace only Event trace is only collected in following cases though: In PEP mode: PC trace stream is enabled and AET PC trigger is currently allowing PC sample capture When one or more of the conditions is not met from being met then any partially buffered event trace messages are exported In AEP mode: Timing and PC trace streams are enabled and AET PC and Timing triggers are currently allowing PC sample capture When one or more of the conditions is not met from being met then any partially buffered event trace messages are exported In EEP mode: Timing trace stream is enabled and AET Timing trigger is currently allowing Timing sample capture When one or more of the conditions is not met from being met then any partially buffered event trace messages are exported In LSS mode: Same as for AEP mode When an event mode is configured, AET triggers pertaining to storing the data value part of memory transactions shall be ignored
26	TRIG_CHN_ENABLE	R/W	0h	Trigger Channel Enable Enable chaining of the two applicaiton control and status registers to support an atomic 64-bit write access
25	DLOST_CLR	R/W	0h	Clear the Data Trace Loss Sticky Status Bit
24	PLOST_CLR	R/W	0h	Clear the PC Trace Loss Sticky Status Bit

Table 14-7880. MATLOCK_REG_TRC_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	TLOST_CLR	R/W	0h	Clear the Timing Trace Loss Sticky Status Bit
22:19	CONT_ENABLE	R/W	0h	Context Enable These bits should be changed when the PC and Data trace streams are both disabled Changing these bits when PC and/or Data Trace stream is enabled shall be ignored
18	CIDS	R/W	0h	Continue during Interrupt During Suspend Allows recordign of activity related ot the servicing of an HPI while the CPU execution has been suspended by any type of debug action This bit should be changed prior to PC, Data, and Timing treams being enabled Changes after this may be ignored by hardware
17	CEMU	R/W	0h	Continue during Debug Activity Allows the recording of stalls due to debug activity while the CPU execution has been suspended by any type of debug action or when CIDS=0 and foreground code execution is active This bit should be changed prior to the timing stream being enabled Changes made while the timing stream is enabled may be ignored by the hardware
16	DBGM_SD	R/W	0h	DBGM Stall Disable
15	STALL_EN	R/W	0h	CPU Stall Enable Controls the action taken when additional data from the CPU will cause buffers to lose data as the trace internal FIFO is full If set, the CPU will be stalled unless the DBGM bit is set or the application is currently in a HPI
14	HPI_MASK	R/W	0h	HPI Mask This bti allows stalling the CPU while processing a high priority interrupt if the FIFO is getting full and STALL_EN bit is set
13	CDAT	R/W	0h	CDAT Allows the recording of activity in the data trace stream either due to debug memory accesses being generated or due to an event trace mode such as EEP mode generating trace activity that is required to be collected in the data trace stream while the CPU execution has been suspended by any type of debug action or when CIDS=0 and foreground code execution is active This bit should be changed prior to the data stream or event trace mode being enabled Changes made whilst data stream is enabled [or an event trace mode is enabled] may be ignored by the hardware
12:11	AEG_ACTIVE	R/W	0h	AEG_ACTIVE This bit reflects the total number of AEG events that are active for trace
10:7	GLOBAL_TIME_EN	R/W	0h	Global Timestamp Enable These enables allow insertion of the global timestamps into trace streams below These bits should be set or cleared before the corresponding stream enables have been set Changing the values after the corresponding stream is enabled shall be ignored
6:2	STREAM_EN	R/W	0h	Trace Stream Enables When an enable bit transitions from 0->1 all FIFO's and scoreboards associated with that stream are reset When an enable bit transitions from 1-> the stream may not be immediately disabled if scoreboards or partial trace packets have to be flushed but the bit4 shall change state immediately
1	BRANCH_RBROADCAST	R/W	0h	Branch Broadcast This bit can be set to enable branch broadcasting mode This bit should be set or cleared before the PC trace stream is enabled Any changes made after the PC trace stream is enabled shall be ignored When branch broadcasting is enabled, PC offset compression is disabled for address parameters of branch and exception command packets and sign extended compression is enabled
0	TCOMP_DISABLE	R/W	0h	Timing Stream Compression Disable This bit can be set to disable the timing stream compression This bit shoudl only be set or cleared when the instruction advance timing stream is disabled Any attempts to change this bit while the timing stream is enabled shall result in writes to this bit being ignored

14.3.2.3.2.67 MATLOCK_REG_TRC_PER_CNT Register

14.3.2.3.2.67.1 MATLOCK_REG_TRC_PER_CNT Register (Offset = Ch) [reset = 400h]

Trace Periodic Counter Register The periodic counter register specifies a count of the total number of bytes transmitted on the ATB interface after which a periodic sync point is generated in the streams that are active. This register is also used to periodically generate alignment synchronization sequences.

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Table 14-7881. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 200Ch
C7X256V1_DEBUG	0007 3800 200Ch

Figure 14-3914. MATLOCK_REG_TRC_PER_CNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTER							
R/W							
400h							
7	6	5	4	3	2	1	0
COUNTER							
R/W							
400h							

Table 14-7882. MATLOCK_REG_TRC_PER_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	reserved
15:0	COUNTER	R/W	400h	Synchronization Frequency A value of 0 disables the counter A reset sets the frequence by default to '1024'

14.3.2.3.2.68 MATLOCK_REG_TRC_STAT Register

14.3.2.3.2.68.1 MATLOCK_REG_TRC_STAT Register (Offset = 10h) [reset = 600007Fh]

Trace Status Register This register is used to establish whether the Matlock Encode Hardware is no longer queuing trace packets in the respective trace streams and also the status of the respective trace queues (whether empty or not). It can also be used to determine if trace capture is currently active or not for any of the trace queues. When a trace stream is being disabled from the enabled state, due to a trigger or ownership loss or disabling the enable bit for the trace stream or clearing the enable bit in export control register, any partially built trace packets must be drained into the respective trace queue. When the partially built trace packets have been drained then the respective done bits shall be set. The respective FIFO empty bits shall only be set when all trace data has been passed from Matlock Encode Hardware to the Matlock Export Block. The statuses available in this register are for debug purposes only and not required in any programming model.

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Table 14-7883. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2010h
C7X256V1_DEBUG	0007 3800 2010h

Figure 14-3915. MATLOCK_REG_TRC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_3	DATA_TRACE_DATA_LOSS	PC_TRACE_DATA_LOSS	TIMING_TRACE_DATA_LOSS	EMULATABLE_CODE_STATUS	PLF_STATUS		EVENT_TRACE_CAPTURE_STATUS
R/W	R	R	R	R	R		R
0h	0h	0h	0h	0h	3h		0h
23	22	21	20	19	18	17	16
EVENT_TRACE_CAPTURE_STATUS	DATA_TRACE_CAPTURE_STATUS					TIMING_TRACE_CAPTURE_STATUS	PC_TRACE_CAPTURE_STATUS
R	R					R	R
0h	0h					0h	0h
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED	RD_DATA_SCOREBOARD_EMPTY	TIMING_STREAM_DONE	DATA_STREAM_DONE	PC_STREAM_DONE	TIMING_FIFO_EMPTY	DATA_FIFO_EMPTY	PC_FIFO_EMPTY
R/W	R	R	R	R	R	R	R
0h	1h	1h	1h	1h	1h	1h	1h

Table 14-7884. MATLOCK_REG_TRC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_3	R/W	0h	reserved
30	DATA_TRACE_DATA_LOSS	R	0h	Set to one by a data trace gap packet being generated Reset by Writing a 1 to TRC_CNTL:DLOST_CLR or when all data trace related streams are disabled [ie memory read, write, streaming buffer and event trace] and then one or more of them are re-enabled indicating a new trace session A loss of ownership also causes this status bit to be reset A simultaneous set and reset causes the bit to be set

Table 14-7884. MATLOCK_REG_TRC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	PC_TRACE_DATA_LOSS	R	0h	Set to one by a PC trace gap packet being generated Reset by Writing a 1 to TRC_CNTL:PLOST_CLR or a zero to one transition on TRC_CNTL:STREAM_EN [PC Trace] or a loss of ownership A simultaneous set and reset causes the bit to be set
28	TIMING_TRACE_DATA_LOSS	R	0h	Set to one by a timing trace gap packet being generated Reset by Writing a 1 to TRC_CNTL:TLOST_CLR or a zero to one transition on TRC_CNTL:STREAM_EN [Timing Trace] or a loss of ownership A simultaneous set and reset causes the bit to be set
27	EMULATABLE_CODE_STATUS	R	0h	The status of whether we are in untraceable secure code or not
26:25	PLF_STATUS	R	3h	The pipeline flattener status
24:23	EVENT_TRACE_CAPTURE_STATUS	R	0h	These bits indicate whether any data is being captured for a particular event trace mode This status accounts for all conditions [ie triggers, CPU states, trace enables and security] required to ascertain whether event trace can be collected or not
22:18	DATA_TRACE_CAPTURE_STATUS	R	0h	This status accounts for triggers, stream enables, enable bit in Trace Export Control Register and PLF conditions and security Bit 22 Streaming Buffer Bit 21 Read Data Bit 20 Read Address Bit 19 Write Data Bit 18 Write Address
17	TIMING_TRACE_CAPTURE_STATUS	R	0h	This status accounts for triggers, stream enables, enable bit in the trace export control register and PLF conditions and security
16	PC_TRACE_CAPTURE_STATUS	R	0h	This status accounts for triggers, stream enables, enable bit in the trace export control register and PLF conditions and security
15:7	RESERVED	R/W	0h	reserved
6	RD_DATA_SCOREBOARD_EMPTY	R	1h	RD_DATA_SCOREBOARD_EMPTY status
5	TIMING_STREAM_DONE	R	1h	TIMING_STREAM_DONE status
4	DATA_STREAM_DONE	R	1h	DATA_STREAM_DONE status
3	PC_STREAM_DONE	R	1h	PC_STREAM_DONE status
2	TIMING_FIFO_EMPTY	R	1h	TIMING_FIFO_EMPTY status
1	DATA_FIFO_EMPTY	R	1h	DATA_FIFO_EMPTY status
0	PC_FIFO_EMPTY	R	1h	PC_FIFO_EMPTY status

14.3.2.3.2.69 MATLOCK_REG_TRC_TRIG0_CNTL_STAT Register

14.3.2.3.2.69.1 MATLOCK_REG_TRC_TRIG0_CNTL_STAT Register (Offset = 14h) [reset = 0h]

Trace Trigger Control and Status Register The trace trigger control and status registers may be used to enable or disable trace data capture in the PC, Timing or Data Trace Streams without touching the AET module. The trigger registers may also be used in conjunction with AET to provide additional resources for trigger generation. When trigger register chaining mode is enabled in the trace ctrl register, software must follow this sequence: Write to TRC_TRIG0_CNTL_STAT register which does not immediately take effect Write to TRC_TRIG1_CNTL_STAT register which results in a 64-bit write taking effect to include the last update to TRC_TRIG1_CNTL_STAT register. The status bits in both of the trigger control and status registers when indicating that a trace capture window is not active do not account for effects such as: Flushing partial branch bits packets PRELIMINARY documents contain information on a product under development and are issued for evaluation purposes only. Features, characteristic data and other information are subject to change. TI Confidential NDA Restrictions UNDER NON DISCLOSURE AGREEMENT. DO NOT COPY. Page 171 of 188 Flushing read data scoreboard Flushing partial timing packets Flushing partial event trace packets Generating Sync Points that are required due to one or more trace streams being disabled The status bit only indicates that a trace capture window is being disabled. The status bits account for all parameters required to decide if a capture window is open or not: AET triggers Application triggers Security PLF conditions (i.e. foreground or background code execution or halted status) Trace Stream Enables Trace Enable bit in the Trace Export Control Register

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Table 14-7885. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2014h
C7X256V1_DEBUG	0007 3800 2014h

Figure 14-3916. MATLOCK_REG_TRC_TRIG0_CNTL_STAT Name Register

31	30	29	28	27	26	25	24
TRACE_NO_STORE_TIMING_LE	TRACE_NO_STORE_TIMING	TRACE_NO_STORE_PC_LE	TRACE_NO_STORE_PC	TRACE_STORE_SBPT_LE	TRACE_STORE_SBPT	TRACE_STORE_WD_LE	TRACE_STORE_WD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRACE_STORE_WA_LE	TRACE_STORE_WA	TRACE_STORE_TIMING_LE	TRACE_STORE_TIMING	TRACE_STORE_RD_LE	TRACE_STORE_RD	TRACE_STORE_RA_LE	TRACE_STORE_RA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRACE_STORE_PCTAG_LE	TRACE_STORE_PCTAG	TRACE_STORE_PC_LE	TRACE_STORE_PC	TRACE_STOP_SBPT	TRACE_STOP_TIMING	TRACE_STOP_PC	TRACE_STOP_DATA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRACE_START_SBPT	TRACE_START_WD	TRACE_START_WA	TRACE_START_TIMING	TRACE_START_RD	TRACE_START_RA	TRACE_START_PCTAG	TRACE_START_PC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-7886. MATLOCK_REG_TRC_TRIG0_CNTL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRACE_NO_STORE_TIMING_LE	R/W	0h	Load Enable for TRACE_NO_STORE_TIMING Write 1: Allows TRACE_NO_STORE_TIMING field to be updated with the value presented to that field Write 0: No effect
30	TRACE_NO_STORE_TIMING	R/W	0h	Write 0/1: This bit updates level of TRACE_NO_STORE_Timing trigger when the next higher bit is set Read 0: Timing trace capture window is active for Timing trace stream Read 1: Timing trace capture is not active or is being disabled for the Timing trace stream
29	TRACE_NO_STORE_PC_LE	R/W	0h	Load Enable for TRACE_NO_STORE_PC Write 1: Allows TRACE_NO_STORE_PC field to be updated with the value presented to that field Write 0: No effect
28	TRACE_NO_STORE_PC	R/W	0h	Write 0/1: This bit updates level of TRACE_NO_STORE_PC trigger when the next higher bit is set Read 0: PC trace capture window is active for PC trace stream Read 1: PC trace capture is not active or is being disabled for the PC trace stream
27	TRACE_STORE_SBPT_LE	R/W	0h	Load Enable for TRACE_STORE_SBPT Write 1: Allows TRACE_STORE_SBPT field to be updated with the value presented to that field Write 0: No effect
26	TRACE_STORE_SBPT	R/W	0h	Write 0/1: This bit updates level of TRACE_STORE_SBPT trigger when the next higher bit is set Read 0: SBPT capture window is not active or is being disabled for data trace stream Read 1: SBPT capture window is active for the data trace stream
25	TRACE_STORE_WD_LE	R/W	0h	Load Enable for TRACE_STORE_WD Write 1: Allows TRACE_STORE_WD field to be updated with the value presented to that field Write 0: No effect
24	TRACE_STORE_WD	R/W	0h	Write 0/1: This bit updates level of TRACE_STORE_WD trigger when the next higher bit is set Read 0: WD capture window is not active or is being disabled for data trace stream Read 1: WD capture window is active for the data trace stream
23	TRACE_STORE_WA_LE	R/W	0h	Load Enable for TRACE_STORE_WA Write 1: Allows TRACE_STORE_WA field to be updated with the value presented to that field Write 0: No effect
22	TRACE_STORE_WA	R/W	0h	Write 0/1: This bit updates level of TRACE_STORE_WA trigger when the next higher bit is set Read 0: WA capture window is not active or is being disabled for data trace stream Read 1: WA capture window is active for the data trace stream
21	TRACE_STORE_TIMING_LE	R/W	0h	Load Enable for TRACE_STORE_TIMING Write 1: Allows TRACE_STORE_TIMING field to be updated with the value presented to that field Write 0: No effect
20	TRACE_STORE_TIMING	R/W	0h	Write 0/1: This bit updates level of TRACE_STORE_TIMING trigger when the next higher bit is set Read 0: Timing capture window is not active or is being disabled for data trace stream Read 1: Timing capture window is active for the data trace stream
19	TRACE_STORE_RD_LE	R/W	0h	Load Enable for TRACE_STORE_RD Write 1: Allows TRACE_STORE_RD field to be updated with the value presented to that field Write 0: No effect
18	TRACE_STORE_RD	R/W	0h	Write 0/1: This bit updates level of TRACE_STORE_RD trigger when the next higher bit is set Read 0: RD capture window is not active or is being disabled for data trace stream Read 1: RD capture window is active for the data trace stream
17	TRACE_STORE_RA_LE	R/W	0h	Load Enable for TRACE_STORE_RA Write 1: Allows TRACE_STORE_RA field to be updated with the value presented to that field Write 0: No effect
16	TRACE_STORE_RA	R/W	0h	Write 0/1: This bit updates level of TRACE_STORE_RA trigger when the next higher bit is set Read 0: RA capture window is not active or is being disabled for data trace stream Read 1: RA capture window is active for the data trace stream
15	TRACE_STORE_PCTAG_LE	R/W	0h	Load Enable for TRACE_STORE_PCTAG Write 1: Allows TRACE_STORE_PCTAG field to be updated with the value presented to that field Write 0: No effect

Table 14-7886. MATLOCK_REG_TRC_TRIG0_CNTL_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	TRACE_STORE_PCTAG	R/W	0h	Write 0/1: This bit updates level of TRACE_STORE_PCTAG trigger when the next higher bit is set Read 0: PCTAG attributes are not being collected or are being disabled for data trace stream Read 1: PCTAG attributes are being collected for the data trace stream
13	TRACE_STORE_PC_LE	R/W	0h	Load Enable for TRACE_STORE_PC Write 1: Allows TRACE_STORE_PC field to be updated with the value presented to that field Write 0: No effect
12	TRACE_STORE_PC	R/W	0h	Write 0/1: This bit updates level of TRACE_STORE_PC trigger when the next higher bit is set Read 0: PC capture window is not active or is being disabled Read 1: PC capture window is active
11	TRACE_STOP_SBPT	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_STOP_SBPT trigger Write 0: No effect Read 0: SBPT capture window is not active or is being disabled Read 1: SBPT capture window is active
10	TRACE_STOP_TIMING	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_STOP_TIMING trigger Write 0: No effect Read 0: Timing trace stream capture window is not active or is being disabled Read 1: Timing trace stream capture window is active
9	TRACE_STOP_PC	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_STOP_PC trigger Write 0: No effect Read 0: PC trace stream capture window is not active or is being disabled Read 1: PC trace stream capture window is active
8	TRACE_STOP_DATA	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_STOP_DATA trigger Write 0: No effect Read 0: Data trace stream window is not active for either of PCTAG, WA, WD, RA, RD or is being disabled Read 1: Data trace stream window is active for any of PCTAG, WA, WD, RA, RD
7	TRACE_START_SBPT	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_START_SBPT trigger Write 0: No effect Read 0: Data trace stream SBPT window is not active or is being disabled Read 1: Data trace stream SBPT window is active
6	TRACE_START_WD	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_START_WD trigger Write 0: No effect Read 0: Data trace stream WD window is not active or is being disabled Read 1: Data trace stream WD window is active
5	TRACE_START_WA	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_START_WA trigger Write 0: No effect Read 0: Data trace stream WA window is not active or is being disabled Read 1: Data trace stream WA window is active
4	TRACE_START_TIMING	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_START_TIMING trigger Write 0: No effect Read 0: Timing trace window is not active or is being disabled Read 1: Timing trace window is active
3	TRACE_START_RD	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_START_RD trigger Write 0: No effect Read 0: Data Stream RD trace window is not active or is being disabled Read 1: Data Stream RD trace window is active
2	TRACE_START_RA	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_START_RA trigger Write 0: No effect Read 0: Data Stream RA trace window is not active or is being disabled Read 1: Data Strea
1	TRACE_START_PCTAG	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_START_PCTAG trigger Write 0: No effect Read 0: PCTAG attribute collection is not active or is being disabled Read 1: PCTAG attribute collection is active
0	TRACE_START_PC	R/W	0h	Write 1: This bit when set shall generate a pulse on the TRACE_START_PC trigger Write 0: No effect Read 0: PC trace window is not active or is being disabled Read 1: PC trace window is active

14.3.2.3.2.70 MATLOCK_REG_TRC_TRIG1_CNTL_STAT Register

14.3.2.3.2.70.1 MATLOCK_REG_TRC_TRIG1_CNTL_STAT Register (Offset = 18h) [reset = 0h]

Trace Trigger Control and Status Register The trace trigger control and status registers may be used to enable or disable trace data capture in the PC, Timing or Data Trace Streams without touching the AET module. The trigger registers may also be used in conjunction with AET to provide additional resources for trigger generation. When trigger register chaining mode is enabled in the trace ctrl register, software must follow this sequence: Write to TRC_TRIG0_CNTL_STAT register which does not immediately take effect Write to TRC_TRIG1_CNTL_STAT register which results in a 64-bit write taking effect to include the last update to TRC_TRIG1_CNTL_STAT register. The status bits in both of the trigger control and status registers when indicating that a trace capture window is not active do not account for effects such as: Flushing partial branch bits packets PRELIMINARY documents contain information on a product under development and are issued for evaluation purposes only. Features, characteristic data and other information are subject to change. TI Confidential NDA Restrictions UNDER NON DISCLOSURE AGREEMENT. DO NOT COPY. Page 171 of 188 Flushing read data scoreboard Flushing partial timing packets Flushing partial event trace packets Generating Sync Points that are required due to one or more trace streams being disabled The status bit only indicates that a trace capture window is being disabled. The status bits account for all parameters required to decide if a capture window is open or not: AET triggers Application triggers Security PLF conditions (i.e. foreground or background code execution or halted status) Trace Stream Enables Trace Enable bit in the Trace Export Control Register

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Table 14-7887. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2018h
C7X256V1_DEBUG	0007 3800 2018h

Figure 14-3917. MATLOCK_REG_TRC_TRIG1_CNTL_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>TRACE_TRIG</td><td>TRACE_END</td><td>TRACE_NO_STORE_SBPT_LE</td><td>TRACE_NO_STORE_SBPT</td><td>TRACE_NO_STORE_DATA_LE</td><td>TRACE_NO_STORE_DATA</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-7888. MATLOCK_REG_TRC_TRIG1_CNTL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R/W	0h	reserved
5	TRACE_TRIG	R/W	0h	Write 1: This bit shall generate a pulse on Trace Trigger Write 0 : No effect

Table 14-7888. MATLOCK_REG_TRC_TRIG1_CNTL_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TRACE_END	R/W	0h	Write 1: This bit shall generate a pulse on Trace End Trigger Write 0 : No effect
3	TRACE_NO_STORE_SBPT_LE	R/W	0h	Load Enable for TRACE_NO_STORE_SBPT Write 1: Allows TRACE_NO_STORE_SBPT field to be updated with the value presented to that field Write 0: No effect
2	TRACE_NO_STORE_SBPT	R/W	0h	Write 0/1: This bit updates level of TRACE_NO_STORE_SBPT trigger when the next higher bit is set Read 0: SPBT trace capture window is active for data trace stream Read 1: SPBT trace capture is not active for the data trace stream or is being disabled
1	TRACE_NO_STORE_DATA_LE	R/W	0h	Load Enable for TRACE_NO_STORE_DATA Write 1: Allows TRACE_NO_STORE_DATA field to be updated with the value presented to that field Write 0: No effect
0	TRACE_NO_STORE_DATA	R/W	0h	Write 0/1: This bit updates level of TRACE_NO_STORE_DATA trigger when the next higher bit is set Read 0: Data trace capture window is active for either of RA,WA,RD,WD Read 1: Data trace capture window is not active for any of RA,WA,RD,WD or is being disabled

14.3.2.3.2.71 MATLOCK_REG_TRC_TIMESTAMP_CNT_REG0 Register

14.3.2.3.2.71.1 MATLOCK_REG_TRC_TIMESTAMP_CNT_REG0 Register (Offset = 1Ch) [reset = 0h]

This register returns the least significant 32-bits of the 48-bit external global timestamp counter. When this register is read the upper 16-bits of the global timestamp are loaded into a shadow register which may be read when the Trace TimeStamp Counter Register 1 is read. The shadow register is only ever updated when the Trace Time Stamp Counter Register 0 is read.

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Table 14-7889. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 201Ch
C7X256V1_DEBUG	0007 3800 201Ch

Figure 14-3918. MATLOCK_REG_TRC_TIMESTAMP_CNT_REG0 Name Register

31	30	29	28	27	26	25	24
GLOBAL_TIMESTAMP							
R/W							
0h							
23	22	21	20	19	18	17	16
GLOBAL_TIMESTAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
GLOBAL_TIMESTAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
GLOBAL_TIMESTAMP							
R/W							
0h							

Table 14-7890. MATLOCK_REG_TRC_TIMESTAMP_CNT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GLOBAL_TIMESTAMP	R/W	0h	Least Significant 32-bits of the external global timestamp

14.3.2.3.2.72 MATLOCK_REG_TRC_TIMESTAMP_CNT_REG1 Register

14.3.2.3.2.72.1 MATLOCK_REG_TRC_TIMESTAMP_CNT_REG1 Register (Offset = 20h) [reset = 0h]

This register returns the most significant 16-bits of the external global timestamp counter loaded from a shadow register. The shadow register is updated every time the Trace Time Stamp Counter Register 0 is read. The value read from this register may be stale (or undefined) if software does not first read the Trace Time Stamp Counter Register 0.

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Table 14-7891. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2020h
C7X256V1_DEBUG	0007 3800 2020h

Figure 14-3919. MATLOCK_REG_TRC_TIMESTAMP_CNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
GLOBAL_TIMESTAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
GLOBAL_TIMESTAMP							
R/W							
0h							

Table 14-7892. MATLOCK_REG_TRC_TIMESTAMP_CNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	reserved
15:0	GLOBAL_TIMESTAMP	R/W	0h	Bits 47:32 of the external global timestamp read from a shadow register which captures the most significant 16-bits of the global timestamp when the bottom 32-bits are read

14.3.2.3.2.73 MATLOCK_REG_TRC_EXPT_CNTL Register

14.3.2.3.2.73.1 MATLOCK_REG_TRC_EXPT_CNTL Register (Offset = 24h) [reset = 0h]

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Table 14-7893. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2024h
C7X256V1_DEBUG	0007 3800 2024h

Figure 14-3920. MATLOCK_REG_TRC_EXPT_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESET	FLUSH	TRIGGER_EN	ENABLE
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-7894. MATLOCK_REG_TRC_EXPT_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R/W	0h	reserved
3	RESET	R/W	0h	Writing a 1 to this bit will initiate a reset of read and write synchronous FIFO pointers and will disable the export module by clearing all writable bits in this register and updating the Trace Export Status register bits to their reset state The bit will reset automatically to a 0 after the reset has been completed and will read as 1 whilst the reset is ongoing
2	FLUSH	R/W	0h	Writing a 1 to this bit will initiate an internal trace flush This bit reads as 1 until the initiated flush is completed
1	TRIGGER_EN	R/W	0h	Writing a 1 to this bit shall enable embedded triggers to be inserted into the ATB data stream
0	ENABLE	R/W	0h	When written with a 1, this is a request to enable trace export and acquisition from the PLF interface When written with a 0, this is a request to disable trace export This also requests disablement of collection of new trace data from the PLF interface since it cannot be exported This is equivalent of clearing AET triggers and not allowing collection of trace data When read as a 1, this means trace export has been requested to be enabled or is enabled When read as a 0, this means trace export has been requested to be disabled or is disabled Trace Export may be confirmed as disabled by waiting for the HALTED bit to go from 0->1 The Trace FIFO is confirmed as empty when the DRAIN_DONE bit is set

14.3.2.3.2.74 MATLOCK_REG_TRC_EXPT_STAT Register

14.3.2.3.2.74.1 MATLOCK_REG_TRC_EXPT_STAT Register (Offset = 28h) [reset = 80000207h]

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Table 14-7895. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 2028h
C7X256V1_DEBUG	0007 3800 2028h

Figure 14-3921. MATLOCK_REG_TRC_EXPT_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>EXPORT_FIFO_EMPTY_STATUS</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FIFO_DEPTH</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">FIFO_DEPTH</td><td colspan="4">MAX_FIFO_DEPTH</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">20h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">MAX_FIFO_DEPTH</td><td>FLUSH_STAT</td><td>ATREADY</td><td>HALTED</td><td>DRAIN_DONE</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">20h</td><td>0h</td><td>1h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-7896. MATLOCK_REG_TRC_EXPT_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EXPORT_FIFO_EMPTY_STATUS	R	1h	Read 0: Export FIFO is not empty Read 1: Export FIFO is empty This is a status for the Export FIFO When this bit is set it does not indicate the state of other storage elements inside Matlocks acquisition logic This status is to be used for debug purposes only The drain_done bit is the initiator status for all storage elements inside Matlock
30:20	RESERVED	R/W	0h	reserved
19:12	FIFO_DEPTH	R	0h	Set to the FIFO depth of the synchronous FIFO in export module in terms of entries as implemented in this module by the designer
11:4	MAX_FIFO_DEPTH	R	20h	This is a field when read indicates the current max depth of export FIFO utilization in terms of FIFO entries 0 indicates FIFO empty The field is updated when trace export is enabled and may be read at any time Reading of the field may indicate FIFO full conditions by comparing the value to the known FIFO depth set at compile time
3	FLUSH_STAT	R	0h	reserved
2	ATREADY	R	1h	reserved
1	HALTED	R	1h	reserved
0	DRAIN_DONE	R	1h	reserved

14.3.2.3.2.75 MATLOCK_REG_TRC_EXPT_ATID Register

14.3.2.3.2.75.1 MATLOCK_REG_TRC_EXPT_ATID Register (Offset = 2Ch) [reset = 0h]

Trace Export Trace ID Register

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Table 14-7897. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 202Ch
C7X256V1_DEBUG	0007 3800 202Ch

Figure 14-3922. MATLOCK_REG_TRC_EXPT_ATID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED				ATID			
R/W				R/W			
0h				0h			

Table 14-7898. MATLOCK_REG_TRC_EXPT_ATID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R/W	0h	reserved
3:0	ATID	R/W	0h	The ATID to output with valid trace data on the ATB interface

14.3.2.3.2.76 CSCTI_CTICONTROL Register

14.3.2.3.2.76.1 CSCTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

The CTI Control Register enables the CTI. >

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Table 14-7899. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3000h
C7X256V0_DEBUG	0007 3400 A000h
C7X256V0_DEBUG	0007 3400 B000h
C7X256V1_DEBUG	0007 3800 3000h
C7X256V1_DEBUG	0007 3800 A000h
C7X256V1_DEBUG	0007 3800 B000h

Figure 14-3923. CSCTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
NONE							R/W
0h							0h

Table 14-7900. CSCTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GLBEN	R/W	0h	Enables or disables the ECT.

14.3.2.3.2.77 CSCTI_CTIINTACK Register

14.3.2.3.2.77.1 CSCTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the ctitrigout output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the ctitrigout is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.

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Table 14-7901. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3010h
C7X256V0_DEBUG	0007 3400 A010h
C7X256V0_DEBUG	0007 3400 B010h
C7X256V1_DEBUG	0007 3800 3010h
C7X256V1_DEBUG	0007 3800 A010h
C7X256V1_DEBUG	0007 3800 B010h

Figure 14-3924. CSCTI_CTIINTACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTACK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7902. CSCTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INTACK	R/W	0h	Acknowledges the corresponding ctitrigout output. There is one bit of the register for each ctitrigout output. When a 1 is written to a bit in this register, the corresponding ctitrigout is acknowledged and is cleared when MAPTRIGOUT is LOW. Writing a 0 to any of the bits in this register has no effect.

14.3.2.3.2.78 CSCTI_CTIAPPSET Register

14.3.2.3.2.78.1 CSCTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.

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Table 14-7903. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3014h
C7X256V0_DEBUG	0007 3400 A014h
C7X256V0_DEBUG	0007 3400 B014h
C7X256V1_DEBUG	0007 3800 3014h
C7X256V1_DEBUG	0007 3800 A014h
C7X256V1_DEBUG	0007 3800 B014h

Figure 14-3925. CSCTI_CTIAPPSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7904. CSCTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPSET	R/W	0h	Setting a bit HIGH generates a channel event for the selected channel. There is one bit of the register for each channel. Read : 0 = application trigger inactive (reset). 1 = application trigger active. Write : 0 = no effect. 1 = generate channel event.

14.3.2.3.2.79 CSCTI_CTIAPPCLR Register

14.3.2.3.2.79.1 CSCTI_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

The CTI Interrupt Acknowledge Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.

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Table 14-7905. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3018h
C7X256V0_DEBUG	0007 3400 A018h
C7X256V0_DEBUG	0007 3400 B018h
C7X256V1_DEBUG	0007 3800 3018h
C7X256V1_DEBUG	0007 3800 A018h
C7X256V1_DEBUG	0007 3800 B018h

Figure 14-3926. CSCTI_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLEAR			
NONE				R/W			
0h				0h			

Table 14-7906. CSCTI_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPCLEAR	R/W	0h	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. When a 1 is written to a bit in this register, the corresponding application trigger is disabled in the CTIAPPSET register. Writing a 0 to any of the bits in this register has no effect.

14.3.2.3.2.80 CSCTI_CTIAPPPULSE Register

14.3.2.3.2.80.1 CSCTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one cticlk period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

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Table 14-7907. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 301Ch
C7X256V0_DEBUG	0007 3400 A01Ch
C7X256V0_DEBUG	0007 3400 B01Ch
C7X256V1_DEBUG	0007 3800 301Ch
C7X256V1_DEBUG	0007 3800 A01Ch
C7X256V1_DEBUG	0007 3800 B01Ch

Figure 14-3927. CSCTI_CTIAPPPULSE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPULSE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7908. CSCTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	APPULSE	R/W	0h	Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. When a 1 is written to a bit in this register, a corresponding channel event pulse is generated for one cticlk period. Writing a 0 to any of the bits in this register has no effect.

14.3.2.3.2.81 CSCTI_CTIINEN0 Register

14.3.2.3.2.81.1 CSCTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

The CTI Trigger 0 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-7909. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3020h
C7X256V0_DEBUG	0007 3400 A020h
C7X256V0_DEBUG	0007 3400 B020h
C7X256V1_DEBUG	0007 3800 3020h
C7X256V1_DEBUG	0007 3800 A020h
C7X256V1_DEBUG	0007 3800 B020h

Figure 14-3928. CSCTI_CTIINEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7910. CSCTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.3.2.3.2.82 CSCTI_CTIINEN1 Register

14.3.2.3.2.82.1 CSCTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

The CTI Trigger 1 to Channel Enable Register enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-7911. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3024h
C7X256V0_DEBUG	0007 3400 A024h
C7X256V0_DEBUG	0007 3400 B024h
C7X256V1_DEBUG	0007 3800 3024h
C7X256V1_DEBUG	0007 3800 A024h
C7X256V1_DEBUG	0007 3800 B024h

Figure 14-3929. CSCTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-7912. CSCTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.3.2.3.2.83 CSCTI_CTIINEN2 Register

14.3.2.3.2.83.1 CSCTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-7913. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3028h
C7X256V0_DEBUG	0007 3400 A028h
C7X256V0_DEBUG	0007 3400 B028h
C7X256V1_DEBUG	0007 3800 3028h
C7X256V1_DEBUG	0007 3800 A028h
C7X256V1_DEBUG	0007 3800 B028h

Figure 14-3930. CSCTI_CTIINEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7914. CSCTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.3.2.3.2.84 CSCTI_CTIINEN3 Register

14.3.2.3.2.84.1 CSCTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-7915. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 302Ch
C7X256V0_DEBUG	0007 3400 A02Ch
C7X256V0_DEBUG	0007 3400 B02Ch
C7X256V1_DEBUG	0007 3800 302Ch
C7X256V1_DEBUG	0007 3800 A02Ch
C7X256V1_DEBUG	0007 3800 B02Ch

Figure 14-3931. CSCTI_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-7916. CSCTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.3.2.3.2.85 CSCTI_CTIINEN4 Register

14.3.2.3.2.85.1 CSCTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-7917. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3030h
C7X256V0_DEBUG	0007 3400 A030h
C7X256V0_DEBUG	0007 3400 B030h
C7X256V1_DEBUG	0007 3800 3030h
C7X256V1_DEBUG	0007 3800 A030h
C7X256V1_DEBUG	0007 3800 B030h

Figure 14-3932. CSCTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-7918. CSCTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.3.2.3.2.86 CSCTI_CTIINEN5 Register

14.3.2.3.2.86.1 CSCTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-7919. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3034h
C7X256V0_DEBUG	0007 3400 A034h
C7X256V0_DEBUG	0007 3400 B034h
C7X256V1_DEBUG	0007 3800 3034h
C7X256V1_DEBUG	0007 3800 A034h
C7X256V1_DEBUG	0007 3800 B034h

Figure 14-3933. CSCTI_CTIINEN5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7920. CSCTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.3.2.3.2.87 CSCTI_CTIINEN6 Register

14.3.2.3.2.87.1 CSCTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-7921. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3038h
C7X256V0_DEBUG	0007 3400 A038h
C7X256V0_DEBUG	0007 3400 B038h
C7X256V1_DEBUG	0007 3800 3038h
C7X256V1_DEBUG	0007 3800 A038h
C7X256V1_DEBUG	0007 3800 B038h

Figure 14-3934. CSCTI_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
NONE				R/W			
0h				0h			

Table 14-7922. CSCTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.3.2.3.2.88 CSCTI_CTIINEN7 Register

14.3.2.3.2.88.1 CSCTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

The CTI Trigger to Channel Enable Register 0 enables the signalling of an event on CTM channels when the core issues a trigger, ctitrigin, to the CTI. Within this register there is one bit for each of the four channels implemented. This register does not affect the application trigger operations.

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Table 14-7923. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 303Ch
C7X256V0_DEBUG	0007 3400 A03Ch
C7X256V0_DEBUG	0007 3400 B03Ch
C7X256V1_DEBUG	0007 3800 303Ch
C7X256V1_DEBUG	0007 3800 A03Ch
C7X256V1_DEBUG	0007 3800 B03Ch

Figure 14-3935. CSCTI_CTIINEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7924. CSCTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGINEN	R/W	0h	Enables a cross trigger event to the corresponding channel when an ctitrigin is activated. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, it enables the ctitrigin signal to generate an event on the respective channel of the CTM. For example, TRIGINEN[0] set to 1 enables ctitrigin onto channel 0. Writing a 0 to any of the bits in this register disables the ctitrigin signal from generating an event on the respective channel of the CTM. Reading this register returns the programmed value.

14.3.2.3.2.89 CSCTI_CTIOUTEN0 Register

14.3.2.3.2.89.1 CSCTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

The CTI Channel to Trigger 0 Enable Registers define which channels can generate a ctitrigout[0] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-7925. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 30A0h
C7X256V0_DEBUG	0007 3400 A0A0h
C7X256V0_DEBUG	0007 3400 B0A0h
C7X256V1_DEBUG	0007 3800 30A0h
C7X256V1_DEBUG	0007 3800 A0A0h
C7X256V1_DEBUG	0007 3800 B0A0h

Figure 14-3936. CSCTI_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-7926. CSCTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[0] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.3.2.3.2.90 CSCTI_CTIOUTEN1 Register

14.3.2.3.2.90.1 CSCTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

The CTI Channel to Trigger 1 Enable Registers define which channels can generate a ctitrigout[1] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-7927. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 30A4h
C7X256V0_DEBUG	0007 3400 A0A4h
C7X256V0_DEBUG	0007 3400 B0A4h
C7X256V1_DEBUG	0007 3800 30A4h
C7X256V1_DEBUG	0007 3800 A0A4h
C7X256V1_DEBUG	0007 3800 B0A4h

Figure 14-3937. CSCTI_CTIOUTEN1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7928. CSCTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[1] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[1] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.3.2.3.2.91 CSCTI_CTIOUTEN2 Register

14.3.2.3.2.91.1 CSCTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

The CTI Channel to Trigger 2 Enable Registers define which channels can generate a ctitrigout[2] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-7929. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 30A8h
C7X256V0_DEBUG	0007 3400 A0A8h
C7X256V0_DEBUG	0007 3400 B0A8h
C7X256V1_DEBUG	0007 3800 30A8h
C7X256V1_DEBUG	0007 3800 A0A8h
C7X256V1_DEBUG	0007 3800 B0A8h

Figure 14-3938. CSCTI_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-7930. CSCTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[2] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[2] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.3.2.3.2.92 CSCTI_CTIOUTEN3 Register

14.3.2.3.2.92.1 CSCTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

The CTI Channel to Trigger 3 Enable Registers define which channels can generate a ctitrigout[3] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-7931. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 30ACh
C7X256V0_DEBUG	0007 3400 A0ACh
C7X256V0_DEBUG	0007 3400 B0ACh
C7X256V1_DEBUG	0007 3800 30ACh
C7X256V1_DEBUG	0007 3800 A0ACh
C7X256V1_DEBUG	0007 3800 B0ACh

Figure 14-3939. CSCTI_CTIOUTEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7932. CSCTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[3] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[3] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.3.2.3.2.93 CSCTI_CTIOUTEN4 Register

14.3.2.3.2.93.1 CSCTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

The CTI Channel to Trigger 4 Enable Registers define which channels can generate a ctitrigout[4] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-7933. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 30B0h
C7X256V0_DEBUG	0007 3400 A0B0h
C7X256V0_DEBUG	0007 3400 B0B0h
C7X256V1_DEBUG	0007 3800 30B0h
C7X256V1_DEBUG	0007 3800 A0B0h
C7X256V1_DEBUG	0007 3800 B0B0h

Figure 14-3940. CSCTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-7934. CSCTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[4] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[4] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.3.2.3.2.94 CSCTI_CTIOUTEN5 Register

14.3.2.3.2.94.1 CSCTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

The CTI Channel to Trigger 5 Enable Registers define which channels can generate a ctitrigout[5] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-7935. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 30B4h
C7X256V0_DEBUG	0007 3400 A0B4h
C7X256V0_DEBUG	0007 3400 B0B4h
C7X256V1_DEBUG	0007 3800 30B4h
C7X256V1_DEBUG	0007 3800 A0B4h
C7X256V1_DEBUG	0007 3800 B0B4h

Figure 14-3941. CSCTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-7936. CSCTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[5] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[5] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.3.2.3.2.95 CSCTI_CTIOUTEN6 Register

14.3.2.3.2.95.1 CSCTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

The CTI Channel to Trigger 6 Enable Registers define which channels can generate a ctitrigout[6] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

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Table 14-7937. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 30B8h
C7X256V0_DEBUG	0007 3400 A0B8h
C7X256V0_DEBUG	0007 3400 B0B8h
C7X256V1_DEBUG	0007 3800 30B8h
C7X256V1_DEBUG	0007 3800 A0B8h
C7X256V1_DEBUG	0007 3800 B0B8h

Figure 14-3942. CSCTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
NONE				R/W			
0h				0h			

Table 14-7938. CSCTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[6] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[6] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.3.2.3.2.96 CSCTI_CTIOUTEN7 Register

14.3.2.3.2.96.1 CSCTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

The CTI Channel to Trigger 7 Enable Registers define which channels can generate a ctitrigout[7] output. Within this register there is one bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

Return to Summary Table

Table 14-7939. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 30BCh
C7X256V0_DEBUG	0007 3400 A0BCh
C7X256V0_DEBUG	0007 3400 B0BCh
C7X256V1_DEBUG	0007 3800 30BCh
C7X256V1_DEBUG	0007 3800 A0BCh
C7X256V1_DEBUG	0007 3800 B0BCh

Figure 14-3943. CSCTI_CTIOUTEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7940. CSCTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	TRIGOUTEN	R/W	0h	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate a ctitrigout[7] output. There is one bit of the field for each of the four channels. When a 1 is written to a bit in this register, the channel input (ctichin) from the CTM is routed to the ctitrigout output. For example, enabling bit 0 enables ctichin[0] to cause a trigger event on the ctitrigout[7] output. When a 0 is written to any of the bits in this register, the channel input (ctichin) from the CTM is not routed to the ctitrigout output. Reading this register returns the programmed value.

14.3.2.3.2.97 CSCTI_CTITRIGINSTATUS Register

14.3.2.3.2.97.1 CSCTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

The CTI Trigger In Status Register provides the status of the ctitrigin inputs.

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Table 14-7941. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3130h
C7X256V0_DEBUG	0007 3400 A130h
C7X256V0_DEBUG	0007 3400 B130h
C7X256V1_DEBUG	0007 3800 3130h
C7X256V1_DEBUG	0007 3800 A130h
C7X256V1_DEBUG	0007 3800 B130h

Figure 14-3944. CSCTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-7942. CSCTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGINSTATUS	R	0h	Shows the status of the ctitrigin inputs. 1 = ctitrigin is active. 0 = ctitrigin is inactive. Because the register provides a view of the raw ctitrigin inputs, the reset value is unknown. There is one bit of the field for each trigger input.

14.3.2.3.2.98 CSCTI_CTITRIGOUTSTATUS Register

14.3.2.3.2.98.1 CSCTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

The CTI Trigger Out Status Register provides the status of the ctitrigout outputs.

Return to Summary Table

Table 14-7943. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3134h
C7X256V0_DEBUG	0007 3400 A134h
C7X256V0_DEBUG	0007 3400 B134h
C7X256V1_DEBUG	0007 3800 3134h
C7X256V1_DEBUG	0007 3800 A134h
C7X256V1_DEBUG	0007 3800 B134h

Figure 14-3945. CSCTI_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-7944. CSCTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the ctitrigout outputs. 1 = ctitrigout is active. 0 = ctitrigout is inactive. There is one bit of the field for each trigger output.

14.3.2.3.2.99 CSCTI_CTICHINSTATUS Register

14.3.2.3.2.99.1 CSCTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

The CTI Channel In Status Register provides the status of the ctichin inputs.

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Table 14-7945. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3138h
C7X256V0_DEBUG	0007 3400 A138h
C7X256V0_DEBUG	0007 3400 B138h
C7X256V1_DEBUG	0007 3800 3138h
C7X256V1_DEBUG	0007 3800 A138h
C7X256V1_DEBUG	0007 3800 B138h

Figure 14-3946. CSCTI_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHINSTATUS			
NONE				R			
0h				0h			

Table 14-7946. CSCTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHINSTATUS	R	0h	Shows the status of the ctichin inputs. 1 = ctichin is active. 0 = ctichin is inactive. Because the register provides a view of the raw ctichin inputs, the reset value is unknown. There is one bit of the field for each channel input.

14.3.2.3.2.100 CSCTI_CTICHOUTSTATUS Register

14.3.2.3.2.100.1 CSCTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

The CTI Channel Out Status Register provides the status of the CTI ctichout outputs.

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Table 14-7947. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 313Ch
C7X256V0_DEBUG	0007 3400 A13Ch
C7X256V0_DEBUG	0007 3400 B13Ch
C7X256V1_DEBUG	0007 3800 313Ch
C7X256V1_DEBUG	0007 3800 A13Ch
C7X256V1_DEBUG	0007 3800 B13Ch

Figure 14-3947. CSCTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTICHOUTSTATUS			
NONE				R			
0h				0h			

Table 14-7948. CSCTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTICHOUTSTATUS	R	0h	Shows the status of the ctichout outputs. 1 = ctichout is active. 0 = ctichout is inactive. There is one bit of the field for each channel output.

14.3.2.3.2.101 CSCTI_CTIGATE Register

14.3.2.3.2.101.1 CSCTI_CTIGATE Register (Offset = 140h) [reset = Fh]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

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Table 14-7949. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3140h
C7X256V0_DEBUG	0007 3400 A140h
C7X256V0_DEBUG	0007 3400 B140h
C7X256V1_DEBUG	0007 3800 3140h
C7X256V1_DEBUG	0007 3800 A140h
C7X256V1_DEBUG	0007 3800 B140h

Figure 14-3948. CSCTI_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0
NONE				R/W	R/W	R/W	R/W
0h				1h	1h	1h	1h

Table 14-7950. CSCTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CTIGATEEN3	R/W	1h	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	R/W	1h	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	R/W	1h	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	R/W	1h	Enable CTICHOUT0. Set to 0 to disable channel propagation.

14.3.2.3.2.102 CSCTI_ASICCTL Register

14.3.2.3.2.102.1 CSCTI_ASICCTL Register (Offset = 144h) [reset = 0h]

Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0].

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Table 14-7951. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3144h
C7X256V0_DEBUG	0007 3400 A144h
C7X256V0_DEBUG	0007 3400 B144h
C7X256V1_DEBUG	0007 3800 3144h
C7X256V1_DEBUG	0007 3800 A144h
C7X256V1_DEBUG	0007 3800 B144h

Figure 14-3949. CSCTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-7952. CSCTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on asicctl[7 : 0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

14.3.2.3.2.103 CSCTI_ITCHINACK Register

14.3.2.3.2.103.1 CSCTI_ITCHINACK Register (Offset = EDCh) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHINACK outputs.

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Table 14-7953. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3EDCh
C7X256V0_DEBUG	0007 3400 AEDCh
C7X256V0_DEBUG	0007 3400 BEDCh
C7X256V1_DEBUG	0007 3800 3EDCh
C7X256V1_DEBUG	0007 3800 AEDCh
C7X256V1_DEBUG	0007 3800 BEDCh

Figure 14-3950. CSCTI_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
NONE				R/W			
0h				0h			

Table 14-7954. CSCTI_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHINACK	R/W	0h	Set the value of the CTCHINACK outputs.

14.3.2.3.2.104 CSCTI_ITTRIGINACK Register

14.3.2.3.2.104.1 CSCTI_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGINACK outputs.

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Table 14-7955. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3EE0h
C7X256V0_DEBUG	0007 3400 AEE0h
C7X256V0_DEBUG	0007 3400 BEE0h
C7X256V1_DEBUG	0007 3800 3EE0h
C7X256V1_DEBUG	0007 3800 AEE0h
C7X256V1_DEBUG	0007 3800 BEE0h

Figure 14-3951. CSCTI_ITTRIGINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGINACK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-7956. CSCTI_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGINACK	R/W	0h	Set the value of the CTTRIGINACK outputs.

14.3.2.3.2.105 CSCTI_ITCHOUT Register

14.3.2.3.2.105.1 CSCTI_ITCHOUT Register (Offset = EE4h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTCHOUT outputs.

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Table 14-7957. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3EE4h
C7X256V0_DEBUG	0007 3400 AEE4h
C7X256V0_DEBUG	0007 3400 BEE4h
C7X256V1_DEBUG	0007 3800 3EE4h
C7X256V1_DEBUG	0007 3800 AEE4h
C7X256V1_DEBUG	0007 3800 BEE4h

Figure 14-3952. CSCTI_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
NONE				R/W			
0h				0h			

Table 14-7958. CSCTI_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUT	R/W	0h	Set the value of the CTCHOUT outputs.

14.3.2.3.2.106 CSCTI_ITTRIGOUT Register

14.3.2.3.2.106.1 CSCTI_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

This register is a write-only register. It can be used to set the value of the CTTRIGOUT outputs.

Return to Summary Table

Table 14-7959. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3EE8h
C7X256V0_DEBUG	0007 3400 AEE8h
C7X256V0_DEBUG	0007 3400 BEE8h
C7X256V1_DEBUG	0007 3800 3EE8h
C7X256V1_DEBUG	0007 3800 AEE8h
C7X256V1_DEBUG	0007 3800 BEE8h

Figure 14-3953. CSCTI_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-7960. CSCTI_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUT	R/W	0h	Set the value of the CTTRIGOUT outputs.

14.3.2.3.2.107 CSCTI_ITCHOUTACK Register

14.3.2.3.2.107.1 CSCTI_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHOUTACK inputs.

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Table 14-7961. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3EECh
C7X256V0_DEBUG	0007 3400 AEECh
C7X256V0_DEBUG	0007 3400 BEECh
C7X256V1_DEBUG	0007 3800 3EECh
C7X256V1_DEBUG	0007 3800 AEECh
C7X256V1_DEBUG	0007 3800 BEECh

Figure 14-3954. CSCTI_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUTACK			
NONE				R			
0h				0h			

Table 14-7962. CSCTI_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHOUTACK	R	0h	Read the values of the CTCHOUTACK inputs.

14.3.2.3.2.108 CSCTI_ITTRIGOUTACK Register

14.3.2.3.2.108.1 CSCTI_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGOUTACK inputs.

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Table 14-7963. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3EF0h
C7X256V0_DEBUG	0007 3400 AEF0h
C7X256V0_DEBUG	0007 3400 BEF0h
C7X256V1_DEBUG	0007 3800 3EF0h
C7X256V1_DEBUG	0007 3800 AEF0h
C7X256V1_DEBUG	0007 3800 BEF0h

Figure 14-3955. CSCTI_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-7964. CSCTI_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGOUTACK	R	0h	Read the value of the CTTRIGOUTACK inputs.

14.3.2.3.2.109 CSCTI_ITCHIN Register

14.3.2.3.2.109.1 CSCTI_ITCHIN Register (Offset = EF4h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTCHIN inputs.

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Table 14-7965. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3EF4h
C7X256V0_DEBUG	0007 3400 AEF4h
C7X256V0_DEBUG	0007 3400 BEF4h
C7X256V1_DEBUG	0007 3800 3EF4h
C7X256V1_DEBUG	0007 3800 AEF4h
C7X256V1_DEBUG	0007 3800 BEF4h

Figure 14-3956. CSCTI_ITCHIN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHIN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7966. CSCTI_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CTCHIN	R	0h	Read the value of the CTCHIN inputs.

14.3.2.3.2.110 CSCTI_ITTRIGIN Register

14.3.2.3.2.110.1 CSCTI_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

This register is a read-only register. It can be used to read the values of the CTTRIGIN inputs.

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Table 14-7967. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3EF8h
C7X256V0_DEBUG	0007 3400 AEF8h
C7X256V0_DEBUG	0007 3400 BEF8h
C7X256V1_DEBUG	0007 3800 3EF8h
C7X256V1_DEBUG	0007 3800 AEF8h
C7X256V1_DEBUG	0007 3800 BEF8h

Figure 14-3957. CSCTI_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-7968. CSCTI_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CTTRIGIN	R	0h	Read the values of the CTTRIGIN inputs.

14.3.2.3.2.111 CSCTI_ITCTRL Register

14.3.2.3.2.111.1 CSCTI_ITCTRL Register (Offset = F00h) [reset = 0h]

This register is used to enable topology detection. For more information see the CoreSight Architecture Specification. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving. Note : When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

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Table 14-7969. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3F00h
C7X256V0_DEBUG	0007 3400 AF00h
C7X256V0_DEBUG	0007 3400 BF00h
C7X256V1_DEBUG	0007 3800 3F00h
C7X256V1_DEBUG	0007 3800 AF00h
C7X256V1_DEBUG	0007 3800 BF00h

Figure 14-3958. CSCTI_ITCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INTEGRATION_MODE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-7970. CSCTI_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INTEGRATION_MODE	R/W	0h	Allows the component to switch from functional mode to integration mode or back.

14.3.2.3.2.112 CSCTI_CLAIMSET Register

14.3.2.3.2.112.1 CSCTI_CLAIMSET Register (Offset = FA0h) [reset = 0h]

This is used in conjunction with Claim Tag Clear Register, CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

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Table 14-7971. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FA0h
C7X256V0_DEBUG	0007 3400 AFA0h
C7X256V0_DEBUG	0007 3400 BFA0h
C7X256V1_DEBUG	0007 3800 3FA0h
C7X256V1_DEBUG	0007 3800 AFA0h
C7X256V1_DEBUG	0007 3800 BFA0h

Figure 14-3959. CSCTI_CLAIMSET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIMSET</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-7972. CSCTI_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMSET	R/W	0h	This claim tag bit is implemented

14.3.2.3.2.113 CSCTI_CLAIMCLR Register

14.3.2.3.2.113.1 CSCTI_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

This register is used in conjunction with Claim Tag Set Register, CLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

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Table 14-7973. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FA4h
C7X256V0_DEBUG	0007 3400 AFA4h
C7X256V0_DEBUG	0007 3400 BFA4h
C7X256V1_DEBUG	0007 3800 3FA4h
C7X256V1_DEBUG	0007 3800 AFA4h
C7X256V1_DEBUG	0007 3800 BFA4h

Figure 14-3960. CSCTI_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLAIMCLR			
NONE				R/W			
0h				0h			

Table 14-7974. CSCTI_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CLAIMCLR	R/W	0h	The value present reflects the current setting of the Claim Tag.

14.3.2.3.2.114 CSCTI_LOCKACCESS Register

14.3.2.3.2.114.1 CSCTI_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

This is used to enable write access to device registers. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. A debugger does not have to unlock the component in order to write and modify the registers in the component.

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Table 14-7975. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FB0h
C7X256V0_DEBUG	0007 3400 AFB0h
C7X256V0_DEBUG	0007 3400 BFB0h
C7X256V1_DEBUG	0007 3800 3FB0h
C7X256V1_DEBUG	0007 3800 AFB0h
C7X256V1_DEBUG	0007 3800 BFB0h

Figure 14-3961. CSCTI_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
ACCESS_W							
R/W							
0h							
23	22	21	20	19	18	17	16
ACCESS_W							
R/W							
0h							
15	14	13	12	11	10	9	8
ACCESS_W							
R/W							
0h							
7	6	5	4	3	2	1	0
ACCESS_W							
R/W							
0h							

Table 14-7976. CSCTI_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ACCESS_W	R/W	0h	A write of 0xC5ACCE55 enables further write access to this device. A write of any value other than 0xC5ACCE55 will have the affect of removing write access.

14.3.2.3.2.115 CSCTI_LOCKSTATUS Register

14.3.2.3.2.115.1 CSCTI_LOCKSTATUS Register (Offset = FB4h) [reset = 3h]

This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug. When locked, write access is blocked to all registers, except the Lock Access Register. External accesses from a debugger (paddrdbg31 = 1) are not subject to the Lock Registers. This register reads as 0 when read from an external debugger (paddrdbg31 = 1).

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Table 14-7977. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FB4h
C7X256V0_DEBUG	0007 3400 AFB4h
C7X256V0_DEBUG	0007 3400 BFB4h
C7X256V1_DEBUG	0007 3800 3FB4h
C7X256V1_DEBUG	0007 3800 AFB4h
C7X256V1_DEBUG	0007 3800 BFB4h

Figure 14-3962. CSCTI_LOCKSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>LOCKTYPE</td><td>LOCKGRANT</td><td>LOCKEXIST</td></tr>
<tr><td colspan="5">NONE</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-7978. CSCTI_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	LOCKTYPE	R	0h	Indicates if the Lock Access Register (0xFB0) is implemented as 8-bit or 32-bit
1	LOCKGRANT	R	1h	Returns the current status of the Lock. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.
0	LOCKEXIST	R	1h	Indicates that a lock control mechanism exists for this device. This bit reads as 0 when read from an external debugger (paddrdbg31 = 1) since external debugger accesses are not subject to Lock Registers.

14.3.2.3.2.116 CSCTI_AUTHSTATUS Register

14.3.2.3.2.116.1 CSCTI_AUTHSTATUS Register (Offset = FB8h) [reset = Ah]

Reports what functionality is currently permitted by the authentication interface.

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Table 14-7979. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FB8h
C7X256V0_DEBUG	0007 3400 AFB8h
C7X256V0_DEBUG	0007 3400 BFB8h
C7X256V1_DEBUG	0007 3800 3FB8h
C7X256V1_DEBUG	0007 3800 AFB8h
C7X256V1_DEBUG	0007 3800 BFB8h

Figure 14-3963. CSCTI_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		2h		2h	

Table 14-7980. CSCTI_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SNID	R	0h	Indicates the security level for secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for secure invasive debug
3:2	NSNID	R	2h	Indicates the security level for non-secure non-invasive debug
1:0	NSID	R	2h	Indicates the security level for non-secure invasive debug

14.3.2.3.2.117 CSCTI_DEVID Register

14.3.2.3.2.117.1 CSCTI_DEVID Register (Offset = FC8h) [reset = 40800h]

This register indicates the capabilities of the CTI.

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Table 14-7981. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FC8h
C7X256V0_DEBUG	0007 3400 AFC8h
C7X256V0_DEBUG	0007 3400 BFC8h
C7X256V1_DEBUG	0007 3800 3FC8h
C7X256V1_DEBUG	0007 3800 AFC8h
C7X256V1_DEBUG	0007 3800 BFC8h

Figure 14-3964. CSCTI_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUMCH</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUMTRIG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">EXTMUXNUM</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-7982. CSCTI_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NUMCH	R	4h	Number of ECT channels available.
15:8	NUMTRIG	R	8h	Number of ECT triggers available.
7:5	RESERVED	NONE	0h	Reserved
4:0	EXTMUXNUM	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using asicctl. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog define EXTMUXNUM that the user must alter accordingly.

14.3.2.3.2.118 CSCTI_DEVTYPE Register

14.3.2.3.2.118.1 CSCTI_DEVTYPE Register (Offset = FCCh) [reset = 14h]

It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

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Table 14-7983. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FCCh
C7X256V0_DEBUG	0007 3400 AFCCh
C7X256V0_DEBUG	0007 3400 BFCCh
C7X256V1_DEBUG	0007 3800 3FCCh
C7X256V1_DEBUG	0007 3800 AFCCh
C7X256V1_DEBUG	0007 3800 BFCCh

Figure 14-3965. CSCTI_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SUB_TYPE				MAJOR_TYPE			
R				R			
1h				4h			

Table 14-7984. CSCTI_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SUB_TYPE	R	1h	Sub-classification within the major category
3:0	MAJOR_TYPE	R	4h	Major classification grouping for this debug/trace component

14.3.2.3.2.119 CSCTI_PERIPHID4 Register

14.3.2.3.2.119.1 CSCTI_PERIPHID4 Register (Offset = FD0h) [reset = 4h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

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Table 14-7985. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FD0h
C7X256V0_DEBUG	0007 3400 AFD0h
C7X256V0_DEBUG	0007 3400 BFD0h
C7X256V1_DEBUG	0007 3800 3FD0h
C7X256V1_DEBUG	0007 3800 AFD0h
C7X256V1_DEBUG	0007 3800 BFD0h

Figure 14-3966. CSCTI_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-7986. CSCTI_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SIZE	R	0h	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB then this should read as 0x0, 4KB only, for 8KB set to 0x1, 16KB == 0x2, 32KB == 0x3, and so on.
3:0	DES_2	R	4h	JEDEC continuation code indicating the designer of the component (along with the identity code)

14.3.2.3.2.120 CSCTI_PERIPHID0 Register

14.3.2.3.2.120.1 CSCTI_PERIPHID0 Register (Offset = FE0h) [reset = 6h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

Return to Summary Table

Table 14-7987. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FE0h
C7X256V0_DEBUG	0007 3400 AFE0h
C7X256V0_DEBUG	0007 3400 BFE0h
C7X256V1_DEBUG	0007 3800 3FE0h
C7X256V1_DEBUG	0007 3800 AFE0h
C7X256V1_DEBUG	0007 3800 BFE0h

Figure 14-3967. CSCTI_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
6h							

Table 14-7988. CSCTI_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PART_0	R	6h	Bits [7 : 0] of the component's part number. This is selected by the designer of the component.

14.3.2.3.2.121 CSCTI_PERIPHID1 Register

14.3.2.3.2.121.1 CSCTI_PERIPHID1 Register (Offset = FE4h) [reset = 9h]

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

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Table 14-7989. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FE4h
C7X256V0_DEBUG	0007 3400 AFE4h
C7X256V0_DEBUG	0007 3400 BFE4h
C7X256V1_DEBUG	0007 3800 3FE4h
C7X256V1_DEBUG	0007 3800 AFE4h
C7X256V1_DEBUG	0007 3800 BFE4h

Figure 14-3968. CSCTI_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DES_0				PART_1			
R				R			
0h				9h			

Table 14-7990. CSCTI_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	DES_0	R	0h	Bits 3 : 0 of the JEDEC identity code indicating the designer of the component (along with the continuation code)
3:0	PART_1	R	9h	Bits [11 : 8] of the component's part number. This is selected by the designer of the component.

14.3.2.3.2.122 CSCTI_PERIPHID2 Register

14.3.2.3.2.122.1 CSCTI_PERIPHID2 Register (Offset = FE8h) [reset = 48h]

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

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Table 14-7991. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FE8h
C7X256V0_DEBUG	0007 3400 AFE8h
C7X256V0_DEBUG	0007 3400 BFE8h
C7X256V1_DEBUG	0007 3800 3FE8h
C7X256V1_DEBUG	0007 3800 AFE8h
C7X256V1_DEBUG	0007 3800 BFE8h

Figure 14-3969. CSCTI_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
4h				1h	0h		

Table 14-7992. CSCTI_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVISION	R	4h	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is simply used as a look-up to establish the exact major/minor revision.
3	JEDEC	R	1h	Always set. Indicates that a JEDEC assigned value is used
2:0	DES_1	R	0h	Bits 6 : 4 of the JEDEC identity code indicating the designer of the component (along with the continuation code)

14.3.2.3.2.123 CSCTI_PERIPHID3 Register

14.3.2.3.2.123.1 CSCTI_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

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Table 14-7993. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FECh
C7X256V0_DEBUG	0007 3400 AFECh
C7X256V0_DEBUG	0007 3400 BFECh
C7X256V1_DEBUG	0007 3800 3FECh
C7X256V1_DEBUG	0007 3800 AFECh
C7X256V1_DEBUG	0007 3800 BFECh

Figure 14-3970. CSCTI_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVAND				CMOD			
R				R			
0h				0h			

Table 14-7994. CSCTI_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	REVAND	R	0h	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero.
3:0	CMOD	R	0h	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero.

14.3.2.3.2.124 CSCTI_COMPID0 Register

14.3.2.3.2.124.1 CSCTI_COMPID0 Register (Offset = FF0h) [reset = Dh]

Reserved Reserved Reserved A component identification register, that indicates that the identification registers are present.

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Table 14-7995. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FF0h
C7X256V0_DEBUG	0007 3400 AFF0h
C7X256V0_DEBUG	0007 3400 BFF0h
C7X256V1_DEBUG	0007 3800 3FF0h
C7X256V1_DEBUG	0007 3800 AFF0h
C7X256V1_DEBUG	0007 3800 BFF0h

Figure 14-3971. CSCTI_COMPID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRMBL_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Dh</td></tr>
</table>

Table 14-7996. CSCTI_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_0	R	Dh	Contains bits [7 : 0] of the component identification

14.3.2.3.2.125 CSCTI_COMPID1 Register

14.3.2.3.2.125.1 CSCTI_COMPID1 Register (Offset = FF4h) [reset = 90h]

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

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Table 14-7997. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FF4h
C7X256V0_DEBUG	0007 3400 AFF4h
C7X256V0_DEBUG	0007 3400 BFF4h
C7X256V1_DEBUG	0007 3800 3FF4h
C7X256V1_DEBUG	0007 3800 AFF4h
C7X256V1_DEBUG	0007 3800 BFF4h

Figure 14-3972. CSCTI_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-7998. CSCTI_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CLASS	R	9h	Class of the component. E.g. ROM table, CoreSight component etc. Constitutes bits [15 : 12] of the component identification.
3:0	PRMBL_1	R	0h	Contains bits [11 : 8] of the component identification

14.3.2.3.2.126 CSCTI_COMPID2 Register

14.3.2.3.2.126.1 CSCTI_COMPID2 Register (Offset = FF8h) [reset = 5h]

A component identification register, that indicates that the identification registers are present.

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Table 14-7999. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FF8h
C7X256V0_DEBUG	0007 3400 AFF8h
C7X256V0_DEBUG	0007 3400 BFF8h
C7X256V1_DEBUG	0007 3800 3FF8h
C7X256V1_DEBUG	0007 3800 AFF8h
C7X256V1_DEBUG	0007 3800 BFF8h

Figure 14-3973. CSCTI_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_2							
R							
5h							

Table 14-8000. CSCTI_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_2	R	5h	Contains bits [23 : 16] of the component identification

14.3.2.3.2.127 CSCTI_COMPID3 Register

14.3.2.3.2.127.1 CSCTI_COMPID3 Register (Offset = FFCh) [reset = 0h]

A component identification register, that indicates that the identification registers are present.

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Table 14-8001. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 3FFCh
C7X256V0_DEBUG	0007 3400 AFFCh
C7X256V0_DEBUG	0007 3400 BFFCh
C7X256V1_DEBUG	0007 3800 3FFCh
C7X256V1_DEBUG	0007 3800 AFFCh
C7X256V1_DEBUG	0007 3800 BFFCh

Figure 14-3974. CSCTI_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRMBL_3							
R							
0h							

Table 14-8002. CSCTI_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRMBL_3	R	0h	Contains bits [31 : 24] of the component identification

14.3.2.3.2.128 CTSET2_CFG_CTSETID Register

14.3.2.3.2.128.1 CTSET2_CFG_CTSETID Register (Offset = 0h) [reset = 62800200h]

CTSET identification register

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Table 14-8003. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8000h

Figure 14-3975. CTSET2_CFG_CTSETID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		280h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
280h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VERSION					MAJOR_REV		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-8004. CTSET2_CFG_CTSETID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old Scheme and current
29:28	BU	R	2h	The value 10b designates this as Processor Business Unit IP
27:16	FUNCTION	R	280h	Function : Indicates a Debug IP (0x2nn) and 0x80 is the identifier for CT-SET
15:11	RTL_VERSION	R	0h	This field changes on bug fix, and resets to '0' when either Minor Revision or Major Revision field changes
10:8	MAJOR_REV	R	2h	Major Revision. This field changes when there is a major feature change.
7:6	CUSTOM	R	0h	Indicates a special version for a particular device. 0 if non-custom
5:0	MINOR_REV	R	0h	Minor Revision. This field changes when features are scaled up or down

14.3.2.3.2.129 CTSET2_CFG_CTSETSYSCFG Register

14.3.2.3.2.129.1 CTSET2_CFG_CTSETSYSCFG Register (Offset = 10h) [reset = 8h]

CTSET system configuration register

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Table 14-8005. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8010h

Figure 14-3976. CTSET2_CFG_CTSETSYSCFG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				IDLEMODE		RESERVED	SOFTRESET
R				R/W		R	R/W
0h				2h		0h	0h

Table 14-8006. CTSET2_CFG_CTSETSYSCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED1	R	0h	Reserved, returns 0
3:2	IDLEMODE	R/W	2h	Sets the Idle Mode for CTSET (0=Force Idle, 1=No Idle, 2=Smart Idle, 3= Smart Idle wakeup)
1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	This will reset entire CTSET, except the registers and the CFG interface. This bit is automatically cleared by hardware. Reads always return 0

14.3.2.3.2.130 CTSET2_CFG_SETSTR Register

14.3.2.3.2.130.1 CTSET2_CFG_SETSTR Register (Offset = 14h) [reset = 101h]

CTSET status register

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Table 14-8007. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8014h

Figure 14-3977. CTSET2_CFG_SETSTR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED1</td><td>HWFIFOEMPTY</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>RESETDONE</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>1h</td></tr>
</table>

Table 14-8008. CTSET2_CFG_SETSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8	HWFIFOEMPTY	R	1h	System Event Trace FIFO status, 1 is empty, 0 means captured data not yet exported
7:1	RESERVED	R	0h	Reserved, returns 0
0	RESETDONE	R	1h	Reset status, 0 means reset ongoing, 1 indicates completed

14.3.2.3.2.131 CTSET2_CFG_DBGTIMELOW Register

14.3.2.3.2.131.1 CTSET2_CFG_DBGTIMELOW Register (Offset = 18h) [reset = 0h]

The 32 low order bits of the debug time value supplied on the time input interface

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Table 14-8009. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8018h

Figure 14-3978. CTSET2_CFG_DBGTIMELOW Name Register

31	30	29	28	27	26	25	24
DBGTIME							
R							
0h							
23	22	21	20	19	18	17	16
DBGTIME							
R							
0h							
15	14	13	12	11	10	9	8
DBGTIME							
R							
0h							
7	6	5	4	3	2	1	0
DBGTIME							
R							
0h							

Table 14-8010. CTSET2_CFG_DBGTIMELOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGTIME	R	0h	debug time

14.3.2.3.2.132 CTSET2_CFG_DBGTIMEHI Register

14.3.2.3.2.132.1 CTSET2_CFG_DBGTIMEHI Register (Offset = 1Ch) [reset = 0h]

The 32 high order bits of the debug time value supplied on the time input interface

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Table 14-8011. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 801Ch

Figure 14-3979. CTSET2_CFG_DBGTIMEHI Name Register

31	30	29	28	27	26	25	24
DBGTIME							
R							
0h							
23	22	21	20	19	18	17	16
DBGTIME							
R							
0h							
15	14	13	12	11	10	9	8
DBGTIME							
R							
0h							
7	6	5	4	3	2	1	0
DBGTIME							
R							
0h							

Table 14-8012. CTSET2_CFG_DBGTIMEHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGTIME	R	0h	debug time

14.3.2.3.2.133 CTSET2_CFG_CTSETCFG Register

14.3.2.3.2.133.1 CTSET2_CFG_CTSETCFG Register (Offset = 24h) [reset = 20000010h]

The 32 low order bits of the debug time value supplied on the time input interface The 32 high order bits of the debug time value supplied on the time input interface. Reading DBGTIMEHI latches the lower 32 bits of debug time value CTSET configuration register

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Table 14-8013. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8024h

Figure 14-3980. CTSET2_CFG_CTSETCFG Name Register

31	30	29	28	27	26	25	24
CLAIM				RESERVED2			
R/W				R			
2h				0h			
23	22	21	20	19	18	17	16
RESERVED2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
SYSEVENTCAPTEN	RESERVED1		EVENTLEVEL	MSGMODE	STOPCAPT	STARTCAPT	RESERVED
R/W	R		R/W	R/W	R/W	R/W	R
0h	0h		1h	0h	0h	0h	0h

Table 14-8014. CTSET2_CFG_CTSETCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CLAIM	R/W	2h	Claim control and status. To program any bits other than 31 : 28, CTSET ownership must be claimed using bits 31 : 28.
27:8	RESERVED2	R	0h	Reserved, returns 0
7	SYSEVENTCAPTEN	R/W	0h	When 1 the System event capture is enabled
6:5	RESERVED1	R	0h	Reserved, returns 0
4	EVENTLEVEL	R/W	1h	0 enables low level event detection, 1 enables high level event detection
3	MSGMODE	R/W	0h	Message generated based on event detection, 0 is sampling window, 1 is event detection
2	STOPCAPT	R/W	0h	Stop capturing system events from external trigger detection
1	STARTCAPT	R/W	0h	Start capturing system events from external trigger detection
0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.134 CTSET2_CFG_SETSPLREG Register

14.3.2.3.2.134.1 CTSET2_CFG_SETSPLREG Register (Offset = 28h) [reset = 0h]

System Event Sampling Window register

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Table 14-8015. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8028h

Figure 14-3981. CTSET2_CFG_SETSPLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
WINDOWSIZE							
R/W							
0h							

Table 14-8016. CTSET2_CFG_SETSPLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	WINDOWSIZE	R/W	0h	System events sampling window size expressed as CTSET cycles

14.3.2.3.2.135 CTSET2_CFG_SETEVTENBL1 Register

14.3.2.3.2.135.1 CTSET2_CFG_SETEVTENBL1 Register (Offset = 30h) [reset = 0h]

System event detection enable register 1

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Table 14-8017. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8030h

Figure 14-3982. CTSET2_CFG_SETEVTENBL1 Name Register

31	30	29	28	27	26	25	24
EVENT32DETEN	EVENT31DETEN	EVENT30DETEN	EVENT29DETEN	EVENT28DETEN	EVENT27DETEN	EVENT26DETEN	EVENT25DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT24DETEN	EVENT23DETEN	EVENT22DETEN	EVENT21DETEN	EVENT20DETEN	EVENT19DETEN	EVENT18DETEN	EVENT17DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT16DETEN	EVENT15DETEN	EVENT14DETEN	EVENT13DETEN	EVENT12DETEN	EVENT11DETEN	EVENT10DETEN	EVENT9DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT8DETEN	EVENT7DETEN	EVENT6DETEN	EVENT5DETEN	EVENT4DETEN	EVENT3DETEN	EVENT2DETEN	EVENT1DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8018. CTSET2_CFG_SETEVTENBL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT32DETEN	R/W	0h	Event(32) Detection Enable
30	EVENT31DETEN	R/W	0h	Event(31) Detection Enable
29	EVENT30DETEN	R/W	0h	Event(30) Detection Enable
28	EVENT29DETEN	R/W	0h	Event(29) Detection Enable
27	EVENT28DETEN	R/W	0h	Event(28) Detection Enable
26	EVENT27DETEN	R/W	0h	Event(27) Detection Enable
25	EVENT26DETEN	R/W	0h	Event(26) Detection Enable
24	EVENT25DETEN	R/W	0h	Event(25) Detection Enable
23	EVENT24DETEN	R/W	0h	Event(24) Detection Enable
22	EVENT23DETEN	R/W	0h	Event(23) Detection Enable
21	EVENT22DETEN	R/W	0h	Event(22) Detection Enable
20	EVENT21DETEN	R/W	0h	Event(21) Detection Enable
19	EVENT20DETEN	R/W	0h	Event(20) Detection Enable
18	EVENT19DETEN	R/W	0h	Event(19) Detection Enable
17	EVENT18DETEN	R/W	0h	Event(18) Detection Enable
16	EVENT17DETEN	R/W	0h	Event(17) Detection Enable
15	EVENT16DETEN	R/W	0h	Event(16) Detection Enable

Table 14-8018. CTSET2_CFG_SETEVTENBL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT15DETEN	R/W	0h	Event(15) Detection Enable
13	EVENT14DETEN	R/W	0h	Event(14) Detection Enable
12	EVENT13DETEN	R/W	0h	Event(13) Detection Enable
11	EVENT12DETEN	R/W	0h	Event(12) Detection Enable
10	EVENT11DETEN	R/W	0h	Event(11) Detection Enable
9	EVENT10DETEN	R/W	0h	Event(10) Detection Enable
8	EVENT9DETEN	R/W	0h	Event(9) Detection Enable
7	EVENT8DETEN	R/W	0h	Event(8) Detection Enable
6	EVENT7DETEN	R/W	0h	Event(7) Detection Enable
5	EVENT6DETEN	R/W	0h	Event(6) Detection Enable
4	EVENT5DETEN	R/W	0h	Event(5) Detection Enable
3	EVENT4DETEN	R/W	0h	Event(4) Detection Enable
2	EVENT3DETEN	R/W	0h	Event(3) Detection Enable
1	EVENT2DETEN	R/W	0h	Event(2) Detection Enable
0	EVENT1DETEN	R/W	0h	Event(1) Detection Enable

14.3.2.3.2.136 CTSET2_CFG_SETEVTENBL2 Register

14.3.2.3.2.136.1 CTSET2_CFG_SETEVTENBL2 Register (Offset = 34h) [reset = 0h]

System event detection enable register 2 (if number of events > 32)

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Table 14-8019. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8034h

Figure 14-3983. CTSET2_CFG_SETEVTENBL2 Name Register

31	30	29	28	27	26	25	24
EVENT64DETEN	EVENT63DETEN	EVENT62DETEN	EVENT61DETEN	EVENT60DETEN	EVENT59DETEN	EVENT58DETEN	EVENT57DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT56DETEN	EVENT55DETEN	EVENT54DETEN	EVENT53DETEN	EVENT52DETEN	EVENT51DETEN	EVENT50DETEN	EVENT49DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT48DETEN	EVENT47DETEN	EVENT46DETEN	EVENT45DETEN	EVENT44DETEN	EVENT43DETEN	EVENT42DETEN	EVENT41DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT40DETEN	EVENT39DETEN	EVENT38DETEN	EVENT37DETEN	EVENT36DETEN	EVENT35DETEN	EVENT34DETEN	EVENT33DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8020. CTSET2_CFG_SETEVTENBL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT64DETEN	R/W	0h	Event(64) Detection Enable
30	EVENT63DETEN	R/W	0h	Event(63) Detection Enable
29	EVENT62DETEN	R/W	0h	Event(62) Detection Enable
28	EVENT61DETEN	R/W	0h	Event(61) Detection Enable
27	EVENT60DETEN	R/W	0h	Event(60) Detection Enable
26	EVENT59DETEN	R/W	0h	Event(59) Detection Enable
25	EVENT58DETEN	R/W	0h	Event(58) Detection Enable
24	EVENT57DETEN	R/W	0h	Event(57) Detection Enable
23	EVENT56DETEN	R/W	0h	Event(56) Detection Enable
22	EVENT55DETEN	R/W	0h	Event(55) Detection Enable
21	EVENT54DETEN	R/W	0h	Event(54) Detection Enable
20	EVENT53DETEN	R/W	0h	Event(53) Detection Enable
19	EVENT52DETEN	R/W	0h	Event(52) Detection Enable
18	EVENT51DETEN	R/W	0h	Event(51) Detection Enable
17	EVENT50DETEN	R/W	0h	Event(50) Detection Enable
16	EVENT49DETEN	R/W	0h	Event(49) Detection Enable
15	EVENT48DETEN	R/W	0h	Event(48) Detection Enable

Table 14-8020. CTSET2_CFG_SETEVTENBL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT47DETEN	R/W	0h	Event(47) Detection Enable
13	EVENT46DETEN	R/W	0h	Event(46) Detection Enable
12	EVENT45DETEN	R/W	0h	Event(45) Detection Enable
11	EVENT44DETEN	R/W	0h	Event(44) Detection Enable
10	EVENT43DETEN	R/W	0h	Event(43) Detection Enable
9	EVENT42DETEN	R/W	0h	Event(42) Detection Enable
8	EVENT41DETEN	R/W	0h	Event(41) Detection Enable
7	EVENT40DETEN	R/W	0h	Event(40) Detection Enable
6	EVENT39DETEN	R/W	0h	Event(39) Detection Enable
5	EVENT38DETEN	R/W	0h	Event(38) Detection Enable
4	EVENT37DETEN	R/W	0h	Event(37) Detection Enable
3	EVENT36DETEN	R/W	0h	Event(36) Detection Enable
2	EVENT35DETEN	R/W	0h	Event(35) Detection Enable
1	EVENT34DETEN	R/W	0h	Event(34) Detection Enable
0	EVENT33DETEN	R/W	0h	Event(33) Detection Enable

14.3.2.3.2.137 CTSET2_CFG_SETEVTENBL3 Register

14.3.2.3.2.137.1 CTSET2_CFG_SETEVTENBL3 Register (Offset = 38h) [reset = 0h]

System event detection enable register 3 (if number of events > 64)

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Table 14-8021. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8038h

Figure 14-3984. CTSET2_CFG_SETEVTENBL3 Name Register

31	30	29	28	27	26	25	24
EVENT96DETEN	EVENT95DETEN	EVENT94DETEN	EVENT93DETEN	EVENT92DETEN	EVENT91DETEN	EVENT90DETEN	EVENT89DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT88DETEN	EVENT87DETEN	EVENT86DETEN	EVENT85DETEN	EVENT84DETEN	EVENT83DETEN	EVENT82DETEN	EVENT81DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT80DETEN	EVENT79DETEN	EVENT78DETEN	EVENT77DETEN	EVENT76DETEN	EVENT75DETEN	EVENT74DETEN	EVENT73DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT72DETEN	EVENT71DETEN	EVENT70DETEN	EVENT69DETEN	EVENT68DETEN	EVENT67DETEN	EVENT66DETEN	EVENT65DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8022. CTSET2_CFG_SETEVTENBL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT96DETEN	R/W	0h	Event(96) Detection Enable
30	EVENT95DETEN	R/W	0h	Event(95) Detection Enable
29	EVENT94DETEN	R/W	0h	Event(94) Detection Enable
28	EVENT93DETEN	R/W	0h	Event(93) Detection Enable
27	EVENT92DETEN	R/W	0h	Event(92) Detection Enable
26	EVENT91DETEN	R/W	0h	Event(91) Detection Enable
25	EVENT90DETEN	R/W	0h	Event(90) Detection Enable
24	EVENT89DETEN	R/W	0h	Event(89) Detection Enable
23	EVENT88DETEN	R/W	0h	Event(88) Detection Enable
22	EVENT87DETEN	R/W	0h	Event(87) Detection Enable
21	EVENT86DETEN	R/W	0h	Event(86) Detection Enable
20	EVENT85DETEN	R/W	0h	Event(85) Detection Enable
19	EVENT84DETEN	R/W	0h	Event(84) Detection Enable
18	EVENT83DETEN	R/W	0h	Event(83) Detection Enable
17	EVENT82DETEN	R/W	0h	Event(82) Detection Enable
16	EVENT81DETEN	R/W	0h	Event(81) Detection Enable
15	EVENT80DETEN	R/W	0h	Event(80) Detection Enable

Table 14-8022. CTSET2_CFG_SETEVTENBL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT79DETEN	R/W	0h	Event(79) Detection Enable
13	EVENT78DETEN	R/W	0h	Event(78) Detection Enable
12	EVENT77DETEN	R/W	0h	Event(77) Detection Enable
11	EVENT76DETEN	R/W	0h	Event(76) Detection Enable
10	EVENT75DETEN	R/W	0h	Event(75) Detection Enable
9	EVENT74DETEN	R/W	0h	Event(74) Detection Enable
8	EVENT73DETEN	R/W	0h	Event(73) Detection Enable
7	EVENT72DETEN	R/W	0h	Event(72) Detection Enable
6	EVENT71DETEN	R/W	0h	Event(71) Detection Enable
5	EVENT70DETEN	R/W	0h	Event(70) Detection Enable
4	EVENT69DETEN	R/W	0h	Event(69) Detection Enable
3	EVENT68DETEN	R/W	0h	Event(68) Detection Enable
2	EVENT67DETEN	R/W	0h	Event(67) Detection Enable
1	EVENT66DETEN	R/W	0h	Event(66) Detection Enable
0	EVENT65DETEN	R/W	0h	Event(65) Detection Enable

14.3.2.3.2.138 CTSET2_CFG_SETEVTENBL4 Register

14.3.2.3.2.138.1 CTSET2_CFG_SETEVTENBL4 Register (Offset = 3Ch) [reset = 0h]

System event detection enable register 4 (if number of events > 96)

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Table 14-8023. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 803Ch

Figure 14-3985. CTSET2_CFG_SETEVTENBL4 Name Register

31	30	29	28	27	26	25	24
EVENT128DETEN	EVENT127DETEN	EVENT126DETEN	EVENT125DETEN	EVENT124DETEN	EVENT123DETEN	EVENT122DETEN	EVENT121DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT120DETEN	EVENT119DETEN	EVENT118DETEN	EVENT117DETEN	EVENT116DETEN	EVENT115DETEN	EVENT114DETEN	EVENT113DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT112DETEN	EVENT111DETEN	EVENT110DETEN	EVENT109DETEN	EVENT108DETEN	EVENT107DETEN	EVENT106DETEN	EVENT105DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT104DETEN	EVENT103DETEN	EVENT102DETEN	EVENT101DETEN	EVENT100DETEN	EVENT99DETEN	EVENT98DETEN	EVENT97DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8024. CTSET2_CFG_SETEVTENBL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT128DETEN	R/W	0h	Event(128) Detection Enable
30	EVENT127DETEN	R/W	0h	Event(127) Detection Enable
29	EVENT126DETEN	R/W	0h	Event(126) Detection Enable
28	EVENT125DETEN	R/W	0h	Event(125) Detection Enable
27	EVENT124DETEN	R/W	0h	Event(124) Detection Enable
26	EVENT123DETEN	R/W	0h	Event(123) Detection Enable
25	EVENT122DETEN	R/W	0h	Event(122) Detection Enable
24	EVENT121DETEN	R/W	0h	Event(121) Detection Enable
23	EVENT120DETEN	R/W	0h	Event(120) Detection Enable
22	EVENT119DETEN	R/W	0h	Event(119) Detection Enable
21	EVENT118DETEN	R/W	0h	Event(118) Detection Enable
20	EVENT117DETEN	R/W	0h	Event(117) Detection Enable
19	EVENT116DETEN	R/W	0h	Event(116) Detection Enable
18	EVENT115DETEN	R/W	0h	Event(115) Detection Enable
17	EVENT114DETEN	R/W	0h	Event(114) Detection Enable
16	EVENT113DETEN	R/W	0h	Event(113) Detection Enable
15	EVENT112DETEN	R/W	0h	Event(112) Detection Enable

Table 14-8024. CTSET2_CFG_SETEVTENBL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT111DETEN	R/W	0h	Event(111) Detection Enable
13	EVENT110DETEN	R/W	0h	Event(110) Detection Enable
12	EVENT109DETEN	R/W	0h	Event(109) Detection Enable
11	EVENT108DETEN	R/W	0h	Event(108) Detection Enable
10	EVENT107DETEN	R/W	0h	Event(107) Detection Enable
9	EVENT106DETEN	R/W	0h	Event(106) Detection Enable
8	EVENT105DETEN	R/W	0h	Event(105) Detection Enable
7	EVENT104DETEN	R/W	0h	Event(104) Detection Enable
6	EVENT103DETEN	R/W	0h	Event(103) Detection Enable
5	EVENT102DETEN	R/W	0h	Event(102) Detection Enable
4	EVENT101DETEN	R/W	0h	Event(101) Detection Enable
3	EVENT100DETEN	R/W	0h	Event(100) Detection Enable
2	EVENT99DETEN	R/W	0h	Event(99) Detection Enable
1	EVENT98DETEN	R/W	0h	Event(98) Detection Enable
0	EVENT97DETEN	R/W	0h	Event(97) Detection Enable

14.3.2.3.2.139 CTSET2_CFG_SETEVTENBL5 Register

14.3.2.3.2.139.1 CTSET2_CFG_SETEVTENBL5 Register (Offset = 40h) [reset = 0h]

System event detection enable register 5 (if number of events > 128)

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Table 14-8025. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8040h

Figure 14-3986. CTSET2_CFG_SETEVTENBL5 Name Register

31	30	29	28	27	26	25	24
EVENT160DETEN	EVENT159DETEN	EVENT158DETEN	EVENT157DETEN	EVENT156DETEN	EVENT155DETEN	EVENT154DETEN	EVENT153DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT152DETEN	EVENT151DETEN	EVENT150DETEN	EVENT149DETEN	EVENT148DETEN	EVENT147DETEN	EVENT1468DETEN	EVENT145DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT144DETEN	EVENT143DETEN	EVENT142DETEN	EVENT141DETEN	EVENT140DETEN	EVENT139DETEN	EVENT138DETEN	EVENT137DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT136DETEN	EVENT135DETEN	EVENT134DETEN	EVENT133DETEN	EVENT132DETEN	EVENT131DETEN	EVENT130DETEN	EVENT129DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8026. CTSET2_CFG_SETEVTENBL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT160DETEN	R/W	0h	Event(160) Detection Enable
30	EVENT159DETEN	R/W	0h	Event(159) Detection Enable
29	EVENT158DETEN	R/W	0h	Event(158) Detection Enable
28	EVENT157DETEN	R/W	0h	Event(157) Detection Enable
27	EVENT156DETEN	R/W	0h	Event(156) Detection Enable
26	EVENT155DETEN	R/W	0h	Event(155) Detection Enable
25	EVENT154DETEN	R/W	0h	Event(154) Detection Enable
24	EVENT153DETEN	R/W	0h	Event(153) Detection Enable
23	EVENT152DETEN	R/W	0h	Event(152) Detection Enable
22	EVENT151DETEN	R/W	0h	Event(151) Detection Enable
21	EVENT150DETEN	R/W	0h	Event(150) Detection Enable
20	EVENT149DETEN	R/W	0h	Event(149) Detection Enable
19	EVENT148DETEN	R/W	0h	Event(148) Detection Enable
18	EVENT147DETEN	R/W	0h	Event(147) Detection Enable
17	EVENT1468DETEN	R/W	0h	Event(146) Detection Enable
16	EVENT145DETEN	R/W	0h	Event(145) Detection Enable
15	EVENT144DETEN	R/W	0h	Event(144) Detection Enable

Table 14-8026. CTSET2_CFG_SETEVTENBL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT143DETEN	R/W	0h	Event(143) Detection Enable
13	EVENT142DETEN	R/W	0h	Event(142) Detection Enable
12	EVENT141DETEN	R/W	0h	Event(141) Detection Enable
11	EVENT140DETEN	R/W	0h	Event(140) Detection Enable
10	EVENT139DETEN	R/W	0h	Event(139) Detection Enable
9	EVENT138DETEN	R/W	0h	Event(138) Detection Enable
8	EVENT137DETEN	R/W	0h	Event(137) Detection Enable
7	EVENT136DETEN	R/W	0h	Event(136) Detection Enable
6	EVENT135DETEN	R/W	0h	Event(135) Detection Enable
5	EVENT134DETEN	R/W	0h	Event(134) Detection Enable
4	EVENT133DETEN	R/W	0h	Event(133) Detection Enable
3	EVENT132DETEN	R/W	0h	Event(132) Detection Enable
2	EVENT131DETEN	R/W	0h	Event(131) Detection Enable
1	EVENT130DETEN	R/W	0h	Event(130) Detection Enable
0	EVENT129DETEN	R/W	0h	Event(129) Detection Enable

14.3.2.3.2.140 CTSET2_CFG_SETEVTENBL6 Register

14.3.2.3.2.140.1 CTSET2_CFG_SETEVTENBL6 Register (Offset = 44h) [reset = 0h]

System event detection enable register 6 (if number of events > 160)

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Table 14-8027. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8044h

Figure 14-3987. CTSET2_CFG_SETEVTENBL6 Name Register

31	30	29	28	27	26	25	24
EVENT192DETEN	EVENT191DETEN	EVENT190DETEN	EVENT189DETEN	EVENT188DETEN	EVENT187DETEN	EVENT186DETEN	EVENT185DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT184DETEN	EVENT183DETEN	EVENT182DETEN	EVENT181DETEN	EVENT180DETEN	EVENT179DETEN	EVENT178DETEN	EVENT177DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT176DETEN	EVENT175DETEN	EVENT174DETEN	EVENT173DETEN	EVENT172DETEN	EVENT171DETEN	EVENT170DETEN	EVENT169DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT168DETEN	EVENT167DETEN	EVENT166DETEN	EVENT165DETEN	EVENT164DETEN	EVENT163DETEN	EVENT162DETEN	EVENT161DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8028. CTSET2_CFG_SETEVTENBL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT192DETEN	R/W	0h	Event(192) Detection Enable
30	EVENT191DETEN	R/W	0h	Event(191) Detection Enable
29	EVENT190DETEN	R/W	0h	Event(190) Detection Enable
28	EVENT189DETEN	R/W	0h	Event(189) Detection Enable
27	EVENT188DETEN	R/W	0h	Event(188) Detection Enable
26	EVENT187DETEN	R/W	0h	Event(187) Detection Enable
25	EVENT186DETEN	R/W	0h	Event(186) Detection Enable
24	EVENT185DETEN	R/W	0h	Event(185) Detection Enable
23	EVENT184DETEN	R/W	0h	Event(184) Detection Enable
22	EVENT183DETEN	R/W	0h	Event(183) Detection Enable
21	EVENT182DETEN	R/W	0h	Event(182) Detection Enable
20	EVENT181DETEN	R/W	0h	Event(181) Detection Enable
19	EVENT180DETEN	R/W	0h	Event(180) Detection Enable
18	EVENT179DETEN	R/W	0h	Event(179) Detection Enable
17	EVENT178DETEN	R/W	0h	Event(178) Detection Enable
16	EVENT177DETEN	R/W	0h	Event(177) Detection Enable
15	EVENT176DETEN	R/W	0h	Event(176) Detection Enable

Table 14-8028. CTSET2_CFG_SETEVTENBL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT175DETEN	R/W	0h	Event(175) Detection Enable
13	EVENT174DETEN	R/W	0h	Event(174) Detection Enable
12	EVENT173DETEN	R/W	0h	Event(173) Detection Enable
11	EVENT172DETEN	R/W	0h	Event(172) Detection Enable
10	EVENT171DETEN	R/W	0h	Event(171) Detection Enable
9	EVENT170DETEN	R/W	0h	Event(170) Detection Enable
8	EVENT169DETEN	R/W	0h	Event(169) Detection Enable
7	EVENT168DETEN	R/W	0h	Event(168) Detection Enable
6	EVENT167DETEN	R/W	0h	Event(167) Detection Enable
5	EVENT166DETEN	R/W	0h	Event(166) Detection Enable
4	EVENT165DETEN	R/W	0h	Event(165) Detection Enable
3	EVENT164DETEN	R/W	0h	Event(164) Detection Enable
2	EVENT163DETEN	R/W	0h	Event(163) Detection Enable
1	EVENT162DETEN	R/W	0h	Event(162) Detection Enable
0	EVENT161DETEN	R/W	0h	Event(161) Detection Enable

14.3.2.3.2.141 CTSET2_CFG_SETEVTENBL7 Register

14.3.2.3.2.141.1 CTSET2_CFG_SETEVTENBL7 Register (Offset = 48h) [reset = 0h]

System event detection enable register 7 (if number of events > 192)

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Table 14-8029. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8048h

Figure 14-3988. CTSET2_CFG_SETEVTENBL7 Name Register

31	30	29	28	27	26	25	24
EVENT224DETEN	EVENT223DETEN	EVENT222DETEN	EVENT221DETEN	EVENT220DETEN	EVENT219DETEN	EVENT218DETEN	EVENT217DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT216DETEN	EVENT215DETEN	EVENT214DETEN	EVENT213DETEN	EVENT212DETEN	EVENT211DETEN	EVENT210DETEN	EVENT209DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT208DETEN	EVENT207DETEN	EVENT206DETEN	EVENT205DETEN	EVENT204DETEN	EVENT203DETEN	EVENT202DETEN	EVENT201DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT200DETEN	EVENT199DETEN	EVENT198DETEN	EVENT197DETEN	EVENT196DETEN	EVENT195DETEN	EVENT194DETEN	EVENT193DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8030. CTSET2_CFG_SETEVTENBL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT224DETEN	R/W	0h	Event(224) Detection Enable
30	EVENT223DETEN	R/W	0h	Event(223) Detection Enable
29	EVENT222DETEN	R/W	0h	Event(222) Detection Enable
28	EVENT221DETEN	R/W	0h	Event(221) Detection Enable
27	EVENT220DETEN	R/W	0h	Event(220) Detection Enable
26	EVENT219DETEN	R/W	0h	Event(219) Detection Enable
25	EVENT218DETEN	R/W	0h	Event(218) Detection Enable
24	EVENT217DETEN	R/W	0h	Event(217) Detection Enable
23	EVENT216DETEN	R/W	0h	Event(216) Detection Enable
22	EVENT215DETEN	R/W	0h	Event(215) Detection Enable
21	EVENT214DETEN	R/W	0h	Event(214) Detection Enable
20	EVENT213DETEN	R/W	0h	Event(213) Detection Enable
19	EVENT212DETEN	R/W	0h	Event(212) Detection Enable
18	EVENT211DETEN	R/W	0h	Event(211) Detection Enable
17	EVENT210DETEN	R/W	0h	Event(210) Detection Enable
16	EVENT209DETEN	R/W	0h	Event(209) Detection Enable
15	EVENT208DETEN	R/W	0h	Event(208) Detection Enable

Table 14-8030. CTSET2_CFG_SETEVTENBL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT207DETEN	R/W	0h	Event(207) Detection Enable
13	EVENT206DETEN	R/W	0h	Event(206) Detection Enable
12	EVENT205DETEN	R/W	0h	Event(205) Detection Enable
11	EVENT204DETEN	R/W	0h	Event(204) Detection Enable
10	EVENT203DETEN	R/W	0h	Event(203) Detection Enable
9	EVENT202DETEN	R/W	0h	Event(202) Detection Enable
8	EVENT201DETEN	R/W	0h	Event(201) Detection Enable
7	EVENT200DETEN	R/W	0h	Event(200) Detection Enable
6	EVENT199DETEN	R/W	0h	Event(199) Detection Enable
5	EVENT198DETEN	R/W	0h	Event(198) Detection Enable
4	EVENT197DETEN	R/W	0h	Event(197) Detection Enable
3	EVENT196DETEN	R/W	0h	Event(196) Detection Enable
2	EVENT195DETEN	R/W	0h	Event(195) Detection Enable
1	EVENT194DETEN	R/W	0h	Event(194) Detection Enable
0	EVENT193DETEN	R/W	0h	Event(193) Detection Enable

14.3.2.3.2.142 CTSET2_CFG_SETEVTENBL8 Register

14.3.2.3.2.142.1 CTSET2_CFG_SETEVTENBL8 Register (Offset = 4Ch) [reset = 0h]

System event detection enable register 8 (if number of events > 224)

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Table 14-8031. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 804Ch

Figure 14-3989. CTSET2_CFG_SETEVTENBL8 Name Register

31	30	29	28	27	26	25	24
EVENT256DETEN	EVENT255DETEN	EVENT254DETEN	EVENT253DETEN	EVENT252DETEN	EVENT251DETEN	EVENT250DETEN	EVENT249DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT248DETEN	EVENT247DETEN	EVENT246DETEN	EVENT245DETEN	EVENT244DETEN	EVENT243DETEN	EVENT242DETEN	EVENT241DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT240DETEN	EVENT239DETEN	EVENT238DETEN	EVENT237DETEN	EVENT236DETEN	EVENT235DETEN	EVENT234DETEN	EVENT233DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT232DETEN	EVENT231DETEN	EVENT230DETEN	EVENT229DETEN	EVENT228DETEN	EVENT227DETEN	EVENT226DETEN	EVENT225DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8032. CTSET2_CFG_SETEVTENBL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT256DETEN	R/W	0h	Event(256) Detection Enable
30	EVENT255DETEN	R/W	0h	Event(255) Detection Enable
29	EVENT254DETEN	R/W	0h	Event(254) Detection Enable
28	EVENT253DETEN	R/W	0h	Event(253) Detection Enable
27	EVENT252DETEN	R/W	0h	Event(252) Detection Enable
26	EVENT251DETEN	R/W	0h	Event(251) Detection Enable
25	EVENT250DETEN	R/W	0h	Event(250) Detection Enable
24	EVENT249DETEN	R/W	0h	Event(249) Detection Enable
23	EVENT248DETEN	R/W	0h	Event(248) Detection Enable
22	EVENT247DETEN	R/W	0h	Event(247) Detection Enable
21	EVENT246DETEN	R/W	0h	Event(246) Detection Enable
20	EVENT245DETEN	R/W	0h	Event(245) Detection Enable
19	EVENT244DETEN	R/W	0h	Event(244) Detection Enable
18	EVENT243DETEN	R/W	0h	Event(243) Detection Enable
17	EVENT242DETEN	R/W	0h	Event(242) Detection Enable
16	EVENT241DETEN	R/W	0h	Event(241) Detection Enable
15	EVENT240DETEN	R/W	0h	Event(240) Detection Enable

Table 14-8032. CTSET2_CFG_SETEVTENBL8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT239DETEN	R/W	0h	Event(239) Detection Enable
13	EVENT238DETEN	R/W	0h	Event(238) Detection Enable
12	EVENT237DETEN	R/W	0h	Event(237) Detection Enable
11	EVENT236DETEN	R/W	0h	Event(236) Detection Enable
10	EVENT235DETEN	R/W	0h	Event(235) Detection Enable
9	EVENT234DETEN	R/W	0h	Event(234) Detection Enable
8	EVENT233DETEN	R/W	0h	Event(233) Detection Enable
7	EVENT232DETEN	R/W	0h	Event(232) Detection Enable
6	EVENT231DETEN	R/W	0h	Event(231) Detection Enable
5	EVENT230DETEN	R/W	0h	Event(230) Detection Enable
4	EVENT229DETEN	R/W	0h	Event(229) Detection Enable
3	EVENT228DETEN	R/W	0h	Event(228) Detection Enable
2	EVENT227DETEN	R/W	0h	Event(227) Detection Enable
1	EVENT226DETEN	R/W	0h	Event(226) Detection Enable
0	EVENT225DETEN	R/W	0h	Event(225) Detection Enable

14.3.2.3.2.143 CTSET2_CFG_SETMSTID Register

14.3.2.3.2.143.1 CTSET2_CFG_SETMSTID Register (Offset = 50h) [reset = 0h]

System Event Initiator ID

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Table 14-8033. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8050h

Figure 14-3990. CTSET2_CFG_SETMSTID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MASTID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8034. CTSET2_CFG_SETMSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	MASTID	R/W	0h	HW Initiator ID for System Event module. Software may overwrite the value at any time, but this is only recommended for scenarios where top-level configuration errors result in a collision between HW initiator IDs

14.3.2.3.2.144 CTSET2_CFG_CTCNTL Register

14.3.2.3.2.144.1 CTSET2_CFG_CTCNTL Register (Offset = 800h) [reset = 0h]

Counter Timer Control

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Table 14-8035. Instance Table

Instance Name	**Physical Address**
C7X256V0_DEBUG	0007 3400 8800h

Figure 14-3991. CTSET2_CFG_CTCNTL Name Register

31	30	29	28	27	26	25	24
NUMSTM						NUMINPT	
R						R	
0h						0h	

23	22	21	20	19	18	17	16
NUMINPT						NUMTIMR	
R						R	
0h						0h	

15	14	13	12	11	10	9	8
NUMTIMR			NUMCNTR				
R			R				
0h			0h				

7	6	5	4	3	2	1	0
NUMCNTR	REVID				RESERVED	RESERVED	NUMCOREMD
R	R				NONE	R	R
0h	0h				0h	0h	0h

Table 14-8036. CTSET2_CFG_CTCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NUMSTM	R	0h	Number of counters that can export via STM
25:18	NUMINPT	R	0h	Number of event input signals
17:13	NUMTIMR	R	0h	Number of timers in the module
12:7	NUMCNTR	R	0h	Number of counters in the module
6:3	REVID	R	0h	Revision ID of CTSET
2	RESERVED	NONE	0h	Reserved
1	RESERVED	R	0h	Reserved, returns 0
0	NUMCOREMD	R	0h	Indicated the number of mode bus interfaces, 0 is 2 CPU buses, 1 is 4 buses

14.3.2.3.2.145 CTSET2_CFG_CTNUMDBG Register

14.3.2.3.2.145.1 CTSET2_CFG_CTNUMDBG Register (Offset = 804h) [reset = 0h]

Counter Timer Number Debug Event Register

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Table 14-8037. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8804h

Figure 14-3992. CTSET2_CFG_CTNUMDBG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	NUMEVT		
R				NONE	R		
0h				0h	0h		

Table 14-8038. CTSET2_CFG_CTNUMDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	NUMEVT	R	0h	Number of input selectors for debug events

14.3.2.3.2.146 CTSET2_CFG_CTUSERACCCTL Register

14.3.2.3.2.146.1 CTSET2_CFG_CTUSERACCCTL Register (Offset = 808h) [reset = 0h]

Counter Timer User Access Control, can only be written in priviledged mode

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Table 14-8039. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8808h

Figure 14-3993. CTSET2_CFG_CTUSERACCCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					SECUSER	RUSER	NRUSER
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-8040. CTSET2_CFG_CTUSERACCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
1	RUSER	R/W	0h	Counter functions while system is in Root-User mode
0	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode

14.3.2.3.2.147 CTSET2_CFG_CTSTMCNTL Register

14.3.2.3.2.147.1 CTSET2_CFG_CTSTMCNTL Register (Offset = 820h) [reset = 0h]

Counter Timer STM Control register

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Table 14-8041. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8820h

Figure 14-3994. CTSET2_CFG_CTSTMCNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				NUMXPORT			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUMXPORT		XPORTACT	CCMPORT	CCMAVAIL	CSMXPORT	SENDOVR	ENBL
R		R	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-8042. CTSET2_CFG_CTSTMCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:6	NUMXPORT	R	0h	The total number of counters designated for export
5	XPORTACT	R	0h	Indicates if a frame is currently being written to the STM.
4	CCMPORT	R/W	0h	SW control of CCM message export
3	CCMAVAIL	R/W	0h	CTSET supports CCM export
2	CSMXPORT	R/W	0h	SW control of CSM message export
1	SENDOVR	R/W	0h	Send overflow data in CSM frame
0	ENBL	R/W	0h	CTSET STM global enable for counter/timer messages

14.3.2.3.2.148 CTSET2_CFG_CTSTMMSTID Register

14.3.2.3.2.148.1 CTSET2_CFG_CTSTMMSTID Register (Offset = 824h) [reset = 0h]

Counter Timer STM Initiator ID register

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Table 14-8043. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8824h

Figure 14-3995. CTSET2_CFG_CTSTMMSTID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
MASTID							
R/W							
0h							

Table 14-8044. CTSET2_CFG_CTSTMMSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	MASTID	R/W	0h	HW Initiator ID for System Event module

14.3.2.3.2.149 CTSET2_CFG_CTSTMINTVL Register

14.3.2.3.2.149.1 CTSET2_CFG_CTSTMINTVL Register (Offset = 828h) [reset = 0h]

Counter Timer STM Interval Register

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Table 14-8045. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8828h

Figure 14-3996. CTSET2_CFG_CTSTMINTVL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">INTERVAL</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8046. CTSET2_CFG_CTSTMINTVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	INTERVAL	R/W	0h	Counter Timer Periodic export interval

14.3.2.3.2.150 CTSET2_CFG_CTSTMSEL0 Register

14.3.2.3.2.150.1 CTSET2_CFG_CTSTMSEL0 Register (Offset = 82Ch) [reset = 0h]

Counter Timer STM Counter Select Register 0. This Selects Counter 0 to 31

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Table 14-8047. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 882Ch

Figure 14-3997. CTSET2_CFG_CTSTMSEL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNTSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNTSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNTSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNTSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8048. CTSET2_CFG_CTSTMSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTSEL	R/W	0h	The individual bit is this field indicate whether the corresponding counter value is included in the CSM message generated via the STM interface

14.3.2.3.2.151 CTSET2_CFG_CTSTMSEL1 Register

14.3.2.3.2.151.1 CTSET2_CFG_CTSTMSEL1 Register (Offset = 830h) [reset = 0h]

Counter Timer STM Counter Select Register 1. This Selects Counter 32 to 63

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Table 14-8049. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8830h

Figure 14-3998. CTSET2_CFG_CTSTMSEL1 Name Register

31	30	29	28	27	26	25	24
COUNTSEL							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEL							
R/W							
0h							

Table 14-8050. CTSET2_CFG_CTSTMSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTSEL	R/W	0h	The individual bit is this field indicate whether the corresponding counter value is included in the CSM message generated via the STM interface

14.3.2.3.2.152 CTSET2_CFG_CTDBGSGL0 Register

14.3.2.3.2.152.1 CTSET2_CFG_CTDBGSGL0 Register (Offset = 8A0h) [reset = 0h]

Timer Interval Register 0. Interval match value for timer 0 in CTSET Timer Interval Register 1. Interval match value for timer 1 in CTSET Timer Interval Register 2. Interval match value for timer 2 in CTSET Timer Interval Register 3. Interval match value for timer 3 in CTSET Timer Interval Register 4. Interval match value for timer 4 in CTSET Timer Interval Register 5. Interval match value for timer 5 in CTSET Timer Interval Register 6. Interval match value for timer 6 in CTSET Timer Interval Register 7. Interval match value for timer 7 in CTSET Timer Interval Register 8. Interval match value for timer 8 in CTSET Timer Interval Register 9. Interval match value for timer 9 in CTSET Timer Interval Register 10. Interval match value for timer 10 in CTSET Timer Interval Register 11. Interval match value for timer 11 in CTSET Timer Interval Register 12. Interval match value for timer 12 in CTSET Timer Interval Register 13. Interval match value for timer 13 in CTSET Timer Interval Register 14. Interval match value for timer 14 in CTSET Timer Interval Register 15. Interval match value for timer 15 in CTSET Counter Timer Debug Event Register 0

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Table 14-8051. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 88A0h

Figure 14-3999. CTSET2_CFG_CTDBGSGL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8052. CTSET2_CFG_CTDBGSGL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.3.2.153 CTSET2_CFG_CTDBGSGL1 Register

14.3.2.3.2.153.1 CTSET2_CFG_CTDBGSGL1 Register (Offset = 8A4h) [reset = 0h]

Counter Timer Debug Event Register 1

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Table 14-8053. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 88A4h

Figure 14-4000. CTSET2_CFG_CTDBGSGL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8054. CTSET2_CFG_CTDBGSGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.3.2.154 CTSET2_CFG_CTDBGSGL2 Register

14.3.2.3.2.154.1 CTSET2_CFG_CTDBGSGL2 Register (Offset = 8A8h) [reset = 0h]

Counter Timer Debug Event Register 2

Return to Summary Table

Table 14-8055. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 88A8h

Figure 14-4001. CTSET2_CFG_CTDBGSGL2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPSEL							
R/W							
0h							

Table 14-8056. CTSET2_CFG_CTDBGSGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.3.2.155 CTSET2_CFG_CTDBGSGL3 Register

14.3.2.3.2.155.1 CTSET2_CFG_CTDBGSGL3 Register (Offset = 8ACh) [reset = 0h]

Counter Timer Debug Event Register 3

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Table 14-8057. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 88ACh

Figure 14-4002. CTSET2_CFG_CTDBGSGL3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8058. CTSET2_CFG_CTDBGSGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.3.2.156 CTSET2_CFG_CTDBGSGL4 Register

14.3.2.3.2.156.1 CTSET2_CFG_CTDBGSGL4 Register (Offset = 8B0h) [reset = 0h]

Counter Timer Debug Event Register 4

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Table 14-8059. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 88B0h

Figure 14-4003. CTSET2_CFG_CTDBGSGL4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8060. CTSET2_CFG_CTDBGSGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.3.2.157 CTSET2_CFG_CTDBGSGL5 Register

14.3.2.3.2.157.1 CTSET2_CFG_CTDBGSGL5 Register (Offset = 8B4h) [reset = 0h]

Counter Timer Debug Event Register5

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Table 14-8061. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 88B4h

Figure 14-4004. CTSET2_CFG_CTDBGSGL5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8062. CTSET2_CFG_CTDBGSGL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.3.2.158 CTSET2_CFG_CTDBGSGL6 Register

14.3.2.3.2.158.1 CTSET2_CFG_CTDBGSGL6 Register (Offset = 8B8h) [reset = 0h]

Counter Timer Debug Event Register 6

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Table 14-8063. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 88B8h

Figure 14-4005. CTSET2_CFG_CTDBGSGL6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8064. CTSET2_CFG_CTDBGSGL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.3.2.159 CTSET2_CFG_CTDBGSGL7 Register

14.3.2.3.2.159.1 CTSET2_CFG_CTDBGSGL7 Register (Offset = 8BCh) [reset = 0h]

Counter Timer Debug Event Register 7

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Table 14-8065. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 88BCh

Figure 14-4006. CTSET2_CFG_CTDBGSGL7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPSEL							
R/W							
0h							

Table 14-8066. CTSET2_CFG_CTDBGSGL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.3.2.160 CTSET2_CFG_CTGNBL0 Register

14.3.2.3.2.160.1 CTSET2_CFG_CTGNBL0 Register (Offset = 9F0h) [reset = 0h]

Counter Timer Global Enable Register 0. This enables Counter 0 to 31

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Table 14-8067. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 89F0h

Figure 14-4007. CTSET2_CFG_CTGNBL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENABLE							
R/W							
0h							

Table 14-8068. CTSET2_CFG_CTGNBL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENABLE	R/W	0h	The individual bit is this field enables the corresponding counter. Bits 30 and 31 will be high if global time stamp output interface is enabled

14.3.2.3.2.161 CTSET2_CFG_CTGNBL1 Register

14.3.2.3.2.161.1 CTSET2_CFG_CTGNBL1 Register (Offset = 9F4h) [reset = 0h]

Counter Timer Global Enable Register 1. This enables Counter 32 to 63

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Table 14-8069. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 89F4h

Figure 14-4008. CTSET2_CFG_CTGNBL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENABLE							
R/W							
0h							

Table 14-8070. CTSET2_CFG_CTGNBL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENABLE	R/W	0h	The individual bit is this field enables the corresponding counter

14.3.2.3.2.162 CTSET2_CFG_CTGRST0 Register

14.3.2.3.2.162.1 CTSET2_CFG_CTGRST0 Register (Offset = 9F8h) [reset = 0h]

Counter Timer Global Reset Register 0. This resets Counter 0 to 31

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Table 14-8071. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 89F8h

Figure 14-4009. CTSET2_CFG_CTGRST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET							
R/W							
0h							

Table 14-8072. CTSET2_CFG_CTGRST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RESET	R/W	0h	The individual bit is this field resets the corresponding counter. These bits are self-clearing, once a '1' is written, after the counters are reset these bits are cleared. When Global Time Stamp output interface is enabled, counter 31 and counter 30 should not be written to any value

14.3.2.3.2.163 CTSET2_CFG_CTGRST1 Register

14.3.2.3.2.163.1 CTSET2_CFG_CTGRST1 Register (Offset = 9FCh) [reset = 0h]

Counter Timer Global Reset Register 0. This resets Counter 32 to 63

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Table 14-8073. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 89FCh

Figure 14-4010. CTSET2_CFG_CTGRST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESET							
R/W							
0h							

Table 14-8074. CTSET2_CFG_CTGRST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RESET	R/W	0h	The individual bit is this field resets the corresponding counter. These bits are self-clearing, once a '1' is written, after the counters are reset these bits are cleared.

14.3.2.3.2.164 CTSET2_CFG_CTCR0 Register

14.3.2.3.2.164.1 CTSET2_CFG_CTCR0 Register (Offset = A00h) [reset = 0h]

Counter Timer Control Register 0

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Table 14-8075. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A00h

Figure 14-4011. CTSET2_CFG_CTCR0 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8076. CTSET2_CFG_CTCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8076. CTSET2_CFG_CTCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.165 CTSET2_CFG_CTCR1 Register

14.3.2.3.2.165.1 CTSET2_CFG_CTCR1 Register (Offset = A04h) [reset = 0h]

Counter Timer Control Register 1

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Table 14-8077. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A04h

Figure 14-4012. CTSET2_CFG_CTCR1 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8078. CTSET2_CFG_CTCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8078. CTSET2_CFG_CTCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.166 CTSET2_CFG_CTCR2 Register

14.3.2.3.2.166.1 CTSET2_CFG_CTCR2 Register (Offset = A08h) [reset = 0h]

Counter Timer Control Register 2

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Table 14-8079. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A08h

Figure 14-4013. CTSET2_CFG_CTCR2 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8080. CTSET2_CFG_CTCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8080. CTSET2_CFG_CTCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.167 CTSET2_CFG_CTCR3 Register

14.3.2.3.2.167.1 CTSET2_CFG_CTCR3 Register (Offset = A0Ch) [reset = 0h]

Counter Timer Control Register 3

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Table 14-8081. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A0Ch

Figure 14-4014. CTSET2_CFG_CTCR3 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8082. CTSET2_CFG_CTCR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8082. CTSET2_CFG_CTCR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.168 CTSET2_CFG_CTCR4 Register

14.3.2.3.2.168.1 CTSET2_CFG_CTCR4 Register (Offset = A10h) [reset = 0h]

Counter Timer Control Register 4

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Table 14-8083. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A10h

Figure 14-4015. CTSET2_CFG_CTCR4 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8084. CTSET2_CFG_CTCR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8084. CTSET2_CFG_CTCR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.169 CTSET2_CFG_CTCR5 Register

14.3.2.3.2.169.1 CTSET2_CFG_CTCR5 Register (Offset = A14h) [reset = 0h]

Counter Timer Control Register 5

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Table 14-8085. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A14h

Figure 14-4016. CTSET2_CFG_CTCR5 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8086. CTSET2_CFG_CTCR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8086. CTSET2_CFG_CTCR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.170 CTSET2_CFG_CTCR6 Register

14.3.2.3.2.170.1 CTSET2_CFG_CTCR6 Register (Offset = A18h) [reset = 0h]

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Table 14-8087. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A18h

Figure 14-4017. CTSET2_CFG_CTCR6 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8088. CTSET2_CFG_CTCR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8088. CTSET2_CFG_CTCR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.171 CTSET2_CFG_CTCR7 Register

14.3.2.3.2.171.1 CTSET2_CFG_CTCR7 Register (Offset = A1Ch) [reset = 0h]

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Table 14-8089. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A1Ch

Figure 14-4018. CTSET2_CFG_CTCR7 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							

23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							

15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8090. CTSET2_CFG_CTCR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8090. CTSET2_CFG_CTCR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.172 CTSET2_CFG_CTCR8 Register

14.3.2.3.2.172.1 CTSET2_CFG_CTCR8 Register (Offset = A20h) [reset = 0h]

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Table 14-8091. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A20h

Figure 14-4019. CTSET2_CFG_CTCR8 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8092. CTSET2_CFG_CTCR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8092. CTSET2_CFG_CTCR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.173 CTSET2_CFG_CTCR9 Register

14.3.2.3.2.173.1 CTSET2_CFG_CTCR9 Register (Offset = A24h) [reset = 0h]

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Table 14-8093. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A24h

Figure 14-4020. CTSET2_CFG_CTCR9 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8094. CTSET2_CFG_CTCR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8094. CTSET2_CFG_CTCR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.174 CTSET2_CFG_CTCR10 Register

14.3.2.3.2.174.1 CTSET2_CFG_CTCR10 Register (Offset = A28h) [reset = 0h]

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Table 14-8095. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A28h

Figure 14-4021. CTSET2_CFG_CTCR10 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8096. CTSET2_CFG_CTCR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8096. CTSET2_CFG_CTCR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.175 CTSET2_CFG_CTCR11 Register

14.3.2.3.2.175.1 CTSET2_CFG_CTCR11 Register (Offset = A2Ch) [reset = 0h]

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Table 14-8097. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A2Ch

Figure 14-4022. CTSET2_CFG_CTCR11 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8098. CTSET2_CFG_CTCR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8098. CTSET2_CFG_CTCR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.176 CTSET2_CFG_CTCR12 Register

14.3.2.3.2.176.1 CTSET2_CFG_CTCR12 Register (Offset = A30h) [reset = 0h]

Counter Timer Control Register 12

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Table 14-8099. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A30h

Figure 14-4023. CTSET2_CFG_CTCR12 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8100. CTSET2_CFG_CTCR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8100. CTSET2_CFG_CTCR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.177 CTSET2_CFG_CTCR13 Register

14.3.2.3.2.177.1 CTSET2_CFG_CTCR13 Register (Offset = A34h) [reset = 0h]

Counter Timer Control Register 13

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Table 14-8101. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A34h

Figure 14-4024. CTSET2_CFG_CTCR13 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8102. CTSET2_CFG_CTCR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8102. CTSET2_CFG_CTCR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.178 CTSET2_CFG_CTCR14 Register

14.3.2.3.2.178.1 CTSET2_CFG_CTCR14 Register (Offset = A38h) [reset = 0h]

Counter Timer Control Register 14

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Table 14-8103. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A38h

Figure 14-4025. CTSET2_CFG_CTCR14 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8104. CTSET2_CFG_CTCR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8104. CTSET2_CFG_CTCR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.179 CTSET2_CFG_CTCR15 Register

14.3.2.3.2.179.1 CTSET2_CFG_CTCR15 Register (Offset = A3Ch) [reset = 0h]

Counter Timer Control Register 15

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Table 14-8105. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A3Ch

Figure 14-4026. CTSET2_CFG_CTCR15 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8106. CTSET2_CFG_CTCR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8106. CTSET2_CFG_CTCR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.180 CTSET2_CFG_CTCR16 Register

14.3.2.3.2.180.1 CTSET2_CFG_CTCR16 Register (Offset = A40h) [reset = 0h]

Counter Timer Control Register 16

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Table 14-8107. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A40h

Figure 14-4027. CTSET2_CFG_CTCR16 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8108. CTSET2_CFG_CTCR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8108. CTSET2_CFG_CTCR16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.181 CTSET2_CFG_CTCR17 Register

14.3.2.3.2.181.1 CTSET2_CFG_CTCR17 Register (Offset = A44h) [reset = 0h]

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Table 14-8109. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A44h

Figure 14-4028. CTSET2_CFG_CTCR17 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8110. CTSET2_CFG_CTCR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8110. CTSET2_CFG_CTCR17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.182 CTSET2_CFG_CTCR18 Register

14.3.2.3.2.182.1 CTSET2_CFG_CTCR18 Register (Offset = A48h) [reset = 0h]

Counter Timer Control Register 18

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Table 14-8111. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A48h

Figure 14-4029. CTSET2_CFG_CTCR18 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8112. CTSET2_CFG_CTCR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8112. CTSET2_CFG_CTCR18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.183 CTSET2_CFG_CTCR19 Register

14.3.2.3.2.183.1 CTSET2_CFG_CTCR19 Register (Offset = A4Ch) [reset = 0h]

Counter Timer Control Register 19

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Table 14-8113. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A4Ch

Figure 14-4030. CTSET2_CFG_CTCR19 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8114. CTSET2_CFG_CTCR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8114. CTSET2_CFG_CTCR19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.184 CTSET2_CFG_CTCR20 Register

14.3.2.3.2.184.1 CTSET2_CFG_CTCR20 Register (Offset = A50h) [reset = 0h]

Counter Timer Control Register 20

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Table 14-8115. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A50h

Figure 14-4031. CTSET2_CFG_CTCR20 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8116. CTSET2_CFG_CTCR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8116. CTSET2_CFG_CTCR20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.185 CTSET2_CFG_CTCR21 Register

14.3.2.3.2.185.1 CTSET2_CFG_CTCR21 Register (Offset = A54h) [reset = 0h]

Counter Timer Control Register 21

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Table 14-8117. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A54h

Figure 14-4032. CTSET2_CFG_CTCR21 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8118. CTSET2_CFG_CTCR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8118. CTSET2_CFG_CTCR21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.186 CTSET2_CFG_CTCR22 Register

14.3.2.3.2.186.1 CTSET2_CFG_CTCR22 Register (Offset = A58h) [reset = 0h]

Counter Timer Control Register 22

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Table 14-8119. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A58h

Figure 14-4033. CTSET2_CFG_CTCR22 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8120. CTSET2_CFG_CTCR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8120. CTSET2_CFG_CTCR22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.187 CTSET2_CFG_CTCR23 Register

14.3.2.3.2.187.1 CTSET2_CFG_CTCR23 Register (Offset = A5Ch) [reset = 0h]

Counter Timer Control Register 23

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Table 14-8121. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A5Ch

Figure 14-4034. CTSET2_CFG_CTCR23 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8122. CTSET2_CFG_CTCR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8122. CTSET2_CFG_CTCR23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.188 CTSET2_CFG_CTCR24 Register

14.3.2.3.2.188.1 CTSET2_CFG_CTCR24 Register (Offset = A60h) [reset = 0h]

Counter Timer Control Register 24

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Table 14-8123. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A60h

Figure 14-4035. CTSET2_CFG_CTCR24 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8124. CTSET2_CFG_CTCR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8124. CTSET2_CFG_CTCR24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.189 CTSET2_CFG_CTCR25 Register

14.3.2.3.2.189.1 CTSET2_CFG_CTCR25 Register (Offset = A64h) [reset = 0h]

Counter Timer Control Register 25

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Table 14-8125. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A64h

Figure 14-4036. CTSET2_CFG_CTCR25 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8126. CTSET2_CFG_CTCR25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8126. CTSET2_CFG_CTCR25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.190 CTSET2_CFG_CTCR26 Register

14.3.2.3.2.190.1 CTSET2_CFG_CTCR26 Register (Offset = A68h) [reset = 0h]

Counter Timer Control Register 26

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Table 14-8127. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A68h

Figure 14-4037. CTSET2_CFG_CTCR26 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8128. CTSET2_CFG_CTCR26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8128. CTSET2_CFG_CTCR26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.191 CTSET2_CFG_CTCR27 Register

14.3.2.3.2.191.1 CTSET2_CFG_CTCR27 Register (Offset = A6Ch) [reset = 0h]

Counter Timer Control Register 27

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Table 14-8129. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A6Ch

Figure 14-4038. CTSET2_CFG_CTCR27 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8130. CTSET2_CFG_CTCR27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8130. CTSET2_CFG_CTCR27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.192 CTSET2_CFG_CTCR28 Register

14.3.2.3.2.192.1 CTSET2_CFG_CTCR28 Register (Offset = A70h) [reset = 0h]

Counter Timer Control Register 28

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Table 14-8131. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A70h

Figure 14-4039. CTSET2_CFG_CTCR28 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8132. CTSET2_CFG_CTCR28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8132. CTSET2_CFG_CTCR28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.193 CTSET2_CFG_CTCR29 Register

14.3.2.3.2.193.1 CTSET2_CFG_CTCR29 Register (Offset = A74h) [reset = 0h]

Counter Timer Control Register 29

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Table 14-8133. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A74h

Figure 14-4040. CTSET2_CFG_CTCR29 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8134. CTSET2_CFG_CTCR29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8134. CTSET2_CFG_CTCR29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.194 CTSET2_CFG_CTCR30 Register

14.3.2.3.2.194.1 CTSET2_CFG_CTCR30 Register (Offset = A78h) [reset = 0h]

Counter Timer Control Register 30

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Table 14-8135. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A78h

Figure 14-4041. CTSET2_CFG_CTCR30 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8136. CTSET2_CFG_CTCR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8136. CTSET2_CFG_CTCR30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.195 CTSET2_CFG_CTCR31 Register

14.3.2.3.2.195.1 CTSET2_CFG_CTCR31 Register (Offset = A7Ch) [reset = 0h]

Counter Timer Control Register 31

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Table 14-8137. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A7Ch

Figure 14-4042. CTSET2_CFG_CTCR31 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8138. CTSET2_CFG_CTCR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8138. CTSET2_CFG_CTCR31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.3.2.196 CTSET2_CFG_CTOWN0 Register

14.3.2.3.2.196.1 CTSET2_CFG_CTOWN0 Register (Offset = A80h) [reset = 20000000h]

Counter/Timer Ownership register 0

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Table 14-8139. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A80h

Figure 14-4043. CTSET2_CFG_CTOWN0 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8140. CTSET2_CFG_CTOWN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.197 CTSET2_CFG_CTOWN1 Register

14.3.2.3.2.197.1 CTSET2_CFG_CTOWN1 Register (Offset = A84h) [reset = 20000000h]

Counter/Timer Ownership register 1

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Table 14-8141. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A84h

Figure 14-4044. CTSET2_CFG_CTOWN1 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8142. CTSET2_CFG_CTOWN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.198 CTSET2_CFG_CTOWN2 Register

14.3.2.3.2.198.1 CTSET2_CFG_CTOWN2 Register (Offset = A88h) [reset = 20000000h]

Counter/Timer Ownership register 2

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Table 14-8143. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A88h

Figure 14-4045. CTSET2_CFG_CTOWN2 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8144. CTSET2_CFG_CTOWN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.199 CTSET2_CFG_CTOWN3 Register

14.3.2.3.2.199.1 CTSET2_CFG_CTOWN3 Register (Offset = A8Ch) [reset = 20000000h]

Counter/Timer Ownership register 3

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Table 14-8145. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A8Ch

Figure 14-4046. CTSET2_CFG_CTOWN3 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8146. CTSET2_CFG_CTOWN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.200 CTSET2_CFG_CTOWN4 Register

14.3.2.3.2.200.1 CTSET2_CFG_CTOWN4 Register (Offset = A90h) [reset = 20000000h]

Counter/Timer Ownership register 4

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Table 14-8147. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A90h

Figure 14-4047. CTSET2_CFG_CTOWN4 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8148. CTSET2_CFG_CTOWN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.201 CTSET2_CFG_CTOWN5 Register

14.3.2.3.2.201.1 CTSET2_CFG_CTOWN5 Register (Offset = A94h) [reset = 20000000h]

Counter/Timer Ownership register 5

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Table 14-8149. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A94h

Figure 14-4048. CTSET2_CFG_CTOWN5 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8150. CTSET2_CFG_CTOWN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.202 CTSET2_CFG_CTOWN6 Register

14.3.2.3.2.202.1 CTSET2_CFG_CTOWN6 Register (Offset = A98h) [reset = 20000000h]

Counter/Timer Ownership register 6

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Table 14-8151. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A98h

Figure 14-4049. CTSET2_CFG_CTOWN6 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8152. CTSET2_CFG_CTOWN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.203 CTSET2_CFG_CTOWN7 Register

14.3.2.3.2.203.1 CTSET2_CFG_CTOWN7 Register (Offset = A9Ch) [reset = 20000000h]

Counter/Timer Ownership register 7

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Table 14-8153. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8A9Ch

Figure 14-4050. CTSET2_CFG_CTOWN7 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8154. CTSET2_CFG_CTOWN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.204 CTSET2_CFG_CTOWN8 Register

14.3.2.3.2.204.1 CTSET2_CFG_CTOWN8 Register (Offset = AA0h) [reset = 20000000h]

Counter/Timer Ownership register 8

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Table 14-8155. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AA0h

Figure 14-4051. CTSET2_CFG_CTOWN8 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8156. CTSET2_CFG_CTOWN8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.205 CTSET2_CFG_CTOWN9 Register

14.3.2.3.2.205.1 CTSET2_CFG_CTOWN9 Register (Offset = AA4h) [reset = 20000000h]

Counter/Timer Ownership register 9

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Table 14-8157. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AA4h

Figure 14-4052. CTSET2_CFG_CTOWN9 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8158. CTSET2_CFG_CTOWN9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.206 CTSET2_CFG_CTOWN10 Register

14.3.2.3.2.206.1 CTSET2_CFG_CTOWN10 Register (Offset = AA8h) [reset = 20000000h]

Counter/Timer Ownership register 10

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Table 14-8159. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AA8h

Figure 14-4053. CTSET2_CFG_CTOWN10 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8160. CTSET2_CFG_CTOWN10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.207 CTSET2_CFG_CTOWN11 Register

14.3.2.3.2.207.1 CTSET2_CFG_CTOWN11 Register (Offset = AACh) [reset = 20000000h]

Counter/Timer Ownership register 11

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Table 14-8161. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AACh

Figure 14-4054. CTSET2_CFG_CTOWN11 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8162. CTSET2_CFG_CTOWN11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.208 CTSET2_CFG_CTOWN12 Register

14.3.2.3.2.208.1 CTSET2_CFG_CTOWN12 Register (Offset = AB0h) [reset = 20000000h]

Counter/Timer Ownership register 12

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Table 14-8163. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AB0h

Figure 14-4055. CTSET2_CFG_CTOWN12 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8164. CTSET2_CFG_CTOWN12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.209 CTSET2_CFG_CTOWN13 Register

14.3.2.3.2.209.1 CTSET2_CFG_CTOWN13 Register (Offset = AB4h) [reset = 20000000h]

Counter/Timer Ownership register 13

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Table 14-8165. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AB4h

Figure 14-4056. CTSET2_CFG_CTOWN13 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8166. CTSET2_CFG_CTOWN13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.210 CTSET2_CFG_CTOWN14 Register

14.3.2.3.2.210.1 CTSET2_CFG_CTOWN14 Register (Offset = AB8h) [reset = 20000000h]

Counter/Timer Ownership register 14

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Table 14-8167. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AB8h

Figure 14-4057. CTSET2_CFG_CTOWN14 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8168. CTSET2_CFG_CTOWN14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.211 CTSET2_CFG_CTOWN15 Register

14.3.2.3.2.211.1 CTSET2_CFG_CTOWN15 Register (Offset = ABCh) [reset = 20000000h]

Counter/Timer Ownership register 15

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Table 14-8169. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8ABCh

Figure 14-4058. CTSET2_CFG_CTOWN15 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8170. CTSET2_CFG_CTOWN15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.212 CTSET2_CFG_CTOWN16 Register

14.3.2.3.2.212.1 CTSET2_CFG_CTOWN16 Register (Offset = AC0h) [reset = 20000000h]

Counter/Timer Ownership register 16

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Table 14-8171. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AC0h

Figure 14-4059. CTSET2_CFG_CTOWN16 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8172. CTSET2_CFG_CTOWN16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.213 CTSET2_CFG_CTOWN17 Register

14.3.2.3.2.213.1 CTSET2_CFG_CTOWN17 Register (Offset = AC4h) [reset = 20000000h]

Counter/Timer Ownership register 17

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Table 14-8173. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AC4h

Figure 14-4060. CTSET2_CFG_CTOWN17 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8174. CTSET2_CFG_CTOWN17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.214 CTSET2_CFG_CTOWN18 Register

14.3.2.3.2.214.1 CTSET2_CFG_CTOWN18 Register (Offset = AC8h) [reset = 20000000h]

Counter/Timer Ownership register 18

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Table 14-8175. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AC8h

Figure 14-4061. CTSET2_CFG_CTOWN18 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8176. CTSET2_CFG_CTOWN18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.215 CTSET2_CFG_CTOWN19 Register

14.3.2.3.2.215.1 CTSET2_CFG_CTOWN19 Register (Offset = ACCh) [reset = 20000000h]

Counter/Timer Ownership register 19

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Table 14-8177. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8ACCh

Figure 14-4062. CTSET2_CFG_CTOWN19 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8178. CTSET2_CFG_CTOWN19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.216 CTSET2_CFG_CTOWN20 Register

14.3.2.3.2.216.1 CTSET2_CFG_CTOWN20 Register (Offset = AD0h) [reset = 20000000h]

Counter/Timer Ownership register 20

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Table 14-8179. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AD0h

Figure 14-4063. CTSET2_CFG_CTOWN20 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8180. CTSET2_CFG_CTOWN20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.217 CTSET2_CFG_CTOWN21 Register

14.3.2.3.2.217.1 CTSET2_CFG_CTOWN21 Register (Offset = AD4h) [reset = 20000000h]

Counter/Timer Ownership register 21

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Table 14-8181. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AD4h

Figure 14-4064. CTSET2_CFG_CTOWN21 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8182. CTSET2_CFG_CTOWN21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.218 CTSET2_CFG_CTOWN22 Register

14.3.2.3.2.218.1 CTSET2_CFG_CTOWN22 Register (Offset = AD8h) [reset = 20000000h]

Counter/Timer Ownership register 22

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Table 14-8183. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AD8h

Figure 14-4065. CTSET2_CFG_CTOWN22 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8184. CTSET2_CFG_CTOWN22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.219 CTSET2_CFG_CTOWN23 Register

14.3.2.3.2.219.1 CTSET2_CFG_CTOWN23 Register (Offset = ADCh) [reset = 20000000h]

Counter/Timer Ownership register23

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Table 14-8185. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8ADCh

Figure 14-4066. CTSET2_CFG_CTOWN23 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8186. CTSET2_CFG_CTOWN23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.220 CTSET2_CFG_CTOWN24 Register

14.3.2.3.2.220.1 CTSET2_CFG_CTOWN24 Register (Offset = AE0h) [reset = 20000000h]

Counter/Timer Ownership register 24

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Table 14-8187. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AE0h

Figure 14-4067. CTSET2_CFG_CTOWN24 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">OWNERSHIP</td><td>DBG_OVERIDE</td><td>CURRENT_OWNER</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td>1h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8188. CTSET2_CFG_CTOWN24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.221 CTSET2_CFG_CTOWN25 Register

14.3.2.3.2.221.1 CTSET2_CFG_CTOWN25 Register (Offset = AE4h) [reset = 20000000h]

Counter/Timer Ownership register 25

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Table 14-8189. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AE4h

Figure 14-4068. CTSET2_CFG_CTOWN25 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8190. CTSET2_CFG_CTOWN25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.222 CTSET2_CFG_CTOWN26 Register

14.3.2.3.2.222.1 CTSET2_CFG_CTOWN26 Register (Offset = AE8h) [reset = 20000000h]

Counter/Timer Ownership register 26

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Table 14-8191. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AE8h

Figure 14-4069. CTSET2_CFG_CTOWN26 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8192. CTSET2_CFG_CTOWN26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.223 CTSET2_CFG_CTOWN27 Register

14.3.2.3.2.223.1 CTSET2_CFG_CTOWN27 Register (Offset = AECh) [reset = 20000000h]

Counter/Timer Ownership register 27

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Table 14-8193. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AECh

Figure 14-4070. CTSET2_CFG_CTOWN27 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8194. CTSET2_CFG_CTOWN27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.224 CTSET2_CFG_CTOWN28 Register

14.3.2.3.2.224.1 CTSET2_CFG_CTOWN28 Register (Offset = AF0h) [reset = 20000000h]

Counter/Timer Ownership register 28

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Table 14-8195. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AF0h

Figure 14-4071. CTSET2_CFG_CTOWN28 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">OWNERSHIP</td><td>DBG_OVERIDE</td><td>CURRENT_OWNER</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td>1h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8196. CTSET2_CFG_CTOWN28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.225 CTSET2_CFG_CTOWN29 Register

14.3.2.3.2.225.1 CTSET2_CFG_CTOWN29 Register (Offset = AF4h) [reset = 20000000h]

Counter/Timer Ownership register 29

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Table 14-8197. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AF4h

Figure 14-4072. CTSET2_CFG_CTOWN29 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8198. CTSET2_CFG_CTOWN29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.226 CTSET2_CFG_CTOWN30 Register

14.3.2.3.2.226.1 CTSET2_CFG_CTOWN30 Register (Offset = AF8h) [reset = 20000000h]

Counter/Timer Ownership register 30

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Table 14-8199. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AF8h

Figure 14-4073. CTSET2_CFG_CTOWN30 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8200. CTSET2_CFG_CTOWN30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.227 CTSET2_CFG_CTOWN31 Register

14.3.2.3.2.227.1 CTSET2_CFG_CTOWN31 Register (Offset = AFCh) [reset = 20000000h]

Counter/Timer Ownership register 31

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Table 14-8201. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8AFCh

Figure 14-4074. CTSET2_CFG_CTOWN31 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8202. CTSET2_CFG_CTOWN31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.228 CTSET2_CFG_CTFILT0 Register

14.3.2.3.2.228.1 CTSET2_CFG_CTFILT0 Register (Offset = B00h) [reset = 0h]

Counter Timer 0 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8203. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B00h

Figure 14-4075. CTSET2_CFG_CTFILT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8204. CTSET2_CFG_CTFILT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.229 CTSET2_CFG_CTFILT1 Register

14.3.2.3.2.229.1 CTSET2_CFG_CTFILT1 Register (Offset = B04h) [reset = 0h]

Counter Timer 1 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8205. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B04h

Figure 14-4076. CTSET2_CFG_CTFILT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8206. CTSET2_CFG_CTFILT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.230 CTSET2_CFG_CTFILT2 Register

14.3.2.3.2.230.1 CTSET2_CFG_CTFILT2 Register (Offset = B08h) [reset = 0h]

Counter Timer 2 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8207. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B08h

Figure 14-4077. CTSET2_CFG_CTFILT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8208. CTSET2_CFG_CTFILT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.231 CTSET2_CFG_CTFILT3 Register

14.3.2.3.2.231.1 CTSET2_CFG_CTFILT3 Register (Offset = B0Ch) [reset = 0h]

Counter Timer 3 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8209. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B0Ch

Figure 14-4078. CTSET2_CFG_CTFILT3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8210. CTSET2_CFG_CTFILT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.232 CTSET2_CFG_CTFILT4 Register

14.3.2.3.2.232.1 CTSET2_CFG_CTFILT4 Register (Offset = B10h) [reset = 0h]

Counter Timer 4 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8211. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B10h

Figure 14-4079. CTSET2_CFG_CTFILT4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8212. CTSET2_CFG_CTFILT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.233 CTSET2_CFG_CTFILT5 Register

14.3.2.3.2.233.1 CTSET2_CFG_CTFILT5 Register (Offset = B14h) [reset = 0h]

Counter Timer 5 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8213. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B14h

Figure 14-4080. CTSET2_CFG_CTFILT5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8214. CTSET2_CFG_CTFILT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.234 CTSET2_CFG_CTFILT6 Register

14.3.2.3.2.234.1 CTSET2_CFG_CTFILT6 Register (Offset = B18h) [reset = 0h]

Counter Timer 6 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8215. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B18h

Figure 14-4081. CTSET2_CFG_CTFILT6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8216. CTSET2_CFG_CTFILT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.235 CTSET2_CFG_CTFILT7 Register

14.3.2.3.2.235.1 CTSET2_CFG_CTFILT7 Register (Offset = B1Ch) [reset = 0h]

Counter Timer 7 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8217. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B1Ch

Figure 14-4082. CTSET2_CFG_CTFILT7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8218. CTSET2_CFG_CTFILT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.236 CTSET2_CFG_CTFILT8 Register

14.3.2.3.2.236.1 CTSET2_CFG_CTFILT8 Register (Offset = B20h) [reset = 0h]

Counter Timer 8 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8219. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B20h

Figure 14-4083. CTSET2_CFG_CTFILT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8220. CTSET2_CFG_CTFILT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.237 CTSET2_CFG_CTFILT9 Register

14.3.2.3.2.237.1 CTSET2_CFG_CTFILT9 Register (Offset = B24h) [reset = 0h]

Counter Timer 9 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8221. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B24h

Figure 14-4084. CTSET2_CFG_CTFILT9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8222. CTSET2_CFG_CTFILT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.238 CTSET2_CFG_CTFILT10 Register

14.3.2.3.2.238.1 CTSET2_CFG_CTFILT10 Register (Offset = B28h) [reset = 0h]

Counter Timer 10 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8223. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B28h

Figure 14-4085. CTSET2_CFG_CTFILT10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8224. CTSET2_CFG_CTFILT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.239 CTSET2_CFG_CTFILT11 Register

14.3.2.3.2.239.1 CTSET2_CFG_CTFILT11 Register (Offset = B2Ch) [reset = 0h]

Counter Timer 11 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8225. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B2Ch

Figure 14-4086. CTSET2_CFG_CTFILT11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8226. CTSET2_CFG_CTFILT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.240 CTSET2_CFG_CTFILT12 Register

14.3.2.3.2.240.1 CTSET2_CFG_CTFILT12 Register (Offset = B30h) [reset = 0h]

Counter Timer 12 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8227. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B30h

Figure 14-4087. CTSET2_CFG_CTFILT12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8228. CTSET2_CFG_CTFILT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.241 CTSET2_CFG_CTFILT13 Register

14.3.2.3.2.241.1 CTSET2_CFG_CTFILT13 Register (Offset = B34h) [reset = 0h]

Counter Timer 13 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8229. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B34h

Figure 14-4088. CTSET2_CFG_CTFILT13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8230. CTSET2_CFG_CTFILT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.242 CTSET2_CFG_CTFILT14 Register

14.3.2.3.2.242.1 CTSET2_CFG_CTFILT14 Register (Offset = B38h) [reset = 0h]

Counter Timer 14 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8231. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B38h

Figure 14-4089. CTSET2_CFG_CTFILT14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8232. CTSET2_CFG_CTFILT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.243 CTSET2_CFG_CTFILT15 Register

14.3.2.3.2.243.1 CTSET2_CFG_CTFILT15 Register (Offset = B3Ch) [reset = 0h]

Counter Timer 15 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8233. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B3Ch

Figure 14-4090. CTSET2_CFG_CTFILT15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8234. CTSET2_CFG_CTFILT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.244 CTSET2_CFG_CTFILT16 Register

14.3.2.3.2.244.1 CTSET2_CFG_CTFILT16 Register (Offset = B40h) [reset = 0h]

Counter Timer 16 Filter Register. These filters are only activated if the CTCRn : FILTER is set

Return to Summary Table

Table 14-8235. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B40h

Figure 14-4091. CTSET2_CFG_CTFILT16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8236. CTSET2_CFG_CTFILT16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.245 CTSET2_CFG_CTFILT17 Register

14.3.2.3.2.245.1 CTSET2_CFG_CTFILT17 Register (Offset = B44h) [reset = 0h]

Counter Timer 17 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8237. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B44h

Figure 14-4092. CTSET2_CFG_CTFILT17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8238. CTSET2_CFG_CTFILT17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.246 CTSET2_CFG_CTFILT18 Register

14.3.2.3.2.246.1 CTSET2_CFG_CTFILT18 Register (Offset = B48h) [reset = 0h]

Counter Timer 18 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8239. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B48h

Figure 14-4093. CTSET2_CFG_CTFILT18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8240. CTSET2_CFG_CTFILT18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.247 CTSET2_CFG_CTFILT19 Register

14.3.2.3.2.247.1 CTSET2_CFG_CTFILT19 Register (Offset = B4Ch) [reset = 0h]

Counter Timer 19 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8241. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B4Ch

Figure 14-4094. CTSET2_CFG_CTFILT19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8242. CTSET2_CFG_CTFILT19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.248 CTSET2_CFG_CTFILT20 Register

14.3.2.3.2.248.1 CTSET2_CFG_CTFILT20 Register (Offset = B50h) [reset = 0h]

Counter Timer 20 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8243. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B50h

Figure 14-4095. CTSET2_CFG_CTFILT20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8244. CTSET2_CFG_CTFILT20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.249 CTSET2_CFG_CTFILT21 Register

14.3.2.3.2.249.1 CTSET2_CFG_CTFILT21 Register (Offset = B54h) [reset = 0h]

Counter Timer 21 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8245. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B54h

Figure 14-4096. CTSET2_CFG_CTFILT21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8246. CTSET2_CFG_CTFILT21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.250 CTSET2_CFG_CTFILT22 Register

14.3.2.3.2.250.1 CTSET2_CFG_CTFILT22 Register (Offset = B58h) [reset = 0h]

Counter Timer 22 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8247. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B58h

Figure 14-4097. CTSET2_CFG_CTFILT22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8248. CTSET2_CFG_CTFILT22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.251 CTSET2_CFG_CTFILT23 Register

14.3.2.3.2.251.1 CTSET2_CFG_CTFILT23 Register (Offset = B5Ch) [reset = 0h]

Counter Timer 23 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8249. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B5Ch

Figure 14-4098. CTSET2_CFG_CTFILT23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8250. CTSET2_CFG_CTFILT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.252 CTSET2_CFG_CTFILT24 Register

14.3.2.3.2.252.1 CTSET2_CFG_CTFILT24 Register (Offset = B60h) [reset = 0h]

Counter Timer 24 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8251. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B60h

Figure 14-4099. CTSET2_CFG_CTFILT24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8252. CTSET2_CFG_CTFILT24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.253 CTSET2_CFG_CTFILT25 Register

14.3.2.3.2.253.1 CTSET2_CFG_CTFILT25 Register (Offset = B64h) [reset = 0h]

Counter Timer 25 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8253. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B64h

Figure 14-4100. CTSET2_CFG_CTFILT25 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SECSUPER</td><td>SECUSER</td><td>RSUPER</td><td>RUSER</td><td>NRSUPER</td><td>NRUSER</td><td>IDLE</td><td>FREE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8254. CTSET2_CFG_CTFILT25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.254 CTSET2_CFG_CTFILT26 Register

14.3.2.3.2.254.1 CTSET2_CFG_CTFILT26 Register (Offset = B68h) [reset = 0h]

Counter Timer 26 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8255. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B68h

Figure 14-4101. CTSET2_CFG_CTFILT26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8256. CTSET2_CFG_CTFILT26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.255 CTSET2_CFG_CTFILT27 Register

14.3.2.3.2.255.1 CTSET2_CFG_CTFILT27 Register (Offset = B6Ch) [reset = 0h]

Counter Timer 27 Filter Register. These filters are only activated if the CTCRn : FILTER is set

Return to Summary Table

Table 14-8257. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B6Ch

Figure 14-4102. CTSET2_CFG_CTFILT27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8258. CTSET2_CFG_CTFILT27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.256 CTSET2_CFG_CTFILT28 Register

14.3.2.3.2.256.1 CTSET2_CFG_CTFILT28 Register (Offset = B70h) [reset = 0h]

Counter Timer 28 Filter Register. These filters are only activated if the CTCRn : FILTER is set

Return to Summary Table

Table 14-8259. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B70h

Figure 14-4103. CTSET2_CFG_CTFILT28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8260. CTSET2_CFG_CTFILT28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.257 CTSET2_CFG_CTFILT29 Register

14.3.2.3.2.257.1 CTSET2_CFG_CTFILT29 Register (Offset = B74h) [reset = 0h]

Counter Timer 29 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8261. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B74h

Figure 14-4104. CTSET2_CFG_CTFILT29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8262. CTSET2_CFG_CTFILT29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.258 CTSET2_CFG_CTFILT30 Register

14.3.2.3.2.258.1 CTSET2_CFG_CTFILT30 Register (Offset = B78h) [reset = 0h]

Counter Timer 30 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8263. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B78h

Figure 14-4105. CTSET2_CFG_CTFILT30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8264. CTSET2_CFG_CTFILT30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.259 CTSET2_CFG_CTFILT31 Register

14.3.2.3.2.259.1 CTSET2_CFG_CTFILT31 Register (Offset = B7Ch) [reset = 0h]

Counter Timer 31 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8265. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B7Ch

Figure 14-4106. CTSET2_CFG_CTFILT31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8266. CTSET2_CFG_CTFILT31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.3.2.260 CTSET2_CFG_CTCNTR0 Register

14.3.2.3.2.260.1 CTSET2_CFG_CTCNTR0 Register (Offset = B80h) [reset = 0h]

Counter Timer Counter Register 0

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Table 14-8267. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B80h

Figure 14-4107. CTSET2_CFG_CTCNTR0 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8268. CTSET2_CFG_CTCNTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.261 CTSET2_CFG_CTCNTR1 Register

14.3.2.3.2.261.1 CTSET2_CFG_CTCNTR1 Register (Offset = B84h) [reset = 0h]

Counter Timer Counter Register 1

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Table 14-8269. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B84h

Figure 14-4108. CTSET2_CFG_CTCNTR1 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8270. CTSET2_CFG_CTCNTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.262 CTSET2_CFG_CTCNTR2 Register

14.3.2.3.2.262.1 CTSET2_CFG_CTCNTR2 Register (Offset = B88h) [reset = 0h]

Counter Timer Counter Register 2

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Table 14-8271. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B88h

Figure 14-4109. CTSET2_CFG_CTCNTR2 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 14-8272. CTSET2_CFG_CTCNTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.263 CTSET2_CFG_CTCNTR3 Register

14.3.2.3.2.263.1 CTSET2_CFG_CTCNTR3 Register (Offset = B8Ch) [reset = 0h]

Counter Timer Counter Register 3

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Table 14-8273. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B8Ch

Figure 14-4110. CTSET2_CFG_CTCNTR3 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8274. CTSET2_CFG_CTCNTR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.264 CTSET2_CFG_CTCNTR4 Register

14.3.2.3.2.264.1 CTSET2_CFG_CTCNTR4 Register (Offset = B90h) [reset = 0h]

Counter Timer Counter Register 4

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Table 14-8275. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B90h

Figure 14-4111. CTSET2_CFG_CTCNTR4 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8276. CTSET2_CFG_CTCNTR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.265 CTSET2_CFG_CTCNTR5 Register

14.3.2.3.2.265.1 CTSET2_CFG_CTCNTR5 Register (Offset = B94h) [reset = 0h]

Counter Timer Counter Register 5

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Table 14-8277. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B94h

Figure 14-4112. CTSET2_CFG_CTCNTR5 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8278. CTSET2_CFG_CTCNTR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.266 CTSET2_CFG_CTCNTR6 Register

14.3.2.3.2.266.1 CTSET2_CFG_CTCNTR6 Register (Offset = B98h) [reset = 0h]

Counter Timer Counter Register 6

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Table 14-8279. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B98h

Figure 14-4113. CTSET2_CFG_CTCNTR6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8280. CTSET2_CFG_CTCNTR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.267 CTSET2_CFG_CTCNTR7 Register

14.3.2.3.2.267.1 CTSET2_CFG_CTCNTR7 Register (Offset = B9Ch) [reset = 0h]

Counter Timer Counter Register 7

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Table 14-8281. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8B9Ch

Figure 14-4114. CTSET2_CFG_CTCNTR7 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8282. CTSET2_CFG_CTCNTR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.268 CTSET2_CFG_CTCNTR8 Register

14.3.2.3.2.268.1 CTSET2_CFG_CTCNTR8 Register (Offset = BA0h) [reset = 0h]

Counter Timer Counter Register 8

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Table 14-8283. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BA0h

Figure 14-4115. CTSET2_CFG_CTCNTR8 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8284. CTSET2_CFG_CTCNTR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.269 CTSET2_CFG_CTCNTR9 Register

14.3.2.3.2.269.1 CTSET2_CFG_CTCNTR9 Register (Offset = BA4h) [reset = 0h]

Counter Timer Counter Register 9

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Table 14-8285. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BA4h

Figure 14-4116. CTSET2_CFG_CTCNTR9 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8286. CTSET2_CFG_CTCNTR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.270 CTSET2_CFG_CTCNTR10 Register

14.3.2.3.2.270.1 CTSET2_CFG_CTCNTR10 Register (Offset = BA8h) [reset = 0h]

Counter Timer Counter Register 10

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Table 14-8287. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BA8h

Figure 14-4117. CTSET2_CFG_CTCNTR10 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8288. CTSET2_CFG_CTCNTR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.271 CTSET2_CFG_CTCNTR11 Register

14.3.2.3.2.271.1 CTSET2_CFG_CTCNTR11 Register (Offset = BACh) [reset = 0h]

Counter Timer Counter Register 11

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Table 14-8289. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BACh

Figure 14-4118. CTSET2_CFG_CTCNTR11 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 14-8290. CTSET2_CFG_CTCNTR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.272 CTSET2_CFG_CTCNTR12 Register

14.3.2.3.2.272.1 CTSET2_CFG_CTCNTR12 Register (Offset = BB0h) [reset = 0h]

Counter Timer Counter Register 12

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Table 14-8291. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BB0h

Figure 14-4119. CTSET2_CFG_CTCNTR12 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8292. CTSET2_CFG_CTCNTR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.273 CTSET2_CFG_CTCNTR13 Register

14.3.2.3.2.273.1 CTSET2_CFG_CTCNTR13 Register (Offset = BB4h) [reset = 0h]

Counter Timer Counter Register 13

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Table 14-8293. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BB4h

Figure 14-4120. CTSET2_CFG_CTCNTR13 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8294. CTSET2_CFG_CTCNTR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.274 CTSET2_CFG_CTCNTR14 Register

14.3.2.3.2.274.1 CTSET2_CFG_CTCNTR14 Register (Offset = BB8h) [reset = 0h]

Counter Timer Counter Register 14

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Table 14-8295. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BB8h

Figure 14-4121. CTSET2_CFG_CTCNTR14 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8296. CTSET2_CFG_CTCNTR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.275 CTSET2_CFG_CTCNTR15 Register

14.3.2.3.2.275.1 CTSET2_CFG_CTCNTR15 Register (Offset = BBCh) [reset = 0h]

Counter Timer Counter Register 15

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Table 14-8297. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BBCh

Figure 14-4122. CTSET2_CFG_CTCNTR15 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 14-8298. CTSET2_CFG_CTCNTR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.276 CTSET2_CFG_CTCNTR16 Register

14.3.2.3.2.276.1 CTSET2_CFG_CTCNTR16 Register (Offset = BC0h) [reset = 0h]

Counter Timer Counter Register 16

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Table 14-8299. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BC0h

Figure 14-4123. CTSET2_CFG_CTCNTR16 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8300. CTSET2_CFG_CTCNTR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.277 CTSET2_CFG_CTCNTR17 Register

14.3.2.3.2.277.1 CTSET2_CFG_CTCNTR17 Register (Offset = BC4h) [reset = 0h]

Counter Timer Counter Register 17

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Table 14-8301. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BC4h

Figure 14-4124. CTSET2_CFG_CTCNTR17 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8302. CTSET2_CFG_CTCNTR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.278 CTSET2_CFG_CTCNTR18 Register

14.3.2.3.2.278.1 CTSET2_CFG_CTCNTR18 Register (Offset = BC8h) [reset = 0h]

Counter Timer Counter Register 18

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Table 14-8303. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BC8h

Figure 14-4125. CTSET2_CFG_CTCNTR18 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8304. CTSET2_CFG_CTCNTR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.279 CTSET2_CFG_CTCNTR19 Register

14.3.2.3.2.279.1 CTSET2_CFG_CTCNTR19 Register (Offset = BCCh) [reset = 0h]

Counter Timer Counter Register 19

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Table 14-8305. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BCCh

Figure 14-4126. CTSET2_CFG_CTCNTR19 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8306. CTSET2_CFG_CTCNTR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.280 CTSET2_CFG_CTCNTR20 Register

14.3.2.3.2.280.1 CTSET2_CFG_CTCNTR20 Register (Offset = BD0h) [reset = 0h]

Counter Timer Counter Register 20

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Table 14-8307. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BD0h

Figure 14-4127. CTSET2_CFG_CTCNTR20 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8308. CTSET2_CFG_CTCNTR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.281 CTSET2_CFG_CTCNTR21 Register

14.3.2.3.2.281.1 CTSET2_CFG_CTCNTR21 Register (Offset = BD4h) [reset = 0h]

Counter Timer Counter Register 21

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Table 14-8309. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BD4h

Figure 14-4128. CTSET2_CFG_CTCNTR21 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8310. CTSET2_CFG_CTCNTR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.282 CTSET2_CFG_CTCNTR22 Register

14.3.2.3.2.282.1 CTSET2_CFG_CTCNTR22 Register (Offset = BD8h) [reset = 0h]

Counter Timer Counter Register 22

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Table 14-8311. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BD8h

Figure 14-4129. CTSET2_CFG_CTCNTR22 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8312. CTSET2_CFG_CTCNTR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.283 CTSET2_CFG_CTCNTR23 Register

14.3.2.3.2.283.1 CTSET2_CFG_CTCNTR23 Register (Offset = BDCh) [reset = 0h]

Counter Timer Counter Register 23

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Table 14-8313. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BDCh

Figure 14-4130. CTSET2_CFG_CTCNTR23 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8314. CTSET2_CFG_CTCNTR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.284 CTSET2_CFG_CTCNTR24 Register

14.3.2.3.2.284.1 CTSET2_CFG_CTCNTR24 Register (Offset = BE0h) [reset = 0h]

Counter Timer Counter Register 24

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Table 14-8315. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BE0h

Figure 14-4131. CTSET2_CFG_CTCNTR24 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8316. CTSET2_CFG_CTCNTR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.285 CTSET2_CFG_CTCNTR25 Register

14.3.2.3.2.285.1 CTSET2_CFG_CTCNTR25 Register (Offset = BE4h) [reset = 0h]

Counter Timer Counter Register 25

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Table 14-8317. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BE4h

Figure 14-4132. CTSET2_CFG_CTCNTR25 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8318. CTSET2_CFG_CTCNTR25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.286 CTSET2_CFG_CTCNTR26 Register

14.3.2.3.2.286.1 CTSET2_CFG_CTCNTR26 Register (Offset = BE8h) [reset = 0h]

Counter Timer Counter Register 26

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Table 14-8319. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BE8h

Figure 14-4133. CTSET2_CFG_CTCNTR26 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8320. CTSET2_CFG_CTCNTR26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.287 CTSET2_CFG_CTCNTR27 Register

14.3.2.3.2.287.1 CTSET2_CFG_CTCNTR27 Register (Offset = BECh) [reset = 0h]

Counter Timer Counter Register 27

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Table 14-8321. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BECh

Figure 14-4134. CTSET2_CFG_CTCNTR27 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8322. CTSET2_CFG_CTCNTR27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.288 CTSET2_CFG_CTCNTR28 Register

14.3.2.3.2.288.1 CTSET2_CFG_CTCNTR28 Register (Offset = BF0h) [reset = 0h]

Counter Timer Counter Register 28

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Table 14-8323. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BF0h

Figure 14-4135. CTSET2_CFG_CTCNTR28 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8324. CTSET2_CFG_CTCNTR28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.289 CTSET2_CFG_CTCNTR29 Register

14.3.2.3.2.289.1 CTSET2_CFG_CTCNTR29 Register (Offset = BF4h) [reset = 0h]

Counter Timer Counter Register 29

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Table 14-8325. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BF4h

Figure 14-4136. CTSET2_CFG_CTCNTR29 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8326. CTSET2_CFG_CTCNTR29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.290 CTSET2_CFG_CTCNTR30 Register

14.3.2.3.2.290.1 CTSET2_CFG_CTCNTR30 Register (Offset = BF8h) [reset = 0h]

Counter Timer Counter Register 30

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Table 14-8327. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BF8h

Figure 14-4137. CTSET2_CFG_CTCNTR30 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8328. CTSET2_CFG_CTCNTR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.291 CTSET2_CFG_CTCNTR31 Register

14.3.2.3.2.291.1 CTSET2_CFG_CTCNTR31 Register (Offset = BFCh) [reset = 0h]

Counter Timer Counter Register 31

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Table 14-8329. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8BFCh

Figure 14-4138. CTSET2_CFG_CTCNTR31 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8330. CTSET2_CFG_CTCNTR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.3.2.292 CTSET2_CFG_CT_EOI Register

14.3.2.3.2.292.1 CTSET2_CFG_CT_EOI Register (Offset = C00h) [reset = 0h]

Counter Timer EOI Register. This register is the End of Interrupt used by SW to signal HW that an interrupt event service is complete and an interrupt can be rearmed. This register exists only if NUMTIMR > 0

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Table 14-8331. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8C00h

Figure 14-4139. CTSET2_CFG_CT_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI
R							R/W
0h							0h

Table 14-8332. CTSET2_CFG_CT_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	EOI	R/W	0h	EOI value

14.3.2.3.2.293 CTSET2_CFG_CTIRQSTAT_RAW Register

14.3.2.3.2.293.1 CTSET2_CFG_CTIRQSTAT_RAW Register (Offset = C04h) [reset = 0h]

Counter Timer IRQSTATUS RAW Register. This register indicates the raw status of the interrupt. It can be written by SW for testing. This register exists only if NUMTIMR > 0

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Table 14-8333. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8C04h

Figure 14-4140. CTSET2_CFG_CTIRQSTAT_RAW Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IRQ							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IRQ							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IRQ							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IRQ							
R/W							
0h							

Table 14-8334. CTSET2_CFG_CTIRQSTAT_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IRQ	R/W	0h	IRQSTATUS_RAW value. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.3.2.3.2.294 CTSET2_CFG_CTIRQSTAT Register

14.3.2.3.2.294.1 CTSET2_CFG_CTIRQSTAT Register (Offset = C08h) [reset = 0h]

Counter Timer IRQSTATUS Register. This bit clears the interrupt event. SW can also read this bit to indicate that the interrupt is active and enabled. This register exists only if NUMTIMR > 0

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Table 14-8335. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8C08h

Figure 14-4141. CTSET2_CFG_CTIRQSTAT Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IE							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IE							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IE							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IE							
R/W							
0h							

Table 14-8336. CTSET2_CFG_CTIRQSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IE	R/W	0h	IRQSTATUS value. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.3.2.3.2.295 CTSET2_CFG_CTIRQENABLE_SET Register

14.3.2.3.2.295.1 CTSET2_CFG_CTIRQENABLE_SET Register (Offset = C0Ch) [reset = 0h]

Counter Timer IRQENABLE_SET Register. This register is to enable generation of Interrupt Event used by SW. This register exists only if NUMTIMR > 0

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Table 14-8337. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8C0Ch

Figure 14-4142. CTSET2_CFG_CTIRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IES							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IES							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IES							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IES							
R/W							
0h							

Table 14-8338. CTSET2_CFG_CTIRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IES	R/W	0h	IRQSET value. This bit sets the enable of the interrupt event. SW can also read this bit to determine if the interrupt is enabled. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.3.2.3.2.296 CTSET2_CFG_CTIRQENABLE_CLR Register

14.3.2.3.2.296.1 CTSET2_CFG_CTIRQENABLE_CLR Register (Offset = C10h) [reset = 0h]

Counter Timer IRQENABLE_CLR Register. This register is to disable generation of Interrupt Event used by SW. This register exists only if NUMTIMR > 0

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Table 14-8339. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 8C10h

Figure 14-4143. CTSET2_CFG_CTIRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IEC							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IEC							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IEC							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IEC							
R/W							
0h							

Table 14-8340. CTSET2_CFG_CTIRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IEC	R/W	0h	IRQCLR value. This bit clears the enable of the interrupt event. SW can also read this bit to determine if the interrupt is enabled. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.3.2.3.2.297 CTSET2_CFG_STPTCR Register

14.3.2.3.2.297.1 CTSET2_CFG_STPTCR Register (Offset = 1800h) [reset = 4h]

STP Trace Control Register

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Table 14-8341. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 9800h

Figure 14-4144. CTSET2_CFG_STPTCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED3</td><td>MOD_FIFOFULL</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>DATA_FIFOFULL</td><td colspan="7">RESERVED2</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED2</td><td>COMPEN</td><td colspan="2">RESERVED1</td><td>SYNCEN</td><td>TSEN</td><td>RESERVED</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="2">R</td><td>R</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="2">0h</td><td>1h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8342. CTSET2_CFG_STPTCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED3	R	0h	Reserved, returns 0
24	MOD_FIFOFULL	R	0h	STPMI2ATB internal MID packet fifo is full
23	DATA_FIFOFULL	R	0h	STPMI2ATB internal Data packet fifo is full
22:6	RESERVED2	R	0h	Reserved, returns 0
5	COMPEN	R/W	0h	Compression of Data enable
4:3	RESERVED1	R	0h	Reserved, returns 0
2	SYNCEN	R	1h	The value 1 indicates STPASYNC is supported
1	TSEN	R/W	0h	Timestamp Enable. This bit is static and should not be changed dynamically. This should be changed before client is enabled.
0	RESERVED	R	0h	Reserved, returns 0

14.3.2.3.2.298 CTSET2_CFG_STPTID Register

14.3.2.3.2.298.1 CTSET2_CFG_STPTID Register (Offset = 1804h) [reset = 0h]

STP Trace ID Register

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Table 14-8343. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 9804h

Figure 14-4145. CTSET2_CFG_STPTID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>RESERVED</td><td colspan="6">TRACEID</td></tr>
<tr><td>R</td><td>NONE</td><td colspan="6">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-8344. CTSET2_CFG_STPTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6	RESERVED	NONE	0h	Reserved
5:0	TRACEID	R/W	0h	Trace ID value. Software may overwrite the value at any time, but this is only recommended for scenarios where top-level configuration errors result in a collision between HW initiator IDs

14.3.2.3.2.299 CTSET2_CFG_STPASYNC Register

14.3.2.3.2.299.1 CTSET2_CFG_STPASYNC Register (Offset = 1810h) [reset = 130Ch]

STP Synchronization Control Register

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Table 14-8345. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 9810h

Figure 14-4146. CTSET2_CFG_STPASYNC Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED			EXPMODE	COUNT			
R			R/W	R/W			
0h			1h	30Ch			
7	6	5	4	3	2	1	0
COUNT							
R/W							
30Ch							

Table 14-8346. CTSET2_CFG_STPASYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	R	0h	Reserved, returns 0
12	EXPMODE	R/W	1h	Exponent mode, A value of 1 sets count to 2 to the Nth, where Nth is ((bits 11 : 8)+12). A value of 0 sets Count to N (bits 11 : 0)
11:0	COUNT	R/W	30Ch	The number of bytes between Synchronization packets

14.3.2.3.2.300 CTSET2_CFG_STPFFCR Register

14.3.2.3.2.300.1 CTSET2_CFG_STPFFCR Register (Offset = 1814h) [reset = 0h]

STP Flush Control Register

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Table 14-8347. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 9814h

Figure 14-4147. CTSET2_CFG_STPFFCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED1</td><td>FORCEFLUSH</td><td colspan="3">RESERVED</td><td>ASYNCPE</td><td>AUTOFLUSH</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="3">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8348. CTSET2_CFG_STPFFCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED1	R	0h	Reserved, returns 0
5	FORCEFLUSH	R/W	0h	Write a 1 to force a flush, automatically clears after the operation is complete
4:2	RESERVED	R	0h	Reserved, returns 0
1	ASYNCPE	R/W	0h	Async Priority Enable. 0 indicates ASYNC packet priority is lower than trace. 1 indicates priority escalates on second synchronization request
0	AUTOFLUSH	R/W	0h	Auto flush enable. When set, on every complete data (ATDATA : WIDTH) in the fifo written, data is exported out when ATREADY is asserted. This should be written before client IP enabled

14.3.2.3.2.301 CTSET2_CFG_STPFEAT1 Register

14.3.2.3.2.301.1 CTSET2_CFG_STPFEAT1 Register (Offset = 1818h) [reset = 21h]

STP Features 1 Register

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Table 14-8349. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3400 9818h

Figure 14-4148. CTSET2_CFG_STPFEAT1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">STP_RTLVER</td><td colspan="3">STP_MAJVER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">STP_CUSTVER</td><td colspan="5">STP_MINVER</td><td>RESERVED</td></tr>
<tr><td colspan="2">R</td><td colspan="5">R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">VERSION</td><td colspan="4">PROT</td></tr>
<tr><td>NONE</td><td colspan="3">R</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td colspan="3">2h</td><td colspan="4">1h</td></tr>
</table>

Table 14-8350. CTSET2_CFG_STPFEAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	STP_RTLVER	R	0h	RTL Version. Reset each time major or minor version is updated
26:24	STP_MAJVER	R	0h	Functional Major Version. This is the first version of STPMI2ATB
23:22	STP_CUSTVER	R	0h	Custom Version (not used)
21:17	STP_MINVER	R	0h	Functional Minor Version
16:8	RESERVED	R	0h	Reserved, returns 0
7	RESERVED	NONE	0h	Reserved
6:4	VERSION	R	2h	STP2.0 Time Stamp, Value of 011 indicates Natural binary timestamp, a value of 100 indicates gray binary timestamps
3:0	PROT	R	1h	Protocol Revision. Value of 0001 indicates STP 2.0

14.3.2.3.2.302 C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_ID Register

14.3.2.3.2.302.1 C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_ID Register (Offset = 0h) [reset = 62810100h]

This is the standard TI peripheral ID register that exists at address 0 in the preipheral space

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Table 14-8351. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0000h
C7X256V1_DEBUG	0007 3804 0000h

Figure 14-4149. C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_ID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		281h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
281h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VER					MAJOR_REV		
R					R		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-8352. C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: cfg_rst_n
29:28	BU	R	2h	Business Unit Reset Source: cfg_rst_n
27:16	FUNCTION	R	281h	function Reset Source: cfg_rst_n
15:11	RTL_VER	R	0h	rtl_ver Reset Source: cfg_rst_n
10:8	MAJOR_REV	R	1h	major_rev Reset Source: cfg_rst_n
7:6	CUSTOM	R	0h	custom Reset Source: cfg_rst_n
5:0	MINOR_REV	R	0h	minor_rev Reset Source: cfg_rst_n

14.3.2.3.2.303 C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_CNTL Register

14.3.2.3.2.303.1 C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_CNTL Register (Offset = 4h) [reset = 0h]

This register contains the controls for serial indrect access and trace processing

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Table 14-8353. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0004h
C7X256V1_DEBUG	0007 3804 0004h

Figure 14-4150. C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_CNTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RSVD1</td><td colspan="2">CONTINUOUS_READ_NUM</td><td>CONTINUOUS_READ_MODE</td></tr>
<tr><td colspan="5">R</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RSVD0</td><td>TRACE_EN</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-8354. C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RSVD1	R	0h	rsvd1 Reset Source: cfg_rst_n
10:9	CONTINUOUS_READ_NUM	R/W	0h	continuous read num Reset Source: cfg_rst_n
8	CONTINUOUS_READ_MODE	R/W	0h	continuous read mode Reset Source: cfg_rst_n
7:1	RSVD0	R	0h	rsvd0 Reset Source: cfg_rst_n
0	TRACE_EN	R/W	0h	trace enable Reset Source: cfg_rst_n

14.3.2.3.2.304 C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_OWN Register

14.3.2.3.2.304.1 C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_OWN Register (Offset = 8h) [reset = 0h]

Module Ownership Control and Status Register

Return to Summary Table

Table 14-8355. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0008h
C7X256V1_DEBUG	0007 3804 0008h

Figure 14-4151. C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_OWN Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD					OWN		CLAIM
R					R		R/W
0h					0h		0h

Table 14-8356. C7X256V_DEBUG_DBG_AGR0_MMR_AGGREGATOR_OWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
2:1	OWN	R	0h	own status bit Reset Source: cfg_rst_n
0	CLAIM	R/W	0h	claim control bit Reset Source: cfg_rst_n

14.3.2.3.2.305 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT0 Register

14.3.2.3.2.305.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT0 Register (Offset = 20h) [reset = 0h]

Designates which port (peripheral) is the target of this port, address, data register group

Return to Summary Table

Table 14-8357. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0020h
C7X256V1_DEBUG	0007 3804 0020h

Figure 14-4152. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RSVD</td><td colspan="5">PORT</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-8358. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
4:0	PORT	R/W	0h	port 0 Reset Source: cfg_rst_n

14.3.2.3.2.306 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR0 Register

14.3.2.3.2.306.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR0 Register (Offset = 24h) [reset = 0h]

Designates the offest (in peripheral space) that is the target of this port, address, data register group

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Table 14-8359. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0024h
C7X256V1_DEBUG	0007 3804 0024h

Figure 14-4153. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR0 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR							
R/W							
0h							

Table 14-8360. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
15:0	ADDR	R/W	0h	The 16-bit address of the target destination in the address space of the targeted peripheral. This is essentially the offset of the target in the peripheral space. Reset Source: cfg_rst_n

14.3.2.3.2.307 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA0 Register

14.3.2.3.2.307.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA0 Register (Offset = 28h) [reset = 0h]

Provides the continuous read data for this port, address, data register group

Return to Summary Table

Table 14-8361. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0028h
C7X256V1_DEBUG	0007 3804 0028h

Figure 14-4154. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA0 Name Register

31	30	29	28	27	26	25	24
DATA							
R							
0h							
23	22	21	20	19	18	17	16
DATA							
R							
0h							
15	14	13	12	11	10	9	8
DATA							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-8362. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R	0h	The read data for the serially accessed register Reset Source: cfg_rst_n

14.3.2.3.2.308 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT1 Register

14.3.2.3.2.308.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT1 Register (Offset = 30h) [reset = 0h]

Designates which port (peripheral) is the target of this port, address, data register group

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Table 14-8363. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0030h
C7X256V1_DEBUG	0007 3804 0030h

Figure 14-4155. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT1 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD			PORT				
R			R/W				
0h			0h				

Table 14-8364. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
4:0	PORT	R/W	0h	port 1 Reset Source: cfg_rst_n

14.3.2.3.2.309 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR1 Register

14.3.2.3.2.309.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR1 Register (Offset = 34h) [reset = 0h]

Designates the offest (in peripheral space) that is the target of this port, address, data register group

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Table 14-8365. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0034h
C7X256V1_DEBUG	0007 3804 0034h

Figure 14-4156. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR1 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR							
R/W							
0h							

Table 14-8366. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
15:0	ADDR	R/W	0h	The 16-bit address of the target destination in the address space of the targeted peripheral. This is essentially the offset of the target in the peripheral space. Reset Source: cfg_rst_n

14.3.2.3.2.310 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA1 Register

14.3.2.3.2.310.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA1 Register (Offset = 38h) [reset = 0h]

Provides the continuous read data for this port, address, data register group

Return to Summary Table

Table 14-8367. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0038h
C7X256V1_DEBUG	0007 3804 0038h

Figure 14-4157. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA1 Name Register

31	30	29	28	27	26	25	24
DATA							
R							
0h							
23	22	21	20	19	18	17	16
DATA							
R							
0h							
15	14	13	12	11	10	9	8
DATA							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-8368. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R	0h	The read data for the serially accessed register Reset Source: cfg_rst_n

14.3.2.3.2.311 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT2 Register

14.3.2.3.2.311.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT2 Register (Offset = 40h) [reset = 0h]

Designates which port (peripheral) is the target of this port, address, data register group

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Table 14-8369. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0040h
C7X256V1_DEBUG	0007 3804 0040h

Figure 14-4158. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT2 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD			PORT				
R			R/W				
0h			0h				

Table 14-8370. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
4:0	PORT	R/W	0h	port 2 Reset Source: cfg_rst_n

14.3.2.3.2.312 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR2 Register

14.3.2.3.2.312.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR2 Register (Offset = 44h) [reset = 0h]

Designates the offest (in peripheral space) that is the target of this port, address, data register group

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Table 14-8371. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0044h
C7X256V1_DEBUG	0007 3804 0044h

Figure 14-4159. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR2 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR							
R/W							
0h							

Table 14-8372. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
15:0	ADDR	R/W	0h	The 16-bit address of the target destination in the address space of the targeted peripheral. This is essentially the offset of the target in the peripheral space. Reset Source: cfg_rst_n

14.3.2.3.2.313 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA2 Register

14.3.2.3.2.313.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA2 Register (Offset = 48h) [reset = 0h]

Provides the continuous read data for this port, address, data register group

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Table 14-8373. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0048h
C7X256V1_DEBUG	0007 3804 0048h

Figure 14-4160. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA2 Name Register

31	30	29	28	27	26	25	24
DATA							
R							
0h							
23	22	21	20	19	18	17	16
DATA							
R							
0h							
15	14	13	12	11	10	9	8
DATA							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-8374. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R	0h	The read data for the serially accessed register Reset Source: cfg_rst_n

14.3.2.3.2.314 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT3 Register

14.3.2.3.2.314.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT3 Register (Offset = 50h) [reset = 0h]

Designates which port (peripheral) is the target of this port, address, data register group

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Table 14-8375. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0050h
C7X256V1_DEBUG	0007 3804 0050h

Figure 14-4161. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD			PORT				
R			R/W				
0h			0h				

Table 14-8376. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_PORT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
4:0	PORT	R/W	0h	port 3 Reset Source: cfg_rst_n

14.3.2.3.2.315 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR3 Register

14.3.2.3.2.315.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR3 Register (Offset = 54h) [reset = 0h]

Designates the offest (in peripheral space) that is the target of this port, address, data register group

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Table 14-8377. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0054h
C7X256V1_DEBUG	0007 3804 0054h

Figure 14-4162. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR3 Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR							
R/W							
0h							

Table 14-8378. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_ADDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSVD	R	0h	rsvd Reset Source: cfg_rst_n
15:0	ADDR	R/W	0h	The 16-bit address of the target destination in the address space of the targeted peripheral. This is essentially the offset of the target in the peripheral space. Reset Source: cfg_rst_n

14.3.2.3.2.316 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA3 Register

14.3.2.3.2.316.1 C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA3 Register (Offset = 58h) [reset = 0h]

Provides the continuous read data for this port, address, data register group

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Table 14-8379. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0058h
C7X256V1_DEBUG	0007 3804 0058h

Figure 14-4163. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA3 Name Register

31	30	29	28	27	26	25	24
DATA							
R							
0h							
23	22	21	20	19	18	17	16
DATA							
R							
0h							
15	14	13	12	11	10	9	8
DATA							
R							
0h							
7	6	5	4	3	2	1	0
DATA							
R							
0h							

Table 14-8380. C7X256V_DEBUG_DBG_AGR0_MMR_CONT_READ_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R	0h	The read data for the serially accessed register Reset Source: cfg_rst_n

14.3.2.3.2.317 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Register

14.3.2.3.2.317.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Register (Offset = 0h) [reset = 4h]

This register contains the control and status settings for STP Trace control register. MID_Fifofull indicates status of internal Initiator/Channel Fifo as full. Data_Fifofull indicates the status of internal Data Fifo as full. It is possible that if MID_Fifofull is full and when new initiator_id is seen on STPMI i/f, the data will not be accepted as MID is full. It will wait for MID to be read out corresponding to Data.

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Table 14-8381. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0100h

Figure 14-4164. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Name Register

31	30	29	28	27	26	25	24
RSVD3							MID_FIFO_FUL
R							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA_FIFO_FULL	RSVD2						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD2		COMPEN	RSVD1		SNCEN	TSEN	RSVD0
R		R/W	R		R	R/W	R
0h		0h	0h		1h	0h	0h

Table 14-8382. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RSVD3	R	0h	reserved
24	MID_FIFO_FUL	R	0h	'1' indicates STPMI2ATB internal MID packet fifo is full
23	DATA_FIFO_FULL	R	0h	'1' indicates STPMI2ATB internal Data packet fifo is full
22:6	RSVD2	R	0h	reserved
5	COMPEN	R/W	0h	Compression Enable: '1' Enables compression of data. '0' disables data compress.
4:3	RSVD1	R	0h	reserved
2	SNCEN	R	1h	ASYNC Enable: 1 indicates STPASYNC is supported. 0 indicates STPASYNC is not supported.
1	TSEN	R/W	0h	Timestamp Enable: 1 enables Timestamp. 0 disables Timestamp (it includes only a nibble TS, when disabled and a time-stamp is indicated on STPMI interface). This bit is static and should not be changed dynamically. This should be changed before client is enabled. The first TS packet sent out after ASYNC export will have either 64/48 (based on TSMAXWIDTH) bit timestamp and followed by only 4 bit Timestamp for TS packets.

Table 14-8382. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RSVD0	R	0h	reserved

14.3.2.3.2.318 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID Register

14.3.2.3.2.318.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID Register (Offset = 4h) [reset = 0h]

This register contains the trace id register settings. This value is sampled from input and is exported on ATB interface as ATID field. This is usually programmed only when top-level configuration errors results in collision between ID's.

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Table 14-8383. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0104h

Figure 14-4165. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD	TRACEID						
R	R/W						
0h	0h						

Table 14-8384. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	reserved
6:0	TRACEID	R/W	0h	Traceid [6:0] value that is forwarded on the ATID interface for all transactions from the Trace Aggreator. The reset value is determined by a tieoff to STPMI2ATB and should be tied to 0000000b internal to the Trace Aggregator. SW must set this to a unique value in the the ATB ID address space to prevent collisions with other ATB sources.

14.3.2.3.2.319 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL Register

14.3.2.3.2.319.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL Register (Offset = 10h) [reset = 1780h]

This register contains the periodic interval after which an ASYNC packet is exported over ATB interface. This counter register controls the interval between synchronization packets. The number of bytes between which a sync packet is sent based on this counter value. Writing a value of 0x0 disables the synchronization counter, however if the client has any other synchronization scheme, that will continue to operate. When this register is written, STPMI2ATB will immediately perform synchronization and reset the counter value to the newly programmed value ensuring subsequent synchronization occurs in the period programmed. This async requests will result in a Initiator switch. A async request will result in async packet followed by VERSION packet which is followed by a new M8/C8 packet before any Dx packet is sent.

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Table 14-8385. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0110h

Figure 14-4166. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD			MODE	COUNT			
R			R/W	R/W			
0h			1h	780h			
7	6	5	4	3	2	1	0
COUNT							
R/W							
780h							

Table 14-8386. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RSVD	R	0h	reserved
12	MODE	R/W	1h	Sync Count Mode: 1 indicates SYNC is 2N bytes N being derived from 11:7, value being between 12 and 27 inclusive 0 indicates N, where N is number of bytes between the ASYNC packets Counter = 2^ N, where [N = 2^m, m=11:7, 12 and 27 inclusive] (mode =1) Counter = N, where [N = 11:0] (mode =0)
11:0	COUNT	R/W	780h	Period Count: Counts the number of bytes between Synchronization packets.

14.3.2.3.2.320 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL Register

14.3.2.3.2.320.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL Register (Offset = 14h) [reset = 1Ch]

This register contains the bits to indicate flush in STPMI2ATB. It also controls priority control for other conditions in STPMI2ATB.

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Table 14-8387. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0114h

Figure 14-4167. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD1		FORCE_FLUSH	RSVD0			ASYNC_PE	AUTO_FLUSH
R		R/W	R			R/W	R/W
0h		0h	7h			0h	0h

Table 14-8388. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RSVD1	R	0h	reserved
5	FORCE_FLUSH	R/W	0h	Forces a flush operation: 1 indicates force a flush, automatically clears after the operation is complete. Refer to 2.10. A '0' is not a valid value to be written at any point of time. It will be ignored. This flush will happen only after any current flush on ATB boundary is completed.
4:2	RSVD0	R	7h	reserved
1	ASYNC_PE	R/W	0h	ASYNC Sequence Priority Enable: 0 indicates ASYNC packet priority is lower than normal trace. 1 indicates priority escalates on second synchronization request
0	AUTO_FLUSH	R/W	0h	Enable ATB Auto-flush: 0 indicates auto flush disabled. 1 indicates auto flush enabled. On every complete data (ATDATA:WIDTH) in the fifo written, data is exported out when ATREADY is asserted. This needs to be written only once before client IP enabled.

14.3.2.3.2.321 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES Register

14.3.2.3.2.321.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES Register (Offset = 18h) [reset = 41h]

This register contains the bits to indicate the features implemented in STPMI2ATB. It shows the VERSION packet implemented based on STP2.0 type of encoding timestamp packet. It also indicates what protocol is followed in the IP.

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Table 14-8389. Instance Table

Instance Name	Physical Address
C7X256V0_DEBUG	0007 3404 0118h

Figure 14-4168. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD	STP_TS_VERSION			PROT			
R	R			R			
0h	4h			1h			

Table 14-8390. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	rsvd
6:4	STP_TS_VERSION	R	4h	Timestamp Version 3 = STP2.0 with Natural binary STP2.0 timestamps. 4 = STP2.0 with Gray STP2.0 timestamps.
3:0	PROT	R	1h	Protocol Version: 0001 indicates STP2.0 protocol

14.3.2.4 C7X256V_DEBUG

C7X256V_DEBUG

14.3.2.4.1 C7X256V_DEBUG Summaries

C7X256V_DEBUG Summaries

Table 14-8391. CTSET2_CFG Registers, Base Address=0007 3800 8000h, Length=8192

Offset	Length	Register Name	C7X256V1_DEBUG Physical Address
0h	32	CTSET2_CFG_CTSETID	0007 3800 8000h
10h	32	CTSET2_CFG_CTSETSYSCFG	0007 3800 8010h
14h	32	CTSET2_CFG_SETSTR	0007 3800 8014h
18h	32	CTSET2_CFG_DBGTIMELOW	0007 3800 8018h
1Ch	32	CTSET2_CFG_DBGTIMEHI	0007 3800 801Ch
24h	32	CTSET2_CFG_CTSETCFG	0007 3800 8024h
28h	32	CTSET2_CFG_SETSPLREG	0007 3800 8028h
30h	32	CTSET2_CFG_SETEVTENBL1	0007 3800 8030h
34h	32	CTSET2_CFG_SETEVTENBL2	0007 3800 8034h
38h	32	CTSET2_CFG_SETEVTENBL3	0007 3800 8038h
3Ch	32	CTSET2_CFG_SETEVTENBL4	0007 3800 803Ch
40h	32	CTSET2_CFG_SETEVTENBL5	0007 3800 8040h
44h	32	CTSET2_CFG_SETEVTENBL6	0007 3800 8044h
48h	32	CTSET2_CFG_SETEVTENBL7	0007 3800 8048h
4Ch	32	CTSET2_CFG_SETEVTENBL8	0007 3800 804Ch
50h	32	CTSET2_CFG_SETMSTID	0007 3800 8050h
800h	32	CTSET2_CFG_CTCNTL	0007 3800 8800h
804h	32	CTSET2_CFG_CTNUMDBG	0007 3800 8804h
808h	32	CTSET2_CFG_CTUSERACCCTL	0007 3800 8808h
820h	32	CTSET2_CFG_CTSTMCNTL	0007 3800 8820h
824h	32	CTSET2_CFG_CTSTMMSTID	0007 3800 8824h
828h	32	CTSET2_CFG_CTSTMINTVL	0007 3800 8828h
82Ch	32	CTSET2_CFG_CTSTMSEL0	0007 3800 882Ch
830h	32	CTSET2_CFG_CTSTMSEL1	0007 3800 8830h
8A0h	32	CTSET2_CFG_CTDBGSGL0	0007 3800 88A0h
8A4h	32	CTSET2_CFG_CTDBGSGL1	0007 3800 88A4h
8A8h	32	CTSET2_CFG_CTDBGSGL2	0007 3800 88A8h
8ACh	32	CTSET2_CFG_CTDBGSGL3	0007 3800 88ACh
8B0h	32	CTSET2_CFG_CTDBGSGL4	0007 3800 88B0h
8B4h	32	CTSET2_CFG_CTDBGSGL5	0007 3800 88B4h
8B8h	32	CTSET2_CFG_CTDBGSGL6	0007 3800 88B8h
8BCh	32	CTSET2_CFG_CTDBGSGL7	0007 3800 88BCh
9F0h	32	CTSET2_CFG_CTGNBL0	0007 3800 89F0h
9F4h	32	CTSET2_CFG_CTGNBL1	0007 3800 89F4h
9F8h	32	CTSET2_CFG_CTGRST0	0007 3800 89F8h
9FCh	32	CTSET2_CFG_CTGRST1	0007 3800 89FCh
A00h	32	CTSET2_CFG_CTCR0	0007 3800 8A00h
A04h	32	CTSET2_CFG_CTCR1	0007 3800 8A04h
A08h	32	CTSET2_CFG_CTCR2	0007 3800 8A08h
A0Ch	32	CTSET2_CFG_CTCR3	0007 3800 8A0Ch

Table 14-8391. CTSET2_CFG Registers, Base Address=0007 3800 8000h, Length=8192 (continued)

Offset	Length	Register Name	C7X256V1_DEBUG Physical Address
A10h	32	CTSET2_CFG_CTCR4	0007 3800 8A10h
A14h	32	CTSET2_CFG_CTCR5	0007 3800 8A14h
A18h	32	CTSET2_CFG_CTCR6	0007 3800 8A18h
A1Ch	32	CTSET2_CFG_CTCR7	0007 3800 8A1Ch
A20h	32	CTSET2_CFG_CTCR8	0007 3800 8A20h
A24h	32	CTSET2_CFG_CTCR9	0007 3800 8A24h
A28h	32	CTSET2_CFG_CTCR10	0007 3800 8A28h
A2Ch	32	CTSET2_CFG_CTCR11	0007 3800 8A2Ch
A30h	32	CTSET2_CFG_CTCR12	0007 3800 8A30h
A34h	32	CTSET2_CFG_CTCR13	0007 3800 8A34h
A38h	32	CTSET2_CFG_CTCR14	0007 3800 8A38h
A3Ch	32	CTSET2_CFG_CTCR15	0007 3800 8A3Ch
A40h	32	CTSET2_CFG_CTCR16	0007 3800 8A40h
A44h	32	CTSET2_CFG_CTCR17	0007 3800 8A44h
A48h	32	CTSET2_CFG_CTCR18	0007 3800 8A48h
A4Ch	32	CTSET2_CFG_CTCR19	0007 3800 8A4Ch
A50h	32	CTSET2_CFG_CTCR20	0007 3800 8A50h
A54h	32	CTSET2_CFG_CTCR21	0007 3800 8A54h
A58h	32	CTSET2_CFG_CTCR22	0007 3800 8A58h
A5Ch	32	CTSET2_CFG_CTCR23	0007 3800 8A5Ch
A60h	32	CTSET2_CFG_CTCR24	0007 3800 8A60h
A64h	32	CTSET2_CFG_CTCR25	0007 3800 8A64h
A68h	32	CTSET2_CFG_CTCR26	0007 3800 8A68h
A6Ch	32	CTSET2_CFG_CTCR27	0007 3800 8A6Ch
A70h	32	CTSET2_CFG_CTCR28	0007 3800 8A70h
A74h	32	CTSET2_CFG_CTCR29	0007 3800 8A74h
A78h	32	CTSET2_CFG_CTCR30	0007 3800 8A78h
A7Ch	32	CTSET2_CFG_CTCR31	0007 3800 8A7Ch
A80h	32	CTSET2_CFG_CTOWN0	0007 3800 8A80h
A84h	32	CTSET2_CFG_CTOWN1	0007 3800 8A84h
A88h	32	CTSET2_CFG_CTOWN2	0007 3800 8A88h
A8Ch	32	CTSET2_CFG_CTOWN3	0007 3800 8A8Ch
A90h	32	CTSET2_CFG_CTOWN4	0007 3800 8A90h
A94h	32	CTSET2_CFG_CTOWN5	0007 3800 8A94h
A98h	32	CTSET2_CFG_CTOWN6	0007 3800 8A98h
A9Ch	32	CTSET2_CFG_CTOWN7	0007 3800 8A9Ch
AA0h	32	CTSET2_CFG_CTOWN8	0007 3800 8AA0h
AA4h	32	CTSET2_CFG_CTOWN9	0007 3800 8AA4h
AA8h	32	CTSET2_CFG_CTOWN10	0007 3800 8AA8h
AACh	32	CTSET2_CFG_CTOWN11	0007 3800 8AACh
AB0h	32	CTSET2_CFG_CTOWN12	0007 3800 8AB0h
AB4h	32	CTSET2_CFG_CTOWN13	0007 3800 8AB4h
AB8h	32	CTSET2_CFG_CTOWN14	0007 3800 8AB8h
ABCh	32	CTSET2_CFG_CTOWN15	0007 3800 8ABCh
AC0h	32	CTSET2_CFG_CTOWN16	0007 3800 8AC0h
AC4h	32	CTSET2_CFG_CTOWN17	0007 3800 8AC4h
AC8h	32	CTSET2_CFG_CTOWN18	0007 3800 8AC8h

Table 14-8391. CTSET2_CFG Registers, Base Address=0007 3800 8000h, Length=8192 (continued)

Offset	Length	Register Name	C7X256V1_DEBUG Physical Address
ACCh	32	CTSET2_CFG_CTOWN19	0007 3800 8ACCh
AD0h	32	CTSET2_CFG_CTOWN20	0007 3800 8AD0h
AD4h	32	CTSET2_CFG_CTOWN21	0007 3800 8AD4h
AD8h	32	CTSET2_CFG_CTOWN22	0007 3800 8AD8h
ADCh	32	CTSET2_CFG_CTOWN23	0007 3800 8ADCh
AE0h	32	CTSET2_CFG_CTOWN24	0007 3800 8AE0h
AE4h	32	CTSET2_CFG_CTOWN25	0007 3800 8AE4h
AE8h	32	CTSET2_CFG_CTOWN26	0007 3800 8AE8h
AECh	32	CTSET2_CFG_CTOWN27	0007 3800 8AECh
AF0h	32	CTSET2_CFG_CTOWN28	0007 3800 8AF0h
AF4h	32	CTSET2_CFG_CTOWN29	0007 3800 8AF4h
AF8h	32	CTSET2_CFG_CTOWN30	0007 3800 8AF8h
AFCh	32	CTSET2_CFG_CTOWN31	0007 3800 8AFCh
B00h	32	CTSET2_CFG_CTFILT0	0007 3800 8B00h
B04h	32	CTSET2_CFG_CTFILT1	0007 3800 8B04h
B08h	32	CTSET2_CFG_CTFILT2	0007 3800 8B08h
B0Ch	32	CTSET2_CFG_CTFILT3	0007 3800 8B0Ch
B10h	32	CTSET2_CFG_CTFILT4	0007 3800 8B10h
B14h	32	CTSET2_CFG_CTFILT5	0007 3800 8B14h
B18h	32	CTSET2_CFG_CTFILT6	0007 3800 8B18h
B1Ch	32	CTSET2_CFG_CTFILT7	0007 3800 8B1Ch
B20h	32	CTSET2_CFG_CTFILT8	0007 3800 8B20h
B24h	32	CTSET2_CFG_CTFILT9	0007 3800 8B24h
B28h	32	CTSET2_CFG_CTFILT10	0007 3800 8B28h
B2Ch	32	CTSET2_CFG_CTFILT11	0007 3800 8B2Ch
B30h	32	CTSET2_CFG_CTFILT12	0007 3800 8B30h
B34h	32	CTSET2_CFG_CTFILT13	0007 3800 8B34h
B38h	32	CTSET2_CFG_CTFILT14	0007 3800 8B38h
B3Ch	32	CTSET2_CFG_CTFILT15	0007 3800 8B3Ch
B40h	32	CTSET2_CFG_CTFILT16	0007 3800 8B40h
B44h	32	CTSET2_CFG_CTFILT17	0007 3800 8B44h
B48h	32	CTSET2_CFG_CTFILT18	0007 3800 8B48h
B4Ch	32	CTSET2_CFG_CTFILT19	0007 3800 8B4Ch
B50h	32	CTSET2_CFG_CTFILT20	0007 3800 8B50h
B54h	32	CTSET2_CFG_CTFILT21	0007 3800 8B54h
B58h	32	CTSET2_CFG_CTFILT22	0007 3800 8B58h
B5Ch	32	CTSET2_CFG_CTFILT23	0007 3800 8B5Ch
B60h	32	CTSET2_CFG_CTFILT24	0007 3800 8B60h
B64h	32	CTSET2_CFG_CTFILT25	0007 3800 8B64h
B68h	32	CTSET2_CFG_CTFILT26	0007 3800 8B68h
B6Ch	32	CTSET2_CFG_CTFILT27	0007 3800 8B6Ch
B70h	32	CTSET2_CFG_CTFILT28	0007 3800 8B70h
B74h	32	CTSET2_CFG_CTFILT29	0007 3800 8B74h
B78h	32	CTSET2_CFG_CTFILT30	0007 3800 8B78h
B7Ch	32	CTSET2_CFG_CTFILT31	0007 3800 8B7Ch
B80h	32	CTSET2_CFG_CTCNTR0	0007 3800 8B80h
B84h	32	CTSET2_CFG_CTCNTR1	0007 3800 8B84h

Table 14-8391. CTSET2_CFG Registers, Base Address=0007 3800 8000h, Length=8192 (continued)

Offset	Length	Register Name	C7X256V1_DEBUG Physical Address
B88h	32	CTSET2_CFG_CTCNTR2	0007 3800 8B88h
B8Ch	32	CTSET2_CFG_CTCNTR3	0007 3800 8B8Ch
B90h	32	CTSET2_CFG_CTCNTR4	0007 3800 8B90h
B94h	32	CTSET2_CFG_CTCNTR5	0007 3800 8B94h
B98h	32	CTSET2_CFG_CTCNTR6	0007 3800 8B98h
B9Ch	32	CTSET2_CFG_CTCNTR7	0007 3800 8B9Ch
BA0h	32	CTSET2_CFG_CTCNTR8	0007 3800 8BA0h
BA4h	32	CTSET2_CFG_CTCNTR9	0007 3800 8BA4h
BA8h	32	CTSET2_CFG_CTCNTR10	0007 3800 8BA8h
BACh	32	CTSET2_CFG_CTCNTR11	0007 3800 8BACh
BB0h	32	CTSET2_CFG_CTCNTR12	0007 3800 8BB0h
BB4h	32	CTSET2_CFG_CTCNTR13	0007 3800 8BB4h
BB8h	32	CTSET2_CFG_CTCNTR14	0007 3800 8BB8h
BBCh	32	CTSET2_CFG_CTCNTR15	0007 3800 8BBCh
BC0h	32	CTSET2_CFG_CTCNTR16	0007 3800 8BC0h
BC4h	32	CTSET2_CFG_CTCNTR17	0007 3800 8BC4h
BC8h	32	CTSET2_CFG_CTCNTR18	0007 3800 8BC8h
BCCh	32	CTSET2_CFG_CTCNTR19	0007 3800 8BCCh
BD0h	32	CTSET2_CFG_CTCNTR20	0007 3800 8BD0h
BD4h	32	CTSET2_CFG_CTCNTR21	0007 3800 8BD4h
BD8h	32	CTSET2_CFG_CTCNTR22	0007 3800 8BD8h
BDCh	32	CTSET2_CFG_CTCNTR23	0007 3800 8BDCh
BE0h	32	CTSET2_CFG_CTCNTR24	0007 3800 8BE0h
BE4h	32	CTSET2_CFG_CTCNTR25	0007 3800 8BE4h
BE8h	32	CTSET2_CFG_CTCNTR26	0007 3800 8BE8h
BECh	32	CTSET2_CFG_CTCNTR27	0007 3800 8BECh
BF0h	32	CTSET2_CFG_CTCNTR28	0007 3800 8BF0h
BF4h	32	CTSET2_CFG_CTCNTR29	0007 3800 8BF4h
BF8h	32	CTSET2_CFG_CTCNTR30	0007 3800 8BF8h
BFCh	32	CTSET2_CFG_CTCNTR31	0007 3800 8BFCh
C00h	32	CTSET2_CFG_CT_EOI	0007 3800 8C00h
C04h	32	CTSET2_CFG_CTIRQSTAT_RAW	0007 3800 8C04h
C08h	32	CTSET2_CFG_CTIRQSTAT	0007 3800 8C08h
C0Ch	32	CTSET2_CFG_CTIRQENABLE_SET	0007 3800 8C0Ch
C10h	32	CTSET2_CFG_CTIRQENABLE_CLR	0007 3800 8C10h
1800h	32	CTSET2_CFG_STPTCR	0007 3800 9800h
1804h	32	CTSET2_CFG_STPTID	0007 3800 9804h
1810h	32	CTSET2_CFG_STPASYNC	0007 3800 9810h
1814h	32	CTSET2_CFG_STPFFCR	0007 3800 9814h
1818h	32	CTSET2_CFG_STPFEAT1	0007 3800 9818h

Table 14-8392. C7X256V_DEBUG_DBG_AGR0_MEM_CFG Registers, Base Address=0007 3804 0100h, Length=256

Offset	Length	Register Name	C7X256V1_DEBUG Physical Address
0h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL	0007 3804 0100h

Table 14-8392. C7X256V_DEBUG_DBG_AGR0_MEM_CFG Registers, Base Address=0007 3804 0100h, Length=256 (continued)

Offset	Length	Register Name	C7X256V1_DEBUG Physical Address
4h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID	0007 3804 0104h
10h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL	0007 3804 0110h
14h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL	0007 3804 0114h
18h	32	C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES	0007 3804 0118h

14.3.2.4.2 C7X256V_DEBUG Registers

C7X256V_DEBUG Registers

14.3.2.4.2.1 CTSET2_CFG_CTSETID Register

14.3.2.4.2.1.1 CTSET2_CFG_CTSETID Register (Offset = 0h) [reset = 62800200h]

CTSET identification register

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Table 14-8393. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8000h

Figure 14-4169. CTSET2_CFG_CTSETID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		280h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
280h							
15	14	13	12	11	10	9	8
RTL_VERSION					MAJOR_REV		
R					R		
0h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-8394. CTSET2_CFG_CTSETID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old Scheme and current
29:28	BU	R	2h	The value 10b designates this as Processor Business Unit IP
27:16	FUNCTION	R	280h	Function : Indicates a Debug IP (0x2nn) and 0x80 is the identifier for CT-SET
15:11	RTL_VERSION	R	0h	This field changes on bug fix, and resets to '0' when either Minor Revision or Major Revision field changes
10:8	MAJOR_REV	R	2h	Major Revision. This field changes when there is a major feature change.
7:6	CUSTOM	R	0h	Indicates a special version for a particular device. 0 if non-custom
5:0	MINOR_REV	R	0h	Minor Revision. This field changes when features are scaled up or down

14.3.2.4.2.2 CTSET2_CFG_CTSETSYSCFG Register

14.3.2.4.2.2.1 CTSET2_CFG_CTSETSYSCFG Register (Offset = 10h) [reset = 8h]

CTSET system configuration register

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Table 14-8395. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8010h

Figure 14-4170. CTSET2_CFG_CTSETSYSCFG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1				IDLEMODE		RESERVED	SOFTRESET
R				R/W		R	R/W
0h				2h		0h	0h

Table 14-8396. CTSET2_CFG_CTSETSYSCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED1	R	0h	Reserved, returns 0
3:2	IDLEMODE	R/W	2h	Sets the Idle Mode for CTSET (0=Force Idle, 1=No Idle, 2=Smart Idle, 3= Smart Idle wakeup)
1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	This will reset entire CTSET, except the registers and the CFG interface. This bit is automatically cleared by hardware. Reads always return 0

14.3.2.4.2.3 CTSET2_CFG_SETSTR Register

14.3.2.4.2.3.1 CTSET2_CFG_SETSTR Register (Offset = 14h) [reset = 101h]

CTSET status register

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Table 14-8397. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8014h

Figure 14-4171. CTSET2_CFG_SETSTR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							HWFIFOEMPTY
R							R
0h							1h
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							1h

Table 14-8398. CTSET2_CFG_SETSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8	HWFIFOEMPTY	R	1h	System Event Trace FIFO status, 1 is empty, 0 means captured data not yet exported
7:1	RESERVED	R	0h	Reserved, returns 0
0	RESETDONE	R	1h	Reset status, 0 means reset ongoing, 1 indicates completed

14.3.2.4.2.4 CTSET2_CFG_DBGTIMELOW Register

14.3.2.4.2.4.1 CTSET2_CFG_DBGTIMELOW Register (Offset = 18h) [reset = 0h]

The 32 low order bits of the debug time value supplied on the time input interface

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Table 14-8399. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8018h

Figure 14-4172. CTSET2_CFG_DBGTIMELOW Name Register

31	30	29	28	27	26	25	24
DBGTIME							
R							
0h							
23	22	21	20	19	18	17	16
DBGTIME							
R							
0h							
15	14	13	12	11	10	9	8
DBGTIME							
R							
0h							
7	6	5	4	3	2	1	0
DBGTIME							
R							
0h							

Table 14-8400. CTSET2_CFG_DBGTIMELOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGTIME	R	0h	debug time

14.3.2.4.2.5 CTSET2_CFG_DBGTIMEHI Register

14.3.2.4.2.5.1 CTSET2_CFG_DBGTIMEHI Register (Offset = 1Ch) [reset = 0h]

The 32 high order bits of the debug time value supplied on the time input interface

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Table 14-8401. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 801Ch

Figure 14-4173. CTSET2_CFG_DBGTIMEHI Name Register

31	30	29	28	27	26	25	24
DBGTIME							
R							
0h							
23	22	21	20	19	18	17	16
DBGTIME							
R							
0h							
15	14	13	12	11	10	9	8
DBGTIME							
R							
0h							
7	6	5	4	3	2	1	0
DBGTIME							
R							
0h							

Table 14-8402. CTSET2_CFG_DBGTIMEHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBGTIME	R	0h	debug time

14.3.2.4.2.6 CTSET2_CFG_CTSETCFG Register

14.3.2.4.2.6.1 CTSET2_CFG_CTSETCFG Register (Offset = 24h) [reset = 20000010h]

The 32 low order bits of the debug time value supplied on the time input interface The 32 high order bits of the debug time value supplied on the time input interface. Reading DBGTIMEHI latches the lower 32 bits of debug time value CTSET configuration register

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Table 14-8403. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8024h

Figure 14-4174. CTSET2_CFG_CTSETCFG Name Register

31	30	29	28	27	26	25	24
CLAIM				RESERVED2			
R/W				R			
2h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYSEVENTCAPTEN	RESERVED1		EVENTLEVEL	MSGMODE	STOPCAPT	STARTCAPT	RESERVED
R/W	R		R/W	R/W	R/W	R/W	R
0h	0h		1h	0h	0h	0h	0h

Table 14-8404. CTSET2_CFG_CTSETCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CLAIM	R/W	2h	Claim control and status. To program any bits other than 31 : 28, CTSET ownership must be claimed using bits 31 : 28.
27:8	RESERVED2	R	0h	Reserved, returns 0
7	SYSEVENTCAPTEN	R/W	0h	When 1 the System event capture is enabled
6:5	RESERVED1	R	0h	Reserved, returns 0
4	EVENTLEVEL	R/W	1h	0 enables low level event detection, 1 enables high level event detection
3	MSGMODE	R/W	0h	Message generated based on event detection, 0 is sampling window, 1 is event detection
2	STOPCAPT	R/W	0h	Stop capturing system events from external trigger detection
1	STARTCAPT	R/W	0h	Start capturing system events from external trigger detection
0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.7 CTSET2_CFG_SETSPLREG Register

14.3.2.4.2.7.1 CTSET2_CFG_SETSPLREG Register (Offset = 28h) [reset = 0h]

System Event Sampling Window register

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Table 14-8405. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8028h

Figure 14-4175. CTSET2_CFG_SETSPLREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WINDOWSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8406. CTSET2_CFG_SETSPLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	WINDOWSIZE	R/W	0h	System events sampling window size expressed as CTSET cycles

14.3.2.4.2.8 CTSET2_CFG_SETEVTENBL1 Register

14.3.2.4.2.8.1 CTSET2_CFG_SETEVTENBL1 Register (Offset = 30h) [reset = 0h]

System event detection enable register 1

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Table 14-8407. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8030h

Figure 14-4176. CTSET2_CFG_SETEVTENBL1 Name Register

31	30	29	28	27	26	25	24
EVENT32DETEN	EVENT31DETEN	EVENT30DETEN	EVENT29DETEN	EVENT28DETEN	EVENT27DETEN	EVENT26DETEN	EVENT25DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT24DETEN	EVENT23DETEN	EVENT22DETEN	EVENT21DETEN	EVENT20DETEN	EVENT19DETEN	EVENT18DETEN	EVENT17DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT16DETEN	EVENT15DETEN	EVENT14DETEN	EVENT13DETEN	EVENT12DETEN	EVENT11DETEN	EVENT10DETEN	EVENT9DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT8DETEN	EVENT7DETEN	EVENT6DETEN	EVENT5DETEN	EVENT4DETEN	EVENT3DETEN	EVENT2DETEN	EVENT1DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8408. CTSET2_CFG_SETEVTENBL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT32DETEN	R/W	0h	Event(32) Detection Enable
30	EVENT31DETEN	R/W	0h	Event(31) Detection Enable
29	EVENT30DETEN	R/W	0h	Event(30) Detection Enable
28	EVENT29DETEN	R/W	0h	Event(29) Detection Enable
27	EVENT28DETEN	R/W	0h	Event(28) Detection Enable
26	EVENT27DETEN	R/W	0h	Event(27) Detection Enable
25	EVENT26DETEN	R/W	0h	Event(26) Detection Enable
24	EVENT25DETEN	R/W	0h	Event(25) Detection Enable
23	EVENT24DETEN	R/W	0h	Event(24) Detection Enable
22	EVENT23DETEN	R/W	0h	Event(23) Detection Enable
21	EVENT22DETEN	R/W	0h	Event(22) Detection Enable
20	EVENT21DETEN	R/W	0h	Event(21) Detection Enable
19	EVENT20DETEN	R/W	0h	Event(20) Detection Enable
18	EVENT19DETEN	R/W	0h	Event(19) Detection Enable
17	EVENT18DETEN	R/W	0h	Event(18) Detection Enable
16	EVENT17DETEN	R/W	0h	Event(17) Detection Enable
15	EVENT16DETEN	R/W	0h	Event(16) Detection Enable

Table 14-8408. CTSET2_CFG_SETEVTENBL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT15DETEN	R/W	0h	Event(15) Detection Enable
13	EVENT14DETEN	R/W	0h	Event(14) Detection Enable
12	EVENT13DETEN	R/W	0h	Event(13) Detection Enable
11	EVENT12DETEN	R/W	0h	Event(12) Detection Enable
10	EVENT11DETEN	R/W	0h	Event(11) Detection Enable
9	EVENT10DETEN	R/W	0h	Event(10) Detection Enable
8	EVENT9DETEN	R/W	0h	Event(9) Detection Enable
7	EVENT8DETEN	R/W	0h	Event(8) Detection Enable
6	EVENT7DETEN	R/W	0h	Event(7) Detection Enable
5	EVENT6DETEN	R/W	0h	Event(6) Detection Enable
4	EVENT5DETEN	R/W	0h	Event(5) Detection Enable
3	EVENT4DETEN	R/W	0h	Event(4) Detection Enable
2	EVENT3DETEN	R/W	0h	Event(3) Detection Enable
1	EVENT2DETEN	R/W	0h	Event(2) Detection Enable
0	EVENT1DETEN	R/W	0h	Event(1) Detection Enable

14.3.2.4.2.9 CTSET2_CFG_SETEVTENBL2 Register

14.3.2.4.2.9.1 CTSET2_CFG_SETEVTENBL2 Register (Offset = 34h) [reset = 0h]

System event detection enable register 2 (if number of events > 32)

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Table 14-8409. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8034h

Figure 14-4177. CTSET2_CFG_SETEVTENBL2 Name Register

31	30	29	28	27	26	25	24
EVENT64DETEN	EVENT63DETEN	EVENT62DETEN	EVENT61DETEN	EVENT60DETEN	EVENT59DETEN	EVENT58DETEN	EVENT57DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT56DETEN	EVENT55DETEN	EVENT54DETEN	EVENT53DETEN	EVENT52DETEN	EVENT51DETEN	EVENT50DETEN	EVENT49DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT48DETEN	EVENT47DETEN	EVENT46DETEN	EVENT45DETEN	EVENT44DETEN	EVENT43DETEN	EVENT42DETEN	EVENT41DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT40DETEN	EVENT39DETEN	EVENT38DETEN	EVENT37DETEN	EVENT36DETEN	EVENT35DETEN	EVENT34DETEN	EVENT33DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8410. CTSET2_CFG_SETEVTENBL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT64DETEN	R/W	0h	Event(64) Detection Enable
30	EVENT63DETEN	R/W	0h	Event(63) Detection Enable
29	EVENT62DETEN	R/W	0h	Event(62) Detection Enable
28	EVENT61DETEN	R/W	0h	Event(61) Detection Enable
27	EVENT60DETEN	R/W	0h	Event(60) Detection Enable
26	EVENT59DETEN	R/W	0h	Event(59) Detection Enable
25	EVENT58DETEN	R/W	0h	Event(58) Detection Enable
24	EVENT57DETEN	R/W	0h	Event(57) Detection Enable
23	EVENT56DETEN	R/W	0h	Event(56) Detection Enable
22	EVENT55DETEN	R/W	0h	Event(55) Detection Enable
21	EVENT54DETEN	R/W	0h	Event(54) Detection Enable
20	EVENT53DETEN	R/W	0h	Event(53) Detection Enable
19	EVENT52DETEN	R/W	0h	Event(52) Detection Enable
18	EVENT51DETEN	R/W	0h	Event(51) Detection Enable
17	EVENT50DETEN	R/W	0h	Event(50) Detection Enable
16	EVENT49DETEN	R/W	0h	Event(49) Detection Enable
15	EVENT48DETEN	R/W	0h	Event(48) Detection Enable

Table 14-8410. CTSET2_CFG_SETEVTENBL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT47DETEN	R/W	0h	Event(47) Detection Enable
13	EVENT46DETEN	R/W	0h	Event(46) Detection Enable
12	EVENT45DETEN	R/W	0h	Event(45) Detection Enable
11	EVENT44DETEN	R/W	0h	Event(44) Detection Enable
10	EVENT43DETEN	R/W	0h	Event(43) Detection Enable
9	EVENT42DETEN	R/W	0h	Event(42) Detection Enable
8	EVENT41DETEN	R/W	0h	Event(41) Detection Enable
7	EVENT40DETEN	R/W	0h	Event(40) Detection Enable
6	EVENT39DETEN	R/W	0h	Event(39) Detection Enable
5	EVENT38DETEN	R/W	0h	Event(38) Detection Enable
4	EVENT37DETEN	R/W	0h	Event(37) Detection Enable
3	EVENT36DETEN	R/W	0h	Event(36) Detection Enable
2	EVENT35DETEN	R/W	0h	Event(35) Detection Enable
1	EVENT34DETEN	R/W	0h	Event(34) Detection Enable
0	EVENT33DETEN	R/W	0h	Event(33) Detection Enable

14.3.2.4.2.10 CTSET2_CFG_SETEVTENBL3 Register

14.3.2.4.2.10.1 CTSET2_CFG_SETEVTENBL3 Register (Offset = 38h) [reset = 0h]

System event detection enable register 3 (if number of events > 64)

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Table 14-8411. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8038h

Figure 14-4178. CTSET2_CFG_SETEVTENBL3 Name Register

31	30	29	28	27	26	25	24
EVENT96DETEN	EVENT95DETEN	EVENT94DETEN	EVENT93DETEN	EVENT92DETEN	EVENT91DETEN	EVENT90DETEN	EVENT89DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT88DETEN	EVENT87DETEN	EVENT86DETEN	EVENT85DETEN	EVENT84DETEN	EVENT83DETEN	EVENT82DETEN	EVENT81DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT80DETEN	EVENT79DETEN	EVENT78DETEN	EVENT77DETEN	EVENT76DETEN	EVENT75DETEN	EVENT74DETEN	EVENT73DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT72DETEN	EVENT71DETEN	EVENT70DETEN	EVENT69DETEN	EVENT68DETEN	EVENT67DETEN	EVENT66DETEN	EVENT65DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8412. CTSET2_CFG_SETEVTENBL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT96DETEN	R/W	0h	Event(96) Detection Enable
30	EVENT95DETEN	R/W	0h	Event(95) Detection Enable
29	EVENT94DETEN	R/W	0h	Event(94) Detection Enable
28	EVENT93DETEN	R/W	0h	Event(93) Detection Enable
27	EVENT92DETEN	R/W	0h	Event(92) Detection Enable
26	EVENT91DETEN	R/W	0h	Event(91) Detection Enable
25	EVENT90DETEN	R/W	0h	Event(90) Detection Enable
24	EVENT89DETEN	R/W	0h	Event(89) Detection Enable
23	EVENT88DETEN	R/W	0h	Event(88) Detection Enable
22	EVENT87DETEN	R/W	0h	Event(87) Detection Enable
21	EVENT86DETEN	R/W	0h	Event(86) Detection Enable
20	EVENT85DETEN	R/W	0h	Event(85) Detection Enable
19	EVENT84DETEN	R/W	0h	Event(84) Detection Enable
18	EVENT83DETEN	R/W	0h	Event(83) Detection Enable
17	EVENT82DETEN	R/W	0h	Event(82) Detection Enable
16	EVENT81DETEN	R/W	0h	Event(81) Detection Enable
15	EVENT80DETEN	R/W	0h	Event(80) Detection Enable

Table 14-8412. CTSET2_CFG_SETEVTENBL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT79DETEN	R/W	0h	Event(79) Detection Enable
13	EVENT78DETEN	R/W	0h	Event(78) Detection Enable
12	EVENT77DETEN	R/W	0h	Event(77) Detection Enable
11	EVENT76DETEN	R/W	0h	Event(76) Detection Enable
10	EVENT75DETEN	R/W	0h	Event(75) Detection Enable
9	EVENT74DETEN	R/W	0h	Event(74) Detection Enable
8	EVENT73DETEN	R/W	0h	Event(73) Detection Enable
7	EVENT72DETEN	R/W	0h	Event(72) Detection Enable
6	EVENT71DETEN	R/W	0h	Event(71) Detection Enable
5	EVENT70DETEN	R/W	0h	Event(70) Detection Enable
4	EVENT69DETEN	R/W	0h	Event(69) Detection Enable
3	EVENT68DETEN	R/W	0h	Event(68) Detection Enable
2	EVENT67DETEN	R/W	0h	Event(67) Detection Enable
1	EVENT66DETEN	R/W	0h	Event(66) Detection Enable
0	EVENT65DETEN	R/W	0h	Event(65) Detection Enable

14.3.2.4.2.11 CTSET2_CFG_SETEVTENBL4 Register

14.3.2.4.2.11.1 CTSET2_CFG_SETEVTENBL4 Register (Offset = 3Ch) [reset = 0h]

System event detection enable register 4 (if number of events > 96)

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Table 14-8413. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 803Ch

Figure 14-4179. CTSET2_CFG_SETEVTENBL4 Name Register

31	30	29	28	27	26	25	24
EVENT128DETEN	EVENT127DETEN	EVENT126DETEN	EVENT125DETEN	EVENT124DETEN	EVENT123DETEN	EVENT122DETEN	EVENT121DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT120DETEN	EVENT119DETEN	EVENT118DETEN	EVENT117DETEN	EVENT116DETEN	EVENT115DETEN	EVENT114DETEN	EVENT113DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT112DETEN	EVENT111DETEN	EVENT110DETEN	EVENT109DETEN	EVENT108DETEN	EVENT107DETEN	EVENT106DETEN	EVENT105DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT104DETEN	EVENT103DETEN	EVENT102DETEN	EVENT101DETEN	EVENT100DETEN	EVENT99DETEN	EVENT98DETEN	EVENT97DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8414. CTSET2_CFG_SETEVTENBL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT128DETEN	R/W	0h	Event(128) Detection Enable
30	EVENT127DETEN	R/W	0h	Event(127) Detection Enable
29	EVENT126DETEN	R/W	0h	Event(126) Detection Enable
28	EVENT125DETEN	R/W	0h	Event(125) Detection Enable
27	EVENT124DETEN	R/W	0h	Event(124) Detection Enable
26	EVENT123DETEN	R/W	0h	Event(123) Detection Enable
25	EVENT122DETEN	R/W	0h	Event(122) Detection Enable
24	EVENT121DETEN	R/W	0h	Event(121) Detection Enable
23	EVENT120DETEN	R/W	0h	Event(120) Detection Enable
22	EVENT119DETEN	R/W	0h	Event(119) Detection Enable
21	EVENT118DETEN	R/W	0h	Event(118) Detection Enable
20	EVENT117DETEN	R/W	0h	Event(117) Detection Enable
19	EVENT116DETEN	R/W	0h	Event(116) Detection Enable
18	EVENT115DETEN	R/W	0h	Event(115) Detection Enable
17	EVENT114DETEN	R/W	0h	Event(114) Detection Enable
16	EVENT113DETEN	R/W	0h	Event(113) Detection Enable
15	EVENT112DETEN	R/W	0h	Event(112) Detection Enable

Table 14-8414. CTSET2_CFG_SETEVTENBL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT111DETEN	R/W	0h	Event(111) Detection Enable
13	EVENT110DETEN	R/W	0h	Event(110) Detection Enable
12	EVENT109DETEN	R/W	0h	Event(109) Detection Enable
11	EVENT108DETEN	R/W	0h	Event(108) Detection Enable
10	EVENT107DETEN	R/W	0h	Event(107) Detection Enable
9	EVENT106DETEN	R/W	0h	Event(106) Detection Enable
8	EVENT105DETEN	R/W	0h	Event(105) Detection Enable
7	EVENT104DETEN	R/W	0h	Event(104) Detection Enable
6	EVENT103DETEN	R/W	0h	Event(103) Detection Enable
5	EVENT102DETEN	R/W	0h	Event(102) Detection Enable
4	EVENT101DETEN	R/W	0h	Event(101) Detection Enable
3	EVENT100DETEN	R/W	0h	Event(100) Detection Enable
2	EVENT99DETEN	R/W	0h	Event(99) Detection Enable
1	EVENT98DETEN	R/W	0h	Event(98) Detection Enable
0	EVENT97DETEN	R/W	0h	Event(97) Detection Enable

14.3.2.4.2.12 CTSET2_CFG_SETEVTENBL5 Register

14.3.2.4.2.12.1 CTSET2_CFG_SETEVTENBL5 Register (Offset = 40h) [reset = 0h]

System event detection enable register 5 (if number of events > 128)

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Table 14-8415. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8040h

Figure 14-4180. CTSET2_CFG_SETEVTENBL5 Name Register

31	30	29	28	27	26	25	24
EVENT160DETEN	EVENT159DETEN	EVENT158DETEN	EVENT157DETEN	EVENT156DETEN	EVENT155DETEN	EVENT154DETEN	EVENT153DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT152DETEN	EVENT151DETEN	EVENT150DETEN	EVENT149DETEN	EVENT148DETEN	EVENT147DETEN	EVENT1468DETEN	EVENT145DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT144DETEN	EVENT143DETEN	EVENT142DETEN	EVENT141DETEN	EVENT140DETEN	EVENT139DETEN	EVENT138DETEN	EVENT137DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT136DETEN	EVENT135DETEN	EVENT134DETEN	EVENT133DETEN	EVENT132DETEN	EVENT131DETEN	EVENT130DETEN	EVENT129DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8416. CTSET2_CFG_SETEVTENBL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT160DETEN	R/W	0h	Event(160) Detection Enable
30	EVENT159DETEN	R/W	0h	Event(159) Detection Enable
29	EVENT158DETEN	R/W	0h	Event(158) Detection Enable
28	EVENT157DETEN	R/W	0h	Event(157) Detection Enable
27	EVENT156DETEN	R/W	0h	Event(156) Detection Enable
26	EVENT155DETEN	R/W	0h	Event(155) Detection Enable
25	EVENT154DETEN	R/W	0h	Event(154) Detection Enable
24	EVENT153DETEN	R/W	0h	Event(153) Detection Enable
23	EVENT152DETEN	R/W	0h	Event(152) Detection Enable
22	EVENT151DETEN	R/W	0h	Event(151) Detection Enable
21	EVENT150DETEN	R/W	0h	Event(150) Detection Enable
20	EVENT149DETEN	R/W	0h	Event(149) Detection Enable
19	EVENT148DETEN	R/W	0h	Event(148) Detection Enable
18	EVENT147DETEN	R/W	0h	Event(147) Detection Enable
17	EVENT1468DETEN	R/W	0h	Event(146) Detection Enable
16	EVENT145DETEN	R/W	0h	Event(145) Detection Enable
15	EVENT144DETEN	R/W	0h	Event(144) Detection Enable

Table 14-8416. CTSET2_CFG_SETEVTENBL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT143DETEN	R/W	0h	Event(143) Detection Enable
13	EVENT142DETEN	R/W	0h	Event(142) Detection Enable
12	EVENT141DETEN	R/W	0h	Event(141) Detection Enable
11	EVENT140DETEN	R/W	0h	Event(140) Detection Enable
10	EVENT139DETEN	R/W	0h	Event(139) Detection Enable
9	EVENT138DETEN	R/W	0h	Event(138) Detection Enable
8	EVENT137DETEN	R/W	0h	Event(137) Detection Enable
7	EVENT136DETEN	R/W	0h	Event(136) Detection Enable
6	EVENT135DETEN	R/W	0h	Event(135) Detection Enable
5	EVENT134DETEN	R/W	0h	Event(134) Detection Enable
4	EVENT133DETEN	R/W	0h	Event(133) Detection Enable
3	EVENT132DETEN	R/W	0h	Event(132) Detection Enable
2	EVENT131DETEN	R/W	0h	Event(131) Detection Enable
1	EVENT130DETEN	R/W	0h	Event(130) Detection Enable
0	EVENT129DETEN	R/W	0h	Event(129) Detection Enable

14.3.2.4.2.13 CTSET2_CFG_SETEVTENBL6 Register

14.3.2.4.2.13.1 CTSET2_CFG_SETEVTENBL6 Register (Offset = 44h) [reset = 0h]

System event detection enable register 6 (if number of events > 160)

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Table 14-8417. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8044h

Figure 14-4181. CTSET2_CFG_SETEVTENBL6 Name Register

31	30	29	28	27	26	25	24
EVENT192DETEN	EVENT191DETEN	EVENT190DETEN	EVENT189DETEN	EVENT188DETEN	EVENT187DETEN	EVENT186DETEN	EVENT185DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT184DETEN	EVENT183DETEN	EVENT182DETEN	EVENT181DETEN	EVENT180DETEN	EVENT179DETEN	EVENT178DETEN	EVENT177DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT176DETEN	EVENT175DETEN	EVENT174DETEN	EVENT173DETEN	EVENT172DETEN	EVENT171DETEN	EVENT170DETEN	EVENT169DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT168DETEN	EVENT167DETEN	EVENT166DETEN	EVENT165DETEN	EVENT164DETEN	EVENT163DETEN	EVENT162DETEN	EVENT161DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8418. CTSET2_CFG_SETEVTENBL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT192DETEN	R/W	0h	Event(192) Detection Enable
30	EVENT191DETEN	R/W	0h	Event(191) Detection Enable
29	EVENT190DETEN	R/W	0h	Event(190) Detection Enable
28	EVENT189DETEN	R/W	0h	Event(189) Detection Enable
27	EVENT188DETEN	R/W	0h	Event(188) Detection Enable
26	EVENT187DETEN	R/W	0h	Event(187) Detection Enable
25	EVENT186DETEN	R/W	0h	Event(186) Detection Enable
24	EVENT185DETEN	R/W	0h	Event(185) Detection Enable
23	EVENT184DETEN	R/W	0h	Event(184) Detection Enable
22	EVENT183DETEN	R/W	0h	Event(183) Detection Enable
21	EVENT182DETEN	R/W	0h	Event(182) Detection Enable
20	EVENT181DETEN	R/W	0h	Event(181) Detection Enable
19	EVENT180DETEN	R/W	0h	Event(180) Detection Enable
18	EVENT179DETEN	R/W	0h	Event(179) Detection Enable
17	EVENT178DETEN	R/W	0h	Event(178) Detection Enable
16	EVENT177DETEN	R/W	0h	Event(177) Detection Enable
15	EVENT176DETEN	R/W	0h	Event(176) Detection Enable

Table 14-8418. CTSET2_CFG_SETEVTENBL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT175DETEN	R/W	0h	Event(175) Detection Enable
13	EVENT174DETEN	R/W	0h	Event(174) Detection Enable
12	EVENT173DETEN	R/W	0h	Event(173) Detection Enable
11	EVENT172DETEN	R/W	0h	Event(172) Detection Enable
10	EVENT171DETEN	R/W	0h	Event(171) Detection Enable
9	EVENT170DETEN	R/W	0h	Event(170) Detection Enable
8	EVENT169DETEN	R/W	0h	Event(169) Detection Enable
7	EVENT168DETEN	R/W	0h	Event(168) Detection Enable
6	EVENT167DETEN	R/W	0h	Event(167) Detection Enable
5	EVENT166DETEN	R/W	0h	Event(166) Detection Enable
4	EVENT165DETEN	R/W	0h	Event(165) Detection Enable
3	EVENT164DETEN	R/W	0h	Event(164) Detection Enable
2	EVENT163DETEN	R/W	0h	Event(163) Detection Enable
1	EVENT162DETEN	R/W	0h	Event(162) Detection Enable
0	EVENT161DETEN	R/W	0h	Event(161) Detection Enable

14.3.2.4.2.14 CTSET2_CFG_SETEVTENBL7 Register

14.3.2.4.2.14.1 CTSET2_CFG_SETEVTENBL7 Register (Offset = 48h) [reset = 0h]

System event detection enable register 7 (if number of events > 192)

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Table 14-8419. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8048h

Figure 14-4182. CTSET2_CFG_SETEVTENBL7 Name Register

31	30	29	28	27	26	25	24
EVENT224DETEN	EVENT223DETEN	EVENT222DETEN	EVENT221DETEN	EVENT220DETEN	EVENT219DETEN	EVENT218DETEN	EVENT217DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT216DETEN	EVENT215DETEN	EVENT214DETEN	EVENT213DETEN	EVENT212DETEN	EVENT211DETEN	EVENT210DETEN	EVENT209DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT208DETEN	EVENT207DETEN	EVENT206DETEN	EVENT205DETEN	EVENT204DETEN	EVENT203DETEN	EVENT202DETEN	EVENT201DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT200DETEN	EVENT199DETEN	EVENT198DETEN	EVENT197DETEN	EVENT196DETEN	EVENT195DETEN	EVENT194DETEN	EVENT193DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8420. CTSET2_CFG_SETEVTENBL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT224DETEN	R/W	0h	Event(224) Detection Enable
30	EVENT223DETEN	R/W	0h	Event(223) Detection Enable
29	EVENT222DETEN	R/W	0h	Event(222) Detection Enable
28	EVENT221DETEN	R/W	0h	Event(221) Detection Enable
27	EVENT220DETEN	R/W	0h	Event(220) Detection Enable
26	EVENT219DETEN	R/W	0h	Event(219) Detection Enable
25	EVENT218DETEN	R/W	0h	Event(218) Detection Enable
24	EVENT217DETEN	R/W	0h	Event(217) Detection Enable
23	EVENT216DETEN	R/W	0h	Event(216) Detection Enable
22	EVENT215DETEN	R/W	0h	Event(215) Detection Enable
21	EVENT214DETEN	R/W	0h	Event(214) Detection Enable
20	EVENT213DETEN	R/W	0h	Event(213) Detection Enable
19	EVENT212DETEN	R/W	0h	Event(212) Detection Enable
18	EVENT211DETEN	R/W	0h	Event(211) Detection Enable
17	EVENT210DETEN	R/W	0h	Event(210) Detection Enable
16	EVENT209DETEN	R/W	0h	Event(209) Detection Enable
15	EVENT208DETEN	R/W	0h	Event(208) Detection Enable

Table 14-8420. CTSET2_CFG_SETEVTENBL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT207DETEN	R/W	0h	Event(207) Detection Enable
13	EVENT206DETEN	R/W	0h	Event(206) Detection Enable
12	EVENT205DETEN	R/W	0h	Event(205) Detection Enable
11	EVENT204DETEN	R/W	0h	Event(204) Detection Enable
10	EVENT203DETEN	R/W	0h	Event(203) Detection Enable
9	EVENT202DETEN	R/W	0h	Event(202) Detection Enable
8	EVENT201DETEN	R/W	0h	Event(201) Detection Enable
7	EVENT200DETEN	R/W	0h	Event(200) Detection Enable
6	EVENT199DETEN	R/W	0h	Event(199) Detection Enable
5	EVENT198DETEN	R/W	0h	Event(198) Detection Enable
4	EVENT197DETEN	R/W	0h	Event(197) Detection Enable
3	EVENT196DETEN	R/W	0h	Event(196) Detection Enable
2	EVENT195DETEN	R/W	0h	Event(195) Detection Enable
1	EVENT194DETEN	R/W	0h	Event(194) Detection Enable
0	EVENT193DETEN	R/W	0h	Event(193) Detection Enable

14.3.2.4.2.15 CTSET2_CFG_SETEVTENBL8 Register

14.3.2.4.2.15.1 CTSET2_CFG_SETEVTENBL8 Register (Offset = 4Ch) [reset = 0h]

System event detection enable register 8 (if number of events > 224)

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Table 14-8421. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 804Ch

Figure 14-4183. CTSET2_CFG_SETEVTENBL8 Name Register

31	30	29	28	27	26	25	24
EVENT256DETEN	EVENT255DETEN	EVENT254DETEN	EVENT253DETEN	EVENT252DETEN	EVENT251DETEN	EVENT250DETEN	EVENT249DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EVENT248DETEN	EVENT247DETEN	EVENT246DETEN	EVENT245DETEN	EVENT244DETEN	EVENT243DETEN	EVENT242DETEN	EVENT241DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
EVENT240DETEN	EVENT239DETEN	EVENT238DETEN	EVENT237DETEN	EVENT236DETEN	EVENT235DETEN	EVENT234DETEN	EVENT233DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
EVENT232DETEN	EVENT231DETEN	EVENT230DETEN	EVENT229DETEN	EVENT228DETEN	EVENT227DETEN	EVENT226DETEN	EVENT225DETEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8422. CTSET2_CFG_SETEVTENBL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVENT256DETEN	R/W	0h	Event(256) Detection Enable
30	EVENT255DETEN	R/W	0h	Event(255) Detection Enable
29	EVENT254DETEN	R/W	0h	Event(254) Detection Enable
28	EVENT253DETEN	R/W	0h	Event(253) Detection Enable
27	EVENT252DETEN	R/W	0h	Event(252) Detection Enable
26	EVENT251DETEN	R/W	0h	Event(251) Detection Enable
25	EVENT250DETEN	R/W	0h	Event(250) Detection Enable
24	EVENT249DETEN	R/W	0h	Event(249) Detection Enable
23	EVENT248DETEN	R/W	0h	Event(248) Detection Enable
22	EVENT247DETEN	R/W	0h	Event(247) Detection Enable
21	EVENT246DETEN	R/W	0h	Event(246) Detection Enable
20	EVENT245DETEN	R/W	0h	Event(245) Detection Enable
19	EVENT244DETEN	R/W	0h	Event(244) Detection Enable
18	EVENT243DETEN	R/W	0h	Event(243) Detection Enable
17	EVENT242DETEN	R/W	0h	Event(242) Detection Enable
16	EVENT241DETEN	R/W	0h	Event(241) Detection Enable
15	EVENT240DETEN	R/W	0h	Event(240) Detection Enable

Table 14-8422. CTSET2_CFG_SETEVTENBL8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	EVENT239DETEN	R/W	0h	Event(239) Detection Enable
13	EVENT238DETEN	R/W	0h	Event(238) Detection Enable
12	EVENT237DETEN	R/W	0h	Event(237) Detection Enable
11	EVENT236DETEN	R/W	0h	Event(236) Detection Enable
10	EVENT235DETEN	R/W	0h	Event(235) Detection Enable
9	EVENT234DETEN	R/W	0h	Event(234) Detection Enable
8	EVENT233DETEN	R/W	0h	Event(233) Detection Enable
7	EVENT232DETEN	R/W	0h	Event(232) Detection Enable
6	EVENT231DETEN	R/W	0h	Event(231) Detection Enable
5	EVENT230DETEN	R/W	0h	Event(230) Detection Enable
4	EVENT229DETEN	R/W	0h	Event(229) Detection Enable
3	EVENT228DETEN	R/W	0h	Event(228) Detection Enable
2	EVENT227DETEN	R/W	0h	Event(227) Detection Enable
1	EVENT226DETEN	R/W	0h	Event(226) Detection Enable
0	EVENT225DETEN	R/W	0h	Event(225) Detection Enable

14.3.2.4.2.16 CTSET2_CFG_SETMSTID Register

14.3.2.4.2.16.1 CTSET2_CFG_SETMSTID Register (Offset = 50h) [reset = 0h]

System Event Master ID

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Table 14-8423. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8050h

Figure 14-4184. CTSET2_CFG_SETMSTID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
MASTID							
R/W							
0h							

Table 14-8424. CTSET2_CFG_SETMSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	MASTID	R/W	0h	HW Master ID for System Event module. Software may overwrite the value at any time, but this is only recommended for scenarios where top-level configuration errors result in a collision between HW master IDs

14.3.2.4.2.17 CTSET2_CFG_CTCNTL Register

14.3.2.4.2.17.1 CTSET2_CFG_CTCNTL Register (Offset = 800h) [reset = 0h]

Counter Timer Control

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Table 14-8425. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8800h

Figure 14-4185. CTSET2_CFG_CTCNTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">NUMSTM</td><td colspan="2">NUMINPT</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">NUMINPT</td><td colspan="2">NUMTIMR</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">NUMTIMR</td><td colspan="5">NUMCNTR</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NUMCNTR</td><td colspan="4">REVID</td><td>RESERVED</td><td>RESERVED</td><td>NUMCOREMD</td></tr>
<tr><td>R</td><td colspan="4">R</td><td>NONE</td><td>R</td><td>R</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8426. CTSET2_CFG_CTCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NUMSTM	R	0h	Number of counters that can export via STM
25:18	NUMINPT	R	0h	Number of event input signals
17:13	NUMTIMR	R	0h	Number of timers in the module
12:7	NUMCNTR	R	0h	Number of counters in the module
6:3	REVID	R	0h	Revision ID of CTSET
2	RESERVED	NONE	0h	Reserved
1	RESERVED	R	0h	Reserved, returns 0
0	NUMCOREMD	R	0h	Indicated the number of mode bus interfaces, 0 is 2 CPU buses, 1 is 4 buses

14.3.2.4.2.18 CTSET2_CFG_CTNUMDBG Register

14.3.2.4.2.18.1 CTSET2_CFG_CTNUMDBG Register (Offset = 804h) [reset = 0h]

Counter Timer Number Debug Event Register

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Table 14-8427. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8804h

Figure 14-4186. CTSET2_CFG_CTNUMDBG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>RESERVED</td><td colspan="3">NUMEVT</td></tr>
<tr><td colspan="4">R</td><td>NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-8428. CTSET2_CFG_CTNUMDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	NUMEVT	R	0h	Number of input selectors for debug events

14.3.2.4.2.19 CTSET2_CFG_CTUSERACCCTL Register

14.3.2.4.2.19.1 CTSET2_CFG_CTUSERACCCTL Register (Offset = 808h) [reset = 0h]

Counter Timer User Access Control, can only be written in priviledged mode

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Table 14-8429. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8808h

Figure 14-4187. CTSET2_CFG_CTUSERACCCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					SECUSER	RUSER	NRUSER
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-8430. CTSET2_CFG_CTUSERACCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
1	RUSER	R/W	0h	Counter functions while system is in Root-User mode
0	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode

14.3.2.4.2.20 CTSET2_CFG_CTSTMCNTL Register

14.3.2.4.2.20.1 CTSET2_CFG_CTSTMCNTL Register (Offset = 820h) [reset = 0h]

Counter Timer STM Control register

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Table 14-8431. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8820h

Figure 14-4188. CTSET2_CFG_CTSTMCNTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUMXPORT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">NUMXPORT</td><td>XPORTACT</td><td>CCMPORT</td><td>CCMAVAIL</td><td>CSMXPORT</td><td>SENDOVR</td><td>ENBL</td></tr>
<tr><td colspan="2">R</td><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8432. CTSET2_CFG_CTSTMCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:6	NUMXPORT	R	0h	The total number of counters designated for export
5	XPORTACT	R	0h	Indicates if a frame is currently being written to the STM.
4	CCMPORT	R/W	0h	SW control of CCM message export
3	CCMAVAIL	R/W	0h	CTSET supports CCM export
2	CSMXPORT	R/W	0h	SW control of CSM message export
1	SENDOVR	R/W	0h	Send overflow data in CSM frame
0	ENBL	R/W	0h	CTSET STM global enable for counter/timer messages

14.3.2.4.2.21 CTSET2_CFG_CTSTMMSTID Register

14.3.2.4.2.21.1 CTSET2_CFG_CTSTMMSTID Register (Offset = 824h) [reset = 0h]

Counter Timer STM Master ID register

Return to Summary Table

Table 14-8433. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8824h

Figure 14-4189. CTSET2_CFG_CTSTMMSTID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MASTID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8434. CTSET2_CFG_CTSTMMSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	MASTID	R/W	0h	HW Master ID for System Event module

14.3.2.4.2.22 CTSET2_CFG_CTSTMINTVL Register

14.3.2.4.2.22.1 CTSET2_CFG_CTSTMINTVL Register (Offset = 828h) [reset = 0h]

Counter Timer STM Interval Register

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Table 14-8435. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8828h

Figure 14-4190. CTSET2_CFG_CTSTMINTVL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">INTERVAL</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTERVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8436. CTSET2_CFG_CTSTMINTVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	INTERVAL	R/W	0h	Counter Timer Periodic export interval

14.3.2.4.2.23 CTSET2_CFG_CTSTMSEL0 Register

14.3.2.4.2.23.1 CTSET2_CFG_CTSTMSEL0 Register (Offset = 82Ch) [reset = 0h]

Counter Timer STM Counter Select Register 0. This Selects Counter 0 to 31

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Table 14-8437. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 882Ch

Figure 14-4191. CTSET2_CFG_CTSTMSEL0 Name Register

31	30	29	28	27	26	25	24
COUNTSEL							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEL							
R/W							
0h							

Table 14-8438. CTSET2_CFG_CTSTMSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTSEL	R/W	0h	The individual bit is this field indicate whether the corresponding counter value is included in the CSM message generated via the STM interface

14.3.2.4.2.24 CTSET2_CFG_CTSTMSEL1 Register

14.3.2.4.2.24.1 CTSET2_CFG_CTSTMSEL1 Register (Offset = 830h) [reset = 0h]

Counter Timer STM Counter Select Register 1. This Selects Counter 32 to 63

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Table 14-8439. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8830h

Figure 14-4192. CTSET2_CFG_CTSTMSEL1 Name Register

31	30	29	28	27	26	25	24
COUNTSEL							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNTSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNTSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEL							
R/W							
0h							

Table 14-8440. CTSET2_CFG_CTSTMSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTSEL	R/W	0h	The individual bit is this field indicate whether the corresponding counter value is included in the CSM message generated via the STM interface

14.3.2.4.2.25 CTSET2_CFG_CTDBGSGL0 Register

14.3.2.4.2.25.1 CTSET2_CFG_CTDBGSGL0 Register (Offset = 8A0h) [reset = 0h]

Timer Interval Register 0. Interval match value for timer 0 in CTSET Timer Interval Register 1. Interval match value for timer 1 in CTSET Timer Interval Register 2. Interval match value for timer 2 in CTSET Timer Interval Register 3. Interval match value for timer 3 in CTSET Timer Interval Register 4. Interval match value for timer 4 in CTSET Timer Interval Register 5. Interval match value for timer 5 in CTSET Timer Interval Register 6. Interval match value for timer 6 in CTSET Timer Interval Register 7. Interval match value for timer 7 in CTSET Timer Interval Register 8. Interval match value for timer 8 in CTSET Timer Interval Register 9. Interval match value for timer 9 in CTSET Timer Interval Register 10. Interval match value for timer 10 in CTSET Timer Interval Register 11. Interval match value for timer 11 in CTSET Timer Interval Register 12. Interval match value for timer 12 in CTSET Timer Interval Register 13. Interval match value for timer 13 in CTSET Timer Interval Register 14. Interval match value for timer 14 in CTSET Timer Interval Register 15. Interval match value for timer 15 in CTSET Counter Timer Debug Event Register 0

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Table 14-8441. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 88A0h

Figure 14-4193. CTSET2_CFG_CTDBGSGL0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8442. CTSET2_CFG_CTDBGSGL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.4.2.26 CTSET2_CFG_CTDBGSGL1 Register

14.3.2.4.2.26.1 CTSET2_CFG_CTDBGSGL1 Register (Offset = 8A4h) [reset = 0h]

Counter Timer Debug Event Register 1

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Table 14-8443. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 88A4h

Figure 14-4194. CTSET2_CFG_CTDBGSGL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8444. CTSET2_CFG_CTDBGSGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.4.2.27 CTSET2_CFG_CTDBGSGL2 Register

14.3.2.4.2.27.1 CTSET2_CFG_CTDBGSGL2 Register (Offset = 8A8h) [reset = 0h]

Counter Timer Debug Event Register 2

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Table 14-8445. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 88A8h

Figure 14-4195. CTSET2_CFG_CTDBGSGL2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8446. CTSET2_CFG_CTDBGSGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.4.2.28 CTSET2_CFG_CTDBGSGL3 Register

14.3.2.4.2.28.1 CTSET2_CFG_CTDBGSGL3 Register (Offset = 8ACh) [reset = 0h]

Counter Timer Debug Event Register 3

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Table 14-8447. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 88ACh

Figure 14-4196. CTSET2_CFG_CTDBGSGL3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8448. CTSET2_CFG_CTDBGSGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.4.2.29 CTSET2_CFG_CTDBGSGL4 Register

14.3.2.4.2.29.1 CTSET2_CFG_CTDBGSGL4 Register (Offset = 8B0h) [reset = 0h]

Counter Timer Debug Event Register 4

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Table 14-8449. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 88B0h

Figure 14-4197. CTSET2_CFG_CTDBGSGL4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8450. CTSET2_CFG_CTDBGSGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.4.2.30 CTSET2_CFG_CTDBGSGL5 Register

14.3.2.4.2.30.1 CTSET2_CFG_CTDBGSGL5 Register (Offset = 8B4h) [reset = 0h]

Counter Timer Debug Event Register5

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Table 14-8451. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 88B4h

Figure 14-4198. CTSET2_CFG_CTDBGSGL5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8452. CTSET2_CFG_CTDBGSGL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.4.2.31 CTSET2_CFG_CTDBGSGL6 Register

14.3.2.4.2.31.1 CTSET2_CFG_CTDBGSGL6 Register (Offset = 8B8h) [reset = 0h]

Counter Timer Debug Event Register 6

Return to Summary Table

Table 14-8453. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 88B8h

Figure 14-4199. CTSET2_CFG_CTDBGSGL6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INPSEL							
R/W							
0h							

Table 14-8454. CTSET2_CFG_CTDBGSGL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.4.2.32 CTSET2_CFG_CTDBGSGL7 Register

14.3.2.4.2.32.1 CTSET2_CFG_CTDBGSGL7 Register (Offset = 8BCh) [reset = 0h]

Counter Timer Debug Event Register 7

Return to Summary Table

Table 14-8455. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 88BCh

Figure 14-4200. CTSET2_CFG_CTDBGSGL7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8456. CTSET2_CFG_CTDBGSGL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INPSEL	R/W	0h	Counter Timer input selection

14.3.2.4.2.33 CTSET2_CFG_CTGNBL0 Register

14.3.2.4.2.33.1 CTSET2_CFG_CTGNBL0 Register (Offset = 9F0h) [reset = 0h]

Counter Timer Global Enable Register 0. This enables Counter 0 to 31

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Table 14-8457. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 89F0h

Figure 14-4201. CTSET2_CFG_CTGNBL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENABLE							
R/W							
0h							

Table 14-8458. CTSET2_CFG_CTGNBL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENABLE	R/W	0h	The individual bit is this field enables the corresponding counter. Bits 30 and 31 will be high if global time stamp output interface is enabled

14.3.2.4.2.34 CTSET2_CFG_CTGNBL1 Register

14.3.2.4.2.34.1 CTSET2_CFG_CTGNBL1 Register (Offset = 9F4h) [reset = 0h]

Counter Timer Global Enable Register 1. This enables Counter 32 to 63

Return to Summary Table

Table 14-8459. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 89F4h

Figure 14-4202. CTSET2_CFG_CTGNBL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENABLE							
R/W							
0h							

Table 14-8460. CTSET2_CFG_CTGNBL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENABLE	R/W	0h	The individual bit is this field enables the corresponding counter

14.3.2.4.2.35 CTSET2_CFG_CTGRST0 Register

14.3.2.4.2.35.1 CTSET2_CFG_CTGRST0 Register (Offset = 9F8h) [reset = 0h]

Counter Timer Global Reset Register 0. This resets Counter 0 to 31

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Table 14-8461. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 89F8h

Figure 14-4203. CTSET2_CFG_CTGRST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESET							
R/W							
0h							

Table 14-8462. CTSET2_CFG_CTGRST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RESET	R/W	0h	The individual bit is this field resets the corresponding counter. These bits are self-clearing, once a '1' is written, after the counters are reset these bits are cleared. When Global Time Stamp output interface is enabled, counter 31 and counter 30 should not be written to any value

14.3.2.4.2.36 CTSET2_CFG_CTGRST1 Register

14.3.2.4.2.36.1 CTSET2_CFG_CTGRST1 Register (Offset = 9FCh) [reset = 0h]

Counter Timer Global Reset Register 0. This resets Counter 32 to 63

Return to Summary Table

Table 14-8463. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 89FCh

Figure 14-4204. CTSET2_CFG_CTGRST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESET							
R/W							
0h							

Table 14-8464. CTSET2_CFG_CTGRST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RESET	R/W	0h	The individual bit is this field resets the corresponding counter. These bits are self-clearing, once a '1' is written, after the counters are reset these bits are cleared.

14.3.2.4.2.37 CTSET2_CFG_CTCR0 Register

14.3.2.4.2.37.1 CTSET2_CFG_CTCR0 Register (Offset = A00h) [reset = 0h]

Counter Timer Control Register 0

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Table 14-8465. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A00h

Figure 14-4205. CTSET2_CFG_CTCR0 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8466. CTSET2_CFG_CTCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8466. CTSET2_CFG_CTCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.38 CTSET2_CFG_CTCR1 Register

14.3.2.4.2.38.1 CTSET2_CFG_CTCR1 Register (Offset = A04h) [reset = 0h]

Counter Timer Control Register 1

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Table 14-8467. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A04h

Figure 14-4206. CTSET2_CFG_CTCR1 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8468. CTSET2_CFG_CTCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8468. CTSET2_CFG_CTCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.39 CTSET2_CFG_CTCR2 Register

14.3.2.4.2.39.1 CTSET2_CFG_CTCR2 Register (Offset = A08h) [reset = 0h]

Counter Timer Control Register 2

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Table 14-8469. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A08h

Figure 14-4207. CTSET2_CFG_CTCR2 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8470. CTSET2_CFG_CTCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8470. CTSET2_CFG_CTCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.40 CTSET2_CFG_CTCR3 Register

14.3.2.4.2.40.1 CTSET2_CFG_CTCR3 Register (Offset = A0Ch) [reset = 0h]

Counter Timer Control Register 3

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Table 14-8471. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A0Ch

Figure 14-4208. CTSET2_CFG_CTCR3 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8472. CTSET2_CFG_CTCR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8472. CTSET2_CFG_CTCR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.41 CTSET2_CFG_CTCR4 Register

14.3.2.4.2.41.1 CTSET2_CFG_CTCR4 Register (Offset = A10h) [reset = 0h]

Counter Timer Control Register 4

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Table 14-8473. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A10h

Figure 14-4209. CTSET2_CFG_CTCR4 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8474. CTSET2_CFG_CTCR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8474. CTSET2_CFG_CTCR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.42 CTSET2_CFG_CTCR5 Register

14.3.2.4.2.42.1 CTSET2_CFG_CTCR5 Register (Offset = A14h) [reset = 0h]

Counter Timer Control Register 5

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Table 14-8475. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A14h

Figure 14-4210. CTSET2_CFG_CTCR5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8476. CTSET2_CFG_CTCR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8476. CTSET2_CFG_CTCR5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.43 CTSET2_CFG_CTCR6 Register

14.3.2.4.2.43.1 CTSET2_CFG_CTCR6 Register (Offset = A18h) [reset = 0h]

Counter Timer Control Register 6

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Table 14-8477. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A18h

Figure 14-4211. CTSET2_CFG_CTCR6 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							

23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							

15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8478. CTSET2_CFG_CTCR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8478. CTSET2_CFG_CTCR6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.44 CTSET2_CFG_CTCR7 Register

14.3.2.4.2.44.1 CTSET2_CFG_CTCR7 Register (Offset = A1Ch) [reset = 0h]

Counter Timer Control Register 7

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Table 14-8479. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A1Ch

Figure 14-4212. CTSET2_CFG_CTCR7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8480. CTSET2_CFG_CTCR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8480. CTSET2_CFG_CTCR7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.45 CTSET2_CFG_CTCR8 Register

14.3.2.4.2.45.1 CTSET2_CFG_CTCR8 Register (Offset = A20h) [reset = 0h]

Counter Timer Control Register 8

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Table 14-8481. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A20h

Figure 14-4213. CTSET2_CFG_CTCR8 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8482. CTSET2_CFG_CTCR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8482. CTSET2_CFG_CTCR8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.46 CTSET2_CFG_CTCR9 Register

14.3.2.4.2.46.1 CTSET2_CFG_CTCR9 Register (Offset = A24h) [reset = 0h]

Counter Timer Control Register 9

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Table 14-8483. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A24h

Figure 14-4214. CTSET2_CFG_CTCR9 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8484. CTSET2_CFG_CTCR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8484. CTSET2_CFG_CTCR9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.47 CTSET2_CFG_CTCR10 Register

14.3.2.4.2.47.1 CTSET2_CFG_CTCR10 Register (Offset = A28h) [reset = 0h]

Counter Timer Control Register 10

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Table 14-8485. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A28h

Figure 14-4215. CTSET2_CFG_CTCR10 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8486. CTSET2_CFG_CTCR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8486. CTSET2_CFG_CTCR10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.48 CTSET2_CFG_CTCR11 Register

14.3.2.4.2.48.1 CTSET2_CFG_CTCR11 Register (Offset = A2Ch) [reset = 0h]

Counter Timer Control Register 11

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Table 14-8487. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A2Ch

Figure 14-4216. CTSET2_CFG_CTCR11 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							

23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							

15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8488. CTSET2_CFG_CTCR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8488. CTSET2_CFG_CTCR11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.49 CTSET2_CFG_CTCR12 Register

14.3.2.4.2.49.1 CTSET2_CFG_CTCR12 Register (Offset = A30h) [reset = 0h]

Counter Timer Control Register 12

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Table 14-8489. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A30h

Figure 14-4217. CTSET2_CFG_CTCR12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WDRESET</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPSEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MODESEL</td><td>FILTER</td><td>DBG_TRIG_STAT</td><td>WDMODE</td><td>RESTART</td><td>DBG</td><td>INT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CHNSDW</td><td>OVRFLW</td><td colspan="2">RESERVED</td><td>DURMODE</td><td>CHAIN</td><td>RESET</td><td>ENBL</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8490. CTSET2_CFG_CTCR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8490. CTSET2_CFG_CTCR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.50 CTSET2_CFG_CTCR13 Register

14.3.2.4.2.50.1 CTSET2_CFG_CTCR13 Register (Offset = A34h) [reset = 0h]

Counter Timer Control Register 13

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Table 14-8491. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A34h

Figure 14-4218. CTSET2_CFG_CTCR13 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8492. CTSET2_CFG_CTCR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8492. CTSET2_CFG_CTCR13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.51 CTSET2_CFG_CTCR14 Register

14.3.2.4.2.51.1 CTSET2_CFG_CTCR14 Register (Offset = A38h) [reset = 0h]

Counter Timer Control Register 14

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Table 14-8493. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A38h

Figure 14-4219. CTSET2_CFG_CTCR14 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8494. CTSET2_CFG_CTCR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8494. CTSET2_CFG_CTCR14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.52 CTSET2_CFG_CTCR15 Register

14.3.2.4.2.52.1 CTSET2_CFG_CTCR15 Register (Offset = A3Ch) [reset = 0h]

Counter Timer Control Register 15

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Table 14-8495. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A3Ch

Figure 14-4220. CTSET2_CFG_CTCR15 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8496. CTSET2_CFG_CTCR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8496. CTSET2_CFG_CTCR15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.53 CTSET2_CFG_CTCR16 Register

14.3.2.4.2.53.1 CTSET2_CFG_CTCR16 Register (Offset = A40h) [reset = 0h]

Counter Timer Control Register 16

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Table 14-8497. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A40h

Figure 14-4221. CTSET2_CFG_CTCR16 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8498. CTSET2_CFG_CTCR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8498. CTSET2_CFG_CTCR16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.54 CTSET2_CFG_CTCR17 Register

14.3.2.4.2.54.1 CTSET2_CFG_CTCR17 Register (Offset = A44h) [reset = 0h]

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Table 14-8499. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A44h

Figure 14-4222. CTSET2_CFG_CTCR17 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8500. CTSET2_CFG_CTCR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8500. CTSET2_CFG_CTCR17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.55 CTSET2_CFG_CTCR18 Register

14.3.2.4.2.55.1 CTSET2_CFG_CTCR18 Register (Offset = A48h) [reset = 0h]

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Table 14-8501. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A48h

Figure 14-4223. CTSET2_CFG_CTCR18 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8502. CTSET2_CFG_CTCR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8502. CTSET2_CFG_CTCR18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.56 CTSET2_CFG_CTCR19 Register

14.3.2.4.2.56.1 CTSET2_CFG_CTCR19 Register (Offset = A4Ch) [reset = 0h]

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Table 14-8503. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A4Ch

Figure 14-4224. CTSET2_CFG_CTCR19 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8504. CTSET2_CFG_CTCR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8504. CTSET2_CFG_CTCR19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.57 CTSET2_CFG_CTCR20 Register

14.3.2.4.2.57.1 CTSET2_CFG_CTCR20 Register (Offset = A50h) [reset = 0h]

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Table 14-8505. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A50h

Figure 14-4225. CTSET2_CFG_CTCR20 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8506. CTSET2_CFG_CTCR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8506. CTSET2_CFG_CTCR20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.58 CTSET2_CFG_CTCR21 Register

14.3.2.4.2.58.1 CTSET2_CFG_CTCR21 Register (Offset = A54h) [reset = 0h]

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Table 14-8507. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A54h

Figure 14-4226. CTSET2_CFG_CTCR21 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8508. CTSET2_CFG_CTCR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8508. CTSET2_CFG_CTCR21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.59 CTSET2_CFG_CTCR22 Register

14.3.2.4.2.59.1 CTSET2_CFG_CTCR22 Register (Offset = A58h) [reset = 0h]

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Table 14-8509. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A58h

Figure 14-4227. CTSET2_CFG_CTCR22 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8510. CTSET2_CFG_CTCR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8510. CTSET2_CFG_CTCR22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.60 CTSET2_CFG_CTCR23 Register

14.3.2.4.2.60.1 CTSET2_CFG_CTCR23 Register (Offset = A5Ch) [reset = 0h]

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Table 14-8511. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A5Ch

Figure 14-4228. CTSET2_CFG_CTCR23 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8512. CTSET2_CFG_CTCR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8512. CTSET2_CFG_CTCR23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.61 CTSET2_CFG_CTCR24 Register

14.3.2.4.2.61.1 CTSET2_CFG_CTCR24 Register (Offset = A60h) [reset = 0h]

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Table 14-8513. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A60h

Figure 14-4229. CTSET2_CFG_CTCR24 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8514. CTSET2_CFG_CTCR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8514. CTSET2_CFG_CTCR24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.62 CTSET2_CFG_CTCR25 Register

14.3.2.4.2.62.1 CTSET2_CFG_CTCR25 Register (Offset = A64h) [reset = 0h]

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Table 14-8515. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A64h

Figure 14-4230. CTSET2_CFG_CTCR25 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							

23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							

15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8516. CTSET2_CFG_CTCR25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8516. CTSET2_CFG_CTCR25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.63 CTSET2_CFG_CTCR26 Register

14.3.2.4.2.63.1 CTSET2_CFG_CTCR26 Register (Offset = A68h) [reset = 0h]

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Table 14-8517. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A68h

Figure 14-4231. CTSET2_CFG_CTCR26 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPSEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8518. CTSET2_CFG_CTCR26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8518. CTSET2_CFG_CTCR26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.64 CTSET2_CFG_CTCR27 Register

14.3.2.4.2.64.1 CTSET2_CFG_CTCR27 Register (Offset = A6Ch) [reset = 0h]

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Table 14-8519. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A6Ch

Figure 14-4232. CTSET2_CFG_CTCR27 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8520. CTSET2_CFG_CTCR27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8520. CTSET2_CFG_CTCR27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.65 CTSET2_CFG_CTCR28 Register

14.3.2.4.2.65.1 CTSET2_CFG_CTCR28 Register (Offset = A70h) [reset = 0h]

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Table 14-8521. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A70h

Figure 14-4233. CTSET2_CFG_CTCR28 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8522. CTSET2_CFG_CTCR28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8522. CTSET2_CFG_CTCR28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.66 CTSET2_CFG_CTCR29 Register

14.3.2.4.2.66.1 CTSET2_CFG_CTCR29 Register (Offset = A74h) [reset = 0h]

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Table 14-8523. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A74h

Figure 14-4234. CTSET2_CFG_CTCR29 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8524. CTSET2_CFG_CTCR29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8524. CTSET2_CFG_CTCR29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.67 CTSET2_CFG_CTCR30 Register

14.3.2.4.2.67.1 CTSET2_CFG_CTCR30 Register (Offset = A78h) [reset = 0h]

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Table 14-8525. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A78h

Figure 14-4235. CTSET2_CFG_CTCR30 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8526. CTSET2_CFG_CTCR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8526. CTSET2_CFG_CTCR30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.68 CTSET2_CFG_CTCR31 Register

14.3.2.4.2.68.1 CTSET2_CFG_CTCR31 Register (Offset = A7Ch) [reset = 0h]

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Table 14-8527. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A7Ch

Figure 14-4236. CTSET2_CFG_CTCR31 Name Register

31	30	29	28	27	26	25	24
WDRESET							
R/W							
0h							
23	22	21	20	19	18	17	16
INPSEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MODESEL		FILTER	DBG_TRIG_STAT	WDMODE	RESTART	DBG	INT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHNSDW	OVRFLW	RESERVED		DURMODE	CHAIN	RESET	ENBL
R/W	R/W	R		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-8528. CTSET2_CFG_CTCR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WDRESET	R/W	0h	WD reset event input selector. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
23:16	INPSEL	R/W	0h	Counter Timer input selection. For WD mode it is the start event selector
15:14	MODESEL	R/W	0h	Counter is in duration or occurrence mode. Only writable by debug accesses
13	FILTER	R/W	0h	Use associated operating mode filter in CTMODEFILTERn
12	DBG_TRIG_STAT	R/W	0h	Debug event triggered. Write 1 will clear this bit. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
11	WDMODE	R/W	0h	WD Timer mode selection. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
10	RESTART	R/W	0h	Restart the timer after an interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
9	DBG	R/W	0h	Signal debug logic on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function
8	INT	R/W	0h	Generate interrupt on interval match. Only available for modules capable of timer and counter functions. This bit is reserved (read only) for counter registers which are only counter function

Table 14-8528. CTSET2_CFG_CTCR31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CHNSDW	R/W	0h	Counter has a shadow register for chain reads. Only valid on counters with an even number index
6	OVRFLW	R/W	0h	Counter is in duration or occurrence mode
5:4	RESERVED	R	0h	Reserved, returns 0
3	DURMODE	R/W	0h	Counter is in duration or occurrence mode
2	CHAIN	R/W	0h	Counter is chained to an adjacent counter
1	RESET	R/W	0h	Counter reset control
0	ENBL	R/W	0h	Counter enable control

14.3.2.4.2.69 CTSET2_CFG_CTOWN0 Register

14.3.2.4.2.69.1 CTSET2_CFG_CTOWN0 Register (Offset = A80h) [reset = 20000000h]

Counter/Timer Ownership register 0

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Table 14-8529. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A80h

Figure 14-4237. CTSET2_CFG_CTOWN0 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8530. CTSET2_CFG_CTOWN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.70 CTSET2_CFG_CTOWN1 Register

14.3.2.4.2.70.1 CTSET2_CFG_CTOWN1 Register (Offset = A84h) [reset = 20000000h]

Counter/Timer Ownership register 1

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Table 14-8531. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A84h

Figure 14-4238. CTSET2_CFG_CTOWN1 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8532. CTSET2_CFG_CTOWN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.71 CTSET2_CFG_CTOWN2 Register

14.3.2.4.2.71.1 CTSET2_CFG_CTOWN2 Register (Offset = A88h) [reset = 20000000h]

Counter/Timer Ownership register 2

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Table 14-8533. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A88h

Figure 14-4239. CTSET2_CFG_CTOWN2 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8534. CTSET2_CFG_CTOWN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.72 CTSET2_CFG_CTOWN3 Register

14.3.2.4.2.72.1 CTSET2_CFG_CTOWN3 Register (Offset = A8Ch) [reset = 20000000h]

Counter/Timer Ownership register 3

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Table 14-8535. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A8Ch

Figure 14-4240. CTSET2_CFG_CTOWN3 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8536. CTSET2_CFG_CTOWN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.73 CTSET2_CFG_CTOWN4 Register

14.3.2.4.2.73.1 CTSET2_CFG_CTOWN4 Register (Offset = A90h) [reset = 20000000h]

Counter/Timer Ownership register 4

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Table 14-8537. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A90h

Figure 14-4241. CTSET2_CFG_CTOWN4 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8538. CTSET2_CFG_CTOWN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.74 CTSET2_CFG_CTOWN5 Register

14.3.2.4.2.74.1 CTSET2_CFG_CTOWN5 Register (Offset = A94h) [reset = 20000000h]

Counter/Timer Ownership register 5

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Table 14-8539. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A94h

Figure 14-4242. CTSET2_CFG_CTOWN5 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8540. CTSET2_CFG_CTOWN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.75 CTSET2_CFG_CTOWN6 Register

14.3.2.4.2.75.1 CTSET2_CFG_CTOWN6 Register (Offset = A98h) [reset = 20000000h]

Counter/Timer Ownership register 6

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Table 14-8541. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A98h

Figure 14-4243. CTSET2_CFG_CTOWN6 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8542. CTSET2_CFG_CTOWN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.76 CTSET2_CFG_CTOWN7 Register

14.3.2.4.2.76.1 CTSET2_CFG_CTOWN7 Register (Offset = A9Ch) [reset = 20000000h]

Counter/Timer Ownership register 7

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Table 14-8543. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8A9Ch

Figure 14-4244. CTSET2_CFG_CTOWN7 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8544. CTSET2_CFG_CTOWN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.77 CTSET2_CFG_CTOWN8 Register

14.3.2.4.2.77.1 CTSET2_CFG_CTOWN8 Register (Offset = AA0h) [reset = 20000000h]

Counter/Timer Ownership register 8

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Table 14-8545. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AA0h

Figure 14-4245. CTSET2_CFG_CTOWN8 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8546. CTSET2_CFG_CTOWN8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.78 CTSET2_CFG_CTOWN9 Register

14.3.2.4.2.78.1 CTSET2_CFG_CTOWN9 Register (Offset = AA4h) [reset = 20000000h]

Counter/Timer Ownership register 9

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Table 14-8547. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AA4h

Figure 14-4246. CTSET2_CFG_CTOWN9 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8548. CTSET2_CFG_CTOWN9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.79 CTSET2_CFG_CTOWN10 Register

14.3.2.4.2.79.1 CTSET2_CFG_CTOWN10 Register (Offset = AA8h) [reset = 20000000h]

Counter/Timer Ownership register 10

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Table 14-8549. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AA8h

Figure 14-4247. CTSET2_CFG_CTOWN10 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8550. CTSET2_CFG_CTOWN10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.80 CTSET2_CFG_CTOWN11 Register

14.3.2.4.2.80.1 CTSET2_CFG_CTOWN11 Register (Offset = AACh) [reset = 20000000h]

Counter/Timer Ownership register 11

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Table 14-8551. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AACh

Figure 14-4248. CTSET2_CFG_CTOWN11 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8552. CTSET2_CFG_CTOWN11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.81 CTSET2_CFG_CTOWN12 Register

14.3.2.4.2.81.1 CTSET2_CFG_CTOWN12 Register (Offset = AB0h) [reset = 20000000h]

Counter/Timer Ownership register 12

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Table 14-8553. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AB0h

Figure 14-4249. CTSET2_CFG_CTOWN12 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8554. CTSET2_CFG_CTOWN12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.82 CTSET2_CFG_CTOWN13 Register

14.3.2.4.2.82.1 CTSET2_CFG_CTOWN13 Register (Offset = AB4h) [reset = 20000000h]

Counter/Timer Ownership register 13

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Table 14-8555. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AB4h

Figure 14-4250. CTSET2_CFG_CTOWN13 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8556. CTSET2_CFG_CTOWN13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.83 CTSET2_CFG_CTOWN14 Register

14.3.2.4.2.83.1 CTSET2_CFG_CTOWN14 Register (Offset = AB8h) [reset = 20000000h]

Counter/Timer Ownership register 14

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Table 14-8557. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AB8h

Figure 14-4251. CTSET2_CFG_CTOWN14 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8558. CTSET2_CFG_CTOWN14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.84 CTSET2_CFG_CTOWN15 Register

14.3.2.4.2.84.1 CTSET2_CFG_CTOWN15 Register (Offset = ABCh) [reset = 20000000h]

Counter/Timer Ownership register 15

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Table 14-8559. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8ABCh

Figure 14-4252. CTSET2_CFG_CTOWN15 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8560. CTSET2_CFG_CTOWN15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.85 CTSET2_CFG_CTOWN16 Register

14.3.2.4.2.85.1 CTSET2_CFG_CTOWN16 Register (Offset = AC0h) [reset = 20000000h]

Counter/Timer Ownership register 16

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Table 14-8561. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AC0h

Figure 14-4253. CTSET2_CFG_CTOWN16 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8562. CTSET2_CFG_CTOWN16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.86 CTSET2_CFG_CTOWN17 Register

14.3.2.4.2.86.1 CTSET2_CFG_CTOWN17 Register (Offset = AC4h) [reset = 20000000h]

Counter/Timer Ownership register 17

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Table 14-8563. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AC4h

Figure 14-4254. CTSET2_CFG_CTOWN17 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8564. CTSET2_CFG_CTOWN17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.87 CTSET2_CFG_CTOWN18 Register

14.3.2.4.2.87.1 CTSET2_CFG_CTOWN18 Register (Offset = AC8h) [reset = 20000000h]

Counter/Timer Ownership register 18

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Table 14-8565. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AC8h

Figure 14-4255. CTSET2_CFG_CTOWN18 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8566. CTSET2_CFG_CTOWN18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.88 CTSET2_CFG_CTOWN19 Register

14.3.2.4.2.88.1 CTSET2_CFG_CTOWN19 Register (Offset = ACCh) [reset = 20000000h]

Counter/Timer Ownership register 19

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Table 14-8567. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8ACCh

Figure 14-4256. CTSET2_CFG_CTOWN19 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8568. CTSET2_CFG_CTOWN19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.89 CTSET2_CFG_CTOWN20 Register

14.3.2.4.2.89.1 CTSET2_CFG_CTOWN20 Register (Offset = AD0h) [reset = 20000000h]

Counter/Timer Ownership register 20

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Table 14-8569. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AD0h

Figure 14-4257. CTSET2_CFG_CTOWN20 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8570. CTSET2_CFG_CTOWN20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.90 CTSET2_CFG_CTOWN21 Register

14.3.2.4.2.90.1 CTSET2_CFG_CTOWN21 Register (Offset = AD4h) [reset = 20000000h]

Counter/Timer Ownership register 21

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Table 14-8571. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AD4h

Figure 14-4258. CTSET2_CFG_CTOWN21 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8572. CTSET2_CFG_CTOWN21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.91 CTSET2_CFG_CTOWN22 Register

14.3.2.4.2.91.1 CTSET2_CFG_CTOWN22 Register (Offset = AD8h) [reset = 20000000h]

Counter/Timer Ownership register 22

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Table 14-8573. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AD8h

Figure 14-4259. CTSET2_CFG_CTOWN22 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8574. CTSET2_CFG_CTOWN22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.92 CTSET2_CFG_CTOWN23 Register

14.3.2.4.2.92.1 CTSET2_CFG_CTOWN23 Register (Offset = ADCh) [reset = 20000000h]

Counter/Timer Ownership register23

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Table 14-8575. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8ADCh

Figure 14-4260. CTSET2_CFG_CTOWN23 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8576. CTSET2_CFG_CTOWN23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.93 CTSET2_CFG_CTOWN24 Register

14.3.2.4.2.93.1 CTSET2_CFG_CTOWN24 Register (Offset = AE0h) [reset = 20000000h]

Counter/Timer Ownership register 24

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Table 14-8577. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AE0h

Figure 14-4261. CTSET2_CFG_CTOWN24 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8578. CTSET2_CFG_CTOWN24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.94 CTSET2_CFG_CTOWN25 Register

14.3.2.4.2.94.1 CTSET2_CFG_CTOWN25 Register (Offset = AE4h) [reset = 20000000h]

Counter/Timer Ownership register 25

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Table 14-8579. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AE4h

Figure 14-4262. CTSET2_CFG_CTOWN25 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8580. CTSET2_CFG_CTOWN25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.95 CTSET2_CFG_CTOWN26 Register

14.3.2.4.2.95.1 CTSET2_CFG_CTOWN26 Register (Offset = AE8h) [reset = 20000000h]

Counter/Timer Ownership register 26

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Table 14-8581. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AE8h

Figure 14-4263. CTSET2_CFG_CTOWN26 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8582. CTSET2_CFG_CTOWN26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.96 CTSET2_CFG_CTOWN27 Register

14.3.2.4.2.96.1 CTSET2_CFG_CTOWN27 Register (Offset = AECh) [reset = 20000000h]

Counter/Timer Ownership register 27

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Table 14-8583. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AECh

Figure 14-4264. CTSET2_CFG_CTOWN27 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8584. CTSET2_CFG_CTOWN27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.97 CTSET2_CFG_CTOWN28 Register

14.3.2.4.2.97.1 CTSET2_CFG_CTOWN28 Register (Offset = AF0h) [reset = 20000000h]

Counter/Timer Ownership register 28

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Table 14-8585. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AF0h

Figure 14-4265. CTSET2_CFG_CTOWN28 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">OWNERSHIP</td><td>DBG_OVERIDE</td><td>CURRENT_OWNER</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">0h</td><td>1h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8586. CTSET2_CFG_CTOWN28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.98 CTSET2_CFG_CTOWN29 Register

14.3.2.4.2.98.1 CTSET2_CFG_CTOWN29 Register (Offset = AF4h) [reset = 20000000h]

Counter/Timer Ownership register 29

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Table 14-8587. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AF4h

Figure 14-4266. CTSET2_CFG_CTOWN29 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8588. CTSET2_CFG_CTOWN29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.99 CTSET2_CFG_CTOWN30 Register

14.3.2.4.2.99.1 CTSET2_CFG_CTOWN30 Register (Offset = AF8h) [reset = 20000000h]

Counter/Timer Ownership register 30

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Table 14-8589. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AF8h

Figure 14-4267. CTSET2_CFG_CTOWN30 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-8590. CTSET2_CFG_CTOWN30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.100 CTSET2_CFG_CTOWN31 Register

14.3.2.4.2.100.1 CTSET2_CFG_CTOWN31 Register (Offset = AFCh) [reset = 20000000h]

Counter/Timer Ownership register 31

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Table 14-8591. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8AFCh

Figure 14-4268. CTSET2_CFG_CTOWN31 Name Register

31	30	29	28	27	26	25	24
OWNERSHIP		DBG_OVERIDE	CURRENT_OWNER	RESERVED			
R/W		R/W	R	R			
0h		1h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R							
0h							

Table 14-8592. CTSET2_CFG_CTOWN31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	OWNERSHIP	R/W	0h	Counter/Timer Ownership Status. The Read encoding is (0=Available, 1=Claimed, 2=Enabled, 3=Reserved). The write commands are (0=release, 1=claim, 2=enable, 3=nop)
29	DBG_OVERIDE	R/W	1h	This bit indicates the debugger is Claiming the resource, always reads back as 1
28	CURRENT_OWNER	R	0h	This value reflects the Counter/Timer ownership when the register is in a non-Available state, 1=Ap owned, 0=Dbg owned
27:0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.101 CTSET2_CFG_CTFILT0 Register

14.3.2.4.2.101.1 CTSET2_CFG_CTFILT0 Register (Offset = B00h) [reset = 0h]

Counter Timer 0 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8593. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B00h

Figure 14-4269. CTSET2_CFG_CTFILT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8594. CTSET2_CFG_CTFILT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.102 CTSET2_CFG_CTFILT1 Register

14.3.2.4.2.102.1 CTSET2_CFG_CTFILT1 Register (Offset = B04h) [reset = 0h]

Counter Timer 1 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8595. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B04h

Figure 14-4270. CTSET2_CFG_CTFILT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8596. CTSET2_CFG_CTFILT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.103 CTSET2_CFG_CTFILT2 Register

14.3.2.4.2.103.1 CTSET2_CFG_CTFILT2 Register (Offset = B08h) [reset = 0h]

Counter Timer 2 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8597. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B08h

Figure 14-4271. CTSET2_CFG_CTFILT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8598. CTSET2_CFG_CTFILT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.104 CTSET2_CFG_CTFILT3 Register

14.3.2.4.2.104.1 CTSET2_CFG_CTFILT3 Register (Offset = B0Ch) [reset = 0h]

Counter Timer 3 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8599. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B0Ch

Figure 14-4272. CTSET2_CFG_CTFILT3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8600. CTSET2_CFG_CTFILT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.105 CTSET2_CFG_CTFILT4 Register

14.3.2.4.2.105.1 CTSET2_CFG_CTFILT4 Register (Offset = B10h) [reset = 0h]

Counter Timer 4 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8601. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B10h

Figure 14-4273. CTSET2_CFG_CTFILT4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8602. CTSET2_CFG_CTFILT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.106 CTSET2_CFG_CTFILT5 Register

14.3.2.4.2.106.1 CTSET2_CFG_CTFILT5 Register (Offset = B14h) [reset = 0h]

Counter Timer 5 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8603. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B14h

Figure 14-4274. CTSET2_CFG_CTFILT5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8604. CTSET2_CFG_CTFILT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.107 CTSET2_CFG_CTFILT6 Register

14.3.2.4.2.107.1 CTSET2_CFG_CTFILT6 Register (Offset = B18h) [reset = 0h]

Counter Timer 6 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8605. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B18h

Figure 14-4275. CTSET2_CFG_CTFILT6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8606. CTSET2_CFG_CTFILT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.108 CTSET2_CFG_CTFILT7 Register

14.3.2.4.2.108.1 CTSET2_CFG_CTFILT7 Register (Offset = B1Ch) [reset = 0h]

Counter Timer 7 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8607. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B1Ch

Figure 14-4276. CTSET2_CFG_CTFILT7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8608. CTSET2_CFG_CTFILT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.109 CTSET2_CFG_CTFILT8 Register

14.3.2.4.2.109.1 CTSET2_CFG_CTFILT8 Register (Offset = B20h) [reset = 0h]

Counter Timer 8 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8609. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B20h

Figure 14-4277. CTSET2_CFG_CTFILT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8610. CTSET2_CFG_CTFILT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.110 CTSET2_CFG_CTFILT9 Register

14.3.2.4.2.110.1 CTSET2_CFG_CTFILT9 Register (Offset = B24h) [reset = 0h]

Counter Timer 9 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8611. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B24h

Figure 14-4278. CTSET2_CFG_CTFILT9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8612. CTSET2_CFG_CTFILT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.111 CTSET2_CFG_CTFILT10 Register

14.3.2.4.2.111.1 CTSET2_CFG_CTFILT10 Register (Offset = B28h) [reset = 0h]

Counter Timer 10 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8613. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B28h

Figure 14-4279. CTSET2_CFG_CTFILT10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8614. CTSET2_CFG_CTFILT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.112 CTSET2_CFG_CTFILT11 Register

14.3.2.4.2.112.1 CTSET2_CFG_CTFILT11 Register (Offset = B2Ch) [reset = 0h]

Counter Timer 11 Filter Register. These filters are only activated if the CTCRn : FILTER is set

Return to Summary Table

Table 14-8615. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B2Ch

Figure 14-4280. CTSET2_CFG_CTFILT11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8616. CTSET2_CFG_CTFILT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.113 CTSET2_CFG_CTFILT12 Register

14.3.2.4.2.113.1 CTSET2_CFG_CTFILT12 Register (Offset = B30h) [reset = 0h]

Counter Timer 12 Filter Register. These filters are only activated if the CTCRn : FILTER is set

Return to Summary Table

Table 14-8617. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B30h

Figure 14-4281. CTSET2_CFG_CTFILT12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SECSUPER</td><td>SECUSER</td><td>RSUPER</td><td>RUSER</td><td>NRSUPER</td><td>NRUSER</td><td>IDLE</td><td>FREE</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8618. CTSET2_CFG_CTFILT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.114 CTSET2_CFG_CTFILT13 Register

14.3.2.4.2.114.1 CTSET2_CFG_CTFILT13 Register (Offset = B34h) [reset = 0h]

Counter Timer 13 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8619. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B34h

Figure 14-4282. CTSET2_CFG_CTFILT13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8620. CTSET2_CFG_CTFILT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.115 CTSET2_CFG_CTFILT14 Register

14.3.2.4.2.115.1 CTSET2_CFG_CTFILT14 Register (Offset = B38h) [reset = 0h]

Counter Timer 14 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8621. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B38h

Figure 14-4283. CTSET2_CFG_CTFILT14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8622. CTSET2_CFG_CTFILT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.116 CTSET2_CFG_CTFILT15 Register

14.3.2.4.2.116.1 CTSET2_CFG_CTFILT15 Register (Offset = B3Ch) [reset = 0h]

Counter Timer 15 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8623. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B3Ch

Figure 14-4284. CTSET2_CFG_CTFILT15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8624. CTSET2_CFG_CTFILT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.117 CTSET2_CFG_CTFILT16 Register

14.3.2.4.2.117.1 CTSET2_CFG_CTFILT16 Register (Offset = B40h) [reset = 0h]

Counter Timer 16 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8625. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B40h

Figure 14-4285. CTSET2_CFG_CTFILT16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8626. CTSET2_CFG_CTFILT16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.118 CTSET2_CFG_CTFILT17 Register

14.3.2.4.2.118.1 CTSET2_CFG_CTFILT17 Register (Offset = B44h) [reset = 0h]

Counter Timer 17 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8627. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B44h

Figure 14-4286. CTSET2_CFG_CTFILT17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8628. CTSET2_CFG_CTFILT17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.119 CTSET2_CFG_CTFILT18 Register

14.3.2.4.2.119.1 CTSET2_CFG_CTFILT18 Register (Offset = B48h) [reset = 0h]

Counter Timer 18 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8629. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B48h

Figure 14-4287. CTSET2_CFG_CTFILT18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8630. CTSET2_CFG_CTFILT18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.120 CTSET2_CFG_CTFILT19 Register

14.3.2.4.2.120.1 CTSET2_CFG_CTFILT19 Register (Offset = B4Ch) [reset = 0h]

Counter Timer 19 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8631. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B4Ch

Figure 14-4288. CTSET2_CFG_CTFILT19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8632. CTSET2_CFG_CTFILT19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.121 CTSET2_CFG_CTFILT20 Register

14.3.2.4.2.121.1 CTSET2_CFG_CTFILT20 Register (Offset = B50h) [reset = 0h]

Counter Timer 20 Filter Register. These filters are only activated if the CTCRn : FILTER is set

Return to Summary Table

Table 14-8633. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B50h

Figure 14-4289. CTSET2_CFG_CTFILT20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8634. CTSET2_CFG_CTFILT20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.122 CTSET2_CFG_CTFILT21 Register

14.3.2.4.2.122.1 CTSET2_CFG_CTFILT21 Register (Offset = B54h) [reset = 0h]

Counter Timer 21 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8635. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B54h

Figure 14-4290. CTSET2_CFG_CTFILT21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8636. CTSET2_CFG_CTFILT21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.123 CTSET2_CFG_CTFILT22 Register

14.3.2.4.2.123.1 CTSET2_CFG_CTFILT22 Register (Offset = B58h) [reset = 0h]

Counter Timer 22 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8637. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B58h

Figure 14-4291. CTSET2_CFG_CTFILT22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8638. CTSET2_CFG_CTFILT22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.124 CTSET2_CFG_CTFILT23 Register

14.3.2.4.2.124.1 CTSET2_CFG_CTFILT23 Register (Offset = B5Ch) [reset = 0h]

Counter Timer 23 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8639. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B5Ch

Figure 14-4292. CTSET2_CFG_CTFILT23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8640. CTSET2_CFG_CTFILT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.125 CTSET2_CFG_CTFILT24 Register

14.3.2.4.2.125.1 CTSET2_CFG_CTFILT24 Register (Offset = B60h) [reset = 0h]

Counter Timer 24 Filter Register. These filters are only activated if the CTCRn : FILTER is set

Return to Summary Table

Table 14-8641. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B60h

Figure 14-4293. CTSET2_CFG_CTFILT24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8642. CTSET2_CFG_CTFILT24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.126 CTSET2_CFG_CTFILT25 Register

14.3.2.4.2.126.1 CTSET2_CFG_CTFILT25 Register (Offset = B64h) [reset = 0h]

Counter Timer 25 Filter Register. These filters are only activated if the CTCRn : FILTER is set

Return to Summary Table

Table 14-8643. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B64h

Figure 14-4294. CTSET2_CFG_CTFILT25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8644. CTSET2_CFG_CTFILT25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.127 CTSET2_CFG_CTFILT26 Register

14.3.2.4.2.127.1 CTSET2_CFG_CTFILT26 Register (Offset = B68h) [reset = 0h]

Counter Timer 26 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8645. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B68h

Figure 14-4295. CTSET2_CFG_CTFILT26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8646. CTSET2_CFG_CTFILT26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.128 CTSET2_CFG_CTFILT27 Register

14.3.2.4.2.128.1 CTSET2_CFG_CTFILT27 Register (Offset = B6Ch) [reset = 0h]

Counter Timer 27 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8647. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B6Ch

Figure 14-4296. CTSET2_CFG_CTFILT27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8648. CTSET2_CFG_CTFILT27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.129 CTSET2_CFG_CTFILT28 Register

14.3.2.4.2.129.1 CTSET2_CFG_CTFILT28 Register (Offset = B70h) [reset = 0h]

Counter Timer 28 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8649. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B70h

Figure 14-4297. CTSET2_CFG_CTFILT28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8650. CTSET2_CFG_CTFILT28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.130 CTSET2_CFG_CTFILT29 Register

14.3.2.4.2.130.1 CTSET2_CFG_CTFILT29 Register (Offset = B74h) [reset = 0h]

Counter Timer 29 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8651. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B74h

Figure 14-4298. CTSET2_CFG_CTFILT29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8652. CTSET2_CFG_CTFILT29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.131 CTSET2_CFG_CTFILT30 Register

14.3.2.4.2.131.1 CTSET2_CFG_CTFILT30 Register (Offset = B78h) [reset = 0h]

Counter Timer 30 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8653. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B78h

Figure 14-4299. CTSET2_CFG_CTFILT30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8654. CTSET2_CFG_CTFILT30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.132 CTSET2_CFG_CTFILT31 Register

14.3.2.4.2.132.1 CTSET2_CFG_CTFILT31 Register (Offset = B7Ch) [reset = 0h]

Counter Timer 31 Filter Register. These filters are only activated if the CTCRn : FILTER is set

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Table 14-8655. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B7Ch

Figure 14-4300. CTSET2_CFG_CTFILT31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SECSUPER	SECUSER	RSUPER	RUSER	NRSUPER	NRUSER	IDLE	FREE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8656. CTSET2_CFG_CTFILT31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7	SECSUPER	R/W	0h	Counter functions while system is in Secure-Supervisor mode
6	SECUSER	R/W	0h	Counter functions while system is in Secure-User mode
5	RSUPER	R/W	0h	Counter functions while system is in Root-Supervisor node
4	RUSER	R/W	0h	Counter functions while system is in Root-User mode
3	NRSUPER	R/W	0h	Counter functions while system is in Non-Root-Supervisor mode
2	NRUSER	R/W	0h	Counter functions while system is in in Non-Root-User mode
1	IDLE	R/W	0h	Counter functions while system/core is in idle
0	FREE	R/W	0h	Counter functions while system/core is halted

14.3.2.4.2.133 CTSET2_CFG_CTCNTR0 Register

14.3.2.4.2.133.1 CTSET2_CFG_CTCNTR0 Register (Offset = B80h) [reset = 0h]

Counter Timer Counter Register 0

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Table 14-8657. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B80h

Figure 14-4301. CTSET2_CFG_CTCNTR0 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 14-8658. CTSET2_CFG_CTCNTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.134 CTSET2_CFG_CTCNTR1 Register

14.3.2.4.2.134.1 CTSET2_CFG_CTCNTR1 Register (Offset = B84h) [reset = 0h]

Counter Timer Counter Register 1

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Table 14-8659. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B84h

Figure 14-4302. CTSET2_CFG_CTCNTR1 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8660. CTSET2_CFG_CTCNTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.135 CTSET2_CFG_CTCNTR2 Register

14.3.2.4.2.135.1 CTSET2_CFG_CTCNTR2 Register (Offset = B88h) [reset = 0h]

Counter Timer Counter Register 2

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Table 14-8661. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B88h

Figure 14-4303. CTSET2_CFG_CTCNTR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8662. CTSET2_CFG_CTCNTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.136 CTSET2_CFG_CTCNTR3 Register

14.3.2.4.2.136.1 CTSET2_CFG_CTCNTR3 Register (Offset = B8Ch) [reset = 0h]

Counter Timer Counter Register 3

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Table 14-8663. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B8Ch

Figure 14-4304. CTSET2_CFG_CTCNTR3 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8664. CTSET2_CFG_CTCNTR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.137 CTSET2_CFG_CTCNTR4 Register

14.3.2.4.2.137.1 CTSET2_CFG_CTCNTR4 Register (Offset = B90h) [reset = 0h]

Counter Timer Counter Register 4

Return to Summary Table

Table 14-8665. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B90h

Figure 14-4305. CTSET2_CFG_CTCNTR4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8666. CTSET2_CFG_CTCNTR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.138 CTSET2_CFG_CTCNTR5 Register

14.3.2.4.2.138.1 CTSET2_CFG_CTCNTR5 Register (Offset = B94h) [reset = 0h]

Counter Timer Counter Register 5

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Table 14-8667. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B94h

Figure 14-4306. CTSET2_CFG_CTCNTR5 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8668. CTSET2_CFG_CTCNTR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.139 CTSET2_CFG_CTCNTR6 Register

14.3.2.4.2.139.1 CTSET2_CFG_CTCNTR6 Register (Offset = B98h) [reset = 0h]

Counter Timer Counter Register 6

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Table 14-8669. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B98h

Figure 14-4307. CTSET2_CFG_CTCNTR6 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8670. CTSET2_CFG_CTCNTR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.140 CTSET2_CFG_CTCNTR7 Register

14.3.2.4.2.140.1 CTSET2_CFG_CTCNTR7 Register (Offset = B9Ch) [reset = 0h]

Counter Timer Counter Register 7

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Table 14-8671. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8B9Ch

Figure 14-4308. CTSET2_CFG_CTCNTR7 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8672. CTSET2_CFG_CTCNTR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.141 CTSET2_CFG_CTCNTR8 Register

14.3.2.4.2.141.1 CTSET2_CFG_CTCNTR8 Register (Offset = BA0h) [reset = 0h]

Counter Timer Counter Register 8

Return to Summary Table

Table 14-8673. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BA0h

Figure 14-4309. CTSET2_CFG_CTCNTR8 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8674. CTSET2_CFG_CTCNTR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.142 CTSET2_CFG_CTCNTR9 Register

14.3.2.4.2.142.1 CTSET2_CFG_CTCNTR9 Register (Offset = BA4h) [reset = 0h]

Counter Timer Counter Register 9

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Table 14-8675. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BA4h

Figure 14-4310. CTSET2_CFG_CTCNTR9 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8676. CTSET2_CFG_CTCNTR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.143 CTSET2_CFG_CTCNTR10 Register

14.3.2.4.2.143.1 CTSET2_CFG_CTCNTR10 Register (Offset = BA8h) [reset = 0h]

Counter Timer Counter Register 10

Return to Summary Table

Table 14-8677. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BA8h

Figure 14-4311. CTSET2_CFG_CTCNTR10 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8678. CTSET2_CFG_CTCNTR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.144 CTSET2_CFG_CTCNTR11 Register

14.3.2.4.2.144.1 CTSET2_CFG_CTCNTR11 Register (Offset = BACh) [reset = 0h]

Counter Timer Counter Register 11

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Table 14-8679. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BACh

Figure 14-4312. CTSET2_CFG_CTCNTR11 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8680. CTSET2_CFG_CTCNTR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.145 CTSET2_CFG_CTCNTR12 Register

14.3.2.4.2.145.1 CTSET2_CFG_CTCNTR12 Register (Offset = BB0h) [reset = 0h]

Counter Timer Counter Register 12

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Table 14-8681. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BB0h

Figure 14-4313. CTSET2_CFG_CTCNTR12 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8682. CTSET2_CFG_CTCNTR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.146 CTSET2_CFG_CTCNTR13 Register

14.3.2.4.2.146.1 CTSET2_CFG_CTCNTR13 Register (Offset = BB4h) [reset = 0h]

Counter Timer Counter Register 13

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Table 14-8683. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BB4h

Figure 14-4314. CTSET2_CFG_CTCNTR13 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 14-8684. CTSET2_CFG_CTCNTR13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.147 CTSET2_CFG_CTCNTR14 Register

14.3.2.4.2.147.1 CTSET2_CFG_CTCNTR14 Register (Offset = BB8h) [reset = 0h]

Counter Timer Counter Register 14

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Table 14-8685. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BB8h

Figure 14-4315. CTSET2_CFG_CTCNTR14 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8686. CTSET2_CFG_CTCNTR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.148 CTSET2_CFG_CTCNTR15 Register

14.3.2.4.2.148.1 CTSET2_CFG_CTCNTR15 Register (Offset = BBCh) [reset = 0h]

Counter Timer Counter Register 15

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Table 14-8687. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BBCh

Figure 14-4316. CTSET2_CFG_CTCNTR15 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8688. CTSET2_CFG_CTCNTR15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.149 CTSET2_CFG_CTCNTR16 Register

14.3.2.4.2.149.1 CTSET2_CFG_CTCNTR16 Register (Offset = BC0h) [reset = 0h]

Counter Timer Counter Register 16

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Table 14-8689. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BC0h

Figure 14-4317. CTSET2_CFG_CTCNTR16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8690. CTSET2_CFG_CTCNTR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.150 CTSET2_CFG_CTCNTR17 Register

14.3.2.4.2.150.1 CTSET2_CFG_CTCNTR17 Register (Offset = BC4h) [reset = 0h]

Counter Timer Counter Register 17

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Table 14-8691. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BC4h

Figure 14-4318. CTSET2_CFG_CTCNTR17 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8692. CTSET2_CFG_CTCNTR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.151 CTSET2_CFG_CTCNTR18 Register

14.3.2.4.2.151.1 CTSET2_CFG_CTCNTR18 Register (Offset = BC8h) [reset = 0h]

Counter Timer Counter Register 18

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Table 14-8693. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BC8h

Figure 14-4319. CTSET2_CFG_CTCNTR18 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8694. CTSET2_CFG_CTCNTR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.152 CTSET2_CFG_CTCNTR19 Register

14.3.2.4.2.152.1 CTSET2_CFG_CTCNTR19 Register (Offset = BCCh) [reset = 0h]

Counter Timer Counter Register 19

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Table 14-8695. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BCCh

Figure 14-4320. CTSET2_CFG_CTCNTR19 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8696. CTSET2_CFG_CTCNTR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.153 CTSET2_CFG_CTCNTR20 Register

14.3.2.4.2.153.1 CTSET2_CFG_CTCNTR20 Register (Offset = BD0h) [reset = 0h]

Counter Timer Counter Register 20

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Table 14-8697. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BD0h

Figure 14-4321. CTSET2_CFG_CTCNTR20 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8698. CTSET2_CFG_CTCNTR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.154 CTSET2_CFG_CTCNTR21 Register

14.3.2.4.2.154.1 CTSET2_CFG_CTCNTR21 Register (Offset = BD4h) [reset = 0h]

Counter Timer Counter Register 21

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Table 14-8699. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BD4h

Figure 14-4322. CTSET2_CFG_CTCNTR21 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8700. CTSET2_CFG_CTCNTR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.155 CTSET2_CFG_CTCNTR22 Register

14.3.2.4.2.155.1 CTSET2_CFG_CTCNTR22 Register (Offset = BD8h) [reset = 0h]

Counter Timer Counter Register 22

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Table 14-8701. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BD8h

Figure 14-4323. CTSET2_CFG_CTCNTR22 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8702. CTSET2_CFG_CTCNTR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.156 CTSET2_CFG_CTCNTR23 Register

14.3.2.4.2.156.1 CTSET2_CFG_CTCNTR23 Register (Offset = BDCh) [reset = 0h]

Counter Timer Counter Register 23

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Table 14-8703. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BDCh

Figure 14-4324. CTSET2_CFG_CTCNTR23 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8704. CTSET2_CFG_CTCNTR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.157 CTSET2_CFG_CTCNTR24 Register

14.3.2.4.2.157.1 CTSET2_CFG_CTCNTR24 Register (Offset = BE0h) [reset = 0h]

Counter Timer Counter Register 24

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Table 14-8705. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BE0h

Figure 14-4325. CTSET2_CFG_CTCNTR24 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8706. CTSET2_CFG_CTCNTR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.158 CTSET2_CFG_CTCNTR25 Register

14.3.2.4.2.158.1 CTSET2_CFG_CTCNTR25 Register (Offset = BE4h) [reset = 0h]

Counter Timer Counter Register 25

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Table 14-8707. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BE4h

Figure 14-4326. CTSET2_CFG_CTCNTR25 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8708. CTSET2_CFG_CTCNTR25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.159 CTSET2_CFG_CTCNTR26 Register

14.3.2.4.2.159.1 CTSET2_CFG_CTCNTR26 Register (Offset = BE8h) [reset = 0h]

Counter Timer Counter Register 26

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Table 14-8709. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BE8h

Figure 14-4327. CTSET2_CFG_CTCNTR26 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8710. CTSET2_CFG_CTCNTR26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.160 CTSET2_CFG_CTCNTR27 Register

14.3.2.4.2.160.1 CTSET2_CFG_CTCNTR27 Register (Offset = BECh) [reset = 0h]

Counter Timer Counter Register 27

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Table 14-8711. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BECh

Figure 14-4328. CTSET2_CFG_CTCNTR27 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8712. CTSET2_CFG_CTCNTR27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.161 CTSET2_CFG_CTCNTR28 Register

14.3.2.4.2.161.1 CTSET2_CFG_CTCNTR28 Register (Offset = BF0h) [reset = 0h]

Counter Timer Counter Register 28

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Table 14-8713. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BF0h

Figure 14-4329. CTSET2_CFG_CTCNTR28 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8714. CTSET2_CFG_CTCNTR28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.162 CTSET2_CFG_CTCNTR29 Register

14.3.2.4.2.162.1 CTSET2_CFG_CTCNTR29 Register (Offset = BF4h) [reset = 0h]

Counter Timer Counter Register 29

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Table 14-8715. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BF4h

Figure 14-4330. CTSET2_CFG_CTCNTR29 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8716. CTSET2_CFG_CTCNTR29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.163 CTSET2_CFG_CTCNTR30 Register

14.3.2.4.2.163.1 CTSET2_CFG_CTCNTR30 Register (Offset = BF8h) [reset = 0h]

Counter Timer Counter Register 30

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Table 14-8717. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BF8h

Figure 14-4331. CTSET2_CFG_CTCNTR30 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8718. CTSET2_CFG_CTCNTR30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.164 CTSET2_CFG_CTCNTR31 Register

14.3.2.4.2.164.1 CTSET2_CFG_CTCNTR31 Register (Offset = BFCh) [reset = 0h]

Counter Timer Counter Register 31

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Table 14-8719. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8BFCh

Figure 14-4332. CTSET2_CFG_CTCNTR31 Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-8720. CTSET2_CFG_CTCNTR31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	This field reflects the current value of the counter. It is incremented when the system events configured in the corresponding Counter Control Register is asserted. If CTCRn.CHNSHD is set, the Counter will increment when the low order counter rolls over.

14.3.2.4.2.165 CTSET2_CFG_CT_EOI Register

14.3.2.4.2.165.1 CTSET2_CFG_CT_EOI Register (Offset = C00h) [reset = 0h]

Counter Timer EOI Register. This register is the End of Interrupt used by SW to signal HW that an interrupt event service is complete and an interrupt can be rearmed. This register exists only if NUMTIMR > 0

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Table 14-8721. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8C00h

Figure 14-4333. CTSET2_CFG_CT_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI
R							R/W
0h							0h

Table 14-8722. CTSET2_CFG_CT_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	EOI	R/W	0h	EOI value

14.3.2.4.2.166 CTSET2_CFG_CTIRQSTAT_RAW Register

14.3.2.4.2.166.1 CTSET2_CFG_CTIRQSTAT_RAW Register (Offset = C04h) [reset = 0h]

Counter Timer IRQSTATUS RAW Register. This register indicates the raw status of the interrupt. It can be written by SW for testing. This register exists only if NUMTIMR > 0

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Table 14-8723. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8C04h

Figure 14-4334. CTSET2_CFG_CTIRQSTAT_RAW Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IRQ							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IRQ							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IRQ							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IRQ							
R/W							
0h							

Table 14-8724. CTSET2_CFG_CTIRQSTAT_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IRQ	R/W	0h	IRQSTATUS_RAW value. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.3.2.4.2.167 CTSET2_CFG_CTIRQSTAT Register

14.3.2.4.2.167.1 CTSET2_CFG_CTIRQSTAT Register (Offset = C08h) [reset = 0h]

Counter Timer IRQSTATUS Register. This bit clears the interrupt event. SW can also read this bit to indicate that the interrupt is active and enabled. This register exists only if NUMTIMR > 0

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Table 14-8725. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8C08h

Figure 14-4335. CTSET2_CFG_CTIRQSTAT Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IE							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IE							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IE							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IE							
R/W							
0h							

Table 14-8726. CTSET2_CFG_CTIRQSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IE	R/W	0h	IRQSTATUS value. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.3.2.4.2.168 CTSET2_CFG_CTIRQENABLE_SET Register

14.3.2.4.2.168.1 CTSET2_CFG_CTIRQENABLE_SET Register (Offset = C0Ch) [reset = 0h]

Counter Timer IRQENABLE_SET Register. This register is to enable generation of Interrupt Event used by SW. This register exists only if NUMTIMR > 0

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Table 14-8727. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8C0Ch

Figure 14-4336. CTSET2_CFG_CTIRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
TIM_INTN_IES							
R/W							
0h							
23	22	21	20	19	18	17	16
TIM_INTN_IES							
R/W							
0h							
15	14	13	12	11	10	9	8
TIM_INTN_IES							
R/W							
0h							
7	6	5	4	3	2	1	0
TIM_INTN_IES							
R/W							
0h							

Table 14-8728. CTSET2_CFG_CTIRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IES	R/W	0h	IRQSET value. This bit sets the enable of the interrupt event. SW can also read this bit to determine if the interrupt is enabled. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.3.2.4.2.169 CTSET2_CFG_CTIRQENABLE_CLR Register

14.3.2.4.2.169.1 CTSET2_CFG_CTIRQENABLE_CLR Register (Offset = C10h) [reset = 0h]

Counter Timer IRQENABLE_CLR Register. This register is to disable generation of Interrupt Event used by SW. This register exists only if NUMTIMR > 0

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Table 14-8729. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 8C10h

Figure 14-4337. CTSET2_CFG_CTIRQENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TIM_INTN_IEC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TIM_INTN_IEC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TIM_INTN_IEC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TIM_INTN_IEC</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8730. CTSET2_CFG_CTIRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIM_INTN_IEC	R/W	0h	IRQCLR value. This bit clears the enable of the interrupt event. SW can also read this bit to determine if the interrupt is enabled. The individual bits is this field correspond to individual interrupts generated for each timer associated with Counter Timer Control Register (CTCRn : INT).

14.3.2.4.2.170 CTSET2_CFG_STPTCR Register

14.3.2.4.2.170.1 CTSET2_CFG_STPTCR Register (Offset = 1800h) [reset = 4h]

STP Trace Control Register

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Table 14-8731. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 9800h

Figure 14-4338. CTSET2_CFG_STPTCR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED3</td><td>MOD_FIFOFULL</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>DATA_FIFOFULL</td><td colspan="7">RESERVED2</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED2</td><td>COMPEN</td><td colspan="2">RESERVED1</td><td>SYNCEN</td><td>TSEN</td><td>RESERVED</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="2">R</td><td>R</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="2">0h</td><td>1h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8732. CTSET2_CFG_STPTCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED3	R	0h	Reserved, returns 0
24	MOD_FIFOFULL	R	0h	STPMI2ATB internal MID packet fifo is full
23	DATA_FIFOFULL	R	0h	STPMI2ATB internal Data packet fifo is full
22:6	RESERVED2	R	0h	Reserved, returns 0
5	COMPEN	R/W	0h	Compression of Data enable
4:3	RESERVED1	R	0h	Reserved, returns 0
2	SYNCEN	R	1h	The value 1 indicates STPASYNC is supported
1	TSEN	R/W	0h	Timestamp Enable. This bit is static and should not be changed dynamically. This should be changed before client is enabled.
0	RESERVED	R	0h	Reserved, returns 0

14.3.2.4.2.171 CTSET2_CFG_STPTID Register

14.3.2.4.2.171.1 CTSET2_CFG_STPTID Register (Offset = 1804h) [reset = 0h]

STP Trace ID Register

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Table 14-8733. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 9804h

Figure 14-4339. CTSET2_CFG_STPTID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	TRACEID					
R	NONE	R/W					
0h	0h	0h					

Table 14-8734. CTSET2_CFG_STPTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6	RESERVED	NONE	0h	Reserved
5:0	TRACEID	R/W	0h	Trace ID value. Software may overwrite the value at any time, but this is only recommended for scenarios where top-level configuration errors result in a collision between HW master IDs

14.3.2.4.2.172 CTSET2_CFG_STPASYNC Register

14.3.2.4.2.172.1 CTSET2_CFG_STPASYNC Register (Offset = 1810h) [reset = 130Ch]

STP Synchronization Control Register

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Table 14-8735. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 9810h

Figure 14-4340. CTSET2_CFG_STPASYNC Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED			EXPMODE	COUNT			
R			R/W	R/W			
0h			1h	30Ch			
7	6	5	4	3	2	1	0
COUNT							
R/W							
30Ch							

Table 14-8736. CTSET2_CFG_STPASYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	R	0h	Reserved, returns 0
12	EXPMODE	R/W	1h	Exponent mode, A value of 1 sets count to 2 to the Nth, where Nth is ((bits 11 : 8)+12). A value of 0 sets Count to N (bits 11 : 0)
11:0	COUNT	R/W	30Ch	The number of bytes between Synchronization packets

14.3.2.4.2.173 CTSET2_CFG_STPFFCR Register

14.3.2.4.2.173.1 CTSET2_CFG_STPFFCR Register (Offset = 1814h) [reset = 0h]

STP Flush Control Register

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Table 14-8737. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 9814h

Figure 14-4341. CTSET2_CFG_STPFFCR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1		FORCEFLUSH	RESERVED			ASYNCPE	AUTOFLUSH
R		R/W	R			R/W	R/W
0h		0h	0h			0h	0h

Table 14-8738. CTSET2_CFG_STPFFCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED1	R	0h	Reserved, returns 0
5	FORCEFLUSH	R/W	0h	Write a 1 to force a flush, automatically clears after the operation is complete
4:2	RESERVED	R	0h	Reserved, returns 0
1	ASYNCPE	R/W	0h	Async Priority Enable. 0 indicates ASYNC packet priority is lower than trace. 1 indicates priority escalates on second synchronization request
0	AUTOFLUSH	R/W	0h	Auto flush enable. When set, on every complete data (ATDATA : WIDTH) in the fifo written, data is exported out when ATREADY is asserted. This should be written before client IP enabled

14.3.2.4.2.174 CTSET2_CFG_STPFEAT1 Register

14.3.2.4.2.174.1 CTSET2_CFG_STPFEAT1 Register (Offset = 1818h) [reset = 21h]

STP Features 1 Register

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Table 14-8739. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3800 9818h

Figure 14-4342. CTSET2_CFG_STPFEAT1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">STP_RTLVER</td><td colspan="3">STP_MAJVER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">STP_CUSTVER</td><td colspan="5">STP_MINVER</td><td>RESERVED</td></tr>
<tr><td colspan="2">R</td><td colspan="5">R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">VERSION</td><td colspan="4">PROT</td></tr>
<tr><td>NONE</td><td colspan="3">R</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td colspan="3">2h</td><td colspan="4">1h</td></tr>
</table>

Table 14-8740. CTSET2_CFG_STPFEAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	STP_RTLVER	R	0h	RTL Version. Reset each time major or minor version is updated
26:24	STP_MAJVER	R	0h	Functional Major Version. This is the first version of STPMI2ATB
23:22	STP_CUSTVER	R	0h	Custom Version (not used)
21:17	STP_MINVER	R	0h	Functional Minor Version
16:8	RESERVED	R	0h	Reserved, returns 0
7	RESERVED	NONE	0h	Reserved
6:4	VERSION	R	2h	STP2.0 Time Stamp, Value of 011 indicates Natural binary timestamp, a value of 100 indicates gray binary timestamps
3:0	PROT	R	1h	Protocol Revision. Value of 0001 indicates STP 2.0

14.3.2.4.2.175 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Register

14.3.2.4.2.175.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Register (Offset = 0h) [reset = 4h]

This register contains the control and status settings for STP Trace control register. MID_Fifofull indicates status of internal Master/Channel Fifo as full. Data_Fifofull indicates the status of internal Data Fifo as full. It is possible that if MID_Fifofull is full and when new master_id is seen on STPMI i/f, the data will not be accepted as MID is full. It will wait for MID to be read out corresponding to Data.

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Table 14-8741. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3804 0100h

Figure 14-4343. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RSVD3</td><td>MID_FIFO_FUL</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>DATA_FIFO_FULL</td><td colspan="7">RSVD2</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RSVD2</td><td>COMPEN</td><td colspan="2">RSVD1</td><td>SNCEN</td><td>TSEN</td><td>RSVD0</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="2">R</td><td>R</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="2">0h</td><td>1h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8742. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RSVD3	R	0h	reserved
24	MID_FIFO_FUL	R	0h	'1' indicates STPMI2ATB internal MID packet fifo is full
23	DATA_FIFO_FULL	R	0h	'1' indicates STPMI2ATB internal Data packet fifo is full
22:6	RSVD2	R	0h	reserved
5	COMPEN	R/W	0h	Compression Enable: '1' Enables compression of data. '0' disables data compress.
4:3	RSVD1	R	0h	reserved
2	SNCEN	R	1h	ASYNC Enable: 1 indicates STPASYNC is supported. 0 indicates STPASYNC is not supported.
1	TSEN	R/W	0h	Timestamp Enable: 1 enables Timestamp. 0 disables Timestamp (it includes only a nibble TS, when disabled and a time-stamp is indicated on STPMI interface). This bit is static and should not be changed dynamically. This should be changed before client is enabled. The first TS packet sent out after ASYNC export will have either 64/48 (based on TSMAXWIDTH) bit timestamp and followed by only 4 bit Timestamp for TS packets.

Table 14-8742. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RSVD0	R	0h	reserved

14.3.2.4.2.176 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID Register

14.3.2.4.2.176.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID Register (Offset = 4h) [reset = 0h]

This register contains the trace id register settings. This value is sampled from input and is exported on ATB interface as ATID field. This is usually programmed only when top-level configuration errors results in collision between ID's.

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Table 14-8743. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3804 0104h

Figure 14-4344. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RSVD</td><td colspan="7">TRACEID</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-8744. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_TRACE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	reserved
6:0	TRACEID	R/W	0h	Traceid [6:0] value that is forwarded on the ATID interface for all transactions from the Trace Aggreator. The reset value is determined by a tieoff to STPMI2ATB and should be tied to 0000000b internal to the Trace Aggregator. SW must set this to a unique value in the the ATB ID address space to prevent collisions with other ATB sources.

14.3.2.4.2.177 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL Register

14.3.2.4.2.177.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL Register (Offset = 10h) [reset = 1780h]

This register contains the periodic interval after which an ASYNC packet is exported over ATB interface. This counter register controls the interval between synchronization packets. The number of bytes between which a sync packet is sent based on this counter value. Writing a value of 0x0 disables the synchronization counter, however if the client has any other synchronization scheme, that will continue to operate. When this register is written, STPMI2ATB will immediately perform synchronization and reset the counter value to the newly programmed value ensuring subsequent synchronization occurs in the period programmed. This async requests will result in a Master switch. A async request will result in async packet followed by VERSION packet which is followed by a new M8/C8 packet before any Dx packet is sent.

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Table 14-8745. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3804 0110h

Figure 14-4345. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD			MODE	COUNT			
R			R/W	R/W			
0h			1h	780h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
780h							

Table 14-8746. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_SYNC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RSVD	R	0h	reserved
12	MODE	R/W	1h	Sync Count Mode: 1 indicates SYNC is 2N bytes N being derived from 11:7, value being between 12 and 27 inclusive 0 indicates N, where N is number of bytes between the ASYNC packets Counter = 2^ N, where [N = 2^m, m=11:7, 12 and 27 inclusive] (mode =1) Counter = N, where [N = 11:0] (mode =0)
11:0	COUNT	R/W	780h	Period Count: Counts the number of bytes between Synchronization packets.

14.3.2.4.2.178 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL Register

14.3.2.4.2.178.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL Register (Offset = 14h) [reset = 1Ch]

This register contains the bits to indicate flush in STPMI2ATB. It also controls priority control for other conditions in STPMI2ATB.

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Table 14-8747. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3804 0114h

Figure 14-4346. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD1		FORCE_FLUSH	RSVD0			ASYNC_PE	AUTO_FLUSH
R		R/W	R			R/W	R/W
0h		0h	7h			0h	0h

Table 14-8748. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FLUSH_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RSVD1	R	0h	reserved
5	FORCE_FLUSH	R/W	0h	Forces a flush operation: 1 indicates force a flush, automatically clears after the operation is complete. Refer to 2.10. A '0' is not a valid value to be written at any point of time. It will be ignored. This flush will happen only after any current flush on ATB boundary is completed.
4:2	RSVD0	R	7h	reserved
1	ASYNC_PE	R/W	0h	ASYNC Sequence Priority Enable: 0 indicates ASYNC packet priority is lower than normal trace. 1 indicates priority escalates on second synchronization request
0	AUTO_FLUSH	R/W	0h	Enable ATB Auto-flush: 0 indicates auto flush disabled. 1 indicates auto flush enabled. On every complete data (ATDATA:WIDTH) in the fifo written, data is exported out when ATREADY is asserted. This needs to be written only once before client IP enabled.

14.3.2.4.2.179 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES Register

14.3.2.4.2.179.1 C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES Register (Offset = 18h) [reset = 41h]

This register contains the bits to indicate the features implemented in STPMI2ATB. It shows the VERSION packet implemented based on STP2.0 type of encoding timestamp packet. It also indicates what protocol is followed in the IP.

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Table 14-8749. Instance Table

Instance Name	Physical Address
C7X256V1_DEBUG	0007 3804 0118h

Figure 14-4347. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD	STP_TS_VERSION			PROT			
R	R			R			
0h	4h			1h			

Table 14-8750. C7X256V_DEBUG_DBG_AGR0_MEM_CFG_STP_FEATURES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	rsvd
6:4	STP_TS_VERSION	R	4h	Timestamp Version 3 = STP2.0 with Natural binary STP2.0 timestamps. 4 = STP2.0 with Gray STP2.0 timestamps.
3:0	PROT	R	1h	Protocol Version: 0001 indicates STP2.0 protocol

14.3.2.5 C7X256V_ECC_AGGR

C7X256V_ECC_AGGR

14.3.2.5.1 C7X256V_ECC_AGGR Summaries

C7X256V_ECC_AGGR Summaries

Table 14-8751. ECC_AGGR Registers, Base Address=0071 A000h, Length=1024

Offset	Length	Register Name	C7X256V0_ECC_AGGR Physical Address	C7X256V1_ECC_AGGR Physical Address
0h	32	ECC_AGGR_REV	0071 A000h	0071 B000h
8h	32	ECC_AGGR_VECTOR	0071 A008h	0071 B008h
Ch	32	ECC_AGGR_STAT	0071 A00Ch	0071 B00Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 A010h + formula	0071 B010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 A03Ch	0071 B03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 A040h	0071 B040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 A080h	0071 B080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 A0C0h	0071 B0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 A13Ch	0071 B13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 A140h	0071 B140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 A180h	0071 B180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 A1C0h	0071 B1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 A200h	0071 B200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 A204h	0071 B204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 A208h	0071 B208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 A20Ch	0071 B20Ch

14.3.2.5.2 C7X256V_ECC_AGGR Registers

C7X256V_ECC_AGGR Registers

14.3.2.5.2.1 ECC_AGGR_REV Register

14.3.2.5.2.1.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-8752. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A000h
C7X256V1_ECC_AGGR	0071 B000h

Figure 14-4348. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-8753. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.3.2.5.2.2 ECC_AGGR_VECTOR Register

14.3.2.5.2.2.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-8754. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A008h
C7X256V1_ECC_AGGR	0071 B008h

Figure 14-4349. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-8755. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.3.2.5.2.3 ECC_AGGR_STAT Register

14.3.2.5.2.3.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 8h]

Misc Status

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Table 14-8756. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A00Ch
C7X256V1_ECC_AGGR	0071 B00Ch

Figure 14-4350. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
</table>

Table 14-8757. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	8h	Indicates the number of RAMS serviced by the ECC aggregator

14.3.2.5.2.4 ECC_AGGR_RESERVED_SVBUS_J Register

14.3.2.5.2.4.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-8758. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A010h + formula
C7X256V1_ECC_AGGR	0071 B010h + formula

Figure 14-4351. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-8759. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.3.2.5.2.5 ECC_AGGR_SEC_EOI_REG Register

14.3.2.5.2.5.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-8760. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A03Ch
C7X256V1_ECC_AGGR	0071 B03Ch

Figure 14-4352. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-8761. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.2.5.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

14.3.2.5.2.6.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-8762. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A040h
C7X256V1_ECC_AGGR	0071 B040h

Figure 14-4353. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EL2_RAM_EDC_CTL_BUSSEC_PEND	CLEC_SRAM_RAMECC_PEND	DRU_RING_EDC_PEND	DRU_RD_BUF_EDC_PEND	DRU_QUEUE_EDC_PEND	DMC_DATA_CTL_BUSECC_PEND	DMC_TAG_CTL_BUSECC_PEND	PMC_BUSECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8763. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EL2_RAM_EDC_CTL_BUSSEC_PEND	R/W1TS	0h	Interrupt Pending Status for el2_ram_edc_ctl_bussecc_pend
6	CLEC_SRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for clec_sram_ramecc_pend
5	DRU_RING_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for dru_ring_edc_pend
4	DRU_RD_BUF_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for dru_rd_buf_edc_pend
3	DRU_QUEUE_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for dru_queue_edc_pend
2	DMC_DATA_CTL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for dmc_data_ctl_busecc_pend
1	DMC_TAG_CTL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for dmc_tag_ctl_busecc_pend
0	PMC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for pmc_busecc_pend

14.3.2.5.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.3.2.5.2.7.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-8764. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A080h
C7X256V1_ECC_AGGR	0071 B080h

Figure 14-4354. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EL2_RAM_EDC_CTL_BUSSEC_ENABLE_SET	CLEC_SRAM_RAMECC_ENABLE_SET	DRU_RING_EDC_ENABLE_SET	DRU_RD_BUF_EDC_ENABLE_SET	DRU_QUEUE_EDC_ENABLE_SET	DMC_DATA_CTL_BUSECC_ENABLE_SET	DMC_TAG_CTL_BUSECC_ENABLE_SET	PMC_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8765. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EL2_RAM_EDC_CTL_BUSSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for el2_ram_edc_ctl_bussecc_pend
6	CLEC_SRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for clec_sram_ramecc_pend
5	DRU_RING_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dru_ring_edc_pend
4	DRU_RD_BUF_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dru_rd_buf_edc_pend
3	DRU_QUEUE_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dru_queue_edc_pend
2	DMC_DATA_CTL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dmc_data_ctl_busecc_pend
1	DMC_TAG_CTL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dmc_tag_ctl_busecc_pend
0	PMC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pmc_busecc_pend

14.3.2.5.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.3.2.5.2.8.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-8766. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A0C0h
C7X256V1_ECC_AGGR	0071 B0C0h

Figure 14-4355. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EL2_RAM_EDC_CTL_BUSSECC_ENABLE_CLR	CLEC_SRAM_RAMECC_ENABLE_CLR	DRU_RING_EDC_ENABLE_CLR	DRU_RD_BUF_EDC_ENABLE_CLR	DRU_QUEUE_EDC_ENABLE_CLR	DMC_DATA_CTL_BUSECC_ENABLE_CLR	DMC_TAG_CTL_BUSECC_ENABLE_CLR	PMC_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8767. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EL2_RAM_EDC_CTL_BUSSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for el2_ram_edc_ctl_bussecc_pend
6	CLEC_SRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for clec_sram_ramecc_pend
5	DRU_RING_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dru_ring_edc_pend
4	DRU_RD_BUF_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dru_rd_buf_edc_pend
3	DRU_QUEUE_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dru_queue_edc_pend
2	DMC_DATA_CTL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dmc_data_ctl_busecc_pend
1	DMC_TAG_CTL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dmc_tag_ctl_busecc_pend
0	PMC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pmc_busecc_pend

14.3.2.5.2.9 ECC_AGGR_DED_EOI_REG Register

14.3.2.5.2.9.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-8768. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A13Ch
C7X256V1_ECC_AGGR	0071 B13Ch

Figure 14-4356. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-8769. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.3.2.5.2.10 ECC_AGGR_DED_STATUS_REG0 Register

14.3.2.5.2.10.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-8770. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A140h
C7X256V1_ECC_AGGR	0071 B140h

Figure 14-4357. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EL2_RAM_EDC_CTL_BUSSEC C_PEND	CLEC_SRAM_RAMECC_PEN D	DRU_RING_ED C_PEND	DRU_RD_BUF _EDC_PEND	DRU_QUEUE_ EDC_PEND	DMC_DATA_CT L_BUSECC_PE ND	DMC_TAG_CT L_BUSECC_PE ND	PMC_BUSECC _PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8771. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EL2_RAM_EDC_CTL_BUSSECC_PEND	R/W1TS	0h	Interrupt Pending Status for el2_ram_edc_ctl_bussecc_pend
6	CLEC_SRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for clec_sram_ramecc_pend
5	DRU_RING_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for dru_ring_edc_pend
4	DRU_RD_BUF_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for dru_rd_buf_edc_pend
3	DRU_QUEUE_EDC_PEND	R/W1TS	0h	Interrupt Pending Status for dru_queue_edc_pend
2	DMC_DATA_CTL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for dmc_data_ctl_busecc_pend
1	DMC_TAG_CTL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for dmc_tag_ctl_busecc_pend
0	PMC_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for pmc_busecc_pend

14.3.2.5.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.3.2.5.2.11.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-8772. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A180h
C7X256V1_ECC_AGGR	0071 B180h

Figure 14-4358. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EL2_RAM_EDC_CTL_BUSSEC_ENABLE_SET	CLEC_SRAM_RAMECC_ENABLE_SET	DRU_RING_EDC_ENABLE_SET	DRU_RD_BUF_EDC_ENABLE_SET	DRU_QUEUE_EDC_ENABLE_SET	DMC_DATA_CTL_BUSECC_ENABLE_SET	DMC_TAG_CTL_BUSECC_ENABLE_SET	PMC_BUSECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8773. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EL2_RAM_EDC_CTL_BUSSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for el2_ram_edc_ctl_bussecc_pend
6	CLEC_SRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for clec_sram_ramecc_pend
5	DRU_RING_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dru_ring_edc_pend
4	DRU_RD_BUF_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dru_rd_buf_edc_pend
3	DRU_QUEUE_EDC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dru_queue_edc_pend
2	DMC_DATA_CTL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dmc_data_ctl_busecc_pend
1	DMC_TAG_CTL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dmc_tag_ctl_busecc_pend
0	PMC_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pmc_busecc_pend

14.3.2.5.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.3.2.5.2.12.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-8774. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A1C0h
C7X256V1_ECC_AGGR	0071 B1C0h

Figure 14-4359. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EL2_RAM_EDC_CTL_BUSSEC C_ENABLE_CLR	CLEC_SRAM_RAMECC_ENABLE_CLR	DRU_RING_EDC_ENABLE_CLR	DRU_RD_BUF_EDC_ENABLE_CLR	DRU_QUEUE_EDC_ENABLE_CLR	DMC_DATA_CTL_BUSECC_ENABLE_CLR	DMC_TAG_CTL_BUSECC_ENABLE_CLR	PMC_BUSECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8775. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EL2_RAM_EDC_CTL_BUSSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for el2_ram_edc_ctl_bussecc_pend
6	CLEC_SRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for clec_sram_ramecc_pend
5	DRU_RING_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dru_ring_edc_pend
4	DRU_RD_BUF_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dru_rd_buf_edc_pend
3	DRU_QUEUE_EDC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dru_queue_edc_pend
2	DMC_DATA_CTL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dmc_data_ctl_busecc_pend
1	DMC_TAG_CTL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dmc_tag_ctl_busecc_pend
0	PMC_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pmc_busecc_pend

14.3.2.5.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

14.3.2.5.2.13.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-8776. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A200h
C7X256V1_ECC_AGGR	0071 B200h

Figure 14-4360. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-8777. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.3.2.5.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

14.3.2.5.2.14.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-8778. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A204h
C7X256V1_ECC_AGGR	0071 B204h

Figure 14-4361. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-8779. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.3.2.5.2.15 ECC_AGGR_AGGR_STATUS_SET Register

14.3.2.5.2.15.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-8780. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A208h
C7X256V1_ECC_AGGR	0071 B208h

Figure 14-4362. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-8781. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.3.2.5.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

14.3.2.5.2.16.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-8782. Instance Table

Instance Name	Physical Address
C7X256V0_ECC_AGGR	0071 A20Ch
C7X256V1_ECC_AGGR	0071 B20Ch

Figure 14-4363. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-8783. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.3.2.6 C7X256V_PBIST

C7X256V_PBIST

14.3.2.6.1 C7X256V_PBIST Summaries

C7X256V_PBIST Summaries

Table 14-8784. PBIST Registers, Base Address=0036 0000h, Length=1024

Offset	Length	Register Name	C7X256V0_PBIST Physical Address	C7X256V1_PBIST Physical Address
0h	32	PBIST_RF0L	0036 0000h	0037 0000h
4h	32	PBIST_RF1L	0036 0004h	0037 0004h
8h	32	PBIST_RF2L	0036 0008h	0037 0008h
Ch	32	PBIST_RF3L	0036 000Ch	0037 000Ch
10h	32	PBIST_RF4L	0036 0010h	0037 0010h
14h	32	PBIST_RF5L	0036 0014h	0037 0014h
18h	32	PBIST_RF6L	0036 0018h	0037 0018h
1Ch	32	PBIST_RF7L	0036 001Ch	0037 001Ch
20h	32	PBIST_RF8L	0036 0020h	0037 0020h
24h	32	PBIST_RF9L	0036 0024h	0037 0024h
28h	32	PBIST_RF10L	0036 0028h	0037 0028h
2Ch	32	PBIST_RF11L	0036 002Ch	0037 002Ch
30h	32	PBIST_RF12L	0036 0030h	0037 0030h
34h	32	PBIST_RF13L	0036 0034h	0037 0034h
38h	32	PBIST_RF14L	0036 0038h	0037 0038h
3Ch	32	PBIST_RF15L	0036 003Ch	0037 003Ch
40h	32	PBIST_RF0U	0036 0040h	0037 0040h
44h	32	PBIST_RF1U	0036 0044h	0037 0044h
48h	32	PBIST_RF2U	0036 0048h	0037 0048h
4Ch	32	PBIST_RF3U	0036 004Ch	0037 004Ch
50h	32	PBIST_RF4U	0036 0050h	0037 0050h
54h	32	PBIST_RF5U	0036 0054h	0037 0054h
58h	32	PBIST_RF6U	0036 0058h	0037 0058h
5Ch	32	PBIST_RF7U	0036 005Ch	0037 005Ch
60h	32	PBIST_RF8U	0036 0060h	0037 0060h
64h	32	PBIST_RF9U	0036 0064h	0037 0064h
68h	32	PBIST_RF10U	0036 0068h	0037 0068h
6Ch	32	PBIST_RF11U	0036 006Ch	0037 006Ch
70h	32	PBIST_RF12U	0036 0070h	0037 0070h
74h	32	PBIST_RF13U	0036 0074h	0037 0074h
78h	32	PBIST_RF14U	0036 0078h	0037 0078h
7Ch	32	PBIST_RF15U	0036 007Ch	0037 007Ch
100h	32	PBIST_A0	0036 0100h	0037 0100h
104h	32	PBIST_A1	0036 0104h	0037 0104h
108h	32	PBIST_A2	0036 0108h	0037 0108h
10Ch	32	PBIST_A3	0036 010Ch	0037 010Ch
110h	32	PBIST_L0	0036 0110h	0037 0110h
114h	32	PBIST_L1	0036 0114h	0037 0114h
118h	32	PBIST_L2	0036 0118h	0037 0118h

Table 14-8784. PBIST Registers, Base Address=0036 0000h, Length=1024 (continued)

Offset	Length	Register Name	C7X256V0_PBIST Physical Address	C7X256V1_PBIST Physical Address
11Ch	32	PBIST_L3	0036 011Ch	0037 011Ch
120h	32	PBIST_D	0036 0120h	0037 0120h
124h	32	PBIST_E	0036 0124h	0037 0124h
130h	32	PBIST_CA0	0036 0130h	0037 0130h
134h	32	PBIST_CA1	0036 0134h	0037 0134h
138h	32	PBIST_CA2	0036 0138h	0037 0138h
13Ch	32	PBIST_CA3	0036 013Ch	0037 013Ch
140h	32	PBIST_CL0	0036 0140h	0037 0140h
144h	32	PBIST_CL1	0036 0144h	0037 0144h
148h	32	PBIST_CL2	0036 0148h	0037 0148h
14Ch	32	PBIST_CL3	0036 014Ch	0037 014Ch
150h	32	PBIST_I0	0036 0150h	0037 0150h
154h	32	PBIST_I1	0036 0154h	0037 0154h
158h	32	PBIST_I2	0036 0158h	0037 0158h
15Ch	32	PBIST_I3	0036 015Ch	0037 015Ch
160h	32	PBIST_RAMT	0036 0160h	0037 0160h
164h	32	PBIST_DLR	0036 0164h	0037 0164h
168h	32	PBIST_CMS	0036 0168h	0037 0168h
16Ch	32	PBIST_STR	0036 016Ch	0037 016Ch
170h	64	PBIST_SCR	0036 0170h	0037 0170h
178h	32	PBIST_CSR	0036 0178h	0037 0178h
17Ch	32	PBIST_FDLY	0036 017Ch	0037 017Ch
180h	32	PBIST_PACT	0036 0180h	0037 0180h
184h	32	PBIST_PID	0036 0184h	0037 0184h
188h	32	PBIST_OVER	0036 0188h	0037 0188h
190h	64	PBIST_FSRF	0036 0190h	0037 0190h
198h	64	PBIST_FSRC	0036 0198h	0037 0198h
1A0h	64	PBIST_FSRA	0036 01A0h	0037 01A0h
1A8h	32	PBIST_FSRDL0	0036 01A8h	0037 01A8h
1B0h	32	PBIST_FSRDL1	0036 01B0h	0037 01B0h
1B4h	32	PBIST_MARGIN_MODE	0036 01B4h	0037 01B4h
1B8h	32	PBIST_WRENZ	0036 01B8h	0037 01B8h
1BCh	32	PBIST_PAGE_PGS	0036 01BCh	0037 01BCh
1C0h	32	PBIST_ROM	0036 01C0h	0037 01C0h
1C4h	32	PBIST_ALGO	0036 01C4h	0037 01C4h
1C8h	64	PBIST_RINFO	0036 01C8h	0037 01C8h

14.3.2.6.2 C7X256V_PBIST Registers

C7X256V_PBIST Registers

14.3.2.6.2.1 PBIST_RF0L Register

14.3.2.6.2.1.1 PBIST_RF0L Register (Offset = 0h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8785. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0000h
C7X256V1_PBIST	0037 0000h

Figure 14-4364. PBIST_RF0L Name Register

31	30	29	28	27	26	25	24
RF0L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF0L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF0L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF0L							
R/W							
0h							

Table 14-8786. PBIST_RF0L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF0L	R/W	0h	Register Files / Instruction Registers RF0 lower (RF0L) Reset Source: mod_g_rst_n

14.3.2.6.2.2 PBIST_RF1L Register

14.3.2.6.2.2.1 PBIST_RF1L Register (Offset = 4h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8787. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0004h
C7X256V1_PBIST	0037 0004h

Figure 14-4365. PBIST_RF1L Name Register

31	30	29	28	27	26	25	24
RF1L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF1L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF1L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF1L							
R/W							
0h							

Table 14-8788. PBIST_RF1L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF1L	R/W	0h	Register Files / Instruction Registers RF1 lower (RF1L) Reset Source: mod_g_rst_n

14.3.2.6.2.3 PBIST_RF2L Register

14.3.2.6.2.3.1 PBIST_RF2L Register (Offset = 8h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8789. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0008h
C7X256V1_PBIST	0037 0008h

Figure 14-4366. PBIST_RF2L Name Register

31	30	29	28	27	26	25	24
RF2L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF2L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF2L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF2L							
R/W							
0h							

Table 14-8790. PBIST_RF2L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF2L	R/W	0h	Register Files / Instruction Registers RF2 lower (RF2L) Reset Source: mod_g_rst_n

14.3.2.6.2.4 PBIST_RF3L Register

14.3.2.6.2.4.1 PBIST_RF3L Register (Offset = Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8791. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 000Ch
C7X256V1_PBIST	0037 000Ch

Figure 14-4367. PBIST_RF3L Name Register

31	30	29	28	27	26	25	24
RF3L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF3L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF3L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF3L							
R/W							
0h							

Table 14-8792. PBIST_RF3L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF3L	R/W	0h	Register Files / Instruction Registers RF3 lower (RF3L) Reset Source: mod_g_rst_n

14.3.2.6.2.5 PBIST_RF4L Register

14.3.2.6.2.5.1 PBIST_RF4L Register (Offset = 10h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8793. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0010h
C7X256V1_PBIST	0037 0010h

Figure 14-4368. PBIST_RF4L Name Register

31	30	29	28	27	26	25	24
RF4L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF4L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF4L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF4L							
R/W							
0h							

Table 14-8794. PBIST_RF4L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF4L	R/W	0h	Register Files / Instruction Registers RF4 lower (RF4L) Reset Source: mod_g_rst_n

14.3.2.6.2.6 PBIST_RF5L Register

14.3.2.6.2.6.1 PBIST_RF5L Register (Offset = 14h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8795. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0014h
C7X256V1_PBIST	0037 0014h

Figure 14-4369. PBIST_RF5L Name Register

31	30	29	28	27	26	25	24
RF5L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RF5L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RF5L							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RF5L							
R/W							
0h							

Table 14-8796. PBIST_RF5L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF5L	R/W	0h	Register Files / Instruction Registers RF5 lower (RF5L) Reset Source: mod_g_rst_n

14.3.2.6.2.7 PBIST_RF6L Register

14.3.2.6.2.7.1 PBIST_RF6L Register (Offset = 18h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8797. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0018h
C7X256V1_PBIST	0037 0018h

Figure 14-4370. PBIST_RF6L Name Register

31	30	29	28	27	26	25	24
RF6L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF6L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF6L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF6L							
R/W							
0h							

Table 14-8798. PBIST_RF6L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF6L	R/W	0h	Register Files / Instruction Registers RF6 lower (RF6L) Reset Source: mod_g_rst_n

14.3.2.6.2.8 PBIST_RF7L Register

14.3.2.6.2.8.1 PBIST_RF7L Register (Offset = 1Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8799. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 001Ch
C7X256V1_PBIST	0037 001Ch

Figure 14-4371. PBIST_RF7L Name Register

31	30	29	28	27	26	25	24
RF7L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF7L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF7L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF7L							
R/W							
0h							

Table 14-8800. PBIST_RF7L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF7L	R/W	0h	Register Files / Instruction Registers RF7 lower (RF7L) Reset Source: mod_g_rst_n

14.3.2.6.2.9 PBIST_RF8L Register

14.3.2.6.2.9.1 PBIST_RF8L Register (Offset = 20h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8801. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0020h
C7X256V1_PBIST	0037 0020h

Figure 14-4372. PBIST_RF8L Name Register

31	30	29	28	27	26	25	24
RF8L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF8L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF8L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF8L							
R/W							
0h							

Table 14-8802. PBIST_RF8L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF8L	R/W	0h	Register Files / Instruction Registers RF8 lower (RF8L) Reset Source: mod_g_rst_n

14.3.2.6.2.10 PBIST_RF9L Register

14.3.2.6.2.10.1 PBIST_RF9L Register (Offset = 24h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8803. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0024h
C7X256V1_PBIST	0037 0024h

Figure 14-4373. PBIST_RF9L Name Register

31	30	29	28	27	26	25	24
RF9L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RF9L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RF9L							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RF9L							
R/W							
0h							

Table 14-8804. PBIST_RF9L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF9L	R/W	0h	Register Files / Instruction Registers RF9 lower (RF9L) Reset Source: mod_g_rst_n

14.3.2.6.2.11 PBIST_RF10L Register

14.3.2.6.2.11.1 PBIST_RF10L Register (Offset = 28h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8805. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0028h
C7X256V1_PBIST	0037 0028h

Figure 14-4374. PBIST_RF10L Name Register

31	30	29	28	27	26	25	24
RF10L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF10L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF10L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF10L							
R/W							
0h							

Table 14-8806. PBIST_RF10L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF10L	R/W	0h	Register Files / Instruction Registers RF10 lower (RF10L) Reset Source: mod_g_rst_n

14.3.2.6.2.12 PBIST_RF11L Register

14.3.2.6.2.12.1 PBIST_RF11L Register (Offset = 2Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8807. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 002Ch
C7X256V1_PBIST	0037 002Ch

Figure 14-4375. PBIST_RF11L Name Register

31	30	29	28	27	26	25	24
RF11L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF11L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF11L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF11L							
R/W							
0h							

Table 14-8808. PBIST_RF11L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF11L	R/W	0h	Register Files / Instruction Registers RF11 lower (RF11L) Reset Source: mod_g_rst_n

14.3.2.6.2.13 PBIST_RF12L Register

14.3.2.6.2.13.1 PBIST_RF12L Register (Offset = 30h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8809. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0030h
C7X256V1_PBIST	0037 0030h

Figure 14-4376. PBIST_RF12L Name Register

31	30	29	28	27	26	25	24
RF12L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF12L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF12L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF12L							
R/W							
0h							

Table 14-8810. PBIST_RF12L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF12L	R/W	0h	Register Files / Instruction Registers RF12 lower (RF12L) Reset Source: mod_g_rst_n

14.3.2.6.2.14 PBIST_RF13L Register

14.3.2.6.2.14.1 PBIST_RF13L Register (Offset = 34h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8811. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0034h
C7X256V1_PBIST	0037 0034h

Figure 14-4377. PBIST_RF13L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF13L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF13L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF13L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF13L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8812. PBIST_RF13L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF13L	R/W	0h	Register Files / Instruction Registers RF13 lower (RF13L) Reset Source: mod_g_rst_n

14.3.2.6.2.15 PBIST_RF14L Register

14.3.2.6.2.15.1 PBIST_RF14L Register (Offset = 38h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-8813. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0038h
C7X256V1_PBIST	0037 0038h

Figure 14-4378. PBIST_RF14L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF14L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF14L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF14L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF14L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8814. PBIST_RF14L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF14L	R/W	0h	Register Files / Instruction Registers RF14 lower (RF14L) Reset Source: mod_g_rst_n

14.3.2.6.2.16 PBIST_RF15L Register

14.3.2.6.2.16.1 PBIST_RF15L Register (Offset = 3Ch) [reset = 0h]

Register Files / Instruction Registers

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Table 14-8815. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 003Ch
C7X256V1_PBIST	0037 003Ch

Figure 14-4379. PBIST_RF15L Name Register

31	30	29	28	27	26	25	24
RF15L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF15L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF15L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF15L							
R/W							
0h							

Table 14-8816. PBIST_RF15L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF15L	R/W	0h	Register Files / Instruction Registers RF15 lower (RF15L) Reset Source: mod_g_rst_n

14.3.2.6.2.17 PBIST_RF0U Register

14.3.2.6.2.17.1 PBIST_RF0U Register (Offset = 40h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-8817. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0040h
C7X256V1_PBIST	0037 0040h

Figure 14-4380. PBIST_RF0U Name Register

31	30	29	28	27	26	25	24
RF0U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF0U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF0U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF0U							
R/W							
0h							

Table 14-8818. PBIST_RF0U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF0U	R/W	0h	Register Files / Instruction Registers RF0 upper (RF0U) Reset Source: mod_g_rst_n

14.3.2.6.2.18 PBIST_RF1U Register

14.3.2.6.2.18.1 PBIST_RF1U Register (Offset = 44h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-8819. Instance Table

Instance Name	**Physical Address**
C7X256V0_PBIST	0036 0044h
C7X256V1_PBIST	0037 0044h

Figure 14-4381. PBIST_RF1U Name Register

31	30	29	28	27	26	25	24
RF1U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF1U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF1U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF1U							
R/W							
0h							

Table 14-8820. PBIST_RF1U Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	RF1U	R/W	0h	Register Files / Instruction Registers RF1 upper (RF1U) Reset Source: mod_g_rst_n

14.3.2.6.2.19 PBIST_RF2U Register

14.3.2.6.2.19.1 PBIST_RF2U Register (Offset = 48h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8821. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0048h
C7X256V1_PBIST	0037 0048h

Figure 14-4382. PBIST_RF2U Name Register

31	30	29	28	27	26	25	24
RF2U							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RF2U							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RF2U							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RF2U							
R/W							
0h							

Table 14-8822. PBIST_RF2U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF2U	R/W	0h	Register Files / Instruction Registers RF2 upper (RF2U) Reset Source: mod_g_rst_n

14.3.2.6.2.20 PBIST_RF3U Register

14.3.2.6.2.20.1 PBIST_RF3U Register (Offset = 4Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8823. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 004Ch
C7X256V1_PBIST	0037 004Ch

Figure 14-4383. PBIST_RF3U Name Register

31	30	29	28	27	26	25	24
RF3U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF3U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF3U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF3U							
R/W							
0h							

Table 14-8824. PBIST_RF3U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF3U	R/W	0h	Register Files / Instruction Registers RF3 upper (RF3U) Reset Source: mod_g_rst_n

14.3.2.6.2.21 PBIST_RF4U Register

14.3.2.6.2.21.1 PBIST_RF4U Register (Offset = 50h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8825. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0050h
C7X256V1_PBIST	0037 0050h

Figure 14-4384. PBIST_RF4U Name Register

31	30	29	28	27	26	25	24
RF4U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF4U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF4U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF4U							
R/W							
0h							

Table 14-8826. PBIST_RF4U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF4U	R/W	0h	Register Files / Instruction Registers RF4 upper (RF4U) Reset Source: mod_g_rst_n

14.3.2.6.2.22 PBIST_RF5U Register

14.3.2.6.2.22.1 PBIST_RF5U Register (Offset = 54h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8827. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0054h
C7X256V1_PBIST	0037 0054h

Figure 14-4385. PBIST_RF5U Name Register

31	30	29	28	27	26	25	24
RF5U							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RF5U							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RF5U							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RF5U							
R/W							
0h							

Table 14-8828. PBIST_RF5U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF5U	R/W	0h	Register Files / Instruction Registers RF5 upper (RF5U) Reset Source: mod_g_rst_n

14.3.2.6.2.23 PBIST_RF6U Register

14.3.2.6.2.23.1 PBIST_RF6U Register (Offset = 58h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8829. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0058h
C7X256V1_PBIST	0037 0058h

Figure 14-4386. PBIST_RF6U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF6U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF6U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF6U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF6U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8830. PBIST_RF6U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF6U	R/W	0h	Register Files / Instruction Registers RF6 upper (RF6U) Reset Source: mod_g_rst_n

14.3.2.6.2.24 PBIST_RF7U Register

14.3.2.6.2.24.1 PBIST_RF7U Register (Offset = 5Ch) [reset = 0h]

Register Files / Instruction Registers

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Table 14-8831. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 005Ch
C7X256V1_PBIST	0037 005Ch

Figure 14-4387. PBIST_RF7U Name Register

31	30	29	28	27	26	25	24
RF7U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF7U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF7U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF7U							
R/W							
0h							

Table 14-8832. PBIST_RF7U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF7U	R/W	0h	Register Files / Instruction Registers RF7 upper (RF7U) Reset Source: mod_g_rst_n

14.3.2.6.2.25 PBIST_RF8U Register

14.3.2.6.2.25.1 PBIST_RF8U Register (Offset = 60h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8833. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0060h
C7X256V1_PBIST	0037 0060h

Figure 14-4388. PBIST_RF8U Name Register

31	30	29	28	27	26	25	24
RF8U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF8U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF8U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF8U							
R/W							
0h							

Table 14-8834. PBIST_RF8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF8U	R/W	0h	Register Files / Instruction Registers RF8 upper (RF8U) Reset Source: mod_g_rst_n

14.3.2.6.2.26 PBIST_RF9U Register

14.3.2.6.2.26.1 PBIST_RF9U Register (Offset = 64h) [reset = 0h]

Register Files / Instruction Registers

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Table 14-8835. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0064h
C7X256V1_PBIST	0037 0064h

Figure 14-4389. PBIST_RF9U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF9U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF9U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF9U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF9U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8836. PBIST_RF9U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF9U	R/W	0h	Register Files / Instruction Registers RF9 upper (RF9U) Reset Source: mod_g_rst_n

14.3.2.6.2.27 PBIST_RF10U Register

14.3.2.6.2.27.1 PBIST_RF10U Register (Offset = 68h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8837. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0068h
C7X256V1_PBIST	0037 0068h

Figure 14-4390. PBIST_RF10U Name Register

31	30	29	28	27	26	25	24
RF10U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF10U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF10U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF10U							
R/W							
0h							

Table 14-8838. PBIST_RF10U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF10U	R/W	0h	Register Files / Instruction Registers RF10 upper (RF10U) Reset Source: mod_g_rst_n

14.3.2.6.2.28 PBIST_RF11U Register

14.3.2.6.2.28.1 PBIST_RF11U Register (Offset = 6Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8839. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 006Ch
C7X256V1_PBIST	0037 006Ch

Figure 14-4391. PBIST_RF11U Name Register

31	30	29	28	27	26	25	24
RF11U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF11U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF11U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF11U							
R/W							
0h							

Table 14-8840. PBIST_RF11U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF11U	R/W	0h	Register Files / Instruction Registers RF11 upper (RF11U) Reset Source: mod_g_rst_n

14.3.2.6.2.29 PBIST_RF12U Register

14.3.2.6.2.29.1 PBIST_RF12U Register (Offset = 70h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8841. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0070h
C7X256V1_PBIST	0037 0070h

Figure 14-4392. PBIST_RF12U Name Register

31	30	29	28	27	26	25	24
RF12U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF12U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF12U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF12U							
R/W							
0h							

Table 14-8842. PBIST_RF12U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF12U	R/W	0h	Register Files / Instruction Registers RF12 upper (RF12U) Reset Source: mod_g_rst_n

14.3.2.6.2.30 PBIST_RF13U Register

14.3.2.6.2.30.1 PBIST_RF13U Register (Offset = 74h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8843. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0074h
C7X256V1_PBIST	0037 0074h

Figure 14-4393. PBIST_RF13U Name Register

31	30	29	28	27	26	25	24
RF13U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF13U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF13U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF13U							
R/W							
0h							

Table 14-8844. PBIST_RF13U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF13U	R/W	0h	Register Files / Instruction Registers RF13 upper (RF13U) Reset Source: mod_g_rst_n

14.3.2.6.2.31 PBIST_RF14U Register

14.3.2.6.2.31.1 PBIST_RF14U Register (Offset = 78h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8845. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0078h
C7X256V1_PBIST	0037 0078h

Figure 14-4394. PBIST_RF14U Name Register

31	30	29	28	27	26	25	24
RF14U							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RF14U							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RF14U							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RF14U							
R/W							
0h							

Table 14-8846. PBIST_RF14U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF14U	R/W	0h	Register Files / Instruction Registers RF14 upper (RF14U) Reset Source: mod_g_rst_n

14.3.2.6.2.32 PBIST_RF15U Register

14.3.2.6.2.32.1 PBIST_RF15U Register (Offset = 7Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-8847. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 007Ch
C7X256V1_PBIST	0037 007Ch

Figure 14-4395. PBIST_RF15U Name Register

31	30	29	28	27	26	25	24
RF15U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF15U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF15U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF15U							
R/W							
0h							

Table 14-8848. PBIST_RF15U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF15U	R/W	0h	Register Files / Instruction Registers RF15 upper (RF15U) Reset Source: mod_g_rst_n

14.3.2.6.2.33 PBIST_A0 Register

14.3.2.6.2.33.1 PBIST_A0 Register (Offset = 100h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-8849. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0100h
C7X256V1_PBIST	0037 0100h

Figure 14-4396. PBIST_A0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A0							
R/W							
0h							
7	6	5	4	3	2	1	0
A0							
R/W							
0h							

Table 14-8850. PBIST_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A0	R/W	0h	Variable Address Register 0 (A0) Reset Source: mod_g_rst_n

14.3.2.6.2.34 PBIST_A1 Register

14.3.2.6.2.34.1 PBIST_A1 Register (Offset = 104h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-8851. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0104h
C7X256V1_PBIST	0037 0104h

Figure 14-4397. PBIST_A1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
A1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A1							
R/W							
0h							

Table 14-8852. PBIST_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A1	R/W	0h	Variable Address Register 1 (A1) Reset Source: mod_g_rst_n

14.3.2.6.2.35 PBIST_A2 Register

14.3.2.6.2.35.1 PBIST_A2 Register (Offset = 108h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-8853. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0108h
C7X256V1_PBIST	0037 0108h

Figure 14-4398. PBIST_A2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A2							
R/W							
0h							
7	6	5	4	3	2	1	0
A2							
R/W							
0h							

Table 14-8854. PBIST_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A2	R/W	0h	Variable Address Register 2 (A2) Reset Source: mod_g_rst_n

14.3.2.6.2.36 PBIST_A3 Register

14.3.2.6.2.36.1 PBIST_A3 Register (Offset = 10Ch) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-8855. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 010Ch
C7X256V1_PBIST	0037 010Ch

Figure 14-4399. PBIST_A3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A3							
R/W							
0h							
7	6	5	4	3	2	1	0
A3							
R/W							
0h							

Table 14-8856. PBIST_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A3	R/W	0h	Variable Address Register 3 (A3) Reset Source: mod_g_rst_n

14.3.2.6.2.37 PBIST_L0 Register

14.3.2.6.2.37.1 PBIST_L0 Register (Offset = 110h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-8857. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0110h
C7X256V1_PBIST	0037 0110h

Figure 14-4400. PBIST_L0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L0							
R/W							
0h							
7	6	5	4	3	2	1	0
L0							
R/W							
0h							

Table 14-8858. PBIST_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L0	R/W	0h	Variable Loop Count Register 0 (L0) Reset Source: mod_g_rst_n

14.3.2.6.2.38 PBIST_L1 Register

14.3.2.6.2.38.1 PBIST_L1 Register (Offset = 114h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-8859. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0114h
C7X256V1_PBIST	0037 0114h

Figure 14-4401. PBIST_L1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L1							
R/W							
0h							
7	6	5	4	3	2	1	0
L1							
R/W							
0h							

Table 14-8860. PBIST_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L1	R/W	0h	Variable Loop Count Register 1 (L1) Reset Source: mod_g_rst_n

14.3.2.6.2.39 PBIST_L2 Register

14.3.2.6.2.39.1 PBIST_L2 Register (Offset = 118h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-8861. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0118h
C7X256V1_PBIST	0037 0118h

Figure 14-4402. PBIST_L2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L2							
R/W							
0h							
7	6	5	4	3	2	1	0
L2							
R/W							
0h							

Table 14-8862. PBIST_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L2	R/W	0h	Variable Loop Count Register 2 (L2) Reset Source: mod_g_rst_n

14.3.2.6.2.40 PBIST_L3 Register

14.3.2.6.2.40.1 PBIST_L3 Register (Offset = 11Ch) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-8863. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 011Ch
C7X256V1_PBIST	0037 011Ch

Figure 14-4403. PBIST_L3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">L3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">L3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8864. PBIST_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L3	R/W	0h	Variable Loop Count Register 3 (L3) Reset Source: mod_g_rst_n

14.3.2.6.2.41 PBIST_D Register

14.3.2.6.2.41.1 PBIST_D Register (Offset = 120h) [reset = 0h]

Data Registers

Return to Summary Table

Table 14-8865. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0120h
C7X256V1_PBIST	0037 0120h

Figure 14-4404. PBIST_D Name Register

31	30	29	28	27	26	25	24
D1							
R/W							
0h							
23	22	21	20	19	18	17	16
D1							
R/W							
0h							
15	14	13	12	11	10	9	8
D0							
R/W							
0h							
7	6	5	4	3	2	1	0
D0							
R/W							
0h							

Table 14-8866. PBIST_D Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	D1	R/W	0h	DD1 Data Register Upper 16 (D1) Reset Source: mod_g_rst_n
15:0	D0	R/W	0h	DD0 Data Register Lower 16 (D0) Reset Source: mod_g_rst_n

14.3.2.6.2.42 PBIST_E Register

14.3.2.6.2.42.1 PBIST_E Register (Offset = 124h) [reset = 0h]

Data Registers

Return to Summary Table

Table 14-8867. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0124h
C7X256V1_PBIST	0037 0124h

Figure 14-4405. PBIST_E Name Register

31	30	29	28	27	26	25	24
E1							
R/W							
0h							
23	22	21	20	19	18	17	16
E1							
R/W							
0h							
15	14	13	12	11	10	9	8
E0							
R/W							
0h							
7	6	5	4	3	2	1	0
E0							
R/W							
0h							

Table 14-8868. PBIST_E Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	E1	R/W	0h	EE1 Data Register Upper 16 (E1) Reset Source: mod_g_rst_n
15:0	E0	R/W	0h	EE0 Data Register Lower 16 (E0) Reset Source: mod_g_rst_n

14.3.2.6.2.43 PBIST_CA0 Register

14.3.2.6.2.43.1 PBIST_CA0 Register (Offset = 130h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-8869. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0130h
C7X256V1_PBIST	0037 0130h

Figure 14-4406. PBIST_CA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA0							
R/W							
0h							
7	6	5	4	3	2	1	0
CA0							
R/W							
0h							

Table 14-8870. PBIST_CA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA0	R/W	0h	Constant Address Register 0 (CA0) Reset Source: mod_g_rst_n

14.3.2.6.2.44 PBIST_CA1 Register

14.3.2.6.2.44.1 PBIST_CA1 Register (Offset = 134h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-8871. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0134h
C7X256V1_PBIST	0037 0134h

Figure 14-4407. PBIST_CA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA1							
R/W							
0h							
7	6	5	4	3	2	1	0
CA1							
R/W							
0h							

Table 14-8872. PBIST_CA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA1	R/W	0h	Constant Address Register 1 (CA1) Reset Source: mod_g_rst_n

14.3.2.6.2.45 PBIST_CA2 Register

14.3.2.6.2.45.1 PBIST_CA2 Register (Offset = 138h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-8873. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0138h
C7X256V1_PBIST	0037 0138h

Figure 14-4408. PBIST_CA2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA2							
R/W							
0h							
7	6	5	4	3	2	1	0
CA2							
R/W							
0h							

Table 14-8874. PBIST_CA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA2	R/W	0h	Constant Address Register 2 (CA2) Reset Source: mod_g_rst_n

14.3.2.6.2.46 PBIST_CA3 Register

14.3.2.6.2.46.1 PBIST_CA3 Register (Offset = 13Ch) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-8875. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 013Ch
C7X256V1_PBIST	0037 013Ch

Figure 14-4409. PBIST_CA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA3							
R/W							
0h							
7	6	5	4	3	2	1	0
CA3							
R/W							
0h							

Table 14-8876. PBIST_CA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA3	R/W	0h	Constant Address Register 3 (CA3) Reset Source: mod_g_rst_n

14.3.2.6.2.47 PBIST_CL0 Register

14.3.2.6.2.47.1 PBIST_CL0 Register (Offset = 140h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-8877. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0140h
C7X256V1_PBIST	0037 0140h

Figure 14-4410. PBIST_CL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL0							
R/W							
0h							
7	6	5	4	3	2	1	0
CL0							
R/W							
0h							

Table 14-8878. PBIST_CL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL0	R/W	0h	Constant Loop Count Register 0 (CL0) Reset Source: mod_g_rst_n

14.3.2.6.2.48 PBIST_CL1 Register

14.3.2.6.2.48.1 PBIST_CL1 Register (Offset = 144h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-8879. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0144h
C7X256V1_PBIST	0037 0144h

Figure 14-4411. PBIST_CL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL1							
R/W							
0h							
7	6	5	4	3	2	1	0
CL1							
R/W							
0h							

Table 14-8880. PBIST_CL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL1	R/W	0h	Constant Loop Count Register 1 (CL1) Reset Source: mod_g_rst_n

14.3.2.6.2.49 PBIST_CL2 Register

14.3.2.6.2.49.1 PBIST_CL2 Register (Offset = 148h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-8881. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0148h
C7X256V1_PBIST	0037 0148h

Figure 14-4412. PBIST_CL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CL2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CL2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8882. PBIST_CL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL2	R/W	0h	Constant Loop Count Register 2 (CL2) Reset Source: mod_g_rst_n

14.3.2.6.2.50 PBIST_CL3 Register

14.3.2.6.2.50.1 PBIST_CL3 Register (Offset = 14Ch) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-8883. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 014Ch
C7X256V1_PBIST	0037 014Ch

Figure 14-4413. PBIST_CL3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL3							
R/W							
0h							
7	6	5	4	3	2	1	0
CL3							
R/W							
0h							

Table 14-8884. PBIST_CL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL3	R/W	0h	Constant Loop Count Register 3 (CL3) Reset Source: mod_g_rst_n

14.3.2.6.2.51 PBIST_I0 Register

14.3.2.6.2.51.1 PBIST_I0 Register (Offset = 150h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-8885. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0150h
C7X256V1_PBIST	0037 0150h

Figure 14-4414. PBIST_I0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
I0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I0							
R/W							
0h							

Table 14-8886. PBIST_I0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 0 (I0) Reset Source: mod_g_rst_n

14.3.2.6.2.52 PBIST_I1 Register

14.3.2.6.2.52.1 PBIST_I1 Register (Offset = 154h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-8887. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0154h
C7X256V1_PBIST	0037 0154h

Figure 14-4415. PBIST_I1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-8888. PBIST_I1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 1 (I1) Reset Source: mod_g_rst_n

14.3.2.6.2.53 PBIST_I2 Register

14.3.2.6.2.53.1 PBIST_I2 Register (Offset = 158h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-8889. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0158h
C7X256V1_PBIST	0037 0158h

Figure 14-4416. PBIST_I2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">I0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">I0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-8890. PBIST_I2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 2 (I2) Reset Source: mod_g_rst_n

14.3.2.6.2.54 PBIST_I3 Register

14.3.2.6.2.54.1 PBIST_I3 Register (Offset = 15Ch) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-8891. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 015Ch
C7X256V1_PBIST	0037 015Ch

Figure 14-4417. PBIST_I3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-8892. PBIST_I3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 3 (I3) Reset Source: mod_g_rst_n

14.3.2.6.2.55 PBIST_RAMT Register

14.3.2.6.2.55.1 PBIST_RAMT Register (Offset = 160h) [reset = 0h]

RAM Configuration Register

Return to Summary Table

Table 14-8893. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0160h
C7X256V1_PBIST	0037 0160h

Figure 14-4418. PBIST_RAMT Name Register

31	30	29	28	27	26	25	24
RGS							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RDS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DWR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PLS				RLS	
NONE		R/W				R/W	
0h		0h				0h	

Table 14-8894. PBIST_RAMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RGS	R/W	0h	RAM Group Select RGS Reset Source: mod_g_rst_n
23:16	RDS	R/W	0h	Return Data select RDS Reset Source: mod_g_rst_n
15:8	DWR	R/W	0h	Data Width Register DWR Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:2	PLS	R/W	0h	Pipeline Latency Select Reset Source: mod_g_rst_n
1:0	RLS	R/W	0h	RAM Latency Select Reset Source: mod_g_rst_n

14.3.2.6.2.56 PBIST_DLR Register

14.3.2.6.2.56.1 PBIST_DLR Register (Offset = 164h) [reset = 208h]

Datalogger Register

Return to Summary Table

Table 14-8895. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0164h
C7X256V1_PBIST	0037 0164h

Figure 14-4419. PBIST_DLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
BRP							
R/W							
0h							

15	14	13	12	11	10	9	8
RESERVED					DLR1_RTM	DLR1_GNG	DLR1_MISR
NONE					R/W	R/W	R/W
0h					0h	1h	0h

7	6	5	4	3	2	1	0
DLR0_TSM	DLR0_CFMM	DLR0_ECAM	DLR0_CAM	DLR0_TCK	DLR0_ROM	DLR0_IDDQ	DLR0_DCM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	1h	0h	0h	0h

Table 14-8896. PBIST_DLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	BRP	R/W	0h	Datalogger 2 (BRP) Reset Source: mod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10	DLR1_RTM	R/W	0h	Retention testing mode Reset Source: mod_g_rst_n
9	DLR1_GNG	R/W	1h	GO / NO-GO testing mode Reset Source: mod_g_rst_n
8	DLR1_MISR	R/W	0h	MISR testing mode (mainly for ROM testing) Reset Source: mod_g_rst_n
7	DLR0_TSM	R/W	0h	Time stamp mode Reset Source: mod_g_rst_n
6	DLR0_CFMM	R/W	0h	Column Fail Masking mode Reset Source: mod_g_rst_n
5	DLR0_ECAM	R/W	0h	Emulation cache access mode Reset Source: mod_g_rst_n
4	DLR0_CAM	R/W	0h	Config access mode Reset Source: mod_g_rst_n

Table 14-8896. PBIST_DLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DLR0_TCK	R/W	1h	TCK Gated mode Reset Source: mod_g_rst_n
2	DLR0_ROM	R/W	0h	ROM-based testing mode Reset Source: mod_g_rst_n
1	DLR0_IDDQ	R/W	0h	IDDQ testing mode Reset Source: mod_g_rst_n
0	DLR0_DCM	R/W	0h	Distributed Compare mode Reset Source: mod_g_rst_n

14.3.2.6.2.57 PBIST_CMS Register

14.3.2.6.2.57.1 PBIST_CMS Register (Offset = 168h) [reset = 0h]

Clock-Mux Select Register

Return to Summary Table

Table 14-8897. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0168h
C7X256V1_PBIST	0037 0168h

Figure 14-4420. PBIST_CMS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMS			
NONE				R/W			
0h				0h			

Table 14-8898. PBIST_CMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CMS	R/W	0h	Clock Mux Select (CMS) Reset Source: mod_g_rst_n

14.3.2.6.2.58 PBIST_STR Register

14.3.2.6.2.58.1 PBIST_STR Register (Offset = 16Ch) [reset = 0h]

Program Control Register

Return to Summary Table

Table 14-8899. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 016Ch
C7X256V1_PBIST	0037 016Ch

Figure 14-4421. PBIST_STR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			CHK	STEP	STOP	RES	START
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-8900. PBIST_STR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	CHK	R/W	0h	Check MISR mode Reset Source: mod_g_rst_n
3	STEP	R/W	0h	Step / Step for emulation mode Reset Source: mod_g_rst_n
2	STOP	R/W	0h	Stop Reset Source: mod_g_rst_n
1	RES	R/W	0h	Resume / Emulation read Reset Source: mod_g_rst_n
0	START	R/W	0h	Start / Time Stamp mode restart Reset Source: mod_g_rst_n

14.3.2.6.2.59 PBIST_SCR Register

14.3.2.6.2.59.1 PBIST_SCR Register (Offset = 170h) [reset = FEDCBA9876542F40h]

Address Scrambling Register

Return to Summary Table

Table 14-8901. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0170h
C7X256V1_PBIST	0037 0170h

Figure 14-4422. PBIST_SCR Name Register

63	62	61	60	59	58	57	48
SCR7							
R/W							
FEh							
55	54	53	52	51	50	49	48
SCR6							
R/W							
DCh							
47	46	45	44	43	42	41	40
SCR5							
R/W							
BAh							
39	38	37	36	35	34	33	32
SCR4							
R/W							
98h							
15	14	13	12	11	10	9	8
SCR1							
R/W							
32h							
7	6	5	4	3	2	1	0
SCR0							
R/W							
10h							

Table 14-8902. PBIST_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
63:56	SCR7	R/W	FEh	Address Scrambling Register 7 Reset Source: mod_g_rst_n
55:48	SCR6	R/W	DCh	Address Scrambling Register 6 Reset Source: mod_g_rst_n
47:40	SCR5	R/W	BAh	Address Scrambling Register 5 Reset Source: mod_g_rst_n
39:32	SCR4	R/W	98h	Address Scrambling Register 4 Reset Source: mod_g_rst_n
31:24	SCR3	R/W	76h	Address Scrambling Register 3 Reset Source: mod_g_rst_n

Table 14-8902. PBIST_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	SCR2	R/W	54h	Address Scrambling Register 2 Reset Source: mod_g_rst_n
15:8	SCR1	R/W	32h	Address Scrambling Register 1 Reset Source: mod_g_rst_n
7:0	SCR0	R/W	10h	Address Scrambling Register 0 Reset Source: mod_g_rst_n

14.3.2.6.2.60 PBIST_CSR Register

14.3.2.6.2.60.1 PBIST_CSR Register (Offset = 178h) [reset = 0h]

Chip Select Register

Return to Summary Table

Table 14-8903. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0178h
C7X256V1_PBIST	0037 0178h

Figure 14-4423. PBIST_CSR Name Register

31	30	29	28	27	26	25	24
CSR3							
R/W							
0h							
23	22	21	20	19	18	17	16
CSR2							
R/W							
0h							
15	14	13	12	11	10	9	8
CSR1							
R/W							
0h							
7	6	5	4	3	2	1	0
CSR0							
R/W							
0h							

Table 14-8904. PBIST_CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CSR3	R/W	0h	Chip Select 3 (CSR3) Reset Source: mod_g_rst_n
23:16	CSR2	R/W	0h	Chip Select 2 (CSR2) Reset Source: mod_g_rst_n
15:8	CSR1	R/W	0h	Chip Select 1(CSR1) Reset Source: mod_g_rst_n
7:0	CSR0	R/W	0h	Chip Select 0 (CSR0) Reset Source: mod_g_rst_n

14.3.2.6.2.61 PBIST_FDLY Register

14.3.2.6.2.61.1 PBIST_FDLY Register (Offset = 17Ch) [reset = 68h]

Fail Delay Register

Return to Summary Table

Table 14-8905. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 017Ch
C7X256V1_PBIST	0037 017Ch

Figure 14-4424. PBIST_FDLY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FDLY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">68h</td></tr>
</table>

Table 14-8906. PBIST_FDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDLY	R/W	68h	Fail Delay (FDLY) Reset Source: mod_g_rst_n

14.3.2.6.2.62 PBIST_PACT Register

14.3.2.6.2.62.1 PBIST_PACT Register (Offset = 180h) [reset = 0h]

PACT Register

Return to Summary Table

Table 14-8907. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0180h
C7X256V1_PBIST	0037 0180h

Figure 14-4425. PBIST_PACT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PACT
NONE							R/W
0h							0h

Table 14-8908. PBIST_PACT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PACT	R/W	0h	PBIST Activate (PACT) Reset Source: mod_g_rst_n

14.3.2.6.2.63 PBIST_PID Register

14.3.2.6.2.63.1 PBIST_PID Register (Offset = 184h) [reset = 0h]

PBIST_ID Register

Return to Summary Table

Table 14-8909. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0184h
C7X256V1_PBIST	0037 0184h

Figure 14-4426. PBIST_PID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PID				
NONE			R/W				
0h			0h				

Table 14-8910. PBIST_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	PID	R/W	0h	PBIST ID Reset Source: mod_g_rst_n

14.3.2.6.2.64 PBIST_OVER Register

14.3.2.6.2.64.1 PBIST_OVER Register (Offset = 188h) [reset = 9h]

Override Register

Return to Summary Table

Table 14-8911. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0188h
C7X256V1_PBIST	0037 0188h

Figure 14-4427. PBIST_OVER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>ALGO</td><td>MM</td><td>READ</td><td>RINFO</td></tr>
<tr><td colspan="4">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>1h</td><td>0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-8912. PBIST_OVER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ALGO	R/W	1h	PBIST Override Algorithm Override Reset Source: mod_g_rst_n
2	MM	R/W	0h	PBIST Override Multiple Memory Reset Source: mod_g_rst_n
1	READ	R/W	0h	PBIST Override READ Override Reset Source: mod_g_rst_n
0	RINFO	R/W	1h	PBIST Override RINFO Override Reset Source: mod_g_rst_n

14.3.2.6.2.65 PBIST_FSRF Register

14.3.2.6.2.65.1 PBIST_FSRF Register (Offset = 190h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-8913. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0190h
C7X256V1_PBIST	0037 0190h

Figure 14-4428. PBIST_FSRF Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="7">RESERVED</td><td>FRSF1</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>FRSF0</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-8914. PBIST_FSRF Register Field Descriptions

Bit	Field	Type	Reset	Description
63:33	RESERVED	NONE	0h	Reserved
32	FRSF1	R	0h	Fail Status Fail - Port 1 (FSRF1) Reset Source: mod_g_rst_n
31:1	RESERVED	NONE	0h	Reserved
0	FRSF0	R	0h	Fail Status Fail - Port 0 (FSRF0) Reset Source: mod_g_rst_n

14.3.2.6.2.66 PBIST_FSRC Register

14.3.2.6.2.66.1 PBIST_FSRC Register (Offset = 198h) [reset = 0h]

Fail Status Count Register

Return to Summary Table

Table 14-8915. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 0198h
C7X256V1_PBIST	0037 0198h

Figure 14-4429. PBIST_FSRC Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FSRC1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FSRC0</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-8916. PBIST_FSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
63:36	RESERVED	NONE	0h	Reserved
35:32	FSRC1	R	0h	Fail Status Count - Port 1 (FSRC1) Reset Source: mod_g_rst_n
31:4	RESERVED	NONE	0h	Reserved
3:0	FSRC0	R	0h	Fail Status Count - Port 0 (FSRC0) Reset Source: mod_g_rst_n

14.3.2.6.2.67 PBIST_FSRA Register

14.3.2.6.2.67.1 PBIST_FSRA Register (Offset = 1A0h) [reset = 0h]

Fail Status Address Register

Return to Summary Table

Table 14-8917. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01A0h
C7X256V1_PBIST	0037 01A0h

Figure 14-4430. PBIST_FSRA Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
FSRA1							
R							
0h							
39	38	37	36	35	34	33	32
FSRA1							
R							
0h							
15	14	13	12	11	10	9	8
FSRA0							
R							
0h							
7	6	5	4	3	2	1	0
FSRA0							
R							
0h							

Table 14-8918. PBIST_FSRA Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RESERVED	NONE	0h	Reserved
47:32	FSRA1	R	0h	Fail Status Address - Port 1 (FSRA1) Reset Source: mod_g_rst_n
31:16	RESERVED	NONE	0h	Reserved
15:0	FSRA0	R	0h	Fail Status Address - Port 0 (FSRA0) Reset Source: mod_g_rst_n

14.3.2.6.2.68 PBIST_FSRDL0 Register

14.3.2.6.2.68.1 PBIST_FSRDL0 Register (Offset = 1A8h) [reset = 0h]

Fail Status Data Registers

Return to Summary Table

Table 14-8919. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01A8h
C7X256V1_PBIST	0037 01A8h

Figure 14-4431. PBIST_FSRDL0 Name Register

31	30	29	28	27	26	25	24
FSRDL0							
R							
0h							
23	22	21	20	19	18	17	16
FSRDL0							
R							
0h							
15	14	13	12	11	10	9	8
FSRDL0							
R							
0h							
7	6	5	4	3	2	1	0
FSRDL0							
R							
0h							

Table 14-8920. PBIST_FSRDL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FSRDL0	R	0h	Fail Status Data - Port 0 (FSRDL0) Reset Source: mod_g_rst_n

14.3.2.6.2.69 PBIST_FSRDL1 Register

14.3.2.6.2.69.1 PBIST_FSRDL1 Register (Offset = 1B0h) [reset = 0h]

Fail Status Data Registers

Return to Summary Table

Table 14-8921. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01B0h
C7X256V1_PBIST	0037 01B0h

Figure 14-4432. PBIST_FSRDL1 Name Register

31	30	29	28	27	26	25	24
FSRDL1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FSRDL1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FSRDL1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FSRDL1							
R							
0h							

Table 14-8922. PBIST_FSRDL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FSRDL1	R	0h	Fail Status Data - Port 1 (FSRDL1) Reset Source: mod_g_rst_n

14.3.2.6.2.70 PBIST_MARGIN_MODE Register

14.3.2.6.2.70.1 PBIST_MARGIN_MODE Register (Offset = 1B4h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-8923. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01B4h
C7X256V1_PBIST	0037 01B4h

Figure 14-4433. PBIST_MARGIN_MODE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PBIST_DFT_READ		PBIST_DFT_WRITE	
NONE				R		R	
0h				0h		0h	

Table 14-8924. PBIST_MARGIN_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	PBIST_DFT_READ	R	0h	pbist_dft_read[1:0] Reset Source: mod_g_rst_n
1:0	PBIST_DFT_WRITE	R	0h	pbist_dft_write[1:0] Reset Source: mod_g_rst_n

14.3.2.6.2.71 PBIST_WRENZ Register

14.3.2.6.2.71.1 PBIST_WRENZ Register (Offset = 1B8h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-8925. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01B8h
C7X256V1_PBIST	0037 01B8h

Figure 14-4434. PBIST_WRENZ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WRENZ	
NONE						R	
0h						0h	

Table 14-8926. PBIST_WRENZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	WRENZ	R	0h	pbist_ram_wrenz[1:0] Reset Source: mod_g_rst_n

14.3.2.6.2.72 PBIST_PAGE_PGS Register

14.3.2.6.2.72.1 PBIST_PAGE_PGS Register (Offset = 1BCh) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-8927. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01BCh
C7X256V1_PBIST	0037 01BCh

Figure 14-4435. PBIST_PAGE_PGS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PGS	
NONE						R	
0h						0h	

Table 14-8928. PBIST_PAGE_PGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PGS	R	0h	pbist_ram_pgs[1:0] Reset Source: mod_g_rst_n

14.3.2.6.2.73 PBIST_ROM Register

14.3.2.6.2.73.1 PBIST_ROM Register (Offset = 1C0h) [reset = 3h]

ROM Mask Register

Return to Summary Table

Table 14-8929. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01C0h
C7X256V1_PBIST	0037 01C0h

Figure 14-4436. PBIST_ROM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ROM	
NONE						R/W	
0h						3h	

Table 14-8930. PBIST_ROM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ROM	R/W	3h	ROM Mask (ROM) Reset Source: mod_g_rst_n

14.3.2.6.2.74 PBIST_ALGO Register

14.3.2.6.2.74.1 PBIST_ALGO Register (Offset = 1C4h) [reset = FFFFFFFFh]

Algorithm Mask Register

Return to Summary Table

Table 14-8931. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01C4h
C7X256V1_PBIST	0037 01C4h

Figure 14-4437. PBIST_ALGO Name Register

31	30	29	28	27	26	25	24
ALGO_3							
R/W							
FFh							
23	22	21	20	19	18	17	16
ALGO_2							
R/W							
FFh							
15	14	13	12	11	10	9	8
ALGO_1							
R/W							
FFh							
7	6	5	4	3	2	1	0
ALGO_0							
R/W							
FFh							

Table 14-8932. PBIST_ALGO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ALGO_3	R/W	FFh	ROM Algorithm Mask 3 (ALGO 3) Reset Source: mod_g_rst_n
23:16	ALGO_2	R/W	FFh	ROM Algorithm Mask 2 (ALGO 2) Reset Source: mod_g_rst_n
15:8	ALGO_1	R/W	FFh	ROM Algorithm Mask 1 (ALGO 1) Reset Source: mod_g_rst_n
7:0	ALGO_0	R/W	FFh	ROM Algorithm Mask 0 (ALGO 0) Reset Source: mod_g_rst_n

14.3.2.6.2.75 PBIST_RINFO Register

14.3.2.6.2.75.1 PBIST_RINFO Register (Offset = 1C8h) [reset = 1000000000000180h]

RAM Info Mask Register

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Table 14-8933. Instance Table

Instance Name	Physical Address
C7X256V0_PBIST	0036 01C8h
C7X256V1_PBIST	0037 01C8h

Figure 14-4438. PBIST_RINFO Name Register

63	62	61	60	59	58	57	48
U3							
R/W							
FFh							
55	54	53	52	51	50	49	48
U2							
R/W							
FFh							
47	46	45	44	43	42	41	40
U1							
R/W							
FFh							
39	38	37	36	35	34	33	32
U0							
R/W							
FFh							
15	14	13	12	11	10	9	8
L1							
R/W							
FFh							
7	6	5	4	3	2	1	0
L0							
R/W							
FFh							

Table 14-8934. PBIST_RINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
63:56	U3	R/W	FFh	RAM Info Mask Upper 3 (RINFOU3) Reset Source: mod_g_rst_n
55:48	U2	R/W	FFh	RAM Info Mask Upper 2 (RINFOU2) Reset Source: mod_g_rst_n
47:40	U1	R/W	FFh	RAM Info Mask Upper 1 (RINFOU1) Reset Source: mod_g_rst_n
39:32	U0	R/W	FFh	RAM Info Mask Upper 0 (RINFOU0) Reset Source: mod_g_rst_n
31:24	L3	R/W	FFh	RAM Info Mask Lower 3 (RINFOL3) Reset Source: mod_g_rst_n

Table 14-8934. PBIST_RINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	L2	R/W	FFh	RAM Info Mask Lower 2 (RINFOL2) Reset Source: mod_g_rst_n
15:8	L1	R/W	FFh	RAM Info Mask Lower 1 (RINFOL1) Reset Source: mod_g_rst_n
7:0	L0	R/W	FFh	RAM Info Mask Lower 0 (RINFOL0) Reset Source: mod_g_rst_n

14.4 Interprocessor Communication Registers

14.4.1 MAILBOX_MAILBOX_CLUSTER_0

MAILBOX_MAILBOX_CLUSTER_0

14.4.1.1 MAILBOX_MAILBOX_CLUSTER_0 Summaries

MAILBOX_MAILBOX_CLUSTER_0 Summaries

Table 14-8935. MAILBOX Registers, Base Address=2900 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_0 Physical Address
0h	32	MAILBOX_REVISION	2900 0000h
10h	32	MAILBOX_SYSCONFIG	2900 0010h
40h	32	MAILBOX_MESSAGE_J	2900 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2900 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2900 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2900 0140h
100h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2900 0100h + formula
104h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2900 0104h + formula
108h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2900 0108h + formula
10Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2900 010Ch + formula

14.4.1.2 MAILBOX_MAILBOX_CLUSTER_0 Registers

MAILBOX_MAILBOX_CLUSTER_0 Registers

14.4.1.2.1 MAILBOX_REVISION Register

14.4.1.2.1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-8936. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 0000h

Figure 14-4439. MAILBOX_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6FCh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6FCh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">12h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-8937. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.1.2.2 MAILBOX_SYSCONFIG Register

14.4.1.2.2.1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

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Table 14-8938. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 0010h

Figure 14-4440. MAILBOX_SYSCONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFT_RESET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-8939. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.1.2.3 MAILBOX_MESSAGE_J Register

14.4.1.2.3.1 MAILBOX_MESSAGE_J Register (Offset = 40h) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Return to Summary Table

Table 14-8940. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 0040h + formula

Figure 14-4441. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-8941. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.1.2.4 MAILBOX_FIFO_STATUS_J Register

14.4.1.2.4.1 MAILBOX_FIFO_STATUS_J Register (Offset = 80h) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

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Table 14-8942. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 0080h + formula

Figure 14-4442. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-8943. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.1.2.5 MAILBOX_MSG_STATUS_J Register

14.4.1.2.5.1 MAILBOX_MSG_STATUS_J Register (Offset = C0h) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

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Table 14-8944. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 00C0h + formula

Figure 14-4443. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-8945. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.1.2.6 MAILBOX_IRQ_EOI Register

14.4.1.2.6.1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

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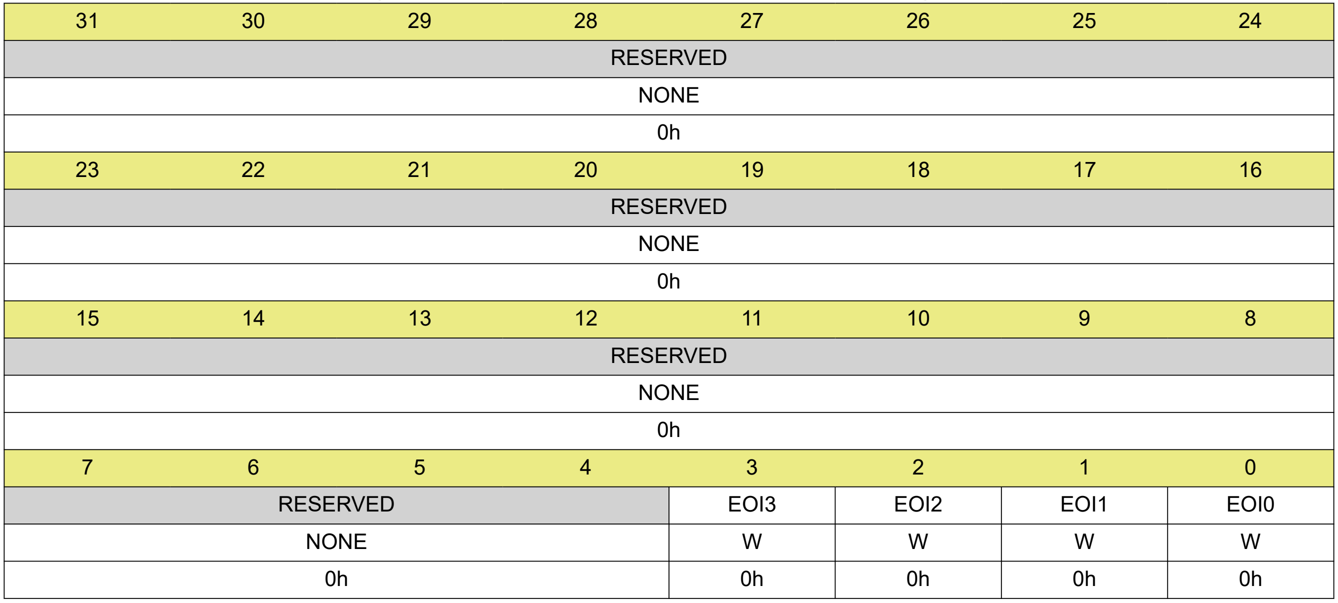
Table 14-8946. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 0140h

Figure 14-4444. MAILBOX_IRQ_EOI Name Register



31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-8947. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.1.2.7 MAILBOX_USER_IRQ_STATUS_RAW_J Register

14.4.1.2.7.1 MAILBOX_USER_IRQ_STATUS_RAW_J Register (Offset = 100h) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

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Table 14-8948. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 0100h + formula

Figure 14-4445. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-8949. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n

Table 14-8949. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n

Table 14-8949. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.1.2.8 MAILBOX_USER_IRQ_STATUS_CLR_J Register

14.4.1.2.8.1 MAILBOX_USER_IRQ_STATUS_CLR_J Register (Offset = 104h) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Return to Summary Table

Table 14-8950. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 0104h + formula

Figure 14-4446. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8951. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-8951. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n

Table 14-8951. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.1.2.9 MAILBOX_USER_IRQ_ENABLE_SET_J Register

14.4.1.2.9.1 MAILBOX_USER_IRQ_ENABLE_SET_J Register (Offset = 108h) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

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Table 14-8952. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 0108h + formula

Figure 14-4447. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8953. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8953. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8953. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.1.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_J Register

14.4.1.2.10.1 MAILBOX_USER_IRQ_ENABLE_CLR_J Register (Offset = 10Ch) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

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Table 14-8954. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_0	2900 010Ch + formula

Figure 14-4448. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8955. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8955. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8955. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.2 MAILBOX_MAILBOX_CLUSTER_1

MAILBOX_MAILBOX_CLUSTER_1

14.4.2.1 MAILBOX_MAILBOX_CLUSTER_1 Summaries

MAILBOX_MAILBOX_CLUSTER_1 Summaries

Table 14-8956. MAILBOX Registers, Base Address=2901 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_1 Physical Address
0h	32	MAILBOX_REVISION	2901 0000h
10h	32	MAILBOX_SYSCONFIG	2901 0010h
40h	32	MAILBOX_MESSAGE_J	2901 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2901 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2901 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2901 0140h
100h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2901 0100h + formula
104h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2901 0104h + formula
108h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2901 0108h + formula
10Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2901 010Ch + formula

14.4.2.2 MAILBOX_MAILBOX_CLUSTER_1 Registers

MAILBOX_MAILBOX_CLUSTER_1 Registers

14.4.2.2.1 MAILBOX_REVISION Register

14.4.2.2.1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-8957. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0000h

Figure 14-4449. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-8958. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.2.2.2 MAILBOX_SYSCONFIG Register

14.4.2.2.2.1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

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Table 14-8959. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0010h

Figure 14-4450. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-8960. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.2.2.3 MAILBOX_MESSAGE_J Register

14.4.2.2.3.1 MAILBOX_MESSAGE_J Register (Offset = 40h) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

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Table 14-8961. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0040h + formula

Figure 14-4451. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-8962. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.2.2.4 MAILBOX_FIFO_STATUS_J Register

14.4.2.2.4.1 MAILBOX_FIFO_STATUS_J Register (Offset = 80h) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

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Table 14-8963. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0080h + formula

Figure 14-4452. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-8964. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.2.2.5 MAILBOX_MSG_STATUS_J Register

14.4.2.2.5.1 MAILBOX_MSG_STATUS_J Register (Offset = C0h) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

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Table 14-8965. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 00C0h + formula

Figure 14-4453. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-8966. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.2.2.6 MAILBOX_IRQ_EOI Register

14.4.2.2.6.1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

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Table 14-8967. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0140h

Figure 14-4454. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-8968. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.2.2.7 MAILBOX_USER_IRQ_STATUS_RAW_J Register

14.4.2.2.7.1 MAILBOX_USER_IRQ_STATUS_RAW_J Register (Offset = 100h) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

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Table 14-8969. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0100h + formula

Figure 14-4455. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-8970. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n

Table 14-8970. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n

Table 14-8970. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.2.2.8 MAILBOX_USER_IRQ_STATUS_CLR_J Register

14.4.2.2.8.1 MAILBOX_USER_IRQ_STATUS_CLR_J Register (Offset = 104h) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

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Table 14-8971. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0104h + formula

Figure 14-4456. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8972. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-8972. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n

Table 14-8972. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.2.2.9 MAILBOX_USER_IRQ_ENABLE_SET_J Register

14.4.2.2.9.1 MAILBOX_USER_IRQ_ENABLE_SET_J Register (Offset = 108h) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

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Table 14-8973. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 0108h + formula

Figure 14-4457. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8974. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8974. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8974. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.2.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_J Register

14.4.2.2.10.1 MAILBOX_USER_IRQ_ENABLE_CLR_J Register (Offset = 10Ch) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

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Table 14-8975. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_1	2901 010Ch + formula

Figure 14-4458. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8976. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8976. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8976. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.3 MAILBOX_MAILBOX_CLUSTER_2

MAILBOX_MAILBOX_CLUSTER_2

14.4.3.1 MAILBOX_MAILBOX_CLUSTER_2 Summaries

MAILBOX_MAILBOX_CLUSTER_2 Summaries

Table 14-8977. MAILBOX Registers, Base Address=2902 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_2 Physical Address
0h	32	MAILBOX_REVISION	2902 0000h
10h	32	MAILBOX_SYSCONFIG	2902 0010h
40h	32	MAILBOX_MESSAGE_J	2902 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2902 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2902 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2902 0140h
100h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2902 0100h + formula
104h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2902 0104h + formula
108h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2902 0108h + formula
10Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2902 010Ch + formula

14.4.3.2 MAILBOX_MAILBOX_CLUSTER_2 Registers

MAILBOX_MAILBOX_CLUSTER_2 Registers

14.4.3.2.1 MAILBOX_REVISION Register

14.4.3.2.1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-8978. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0000h

Figure 14-4459. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-8979. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.3.2.2 MAILBOX_SYSCONFIG Register

14.4.3.2.2.1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

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Table 14-8980. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0010h

Figure 14-4460. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-8981. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.3.2.3 MAILBOX_MESSAGE_J Register

14.4.3.2.3.1 MAILBOX_MESSAGE_J Register (Offset = 40h) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

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Table 14-8982. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0040h + formula

Figure 14-4461. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-8983. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.3.2.4 MAILBOX_FIFO_STATUS_J Register

14.4.3.2.4.1 MAILBOX_FIFO_STATUS_J Register (Offset = 80h) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

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Table 14-8984. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0080h + formula

Figure 14-4462. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-8985. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.3.2.5 MAILBOX_MSG_STATUS_J Register

14.4.3.2.5.1 MAILBOX_MSG_STATUS_J Register (Offset = C0h) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

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Table 14-8986. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 00C0h + formula

Figure 14-4463. MAILBOX_MSG_STATUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_MESSAGES</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-8987. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.3.2.6 MAILBOX_IRQ_EOI Register

14.4.3.2.6.1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

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Table 14-8988. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0140h

Figure 14-4464. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-8989. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.3.2.7 MAILBOX_USER_IRQ_STATUS_RAW_J Register

14.4.3.2.7.1 MAILBOX_USER_IRQ_STATUS_RAW_J Register (Offset = 100h) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

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Table 14-8990. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0100h + formula

Figure 14-4465. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-8991. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n

Table 14-8991. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n

Table 14-8991. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.3.2.8 MAILBOX_USER_IRQ_STATUS_CLR_J Register

14.4.3.2.8.1 MAILBOX_USER_IRQ_STATUS_CLR_J Register (Offset = 104h) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

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Table 14-8992. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0104h + formula

Figure 14-4466. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8993. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-8993. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n

Table 14-8993. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.3.2.9 MAILBOX_USER_IRQ_ENABLE_SET_J Register

14.4.3.2.9.1 MAILBOX_USER_IRQ_ENABLE_SET_J Register (Offset = 108h) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

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Table 14-8994. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 0108h + formula

Figure 14-4467. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8995. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8995. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8995. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.3.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_J Register

14.4.3.2.10.1 MAILBOX_USER_IRQ_ENABLE_CLR_J Register (Offset = 10Ch) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

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Table 14-8996. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_2	2902 010Ch + formula

Figure 14-4468. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-8997. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8997. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-8997. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.4 MAILBOX_MAILBOX_CLUSTER_3

MAILBOX_MAILBOX_CLUSTER_3

14.4.4.1 MAILBOX_MAILBOX_CLUSTER_3 Summaries

MAILBOX_MAILBOX_CLUSTER_3 Summaries

Table 14-8998. MAILBOX Registers, Base Address=2903 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_3 Physical Address
0h	32	MAILBOX_REVISION	2903 0000h
10h	32	MAILBOX_SYSCONFIG	2903 0010h
40h	32	MAILBOX_MESSAGE_J	2903 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2903 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2903 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2903 0140h
100h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2903 0100h + formula
104h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2903 0104h + formula
108h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2903 0108h + formula
10Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2903 010Ch + formula

14.4.4.2 MAILBOX_MAILBOX_CLUSTER_3 Registers

MAILBOX_MAILBOX_CLUSTER_3 Registers

14.4.4.2.1 MAILBOX_REVISION Register

14.4.4.2.1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-8999. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 0000h

Figure 14-4469. MAILBOX_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6FCh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6FCh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">12h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-9000. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.4.2.2 MAILBOX_SYSCONFIG Register

14.4.4.2.2.1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

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Table 14-9001. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 0010h

Figure 14-4470. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-9002. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.4.2.3 MAILBOX_MESSAGE_J Register

14.4.4.2.3.1 MAILBOX_MESSAGE_J Register (Offset = 40h) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

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Table 14-9003. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 0040h + formula

Figure 14-4471. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-9004. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.4.2.4 MAILBOX_FIFO_STATUS_J Register

14.4.4.2.4.1 MAILBOX_FIFO_STATUS_J Register (Offset = 80h) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

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Table 14-9005. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 0080h + formula

Figure 14-4472. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-9006. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.4.2.5 MAILBOX_MSG_STATUS_J Register

14.4.4.2.5.1 MAILBOX_MSG_STATUS_J Register (Offset = C0h) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

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Table 14-9007. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 00C0h + formula

Figure 14-4473. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-9008. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.4.2.6 MAILBOX_IRQ_EOI Register

14.4.4.2.6.1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

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Table 14-9009. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 0140h

Figure 14-4474. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-9010. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.4.2.7 MAILBOX_USER_IRQ_STATUS_RAW_J Register

14.4.4.2.7.1 MAILBOX_USER_IRQ_STATUS_RAW_J Register (Offset = 100h) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

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Table 14-9011. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 0100h + formula

Figure 14-4475. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-9012. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n

Table 14-9012. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n

Table 14-9012. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.4.2.8 MAILBOX_USER_IRQ_STATUS_CLR_J Register

14.4.4.2.8.1 MAILBOX_USER_IRQ_STATUS_CLR_J Register (Offset = 104h) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

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Table 14-9013. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 0104h + formula

Figure 14-4476. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9014. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-9014. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n

Table 14-9014. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.4.2.9 MAILBOX_USER_IRQ_ENABLE_SET_J Register

14.4.4.2.9.1 MAILBOX_USER_IRQ_ENABLE_SET_J Register (Offset = 108h) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

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Table 14-9015. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 0108h + formula

Figure 14-4477. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9016. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9016. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9016. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.4.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_J Register

14.4.4.2.10.1 MAILBOX_USER_IRQ_ENABLE_CLR_J Register (Offset = 10Ch) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

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Table 14-9017. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_3	2903 010Ch + formula

Figure 14-4478. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9018. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9018. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9018. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.5 MAILBOX_MAILBOX_CLUSTER_4

MAILBOX_MAILBOX_CLUSTER_4

14.4.5.1 MAILBOX_MAILBOX_CLUSTER_4 Summaries

MAILBOX_MAILBOX_CLUSTER_4 Summaries

Table 14-9019. MAILBOX Registers, Base Address=2904 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_4 Physical Address
0h	32	MAILBOX_REVISION	2904 0000h
10h	32	MAILBOX_SYSCONFIG	2904 0010h
40h	32	MAILBOX_MESSAGE_J	2904 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2904 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2904 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2904 0140h
100h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2904 0100h + formula
104h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2904 0104h + formula
108h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2904 0108h + formula
10Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2904 010Ch + formula

14.4.5.2 MAILBOX_MAILBOX_CLUSTER_4 Registers

MAILBOX_MAILBOX_CLUSTER_4 Registers

14.4.5.2.1 MAILBOX_REVISION Register

14.4.5.2.1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-9020. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 0000h

Figure 14-4479. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-9021. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.5.2.2 MAILBOX_SYSCONFIG Register

14.4.5.2.2.1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

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Table 14-9022. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 0010h

Figure 14-4480. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-9023. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.5.2.3 MAILBOX_MESSAGE_J Register

14.4.5.2.3.1 MAILBOX_MESSAGE_J Register (Offset = 40h) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

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Table 14-9024. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 0040h + formula

Figure 14-4481. MAILBOX_MESSAGE_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MESSAGE_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MESSAGE_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MESSAGE_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MESSAGE_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9025. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.5.2.4 MAILBOX_FIFO_STATUS_J Register

14.4.5.2.4.1 MAILBOX_FIFO_STATUS_J Register (Offset = 80h) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

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Table 14-9026. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 0080h + formula

Figure 14-4482. MAILBOX_FIFO_STATUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>FIFO_FULL</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9027. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.5.2.5 MAILBOX_MSG_STATUS_J Register

14.4.5.2.5.1 MAILBOX_MSG_STATUS_J Register (Offset = C0h) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

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Table 14-9028. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 00C0h + formula

Figure 14-4483. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-9029. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.5.2.6 MAILBOX_IRQ_EOI Register

14.4.5.2.6.1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

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Table 14-9030. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 0140h

Figure 14-4484. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-9031. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.5.2.7 MAILBOX_USER_IRQ_STATUS_RAW_J Register

14.4.5.2.7.1 MAILBOX_USER_IRQ_STATUS_RAW_J Register (Offset = 100h) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

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Table 14-9032. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 0100h + formula

Figure 14-4485. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-9033. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n

Table 14-9033. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n

Table 14-9033. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.5.2.8 MAILBOX_USER_IRQ_STATUS_CLR_J Register

14.4.5.2.8.1 MAILBOX_USER_IRQ_STATUS_CLR_J Register (Offset = 104h) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

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Table 14-9034. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 0104h + formula

Figure 14-4486. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9035. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-9035. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n

Table 14-9035. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.5.2.9 MAILBOX_USER_IRQ_ENABLE_SET_J Register

14.4.5.2.9.1 MAILBOX_USER_IRQ_ENABLE_SET_J Register (Offset = 108h) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

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Table 14-9036. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 0108h + formula

Figure 14-4487. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9037. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9037. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9037. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.5.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_J Register

14.4.5.2.10.1 MAILBOX_USER_IRQ_ENABLE_CLR_J Register (Offset = 10Ch) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

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Table 14-9038. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_4	2904 010Ch + formula

Figure 14-4488. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9039. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9039. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9039. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.6 MAILBOX_MAILBOX_CLUSTER_5

MAILBOX_MAILBOX_CLUSTER_5

14.4.6.1 MAILBOX_MAILBOX_CLUSTER_5 Summaries

MAILBOX_MAILBOX_CLUSTER_5 Summaries

Table 14-9040. MAILBOX Registers, Base Address=2905 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_5 Physical Address
0h	32	MAILBOX_REVISION	2905 0000h
10h	32	MAILBOX_SYSCONFIG	2905 0010h
40h	32	MAILBOX_MESSAGE_J	2905 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2905 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2905 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2905 0140h
100h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2905 0100h + formula
104h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2905 0104h + formula
108h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2905 0108h + formula
10Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2905 010Ch + formula

14.4.6.2 MAILBOX_MAILBOX_CLUSTER_5 Registers

MAILBOX_MAILBOX_CLUSTER_5 Registers

14.4.6.2.1 MAILBOX_REVISION Register

14.4.6.2.1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-9041. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 0000h

Figure 14-4489. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
6FCh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-9042. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.6.2.2 MAILBOX_SYSCONFIG Register

14.4.6.2.2.1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

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Table 14-9043. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 0010h

Figure 14-4490. MAILBOX_SYSCONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFT_RESET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9044. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.6.2.3 MAILBOX_MESSAGE_J Register

14.4.6.2.3.1 MAILBOX_MESSAGE_J Register (Offset = 40h) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

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Table 14-9045. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 0040h + formula

Figure 14-4491. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-9046. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.6.2.4 MAILBOX_FIFO_STATUS_J Register

14.4.6.2.4.1 MAILBOX_FIFO_STATUS_J Register (Offset = 80h) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

Return to Summary Table

Table 14-9047. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 0080h + formula

Figure 14-4492. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-9048. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.6.2.5 MAILBOX_MSG_STATUS_J Register

14.4.6.2.5.1 MAILBOX_MSG_STATUS_J Register (Offset = C0h) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Table 14-9049. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 00C0h + formula

Figure 14-4493. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-9050. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.6.2.6 MAILBOX_IRQ_EOI Register

14.4.6.2.6.1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

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Table 14-9051. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 0140h

Figure 14-4494. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-9052. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.6.2.7 MAILBOX_USER_IRQ_STATUS_RAW_J Register

14.4.6.2.7.1 MAILBOX_USER_IRQ_STATUS_RAW_J Register (Offset = 100h) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

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Table 14-9053. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 0100h + formula

Figure 14-4495. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-9054. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n

Table 14-9054. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n

Table 14-9054. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.6.2.8 MAILBOX_USER_IRQ_STATUS_CLR_J Register

14.4.6.2.8.1 MAILBOX_USER_IRQ_STATUS_CLR_J Register (Offset = 104h) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

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Table 14-9055. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 0104h + formula

Figure 14-4496. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9056. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-9056. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n

Table 14-9056. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.6.2.9 MAILBOX_USER_IRQ_ENABLE_SET_J Register

14.4.6.2.9.1 MAILBOX_USER_IRQ_ENABLE_SET_J Register (Offset = 108h) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

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Table 14-9057. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 0108h + formula

Figure 14-4497. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9058. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9058. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9058. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.6.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_J Register

14.4.6.2.10.1 MAILBOX_USER_IRQ_ENABLE_CLR_J Register (Offset = 10Ch) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Return to Summary Table

Table 14-9059. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_5	2905 010Ch + formula

Figure 14-4498. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9060. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9060. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9060. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.7 MAILBOX_MAILBOX_CLUSTER_6

MAILBOX_MAILBOX_CLUSTER_6

14.4.7.1 MAILBOX_MAILBOX_CLUSTER_6 Summaries

MAILBOX_MAILBOX_CLUSTER_6 Summaries

Table 14-9061. MAILBOX Registers, Base Address=2906 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_6 Physical Address
0h	32	MAILBOX_REVISION	2906 0000h
10h	32	MAILBOX_SYSCONFIG	2906 0010h
40h	32	MAILBOX_MESSAGE_J	2906 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2906 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2906 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2906 0140h
100h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2906 0100h + formula
104h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2906 0104h + formula
108h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2906 0108h + formula
10Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2906 010Ch + formula

14.4.7.2 MAILBOX_MAILBOX_CLUSTER_6 Registers

MAILBOX_MAILBOX_CLUSTER_6 Registers

14.4.7.2.1 MAILBOX_REVISION Register

14.4.7.2.1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-9062. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0000h

Figure 14-4499. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-9063. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.7.2.2 MAILBOX_SYSCONFIG Register

14.4.7.2.2.1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

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Table 14-9064. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0010h

Figure 14-4500. MAILBOX_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 14-9065. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.7.2.3 MAILBOX_MESSAGE_J Register

14.4.7.2.3.1 MAILBOX_MESSAGE_J Register (Offset = 40h) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

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Table 14-9066. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0040h + formula

Figure 14-4501. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-9067. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.7.2.4 MAILBOX_FIFO_STATUS_J Register

14.4.7.2.4.1 MAILBOX_FIFO_STATUS_J Register (Offset = 80h) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

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Table 14-9068. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0080h + formula

Figure 14-4502. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-9069. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.7.2.5 MAILBOX_MSG_STATUS_J Register

14.4.7.2.5.1 MAILBOX_MSG_STATUS_J Register (Offset = C0h) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

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Table 14-9070. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 00C0h + formula

Figure 14-4503. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-9071. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.7.2.6 MAILBOX_IRQ_EOI Register

14.4.7.2.6.1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

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Table 14-9072. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0140h

Figure 14-4504. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-9073. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.7.2.7 MAILBOX_USER_IRQ_STATUS_RAW_J Register

14.4.7.2.7.1 MAILBOX_USER_IRQ_STATUS_RAW_J Register (Offset = 100h) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

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Table 14-9074. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0100h + formula

Figure 14-4505. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-9075. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n

Table 14-9075. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n

Table 14-9075. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.7.2.8 MAILBOX_USER_IRQ_STATUS_CLR_J Register

14.4.7.2.8.1 MAILBOX_USER_IRQ_STATUS_CLR_J Register (Offset = 104h) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

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Table 14-9076. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0104h + formula

Figure 14-4506. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9077. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-9077. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n

Table 14-9077. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.7.2.9 MAILBOX_USER_IRQ_ENABLE_SET_J Register

14.4.7.2.9.1 MAILBOX_USER_IRQ_ENABLE_SET_J Register (Offset = 108h) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

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Table 14-9078. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 0108h + formula

Figure 14-4507. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9079. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9079. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9079. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.7.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_J Register

14.4.7.2.10.1 MAILBOX_USER_IRQ_ENABLE_CLR_J Register (Offset = 10Ch) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

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Table 14-9080. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_6	2906 010Ch + formula

Figure 14-4508. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9081. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9081. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9081. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.8 MAILBOX_MAILBOX_CLUSTER_7

MAILBOX_MAILBOX_CLUSTER_7

14.4.8.1 MAILBOX_MAILBOX_CLUSTER_7 Summaries

MAILBOX_MAILBOX_CLUSTER_7 Summaries

Table 14-9082. MAILBOX Registers, Base Address=2907 0000h, Length=512

Offset	Length	Register Name	MAILBOX0_MAILBOX_CLUSTER_7 Physical Address
0h	32	MAILBOX_REVISION	2907 0000h
10h	32	MAILBOX_SYSCONFIG	2907 0010h
40h	32	MAILBOX_MESSAGE_J	2907 0040h + formula
80h	32	MAILBOX_FIFO_STATUS_J	2907 0080h + formula
C0h	32	MAILBOX_MSG_STATUS_J	2907 00C0h + formula
140h	32	MAILBOX_IRQ_EOI	2907 0140h
100h	32	MAILBOX_USER_IRQ_STATUS_RAW_J	2907 0100h + formula
104h	32	MAILBOX_USER_IRQ_STATUS_CLR_J	2907 0104h + formula
108h	32	MAILBOX_USER_IRQ_ENABLE_SET_J	2907 0108h + formula
10Ch	32	MAILBOX_USER_IRQ_ENABLE_CLR_J	2907 010Ch + formula

14.4.8.2 MAILBOX_MAILBOX_CLUSTER_7 Registers

MAILBOX_MAILBOX_CLUSTER_7 Registers

14.4.8.2.1 MAILBOX_REVISION Register

14.4.8.2.1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = 66FC9100h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-9083. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 0000h

Figure 14-4509. MAILBOX_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FCh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FCh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
12h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-9084. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: rst_n
29:28	BU	R	2h	BU identifier Reset Source: rst_n
27:16	FUNCTION	R	6FCh	Module family. Reset Source: rst_n
15:11	RTL_VER	R	12h	RTL version. R of X.Y.R.Z Reset Source: rst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: rst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: rst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: rst_n

14.4.8.2.2 MAILBOX_SYSCONFIG Register

14.4.8.2.2.1 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = 0h]

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

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Table 14-9085. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 0010h

Figure 14-4510. MAILBOX_SYSCONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFT_RESET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9086. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes Reset Source: rst_n

14.4.8.2.3 MAILBOX_MESSAGE_J Register

14.4.8.2.3.1 MAILBOX_MESSAGE_J Register (Offset = 40h) [reset = 0h]

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

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Table 14-9087. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 0040h + formula

Figure 14-4511. MAILBOX_MESSAGE_j Name Register

31	30	29	28	27	26	25	24
MESSAGE_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MESSAGE_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MESSAGE_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MESSAGE_VALUE							
R/W							
0h							

Table 14-9088. MAILBOX_MESSAGE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MESSAGE_VALUE	R/W	0h	Message in Mailbox [a] Reset Source: rst_n

14.4.8.2.4 MAILBOX_FIFO_STATUS_J Register

14.4.8.2.4.1 MAILBOX_FIFO_STATUS_J Register (Offset = 80h) [reset = 0h]

The FIFO status register has the status of the Mailbox[a] FIFO

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Table 14-9089. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 0080h + formula

Figure 14-4512. MAILBOX_FIFO_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FIFO_FULL
NONE							R
0h							0h

Table 14-9090. MAILBOX_FIFO_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FIFO_FULL	R	0h	Full flag for Mailbox m Reset Source: rst_n

14.4.8.2.5 MAILBOX_MSG_STATUS_J Register

14.4.8.2.5.1 MAILBOX_MSG_STATUS_J Register (Offset = C0h) [reset = 0h]

The message status register has the status of the messages in Mailbox[a]

Return to Summary Table

Table 14-9091. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 00C0h + formula

Figure 14-4513. MAILBOX_MSG_STATUS_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
NONE					R		
0h					0h		

Table 14-9092. MAILBOX_MSG_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	NUM_MESSAGES	R	0h	Number of messages in Mailbox[a] Reset Source: rst_n

14.4.8.2.6 MAILBOX_IRQ_EOI Register

14.4.8.2.6.1 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = 0h]

This is the EOI register with which the software is enabled to do the interrupt clearance.

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Table 14-9093. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 0140h

Figure 14-4514. MAILBOX_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
NONE				W	W	W	W
0h				0h	0h	0h	0h

Table 14-9094. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt Reset Source: rst_n
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt Reset Source: rst_n
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt Reset Source: rst_n
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt Reset Source: rst_n

14.4.8.2.7 MAILBOX_USER_IRQ_STATUS_RAW_J Register

14.4.8.2.7.1 MAILBOX_USER_IRQ_STATUS_RAW_J Register (Offset = 100h) [reset = AAAAAAAAh]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user . Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Return to Summary Table

Table 14-9095. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 0100h + formula

Figure 14-4515. MAILBOX_USER_IRQ_STATUS_RAW_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	1h	0h	1h	0h	1h	0h

Table 14-9096. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full Reset Source: rst_n
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full Reset Source: rst_n

Table 14-9096. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 Reset Source: rst_n
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 Reset Source: rst_n

Table 14-9096. MAILBOX_USER_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 Reset Source: rst_n

14.4.8.2.8 MAILBOX_USER_IRQ_STATUS_CLR_J Register

14.4.8.2.8.1 MAILBOX_USER_IRQ_STATUS_CLR_J Register (Offset = 104h) [reset = 0h]

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

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Table 14-9097. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 0104h + formula

Figure 14-4516. MAILBOX_USER_IRQ_STATUS_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLSTATUSMB15	NEWMSGSTATUSMB15	NOTFULLSTATUSMB14	NEWMSGSTATUSMB14	NOTFULLSTATUSMB13	NEWMSGSTATUSMB13	NOTFULLSTATUSMB12	NEWMSGSTATUSMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLSTATUSMB11	NEWMSGSTATUSMB11	NOTFULLSTATUSMB10	NEWMSGSTATUSMB10	NOTFULLSTATUSMB9	NEWMSGSTATUSMB9	NOTFULLSTATUSMB8	NEWMSGSTATUSMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLSTATUSMB7	NEWMSGSTATUSMB7	NOTFULLSTATUSMB6	NEWMSGSTATUSMB6	NOTFULLSTATUSMB5	NEWMSGSTATUSMB5	NOTFULLSTATUSMB4	NEWMSGSTATUSMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLSTATUSMB3	NEWMSGSTATUSMB3	NOTFULLSTATUSMB2	NEWMSGSTATUSMB2	NOTFULLSTATUSMB1	NEWMSGSTATUSMB1	NOTFULLSTATUSMB0	NEWMSGSTATUSMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9098. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled Reset Source: rst_n
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled Reset Source: rst_n
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled Reset Source: rst_n
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled Reset Source: rst_n
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled Reset Source: rst_n

Table 14-9098. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled Reset Source: rst_n
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled Reset Source: rst_n
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled Reset Source: rst_n
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled Reset Source: rst_n
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled Reset Source: rst_n
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled Reset Source: rst_n
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled Reset Source: rst_n
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled Reset Source: rst_n
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled Reset Source: rst_n
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled Reset Source: rst_n
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled Reset Source: rst_n
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled Reset Source: rst_n
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled Reset Source: rst_n
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled Reset Source: rst_n
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled Reset Source: rst_n
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled Reset Source: rst_n
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled Reset Source: rst_n
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled Reset Source: rst_n
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled Reset Source: rst_n

Table 14-9098. MAILBOX_USER_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled Reset Source: rst_n
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled Reset Source: rst_n
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled Reset Source: rst_n
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled Reset Source: rst_n
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled Reset Source: rst_n
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled Reset Source: rst_n
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled Reset Source: rst_n
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled Reset Source: rst_n

14.4.8.2.9 MAILBOX_USER_IRQ_ENABLE_SET_J Register

14.4.8.2.9.1 MAILBOX_USER_IRQ_ENABLE_SET_J Register (Offset = 108h) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

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Table 14-9099. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 0108h + formula

Figure 14-4517. MAILBOX_USER_IRQ_ENABLE_SET_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9100. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9100. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9100. MAILBOX_USER_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.8.2.10 MAILBOX_USER_IRQ_ENABLE_CLR_J Register

14.4.8.2.10.1 MAILBOX_USER_IRQ_ENABLE_CLR_J Register (Offset = 10Ch) [reset = 0h]

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user [a]. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

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Table 14-9101. Instance Table

Instance Name	Physical Address
MAILBOX0_MAILBOX_CLUSTER_7	2907 010Ch + formula

Figure 14-4518. MAILBOX_USER_IRQ_ENABLE_CLR_j Name Register

31	30	29	28	27	26	25	24
NOTFULLENABLEMB15	NEWMSGENABLEMB15	NOTFULLENABLEMB14	NEWMSGENABLEMB14	NOTFULLENABLEMB13	NEWMSGENABLEMB13	NOTFULLENABLEMB12	NEWMSGENABLEMB12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NOTFULLENABLEMB11	NEWMSGENABLEMB11	NOTFULLENABLEMB10	NEWMSGENABLEMB10	NOTFULLENABLEMB9	NEWMSGENABLEMB9	NOTFULLENABLEMB8	NEWMSGENABLEMB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NOTFULLENABLEMB7	NEWMSGENABLEMB7	NOTFULLENABLEMB6	NEWMSGENABLEMB6	NOTFULLENABLEMB5	NEWMSGENABLEMB5	NOTFULLENABLEMB4	NEWMSGENABLEMB4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOTFULLENABLEMB3	NEWMSGENABLEMB3	NOTFULLENABLEMB2	NEWMSGENABLEMB2	NOTFULLENABLEMB1	NEWMSGENABLEMB1	NOTFULLENABLEMB0	NEWMSGENABLEMB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9102. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9102. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

Table 14-9102. MAILBOX_USER_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 does nothing. Reset Source: rst_n

14.4.9 SPINLOCK

SPINLOCK

14.4.9.1 SPINLOCK Summaries

SPINLOCK Summaries

Table 14-9103. SPINLOCK Registers, Base Address=2A00 0000h, Length=32768

Offset	Length	Register Name	SPINLOCK0 Physical Address
0h	32	SPINLOCK_REVISION	2A00 0000h
10h	32	SPINLOCK_SYSCONFIG	2A00 0010h
14h	32	SPINLOCK_SYSTATUS	2A00 0014h
800h	32	SPINLOCK_LOCK_REG_J	2A00 0800h + formula

14.4.9.2 SPINLOCK Registers

SPINLOCK Registers

14.4.9.2.1 SPINLOCK_REVISION Register

14.4.9.2.1.1 SPINLOCK_REVISION Register (Offset = 0h) [reset = 66FA6900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 14-9104. Instance Table

Instance Name	Physical Address
SPINLOCK0	2A00 0000h

Figure 14-4519. SPINLOCK_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FAh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FAh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
Dh					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 14-9105. SPINLOCK_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: core_srst_n
29:28	BU	R	2h	BU identifier Reset Source: core_srst_n
27:16	FUNCTION	R	6FAh	Module family. Reset Source: core_srst_n
15:11	RTL_VER	R	Dh	RTL version. R of X.Y.R.Z Reset Source: core_srst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: core_srst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: core_srst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: core_srst_n

14.4.9.2.2 SPINLOCK_SYSCONFIG Register

14.4.9.2.2.1 SPINLOCK_SYSCONFIG Register (Offset = 10h) [reset = 0h]

Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock

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Table 14-9106. Instance Table

Instance Name	Physical Address
SPINLOCK0	2A00 0010h

Figure 14-4520. SPINLOCK_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT_RESET	RESERVED
NONE						R/W	NONE
0h						0h	0h

Table 14-9107. SPINLOCK_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0 It has the same effect as the hardware reset Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks Reset Source: core_srst_n
0	RESERVED	NONE	0h	Reserved

14.4.9.2.3 SPINLOCK_SYSTATUS Register

14.4.9.2.3.1 SPINLOCK_SYSTATUS Register (Offset = 14h) [reset = 8000000h]

Provides information about the Spinlock module

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Table 14-9108. Instance Table

Instance Name	Physical Address
SPINLOCK0	2A00 0014h

Figure 14-4521. SPINLOCK_SYSTATUS Name Register

31	30	29	28	27	26	25	24
NUM_LOCKS							
R							
8h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IN_USE7	IN_USE6	IN_USE5	IN_USE4	IN_USE3	IN_USE2	IN_USE1	IN_USE0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9109. SPINLOCK_SYSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NUM_LOCKS	R	8h	Module configuration parameter n, the total number of spinlocks divided by 32. e.g. For 256 spin locks, this will return the number 0x08 Reset Source: core_srst_n
23:8	RESERVED	NONE	0h	Reserved
7	IN_USE7	R	0h	In-Use flag 7 covering lock registers 224 - 255. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 224 - 255 are in the Not Taken state Read 1 : At least one of the lock registers 224 - 255 are in the Taken state Reset Source: core_srst_n
6	IN_USE6	R	0h	In-Use flag 6 covering lock registers 192 - 223. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 192 - 223 are in the Not Taken state Read 1 : At least one of the lock registers 192 - 223 are in the Taken state Reset Source: core_srst_n
5	IN_USE5	R	0h	In-Use flag 5 covering lock registers 160 - 191. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 160 - 191 are in the Not Taken state Read 1 : At least one of the lock registers 160 - 191 are in the Taken state Reset Source: core_srst_n

Table 14-9109. SPINLOCK_SYSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IN_USE4	R	0h	In-Use flag 4 covering lock registers 128 - 159. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 128 - 159 are in the Not Taken state Read 1 : At least one of the lock registers 128 - 159 are in the Taken state Reset Source: core_srst_n
3	IN_USE3	R	0h	In-Use flag 3 covering lock registers 96 - 127. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 96 - 127 are in the Not Taken state Read 1 : At least one of the lock registers 96 - 127 are in the Taken state Reset Source: core_srst_n
2	IN_USE2	R	0h	In-Use flag 2 covering lock registers 64 - 95. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 64 - 95 are in the Not Taken state Read 1 : At least one of the lock registers 64 - 95 are in the Taken state Reset Source: core_srst_n
1	IN_USE1	R	0h	In-Use flag 1 covering lock registers 32 - 63. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 32 - 63 are in the Not Taken state Read 1 : At least one of the lock registers 32 - 63 are in the Taken state Reset Source: core_srst_n
0	IN_USE0	R	0h	In-Use flag 0 covering lock registers 0 - 31. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 0 - 31 are in the Not Taken state Read 1 : At least one of the lock registers 0 - 31 are in the Taken state Reset Source: core_srst_n

14.4.9.2.4 SPINLOCK_LOCK_REG_J Register

14.4.9.2.4.1 SPINLOCK_LOCK_REG_J Register (Offset = 800h) [reset = 0h]

The Lock[a] register is read and written to perform lock and unlock operations on lock 'a'

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Table 14-9110. Instance Table

Instance Name	Physical Address
SPINLOCK0	2A00 0800h + formula

Figure 14-4522. SPINLOCK_LOCK_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TAKEN
NONE							R/W
0h							0h

Table 14-9111. SPINLOCK_LOCK_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TAKEN	R/W	0h	Lock Status Read 0 : Lock was previously free. The reader now has been granted the lock. Read 1 : Lock was previously taken. The reader has not been granted the lock and must retry. Write 0 : Free the lock by setting TAKEN to zero. Write 1 : No effect Reset Source: core_srst_n

14.5 Interrupt Router Registers

14.5.1 MAIN_GPIOMUX_INTROUTER

MAIN_GPIOMUX_INTROUTER

14.5.1.1 MAIN_GPIOMUX_INTROUTER Summaries

MAIN_GPIOMUX_INTROUTER Summaries

Table 14-9112. INTR_ROUTER_CFG Registers, Base Address=00A0 0000h, Length=4096

Offset	Length	Register Name	MAIN_GPIOMUX_INTROUTER0 Physical Address
0h	32	INTR_ROUTER_CFG_PID	00A0 0000h
4h	32	INTR_ROUTER_CFG_MUXCNTL_J	00A0 0004h + formula

14.5.1.2 MAIN_GPIOMUX_INTROUTER Registers

MAIN_GPIOMUX_INTROUTER Registers

14.5.1.2.1 INTR_ROUTER_CFG_PID Register

14.5.1.2.1.1 INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Identification register

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Table 14-9113. Instance Table

Instance Name	Physical Address
MAIN_GPIOMUX_INTROUTER0	00A0 0000h

Figure 14-4523. INTR_ROUTER_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
694h							
15	14	13	12	11	10	9	8
RTLVER					MAJREV		
R					R		
10h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-9114. INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	Business Unit Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

14.5.1.2.2 INTR_ROUTER_CFG_MUXCNTL_J Register

14.5.1.2.2.1 INTR_ROUTER_CFG_MUXCNTL_J Register (Offset = 4h) [reset = 0h]

Interrupt mux control register

Return to Summary Table

Table 14-9115. Instance Table

Instance Name	Physical Address
MAIN_GPIOMUX_INTROUTER0	00A0 0004h + formula

Figure 14-4524. INTR_ROUTER_CFG_MUXCNTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>INT_ENABLE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MUX_CNTL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9116. INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:8	RESERVED	NONE	0h	Reserved
7:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

14.5.2 MCU_GPIOMUX_INTROUTER

MCU_GPIOMUX_INTROUTER

14.5.2.1 MCU_GPIOMUX_INTROUTER Summaries

MCU_GPIOMUX_INTROUTER Summaries

Table 14-9117. INTR_ROUTER_CFG Registers, Base Address=0421 0000h, Length=1024

Offset	Length	Register Name	MCU_MCU_GPIOMUX_INTROUTER0 Physical Address
0h	32	INTR_ROUTER_CFG_PID	0421 0000h
4h	32	INTR_ROUTER_CFG_MUXCNTL_J	0421 0004h + formula

14.5.2.2 MCU_GPIOMUX_INTROUTER Registers

MCU_GPIOMUX_INTROUTER Registers

14.5.2.2.1 INTR_ROUTER_CFG_PID Register

14.5.2.2.1.1 INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Identification register

Return to Summary Table

Table 14-9118. Instance Table

Instance Name	Physical Address
MCU_MCU_GPIOMUX_INTROUTER0	0421 0000h

Figure 14-4525. INTR_ROUTER_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
694h							
15	14	13	12	11	10	9	8
RTLVER					MAJREV		
R					R		
10h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-9119. INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	Business Unit Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

14.5.2.2.2 INTR_ROUTER_CFG_MUXCNTL_J Register

14.5.2.2.2.1 INTR_ROUTER_CFG_MUXCNTL_J Register (Offset = 4h) [reset = 0h]

Interrupt mux control register

Return to Summary Table

Table 14-9120. Instance Table

Instance Name	Physical Address
MCU_MCU_GPIOMUX_INTROUTER0	0421 0004h + formula

Figure 14-4526. INTR_ROUTER_CFG_MUXCNTL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							INT_ENABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			MUX_CNTL				
NONE			R/W				
0h			0h				

Table 14-9121. INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:5	RESERVED	NONE	0h	Reserved
4:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

14.6 DMA Controller Registers

14.6.1 DMASS_BCDMA_0

DMASS_BCDMA_0

14.6.1.1 DMASS_BCDMA_0 Summaries

DMASS_BCDMA_0 Summaries

Table 14-9122. LCDMA_RINGACC_CRED Registers, Base Address=4581 2000h, Length=2048

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	LCDMA_RINGACC_CRED_RING_CRED_J	4581 2000h + formula

Table 14-9123. BCDMA_BCCFG Registers, Base Address=4842 0000h, Length=8192

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_BCCFG_CHAN_CFG_J	4842 0000h + formula
64h	32	BCDMA_BCCFG_CHAN_PRI_CTRL_J	4842 0064h + formula
80h	32	BCDMA_BCCFG_CHAN_TST_SCHED_J	4842 0080h + formula

Table 14-9124. BCDMA_TXCCFG Registers, Base Address=484A 4000h, Length=16384

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_TXCCFG_CHAN_TCFG_J	484A 4000h + formula
64h	32	BCDMA_TXCCFG_CHAN_TPRI_CTRL_J	484A 4064h + formula
68h	32	BCDMA_TXCCFG_CHAN_THREAD_J	484A 4068h + formula
70h	32	BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_J	484A 4070h + formula
80h	32	BCDMA_TXCCFG_CHAN_TST_SCHED_J	484A 4080h + formula

Table 14-9125. BCDMA_RXCCFG Registers, Base Address=484C 4000h, Length=16384

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_RXCCFG_CHAN_RCFG_J	484C 4000h + formula
64h	32	BCDMA_RXCCFG_CHAN_RPRI_CTRL_J	484C 4064h + formula
68h	32	BCDMA_RXCCFG_CHAN_THREAD_J	484C 4068h + formula
80h	32	BCDMA_RXCCFG_CHAN_RST_SCHED_J	484C 4080h + formula

Table 14-9126. BCDMA_GCFG Registers, Base Address=485C 0100h, Length=256

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_GCFG_REVISION	485C 0100h
4h	32	BCDMA_GCFG_PERF_CTRL	485C 0104h
8h	32	BCDMA_GCFG_EMU_CTRL	485C 0108h
10h	32	BCDMA_GCFG_PSIL_TO	485C 0110h
20h	32	BCDMA_GCFG_CAP0	485C 0120h
24h	32	BCDMA_GCFG_CAP1	485C 0124h
28h	32	BCDMA_GCFG_CAP2	485C 0128h
2Ch	32	BCDMA_GCFG_CAP3	485C 012Ch
30h	32	BCDMA_GCFG_CAP4	485C 0130h
60h	32	BCDMA_GCFG_PM0	485C 0160h
64h	32	BCDMA_GCFG_PM1	485C 0164h
78h	32	BCDMA_GCFG_DBGADDR	485C 0178h
7Ch	32	BCDMA_GCFG_DBGDATA	485C 017Ch

Table 14-9127. LCDMA_RINGACC_RING_CFG Registers, Base Address=4860 0000h, Length=32768

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
40h	32	LCDMA_RINGACC_RING_CFG_RING_BA_LO_J	4860 0040h + formula
44h	32	LCDMA_RINGACC_RING_CFG_RING_BA_HI_J	4860 0044h + formula
48h	32	LCDMA_RINGACC_RING_CFG_RING_SIZE_J	4860 0048h + formula

Table 14-9128. BCDMA_RXCRT Registers, Base Address=4A84 0000h, Length=262144

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_RXCRT_CHAN_CTL_J	4A84 0000h + formula
8h	32	BCDMA_RXCRT_CHAN_SWTRIG_J	4A84 0008h + formula
40h	32	BCDMA_RXCRT_CHAN_STATUS0_J	4A84 0040h + formula
44h	32	BCDMA_RXCRT_CHAN_STATUS1_J	4A84 0044h + formula
80h	32	BCDMA_RXCRT_CHAN_STDATA_J_K	4A84 0080h + formula
200h	32	BCDMA_RXCRT_CHAN_PEER0_J	4A84 0200h + formula
204h	32	BCDMA_RXCRT_CHAN_PEER1_J	4A84 0204h + formula
208h	32	BCDMA_RXCRT_CHAN_PEER2_J	4A84 0208h + formula
20Ch	32	BCDMA_RXCRT_CHAN_PEER3_J	4A84 020Ch + formula
210h	32	BCDMA_RXCRT_CHAN_PEER4_J	4A84 0210h + formula
214h	32	BCDMA_RXCRT_CHAN_PEER5_J	4A84 0214h + formula
218h	32	BCDMA_RXCRT_CHAN_PEER6_J	4A84 0218h + formula
21Ch	32	BCDMA_RXCRT_CHAN_PEER7_J	4A84 021Ch + formula
220h	32	BCDMA_RXCRT_CHAN_PEER8_J	4A84 0220h + formula
224h	32	BCDMA_RXCRT_CHAN_PEER9_J	4A84 0224h + formula
228h	32	BCDMA_RXCRT_CHAN_PEER10_J	4A84 0228h + formula
22Ch	32	BCDMA_RXCRT_CHAN_PEER11_J	4A84 022Ch + formula
230h	32	BCDMA_RXCRT_CHAN_PEER12_J	4A84 0230h + formula
234h	32	BCDMA_RXCRT_CHAN_PEER13_J	4A84 0234h + formula
238h	32	BCDMA_RXCRT_CHAN_PEER14_J	4A84 0238h + formula
23Ch	32	BCDMA_RXCRT_CHAN_PEER15_J	4A84 023Ch + formula
400h	32	BCDMA_RXCRT_CHAN_PCNT_J	4A84 0400h + formula
408h	32	BCDMA_RXCRT_CHAN_BCNT_J	4A84 0408h + formula
410h	32	BCDMA_RXCRT_CHAN_SBCNT_J	4A84 0410h + formula

Table 14-9129. BCDMA_TXCRT Registers, Base Address=4AA4 0000h, Length=262144

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_TXCRT_CHAN_CTL_J	4AA4 0000h + formula
8h	32	BCDMA_TXCRT_CHAN_SWTRIG_J	4AA4 0008h + formula
40h	32	BCDMA_TXCRT_CHAN_STATUS0_J	4AA4 0040h + formula
44h	32	BCDMA_TXCRT_CHAN_STATUS1_J	4AA4 0044h + formula
80h	32	BCDMA_TXCRT_CHAN_STDATA_J_K	4AA4 0080h + formula
200h	32	BCDMA_TXCRT_CHAN_PEER0_J	4AA4 0200h + formula
204h	32	BCDMA_TXCRT_CHAN_PEER1_J	4AA4 0204h + formula
208h	32	BCDMA_TXCRT_CHAN_PEER2_J	4AA4 0208h + formula
20Ch	32	BCDMA_TXCRT_CHAN_PEER3_J	4AA4 020Ch + formula
210h	32	BCDMA_TXCRT_CHAN_PEER4_J	4AA4 0210h + formula
214h	32	BCDMA_TXCRT_CHAN_PEER5_J	4AA4 0214h + formula
218h	32	BCDMA_TXCRT_CHAN_PEER6_J	4AA4 0218h + formula

Table 14-9129. BCDMA_TXCRT Registers, Base Address=4AA4 0000h, Length=262144 (continued)

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
21Ch	32	BCDMA_TXCRT_CHAN_PEER7_J	4AA4 021Ch + formula
220h	32	BCDMA_TXCRT_CHAN_PEER8_J	4AA4 0220h + formula
224h	32	BCDMA_TXCRT_CHAN_PEER9_J	4AA4 0224h + formula
228h	32	BCDMA_TXCRT_CHAN_PEER10_J	4AA4 0228h + formula
22Ch	32	BCDMA_TXCRT_CHAN_PEER11_J	4AA4 022Ch + formula
230h	32	BCDMA_TXCRT_CHAN_PEER12_J	4AA4 0230h + formula
234h	32	BCDMA_TXCRT_CHAN_PEER13_J	4AA4 0234h + formula
238h	32	BCDMA_TXCRT_CHAN_PEER14_J	4AA4 0238h + formula
23Ch	32	BCDMA_TXCRT_CHAN_PEER15_J	4AA4 023Ch + formula
400h	32	BCDMA_TXCRT_CHAN_PCNT_J	4AA4 0400h + formula
408h	32	BCDMA_TXCRT_CHAN_BCNT_J	4AA4 0408h + formula
410h	32	BCDMA_TXCRT_CHAN_SBCNT_J	4AA4 0410h + formula

Table 14-9130. LCDMA_RINGACC_RINGRT Registers, Base Address=4BC0 0000h, Length=1048576

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
10h	32	LCDMA_RINGACC_RINGRT_RING_FDB_J	4BC0 0010h + formula
18h	32	LCDMA_RINGACC_RINGRT_RING_FOCC_J	4BC0 0018h + formula
1010h	32	LCDMA_RINGACC_RINGRT_RING_RDB_J	4BC0 1010h + formula
1018h	32	LCDMA_RINGACC_RINGRT_RING_ROCC_J	4BC0 1018h + formula

Table 14-9131. BCDMA_BCRT Registers, Base Address=4C00 0000h, Length=262144

Offset	Length	Register Name	DMASS0_BCDMA_0 Physical Address
0h	32	BCDMA_BCRT_CHAN_CTL_J	4C00 0000h + formula
8h	32	BCDMA_BCRT_CHAN_SWTRIG_J	4C00 0008h + formula
40h	32	BCDMA_BCRT_CHAN_STATUS0_J	4C00 0040h + formula
44h	32	BCDMA_BCRT_CHAN_STATUS1_J	4C00 0044h + formula
48h	32	BCDMA_BCRT_CHAN_STATUS2_J	4C00 0048h + formula
4Ch	32	BCDMA_BCRT_CHAN_STATUS3_J	4C00 004Ch + formula
80h	32	BCDMA_BCRT_CHAN_STDATA_J_K	4C00 0080h + formula
100h	32	BCDMA_BCRT_CHAN_STDATAW_J_K	4C00 0100h + formula
400h	32	BCDMA_BCRT_CHAN_PCNT_J	4C00 0400h + formula
408h	32	BCDMA_BCRT_CHAN_BCNT_J	4C00 0408h + formula
410h	32	BCDMA_BCRT_CHAN_SBCNT_J	4C00 0410h + formula

14.6.1.2 DMASS_BCDMA_0 Registers

DMASS_BCDMA_0 Registers

14.6.1.2.1 LCDMA_RINGACC_CRED_RING_CRED_J Register

14.6.1.2.1.1 LCDMA_RINGACC_CRED_RING_CRED_J Register (Offset = 0h) [reset = 0h]

The Credentials Register provides credentials to be used when performing memory accesses using this flow.

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Table 14-9132. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4581 2000h + formula

Figure 14-4527. LCDMA_RINGACC_CRED_RING_CRED_j Name Register

31	30	29	28	27	26	25	24
RESERVED					SECURE	PRIV	
NONE					R/W	R/W	
0h					0h	0h	
23	22	21	20	19	18	17	16
PRIVID							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9133. LCDMA_RINGACC_CRED_RING_CRED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	SECURE	R/W	0h	Secure attribute Reset Source: rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Privelege attribute Reset Source: rst_mod_g_rst_n
23:16	PRIVID	R/W	0h	Privelege ID attribute Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.1.2.2 BCDMA_BCCFG_CHAN_CFG_J Register

14.6.1.2.2.1 BCDMA_BCCFG_CHAN_CFG_J Register (Offset = 0h) [reset = C0400h]

The Channel Configuration Register is used to initialize static mode settings for the Block Copy DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

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Table 14-9134. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4842 0000h + formula

Figure 14-4528. BCDMA_BCCFG_CHAN_CFG_j Name Register

31	30	29	28	27	26	25	24
PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				CHAN_TYPE			
NONE				R/NA			
0h				Ch			
15	14	13	12	11	10	9	8
RESERVED				BURST_SIZE		RESERVED	
NONE				R/W		NONE	
0h				1h		0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9135. BCDMA_BCCFG_CHAN_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	CHAN_TYPE	R/NA	Ch	Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-11 = RESERVED 12 = Channel performs Third Party Block Copy DMA transfers from memory to memory using pass by reference rings. 13-15 = RESERVED `12      Pass by reference block copy`
15:12	RESERVED	NONE	0h	Reserved
11:10	BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes All other values are reserved The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n
9:0	RESERVED	NONE	0h	Reserved

14.6.1.2.3 BCDMA_BCCFG_CHAN_PRI_CTRL_J Register

14.6.1.2.3.1 BCDMA_BCCFG_CHAN_PRI_CTRL_J Register (Offset = 64h) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

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Table 14-9136. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4842 0064h + formula

Figure 14-4529. BCDMA_BCCFG_CHAN_PRI_CTRL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="3">PRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ORDERID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9137. BCDMA_BCCFG_CHAN_PRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.4 BCDMA_BCCFG_CHAN_TST_SCHED_J Register

14.6.1.2.4.1 BCDMA_BCCFG_CHAN_TST_SCHED_J Register (Offset = 80h) [reset = 0h]

The Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

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Table 14-9138. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4842 0080h + formula

Figure 14-4530. BCDMA_BCCFG_CHAN_TST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-9139. BCDMA_BCCFG_CHAN_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx/Rx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.6.1.2.5 BCDMA_TXCCFG_CHAN_TCFG_J Register

14.6.1.2.5.1 BCDMA_TXCCFG_CHAN_TCFG_J Register (Offset = 0h) [reset = A0400h]

The Tx Channel Configuration Register is used to initialize static mode settings for the Tx DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

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Table 14-9140. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484A 4000h + formula

Figure 14-4531. BCDMA_TXCCFG_CHAN_TCFG_j Name Register

31	30	29	28	27	26	25	24
TX_PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				TX_CHAN_TYPE			
NONE				R/NA			
0h				Ah			
15	14	13	12	11	10	9	8
RESERVED				TX_BURST_SIZE		TX_TDTYPE	TX_NOTDPKT
NONE				R/W		R/W	R/W
0h				1h		0h	0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9141. BCDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	TX_CHAN_TYPE	R/NA	Ah	Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-9 = RESERVED 10 = Channel performs Third Party Block Copy DMA transfers from memory to PSI-L using pass by reference rings. 11-15 = RESERVED `12      Pass by reference block copy`
15:12	RESERVED	NONE	0h	Reserved
11:10	TX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes All other values are reserved The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n

Table 14-9141. BCDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	TX_TDTYPE	R/W	0h	Specifies whether or not the channel should immediately return a teardown completion response to the default completion queue or wait until a status message is returned from the remote PSI-L paired peripheral. 0 = return immediately once all traffic is complete in BCDMA. 1 = wait until remote peer sends back a completion message. Reset Source: rst_mod_g_rst_n
8	TX_NOTDPKT	R/W	0h	Specifies whether or not the channel should suppress sending the single data phase teardown packet when teardown is complete. 0 = TD packet is sent 1 = Suppress sending TD packet Reset Source: rst_mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.6.1.2.6 BCDMA_TXCCFG_CHAN_TPRI_CTRL_J Register

14.6.1.2.6.1 BCDMA_TXCCFG_CHAN_TPRI_CTRL_J Register (Offset = 64h) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

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Table 14-9142. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484A 4064h + formula

Figure 14-4532. BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-9143. BCDMA_TXCCFG_CHAN_TPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Tx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Tx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.7 BCDMA_TXCCFG_CHAN_THREAD_J Register

14.6.1.2.7.1 BCDMA_TXCCFG_CHAN_THREAD_J Register (Offset = 68h) [reset = 0h]

The thread ID mapping register is used to pair the Tx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

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Table 14-9144. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484A 4068h + formula

Figure 14-4533. BCDMA_TXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-9145. BCDMA_TXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.8 BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_J Register

14.6.1.2.8.1 BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_J Register (Offset = 70h) [reset = C0h]

The fifo depth register is used to specify how many FIFO data phases deep the Tx per channel FIFO will be for the channel. While the maximum depth of the Tx FIFO is set at design time, the FIFO depth can be artificially reduced in order to control the maximum latency which can be introduced due to buffering effects.

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Table 14-9146. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484A 4070h + formula

Figure 14-4534. BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FDEPTH							
R/W							
C0h							

Table 14-9147. BCDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDEPTH	R/W	C0h	FIFO Depth: This field contains the number of Tx FIFO bytes which will be allowed to be stored for the channel. The minimum value is equal to the PSI-L interface data path width (tstrm_wdth), the maximum value varies by channel class (ultra-high capacity/high capacity/normal capacity) and is equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L data path width (tstrm_wdth). The fdepth must always be an integer multiple of tstrm_wdth. The reset value of this register varies by channel class (ultra-high capacity/high capacity/normal capacity) but will be equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L interface data width (tstrm_wdth). Reset Source: rst_mod_g_rst_n

14.6.1.2.9 BCDMA_TXCCFG_CHAN_TST_SCHED_J Register

14.6.1.2.9.1 BCDMA_TXCCFG_CHAN_TST_SCHED_J Register (Offset = 80h) [reset = 0h]

The Tx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

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Table 14-9148. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484A 4080h + formula

Figure 14-4535. BCDMA_TXCCFG_CHAN_TST_SCHED_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PRIORITY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-9149. BCDMA_TXCCFG_CHAN_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Tx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.6.1.2.10 BCDMA_RXCCFG_CHAN_RCFG_J Register

14.6.1.2.10.1 BCDMA_RXCCFG_CHAN_RCFG_J Register (Offset = 0h) [reset = A0400h]

The Rx Channel Configuration Register is used to initialize static mode settings for the Rx DMA channel. This register may only be written when the channel is disabled (rx_enable in realtime control reg is 0).

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Table 14-9150. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484C 4000h + formula

Figure 14-4536. BCDMA_RXCCFG_CHAN_RCFG_j Name Register

31	30	29	28	27	26	25	24
RX_PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED				RX_CHAN_TYPE			
NONE				R/NA			
0h				Ah			
15	14	13	12	11	10	9	8
RESERVED	RX_IGNORE_LONG	RESERVED		RX_BURST_SIZE		RESERVED	
NONE	R/W	NONE		R/W		NONE	
0h	0h	0h		1h		0h	
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9151. BCDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	RX_CHAN_TYPE	R/NA	Ah	Rx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 0-9 = RESERVED 10 = Channel performs Third Party Block Copy DMA transfers from PSI-L to memory using pass by reference rings. 11-15 = RESERVED Reset Source: rst_mod_g_rst_n
15	RESERVED	NONE	0h	Reserved
14	RX_IGNORE_LONG	R/W	0h	This field controls whether or not long packets will be treated as exceptions or ignored for the channel. This field is only used when the channel is in split UTC mode. The values are encoded as follows: 0 = Long packets are treated as exceptions and handled appropriately. 1 = Long packets are ignored and the next TR will be fetched even if the current TR is marked or interpreted as EOP. Reset Source: rst_mod_g_rst_n

Table 14-9151. BCDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	RESERVED	NONE	0h	Reserved
11:10	RX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = 32 Bytes 1 = 64 Bytes only if the channel buffer size is greater than 128 bytes All other values are reserved The optimal burst size setting is 64 Bytes to maximize utilization of the channel FIFOs. Reset Source: rst_mod_g_rst_n
9:0	RESERVED	NONE	0h	Reserved

14.6.1.2.11 BCDMA_RXCCFG_CHAN_RPRI_CTRL_J Register

14.6.1.2.11.1 BCDMA_RXCCFG_CHAN_RPRI_CTRL_J Register (Offset = 64h) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

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Table 14-9152. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484C 4064h + formula

Figure 14-4537. BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-9153. BCDMA_RXCCFG_CHAN_RPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Rx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem*_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Rx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.12 BCDMA_RXCCFG_CHAN_THREAD_J Register

14.6.1.2.12.1 BCDMA_RXCCFG_CHAN_THREAD_J Register (Offset = 68h) [reset = 0h]

The thread ID mapping register is used to pair the Rx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

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Table 14-9154. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484C 4068h + formula

Figure 14-4538. BCDMA_RXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-9155. BCDMA_RXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.13 BCDMA_RXCCFG_CHAN_RST_SCHED_J Register

14.6.1.2.13.1 BCDMA_RXCCFG_CHAN_RST_SCHED_J Register (Offset = 80h) [reset = 0h]

The Rx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

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Table 14-9156. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	484C 4080h + formula

Figure 14-4539. BCDMA_RXCCFG_CHAN_RST_SCHED_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">PRIORITY</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-9157. BCDMA_RXCCFG_CHAN_RST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Rx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Rx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.6.1.2.14 BCDMA_GCFG_REVISION Register

14.6.1.2.14.1 BCDMA_GCFG_REVISION Register (Offset = 0h) [reset = 662ED101h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-9158. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0100h

Figure 14-4540. BCDMA_GCFG_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">662Eh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">662Eh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">1Ah</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-9159. BCDMA_GCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	662Eh	Module ID field Reset Source: rst_mod_g_rst_n
15:11	REVRTL	R	1Ah	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: rst_mod_g_rst_n

14.6.1.2.15 BCDMA_GCFG_PERF_CTRL Register

14.6.1.2.15.1 BCDMA_GCFG_PERF_CTRL Register (Offset = 4h) [reset = 40h]

The performance control register contains fields which can be used to adjust the performance of the BCDMA in the system.

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Table 14-9160. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0104h

Figure 14-4541. BCDMA_GCFG_PERF_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TIMEOUT_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">40h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TIMEOUT_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">40h</td></tr>
</table>

Table 14-9161. BCDMA_GCFG_PERF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TIMEOUT_CNT	R/W	40h	This feature is not currently supported. Reset Source: rst_mod_g_rst_n

14.6.1.2.16 BCDMA_GCFG_EMU_CTRL Register

14.6.1.2.16.1 BCDMA_GCFG_EMU_CTRL Register (Offset = 8h) [reset = 0h]

The emulation control register is used to control the behavior of the DMA when the emususp input is asserted.

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Table 14-9162. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0108h

Figure 14-4542. BCDMA_GCFG_EMU_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-9163. BCDMA_GCFG_EMU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Soft Reset Source: rst_mod_g_rst_n
0	FREE	R/W	0h	Free Reset Source: rst_mod_g_rst_n

14.6.1.2.17 BCDMA_GCFG_PSIL_TO Register

14.6.1.2.17.1 BCDMA_GCFG_PSIL_TO Register (Offset = 10h) [reset = 400h]

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrances on PSI-L configuration transactions issued by the built in PSI-L proxy.

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Table 14-9164. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0110h

Figure 14-4543. BCDMA_GCFG_PSIL_TO Name Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W							
400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W							
400h							

Table 14-9165. BCDMA_GCFG_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a conifiguration read or write transaction and asserting the tout bit Reset Source: rst_mod_g_rst_n

14.6.1.2.18 BCDMA_GCFG_CAP0 Register

14.6.1.2.18.1 BCDMA_GCFG_CAP0 Register (Offset = 20h) [reset = A800Fh]

The Capabilities Register 0 specifies which standard features this BCDMA instance supports.

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Table 14-9166. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0120h

Figure 14-4544. BCDMA_GCFG_CAP0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				GLOBAL_TRIG	LOCAL_TRIG	EOL	STATIC
NONE				R	R	R	R
0h				1h	0h	1h	0h
15	14	13	12	11	10	9	8
TYPE15	TYPE14	TYPE13	TYPE12	TYPE11	TYPE10	TYPE9	TYPE8
R	R	R	R	R	R	R	R
1h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TYPE7	TYPE6	TYPE5	TYPE4	TYPE3	TYPE2	TYPE1	TYPE0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	1h	1h	1h	1h

Table 14-9167. BCDMA_GCFG_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	GLOBAL_TRIG	R	1h	Global triggers 0 and 1 are supported Reset Source: rst_mod_g_rst_n
18	LOCAL_TRIG	R	0h	Dedicated local trigger is supported Reset Source: rst_mod_g_rst_n
17	EOL	R	1h	EOL field is supported Reset Source: rst_mod_g_rst_n
16	STATIC	R	0h	STATIC field is supported Reset Source: rst_mod_g_rst_n
15	TYPE15	R	1h	Type 15 TR is supported Reset Source: rst_mod_g_rst_n
14	TYPE14	R	0h	Type 14 TR is supported Reset Source: rst_mod_g_rst_n
13	TYPE13	R	0h	Type 13 TR is supported Reset Source: rst_mod_g_rst_n
12	TYPE12	R	0h	Type 12 TR is supported Reset Source: rst_mod_g_rst_n
11	TYPE11	R	0h	Type 11 TR is supported Reset Source: rst_mod_g_rst_n

Table 14-9167. BCDMA_GCFG_CAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TYPE10	R	0h	Type 10 TR is supported Reset Source: rst_mod_g_rst_n
9	TYPE9	R	0h	Type 9 TR is supported Reset Source: rst_mod_g_rst_n
8	TYPE8	R	0h	Type 8 TR is supported Reset Source: rst_mod_g_rst_n
7	TYPE7	R	0h	Type 7 TR is supported Reset Source: rst_mod_g_rst_n
6	TYPE6	R	0h	Type 6 TR is supported Reset Source: rst_mod_g_rst_n
5	TYPE5	R	0h	Type 5 TR is supported Reset Source: rst_mod_g_rst_n
4	TYPE4	R	0h	Type 4 TR is supported Reset Source: rst_mod_g_rst_n
3	TYPE3	R	1h	Type 3 TR is supported Reset Source: rst_mod_g_rst_n
2	TYPE2	R	1h	Type 2 TR is supported Reset Source: rst_mod_g_rst_n
1	TYPE1	R	1h	Type 1 TR is supported Reset Source: rst_mod_g_rst_n
0	TYPE0	R	1h	Type 0 TR is supported Reset Source: rst_mod_g_rst_n

14.6.1.2.19 BCDMA_GCFG_CAP1 Register

14.6.1.2.19.1 BCDMA_GCFG_CAP1 Register (Offset = 24h) [reset = 0h]

The Capabilities Register 1 specifies which standard features this BCDMA instance supports.

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Table 14-9168. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0124h

Figure 14-4545. BCDMA_GCFG_CAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SECTR	DFMT	ELTYPE	AMODE
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-9169. BCDMA_GCFG_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	SECTR	R	0h	Maximum second TR function that is supported Reset Source: rst_mod_g_rst_n
2	DFMT	R	0h	Maximum data reformatting function that is supported Reset Source: rst_mod_g_rst_n
1	ELTYPE	R	0h	Maximum element type value that is supported. Reset Source: rst_mod_g_rst_n
0	AMODE	R	0h	The maximum AMODE that is supported. If AMODE is supported then DIR field must be supported for that AMODE. Reset Source: rst_mod_g_rst_n

14.6.1.2.20 BCDMA_GCFG_CAP2 Register

14.6.1.2.20.1 BCDMA_GCFG_CAP2 Register (Offset = 28h) [reset = C86018h]

The Capabilities Register 2 specifies how many resources this BCDMA instance supports.

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Table 14-9170. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0128h

Figure 14-4546. BCDMA_GCFG_CAP2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">RCHAN_CNT</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">32h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RCHAN_CNT</td><td colspan="2">TCHAN_CNT</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">32h</td><td colspan="2">30h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">TCHAN_CNT</td><td>CHAN_CNT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">30h</td><td>18h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CHAN_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">18h</td></tr>
</table>

Table 14-9171. BCDMA_GCFG_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:18	RCHAN_CNT	R	32h	Rx split channel count including high capacity and ultra high capacity Reset Source: rst_mod_g_rst_n
17:9	TCHAN_CNT	R	30h	Tx split channel count including high capacity and ultra high capacity Reset Source: rst_mod_g_rst_n
8:0	CHAN_CNT	R	18h	BC channel count including high capacity and ultra high capacity Reset Source: rst_mod_g_rst_n

14.6.1.2.21 BCDMA_GCFG_CAP3 Register

14.6.1.2.21.1 BCDMA_GCFG_CAP3 Register (Offset = 2Ch) [reset = 0h]

The Capabilities Register 3 specifies how many resources this BCDMA instance supports.

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Table 14-9172. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 012Ch

Figure 14-4547. BCDMA_GCFG_CAP3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">UCHAN_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>UCHAN_CNT</td><td colspan="7">HCHAN_CNT</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">HCHAN_CNT</td><td colspan="6">RESERVED</td></tr>
<tr><td colspan="2">R</td><td colspan="6">NONE</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9173. BCDMA_GCFG_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	UCHAN_CNT	R	0h	BC ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
22:14	HCHAN_CNT	R	0h	BC high capacity internal channel count Reset Source: rst_mod_g_rst_n
13:0	RESERVED	NONE	0h	Reserved

14.6.1.2.22 BCDMA_GCFG_CAP4 Register

14.6.1.2.22.1 BCDMA_GCFG_CAP4 Register (Offset = 30h) [reset = 0h]

The Capabilities Register 4 specifies how many resources this BCDMA instance supports.

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Table 14-9174. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0130h

Figure 14-4548. BCDMA_GCFG_CAP4 Name Register

31	30	29	28	27	26	25	24
TUCHAN_CNT							
R							
0h							
23	22	21	20	19	18	17	16
THCHAN_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RUCHAN_CNT							
R							
0h							
7	6	5	4	3	2	1	0
RHCHAN_CNT							
R							
0h							

Table 14-9175. BCDMA_GCFG_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TUCHAN_CNT	R	0h	TX ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
23:16	THCHAN_CNT	R	0h	TX high capacity internal channel count Reset Source: rst_mod_g_rst_n
15:8	RUCHAN_CNT	R	0h	RX ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
7:0	RHCHAN_CNT	R	0h	RX high capacity internal channel count Reset Source: rst_mod_g_rst_n

14.6.1.2.23 BCDMA_GCFG_PM0 Register

14.6.1.2.23.1 BCDMA_GCFG_PM0 Register (Offset = 60h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

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Table 14-9176. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0160h

Figure 14-4549. BCDMA_GCFG_PM0 Name Register

31	30	29	28	27	26	25	24
NOGATE_RSVD4							
R/W							
0h							
23	22	21	20	19	18	17	16
NOGATE_RSVD4							
R/W							
0h							
15	14	13	12	11	10	9	8
NOGATE_RSVD4	NOGATE_RDEC2	NOGATE_RSVD3		NOGATE_SDEC3	NOGATE_RSVD2		
R/W	R/W	R/W		R/W	R/W		
0h	0h	0h		0h	0h		
7	6	5	4	3	2	1	0
NOGATE_WARB3	NOGATE_RSVD1			NOGATE_CARB3	NOGATE_CARB2	NOGATE_RSVD0	
R/W	R/W			R/W	R/W	R/W	
0h	0h			0h	0h	0h	

Table 14-9177. BCDMA_GCFG_PM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	NOGATE_RSVD4	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
14	NOGATE_RDEC2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
13:12	NOGATE_RSVD3	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
11	NOGATE_SDEC3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
10:8	NOGATE_RSVD2	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
7	NOGATE_WARB3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
6:4	NOGATE_RSVD1	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
3	NOGATE_CARB3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
2	NOGATE_CARB2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-9177. BCDMA_GCFG_PM0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	NOGATE_RSVD0	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n

14.6.1.2.24 BCDMA_GCFG_PM1 Register

14.6.1.2.24.1 BCDMA_GCFG_PM1 Register (Offset = 64h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

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Table 14-9178. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0164h

Figure 14-4550. BCDMA_GCFG_PM1 Name Register

31	30	29	28	27	26	25	24
NOGATE_EDC	NOGATE_STATS	NOGATE_PROXY	NOGATE_PSILIF	NOGATE_P2P	NOGATE_RSVD8	NOGATE_EHANDLER	NOGATE_RINGOCC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOGATE_RPCF	NOGATE_TPCF	NOGATE_PCF	NOGATE_RSVD7		NOGATE_CFG	NOGATE_RSVD6	
R/W	R/W	R/W	R/W		R/W	R/W	
0h	0h	0h	0h		0h	0h	
15	14	13	12	11	10	9	8
NOGATE_RSVD6					NOGATE_TRCU	NOGATE_RSVD5	NOGATE_EVTCU
R/W					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
NOGATE_RWU3	NOGATE_RWU2	NOGATE_RWU1	NOGATE_RWU0	NOGATE_TRU3	NOGATE_TRU2	NOGATE_TRU1	NOGATE_TRU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9179. BCDMA_GCFG_PM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOGATE_EDC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
30	NOGATE_STATS	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
29	NOGATE_PROXY	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
28	NOGATE_PSILIF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
27	NOGATE_P2P	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
26	NOGATE_RSVD8	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
25	NOGATE_EHANDLER	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
24	NOGATE_RINGOCC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-9179. BCDMA_GCFG_PM1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	NOGATE_RPCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
22	NOGATE_TPCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
21	NOGATE_PCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
20:19	NOGATE_RSVD7	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
18	NOGATE_CFG	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
17:11	NOGATE_RSVD6	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
10	NOGATE_TRCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
9	NOGATE_RSVD5	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
8	NOGATE_EVTCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
7	NOGATE_RWU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
6	NOGATE_RWU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
5	NOGATE_RWU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
4	NOGATE_RWU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
3	NOGATE_TRU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
2	NOGATE_TRU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
1	NOGATE_TRU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
0	NOGATE_TRU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

14.6.1.2.25 BCDMA_GCFG_DBGADDR Register

14.6.1.2.25.1 BCDMA_GCFG_DBGADDR Register (Offset = 78h) [reset = 0h]

This register provides a writable address which allows debug information to be read from the Debug Data Register

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Table 14-9180. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 0178h

Figure 14-4551. BCDMA_GCFG_DBGADDR Name Register

31	30	29	28	27	26	25	24
DBG_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DBG_UNIT							
R/W							
0h							
7	6	5	4	3	2	1	0
DBG_ADDR							
R/W							
0h							

Table 14-9181. BCDMA_GCFG_DBGADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBG_EN	R/W	0h	Debug enable Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	DBG_UNIT	R/W	0h	Selects which unit to read debug information from Reset Source: rst_mod_g_rst_n
7:0	DBG_ADDR	R/W	0h	Selects offset within unit to access seperate debug registers Reset Source: rst_mod_g_rst_n

14.6.1.2.26 BCDMA_GCFG_DBGDATA Register

14.6.1.2.26.1 BCDMA_GCFG_DBGDATA Register (Offset = 7Ch) [reset = 0h]

This register provides read only debug data

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Table 14-9182. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	485C 017Ch

Figure 14-4552. BCDMA_GCFG_DBGDATA Name Register

31	30	29	28	27	26	25	24
DBG_DATA							
R/NA							
0h							
23	22	21	20	19	18	17	16
DBG_DATA							
R/NA							
0h							
15	14	13	12	11	10	9	8
DBG_DATA							
R/NA							
0h							
7	6	5	4	3	2	1	0
DBG_DATA							
R/NA							
0h							

Table 14-9183. BCDMA_GCFG_DBGDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBG_DATA	R/NA	0h	Provides debug information from various internal units. The value which is read back depends on which unit and register are selected in the Debug Address Register Reset Source: rst_mod_g_rst_n

14.6.1.2.27 LCDMA_RINGACC_RING_CFG_RING_BA_LO_J Register

14.6.1.2.27.1 LCDMA_RINGACC_RING_CFG_RING_BA_LO_J Register (Offset = 40h) [reset = 0h]

The Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9184. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4860 0040h + formula

Figure 14-4553. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Name Register

31	30	29	28	27	26	25	24
ADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_LO							
R/W							
0h							

Table 14-9185. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_LO	R/W	0h	Ring base address (LSBs) Reset Source: rst_mod_g_rst_n

14.6.1.2.28 LCDMA_RINGACC_RING_CFG_RING_BA_HI_J Register

14.6.1.2.28.1 LCDMA_RINGACC_RING_CFG_RING_BA_HI_J Register (Offset = 44h) [reset = 0h]

The Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9186. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4860 0044h + formula

Figure 14-4554. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				ASEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADDR_HI			
NONE				R/W			
0h				0h			

Table 14-9187. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	ASEL	R/W	0h	Ring base address select Reset Source: rst_mod_g_rst_n
15:4	RESERVED	NONE	0h	Reserved
3:0	ADDR_HI	R/W	0h	Ring base address (MSBs) Reset Source: rst_mod_g_rst_n

14.6.1.2.29 LCDMA_RINGACC_RING_CFG_RING_SIZE_J Register

14.6.1.2.29.1 LCDMA_RINGACC_RING_CFG_RING_SIZE_J Register (Offset = 48h) [reset = 21000000h]

The Ring Size Register contains the element count for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9188. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4860 0048h + formula

Figure 14-4555. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">QMODE</td><td colspan="2">RESERVED</td><td colspan="3">RING_ELSIZE</td></tr>
<tr><td colspan="3">R/NA</td><td colspan="2">NONE</td><td colspan="3">R/NA</td></tr>
<tr><td colspan="3">1h</td><td colspan="2">0h</td><td colspan="3">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9189. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	QMODE	R/NA	1h	Defines the mode for this ring or queue. `1      exposed ring mode with dual queues (forward/reverse) for SW direct access`
28:27	RESERVED	NONE	0h	Reserved
26:24	RING_ELSIZE	R/NA	1h	Reset Source: rst_mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:0	SIZE	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. Reset Source: rst_mod_g_rst_n

14.6.1.2.30 BCDMA_RXCRT_CHAN_CTL_J Register

14.6.1.2.30.1 BCDMA_RXCRT_CHAN_CTL_J Register (Offset = 0h) [reset = 0h]

The Rx Channel Realtime Control Register contains real-time control and status information for the Rx DMA channel. The fields in this register can safely be changed while the channel is in operation.

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Table 14-9190. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0000h + formula

Figure 14-4556. BCDMA_RXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
RX_ENABLE	RX_TEARDOWN	RX_PAUSE	RX_FORCED_TEARDOWN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						RX_STARVATION	RX_ERROR
NONE						R	R
0h						0h	0h

Table 14-9191. BCDMA_RXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in overflow conditions in the attached application and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit shoudl be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate tha the channel teardown is complete. If the host is enabling a channel that is just being set up, the host must initialize all of the other channel configuration fields before setting this bit. Reset Source: rst_mod_g_rst_n
30	RX_TEARDOWN	R/W	0h	This field indicates whether or not an Rx teardown operation is complete. This field should be cleared when a channel is initialized. This field will be set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	RX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n

Table 14-9191. BCDMA_RXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	RX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Uso fo this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:2	RESERVED	NONE	0h	Reserved
1	RX_STARVATION	R	0h	Rx starvation. This bit is set if the port receives a packet and the ring is empty. The bit clears when the doorbell is written with a positive value. Reset Source: rst_mod_g_rst_n
0	RX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared when the channel is disabled and re-enabled. Reset Source: rst_mod_g_rst_n

14.6.1.2.31 BCDMA_RXCRT_CHAN_SWTRIG_J Register

14.6.1.2.31.1 BCDMA_RXCRT_CHAN_SWTRIG_J Register (Offset = 8h) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

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Table 14-9192. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0008h + formula

Figure 14-4557. BCDMA_RXCRT_CHAN_SWTRIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
NONE							NA/W
0h							0h

Table 14-9193. BCDMA_RXCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.6.1.2.32 BCDMA_RXCRT_CHAN_STATUS0_J Register

14.6.1.2.32.1 BCDMA_RXCRT_CHAN_STATUS0_J Register (Offset = 40h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Table 14-9194. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0040h + formula

Figure 14-4558. BCDMA_RXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
RRING_PEND	RXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	RX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9195. BCDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	RXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n

Table 14-9195. BCDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.1.2.33 BCDMA_RXCRT_CHAN_STATUS1_J Register

14.6.1.2.33.1 BCDMA_RXCRT_CHAN_STATUS1_J Register (Offset = 44h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Table 14-9196. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0044h + formula

Figure 14-4559. BCDMA_RXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
RX_REQS	RESERVED					FIFO_PEND	FIFO_BUSY
R	NONE					R	R
0h	0h					0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-9197. BCDMA_RXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	FIFO_PEND	R	0h	The FIFO has enough data for a burst Reset Source: rst_mod_g_rst_n
24	FIFO_BUSY	R	0h	The fifo has data Reset Source: rst_mod_g_rst_n
23:8	RESERVED	NONE	0h	Reserved
7	CHANNEL_OK	R	0h	Channel is trying to send data Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Channel has active transactions Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.6.1.2.34 BCDMA_RXCRT_CHAN_STDATA_J_K Register

14.6.1.2.34.1 BCDMA_RXCRT_CHAN_STDATA_J_K Register (Offset = 80h) [reset = 0h]

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

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Table 14-9198. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0080h + formula

Figure 14-4560. BCDMA_RXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/W							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/W							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/W							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/W							
0h							

Table 14-9199. BCDMA_RXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/W	0h	See Rx state mapping table Reset Source: rst_mod_g_rst_n

14.6.1.2.35 BCDMA_RXCRT_CHAN_PEER0_J Register

14.6.1.2.35.1 BCDMA_RXCRT_CHAN_PEER0_J Register (Offset = 200h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

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Table 14-9200. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0200h + formula

Figure 14-4561. BCDMA_RXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9201. BCDMA_RXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.36 BCDMA_RXCRT_CHAN_PEER1_J Register

14.6.1.2.36.1 BCDMA_RXCRT_CHAN_PEER1_J Register (Offset = 204h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

Return to Summary Table

Table 14-9202. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0204h + formula

Figure 14-4562. BCDMA_RXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9203. BCDMA_RXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.37 BCDMA_RXCRT_CHAN_PEER2_J Register

14.6.1.2.37.1 BCDMA_RXCRT_CHAN_PEER2_J Register (Offset = 208h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

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Table 14-9204. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0208h + formula

Figure 14-4563. BCDMA_RXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9205. BCDMA_RXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.38 BCDMA_RXCRT_CHAN_PEER3_J Register

14.6.1.2.38.1 BCDMA_RXCRT_CHAN_PEER3_J Register (Offset = 20Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

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Table 14-9206. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 020Ch + formula

Figure 14-4564. BCDMA_RXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9207. BCDMA_RXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.39 BCDMA_RXCRT_CHAN_PEER4_J Register

14.6.1.2.39.1 BCDMA_RXCRT_CHAN_PEER4_J Register (Offset = 210h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

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Table 14-9208. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0210h + formula

Figure 14-4565. BCDMA_RXCRT_CHAN_PEER4_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9209. BCDMA_RXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.40 BCDMA_RXCRT_CHAN_PEER5_J Register

14.6.1.2.40.1 BCDMA_RXCRT_CHAN_PEER5_J Register (Offset = 214h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

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Table 14-9210. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0214h + formula

Figure 14-4566. BCDMA_RXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9211. BCDMA_RXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.41 BCDMA_RXCRT_CHAN_PEER6_J Register

14.6.1.2.41.1 BCDMA_RXCRT_CHAN_PEER6_J Register (Offset = 218h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

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Table 14-9212. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0218h + formula

Figure 14-4567. BCDMA_RXCRT_CHAN_PEER6_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9213. BCDMA_RXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.42 BCDMA_RXCRT_CHAN_PEER7_J Register

14.6.1.2.42.1 BCDMA_RXCRT_CHAN_PEER7_J Register (Offset = 21Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

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Table 14-9214. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 021Ch + formula

Figure 14-4568. BCDMA_RXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9215. BCDMA_RXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.43 BCDMA_RXCRT_CHAN_PEER8_J Register

14.6.1.2.43.1 BCDMA_RXCRT_CHAN_PEER8_J Register (Offset = 220h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

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Table 14-9216. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0220h + formula

Figure 14-4569. BCDMA_RXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9217. BCDMA_RXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.44 BCDMA_RXCRT_CHAN_PEER9_J Register

14.6.1.2.44.1 BCDMA_RXCRT_CHAN_PEER9_J Register (Offset = 224h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

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Table 14-9218. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0224h + formula

Figure 14-4570. BCDMA_RXCRT_CHAN_PEER9_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9219. BCDMA_RXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.45 BCDMA_RXCRT_CHAN_PEER10_J Register

14.6.1.2.45.1 BCDMA_RXCRT_CHAN_PEER10_J Register (Offset = 228h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

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Table 14-9220. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0228h + formula

Figure 14-4571. BCDMA_RXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9221. BCDMA_RXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.46 BCDMA_RXCRT_CHAN_PEER11_J Register

14.6.1.2.46.1 BCDMA_RXCRT_CHAN_PEER11_J Register (Offset = 22Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

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Table 14-9222. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 022Ch + formula

Figure 14-4572. BCDMA_RXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9223. BCDMA_RXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.47 BCDMA_RXCRT_CHAN_PEER12_J Register

14.6.1.2.47.1 BCDMA_RXCRT_CHAN_PEER12_J Register (Offset = 230h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

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Table 14-9224. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0230h + formula

Figure 14-4573. BCDMA_RXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9225. BCDMA_RXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.48 BCDMA_RXCRT_CHAN_PEER13_J Register

14.6.1.2.48.1 BCDMA_RXCRT_CHAN_PEER13_J Register (Offset = 234h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

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Table 14-9226. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0234h + formula

Figure 14-4574. BCDMA_RXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9227. BCDMA_RXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.49 BCDMA_RXCRT_CHAN_PEER14_J Register

14.6.1.2.49.1 BCDMA_RXCRT_CHAN_PEER14_J Register (Offset = 238h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

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Table 14-9228. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0238h + formula

Figure 14-4575. BCDMA_RXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9229. BCDMA_RXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.50 BCDMA_RXCRT_CHAN_PEER15_J Register

14.6.1.2.50.1 BCDMA_RXCRT_CHAN_PEER15_J Register (Offset = 23Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

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Table 14-9230. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 023Ch + formula

Figure 14-4576. BCDMA_RXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9231. BCDMA_RXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.51 BCDMA_RXCRT_CHAN_PCNT_J Register

14.6.1.2.51.1 BCDMA_RXCRT_CHAN_PCNT_J Register (Offset = 400h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9232. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0400h + formula

Figure 14-4577. BCDMA_RXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-9233. BCDMA_RXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.52 BCDMA_RXCRT_CHAN_BCNT_J Register

14.6.1.2.52.1 BCDMA_RXCRT_CHAN_BCNT_J Register (Offset = 408h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

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Table 14-9234. Instance Table

Instance Name	**Physical Address**
DMASS0_BCDMA_0	4A84 0408h + formula

Figure 14-4578. BCDMA_RXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-9235. BCDMA_RXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	**Field**	**Type**	**Reset**	**Description**
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.53 BCDMA_RXCRT_CHAN_SBCNT_J Register

14.6.1.2.53.1 BCDMA_RXCRT_CHAN_SBCNT_J Register (Offset = 410h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

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Table 14-9236. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4A84 0410h + formula

Figure 14-4579. BCDMA_RXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-9237. BCDMA_RXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.54 BCDMA_TXCRT_CHAN_CTL_J Register

14.6.1.2.54.1 BCDMA_TXCRT_CHAN_CTL_J Register (Offset = 0h) [reset = 0h]

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

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Table 14-9238. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0000h + formula

Figure 14-4580. BCDMA_TXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
TX_ENABLE	TX_TEARDOWN	TX_PAUSE	TX_FORCED_TEARDOWN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TX_ERROR
NONE							R
0h							0h

Table 14-9239. BCDMA_TXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete. Reset Source: rst_mod_g_rst_n
30	TX_TEARDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	TX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n

Table 14-9239. BCDMA_TXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	TX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Uso fo this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:1	RESERVED	NONE	0h	Reserved
0	TX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared by writing back a 0. Reset Source: rst_mod_g_rst_n

14.6.1.2.55 BCDMA_TXCRT_CHAN_SWTRIG_J Register

14.6.1.2.55.1 BCDMA_TXCRT_CHAN_SWTRIG_J Register (Offset = 8h) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

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Table 14-9240. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0008h + formula

Figure 14-4581. BCDMA_TXCRT_CHAN_SWTRIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
NONE							NA/W
0h							0h

Table 14-9241. BCDMA_TXCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.6.1.2.56 BCDMA_TXCRT_CHAN_STATUS0_J Register

14.6.1.2.56.1 BCDMA_TXCRT_CHAN_STATUS0_J Register (Offset = 40h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

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Table 14-9242. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0040h + formula

Figure 14-4582. BCDMA_TXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
TRING_PEND	TXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	TX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9243. BCDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	TXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n

Table 14-9243. BCDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.1.2.57 BCDMA_TXCRT_CHAN_STATUS1_J Register

14.6.1.2.57.1 BCDMA_TXCRT_CHAN_STATUS1_J Register (Offset = 44h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

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Table 14-9244. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0044h + formula

Figure 14-4583. BCDMA_TXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
TX_REQS	RESERVED						WAVAIL
R	NONE						R
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TDNULL
NONE							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-9245. BCDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:25	RESERVED	NONE	0h	Reserved
24	WAVAIL	R	0h	The fifo has space for a burst size Reset Source: rst_mod_g_rst_n
23:9	RESERVED	NONE	0h	Reserved
8	TDNULL	R	0h	The channel has met the conditions to do teardown Reset Source: rst_mod_g_rst_n
7	CHANNEL_OK	R	0h	Channel is trying to schedule work Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Channel has outstanding work to do Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.6.1.2.58 BCDMA_TXCRT_CHAN_STDATA_J_K Register

14.6.1.2.58.1 BCDMA_TXCRT_CHAN_STDATA_J_K Register (Offset = 80h) [reset = 0h]

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

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Table 14-9246. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0080h + formula

Figure 14-4584. BCDMA_TXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/NA							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/NA							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/NA							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/NA							
0h							

Table 14-9247. BCDMA_TXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/NA	0h	See Tx state mapping table Reset Source: rst_mod_g_rst_n

14.6.1.2.59 BCDMA_TXCRT_CHAN_PEER0_J Register

14.6.1.2.59.1 BCDMA_TXCRT_CHAN_PEER0_J Register (Offset = 200h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

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Table 14-9248. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0200h + formula

Figure 14-4585. BCDMA_TXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9249. BCDMA_TXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.60 BCDMA_TXCRT_CHAN_PEER1_J Register

14.6.1.2.60.1 BCDMA_TXCRT_CHAN_PEER1_J Register (Offset = 204h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

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Table 14-9250. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0204h + formula

Figure 14-4586. BCDMA_TXCRT_CHAN_PEER1_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9251. BCDMA_TXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.61 BCDMA_TXCRT_CHAN_PEER2_J Register

14.6.1.2.61.1 BCDMA_TXCRT_CHAN_PEER2_J Register (Offset = 208h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

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Table 14-9252. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0208h + formula

Figure 14-4587. BCDMA_TXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9253. BCDMA_TXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.62 BCDMA_TXCRT_CHAN_PEER3_J Register

14.6.1.2.62.1 BCDMA_TXCRT_CHAN_PEER3_J Register (Offset = 20Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

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Table 14-9254. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 020Ch + formula

Figure 14-4588. BCDMA_TXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9255. BCDMA_TXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.63 BCDMA_TXCRT_CHAN_PEER4_J Register

14.6.1.2.63.1 BCDMA_TXCRT_CHAN_PEER4_J Register (Offset = 210h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

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Table 14-9256. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0210h + formula

Figure 14-4589. BCDMA_TXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9257. BCDMA_TXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.64 BCDMA_TXCRT_CHAN_PEER5_J Register

14.6.1.2.64.1 BCDMA_TXCRT_CHAN_PEER5_J Register (Offset = 214h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

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Table 14-9258. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0214h + formula

Figure 14-4590. BCDMA_TXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9259. BCDMA_TXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.65 BCDMA_TXCRT_CHAN_PEER6_J Register

14.6.1.2.65.1 BCDMA_TXCRT_CHAN_PEER6_J Register (Offset = 218h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

Return to Summary Table

Table 14-9260. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0218h + formula

Figure 14-4591. BCDMA_TXCRT_CHAN_PEER6_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9261. BCDMA_TXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.66 BCDMA_TXCRT_CHAN_PEER7_J Register

14.6.1.2.66.1 BCDMA_TXCRT_CHAN_PEER7_J Register (Offset = 21Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

Return to Summary Table

Table 14-9262. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 021Ch + formula

Figure 14-4592. BCDMA_TXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PEER_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PEER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PEER_DATA							
R/W							
0h							

Table 14-9263. BCDMA_TXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.67 BCDMA_TXCRT_CHAN_PEER8_J Register

14.6.1.2.67.1 BCDMA_TXCRT_CHAN_PEER8_J Register (Offset = 220h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Table 14-9264. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0220h + formula

Figure 14-4593. BCDMA_TXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9265. BCDMA_TXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.68 BCDMA_TXCRT_CHAN_PEER9_J Register

14.6.1.2.68.1 BCDMA_TXCRT_CHAN_PEER9_J Register (Offset = 224h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Table 14-9266. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0224h + formula

Figure 14-4594. BCDMA_TXCRT_CHAN_PEER9_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PEER_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PEER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PEER_DATA							
R/W							
0h							

Table 14-9267. BCDMA_TXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.69 BCDMA_TXCRT_CHAN_PEER10_J Register

14.6.1.2.69.1 BCDMA_TXCRT_CHAN_PEER10_J Register (Offset = 228h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Table 14-9268. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0228h + formula

Figure 14-4595. BCDMA_TXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PEER_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PEER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PEER_DATA							
R/W							
0h							

Table 14-9269. BCDMA_TXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.70 BCDMA_TXCRT_CHAN_PEER11_J Register

14.6.1.2.70.1 BCDMA_TXCRT_CHAN_PEER11_J Register (Offset = 22Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Table 14-9270. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 022Ch + formula

Figure 14-4596. BCDMA_TXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9271. BCDMA_TXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.71 BCDMA_TXCRT_CHAN_PEER12_J Register

14.6.1.2.71.1 BCDMA_TXCRT_CHAN_PEER12_J Register (Offset = 230h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Table 14-9272. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0230h + formula

Figure 14-4597. BCDMA_TXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9273. BCDMA_TXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.72 BCDMA_TXCRT_CHAN_PEER13_J Register

14.6.1.2.72.1 BCDMA_TXCRT_CHAN_PEER13_J Register (Offset = 234h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Table 14-9274. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0234h + formula

Figure 14-4598. BCDMA_TXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9275. BCDMA_TXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.73 BCDMA_TXCRT_CHAN_PEER14_J Register

14.6.1.2.73.1 BCDMA_TXCRT_CHAN_PEER14_J Register (Offset = 238h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Table 14-9276. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0238h + formula

Figure 14-4599. BCDMA_TXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9277. BCDMA_TXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.74 BCDMA_TXCRT_CHAN_PEER15_J Register

14.6.1.2.74.1 BCDMA_TXCRT_CHAN_PEER15_J Register (Offset = 23Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Table 14-9278. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 023Ch + formula

Figure 14-4600. BCDMA_TXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9279. BCDMA_TXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.1.2.75 BCDMA_TXCRT_CHAN_PCNT_J Register

14.6.1.2.75.1 BCDMA_TXCRT_CHAN_PCNT_J Register (Offset = 400h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9280. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0400h + formula

Figure 14-4601. BCDMA_TXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-9281. BCDMA_TXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.76 BCDMA_TXCRT_CHAN_BCNT_J Register

14.6.1.2.76.1 BCDMA_TXCRT_CHAN_BCNT_J Register (Offset = 408h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9282. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0408h + formula

Figure 14-4602. BCDMA_TXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-9283. BCDMA_TXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.77 BCDMA_TXCRT_CHAN_SBCNT_J Register

14.6.1.2.77.1 BCDMA_TXCRT_CHAN_SBCNT_J Register (Offset = 410h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9284. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4AA4 0410h + formula

Figure 14-4603. BCDMA_TXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-9285. BCDMA_TXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.78 LCDMA_RINGACC_RINGRT_RING_FDB_J Register

14.6.1.2.78.1 LCDMA_RINGACC_RINGRT_RING_FDB_J Register (Offset = 10h) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Table 14-9286. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4BC0 0010h + formula

Figure 14-4604. LCDMA_RINGACC_RINGRT_RING_FDB_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-9287. LCDMA_RINGACC_RINGRT_RING_FDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.6.1.2.79 LCDMA_RINGACC_RINGRT_RING_FOCC_J Register

14.6.1.2.79.1 LCDMA_RINGACC_RINGRT_RING_FOCC_J Register (Offset = 18h) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Table 14-9288. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4BC0 0018h + formula

Figure 14-4605. LCDMA_RINGACC_RINGRT_RING_FOCC_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>OCC</td></tr>
<tr><td colspan="7">NONE</td><td>R/NA</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OCC</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OCC</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9289. LCDMA_RINGACC_RINGRT_RING_FOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.6.1.2.80 LCDMA_RINGACC_RINGRT_RING_RDB_J Register

14.6.1.2.80.1 LCDMA_RINGACC_RINGRT_RING_RDB_J Register (Offset = 1010h) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Return to Summary Table

Table 14-9290. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4BC0 1010h + formula

Figure 14-4606. LCDMA_RINGACC_RINGRT_RING_RDB_j Name Register

31	30	29	28	27	26	25	24
TDOWN_ACK	RESERVED						
NA/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-9291. LCDMA_RINGACC_RINGRT_RING_RDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_ACK	NA/W	0h	This bit is set to 1 to ackowledge (and clear) the tdown_complete bit in the corresponding Ring N Occupancy Register. this bit is only valid on the reverse rings (rings consumed by the Host SW) Reset Source: rst_mod_g_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.6.1.2.81 LCDMA_RINGACC_RINGRT_RING_ROCC_J Register

14.6.1.2.81.1 LCDMA_RINGACC_RINGRT_RING_ROCC_J Register (Offset = 1018h) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Table 14-9292. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4BC0 1018h + formula

Figure 14-4607. LCDMA_RINGACC_RINGRT_RING_ROCC_j Name Register

31	30	29	28	27	26	25	24
TDOWN_COMPLETE	RESERVED						
R/NA	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OCC
NONE							R/NA
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OCC							
R/NA							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OCC							
R/NA							
0h							

Table 14-9293. LCDMA_RINGACC_RINGRT_RING_ROCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_COMPLETE	R/NA	0h	This bit when set indicates that a teardown is complete on the channel. This bit is cleared anytime the tdown_ack bit is written as a 1 in the corresponding Ring N Doorbell Register. This bit is only valid on the reverse rings (rings consumed by the Host SW). Reset Source: rst_mod_g_rst_n
30:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.6.1.2.82 BCDMA_BCRT_CHAN_CTL_J Register

14.6.1.2.82.1 BCDMA_BCRT_CHAN_CTL_J Register (Offset = 0h) [reset = 0h]

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

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Table 14-9294. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0000h + formula

Figure 14-4608. BCDMA_BCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
TX_ENABLE	TX_TEARDOWN	TX_PAUSE	TX_FORCED_TEARDOWN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TX_ERROR
NONE							R
0h							0h

Table 14-9295. BCDMA_BCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete. Reset Source: rst_mod_g_rst_n
30	TX_TEARDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	TX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n

Table 14-9295. BCDMA_BCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	TX_FORCED_TEARDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the BCDMA even if the trigger source is no longer functioning. Use og this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
27:1	RESERVED	NONE	0h	Reserved
0	TX_ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared by writing back a 0. Reset Source: rst_mod_g_rst_n

14.6.1.2.83 BCDMA_BCRT_CHAN_SWTRIG_J Register

14.6.1.2.83.1 BCDMA_BCRT_CHAN_SWTRIG_J Register (Offset = 8h) [reset = 0h]

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Return to Summary Table

Table 14-9296. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0008h + formula

Figure 14-4609. BCDMA_BCRT_CHAN_SWTRIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
NONE							NA/W
0h							0h

Table 14-9297. BCDMA_BCRT_CHAN_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TRIGGER	NA/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel Reset Source: rst_mod_g_rst_n

14.6.1.2.84 BCDMA_BCRT_CHAN_STATUS0_J Register

14.6.1.2.84.1 BCDMA_BCRT_CHAN_STATUS0_J Register (Offset = 40h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

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Table 14-9298. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0040h + formula

Figure 14-4610. BCDMA_BCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
TRING_PEND	TXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	TX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9299. BCDMA_BCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	TXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n

Table 14-9299. BCDMA_BCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.1.2.85 BCDMA_BCRT_CHAN_STATUS1_J Register

14.6.1.2.85.1 BCDMA_BCRT_CHAN_STATUS1_J Register (Offset = 44h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

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Table 14-9300. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0044h + formula

Figure 14-4611. BCDMA_BCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
TX_REQS	RESERVED						WAVAIL
R	NONE						R
0h	0h						0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TDNULL
NONE							R
0h							0h
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-9301. BCDMA_BCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:25	RESERVED	NONE	0h	Reserved
24	WAVAIL	R	0h	The fifo has space for a burst size Reset Source: rst_mod_g_rst_n
23:9	RESERVED	NONE	0h	Reserved
8	TDNULL	R	0h	Channel is trying to teardown and has met conditions Reset Source: rst_mod_g_rst_n
7	CHANNEL_OK	R	0h	Channel is trying to schedule a transaction Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	The channel is active Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.6.1.2.86 BCDMA_BCRT_CHAN_STATUS2_J Register

14.6.1.2.86.1 BCDMA_BCRT_CHAN_STATUS2_J Register (Offset = 48h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

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Table 14-9302. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0048h + formula

Figure 14-4612. BCDMA_BCRT_CHAN_STATUS2_j Name Register

31	30	29	28	27	26	25	24
RRING_PEND	RXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	RX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-9303. BCDMA_BCRT_CHAN_STATUS2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	RXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n

Table 14-9303. BCDMA_BCRT_CHAN_STATUS2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.1.2.87 BCDMA_BCRT_CHAN_STATUS3_J Register

14.6.1.2.87.1 BCDMA_BCRT_CHAN_STATUS3_J Register (Offset = 4Ch) [reset = 0h]

The Status Register provides a read only view of channel status bits.

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Table 14-9304. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 004Ch + formula

Figure 14-4613. BCDMA_BCRT_CHAN_STATUS3_j Name Register

31	30	29	28	27	26	25	24
RX_REQS	RESERVED					FIFO_PEND	FIFO_BUSY
R	NONE					R	R
0h	0h					0h	0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-9305. BCDMA_BCRT_CHAN_STATUS3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	FIFO_PEND	R	0h	The FIFO has enough data for a burst Reset Source: rst_mod_g_rst_n
24	FIFO_BUSY	R	0h	The fifo has data Reset Source: rst_mod_g_rst_n
23:8	RESERVED	NONE	0h	Reserved
7	CHANNEL_OK	R	0h	Reserved Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	Reserved Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	Reserved Reset Source: rst_mod_g_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.6.1.2.88 BCDMA_BCRT_CHAN_STDATA_J_K Register

14.6.1.2.88.1 BCDMA_BCRT_CHAN_STDATA_J_K Register (Offset = 80h) [reset = 0h]

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

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Table 14-9306. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0080h + formula

Figure 14-4614. BCDMA_BCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/NA							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/NA							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/NA							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/NA							
0h							

Table 14-9307. BCDMA_BCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/NA	0h	See Tx state mapping table Reset Source: rst_mod_g_rst_n

14.6.1.2.89 BCDMA_BCRT_CHAN_STDATAW_J_K Register

14.6.1.2.89.1 BCDMA_BCRT_CHAN_STDATAW_J_K Register (Offset = 100h) [reset = 0h]

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the BCDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

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Table 14-9308. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0100h + formula

Figure 14-4615. BCDMA_BCRT_CHAN_STDATAW_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/W							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/W							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/W							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/W							
0h							

Table 14-9309. BCDMA_BCRT_CHAN_STDATAW_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/W	0h	See Rx state mapping table Reset Source: rst_mod_g_rst_n

14.6.1.2.90 BCDMA_BCRT_CHAN_PCNT_J Register

14.6.1.2.90.1 BCDMA_BCRT_CHAN_PCNT_J Register (Offset = 400h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

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Table 14-9310. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0400h + formula

Figure 14-4616. BCDMA_BCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PCNT							
R/WTD							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PCNT							
R/WTD							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCNT							
R/WTD							
0h							

Table 14-9311. BCDMA_BCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.91 BCDMA_BCRT_CHAN_BCNT_J Register

14.6.1.2.91.1 BCDMA_BCRT_CHAN_BCNT_J Register (Offset = 408h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9312. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0408h + formula

Figure 14-4617. BCDMA_BCRT_CHAN_BCNT_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9313. BCDMA_BCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.1.2.92 BCDMA_BCRT_CHAN_SBCNT_J Register

14.6.1.2.92.1 BCDMA_BCRT_CHAN_SBCNT_J Register (Offset = 410h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

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Table 14-9314. Instance Table

Instance Name	Physical Address
DMASS0_BCDMA_0	4C00 0410h + formula

Figure 14-4618. BCDMA_BCRT_CHAN_SBCNT_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SBCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SBCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SBCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SBCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9315. BCDMA_BCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.2 DMASS_ECC_AGGR_0

DMASS_ECC_AGGR_0

14.6.2.1 DMASS_ECC_AGGR_0 Summaries

DMASS_ECC_AGGR_0 Summaries

Table 14-9316. DMASS_ECC_AGGR_0_ECCAGGR Registers, Base Address=3F00 5000h, Length=1024

Offset	Length	Register Name	DMASS0_ECC_AGGR_0 Physical Address
0h	32	DMASS_ECC_AGGR_0_ECCAGGR_REV	3F00 5000h
8h	32	DMASS_ECC_AGGR_0_ECCAGGR_VECTOR	3F00 5008h
Ch	32	DMASS_ECC_AGGR_0_ECCAGGR_STAT	3F00 500Ch
10h	32	DMASS_ECC_AGGR_0_ECCAGGR_RESERVED_SVBUS	3F00 5010h
3Ch	32	DMASS_ECC_AGGR_0_ECCAGGR_SEC_EOI_REG	3F00 503Ch
40h	32	DMASS_ECC_AGGR_0_ECCAGGR_SEC_STATUS_REG0	3F00 5040h
80h	32	DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_SET_REG0	3F00 5080h
C0h	32	DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_CLR_REG0	3F00 50C0h
13Ch	32	DMASS_ECC_AGGR_0_ECCAGGR_DED_EOI_REG	3F00 513Ch
140h	32	DMASS_ECC_AGGR_0_ECCAGGR_DED_STATUS_REG0	3F00 5140h
180h	32	DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_SET_REG0	3F00 5180h
1C0h	32	DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_CLR_REG0	3F00 51C0h
200h	32	DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_SET	3F00 5200h
204h	32	DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_CLR	3F00 5204h
208h	32	DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_SET	3F00 5208h
20Ch	32	DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_CLR	3F00 520Ch

14.6.2.2 DMASS_ECC_AGGR_0 Registers

DMASS_ECC_AGGR_0 Registers

14.6.2.2.1 DMASS_ECC_AGGR_0_ECCAGGR_REV Register

14.6.2.2.1.1 DMASS_ECC_AGGR_0_ECCAGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-9317. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5000h

Figure 14-4619. DMASS_ECC_AGGR_0_ECCAGGR_REV Name Register

32	31	30	29	28	27	26	25
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6a0h			
24	23	22	21	20	19	18	17
MODULE_ID							
R							
6a0h							
16	15	14	13	12	11	10	9
REVRTL					REVMAJ		
R					R		
7h					2h		
8	7	6	5	4	3	2	1
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-9318. DMASS_ECC_AGGR_0_ECCAGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6a0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.6.2.2.2 DMASS_ECC_AGGR_0_ECCAGGR_VECTOR Register

14.6.2.2.2.1 DMASS_ECC_AGGR_0_ECCAGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-9319. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5008h

Figure 14-4620. DMASS_ECC_AGGR_0_ECCAGGR_VECTOR Name Register

32	31	30	29	28	27	26	25
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
24	23	22	21	20	19	18	17
RD_SVBUS_ADDRESS							
R/W							
0h							
16	15	14	13	12	11	10	9
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
8	7	6	5	4	3	2	1
ECC_VECTOR							
R/W							
0h							

Table 14-9320. DMASS_ECC_AGGR_0_ECCAGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.6.2.2.3 DMASS_ECC_AGGR_0_ECCAGGR_STAT Register

14.6.2.2.3.1 DMASS_ECC_AGGR_0_ECCAGGR_STAT Register (Offset = Ch) [reset = 1Ch]

Misc Status

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Table 14-9321. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 500Ch

Figure 14-4621. DMASS_ECC_AGGR_0_ECCAGGR_STAT Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
456h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
456h							
16	15	14	13	12	11	10	9
RESERVED					NUM_RAMS		
NONE					R		
456h					1ch		
8	7	6	5	4	3	2	1
NUM_RAMS							
R							
1ch							

Table 14-9322. DMASS_ECC_AGGR_0_ECCAGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	456h	Reserved
10:0	NUM_RAMS	R	1ch	Indicates the number of RAMS serviced by the ECC aggregator

14.6.2.2.4 DMASS_ECC_AGGR_0_ECCAGGR_RESERVED_SVBUS Register

14.6.2.2.4.1 DMASS_ECC_AGGR_0_ECCAGGR_RESERVED_SVBUS Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-9323. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5010h

Figure 14-4622. DMASS_ECC_AGGR_0_ECCAGGR_RESERVED_SVBUS Name Register

32	31	30	29	28	27	26	25
DATA							
R/W							
0h							
24	23	22	21	20	19	18	17
DATA							
R/W							
0h							
16	15	14	13	12	11	10	9
DATA							
R/W							
0h							
8	7	6	5	4	3	2	1
DATA							
R/W							
0h							

Table 14-9324. DMASS_ECC_AGGR_0_ECCAGGR_RESERVED_SVBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.6.2.2.5 DMASS_ECC_AGGR_0_ECCAGGR_SEC_EOI_REG Register

14.6.2.2.5.1 DMASS_ECC_AGGR_0_ECCAGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-9325. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 503Ch

Figure 14-4623. DMASS_ECC_AGGR_0_ECCAGGR_SEC_EOI_REG Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9326. DMASS_ECC_AGGR_0_ECCAGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.2.2.6 DMASS_ECC_AGGR_0_ECCAGGR_SEC_STATUS_REG0 Register

14.6.2.2.6.1 DMASS_ECC_AGGR_0_ECCAGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9327. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5040h

Figure 14-4624. DMASS_ECC_AGGR_0_ECCAGGR_SEC_STATUS_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED				MSRAM_RAMECC0_PEND	SEC_PROXY_BUFRAM_RAMECC_PEND	SEC_PROXY_STRAM_RAMECC_PEND	RINGACC_STRAM_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
24	23	22	21	20	19	18	17
MAP_RAMECC_PEND	SR_RAMECC_PEND	BCDMA_RNGOCC_RAMECC_PEND	BCDMA_STS_RAMECC1_PEND	BCDMA_STS_RAMECC0_PEND	BCDMA_RPCF2_RAMECC_PEND	BCDMA_RPCF1_RAMECC_PEND	BCDMA_RPCF0_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
16	15	14	13	12	11	10	9
BCDMA_TPCF1_RAMECC_PEND	BCDMA_TPCF0_RAMECC_PEND	PCFD1_RAMECC_PEND	PCFD0_RAMECC_PEND	BCDMA_STATE_RAMECC_PEND	BCDMA_CFG_RAMECC_PEND	PKTDMA_RNGOCC_RAMECC_PEND	PKTDMA_STS_RAMECC1_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
PKTDMA_STS_RAMECC0_PEND	PKTDMA_RPCF2_RAMECC_PEND	PKTDMA_RPCF1_RAMECC_PEND	PKTDMA_RPCF0_RAMECC_PEND	PKTDMA_TPCF1_RAMECC_PEND	PKTDMA_TPCF0_RAMECC_PEND	PKTDMA_STATE_RAMECC_PEND	PKTDMA_CFG_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9328. DMASS_ECC_AGGR_0_ECCAGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ringacc_stram_ramecc_pend
23	MAP_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for map_ramecc_pend
22	SR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sr_ramecc_pend
21	BCDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc1_pend

Table 14-9328. DMASS_ECC_AGGR_0_ECCAGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	BCDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd1_ramecc_pend
12	PCFD0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_cfg_ramecc_pend

14.6.2.2.7 DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_SET_REG0 Register

14.6.2.2.7.1 DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9329. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5080h

Figure 14-4625. DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_SET_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED				MSRAM_RAMECC0_ENABLE_SET	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	RINGACC_STRAM_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
24	23	22	21	20	19	18	17
MAP_RAMECC_ENABLE_SET	SR_RAMECC_ENABLE_SET	BCDMA_RNGOCC_RAMECC_ENABLE_SET	BCDMA_STS_RAMECC1_ENABLE_SET	BCDMA_STS_RAMECC0_ENABLE_SET	BCDMA_RPCF2_RAMECC_ENABLE_SET	BCDMA_RPCF1_RAMECC_ENABLE_SET	BCDMA_RPCF0_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
16	15	14	13	12	11	10	9
BCDMA_TPCF1_RAMECC_ENABLE_SET	BCDMA_TPCF0_RAMECC_ENABLE_SET	PCFD1_RAMECC_ENABLE_SET	PCFD0_RAMECC_ENABLE_SET	BCDMA_STATE_RAMECC_ENABLE_SET	BCDMA_CFG_RAMECC_ENABLE_SET	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	PKTDMA_STS_RAMECC1_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
PKTDMA_STS_RAMECC0_ENABLE_SET	PKTDMA_RPCF2_RAMECC_ENABLE_SET	PKTDMA_RPCF1_RAMECC_ENABLE_SET	PKTDMA_RPCF0_RAMECC_ENABLE_SET	PKTDMA_TPCF1_RAMECC_ENABLE_SET	PKTDMA_TPCF0_RAMECC_ENABLE_SET	PKTDMA_STATE_RAMECC_ENABLE_SET	PKTDMA_CFG_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9330. DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sr_ramecc_pend

Table 14-9330. DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_cfg_ramecc_pend

14.6.2.2.8 DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_CLR_REG0 Register

14.6.2.2.8.1 DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9331. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 50C0h

Figure 14-4626. DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_CLR_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED				MSRAM_RAMECC0_ENABLE_CLR	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	RINGACC_STRAM_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
24	23	22	21	20	19	18	17
MAP_RAMECC_ENABLE_CLR	SR_RAMECC_ENABLE_CLR	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	BCDMA_STS_RAMECC1_ENABLE_CLR	BCDMA_STS_RAMECC0_ENABLE_CLR	BCDMA_RPCF2_RAMECC_ENABLE_CLR	BCDMA_RPCF1_RAMECC_ENABLE_CLR	BCDMA_RPCF0_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
16	15	14	13	12	11	10	9
BCDMA_TPCF1_RAMECC_ENABLE_CLR	BCDMA_TPCF0_RAMECC_ENABLE_CLR	PCFD1_RAMECC_ENABLE_CLR	PCFD0_RAMECC_ENABLE_CLR	BCDMA_STATE_RAMECC_ENABLE_CLR	BCDMA_CFG_RAMECC_ENABLE_CLR	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	PKTDMA_STS_RAMECC1_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
PKTDMA_STS_RAMECC0_ENABLE_CLR	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	PKTDMA_STATE_RAMECC_ENABLE_CLR	PKTDMA_CFG_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9332. DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sr_ramecc_pend

Table 14-9332. DMASS_ECC_AGGR_0_ECCAGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_cfg_ramecc_pend

14.6.2.2.9 DMASS_ECC_AGGR_0_ECCAGGR_DED_EOI_REG Register

14.6.2.2.9.1 DMASS_ECC_AGGR_0_ECCAGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-9333. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 513Ch

Figure 14-4627. DMASS_ECC_AGGR_0_ECCAGGR_DED_EOI_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-9334. DMASS_ECC_AGGR_0_ECCAGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.2.2.10 DMASS_ECC_AGGR_0_ECCAGGR_DED_STATUS_REG0 Register

14.6.2.2.10.1 DMASS_ECC_AGGR_0_ECCAGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9335. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5140h

Figure 14-4628. DMASS_ECC_AGGR_0_ECCAGGR_DED_STATUS_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED				MSRAM_RAMECC0_PEND	SEC_PROXY_BUFRAM_RAMECC_PEND	SEC_PROXY_STRAM_RAMECC_PEND	RINGACC_STRAM_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
24	23	22	21	20	19	18	17
MAP_RAMECC_PEND	SR_RAMECC_PEND	BCDMA_RNGOCC_RAMECC_PEND	BCDMA_STS_RAMECC1_PEND	BCDMA_STS_RAMECC0_PEND	BCDMA_RPCF2_RAMECC_PEND	BCDMA_RPCF1_RAMECC_PEND	BCDMA_RPCF0_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
16	15	14	13	12	11	10	9
BCDMA_TPCF1_RAMECC_PEND	BCDMA_TPCF0_RAMECC_PEND	PCFD1_RAMECC_PEND	PCFD0_RAMECC_PEND	BCDMA_STATE_RAMECC_PEND	BCDMA_CFG_RAMECC_PEND	PKTDMA_RNGOCC_RAMECC_PEND	PKTDMA_STS_RAMECC1_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
PKTDMA_STS_RAMECC0_PEND	PKTDMA_RPCF2_RAMECC_PEND	PKTDMA_RPCF1_RAMECC_PEND	PKTDMA_RPCF0_RAMECC_PEND	PKTDMA_TPCF1_RAMECC_PEND	PKTDMA_TPCF0_RAMECC_PEND	PKTDMA_STATE_RAMECC_PEND	PKTDMA_CFG_RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9336. DMASS_ECC_AGGR_0_ECCAGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ringacc_stram_ramecc_pend
23	MAP_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for map_ramecc_pend
22	SR_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for sr_ramecc_pend
21	BCDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc1_pend

Table 14-9336. DMASS_ECC_AGGR_0_ECCAGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	BCDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd1_ramecc_pend
12	PCFD0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for pktdma_cfg_ramecc_pend

14.6.2.2.11 DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_SET_REG0 Register

14.6.2.2.11.1 DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9337. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5180h

Figure 14-4629. DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_SET_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED				MSRAM_RAMECC0_ENABLE_SET	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	RINGACC_STRAM_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
24	23	22	21	20	19	18	17
MAP_RAMECC_ENABLE_SET	SR_RAMECC_ENABLE_SET	BCDMA_RNGOCC_RAMECC_ENABLE_SET	BCDMA_STS_RAMECC1_ENABLE_SET	BCDMA_STS_RAMECC0_ENABLE_SET	BCDMA_RPCF2_RAMECC_ENABLE_SET	BCDMA_RPCF1_RAMECC_ENABLE_SET	BCDMA_RPCF0_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
16	15	14	13	12	11	10	9
BCDMA_TPCF1_RAMECC_ENABLE_SET	BCDMA_TPCF0_RAMECC_ENABLE_SET	PCFD1_RAMECC_ENABLE_SET	PCFD0_RAMECC_ENABLE_SET	BCDMA_STATE_RAMECC_ENABLE_SET	BCDMA_CFG_RAMECC_ENABLE_SET	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	PKTDMA_STS_RAMECC1_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
PKTDMA_STS_RAMECC0_ENABLE_SET	PKTDMA_RPCF2_RAMECC_ENABLE_SET	PKTDMA_RPCF1_RAMECC_ENABLE_SET	PKTDMA_RPCF0_RAMECC_ENABLE_SET	PKTDMA_TPCF1_RAMECC_ENABLE_SET	PKTDMA_TPCF0_RAMECC_ENABLE_SET	PKTDMA_STATE_RAMECC_ENABLE_SET	PKTDMA_CFG_RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9338. DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sr_ramecc_pend

Table 14-9338. DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pktdma_cfg_ramecc_pend

14.6.2.2.12 DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_CLR_REG0 Register

14.6.2.2.12.1 DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9339. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 51C0h

Figure 14-4630. DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_CLR_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED				MSRAM_RAMECC0_ENABLE_CLR	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	RINGACC_STRAM_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
24	23	22	21	20	19	18	17
MAP_RAMECC_ENABLE_CLR	SR_RAMECC_ENABLE_CLR	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	BCDMA_STS_RAMECC1_ENABLE_CLR	BCDMA_STS_RAMECC0_ENABLE_CLR	BCDMA_RPCF2_RAMECC_ENABLE_CLR	BCDMA_RPCF1_RAMECC_ENABLE_CLR	BCDMA_RPCF0_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
16	15	14	13	12	11	10	9
BCDMA_TPCF1_RAMECC_ENABLE_CLR	BCDMA_TPCF0_RAMECC_ENABLE_CLR	PCFD1_RAMECC_ENABLE_CLR	PCFD0_RAMECC_ENABLE_CLR	BCDMA_STATE_RAMECC_ENABLE_CLR	BCDMA_CFG_RAMECC_ENABLE_CLR	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	PKTDMA_STS_RAMECC1_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
PKTDMA_STS_RAMECC0_ENABLE_CLR	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	PKTDMA_STATE_RAMECC_ENABLE_CLR	PKTDMA_CFG_RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9340. DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27	MSRAM_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for msram_ramecc0_pend
26	SEC_PROXY_BUFRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_bufram_ramecc_pend
25	SEC_PROXY_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sec_proxy_stram_ramecc_pend
24	RINGACC_STRAM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ringacc_stram_ramecc_pend
23	MAP_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for map_ramecc_pend
22	SR_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sr_ramecc_pend

Table 14-9340. DMASS_ECC_AGGR_0_ECCAGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BCDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rngocc_ramecc_pend
20	BCDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc1_pend
19	BCDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_sts_ramecc0_pend
18	BCDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf2_ramecc_pend
17	BCDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf1_ramecc_pend
16	BCDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_rpcf0_ramecc_pend
15	BCDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf1_ramecc_pend
14	BCDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_tpcf0_ramecc_pend
13	PCFD1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd1_ramecc_pend
12	PCFD0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pcfd0_ramecc_pend
11	BCDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_state_ramecc_pend
10	BCDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for bcdma_cfg_ramecc_pend
9	PKTDMA_RNGOCC_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rngocc_ramecc_pend
8	PKTDMA_STS_RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc1_pend
7	PKTDMA_STS_RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_sts_ramecc0_pend
6	PKTDMA_RPCF2_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf2_ramecc_pend
5	PKTDMA_RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf1_ramecc_pend
4	PKTDMA_RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_rpcf0_ramecc_pend
3	PKTDMA_TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf1_ramecc_pend
2	PKTDMA_TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_tpcf0_ramecc_pend
1	PKTDMA_STATE_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_state_ramecc_pend
0	PKTDMA_CFG_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pktdma_cfg_ramecc_pend

14.6.2.2.13 DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_SET Register

14.6.2.2.13.1 DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-9341. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5200h

Figure 14-4631. DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_SET Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-9342. DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.6.2.2.14 DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_CLR Register

14.6.2.2.14.1 DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-9343. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5204h

Figure 14-4632. DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_CLR Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-9344. DMASS_ECC_AGGR_0_ECCAGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.6.2.2.15 DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_SET Register

14.6.2.2.15.1 DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-9345. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 5208h

Figure 14-4633. DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_SET Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-9346. DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.6.2.2.16 DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_CLR Register

14.6.2.2.16.1 DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-9347. Instance Table

Instance Name	Physical Address
DMASS0_ECC_AGGR_0	3F00 520Ch

Figure 14-4634. DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-9348. DMASS_ECC_AGGR_0_ECCAGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.6.3 DMASS_INTAGGR_0

DMASS_INTAGGR_0

14.6.3.1 DMASS_INTAGGR_0 Summaries

DMASS_INTAGGR_0 Summaries

Table 14-9349. INTAGGR_INTR Registers, Base Address=4800 0000h, Length=1048576

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_INTR_VINT_ENABLE_SET_J	4800 0000h + formula
8h	64	INTAGGR_INTR_VINT_ENABLE_CLEAR_J	4800 0008h + formula
10h	64	INTAGGR_INTR_VINT_STATUS_SET_J	4800 0010h + formula
18h	64	INTAGGR_INTR_VINT_STATUS_CLEAR_J	4800 0018h + formula
20h	64	INTAGGR_INTR_VINT_STATUSM_J	4800 0020h + formula

Table 14-9350. INTAGGR_IMAP Registers, Base Address=4810 0000h, Length=16384

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_IMAP_GEVI_IMAP_J	4810 0000h + formula

Table 14-9351. INTAGGR_CFG Registers, Base Address=4811 0000h, Length=32

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_CFG_REVISION	4811 0000h
8h	64	INTAGGR_CFG_INTCAP	4811 0008h
10h	64	INTAGGR_CFG_AUXCAP	4811 0010h

Table 14-9352. INTAGGR_L2G Registers, Base Address=4812 0000h, Length=1024

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_L2G_LEVI_MAP_J	4812 0000h + formula

Table 14-9353. INTAGGR_UNMAP Registers, Base Address=4818 0000h, Length=131072

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
8000h	64	INTAGGR_UNMAP_UNMAP0_MAP_J	4818 8000h + formula
9000h	64	INTAGGR_UNMAP_UNMAP1_MAP_J	4818 9000h + formula
A000h	64	INTAGGR_UNMAP_UNMAP2_MAP_J	4818 A000h + formula
B000h	64	INTAGGR_UNMAP_UNMAP3_MAP_J	4818 B000h + formula
C000h	64	INTAGGR_UNMAP_UNMAP4_MAP_J	4818 C000h + formula
D000h	64	INTAGGR_UNMAP_UNMAP5_MAP	4818 D000h + formula
10000h	64	INTAGGR_UNMAP_UNMAP6_MAP_J	4819 0000h + formula
11000h	64	INTAGGR_UNMAP_UNMAP7_MAP_J	4819 1000h + formula
12000h	64	INTAGGR_UNMAP_UNMAP8_MAP_J	4819 2000h + formula
13000h	64	INTAGGR_UNMAP_UNMAP9_MAP_J	4819 3000h + formula
14000h	64	INTAGGR_UNMAP_UNMAP10_MAP_J	4819 4000h + formula
15000h	64	INTAGGR_UNMAP_UNMAP11_MAP_J	4819 5000h + formula
16000h	64	INTAGGR_UNMAP_UNMAP12_MAP_J	4819 6000h + formula
17000h	64	INTAGGR_UNMAP_UNMAP13_MAP_J	4819 7000h + formula
18000h	64	INTAGGR_UNMAP_UNMAP14_MAP_J	4819 8000h + formula

Table 14-9354. INTAGGR_MCAST Registers, Base Address=4821 0000h, Length=4096

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_MCAST_GEVI_MCMAP_J	4821 0000h + formula

Table 14-9355. INTAGGR_GCNTCFG Registers, Base Address=4822 0000h, Length=8192

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_GCNTCFG_GEVI_MAP_J	4822 0000h + formula

Table 14-9356. INTAGGR_GCNTRTI Registers, Base Address=4A00 0000h, Length=1048576

Offset	Length	Register Name	DMASS0_INTAGGR_0 Physical Address
0h	64	INTAGGR_GCNTRTI_GEVI_COUNT_J	4A00 0000h + formula

14.6.3.2 DMASS_INTAGGR_0 Registers

DMASS_INTAGGR_0 Registers

14.6.3.2.1 INTAGGR_INTR_VINT_ENABLE_SET_J Register

14.6.3.2.1.1 INTAGGR_INTR_VINT_ENABLE_SET_J Register (Offset = 0h) [reset = 0h]

The Interrupt Enable Set register is written by software to enable (i.e. unmask) specified bits to allow their current status to be considered in the generation of the corresponding level sensitive virtual interrupt output.

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Table 14-9357. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4800 0000h + formula

Figure 14-4635. INTAGGR_INTR_VINT_ENABLE_SET_j Name Register

63	62	61	60	59	58	57	48
INTR_ENABLE							
R/W1TS							
0h							
55	54	53	52	51	50	49	48
INTR_ENABLE							
R/W1TS							
0h							
47	46	45	44	43	42	41	40
INTR_ENABLE							
R/W1TS							
0h							
39	38	37	36	35	34	33	32
INTR_ENABLE							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
INTR_ENABLE							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
INTR_ENABLE							
R/W1TS							
0h							

Table 14-9358. INTAGGR_INTR_VINT_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_ENABLE	R/W1TS	0h	Interrupt enable set value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be set. Reads will reflect back the current status of the internal interrupt enable register. Reset Source: srst_n

14.6.3.2.2 INTAGGR_INTR_VINT_ENABLE_CLEAR_J Register

14.6.3.2.2.1 INTAGGR_INTR_VINT_ENABLE_CLEAR_J Register (Offset = 8h) [reset = 0h]

The Interrupt Enable Clear register is written by software to disable (i.e. mask) specified bits to disallow their current status from be considered in the generation of the corresponding level sensitive virtual interrupt output.

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Table 14-9359. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4800 0008h + formula

Figure 14-4636. INTAGGR_INTR_VINT_ENABLE_CLEAR_j Name Register

63	62	61	60	59	58	57	48
INTR_ENABLE							
R/W1TC							
0h							
55	54	53	52	51	50	49	48
INTR_ENABLE							
R/W1TC							
0h							
47	46	45	44	43	42	41	40
INTR_ENABLE							
R/W1TC							
0h							
39	38	37	36	35	34	33	32
INTR_ENABLE							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
INTR_ENABLE							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
INTR_ENABLE							
R/W1TC							
0h							

Table 14-9360. INTAGGR_INTR_VINT_ENABLE_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_ENABLE	R/W1TC	0h	Interrupt enable clear value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be cleared. Reads will reflect back the current status of the internal interrupt enable register. Reset Source: srst_n

14.6.3.2.3 INTAGGR_INTR_VINT_STATUS_SET_J Register

14.6.3.2.3.1 INTAGGR_INTR_VINT_STATUS_SET_J Register (Offset = 10h) [reset = 0h]

The Interrupt Status register is read by software to determine the cause of an interrupt.

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Table 14-9361. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4800 0010h + formula

Figure 14-4637. INTAGGR_INTR_VINT_STATUS_SET_j Name Register

63	62	61	60	59	58	57	48
INTR_STATUS							
R/W1TS							
0h							
55	54	53	52	51	50	49	48
INTR_STATUS							
R/W1TS							
0h							
47	46	45	44	43	42	41	40
INTR_STATUS							
R/W1TS							
0h							
39	38	37	36	35	34	33	32
INTR_STATUS							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
INTR_STATUS							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
INTR_STATUS							
R/W1TS							
0h							

Table 14-9362. INTAGGR_INTR_VINT_STATUS_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUS	R/W1TS	0h	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be set Reset Source: srst_n

14.6.3.2.4 INTAGGR_INTR_VINT_STATUS_CLEAR_J Register

14.6.3.2.4.1 INTAGGR_INTR_VINT_STATUS_CLEAR_J Register (Offset = 18h) [reset = 0h]

The Interrupt Status register is read by software to determine the cause of an interrupt.

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Table 14-9363. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4800 0018h + formula

Figure 14-4638. INTAGGR_INTR_VINT_STATUS_CLEAR_j Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">INTR_STATUS</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">INTR_STATUS</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">INTR_STATUS</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">INTR_STATUS</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">INTR_STATUS</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTR_STATUS</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9364. INTAGGR_INTR_VINT_STATUS_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUS	R/W1TC	0h	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be cleared Reset Source: srst_n

14.6.3.2.5 INTAGGR_INTR_VINT_STATUSM_J Register

14.6.3.2.5.1 INTAGGR_INTR_VINT_STATUSM_J Register (Offset = 20h) [reset = 0h]

The Interrupt Masked Status register can be read by software to determine the cause of an interrupt.

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Table 14-9365. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4800 0020h + formula

Figure 14-4639. INTAGGR_INTR_VINT_STATUSM_j Name Register

63	62	61	60	59	58	57	48
INTR_STATUSM							
R/NA							
0h							
55	54	53	52	51	50	49	48
INTR_STATUSM							
R/NA							
0h							
47	46	45	44	43	42	41	40
INTR_STATUSM							
R/NA							
0h							
39	38	37	36	35	34	33	32
INTR_STATUSM							
R/NA							
0h							
15	14	13	12	11	10	9	8
INTR_STATUSM							
R/NA							
0h							
7	6	5	4	3	2	1	0
INTR_STATUSM							
R/NA							
0h							

Table 14-9366. INTAGGR_INTR_VINT_STATUSM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTR_STATUSM	R/NA	0h	Masked state of bits in internal interrupt status register. This value is the result of bitwise ANDing the interrupt enable and status registers Reset Source: srst_n

14.6.3.2.6 INTAGGR_IMAP_GEVI_IMAP_J Register

14.6.3.2.6.1 INTAGGR_IMAP_GEVI_IMAP_J Register (Offset = 0h) [reset = 0h]

The Interrupt Mapping Register controls which of N virtual interrupt source outputs this channels physical interrupt sources will map onto.

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Table 14-9367. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4810 0000h + formula

Figure 14-4640. INTAGGR_IMAP_GEVI_IMAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
REGNUM							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED		BITNUM					
NONE		R/W					
0h		0h					

Table 14-9368. INTAGGR_IMAP_GEVI_IMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:17	RESERVED	NONE	0h	Reserved
16:8	REGNUM	R/W	0h	Virtual interrupt status register number: this field specifies which of the potential virtual interrupt cause registers the event pending bit will appear in. Reset Source: srst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	BITNUM	R/W	0h	Virtual interrupt cause register bit number: this field specifies which of the 64 bits in the specified virtual interrupt cause register the event pending bit will appear in. Reset Source: srst_n

14.6.3.2.7 INTAGGR_CFG_REVISION Register

14.6.3.2.7.1 INTAGGR_CFG_REVISION Register (Offset = 0h) [reset = 66961101h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-9369. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4811 0000h

Figure 14-4641. INTAGGR_CFG_REVISION Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
2h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-9370. INTAGGR_CFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31:16	MODID	R	6696h	Module ID field Reset Source: srst_n
15:11	REVRTL	R	2h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: srst_n

14.6.3.2.8 INTAGGR_CFG_INTCAP Register

14.6.3.2.8.1 INTAGGR_CFG_INTCAP Register (Offset = 8h) [reset = B80600h]

The IntCap Register contains information on virtual interrupts.

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Table 14-9371. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4811 0008h

Figure 14-4642. INTAGGR_CFG_INTCAP Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SEVT_CNT							
R							
600h							
7	6	5	4	3	2	1	0
SEVT_CNT							
R							
600h							

Table 14-9372. INTAGGR_CFG_INTCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31:16	VINTR_CNT	R	B8h	Virtual interrupt register/pin count Reset Source: srst_n
15:0	SEVT_CNT	R	600h	Number of 'event to virt int' mapping registers Reset Source: srst_n

14.6.3.2.9 INTAGGR_CFG_AUXCAP Register

14.6.3.2.9.1 INTAGGR_CFG_AUXCAP Register (Offset = 10h) [reset = 30320080002000E8h]

The AuxCap Register contains information on additional capabilities.

Return to Summary Table

Table 14-9373. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4811 0010h

Figure 14-4643. INTAGGR_CFG_AUXCAP Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">UNMAP_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3032h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">UNMAP_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3032h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">MEVI_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">80h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">MEVI_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">80h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GEVI_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GEVI_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">100h</td></tr>
</table>

Table 14-9374. INTAGGR_CFG_AUXCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	UNMAP_CNT	R	3032h	Number of multicast event registers. Not all registers in the range are necessarily valid. Reset Source: srst_n
47:32	MEVI_CNT	R	80h	Number of multicast event registers Reset Source: srst_n
31:16	LEVI_CNT	R	20h	Local input events for local to global translation Reset Source: srst_n
15:0	GEVI_CNT	R	100h	Number of event counting registers Reset Source: srst_n

14.6.3.2.10 INTAGGR_L2G_LEVI_MAP_J Register

14.6.3.2.10.1 INTAGGR_L2G_LEVI_MAP_J Register (Offset = 0h) [reset = FFFFh]

This register determines how the ordinal local event is translated to a global event on the outgoing event transport lane. Both pulse and rising edge local event types are supported. With pulsed events, the event count is determined by the number of cycles for which the event signal remains high. For rising edge events, the count represents the total number of rising edge transitions. The index field of the register determines the outgoing global event index, and the mode bit specifies either pulsed or rising edge local event detection.

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Table 14-9375. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4812 0000h + formula

Figure 14-4644. INTAGGR_L2G_LEVI_MAP_j Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GEVIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GEVIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-9376. INTAGGR_L2G_LEVI_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	MODE	R/W	0h	Local event detection mode. This field is set to 0 for pulsed events, and to 1 for rising edge eventss Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	GEVIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.11 INTAGGR_UNMAP_UNMAP0_MAP_J Register

14.6.3.2.11.1 INTAGGR_UNMAP_UNMAP0_MAP_J Register (Offset = 8000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9377. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4818 8000h + formula

Figure 14-4645. INTAGGR_UNMAP_UNMAP0_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9378. INTAGGR_UNMAP_UNMAP0_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.12 INTAGGR_UNMAP_UNMAP1_MAP_J Register

14.6.3.2.12.1 INTAGGR_UNMAP_UNMAP1_MAP_J Register (Offset = 9000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9379. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4818 9000h + formula

Figure 14-4646. INTAGGR_UNMAP_UNMAP1_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9380. INTAGGR_UNMAP_UNMAP1_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.13 INTAGGR_UNMAP_UNMAP2_MAP_J Register

14.6.3.2.13.1 INTAGGR_UNMAP_UNMAP2_MAP_J Register (Offset = A000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9381. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4818 A000h + formula

Figure 14-4647. INTAGGR_UNMAP_UNMAP2_MAP_j Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-9382. INTAGGR_UNMAP_UNMAP2_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.14 INTAGGR_UNMAP_UNMAP3_MAP_J Register

14.6.3.2.14.1 INTAGGR_UNMAP_UNMAP3_MAP_J Register (Offset = B000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9383. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4818 B000h + formula

Figure 14-4648. INTAGGR_UNMAP_UNMAP3_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9384. INTAGGR_UNMAP_UNMAP3_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.15 INTAGGR_UNMAP_UNMAP4_MAP_J Register

14.6.3.2.15.1 INTAGGR_UNMAP_UNMAP4_MAP_J Register (Offset = C000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9385. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4818 C000h + formula

Figure 14-4649. INTAGGR_UNMAP_UNMAP4_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9386. INTAGGR_UNMAP_UNMAP4_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.16 INTAGGR_UNMAP_UNMAP5_MAP Register

14.6.3.2.16.1 INTAGGR_UNMAP_UNMAP5_MAP Register (Offset = D000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9387. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4818 D000h + formula

Figure 14-4650. INTAGGR_UNMAP_UNMAP5_MAP Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UMAPIDX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-9388. INTAGGR_UNMAP_UNMAP5_MAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.17 INTAGGR_UNMAP_UNMAP6_MAP_J Register

14.6.3.2.17.1 INTAGGR_UNMAP_UNMAP6_MAP_J Register (Offset = 10000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9389. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 0000h + formula

Figure 14-4651. INTAGGR_UNMAP_UNMAP6_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9390. INTAGGR_UNMAP_UNMAP6_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.18 INTAGGR_UNMAP_UNMAP7_MAP_J Register

14.6.3.2.18.1 INTAGGR_UNMAP_UNMAP7_MAP_J Register (Offset = 11000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9391. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 1000h + formula

Figure 14-4652. INTAGGR_UNMAP_UNMAP7_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9392. INTAGGR_UNMAP_UNMAP7_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.19 INTAGGR_UNMAP_UNMAP8_MAP_J Register

14.6.3.2.19.1 INTAGGR_UNMAP_UNMAP8_MAP_J Register (Offset = 12000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9393. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 2000h + formula

Figure 14-4653. INTAGGR_UNMAP_UNMAP8_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9394. INTAGGR_UNMAP_UNMAP8_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.20 INTAGGR_UNMAP_UNMAP9_MAP_J Register

14.6.3.2.20.1 INTAGGR_UNMAP_UNMAP9_MAP_J Register (Offset = 13000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9395. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 3000h + formula

Figure 14-4654. INTAGGR_UNMAP_UNMAP9_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9396. INTAGGR_UNMAP_UNMAP9_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.21 INTAGGR_UNMAP_UNMAP10_MAP_J Register

14.6.3.2.21.1 INTAGGR_UNMAP_UNMAP10_MAP_J Register (Offset = 14000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9397. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 4000h + formula

Figure 14-4655. INTAGGR_UNMAP_UNMAP10_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9398. INTAGGR_UNMAP_UNMAP10_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.22 INTAGGR_UNMAP_UNMAP11_MAP_J Register

14.6.3.2.22.1 INTAGGR_UNMAP_UNMAP11_MAP_J Register (Offset = 15000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9399. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 5000h + formula

Figure 14-4656. INTAGGR_UNMAP_UNMAP11_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9400. INTAGGR_UNMAP_UNMAP11_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.23 INTAGGR_UNMAP_UNMAP12_MAP_J Register

14.6.3.2.23.1 INTAGGR_UNMAP_UNMAP12_MAP_J Register (Offset = 16000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

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Table 14-9401. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 6000h + formula

Figure 14-4657. INTAGGR_UNMAP_UNMAP12_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9402. INTAGGR_UNMAP_UNMAP12_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.24 INTAGGR_UNMAP_UNMAP13_MAP_J Register

14.6.3.2.24.1 INTAGGR_UNMAP_UNMAP13_MAP_J Register (Offset = 17000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9403. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 7000h + formula

Figure 14-4658. INTAGGR_UNMAP_UNMAP13_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9404. INTAGGR_UNMAP_UNMAP13_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.25 INTAGGR_UNMAP_UNMAP14_MAP_J Register

14.6.3.2.25.1 INTAGGR_UNMAP_UNMAP14_MAP_J Register (Offset = 18000h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this unmapped event. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

Return to Summary Table

Table 14-9405. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4819 8000h + formula

Figure 14-4659. INTAGGR_UNMAP_UNMAP14_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UMAPIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
UMAPIDX							
R/W							
FFFFh							

Table 14-9406. INTAGGR_UNMAP_UNMAP14_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	UMAPIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.26 INTAGGR_MCAST_GEVI_MCMAP_J Register

14.6.3.2.26.1 INTAGGR_MCAST_GEVI_MCMAP_J Register (Offset = 0h) [reset = FFFF0000FFFFh]

This register determines how ingress global events from the ingress global event ETL are written out to the two egress global event ETL intefaces. The index of each of the two egress events is stored in this register, which is selected based in the ingress event index value.

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Table 14-9407. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4821 0000h + formula

Figure 14-4660. INTAGGR_MCAST_GEVI_MCMAP_j Name Register

63	62	61	60	59	58	57	48
IRQMODE1	RESERVED						
R/W	NONE						
0h	0h						
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
GEVIDX1							
R/W							
FFFFh							
39	38	37	36	35	34	33	32
GEVIDX1							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
GEVIDX0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
GEVIDX0							
R/W							
FFFFh							

Table 14-9408. INTAGGR_MCAST_GEVI_MCMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63	IRQMODE1	R/W	0h	IRQ Mode Flag 1. When set, this register act like a mapper with bitnum in 37:32 and regnum in 46:38. Reset Source: srst_n
62:48	RESERVED	NONE	0h	Reserved
47:32	GEVIDX1	R/W	FFFFh	Global event index 1. This field specifies the index of the outgoing global event on ETL 1. Set to 0xFFFF to disable. Reset Source: srst_n
31	IRQMODE0	R/W	0h	IRQ Mode Flag 0. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved

Table 14-9408. INTAGGR_MCAST_GEVI_MCMAP_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	GEVIDX0	R/W	FFFFh	Global event index 0. This field specifies the index of the outgoing global event on ETL 0. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.27 INTAGGR_GCNTCFG_GEVI_MAP_J Register

14.6.3.2.27.1 INTAGGR_GCNTCFG_GEVI_MAP_J Register (Offset = 0h) [reset = FFFFh]

The Global Event Mapping register controls the egress global event index for this event count. This register may also be optionally used to directly set an interrupt status bit by using the irqmode flag.

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Table 14-9409. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4822 0000h + formula

Figure 14-4661. INTAGGR_GCNTCFG_GEVI_MAP_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
GEVIDX							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
GEVIDX							
R/W							
FFFFh							

Table 14-9410. INTAGGR_GCNTCFG_GEVI_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31	IRQMODE	R/W	0h	IRQ Mode Flag. When set, this register act like a mapper with bitnum in 5:0 and regnum in 14:6. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	GEVIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable. Reset Source: srst_n

14.6.3.2.28 INTAGGR_GCNTRTI_GEVI_COUNT_J Register

14.6.3.2.28.1 INTAGGR_GCNTRTI_GEVI_COUNT_J Register (Offset = 0h) [reset = 0h]

The ETL Count register is read by software to determine how many times the event message has been received. This register can be written to decrement the count by a specified amount to acknowledge that a count has been processed by the host.

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Table 14-9411. Instance Table

Instance Name	Physical Address
DMASS0_INTAGGR_0	4A00 0000h + formula

Figure 14-4662. INTAGGR_GCNTRTI_GEVI_COUNT_j Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/WTD							
0h							

Table 14-9412. INTAGGR_GCNTRTI_GEVI_COUNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63:32	RESERVED	NONE	0h	Reserved
31:0	CCNT	R/WTD	0h	Current count. This field is incremented by the event count for each message received with this event on the Counted ETL Interface. On write, this field will be decremented by the value written. Writing a value greater than the current count is illegal. Reset Source: srst_n

14.6.4 DMASS_PKTDMA_0

DMASS_PKTDMA_0

14.6.4.1 DMASS_PKTDMA_0 Summaries

DMASS_PKTDMA_0 Summaries

Table 14-9413. LCDMA_RINGACC_CRED Registers, Base Address=4581 0000h, Length=4096

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	LCDMA_RINGACC_CRED_RING_CRED_J	4581 0000h + formula

Table 14-9414. PKTDMA_RXFCFG Registers, Base Address=4843 0000h, Length=4096

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_RXFCFG_FLOW_RFA_J	4843 0000h + formula

Table 14-9415. PKTDMA_TXCCFG Registers, Base Address=484A 0000h, Length=16384

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_TXCCFG_CHAN_TCFG_J	484A 0000h + formula
64h	32	PKTDMA_TXCCFG_CHAN_TPRI_CTRL_J	484A 0064h + formula
68h	32	PKTDMA_TXCCFG_CHAN_THREAD_J	484A 0068h + formula
70h	32	PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_J	484A 0070h + formula
80h	32	PKTDMA_TXCCFG_CHAN_TST_SCHED_J	484A 0080h + formula

Table 14-9416. PKTDMA_RXCCFG Registers, Base Address=484C 0000h, Length=8192

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_RXCCFG_CHAN_RCFG_J	484C 0000h + formula
64h	32	PKTDMA_RXCCFG_CHAN_RPRI_CTRL_J	484C 0064h + formula
68h	32	PKTDMA_RXCCFG_CHAN_THREAD_J	484C 0068h + formula
80h	32	PKTDMA_RXCCFG_CHAN_RST_SCHED_J	484C 0080h + formula

Table 14-9417. PKTDMA_GCFG Registers, Base Address=485C 0000h, Length=256

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_GCFG_REVISION	485C 0000h
4h	32	PKTDMA_GCFG_PERF_CTRL	485C 0004h
8h	32	PKTDMA_GCFG_EMU_CTRL	485C 0008h
10h	32	PKTDMA_GCFG_PSIL_TO	485C 0010h
20h	32	PKTDMA_GCFG_CAP0	485C 0020h
24h	32	PKTDMA_GCFG_CAP1	485C 0024h
28h	32	PKTDMA_GCFG_CAP2	485C 0028h
2Ch	32	PKTDMA_GCFG_CAP3	485C 002Ch
30h	32	PKTDMA_GCFG_CAP4	485C 0030h
60h	32	PKTDMA_GCFG_PM0	485C 0060h
64h	32	PKTDMA_GCFG_PM1	485C 0064h
78h	32	PKTDMA_GCFG_DBGADDR	485C 0078h
7Ch	32	PKTDMA_GCFG_DBGDATA	485C 007Ch
88h	32	PKTDMA_GCFG_RFLOWFWSTAT	485C 0088h

Table 14-9418. LCDMA_RINGACC_RING_CFG Registers, Base Address=485E 0000h, Length=65536

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
40h	32	LCDMA_RINGACC_RING_CFG_RING_BA_LO_J	485E 0040h + formula
44h	32	LCDMA_RINGACC_RING_CFG_RING_BA_HI_J	485E 0044h + formula
48h	32	LCDMA_RINGACC_RING_CFG_RING_SIZE_J	485E 0048h + formula

Table 14-9419. PKTDMA_RXCRT Registers, Base Address=4A80 0000h, Length=131072

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_RXCRT_CHAN_CTL_J	4A80 0000h + formula
40h	32	PKTDMA_RXCRT_CHAN_STATUS0_J	4A80 0040h + formula
44h	32	PKTDMA_RXCRT_CHAN_STATUS1_J	4A80 0044h + formula
80h	32	PKTDMA_RXCRT_CHAN_STDATA_J_K	4A80 0080h + formula
200h	32	PKTDMA_RXCRT_CHAN_PEER0_J	4A80 0200h + formula
204h	32	PKTDMA_RXCRT_CHAN_PEER1_J	4A80 0204h + formula
208h	32	PKTDMA_RXCRT_CHAN_PEER2_J	4A80 0208h + formula
20Ch	32	PKTDMA_RXCRT_CHAN_PEER3_J	4A80 020Ch + formula
210h	32	PKTDMA_RXCRT_CHAN_PEER4_J	4A80 0210h + formula
214h	32	PKTDMA_RXCRT_CHAN_PEER5_J	4A80 0214h + formula
218h	32	PKTDMA_RXCRT_CHAN_PEER6_J	4A80 0218h + formula
21Ch	32	PKTDMA_RXCRT_CHAN_PEER7_J	4A80 021Ch + formula
220h	32	PKTDMA_RXCRT_CHAN_PEER8_J	4A80 0220h + formula
224h	32	PKTDMA_RXCRT_CHAN_PEER9_J	4A80 0224h + formula
228h	32	PKTDMA_RXCRT_CHAN_PEER10_J	4A80 0228h + formula
22Ch	32	PKTDMA_RXCRT_CHAN_PEER11_J	4A80 022Ch + formula
230h	32	PKTDMA_RXCRT_CHAN_PEER12_J	4A80 0230h + formula
234h	32	PKTDMA_RXCRT_CHAN_PEER13_J	4A80 0234h + formula
238h	32	PKTDMA_RXCRT_CHAN_PEER14_J	4A80 0238h + formula
23Ch	32	PKTDMA_RXCRT_CHAN_PEER15_J	4A80 023Ch + formula
400h	32	PKTDMA_RXCRT_CHAN_PCNT_J	4A80 0400h + formula
404h	32	PKTDMA_RXCRT_CHAN_DCNT_J	4A80 0404h + formula
408h	32	PKTDMA_RXCRT_CHAN_BCNT_J	4A80 0408h + formula
410h	32	PKTDMA_RXCRT_CHAN_SBCNT_J	4A80 0410h + formula

Table 14-9420. PKTDMA_TXCRT Registers, Base Address=4AA0 0000h, Length=262144

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
0h	32	PKTDMA_TXCRT_CHAN_CTL_J	4AA0 0000h + formula
40h	32	PKTDMA_TXCRT_CHAN_STATUS0_J	4AA0 0040h + formula
44h	32	PKTDMA_TXCRT_CHAN_STATUS1_J	4AA0 0044h + formula
80h	32	PKTDMA_TXCRT_CHAN_STDATA_J_K	4AA0 0080h + formula
200h	32	PKTDMA_TXCRT_CHAN_PEER0_J	4AA0 0200h + formula
204h	32	PKTDMA_TXCRT_CHAN_PEER1_J	4AA0 0204h + formula
208h	32	PKTDMA_TXCRT_CHAN_PEER2_J	4AA0 0208h + formula
20Ch	32	PKTDMA_TXCRT_CHAN_PEER3_J	4AA0 020Ch + formula
210h	32	PKTDMA_TXCRT_CHAN_PEER4_J	4AA0 0210h + formula
214h	32	PKTDMA_TXCRT_CHAN_PEER5_J	4AA0 0214h + formula
218h	32	PKTDMA_TXCRT_CHAN_PEER6_J	4AA0 0218h + formula
21Ch	32	PKTDMA_TXCRT_CHAN_PEER7_J	4AA0 021Ch + formula
220h	32	PKTDMA_TXCRT_CHAN_PEER8_J	4AA0 0220h + formula

Table 14-9420. PKTDMA_TXCRT Registers, Base Address=4AA0 0000h, Length=262144 (continued)

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
224h	32	PKTDMA_TXCRT_CHAN_PEER9_J	4AA0 0224h + formula
228h	32	PKTDMA_TXCRT_CHAN_PEER10_J	4AA0 0228h + formula
22Ch	32	PKTDMA_TXCRT_CHAN_PEER11_J	4AA0 022Ch + formula
230h	32	PKTDMA_TXCRT_CHAN_PEER12_J	4AA0 0230h + formula
234h	32	PKTDMA_TXCRT_CHAN_PEER13_J	4AA0 0234h + formula
238h	32	PKTDMA_TXCRT_CHAN_PEER14_J	4AA0 0238h + formula
23Ch	32	PKTDMA_TXCRT_CHAN_PEER15_J	4AA0 023Ch + formula
400h	32	PKTDMA_TXCRT_CHAN_PCNT_J	4AA0 0400h + formula
408h	32	PKTDMA_TXCRT_CHAN_BCNT_J	4AA0 0408h + formula
410h	32	PKTDMA_TXCRT_CHAN_SBCNT_J	4AA0 0410h + formula

Table 14-9421. LCDMA_RINGACC_RINGRT Registers, Base Address=4B80 0000h, Length=2097152

Offset	Length	Register Name	DMASS0_PKTDMA_0 Physical Address
10h	32	LCDMA_RINGACC_RINGRT_RING_FDB_J	4B80 0010h + formula
18h	32	LCDMA_RINGACC_RINGRT_RING_FOCC_J	4B80 0018h + formula
1010h	32	LCDMA_RINGACC_RINGRT_RING_RDB_J	4B80 1010h + formula
1018h	32	LCDMA_RINGACC_RINGRT_RING_ROCC_J	4B80 1018h + formula

14.6.4.2 DMASS_PKTDMA_0 Registers

DMASS_PKTDMA_0 Registers

14.6.4.2.1 LCDMA_RINGACC_CRED_RING_CRED_J Register

14.6.4.2.1.1 LCDMA_RINGACC_CRED_RING_CRED_J Register (Offset = 0h) [reset = 0h]

The Credentials Register provides credentials to be used when performing memory accesses using this flow.

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Table 14-9422. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4581 0000h + formula

Figure 14-4663. LCDMA_RINGACC_CRED_RING_CRED_j Name Register

31	30	29	28	27	26	25	24
CHK_SECURE	RESERVED				SECURE	PRIV	
R/W	NONE				R/W	R/W	
0h	0h				0h	0h	
23	22	21	20	19	18	17	16
PRIVID							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9423. LCDMA_RINGACC_CRED_RING_CRED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CHK_SECURE	R/W	0h	Check secure control bit Reset Source: rst_mod_g_rst_n
30:27	RESERVED	NONE	0h	Reserved
26	SECURE	R/W	0h	Secure attribute Reset Source: rst_mod_g_rst_n
25:24	PRIV	R/W	0h	Privelege attribute Reset Source: rst_mod_g_rst_n
23:16	PRIVID	R/W	0h	Privelege ID attribute Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.4.2.2 PKTDMA_RXFCFG_FLOW_RFA_J Register

14.6.4.2.2.1 PKTDMA_RXFCFG_FLOW_RFA_J Register (Offset = 0h) [reset = 0h]

The Rx Flow N Configuration Register A contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. The fields in this register are as follows:

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Table 14-9424. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4843 0000h + formula

Figure 14-4664. PKTDMA_RXFCFG_FLOW_RFA_j Name Register

31	30	29	28	27	26	25	24
RESERVED	RX_EINFO_PRESENT	RX_PSINFO_PRESENT	RX_ERROR_HANDLING	RESERVED			RX_SOP_OFFSET
NONE	R/W	R/W	R/W	NONE			R/W
0h	0h	0h	0h	0h			0h
23	22	21	20	19	18	17	16
RX_SOP_OFFSET							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9425. PKTDMA_RXFCFG_FLOW_RFA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30	RX_EINFO_PRESENT	R/W	0h	Rx Extended Packet Info Block Present: This bit controls whether or not the Extended Packet Info Block will be present in the Rx Packet Descriptor. If this bit is clear, the port DMA will clear the Extended Packet Info Present bit in the PD and will drop any Timestamp or SW Data words that are presented from the back end application. If this bit is set, the port DMA will set the Extended Packet Info Block Present bit in the PD and will copy any Timestamp or SW Data words that are presented across the Rx streaming interface into the Extended Packet Info Block words in the descriptor. If no Timestamp or SW Data words are presented from the back end application, the port DMA will overwrite the fields in the PD with zeroes. Reset Source: rst_mod_g_rst_n
29	RX_PSINFO_PRESENT	R/W	0h	Rx PS Words Present: This bit controls whether or not the Protocol Specific words will be present in the Rx Packet Descriptor. If this bit is clear, the port DMA will set the PS word count to 0 in the PD and will drop any PS words that are presented from the back end application. If this bit is set, the port DMA will set the PS word count to the value given by the back end application and will copy the PS words from the back end application to the location Reset Source: rst_mod_g_rst_n

Table 14-9425. PKTDMA_RXFCFG_FLOW_RFA_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	RX_ERROR_HANDLING	R/W	0h	Rx Error Handling Mode: This bit controls the error handling mode for the flow and is only used when channel errors (i.e. descriptor starvation) occurs. 0 = Starvation errors result in dropping packet and incrementing dropped packet count. 1 = Starvation errors result in the channel waiting until descriptors are added to the free queue before the channel will be scheduled. Reset Source: rst_mod_g_rst_n
27:25	RESERVED	NONE	0h	Reserved
24:16	RX_SOP_OFFSET	R/W	0h	Rx Start of Packet Offset: This field specifies the number of bytes that are to be skipped in the SOP buffer before beginning to write the payload or protocol specific bytes(if they are in the sop buffer). This value must be less than the minimum size of a buffer in the system. Valid values are 0 - 255 bytes. The primary purpose of this field is to ensure that space is left in the descriptor to place the protocol specific information without overwriting or being overwritten by the Rx data. The secondary purpose of this field is to allow space to be left prior to the data in the descriptor in case header information needs to be added as the packet is passed thorough the system. Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.4.2.3 PKTDMA_TXCCFG_CHAN_TCFG_J Register

14.6.4.2.3.1 PKTDMA_TXCCFG_CHAN_TCFG_J Register (Offset = 0h) [reset = 20400h]

The Tx Channel Configuration Register is used to initialize static mode settings for the Tx DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

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Table 14-9426. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484A 0000h + formula

Figure 14-4665. PKTDMA_TXCCFG_CHAN_TCFG_j Name Register

31	30	29	28	27	26	25	24
TX_PAUSE_ON_ERR	TX_FILT_EINFO	TX_FILT_PSWORDS	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED				TX_CHAN_TYPE			
NONE				R			
0h				2h			
15	14	13	12	11	10	9	8
RESERVED				TX_BURST_SIZE		TX_TDTYPE	TX_NOTDPKT
NONE				R/W		R/W	R/W
0h				1h		0h	0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9427. PKTDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30	TX_FILT_EINFO	R/W	0h	This field controls whether or not the DMA controller will pass the extended packet information fields (if present) from the descriptor to the back end application. This field is encoded as follows: 0=DMA controller will pass extended packet info words if they are present in the descriptor 1=DMA controller will filter extended packet info words. Reset Source: rst_mod_g_rst_n
29	TX_FILT_PSWORDS	R/W	0h	This field controls whether or not the DMA controller will pass the protocol specific words (if present) from the descriptor to the back end application. This field is encoded as follows: 0=DMA controller will pass PS words if present in descriptor 1=DMA controller will filter PS words. Reset Source: rst_mod_g_rst_n
28:20	RESERVED	NONE	0h	Reserved

Table 14-9427. PKTDMA_TXCCFG_CHAN_TCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	TX_CHAN_TYPE	R	2h	Tx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 2 = Channel performs packet oriented data transfers using pass by reference rings. Channels configured in this mode can only use Host and Monolithic descriptors and the pointers to those descriptors are passed from/to SW using rings in the Ring Accelerator. Reset Source: rst_mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:10	TX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0,1 = 64 Bytes 2 = 128 Bytes All other values are reserved Reset Source: rst_mod_g_rst_n
9	TX_TDTYPE	R/W	0h	Specifies whether or not the channel should immediately return a teardown completion response to the default completion queue or wait until a status message is returned from the remote PSI-L paired peripheral. 0 = return immediately once all traffic is complete in PKTDMA. 1 = wait until remote peer sends back a completion message. Reset Source: rst_mod_g_rst_n
8	TX_NOTDPKT	R/W	0h	Specifies whether or not the channel should suppress sending the single data phase teardown packet when teardown is complete. 0 = TD packet is sent 1 = Suppress sending TD packet Reset Source: rst_mod_g_rst_n
7:0	RESERVED	NONE	0h	Reserved

14.6.4.2.4 PKTDMA_TXCCFG_CHAN_TPRI_CTRL_J Register

14.6.4.2.4.1 PKTDMA_TXCCFG_CHAN_TPRI_CTRL_J Register (Offset = 64h) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

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Table 14-9428. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484A 0064h + formula

Figure 14-4666. PKTDMA_TXCCFG_CHAN_TPRI_CTRL_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRIORITY			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ORDERID			
NONE				R/W			
0h				0h			

Table 14-9429. PKTDMA_TXCCFG_CHAN_TPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Tx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Tx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.5 PKTDMA_TXCCFG_CHAN_THREAD_J Register

14.6.4.2.5.1 PKTDMA_TXCCFG_CHAN_THREAD_J Register (Offset = 68h) [reset = 0h]

The thread ID mapping register is used to pair the Tx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

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Table 14-9430. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484A 0068h + formula

Figure 14-4667. PKTDMA_TXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-9431. PKTDMA_TXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.6 PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_J Register

14.6.4.2.6.1 PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_J Register (Offset = 70h) [reset = C0h]

The fifo depth register is used to specify how many FIFO data phases deep the Tx per channel FIFO will be for the channel. While the maximum depth of the Tx FIFO is set at design time, the FIFO depth can be artificially reduced in order to control the maximum latency which can be introduced due to buffering effects.

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Table 14-9432. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484A 0070h + formula

Figure 14-4668. PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FDEPTH							
R/W							
C0h							

Table 14-9433. PKTDMA_TXCCFG_CHAN_TFIFO_DEPTH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDEPTH	R/W	C0h	FIFO Depth: This field contains the number of Tx FIFO bytes which will be allowed to be stored for the channel. The minimum value is equal to the PSI-L interface data path width but must be greater than 32 bytes + the burst size, the maximum value varies by channel class (ultra-high capacity/high capacity/normal capacity) and is equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L data path width (tstrm_wdth). The fdepth must always be an integer multiple of tstrm_wdth. The reset value of this register varies by channel class (ultra-high capacity/ high capacity/normal capacity) but will be equal to the tubuf_size/ thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L interface data width (tstrm_wdth). Reset Source: rst_mod_g_rst_n

14.6.4.2.7 PKTDMA_TXCCFG_CHAN_TST_SCHED_J Register

14.6.4.2.7.1 PKTDMA_TXCCFG_CHAN_TST_SCHED_J Register (Offset = 80h) [reset = 0h]

The Tx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

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Table 14-9434. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484A 0080h + formula

Figure 14-4669. PKTDMA_TXCCFG_CHAN_TST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-9435. PKTDMA_TXCCFG_CHAN_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Tx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.6.4.2.8 PKTDMA_RXCCFG_CHAN_RCFG_J Register

14.6.4.2.8.1 PKTDMA_RXCCFG_CHAN_RCFG_J Register (Offset = 0h) [reset = 20400h]

The Rx Channel Configuration Register is used to initialize static mode settings for the Rx DMA channel. This register may only be written when the channel is disabled (rx_enable in realtime control reg is 0).

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Table 14-9436. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484C 0000h + formula

Figure 14-4670. PKTDMA_RXCCFG_CHAN_RCFG_j Name Register

31	30	29	28	27	26	25	24
RX_PAUSE_ON_ERR	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED				RX_CHAN_TYPE			
NONE				R/W			
0h				2h			

15	14	13	12	11	10	9	8
RESERVED				RX_BURST_SIZE		RESERVED	
NONE				R/W		NONE	
0h				1h		0h	

7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9437. PKTDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel. Reset Source: rst_mod_g_rst_n
30:20	RESERVED	NONE	0h	Reserved
19:16	RX_CHAN_TYPE	R/W	2h	Rx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host. Available channel types are as follows: 2 = Channel performs packet oriented data transfers using pass by reference rings. Channels configured in this mode can only use Host and Monolithic descriptors and the pointers to those descriptors are passed from/to SW using rings in the Ring Accelerator. 3 = Channel performs packet oriented data transfers using pass by reference rings with single buffer packet mode enabled. Channels configured in this mode can only use Host descriptors and each descriptor will be processed as an independent packet (no buffer chaining). This is the only packet oriented mode that can be used with data sources that are infinite streams (no EOP) 2 Normal channel 3 Single buffer mode channel
15:12	RESERVED	NONE	0h	Reserved

Table 14-9437. PKTDMA_RXCCFG_CHAN_RCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	RX_BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0,1 = 64 Bytes 2 = 128 Bytes All other values are reserved Reset Source: rst_mod_g_rst_n
9:0	RESERVED	NONE	0h	Reserved

14.6.4.2.9 PKTDMA_RXCCFG_CHAN_RPRI_CTRL_J Register

14.6.4.2.9.1 PKTDMA_RXCCFG_CHAN_RPRI_CTRL_J Register (Offset = 64h) [reset = 0h]

The priority control register is used to control the priority of the transactions which the DMA generates on it's initiator interface.

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Table 14-9438. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484C 0064h + formula

Figure 14-4671. PKTDMA_RXCCFG_CHAN_RPRI_CTRL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="3">PRIORITY</td><td colspan="4">RESERVED</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td colspan="4">NONE</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ORDERID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9439. PKTDMA_RXCCFG_CHAN_RPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRIORITY	R/W	0h	Rx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem*_cepriority outputs during all transactions for this channel. Reset Source: rst_mod_g_rst_n
27:4	RESERVED	NONE	0h	Reserved
3:0	ORDERID	R/W	0h	Rx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.10 PKTDMA_RXCCFG_CHAN_THREAD_J Register

14.6.4.2.10.1 PKTDMA_RXCCFG_CHAN_THREAD_J Register (Offset = 68h) [reset = 0h]

The thread ID mapping register is used to pair the Rx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

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Table 14-9440. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484C 0068h + formula

Figure 14-4672. PKTDMA_RXCCFG_CHAN_THREAD_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W							
0h							

Table 14-9441. PKTDMA_RXCCFG_CHAN_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	THREAD_ID	R/W	0h	Thread ID: This field contains the (up-to) 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.11 PKTDMA_RXCCFG_CHAN_RST_SCHED_J Register

14.6.4.2.11.1 PKTDMA_RXCCFG_CHAN_RST_SCHED_J Register (Offset = 80h) [reset = 0h]

The Rx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

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Table 14-9442. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	484C 0080h + formula

Figure 14-4673. PKTDMA_RXCCFG_CHAN_RST_SCHED_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
NONE						R/W	
0h						0h	

Table 14-9443. PKTDMA_RXCCFG_CHAN_RST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PRIORITY	R/W	0h	Rx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Rx DMA units. This field is encoded as follows: 0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority Arbitration between bins is performed in a strict priority fashion. High priority channels will always be serviced first. If no high priority channels are requesting then all medium-high priority channels will be serviced next. If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next. When no other channels are requesting, the low priority channels will be serviced. All channels within a given bin are serviced in a round robin order. Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration. Reset Source: rst_mod_g_rst_n

14.6.4.2.12 PKTDMA_GCFG_REVISION Register

14.6.4.2.12.1 PKTDMA_GCFG_REVISION Register (Offset = 0h) [reset = 662A9901h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-9444. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0000h

Figure 14-4674. PKTDMA_GCFG_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">662Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">662Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">13h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-9445. PKTDMA_GCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	662Ah	Module ID field Reset Source: rst_mod_g_rst_n
15:11	REVRTL	R	13h	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: rst_mod_g_rst_n

14.6.4.2.13 PKTDMA_GCFG_PERF_CTRL Register

14.6.4.2.13.1 PKTDMA_GCFG_PERF_CTRL Register (Offset = 4h) [reset = 40h]

The performance control register contains fields which can be used to adjust the performance of the PKTDMA in the system.

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Table 14-9446. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0004h

Figure 14-4675. PKTDMA_GCFG_PERF_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TIMEOUT_CNT							
R/W							
40h							
7	6	5	4	3	2	1	0
TIMEOUT_CNT							
R/W							
40h							

Table 14-9447. PKTDMA_GCFG_PERF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TIMEOUT_CNT	R/W	40h	This feature is not currently supported Reset Source: rst_mod_g_rst_n

14.6.4.2.14 PKTDMA_GCFG_EMU_CTRL Register

14.6.4.2.14.1 PKTDMA_GCFG_EMU_CTRL Register (Offset = 8h) [reset = 0h]

The emulation control register is used to control the behavior of the DMA when the emususp input is asserted.

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Table 14-9448. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0008h

Figure 14-4676. PKTDMA_GCFG_EMU_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-9449. PKTDMA_GCFG_EMU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Soft Reset Source: rst_mod_g_rst_n
0	FREE	R/W	0h	Free Reset Source: rst_mod_g_rst_n

14.6.4.2.15 PKTDMA_GCFG_PSIL_TO Register

14.6.4.2.15.1 PKTDMA_GCFG_PSIL_TO Register (Offset = 10h) [reset = 400h]

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrances on PSI-L configuration transactions issued by the built in PSI-L proxy.

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Table 14-9450. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0010h

Figure 14-4677. PKTDMA_GCFG_PSIL_TO Name Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W							
400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W							
400h							

Table 14-9451. PKTDMA_GCFG_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a conifiguration read or write transaction and asserting the tout bit Reset Source: rst_mod_g_rst_n

14.6.4.2.16 PKTDMA_GCFG_CAP0 Register

14.6.4.2.16.1 PKTDMA_GCFG_CAP0 Register (Offset = 20h) [reset = 0h]

The Capabilities Register 0 specifies which standard features this PKTDMA instance supports.

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Table 14-9452. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0020h

Figure 14-4678. PKTDMA_GCFG_CAP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9453. PKTDMA_GCFG_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.6.4.2.17 PKTDMA_GCFG_CAP1 Register

14.6.4.2.17.1 PKTDMA_GCFG_CAP1 Register (Offset = 24h) [reset = 0h]

The Capabilities Register 1 specifies which standard features this PKTDMA instance supports.

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Table 14-9454. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0024h

Figure 14-4679. PKTDMA_GCFG_CAP1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9455. PKTDMA_GCFG_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.6.4.2.18 PKTDMA_GCFG_CAP2 Register

14.6.4.2.18.1 PKTDMA_GCFG_CAP2 Register (Offset = 28h) [reset = 800025h]

The Capabilities Register 2 specifies how many resources this PKTDMA instance supports.

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Table 14-9456. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0028h

Figure 14-4680. PKTDMA_GCFG_CAP2 Name Register

31	30	29	28	27	26	25	24
RESERVED					RCHAN_CNT		
NONE					R		
0h					20h		
23	22	21	20	19	18	17	16
RCHAN_CNT						RESERVED	
R						NONE	
20h						0h	
15	14	13	12	11	10	9	8
RESERVED							TCHAN_CNT
NONE							R
0h							25h
7	6	5	4	3	2	1	0
TCHAN_CNT							
R							
25h							

Table 14-9457. PKTDMA_GCFG_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:18	RCHAN_CNT	R	20h	Rx internal channel count Reset Source: rst_mod_g_rst_n
17:9	RESERVED	NONE	0h	Reserved
8:0	TCHAN_CNT	R	25h	Tx internal channel count Reset Source: rst_mod_g_rst_n

14.6.4.2.19 PKTDMA_GCFG_CAP3 Register

14.6.4.2.19.1 PKTDMA_GCFG_CAP3 Register (Offset = 2Ch) [reset = 3Bh]

The Capabilities Register 3 specifies how many resources this PKTDMA instance supports.

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Table 14-9458. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 002Ch

Figure 14-4681. PKTDMA_GCFG_CAP3 Name Register

31	30	29	28	27	26	25	24
UCHAN_CNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UCHAN_CNT	HCHAN_CNT						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HCHAN_CNT		RFLOW_CNT					
R		R					
0h		3Bh					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RFLOW_CNT							
R							
3Bh							

Table 14-9459. PKTDMA_GCFG_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	UCHAN_CNT	R	0h	Tx ultra high capacity internal channel count Reset Source: rst_mod_g_rst_n
22:14	HCHAN_CNT	R	0h	Tx high capacity internal channel count Reset Source: rst_mod_g_rst_n
13:0	RFLOW_CNT	R	3Bh	Rx flow table entry count Reset Source: rst_mod_g_rst_n

14.6.4.2.20 PKTDMA_GCFG_CAP4 Register

14.6.4.2.20.1 PKTDMA_GCFG_CAP4 Register (Offset = 30h) [reset = 6Bh]

The Capabilities Register 4 specifies how many resources this PKTDMA instance supports.

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Table 14-9460. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0030h

Figure 14-4682. PKTDMA_GCFG_CAP4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TFLOW_CNT					
NONE		R					
0h		6Bh					
7	6	5	4	3	2	1	0
TFLOW_CNT							
R							
6Bh							

Table 14-9461. PKTDMA_GCFG_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TFLOW_CNT	R	6Bh	Tx flow table entry count Reset Source: rst_mod_g_rst_n

14.6.4.2.21 PKTDMA_GCFG_PM0 Register

14.6.4.2.21.1 PKTDMA_GCFG_PM0 Register (Offset = 60h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

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Table 14-9462. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0060h

Figure 14-4683. PKTDMA_GCFG_PM0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>NOGATE_RDU3</td><td>NOGATE_RDU2</td><td>NOGATE_RDU1</td><td>NOGATE_RDU0</td><td>NOGATE_TDU3</td><td>NOGATE_TDU2</td><td>NOGATE_TDU1</td><td>NOGATE_TDU0</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">NOGATE_RSVD4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">NOGATE_RSVD4</td><td>NOGATE_RDEC</td><td colspan="3">NOGATE_RSVD3</td><td>NOGATE_SDEC</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="3">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">NOGATE_RSVD2</td><td>NOGATE_WARB</td><td colspan="3">NOGATE_RSVD1</td><td>NOGATE_CARB</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="3">R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-9463. PKTDMA_GCFG_PM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOGATE_RDU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
30	NOGATE_RDU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
29	NOGATE_RDU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
28	NOGATE_RDU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
27	NOGATE_TDU3	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
26	NOGATE_TDU2	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
25	NOGATE_TDU1	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
24	NOGATE_TDU0	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-9463. PKTDMA_GCFG_PM0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:13	NOGATE_RSVD4	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
12	NOGATE_RDEC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
11:9	NOGATE_RSVD3	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
8	NOGATE_SDEC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
7:5	NOGATE_RSVD2	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
4	NOGATE_WARB	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
3:1	NOGATE_RSVD1	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
0	NOGATE_CARB	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

14.6.4.2.22 PKTDMA_GCFG_PM1 Register

14.6.4.2.22.1 PKTDMA_GCFG_PM1 Register (Offset = 64h) [reset = 0h]

This register enables or inhibits automatic clock gating to individual sub-blocks

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Table 14-9464. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0064h

Figure 14-4684. PKTDMA_GCFG_PM1 Name Register

31	30	29	28	27	26	25	24
NOGATE_RSVD12	NOGATE_STATS	NOGATE_PROXY	NOGATE_RSVD11	NOGATE_P2P	NOGATE_RSVD10	NOGATE_EHANDLER	NOGATE_RINGOCC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
NOGATE_RSVD9	NOGATE_TPCF	NOGATE_RSVD8			NOGATE_CFG	NOGATE_RSVD7	
R/W	R/W	R/W			R/W	R/W	
0h	0h	0h			0h	0h	
15	14	13	12	11	10	9	8
NOGATE_RFLOWFW	NOGATE_RSVD6	NOGATE_RCU	NOGATE_TCU	NOGATE_RSVD5			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
NOGATE_RSVD5							
R/W							
0h							

Table 14-9465. PKTDMA_GCFG_PM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOGATE_RSVD12	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
30	NOGATE_STATS	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
29	NOGATE_PROXY	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
28	NOGATE_RSVD11	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
27	NOGATE_P2P	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
26	NOGATE_RSVD10	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
25	NOGATE_EHANDLER	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
24	NOGATE_RINGOCC	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n

Table 14-9465. PKTDMA_GCFG_PM1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	NOGATE_RSVD9	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
22	NOGATE_TPCF	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
21:19	NOGATE_RSVD8	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
18	NOGATE_CFG	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
17:16	NOGATE_RSVD7	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
15	NOGATE_RFLOWFW	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
14	NOGATE_RSVD6	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n
13	NOGATE_RCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
12	NOGATE_TCU	R/W	0h	When set inhibits automatic gating of clock. Reset Source: rst_mod_g_rst_n
11:0	NOGATE_RSVD5	R/W	0h	Reserved PM signals. Reset Source: rst_mod_g_rst_n

14.6.4.2.23 PKTDMA_GCFG_DBGADDR Register

14.6.4.2.23.1 PKTDMA_GCFG_DBGADDR Register (Offset = 78h) [reset = 0h]

This register provides a writable address which allows debug information to be read from the Debug Data Register

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Table 14-9466. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0078h

Figure 14-4685. PKTDMA_GCFG_DBGADDR Name Register

31	30	29	28	27	26	25	24
DBG_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DBG_UNIT							
R/W							
0h							
7	6	5	4	3	2	1	0
DBG_ADDR							
R/W							
0h							

Table 14-9467. PKTDMA_GCFG_DBGADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBG_EN	R/W	0h	Debug enable Reset Source: rst_mod_g_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	DBG_UNIT	R/W	0h	Selects which unit to read debug information from Reset Source: rst_mod_g_rst_n
7:0	DBG_ADDR	R/W	0h	Selects offset within unit to access seperate debug registers Reset Source: rst_mod_g_rst_n

14.6.4.2.24 PKTDMA_GCFG_DBGDATA Register

14.6.4.2.24.1 PKTDMA_GCFG_DBGDATA Register (Offset = 7Ch) [reset = 0h]

This register provides read only debug data

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Table 14-9468. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 007Ch

Figure 14-4686. PKTDMA_GCFG_DBGDATA Name Register

31	30	29	28	27	26	25	24
DBG_DATA							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBG_DATA							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DBG_DATA							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBG_DATA							
R							
0h							

Table 14-9469. PKTDMA_GCFG_DBGDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DBG_DATA	R	0h	Provides debug information from various internal units. The value which is read back depends on which unit and register are selected in the Debug Address Register Reset Source: rst_mod_g_rst_n

14.6.4.2.25 PKTDMA_GCFG_RFLOWFWSTAT Register

14.6.4.2.25.1 PKTDMA_GCFG_RFLOWFWSTAT Register (Offset = 88h) [reset = 0h]

The Rx Flow FW Status Register 0 captures information about the thread/channel and received flow ID which failed a range check. Values in this register will remain persistent once an exception has been detected until the pend bit is written back to 0

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Table 14-9470. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485C 0088h

Figure 14-4687. PKTDMA_GCFG_RFLOWFWSTAT Name Register

31	30	29	28	27	26	25	24
PEND	RESERVED	FLOWID					
R/W	NONE	R/W					
0h	0h	0h					
23	22	21	20	19	18	17	16
FLOWID							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							CHANNEL
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
CHANNEL							
R/W							
0h							

Table 14-9471. PKTDMA_GCFG_RFLOWFWSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PEND	R/W	0h	This bit is set whenever the Flow ID firewall detects a Flow ID is out of range for an incoming packet. Once this bit is set, the remaining fields in this register will not be modified. SW is required to write this bit to 0 to allow another exception to be captured. Reset Source: rst_mod_g_rst_n
30	RESERVED	NONE	0h	Reserved
29:16	FLOWID	R/W	0h	This is the flow ID that was received on the trapped packet Reset Source: rst_mod_g_rst_n
15:9	RESERVED	NONE	0h	Reserved
8:0	CHANNEL	R/W	0h	This is the channel number on which the trapped packet was received Reset Source: rst_mod_g_rst_n

14.6.4.2.26 LCDMA_RINGACC_RING_CFG_RING_BA_LO_J Register

14.6.4.2.26.1 LCDMA_RINGACC_RING_CFG_RING_BA_LO_J Register (Offset = 40h) [reset = 0h]

The Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9472. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485E 0040h + formula

Figure 14-4688. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Name Register

31	30	29	28	27	26	25	24
ADDR_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_LO							
R/W							
0h							

Table 14-9473. LCDMA_RINGACC_RING_CFG_RING_BA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_LO	R/W	0h	Ring base address (LSBs) Reset Source: rst_mod_g_rst_n

14.6.4.2.27 LCDMA_RINGACC_RING_CFG_RING_BA_HI_J Register

14.6.4.2.27.1 LCDMA_RINGACC_RING_CFG_RING_BA_HI_J Register (Offset = 44h) [reset = 0h]

The Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to 0x8. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9474. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485E 0044h + formula

Figure 14-4689. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				ASEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ADDR_HI			
NONE				R/W			
0h				0h			

Table 14-9475. LCDMA_RINGACC_RING_CFG_RING_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	ASEL	R/W	0h	Ring base address select Reset Source: rst_mod_g_rst_n
15:4	RESERVED	NONE	0h	Reserved
3:0	ADDR_HI	R/W	0h	Ring base address (MSBs) Reset Source: rst_mod_g_rst_n

14.6.4.2.28 LCDMA_RINGACC_RING_CFG_RING_SIZE_J Register

14.6.4.2.28.1 LCDMA_RINGACC_RING_CFG_RING_SIZE_J Register (Offset = 48h) [reset = 21000000h]

The Ring Size Register contains the element count for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9476. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	485E 0048h + formula

Figure 14-4690. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Name Register

31	30	29	28	27	26	25	24
QMODE			RESERVED		RING_ELSIZE		
R/NA			NONE		R/NA		
1h			0h		1h		
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
SIZE							
R/W							
0h							

Table 14-9477. LCDMA_RINGACC_RING_CFG_RING_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	QMODE	R/NA	1h	Defines the mode for this ring or queue. 1 exposed ring mode with dual queues (forward/reverse) for SW direct access
28:27	RESERVED	NONE	0h	Reserved
26:24	RING_ELSIZE	R/NA	1h	Reset Source: rst_mod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:0	SIZE	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. Reset Source: rst_mod_g_rst_n

14.6.4.2.29 PKTDMA_RXCRT_CHAN_CTL_J Register

14.6.4.2.29.1 PKTDMA_RXCRT_CHAN_CTL_J Register (Offset = 0h) [reset = 0h]

The Rx Channel Realtime Control Register contains real-time control and status information for the Rx DMA channel. The fields in this register can safely be changed while the channel is in operation.

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Table 14-9478. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0000h + formula

Figure 14-4691. PKTDMA_RXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
RX_ENABLE	RX_TEARDOWN	RX_PAUSE	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RX_ERROR
NONE							R/W
0h							0h

Table 14-9479. PKTDMA_RXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in overflow conditions in the attached application and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate tha the channel teardown is complete. If the host is enabling a channel that is just being set up, the host must initialize all of the other channel configuration fields before setting this bit. Reset Source: rst_mod_g_rst_n
30	RX_TEARDOWN	R/W	0h	This field indicates whether or not an Rx teardown operation is complete. This field should be cleared when a channel is initialized. This field will be set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	RX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n
28:1	RESERVED	NONE	0h	Reserved

Table 14-9479. PKTDMA_RXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RX_ERROR	R/W	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared when the channel is disabled and re-enabled. Reset Source: rst_mod_g_rst_n

14.6.4.2.30 PKTDMA_RXCRT_CHAN_STATUS0_J Register

14.6.4.2.30.1 PKTDMA_RXCRT_CHAN_STATUS0_J Register (Offset = 40h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

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Table 14-9480. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0040h + formula

Figure 14-4692. PKTDMA_RXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
RRING_PEND	RXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	RX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-9481. PKTDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	RXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n

Table 14-9481. PKTDMA_RXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.4.2.31 PKTDMA_RXCRT_CHAN_STATUS1_J Register

14.6.4.2.31.1 PKTDMA_RXCRT_CHAN_STATUS1_J Register (Offset = 44h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

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Table 14-9482. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0044h + formula

Figure 14-4693. PKTDMA_RXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
RX_REQS	RESERVED					FIFO_PEND	FIFO_BUSY
R	NONE					R	R
0h	0h					0h	0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-9483. PKTDMA_RXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:26	RESERVED	NONE	0h	Reserved
25	FIFO_PEND	R	0h	The FIFO has enough data for a burst Reset Source: rst_mod_g_rst_n
24	FIFO_BUSY	R	0h	The fifo has data Reset Source: rst_mod_g_rst_n
23:8	RESERVED	NONE	0h	Reserved
7	CHANNEL_OK	R	0h	The channel is trying to schedule work Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	The channel has active work Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n
2:0	RESERVED	NONE	0h	Reserved

14.6.4.2.32 PKTDMA_RXCRT_CHAN_STDATA_J_K Register

14.6.4.2.32.1 PKTDMA_RXCRT_CHAN_STDATA_J_K Register (Offset = 80h) [reset = 0h]

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the PKTDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

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Table 14-9484. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0080h + formula

Figure 14-4694. PKTDMA_RXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/W							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/W							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/W							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/W							
0h							

Table 14-9485. PKTDMA_RXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/W	0h	See Rx state mapping table Reset Source: rst_mod_g_rst_n

14.6.4.2.33 PKTDMA_RXCRT_CHAN_PEER0_J Register

14.6.4.2.33.1 PKTDMA_RXCRT_CHAN_PEER0_J Register (Offset = 200h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

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Table 14-9486. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0200h + formula

Figure 14-4695. PKTDMA_RXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9487. PKTDMA_RXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.34 PKTDMA_RXCRT_CHAN_PEER1_J Register

14.6.4.2.34.1 PKTDMA_RXCRT_CHAN_PEER1_J Register (Offset = 204h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

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Table 14-9488. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0204h + formula

Figure 14-4696. PKTDMA_RXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9489. PKTDMA_RXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.35 PKTDMA_RXCRT_CHAN_PEER2_J Register

14.6.4.2.35.1 PKTDMA_RXCRT_CHAN_PEER2_J Register (Offset = 208h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

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Table 14-9490. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0208h + formula

Figure 14-4697. PKTDMA_RXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9491. PKTDMA_RXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.36 PKTDMA_RXCRT_CHAN_PEER3_J Register

14.6.4.2.36.1 PKTDMA_RXCRT_CHAN_PEER3_J Register (Offset = 20Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

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Table 14-9492. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 020Ch + formula

Figure 14-4698. PKTDMA_RXCRT_CHAN_PEER3_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PEER_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PEER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PEER_DATA							
R/W							
0h							

Table 14-9493. PKTDMA_RXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.37 PKTDMA_RXCRT_CHAN_PEER4_J Register

14.6.4.2.37.1 PKTDMA_RXCRT_CHAN_PEER4_J Register (Offset = 210h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

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Table 14-9494. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0210h + formula

Figure 14-4699. PKTDMA_RXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9495. PKTDMA_RXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.38 PKTDMA_RXCRT_CHAN_PEER5_J Register

14.6.4.2.38.1 PKTDMA_RXCRT_CHAN_PEER5_J Register (Offset = 214h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

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Table 14-9496. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0214h + formula

Figure 14-4700. PKTDMA_RXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9497. PKTDMA_RXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.39 PKTDMA_RXCRT_CHAN_PEER6_J Register

14.6.4.2.39.1 PKTDMA_RXCRT_CHAN_PEER6_J Register (Offset = 218h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

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Table 14-9498. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0218h + formula

Figure 14-4701. PKTDMA_RXCRT_CHAN_PEER6_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PEER_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PEER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PEER_DATA							
R/W							
0h							

Table 14-9499. PKTDMA_RXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.40 PKTDMA_RXCRT_CHAN_PEER7_J Register

14.6.4.2.40.1 PKTDMA_RXCRT_CHAN_PEER7_J Register (Offset = 21Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

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Table 14-9500. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 021Ch + formula

Figure 14-4702. PKTDMA_RXCRT_CHAN_PEER7_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9501. PKTDMA_RXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.41 PKTDMA_RXCRT_CHAN_PEER8_J Register

14.6.4.2.41.1 PKTDMA_RXCRT_CHAN_PEER8_J Register (Offset = 220h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Table 14-9502. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0220h + formula

Figure 14-4703. PKTDMA_RXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9503. PKTDMA_RXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.42 PKTDMA_RXCRT_CHAN_PEER9_J Register

14.6.4.2.42.1 PKTDMA_RXCRT_CHAN_PEER9_J Register (Offset = 224h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Table 14-9504. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0224h + formula

Figure 14-4704. PKTDMA_RXCRT_CHAN_PEER9_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9505. PKTDMA_RXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.43 PKTDMA_RXCRT_CHAN_PEER10_J Register

14.6.4.2.43.1 PKTDMA_RXCRT_CHAN_PEER10_J Register (Offset = 228h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Table 14-9506. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0228h + formula

Figure 14-4705. PKTDMA_RXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9507. PKTDMA_RXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.44 PKTDMA_RXCRT_CHAN_PEER11_J Register

14.6.4.2.44.1 PKTDMA_RXCRT_CHAN_PEER11_J Register (Offset = 22Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Table 14-9508. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 022Ch + formula

Figure 14-4706. PKTDMA_RXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9509. PKTDMA_RXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.45 PKTDMA_RXCRT_CHAN_PEER12_J Register

14.6.4.2.45.1 PKTDMA_RXCRT_CHAN_PEER12_J Register (Offset = 230h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Table 14-9510. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0230h + formula

Figure 14-4707. PKTDMA_RXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9511. PKTDMA_RXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.46 PKTDMA_RXCRT_CHAN_PEER13_J Register

14.6.4.2.46.1 PKTDMA_RXCRT_CHAN_PEER13_J Register (Offset = 234h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Table 14-9512. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0234h + formula

Figure 14-4708. PKTDMA_RXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9513. PKTDMA_RXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.47 PKTDMA_RXCRT_CHAN_PEER14_J Register

14.6.4.2.47.1 PKTDMA_RXCRT_CHAN_PEER14_J Register (Offset = 238h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Table 14-9514. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0238h + formula

Figure 14-4709. PKTDMA_RXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9515. PKTDMA_RXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.48 PKTDMA_RXCRT_CHAN_PEER15_J Register

14.6.4.2.48.1 PKTDMA_RXCRT_CHAN_PEER15_J Register (Offset = 23Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Table 14-9516. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 023Ch + formula

Figure 14-4710. PKTDMA_RXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9517. PKTDMA_RXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.49 PKTDMA_RXCRT_CHAN_PCNT_J Register

14.6.4.2.49.1 PKTDMA_RXCRT_CHAN_PCNT_J Register (Offset = 400h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9518. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0400h + formula

Figure 14-4711. PKTDMA_RXCRT_CHAN_PCNT_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9519. PKTDMA_RXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.50 PKTDMA_RXCRT_CHAN_DCNT_J Register

14.6.4.2.50.1 PKTDMA_RXCRT_CHAN_DCNT_J Register (Offset = 404h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9520. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0404h + formula

Figure 14-4712. PKTDMA_RXCRT_CHAN_DCNT_j Name Register

31	30	29	28	27	26	25	24
DCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
DCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
DCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
DCNT							
R/WTD							
0h							

Table 14-9521. PKTDMA_RXCRT_CHAN_DCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DCNT	R/WTD	0h	Current dropped packet count for the channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.51 PKTDMA_RXCRT_CHAN_BCNT_J Register

14.6.4.2.51.1 PKTDMA_RXCRT_CHAN_BCNT_J Register (Offset = 408h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9522. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0408h + formula

Figure 14-4713. PKTDMA_RXCRT_CHAN_BCNT_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BCNT</td></tr>
<tr><td colspan="8">R/WTD</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9523. PKTDMA_RXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.52 PKTDMA_RXCRT_CHAN_SBCNT_J Register

14.6.4.2.52.1 PKTDMA_RXCRT_CHAN_SBCNT_J Register (Offset = 410h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9524. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4A80 0410h + formula

Figure 14-4714. PKTDMA_RXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-9525. PKTDMA_RXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.53 PKTDMA_TXCRT_CHAN_CTL_J Register

14.6.4.2.53.1 PKTDMA_TXCRT_CHAN_CTL_J Register (Offset = 0h) [reset = 0h]

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Return to Summary Table

Table 14-9526. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0000h + formula

Figure 14-4715. PKTDMA_TXCRT_CHAN_CTL_j Name Register

31	30	29	28	27	26	25	24
TX_ENABLE	TX_TEARDOWN	TX_PAUSE	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TX_ERROR
NONE							R/W
0h							0h

Table 14-9527. PKTDMA_TXCRT_CHAN_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete. Reset Source: rst_mod_g_rst_n
30	TX_TEARDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete. Reset Source: rst_mod_g_rst_n
29	TX_PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately. Reset Source: rst_mod_g_rst_n
28:1	RESERVED	NONE	0h	Reserved

Table 14-9527. PKTDMA_TXCRT_CHAN_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TX_ERROR	R/W	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared by writing back a 0. Reset Source: rst_mod_g_rst_n

14.6.4.2.54 PKTDMA_TXCRT_CHAN_STATUS0_J Register

14.6.4.2.54.1 PKTDMA_TXCRT_CHAN_STATUS0_J Register (Offset = 40h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Table 14-9528. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0040h + formula

Figure 14-4716. PKTDMA_TXCRT_CHAN_STATUS0_j Name Register

31	30	29	28	27	26	25	24
TRING_PEND	TXQ_PEND	PKTID_AVAIL	PKTID_BUSY	RESERVED		BUSY	TRANSBUSY
R	R	R	R	NONE		R	R
0h	0h	0h	0h	0h		0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN_PACKET	OK	WAVAIL	RESERVED		TDOWN_MSG_PEND	TX_REQS	ERR_EVENT_REQS
R	R	R	NONE		R	R	R
0h	0h	0h	0h		0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-9529. PKTDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRING_PEND	R	0h	The channel ring has a descriptor Reset Source: rst_mod_g_rst_n
30	TXQ_PEND	R	0h	The channel fifo is available Reset Source: rst_mod_g_rst_n
29	PKTID_AVAIL	R	0h	The channel has an available packet id Reset Source: rst_mod_g_rst_n
28	PKTID_BUSY	R	0h	There is an outstanding pktid for the channel Reset Source: rst_mod_g_rst_n
27:26	RESERVED	NONE	0h	Reserved
25	BUSY	R	0h	The channel is busy Reset Source: rst_mod_g_rst_n
24	TRANSBUSY	R	0h	The channel has an outstanding transaction Reset Source: rst_mod_g_rst_n
23	IN_PACKET	R	0h	The channel is currently in a packet Reset Source: rst_mod_g_rst_n
22	OK	R	0h	The channel is ready to be scheduled Reset Source: rst_mod_g_rst_n
21	WAVAIL	R	0h	The fifo for the channel has space to place a burst size entry Reset Source: rst_mod_g_rst_n

Table 14-9529. PKTDMA_TXCRT_CHAN_STATUS0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:19	RESERVED	NONE	0h	Reserved
18	TDOWN_MSG_PEND	R	0h	A teardown message is pending Reset Source: rst_mod_g_rst_n
17	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
16	ERR_EVENT_REQS	R	0h	The channel is trying to schedule an error event Reset Source: rst_mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.6.4.2.55 PKTDMA_TXCRT_CHAN_STATUS1_J Register

14.6.4.2.55.1 PKTDMA_TXCRT_CHAN_STATUS1_J Register (Offset = 44h) [reset = 0h]

The Status Register provides a read only view of channel status bits.

Return to Summary Table

Table 14-9530. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0044h + formula

Figure 14-4717. PKTDMA_TXCRT_CHAN_STATUS1_j Name Register

31	30	29	28	27	26	25	24
TX_REQS	RESERVED				SOP_WAVAIL	MOP_WAVAIL	WAVAIL
R	NONE				R	R	R
0h	0h				0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TDNULL
NONE							R
0h							0h
7	6	5	4	3	2	1	0
CHANNEL_OK	CHANNEL_BUSY	RESERVED		IN_PACKET_ARRAY	RESERVED		
R	R	NONE		R	NONE		
0h	0h	0h		0h	0h		

Table 14-9531. PKTDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_REQS	R	0h	The channel is sending a schedule request Reset Source: rst_mod_g_rst_n
30:27	RESERVED	NONE	0h	Reserved
26	SOP_WAVAIL	R	0h	The FIFO has space for the start of a packet Reset Source: rst_mod_g_rst_n
25	MOP_WAVAIL	R	0h	The FIFO has space for the middle of a packet Reset Source: rst_mod_g_rst_n
24	WAVAIL	R	0h	The fifo has space for a burst size Reset Source: rst_mod_g_rst_n
23:9	RESERVED	NONE	0h	Reserved
8	TDNULL	R	0h	The channel has met the conditions to attempt to teardown Reset Source: rst_mod_g_rst_n
7	CHANNEL_OK	R	0h	The channel is trying to schedule work Reset Source: rst_mod_g_rst_n
6	CHANNEL_BUSY	R	0h	The channel has active work Reset Source: rst_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	IN_PACKET_ARRAY	R	0h	The channel is in a packet Reset Source: rst_mod_g_rst_n

Table 14-9531. PKTDMA_TXCRT_CHAN_STATUS1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	NONE	0h	Reserved

14.6.4.2.56 PKTDMA_TXCRT_CHAN_STDATA_J_K Register

14.6.4.2.56.1 PKTDMA_TXCRT_CHAN_STDATA_J_K Register (Offset = 80h) [reset = 0h]

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the PKTDMA is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Return to Summary Table

Table 14-9532. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0080h + formula

Figure 14-4718. PKTDMA_TXCRT_CHAN_STDATA_j_k Name Register

31	30	29	28	27	26	25	24
STATE_INFO							
R/NA							
0h							
23	22	21	20	19	18	17	16
STATE_INFO							
R/NA							
0h							
15	14	13	12	11	10	9	8
STATE_INFO							
R/NA							
0h							
7	6	5	4	3	2	1	0
STATE_INFO							
R/NA							
0h							

Table 14-9533. PKTDMA_TXCRT_CHAN_STDATA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATE_INFO	R/NA	0h	See Tx state mapping table Reset Source: rst_mod_g_rst_n

14.6.4.2.57 PKTDMA_TXCRT_CHAN_PEER0_J Register

14.6.4.2.57.1 PKTDMA_TXCRT_CHAN_PEER0_J Register (Offset = 200h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x400.

Return to Summary Table

Table 14-9534. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0200h + formula

Figure 14-4719. PKTDMA_TXCRT_CHAN_PEER0_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9535. PKTDMA_TXCRT_CHAN_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.58 PKTDMA_TXCRT_CHAN_PEER1_J Register

14.6.4.2.58.1 PKTDMA_TXCRT_CHAN_PEER1_J Register (Offset = 204h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x401.

Return to Summary Table

Table 14-9536. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0204h + formula

Figure 14-4720. PKTDMA_TXCRT_CHAN_PEER1_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9537. PKTDMA_TXCRT_CHAN_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.59 PKTDMA_TXCRT_CHAN_PEER2_J Register

14.6.4.2.59.1 PKTDMA_TXCRT_CHAN_PEER2_J Register (Offset = 208h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x402.

Return to Summary Table

Table 14-9538. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0208h + formula

Figure 14-4721. PKTDMA_TXCRT_CHAN_PEER2_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9539. PKTDMA_TXCRT_CHAN_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.60 PKTDMA_TXCRT_CHAN_PEER3_J Register

14.6.4.2.60.1 PKTDMA_TXCRT_CHAN_PEER3_J Register (Offset = 20Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x403.

Return to Summary Table

Table 14-9540. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 020Ch + formula

Figure 14-4722. PKTDMA_TXCRT_CHAN_PEER3_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9541. PKTDMA_TXCRT_CHAN_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.61 PKTDMA_TXCRT_CHAN_PEER4_J Register

14.6.4.2.61.1 PKTDMA_TXCRT_CHAN_PEER4_J Register (Offset = 210h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x404.

Return to Summary Table

Table 14-9542. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0210h + formula

Figure 14-4723. PKTDMA_TXCRT_CHAN_PEER4_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9543. PKTDMA_TXCRT_CHAN_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.62 PKTDMA_TXCRT_CHAN_PEER5_J Register

14.6.4.2.62.1 PKTDMA_TXCRT_CHAN_PEER5_J Register (Offset = 214h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x405.

Return to Summary Table

Table 14-9544. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0214h + formula

Figure 14-4724. PKTDMA_TXCRT_CHAN_PEER5_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9545. PKTDMA_TXCRT_CHAN_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.63 PKTDMA_TXCRT_CHAN_PEER6_J Register

14.6.4.2.63.1 PKTDMA_TXCRT_CHAN_PEER6_J Register (Offset = 218h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x406.

Return to Summary Table

Table 14-9546. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0218h + formula

Figure 14-4725. PKTDMA_TXCRT_CHAN_PEER6_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PEER_DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9547. PKTDMA_TXCRT_CHAN_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.64 PKTDMA_TXCRT_CHAN_PEER7_J Register

14.6.4.2.64.1 PKTDMA_TXCRT_CHAN_PEER7_J Register (Offset = 21Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x407.

Return to Summary Table

Table 14-9548. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 021Ch + formula

Figure 14-4726. PKTDMA_TXCRT_CHAN_PEER7_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9549. PKTDMA_TXCRT_CHAN_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.65 PKTDMA_TXCRT_CHAN_PEER8_J Register

14.6.4.2.65.1 PKTDMA_TXCRT_CHAN_PEER8_J Register (Offset = 220h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x408.

Return to Summary Table

Table 14-9550. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0220h + formula

Figure 14-4727. PKTDMA_TXCRT_CHAN_PEER8_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9551. PKTDMA_TXCRT_CHAN_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.66 PKTDMA_TXCRT_CHAN_PEER9_J Register

14.6.4.2.66.1 PKTDMA_TXCRT_CHAN_PEER9_J Register (Offset = 224h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x409.

Return to Summary Table

Table 14-9552. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0224h + formula

Figure 14-4728. PKTDMA_TXCRT_CHAN_PEER9_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9553. PKTDMA_TXCRT_CHAN_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.67 PKTDMA_TXCRT_CHAN_PEER10_J Register

14.6.4.2.67.1 PKTDMA_TXCRT_CHAN_PEER10_J Register (Offset = 228h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40A.

Return to Summary Table

Table 14-9554. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0228h + formula

Figure 14-4729. PKTDMA_TXCRT_CHAN_PEER10_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9555. PKTDMA_TXCRT_CHAN_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.68 PKTDMA_TXCRT_CHAN_PEER11_J Register

14.6.4.2.68.1 PKTDMA_TXCRT_CHAN_PEER11_J Register (Offset = 22Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40B.

Return to Summary Table

Table 14-9556. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 022Ch + formula

Figure 14-4730. PKTDMA_TXCRT_CHAN_PEER11_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9557. PKTDMA_TXCRT_CHAN_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.69 PKTDMA_TXCRT_CHAN_PEER12_J Register

14.6.4.2.69.1 PKTDMA_TXCRT_CHAN_PEER12_J Register (Offset = 230h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40C.

Return to Summary Table

Table 14-9558. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0230h + formula

Figure 14-4731. PKTDMA_TXCRT_CHAN_PEER12_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PEER_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PEER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PEER_DATA							
R/W							
0h							

Table 14-9559. PKTDMA_TXCRT_CHAN_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.70 PKTDMA_TXCRT_CHAN_PEER13_J Register

14.6.4.2.70.1 PKTDMA_TXCRT_CHAN_PEER13_J Register (Offset = 234h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40D.

Return to Summary Table

Table 14-9560. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0234h + formula

Figure 14-4732. PKTDMA_TXCRT_CHAN_PEER13_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9561. PKTDMA_TXCRT_CHAN_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.71 PKTDMA_TXCRT_CHAN_PEER14_J Register

14.6.4.2.71.1 PKTDMA_TXCRT_CHAN_PEER14_J Register (Offset = 238h) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40E.

Return to Summary Table

Table 14-9562. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0238h + formula

Figure 14-4733. PKTDMA_TXCRT_CHAN_PEER14_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9563. PKTDMA_TXCRT_CHAN_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.72 PKTDMA_TXCRT_CHAN_PEER15_J Register

14.6.4.2.72.1 PKTDMA_TXCRT_CHAN_PEER15_J Register (Offset = 23Ch) [reset = 0h]

This register provides access to the remote peer's realtime register at 0x40F.

Return to Summary Table

Table 14-9564. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 023Ch + formula

Figure 14-4734. PKTDMA_TXCRT_CHAN_PEER15_j Name Register

31	30	29	28	27	26	25	24
PEER_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PEER_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PEER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PEER_DATA							
R/W							
0h							

Table 14-9565. PKTDMA_TXCRT_CHAN_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer). Reset Source: rst_mod_g_rst_n

14.6.4.2.73 PKTDMA_TXCRT_CHAN_PCNT_J Register

14.6.4.2.73.1 PKTDMA_TXCRT_CHAN_PCNT_J Register (Offset = 400h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9566. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0400h + formula

Figure 14-4735. PKTDMA_TXCRT_CHAN_PCNT_j Name Register

31	30	29	28	27	26	25	24
PCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
PCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
PCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
PCNT							
R/WTD							
0h							

Table 14-9567. PKTDMA_TXCRT_CHAN_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PCNT	R/WTD	0h	Current completed packet count for the channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.74 PKTDMA_TXCRT_CHAN_BCNT_J Register

14.6.4.2.74.1 PKTDMA_TXCRT_CHAN_BCNT_J Register (Offset = 408h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9568. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0408h + formula

Figure 14-4736. PKTDMA_TXCRT_CHAN_BCNT_j Name Register

31	30	29	28	27	26	25	24
BCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
BCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
BCNT							
R/WTD							
0h							

Table 14-9569. PKTDMA_TXCRT_CHAN_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCNT	R/WTD	0h	Current completed payload byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.75 PKTDMA_TXCRT_CHAN_SBCNT_J Register

14.6.4.2.75.1 PKTDMA_TXCRT_CHAN_SBCNT_J Register (Offset = 410h) [reset = 0h]

The statistics registers are supplied to give software applications operational progress status for the channel.

Return to Summary Table

Table 14-9570. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4AA0 0410h + formula

Figure 14-4737. PKTDMA_TXCRT_CHAN_SBCNT_j Name Register

31	30	29	28	27	26	25	24
SBCNT							
R/WTD							
0h							
23	22	21	20	19	18	17	16
SBCNT							
R/WTD							
0h							
15	14	13	12	11	10	9	8
SBCNT							
R/WTD							
0h							
7	6	5	4	3	2	1	0
SBCNT							
R/WTD							
0h							

Table 14-9571. PKTDMA_TXCRT_CHAN_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SBCNT	R/WTD	0h	Current started byte count for the channel. Reset Source: rst_mod_g_rst_n

14.6.4.2.76 LCDMA_RINGACC_RINGRT_RING_FDB_J Register

14.6.4.2.76.1 LCDMA_RINGACC_RINGRT_RING_FDB_J Register (Offset = 10h) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

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Table 14-9572. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4B80 0010h + formula

Figure 14-4738. LCDMA_RINGACC_RINGRT_RING_FDB_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-9573. LCDMA_RINGACC_RINGRT_RING_FDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.6.4.2.77 LCDMA_RINGACC_RINGRT_RING_FOCC_J Register

14.6.4.2.77.1 LCDMA_RINGACC_RINGRT_RING_FOCC_J Register (Offset = 18h) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

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Table 14-9574. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4B80 0018h + formula

Figure 14-4739. LCDMA_RINGACC_RINGRT_RING_FOCC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OCC
NONE							R/NA
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OCC							
R/NA							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OCC							
R/NA							
0h							

Table 14-9575. LCDMA_RINGACC_RINGRT_RING_FOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.6.4.2.78 LCDMA_RINGACC_RINGRT_RING_RDB_J Register

14.6.4.2.78.1 LCDMA_RINGACC_RINGRT_RING_RDB_J Register (Offset = 1010h) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

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Table 14-9576. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4B80 1010h + formula

Figure 14-4740. LCDMA_RINGACC_RINGRT_RING_RDB_j Name Register

31	30	29	28	27	26	25	24
TDOWN_ACK	RESERVED						
NA/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-9577. LCDMA_RINGACC_RINGRT_RING_RDB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_ACK	NA/W	0h	This bit is set to 1 to ackowledge (and clear) the tdown_complete bit in the corresponding Ring N Occupancy Register. this bit is only valid on the reverse rings (rings consumed by the Host SW) Reset Source: rst_mod_g_rst_n
30:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: rst_mod_g_rst_n

14.6.4.2.79 LCDMA_RINGACC_RINGRT_RING_ROCC_J Register

14.6.4.2.79.1 LCDMA_RINGACC_RINGRT_RING_ROCC_J Register (Offset = 1018h) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

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Table 14-9578. Instance Table

Instance Name	Physical Address
DMASS0_PKTDMA_0	4B80 1018h + formula

Figure 14-4741. LCDMA_RINGACC_RINGRT_RING_ROCC_j Name Register

31	30	29	28	27	26	25	24
TDOWN_COMPLETE	RESERVED						
R/NA	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OCC
NONE							R/NA
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OCC							
R/NA							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OCC							
R/NA							
0h							

Table 14-9579. LCDMA_RINGACC_RINGRT_RING_ROCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDOWN_COMPLETE	R/NA	0h	This bit when set indicates that a teardown is complete on the channel. This bit is cleared anytime the tdown_ack bit is written as a 1 in the corresponding Ring N Doorbell Register. This bit is only valid on the reverse rings (rings consumed by the Host SW). Reset Source: rst_mod_g_rst_n
30:17	RESERVED	NONE	0h	Reserved
16:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: rst_mod_g_rst_n

14.6.5 DMASS_PSILCFG_0

DMASS_PSILCFG_0

14.6.5.1 DMASS_PSILCFG_0 Summaries

DMASS_PSILCFG_0 Summaries

Table 14-9580. PSILCFG Registers, Base Address=4813 0000h, Length=512

Offset	Length	Register Name	DMASS0_PSILCFG_0 Physical Address
0h	32	PSILCFG_REVISION	4813 0000h
10h	32	PSILCFG_PSIL_TO	4813 0010h
100h	32	PSILCFG_CMDA	4813 0100h
104h	32	PSILCFG_CMDB	4813 0104h
108h	32	PSILCFG_WDATA	4813 0108h
140h	32	PSILCFG_RDATA	4813 0140h

14.6.5.2 DMASS_PSILCFG_0 Registers

DMASS_PSILCFG_0 Registers

14.6.5.2.1 PSILCFG_REVISION Register

14.6.5.2.1.1 PSILCFG_REVISION Register (Offset = 0h) [reset = 66C00100h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-9581. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	4813 0000h

Figure 14-4742. PSILCFG_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
66C0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODID							
R							
66C0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-9582. PSILCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	66C0h	Module ID field Reset Source: srst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: srst_n

14.6.5.2.2 PSILCFG_PSIL_TO Register

14.6.5.2.2.1 PSILCFG_PSIL_TO Register (Offset = 10h) [reset = 400h]

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrances on PSI-L configuration transactions issued by the built in PSI-L proxy.

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Table 14-9583. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	4813 0010h

Figure 14-4743. PSILCFG_PSIL_TO Name Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W							
400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W							
400h							

Table 14-9584. PSILCFG_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access. Once set, this bit is persistent until manually cleared Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a conifiguration read or write transaction and asserting the tout bit Reset Source: srst_n

14.6.5.2.3 PSILCFG_CMDA Register

14.6.5.2.3.1 PSILCFG_CMDA Register (Offset = 100h) [reset = 0h]

The Command Register A contains the busy indicator, direction, and thread number for the configuration transaction.

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Table 14-9585. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	4813 0100h

Figure 14-4744. PSILCFG_CMDA Name Register

31	30	29	28	27	26	25	24
PROXY_BUSY	PROXY_DIR	PROXY_TOUT	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PROXY_THREAD_ID							
R/W							
0h							
7	6	5	4	3	2	1	0
PROXY_THREAD_ID							
R/W							
0h							

Table 14-9586. PSILCFG_CMDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PROXY_BUSY	R/W	0h	Indication that a configuration read or write is in progress 0 `No transaction is in progress` 1 `Transaction is in progress`
30	PROXY_DIR	R/W	0h	Direction of configuration transaction 0 `Write transaction` 1 `Read transaction`
29	PROXY_TOUT	R/W	0h	Indication that a timeout occurred. This bit should be written to 0 on each new transaction. 0 `Transaction completed normally` 1 `Timeout Occurred`
28:16	RESERVED	NONE	0h	Reserved
15:0	PROXY_THREAD_ID	R/W	0h	Thread ID to which configuration read or write is being sent Reset Source: srst_n

14.6.5.2.4 PSILCFG_CMDB Register

14.6.5.2.4.1 PSILCFG_CMDB Register (Offset = 104h) [reset = 0h]

The Command Register B contains the byte enables and word address for the configuration transaction.

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Table 14-9587. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	4813 0104h

Figure 14-4745. PSILCFG_CMDB Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">PROXY_BYTEN</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PROXY_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PROXY_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9588. PSILCFG_CMDB Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PROXY_BYTEN	R/W	0h	Byte enables to use for configuration read or write Reset Source: srst_n
27:16	RESERVED	NONE	0h	Reserved

15:0	PROXY_ADDRESS	R/W	0h	Word (32-bit) address within thread configuration space for transaction
				`0      Peer thread ID register. Implemented for src threads only.`
				`1      Peer credit register. Implemented for src threads only.`
				`2      Enable register`
				`64     Capabilities register`
				`1024   Static TR register`

14.6.5.2.5 PSILCFG_WDATA Register

14.6.5.2.5.1 PSILCFG_WDATA Register (Offset = 108h) [reset = 0h]

The Write Data Register contains the data which is to be written during the configuration transaction.

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Table 14-9589. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	4813 0108h

Figure 14-4746. PSILCFG_WDATA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PROXY_WDATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PROXY_WDATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PROXY_WDATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PROXY_WDATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9590. PSILCFG_WDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PROXY_WDATA	R/W	0h	Configuration data word to be written Reset Source: srst_n

14.6.5.2.6 PSILCFG_RDATA Register

14.6.5.2.6.1 PSILCFG_RDATA Register (Offset = 140h) [reset = 0h]

The Read Data Register contains the data which which was read back during the configuration transaction.

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Table 14-9591. Instance Table

Instance Name	Physical Address
DMASS0_PSILCFG_0	4813 0140h

Figure 14-4747. PSILCFG_RDATA Name Register

31	30	29	28	27	26	25	24
PROXY_RDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
PROXY_RDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
PROXY_RDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
PROXY_RDATA							
R/W							
0h							

Table 14-9592. PSILCFG_RDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PROXY_RDATA	R/W	0h	Configuration data word that was read Reset Source: srst_n

14.6.6 DMASS_PSILSS_0

DMASS_PSILSS_0

14.6.6.1 DMASS_PSILSS_0 Summaries

DMASS_PSILSS_0 Summaries

Table 14-9593. PSILSS Registers, Base Address=4814 0000h, Length=4096

Offset	Length	Register Name	DMASS0_PSILSS_0 Physical Address
0h	32	PSILSS_PID	4814 0000h
4h	32	PSILSS_CONFIG	4814 0004h
10h	32	PSILSS_EVENT	4814 0010h
20h	32	PSILSS_LINK	4814 0020h
40h	32	PSILSS_DOWN	4814 0040h

14.6.6.2 DMASS_PSILSS_0 Registers

DMASS_PSILSS_0 Registers

14.6.6.2.1 PSILSS_PID Register

14.6.6.2.1.1 PSILSS_PID Register (Offset = 0h) [reset = 66C4D100h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-9594. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	4814 0000h

Figure 14-4748. PSILSS_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6C4h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6C4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">1Ah</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-9595. PSILSS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: rst_mod_g_rst_n
27:16	FUNC	R	6C4h	Module ID Reset Source: rst_mod_g_rst_n
15:11	RTL	R	1Ah	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: rst_mod_g_rst_n

14.6.6.2.2 PSILSS_CONFIG Register

14.6.6.2.2.1 PSILSS_CONFIG Register (Offset = 4h) [reset = 1Dh]

The Config Register shows configured params.

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Table 14-9596. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	4814 0004h

Figure 14-4749. PSILSS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ENDPOINTS							
R							
1Dh							
7	6	5	4	3	2	1	0
ENDPOINTS							
R							
1Dh							

Table 14-9597. PSILSS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ENDPOINTS	R	1Dh	Number of endpoints supported. Reset Source: rst_mod_g_rst_n

14.6.6.2.3 PSILSS_EVENT Register

14.6.6.2.3.1 PSILSS_EVENT Register (Offset = 10h) [reset = FFFFh]

The Event Register defines the event to produce for a link down event.

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Table 14-9598. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	4814 0010h

Figure 14-4750. PSILSS_EVENT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-9599. PSILSS_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	The event to produce. Reset Source: rst_mod_g_rst_n

14.6.6.2.4 PSILSS_LINK Register

14.6.6.2.4.1 PSILSS_LINK Register (Offset = 20h) [reset = 0h]

The Link Register shows the current status of the endpoint links.

Return to Summary Table

Table 14-9600. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	4814 0020h

Figure 14-4751. PSILSS_LINK Name Register

31	30	29	28	27	26	25	24
STATUS							
R							
0h							
23	22	21	20	19	18	17	16
STATUS							
R							
0h							
15	14	13	12	11	10	9	8
STATUS							
R							
0h							
7	6	5	4	3	2	1	0
STATUS							
R							
0h							

Table 14-9601. PSILSS_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATUS	R	0h	The status of the endpoint links. Indices: 0: .saul0_psil 1: .pdma_main0_psil 2: .pdma_main1_psil 3: .pdma_main2_psil 4: .pdma_mcasp_psil 5: .pdma_mcasp1_psil 6: .pdma_adc_psil 7: .pdma_asrc0_psil 8: .pdma_asrc1_psil 9: .cpsw_psil 10: .dru0_i_etl 11: .dru0_o_etl 12: .dru1_i_etl 13: .dru1_o_etl 14: pktdma.strm 15: pktdma.cfgstrm 16: bcdma.cfgstrm 17: bcdma.strm 18: bcdma.trig 19: intaggr.evt 20: intaggr.cevt 21: intaggr.cevt_out 22: intaggr.mevt_in 23: intaggr.mevt_out 24: intaggr.evto 25: intaggr.levt_out 26: psilcfg.cfgstrm 27: ipcss.sec_proxy_evt 28: ipcss.ringacc_evt Reset Source: rst_mod_g_rst_n

14.6.6.2.5 PSILSS_DOWN Register

14.6.6.2.5.1 PSILSS_DOWN Register (Offset = 40h) [reset = 0h]

The Link Down Register shows which links are down for the endpoints.

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Table 14-9602. Instance Table

Instance Name	Physical Address
DMASS0_PSILSS_0	4814 0040h

Figure 14-4752. PSILSS_DOWN Name Register

31	30	29	28	27	26	25	24
STATUS							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STATUS							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STATUS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STATUS							
R/W1TC							
0h							

Table 14-9603. PSILSS_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STATUS	R/W1TC	0h	The down status of the endpoint links. Indices: 0: .saul0_psil 1: .pdma_main0_psil 2: .pdma_main1_psil 3: .pdma_main2_psil 4: .pdma_mcasp_psil 5: .pdma_mcasp1_psil 6: .pdma_adc_psil 7: .pdma_asrc0_psil 8: .pdma_asrc1_psil 9: .cpsw_psil 10: .dru0_i_etl 11: .dru0_o_etl 12: .dru1_i_etl 13: .dru1_o_etl 14: pktdma.strm 15: pktdma.cfgstrm 16: bcdma.cfgstrm 17: bcdma.strm 18: bcdma.trig 19: intaggr.evt 20: intaggr.cevt 21: intaggr.cevt_out 22: intaggr.mevt_in 23: intaggr.mevt_out 24: intaggr.evto 25: intaggr.levt_out 26: psilcfg.cfgstrm 27: ipcss.sec_proxy_evt 28: ipcss.ringacc_evt Reset Source: rst_mod_g_rst_n

14.6.7 DMASS_RINGACC_0

DMASS_RINGACC_0

14.6.7.1 DMASS_RINGACC_0 Summaries

DMASS_RINGACC_0 Summaries

Table 14-9604. RINGACC_GCFG Registers, Base Address=4824 0000h, Length=1024

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
0h	32	RINGACC_GCFG_REVISION	4824 0000h
10h	32	RINGACC_GCFG_TRACE_CTL	4824 0010h
20h	32	RINGACC_GCFG_OVRFLOW	4824 0020h
40h	32	RINGACC_GCFG_ERROR_EVT	4824 0040h
44h	32	RINGACC_GCFG_ERROR_LOG	4824 0044h

Table 14-9605. RINGACC_RT Registers, Base Address=4900 0000h, Length=4194304

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
10h	32	RINGACC_RT_RINGRT_DB_J	4900 0010h + formula
18h	32	RINGACC_RT_RINGRT_OCC_J	4900 0018h + formula
1Ch	32	RINGACC_RT_RINGRT_INDX_J	4900 001Ch + formula
20h	32	RINGACC_RT_RINGRT_HWOCC_J	4900 0020h + formula
24h	32	RINGACC_RT_RINGRT_HWINDX_J	4900 0024h + formula

Table 14-9606. RINGACC_CFG Registers, Base Address=4980 0000h, Length=262144

Offset	Length	Register Name	DMASS0_RINGACC_0 Physical Address
40h	32	RINGACC_CFG_RING_BA_LO_J	4980 0040h + formula
44h	32	RINGACC_CFG_RING_BA_HI_J	4980 0044h + formula
48h	32	RINGACC_CFG_RING_SIZE_J	4980 0048h + formula
4Ch	32	RINGACC_CFG_RING_EVENT_J	4980 004Ch + formula
50h	32	RINGACC_CFG_RING_ORDERID_J	4980 0050h + formula

14.6.7.2 DMASS_RINGACC_0 Registers

DMASS_RINGACC_0 Registers

14.6.7.2.1 RINGACC_GCFG_REVISION Register

14.6.7.2.1.1 RINGACC_GCFG_REVISION Register (Offset = 0h) [reset = 663C0101h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-9607. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4824 0000h

Figure 14-4753. RINGACC_GCFG_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
663Ch							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODID							
R							
663Ch							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-9608. RINGACC_GCFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	663Ch	Module ID field Reset Source: srst_n
15:11	REVRTL	R	0h	RTL revision. Will vary depending on release. Reset Source: srst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: srst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: srst_n

14.6.7.2.2 RINGACC_GCFG_TRACE_CTL Register

14.6.7.2.2.1 RINGACC_GCFG_TRACE_CTL Register (Offset = 10h) [reset = 0h]

Trace Control Register

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Table 14-9609. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4824 0010h

Figure 14-4754. RINGACC_GCFG_TRACE_CTL Name Register

31	30	29	28	27	26	25	24
EN	ALL_QUEUES	MSG	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
QUEUE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUEUE							
R/W							
0h							

Table 14-9610. RINGACC_GCFG_TRACE_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Trace enable 0 = disable 1 = enable. Reset Source: srst_n
30	ALL_QUEUES	R/W	0h	Trace everything 0 = only the selected queue 1 = every queue. Reset Source: srst_n
29	MSG	R/W	0h	Trace message data 0 = include only the operation 1 = include message data. Reset Source: srst_n
28:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R/W	0h	Queue number when tracing a single queue. Reset Source: srst_n

14.6.7.2.3 RINGACC_GCFG_OVRFLOW Register

14.6.7.2.3.1 RINGACC_GCFG_OVRFLOW Register (Offset = 20h) [reset = 0h]

Overflow Queue Register

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Table 14-9611. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4824 0020h

Figure 14-4755. RINGACC_GCFG_OVRFLOW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE							
R/W							
0h							

Table 14-9612. RINGACC_GCFG_OVRFLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R/W	0h	Queue to send overflow messages. A value of 0xffff will disable the overflow function. Reset Source: srst_n

14.6.7.2.4 RINGACC_GCFG_ERROR_EVT Register

14.6.7.2.4.1 RINGACC_GCFG_ERROR_EVT Register (Offset = 40h) [reset = FFFFh]

The Error Event Register is an Output Event Steering 'OES' register that specifies the event number used to denote detection of a ring memory transaction bus error.

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Table 14-9613. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4824 0040h

Figure 14-4756. RINGACC_GCFG_ERROR_EVT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EVT							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
EVT							
R/W							
FFFFh							

Table 14-9614. RINGACC_GCFG_ERROR_EVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	Event to send when detecting a bus error. Reset Source: srst_n

14.6.7.2.5 RINGACC_GCFG_ERROR_LOG Register

14.6.7.2.5.1 RINGACC_GCFG_ERROR_LOG Register (Offset = 44h) [reset = 0h]

Error Log Register. A read of this register will clear the pending error log event and allow a new error to be captured. It does not clear the contents of this register which are only valid while the error event is pending.

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Table 14-9615. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4824 0044h

Figure 14-4757. RINGACC_GCFG_ERROR_LOG Name Register

31	30	29	28	27	26	25	24
PUSH	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE							
R							
0h							

Table 14-9616. RINGACC_GCFG_ERROR_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PUSH	R	0h	Bus error was caused by a push. 0 = pop. 1 = push. Reset Source: srst_n
30:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE	R	0h	Queue that received the bus error. Reset Source: srst_n

14.6.7.2.6 RINGACC_RT_RINGRT_DB_J Register

14.6.7.2.6.1 RINGACC_RT_RINGRT_DB_J Register (Offset = 10h) [reset = 0h]

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

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Table 14-9617. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4900 0010h + formula

Figure 14-4758. RINGACC_RT_RINGRT_DB_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ENTRY_CNT							
NA/W							
0h							

Table 14-9618. RINGACC_RT_RINGRT_DB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ENTRY_CNT	NA/W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the ENTRY_CNT). Reset Source: srst_n

14.6.7.2.7 RINGACC_RT_RINGRT_OCC_J Register

14.6.7.2.7.1 RINGACC_RT_RINGRT_OCC_J Register (Offset = 18h) [reset = 0h]

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Return to Summary Table

Table 14-9619. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4900 0018h + formula

Figure 14-4759. RINGACC_RT_RINGRT_OCC_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">OCC</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/NA</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OCC</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OCC</td></tr>
<tr><td colspan="8">R/NA</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9620. RINGACC_RT_RINGRT_OCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: srst_n

14.6.7.2.8 RINGACC_RT_RINGRT_INDX_J Register

14.6.7.2.8.1 RINGACC_RT_RINGRT_INDX_J Register (Offset = 1Ch) [reset = 0h]

The Ring N Current Index Register can be read by software for debug purposes to determine the current SW read index for the Ring for the channel.

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Table 14-9621. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4900 001Ch + formula

Figure 14-4760. RINGACC_RT_RINGRT_INDX_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INDX			
NONE				R/NA			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INDX							
R/NA							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INDX							
R/NA							
0h							

Table 14-9622. RINGACC_RT_RINGRT_INDX_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INDX	R/NA	0h	Current SW owned read index for the ring. This value is initialized to 0 when the ring is set up and will be incremented by SW each time SW processes a ring entry. When the index is incremented to a value equal to the size field in the Ring Size Register for the ring the index will be reset back to 0. Reset Source: srst_n

14.6.7.2.9 RINGACC_RT_RINGRT_HWOCC_J Register

14.6.7.2.9.1 RINGACC_RT_RINGRT_HWOCC_J Register (Offset = 20h) [reset = 0h]

The Ring N Hardware Occupancy Register contains the early increment/decrement version of the the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

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Table 14-9623. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4900 0020h + formula

Figure 14-4761. RINGACC_RT_RINGRT_HWOCC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			OCC				
NONE			R/NA				
0h			0h				
15	14	13	12	11	10	9	8
OCC							
R/NA							
0h							
7	6	5	4	3	2	1	0
OCC							
R/NA							
0h							

Table 14-9624. RINGACC_RT_RINGRT_HWOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:0	OCC	R/NA	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed. Reset Source: srst_n

14.6.7.2.10 RINGACC_RT_RINGRT_HWINDX_J Register

14.6.7.2.10.1 RINGACC_RT_RINGRT_HWINDX_J Register (Offset = 24h) [reset = 0h]

The Ring N Current Index Register can be read by software for debug purposes to determine the current HW read index for the Ring for the channel.

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Table 14-9625. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4900 0024h + formula

Figure 14-4762. RINGACC_RT_RINGRT_HWINDX_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INDX			
NONE				R/NA			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INDX							
R/NA							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INDX							
R/NA							
0h							

Table 14-9626. RINGACC_RT_RINGRT_HWINDX_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INDX	R/NA	0h	Current HW owned read index for the ring. This value is initialized to 0 when the ring is set up and will be incremented by HW each time HW processes a ring entry. When the index is incremented to a value equal to the size field in the Ring Size Register for the ring the index will be reset back to 0. Reset Source: srst_n

14.6.7.2.11 RINGACC_CFG_RING_BA_LO_J Register

14.6.7.2.11.1 RINGACC_CFG_RING_BA_LO_J Register (Offset = 40h) [reset = 0h]

The Tx Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to the element size of the ring, or to double the element size of the ring if the qmode is CREDENTIALS or QM modes. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9627. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4980 0040h + formula

Figure 14-4763. RINGACC_CFG_RING_BA_LO_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9628. RINGACC_CFG_RING_BA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_LO	R/W	0h	Tx Ring base address (LSBs) Reset Source: srst_n

14.6.7.2.12 RINGACC_CFG_RING_BA_HI_J Register

14.6.7.2.12.1 RINGACC_CFG_RING_BA_HI_J Register (Offset = 44h) [reset = 0h]

The Tx Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to the element size of the ring, or to double the element size of the ring if the qmode is CREDENTIALS or QM modes. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9629. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4980 0044h + formula

Figure 14-4764. RINGACC_CFG_RING_BA_HI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDR_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR_HI							
R/W							
0h							

Table 14-9630. RINGACC_CFG_RING_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_HI	R/W	0h	Tx Ring base address (MSBs) Reset Source: srst_n

14.6.7.2.13 RINGACC_CFG_RING_SIZE_J Register

14.6.7.2.13.1 RINGACC_CFG_RING_SIZE_J Register (Offset = 48h) [reset = 0h]

The Tx Ring Size Register contains the element size and element counts for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

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Table 14-9631. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4980 0048h + formula

Figure 14-4765. RINGACC_CFG_RING_SIZE_j Name Register

31	30	29	28	27	26	25	24
QMODE		RESERVED			ELSIZE		
R/W		NONE			R/W		
0h		0h			0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				SIZE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SIZE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIZE							
R/W							
0h							

Table 14-9632. RINGACC_CFG_RING_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	QMODE	R/W	0h	Defines the mode for this ring or queue. 0 `exposed ring mode for SW direct access` 1 `messaging mode when all operations are through bus accesses, allowing multiple producers or consumers.` 2 `credentials mode is message mode plus stores credentials with each message, requiring the ring size to be doubled to fit the credentials along with the same number of elements when using the first 2 modes. Any exposed memory should be protected by a firewall from unwanted access.`
29:27	RESERVED	NONE	0h	Reserved
26:24	ELSIZE	R/W	0h	Ring element size. This field is encoded as follows: 0 = 4 bytes 1 = 8 bytes 2 = 16 bytes 3 = 32 bytes 4 = 64 bytes 5 = 128 bytes 6 = 256 bytes 7 = RESERVED Reset Source: srst_n
23:20	RESERVED	NONE	0h	Reserved
19:0	SIZE	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. For rings in CREDENTIALS or QM modes the size must be an even number. Reset Source: srst_n

14.6.7.2.14 RINGACC_CFG_RING_EVENT_J Register

14.6.7.2.14.1 RINGACC_CFG_RING_EVENT_J Register (Offset = 4Ch) [reset = FFFFh]

The Ring Event Register is an Output Event Steering 'OES' register that specifies the event number used to denote the occurrence of an up event [empty to not-empty] or a down event [non-empty to empty] for this ring.

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Table 14-9633. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4980 004Ch + formula

Figure 14-4766. RINGACC_CFG_RING_EVENT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EVT							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
EVT							
R/W							
FFFFh							

Table 14-9634. RINGACC_CFG_RING_EVENT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EVT	R/W	FFFFh	Defines the event for this ring or queue. Reset Source: srst_n

14.6.7.2.15 RINGACC_CFG_RING_ORDERID_J Register

14.6.7.2.15.1 RINGACC_CFG_RING_ORDERID_J Register (Offset = 50h) [reset = 0h]

The Ring OrderID Register contains the bus orderid value for the ring memory access.

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Table 14-9635. Instance Table

Instance Name	Physical Address
DMASS0_RINGACC_0	4980 0050h + formula

Figure 14-4767. RINGACC_CFG_RING_ORDERID_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			REPLACE	ORDERID			
NONE			R/W	R/W			
0h			0h	0h			

Table 14-9636. RINGACC_CFG_RING_ORDERID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	REPLACE	R/W	0h	Indicates to replace the bus orderid value for this ring or queue with the orderid MMR field. This allows control over the orderid value when it must be restricted due to the topology for QoS reasons. 0 = bypass and use the orderid from the source transaction for the destination transaction. 1 = use the orderid MMR field value for the destination transaction. Reset Source: srst_n
3:0	ORDERID	R/W	0h	Defines the bus orderid value for this ring or queue. Reset Source: srst_n

14.6.8 DMASS_SEC_PROXY_0 Summaries

DMASS_SEC_PROXY_0 Summaries

Table 14-9637. SEC_PROXY Registers, Base Address=4825 0000h, Length=256

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_PID	4825 0000h
4h	32	SEC_PROXY_CONFIG	4825 0004h
14h	32	SEC_PROXY_GLB_EVT	4825 0014h

Table 14-9638. SEC_PROXY_SCFG Registers, Base Address=4A40 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_SCFG_BUFFER_L	4A40 0000h
4h	32	SEC_PROXY_SCFG_BUFFER_H	4A40 0004h
8h	32	SEC_PROXY_SCFG_TARGET_L	4A40 0008h
Ch	32	SEC_PROXY_SCFG_TARGET_H	4A40 000Ch
10h	32	SEC_PROXY_SCFG_ORDERID	4A40 0010h
1000h	32	SEC_PROXY_SCFG_THREAD_CTL_J	4A40 1000h + formula
1004h	32	SEC_PROXY_SCFG_THREAD_EVT_MAP_J	4A40 1004h + formula
1008h	32	SEC_PROXY_SCFG_THREAD_DST_J	4A40 1008h + formula

Table 14-9639. SEC_PROXY_RT Registers, Base Address=4A60 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	SEC_PROXY_RT_THREAD_STATUS_J	4A60 0000h + formula
4h	32	SEC_PROXY_RT_THREAD_THR_J	4A60 0004h + formula

Table 14-9640. PROXY_TARGET Registers, Base Address=4D00 0000h, Length=524288

Offset	Length	Register Name	DMASS0_SEC_PROXY_0 Physical Address
0h	32	PROXY_TARGET_THREAD_DATA_J	4D00 0000h + formula
4h	32	PROXY_TARGET_THREAD_MESSAGE_J_K	4D00 0004h + formula

14.6.9 Note on PDMA Instances

Only PDMA0, PDMA1, and PDMA4 are shown in the next section. All other PDMAs are implemented in FIFO, so there are no register instances.

14.6.10 PDMA

PDMA

14.6.10.1 PDMA Summaries

PDMA Summaries

Table 14-9641. ECC_AGGR Registers, Base Address=00C0 1000h, Length=1024

Offset	Length	Register Name	PDMA1 Physical Address	PDMA0 Physical Address
0h	32	ECC_AGGR_REV	00C0 0000h	00C0 1000h
8h	32	ECC_AGGR_VECTOR	00C0 0008h	00C0 1008h
Ch	32	ECC_AGGR_STAT	00C0 000Ch	00C0 100Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	00C0 0010h + formula	00C0 1010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	00C0 003Ch	00C0 103Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	00C0 0040h	00C0 1040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	00C0 0080h	00C0 1080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	00C0 00C0h	00C0 10C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	00C0 013Ch	00C0 113Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	00C0 0140h	00C0 1140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	00C0 0180h	00C0 1180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	00C0 01C0h	00C0 11C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	00C0 0200h	00C0 1200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	00C0 0204h	00C0 1204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	00C0 0208h	00C0 1208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	00C0 020Ch	00C0 120Ch

14.6.10.2 PDMA Registers

PDMA Registers

14.6.10.2.1 ECC_AGGR_REV Register

14.6.10.2.1.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-9642. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0000h
PDMA1	00C0 1000h

Figure 14-4768. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
5h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-9643. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.6.10.2.2 ECC_AGGR_VECTOR Register

14.6.10.2.2.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-9644. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0008h
PDMA1	00C0 1008h

Figure 14-4769. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9645. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.6.10.2.3 ECC_AGGR_STAT Register

14.6.10.2.3.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

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Table 14-9646. Instance Table

Instance Name	Physical Address
PDMA0	00C0 000Ch
PDMA1	00C0 100Ch

Figure 14-4770. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-9647. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.6.10.2.4 ECC_AGGR_RESERVED_SVBUS_J Register

14.6.10.2.4.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-9648. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0010h + formula
PDMA1	00C0 1010h + formula

Figure 14-4771. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-9649. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.6.10.2.5 ECC_AGGR_SEC_EOI_REG Register

14.6.10.2.5.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-9650. Instance Table

Instance Name	Physical Address
PDMA0	00C0 003Ch
PDMA1	00C0 103Ch

Figure 14-4772. ECC_AGGR_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9651. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.10.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

14.6.10.2.6.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9652. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0040h
PDMA1	00C0 1040h

Figure 14-4773. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_PEND	RPCF0_RAMECC_PEND	TPCF1_RAMECC_PEND	TPCF0_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9653. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf1_ramecc_pend
2	RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf0_ramecc_pend
1	TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf1_ramecc_pend
0	TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf0_ramecc_pend

14.6.10.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.6.10.2.7.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9654. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0080h
PDMA1	00C0 1080h

Figure 14-4774. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9655. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf0_ramecc_pend

14.6.10.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.6.10.2.8.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9656. Instance Table

Instance Name	Physical Address
PDMA0	00C0 00C0h
PDMA1	00C0 10C0h

Figure 14-4775. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RPCF1_RAMECC_ENABLE_CLR	RPCF0_RAMECC_ENABLE_CLR	TPCF1_RAMECC_ENABLE_CLR	TPCF0_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9657. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf0_ramecc_pend

14.6.10.2.9 ECC_AGGR_DED_EOI_REG Register

14.6.10.2.9.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-9658. Instance Table

Instance Name	Physical Address
PDMA0	00C0 013Ch
PDMA1	00C0 113Ch

Figure 14-4776. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-9659. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.10.2.10 ECC_AGGR_DED_STATUS_REG0 Register

14.6.10.2.10.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9660. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0140h
PDMA1	00C0 1140h

Figure 14-4777. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RPCF1_RAMECC_PEND	RPCF0_RAMECC_PEND	TPCF1_RAMECC_PEND	TPCF0_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9661. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf1_ramecc_pend
2	RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf0_ramecc_pend
1	TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf1_ramecc_pend
0	TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf0_ramecc_pend

14.6.10.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.6.10.2.11.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-9662. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0180h
PDMA1	00C0 1180h

Figure 14-4778. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9663. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf0_ramecc_pend

14.6.10.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.6.10.2.12.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9664. Instance Table

Instance Name	Physical Address
PDMA0	00C0 01C0h
PDMA1	00C0 11C0h

Figure 14-4779. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_CLR	RPCF0_RAMECC_ENABLE_CLR	TPCF1_RAMECC_ENABLE_CLR	TPCF0_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9665. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf0_ramecc_pend

14.6.10.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

14.6.10.2.13.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 14-9666. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0200h
PDMA1	00C0 1200h

Figure 14-4780. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9667. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.6.10.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

14.6.10.2.14.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-9668. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0204h
PDMA1	00C0 1204h

Figure 14-4781. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9669. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.6.10.2.15 ECC_AGGR_AGGR_STATUS_SET Register

14.6.10.2.15.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-9670. Instance Table

Instance Name	Physical Address
PDMA0	00C0 0208h
PDMA1	00C0 1208h

Figure 14-4782. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-9671. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.6.10.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

14.6.10.2.16.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-9672. Instance Table

Instance Name	Physical Address
PDMA0	00C0 020Ch
PDMA1	00C0 120Ch

Figure 14-4783. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-9673. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.6.11 PDMA

PDMA

14.6.11.1 PDMA Summaries

PDMA Summaries

Table 14-9674. ECC_AGGR Registers, Base Address=00C0 2000h, Length=1024

Offset	Length	Register Name	PDMA4 Physical Address
0h	32	ECC_AGGR_REV	00C0 2000h
8h	32	ECC_AGGR_VECTOR	00C0 2008h
Ch	32	ECC_AGGR_STAT	00C0 200Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	00C0 2010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	00C0 203Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	00C0 2040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	00C0 2080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	00C0 20C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	00C0 213Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	00C0 2140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	00C0 2180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	00C0 21C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	00C0 2200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	00C0 2204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	00C0 2208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	00C0 220Ch

14.6.11.2 PDMA Registers

PDMA Registers

14.6.11.2.1 ECC_AGGR_REV Register

14.6.11.2.1.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A02A01h]

Revision parameters

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Table 14-9675. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2000h

Figure 14-4784. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">5h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-9676. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	5h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.6.11.2.2 ECC_AGGR_VECTOR Register

14.6.11.2.2.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-9677. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2008h

Figure 14-4785. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-9678. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.6.11.2.3 ECC_AGGR_STAT Register

14.6.11.2.3.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 4h]

Misc Status

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Table 14-9679. Instance Table

Instance Name	Physical Address
PDMA4	00C0 200Ch

Figure 14-4786. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					NUM_RAMS		
NONE					R		
0h					4h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_RAMS							
R							
4h							

Table 14-9680. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

14.6.11.2.4 ECC_AGGR_RESERVED_SVBUS_J Register

14.6.11.2.4.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-9681. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2010h + formula

Figure 14-4787. ECC_AGGR_RESERVED_SVBUS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9682. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.6.11.2.5 ECC_AGGR_SEC_EOI_REG Register

14.6.11.2.5.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-9683. Instance Table

Instance Name	Physical Address
PDMA4	00C0 203Ch

Figure 14-4788. ECC_AGGR_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-9684. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.11.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

14.6.11.2.6.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9685. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2040h

Figure 14-4789. ECC_AGGR_SEC_STATUS_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>RPCF1_RAMECC_PEND</td><td>RPCF0_RAMECC_PEND</td><td>TPCF1_RAMECC_PEND</td><td>TPCF0_RAMECC_PEND</td></tr>
<tr><td colspan="4">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9686. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf1_ramecc_pend
2	RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf0_ramecc_pend
1	TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf1_ramecc_pend
0	TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf0_ramecc_pend

14.6.11.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.6.11.2.7.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9687. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2080h

Figure 14-4790. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9688. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf0_ramecc_pend

14.6.11.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.6.11.2.8.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9689. Instance Table

Instance Name	Physical Address
PDMA4	00C0 20C0h

Figure 14-4791. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_CLR	RPCF0_RAMECC_ENABLE_CLR	TPCF1_RAMECC_ENABLE_CLR	TPCF0_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9690. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf0_ramecc_pend

14.6.11.2.9 ECC_AGGR_DED_EOI_REG Register

14.6.11.2.9.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-9691. Instance Table

Instance Name	Physical Address
PDMA4	00C0 213Ch

Figure 14-4792. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-9692. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.6.11.2.10 ECC_AGGR_DED_STATUS_REG0 Register

14.6.11.2.10.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-9693. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2140h

Figure 14-4793. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_PEND	RPCF0_RAMECC_PEND	TPCF1_RAMECC_PEND	TPCF0_RAMECC_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9694. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf1_ramecc_pend
2	RPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for rpcf0_ramecc_pend
1	TPCF1_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf1_ramecc_pend
0	TPCF0_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for tpcf0_ramecc_pend

14.6.11.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.6.11.2.11.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-9695. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2180h

Figure 14-4794. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9696. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tpcf0_ramecc_pend

14.6.11.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.6.11.2.12.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-9697. Instance Table

Instance Name	Physical Address
PDMA4	00C0 21C0h

Figure 14-4795. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_CLR	RPCF0_RAMECC_ENABLE_CLR	TPCF1_RAMECC_ENABLE_CLR	TPCF0_RAMECC_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9698. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf1_ramecc_pend
2	RPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rpcf0_ramecc_pend
1	TPCF1_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf1_ramecc_pend
0	TPCF0_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tpcf0_ramecc_pend

14.6.11.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

14.6.11.2.13.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-9699. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2200h

Figure 14-4796. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-9700. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.6.11.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

14.6.11.2.14.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-9701. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2204h

Figure 14-4797. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-9702. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.6.11.2.15 ECC_AGGR_AGGR_STATUS_SET Register

14.6.11.2.15.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-9703. Instance Table

Instance Name	Physical Address
PDMA4	00C0 2208h

Figure 14-4798. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-9704. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.6.11.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

14.6.11.2.16.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-9705. Instance Table

Instance Name	Physical Address
PDMA4	00C0 220Ch

Figure 14-4799. ECC_AGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-9706. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7 Peripherals Registers

14.7.1 Audio Peripherals Registers

14.7.1.1 aasrc

aasrc

14.7.1.1.1 aasrc Summaries

aasrc Summaries

Table 14-9707. AASRC_CFG Registers, Base Address=02D0 0000h, Length=16384

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
0h	32	AASRC_CFG_AASRC_PID	02D0 0000h	02D4 0000h
10h	32	AASRC_CFG_AASRC_SYSCONFIG	02D0 0010h	02D4 0010h
20h	32	AASRC_CFG_IRQ_EOI_REGISTER	02D0 0020h	02D4 0020h
24h	32	AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER	02D0 0024h	02D4 0024h
28h	32	AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER	02D0 0028h	02D4 0028h
2Ch	32	AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER	02D0 002Ch	02D4 002Ch
30h	32	AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER	02D0 0030h	02D4 0030h
34h	32	AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER	02D0 0034h	02D4 0034h
38h	32	AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER	02D0 0038h	02D4 0038h
3Ch	32	AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER	02D0 003Ch	02D4 003Ch
40h	32	AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER	02D0 0040h	02D4 0040h
44h	32	AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER	02D0 0044h	02D4 0044h
48h	32	AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER	02D0 0048h	02D4 0048h
4Ch	32	AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER	02D0 004Ch	02D4 004Ch
50h	32	AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER	02D0 0050h	02D4 0050h
54h	32	AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER	02D0 0054h	02D4 0054h
58h	32	AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER	02D0 0058h	02D4 0058h
5Ch	32	AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER	02D0 005Ch	02D4 005Ch
60h	32	AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER	02D0 0060h	02D4 0060h
64h	32	AASRC_CFG_ERROR_INTERRUPT_STATUS_RAW_REGISTER	02D0 0064h	02D4 0064h
68h	32	AASRC_CFG_ERROR_INTERRUPT_STATUS_ENABLED_REGISTER	02D0 0068h	02D4 0068h
6Ch	32	AASRC_CFG_ERROR_INTERRUPT_ENABLE_SET_REGISTER	02D0 006Ch	02D4 006Ch
70h	32	AASRC_CFG_ERROR_INTERRUPT_ENABLE_CLEAR_REGISTER	02D0 0070h	02D4 0070h
74h	32	AASRC_CFG_INPUT_GROUP_0_SELECT	02D0 0074h	02D4 0074h
78h	32	AASRC_CFG_INPUT_GROUP_1_SELECT	02D0 0078h	02D4 0078h
7Ch	32	AASRC_CFG_INPUT_GROUP_2_SELECT	02D0 007Ch	02D4 007Ch

Table 14-9707. AASRC_CFG Registers, Base Address=02D0 0000h, Length=16384 (continued)

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
80h	32	AASRC_CFG_INPUT_GROUP_3_SELECT	02D0 0080h	02D4 0080h
94h	32	AASRC_CFG_OUTPUT_GROUP_0_SELECT	02D0 0094h	02D4 0094h
98h	32	AASRC_CFG_OUTPUT_GROUP_1_SELECT	02D0 0098h	02D4 0098h
9Ch	32	AASRC_CFG_OUTPUT_GROUP_2_SELECT	02D0 009Ch	02D4 009Ch
A0h	32	AASRC_CFG_OUTPUT_GROUP_3_SELECT	02D0 00A0h	02D4 00A0h
100h	32	AASRC_CFG_SRC_FIFO_CONTROL_0	02D0 0100h	02D4 0100h
104h	32	AASRC_CFG_SRC_CONTROL_0	02D0 0104h	02D4 0104h
108h	32	AASRC_CFG_SRC_STATUS_0	02D0 0108h	02D4 0108h
110h	32	AASRC_CFG_SRC_FIFO_CONTROL_1	02D0 0110h	02D4 0110h
114h	32	AASRC_CFG_SRC_CONTROL_1	02D0 0114h	02D4 0114h
118h	32	AASRC_CFG_SRC_STATUS_1	02D0 0118h	02D4 0118h
120h	32	AASRC_CFG_SRC_FIFO_CONTROL_2	02D0 0120h	02D4 0120h
124h	32	AASRC_CFG_SRC_CONTROL_2	02D0 0124h	02D4 0124h
128h	32	AASRC_CFG_SRC_STATUS_2	02D0 0128h	02D4 0128h
130h	32	AASRC_CFG_SRC_FIFO_CONTROL_3	02D0 0130h	02D4 0130h
134h	32	AASRC_CFG_SRC_CONTROL_3	02D0 0134h	02D4 0134h
138h	32	AASRC_CFG_SRC_STATUS_3	02D0 0138h	02D4 0138h
140h	32	AASRC_CFG_SRC_FIFO_CONTROL_4	02D0 0140h	02D4 0140h
144h	32	AASRC_CFG_SRC_CONTROL_4	02D0 0144h	02D4 0144h
148h	32	AASRC_CFG_SRC_STATUS_4	02D0 0148h	02D4 0148h
150h	32	AASRC_CFG_SRC_FIFO_CONTROL_5	02D0 0150h	02D4 0150h
154h	32	AASRC_CFG_SRC_CONTROL_5	02D0 0154h	02D4 0154h
158h	32	AASRC_CFG_SRC_STATUS_5	02D0 0158h	02D4 0158h
160h	32	AASRC_CFG_SRC_FIFO_CONTROL_6	02D0 0160h	02D4 0160h
164h	32	AASRC_CFG_SRC_CONTROL_6	02D0 0164h	02D4 0164h
168h	32	AASRC_CFG_SRC_STATUS_6	02D0 0168h	02D4 0168h
170h	32	AASRC_CFG_SRC_FIFO_CONTROL_7	02D0 0170h	02D4 0170h
174h	32	AASRC_CFG_SRC_CONTROL_7	02D0 0174h	02D4 0174h
178h	32	AASRC_CFG_SRC_STATUS_7	02D0 0178h	02D4 0178h
180h	32	AASRC_CFG_GROUP_FIFO_CONTROL_0	02D0 0180h	02D4 0180h
184h	32	AASRC_CFG_GROUP_SRC_CONTROL_0	02D0 0184h	02D4 0184h
188h	32	AASRC_CFG_GROUP_FIFO_CONTROL_1	02D0 0188h	02D4 0188h
18Ch	32	AASRC_CFG_GROUP_SRC_CONTROL_1	02D0 018Ch	02D4 018Ch
190h	32	AASRC_CFG_GROUP_FIFO_CONTROL_2	02D0 0190h	02D4 0190h
194h	32	AASRC_CFG_GROUP_SRC_CONTROL_2	02D0 0194h	02D4 0194h
198h	32	AASRC_CFG_GROUP_FIFO_CONTROL_3	02D0 0198h	02D4 0198h
19Ch	32	AASRC_CFG_GROUP_SRC_CONTROL_3	02D0 019Ch	02D4 019Ch
200h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_0	02D0 0200h	02D4 0200h
204h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_0	02D0 0204h	02D4 0204h
208h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_0	02D0 0208h	02D4 0208h
20Ch	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_0	02D0 020Ch	02D4 020Ch

Table 14-9707. AASRC_CFG Registers, Base Address=02D0 0000h, Length=16384 (continued)

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
210h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0	02D0 0210h	02D4 0210h
214h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0	02D0 0214h	02D4 0214h
218h	32	AASRC_CFG_INPUT_CLOCKZONE_COUNT_0	02D0 0218h	02D4 0218h
21Ch	32	AASRC_CFG_INPUT_CLOCKZONE_CONTROL_0	02D0 021Ch	02D4 021Ch
220h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_0	02D0 0220h	02D4 0220h
224h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_0	02D0 0224h	02D4 0224h
228h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_0	02D0 0228h	02D4 0228h
22Ch	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_0	02D0 022Ch	02D4 022Ch
230h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0	02D0 0230h	02D4 0230h
234h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0	02D0 0234h	02D4 0234h
238h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_0	02D0 0238h	02D4 0238h
23Ch	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_0	02D0 023Ch	02D4 023Ch
240h	32	AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_0	02D0 0240h	02D4 0240h
244h	32	AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_0	02D0 0244h	02D4 0244h
248h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0	02D0 0248h	02D4 0248h
24Ch	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0	02D0 024Ch	02D4 024Ch
250h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0	02D0 0250h	02D4 0250h
254h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0	02D0 0254h	02D4 0254h
280h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_1	02D0 0280h	02D4 0280h
284h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_1	02D0 0284h	02D4 0284h
288h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_1	02D0 0288h	02D4 0288h
28Ch	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_1	02D0 028Ch	02D4 028Ch
290h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1	02D0 0290h	02D4 0290h
294h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1	02D0 0294h	02D4 0294h
298h	32	AASRC_CFG_INPUT_CLOCKZONE_COUNT_1	02D0 0298h	02D4 0298h
29Ch	32	AASRC_CFG_INPUT_CLOCKZONE_CONTROL_1	02D0 029Ch	02D4 029Ch
2A0h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_1	02D0 02A0h	02D4 02A0h

Table 14-9707. AASRC_CFG Registers, Base Address=02D0 0000h, Length=16384 (continued)

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
2A4h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_1	02D0 02A4h	02D4 02A4h
2A8h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_1	02D0 02A8h	02D4 02A8h
2ACh	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_1	02D0 02ACh	02D4 02ACh
2B0h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1	02D0 02B0h	02D4 02B0h
2B4h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1	02D0 02B4h	02D4 02B4h
2B8h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_1	02D0 02B8h	02D4 02B8h
2BCh	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_1	02D0 02BCh	02D4 02BCh
2C0h	32	AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_1	02D0 02C0h	02D4 02C0h
2C4h	32	AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_1	02D0 02C4h	02D4 02C4h
2C8h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1	02D0 02C8h	02D4 02C8h
2CCh	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1	02D0 02CCh	02D4 02CCh
2D0h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1	02D0 02D0h	02D4 02D0h
2D4h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1	02D0 02D4h	02D4 02D4h
300h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_2	02D0 0300h	02D4 0300h
304h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_2	02D0 0304h	02D4 0304h
308h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_2	02D0 0308h	02D4 0308h
30Ch	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_2	02D0 030Ch	02D4 030Ch
310h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2	02D0 0310h	02D4 0310h
314h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2	02D0 0314h	02D4 0314h
318h	32	AASRC_CFG_INPUT_CLOCKZONE_COUNT_2	02D0 0318h	02D4 0318h
31Ch	32	AASRC_CFG_INPUT_CLOCKZONE_CONTROL_2	02D0 031Ch	02D4 031Ch
320h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_2	02D0 0320h	02D4 0320h
324h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_2	02D0 0324h	02D4 0324h
328h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_2	02D0 0328h	02D4 0328h
32Ch	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_2	02D0 032Ch	02D4 032Ch
330h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2	02D0 0330h	02D4 0330h
334h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2	02D0 0334h	02D4 0334h

Table 14-9707. AASRC_CFG Registers, Base Address=02D0 0000h, Length=16384 (continued)

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
338h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_2	02D0 0338h	02D4 0338h
33Ch	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_2	02D0 033Ch	02D4 033Ch
340h	32	AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_2	02D0 0340h	02D4 0340h
344h	32	AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_2	02D0 0344h	02D4 0344h
348h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2	02D0 0348h	02D4 0348h
34Ch	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2	02D0 034Ch	02D4 034Ch
350h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2	02D0 0350h	02D4 0350h
354h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2	02D0 0354h	02D4 0354h
380h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_3	02D0 0380h	02D4 0380h
384h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_3	02D0 0384h	02D4 0384h
388h	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_3	02D0 0388h	02D4 0388h
38Ch	32	AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_3	02D0 038Ch	02D4 038Ch
390h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3	02D0 0390h	02D4 0390h
394h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3	02D0 0394h	02D4 0394h
398h	32	AASRC_CFG_INPUT_CLOCKZONE_COUNT_3	02D0 0398h	02D4 0398h
39Ch	32	AASRC_CFG_INPUT_CLOCKZONE_CONTROL_3	02D0 039Ch	02D4 039Ch
3A0h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_3	02D0 03A0h	02D4 03A0h
3A4h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_3	02D0 03A4h	02D4 03A4h
3A8h	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_3	02D0 03A8h	02D4 03A8h
3ACh	32	AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_3	02D0 03ACh	02D4 03ACh
3B0h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3	02D0 03B0h	02D4 03B0h
3B4h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3	02D0 03B4h	02D4 03B4h
3B8h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_3	02D0 03B8h	02D4 03B8h
3BCh	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_3	02D0 03BCh	02D4 03BCh
3C0h	32	AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_3	02D0 03C0h	02D4 03C0h
3C4h	32	AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_3	02D0 03C4h	02D4 03C4h
3C8h	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3	02D0 03C8h	02D4 03C8h

Table 14-9707. AASRC_CFG Registers, Base Address=02D0 0000h, Length=16384 (continued)

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
3CCh	32	AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3	02D0 03CCh	02D4 03CCh
3D0h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3	02D0 03D0h	02D4 03D0h
3D4h	32	AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3	02D0 03D4h	02D4 03D4h
400h	32	AASRC_CFG_INPUT_CLOCK_ZONE_DIVIDER	02D0 0400h	02D4 0400h
404h	32	AASRC_CFG_OUTPUT_CLOCK_ZONE_DIVIDER	02D0 0404h	02D4 0404h

Table 14-9708. AASRC_DATA_R0 Registers, Base Address=02D1 0000h, Length=16384

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
0h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L0	02D1 0000h	02D5 0000h
4h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R0	02D1 0004h	02D5 0004h
8h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L1	02D1 0008h	02D5 0008h
Ch	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R1	02D1 000Ch	02D5 000Ch
10h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L2	02D1 0010h	02D5 0010h
14h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R2	02D1 0014h	02D5 0014h
18h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L3	02D1 0018h	02D5 0018h
1Ch	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R3	02D1 001Ch	02D5 001Ch
20h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L4	02D1 0020h	02D5 0020h
24h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R4	02D1 0024h	02D5 0024h
28h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L5	02D1 0028h	02D5 0028h
2Ch	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R5	02D1 002Ch	02D5 002Ch
30h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L6	02D1 0030h	02D5 0030h
34h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R6	02D1 0034h	02D5 0034h
38h	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L7	02D1 0038h	02D5 0038h
3Ch	32	AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R7	02D1 003Ch	02D5 003Ch
80h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L0	02D1 0080h	02D5 0080h
84h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R0	02D1 0084h	02D5 0084h
88h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L1	02D1 0088h	02D5 0088h
8Ch	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R1	02D1 008Ch	02D5 008Ch

Table 14-9708. AASRC_DATA_R0 Registers, Base Address=02D1 0000h, Length=16384 (continued)

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
90h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L2	02D1 0090h	02D5 0090h
94h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R2	02D1 0094h	02D5 0094h
98h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L3	02D1 0098h	02D5 0098h
9Ch	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R3	02D1 009Ch	02D5 009Ch
A0h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L4	02D1 00A0h	02D5 00A0h
A4h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R4	02D1 00A4h	02D5 00A4h
A8h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L5	02D1 00A8h	02D5 00A8h
ACh	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R5	02D1 00ACh	02D5 00ACh
B0h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L6	02D1 00B0h	02D5 00B0h
B4h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R6	02D1 00B4h	02D5 00B4h
B8h	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L7	02D1 00B8h	02D5 00B8h
BCh	32	AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R7	02D1 00BCh	02D5 00BCh

Table 14-9709. AASRC_DATA_R1 Registers, Base Address=02D2 0000h, Length=16384

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
0h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L0	02D2 0000h	02D6 0000h
100h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R0	02D2 0100h	02D6 0100h
200h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L1	02D2 0200h	02D6 0200h
300h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R1	02D2 0300h	02D6 0300h
400h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L2	02D2 0400h	02D6 0400h
500h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R2	02D2 0500h	02D6 0500h
600h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L3	02D2 0600h	02D6 0600h
700h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R3	02D2 0700h	02D6 0700h
800h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L4	02D2 0800h	02D6 0800h
900h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R4	02D2 0900h	02D6 0900h
A00h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L5	02D2 0A00h	02D6 0A00h
B00h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R5	02D2 0B00h	02D6 0B00h
C00h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L6	02D2 0C00h	02D6 0C00h

Table 14-9709. AASRC_DATA_R1 Registers, Base Address=02D2 0000h, Length=16384 (continued)

Offset	Length	Register Name	AASRC0 Physical Address	AASRC1 Physical Address
D00h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R6	02D2 0D00h	02D6 0D00h
E00h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L7	02D2 0E00h	02D6 0E00h
F00h	32	AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R7	02D2 0F00h	02D6 0F00h
1000h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L0	02D2 1000h	02D6 1000h
1100h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R0	02D2 1100h	02D6 1100h
1200h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L1	02D2 1200h	02D6 1200h
1300h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R1	02D2 1300h	02D6 1300h
1400h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L2	02D2 1400h	02D6 1400h
1500h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R2	02D2 1500h	02D6 1500h
1600h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L3	02D2 1600h	02D6 1600h
1700h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R3	02D2 1700h	02D6 1700h
1800h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L4	02D2 1800h	02D6 1800h
1900h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R4	02D2 1900h	02D6 1900h
1A00h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L5	02D2 1A00h	02D6 1A00h
1B00h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R5	02D2 1B00h	02D6 1B00h
1C00h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L6	02D2 1C00h	02D6 1C00h
1D00h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R6	02D2 1D00h	02D6 1D00h
1E00h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L7	02D2 1E00h	02D6 1E00h
1F00h	32	AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R7	02D2 1F00h	02D6 1F00h

14.7.1.1.2 aasrc Registers

aasrc Registers

14.7.1.1.2.1 AASRC_CFG_AASRC_PID Register

14.7.1.1.2.1.1 AASRC_CFG_AASRC_PID Register (Offset = 0h) [reset = 64004900h]

Revision register

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Table 14-9710. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0000h
AASRC1	02D4 0000h

Figure 14-4800. AASRC_CFG_AASRC_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BUSINESS_UNIT		FUNC			
R		R		R			
1h		2h		400h			
23	22	21	20	19	18	17	16
FUNC							
R							
400h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
9h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-9711. AASRC_CFG_AASRC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	The scheme of the register used This indicates the PDR35 Method
29:28	BUSINESS_UNIT	R	2h	00:ASP, 01:WTBU, 10:Processors, 11:Reserved
27:16	FUNC	R	400h	The function of the module being used
15:11	RTL	R	9h	RTL Release Version. The PDR release number of this IP
10:8	MAJOR	R	1h	Major Release Number
7:6	CUSTOM	R	0h	Custom IP
5:0	MINOR	R	0h	Minor Release Number

14.7.1.1.2.2 AASRC_CFG_AASRC_SYSCONFIG Register

14.7.1.1.2.2.1 AASRC_CFG_AASRC_SYSCONFIG Register (Offset = 10h) [reset = 0h]

AASRC SYSCONFIG

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Table 14-9712. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0010h
AASRC1	02D4 0010h

Figure 14-4801. AASRC_CFG_AASRC_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						DATA_FORMAT_DISABLE	SOFTRESET
R						R/W	R/W
0h						0h	0h

Table 14-9713. AASRC_CFG_AASRC_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0
1	DATA_FORMAT_DISABLE	R/W	0h	If this bit is set, data formatting needs to be done outside 0 `Data formatting enabled` 1 `Data formatting disabled`
0	SOFTRESET	R/W	0h	Write 1'b1 for reset assertion and 1'b0 for reset de-assertion 0 `Reset not asserted` 1 `Reset is asserted`

14.7.1.1.2.3 AASRC_CFG_IRQ_EOI_REGISTER Register

14.7.1.1.2.3.1 AASRC_CFG_IRQ_EOI_REGISTER Register (Offset = 20h) [reset = 0h]

This register contains the EOI vector register contents as defined by HL0.8

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Table 14-9714. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0020h
AASRC1	02D4 0020h

Figure 14-4802. AASRC_CFG_IRQ_EOI_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9715. AASRC_CFG_IRQ_EOI_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Always read as 0
7:0	EOI_VECTOR	R/W	0h	Number associated with the ipgenericirq for intr output Write 0x0 _ Write to input_intr Write 0x1 _ Write to output_intr Write 0x2 _ Write to ingroup_intr Write 0x3 _ Write to outgroup_intr Write 0x4 _ Write to error_intr Any other write value is ignoredAlways read as 0

14.7.1.1.2.4 AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register

14.7.1.1.2.4.1 AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register (Offset = 24h) [reset = 0h]

Input FIFO Interrupt Status Raw/Set Register. Note that reading this register immediately after writing to it would reflect old value instead of the written value; wait for 2 system clock cycles after writing to read written value

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Table 14-9716. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0024h
AASRC1	02D4 0024h

Figure 14-4803. AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_14_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_13_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_12_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_11_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_10_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_9_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_8_INPUT_FIFO_THRESHOLD_RAW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_6_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_5_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_4_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_3_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_2_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_1_INPUT_FIFO_THRESHOLD_RAW	CHANNEL_0_INPUT_FIFO_THRESHOLD_RAW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9717. AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 15 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
14	CHANNEL_14_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 14 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

Table 14-9717. AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 13 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
12	CHANNEL_12_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 12 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
11	CHANNEL_11_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 11 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
10	CHANNEL_10_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 10 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
9	CHANNEL_9_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 9 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
8	CHANNEL_8_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 8 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
7	CHANNEL_7_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 7 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
6	CHANNEL_6_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 6 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
5	CHANNEL_5_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 5 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9717. AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CHANNEL_4_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 4 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
3	CHANNEL_3_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 3 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
2	CHANNEL_2_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 2 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
1	CHANNEL_1_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 1 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
0	CHANNEL_0_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 0 Input FIFO Threshold Interrupt Read indicates raw status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active

14.7.1.1.2.5 AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register

14.7.1.1.2.5.1 AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register (Offset = 28h) [reset = 0h]

This register contains the enabled interrupt status as defined in HL0.8 for the Input FIFO for each Channel. A read of the Interrupt Status Register returns the current pending status of the interrupt sources as masked by the current enable flag for each of those sources. A write to this register clears the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written

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Table 14-9718. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0028h
AASRC1	02D4 0028h

Figure 14-4804. AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_14_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_13_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_12_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_11_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_10_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_9_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_8_INPUT_FIFO_THRESHOLD_ENABLED
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_6_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_5_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_4_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_3_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_2_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_1_INPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_0_INPUT_FIFO_THRESHOLD_ENABLED
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9719. AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 15 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
14	CHANNEL_14_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 14 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9719. AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 13 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
12	CHANNEL_12_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 12 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
11	CHANNEL_11_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 11 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
10	CHANNEL_10_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 10 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
9	CHANNEL_9_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 9 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
8	CHANNEL_8_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 8 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
7	CHANNEL_7_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 7 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
6	CHANNEL_6_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 6 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
5	CHANNEL_5_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 5 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9719. AASRC_CFG_INPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CHANNEL_4_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 4 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
3	CHANNEL_3_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 3 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
2	CHANNEL_2_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 2 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
1	CHANNEL_1_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 1 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
0	CHANNEL_0_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 0 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when the Input FIFO for this Channel is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

14.7.1.1.2.6 AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register

14.7.1.1.2.6.1 AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register (Offset = 2Ch) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Input FIFO interrupts. The FIFO interrupt for each Channel is configured in the control register for the Channel. This register is used to read and set the interrupt source enables. The enable bit is active high and a 1 indicates the source is enabled to interrupt the processor(s), while a 0 indicates the source will not interrupt the processor(s).

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Table 14-9720. Instance Table

Instance Name	Physical Address
AASRC0	02D0 002Ch
AASRC1	02D4 002Ch

Figure 14-4805. AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_14_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_13_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_12_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_11_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_10_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_9_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_8_INPUT_FIFO_THRESHOLD_ENABLE
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_6_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_5_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_4_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_3_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_2_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_1_INPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_0_INPUT_FIFO_THRESHOLD_ENABLE
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9721. AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 15 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
14	CHANNEL_14_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 14 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

Table 14-9721. AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 13 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
12	CHANNEL_12_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 12 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
11	CHANNEL_11_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 11 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
10	CHANNEL_10_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 10 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
9	CHANNEL_9_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 9 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
8	CHANNEL_8_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 8 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
7	CHANNEL_7_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 7 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
6	CHANNEL_6_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 6 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
5	CHANNEL_5_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 5 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
4	CHANNEL_4_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 4 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
3	CHANNEL_3_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 3 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
2	CHANNEL_2_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 2 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
1	CHANNEL_1_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 1 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9721. AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CHANNEL_0_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 10 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.7 AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register

14.7.1.1.2.7.1 AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register (Offset = 30h) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Input FIFO interrupts. The FIFO interrupt for each Channel is configured in the control register for the Channel. A read of the Interrupt Enable Clr register returns the current enable bits for the interrupt sources. A write to this register sets the enable to 0 for any source whose corresponding bit is 1 in the value written

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Table 14-9722. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0030h
AASRC1	02D4 0030h

Figure 14-4806. AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_14_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_13_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_12_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_11_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_10_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_9_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_8_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_6_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_5_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_4_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_3_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_2_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_1_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_0_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9723. AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 15 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
14	CHANNEL_14_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 14 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9723. AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 13 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
12	CHANNEL_12_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 12 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
11	CHANNEL_11_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 11 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
10	CHANNEL_10_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 10 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
9	CHANNEL_9_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 9 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
8	CHANNEL_8_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 8 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
7	CHANNEL_7_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 7 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
6	CHANNEL_6_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 6 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
5	CHANNEL_5_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 5 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
4	CHANNEL_4_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 4 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
3	CHANNEL_3_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 3 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
2	CHANNEL_2_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 2 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
1	CHANNEL_1_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 1 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

Table 14-9723. AASRC_CFG_INPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CHANNEL_0_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 0 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.8 AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register

14.7.1.1.2.8.1 AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register (Offset = 34h) [reset = 0h]

This register contains the raw interrupt status as defined in HL0.8 for the Output FIFO interrupts. The FIFO interrupt for each channel is configured in the control register for the channel. A read of the Interrupt Status Raw / Set Register returns the current pending status of the interrupt sources with no regard to any enable settings. A write to this register sets the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written. Note that reading this register immediately after writing to it would reflect old value instead of the written value; wait for 2 system clock cycles after writing to read written value.

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Table 14-9724. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0034h
AASRC1	02D4 0034h

Figure 14-4807. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_14_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_13_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_12_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_11_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_10_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_9_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_8_OUTPUT_FIFO_THRESHOLD_RAW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_6_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_5_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_4_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_3_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_2_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_1_OUTPUT_FIFO_THRESHOLD_RAW	CHANNEL_0_OUTPUT_FIFO_THRESHOLD_RAW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9725. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 15 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9725. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	CHANNEL_14_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 14 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
13	CHANNEL_13_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 13 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
12	CHANNEL_12_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 12 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
11	CHANNEL_11_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 11 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
10	CHANNEL_10_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 10 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
9	CHANNEL_9_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 9 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
8	CHANNEL_8_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 8 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
7	CHANNEL_7_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 7 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
6	CHANNEL_6_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 6 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

Table 14-9725. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 5 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
4	CHANNEL_4_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 4 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
3	CHANNEL_3_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 3 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
2	CHANNEL_2_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 2 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
1	CHANNEL_1_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 1 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
0	CHANNEL_0_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Channel 0 Output FIFO Threshold Interrupt Read indicates raw status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active

14.7.1.1.2.9 AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register

14.7.1.1.2.9.1 AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register (Offset = 38h) [reset = 0h]

This register contains the enabled interrupt status as defined in HL0.8 for the Output FIFO for each Channel. A read of the Interrupt Status Register returns the current pending status of the interrupt sources as masked by the current enable flag for each of those sources. A write to this register clears the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written.

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Table 14-9726. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0038h
AASRC1	02D4 0038h

Figure 14-4808. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_14_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_13_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_12_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_11_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_10_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_9_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_8_OUTPUT_FIFO_THRESHOLD_ENABLED
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_6_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_5_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_4_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_3_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_2_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_1_OUTPUT_FIFO_THRESHOLD_ENABLED	CHANNEL_0_OUTPUT_FIFO_THRESHOLD_ENABLED
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9727. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 15 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9727. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	CHANNEL_14_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 14 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
13	CHANNEL_13_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 13 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
12	CHANNEL_12_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 12 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
11	CHANNEL_11_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 11 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
10	CHANNEL_10_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 10 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
9	CHANNEL_9_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 9 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
8	CHANNEL_8_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 8 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
7	CHANNEL_7_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 7 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
6	CHANNEL_6_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 6 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9727. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 5 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
4	CHANNEL_4_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 4 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
3	CHANNEL_3_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 3 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
2	CHANNEL_2_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 2 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
1	CHANNEL_1_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 1 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
0	CHANNEL_0_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Channel 0 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when the Output FIFO for this Channel is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

14.7.1.1.2.10 AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register

14.7.1.1.2.10.1 AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register (Offset = 3Ch) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Output FIFO interrupts. The FIFO interrupt for each Channel is configured in the control register for the Channel. This register is used to read and set the interrupt source enables. The enable bit is active high and a 1 indicates the source is enabled to interrupt the processor(s), while a 0 indicates the source will not interrupt the processor(s).

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Table 14-9728. Instance Table

Instance Name	Physical Address
AASRC0	02D0 003Ch
AASRC1	02D4 003Ch

Figure 14-4809. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_14_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_13_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_12_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_11_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_10_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_9_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_8_OUTPUT_FIFO_THRESHOLD_ENABLE
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_6_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_5_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_4_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_3_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_2_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_1_OUTPUT_FIFO_THRESHOLD_ENABLE	CHANNEL_0_OUTPUT_FIFO_THRESHOLD_ENABLE
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9729. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 15 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
14	CHANNEL_14_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 14 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9729. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 13 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
12	CHANNEL_12_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 12 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
11	CHANNEL_11_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 11 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
10	CHANNEL_10_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 10 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
9	CHANNEL_9_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 9 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
8	CHANNEL_8_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 8 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
7	CHANNEL_7_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 7 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
6	CHANNEL_6_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 6 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
5	CHANNEL_5_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 5 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
4	CHANNEL_4_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 4 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
3	CHANNEL_3_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 3 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
2	CHANNEL_2_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 2 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
1	CHANNEL_1_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 1 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

Table 14-9729. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CHANNEL_0_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Channel 10 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.11 AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register

14.7.1.1.2.11.1 AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register (Offset = 40h) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Output FIFO interrupts. The FIFO interrupt for each Channel is configured in the control register for the Channel. A read of the Interrupt Enable Clr register returns the current enable bits for the interrupt sources. A write to this register sets the enable to 0 for any source whose corresponding bit is 1 in the value written

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Table 14-9730. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0040h
AASRC1	02D4 0040h

Figure 14-4810. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_14_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_13_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_12_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_11_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_10_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_9_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_8_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_6_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_5_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_4_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_3_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_2_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_1_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	CHANNEL_0_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9731. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 15 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
14	CHANNEL_14_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 14 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9731. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 13 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
12	CHANNEL_12_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 12 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
11	CHANNEL_11_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 11 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
10	CHANNEL_10_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 10 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
9	CHANNEL_9_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 9 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
8	CHANNEL_8_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 8 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
7	CHANNEL_7_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 7 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
6	CHANNEL_6_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 6 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
5	CHANNEL_5_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 5 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
4	CHANNEL_4_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 4 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
3	CHANNEL_3_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 3 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
2	CHANNEL_2_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 2 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
1	CHANNEL_1_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 1 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9731. AASRC_CFG_OUTPUT_FIFO_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CHANNEL_0_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Channel 0 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.12 AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Register

14.7.1.1.2.12.1 AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Register (Offset = 44h) [reset = 0h]

This register contains the raw interrupt status as defined in HL0.8 for the Input Group interrupts. The FIFO interrupt for each group is configured in the control register for the group. A read of the Interrupt Status Raw / Set Register returns the current pending status of the interrupt sources with no regard to any enable settings. A write to this register sets the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written. Note that reading this register immediately after writing to it would reflect old value instead of the written value; wait for 2 system clock cycles after writing to read written value.

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Table 14-9732. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0044h
AASRC1	02D4 0044h

Figure 14-4811. AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				GROUP_3_INPUT_FIFO_THRESHOLD_RAW	GROUP_2_INPUT_FIFO_THRESHOLD_RAW	GROUP_1_INPUT_FIFO_THRESHOLD_RAW	GROUP_0_INPUT_FIFO_THRESHOLD_RAW
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-9733. AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Always read as 0
3	GROUP_3_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Group 3 Input FIFO Threshold Interrupt Read indicates raw status. This fires when all the Input FIFOs for this Group is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
2	GROUP_2_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Group 2 Input FIFO Threshold Interrupt Read indicates raw status. This fires when all the the Input FIFOs for this Group is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9733. AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	GROUP_1_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Group 1 Input FIFO Threshold Interrupt Read indicates raw status. This fires when all the Input FIFOs for this Group is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
0	GROUP_0_INPUT_FIFO_THRESHOLD_RAW	R/W	0h	Group 0 Input FIFO Threshold Interrupt Read indicates raw status. This fires when all the Input FIFOs for this Group is below the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

14.7.1.1.2.13 AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Register

14.7.1.1.2.13.1 AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Register (Offset = 48h) [reset = 0h]

This register contains the enabled interrupt status as defined in HL0.8 for the Input Group. A read of the Interrupt Status Register returns the current pending status of the interrupt sources as masked by the current enable flag for each of those sources. A write to this register clears the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written

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Table 14-9734. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0048h
AASRC1	02D4 0048h

Figure 14-4812. AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				GROUP_3_INPUT_FIFO_THRESHOLD_ENABLED	GROUP_2_INPUT_FIFO_THRESHOLD_ENABLED	GROUP_1_INPUT_FIFO_THRESHOLD_ENABLED	GROUP_0_INPUT_FIFO_THRESHOLD_ENABLED
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9735. AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Always read as 0
3	GROUP_3_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Group 3 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when all the Input FIFOs for this Group is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
2	GROUP_2_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Group 2 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when all the Input FIFOs for this Group is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9735. AASRC_CFG_INPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	GROUP_1_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Group 1 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when all the Input FIFOs for this Group is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
0	GROUP_0_INPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Group 0 Input FIFO Threshold Interrupt Read indicates enabled status. This fires when all the Input FIFOs for this Group is below the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

14.7.1.1.2.14 AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Register

14.7.1.1.2.14.1 AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Register (Offset = 4Ch) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Input Group interrupts. The FIFO interrupt for each group is configured in the control register for the group. This register is used to read and set the interrupt source enables. The enable bit is active high and a 1 indicates the source is enabled to interrupt the processor(s), while a 0 indicates the source will not interrupt the processor(s).

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Table 14-9736. Instance Table

Instance Name	Physical Address
AASRC0	02D0 004Ch
AASRC1	02D4 004Ch

Figure 14-4813. AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				GROUP_3_INPUT_FIFO_THRESHOLD_ENABLE	GROUP_2_INPUT_FIFO_THRESHOLD_ENABLE	GROUP_1_INPUT_FIFO_THRESHOLD_ENABLE	GROUP_0_INPUT_FIFO_THRESHOLD_ENABLE
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9737. AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Always read as 0
3	GROUP_3_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Group 3 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
2	GROUP_2_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Group 2 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
1	GROUP_1_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Group 1 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9737. AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GROUP_0_INPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Group 10 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.15 AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Register

14.7.1.1.2.15.1 AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Register (Offset = 50h) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Input Group interrupts. The FIFO interrupt for each group is configured in the control register for the group. A read of the Interrupt Enable Clr register returns the current enable bits for the interrupt sources. A write to this register sets the enable to 0 for any source whose corresponding bit is 1 in the value written

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Table 14-9738. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0050h
AASRC1	02D4 0050h

Figure 14-4814. AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				GROUP_3_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	GROUP_2_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	GROUP_1_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	GROUP_0_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9739. AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Always read as 0
3	GROUP_3_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Group 3 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
2	GROUP_2_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Group 2 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
1	GROUP_1_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Group 1 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

Table 14-9739. AASRC_CFG_INPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GROUP_0_INPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Group 0 Input FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.16 AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Register

14.7.1.1.2.16.1 AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Register (Offset = 54h) [reset = 0h]

This register contains the raw interrupt status as defined in HL0.8 for the Output Group interrupts. The FIFO interrupt for each group is configured in the control register for the group. A read of the Interrupt Status Raw / Set Register returns the current pending status of the interrupt sources with no regard to any enable settings. A write to this register sets the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written. Note that reading this register immediately after writing to it would reflect old value instead of the written value; wait for 2 system clock cycles after writing to read written value.

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Table 14-9740. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0054h
AASRC1	02D4 0054h

Figure 14-4815. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				GROUP_3_OUTPUT_FIFO_THRESHOLD_RAW	GROUP_2_OUTPUT_FIFO_THRESHOLD_RAW	GROUP_1_OUTPUT_FIFO_THRESHOLD_RAW	GROUP_0_OUTPUT_FIFO_THRESHOLD_RAW
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-9741. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Always read as 0
3	GROUP_3_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Group 3 Output FIFO Threshold Interrupt Read indicates raw status. This fires when all the Output FIFOs for this Group is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
2	GROUP_2_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Group 2 Output FIFO Threshold Interrupt Read indicates raw status. This fires when all the the Output FIFOs for this Group is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9741. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	GROUP_1_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Group 1 Output FIFO Threshold Interrupt Read indicates raw status. This fires when all the Output FIFOs for this Group is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
0	GROUP_0_OUTPUT_FIFO_THRESHOLD_RAW	R/W	0h	Group 0 Output FIFO Threshold Interrupt Read indicates raw status. This fires when all the Output FIFOs for this Group is above the level set in the Configuration register. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

14.7.1.1.2.17 AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Register

14.7.1.1.2.17.1 AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Register (Offset = 58h) [reset = 0h]

This register contains the enabled interrupt status as defined in HL0.8 for the Output Group. A read of the Interrupt Status Register returns the current pending status of the interrupt sources as masked by the current enable flag for each of those sources. A write to this register clears the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written

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Table 14-9742. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0058h
AASRC1	02D4 0058h

Figure 14-4816. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				GROUP_3_OUTPUT_FIFO_THRESHOLD_ENABLED	GROUP_2_OUTPUT_FIFO_THRESHOLD_ENABLED	GROUP_1_OUTPUT_FIFO_THRESHOLD_ENABLED	GROUP_0_OUTPUT_FIFO_THRESHOLD_ENABLED
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9743. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Always read as 0
3	GROUP_3_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Group 3 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when all the Output FIFOs for this Group is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
2	GROUP_2_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Group 2 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when all the Output FIFOs for this Group is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9743. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	GROUP_1_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Group 1 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when all the Output FIFOs for this Group is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
0	GROUP_0_OUTPUT_FIFO_THRESHOLD_ENABLED	R/W1TC	0h	Group 0 Output FIFO Threshold Interrupt Read indicates enabled status. This fires when all the Output FIFOs for this Group is above the level set in the Configuration register. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

14.7.1.1.2.18 AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Register

14.7.1.1.2.18.1 AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Register (Offset = 5Ch) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Output Group interrupts. The FIFO interrupt for each group is configured in the control register for the group. This register is used to read and set the interrupt source enables. The enable bit is active high and a 1 indicates the source is enabled to interrupt the processor(s), while a 0 indicates the source will not interrupt the processor(s).

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Table 14-9744. Instance Table

Instance Name	Physical Address
AASRC0	02D0 005Ch
AASRC1	02D4 005Ch

Figure 14-4817. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				GROUP_3_OUTPUT_FIFO_THRESHOLD_ENABLE	GROUP_2_OUTPUT_FIFO_THRESHOLD_ENABLE	GROUP_1_OUTPUT_FIFO_THRESHOLD_ENABLE	GROUP_0_OUTPUT_FIFO_THRESHOLD_ENABLE
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-9745. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Always read as 0
3	GROUP_3_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Group 3 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
2	GROUP_2_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Group 2 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
1	GROUP_1_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Group 1 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9745. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GROUP_0_OUTPUT_FIFO_THRESHOLD_ENABLE	R/W1TS	0h	Group 10 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.19 AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Register

14.7.1.1.2.19.1 AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Register (Offset = 60h) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Output Group interrupts. The FIFO interrupt for each group is configured in the control register for the group. A read of the Interrupt Enable Clr register returns the current enable bits for the interrupt sources. A write to this register sets the enable to 0 for any source whose corresponding bit is 1 in the value written

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Table 14-9746. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0060h
AASRC1	02D4 0060h

Figure 14-4818. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				GROUP_3_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	GROUP_2_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	GROUP_1_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	GROUP_0_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-9747. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Always read as 0
3	GROUP_3_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Group 3 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
2	GROUP_2_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Group 2 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
1	GROUP_1_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Group 1 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9747. AASRC_CFG_OUTPUT_GROUP_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GROUP_0_OUTPUT_FIFO_THRESHOLD_ENABLE_CLEAR	R/W1TC	0h	Group 0 Output FIFO Threshold Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.20 AASRC_CFG_ERROR_INTERRUPT_STATUS_RAW_REGISTER Register

14.7.1.1.2.20.1 AASRC_CFG_ERROR_INTERRUPT_STATUS_RAW_REGISTER Register (Offset = 64h) [reset = 0h]

This register contains the raw interrupt status as defined in HL0.8 for the Error interrupts. A read of the Interrupt Status Raw / Set Register returns the current pending status of the interrupt sources with no regard to any enable settings. A write to this register sets the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written. Note that reading this register immediately after writing to it would reflect old value instead of the written value; wait for 2 system clock cycles after writing to read written value.

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Table 14-9748. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0064h
AASRC1	02D4 0064h

Figure 14-4819. AASRC_CFG_ERROR_INTERRUPT_STATUS_RAW_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_ERROR_RAW	CHANNEL_14_ERROR_RAW	CHANNEL_13_ERROR_RAW	CHANNEL_12_ERROR_RAW	CHANNEL_11_ERROR_RAW	CHANNEL_10_ERROR_RAW	CHANNEL_9_ERROR_RAW	CHANNEL_8_ERROR_RAW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_ERROR_RAW	CHANNEL_6_ERROR_RAW	CHANNEL_5_ERROR_RAW	CHANNEL_4_ERROR_RAW	CHANNEL_3_ERROR_RAW	CHANNEL_2_ERROR_RAW	CHANNEL_1_ERROR_RAW	CHANNEL_0_ERROR_RAW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9749. AASRC_CFG_ERROR_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_ERROR_RAW	R/W	0h	Channel 15 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active
14	CHANNEL_14_ERROR_RAW	R/W	0h	Channel 14 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 Status inactive 1 Status active

Table 14-9749. AASRC_CFG_ERROR_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_ERROR_RAW	R/W	0h	Channel 13 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
12	CHANNEL_12_ERROR_RAW	R/W	0h	Channel 12 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
11	CHANNEL_11_ERROR_RAW	R/W	0h	Channel 11 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
10	CHANNEL_10_ERROR_RAW	R/W	0h	Channel 10 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
9	CHANNEL_9_ERROR_RAW	R/W	0h	Channel 9 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
8	CHANNEL_8_ERROR_RAW	R/W	0h	Channel 8 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
7	CHANNEL_7_ERROR_RAW	R/W	0h	Channel 7 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
6	CHANNEL_6_ERROR_RAW	R/W	0h	Channel 6 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
5	CHANNEL_5_ERROR_RAW	R/W	0h	Channel 5 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
4	CHANNEL_4_ERROR_RAW	R/W	0h	Channel 4 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
3	CHANNEL_3_ERROR_RAW	R/W	0h	Channel 3 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

Table 14-9749. AASRC_CFG_ERROR_INTERRUPT_STATUS_RAW_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CHANNEL_2_ERROR_RAW	R/W	0h	Channel 2 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
1	CHANNEL_1_ERROR_RAW	R/W	0h	Channel 1 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
0	CHANNEL_0_ERROR_RAW	R/W	0h	Channel 0 FIFOs Error Interrupt Read indicates raw status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will set status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

14.7.1.1.2.21 AASRC_CFG_ERROR_INTERRUPT_STATUS_ENABLED_REGISTER Register

14.7.1.1.2.21.1 AASRC_CFG_ERROR_INTERRUPT_STATUS_ENABLED_REGISTER Register (Offset = 68h) [reset = 0h]

This register contains the enabled interrupt status as defined in HL0.8 for the Error for each Channel. A read of the Interrupt Status Register returns the current pending status of the interrupt sources as masked by the current enable flag for each of those sources. A write to this register clears the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written.

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Table 14-9750. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0068h
AASRC1	02D4 0068h

Figure 14-4820. AASRC_CFG_ERROR_INTERRUPT_STATUS_ENABLED_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_ERROR_ENABLED	CHANNEL_14_ERROR_ENABLED	CHANNEL_13_ERROR_ENABLED	CHANNEL_12_ERROR_ENABLED	CHANNEL_11_ERROR_ENABLED	CHANNEL_10_ERROR_ENABLED	CHANNEL_9_ERROR_ENABLED	CHANNEL_8_ERROR_ENABLED
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_ERROR_ENABLED	CHANNEL_6_ERROR_ENABLED	CHANNEL_5_ERROR_ENABLED	CHANNEL_4_ERROR_ENABLED	CHANNEL_3_ERROR_ENABLED	CHANNEL_2_ERROR_ENABLED	CHANNEL_1_ERROR_ENABLED	CHANNEL_0_ERROR_ENABLED
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9751. AASRC_CFG_ERROR_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_ERROR_ENABLED	R/W1TC	0h	Channel 15 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/ Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
14	CHANNEL_14_ERROR_ENABLED	R/W1TC	0h	Channel 14 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/ Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

Table 14-9751. AASRC_CFG_ERROR_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_ERROR_ENABLED	R/W1TC	0h	Channel 13 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/ Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
12	CHANNEL_12_ERROR_ENABLED	R/W1TC	0h	Channel 12 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/ Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
11	CHANNEL_11_ERROR_ENABLED	R/W1TC	0h	Channel 11 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/ Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
10	CHANNEL_10_ERROR_ENABLED	R/W1TC	0h	Channel 10 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/ Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
9	CHANNEL_9_ERROR_ENABLED	R/W1TC	0h	Channel 9 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
8	CHANNEL_8_ERROR_ENABLED	R/W1TC	0h	Channel 8 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
7	CHANNEL_7_ERROR_ENABLED	R/W1TC	0h	Channel 7 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
6	CHANNEL_6_ERROR_ENABLED	R/W1TC	0h	Channel 6 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
5	CHANNEL_5_ERROR_ENABLED	R/W1TC	0h	Channel 5 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
4	CHANNEL_4_ERROR_ENABLED	R/W1TC	0h	Channel 4 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`
3	CHANNEL_3_ERROR_ENABLED	R/W1TC	0h	Channel 3 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 `Status inactive` 1 `Status active`

Table 14-9751. AASRC_CFG_ERROR_INTERRUPT_STATUS_ENABLED_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CHANNEL_2_ERROR_ENABLED	R/W1TC	0h	Channel 2 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
1	CHANNEL_1_ERROR_ENABLED	R/W1TC	0h	Channel 1 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active
0	CHANNEL_0_ERROR_ENABLED	R/W1TC	0h	Channel 0 FIFOs Error Interrupt Read indicates enabled status. This fires when the FIFOs for this Channel isUnderflowed/Overflowed. Writing 1 will clear status and Writing 0 has no effect 0 Status inactive 1 Status active

14.7.1.1.2.22 AASRC_CFG_ERROR_INTERRUPT_ENABLE_SET_REGISTER Register

14.7.1.1.2.22.1 AASRC_CFG_ERROR_INTERRUPT_ENABLE_SET_REGISTER Register (Offset = 6Ch) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Error interrupts. The FIFO interrupt for each Channel is configured in the control register for the Channel. This register is used to read and set the interrupt source enables. The enable bit is active high and a 1 indicates the source is enabled to interrupt the processor(s), while a 0 indicates the source will not interrupt the processor(s).

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Table 14-9752. Instance Table

Instance Name	Physical Address
AASRC0	02D0 006Ch
AASRC1	02D4 006Ch

Figure 14-4821. AASRC_CFG_ERROR_INTERRUPT_ENABLE_SET_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_ERROR_ENABLE	CHANNEL_14_ERROR_ENABLE	CHANNEL_13_ERROR_ENABLE	CHANNEL_12_ERROR_ENABLE	CHANNEL_11_ERROR_ENABLE	CHANNEL_10_ERROR_ENABLE	CHANNEL_9_ERROR_ENABLE	CHANNEL_8_ERROR_ENABLE
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_ERROR_ENABLE	CHANNEL_6_ERROR_ENABLE	CHANNEL_5_ERROR_ENABLE	CHANNEL_4_ERROR_ENABLE	CHANNEL_3_ERROR_ENABLE	CHANNEL_2_ERROR_ENABLE	CHANNEL_1_ERROR_ENABLE	CHANNEL_0_ERROR_ENABLE
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9753. AASRC_CFG_ERROR_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_ERROR_ENABLE	R/W1TS	0h	Channel 15 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
14	CHANNEL_14_ERROR_ENABLE	R/W1TS	0h	Channel 14 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
13	CHANNEL_13_ERROR_ENABLE	R/W1TS	0h	Channel 13 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9753. AASRC_CFG_ERROR_INTERRUPT_ENABLE_SET_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CHANNEL_12_ERROR_ENABLE	R/W1TS	0h	Channel 12 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
11	CHANNEL_11_ERROR_ENABLE	R/W1TS	0h	Channel 11 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
10	CHANNEL_10_ERROR_ENABLE	R/W1TS	0h	Channel 10 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
9	CHANNEL_9_ERROR_ENABLE	R/W1TS	0h	Channel 9 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
8	CHANNEL_8_ERROR_ENABLE	R/W1TS	0h	Channel 8 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
7	CHANNEL_7_ERROR_ENABLE	R/W1TS	0h	Channel 7 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
6	CHANNEL_6_ERROR_ENABLE	R/W1TS	0h	Channel 6 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
5	CHANNEL_5_ERROR_ENABLE	R/W1TS	0h	Channel 5 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
4	CHANNEL_4_ERROR_ENABLE	R/W1TS	0h	Channel 4 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
3	CHANNEL_3_ERROR_ENABLE	R/W1TS	0h	Channel 3 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
2	CHANNEL_2_ERROR_ENABLE	R/W1TS	0h	Channel 2 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
1	CHANNEL_1_ERROR_ENABLE	R/W1TS	0h	Channel 1 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`
0	CHANNEL_0_ERROR_ENABLE	R/W1TS	0h	Channel 10 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will set enable and Writing 0 has no effect 0 `Interrupt is not enabled` 1 `Interrupt is enabled`

14.7.1.1.2.23 AASRC_CFG_ERROR_INTERRUPT_ENABLE_CLEAR_REGISTER Register

14.7.1.1.2.23.1 AASRC_CFG_ERROR_INTERRUPT_ENABLE_CLEAR_REGISTER Register (Offset = 70h) [reset = 0h]

This register contains the enable interrupt status as defined in HL0.8 for the Error interrupts. The FIFO interrupt for each Channel is configured in the control register for the Channel. A read of the Interrupt Enable Clr register returns the current enable bits for the interrupt sources. A write to this register sets the enable to 0 for any source whose corresponding bit is 1 in the value written

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Table 14-9754. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0070h
AASRC1	02D4 0070h

Figure 14-4822. AASRC_CFG_ERROR_INTERRUPT_ENABLE_CLEAR_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
CHANNEL_15_ERROR_ENABLE_CLEAR	CHANNEL_14_ERROR_ENABLE_CLEAR	CHANNEL_13_ERROR_ENABLE_CLEAR	CHANNEL_12_ERROR_ENABLE_CLEAR	CHANNEL_11_ERROR_ENABLE_CLEAR	CHANNEL_10_ERROR_ENABLE_CLEAR	CHANNEL_9_ERROR_ENABLE_CLEAR	CHANNEL_8_ERROR_ENABLE_CLEAR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
CHANNEL_7_ERROR_ENABLE_CLEAR	CHANNEL_6_ERROR_ENABLE_CLEAR	CHANNEL_5_ERROR_ENABLE_CLEAR	CHANNEL_4_ERROR_ENABLE_CLEAR	CHANNEL_3_ERROR_ENABLE_CLEAR	CHANNEL_2_ERROR_ENABLE_CLEAR	CHANNEL_1_ERROR_ENABLE_CLEAR	CHANNEL_0_ERROR_ENABLE_CLEAR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9755. AASRC_CFG_ERROR_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 15 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
14	CHANNEL_14_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 14 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
13	CHANNEL_13_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 13 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

Table 14-9755. AASRC_CFG_ERROR_INTERRUPT_ENABLE_CLEAR_REGISTER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CHANNEL_12_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 12 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
11	CHANNEL_11_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 11 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
10	CHANNEL_10_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 10 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
9	CHANNEL_9_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 9 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
8	CHANNEL_8_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 8 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
7	CHANNEL_7_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 7 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
6	CHANNEL_6_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 6 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
5	CHANNEL_5_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 5 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
4	CHANNEL_4_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 4 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
3	CHANNEL_3_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 3 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
2	CHANNEL_2_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 2 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
1	CHANNEL_1_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 1 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled
0	CHANNEL_0_ERROR_ENABLE_CLEAR	R/W1TC	0h	Channel 0 FIFOs Error Interrupt Read indicates interrupt enable. Writing 1 will clear enable and Writing 0 has no effect 0 Interrupt is not enabled 1 Interrupt is enabled

14.7.1.1.2.24 AASRC_CFG_INPUT_GROUP_0_SELECT Register

14.7.1.1.2.24.1 AASRC_CFG_INPUT_GROUP_0_SELECT Register (Offset = 74h) [reset = 0h]

This register selects which channel make up the input group 0. This is used for group event generation and group mode settings

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Table 14-9756. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0074h
AASRC1	02D4 0074h

Figure 14-4823. AASRC_CFG_INPUT_GROUP_0_SELECT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_GROUP_ENABLE	CHANNEL_14_GROUP_ENABLE	CHANNEL_13_GROUP_ENABLE	CHANNEL_12_GROUP_ENABLE	CHANNEL_11_GROUP_ENABLE	CHANNEL_10_GROUP_ENABLE	CHANNEL_9_GROUP_ENABLE	CHANNEL_8_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_GROUP_ENABLE	CHANNEL_6_GROUP_ENABLE	CHANNEL_5_GROUP_ENABLE	CHANNEL_4_GROUP_ENABLE	CHANNEL_3_GROUP_ENABLE	CHANNEL_2_GROUP_ENABLE	CHANNEL_1_GROUP_ENABLE	CHANNEL_0_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9757. AASRC_CFG_INPUT_GROUP_0_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_GROUP_ENABLE	R/W	0h	Input Channel 15 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
14	CHANNEL_14_GROUP_ENABLE	R/W	0h	Input Channel 14 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

Table 14-9757. AASRC_CFG_INPUT_GROUP_0_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_GROUP_ENABLE	R/W	0h	Input Channel 13 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
12	CHANNEL_12_GROUP_ENABLE	R/W	0h	Input Channel 12 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
11	CHANNEL_11_GROUP_ENABLE	R/W	0h	Input Channel 11 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
10	CHANNEL_10_GROUP_ENABLE	R/W	0h	Input Channel 10 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
9	CHANNEL_9_GROUP_ENABLE	R/W	0h	Input Channel 9 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
8	CHANNEL_8_GROUP_ENABLE	R/W	0h	Input Channel 8 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
7	CHANNEL_7_GROUP_ENABLE	R/W	0h	Input Channel 7 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
6	CHANNEL_6_GROUP_ENABLE	R/W	0h	Input Channel 6 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

Table 14-9757. AASRC_CFG_INPUT_GROUP_0_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_GROUP_ENABLE	R/W	0h	Input Channel 5 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
4	CHANNEL_4_GROUP_ENABLE	R/W	0h	Input Channel 4 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
3	CHANNEL_3_GROUP_ENABLE	R/W	0h	Input Channel 3 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
2	CHANNEL_2_GROUP_ENABLE	R/W	0h	Input Channel 2 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
1	CHANNEL_1_GROUP_ENABLE	R/W	0h	Input Channel 1 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
0	CHANNEL_0_GROUP_ENABLE	R/W	0h	Input Channel 0 Group Enable indicates if the Input Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

14.7.1.1.2.25 AASRC_CFG_INPUT_GROUP_1_SELECT Register

14.7.1.1.2.25.1 AASRC_CFG_INPUT_GROUP_1_SELECT Register (Offset = 78h) [reset = 0h]

This register selects which channel make up the input group 1. This is used for group event generation and group mode settings

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Table 14-9758. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0078h
AASRC1	02D4 0078h

Figure 14-4824. AASRC_CFG_INPUT_GROUP_1_SELECT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_GROUP_ENABLE	CHANNEL_14_GROUP_ENABLE	CHANNEL_13_GROUP_ENABLE	CHANNEL_12_GROUP_ENABLE	CHANNEL_11_GROUP_ENABLE	CHANNEL_10_GROUP_ENABLE	CHANNEL_9_GROUP_ENABLE	CHANNEL_8_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_GROUP_ENABLE	CHANNEL_6_GROUP_ENABLE	CHANNEL_5_GROUP_ENABLE	CHANNEL_4_GROUP_ENABLE	CHANNEL_3_GROUP_ENABLE	CHANNEL_2_GROUP_ENABLE	CHANNEL_1_GROUP_ENABLE	CHANNEL_0_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9759. AASRC_CFG_INPUT_GROUP_1_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0

15	CHANNEL_15_GROUP_ENABLE	R/W	0h	Input Channel 15 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable
				`0 This channel is not part of this group`
				`1 This channel is part of this group`

14	CHANNEL_14_GROUP_ENABLE	R/W	0h	Input Channel 14 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable
				`0 This channel is not part of this group`
				`1 This channel is part of this group`

Table 14-9759. AASRC_CFG_INPUT_GROUP_1_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_GROUP_ENABLE	R/W	0h	Input Channel 13 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
12	CHANNEL_12_GROUP_ENABLE	R/W	0h	Input Channel 12 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
11	CHANNEL_11_GROUP_ENABLE	R/W	0h	Input Channel 11 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
10	CHANNEL_10_GROUP_ENABLE	R/W	0h	Input Channel 10 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
9	CHANNEL_9_GROUP_ENABLE	R/W	0h	Input Channel 9 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
8	CHANNEL_8_GROUP_ENABLE	R/W	0h	Input Channel 8 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
7	CHANNEL_7_GROUP_ENABLE	R/W	0h	Input Channel 7 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
6	CHANNEL_6_GROUP_ENABLE	R/W	0h	Input Channel 6 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9759. AASRC_CFG_INPUT_GROUP_1_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_GROUP_ENABLE	R/W	0h	Input Channel 5 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
4	CHANNEL_4_GROUP_ENABLE	R/W	0h	Input Channel 4 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
3	CHANNEL_3_GROUP_ENABLE	R/W	0h	Input Channel 3 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
2	CHANNEL_2_GROUP_ENABLE	R/W	0h	Input Channel 2 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
1	CHANNEL_1_GROUP_ENABLE	R/W	0h	Input Channel 1 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
0	CHANNEL_0_GROUP_ENABLE	R/W	0h	Input Channel 0 Group Enable indicates if the Input Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

14.7.1.1.2.26 AASRC_CFG_INPUT_GROUP_2_SELECT Register

14.7.1.1.2.26.1 AASRC_CFG_INPUT_GROUP_2_SELECT Register (Offset = 7Ch) [reset = 0h]

This register selects which channel make up the input group 2. This is used for group event generation and group mode settings.

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Table 14-9760. Instance Table

Instance Name	Physical Address
AASRC0	02D0 007Ch
AASRC1	02D4 007Ch

Figure 14-4825. AASRC_CFG_INPUT_GROUP_2_SELECT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_GROUP_ENABLE	CHANNEL_14_GROUP_ENABLE	CHANNEL_13_GROUP_ENABLE	CHANNEL_12_GROUP_ENABLE	CHANNEL_11_GROUP_ENABLE	CHANNEL_10_GROUP_ENABLE	CHANNEL_9_GROUP_ENABLE	CHANNEL_8_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_GROUP_ENABLE	CHANNEL_6_GROUP_ENABLE	CHANNEL_5_GROUP_ENABLE	CHANNEL_4_GROUP_ENABLE	CHANNEL_3_GROUP_ENABLE	CHANNEL_2_GROUP_ENABLE	CHANNEL_1_GROUP_ENABLE	CHANNEL_0_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9761. AASRC_CFG_INPUT_GROUP_2_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_GROUP_ENABLE	R/W	0h	Input Channel 15 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
14	CHANNEL_14_GROUP_ENABLE	R/W	0h	Input Channel 14 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9761. AASRC_CFG_INPUT_GROUP_2_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_GROUP_ENABLE	R/W	0h	Input Channel 13 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
12	CHANNEL_12_GROUP_ENABLE	R/W	0h	Input Channel 12 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
11	CHANNEL_11_GROUP_ENABLE	R/W	0h	Input Channel 11 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
10	CHANNEL_10_GROUP_ENABLE	R/W	0h	Input Channel 10 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
9	CHANNEL_9_GROUP_ENABLE	R/W	0h	Input Channel 9 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
8	CHANNEL_8_GROUP_ENABLE	R/W	0h	Input Channel 8 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
7	CHANNEL_7_GROUP_ENABLE	R/W	0h	Input Channel 7 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
6	CHANNEL_6_GROUP_ENABLE	R/W	0h	Input Channel 6 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9761. AASRC_CFG_INPUT_GROUP_2_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_GROUP_ENABLE	R/W	0h	Input Channel 5 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
4	CHANNEL_4_GROUP_ENABLE	R/W	0h	Input Channel 4 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
3	CHANNEL_3_GROUP_ENABLE	R/W	0h	Input Channel 3 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
2	CHANNEL_2_GROUP_ENABLE	R/W	0h	Input Channel 2 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
1	CHANNEL_1_GROUP_ENABLE	R/W	0h	Input Channel 1 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
0	CHANNEL_0_GROUP_ENABLE	R/W	0h	Input Channel 0 Group Enable indicates if the Input Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

14.7.1.1.2.27 AASRC_CFG_INPUT_GROUP_3_SELECT Register

14.7.1.1.2.27.1 AASRC_CFG_INPUT_GROUP_3_SELECT Register (Offset = 80h) [reset = 0h]

This register selects which channel make up the input group 3. This is used for group event generation and group mode settings.

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Table 14-9762. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0080h
AASRC1	02D4 0080h

Figure 14-4826. AASRC_CFG_INPUT_GROUP_3_SELECT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_GROUP_ENABLE	CHANNEL_14_GROUP_ENABLE	CHANNEL_13_GROUP_ENABLE	CHANNEL_12_GROUP_ENABLE	CHANNEL_11_GROUP_ENABLE	CHANNEL_10_GROUP_ENABLE	CHANNEL_9_GROUP_ENABLE	CHANNEL_8_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_GROUP_ENABLE	CHANNEL_6_GROUP_ENABLE	CHANNEL_5_GROUP_ENABLE	CHANNEL_4_GROUP_ENABLE	CHANNEL_3_GROUP_ENABLE	CHANNEL_2_GROUP_ENABLE	CHANNEL_1_GROUP_ENABLE	CHANNEL_0_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9763. AASRC_CFG_INPUT_GROUP_3_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_GROUP_ENABLE	R/W	0h	Input Channel 15 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
14	CHANNEL_14_GROUP_ENABLE	R/W	0h	Input Channel 14 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

Table 14-9763. AASRC_CFG_INPUT_GROUP_3_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_GROUP_ENABLE	R/W	0h	Input Channel 13 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
12	CHANNEL_12_GROUP_ENABLE	R/W	0h	Input Channel 12 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
11	CHANNEL_11_GROUP_ENABLE	R/W	0h	Input Channel 11 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
10	CHANNEL_10_GROUP_ENABLE	R/W	0h	Input Channel 10 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
9	CHANNEL_9_GROUP_ENABLE	R/W	0h	Input Channel 9 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
8	CHANNEL_8_GROUP_ENABLE	R/W	0h	Input Channel 8 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
7	CHANNEL_7_GROUP_ENABLE	R/W	0h	Input Channel 7 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
6	CHANNEL_6_GROUP_ENABLE	R/W	0h	Input Channel 6 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

Table 14-9763. AASRC_CFG_INPUT_GROUP_3_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_GROUP_ENABLE	R/W	0h	Input Channel 5 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
4	CHANNEL_4_GROUP_ENABLE	R/W	0h	Input Channel 4 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
3	CHANNEL_3_GROUP_ENABLE	R/W	0h	Input Channel 3 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
2	CHANNEL_2_GROUP_ENABLE	R/W	0h	Input Channel 2 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
1	CHANNEL_1_GROUP_ENABLE	R/W	0h	Input Channel 1 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
0	CHANNEL_0_GROUP_ENABLE	R/W	0h	Input Channel 0 Group Enable indicates if the Input Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Input Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

14.7.1.1.2.28 AASRC_CFG_OUTPUT_GROUP_0_SELECT Register

14.7.1.1.2.28.1 AASRC_CFG_OUTPUT_GROUP_0_SELECT Register (Offset = 94h) [reset = 0h]

This register selects which channel make up the Output group 0. This is used for group event generation and group mode settings.

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Table 14-9764. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0094h
AASRC1	02D4 0094h

Figure 14-4827. AASRC_CFG_OUTPUT_GROUP_0_SELECT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_GROUP_ENABLE	CHANNEL_14_GROUP_ENABLE	CHANNEL_13_GROUP_ENABLE	CHANNEL_12_GROUP_ENABLE	CHANNEL_11_GROUP_ENABLE	CHANNEL_10_GROUP_ENABLE	CHANNEL_9_GROUP_ENABLE	CHANNEL_8_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_GROUP_ENABLE	CHANNEL_6_GROUP_ENABLE	CHANNEL_5_GROUP_ENABLE	CHANNEL_4_GROUP_ENABLE	CHANNEL_3_GROUP_ENABLE	CHANNEL_2_GROUP_ENABLE	CHANNEL_1_GROUP_ENABLE	CHANNEL_0_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9765. AASRC_CFG_OUTPUT_GROUP_0_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_GROUP_ENABLE	R/W	0h	Output Channel 15 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
14	CHANNEL_14_GROUP_ENABLE	R/W	0h	Output Channel 14 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9765. AASRC_CFG_OUTPUT_GROUP_0_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_GROUP_ENABLE	R/W	0h	Output Channel 13 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
12	CHANNEL_12_GROUP_ENABLE	R/W	0h	Output Channel 12 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
11	CHANNEL_11_GROUP_ENABLE	R/W	0h	Output Channel 11 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
10	CHANNEL_10_GROUP_ENABLE	R/W	0h	Output Channel 10 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
9	CHANNEL_9_GROUP_ENABLE	R/W	0h	Output Channel 9 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
8	CHANNEL_8_GROUP_ENABLE	R/W	0h	Output Channel 8 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
7	CHANNEL_7_GROUP_ENABLE	R/W	0h	Output Channel 7 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
6	CHANNEL_6_GROUP_ENABLE	R/W	0h	Output Channel 6 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9765. AASRC_CFG_OUTPUT_GROUP_0_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_GROUP_ENABLE	R/W	0h	Output Channel 5 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
4	CHANNEL_4_GROUP_ENABLE	R/W	0h	Output Channel 4 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
3	CHANNEL_3_GROUP_ENABLE	R/W	0h	Output Channel 3 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
2	CHANNEL_2_GROUP_ENABLE	R/W	0h	Output Channel 2 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
1	CHANNEL_1_GROUP_ENABLE	R/W	0h	Output Channel 1 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
0	CHANNEL_0_GROUP_ENABLE	R/W	0h	Output Channel 0 Group Enable indicates if the Output Channel is part of the group0 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

14.7.1.1.2.29 AASRC_CFG_OUTPUT_GROUP_1_SELECT Register

14.7.1.1.2.29.1 AASRC_CFG_OUTPUT_GROUP_1_SELECT Register (Offset = 98h) [reset = 0h]

This register selects which channel make up the Output group 1. This is used for group event generation and group mode settings

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Table 14-9766. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0098h
AASRC1	02D4 0098h

Figure 14-4828. AASRC_CFG_OUTPUT_GROUP_1_SELECT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_GROUP_ENABLE	CHANNEL_14_GROUP_ENABLE	CHANNEL_13_GROUP_ENABLE	CHANNEL_12_GROUP_ENABLE	CHANNEL_11_GROUP_ENABLE	CHANNEL_10_GROUP_ENABLE	CHANNEL_9_GROUP_ENABLE	CHANNEL_8_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_GROUP_ENABLE	CHANNEL_6_GROUP_ENABLE	CHANNEL_5_GROUP_ENABLE	CHANNEL_4_GROUP_ENABLE	CHANNEL_3_GROUP_ENABLE	CHANNEL_2_GROUP_ENABLE	CHANNEL_1_GROUP_ENABLE	CHANNEL_0_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9767. AASRC_CFG_OUTPUT_GROUP_1_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15	CHANNEL_15_GROUP_ENABLE	R/W	0h	Output Channel 15 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
14	CHANNEL_14_GROUP_ENABLE	R/W	0h	Output Channel 14 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9767. AASRC_CFG_OUTPUT_GROUP_1_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_GROUP_ENABLE	R/W	0h	Output Channel 13 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
12	CHANNEL_12_GROUP_ENABLE	R/W	0h	Output Channel 12 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
11	CHANNEL_11_GROUP_ENABLE	R/W	0h	Output Channel 11 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
10	CHANNEL_10_GROUP_ENABLE	R/W	0h	Output Channel 10 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
9	CHANNEL_9_GROUP_ENABLE	R/W	0h	Output Channel 9 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
8	CHANNEL_8_GROUP_ENABLE	R/W	0h	Output Channel 8 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
7	CHANNEL_7_GROUP_ENABLE	R/W	0h	Output Channel 7 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
6	CHANNEL_6_GROUP_ENABLE	R/W	0h	Output Channel 6 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9767. AASRC_CFG_OUTPUT_GROUP_1_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_GROUP_ENABLE	R/W	0h	Output Channel 5 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
4	CHANNEL_4_GROUP_ENABLE	R/W	0h	Output Channel 4 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
3	CHANNEL_3_GROUP_ENABLE	R/W	0h	Output Channel 3 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
2	CHANNEL_2_GROUP_ENABLE	R/W	0h	Output Channel 2 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
1	CHANNEL_1_GROUP_ENABLE	R/W	0h	Output Channel 1 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
0	CHANNEL_0_GROUP_ENABLE	R/W	0h	Output Channel 0 Group Enable indicates if the Output Channel is part of the group1 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

14.7.1.1.2.30 AASRC_CFG_OUTPUT_GROUP_2_SELECT Register

14.7.1.1.2.30.1 AASRC_CFG_OUTPUT_GROUP_2_SELECT Register (Offset = 9Ch) [reset = 0h]

This register selects which channel make up the Output group 2. This is used for group event generation and group mode settings

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Table 14-9768. Instance Table

Instance Name	Physical Address
AASRC0	02D0 009Ch
AASRC1	02D4 009Ch

Figure 14-4829. AASRC_CFG_OUTPUT_GROUP_2_SELECT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_GROUP_ENABLE	CHANNEL_14_GROUP_ENABLE	CHANNEL_13_GROUP_ENABLE	CHANNEL_12_GROUP_ENABLE	CHANNEL_11_GROUP_ENABLE	CHANNEL_10_GROUP_ENABLE	CHANNEL_9_GROUP_ENABLE	CHANNEL_8_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_GROUP_ENABLE	CHANNEL_6_GROUP_ENABLE	CHANNEL_5_GROUP_ENABLE	CHANNEL_4_GROUP_ENABLE	CHANNEL_3_GROUP_ENABLE	CHANNEL_2_GROUP_ENABLE	CHANNEL_1_GROUP_ENABLE	CHANNEL_0_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9769. AASRC_CFG_OUTPUT_GROUP_2_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0

15	CHANNEL_15_GROUP_ENABLE	R/W	0h	Output Channel 15 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable
				`0 This channel is not part of this group`
				`1 This channel is part of this group`

14	CHANNEL_14_GROUP_ENABLE	R/W	0h	Output Channel 14 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable
				`0 This channel is not part of this group`
				`1 This channel is part of this group`

Table 14-9769. AASRC_CFG_OUTPUT_GROUP_2_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_GROUP_ENABLE	R/W	0h	Output Channel 13 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
12	CHANNEL_12_GROUP_ENABLE	R/W	0h	Output Channel 12 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
11	CHANNEL_11_GROUP_ENABLE	R/W	0h	Output Channel 11 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
10	CHANNEL_10_GROUP_ENABLE	R/W	0h	Output Channel 10 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
9	CHANNEL_9_GROUP_ENABLE	R/W	0h	Output Channel 9 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
8	CHANNEL_8_GROUP_ENABLE	R/W	0h	Output Channel 8 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
7	CHANNEL_7_GROUP_ENABLE	R/W	0h	Output Channel 7 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
6	CHANNEL_6_GROUP_ENABLE	R/W	0h	Output Channel 6 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9769. AASRC_CFG_OUTPUT_GROUP_2_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_GROUP_ENABLE	R/W	0h	Output Channel 5 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
4	CHANNEL_4_GROUP_ENABLE	R/W	0h	Output Channel 4 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
3	CHANNEL_3_GROUP_ENABLE	R/W	0h	Output Channel 3 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
2	CHANNEL_2_GROUP_ENABLE	R/W	0h	Output Channel 2 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
1	CHANNEL_1_GROUP_ENABLE	R/W	0h	Output Channel 1 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
0	CHANNEL_0_GROUP_ENABLE	R/W	0h	Output Channel 0 Group Enable indicates if the Output Channel is part of the group2 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

14.7.1.1.2.31 AASRC_CFG_OUTPUT_GROUP_3_SELECT Register

14.7.1.1.2.31.1 AASRC_CFG_OUTPUT_GROUP_3_SELECT Register (Offset = A0h) [reset = 0h]

This register selects which channel make up the Output group 3. This is used for group event generation and group mode settings.

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Table 14-9770. Instance Table

Instance Name	Physical Address
AASRC0	02D0 00A0h
AASRC1	02D4 00A0h

Figure 14-4830. AASRC_CFG_OUTPUT_GROUP_3_SELECT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CHANNEL_15_GROUP_ENABLE	CHANNEL_14_GROUP_ENABLE	CHANNEL_13_GROUP_ENABLE	CHANNEL_12_GROUP_ENABLE	CHANNEL_11_GROUP_ENABLE	CHANNEL_10_GROUP_ENABLE	CHANNEL_9_GROUP_ENABLE	CHANNEL_8_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CHANNEL_7_GROUP_ENABLE	CHANNEL_6_GROUP_ENABLE	CHANNEL_5_GROUP_ENABLE	CHANNEL_4_GROUP_ENABLE	CHANNEL_3_GROUP_ENABLE	CHANNEL_2_GROUP_ENABLE	CHANNEL_1_GROUP_ENABLE	CHANNEL_0_GROUP_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-9771. AASRC_CFG_OUTPUT_GROUP_3_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0

15	CHANNEL_15_GROUP_ENABLE	R/W	0h	Output Channel 15 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable
				`0 This channel is not part of this group`
				`1 This channel is part of this group`

14	CHANNEL_14_GROUP_ENABLE	R/W	0h	Output Channel 14 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable
				`0 This channel is not part of this group`
				`1 This channel is part of this group`

Table 14-9771. AASRC_CFG_OUTPUT_GROUP_3_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CHANNEL_13_GROUP_ENABLE	R/W	0h	Output Channel 13 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
12	CHANNEL_12_GROUP_ENABLE	R/W	0h	Output Channel 12 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
11	CHANNEL_11_GROUP_ENABLE	R/W	0h	Output Channel 11 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
10	CHANNEL_10_GROUP_ENABLE	R/W	0h	Output Channel 10 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
9	CHANNEL_9_GROUP_ENABLE	R/W	0h	Output Channel 9 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
8	CHANNEL_8_GROUP_ENABLE	R/W	0h	Output Channel 8 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
7	CHANNEL_7_GROUP_ENABLE	R/W	0h	Output Channel 7 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group
6	CHANNEL_6_GROUP_ENABLE	R/W	0h	Output Channel 6 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 This channel is not part of this group 1 This channel is part of this group

Table 14-9771. AASRC_CFG_OUTPUT_GROUP_3_SELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHANNEL_5_GROUP_ENABLE	R/W	0h	Output Channel 5 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
4	CHANNEL_4_GROUP_ENABLE	R/W	0h	Output Channel 4 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
3	CHANNEL_3_GROUP_ENABLE	R/W	0h	Output Channel 3 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
2	CHANNEL_2_GROUP_ENABLE	R/W	0h	Output Channel 2 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
1	CHANNEL_1_GROUP_ENABLE	R/W	0h	Output Channel 1 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`
0	CHANNEL_0_GROUP_ENABLE	R/W	0h	Output Channel 0 Group Enable indicates if the Output Channel is part of the group3 for the group settings and interrupt event generation If this bit is set then the group event and interrupt will not fire until the threshold condition for this Output Channel is met. Writing 1 will enable and Writing 0 will disable 0 `This channel is not part of this group` 1 `This channel is part of this group`

14.7.1.1.2.32 AASRC_CFG_SRC_FIFO_CONTROL_0 Register

14.7.1.1.2.32.1 AASRC_CFG_SRC_FIFO_CONTROL_0 Register (Offset = 100h) [reset = 10001h]

This is where the SRC0 FIFOs are configured

Return to Summary Table

Table 14-9772. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0100h
AASRC1	02D4 0100h

Figure 14-4831. AASRC_CFG_SRC_FIFO_CONTROL_0 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9773. AASRC_CFG_SRC_FIFO_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC0 is underflowed 0 No underflow is detected 1 Underflow is detected
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC0 is underflowed 0 No underflow is detected 1 Underflow is detected
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC0 is overflowed 0 No overflow is detected 1 Overflow is detected
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC0 is overflowed 0 No overflow is detected 1 Overflow is detected

Table 14-9773. AASRC_CFG_SRC_FIFO_CONTROL_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC0 OUTFIFOs event to fire 1-32: 1-32 samples
15:12	RESERVED1	R	0h	Reserved
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC0 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC0 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC0 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC0 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC0 INFIFOs event to fire 1-32: 1-32 samples

14.7.1.1.2.33 AASRC_CFG_SRC_CONTROL_0 Register

14.7.1.1.2.33.1 AASRC_CFG_SRC_CONTROL_0 Register (Offset = 104h) [reset = 0h]

This is where the SRC0 filter is configured

Return to Summary Table

Table 14-9774. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0104h
AASRC1	02D4 0104h

Figure 14-4832. AASRC_CFG_SRC_CONTROL_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">CHANNEL_ENABLE</td><td colspan="2">OUTPUT_WORD_LENGTH</td><td colspan="2">GROUP_DELAY</td><td colspan="2">DE_EMPHASIS_MODE</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ATTENUATION</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>DIRECT_DOWN_SAMPLE</td><td>MUTE</td><td>DITHER_ENABLE</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">INPUT_WORD_LENGTH</td><td colspan="3">OUTPUT_CLOCK_ZONE_SELECT</td><td colspan="3">INPUT_CLOCK_ZONE_SELECT</td></tr>
<tr><td colspan="2">R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-9775. AASRC_CFG_SRC_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of SRC0 The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9775. AASRC_CFG_SRC_CONTROL_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 Decimation Filter 1 Direct Down Sampling
9	MUTE	R/W	0h	This bit enables or disables the SRC output soft mute function; output data set to all zeros 0 Mute disabled 1 Mute enabled
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the SRC filters dithering 0 Dithering disabled 1 Dithering enabled
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.34 AASRC_CFG_SRC_STATUS_0 Register

14.7.1.1.2.34.1 AASRC_CFG_SRC_STATUS_0 Register (Offset = 108h) [reset = 0h]

This is where the SRC0 filter status is checked

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Table 14-9776. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0108h
AASRC1	02D4 0108h

Figure 14-4833. AASRC_CFG_SRC_STATUS_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							UPSAMPLE
R							R
0h							0h
15	14	13	12	11	10	9	8
RATE_RATIO							
R							
0h							
7	6	5	4	3	2	1	0
RATE_RATIO							
R							
0h							

Table 14-9777. AASRC_CFG_SRC_STATUS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	UPSAMPLE	R	0h	This signal becomes high when Output sampling rate is greater than Input sampling rate 0 `Output sampling rate < Input sampling rate` 1 `Output sampling rate > Input sampling rate`
15:0	RATE_RATIO	R	0h	Input to Output sampling ratio for SRC0

14.7.1.1.2.35 AASRC_CFG_SRC_FIFO_CONTROL_1 Register

14.7.1.1.2.35.1 AASRC_CFG_SRC_FIFO_CONTROL_1 Register (Offset = 110h) [reset = 10001h]

This is where the SRC1 FIFOs are configured

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Table 14-9778. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0110h
AASRC1	02D4 0110h

Figure 14-4834. AASRC_CFG_SRC_FIFO_CONTROL_1 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9779. AASRC_CFG_SRC_FIFO_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0

27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC1 is underflowed
				`0 No underflow is detected`
				`1 Underflow is detected`

26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC1 is underflowed
				`0 No underflow is detected`
				`1 Underflow is detected`

25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC1 is overflowed
				`0 No overflow is detected`
				`1 Overflow is detected`

24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC1 is overflowed
				`0 No overflow is detected`
				`1 Overflow is detected`

Table 14-9779. AASRC_CFG_SRC_FIFO_CONTROL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC1 OUTFIFOs event to fire 1-32: 1-32 samples
15:12	RESERVED1	R	0h	Reserved
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC1 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC1 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC1 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC1 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC1 INFIFOs event to fire 1-32: 1-32 samples

14.7.1.1.2.36 AASRC_CFG_SRC_CONTROL_1 Register

14.7.1.1.2.36.1 AASRC_CFG_SRC_CONTROL_1 Register (Offset = 114h) [reset = 0h]

This is where the SRC1 filter is configured

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Table 14-9780. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0114h
AASRC1	02D4 0114h

Figure 14-4835. AASRC_CFG_SRC_CONTROL_1 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	22	21	20	19	18	17	16
ATTENUATION							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9781. AASRC_CFG_SRC_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of SRC1 The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC1 output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9781. AASRC_CFG_SRC_CONTROL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing
				`0 Decimation Filter`
				`1 Direct Down Sampling`

9	MUTE	R/W	0h	This bit enables or disables the SRC output soft mute function; output data set to all zeros
				`0 Mute disabled`
				`1 Mute enabled`

8	DITHER_ENABLE	R/W	0h	This bit enables or disables the SRC filters dithering
				`0 Dithering disabled`
				`1 Dithering enabled`

7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.37 AASRC_CFG_SRC_STATUS_1 Register

14.7.1.1.2.37.1 AASRC_CFG_SRC_STATUS_1 Register (Offset = 118h) [reset = 0h]

This is where the SRC1 filter status is checked

Return to Summary Table

Table 14-9782. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0118h
AASRC1	02D4 0118h

Figure 14-4836. AASRC_CFG_SRC_STATUS_1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>UPSAMPLE</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RATE_RATIO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATE_RATIO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9783. AASRC_CFG_SRC_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	UPSAMPLE	R	0h	This signal becomes high when Output sampling rate is greater than Input sampling rate 0 `Output sampling rate < Input sampling rate` 1 `Output sampling rate > Input sampling rate`
15:0	RATE_RATIO	R	0h	Input to Output sampling ratio for SRC1

14.7.1.1.2.38 AASRC_CFG_SRC_FIFO_CONTROL_2 Register

14.7.1.1.2.38.1 AASRC_CFG_SRC_FIFO_CONTROL_2 Register (Offset = 120h) [reset = 10001h]

This is where the SRC2 FIFOs are configured

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Table 14-9784. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0120h
AASRC1	02D4 0120h

Figure 14-4837. AASRC_CFG_SRC_FIFO_CONTROL_2 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9785. AASRC_CFG_SRC_FIFO_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0

27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC2 is underflowed
				`0 No underflow is detected`
				`1 Underflow is detected`

26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC2 is underflowed
				`0 No underflow is detected`
				`1 Underflow is detected`

25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC2 is overflowed
				`0 No overflow is detected`
				`1 Overflow is detected`

24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC2 is overflowed
				`0 No overflow is detected`
				`1 Overflow is detected`

Table 14-9785. AASRC_CFG_SRC_FIFO_CONTROL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC2 OUTFIFOs event to fire 1-32: 1-32 samples
15:12	RESERVED1	R	0h	Reserved
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC2 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC2 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC2 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC2 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC2 INFIFOs event to fire 1-32: 1-32 samples

14.7.1.1.2.39 AASRC_CFG_SRC_CONTROL_2 Register

14.7.1.1.2.39.1 AASRC_CFG_SRC_CONTROL_2 Register (Offset = 124h) [reset = 0h]

This is where the SRC2 filter is configured

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Table 14-9786. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0124h
AASRC1	02D4 0124h

Figure 14-4838. AASRC_CFG_SRC_CONTROL_2 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ATTENUATION							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9787. AASRC_CFG_SRC_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of SRC2 The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC2 output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9787. AASRC_CFG_SRC_CONTROL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 `Decimation Filter` 1 `Direct Down Sampling`
9	MUTE	R/W	0h	This bit enables or disables the SRC output soft mute function; output data set to all zeros 0 `Mute disabled` 1 `Mute enabled`
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the SRC filters dithering 0 `Dithering disabled` 1 `Dithering enabled`
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.40 AASRC_CFG_SRC_STATUS_2 Register

14.7.1.1.2.40.1 AASRC_CFG_SRC_STATUS_2 Register (Offset = 128h) [reset = 0h]

This is where the SRC2 filter status is checked

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Table 14-9788. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0128h
AASRC1	02D4 0128h

Figure 14-4839. AASRC_CFG_SRC_STATUS_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							UPSAMPLE
R							R
0h							0h
15	14	13	12	11	10	9	8
RATE_RATIO							
R							
0h							
7	6	5	4	3	2	1	0
RATE_RATIO							
R							
0h							

Table 14-9789. AASRC_CFG_SRC_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	UPSAMPLE	R	0h	This signal becomes high when Output sampling rate is greater than Input sampling rate 0 `Output sampling rate < Input sampling rate` 1 `Output sampling rate > Input sampling rate`
15:0	RATE_RATIO	R	0h	Input to Output sampling ratio for SRC2

14.7.1.1.2.41 AASRC_CFG_SRC_FIFO_CONTROL_3 Register

14.7.1.1.2.41.1 AASRC_CFG_SRC_FIFO_CONTROL_3 Register (Offset = 130h) [reset = 10001h]

This is where the SRC3 FIFOs are configured

Return to Summary Table

Table 14-9790. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0130h
AASRC1	02D4 0130h

Figure 14-4840. AASRC_CFG_SRC_FIFO_CONTROL_3 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
OUTFIFO_THRESHOLD							
R/W							
1h							
15	14	13	12	11	10	9	8
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9791. AASRC_CFG_SRC_FIFO_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC3 is underflowed 0 No underflow is detected 1 Underflow is detected
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC3 is underflowed 0 No underflow is detected 1 Underflow is detected
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC3 is overflowed 0 No overflow is detected 1 Overflow is detected
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC3 is overflowed 0 No overflow is detected 1 Overflow is detected

Table 14-9791. AASRC_CFG_SRC_FIFO_CONTROL_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC3 OUTFIFOs event to fire 1-32: 1-32 samples
15:12	RESERVED1	R	0h	Reserved
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC3 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC3 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC3 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC3 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC3 INFIFOs event to fire 1-32: 1-32 samples

14.7.1.1.2.42 AASRC_CFG_SRC_CONTROL_3 Register

14.7.1.1.2.42.1 AASRC_CFG_SRC_CONTROL_3 Register (Offset = 134h) [reset = 0h]

This is where the SRC3 filter is configured

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Table 14-9792. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0134h
AASRC1	02D4 0134h

Figure 14-4841. AASRC_CFG_SRC_CONTROL_3 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	22	21	20	19	18	17	16
ATTENUATION							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9793. AASRC_CFG_SRC_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of SRC3 The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC3 output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9793. AASRC_CFG_SRC_CONTROL_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 `Decimation Filter` 1 `Direct Down Sampling`
9	MUTE	R/W	0h	This bit enables or disables the SRC output soft mute function; output data set to all zeros 0 `Mute disabled` 1 `Mute enabled`
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the SRC filters dithering 0 `Dithering disabled` 1 `Dithering enabled`
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.43 AASRC_CFG_SRC_STATUS_3 Register

14.7.1.1.2.43.1 AASRC_CFG_SRC_STATUS_3 Register (Offset = 138h) [reset = 0h]

This is where the SRC3 filter status is checked

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Table 14-9794. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0138h
AASRC1	02D4 0138h

Figure 14-4842. AASRC_CFG_SRC_STATUS_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							UPSAMPLE
R							R
0h							0h
15	14	13	12	11	10	9	8
RATE_RATIO							
R							
0h							
7	6	5	4	3	2	1	0
RATE_RATIO							
R							
0h							

Table 14-9795. AASRC_CFG_SRC_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	UPSAMPLE	R	0h	This signal becomes high when Output sampling rate is greater than Input sampling rate 0 `Output sampling rate < Input sampling rate` 1 `Output sampling rate > Input sampling rate`
15:0	RATE_RATIO	R	0h	Input to Output sampling ratio for SRC3

14.7.1.1.2.44 AASRC_CFG_SRC_FIFO_CONTROL_4 Register

14.7.1.1.2.44.1 AASRC_CFG_SRC_FIFO_CONTROL_4 Register (Offset = 140h) [reset = 10001h]

This is where the SRC4 FIFOs are configured

Return to Summary Table

Table 14-9796. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0140h
AASRC1	02D4 0140h

Figure 14-4843. AASRC_CFG_SRC_FIFO_CONTROL_4 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9797. AASRC_CFG_SRC_FIFO_CONTROL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC4 is underflowed 0 No underflow is detected 1 Underflow is detected
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC4 is underflowed 0 No underflow is detected 1 Underflow is detected
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC4 is overflowed 0 No overflow is detected 1 Overflow is detected
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC4 is overflowed 0 No overflow is detected 1 Overflow is detected

Table 14-9797. AASRC_CFG_SRC_FIFO_CONTROL_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC4 OUTFIFOs event to fire 1-32: 1-32 samples
15:12	RESERVED1	R	0h	Reserved
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC4 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC4 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC4 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC4 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC4 INFIFOs event to fire 1-32: 1-32 samples

14.7.1.1.2.45 AASRC_CFG_SRC_CONTROL_4 Register

14.7.1.1.2.45.1 AASRC_CFG_SRC_CONTROL_4 Register (Offset = 144h) [reset = 0h]

This is where the SRC4 filter is configured

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Table 14-9798. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0144h
AASRC1	02D4 0144h

Figure 14-4844. AASRC_CFG_SRC_CONTROL_4 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	22	21	20	19	18	17	16
ATTENUATION							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9799. AASRC_CFG_SRC_CONTROL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of SRC4 The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC4 output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9799. AASRC_CFG_SRC_CONTROL_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 `Decimation Filter` 1 `Direct Down Sampling`
9	MUTE	R/W	0h	This bit enables or disables the SRC output soft mute function; output data set to all zeros 0 `Mute disabled` 1 `Mute enabled`
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the SRC filters dithering 0 `Dithering disabled` 1 `Dithering enabled`
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.46 AASRC_CFG_SRC_STATUS_4 Register

14.7.1.1.2.46.1 AASRC_CFG_SRC_STATUS_4 Register (Offset = 148h) [reset = 0h]

This is where the SRC4 filter status is checked

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Table 14-9800. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0148h
AASRC1	02D4 0148h

Figure 14-4845. AASRC_CFG_SRC_STATUS_4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							UPSAMPLE
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_RATIO							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_RATIO							
R							
0h							

Table 14-9801. AASRC_CFG_SRC_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	UPSAMPLE	R	0h	This signal becomes high when Output sampling rate is greater than Input sampling rate 0 `Output sampling rate < Input sampling rate` 1 `Output sampling rate > Input sampling rate`
15:0	RATE_RATIO	R	0h	Input to Output sampling ratio for SRC4

14.7.1.1.2.47 AASRC_CFG_SRC_FIFO_CONTROL_5 Register

14.7.1.1.2.47.1 AASRC_CFG_SRC_FIFO_CONTROL_5 Register (Offset = 150h) [reset = 10001h]

This is where the SRC5 FIFOs are configured

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Table 14-9802. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0150h
AASRC1	02D4 0150h

Figure 14-4846. AASRC_CFG_SRC_FIFO_CONTROL_5 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
OUTFIFO_THRESHOLD							
R/W							
1h							
15	14	13	12	11	10	9	8
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9803. AASRC_CFG_SRC_FIFO_CONTROL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC5 is underflowed 0 No underflow is detected 1 Underflow is detected
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC5 is underflowed 0 No underflow is detected 1 Underflow is detected
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC5 is overflowed 0 No overflow is detected 1 Overflow is detected
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC5 is overflowed 0 No overflow is detected 1 Overflow is detected

Table 14-9803. AASRC_CFG_SRC_FIFO_CONTROL_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC5 OUTFIFOs event to fire 1-32: 1-32 samples
15:12	RESERVED1	R	0h	Reserved
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC5 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC5 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC5 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC5 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC5 INFIFOs event to fire 1-32: 1-32 samples

14.7.1.1.2.48 AASRC_CFG_SRC_CONTROL_5 Register

14.7.1.1.2.48.1 AASRC_CFG_SRC_CONTROL_5 Register (Offset = 154h) [reset = 0h]

This is where the SRC5 filter is configured

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Table 14-9804. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0154h
AASRC1	02D4 0154h

Figure 14-4847. AASRC_CFG_SRC_CONTROL_5 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ATTENUATION							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9805. AASRC_CFG_SRC_CONTROL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of SRC5 The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC5 output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9805. AASRC_CFG_SRC_CONTROL_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 Decimation Filter 1 Direct Down Sampling
9	MUTE	R/W	0h	This bit enables or disables the SRC output soft mute function; output data set to all zeros 0 Mute disabled 1 Mute enabled
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the SRC filters dithering 0 Dithering disabled 1 Dithering enabled
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.49 AASRC_CFG_SRC_STATUS_5 Register

14.7.1.1.2.49.1 AASRC_CFG_SRC_STATUS_5 Register (Offset = 158h) [reset = 0h]

This is where the SRC5 filter status is checked

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Table 14-9806. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0158h
AASRC1	02D4 0158h

Figure 14-4848. AASRC_CFG_SRC_STATUS_5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>UPSAMPLE</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RATE_RATIO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATE_RATIO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9807. AASRC_CFG_SRC_STATUS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	UPSAMPLE	R	0h	This signal becomes high when Output sampling rate is greater than Input sampling rate 0 `Output sampling rate < Input sampling rate` 1 `Output sampling rate > Input sampling rate`
15:0	RATE_RATIO	R	0h	Input to Output sampling ratio for SRC5

14.7.1.1.2.50 AASRC_CFG_SRC_FIFO_CONTROL_6 Register

14.7.1.1.2.50.1 AASRC_CFG_SRC_FIFO_CONTROL_6 Register (Offset = 160h) [reset = 10001h]

This is where the SRC6 FIFOs are configured

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Table 14-9808. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0160h
AASRC1	02D4 0160h

Figure 14-4849. AASRC_CFG_SRC_FIFO_CONTROL_6 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9809. AASRC_CFG_SRC_FIFO_CONTROL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC6 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC6 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC6 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC6 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`

Table 14-9809. AASRC_CFG_SRC_FIFO_CONTROL_6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC6 OUTFIFOs event to fire 1-32: 1-32 samples
15:12	RESERVED1	R	0h	Reserved
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC6 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC6 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC6 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC6 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC6 INFIFOs event to fire 1-32: 1-32 samples

14.7.1.1.2.51 AASRC_CFG_SRC_CONTROL_6 Register

14.7.1.1.2.51.1 AASRC_CFG_SRC_CONTROL_6 Register (Offset = 164h) [reset = 0h]

This is where the SRC6 filter is configured

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Table 14-9810. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0164h
AASRC1	02D4 0164h

Figure 14-4850. AASRC_CFG_SRC_CONTROL_6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">CHANNEL_ENABLE</td><td colspan="2">OUTPUT_WORD_LENGTH</td><td colspan="2">GROUP_DELAY</td><td colspan="2">DE_EMPHASIS_MODE</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ATTENUATION</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>DIRECT_DOWN_SAMPLE</td><td>MUTE</td><td>DITHER_ENABLE</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">INPUT_WORD_LENGTH</td><td colspan="3">OUTPUT_CLOCK_ZONE_SELECT</td><td colspan="3">INPUT_CLOCK_ZONE_SELECT</td></tr>
<tr><td colspan="2">R/W</td><td colspan="3">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-9811. AASRC_CFG_SRC_CONTROL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of SRC6 The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC6 output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9811. AASRC_CFG_SRC_CONTROL_6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 `Decimation Filter` 1 `Direct Down Sampling`
9	MUTE	R/W	0h	This bit enables or disables the SRC output soft mute function; output data set to all zeros 0 `Mute disabled` 1 `Mute enabled`
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the SRC filters dithering 0 `Dithering disabled` 1 `Dithering enabled`
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.52 AASRC_CFG_SRC_STATUS_6 Register

14.7.1.1.2.52.1 AASRC_CFG_SRC_STATUS_6 Register (Offset = 168h) [reset = 0h]

This is where the SRC6 filter status is checked

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Table 14-9812. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0168h
AASRC1	02D4 0168h

Figure 14-4851. AASRC_CFG_SRC_STATUS_6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							UPSAMPLE
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_RATIO							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_RATIO							
R							
0h							

Table 14-9813. AASRC_CFG_SRC_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	UPSAMPLE	R	0h	This signal becomes high when Output sampling rate is greater than Input sampling rate 0 `Output sampling rate < Input sampling rate` 1 `Output sampling rate > Input sampling rate`
15:0	RATE_RATIO	R	0h	Input to Output sampling ratio for SRC6

14.7.1.1.2.53 AASRC_CFG_SRC_FIFO_CONTROL_7 Register

14.7.1.1.2.53.1 AASRC_CFG_SRC_FIFO_CONTROL_7 Register (Offset = 170h) [reset = 10001h]

This is where the SRC7 FIFOs are configured

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Table 14-9814. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0170h
AASRC1	02D4 0170h

Figure 14-4852. AASRC_CFG_SRC_FIFO_CONTROL_7 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9815. AASRC_CFG_SRC_FIFO_CONTROL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0

27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC7 is underflowed
				`0` `No underflow is detected`
				`1` `Underflow is detected`

26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC7 is underflowed
				`0` `No underflow is detected`
				`1` `Underflow is detected`

25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel OUTFIFO for SRC7 is overflowed
				`0` `No overflow is detected`
				`1` `Overflow is detected`

24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel OUTFIFO for SRC7 is overflowed
				`0` `No overflow is detected`
				`1` `Overflow is detected`

Table 14-9815. AASRC_CFG_SRC_FIFO_CONTROL_7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC7 OUTFIFOs event to fire 1-32: 1-32 samples
15:12	RESERVED1	R	0h	Reserved
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC7 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC7 is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Right Channel INFIFO for SRC7 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when Left Channel INFIFO for SRC7 is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and SRC7 INFIFOs event to fire 1-32: 1-32 samples

14.7.1.1.2.54 AASRC_CFG_SRC_CONTROL_7 Register

14.7.1.1.2.54.1 AASRC_CFG_SRC_CONTROL_7 Register (Offset = 174h) [reset = 0h]

This is where the SRC7 filter is configured

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Table 14-9816. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0174h
AASRC1	02D4 0174h

Figure 14-4853. AASRC_CFG_SRC_CONTROL_7 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	22	21	20	19	18	17	16
ATTENUATION							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9817. AASRC_CFG_SRC_CONTROL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of SRC7 The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC7 output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9817. AASRC_CFG_SRC_CONTROL_7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 `Decimation Filter` 1 `Direct Down Sampling`
9	MUTE	R/W	0h	This bit enables or disables the SRC output soft mute function; output data set to all zeros 0 `Mute disabled` 1 `Mute enabled`
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the SRC filters dithering 0 `Dithering disabled` 1 `Dithering enabled`
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the stream0 It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.55 AASRC_CFG_SRC_STATUS_7 Register

14.7.1.1.2.55.1 AASRC_CFG_SRC_STATUS_7 Register (Offset = 178h) [reset = 0h]

This is where the SRC7 filter status is checked

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Table 14-9818. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0178h
AASRC1	02D4 0178h

Figure 14-4854. AASRC_CFG_SRC_STATUS_7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>UPSAMPLE</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RATE_RATIO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATE_RATIO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9819. AASRC_CFG_SRC_STATUS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	UPSAMPLE	R	0h	This signal becomes high when Output sampling rate is greater than Input sampling rate 0 `Output sampling rate < Input sampling rate` 1 `Output sampling rate > Input sampling rate`
15:0	RATE_RATIO	R	0h	Input to Output sampling ratio for SRC7

14.7.1.1.2.56 AASRC_CFG_GROUP_FIFO_CONTROL_0 Register

14.7.1.1.2.56.1 AASRC_CFG_GROUP_FIFO_CONTROL_0 Register (Offset = 180h) [reset = 10001h]

This register configures the FIFO settings for Group 0

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Table 14-9820. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0180h
AASRC1	02D4 0180h

Figure 14-4855. AASRC_CFG_GROUP_FIFO_CONTROL_0 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9821. AASRC_CFG_GROUP_FIFO_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Right Channel OUTFIFO for Group0 SRCs is underflowed
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Left Channel OUTFIFO for Group0 SRCs is underflowed 0 No underflow is detected 1 Underflow is detected
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Right Channel OUTFIFO for Group0 SRCs is overflowed 0 No overflow is detected 1 Overflow is detected
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Left Channel OUTFIFO for Group0 SRCs is overflowed 0 No overflow is detected 1 Overflow is detected
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and Group0 SRCs OUTFIFOs event to fire
15:12	RESERVED1	R	0h	Always read as 0

Table 14-9821. AASRC_CFG_GROUP_FIFO_CONTROL_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Right Channel INFIFO for Group0 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Left Channel INFIFO for Group0 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Right Channel INFIFO for Group0 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Left Channel INFIFO for Group0 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and Group0 SRCs INFIFOs event to fire

14.7.1.1.2.57 AASRC_CFG_GROUP_SRC_CONTROL_0 Register

14.7.1.1.2.57.1 AASRC_CFG_GROUP_SRC_CONTROL_0 Register (Offset = 184h) [reset = 0h]

This is where all the SRCs of Group0 is configured

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Table 14-9822. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0184h
AASRC1	02D4 0184h

Figure 14-4856. AASRC_CFG_GROUP_SRC_CONTROL_0 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ATTENUATION							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9823. AASRC_CFG_GROUP_SRC_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of Group0 SRCs The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the Group0 SRC output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the Group0 SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9823. AASRC_CFG_GROUP_SRC_CONTROL_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 Decimation Filter 1 Direct Down Sampling
9	MUTE	R/W	0h	This bit enables or disables the Group0 SRC output soft mute function; output data set to all zeros 0 Mute disabled 1 Mute enabled
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the Group0 SRC filters dithering 0 Dithering disabled 1 Dithering enabled
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the Group0 SRCs It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the Group0 SRCs It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.58 AASRC_CFG_GROUP_FIFO_CONTROL_1 Register

14.7.1.1.2.58.1 AASRC_CFG_GROUP_FIFO_CONTROL_1 Register (Offset = 188h) [reset = 10001h]

This register configures the FIFO settings for Group 1.

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Table 14-9824. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0188h
AASRC1	02D4 0188h

Figure 14-4857. AASRC_CFG_GROUP_FIFO_CONTROL_1 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9825. AASRC_CFG_GROUP_FIFO_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Right Channel OUTFIFO for Group1 SRCs is underflowed 0 No underflow is detected 1 Underflow is detected
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Left Channel OUTFIFO for Group1 SRCs is underflowed 0 No underflow is detected 1 Underflow is detected
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Right Channel OUTFIFO for Group1 SRCs is overflowed 0 No overflow is detected 1 Overflow is detected
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Left Channel OUTFIFO for Group1 SRCs is overflowed 0 No overflow is detected 1 Overflow is detected

Table 14-9825. AASRC_CFG_GROUP_FIFO_CONTROL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and Group1 SRCs OUTFIFOs event to fire
15:12	RESERVED1	R	0h	Always read as 0
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Right Channel INFIFO for Group1 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Left Channel INFIFO for Group1 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Right Channel INFIFO for Group1 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Left Channel INFIFO for Group1 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and Group1 SRCs INFIFOs event to fire

14.7.1.1.2.59 AASRC_CFG_GROUP_SRC_CONTROL_1 Register

14.7.1.1.2.59.1 AASRC_CFG_GROUP_SRC_CONTROL_1 Register (Offset = 18Ch) [reset = 0h]

This is where all the SRCs of Group1 is configured

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Table 14-9826. Instance Table

Instance Name	Physical Address
AASRC0	02D0 018Ch
AASRC1	02D4 018Ch

Figure 14-4858. AASRC_CFG_GROUP_SRC_CONTROL_1 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ATTENUATION							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9827. AASRC_CFG_GROUP_SRC_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of Group1 SRCs The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the Group1 SRC output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the Group1 SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9827. AASRC_CFG_GROUP_SRC_CONTROL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 `Decimation Filter` 1 `Direct Down Sampling`
9	MUTE	R/W	0h	This bit enables or disables the Group1 SRC output soft mute function; output data set to all zeros 0 `Mute disabled` 1 `Mute enabled`
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the Group1 SRC filters dithering 0 `Dithering disabled` 1 `Dithering enabled`
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the Group1 SRCs It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the Group1 SRCs It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.60 AASRC_CFG_GROUP_FIFO_CONTROL_2 Register

14.7.1.1.2.60.1 AASRC_CFG_GROUP_FIFO_CONTROL_2 Register (Offset = 190h) [reset = 10001h]

This register configures the FIFO settings for Group 2

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Table 14-9828. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0190h
AASRC1	02D4 0190h

Figure 14-4859. AASRC_CFG_GROUP_FIFO_CONTROL_2 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9829. AASRC_CFG_GROUP_FIFO_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Right Channel OUTFIFO for Group2 SRCs is underflowed 0 No underflow is detected 1 Underflow is detected
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Left Channel OUTFIFO for Group2 SRCs is underflowed 0 No underflow is detected 1 Underflow is detected
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Right Channel OUTFIFO for Group2 SRCs is overflowed 0 No overflow is detected 1 Overflow is detected
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Left Channel OUTFIFO for Group2 SRCs is overflowed 0 No overflow is detected 1 Overflow is detected

Table 14-9829. AASRC_CFG_GROUP_FIFO_CONTROL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and Group2 SRCs OUTFIFOs event to fire
15:12	RESERVED1	R	0h	Always read as 0
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Right Channel INFIFO for Group2 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Left Channel INFIFO for Group2 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Right Channel INFIFO for Group2 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Left Channel INFIFO for Group2 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and Group2 SRCs INFIFOs event to fire

14.7.1.1.2.61 AASRC_CFG_GROUP_SRC_CONTROL_2 Register

14.7.1.1.2.61.1 AASRC_CFG_GROUP_SRC_CONTROL_2 Register (Offset = 194h) [reset = 0h]

This is where all the SRCs of Group2 is configured

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Table 14-9830. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0194h
AASRC1	02D4 0194h

Figure 14-4860. AASRC_CFG_GROUP_SRC_CONTROL_2 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

23	22	21	20	19	18	17	16
ATTENUATION							
R/W							
0h							

15	14	13	12	11	10	9	8
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h

7	6	5	4	3	2	1	0
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9831. AASRC_CFG_GROUP_SRC_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of Group2 SRCs The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the Group2 SRC output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the Group2 SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9831. AASRC_CFG_GROUP_SRC_CONTROL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 `Decimation Filter` 1 `Direct Down Sampling`
9	MUTE	R/W	0h	This bit enables or disables the Group2 SRC output soft mute function; output data set to all zeros 0 `Mute disabled` 1 `Mute enabled`
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the Group2 SRC filters dithering 0 `Dithering disabled` 1 `Dithering enabled`
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the Group2 SRCs It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the Group2 SRCs It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.62 AASRC_CFG_GROUP_FIFO_CONTROL_3 Register

14.7.1.1.2.62.1 AASRC_CFG_GROUP_FIFO_CONTROL_3 Register (Offset = 198h) [reset = 10001h]

This register configures the FIFO settings for Group 3

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Table 14-9832. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0198h
AASRC1	02D4 0198h

Figure 14-4861. AASRC_CFG_GROUP_FIFO_CONTROL_3 Name Register

31	30	29	28	27	26	25	24
RESERVED				R_CHANNEL_OUTFIFO_UNDERFLOW	L_CHANNEL_OUTFIFO_UNDERFLOW	R_CHANNEL_OUTFIFO_OVERFLOW	L_CHANNEL_OUTFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTFIFO_THRESHOLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				R_CHANNEL_INFIFO_UNDERFLOW	L_CHANNEL_INFIFO_UNDERFLOW	R_CHANNEL_INFIFO_OVERFLOW	L_CHANNEL_INFIFO_OVERFLOW
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INFIFO_THRESHOLD							
R/W							
1h							

Table 14-9833. AASRC_CFG_GROUP_FIFO_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	R	0h	Always read as 0
27	R_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Right Channel OUTFIFO for Group3 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
26	L_CHANNEL_OUTFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Left Channel OUTFIFO for Group3 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
25	R_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Right Channel OUTFIFO for Group3 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
24	L_CHANNEL_OUTFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Left Channel OUTFIFO for Group3 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`

Table 14-9833. AASRC_CFG_GROUP_FIFO_CONTROL_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	OUTFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and Group3 SRCs OUTFIFOs event to fire
15:12	RESERVED1	R	0h	Always read as 0
11	R_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Right Channel INFIFO for Group3 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
10	L_CHANNEL_INFIFO_UNDERFLOW	R	0h	This signal is set to 1 when any of the Left Channel INFIFO for Group3 SRCs is underflowed 0 `No underflow is detected` 1 `Underflow is detected`
9	R_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Right Channel INFIFO for Group3 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
8	L_CHANNEL_INFIFO_OVERFLOW	R	0h	This signal is set to 1 when any of the Left Channel INFIFO for Group3 SRCs is overflowed 0 `No overflow is detected` 1 `Overflow is detected`
7:0	INFIFO_THRESHOLD	R/W	1h	This is the number of samples that must be available for the interrupt and Group3 SRCs INFIFOs event to fire

14.7.1.1.2.63 AASRC_CFG_GROUP_SRC_CONTROL_3 Register

14.7.1.1.2.63.1 AASRC_CFG_GROUP_SRC_CONTROL_3 Register (Offset = 19Ch) [reset = 0h]

This is where all the SRCs of Group3 is configured

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Table 14-9834. Instance Table

Instance Name	Physical Address
AASRC0	02D0 019Ch
AASRC1	02D4 019Ch

Figure 14-4862. AASRC_CFG_GROUP_SRC_CONTROL_3 Name Register

31	30	29	28	27	26	25	24
CHANNEL_ENABLE		OUTPUT_WORD_LENGTH		GROUP_DELAY		DE_EMPHASIS_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ATTENUATION							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					DIRECT_DOWN_SAMPLE	MUTE	DITHER_ENABLE
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPUT_WORD_LENGTH		OUTPUT_CLOCK_ZONE_SELECT			INPUT_CLOCK_ZONE_SELECT		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-9835. AASRC_CFG_GROUP_SRC_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	CHANNEL_ENABLE	R/W	0h	Setting this enables the Channels of Group3 SRCs The output FIFOs for the stream must be enabled before the input FIFOs 00: No channel enabled 01: Only Right Channel enabled 10: Only Left Channel enabled 11: Both channels enabled Clearing this register will clear the data path
29:28	OUTPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the Group3 SRC output data The word length reduction is performed by utilizing triangular PDF dithering 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
27:26	GROUP_DELAY	R/W	0h	These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function 0: 64 Samples [Default] 1: 32 Samples 2: 16 Samples 3: 8 Samples
25:24	DE_EMPHASIS_MODE	R/W	0h	These bits are utilized to enable or disable the digital de-emphasis filter manually The de-emphasis filter is intended to process 50/15s pre-emphasized audio material at the following input sampling rates 0: De-Emphasis Disabled [Default] 1: De-Emphasis Enabled for fS = 48kHz 2: De-Emphasis Enabled for fS = 441kHz 3: De-Emphasis Enabled for fS = 32kHz
23:16	ATTENUATION	R/W	0h	These bits are utilized to configure the Group3 SRC digital output attenuation for the stream Output Attenuation [dB] = N 05, where N = Attenuation[7:0]DEC
15:11	RESERVED	R	0h	Always read as 0

Table 14-9835. AASRC_CFG_GROUP_SRC_CONTROL_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIRECT_DOWN_SAMPLE	R/W	0h	This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering DDN Decimation Function. Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing 0 Decimation Filter 1 Direct Down Sampling
9	MUTE	R/W	0h	This bit enables or disables the Group3 SRC output soft mute function; output data set to all zeros 0 Mute disabled 1 Mute enabled
8	DITHER_ENABLE	R/W	0h	This bit enables or disables the Group3 SRC filters dithering 0 Dithering disabled 1 Dithering enabled
7:6	INPUT_WORD_LENGTH	R/W	0h	These bits select the word length for the SRC0 input data 0: 24 Bits [Default] 1: 20 Bits 2: 18 Bits 3: 16 Bits
5:3	OUTPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the output clock zone for the Group3 SRCs It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 00: This selects the Clock Recovery loop 0 01: This selects the Clock Recovery loop 1 10: This selects the Clock Recovery loop 2 11: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid
2:0	INPUT_CLOCK_ZONE_SELECT	R/W	0h	This selects the input clock zone for the Group3 SRCs It can select between the 4 external audio clock zones Based on this number rate and stamp is passed to the Stream0 Sample rate converter from respective clock recovery loop 000: This selects the Clock Recovery loop 0 001: This selects the Clock Recovery loop 1 010: This selects the Clock Recovery loop 2 011: This selects the Clock Recovery loop 3 In case of Galileo other values are not valid

14.7.1.1.2.64 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_0 Register

14.7.1.1.2.64.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_0 Register (Offset = 200h) [reset = 0h]

This is the value of the next timestamp for the input clock generator 0. This contains the 24 bit fractional and the first 8 bits of the integer. This register is used to generate soft clock

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Table 14-9836. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0200h
AASRC1	02D4 0200h

Figure 14-4863. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">STAMP_INT_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9837. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.65 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_0 Register

14.7.1.1.2.65.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_0 Register (Offset = 204h) [reset = 0h]

This is the value of the rate for the clock generator 0. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock.

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Table 14-9838. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0204h
AASRC1	02D4 0204h

Figure 14-4864. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R/W							
0h							

Table 14-9839. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.66 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_0 Register

14.7.1.1.2.66.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_0 Register (Offset = 208h) [reset = 0h]

This is the value of the rate for the clock generator 0. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock.

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Table 14-9840. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0208h
AASRC1	02D4 0208h

Figure 14-4865. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_0 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9841. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the clock source

14.7.1.1.2.67 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_0 Register

14.7.1.1.2.67.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_0 Register (Offset = 20Ch) [reset = 0h]

This is the value of the rate for the clock generator 0. This contains the upper 16 bits of the integer and the enable for the clock generator. This register is used to generate soft clock.

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Table 14-9842. Instance Table

Instance Name	Physical Address
AASRC0	02D0 020Ch
AASRC1	02D4 020Ch

Figure 14-4866. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_0 Name Register

31	30	29	28	27	26	25	24
INPUT_CLK_GEN_EN	RESERVED						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_INT_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_INT_HI							
R/W							
0h							

Table 14-9843. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description

31	INPUT_CLK_GEN_EN	R/W	0h	This signal enables the Input Clock Generator 0
				`0 Clock generator disabled`
				`1 Clock generator enabled`

30:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.68 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0 Register

14.7.1.1.2.68.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0 Register (Offset = 210h) [reset = 0h]

This is the value of the rate for the input clock recovery loop 0. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9844. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0210h
AASRC1	02D4 0210h

Figure 14-4867. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9845. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the rate for the intput clock recovery loop 0
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the rate for the intput clock recovery loop 0

14.7.1.1.2.69 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0 Register

14.7.1.1.2.69.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0 Register (Offset = 214h) [reset = 0h]

This is the value of the rate for the input clock recovery loop 0. This contains the upper 16 bits of the rate input clock recovery loop

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Table 14-9846. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0214h
AASRC1	02D4 0214h

Figure 14-4868. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RATE_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R							
0h							

Table 14-9847. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R	0h	This is the upper 16 bits of the integer multiple of the rate for the intput clock recovery loop 0

14.7.1.1.2.70 AASRC_CFG_INPUT_CLOCKZONE_COUNT_0 Register

14.7.1.1.2.70.1 AASRC_CFG_INPUT_CLOCKZONE_COUNT_0 Register (Offset = 218h) [reset = 0h]

Free Running counter for clockzone 0

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Table 14-9848. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0218h
AASRC1	02D4 0218h

Figure 14-4869. AASRC_CFG_INPUT_CLOCKZONE_COUNT_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
INPUT_CLOCK_ZONE_COUNT							
R							
0h							
15	14	13	12	11	10	9	8
INPUT_CLOCK_ZONE_COUNT							
R							
0h							
7	6	5	4	3	2	1	0
INPUT_CLOCK_ZONE_COUNT							
R							
0h							

Table 14-9849. AASRC_CFG_INPUT_CLOCKZONE_COUNT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Always read as 0
23:0	INPUT_CLOCK_ZONE_COUNT	R	0h	This gives the value of free running counter at every posedge of sync signal

14.7.1.1.2.71 AASRC_CFG_INPUT_CLOCKZONE_CONTROL_0 Register

14.7.1.1.2.71.1 AASRC_CFG_INPUT_CLOCKZONE_CONTROL_0 Register (Offset = 21Ch) [reset = 0h]

This is the configuration for Input Clock zone 0

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Table 14-9850. Instance Table

Instance Name	Physical Address
AASRC0	02D0 021Ch
AASRC1	02D4 021Ch

Figure 14-4870. AASRC_CFG_INPUT_CLOCKZONE_CONTROL_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED					OVERRIDE_SETTLE_VALUE	OVERRIDE_SETTLE	LOOP_SETUP
R					R/W	R/W	R/W
0h					0h	0h	0h
15	14	13	12	11	10	9	8
LOOP_SETUP							SETTLE
R/W							R
0h							0h
7	6	5	4	3	2	1	0
LOOP_STATE				INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT			
R				R/W			
0h				0h			

Table 14-9851. AASRC_CFG_INPUT_CLOCKZONE_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	R	0h	Always read as 0
18	OVERRIDE_SETTLE_VALUE	R/W	0h	Value written to this field will be used as settle if override settle signal is set
17	OVERRIDE_SETTLE	R/W	0h	This signal override the settle of input clock zone 0 clock recovery loop 0 Settle from clock recovery will be used 1 Value written to override settle value will be used
16:9	LOOP_SETUP	R/W	0h	This is the setting for input clock recovery loop for zone 0 8h00: Slow loop 8h40: Medium1 loop 8h80: Medium2 loop 8hC0: Slow loop
8	SETTLE	R	0h	This signals sets to 1 when clock recovery loop is settled
7:4	LOOP_STATE	R	0h	Loop debug State
3:0	INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT	R/W	0h	This selects the 8x1 and 2x1 mux structure for input clock zone 0 1xxx: Clock comes from output clock gen 0 0000-0111: Selects rxsync signal from 0-7

14.7.1.1.2.72 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_0 Register

14.7.1.1.2.72.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_0 Register (Offset = 220h) [reset = 0h]

This is the value of the next timestamp for the Output clock generator 0. This contains the 24 bit fractional and the first 8 bits of the integer. This register is used to generate soft clock

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Table 14-9852. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0220h
AASRC1	02D4 0220h

Figure 14-4871. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_0 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9853. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.73 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_0 Register

14.7.1.1.2.73.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_0 Register (Offset = 224h) [reset = 0h]

This is the value of the next timestamp for the Output clock generator 0. This contains the first 16 bits of the integer. This register is used to generate soft clock.

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Table 14-9854. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0224h
AASRC1	02D4 0224h

Figure 14-4872. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R/W							
0h							

Table 14-9855. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.74 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_0 Register

14.7.1.1.2.74.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_0 Register (Offset = 228h) [reset = 0h]

This is the value of the rate for the clock generator 0. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock

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Table 14-9856. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0228h
AASRC1	02D4 0228h

Figure 14-4873. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_0 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9857. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the clock source

14.7.1.1.2.75 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_0 Register

14.7.1.1.2.75.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_0 Register (Offset = 22Ch) [reset = 0h]

This is the value of the rate for the clock generator 0. This contains the upper 16 bits of the integer and the enable for the clock generator. This register is used to generate soft clock.

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Table 14-9858. Instance Table

Instance Name	Physical Address
AASRC0	02D0 022Ch
AASRC1	02D4 022Ch

Figure 14-4874. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_0 Name Register

31	30	29	28	27	26	25	24
OUTPUT_CLOCK_GEN_EN	RESERVED						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_INT_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_INT_HI							
R/W							
0h							

Table 14-9859. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OUTPUT_CLOCK_GEN_EN	R/W	0h	This signal enables the Output Clock Generator 0
30:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.76 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0 Register

14.7.1.1.2.76.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0 Register (Offset = 230h) [reset = 0h]

This is the value of the rate for the Output clock recovery loop 0. This contains the 24 bit fractional and the first 8 bits of the integer.

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Table 14-9860. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0230h
AASRC1	02D4 0230h

Figure 14-4875. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9861. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the rate for the outtput clock recovery loop 0
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the rate for the outtput clock recovery loop 0

14.7.1.1.2.77 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0 Register

14.7.1.1.2.77.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0 Register (Offset = 234h) [reset = 0h]

This is the value of the rate for the Output clock recovery loop 0. This contains the upper 16 bits of the Output clock recovery loop

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Table 14-9862. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0234h
AASRC1	02D4 0234h

Figure 14-4876. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RATE_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R							
0h							

Table 14-9863. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R	0h	This is the Upper 16 bits of the integer multiple of the rate for the outtput clock recovery loop 0

14.7.1.1.2.78 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_0 Register

14.7.1.1.2.78.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_0 Register (Offset = 238h) [reset = 0h]

This is the value of the timestamp for the Output clock recovery loop 0. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9864. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0238h
AASRC1	02D4 0238h

Figure 14-4877. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_0 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9865. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated when output fifo event occurs
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated when output fifo event occurs

14.7.1.1.2.79 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_0 Register

14.7.1.1.2.79.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_0 Register (Offset = 23Ch) [reset = 0h]

This is the value of the next timestamp for the Output clock recovery loop 0. This contains the first 16 bits of the integer

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Table 14-9866. Instance Table

Instance Name	Physical Address
AASRC0	02D0 023Ch
AASRC1	02D4 023Ch

Figure 14-4878. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R							
0h							

Table 14-9867. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock recovery loop This register will be updated when output fifo event occurs

14.7.1.1.2.80 AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_0 Register

14.7.1.1.2.80.1 AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_0 Register (Offset = 240h) [reset = 0h]

Free Running counter for clockzone 0

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Table 14-9868. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0240h
AASRC1	02D4 0240h

Figure 14-4879. AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							
15	14	13	12	11	10	9	8
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							
7	6	5	4	3	2	1	0
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							

Table 14-9869. AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Always read as 0
23:0	OUTPUT_CLOCK_ZONE_COUNT	R	0h	This gives the value of free running counter at every posedge of sync signal

14.7.1.1.2.81 AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_0 Register

14.7.1.1.2.81.1 AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_0 Register (Offset = 244h) [reset = 0h]

This is the configuration for Output Clock zone 0

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Table 14-9870. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0244h
AASRC1	02D4 0244h

Figure 14-4880. AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td>OVERRIDE_SETTLE_VALUE</td><td>OVERRIDE_SETTLE</td><td>LOOP_SETUP</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">LOOP_SETUP</td><td>SETTLE</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">LOOP_STATE</td><td colspan="4">OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9871. AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	R	0h	Always read as 0
18	OVERRIDE_SETTLE_VALUE	R/W	0h	Value written to this field will be used as settle if override settle signal is set
17	OVERRIDE_SETTLE	R/W	0h	This signal override the settle of output clock zone 0 clock recovery loop 0 Settle from clock recovery will be used 1 Value written to override settle value will be used
16:9	LOOP_SETUP	R/W	0h	This is the setting for input clock recovery loop for zone 0 8h00: Slow loop 8h40: Medium1 loop 8h80: Medium2 loop 8hC0: Slow loop
8	SETTLE	R	0h	This signals sets to 1 when clock recovery loop is settled
7:4	LOOP_STATE	R	0h	Loop debug state
3:0	OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT	R/W	0h	This selects the 8x1 and 2x1 mux structure for output clock zone 0 1xxx: Clock comes from output clock gen 0 0000-0111: Selects txsync signal from 0-7

14.7.1.1.2.82 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0 Register

14.7.1.1.2.82.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0 Register (Offset = 248h) [reset = 0h]

This is the override value of the rate for the input clock recovery loop 0. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9872. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0248h
AASRC1	02D4 0248h

Figure 14-4881. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9873. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the override clock recovery loop 0
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the override clock recovery loop 0

14.7.1.1.2.83 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0 Register

14.7.1.1.2.83.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0 Register (Offset = 24Ch) [reset = 0h]

This is the Override value of the rate for the input clock recovery loop 0. This contains the upper 16 bits of the rate input clock recovery loop

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Table 14-9874. Instance Table

Instance Name	Physical Address
AASRC0	02D0 024Ch
AASRC1	02D4 024Ch

Figure 14-4882. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>OVERRIDE_RATE</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9875. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	OVERRIDE_RATE	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the override clock recovery loop 0
15:0	RATE_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the override clock recovery loop 0

14.7.1.1.2.84 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0 Register

14.7.1.1.2.84.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0 Register (Offset = 250h) [reset = 0h]

This is the override value of the rate for the Output clock recovery loop 0. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9876. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0250h
AASRC1	02D4 0250h

Figure 14-4883. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RATE_INT_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9877. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the output override clock recovery loop 0
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the output override clock recovery loop 0

14.7.1.1.2.85 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0 Register

14.7.1.1.2.85.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0 Register (Offset = 254h) [reset = 0h]

This is the override value of the rate for the Output clock recovery loop 0. This contains the upper 16 bits of the Output clock recovery loop

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Table 14-9878. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0254h
AASRC1	02D4 0254h

Figure 14-4884. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OVERRIDE_RATE
R							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_INT_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_INT_HI							
R/W							
0h							

Table 14-9879. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	OVERRIDE_RATE	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the output override clock recovery loop 0
15:0	RATE_INT_HI	R/W	0h	This is the Upper 16 bits of the integer multiple of the rate for the output override clock recovery loop 0

14.7.1.1.2.86 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_1 Register

14.7.1.1.2.86.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_1 Register (Offset = 280h) [reset = 0h]

This is the value of the next timestamp for the input clock generator 1. This contains the 24 bit fractional and the first 8 bits of the integer. This register is used to generate soft clock.

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Table 14-9880. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0280h
AASRC1	02D4 0280h

Figure 14-4885. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_1 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9881. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.87 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_1 Register

14.7.1.1.2.87.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_1 Register (Offset = 284h) [reset = 0h]

This is the value of the next timestamp for the input clock generator 1. This contains the first 16 bits of the integer. This register is used to generate soft clock.

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Table 14-9882. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0284h
AASRC1	02D4 0284h

Figure 14-4886. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R/W							
0h							

Table 14-9883. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.88 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_1 Register

14.7.1.1.2.88.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_1 Register (Offset = 288h) [reset = 0h]

This is the value of the rate for the clock generator 1. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock.

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Table 14-9884. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0288h
AASRC1	02D4 0288h

Figure 14-4887. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_1 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9885. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the clock source

14.7.1.1.2.89 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_1 Register

14.7.1.1.2.89.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_1 Register (Offset = 28Ch) [reset = 0h]

This is the value of the rate for the clock generator 1. This contains the upper 16 bits of the integer and the enable for the clock generator. This register is used to generate soft clock

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Table 14-9886. Instance Table

Instance Name	Physical Address
AASRC0	02D0 028Ch
AASRC1	02D4 028Ch

Figure 14-4888. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_1 Name Register

31	30	29	28	27	26	25	24
INPUT_CLK_GEN_EN	RESERVED						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_INT_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_INT_HI							
R/W							
0h							

Table 14-9887. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INPUT_CLK_GEN_EN	R/W	0h	This signal enables the Input Clock Generator 1 0 `Clock generator disabled` 1 `Clock generator enabled`
30:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.90 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1 Register

14.7.1.1.2.90.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1 Register (Offset = 290h) [reset = 0h]

This is the value of the rate for the input clock recovery loop 1. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9888. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0290h
AASRC1	02D4 0290h

Figure 14-4889. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9889. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the rate for the intput clock recovery loop 1
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the rate for the intput clock recovery loop 1

14.7.1.1.2.91 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1 Register

14.7.1.1.2.91.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1 Register (Offset = 294h) [reset = 0h]

This is the value of the rate for the input clock recovery loop 1. This contains the upper 16 bits of the rate input clock recovery loop

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Table 14-9890. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0294h
AASRC1	02D4 0294h

Figure 14-4890. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RATE_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R							
0h							

Table 14-9891. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R	0h	This is the upper 16 bits of the integer multiple of the rate for the intput clock recovery loop 1

14.7.1.1.2.92 AASRC_CFG_INPUT_CLOCKZONE_COUNT_1 Register

14.7.1.1.2.92.1 AASRC_CFG_INPUT_CLOCKZONE_COUNT_1 Register (Offset = 298h) [reset = 0h]

Free Running counter for clock zone 1

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Table 14-9892. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0298h
AASRC1	02D4 0298h

Figure 14-4891. AASRC_CFG_INPUT_CLOCKZONE_COUNT_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
INPUT_CLOCK_ZONE_COUNT							
R							
0h							
15	14	13	12	11	10	9	8
INPUT_CLOCK_ZONE_COUNT							
R							
0h							
7	6	5	4	3	2	1	0
INPUT_CLOCK_ZONE_COUNT							
R							
0h							

Table 14-9893. AASRC_CFG_INPUT_CLOCKZONE_COUNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Always read as 0
23:0	INPUT_CLOCK_ZONE_COUNT	R	0h	This gives the value of free running counter at every posedge of sync signal

14.7.1.1.2.93 AASRC_CFG_INPUT_CLOCKZONE_CONTROL_1 Register

14.7.1.1.2.93.1 AASRC_CFG_INPUT_CLOCKZONE_CONTROL_1 Register (Offset = 29Ch) [reset = 0h]

This is the configuration for Input Clock zone 1

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Table 14-9894. Instance Table

Instance Name	Physical Address
AASRC0	02D0 029Ch
AASRC1	02D4 029Ch

Figure 14-4892. AASRC_CFG_INPUT_CLOCKZONE_CONTROL_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED					OVERRIDE_SETTLE_VALUE	OVERRIDE_SETTLE	LOOP_SETUP
R					R/W	R/W	R/W
0h					0h	0h	0h
15	14	13	12	11	10	9	8
LOOP_SETUP							SETTLE
R/W							R
0h							0h
7	6	5	4	3	2	1	0
LOOP_STATE				INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT			
R				R/W			
0h				0h			

Table 14-9895. AASRC_CFG_INPUT_CLOCKZONE_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	R	0h	Always read as 0
18	OVERRIDE_SETTLE_VALUE	R/W	0h	Value written to this field will be used as settle if override settle signal is set
17	OVERRIDE_SETTLE	R/W	0h	This signal override the settle of input clock zone 1 clock recovery loop 0 Settle from clock recovery will be used 1 Value written to override settle value will be used
16:9	LOOP_SETUP	R/W	0h	This is the setting for input clock recovery loop for zone 1 8h00: Slow loop 8h40: Medium1 loop 8h80: Medium2 loop 8hC0: Slow loop
8	SETTLE	R	0h	This signals sets to 1 when clock recovery loop is settled
7:4	LOOP_STATE	R	0h	Loop debug State
3:0	INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT	R/W	0h	This selects the 8x1 and 2x1 mux structure for input clock zone 1 1xxx: Clock comes from output clock gen 0 0000-0111: Selects rxsync signal from 0-7

14.7.1.1.2.94 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_1 Register

14.7.1.1.2.94.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_1 Register (Offset = 2A0h) [reset = 0h]

This is the value of the next timestamp for the Output clock generator a. This contains the 24 bit fractional and the first 8 bits of the integer. This register is used to generate soft clock

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Table 14-9896. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02A0h
AASRC1	02D4 02A0h

Figure 14-4893. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_1 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9897. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.95 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_1 Register

14.7.1.1.2.95.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_1 Register (Offset = 2A4h) [reset = 0h]

This is the value of the next timestamp for the Output clock generator 1. This contains the first 16 bits of the integer. This register is used to generate soft clock

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Table 14-9898. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02A4h
AASRC1	02D4 02A4h

Figure 14-4894. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R/W							
0h							

Table 14-9899. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.96 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_1 Register

14.7.1.1.2.96.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_1 Register (Offset = 2A8h) [reset = 0h]

This is the value of the rate for the clock generator 1. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock

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Table 14-9900. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02A8h
AASRC1	02D4 02A8h

Figure 14-4895. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_1 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9901. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the clock source

14.7.1.1.2.97 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_1 Register

14.7.1.1.2.97.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_1 Register (Offset = 2ACh) [reset = 0h]

This is the value of the rate for the clock generator 1. This contains the upper 16 bits of the integer and the enable for the clock generator. This register is used to generate soft clock

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Table 14-9902. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02ACh
AASRC1	02D4 02ACh

Figure 14-4896. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_1 Name Register

31	30	29	28	27	26	25	24
OUTPUT_CLOCK_GEN_EN	RESERVED						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_INT_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_INT_HI							
R/W							
0h							

Table 14-9903. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OUTPUT_CLOCK_GEN_EN	R/W	0h	This signal enables the Output Clock Generator 1 0 `Clock generator disabled` 1 `Clock generator enabled`
30:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.98 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1 Register

14.7.1.1.2.98.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1 Register (Offset = 2B0h) [reset = 0h]

This is the value of the rate for the Output clock recovery loop 1. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9904. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02B0h
AASRC1	02D4 02B0h

Figure 14-4897. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9905. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the rate for the output clock recovery loop 1
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the rate for the output clock recovery loop 1

14.7.1.1.2.99 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1 Register

14.7.1.1.2.99.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1 Register (Offset = 2B4h) [reset = 0h]

This is the value of the rate for the Output clock recovery loop 1. This contains the upper 16 bits of the Output clock recovery loop

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Table 14-9906. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02B4h
AASRC1	02D4 02B4h

Figure 14-4898. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RATE_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R							
0h							

Table 14-9907. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R	0h	This is the Upper 16 bits of the integer multiple of the rate for the output clock recovery loop 1

14.7.1.1.2.100 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_1 Register

14.7.1.1.2.100.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_1 Register (Offset = 2B8h) [reset = 0h]

This is the value of the timestamp for the Output clock recovery loop 1. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9908. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02B8h
AASRC1	02D4 02B8h

Figure 14-4899. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_1 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9909. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated when output fifo event occurs
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated when output fifo event occurs

14.7.1.1.2.101 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_1 Register

14.7.1.1.2.101.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_1 Register (Offset = 2BCh) [reset = 0h]

This is the value of the next timestamp for the Output clock recovery loop 1. This contains the first 16 bits of the integer

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Table 14-9910. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02BCh
AASRC1	02D4 02BCh

Figure 14-4900. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R							
0h							

Table 14-9911. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock recovery loop This register will be updated when output fifo event occurs

14.7.1.1.2.102 AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_1 Register

14.7.1.1.2.102.1 AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_1 Register (Offset = 2C0h) [reset = 0h]

Free Running counter for clock zone 1

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Table 14-9912. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02C0h
AASRC1	02D4 02C0h

Figure 14-4901. AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							
15	14	13	12	11	10	9	8
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							
7	6	5	4	3	2	1	0
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							

Table 14-9913. AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Always read as 0
23:0	OUTPUT_CLOCK_ZONE_COUNT	R	0h	This gives the value of free running counter at every posedge of sync signal

14.7.1.1.2.103 AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_1 Register

14.7.1.1.2.103.1 AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_1 Register (Offset = 2C4h) [reset = 0h]

This is the configuration for Output Clock zone 1

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Table 14-9914. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02C4h
AASRC1	02D4 02C4h

Figure 14-4902. AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED					OVERRIDE_SETTLE_VALUE	OVERRIDE_SETTLE	LOOP_SETUP
R					R/W	R/W	R/W
0h					0h	0h	0h
15	14	13	12	11	10	9	8
LOOP_SETUP							SETTLE
R/W							R
0h							0h
7	6	5	4	3	2	1	0
LOOP_STATE				OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT			
R				R/W			
0h				0h			

Table 14-9915. AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	R	0h	Always read as 0
18	OVERRIDE_SETTLE_VALUE	R/W	0h	Value written to this field will be used as settle if override settle signal is set
17	OVERRIDE_SETTLE	R/W	0h	This signal override the settle of output clock zone 1 clock recovery loop 0 Settle from clock recovery will be used 1 Value written to override settle value will be used
16:9	LOOP_SETUP	R/W	0h	This is the setting for input clock recovery loop for zone 1 8h00: Slow loop 8h40: Medium1 loop 8h80: Medium2 loop 8hC0: Slow loop
8	SETTLE	R	0h	This signals sets to 1 when clock recovery loop is settled
7:4	LOOP_STATE	R	0h	Loop debug state
3:0	OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT	R/W	0h	This selects the 8x1 and 2x1 mux structure for output clock zone 1 1xxx: Clock comes from output clock gen 0 0000-0111: Selects txsync signal from 0-7

14.7.1.1.2.104 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1 Register

14.7.1.1.2.104.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1 Register (Offset = 2C8h) [reset = 0h]

This is the override value of the rate for the input clock recovery loop 1. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9916. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02C8h
AASRC1	02D4 02C8h

Figure 14-4903. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9917. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the override clock recovery loop 0
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the override clock recovery loop 0

14.7.1.1.2.105 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1 Register

14.7.1.1.2.105.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1 Register (Offset = 2CCh) [reset = 0h]

This is the override value of the rate for the input clock recovery loop 1. This contains the upper 16 bits of the rate input clock recovery loop

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Table 14-9918. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02CCh
AASRC1	02D4 02CCh

Figure 14-4904. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							OVERRIDE_RATE
R							R/W
0h							0h
15	14	13	12	11	10	9	8
RATE_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R/W							
0h							

Table 14-9919. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	OVERRIDE_RATE	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the override clock recovery loop 0
15:0	RATE_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the override clock recovery loop 0

14.7.1.1.2.106 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1 Register

14.7.1.1.2.106.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1 Register (Offset = 2D0h) [reset = 0h]

This is the override value of the rate for the Output clock recovery loop 1. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9920. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02D0h
AASRC1	02D4 02D0h

Figure 14-4905. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9921. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the output override clock recovery loop 1
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the output override clock recovery loop 1

14.7.1.1.2.107 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1 Register

14.7.1.1.2.107.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1 Register (Offset = 2D4h) [reset = 0h]

This is the override value of the rate for the Output clock recovery loop 1. This contains the upper 16 bits of the Output clock recovery loop

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Table 14-9922. Instance Table

Instance Name	Physical Address
AASRC0	02D0 02D4h
AASRC1	02D4 02D4h

Figure 14-4906. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							OVERRIDE_RATE
R							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_INT_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_INT_HI							
R/W							
0h							

Table 14-9923. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	OVERRIDE_RATE	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the output override clock recovery loop 1
15:0	RATE_INT_HI	R/W	0h	This is the Upper 16 bits of the integer multiple of the rate for the output override clock recovery loop 1

14.7.1.1.2.108 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_2 Register

14.7.1.1.2.108.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_2 Register (Offset = 300h) [reset = 0h]

This is the value of the next timestamp for the input clock generator 2. This contains the 24 bit fractional and the first 8 bits of the integer. This register is used to generate soft clock

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Table 14-9924. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0300h
AASRC1	02D4 0300h

Figure 14-4907. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_2 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9925. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.109 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_2 Register

14.7.1.1.2.109.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_2 Register (Offset = 304h) [reset = 0h]

This is the value of the next timestamp for the input clock generator 2. This contains the first 16 bits of the integer. This register is used to generate soft clock.

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Table 14-9926. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0304h
AASRC1	02D4 0304h

Figure 14-4908. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R/W							
0h							

Table 14-9927. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.110 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_2 Register

14.7.1.1.2.110.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_2 Register (Offset = 308h) [reset = 0h]

This is the value of the rate for the clock generator 2. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock

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Table 14-9928. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0308h
AASRC1	02D4 0308h

Figure 14-4909. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_2 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9929. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the clock source

14.7.1.1.2.111 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_2 Register

14.7.1.1.2.111.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_2 Register (Offset = 30Ch) [reset = 0h]

This is the value of the rate for the clock generator 2. This contains the upper 16 bits of the integer and the enable for the clock generator. This register is used to generate soft clock

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Table 14-9930. Instance Table

Instance Name	Physical Address
AASRC0	02D0 030Ch
AASRC1	02D4 030Ch

Figure 14-4910. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_2 Name Register

31	30	29	28	27	26	25	24
INPUT_CLK_GEN_EN	RESERVED						
R/W	R						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RATE_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R/W							
0h							

Table 14-9931. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INPUT_CLK_GEN_EN	R/W	0h	This signal enables the Input Clock Generator 2 0 Clock generator disabled 1 Clock generator enabled
30:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.112 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2 Register

14.7.1.1.2.112.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2 Register (Offset = 310h) [reset = 0h]

This is the value of the rate for the input clock recovery loop 2. This contains the 24 bit fractional and the first 8 bits of the integer.

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Table 14-9932. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0310h
AASRC1	02D4 0310h

Figure 14-4911. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9933. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the rate for the input clock recovery loop 2
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the rate for the input clock recovery loop 2

14.7.1.1.2.113 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2 Register

14.7.1.1.2.113.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2 Register (Offset = 314h) [reset = 0h]

This is the value of the rate for the input clock recovery loop 2. This contains the upper 16 bits of the rate input clock recovery loop

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Table 14-9934. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0314h
AASRC1	02D4 0314h

Figure 14-4912. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RATE_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R							
0h							

Table 14-9935. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R	0h	This is the upper 16 bits of the integer multiple of the rate for the input clock recovery loop 2

14.7.1.1.2.114 AASRC_CFG_INPUT_CLOCKZONE_COUNT_2 Register

14.7.1.1.2.114.1 AASRC_CFG_INPUT_CLOCKZONE_COUNT_2 Register (Offset = 318h) [reset = 0h]

Free Running counter for clock zone 2

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Table 14-9936. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0318h
AASRC1	02D4 0318h

Figure 14-4913. AASRC_CFG_INPUT_CLOCKZONE_COUNT_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
INPUT_CLOCK_ZONE_COUNT							
R							
0h							
15	14	13	12	11	10	9	8
INPUT_CLOCK_ZONE_COUNT							
R							
0h							
7	6	5	4	3	2	1	0
INPUT_CLOCK_ZONE_COUNT							
R							
0h							

Table 14-9937. AASRC_CFG_INPUT_CLOCKZONE_COUNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Always read as 0
23:0	INPUT_CLOCK_ZONE_COUNT	R	0h	This gives the value of free running counter at every posedge of sync signal

14.7.1.1.2.115 AASRC_CFG_INPUT_CLOCKZONE_CONTROL_2 Register

14.7.1.1.2.115.1 AASRC_CFG_INPUT_CLOCKZONE_CONTROL_2 Register (Offset = 31Ch) [reset = 0h]

This is the configuration for Input Clock zone 2

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Table 14-9938. Instance Table

Instance Name	Physical Address
AASRC0	02D0 031Ch
AASRC1	02D4 031Ch

Figure 14-4914. AASRC_CFG_INPUT_CLOCKZONE_CONTROL_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td>OVERRIDE_SETTLE_VALUE</td><td>OVERRIDE_SETTLE</td><td>LOOP_SETUP</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">LOOP_SETUP</td><td>SETTLE</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">LOOP_STATE</td><td colspan="4">INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9939. AASRC_CFG_INPUT_CLOCKZONE_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	R	0h	Always read as 0
18	OVERRIDE_SETTLE_VALUE	R/W	0h	Value written to this field will be used as settle if override settle signal is set
17	OVERRIDE_SETTLE	R/W	0h	This signal override the settle of input clock zone 2 clock recovery loop 0 `Settle from clock recovery will be used` 1 `Value written to override settle value will be used`
16:9	LOOP_SETUP	R/W	0h	This is the setting for input clock recovery loop for zone 2 8h00: Slow loop 8h40: Medium1 loop 8h80: Medium2 loop 8hC0: Slow loop
8	SETTLE	R	0h	This signals sets to 1 when clock recovery loop is settled
7:4	LOOP_STATE	R	0h	Loop debug State
3:0	INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT	R/W	0h	This selects the 8x1 and 2x1 mux structure for input clock zone 2 1xxx: Clock comes from output clock gen 0 0000-0111: Selects rxsync signal from 0-7

14.7.1.1.2.116 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_2 Register

14.7.1.1.2.116.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_2 Register (Offset = 320h) [reset = 0h]

This is the value of the next timestamp for the Output clock generator a. This contains the 24 bit fractional and the first 8 bits of the integer. . This register is used to generate soft clock

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Table 14-9940. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0320h
AASRC1	02D4 0320h

Figure 14-4915. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_2 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9941. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.117 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_2 Register

14.7.1.1.2.117.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_2 Register (Offset = 324h) [reset = 0h]

This is the value of the next timestamp for the Output clock generator 2. This contains the first 16 bits of the integer. This register is used to generate soft clock

Return to Summary Table

Table 14-9942. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0324h
AASRC1	02D4 0324h

Figure 14-4916. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">STAMP_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">STAMP_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9943. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.118 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_2 Register

14.7.1.1.2.118.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_2 Register (Offset = 328h) [reset = 0h]

This is the value of the rate for the clock generator 2. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock

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Table 14-9944. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0328h
AASRC1	02D4 0328h

Figure 14-4917. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_2 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9945. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the clock source

14.7.1.1.2.119 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_2 Register

14.7.1.1.2.119.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_2 Register (Offset = 32Ch) [reset = 0h]

This is the value of the rate for the clock generator 2. This contains the upper 16 bits of the integer and the enable for the clock generator. This register is used to generate soft clock

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Table 14-9946. Instance Table

Instance Name	Physical Address
AASRC0	02D0 032Ch
AASRC1	02D4 032Ch

Figure 14-4918. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_2 Name Register

31	30	29	28	27	26	25	24
OUTPUT_CLOCK_GEN_EN	RESERVED						
R/W	R						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RATE_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R/W							
0h							

Table 14-9947. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description

31	OUTPUT_CLOCK_GEN_EN	R/W	0h	This signal enables the Output Clock Generator 2
				`0 Clock generator disabled`
				`1 Clock generator enabled`

30:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.120 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2 Register

14.7.1.1.2.120.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2 Register (Offset = 330h) [reset = 0h]

This is the value of the rate for the Output clock recovery loop 2. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9948. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0330h
AASRC1	02D4 0330h

Figure 14-4919. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9949. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the rate for the output clock recovery loop 2
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the rate for the output clock recovery loop 2

14.7.1.1.2.121 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2 Register

14.7.1.1.2.121.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2 Register (Offset = 334h) [reset = 0h]

This is the value of the rate for the Output clock recovery loop 2. This contains the upper 16 bits of the Output clock recovery loop

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Table 14-9950. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0334h
AASRC1	02D4 0334h

Figure 14-4920. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9951. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R	0h	This is the Upper 16 bits of the integer multiple of the rate for the output clock recovery loop 2

14.7.1.1.2.122 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_2 Register

14.7.1.1.2.122.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_2 Register (Offset = 338h) [reset = 0h]

This is the value of the timestamp for the Output clock recovery loop 2. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9952. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0338h
AASRC1	02D4 0338h

Figure 14-4921. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_2 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9953. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated when output fifo event occurs
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated when output fifo event occurs

14.7.1.1.2.123 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_2 Register

14.7.1.1.2.123.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_2 Register (Offset = 33Ch) [reset = 0h]

This is the value of the next timestamp for the Output clock recovery loop 2. This contains the first 16 bits of the integer

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Table 14-9954. Instance Table

Instance Name	Physical Address
AASRC0	02D0 033Ch
AASRC1	02D4 033Ch

Figure 14-4922. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">STAMP_INT_HI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">STAMP_INT_HI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9955. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock recovery loop This register will be updated when output fifo event occurs

14.7.1.1.2.124 AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_2 Register

14.7.1.1.2.124.1 AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_2 Register (Offset = 340h) [reset = 0h]

Free Running counter for clock zone 2

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Table 14-9956. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0340h
AASRC1	02D4 0340h

Figure 14-4923. AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							
15	14	13	12	11	10	9	8
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							
7	6	5	4	3	2	1	0
OUTPUT_CLOCK_ZONE_COUNT							
R							
0h							

Table 14-9957. AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Always read as 0
23:0	OUTPUT_CLOCK_ZONE_COUNT	R	0h	This gives the value of free running counter at every posedge of sync signal

14.7.1.1.2.125 AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_2 Register

14.7.1.1.2.125.1 AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_2 Register (Offset = 344h) [reset = 0h]

This is the configuration for Output Clock zone 2

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Table 14-9958. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0344h
AASRC1	02D4 0344h

Figure 14-4924. AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED					OVERRIDE_SETTLE_VALUE	OVERRIDE_SETTLE	LOOP_SETUP
R					R/W	R/W	R/W
0h					0h	0h	0h
15	14	13	12	11	10	9	8
LOOP_SETUP							SETTLE
R/W							R
0h							0h
7	6	5	4	3	2	1	0
LOOP_STATE				OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT			
R				R/W			
0h				0h			

Table 14-9959. AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	R	0h	Always read as 0
18	OVERRIDE_SETTLE_VALUE	R/W	0h	Value written to this field will be used as settle if override settle signal is set
17	OVERRIDE_SETTLE	R/W	0h	This signal override the settle of output clock zone 2 clock recovery loop 0 Settle from clock recovery will be used 1 Value written to override settle value will be used
16:9	LOOP_SETUP	R/W	0h	This is the setting for input clock recovery loop for zone 2 8h00: Slow loop 8h40: Medium1 loop 8h80: Medium2 loop 8hC0: Slow loop
8	SETTLE	R	0h	This signals sets to 1 when clock recovery loop is settled
7:4	LOOP_STATE	R	0h	Loop debug state
3:0	OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT	R/W	0h	This selects the 8x1 and 2x1 mux structure for output clock zone 2 1xxx: Clock comes from output clock gen 0 0000-0111: Selects txsync signal from 0-7

14.7.1.1.2.126 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2 Register

14.7.1.1.2.126.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2 Register (Offset = 348h) [reset = 0h]

This is the override value of the rate for the input clock recovery loop 2. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9960. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0348h
AASRC1	02D4 0348h

Figure 14-4925. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RATE_INT_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9961. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the override clock recovery loop 2
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the override clock recovery loop 2

14.7.1.1.2.127 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2 Register

14.7.1.1.2.127.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2 Register (Offset = 34Ch) [reset = 0h]

This is the override value of the rate for the input clock recovery loop 2. This contains the upper 16 bits of the rate input clock recovery loop

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Table 14-9962. Instance Table

Instance Name	Physical Address
AASRC0	02D0 034Ch
AASRC1	02D4 034Ch

Figure 14-4926. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>OVERRIDE_RATE</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9963. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	OVERRIDE_RATE	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the override clock recovery loop 2
15:0	RATE_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the override clock recovery loop 2

14.7.1.1.2.128 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2 Register

14.7.1.1.2.128.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2 Register (Offset = 350h) [reset = 0h]

This is the override value of the rate for the Output clock recovery loop 2. This contains the 24 bit fractional and the first 8 bits of the integer

Return to Summary Table

Table 14-9964. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0350h
AASRC1	02D4 0350h

Figure 14-4927. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9965. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the output override clock recovery loop 2
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the output override clock recovery loop 2

14.7.1.1.2.129 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2 Register

14.7.1.1.2.129.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2 Register (Offset = 354h) [reset = 0h]

This is the override value of the rate for the Output clock recovery loop 2. This contains the upper 16 bits of the Output clock recovery loop

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Table 14-9966. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0354h
AASRC1	02D4 0354h

Figure 14-4928. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							OVERRIDE_RATE
R							R/W
0h							0h
15	14	13	12	11	10	9	8
RATE_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R/W							
0h							

Table 14-9967. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	OVERRIDE_RATE	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the output override clock recovery loop 2
15:0	RATE_INT_HI	R/W	0h	This is the Upper 16 bits of the integer multiple of the rate for the output override clock recovery loop 2

14.7.1.1.2.130 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_3 Register

14.7.1.1.2.130.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_3 Register (Offset = 380h) [reset = 0h]

This is the value of the next timestamp for the input clock generator 3. This contains the 24 bit fractional and the first 8 bits of the integer. This register is used to generate soft clock

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Table 14-9968. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0380h
AASRC1	02D4 0380h

Figure 14-4929. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_3 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9969. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.131 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_3 Register

14.7.1.1.2.131.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_3 Register (Offset = 384h) [reset = 0h]

This is the value of the next timestamp for the input clock generator 3. This contains the first 16 bits of the integer. This register is used to generate soft clock

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Table 14-9970. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0384h
AASRC1	02D4 0384h

Figure 14-4930. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">STAMP_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">STAMP_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9971. AASRC_CFG_INPUT_CLOCK_GENERATOR_STAMP_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.132 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_3 Register

14.7.1.1.2.132.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_3 Register (Offset = 388h) [reset = 0h]

This is the value of the rate for the clock generator 3. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock

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Table 14-9972. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0388h
AASRC1	02D4 0388h

Figure 14-4931. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_3 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9973. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the clock source

14.7.1.1.2.133 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_3 Register

14.7.1.1.2.133.1 AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_3 Register (Offset = 38Ch) [reset = 0h]

This is the value of the rate for the clock generator 3. This contains the upper 16 bits of the integer and the enable for the clock generator. This register is used to generate soft clock

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Table 14-9974. Instance Table

Instance Name	Physical Address
AASRC0	02D0 038Ch
AASRC1	02D4 038Ch

Figure 14-4932. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_3 Name Register

31	30	29	28	27	26	25	24
INPUT_CLK_GEN_EN	RESERVED						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_INT_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_INT_HI							
R/W							
0h							

Table 14-9975. AASRC_CFG_INPUT_CLOCK_GENERATOR_RATE_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description

31	INPUT_CLK_GEN_EN	R/W	0h	This signal enables the Input Clock Generator 3
				`0 Clock generator disabled`
				`1 Clock generator enabled`

30:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.134 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3 Register

14.7.1.1.2.134.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3 Register (Offset = 390h) [reset = 0h]

This is the value of the rate for the input clock recovery loop 3. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9976. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0390h
AASRC1	02D4 0390h

Figure 14-4933. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9977. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the rate for the input clock recovery loop 3
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the rate for the input clock recovery loop 3

14.7.1.1.2.135 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3 Register

14.7.1.1.2.135.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3 Register (Offset = 394h) [reset = 0h]

This is the value of the rate for the input clock recovery loop 3. This contains the upper 16 bits of the rate input clock recovery loop

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Table 14-9978. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0394h
AASRC1	02D4 0394h

Figure 14-4934. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9979. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R	0h	This is the upper 16 bits of the integer multiple of the rate for the input clock recovery loop 3

14.7.1.1.2.136 AASRC_CFG_INPUT_CLOCKZONE_COUNT_3 Register

14.7.1.1.2.136.1 AASRC_CFG_INPUT_CLOCKZONE_COUNT_3 Register (Offset = 398h) [reset = 0h]

Free Running counter for clock zone 3

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Table 14-9980. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0398h
AASRC1	02D4 0398h

Figure 14-4935. AASRC_CFG_INPUT_CLOCKZONE_COUNT_3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INPUT_CLOCK_ZONE_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">INPUT_CLOCK_ZONE_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INPUT_CLOCK_ZONE_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9981. AASRC_CFG_INPUT_CLOCKZONE_COUNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Always read as 0
23:0	INPUT_CLOCK_ZONE_COUNT	R	0h	This gives the value of free running counter at every posedge of sync signal

14.7.1.1.2.137 AASRC_CFG_INPUT_CLOCKZONE_CONTROL_3 Register

14.7.1.1.2.137.1 AASRC_CFG_INPUT_CLOCKZONE_CONTROL_3 Register (Offset = 39Ch) [reset = 0h]

This is the configuration for Input Clock zone 3

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Table 14-9982. Instance Table

Instance Name	Physical Address
AASRC0	02D0 039Ch
AASRC1	02D4 039Ch

Figure 14-4936. AASRC_CFG_INPUT_CLOCKZONE_CONTROL_3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td>OVERRIDE_SETTLE_VALUE</td><td>OVERRIDE_SETTLE</td><td>LOOP_SETUP</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">LOOP_SETUP</td><td>SETTLE</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">LOOP_STATE</td><td colspan="4">INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-9983. AASRC_CFG_INPUT_CLOCKZONE_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	R	0h	Always read as 0
18	OVERRIDE_SETTLE_VALUE	R/W	0h	Value written to this field will be used as settle if override settle signal is set
17	OVERRIDE_SETTLE	R/W	0h	This signal override the settle of input clock zone 3 clock recovery loop 0 Settle from clock recovery will be used 1 Value written to override settle value will be used
16:9	LOOP_SETUP	R/W	0h	This is the setting for input clock recovery loop for zone 3 8h00: Slow loop 8h40: Medium1 loop 8h80: Medium2 loop 8hC0: Slow loop
8	SETTLE	R	0h	This signals sets to 1 when clock recovery loop is settled
7:4	LOOP_STATE	R	0h	Loop debug State
3:0	INPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT	R/W	0h	This selects the 8x1 and 2x1 mux structure for input clock zone 3 1xxx: Clock comes from output clock gen 0 0000-0111: Selects rxsync signal from 0-7

14.7.1.1.2.138 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_3 Register

14.7.1.1.2.138.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_3 Register (Offset = 3A0h) [reset = 0h]

This is the value of the next timestamp for the Output clock generator a. This contains the 24 bit fractional and the first 8 bits of the integer. . This register is used to generate soft clock

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Table 14-9984. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03A0h
AASRC1	02D4 03A0h

Figure 14-4937. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_3 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9985. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.139 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_3 Register

14.7.1.1.2.139.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_3 Register (Offset = 3A4h) [reset = 0h]

This is the value of the next timestamp for the Output clock generator 3. This contains the first 16 bits of the integer. This register is used to generate soft clock

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Table 14-9986. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03A4h
AASRC1	02D4 03A4h

Figure 14-4938. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R/W							
0h							

Table 14-9987. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_STAMP_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock source This register will be updated by adding the Clock Generator Rate to the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.140 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_3 Register

14.7.1.1.2.140.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_3 Register (Offset = 3A8h) [reset = 0h]

This is the value of the rate for the clock generator 3. This contains the 24 bit fractional and the first 8 bits of the integer. This is based on a free running counter running on sys_clk. This register is used to generate soft clock

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Table 14-9988. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03A8h
AASRC1	02D4 03A8h

Figure 14-4939. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_3 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-9989. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the clock source

14.7.1.1.2.141 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_3 Register

14.7.1.1.2.141.1 AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_3 Register (Offset = 3ACh) [reset = 0h]

This is the value of the rate for the clock generator 3. This contains the upper 16 bits of the integer and the enable for the clock generator. This register is used to generate soft clock

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Table 14-9990. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03ACh
AASRC1	02D4 03ACh

Figure 14-4940. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_3 Name Register

31	30	29	28	27	26	25	24
OUTPUT_CLOCK_GEN_EN	RESERVED						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RATE_INT_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RATE_INT_HI							
R/W							
0h							

Table 14-9991. AASRC_CFG_OUTPUT_CLOCK_GENERATOR_RATE_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description

31	OUTPUT_CLOCK_GEN_EN	R/W	0h	This signal enables the Output Clock Generator 3
				`0 Clock generator disabled`
				`1 Clock generator enabled`

30:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the clock source This register will be added with the Clock Generator Stamp to update the Stamp value whenever the Free Running Counter passes the Stamp value

14.7.1.1.2.142 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3 Register

14.7.1.1.2.142.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3 Register (Offset = 3B0h) [reset = 0h]

This is the value of the rate for the Output clock recovery loop 3. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9992. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03B0h
AASRC1	02D4 03B0h

Figure 14-4941. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RATE_INT_LO</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FRACTIONAL_STAMP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-9993. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the rate for the output clock recovery loop 3
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the rate for the output clock recovery loop 3

14.7.1.1.2.143 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3 Register

14.7.1.1.2.143.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3 Register (Offset = 3B4h) [reset = 0h]

This is the value of the rate for the Output clock recovery loop 3. This contains the upper 16 bits of the Output clock recovery loop

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Table 14-9994. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03B4h
AASRC1	02D4 03B4h

Figure 14-4942. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RATE_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R							
0h							

Table 14-9995. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_RATE_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	RATE_INT_HI	R	0h	This is the Upper 16 bits of the integer multiple of the rate for the output clock recovery loop 3

14.7.1.1.2.144 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_3 Register

14.7.1.1.2.144.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_3 Register (Offset = 3B8h) [reset = 0h]

This is the value of the timestamp for the Output clock recovery loop 3. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-9996. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03B8h
AASRC1	02D4 03B8h

Figure 14-4943. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_3 Name Register

31	30	29	28	27	26	25	24
STAMP_INT_LO							
R							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R							
0h							

Table 14-9997. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	STAMP_INT_LO	R	0h	This is the lower 8 bits of the integer multiple of the next timestamp for the clock source This register will be updated when output fifo event occurs
23:0	FRACTIONAL_STAMP	R	0h	This is the fractional portion of the next timestamp for the clock source This register will be updated when output fifo event occurs

14.7.1.1.2.145 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_3 Register

14.7.1.1.2.145.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_3 Register (Offset = 3BCh) [reset = 0h]

This is the value of the next timestamp for the Output clock recovery loop 3. This contains the first 16 bits of the integer

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Table 14-9998. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03BCh
AASRC1	02D4 03BCh

Figure 14-4944. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAMP_INT_HI							
R							
0h							
7	6	5	4	3	2	1	0
STAMP_INT_HI							
R							
0h							

Table 14-9999. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_STAMP_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Always read as 0
15:0	STAMP_INT_HI	R	0h	This is the upper 16 bits of the integer multiple of the next timestamp for the clock recovery loop This register will be updated when output fifo event occurs

14.7.1.1.2.146 AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_3 Register

14.7.1.1.2.146.1 AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_3 Register (Offset = 3C0h) [reset = 0h]

Free Running counter for clock zone 3

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Table 14-10000. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03C0h
AASRC1	02D4 03C0h

Figure 14-4945. AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OUTPUT_CLOCK_ZONE_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUTPUT_CLOCK_ZONE_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUTPUT_CLOCK_ZONE_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10001. AASRC_CFG_OUTPUT_CLOCKZONE_COUNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Always read as 0
23:0	OUTPUT_CLOCK_ZONE_COUNT	R	0h	This gives the value of free running counter at every posedge of sync signal

14.7.1.1.2.147 AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_3 Register

14.7.1.1.2.147.1 AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_3 Register (Offset = 3C4h) [reset = 0h]

This is the configuration for Output Clock zone 3

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Table 14-10002. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03C4h
AASRC1	02D4 03C4h

Figure 14-4946. AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					OVERRIDE_SETTLE_VALUE	OVERRIDE_SETTLE	LOOP_SETUP
R					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOOP_SETUP							SETTLE
R/W							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOOP_STATE				OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT			
R				R/W			
0h				0h			

Table 14-10003. AASRC_CFG_OUTPUT_CLOCKZONE_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	R	0h	Always read as 0
18	OVERRIDE_SETTLE_VALUE	R/W	0h	Value written to this field will be used as settle if override settle signal is set
17	OVERRIDE_SETTLE	R/W	0h	This signal override the settle of output clock zone 3 clock recovery loop 0 Settle from clock recovery will be used 1 Value written to override settle value will be used
16:9	LOOP_SETUP	R/W	0h	This is the setting for input clock recovery loop for zone 3 8h00: Slow loop 8h40: Medium1 loop 8h80: Medium2 loop 8hC0: Slow loop
8	SETTLE	R	0h	This signals sets to 1 when clock recovery loop is settled
7:4	LOOP_STATE	R	0h	Loop debug state
3:0	OUTPUT_CLOCK_ZONE_CLOCK_SOURCE_SELECT	R/W	0h	This selects the 8x1 and 2x1 mux structure for output clock zone 3 1xxx: Clock comes from output clock gen 0 0000-0111: Selects txsync signal from 0-7

14.7.1.1.2.148 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3 Register

14.7.1.1.2.148.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3 Register (Offset = 3C8h) [reset = 0h]

This is the override value of the rate for the input clock recovery loop 3. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-10004. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03C8h
AASRC1	02D4 03C8h

Figure 14-4947. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-10005. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the override clock recovery loop 3
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the override clock recovery loop 3

14.7.1.1.2.149 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3 Register

14.7.1.1.2.149.1 AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3 Register (Offset = 3CCh) [reset = 0h]

This is the override value of the rate for the input clock recovery loop 3. This contains the upper 16 bits of the rate input clock recovery loop

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Table 14-10006. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03CCh
AASRC1	02D4 03CCh

Figure 14-4948. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED</td><td>OVERRIDE_RATE</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RATE_INT_HI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10007. AASRC_CFG_INPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	OVERRIDE_RATE	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the override clock recovery loop 3
15:0	RATE_INT_HI	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the override clock recovery loop 3

14.7.1.1.2.150 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3 Register

14.7.1.1.2.150.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3 Register (Offset = 3D0h) [reset = 0h]

This is the override value of the rate for the Output clock recovery loop 3. This contains the 24 bit fractional and the first 8 bits of the integer

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Table 14-10008. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03D0h
AASRC1	02D4 03D0h

Figure 14-4949. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3 Name Register

31	30	29	28	27	26	25	24
RATE_INT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
FRACTIONAL_STAMP							
R/W							
0h							
15	14	13	12	11	10	9	8
FRACTIONAL_STAMP							
R/W							
0h							
7	6	5	4	3	2	1	0
FRACTIONAL_STAMP							
R/W							
0h							

Table 14-10009. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_LO_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RATE_INT_LO	R/W	0h	This is the lower 8 bits of the integer multiple of the rate for the output override clock recovery loop 3
23:0	FRACTIONAL_STAMP	R/W	0h	This is the fractional portion of the rate for the output override clock recovery loop 3

14.7.1.1.2.151 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3 Register

14.7.1.1.2.151.1 AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3 Register (Offset = 3D4h) [reset = 0h]

This is the override value of the rate for the Output clock recovery loop 3. This contains the upper 16 bits of the Output clock recovery loop

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Table 14-10010. Instance Table

Instance Name	Physical Address
AASRC0	02D0 03D4h
AASRC1	02D4 03D4h

Figure 14-4950. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							OVERRIDE_RATE
R							R/W
0h							0h
15	14	13	12	11	10	9	8
RATE_INT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
RATE_INT_HI							
R/W							
0h							

Table 14-10011. AASRC_CFG_OUTPUT_CLOCK_RECOVERY_LOOP_OVERRIDE_RATE_HI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	Always read as 0
16	OVERRIDE_RATE	R/W	0h	This is the upper 16 bits of the integer multiple of the rate for the output override clock recovery loop 3
15:0	RATE_INT_HI	R/W	0h	This is the Upper 16 bits of the integer multiple of the rate for the output override clock recovery loop 3

14.7.1.1.2.152 AASRC_CFG_INPUT_CLOCK_ZONE_DIVIDER Register

14.7.1.1.2.152.1 AASRC_CFG_INPUT_CLOCK_ZONE_DIVIDER Register (Offset = 400h) [reset = 10001h]

This is the configuration for Clock divider of input zone 0 and input zone1

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Table 14-10012. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0400h
AASRC1	02D4 0400h

Figure 14-4951. AASRC_CFG_INPUT_CLOCK_ZONE_DIVIDER Name Register

31	30	29	28	27	26	25	24
RESERVED	CLOCK_ZONE1_DIVIDE_EN	CLOCK_ZONE1_DIVIDE					
R	R/W	R/W					
0h	0h	1h					

23	22	21	20	19	18	17	16
CLOCK_ZONE1_DIVIDE							
R/W							
1h							

15	14	13	12	11	10	9	8
RESERVED1	CLOCK_ZONE0_DIVIDE_EN	CLOCK_ZONE0_DIVIDE					
R	R/W	R/W					
0h	0h	1h					

7	6	5	4	3	2	1	0
CLOCK_ZONE0_DIVIDE							
R/W							
1h							

Table 14-10013. AASRC_CFG_INPUT_CLOCK_ZONE_DIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Always read as 0
30	CLOCK_ZONE1_DIVIDE_EN	R/W	0h	Clock zone 1 divider enable 1'b1:Divider logic enable 1'b0:Divider logic disable 0 Clock divider disabled 1 Clock divider enabled
29:16	CLOCK_ZONE1_DIVIDE	R/W	1h	This is the setting for input clock zone1 sync signal division value
15	RESERVED1	R	0h	Always read as 0
14	CLOCK_ZONE0_DIVIDE_EN	R/W	0h	Clock zone 0 divider enable 1'b1:Divider logic enable 1'b0:Divider logic disable 0 Clock divider disabled 1 Clock divider enabled
13:0	CLOCK_ZONE0_DIVIDE	R/W	1h	This is the setting for input clock zone0 sync signal division value

14.7.1.1.2.153 AASRC_CFG_OUTPUT_CLOCK_ZONE_DIVIDER Register

14.7.1.1.2.153.1 AASRC_CFG_OUTPUT_CLOCK_ZONE_DIVIDER Register (Offset = 404h) [reset = 10001h]

This is the configuration for Clock divider of output zone 0 and output zone1

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Table 14-10014. Instance Table

Instance Name	Physical Address
AASRC0	02D0 0404h
AASRC1	02D4 0404h

Figure 14-4952. AASRC_CFG_OUTPUT_CLOCK_ZONE_DIVIDER Name Register

31	30	29	28	27	26	25	24
RESERVED	CLOCK_ZONE1_DIVIDE_EN	CLOCK_ZONE1_DIVIDE					
R	R/W	R/W					
0h	0h	1h					
23	22	21	20	19	18	17	16
CLOCK_ZONE1_DIVIDE							
R/W							
1h							
15	14	13	12	11	10	9	8
RESERVED1	CLOCK_ZONE0_DIVIDE_EN	CLOCK_ZONE0_DIVIDE					
R	R/W	R/W					
0h	0h	1h					
7	6	5	4	3	2	1	0
CLOCK_ZONE0_DIVIDE							
R/W							
1h							

Table 14-10015. AASRC_CFG_OUTPUT_CLOCK_ZONE_DIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Always read as 0

30	CLOCK_ZONE1_DIVIDE_EN	R/W	0h	Clock zone 1 divider enable 1'b1:Divider logic enable 1'b0:Divider logic disable
				`0 Clock divider disabled`
				`1 Clock divider enabled`

29:16	CLOCK_ZONE1_DIVIDE	R/W	1h	This is the setting for output clock zone1 sync signal division value
15	RESERVED1	R	0h	Always read as 0

14	CLOCK_ZONE0_DIVIDE_EN	R/W	0h	Clock zone 0 divider enable 1'b1:Divider logic enable 1'b0:Divider logic disable
				`0 Clock divider disabled`
				`1 Clock divider enabled`

13:0	CLOCK_ZONE0_DIVIDE	R/W	1h	This is the setting for output clock zone0 sync signal division value

14.7.1.1.2.154 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L0 Register

14.7.1.1.2.154.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L0 Register (Offset = 0h) [reset = 0h]

This is where the input samples are written for stream0 left channel

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Table 14-10016. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0000h
AASRC1	02D5 0000h

Figure 14-4953. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L0 Name Register

31	30	29	28	27	26	25	24
IN_DATA0							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA0							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA0							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA0							
R/W							
0h							

Table 14-10017. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA0	R/W	0h	This is where the input samples are written for stream0 left channel

14.7.1.1.2.155 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R0 Register

14.7.1.1.2.155.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R0 Register (Offset = 4h) [reset = 0h]

This is where the input samples are written for stream0 right channel

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Table 14-10018. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0004h
AASRC1	02D5 0004h

Figure 14-4954. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R0 Name Register

31	30	29	28	27	26	25	24
IN_DATA1							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA1							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA1							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA1							
R/W							
0h							

Table 14-10019. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA1	R/W	0h	This is where the input samples are written for stream0 right channel

14.7.1.1.2.156 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L1 Register

14.7.1.1.2.156.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L1 Register (Offset = 8h) [reset = 0h]

This is where the input samples are written for stream1 left channel

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Table 14-10020. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0008h
AASRC1	02D5 0008h

Figure 14-4955. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L1 Name Register

31	30	29	28	27	26	25	24
IN_DATA2							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA2							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA2							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA2							
R/W							
0h							

Table 14-10021. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA2	R/W	0h	This is where the input samples are written for stream1 left channel

14.7.1.1.2.157 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R1 Register

14.7.1.1.2.157.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R1 Register (Offset = Ch) [reset = 0h]

This is where the input samples are written for stream1 right channel

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Table 14-10022. Instance Table

Instance Name	Physical Address
AASRC0	02D1 000Ch
AASRC1	02D5 000Ch

Figure 14-4956. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R1 Name Register

31	30	29	28	27	26	25	24
IN_DATA3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IN_DATA3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IN_DATA3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IN_DATA3							
R/W							
0h							

Table 14-10023. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA3	R/W	0h	This is where the input samples are written for stream1 right channel

14.7.1.1.2.158 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L2 Register

14.7.1.1.2.158.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L2 Register (Offset = 10h) [reset = 0h]

This is where the input samples are written for stream2 left channel

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Table 14-10024. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0010h
AASRC1	02D5 0010h

Figure 14-4957. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IN_DATA4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IN_DATA4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IN_DATA4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IN_DATA4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10025. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA4	R/W	0h	This is where the input samples are written for stream2 left channel

14.7.1.1.2.159 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R2 Register

14.7.1.1.2.159.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R2 Register (Offset = 14h) [reset = 0h]

This is where the input samples are written for stream2 right channel

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Table 14-10026. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0014h
AASRC1	02D5 0014h

Figure 14-4958. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R2 Name Register

31	30	29	28	27	26	25	24
IN_DATA5							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA5							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA5							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA5							
R/W							
0h							

Table 14-10027. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA5	R/W	0h	This is where the input samples are written for stream2 right channel

14.7.1.1.2.160 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L3 Register

14.7.1.1.2.160.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L3 Register (Offset = 18h) [reset = 0h]

This is where the input samples are written for stream3 left channel

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Table 14-10028. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0018h
AASRC1	02D5 0018h

Figure 14-4959. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L3 Name Register

31	30	29	28	27	26	25	24
IN_DATA6							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA6							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA6							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA6							
R/W							
0h							

Table 14-10029. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA6	R/W	0h	This is where the input samples are written for stream3 left channel

14.7.1.1.2.161 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R3 Register

14.7.1.1.2.161.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R3 Register (Offset = 1Ch) [reset = 0h]

This is where the input samples are written for stream3 right channel

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Table 14-10030. Instance Table

Instance Name	Physical Address
AASRC0	02D1 001Ch
AASRC1	02D5 001Ch

Figure 14-4960. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R3 Name Register

31	30	29	28	27	26	25	24
IN_DATA7							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA7							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA7							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA7							
R/W							
0h							

Table 14-10031. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA7	R/W	0h	This is where the input samples are written for stream3 right channel

14.7.1.1.2.162 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L4 Register

14.7.1.1.2.162.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L4 Register (Offset = 20h) [reset = 0h]

This is where the input samples are written for stream4 left channel

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Table 14-10032. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0020h
AASRC1	02D5 0020h

Figure 14-4961. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L4 Name Register

31	30	29	28	27	26	25	24
IN_DATA8							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA8							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA8							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA8							
R/W							
0h							

Table 14-10033. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA8	R/W	0h	This is where the input samples are written for stream4 left channel

14.7.1.1.2.163 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R4 Register

14.7.1.1.2.163.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R4 Register (Offset = 24h) [reset = 0h]

This is where the input samples are written for stream4 right channel

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Table 14-10034. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0024h
AASRC1	02D5 0024h

Figure 14-4962. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R4 Name Register

31	30	29	28	27	26	25	24
IN_DATA9							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA9							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA9							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA9							
R/W							
0h							

Table 14-10035. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA9	R/W	0h	This is where the input samples are written for stream4 right channel

14.7.1.1.2.164 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L5 Register

14.7.1.1.2.164.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L5 Register (Offset = 28h) [reset = 0h]

This is where the input samples are written for stream5 left channel

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Table 14-10036. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0028h
AASRC1	02D5 0028h

Figure 14-4963. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L5 Name Register

31	30	29	28	27	26	25	24
IN_DATA10							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA10							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA10							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA10							
R/W							
0h							

Table 14-10037. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA10	R/W	0h	This is where the input samples are written for stream5 left channel

14.7.1.1.2.165 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R5 Register

14.7.1.1.2.165.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R5 Register (Offset = 2Ch) [reset = 0h]

This is where the input samples are written for stream5 right channel

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Table 14-10038. Instance Table

Instance Name	Physical Address
AASRC0	02D1 002Ch
AASRC1	02D5 002Ch

Figure 14-4964. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R5 Name Register

31	30	29	28	27	26	25	24
IN_DATA11							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA11							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA11							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA11							
R/W							
0h							

Table 14-10039. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA11	R/W	0h	This is where the input samples are written for stream5 right channel

14.7.1.1.2.166 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L6 Register

14.7.1.1.2.166.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L6 Register (Offset = 30h) [reset = 0h]

This is where the input samples are written for stream6 left channel

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Table 14-10040. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0030h
AASRC1	02D5 0030h

Figure 14-4965. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L6 Name Register

31	30	29	28	27	26	25	24
IN_DATA12							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA12							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA12							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA12							
R/W							
0h							

Table 14-10041. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA12	R/W	0h	This is where the input samples are written for stream6 left channel

14.7.1.1.2.167 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R6 Register

14.7.1.1.2.167.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R6 Register (Offset = 34h) [reset = 0h]

This is where the input samples are written for stream6 right channel

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Table 14-10042. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0034h
AASRC1	02D5 0034h

Figure 14-4966. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R6 Name Register

31	30	29	28	27	26	25	24
IN_DATA13							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA13							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA13							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA13							
R/W							
0h							

Table 14-10043. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA13	R/W	0h	This is where the input samples are written for stream6 right channel

14.7.1.1.2.168 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L7 Register

14.7.1.1.2.168.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L7 Register (Offset = 38h) [reset = 0h]

This is where the input samples are written for stream7 left channel

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Table 14-10044. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0038h
AASRC1	02D5 0038h

Figure 14-4967. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L7 Name Register

31	30	29	28	27	26	25	24
IN_DATA14							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA14							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA14							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA14							
R/W							
0h							

Table 14-10045. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_L7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA14	R/W	0h	This is where the input samples are written for stream7 left channel

14.7.1.1.2.169 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R7 Register

14.7.1.1.2.169.1 AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R7 Register (Offset = 3Ch) [reset = 0h]

This is where the input samples are written for stream7 right channel

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Table 14-10046. Instance Table

Instance Name	Physical Address
AASRC0	02D1 003Ch
AASRC1	02D5 003Ch

Figure 14-4968. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R7 Name Register

31	30	29	28	27	26	25	24
IN_DATA15							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA15							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA15							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA15							
R/W							
0h							

Table 14-10047. AASRC_DATA_R0_GROUP_INPUT_FIFO_DATA_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA15	R/W	0h	This is where the input samples are written for stream7 right channel

14.7.1.1.2.170 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L0 Register

14.7.1.1.2.170.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L0 Register (Offset = 80h) [reset = 0h]

This is where the outpuput samples are written for stream0 left channel

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Table 14-10048. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0080h
AASRC1	02D5 0080h

Figure 14-4969. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L0 Name Register

31	30	29	28	27	26	25	24
OUT_DATA0							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA0							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA0							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA0							
R							
0h							

Table 14-10049. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA0	R	0h	This is from where the output samples are read for stream0 left channel

14.7.1.1.2.171 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R0 Register

14.7.1.1.2.171.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R0 Register (Offset = 84h) [reset = 0h]

This is where the outpuput samples are written for stream0 right channel

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Table 14-10050. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0084h
AASRC1	02D5 0084h

Figure 14-4970. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R0 Name Register

31	30	29	28	27	26	25	24
OUT_DATA1							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA1							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA1							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA1							
R							
0h							

Table 14-10051. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA1	R	0h	This is from where the output samples are read for stream0 right channel

14.7.1.1.2.172 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L1 Register

14.7.1.1.2.172.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L1 Register (Offset = 88h) [reset = 0h]

This is where the outpuput samples are written for stream1 left channel

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Table 14-10052. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0088h
AASRC1	02D5 0088h

Figure 14-4971. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L1 Name Register

31	30	29	28	27	26	25	24
OUT_DATA2							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA2							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA2							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA2							
R							
0h							

Table 14-10053. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA2	R	0h	This is from where the output samples are read for stream1 left channel

14.7.1.1.2.173 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R1 Register

14.7.1.1.2.173.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R1 Register (Offset = 8Ch) [reset = 0h]

This is where the outpuput samples are written for stream1 right channel

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Table 14-10054. Instance Table

Instance Name	Physical Address
AASRC0	02D1 008Ch
AASRC1	02D5 008Ch

Figure 14-4972. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R1 Name Register

31	30	29	28	27	26	25	24
OUT_DATA3							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA3							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA3							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA3							
R							
0h							

Table 14-10055. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA3	R	0h	This is from where the output samples are read for stream1 right channel

14.7.1.1.2.174 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L2 Register

14.7.1.1.2.174.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L2 Register (Offset = 90h) [reset = 0h]

This is where the outpuput samples are written for stream2 left channel

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Table 14-10056. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0090h
AASRC1	02D5 0090h

Figure 14-4973. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L2 Name Register

31	30	29	28	27	26	25	24
OUT_DATA4							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA4							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA4							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA4							
R							
0h							

Table 14-10057. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA4	R	0h	This is from where the output samples are read for stream2 left channel

14.7.1.1.2.175 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R2 Register

14.7.1.1.2.175.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R2 Register (Offset = 94h) [reset = 0h]

This is where the outpuput samples are written for stream2 right channel

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Table 14-10058. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0094h
AASRC1	02D5 0094h

Figure 14-4974. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R2 Name Register

31	30	29	28	27	26	25	24
OUT_DATA5							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUT_DATA5							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUT_DATA5							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUT_DATA5							
R							
0h							

Table 14-10059. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA5	R	0h	This is from where the output samples are read for stream2 right channel

14.7.1.1.2.176 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L3 Register

14.7.1.1.2.176.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L3 Register (Offset = 98h) [reset = 0h]

This is where the outpuput samples are written for stream3 left channel

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Table 14-10060. Instance Table

Instance Name	Physical Address
AASRC0	02D1 0098h
AASRC1	02D5 0098h

Figure 14-4975. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L3 Name Register

31	30	29	28	27	26	25	24
OUT_DATA6							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA6							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA6							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA6							
R							
0h							

Table 14-10061. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA6	R	0h	This is from where the output samples are read for stream3 left channel

14.7.1.1.2.177 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R3 Register

14.7.1.1.2.177.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R3 Register (Offset = 9Ch) [reset = 0h]

This is where the outpuput samples are written for stream3 right channel

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Table 14-10062. Instance Table

Instance Name	Physical Address
AASRC0	02D1 009Ch
AASRC1	02D5 009Ch

Figure 14-4976. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R3 Name Register

31	30	29	28	27	26	25	24
OUT_DATA7							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA7							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA7							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA7							
R							
0h							

Table 14-10063. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA7	R	0h	This is from where the output samples are read for stream3 right channel

14.7.1.1.2.178 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L4 Register

14.7.1.1.2.178.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L4 Register (Offset = A0h) [reset = 0h]

This is where the outpuput samples are written for stream4 left channel

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Table 14-10064. Instance Table

Instance Name	Physical Address
AASRC0	02D1 00A0h
AASRC1	02D5 00A0h

Figure 14-4977. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L4 Name Register

31	30	29	28	27	26	25	24
OUT_DATA8							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA8							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA8							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA8							
R							
0h							

Table 14-10065. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA8	R	0h	This is from where the output samples are read for stream4 left channel

14.7.1.1.2.179 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R4 Register

14.7.1.1.2.179.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R4 Register (Offset = A4h) [reset = 0h]

This is where the outpuput samples are written for stream4 right channel

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Table 14-10066. Instance Table

Instance Name	Physical Address
AASRC0	02D1 00A4h
AASRC1	02D5 00A4h

Figure 14-4978. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R4 Name Register

31	30	29	28	27	26	25	24
OUT_DATA9							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA9							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA9							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA9							
R							
0h							

Table 14-10067. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA9	R	0h	This is from where the output samples are read for stream4 right channel

14.7.1.1.2.180 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L5 Register

14.7.1.1.2.180.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L5 Register (Offset = A8h) [reset = 0h]

This is where the outpuput samples are written for stream5 left channel

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Table 14-10068. Instance Table

Instance Name	Physical Address
AASRC0	02D1 00A8h
AASRC1	02D5 00A8h

Figure 14-4979. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L5 Name Register

31	30	29	28	27	26	25	24
OUT_DATA10							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA10							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA10							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA10							
R							
0h							

Table 14-10069. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA10	R	0h	This is from where the output samples are read for stream5 left channel

14.7.1.1.2.181 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R5 Register

14.7.1.1.2.181.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R5 Register (Offset = ACh) [reset = 0h]

This is where the outpuput samples are written for stream5 right channel

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Table 14-10070. Instance Table

Instance Name	Physical Address
AASRC0	02D1 00ACh
AASRC1	02D5 00ACh

Figure 14-4980. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R5 Name Register

31	30	29	28	27	26	25	24
OUT_DATA11							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA11							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA11							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA11							
R							
0h							

Table 14-10071. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA11	R	0h	This is from where the output samples are read for stream5 right channel

14.7.1.1.2.182 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L6 Register

14.7.1.1.2.182.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L6 Register (Offset = B0h) [reset = 0h]

This is where the outpuput samples are written for stream6 left channel

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Table 14-10072. Instance Table

Instance Name	Physical Address
AASRC0	02D1 00B0h
AASRC1	02D5 00B0h

Figure 14-4981. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L6 Name Register

31	30	29	28	27	26	25	24
OUT_DATA12							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA12							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA12							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA12							
R							
0h							

Table 14-10073. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA12	R	0h	This is from where the output samples are read for stream6 left channel

14.7.1.1.2.183 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R6 Register

14.7.1.1.2.183.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R6 Register (Offset = B4h) [reset = 0h]

This is where the outpuput samples are written for stream6 right channel

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Table 14-10074. Instance Table

Instance Name	Physical Address
AASRC0	02D1 00B4h
AASRC1	02D5 00B4h

Figure 14-4982. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R6 Name Register

31	30	29	28	27	26	25	24
OUT_DATA13							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA13							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA13							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA13							
R							
0h							

Table 14-10075. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA13	R	0h	This is from where the output samples are read for stream6 right channel

14.7.1.1.2.184 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L7 Register

14.7.1.1.2.184.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L7 Register (Offset = B8h) [reset = 0h]

This is where the outpuput samples are written for stream7 left channel

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Table 14-10076. Instance Table

Instance Name	Physical Address
AASRC0	02D1 00B8h
AASRC1	02D5 00B8h

Figure 14-4983. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">OUT_DATA14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OUT_DATA14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUT_DATA14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUT_DATA14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10077. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_L7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA14	R	0h	This is from where the output samples are read for stream7 left channel

14.7.1.1.2.185 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R7 Register

14.7.1.1.2.185.1 AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R7 Register (Offset = BCh) [reset = 0h]

This is where the outpuput samples are written for stream7 right channel

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Table 14-10078. Instance Table

Instance Name	Physical Address
AASRC0	02D1 00BCh
AASRC1	02D5 00BCh

Figure 14-4984. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">OUT_DATA15</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OUT_DATA15</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUT_DATA15</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUT_DATA15</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10079. AASRC_DATA_R0_GROUP_OUTPUT_FIFO_DATA_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA15	R	0h	This is from where the output samples are read for stream7 right channel

14.7.1.1.2.186 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L0 Register

14.7.1.1.2.186.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L0 Register (Offset = 0h) [reset = 0h]

This is where the input samples are written for stream0 left channel

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Table 14-10080. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0000h
AASRC1	02D6 0000h

Figure 14-4985. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L0 Name Register

31	30	29	28	27	26	25	24
IN_DATA0							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA0							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA0							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA0							
R/W							
0h							

Table 14-10081. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA0	R/W	0h	This is where the input samples are written for stream0 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.187 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R0 Register

14.7.1.1.2.187.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R0 Register (Offset = 100h) [reset = 0h]

This is where the input samples are written for stream0 right channel

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Table 14-10082. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0100h
AASRC1	02D6 0100h

Figure 14-4986. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R0 Name Register

31	30	29	28	27	26	25	24
IN_DATA1							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA1							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA1							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA1							
R/W							
0h							

Table 14-10083. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA1	R/W	0h	This is where the input samples are written for stream0 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.188 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L1 Register

14.7.1.1.2.188.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L1 Register (Offset = 200h) [reset = 0h]

This is where the input samples are written for stream1 left channel

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Table 14-10084. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0200h
AASRC1	02D6 0200h

Figure 14-4987. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L1 Name Register

31	30	29	28	27	26	25	24
IN_DATA2							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA2							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA2							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA2							
R/W							
0h							

Table 14-10085. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA2	R/W	0h	This is where the input samples are written for stream1 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.189 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R1 Register

14.7.1.1.2.189.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R1 Register (Offset = 300h) [reset = 0h]

This is where the input samples are written for stream1 right channel

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Table 14-10086. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0300h
AASRC1	02D6 0300h

Figure 14-4988. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R1 Name Register

31	30	29	28	27	26	25	24
IN_DATA3							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA3							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA3							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA3							
R/W							
0h							

Table 14-10087. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA3	R/W	0h	This is where the input samples are written for stream1 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.190 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L2 Register

14.7.1.1.2.190.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L2 Register (Offset = 400h) [reset = 0h]

This is where the input samples are written for stream2 left channel

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Table 14-10088. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0400h
AASRC1	02D6 0400h

Figure 14-4989. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L2 Name Register

31	30	29	28	27	26	25	24
IN_DATA4							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA4							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA4							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA4							
R/W							
0h							

Table 14-10089. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA4	R/W	0h	This is where the input samples are written for stream2 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.191 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R2 Register

14.7.1.1.2.191.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R2 Register (Offset = 500h) [reset = 0h]

This is where the input samples are written for stream2 right channel

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Table 14-10090. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0500h
AASRC1	02D6 0500h

Figure 14-4990. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R2 Name Register

31	30	29	28	27	26	25	24
IN_DATA5							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA5							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA5							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA5							
R/W							
0h							

Table 14-10091. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA5	R/W	0h	This is where the input samples are written for stream2 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.192 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L3 Register

14.7.1.1.2.192.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L3 Register (Offset = 600h) [reset = 0h]

This is where the input samples are written for stream3 left channel

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Table 14-10092. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0600h
AASRC1	02D6 0600h

Figure 14-4991. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L3 Name Register

31	30	29	28	27	26	25	24
IN_DATA6							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA6							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA6							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA6							
R/W							
0h							

Table 14-10093. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA6	R/W	0h	This is where the input samples are written for stream3 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.193 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R3 Register

14.7.1.1.2.193.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R3 Register (Offset = 700h) [reset = 0h]

This is where the input samples are written for stream3 right channel

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Table 14-10094. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0700h
AASRC1	02D6 0700h

Figure 14-4992. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R3 Name Register

31	30	29	28	27	26	25	24
IN_DATA7							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA7							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA7							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA7							
R/W							
0h							

Table 14-10095. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA7	R/W	0h	This is where the input samples are written for stream3 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.194 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L4 Register

14.7.1.1.2.194.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L4 Register (Offset = 800h) [reset = 0h]

This is where the input samples are written for stream4 left channel

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Table 14-10096. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0800h
AASRC1	02D6 0800h

Figure 14-4993. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L4 Name Register

31	30	29	28	27	26	25	24
IN_DATA8							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA8							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA8							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA8							
R/W							
0h							

Table 14-10097. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA8	R/W	0h	This is where the input samples are written for stream4 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.195 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R4 Register

14.7.1.1.2.195.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R4 Register (Offset = 900h) [reset = 0h]

This is where the input samples are written for stream4 right channel

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Table 14-10098. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0900h
AASRC1	02D6 0900h

Figure 14-4994. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R4 Name Register

31	30	29	28	27	26	25	24
IN_DATA9							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA9							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA9							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA9							
R/W							
0h							

Table 14-10099. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA9	R/W	0h	This is where the input samples are written for stream4 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.196 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L5 Register

14.7.1.1.2.196.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L5 Register (Offset = A00h) [reset = 0h]

This is where the input samples are written for stream5 left channel

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Table 14-10100. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0A00h
AASRC1	02D6 0A00h

Figure 14-4995. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IN_DATA10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IN_DATA10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IN_DATA10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IN_DATA10</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10101. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA10	R/W	0h	This is where the input samples are written for stream5 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.197 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R5 Register

14.7.1.1.2.197.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R5 Register (Offset = B00h) [reset = 0h]

This is where the input samples are written for stream5 right channel

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Table 14-10102. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0B00h
AASRC1	02D6 0B00h

Figure 14-4996. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R5 Name Register

31	30	29	28	27	26	25	24
IN_DATA11							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA11							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA11							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA11							
R/W							
0h							

Table 14-10103. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA11	R/W	0h	This is where the input samples are written for stream5 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.198 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L6 Register

14.7.1.1.2.198.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L6 Register (Offset = C00h) [reset = 0h]

This is where the input samples are written for stream6 left channel

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Table 14-10104. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0C00h
AASRC1	02D6 0C00h

Figure 14-4997. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IN_DATA12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IN_DATA12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IN_DATA12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IN_DATA12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10105. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA12	R/W	0h	This is where the input samples are written for stream6 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.199 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R6 Register

14.7.1.1.2.199.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R6 Register (Offset = D00h) [reset = 0h]

This is where the input samples are written for stream6 right channel

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Table 14-10106. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0D00h
AASRC1	02D6 0D00h

Figure 14-4998. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R6 Name Register

31	30	29	28	27	26	25	24
IN_DATA13							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA13							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA13							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA13							
R/W							
0h							

Table 14-10107. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA13	R/W	0h	This is where the input samples are written for stream6 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.200 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L7 Register

14.7.1.1.2.200.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L7 Register (Offset = E00h) [reset = 0h]

This is where the input samples are written for stream7 left channel

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Table 14-10108. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0E00h
AASRC1	02D6 0E00h

Figure 14-4999. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L7 Name Register

31	30	29	28	27	26	25	24
IN_DATA14							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA14							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA14							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA14							
R/W							
0h							

Table 14-10109. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_L7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA14	R/W	0h	This is where the input samples are written for stream7 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.201 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R7 Register

14.7.1.1.2.201.1 AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R7 Register (Offset = F00h) [reset = 0h]

This is where the input samples are written for stream7 right channel

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Table 14-10110. Instance Table

Instance Name	Physical Address
AASRC0	02D2 0F00h
AASRC1	02D6 0F00h

Figure 14-5000. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R7 Name Register

31	30	29	28	27	26	25	24
IN_DATA15							
R/W							
0h							
23	22	21	20	19	18	17	16
IN_DATA15							
R/W							
0h							
15	14	13	12	11	10	9	8
IN_DATA15							
R/W							
0h							
7	6	5	4	3	2	1	0
IN_DATA15							
R/W							
0h							

Table 14-10111. AASRC_DATA_R1_STREAM_INPUT_FIFO_DATA_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IN_DATA15	R/W	0h	This is where the input samples are written for stream7 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.202 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L0 Register

14.7.1.1.2.202.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L0 Register (Offset = 1000h) [reset = 0h]

This is from where the output samples are read for stream0 left channel

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Table 14-10112. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1000h
AASRC1	02D6 1000h

Figure 14-5001. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L0 Name Register

31	30	29	28	27	26	25	24
OUT_DATA0							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA0							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA0							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA0							
R							
0h							

Table 14-10113. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA0	R	0h	This is from where the output samples are read for stream0 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.203 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R0 Register

14.7.1.1.2.203.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R0 Register (Offset = 1100h) [reset = 0h]

This is from where the output samples are read for stream0 right channel

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Table 14-10114. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1100h
AASRC1	02D6 1100h

Figure 14-5002. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R0 Name Register

31	30	29	28	27	26	25	24
OUT_DATA1							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA1							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA1							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA1							
R							
0h							

Table 14-10115. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA1	R	0h	This is from where the output samples are read for stream0 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.204 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L1 Register

14.7.1.1.2.204.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L1 Register (Offset = 1200h) [reset = 0h]

This is from where the output samples are read for stream1 left channel

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Table 14-10116. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1200h
AASRC1	02D6 1200h

Figure 14-5003. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-10117. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.1.1.2.205 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R1 Register

14.7.1.1.2.205.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R1 Register (Offset = 1300h) [reset = 0h]

This is from where the output samples are read for stream1 right channel

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Table 14-10118. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1300h
AASRC1	02D6 1300h

Figure 14-5004. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R1 Name Register

31	30	29	28	27	26	25	24
OUT_DATA3							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA3							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA3							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA3							
R							
0h							

Table 14-10119. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA3	R	0h	This is from where the output samples are read for stream1 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.206 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L2 Register

14.7.1.1.2.206.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L2 Register (Offset = 1400h) [reset = 0h]

This is from where the output samples are read for stream2 left channel

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Table 14-10120. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1400h
AASRC1	02D6 1400h

Figure 14-5005. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L2 Name Register

31	30	29	28	27	26	25	24
OUT_DATA4							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA4							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA4							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA4							
R							
0h							

Table 14-10121. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA4	R	0h	This is from where the output samples are read for stream2 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.207 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R2 Register

14.7.1.1.2.207.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R2 Register (Offset = 1500h) [reset = 0h]

This is from where the output samples are read for stream2 right channel

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Table 14-10122. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1500h
AASRC1	02D6 1500h

Figure 14-5006. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R2 Name Register

31	30	29	28	27	26	25	24
OUT_DATA5							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA5							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA5							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA5							
R							
0h							

Table 14-10123. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA5	R	0h	This is from where the output samples are read for stream2 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.208 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L3 Register

14.7.1.1.2.208.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L3 Register (Offset = 1600h) [reset = 0h]

This is from where the output samples are read for stream3 left channel

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Table 14-10124. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1600h
AASRC1	02D6 1600h

Figure 14-5007. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L3 Name Register

31	30	29	28	27	26	25	24
OUT_DATA6							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA6							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA6							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA6							
R							
0h							

Table 14-10125. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA6	R	0h	This is from where the output samples are read for stream3 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.209 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R3 Register

14.7.1.1.2.209.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R3 Register (Offset = 1700h) [reset = 0h]

This is from where the output samples are read for stream3 right channel

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Table 14-10126. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1700h
AASRC1	02D6 1700h

Figure 14-5008. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R3 Name Register

31	30	29	28	27	26	25	24
OUT_DATA7							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA7							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA7							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA7							
R							
0h							

Table 14-10127. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA7	R	0h	This is from where the output samples are read for stream3 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.210 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L4 Register

14.7.1.1.2.210.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L4 Register (Offset = 1800h) [reset = 0h]

This is from where the output samples are read for stream4 left channel

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Table 14-10128. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1800h
AASRC1	02D6 1800h

Figure 14-5009. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L4 Name Register

31	30	29	28	27	26	25	24
OUT_DATA8							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA8							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA8							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA8							
R							
0h							

Table 14-10129. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA8	R	0h	This is from where the output samples are read for stream4 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.211 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R4 Register

14.7.1.1.2.211.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R4 Register (Offset = 1900h) [reset = 0h]

This is from where the output samples are read for stream4 right channel

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Table 14-10130. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1900h
AASRC1	02D6 1900h

Figure 14-5010. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R4 Name Register

31	30	29	28	27	26	25	24
OUT_DATA9							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA9							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA9							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA9							
R							
0h							

Table 14-10131. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA9	R	0h	This is from where the output samples are read for stream4 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.212 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L5 Register

14.7.1.1.2.212.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L5 Register (Offset = 1A00h) [reset = 0h]

This is from where the output samples are read for stream5 left channel

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Table 14-10132. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1A00h
AASRC1	02D6 1A00h

Figure 14-5011. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L5 Name Register

31	30	29	28	27	26	25	24
OUT_DATA10							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA10							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA10							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA10							
R							
0h							

Table 14-10133. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA10	R	0h	This is from where the output samples are read for stream5 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.213 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R5 Register

14.7.1.1.2.213.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R5 Register (Offset = 1B00h) [reset = 0h]

This is from where the output samples are read for stream5 right channel

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Table 14-10134. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1B00h
AASRC1	02D6 1B00h

Figure 14-5012. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R5 Name Register

31	30	29	28	27	26	25	24
OUT_DATA11							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA11							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA11							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA11							
R							
0h							

Table 14-10135. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA11	R	0h	This is from where the output samples are read for stream5 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.214 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L6 Register

14.7.1.1.2.214.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L6 Register (Offset = 1C00h) [reset = 0h]

This is from where the output samples are read for stream6 left channel

Return to Summary Table

Table 14-10136. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1C00h
AASRC1	02D6 1C00h

Figure 14-5013. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L6 Name Register

31	30	29	28	27	26	25	24
OUT_DATA12							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA12							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA12							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA12							
R							
0h							

Table 14-10137. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA12	R	0h	This is from where the output samples are read for stream6 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.215 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R6 Register

14.7.1.1.2.215.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R6 Register (Offset = 1D00h) [reset = 0h]

This is from where the output samples are read for stream6 right channel

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Table 14-10138. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1D00h
AASRC1	02D6 1D00h

Figure 14-5014. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R6 Name Register

31	30	29	28	27	26	25	24
OUT_DATA13							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA13							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA13							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA13							
R							
0h							

Table 14-10139. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA13	R	0h	This is from where the output samples are read for stream6 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.216 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L7 Register

14.7.1.1.2.216.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L7 Register (Offset = 1E00h) [reset = 0h]

This is from where the output samples are read for stream7 left channel

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Table 14-10140. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1E00h
AASRC1	02D6 1E00h

Figure 14-5015. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L7 Name Register

31	30	29	28	27	26	25	24
OUT_DATA14							
R							
0h							
23	22	21	20	19	18	17	16
OUT_DATA14							
R							
0h							
15	14	13	12	11	10	9	8
OUT_DATA14							
R							
0h							
7	6	5	4	3	2	1	0
OUT_DATA14							
R							
0h							

Table 14-10141. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_L7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA14	R	0h	This is from where the output samples are read for stream7 left channel. Note that reads from any address within this stream region address range reads same value

14.7.1.1.2.217 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R7 Register

14.7.1.1.2.217.1 AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R7 Register (Offset = 1F00h) [reset = 0h]

This is from where the output samples are read for stream7 right channel

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Table 14-10142. Instance Table

Instance Name	Physical Address
AASRC0	02D2 1F00h
AASRC1	02D6 1F00h

Figure 14-5016. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">OUT_DATA15</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OUT_DATA15</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUT_DATA15</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUT_DATA15</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10143. AASRC_DATA_R1_STREAM_OUTPUT_FIFO_DATA_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUT_DATA15	R	0h	This is from where the output samples are read for stream7 right channel. Note that reads from any address within this stream region address range reads same value

14.7.1.2 MCASP

MCASP

14.7.1.2.1 MCASP Summaries

MCASP Summaries

Table 14-10144. MCASP Registers, Base Address=02B0 0000h, Length=8192

Offset	Length	Register Name	MCASP0 Physical Address	MCASP1 Physical Address	MCASP2 Physical Address
0h	32	MCASP_PID	02B0 0000h	02B1 0000h	02B2 0000h
4h	32	MCASP_PWRIDLESYSCONFIG	02B0 0004h	02B1 0004h	02B2 0004h
10h	32	MCASP_PFUNC	02B0 0010h	02B1 0010h	02B2 0010h
14h	32	MCASP_PDIR	02B0 0014h	02B1 0014h	02B2 0014h
18h	32	MCASP_PDOUT	02B0 0018h	02B1 0018h	02B2 0018h
1Ch	32	MCASP_PDIN	02B0 001Ch	02B1 001Ch	02B2 001Ch
20h	32	MCASP_PDCLR	02B0 0020h	02B1 0020h	02B2 0020h
44h	32	MCASP_GBLCTL	02B0 0044h	02B1 0044h	02B2 0044h
48h	32	MCASP_AMUTE	02B0 0048h	02B1 0048h	02B2 0048h
4Ch	32	MCASP_DLBCTL	02B0 004Ch	02B1 004Ch	02B2 004Ch
50h	32	MCASP_DITCTL	02B0 0050h	02B1 0050h	02B2 0050h
60h	32	MCASP_RGBLCTL	02B0 0060h	02B1 0060h	02B2 0060h
64h	32	MCASP_RMASK	02B0 0064h	02B1 0064h	02B2 0064h
68h	32	MCASP_RFMT	02B0 0068h	02B1 0068h	02B2 0068h
6Ch	32	MCASP_AFSRCTL	02B0 006Ch	02B1 006Ch	02B2 006Ch
70h	32	MCASP_ACLKRCTL	02B0 0070h	02B1 0070h	02B2 0070h
74h	32	MCASP_AHCLKRCTL	02B0 0074h	02B1 0074h	02B2 0074h
78h	32	MCASP_RTDM	02B0 0078h	02B1 0078h	02B2 0078h
7Ch	32	MCASP_RINTCTL	02B0 007Ch	02B1 007Ch	02B2 007Ch
80h	32	MCASP_RSTAT	02B0 0080h	02B1 0080h	02B2 0080h
84h	32	MCASP_RSLOT	02B0 0084h	02B1 0084h	02B2 0084h
88h	32	MCASP_RCLKCHK	02B0 0088h	02B1 0088h	02B2 0088h
A0h	32	MCASP_XGBLCTL	02B0 00A0h	02B1 00A0h	02B2 00A0h
A4h	32	MCASP_XMASK	02B0 00A4h	02B1 00A4h	02B2 00A4h
A8h	32	MCASP_XFMT	02B0 00A8h	02B1 00A8h	02B2 00A8h
ACh	32	MCASP_AFSXCTL	02B0 00ACh	02B1 00ACh	02B2 00ACh
B0h	32	MCASP_ACLKXCTL	02B0 00B0h	02B1 00B0h	02B2 00B0h
B4h	32	MCASP_AHCLKXCTL	02B0 00B4h	02B1 00B4h	02B2 00B4h
B8h	32	MCASP_XTDM	02B0 00B8h	02B1 00B8h	02B2 00B8h
BCh	32	MCASP_XINTCTL	02B0 00BCh	02B1 00BCh	02B2 00BCh
C0h	32	MCASP_XSTAT	02B0 00C0h	02B1 00C0h	02B2 00C0h
C4h	32	MCASP_XSLOT	02B0 00C4h	02B1 00C4h	02B2 00C4h
C8h	32	MCASP_XCLKCHK	02B0 00C8h	02B1 00C8h	02B2 00C8h
CCh	32	MCASP_XEVTCTL	02B0 00CCh	02B1 00CCh	02B2 00CCh
100h	32	MCASP_DITCSRA0	02B0 0100h	02B1 0100h	02B2 0100h
104h	32	MCASP_DITCSRA1	02B0 0104h	02B1 0104h	02B2 0104h
108h	32	MCASP_DITCSRA2	02B0 0108h	02B1 0108h	02B2 0108h
10Ch	32	MCASP_DITCSRA3	02B0 010Ch	02B1 010Ch	02B2 010Ch
110h	32	MCASP_DITCSRA4	02B0 0110h	02B1 0110h	02B2 0110h

Table 14-10144. MCASP Registers, Base Address=02B0 0000h, Length=8192 (continued)

Offset	Length	Register Name	MCASP0 Physical Address	MCASP1 Physical Address	MCASP2 Physical Address
114h	32	MCASP_DITCSRA5	02B0 0114h	02B1 0114h	02B2 0114h
118h	32	MCASP_DITCSRB0	02B0 0118h	02B1 0118h	02B2 0118h
11Ch	32	MCASP_DITCSRB1	02B0 011Ch	02B1 011Ch	02B2 011Ch
120h	32	MCASP_DITCSRB2	02B0 0120h	02B1 0120h	02B2 0120h
124h	32	MCASP_DITCSRB3	02B0 0124h	02B1 0124h	02B2 0124h
128h	32	MCASP_DITCSRB4	02B0 0128h	02B1 0128h	02B2 0128h
12Ch	32	MCASP_DITCSRB5	02B0 012Ch	02B1 012Ch	02B2 012Ch
130h	32	MCASP_DITUDRA0	02B0 0130h	02B1 0130h	02B2 0130h
134h	32	MCASP_DITUDRA1	02B0 0134h	02B1 0134h	02B2 0134h
138h	32	MCASP_DITUDRA2	02B0 0138h	02B1 0138h	02B2 0138h
13Ch	32	MCASP_DITUDRA3	02B0 013Ch	02B1 013Ch	02B2 013Ch
140h	32	MCASP_DITUDRA4	02B0 0140h	02B1 0140h	02B2 0140h
144h	32	MCASP_DITUDRA5	02B0 0144h	02B1 0144h	02B2 0144h
148h	32	MCASP_DITUDRB0	02B0 0148h	02B1 0148h	02B2 0148h
14Ch	32	MCASP_DITUDRB1	02B0 014Ch	02B1 014Ch	02B2 014Ch
150h	32	MCASP_DITUDRB2	02B0 0150h	02B1 0150h	02B2 0150h
154h	32	MCASP_DITUDRB3	02B0 0154h	02B1 0154h	02B2 0154h
158h	32	MCASP_DITUDRB4	02B0 0158h	02B1 0158h	02B2 0158h
15Ch	32	MCASP_DITUDRB5	02B0 015Ch	02B1 015Ch	02B2 015Ch
180h	32	MCASP_SRCTL0	02B0 0180h	02B1 0180h	02B2 0180h
184h	32	MCASP_SRCTL1	02B0 0184h	02B1 0184h	02B2 0184h
188h	32	MCASP_SRCTL2	02B0 0188h	02B1 0188h	02B2 0188h
18Ch	32	MCASP_SRCTL3	02B0 018Ch	02B1 018Ch	02B2 018Ch
190h	32	MCASP_SRCTL4	02B0 0190h	02B1 0190h	02B2 0190h
194h	32	MCASP_SRCTL5	02B0 0194h	02B1 0194h	02B2 0194h
198h	32	MCASP_SRCTL6	02B0 0198h	02B1 0198h	02B2 0198h
19Ch	32	MCASP_SRCTL7	02B0 019Ch	02B1 019Ch	02B2 019Ch
1A0h	32	MCASP_SRCTL8	02B0 01A0h	02B1 01A0h	02B2 01A0h
1A4h	32	MCASP_SRCTL9	02B0 01A4h	02B1 01A4h	02B2 01A4h
1A8h	32	MCASP_SRCTL10	02B0 01A8h	02B1 01A8h	02B2 01A8h
1ACh	32	MCASP_SRCTL11	02B0 01ACh	02B1 01ACh	02B2 01ACh
1B0h	32	MCASP_SRCTL12	02B0 01B0h	02B1 01B0h	02B2 01B0h
1B4h	32	MCASP_SRCTL13	02B0 01B4h	02B1 01B4h	02B2 01B4h
1B8h	32	MCASP_SRCTL14	02B0 01B8h	02B1 01B8h	02B2 01B8h
1BCh	32	MCASP_SRCTL15	02B0 01BCh	02B1 01BCh	02B2 01BCh
200h	32	MCASP_XBUF0	02B0 0200h	02B1 0200h	02B2 0200h
204h	32	MCASP_XBUF1	02B0 0204h	02B1 0204h	02B2 0204h
208h	32	MCASP_XBUF2	02B0 0208h	02B1 0208h	02B2 0208h
20Ch	32	MCASP_XBUF3	02B0 020Ch	02B1 020Ch	02B2 020Ch
210h	32	MCASP_XBUF4	02B0 0210h	02B1 0210h	02B2 0210h
214h	32	MCASP_XBUF5	02B0 0214h	02B1 0214h	02B2 0214h
218h	32	MCASP_XBUF6	02B0 0218h	02B1 0218h	02B2 0218h
21Ch	32	MCASP_XBUF7	02B0 021Ch	02B1 021Ch	02B2 021Ch
220h	32	MCASP_XBUF8	02B0 0220h	02B1 0220h	02B2 0220h
224h	32	MCASP_XBUF9	02B0 0224h	02B1 0224h	02B2 0224h
228h	32	MCASP_XBUF10	02B0 0228h	02B1 0228h	02B2 0228h

Table 14-10144. MCASP Registers, Base Address=02B0 0000h, Length=8192 (continued)

Offset	Length	Register Name	MCASP0 Physical Address	MCASP1 Physical Address	MCASP2 Physical Address
22Ch	32	MCASP_XBUF11	02B0 022Ch	02B1 022Ch	02B2 022Ch
230h	32	MCASP_XBUF12	02B0 0230h	02B1 0230h	02B2 0230h
234h	32	MCASP_XBUF13	02B0 0234h	02B1 0234h	02B2 0234h
238h	32	MCASP_XBUF14	02B0 0238h	02B1 0238h	02B2 0238h
23Ch	32	MCASP_XBUF15	02B0 023Ch	02B1 023Ch	02B2 023Ch
280h	32	MCASP_RBUF0	02B0 0280h	02B1 0280h	02B2 0280h
284h	32	MCASP_RBUF1	02B0 0284h	02B1 0284h	02B2 0284h
288h	32	MCASP_RBUF2	02B0 0288h	02B1 0288h	02B2 0288h
28Ch	32	MCASP_RBUF3	02B0 028Ch	02B1 028Ch	02B2 028Ch
290h	32	MCASP_RBUF4	02B0 0290h	02B1 0290h	02B2 0290h
294h	32	MCASP_RBUF5	02B0 0294h	02B1 0294h	02B2 0294h
298h	32	MCASP_RBUF6	02B0 0298h	02B1 0298h	02B2 0298h
29Ch	32	MCASP_RBUF7	02B0 029Ch	02B1 029Ch	02B2 029Ch
2A0h	32	MCASP_RBUF8	02B0 02A0h	02B1 02A0h	02B2 02A0h
2A4h	32	MCASP_RBUF9	02B0 02A4h	02B1 02A4h	02B2 02A4h
2A8h	32	MCASP_RBUF10	02B0 02A8h	02B1 02A8h	02B2 02A8h
2ACh	32	MCASP_RBUF11	02B0 02ACh	02B1 02ACh	02B2 02ACh
2B0h	32	MCASP_RBUF12	02B0 02B0h	02B1 02B0h	02B2 02B0h
2B4h	32	MCASP_RBUF13	02B0 02B4h	02B1 02B4h	02B2 02B4h
2B8h	32	MCASP_RBUF14	02B0 02B8h	02B1 02B8h	02B2 02B8h
2BCh	32	MCASP_RBUF15	02B0 02BCh	02B1 02BCh	02B2 02BCh
1000h	32	MCASP_WFIFOCTL	02B0 1000h	02B1 1000h	02B2 1000h
1004h	32	MCASP_WFIFOSTS	02B0 1004h	02B1 1004h	02B2 1004h
1008h	32	MCASP_RFIFOCTL	02B0 1008h	02B1 1008h	02B2 1008h
100Ch	32	MCASP_RFIFOSTS	02B0 100Ch	02B1 100Ch	02B2 100Ch

Table 14-10145. MCASP Registers, Base Address=02B0 0000h, Length=8192

Offset	Length	Register Name	MCASP3 Physical Address	MCASP4 Physical Address
0h	32	MCASP_PID	02B3 0000h	02B4 0000h
4h	32	MCASP_PWRIDLESYSCONFIG	02B3 0004h	02B4 0004h
10h	32	MCASP_PFUNC	02B3 0010h	02B4 0010h
14h	32	MCASP_PDIR	02B3 0014h	02B4 0014h
18h	32	MCASP_PDOUT	02B3 0018h	02B4 0018h
1Ch	32	MCASP_PDIN	02B3 001Ch	02B4 001Ch
20h	32	MCASP_PDCLR	02B3 0020h	02B4 0020h
44h	32	MCASP_GBLCTL	02B3 0044h	02B4 0044h
48h	32	MCASP_AMUTE	02B3 0048h	02B4 0048h
4Ch	32	MCASP_DLBCTL	02B3 004Ch	02B4 004Ch
50h	32	MCASP_DITCTL	02B3 0050h	02B4 0050h
60h	32	MCASP_RGBLCTL	02B3 0060h	02B4 0060h
64h	32	MCASP_RMASK	02B3 0064h	02B4 0064h
68h	32	MCASP_RFMT	02B3 0068h	02B4 0068h
6Ch	32	MCASP_AFSRCTL	02B3 006Ch	02B4 006Ch
70h	32	MCASP_ACLKRCTL	02B3 0070h	02B4 0070h
74h	32	MCASP_AHCLKRCTL	02B3 0074h	02B4 0074h
78h	32	MCASP_RTDM	02B3 0078h	02B4 0078h

Table 14-10145. MCASP Registers, Base Address=02B0 0000h, Length=8192 (continued)

Offset	Length	Register Name	MCASP3 Physical Address	MCASP4 Physical Address
7Ch	32	MCASP_RINTCTL	02B3 007Ch	02B4 007Ch
80h	32	MCASP_RSTAT	02B3 0080h	02B4 0080h
84h	32	MCASP_RSLOT	02B3 0084h	02B4 0084h
88h	32	MCASP_RCLKCHK	02B3 0088h	02B4 0088h
A0h	32	MCASP_XGBLCTL	02B3 00A0h	02B4 00A0h
A4h	32	MCASP_XMASK	02B3 00A4h	02B4 00A4h
A8h	32	MCASP_XFMT	02B3 00A8h	02B4 00A8h
ACh	32	MCASP_AFSXCTL	02B3 00ACh	02B4 00ACh
B0h	32	MCASP_ACLKXCTL	02B3 00B0h	02B4 00B0h
B4h	32	MCASP_AHCLKXCTL	02B3 00B4h	02B4 00B4h
B8h	32	MCASP_XTDM	02B3 00B8h	02B4 00B8h
BCh	32	MCASP_XINTCTL	02B3 00BCh	02B4 00BCh
C0h	32	MCASP_XSTAT	02B3 00C0h	02B4 00C0h
C4h	32	MCASP_XSLOT	02B3 00C4h	02B4 00C4h
C8h	32	MCASP_XCLKCHK	02B3 00C8h	02B4 00C8h
CCh	32	MCASP_XEVTCTL	02B3 00CCh	02B4 00CCh
100h	32	MCASP_DITCSRA0	02B3 0100h	02B4 0100h
104h	32	MCASP_DITCSRA1	02B3 0104h	02B4 0104h
108h	32	MCASP_DITCSRA2	02B3 0108h	02B4 0108h
10Ch	32	MCASP_DITCSRA3	02B3 010Ch	02B4 010Ch
110h	32	MCASP_DITCSRA4	02B3 0110h	02B4 0110h
114h	32	MCASP_DITCSRA5	02B3 0114h	02B4 0114h
118h	32	MCASP_DITCSRB0	02B3 0118h	02B4 0118h
11Ch	32	MCASP_DITCSRB1	02B3 011Ch	02B4 011Ch
120h	32	MCASP_DITCSRB2	02B3 0120h	02B4 0120h
124h	32	MCASP_DITCSRB3	02B3 0124h	02B4 0124h
128h	32	MCASP_DITCSRB4	02B3 0128h	02B4 0128h
12Ch	32	MCASP_DITCSRB5	02B3 012Ch	02B4 012Ch
130h	32	MCASP_DITUDRA0	02B3 0130h	02B4 0130h
134h	32	MCASP_DITUDRA1	02B3 0134h	02B4 0134h
138h	32	MCASP_DITUDRA2	02B3 0138h	02B4 0138h
13Ch	32	MCASP_DITUDRA3	02B3 013Ch	02B4 013Ch
140h	32	MCASP_DITUDRA4	02B3 0140h	02B4 0140h
144h	32	MCASP_DITUDRA5	02B3 0144h	02B4 0144h
148h	32	MCASP_DITUDRB0	02B3 0148h	02B4 0148h
14Ch	32	MCASP_DITUDRB1	02B3 014Ch	02B4 014Ch
150h	32	MCASP_DITUDRB2	02B3 0150h	02B4 0150h
154h	32	MCASP_DITUDRB3	02B3 0154h	02B4 0154h
158h	32	MCASP_DITUDRB4	02B3 0158h	02B4 0158h
15Ch	32	MCASP_DITUDRB5	02B3 015Ch	02B4 015Ch
180h	32	MCASP_SRCTL0	02B3 0180h	02B4 0180h
184h	32	MCASP_SRCTL1	02B3 0184h	02B4 0184h
188h	32	MCASP_SRCTL2	02B3 0188h	02B4 0188h
18Ch	32	MCASP_SRCTL3	02B3 018Ch	02B4 018Ch
190h	32	MCASP_SRCTL4	02B3 0190h	02B4 0190h
194h	32	MCASP_SRCTL5	02B3 0194h	02B4 0194h
198h	32	MCASP_SRCTL6	02B3 0198h	02B4 0198h

Table 14-10145. MCASP Registers, Base Address=02B0 0000h, Length=8192 (continued)

Offset	Length	Register Name	MCASP3 Physical Address	MCASP4 Physical Address
19Ch	32	MCASP_SRCTL7	02B3 019Ch	02B4 019Ch
1A0h	32	MCASP_SRCTL8	02B3 01A0h	02B4 01A0h
1A4h	32	MCASP_SRCTL9	02B3 01A4h	02B4 01A4h
1A8h	32	MCASP_SRCTL10	02B3 01A8h	02B4 01A8h
1ACh	32	MCASP_SRCTL11	02B3 01ACh	02B4 01ACh
1B0h	32	MCASP_SRCTL12	02B3 01B0h	02B4 01B0h
1B4h	32	MCASP_SRCTL13	02B3 01B4h	02B4 01B4h
1B8h	32	MCASP_SRCTL14	02B3 01B8h	02B4 01B8h
1BCh	32	MCASP_SRCTL15	02B3 01BCh	02B4 01BCh
200h	32	MCASP_XBUF0	02B3 0200h	02B4 0200h
204h	32	MCASP_XBUF1	02B3 0204h	02B4 0204h
208h	32	MCASP_XBUF2	02B3 0208h	02B4 0208h
20Ch	32	MCASP_XBUF3	02B3 020Ch	02B4 020Ch
210h	32	MCASP_XBUF4	02B3 0210h	02B4 0210h
214h	32	MCASP_XBUF5	02B3 0214h	02B4 0214h
218h	32	MCASP_XBUF6	02B3 0218h	02B4 0218h
21Ch	32	MCASP_XBUF7	02B3 021Ch	02B4 021Ch
220h	32	MCASP_XBUF8	02B3 0220h	02B4 0220h
224h	32	MCASP_XBUF9	02B3 0224h	02B4 0224h
228h	32	MCASP_XBUF10	02B3 0228h	02B4 0228h
22Ch	32	MCASP_XBUF11	02B3 022Ch	02B4 022Ch
230h	32	MCASP_XBUF12	02B3 0230h	02B4 0230h
234h	32	MCASP_XBUF13	02B3 0234h	02B4 0234h
238h	32	MCASP_XBUF14	02B3 0238h	02B4 0238h
23Ch	32	MCASP_XBUF15	02B3 023Ch	02B4 023Ch
280h	32	MCASP_RBUF0	02B3 0280h	02B4 0280h
284h	32	MCASP_RBUF1	02B3 0284h	02B4 0284h
288h	32	MCASP_RBUF2	02B3 0288h	02B4 0288h
28Ch	32	MCASP_RBUF3	02B3 028Ch	02B4 028Ch
290h	32	MCASP_RBUF4	02B3 0290h	02B4 0290h
294h	32	MCASP_RBUF5	02B3 0294h	02B4 0294h
298h	32	MCASP_RBUF6	02B3 0298h	02B4 0298h
29Ch	32	MCASP_RBUF7	02B3 029Ch	02B4 029Ch
2A0h	32	MCASP_RBUF8	02B3 02A0h	02B4 02A0h
2A4h	32	MCASP_RBUF9	02B3 02A4h	02B4 02A4h
2A8h	32	MCASP_RBUF10	02B3 02A8h	02B4 02A8h
2ACh	32	MCASP_RBUF11	02B3 02ACh	02B4 02ACh
2B0h	32	MCASP_RBUF12	02B3 02B0h	02B4 02B0h
2B4h	32	MCASP_RBUF13	02B3 02B4h	02B4 02B4h
2B8h	32	MCASP_RBUF14	02B3 02B8h	02B4 02B8h
2BCh	32	MCASP_RBUF15	02B3 02BCh	02B4 02BCh
1000h	32	MCASP_WFIFOCTL	02B3 1000h	02B4 1000h
1004h	32	MCASP_WFIFOSTS	02B3 1004h	02B4 1004h
1008h	32	MCASP_RFIFOCTL	02B3 1008h	02B4 1008h
100Ch	32	MCASP_RFIFOSTS	02B3 100Ch	02B4 100Ch

14.7.1.2.2 MCASP Registers

MCASP Registers

14.7.1.2.2.1 MCASP_PID Register

14.7.1.2.2.1.1 MCASP_PID Register (Offset = 0h) [reset = 44307B02h]

The revision identification register (PID) contains identification data for the peripheral.

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Table 14-10146. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0000h
MCASP1	02B1 0000h
MCASP2	02B2 0000h
MCASP3	02B3 0000h
MCASP4	02B4 0000h

Figure 14-5017. MCASP_PID Name Register

31	30	29	28	27	26	25	24
REV							
R							
44307B02h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REV							
R							
44307B02h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REV							
R							
44307B02h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REV							
R							
44307B02h							

Table 14-10147. MCASP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REV	R	44307B02h	Identifies revision of peripheral.

14.7.1.2.2.2 MCASP_PWRIDLESYSCONFIG Register

14.7.1.2.2.2.1 MCASP_PWRIDLESYSCONFIG Register (Offset = 4h) [reset = 2h]

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Table 14-10148. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0004h
MCASP1	02B1 0004h
MCASP2	02B2 0004h
MCASP3	02B3 0004h
MCASP4	02B4 0004h

Figure 14-5018. MCASP_PWRIDLESYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED66							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED66							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED66							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED66		OTHER				IDLEMODE	
R		R/W				R/W	
0h		0h				2h	

Table 14-10149. MCASP_PWRIDLESYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED66	R	0h	
5:2	OTHER	R/W	0h	Reserved for future programming.
1:0	IDLEMODE	R/W	2h	Power management Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0 `Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements. Backup mode, for debug only.` 1 `No-idle mode: local target never enters idle state. Backup mode, for debug only.` 2 `Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events.` 3 `Reserved.`

14.7.1.2.2.3 MCASP_PFUNC Register

14.7.1.2.2.3.1 MCASP_PFUNC Register (Offset = 10h) [reset = 0h]

The pin function register (PFUNC) specifies the function of AXRn, ACLKX, AHCLKX, AFSX, ACLKR, AHCLKR, and AFSR pins as either a McASP pin or a general-purpose input/output (GPIO) pin. CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation.

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Table 14-10150. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0010h
MCASP1	02B1 0010h
MCASP2	02B2 0010h
MCASP3	02B3 0010h
MCASP4	02B4 0010h

Figure 14-5019. MCASP_PFUNC Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED67
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED67							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED67							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED67				AXR			
R				R/W			
0h				0h			

Table 14-10151. MCASP_PFUNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Determines if AFSR pin functions as McASP or GPIO. 0 `Pin functions as MCASP pin.` 1 `Pin functions as GPIO pin.`
30	AHCLKR	R/W	0h	Determines if AHCLKR pin functions as McASP or GPIO. 0 `Pin functions as MCASP pin.` 1 `Pin functions as GPIO pin.`
29	ACLKR	R/W	0h	Determines if ACLKR pin functions as McASP or GPIO. 0 `Pin functions as MCASP pin.` 1 `Pin functions as GPIO pin.`
28	AFSX	R/W	0h	Determines if AFSX pin functions as McASP or GPIO. 0 `Pin functions as MCASP pin.` 1 `Pin functions as GPIO pin.`
27	AHCLKX	R/W	0h	Determines if AHCLKX pin functions as McASP or GPIO. 0 `Pin functions as MCASP pin.` 1 `Pin functions as GPIO pin.`

Table 14-10151. MCASP_PFUNC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	ACLKX	R/W	0h	Determines if ACLKX pin functions as McASP or GPIO. 0 `Pin functions as McASP pin.` 1 `Pin functions as GPIO pin.`
25	AMUTE	R/W	0h	Determines if AMUTE pin functions as McASP or GPIO. 0 `Pin functions as McASP pin.` 1 `Pin functions as GPIO pin.`
24:4	RESERVED67	R	0h	
3:0	AXR	R/W	0h	Determines if AXRn pin functions as McASP or GPIO. 0 `Pin functions as McASP pin.` 1 `Pin functions as GPIO pin.`

14.7.1.2.2.4 MCASP_PDIR Register

14.7.1.2.2.4.1 MCASP_PDIR Register (Offset = 14h) [reset = 0h]

The pin direction register (PDIR) specifies the direction of AXRn, ACLKX, AHCLKX, AFSX, ACLKR, AHCLKR, and AFSR pins as either an input or an output pin. Regardless of the pin function register (PFUNC) setting, each PDIR bit must be set to 1 for the specified pin to be enabled as an output and each PDIR bit must be cleared to 0 for the specified pin to be an input. For example, if the McASP is configured to use an internally-generated bit clock and the clock is to be driven out to the system, the PFUNC bit must be cleared to 0 (McASP function) and the PDIR bit must be set to 1 (an output). When AXRn is configured to transmit, the PFUNC bit must be cleared to 0 (McASP function) and the PDIR bit must be set to 1 (an output). Similarly, when AXRn is configured to receive, the PFUNC bit must be cleared to 0 (McASP function) and the PDIR bit must be cleared to 0 (an input). CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation. The number of serializers is device/instance specific. See device datasheet for the number of serializers supported by each instance. Invalid bit settings are reserved.

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Table 14-10152. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0014h
MCASP1	02B1 0014h
MCASP2	02B2 0014h
MCASP3	02B3 0014h
MCASP4	02B4 0014h

Figure 14-5020. MCASP_PDIR Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED68
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED68							
R							
0h							
15	14	13	12	11	10	9	8
AXR							
R/W							
0h							
7	6	5	4	3	2	1	0
AXR							
R/W							
0h							

Table 14-10153. MCASP_PDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Determines if AFSR pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`

Table 14-10153. MCASP_PDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	AHCLKR	R/W	0h	NOTE: AHCLKR, AHCLKX pins are not available on the SOC pinmux directly, but through a clock routing logic that maps the SOC pins (AUDIO_EXT_REFCLK[1:0]) to the McASP clocks. Therefore, GPIO mode control is not functional for these specific pins. 0 `Pin functions as input.` 1 `Pin functions as output.`
29	ACLKR	R/W	0h	Determines if ACLKR pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`
28	AFSX	R/W	0h	Determines if AFSX pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`
27	AHCLKX	R/W	0h	NOTE: AHCLKR, AHCLKX pins are not available on the SOC pinmux directly, but through a clock routing logic that maps the SOC pins (AUDIO_EXT_REFCLK[1:0]) to the McASP clocks. Therefore, GPIO mode control is not functional for these specific pins. 0 `Pin functions as input.` 1 `Pin functions as output.`
26	ACLKX	R/W	0h	Determines if ACLKX pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`
25	AMUTE	R/W	0h	Determines if AMUTE pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`
24:16	RESERVED68	R	0h	
15:0	AXR	R/W	0h	Determines if AXRn pin functions as an input or output. 0 `Pin functions as input.` 1 `Pin functions as output.`

14.7.1.2.2.5 MCASP_PDOUT Register

14.7.1.2.2.5.1 MCASP_PDOUT Register (Offset = 18h) [reset = 0h]

The pin data output register (PDOUT) holds a value for data out at all times, and may be read back at all times. The value held by PDOUT is not affected by writing to PDIR and PFUNC. However, the data value in PDOUT is driven out onto the McASP pin only if the corresponding bit in PFUNC is set to 1 (GPIO function) and the corresponding bit in PDIR is set to 1 (output). When reading data, returns the corresponding bit value in PDOUT[n], does not return input from I/O pin; when writing data, writes to the corresponding PDOUT[n] bit. PDOUT has these aliases or alternate addresses: PDSET When written to at this address, writing a 1 to a bit in PDSET sets the corresponding bit in PDOUT to 1; writing a 0 has no effect and keeps the bits in PDOUT unchanged. PDCLR When written to at this address, writing a 1 to a bit in PDCLR clears the corresponding bit in PDOUT to 0; writing a 0 has no effect and keeps the bits in PDOUT unchanged. There is only one set of data out bits, PDOUT[31-0]. The other registers, PDSET and PDCLR, are just different addresses for the same control bits, with different behaviors during writes. CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation.

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Table 14-10154. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0018h
MCASP1	02B1 0018h
MCASP2	02B2 0018h
MCASP3	02B3 0018h
MCASP4	02B4 0018h

Figure 14-5021. MCASP_PDOUT Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED69
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED69							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED69							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED69				AXR			
R				R/W			
0h				0h			

Table 14-10155. MCASP_PDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Determines drive on AFSR output pin when the corresponding PFUNC[31] and PDIR[31] bits are set to 1. 0 Pin drives low. 1 Pin drives high.

Table 14-10155. MCASP_PDOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	AHCLKR	R/W	0h	Determines drive on AHCLKR output pin when the corresponding PFUNC[30] and PDIR[30] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
29	ACLKR	R/W	0h	Determines drive on ACLKR output pin when the corresponding PFUNC[29] and PDIR[29] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
28	AFSX	R/W	0h	Determines drive on AFSX output pin when the corresponding PFUNC[28] and PDIR[28] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
27	AHCLKX	R/W	0h	Determines drive on AHCLKX output pin when the corresponding PFUNC[27] and PDIR[27] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
26	ACLKX	R/W	0h	Determines drive on ACLKX output pin when the corresponding PFUNC[26] and PDIR[26] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
25	AMUTE	R/W	0h	Determines drive on AMUTE output pin when the corresponding PFUNC[25] and PDIR[25] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`
24:4	RESERVED69	R	0h	
3:0	AXR	R/W	0h	Determines drive on AXR[n] output pin when the corresponding PFUNC[n] and PDIR[n] bits are set to 1. 0 `Pin drives low.` 1 `Pin drives high.`

14.7.1.2.2.6 MCASP_PDIN Register

14.7.1.2.2.6.1 MCASP_PDIN Register (Offset = 1Ch) [reset = 0h]

The pin data input register (PDIN) holds the I/O pin state of each of the McASP pins. PDIN allows the actual value of the pin to be read, regardless of the state of PFUNC and PDIR. The value after reset for registers 1 through 15 and 24 through 31 depends on how the pins are being driven. CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation.

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Table 14-10156. Instance Table

Instance Name	Physical Address
MCASP0	02B0 001Ch
MCASP1	02B1 001Ch
MCASP2	02B2 001Ch
MCASP3	02B3 001Ch
MCASP4	02B4 001Ch

Figure 14-5022. MCASP_PDIN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>AFSR</td><td>AHCLKR</td><td>ACLKR</td><td>AFSX</td><td>AHCLKX</td><td>ACLKX</td><td>AMUTE</td><td>RESERVED70</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED70</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED70</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED70</td><td colspan="4">AXR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-10157. MCASP_PDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Logic level on AFSR pin. 0 Pin is logic low. 1 Pin is logic high.
30	AHCLKR	R/W	0h	Logic level on AHCLKR pin. 0 Pin is logic low. 1 Pin is logic high.
29	ACLKR	R/W	0h	Logic level on ACLKR pin. 0 Pin is logic low. 1 Pin is logic high.
28	AFSX	R/W	0h	Logic level on AFSX pin. 0 Pin is logic low. 1 Pin is logic high.

Table 14-10157. MCASP_PDIN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	AHCLKX	R/W	0h	Logic level on AHCLKX pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
26	ACLKX	R/W	0h	Logic level on ACLKX pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
25	AMUTE	R/W	0h	Logic level on AMUTE pin. 0 `Pin is logic low.` 1 `Pin is logic high.`
24:4	RESERVED70	R	0h	
3:0	AXR	R/W	0h	Logic level on AXR[n] pin. 0 `Pin is logic low.` 1 `Pin is logic high.`

14.7.1.2.2.7 MCASP_PDCLR Register

14.7.1.2.2.7.1 MCASP_PDCLR Register (Offset = 20h) [reset = 0h]

The pin data clear register (PDCLR) is an alias of the pin data output register (PDOUT) for writes only. Writing a 1 to the PDCLR bit clears the corresponding bit in PDOUT and, if PFUNC = 1 (GPIO function) and PDIR = 1 (output), drives a logic low on the pin. PDCLR is useful for a multitasking system because it allows you to clear to a logic low only the desired pin(s) within a system without affecting other I/O pins controlled by the same McASP. CAUTION: Writing a value other than 0 to reserved bits in this register may cause improper device operation.

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Table 14-10158. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0020h
MCASP1	02B1 0020h
MCASP2	02B2 0020h
MCASP3	02B3 0020h
MCASP4	02B4 0020h

Figure 14-5023. MCASP_PDCLR Name Register

31	30	29	28	27	26	25	24
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED71
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED71							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED71							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED71				AXR			
R				R/W			
0h				0h			

Table 14-10159. MCASP_PDCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AFSR	R/W	0h	Allows the corresponding AFSR bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[31] bit is cleared to 0.`
30	AHCLKR	R/W	0h	Allows the corresponding AHCLKR bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[30] bit is cleared to 0.`
29	ACLKR	R/W	0h	Allows the corresponding ACLKR bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[29] bit is cleared to 0.`

Table 14-10159. MCASP_PDCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	AFSX	R/W	0h	Allows the corresponding AFSX bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[28] bit is cleared to 0.`
27	AHCLKX	R/W	0h	Allows the corresponding AHCLKX bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[27] bit is cleared to 0.`
26	ACLKX	R/W	0h	Allows the corresponding ACLKX bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[26] bit is cleared to 0.`
25	AMUTE	R/W	0h	Allows the corresponding AMUTE bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[25] bit is cleared to 0.`
24:4	RESERVED71	R	0h	
3:0	AXR	R/W	0h	Allows the corresponding AXR[n] bit in PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0 `No effect.` 1 `PDOUT[n] bit is cleared to 0.`

14.7.1.2.2.8 MCASP_GBLCTL Register

14.7.1.2.2.8.1 MCASP_GBLCTL Register (Offset = 44h) [reset = 0h]

The global control register (GBLCTL) provides initialization of the transmit and receive sections. The bit fields in GBLCTL are synchronized and latched by the corresponding clocks (ACLKX for bits 12-8 and ACLKR for bits 4-0). Before GBLCTL is programmed, you must ensure that serial clocks are running. If the corresponding external serial clocks, ACLKX and ACLKR, are not yet running, you should select the internal serial clock source in AHCLKXCTL, AHCLKRCTL, ACLKXCTL, and ACLKRCTL before GBLCTL is programmed. Also, after programming any bits in GBLCTL you should not proceed until you have read back from GBLCTL and verified that the bits are latched in GBLCTL.

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Table 14-10160. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0044h
MCASP1	02B1 0044h
MCASP2	02B2 0044h
MCASP3	02B3 0044h
MCASP4	02B4 0044h

Figure 14-5024. MCASP_GBLCTL Name Register

31	30	29	28	27	26	25	24
RESERVED73							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED73							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED73			XFRST	XSMRST	XSRCLR	XHCLKRST	XCLKRST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED72			RFRST	RSMRST	RSRCLR	RHCLKRST	RCLKRST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-10161. MCASP_GBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED73	R	0h	
12	XFRST	R/W	0h	Transmit frame sync generator reset enable bit. 0 Transmit frame sync generator is reset. 1 Transmit frame sync generator is active. When released from reset, the transmit frame sync generator begins counting serial clocks and generating frame sync as programmed.

Table 14-10161. MCASP_GBLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	XSMRST	R/W	0h	Transmit state machine reset enable bit. 0 Transmit state machine is held in reset. AXRn pin state: If PFUNC[n] = 0 and PDIR[n] = 1; then the serializer drives the AXRn pin to the state specified for inactive time slot (as determined by DISMOD bits in SRCTL). 1 Transmit state machine is released from reset. When released from reset, the transmit state machine immediately transfers data from XRBUF[n] to XRSR[n]. The transmit state machine sets the underrun flag (XUNDRN) in XSTAT, if XRBUF[n] have not been preloaded with data before reset is released. The transmit state machine also immediately begins detecting frame sync and is ready to transmit. Transmit TDM time slot begins at slot 0 after reset is released.
10	XSRCLR	R/W	0h	Transmit serializer clear enable bit. By clearing then setting this bit, the transmit buffer is flushed to an empty state [XDATA = 1]. If XSMRST = 1, XSRCLR = 1, XDATA = 1, and XBUF is not loaded with new data before the start of the next active time slot, an underrun will occur. 0 Transmit serializers are cleared. 1 Transmit serializers are active. When the transmit serializers are first taken out of reset (XSRCLR changes from 0 to 1), the transmit data ready bit (XDATA) in XSTAT is set to indicate XBUF is ready to be written.
9	XHCLKRST	R/W	0h	Transmit high-frequency clock divider reset enable bit. 0 Transmit high-frequency clock divider is held in reset and passes through its input as divide-by-1. 1 Transmit high-frequency clock divider is running.
8	XCLKRST	R/W	0h	Transmit clock divider reset enable bit. 0 Transmit clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 1 Transmit clock divider is running.
7:5	RESERVED72	R	0h	
4	RFRST	R/W	0h	Receive frame sync generator reset enable bit. 0 Receive frame sync generator is reset. 1 Receive frame sync generator is active. When released from reset, the receive frame sync generator begins counting serial clocks and generating frame sync as programmed.
3	RSMRST	R/W	0h	Receive state machine reset enable bit. 0 Receive state machine is held in reset. 1 Receive state machine is released from reset. When released from reset, the receive state machine immediately begins detecting frame sync and is ready to receive. Receive TDM time slot begins at slot 0 after reset is released.
2	RSRCLR	R/W	0h	Receive serializer clear enable bit. By clearing then setting this bit, the receive buffer is flushed. 0 Receive serializers are cleared. 1 Receive serializers are active.

Table 14-10161. MCASP_GBLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RHCLKRST	R/W	0h	Receive high-frequency clock divider reset enable bit. 0 Receive high-frequency clock divider is held in reset and passes through its input as divide-by-1. 1 Receive high-frequency clock divider is running.
0	RCLKRST	R/W	0h	Receive high-frequency clock divider reset enable bit. 0 Receive clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 1 Receive clock divider is running.

14.7.1.2.2.9 MCASP_AMUTE Register

14.7.1.2.2.9.1 MCASP_AMUTE Register (Offset = 48h) [reset = 0h]

The audio mute control register (AMUTE) controls the McASP audio mute (AMUTE) output pin. The value after reset for register 4 depends on how the pins are being driven.

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Table 14-10162. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0048h
MCASP1	02B1 0048h
MCASP2	02B2 0048h
MCASP3	02B3 0048h
MCASP4	02B4 0048h

Figure 14-5025. MCASP_AMUTE Name Register

31	30	29	28	27	26	25	24
RESERVED74							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED74							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED74			XDMAERR	RDMAERR	XCKFAIL	RCKFAIL	XSYNCERR
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RSYNCERR	XUNDRN	ROVRN	INSTAT	INEN	INPOL	MUTEN	
R/W	R/W	R/W	R	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-10163. MCASP_AMUTE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED74	R	0h	
12	XDMAERR	R/W	0h	If transmit DMA error [XDMAERR], drive AMUTE active enable bit. 0 Drive is disabled. Detection of transmit DMA error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of transmit DMA error, AMUTE is active and is driven according to MUTEN bit.
11	RDMAERR	R/W	0h	If receive DMA error [RDMAERR], drive AMUTE active enable bit. 0 Drive is disabled. Detection of receive DMA error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of receive DMA error, AMUTE is active and is driven according to MUTEN bit.
10	XCKFAIL	R/W	0h	If transmit clock failure [XCKFAIL], drive AMUTE active enable bit. 0 Drive is disabled. Detection of transmit clock failure is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of transmit clock failure, AMUTE is active and is driven according to MUTEN bit

Table 14-10163. MCASP_AMUTE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RCKFAIL	R/W	0h	If receive clock failure [RCKFAIL], drive AMUTE active enable bit. 0 Drive is disabled. Detection of receive clock failure is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of receive clock failure, AMUTE is active and is driven according to MUTEN bit.
8	XSYNCERR	R/W	0h	If unexpected transmit frame sync error [XSYNCERR], drive AMUTE active enable bit. 0 Drive is disabled. Detection of unexpected transmit frame sync error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of unexpected transmit frame sync error, AMUTE is active and is driven according to MUTEN bit.
7	RSYNCERR	R/W	0h	If unexpected receive frame sync error [RSYNCERR], drive AMUTE active enable bit. 0 Drive is disabled. Detection of unexpected receive frame sync error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of unexpected receive frame sync error, AMUTE is active and is driven according to MUTEN bit.
6	XUNDRN	R/W	0h	If transmit underrun error [XUNDRN], drive AMUTE active enable bit. 0 Drive is disabled. Detection of transmit underrun error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of transmit underrun error, AMUTE is active and is driven according to MUTEN bit.
5	ROVRN	R/W	0h	If receiver overrun error [ROVRN], drive AMUTE active enable bit. 0 Drive is disabled. Detection of receiver overrun error is ignored by AMUTE. 1 Drive is enabled (active). Upon detection of receiver overrun error, AMUTE is active and is driven according to MUTEN bit.
4	INSTAT	R	0h	Determines drive on AXRn pin when PFUNC[n] and PDIR[n] bits are set to 1. 0 AMUTEIN pin is inactive. 1 AMUTEIN pin is active. Audio mute in error is detected.
3	INEN	R/W	0h	Drive AMUTE active when AMUTEIN error is active [INSTAT = 1]. 0 Drive is disabled. AMUTEIN is ignored by AMUTE. 1 Drive is enabled (active). INSTAT = 1 drives AMUTE active.
2	INPOL	R/W	0h	Audio mute in [AMUTEIN] polarity select bit. 0 Polarity is active high. A high on AMUTEIN sets INSTAT to 1. 1 Polarity is active low. A low on AM UTEIN sets INSTAT to 1.
1:0	MUTEN	R/W	0h	AMUTE pin enable bit [unless overridden by GPIO registers]. 0 AMUTE pin is disabled, pin goes to tri-state condition. 1 AMUTE pin is driven high if error is detected. 2 AMUTE pin is driven low if error is detected. 3 Reserved

14.7.1.2.2.10 MCASP_DLBCTL Register

14.7.1.2.2.10.1 MCASP_DLBCTL Register (Offset = 4Ch) [reset = 0h]

The digital loopback control register (DLBCTL) controls the internal loopback settings of the McASP in TDM mode.

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Table 14-10164. Instance Table

Instance Name	Physical Address
MCASP0	02B0 004Ch
MCASP1	02B1 004Ch
MCASP2	02B2 004Ch
MCASP3	02B3 004Ch
MCASP4	02B4 004Ch

Figure 14-5026. MCASP_DLBCTL Name Register

31	30	29	28	27	26	25	24
RESERVED75							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED75							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED75							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED75				MODE		ORD	DLBEN
R				R/W		R/W	R/W
0h				0h		0h	0h

Table 14-10165. MCASP_DLBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED75	R	0h	
3:2	MODE	R/W	0h	Loopback generator mode bits. Applies only when loopback mode is enabled [DLBEN = 1]. 0 `Default and reserved on loopback mode (DLBEN = 1). When in non-loopback mode (DLBEN = 0), MODE should be left at default (00). When in loopback mode (DLBEN = 1), MODE = 00 is reserved and is not applicable.` 1 `Transmit clock and frame sync generators used by both transmit and receive sections. When in loopback mode (DLBEN = 1), MODE must be 01.` 2 `Reserved.` 3 `Reserved.`

Table 14-10165. MCASP_DLBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ORD	R/W	0h	Loopback order bit when loopback mode is enabled [DLBEN = 1]. 0 `Odd serializers N + 1 transmit to even serializers N that receive. The corresponding serializers must be programmed properly.` 1 `Even serializers N transmit to odd serializers N + 1 that receive. The corresponding serializers must be programmed properly.`
0	DLBEN	R/W	0h	Loopback mode enable bit. 0 `Loopback mode is disabled.` 1 `Loopback mode is enabled.`

14.7.1.2.2.11 MCASP_DITCTL Register

14.7.1.2.2.11.1 MCASP_DITCTL Register (Offset = 50h) [reset = 0h]

The DIT mode control register (DITCTL) controls DIT operations of the McASP.

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Table 14-10166. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0050h
MCASP1	02B1 0050h
MCASP2	02B2 0050h
MCASP3	02B3 0050h
MCASP4	02B4 0050h

Figure 14-5027. MCASP_DITCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED77</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED77</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED77</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED77</td><td>VB</td><td>VA</td><td>RESERVED76</td><td>DITEN</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td>R/W</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10167. MCASP_DITCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED77	R	0h	
3	VB	R/W	0h	Valid bit for odd time slots [DIT right subframe]. 0 `V bit is 0 during odd DIT subframes.` 1 `V bit is 1 during odd DIT subframes.`
2	VA	R/W	0h	Valid bit for even time slots [DIT left subframe]. 0 `V bit is 0 during even DIT subframes.` 1 `V bit is 1 during even DIT subframes.`
1	RESERVED76	R	0h	
0	DITEN	R/W	0h	DIT mode enable bit. DITEN should only be changed while the XSMRST bit in GBLCTL is in reset [and for startup, XSRCLR also in reset]. However, it is not necessary to reset the XCLKRST or XHCLKRST bits in GBLCTL to change DITEN. 0 `DIT mode is disabled. Transmitter operates in TDM or burst mode.` 1 `DIT mode is enabled. Transmitter operates in DIT encoded mode.`

14.7.1.2.2.12 MCASP_RGBLCTL Register

14.7.1.2.2.12.1 MCASP_RGBLCTL Register (Offset = 60h) [reset = 0h]

Alias of the global control register (GBLCTL). Writing to the receiver global control register (RGBLCTL) affects only the receive bits of GBLCTL (bits 4-0). Reads from RGBLCTL return the value of GBLCTL. RGBLCTL allows the receiver to be reset independently from the transmitter.

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Table 14-10168. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0060h
MCASP1	02B1 0060h
MCASP2	02B2 0060h
MCASP3	02B3 0060h
MCASP4	02B4 0060h

Figure 14-5028. MCASP_RGBLCTL Name Register

31	30	29	28	27	26	25	24
RESERVED79							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED79							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED79			XFRST	XSMRST	XSRCLR	XHCLKRST	XCLKRST
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED78			RFRST	RSMRST	RSRCLR	RHCLKRST	RCLKRST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-10169. MCASP_RGBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED79	R	0h	
12	XFRST	R	0h	Transmit frame sync generator reset enable bit. A read of this bit returns the XFRST bit value of GBLCTL. Writes have no effect.
11	XSMRST	R	0h	Transmit state machine reset enable bit. A read of this bit returns the XSMRST bit value of GBLCTL. Writes have no effect.
10	XSRCLR	R	0h	Transmit serializer clear enable bit. A read of this bit returns the XSRCLR bit value of GBLCTL. Writes have no effect.
9	XHCLKRST	R	0h	Transmit high-frequency clock divider reset enable bit. A read of this bit returns the XHCLKRST bit value of GBLCTL. Writes have no effect.
8	XCLKRST	R	0h	Transmit clock divider reset enable bit. A read of this bit returns the XCLKRST bit value of GBLCTL. Writes have no effect.
7:5	RESERVED78	R	0h	

Table 14-10169. MCASP_RGBLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RFRST	R/W	0h	Receive frame sync generator reset enable bit. A write to this bit affects the RFRST bit of GBLCTL. 0 Receive frame sync generator is reset. 1 Receive frame sync generator is active.
3	RSMRST	R/W	0h	Receive state machine reset enable bit. A write to this bit affects the RSMRST bit of GBLCTL. 0 Receive state machine is held in reset. 1 Receive state machine is released from reset.
2	RSRCLR	R/W	0h	Receive serializer clear enable bit. A write to this bit affects the RSRCLR bit of GBLCTL. 0 Receive serializers are cleared. 1 Receive serializers are active.
1	RHCLKRST	R/W	0h	Receive high-frequency clock divider reset enable bit. A write to this bit affects the RHCLKRST bit of GBLCTL. 0 Receive high-frequency clock divider is held in reset and passes through its input as divide-by-1. 1 Receive high-frequency clock divider is running.
0	RCLKRST	R/W	0h	Receive clock divider reset enable bit. A write to this bit affects the RCLKRST bit of GBLCTL. 0 Receive clock divider is held in reset. 1 Receive clock divider is running.

14.7.1.2.2.13 MCASP_RMASK Register

14.7.1.2.2.13.1 MCASP_RMASK Register (Offset = 64h) [reset = 0h]

The receive format unit bit mask register (RMASK) determines which bits of the received data are masked off and padded with a known value before being read by the CPU or DMA.

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Table 14-10170. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0064h
MCASP1	02B1 0064h
MCASP2	02B2 0064h
MCASP3	02B3 0064h
MCASP4	02B4 0064h

Figure 14-5029. MCASP_RMASK Name Register

31	30	29	28	27	26	25	24
RMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
RMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
RMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
RMASK							
R/W							
0h							

Table 14-10171. MCASP_RMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RMASK	R/W	0h	Receive data mask n enable bit. 0 Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in RFMT). 1 Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA.

14.7.1.2.2.14 MCASP_RFMT Register

14.7.1.2.2.14.1 MCASP_RFMT Register (Offset = 68h) [reset = 0h]

The receive bit stream format register (RFMT) configures the receive data format.

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Table 14-10172. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0068h
MCASP1	02B1 0068h
MCASP2	02B2 0068h
MCASP3	02B3 0068h
MCASP4	02B4 0068h

Figure 14-5030. MCASP_RFMT Name Register

31	30	29	28	27	26	25	24
RESERVED80							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED80						RDATDLY	
R						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RRVRS	RPAD		RPBIT				
R/W	R/W		R/W				
0h	0h		0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSSZ				RBUSEL	RROT		
R/W				R/W	R/W		
0h				0h	0h		

Table 14-10173. MCASP_RFMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED80	R	0h	
17:16	RDATDLY	R/W	0h	Receive bit delay. 0 `0-bit delay. The first receive data bit, AXRn, occurs in same ACLKR cycle as the receive frame sync (AFSR).` 1 `1-bit delay. The first receive data bit, AXRn, occurs one ACLKR cycle after the receive frame sync (AFSR).` 2 `2-bit delay. The first receive data bit, AXRn, occurs two ACLKR cycles after the receive frame sync (AFSR).` 3 `Reserved.`
15	RRVRS	R/W	0h	Receive serial bitstream order. 0 `Bitstream is LSB first. No bit reversal is performed in receive format bit reverse unit.` 1 `Bitstream is MSB first. Bit reversal is performed in receive format bit reverse unit.`

Table 14-10173. MCASP_RFMT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	RPAD	R/W	0h	Pad value for extra bits in slot not belonging to the word. This field only applies to bits when RMASK[n] = 0. 0 Pad extra bits with 0. 1 Pad extra bits with 1. 2 Pad extra bits with one of the bits from the word as specified by RPBIT bits. 3 Reserved.
12:8	RPBIT	R/W	0h	RPBIT value determines which bit [as read by the CPU or DMA from RBUF[n]] is used to pad the extra bits. This field only applies when RPAD = 2h. 0 Pad with bit 0 value. 1 Pad with bit 1 to bit 31 value from 1h to 1Fh.
7:4	RSSZ	R/W	0h	Receive slot size. 0 Reserved. 1 Reserved. 2 Reserved. 3 Slot size is 8 bits. 4 Reserved 5 Slot size is 12 bits. 6 Reserved 7 Slot size is 16 bits. 8 Reserved 9 Slot size is 20 bits. 10 Reserved 11 Slot size is 24 bits 12 Reserved 13 Slot size is 28 bits. 14 Reserved 15 Slot size is 32 bits.
3	RBUSEL	R/W	0h	Selects whether reads from serializer buffer XRBUF[n] originate from the configuration bus [CFG] or the data [DAT] port. 0 Reads from XRBUF[n] originate on data port. Reads from XRBUF[n] on configuration bus are ignored. 1 Reads from XRBUF[n] originate on configuration bus. Reads from XRBUF[n] on data port are ignored.
2:0	RROT	R/W	0h	Right-rotation value for receive rotate right format unit. 0 Rotate right by 0 (no rotation). 1 Rotate right by 4 bit positions. 2 Rotate right by 8 bit positions. 3 Rotate right by 12 bit positions. 4 Rotate right by 16 bit positions. 5 Rotate right by 20 bit positions. 6 Rotate right by 24 bit positions. 7 Rotate right by 28 bit positions.

14.7.1.2.2.15 MCASP_AFSRCTL Register

14.7.1.2.2.15.1 MCASP_AFSRCTL Register (Offset = 6Ch) [reset = 0h]

The receive frame sync control register (AFSRCTL) configures the receive frame sync (AFSR).

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Table 14-10174. Instance Table

Instance Name	Physical Address
MCASP0	02B0 006Ch
MCASP1	02B1 006Ch
MCASP2	02B2 006Ch
MCASP3	02B3 006Ch
MCASP4	02B4 006Ch

Figure 14-5031. MCASP_AFSRCTL Name Register

31	30	29	28	27	26	25	24
RESERVED83							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED83							
R							
0h							
15	14	13	12	11	10	9	8
RMOD							
R/W							
0h							
7	6	5	4	3	2	1	0
RMOD	RESERVED82		FRWID	RESERVED81		FSRM	FSRP
R/W	R		R/W	R		R/W	R/W
0h	0h		0h	0h		0h	0h

Table 14-10175. MCASP_AFSRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED83	R	0h	

15:7	RMOD	R/W	0h	Receive frame sync mode select bits. 1FFh = Reserved from 181h to 1FFh.
				`0` `Burst mode.`
				`1` `Reserved.`
				`2` `2-slot TDM (I2S mode) to 32-slot TDM from 2h to 20h.`
				`33` `Reserved from 21h to 17Fh.`
				`384` `384-slot TDM (external DIR IC inputting 384-slot DIR frames to MCASP over I2S interface).`
				`385` `Reserved from 181h to 1FFh.`

6:5	RESERVED82	R	0h	

4	FRWID	R/W	0h	Receive frame sync width select bit indicates the width of the receive frame sync [AFSR] during its active period.
				`0` `Single bit.`
				`1` `Single word.`

3:2	RESERVED81	R	0h	

Table 14-10175. MCASP_AFSRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FSRM	R/W	0h	Receive frame sync generation select bit. 0 `Externally-generated receive frame sync.` 1 `Internally-generated receive frame sync.`
0	FSRP	R/W	0h	Receive frame sync polarity select bit. 0 `A rising edge on receive frame sync (AFSR) indicates the beginning of a frame.` 1 `A falling edge on receive frame sync (AFSR) indicates the beginning of a frame.`

14.7.1.2.2.16 MCASP_ACLKRCTL Register

14.7.1.2.2.16.1 MCASP_ACLKRCTL Register (Offset = 70h) [reset = 20h]

The receive clock control register (ACLKRCTL) configures the receive bit clock (ACLKR) and the receive clock generator.

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Table 14-10176. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0070h
MCASP1	02B1 0070h
MCASP2	02B2 0070h
MCASP3	02B3 0070h
MCASP4	02B4 0070h

Figure 14-5032. MCASP_ACLKRCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED86</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED86</td><td>BUSY</td><td>DIVBUSY</td><td>ADJBUSY</td><td colspan="2">CLKRADJ</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED85</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CLKRP</td><td>RESERVED84</td><td>CLKRM</td><td colspan="5">CLKRDIV</td></tr>
<tr><td>R/W</td><td>R</td><td>R/W</td><td colspan="5">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>1h</td><td colspan="5">0h</td></tr>
</table>

Table 14-10177. MCASP_ACLKRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED86	R/W	0h	
20	BUSY	R/W	0h	Status: logical OR of DIVBUSY, ADJBUSY
19	DIVBUSY	R/W	0h	Status: divide ratio change in progress
18	ADJBUSY	R/W	0h	Status: one-shot adjustment in progress
17:16	CLKRADJ	W	0h	CLKRDIV one-shot adjustment
15:8	RESERVED85	R/W	0h	
7	CLKRP	R/W	0h	Receive bitstream clock polarity select bit. 0 Falling edge. Receiver samples data on the falling edge of the serial clock, so the external transmitter driving this receiver must shift data out on the rising edge of the serial clock. 1 Rising edge. Receiver samples data on the rising edge of the serial clock, so the external transmitter driving this receiver must shift data out on the falling edge of the serial clock.
6	RESERVED84	R	0h	

Table 14-10177. MCASP_ACLKRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLKRM	R/W	1h	Receive bit clock source bit. Note that this bit does not have any effect, if ACLKXCTL.ASYNC = 0. 0 `External receive clock source from ACLKR pin.` 1 `Internal receive clock source from output of programmable bit clock divider.`
4:0	CLKRDIV	R/W	0h	Receive bit clock divide ratio bits determine the divide-down ratio from AHCLKR to ACLKR. Note that this bit does not have any effect, if ACLKXCTL.ASYNC = 0. 0 `Divide-by-1.` 1 `Divide-by-2.` 2 `Divide-by-3 to divide-by-32 from 2h to 1Fh.`

14.7.1.2.2.17 MCASP_AHCLKRCTL Register

14.7.1.2.2.17.1 MCASP_AHCLKRCTL Register (Offset = 74h) [reset = 8000h]

The receive high-frequency clock control register (AHCLKRCTL) configures the receive high-frequency controller clock (AHCLKR) and the receive clock generator.

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Table 14-10178. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0074h
MCASP1	02B1 0074h
MCASP2	02B2 0074h
MCASP3	02B3 0074h
MCASP4	02B4 0074h

Figure 14-5033. MCASP_AHCLKRCTL Name Register

31	30	29	28	27	26	25	24
RESERVED88							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED88			BUSY	DIVBUSY	ADJBUSY	HCLKRADJ	
R/W			R/W	R/W	R/W	W	
0h			0h	0h	0h	0h	
15	14	13	12	11	10	9	8
HCLKRM	HCLKRP	RESERVED87		HCLKRDIV			
R/W	R/W	R		R/W			
1h	0h	0h		0h			
7	6	5	4	3	2	1	0
HCLKRDIV							
R/W							
0h							

Table 14-10179. MCASP_AHCLKRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED88	R/W	0h	
20	BUSY	R/W	0h	Status: logical OR of DIVBUSY, ADJBUSY
19	DIVBUSY	R/W	0h	Status: divide ratio change in progress?
18	ADJBUSY	R/W	0h	Status: one-shot adjustment in progress?
17:16	HCLKRADJ	W	0h	HCLKRDIV one-shot adjustment
15	HCLKRM	R/W	1h	Receive high-frequency clock source bit. 0 External receive high-frequency clock source from AHCLKR pin. 1 Internal receive high-frequency clock source from output of programmable high clock divider.

Table 14-10179. MCASP_AHCLKRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	HCLKRP	R/W	0h	Receive bitstream high-frequency clock polarity select bit. 0 AHCLKR is not inverted before programmable bit clock divider. In the special case where the receive bit clock (ACLKR) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKRDIV = 0 in ACLKRCTL), AHCLKR is directly passed through to the ACLKR pin. 1 AHCLKR is inverted before programmable bit clock divider. In the special case where the receive bit clock (ACLKR) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKRDIV = 0 in ACLKRCTL), AHCLKR is directly passed through to the ACLKR pin.
13:12	RESERVED87	R	0h	
11:0	HCLKRDIV	R/W	0h	Receive high-frequency clock divide ratio bits determine the divide-down ratio from AUXCLK to AHCLKR. 0 Divide-by-1. 1 Divide-by-2. 2 Divide-by-3 to divide-by-4096 from 2h to FFFh.

14.7.1.2.2.18 MCASP_RTDM Register

14.7.1.2.2.18.1 MCASP_RTDM Register (Offset = 78h) [reset = 0h]

The receive TDM time slot register (RTDM) specifies which TDM time slot the receiver is active.

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Table 14-10180. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0078h
MCASP1	02B1 0078h
MCASP2	02B2 0078h
MCASP3	02B3 0078h
MCASP4	02B4 0078h

Figure 14-5034. MCASP_RTDM Name Register

31	30	29	28	27	26	25	24
RTDMS							
R/W							
0h							
23	22	21	20	19	18	17	16
RTDMS							
R/W							
0h							
15	14	13	12	11	10	9	8
RTDMS							
R/W							
0h							
7	6	5	4	3	2	1	0
RTDMS							
R/W							
0h							

Table 14-10181. MCASP_RTDM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RTDMS	R/W	0h	Receiver mode during TDM time slot n. 0 `Receive TDM time slot n is inactive. The receive serializer does not shift in data during this slot.` 1 `Receive TDM time slot n is active. The receive serializer shifts in data during this slot.`

14.7.1.2.2.19 MCASP_RINTCTL Register

14.7.1.2.2.19.1 MCASP_RINTCTL Register (Offset = 7Ch) [reset = 0h]

The receiver interrupt control register (RINTCTL) controls generation of the McASP receive interrupt (RINT). When the register bit(s) is set to 1, the occurrence of the enabled McASP condition(s) generates RINT. See the RSTAT register for a description of the interrupt conditions.

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Table 14-10182. Instance Table

Instance Name	Physical Address
MCASP0	02B0 007Ch
MCASP1	02B1 007Ch
MCASP2	02B2 007Ch
MCASP3	02B3 007Ch
MCASP4	02B4 007Ch

Figure 14-5035. MCASP_RINTCTL Name Register

31	30	29	28	27	26	25	24
RESERVED90							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED90							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED90							
R							
0h							
7	6	5	4	3	2	1	0
RSTAFRM	RESERVED89	RDATA	RLAST	RDMAERR	RCKFAIL	RSYNCERR	ROVRN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10183. MCASP_RINTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED90	R	0h	
7	RSTAFRM	R/W	0h	Receive start of frame interrupt enable bit. 0 `Interrupt is disabled. A receive start of frame interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. A receive start of frame interrupt generates a McASP receive interrupt (RINT).`
6	RESERVED89	R	0h	
5	RDATA	R/W	0h	Receive data ready interrupt enable bit. 0 `Interrupt is disabled. A receive data ready interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. A receive data ready interrupt generates a McASP receive interrupt (RINT).`

Table 14-10183. MCASP_RINTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RLAST	R/W	0h	Receive last slot interrupt enable bit. 0 `Interrupt is disabled. A receive last slot interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. A receive last slot interrupt generates a McASP receive interrupt (RINT).`
3	RDMAERR	R/W	0h	Receive DMA error interrupt enable bit. 0 `Interrupt is disabled. A receive DMA error interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. A receive DMA error interrupt generates a McASP receive interrupt (RINT).`
2	RCKFAIL	R/W	0h	Receive clock failure interrupt enable bit. 0 `Interrupt is disabled. A receive clock failure interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. A receive clock failure interrupt generates a McASP receive interrupt (RINT).`
1	RSYNCERR	R/W	0h	Unexpected receive frame sync interrupt enable bit. 0 `Interrupt is disabled. An unexpected receive frame sync interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. An unexpected receive frame sync interrupt generates a McASP receive interrupt (RINT).`
0	ROVRN	R/W	0h	Receiver overrun interrupt enable bit. 0 `Interrupt is disabled. A receiver overrun interrupt does not generate a McASP receive interrupt (RINT).` 1 `Interrupt is enabled. A receiver overrun interrupt generates a McASP receive interrupt (RINT).`

14.7.1.2.2.20 MCASP_RSTAT Register

14.7.1.2.2.20.1 MCASP_RSTAT Register (Offset = 80h) [reset = 0h]

The receiver status register (RSTAT) provides the receiver status and receive TDM time slot number. If the McASP logic attempts to set an interrupt flag in the same cycle that the CPU writes to the flag to clear it, the McASP logic has priority and the flag remains set. This also causes a new interrupt request to be generated.

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Table 14-10184. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0080h
MCASP1	02B1 0080h
MCASP2	02B2 0080h
MCASP3	02B3 0080h
MCASP4	02B4 0080h

Figure 14-5036. MCASP_RSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED91</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED91</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED91</td><td>RERR</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RDMAERR</td><td>RSTAFRM</td><td>RDATA</td><td>RLAST</td><td>RTDMSLOT</td><td>RCKFAIL</td><td>RSYNCERR</td><td>ROVRN</td></tr>
<tr><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10185. MCASP_RSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED91	R	0h	
8	RERR	R/W	0h	RERR bit always returns a logic-OR of: ROVRN OR RSYNCERR OR RCKFAIL OR RDMAERR. Allows a single bit to be checked to determine if a receiver error interrupt has occurred. 0 No errors have occurred. 1 An error has occurred.
7	RDMAERR	R/W1TC	0h	Receive DMA error flag. RDMAERR is set when the CPU or DMA reads more serializers through the data port in a given time slot than were programmed as receivers. Causes a receive interrupt [RINT], if this bit is set and RDMAERR in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 Receive DMA error did not occur. 1 Receive DMA error did occur.

Table 14-10185. MCASP_RSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RSTAFRM	R/W1TC	0h	Receive start of frame flag. Causes a receive interrupt [RINT], if this bit is set and RSTAFRM in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 `No new receive frame sync (AFSR) is detected.` 1 `A new receive frame sync (AFSR) is detected.`
5	RDATA	R/W1TC	0h	Receive data ready flag. Causes a receive interrupt [RINT], if this bit is set and RDATA in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 `No new data in RBUF.` 1 `Data is transferred from XRSR to RBUF and ready to be serviced by the CPU or DMA. When RDATA is set, it always causes a DMA event (AREVT).`
4	RLAST	R/W1TC	0h	Receive last slot flag. RLAST is set along with RDATA, if the current slot is the last slot in a frame. Causes a receive interrupt [RINT], if this bit is set and RLAST in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 `Current slot is not the last slot in a frame.` 1 `Current slot is the last slot in a frame. RDATA is also set.`
3	RTDMSLOT	R	0h	Returns the LSB of RSLOT. Allows a single read of RSTAT to determine whether the current TDM time slot is even or odd. 0 `Current TDM time slot is odd.` 1 `Current TDM time slot is even.`
2	RCKFAIL	R/W1TC	0h	Receive clock failure flag. RCKFAIL is set when the receive clock failure detection circuit reports an error. Causes a receive interrupt [RINT], if this bit is set and RCKFAIL in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 `Receive clock failure did not occur.` 1 `Receive clock failure did occur.`
1	RSYNCERR	R/W1TC	0h	Unexpected receive frame sync flag. RSYNCERR is set when a new receive frame sync [AFSR] occurs before it is expected. Causes a receive interrupt [RINT], if this bit is set and RSYNCERR in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 `Unexpected receive frame sync did not occur.` 1 `Unexpected receive frame sync did occur.`
0	ROVRN	R/W1TC	0h	Receiver overrun flag. ROVRN is set when the receive serializer is instructed to transfer data from XRSR to RBUF, but the former data in RBUF has not yet been read by the CPU or DMA. Causes a receive interrupt [RINT], if this bit is set and ROVRN in RINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 to this bit has no effect. 0 `Receiver overrun did not occur.` 1 `Receiver overrun did occur.`

14.7.1.2.2.21 MCASP_RSLOT Register

14.7.1.2.2.21.1 MCASP_RSLOT Register (Offset = 84h) [reset = 0h]

The current receive TDM time slot register (RSLOT) indicates the current time slot for the receive data frame.

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Table 14-10186. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0084h
MCASP1	02B1 0084h
MCASP2	02B2 0084h
MCASP3	02B3 0084h
MCASP4	02B4 0084h

Figure 14-5037. MCASP_RSLOT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED92</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED92</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED92</td><td>RSLOTCNT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RSLOTCNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10187. MCASP_RSLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED92	R	0h	
8:0	RSLOTCNT	R	0h	0-17Fh = Current receive time slot count. Legal values: 0 to 383 [17Fh]. TDM function is not supported for > 32 time slots. However, TDM time slot counter may count to 383 when used to receive a DIR block [transferred over TDM format].

14.7.1.2.2.22 MCASP_RCLKCHK Register

14.7.1.2.2.22.1 MCASP_RCLKCHK Register (Offset = 88h) [reset = 0h]

The receive clock check control register (RCLKCHK) configures the receive clock failure detection circuit.

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Table 14-10188. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0088h
MCASP1	02B1 0088h
MCASP2	02B2 0088h
MCASP3	02B3 0088h
MCASP4	02B4 0088h

Figure 14-5038. MCASP_RCLKCHK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RCNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RMAX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RMIN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED93</td><td colspan="4">RPS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-10189. MCASP_RCLKCHK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RCNT	R	0h	Receive clock count value [from previous measurement]. The clock circuit continually counts the number of system clocks for every 32 receive high-frequency controller clock [AHCLKR] signals, and stores the count in RCNT until the next measurement is taken.
23:16	RMAX	R/W	0h	Receive clock maximum boundary. This 8 bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 receive high-frequency controller clock [AHCLKR] signals have been received. If the current counter value is greater than RMAX after counting 32 AHCLKR signals, RCKFAIL in RSTAT is set. The comparison is performed using unsigned arithmetic.
15:8	RMIN	R/W	0h	Receive clock minimum boundary. This 8 bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 receive high-frequency controller clock [AHCLKR] signals have been received. If RCNT is less than RMIN after counting 32 AHCLKR signals, RCKFAIL in RSTAT is set. The comparison is performed using unsigned arithmetic.
7:4	RESERVED93	R	0h	

Table 14-10189. MCASP_RCLKCHK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RPS	R/W	0h	Receive clock check prescaler value. 0 MCASP system clock divided by 1. 1 MCASP system clock divided by 2. 2 MCASP system clock divided by 4. 3 MCASP system clock divided by 8. 4 MCASP system clock divided by 16. 5 MCASP system clock divided by 32. 6 MCASP system clock divided by 64. 7 MCASP system clock divided by 128. 8 MCASP system clock divided by 256. 9 Reserved from 9h to Fh.

14.7.1.2.2.23 MCASP_XGBLCTL Register

14.7.1.2.2.23.1 MCASP_XGBLCTL Register (Offset = A0h) [reset = 0h]

Alias of the global control register (GBLCTL). Writing to the transmitter global control register (XGBLCTL) affects only the transmit bits of GBLCTL (bits 12-8). Reads from XGBLCTL return the value of GBLCTL. XGBLCTL allows the transmitter to be reset independently from the receiver. See the GBLCTL register for a detailed description of GBLCTL.

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Table 14-10190. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00A0h
MCASP1	02B1 00A0h
MCASP2	02B2 00A0h
MCASP3	02B3 00A0h
MCASP4	02B4 00A0h

Figure 14-5039. MCASP_XGBLCTL Name Register

31	30	29	28	27	26	25	24
RESERVED96							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED96							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED96			XFRST	XSMRST	XSRCLR	XHCLKRST	XCLKRST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED95			RFRST	RSMRST	RSRCLR	RHCLKRST	RCLKRST
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h

Table 14-10191. MCASP_XGBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED96	R	0h	
12	XFRST	R/W	0h	Transmit frame sync generator reset enable bit. A write to this bit affects the XFRST bit of GBLCTL. 0 `Transmit frame sync generator is reset.` 1 `Transmit frame sync generator is active.`
11	XSMRST	R/W	0h	Transmit state machine reset enable bit. A write to this bit affects the XSMRST bit of GBLCTL. 0 `Transmit state machine is held in reset.` 1 `Transmit state machine is released from reset.`
10	XSRCLR	R/W	0h	Transmit serializer clear enable bit. A write to this bit affects the XSRCLR bit of GBLCTL. 0 `Transmit serializers are cleared.` 1 `Transmit serializers are active.`

Table 14-10191. MCASP_XGBLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	XHCLKRST	R/W	0h	Transmit high-frequency clock divider reset enable bit. A write to this bit affects the XHCLKRST bit of GBLCTL. 0 `Transmit high-frequency clock divider is held in reset.` 1 `Transmit high-frequency clock divider is running.`
8	XCLKRST	R/W	0h	Transmit clock divider reset enable bit. A write to this bit affects the XCLKRST bit of GBLCTL. 0 `Transmit clock divider is held in reset.` 1 `Transmit clock divider is running.`
7:5	RESERVED95	R	0h	
4	RFRST	R	0h	Receive frame sync generator reset enable bit. A read of this bit returns the RFRST bit value of GBLCTL. Writes have no effect.
3	RSMRST	R	0h	Receive state machine reset enable bit. A read of this bit returns the RSMRST bit value of GBLCTL. Writes have no effect.
2	RSRCLR	R	0h	Receive serializer clear enable bit. A read of this bit returns the RSRSCLR bit value of GBLCTL. Writes have no effect.
1	RHCLKRST	R	0h	Receive high-frequency clock divider reset enable bit. A read of this bit returns the RHCLKRST bit value of GBLCTL. Writes have no effect.
0	RCLKRST	R	0h	Receive clock divider reset enable bit. A read of this bit returns the RCLKRST bit value of GBLCTL. Writes have no effect.

14.7.1.2.2.24 MCASP_XMASK Register

14.7.1.2.2.24.1 MCASP_XMASK Register (Offset = A4h) [reset = 0h]

The transmit format unit bit mask register (XMASK) determines which bits of the transmitted data are masked off and padded with a known value before being shifted out the McASP.

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Table 14-10192. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00A4h
MCASP1	02B1 00A4h
MCASP2	02B2 00A4h
MCASP3	02B3 00A4h
MCASP4	02B4 00A4h

Figure 14-5040. MCASP_XMASK Name Register

31	30	29	28	27	26	25	24
XMASK							
R/W							
0h							
23	22	21	20	19	18	17	16
XMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
XMASK							
R/W							
0h							
7	6	5	4	3	2	1	0
XMASK							
R/W							
0h							

Table 14-10193. MCASP_XMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XMASK	R/W	0h	Transmit data mask n enable bit. 0 Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in XFMT), which is transmitted out the McASP in place of the original bit. 1 Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP.

14.7.1.2.2.25 MCASP_XFMT Register

14.7.1.2.2.25.1 MCASP_XFMT Register (Offset = A8h) [reset = 0h]

The transmit bit stream format register (XFMT) configures the transmit data format.

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Table 14-10194. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00A8h
MCASP1	02B1 00A8h
MCASP2	02B2 00A8h
MCASP3	02B3 00A8h
MCASP4	02B4 00A8h

Figure 14-5041. MCASP_XFMT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED97</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED97</td><td colspan="2">XDATDLY</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>XRVRS</td><td colspan="2">XPAD</td><td colspan="5">XPBIT</td></tr>
<tr><td>R/W</td><td colspan="2">R/W</td><td colspan="5">R/W</td></tr>
<tr><td>0h</td><td colspan="2">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">XSSZ</td><td>XBUSEL</td><td colspan="3">XROT</td></tr>
<tr><td colspan="4">R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-10195. MCASP_XFMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED97	R	0h	
17:16	XDATDLY	R/W	0h	Transmit sync bit delay. 0 0-bit delay. The first transmit data bit, AXRn, occurs in same ACLKX cycle as the transmit frame sync (AFSX). 1 1-bit delay. The first transmit data bit, AXRn, occurs one ACLKX cycle after the transmit frame sync (AFSX). 2 2-bit delay. The first transmit data bit, AXRn, occurs two ACLKX cycles after the transmit frame sync (AFSX). 3 Reserved.
15	XRVRS	R/W	0h	Transmit serial bitstream order. 0 Bitstream is LSB first. No bit reversal is performed in transmit format bit reverse unit. 1 Bitstream is MSB first. Bit reversal is performed in transmit format bit reverse unit.

Table 14-10195. MCASP_XFMT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	XPAD	R/W	0h	Pad value for extra bits in slot not belonging to word defined by XMASK. This field only applies to bits when XMASK[n] = 0. 0 Pad extra bits with 0. 1 Pad extra bits with 1. 2 Pad extra bits with one of the bits from the word as specified by XPBIT bits. 3 Reserved.
12:8	XPBIT	R/W	0h	XPBIT value determines which bit [as written by the CPU or DMA to XBUF[n]] is used to pad the extra bits before shifting. This field only applies when XPAD = 2h. 0 Pad with bit 0 value. 1 Pad with bit 1 to bit 31 value from 1h to 1Fh.
7:4	XSSZ	R/W	0h	Transmit slot size. 0 Reserved. 1 Reserved. 2 Reserved. 3 Slot size is 8 bits. 4 Reserved. 5 Slot size is 12 bits. 6 Reserved. 7 Slot size is 16 bits. 8 Reserved. 9 Slot size is 20 bits. 10 Reserved. 11 Slot size is 24 bits. 12 Reserved. 13 Slot size is 28 bits. 14 Reserved. 15 Slot size is 32 bits.
3	XBUSEL	R/W	0h	Selects whether writes to serializer buffer XRBUF[n] originate from the configuration bus [CFG] or the data [DAT] port. 0 Writes to XRBUF[n] originate from the data port. Writes to XRBUF[n] from the configuration bus are ignored with no effect to the McASP. 1 Writes to XRBUF[n] originate from the configuration bus. Writes to XRBUF[n] from the data port are ignored with no effect to the McASP.
2:0	XROT	R/W	0h	Right-rotation value for transmit rotate right format unit. 0 Rotate right by 0 (no rotation). 1 Rotate right by 4 bit positions. 2 Rotate right by 8 bit positions. 3 Rotate right by 12 bit positions. 4 Rotate right by 16 bit positions. 5 Rotate right by 20 bit positions. 6 Rotate right by 24 bit positions. 7 Rotate right by 28 bit positions.

14.7.1.2.2.26 MCASP_AFSXCTL Register

14.7.1.2.2.26.1 MCASP_AFSXCTL Register (Offset = ACh) [reset = 0h]

The transmit frame sync control register (AFSXCTL) configures the transmit frame sync (AFSX).

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Table 14-10196. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00ACh
MCASP1	02B1 00ACh
MCASP2	02B2 00ACh
MCASP3	02B3 00ACh
MCASP4	02B4 00ACh

Figure 14-5042. MCASP_AFSXCTL Name Register

31	30	29	28	27	26	25	24
RESERVED100							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED100							
R							
0h							
15	14	13	12	11	10	9	8
XMOD							
R/W							
0h							
7	6	5	4	3	2	1	0
XMOD	RESERVED99		FXWID	RESERVED98		FSXM	FSXP
R/W	R		R/W	R		R/W	R/W
0h	0h		0h	0h		0h	0h

Table 14-10197. MCASP_AFSXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED100	R	0h	
15:7	XMOD	R/W	0h	Transmit frame sync mode select bits. 1FFh = Reserved from 181h to 1FFh. 0 Burst mode. 1 Reserved. 2 2-slot TDM (I2S mode) to 32-slot TDM from 2h to 20h. 33 Reserved from 21h to 17Fh. 384 384-slot DIT mode. 385 Reserved from 181h to 1FFh.
6:5	RESERVED99	R	0h	
4	FXWID	R/W	0h	Transmit frame sync width select bit indicates the width of the transmit frame sync [AFSX] during its active period. 0 Single bit. 1 Single word.
3:2	RESERVED98	R	0h	
1	FSXM	R/W	0h	Transmit frame sync generation select bit. 0 Externally-generated transmit frame sync. 1 Internally-generated transmit frame sync.

Table 14-10197. MCASP_AFSXCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FSXP	R/W	0h	Transmit frame sync polarity select bit. 0 `A rising edge on transmit frame sync (AFSX) indicates the beginning of a frame.` 1 `A falling edge on transmit frame sync (AFSX) indicates the beginning of a frame.`

14.7.1.2.2.27 MCASP_ACLKXCTL Register

14.7.1.2.2.27.1 MCASP_ACLKXCTL Register (Offset = B0h) [reset = 60h]

The transmit clock control register (ACLKXCTL) configures the transmit bit clock (ACLKX) and the transmit clock generator.

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Table 14-10198. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00B0h
MCASP1	02B1 00B0h
MCASP2	02B2 00B0h
MCASP3	02B3 00B0h
MCASP4	02B4 00B0h

Figure 14-5043. MCASP_ACLKXCTL Name Register

31	30	29	28	27	26	25	24
RESERVED102							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED102			BUSY	DIVBUSY	ADJBUSY	CLKXADJ	
R/W			R/W	R/W	R/W	W	
0h			0h	0h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED101							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKXP	ASYNC	CLKXM	CLKXDIV				
R/W	R/W	R/W	R/W				
0h	1h	1h	0h				

Table 14-10199. MCASP_ACLKXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED102	R/W	0h	
20	BUSY	R/W	0h	Status: logical OR of DIVBUSY, ADJBUSY
19	DIVBUSY	R/W	0h	Status: divide ratio change in progress
18	ADJBUSY	R/W	0h	Status: one-shot adjustment in progress
17:16	CLKXADJ	W	0h	CLKXDIV one-shot adjustment
15:8	RESERVED101	R/W	0h	
7	CLKXP	R/W	0h	Transmit bitstream clock polarity select bit. 0 Rising edge. External receiver samples data on the falling edge of the serial clock, so the transmitter must shift data out on the rising edge of the serial clock. 1 Falling edge. External receiver samples data on the rising edge of the serial clock, so the transmitter must shift data out on the falling edge of the serial clock.

Table 14-10199. MCASP_ACLKXCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ASYNC	R/W	1h	Transmit/receive operation asynchronous enable bit. 0 Synchronous. Transmit clock and frame sync provides the source for both the transmit and receive sections. 1 Asynchronous. Separate clock and frame sync used by transmit and receive sections.
5	CLKXM	R/W	1h	Transmit bit clock source bit. 0 External transmit clock source from ACLKX pin. 1 Internal transmit clock source from output of programmable bit clock divider.
4:0	CLKXDIV	R/W	0h	Transmit bit clock divide ratio bits determine the divide-down ratio from AHCLKX to ACLKX. 0 Divide-by-1. 1 Divide-by-2. 2 Divide-by-3 to divide-by-32 from 2h to 1Fh.

14.7.1.2.2.28 MCASP_AHCLKXCTL Register

14.7.1.2.2.28.1 MCASP_AHCLKXCTL Register (Offset = B4h) [reset = 8000h]

The transmit high-frequency clock control register (AHCLKXCTL) configures the transmit high-frequency controller clock (AHCLKX) and the transmit clock generator.

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Table 14-10200. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00B4h
MCASP1	02B1 00B4h
MCASP2	02B2 00B4h
MCASP3	02B3 00B4h
MCASP4	02B4 00B4h

Figure 14-5044. MCASP_AHCLKXCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED104</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED104</td><td>BUSY</td><td>DIVBUSY</td><td>ADJBUSY</td><td colspan="2">HCLKXADJ</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>HCLKXM</td><td>HCLKXP</td><td colspan="2">RESERVED103</td><td colspan="4">HCLKXDIV</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>0h</td><td colspan="2">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">HCLKXDIV</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10201. MCASP_AHCLKXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED104	R/W	0h	
20	BUSY	R/W	0h	Status: logical OR of DIVBUSY, ADJBUSY
19	DIVBUSY	R/W	0h	Status: divide ratio change in progress?
18	ADJBUSY	R/W	0h	Status: one-shot adjustment in progress?
17:16	HCLKXADJ	W	0h	HCLKXDIV one-shot adjustment
15	HCLKXM	R/W	1h	Transmit high-frequency clock source bit. 0 External transmit high-frequency clock source from AHCLKX pin. 1 Internal transmit high-frequency clock source from output of programmable high clock divider.

Table 14-10201. MCASP_AHCLKXCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	HCLKXP	R/W	0h	Transmit bitstream high-frequency clock polarity select bit. 0 AHCLKX is not inverted before programmable bit clock divider. In the special case where the transmit bit clock (ACLKX) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKXDIV = 0 in ACLKXCTL), AHCLKX is directly passed through to the ACLKX pin. 1 AHCLKX is inverted before programmable bit clock divider. In the special case where the transmit bit clock (ACLKX) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKXDIV = 0 in ACLKXCTL), AHCLKX is directly passed through to the ACLKX pin.
13:12	RESERVED103	R	0h	
11:0	HCLKXDIV	R/W	0h	Transmit high-frequency clock divide ratio bits determine the divide-down ratio from AUXCLK to AHCLKX. 0 Divide-by-1. 1 Divide-by-2. 2 Divide-by-3 to divide-by-4096 from 2h to FFFh.

14.7.1.2.2.29 MCASP_XTDM Register

14.7.1.2.2.29.1 MCASP_XTDM Register (Offset = B8h) [reset = 0h]

The transmit TDM time slot register (XTDM) specifies in which TDM time slot the transmitter is active. TDM time slot counter range is extended to 384 slots (to support SPDIF blocks of 384 subframes). XTDM operates modulo 32, that is, XTDMS specifies the TDM activity for time slots 0, 32, 64, 96, 128, and so on.

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Table 14-10202. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00B8h
MCASP1	02B1 00B8h
MCASP2	02B2 00B8h
MCASP3	02B3 00B8h
MCASP4	02B4 00B8h

Figure 14-5045. MCASP_XTDM Name Register

31	30	29	28	27	26	25	24
XTDMS							
R/W							
0h							
23	22	21	20	19	18	17	16
XTDMS							
R/W							
0h							
15	14	13	12	11	10	9	8
XTDMS							
R/W							
0h							
7	6	5	4	3	2	1	0
XTDMS							
R/W							
0h							

Table 14-10203. MCASP_XTDM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XTDMS	R/W	0h	Transmitter mode during TDM time slot n. 0 Transmit TDM time slot n is inactive. The transmit serializer does not shift out data during this slot. 1 Transmit TDM time slot n is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL).

14.7.1.2.2.30 MCASP_XINTCTL Register

14.7.1.2.2.30.1 MCASP_XINTCTL Register (Offset = BCh) [reset = 0h]

The transmitter interrupt control register (XINTCTL) controls generation of the McASP transmit interrupt (XINT). When the register bit(s) is set to 1, the occurrence of the enabled McASP condition(s) generates XINT. See the XSTAT register for a description of the interrupt conditions.

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Table 14-10204. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00BCh
MCASP1	02B1 00BCh
MCASP2	02B2 00BCh
MCASP3	02B3 00BCh
MCASP4	02B4 00BCh

Figure 14-5046. MCASP_XINTCTL Name Register

31	30	29	28	27	26	25	24
RESERVED106							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED106							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED106							
R							
0h							
7	6	5	4	3	2	1	0
XSTAFRM	RESERVED105	XDATA	XLAST	XDMAERR	XCKFAIL	XSYNCERR	XUNDRN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10205. MCASP_XINTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED106	R	0h	
7	XSTAFRM	R/W	0h	Transmit start of frame interrupt enable bit. 0 Interrupt is disabled. A transmit start of frame interrupt does not generate a McASP transmit interrupt (XINT). 1 Interrupt is enabled. A transmit start of frame interrupt generates a McASP transmit interrupt (XINT).
6	RESERVED105	R	0h	
5	XDATA	R/W	0h	Transmit data ready interrupt enable bit. 0 Interrupt is disabled. A transmit data ready interrupt does not generate a McASP transmit interrupt (XINT). 1 Interrupt is enabled. A transmit data ready interrupt generates a McASP transmit interrupt (XINT).

Table 14-10205. MCASP_XINTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XLAST	R/W	0h	Transmit last slot interrupt enable bit. 0 `Interrupt is disabled. A transmit last slot interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmit last slot interrupt generates a McASP transmit interrupt (XINT).`
3	XDMAERR	R/W	0h	Transmit DMA error interrupt enable bit. 0 `Interrupt is disabled. A transmit DMA error interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmit DMA error interrupt generates a McASP transmit interrupt (XINT).`
2	XCKFAIL	R/W	0h	Transmit clock failure interrupt enable bit. 0 `Interrupt is disabled. A transmit clock failure interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmit clock failure interrupt generates a McASP transmit interrupt (XINT).`
1	XSYNCERR	R/W	0h	Unexpected transmit frame sync interrupt enable bit. 0 `Interrupt is disabled. An unexpected transmit frame sync interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. An unexpected transmit frame sync interrupt generates a McASP transmit interrupt (XINT).`
0	XUNDRN	R/W	0h	Transmitter underrun interrupt enable bit. 0 `Interrupt is disabled. A transmitter underrun interrupt does not generate a McASP transmit interrupt (XINT).` 1 `Interrupt is enabled. A transmitter underrun interrupt generates a McASP transmit interrupt (XINT).`

14.7.1.2.2.31 MCASP_XSTAT Register

14.7.1.2.2.31.1 MCASP_XSTAT Register (Offset = C0h) [reset = 0h]

The transmitter status register (XSTAT) provides the transmitter status and transmit TDM time slot number. If the McASP logic attempts to set an interrupt flag in the same cycle that the CPU writes to the flag to clear it, the McASP logic has priority and the flag remains set. This also causes a new interrupt request to be generated.

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Table 14-10206. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00C0h
MCASP1	02B1 00C0h
MCASP2	02B2 00C0h
MCASP3	02B3 00C0h
MCASP4	02B4 00C0h

Figure 14-5047. MCASP_XSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED107							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED107							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED107							XERR
R							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XDMAERR	XSTAFRM	XDATA	XLAST	XTDMSLOT	XCKFAIL	XSYNCERR	XUNDRN
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10207. MCASP_XSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED107	R	0h	

8	XERR	R/W	0h	XERR bit always returns a logic-OR of: XUNDRN OR XSYNCERR OR XCKFAIL OR XDMAERR. Allows a single bit to be checked to determine if a transmitter error interrupt has occurred.
				`0 No errors have occurred.`
				`1 An error has occurred.`

7	XDMAERR	R/W1TC	0h	Transmit DMA error flag. XDMAERR is set when the CPU or DMA writes more serializers through the data port in a given time slot than were programmed as transmitters. Causes a transmit interrupt [XINT], if this bit is set and XDMAERR in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect.
				`0 Transmit DMA error did not occur.`
				`1 Transmit DMA error did occur.`

Table 14-10207. MCASP_XSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	XSTAFRM	R/W1TC	0h	Transmit start of frame flag. Causes a transmit interrupt [XINT], if this bit is set and XSTAFRM in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 No new transmit frame sync (AFSX) is detected. 1 A new transmit frame sync (AFSX) is detected.
5	XDATA	R/W1TC	0h	Transmit data ready flag. Causes a transmit interrupt [XINT], if this bit is set and XDATA in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 XBUF is written and is full. 1 Data is copied from XBUF to XRSR. XBUF is empty and ready to be written. XDATA is also set when the transmit serializers are taken out of reset. When XDATA is set, it always causes a DMA event (AXEVT).
4	XLAST	R/W1TC	0h	Transmit last slot flag. XLAST is set along with XDATA, if the current slot is the last slot in a frame. Causes a transmit interrupt [XINT], if this bit is set and XLAST in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 Current slot is not the last slot in a frame. 1 Current slot is the last slot in a frame. XDATA is also set.
3	XTDMSLOT	R	0h	Returns the LSB of XSLOT. Allows a single read of XSTAT to determine whether the current TDM time slot is even or odd. 0 Current TDM time slot is odd. 1 Current TDM time slot is even.
2	XCKFAIL	R/W1TC	0h	Transmit clock failure flag. XCKFAIL is set when the transmit clock failure detection circuit reports an error. Causes a transmit interrupt [XINT], if this bit is set and XCKFAIL in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 Transmit clock failure did not occur. 1 Transmit clock failure did occur.
1	XSYNCERR	R/W1TC	0h	Unexpected transmit frame sync flag. XSYNCERR is set when a new transmit frame sync [AFSX] occurs before it is expected. Causes a transmit interrupt [XINT], if this bit is set and XSYNCERR in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 Unexpected transmit frame sync did not occur. 1 Unexpected transmit frame sync did occur.
0	XUNDRN	R/W1TC	0h	Transmitter underrun flag. XUNDRN is set when the transmit serializer is instructed to transfer data from XBUF to XRSR, but XBUF has not yet been serviced with new data since the last transfer. Causes a transmit interrupt [XINT], if this bit is set and XUNDRN in XINTCTL is set. This bit is cleared by Writing a 1 to this bit. Writing a 0 has no effect. 0 Transmitter underrun did not occur. 1 Transmitter underrun did occur. For details on McASP action upon underrun conditions, see Buffer Underrun Error - Transmitter.

14.7.1.2.2.32 MCASP_XSLOT Register

14.7.1.2.2.32.1 MCASP_XSLOT Register (Offset = C4h) [reset = 17Fh]

The current transmit TDM time slot register (XSLOT) indicates the current time slot for the transmit data frame.

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Table 14-10208. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00C4h
MCASP1	02B1 00C4h
MCASP2	02B2 00C4h
MCASP3	02B3 00C4h
MCASP4	02B4 00C4h

Figure 14-5048. MCASP_XSLOT Name Register

31	30	29	28	27	26	25	24
RESERVED108							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED108							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED108						XSLOTCNT	
R						R	
0h						17Fh	
7	6	5	4	3	2	1	0
XSLOTCNT							
R							
17Fh							

Table 14-10209. MCASP_XSLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED108	R	0h	
9:0	XSLOTCNT	R	17Fh	Current transmit time slot count. Legal values: 0 to 383 [17Fh]. During reset, this counter value is 383 so the next count value, which is used to encode the first DIT group of data, will be 0 and encodes the B preamble. TDM function is not supported for >32 time slots. However, TDM time slot counter may count to 383 when used to transmit a DIT block.

14.7.1.2.2.33 MCASP_XCLKCHK Register

14.7.1.2.2.33.1 MCASP_XCLKCHK Register (Offset = C8h) [reset = 0h]

The transmit clock check control register (XCLKCHK) configures the transmit clock failure detection circuit.

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Table 14-10210. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00C8h
MCASP1	02B1 00C8h
MCASP2	02B2 00C8h
MCASP3	02B3 00C8h
MCASP4	02B4 00C8h

Figure 14-5049. MCASP_XCLKCHK Name Register

31	30	29	28	27	26	25	24
XCNT							
R							
0h							
23	22	21	20	19	18	17	16
XMAX							
R/W							
0h							
15	14	13	12	11	10	9	8
XMIN							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED109				XPS			
R				R/W			
0h				0h			

Table 14-10211. MCASP_XCLKCHK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	XCNT	R	0h	Transmit clock count value [from previous measurement]. The clock circuit continually counts the number of system clocks for every 32 transmit high-frequency controller clock [AHCLKX] signals, and stores the count in XCNT until the next measurement is taken.
23:16	XMAX	R/W	0h	Transmit clock maximum boundary. This 8 bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 transmit high-frequency controller clock [AHCLKX] signals have been received. If the current counter value is greater than XMAX after counting 32 AHCLKX signals, XCKFAIL in XSTAT is set. The comparison is performed using unsigned arithmetic.
15:8	XMIN	R/W	0h	Transmit clock minimum boundary. This 8 bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 transmit high-frequency controller clock [AHCLKX] signals have been received. If XCNT is less than XMIN after counting 32 AHCLKX signals, XCKFAIL in XSTAT is set. The comparison is performed using unsigned arithmetic.
7:4	RESERVED109	R	0h	

Table 14-10211. MCASP_XCLKCHK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	XPS	R/W	0h	Transmit clock check prescaler value. Fh = Reserved from 9h to Fh. 0 `MCASP system clock divided by 1.` 1 `MCASP system clock divided by 2.` 2 `MCASP system clock divided by 4.` 3 `MCASP system clock divided by 8.` 4 `MCASP system clock divided by 16.` 5 `MCASP system clock divided by 32.` 6 `MCASP system clock divided by 64.` 7 `MCASP system clock divided by 128.` 8 `MCASP system clock divided by 256.` 9 `Reserved from 9h to Fh.`

14.7.1.2.2.34 MCASP_XEVTCTL Register

14.7.1.2.2.34.1 MCASP_XEVTCTL Register (Offset = CCh) [reset = 0h]

The transmitter DMA event control register (XEVTCTL) contains a disable bit for the transmit DMA event. Note for device-specific registers: Accessing XEVTCTL not implemented on a specific device may cause improper device operation.

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Table 14-10212. Instance Table

Instance Name	Physical Address
MCASP0	02B0 00CCh
MCASP1	02B1 00CCh
MCASP2	02B2 00CCh
MCASP3	02B3 00CCh
MCASP4	02B4 00CCh

Figure 14-5050. MCASP_XEVTCTL Name Register

31	30	29	28	27	26	25	24
RESERVED110							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED110							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED110							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED110							XDATDMA
R							R/W
0h							0h

Table 14-10213. MCASP_XEVTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED110	R	0h	
0	XDATDMA	R/W	0h	Transmit data DMA request enable bit. If Writing to this bit, always write the default value of 0. 0 Transmit data DMA request is enabled. 1 Reserved

14.7.1.2.2.35 MCASP_DITCSRA0 Register

14.7.1.2.2.35.1 MCASP_DITCSRA0 Register (Offset = 100h) [reset = 0h]

The DIT left channel status registers (DITCSRA0) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10214. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0100h
MCASP1	02B1 0100h
MCASP2	02B2 0100h
MCASP3	02B3 0100h
MCASP4	02B4 0100h

Figure 14-5051. MCASP_DITCSRA0 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-10215. MCASP_DITCSRA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.7.1.2.2.36 MCASP_DITCSRA1 Register

14.7.1.2.2.36.1 MCASP_DITCSRA1 Register (Offset = 104h) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10216. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0104h
MCASP1	02B1 0104h
MCASP2	02B2 0104h
MCASP3	02B3 0104h
MCASP4	02B4 0104h

Figure 14-5052. MCASP_DITCSRA1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DITCSRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DITCSRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DITCSRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DITCSRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10217. MCASP_DITCSRA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.7.1.2.2.37 MCASP_DITCSRA2 Register

14.7.1.2.2.37.1 MCASP_DITCSRA2 Register (Offset = 108h) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10218. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0108h
MCASP1	02B1 0108h
MCASP2	02B2 0108h
MCASP3	02B3 0108h
MCASP4	02B4 0108h

Figure 14-5053. MCASP_DITCSRA2 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-10219. MCASP_DITCSRA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.7.1.2.2.38 MCASP_DITCSRA3 Register

14.7.1.2.2.38.1 MCASP_DITCSRA3 Register (Offset = 10Ch) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10220. Instance Table

Instance Name	Physical Address
MCASP0	02B0 010Ch
MCASP1	02B1 010Ch
MCASP2	02B2 010Ch
MCASP3	02B3 010Ch
MCASP4	02B4 010Ch

Figure 14-5054. MCASP_DITCSRA3 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-10221. MCASP_DITCSRA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.7.1.2.2.39 MCASP_DITCSRA4 Register

14.7.1.2.2.39.1 MCASP_DITCSRA4 Register (Offset = 110h) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10222. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0110h
MCASP1	02B1 0110h
MCASP2	02B2 0110h
MCASP3	02B3 0110h
MCASP4	02B4 0110h

Figure 14-5055. MCASP_DITCSRA4 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-10223. MCASP_DITCSRA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.7.1.2.2.40 MCASP_DITCSRA5 Register

14.7.1.2.2.40.1 MCASP_DITCSRA5 Register (Offset = 114h) [reset = 0h]

The DIT left channel status registers (DITCSRA) provide the status of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10224. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0114h
MCASP1	02B1 0114h
MCASP2	02B2 0114h
MCASP3	02B3 0114h
MCASP4	02B4 0114h

Figure 14-5056. MCASP_DITCSRA5 Name Register

31	30	29	28	27	26	25	24
DITCSRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRA							
R/W							
0h							

Table 14-10225. MCASP_DITCSRA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRA	R/W	0h	DIT left channel status registers.

14.7.1.2.2.41 MCASP_DITCSRB0 Register

14.7.1.2.2.41.1 MCASP_DITCSRB0 Register (Offset = 118h) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10226. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0118h
MCASP1	02B1 0118h
MCASP2	02B2 0118h
MCASP3	02B3 0118h
MCASP4	02B4 0118h

Figure 14-5057. MCASP_DITCSRB0 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-10227. MCASP_DITCSRB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.7.1.2.2.42 MCASP_DITCSRB1 Register

14.7.1.2.2.42.1 MCASP_DITCSRB1 Register (Offset = 11Ch) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10228. Instance Table

Instance Name	Physical Address
MCASP0	02B0 011Ch
MCASP1	02B1 011Ch
MCASP2	02B2 011Ch
MCASP3	02B3 011Ch
MCASP4	02B4 011Ch

Figure 14-5058. MCASP_DITCSRB1 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-10229. MCASP_DITCSRB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.7.1.2.2.43 MCASP_DITCSRB2 Register

14.7.1.2.2.43.1 MCASP_DITCSRB2 Register (Offset = 120h) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10230. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0120h
MCASP1	02B1 0120h
MCASP2	02B2 0120h
MCASP3	02B3 0120h
MCASP4	02B4 0120h

Figure 14-5059. MCASP_DITCSRB2 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-10231. MCASP_DITCSRB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.7.1.2.2.44 MCASP_DITCSRB3 Register

14.7.1.2.2.44.1 MCASP_DITCSRB3 Register (Offset = 124h) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10232. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0124h
MCASP1	02B1 0124h
MCASP2	02B2 0124h
MCASP3	02B3 0124h
MCASP4	02B4 0124h

Figure 14-5060. MCASP_DITCSRB3 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-10233. MCASP_DITCSRB3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.7.1.2.2.45 MCASP_DITCSRB4 Register

14.7.1.2.2.45.1 MCASP_DITCSRB4 Register (Offset = 128h) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10234. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0128h
MCASP1	02B1 0128h
MCASP2	02B2 0128h
MCASP3	02B3 0128h
MCASP4	02B4 0128h

Figure 14-5061. MCASP_DITCSRB4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DITCSRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DITCSRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DITCSRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DITCSRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10235. MCASP_DITCSRB4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.7.1.2.2.46 MCASP_DITCSRB5 Register

14.7.1.2.2.46.1 MCASP_DITCSRB5 Register (Offset = 12Ch) [reset = 0h]

The DIT right channel status registers (DITCSRB0) provide the status of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register file in time, if a different set of data need to be sent.

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Table 14-10236. Instance Table

Instance Name	Physical Address
MCASP0	02B0 012Ch
MCASP1	02B1 012Ch
MCASP2	02B2 012Ch
MCASP3	02B3 012Ch
MCASP4	02B4 012Ch

Figure 14-5062. MCASP_DITCSRB5 Name Register

31	30	29	28	27	26	25	24
DITCSRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITCSRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITCSRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITCSRB							
R/W							
0h							

Table 14-10237. MCASP_DITCSRB5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITCSRB	R/W	0h	DIT right channel status registers.

14.7.1.2.2.47 MCASP_DITUDRA0 Register

14.7.1.2.2.47.1 MCASP_DITUDRA0 Register (Offset = 130h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10238. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0130h
MCASP1	02B1 0130h
MCASP2	02B2 0130h
MCASP3	02B3 0130h
MCASP4	02B4 0130h

Figure 14-5063. MCASP_DITUDRA0 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-10239. MCASP_DITUDRA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.7.1.2.2.48 MCASP_DITUDRA1 Register

14.7.1.2.2.48.1 MCASP_DITUDRA1 Register (Offset = 134h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10240. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0134h
MCASP1	02B1 0134h
MCASP2	02B2 0134h
MCASP3	02B3 0134h
MCASP4	02B4 0134h

Figure 14-5064. MCASP_DITUDRA1 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-10241. MCASP_DITUDRA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.7.1.2.2.49 MCASP_DITUDRA2 Register

14.7.1.2.2.49.1 MCASP_DITUDRA2 Register (Offset = 138h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10242. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0138h
MCASP1	02B1 0138h
MCASP2	02B2 0138h
MCASP3	02B3 0138h
MCASP4	02B4 0138h

Figure 14-5065. MCASP_DITUDRA2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DITUDRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DITUDRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DITUDRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DITUDRA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10243. MCASP_DITUDRA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.7.1.2.2.50 MCASP_DITUDRA3 Register

14.7.1.2.2.50.1 MCASP_DITUDRA3 Register (Offset = 13Ch) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10244. Instance Table

Instance Name	Physical Address
MCASP0	02B0 013Ch
MCASP1	02B1 013Ch
MCASP2	02B2 013Ch
MCASP3	02B3 013Ch
MCASP4	02B4 013Ch

Figure 14-5066. MCASP_DITUDRA3 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-10245. MCASP_DITUDRA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.7.1.2.2.51 MCASP_DITUDRA4 Register

14.7.1.2.2.51.1 MCASP_DITUDRA4 Register (Offset = 140h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10246. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0140h
MCASP1	02B1 0140h
MCASP2	02B2 0140h
MCASP3	02B3 0140h
MCASP4	02B4 0140h

Figure 14-5067. MCASP_DITUDRA4 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-10247. MCASP_DITUDRA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.7.1.2.2.52 MCASP_DITUDRA5 Register

14.7.1.2.2.52.1 MCASP_DITUDRA5 Register (Offset = 144h) [reset = 0h]

The DIT left channel user data registers (DITUDRA0) provides the user data of each left channel (even TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10248. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0144h
MCASP1	02B1 0144h
MCASP2	02B2 0144h
MCASP3	02B3 0144h
MCASP4	02B4 0144h

Figure 14-5068. MCASP_DITUDRA5 Name Register

31	30	29	28	27	26	25	24
DITUDRA							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRA							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRA							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRA							
R/W							
0h							

Table 14-10249. MCASP_DITUDRA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRA	R/W	0h	DIT left channel user data registers.

14.7.1.2.2.53 MCASP_DITUDRB0 Register

14.7.1.2.2.53.1 MCASP_DITUDRB0 Register (Offset = 148h) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10250. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0148h
MCASP1	02B1 0148h
MCASP2	02B2 0148h
MCASP3	02B3 0148h
MCASP4	02B4 0148h

Figure 14-5069. MCASP_DITUDRB0 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-10251. MCASP_DITUDRB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.7.1.2.2.54 MCASP_DITUDRB1 Register

14.7.1.2.2.54.1 MCASP_DITUDRB1 Register (Offset = 14Ch) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10252. Instance Table

Instance Name	Physical Address
MCASP0	02B0 014Ch
MCASP1	02B1 014Ch
MCASP2	02B2 014Ch
MCASP3	02B3 014Ch
MCASP4	02B4 014Ch

Figure 14-5070. MCASP_DITUDRB1 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-10253. MCASP_DITUDRB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.7.1.2.2.55 MCASP_DITUDRB2 Register

14.7.1.2.2.55.1 MCASP_DITUDRB2 Register (Offset = 150h) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10254. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0150h
MCASP1	02B1 0150h
MCASP2	02B2 0150h
MCASP3	02B3 0150h
MCASP4	02B4 0150h

Figure 14-5071. MCASP_DITUDRB2 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-10255. MCASP_DITUDRB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.7.1.2.2.56 MCASP_DITUDRB3 Register

14.7.1.2.2.56.1 MCASP_DITUDRB3 Register (Offset = 154h) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10256. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0154h
MCASP1	02B1 0154h
MCASP2	02B2 0154h
MCASP3	02B3 0154h
MCASP4	02B4 0154h

Figure 14-5072. MCASP_DITUDRB3 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-10257. MCASP_DITUDRB3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.7.1.2.2.57 MCASP_DITUDRB4 Register

14.7.1.2.2.57.1 MCASP_DITUDRB4 Register (Offset = 158h) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10258. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0158h
MCASP1	02B1 0158h
MCASP2	02B2 0158h
MCASP3	02B3 0158h
MCASP4	02B4 0158h

Figure 14-5073. MCASP_DITUDRB4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DITUDRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DITUDRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DITUDRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DITUDRB</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10259. MCASP_DITUDRB4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.7.1.2.2.58 MCASP_DITUDRB5 Register

14.7.1.2.2.58.1 MCASP_DITUDRB5 Register (Offset = 15Ch) [reset = 0h]

The DIT right channel user data registers (DITUDRB0) provides the user data of each right channel (odd TDM time slot). Each of the six 32-bit registers can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. It is your responsibility to update the register in time, if a different set of data need to be sent.

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Table 14-10260. Instance Table

Instance Name	Physical Address
MCASP0	02B0 015Ch
MCASP1	02B1 015Ch
MCASP2	02B2 015Ch
MCASP3	02B3 015Ch
MCASP4	02B4 015Ch

Figure 14-5074. MCASP_DITUDRB5 Name Register

31	30	29	28	27	26	25	24
DITUDRB							
R/W							
0h							
23	22	21	20	19	18	17	16
DITUDRB							
R/W							
0h							
15	14	13	12	11	10	9	8
DITUDRB							
R/W							
0h							
7	6	5	4	3	2	1	0
DITUDRB							
R/W							
0h							

Table 14-10261. MCASP_DITUDRB5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DITUDRB	R/W	0h	DIT right channel user data registers.

14.7.1.2.2.59 MCASP_SRCTL0 Register

14.7.1.2.2.59.1 MCASP_SRCTL0 Register (Offset = 180h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10262. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0180h
MCASP1	02B1 0180h
MCASP2	02B2 0180h
MCASP3	02B3 0180h
MCASP4	02B4 0180h

Figure 14-5075. MCASP_SRCTL0 Name Register

31	30	29	28	27	26	25	24
RESERVED111							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED111							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED111							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED111		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10263. MCASP_SRCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED111	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10263. MCASP_SRCTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.60 MCASP_SRCTL1 Register

14.7.1.2.2.60.1 MCASP_SRCTL1 Register (Offset = 184h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10264. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0184h
MCASP1	02B1 0184h
MCASP2	02B2 0184h
MCASP3	02B3 0184h
MCASP4	02B4 0184h

Figure 14-5076. MCASP_SRCTL1 Name Register

31	30	29	28	27	26	25	24
RESERVED112							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED112							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED112							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED112		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10265. MCASP_SRCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED112	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10265. MCASP_SRCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.7.1.2.2.61 MCASP_SRCTL2 Register

14.7.1.2.2.61.1 MCASP_SRCTL2 Register (Offset = 188h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10266. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0188h
MCASP1	02B1 0188h
MCASP2	02B2 0188h
MCASP3	02B3 0188h
MCASP4	02B4 0188h

Figure 14-5077. MCASP_SRCTL2 Name Register

31	30	29	28	27	26	25	24
RESERVED113							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED113							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED113							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED113		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10267. MCASP_SRCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED113	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10267. MCASP_SRCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.62 MCASP_SRCTL3 Register

14.7.1.2.2.62.1 MCASP_SRCTL3 Register (Offset = 18Ch) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10268. Instance Table

Instance Name	Physical Address
MCASP0	02B0 018Ch
MCASP1	02B1 018Ch
MCASP2	02B2 018Ch
MCASP3	02B3 018Ch
MCASP4	02B4 018Ch

Figure 14-5078. MCASP_SRCTL3 Name Register

31	30	29	28	27	26	25	24
RESERVED114							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED114							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED114							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED114		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10269. MCASP_SRCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED114	R	0h	

5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF.
				`0 Receive buffer (RBUF) is empty.`
				`1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-10269. MCASP_SRCTL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.63 MCASP_SRCTL4 Register

14.7.1.2.2.63.1 MCASP_SRCTL4 Register (Offset = 190h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10270. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0190h
MCASP1	02B1 0190h
MCASP2	02B2 0190h
MCASP3	02B3 0190h
MCASP4	02B4 0190h

Figure 14-5079. MCASP_SRCTL4 Name Register

31	30	29	28	27	26	25	24
RESERVED115							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED115							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED115							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED115		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10271. MCASP_SRCTL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED115	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10271. MCASP_SRCTL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.64 MCASP_SRCTL5 Register

14.7.1.2.2.64.1 MCASP_SRCTL5 Register (Offset = 194h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10272. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0194h
MCASP1	02B1 0194h
MCASP2	02B2 0194h
MCASP3	02B3 0194h
MCASP4	02B4 0194h

Figure 14-5080. MCASP_SRCTL5 Name Register

31	30	29	28	27	26	25	24
RESERVED116							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED116							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED116							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED116		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10273. MCASP_SRCTL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED116	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10273. MCASP_SRCTL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.65 MCASP_SRCTL6 Register

14.7.1.2.2.65.1 MCASP_SRCTL6 Register (Offset = 198h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10274. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0198h
MCASP1	02B1 0198h
MCASP2	02B2 0198h
MCASP3	02B3 0198h
MCASP4	02B4 0198h

Figure 14-5081. MCASP_SRCTL6 Name Register

31	30	29	28	27	26	25	24
RESERVED117							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED117							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED117							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED117		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10275. MCASP_SRCTL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED117	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10275. MCASP_SRCTL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.66 MCASP_SRCTL7 Register

14.7.1.2.2.66.1 MCASP_SRCTL7 Register (Offset = 19Ch) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10276. Instance Table

Instance Name	Physical Address
MCASP0	02B0 019Ch
MCASP1	02B1 019Ch
MCASP2	02B2 019Ch
MCASP3	02B3 019Ch
MCASP4	02B4 019Ch

Figure 14-5082. MCASP_SRCTL7 Name Register

31	30	29	28	27	26	25	24
RESERVED118							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED118							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED118							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED118		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10277. MCASP_SRCTL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED118	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 `Receive buffer (RBUF) is empty.` 1 `Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-10277. MCASP_SRCTL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.7.1.2.2.67 MCASP_SRCTL8 Register

14.7.1.2.2.67.1 MCASP_SRCTL8 Register (Offset = 1A0h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10278. Instance Table

Instance Name	Physical Address
MCASP0	02B0 01A0h
MCASP1	02B1 01A0h
MCASP2	02B2 01A0h
MCASP3	02B3 01A0h
MCASP4	02B4 01A0h

Figure 14-5083. MCASP_SRCTL8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED119</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED119</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED119</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED119</td><td>RRDY</td><td>XRDY</td><td colspan="2">DISMOD</td><td colspan="2">SRMOD</td></tr>
<tr><td colspan="2">R</td><td>R</td><td>R</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-10279. MCASP_SRCTL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED119	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10279. MCASP_SRCTL8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.68 MCASP_SRCTL9 Register

14.7.1.2.2.68.1 MCASP_SRCTL9 Register (Offset = 1A4h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10280. Instance Table

Instance Name	Physical Address
MCASP0	02B0 01A4h
MCASP1	02B1 01A4h
MCASP2	02B2 01A4h
MCASP3	02B3 01A4h
MCASP4	02B4 01A4h

Figure 14-5084. MCASP_SRCTL9 Name Register

31	30	29	28	27	26	25	24
RESERVED120							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED120							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED120							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED120		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10281. MCASP_SRCTL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED120	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10281. MCASP_SRCTL9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.69 MCASP_SRCTL10 Register

14.7.1.2.2.69.1 MCASP_SRCTL10 Register (Offset = 1A8h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10282. Instance Table

Instance Name	Physical Address
MCASP0	02B0 01A8h
MCASP1	02B1 01A8h
MCASP2	02B2 01A8h
MCASP3	02B3 01A8h
MCASP4	02B4 01A8h

Figure 14-5085. MCASP_SRCTL10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED121</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED121</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED121</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED121</td><td>RRDY</td><td>XRDY</td><td colspan="2">DISMOD</td><td colspan="2">SRMOD</td></tr>
<tr><td colspan="2">R</td><td>R</td><td>R</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-10283. MCASP_SRCTL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED121	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10283. MCASP_SRCTL10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.7.1.2.2.70 MCASP_SRCTL11 Register

14.7.1.2.2.70.1 MCASP_SRCTL11 Register (Offset = 1ACh) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10284. Instance Table

Instance Name	Physical Address
MCASP0	02B0 01ACh
MCASP1	02B1 01ACh
MCASP2	02B2 01ACh
MCASP3	02B3 01ACh
MCASP4	02B4 01ACh

Figure 14-5086. MCASP_SRCTL11 Name Register

31	30	29	28	27	26	25	24
RESERVED122							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED122							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED122							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED122		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10285. MCASP_SRCTL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED122	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10285. MCASP_SRCTL11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.71 MCASP_SRCTL12 Register

14.7.1.2.2.71.1 MCASP_SRCTL12 Register (Offset = 1B0h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10286. Instance Table

Instance Name	Physical Address
MCASP0	02B0 01B0h
MCASP1	02B1 01B0h
MCASP2	02B2 01B0h
MCASP3	02B3 01B0h
MCASP4	02B4 01B0h

Figure 14-5087. MCASP_SRCTL12 Name Register

31	30	29	28	27	26	25	24
RESERVED123							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED123							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED123							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED123		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10287. MCASP_SRCTL12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED123	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 `Receive buffer (RBUF) is empty.` 1 `Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-10287. MCASP_SRCTL12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.72 MCASP_SRCTL13 Register

14.7.1.2.2.72.1 MCASP_SRCTL13 Register (Offset = 1B4h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10288. Instance Table

Instance Name	Physical Address
MCASP0	02B0 01B4h
MCASP1	02B1 01B4h
MCASP2	02B2 01B4h
MCASP3	02B3 01B4h
MCASP4	02B4 01B4h

Figure 14-5088. MCASP_SRCTL13 Name Register

31	30	29	28	27	26	25	24
RESERVED124							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED124							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED124							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED124		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10289. MCASP_SRCTL13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED124	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10289. MCASP_SRCTL13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.7.1.2.2.73 MCASP_SRCTL14 Register

14.7.1.2.2.73.1 MCASP_SRCTL14 Register (Offset = 1B8h) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10290. Instance Table

Instance Name	Physical Address
MCASP0	02B0 01B8h
MCASP1	02B1 01B8h
MCASP2	02B2 01B8h
MCASP3	02B3 01B8h
MCASP4	02B4 01B8h

Figure 14-5089. MCASP_SRCTL14 Name Register

31	30	29	28	27	26	25	24
RESERVED125							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED125							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED125							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED125		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10291. MCASP_SRCTL14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED125	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 Receive buffer (RBUF) is empty. 1 Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.

Table 14-10291. MCASP_SRCTL14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 Transmit buffer (XBUF) contains data. 1 Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 Drive on pin is 3-state. 1 Reserved. 2 Drive on pin is logic low. 3 Drive on pin is logic high.
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 Serializer is inactive. 1 Serializer is transmitter. 2 Serializer is receiver. 3 Reserved.

14.7.1.2.2.74 MCASP_SRCTL15 Register

14.7.1.2.2.74.1 MCASP_SRCTL15 Register (Offset = 1BCh) [reset = 0h]

Each serializer on the McASP has a serializer control register (SRCTL0). There are up to 16 serializers per McASP. Note for device-specific registers: Accessing SRCTL0n not implemented on a specific device may cause improper device operation.

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Table 14-10292. Instance Table

Instance Name	Physical Address
MCASP0	02B0 01BCh
MCASP1	02B1 01BCh
MCASP2	02B2 01BCh
MCASP3	02B3 01BCh
MCASP4	02B4 01BCh

Figure 14-5090. MCASP_SRCTL15 Name Register

31	30	29	28	27	26	25	24
RESERVED126							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED126							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED126							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED126		RRDY	XRDY	DISMOD		SRMOD	
R		R	R	R/W		R/W	
0h		0h	0h	0h		0h	

Table 14-10293. MCASP_SRCTL15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED126	R	0h	
5	RRDY	R	0h	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0 `Receive buffer (RBUF) is empty.` 1 `Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.`

Table 14-10293. MCASP_SRCTL15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R	0h	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0 `Transmit buffer (XBUF) contains data.` 1 `Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.`
3:2	DISMOD	R/W	0h	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a McASP pin [PFUNC = 0]. 0 `Drive on pin is 3-state.` 1 `Reserved.` 2 `Drive on pin is logic low.` 3 `Drive on pin is logic high.`
1:0	SRMOD	R/W	0h	Serializer mode bit. 0 `Serializer is inactive.` 1 `Serializer is transmitter.` 2 `Serializer is receiver.` 3 `Reserved.`

14.7.1.2.2.75 MCASP_XBUF0 Register

14.7.1.2.2.75.1 MCASP_XBUF0 Register (Offset = 200h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10294. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0200h
MCASP1	02B1 0200h
MCASP2	02B2 0200h
MCASP3	02B3 0200h
MCASP4	02B4 0200h

Figure 14-5091. MCASP_XBUF0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">XBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">XBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">XBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">XBUF</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10295. MCASP_XBUF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.76 MCASP_XBUF1 Register

14.7.1.2.2.76.1 MCASP_XBUF1 Register (Offset = 204h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10296. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0204h
MCASP1	02B1 0204h
MCASP2	02B2 0204h
MCASP3	02B3 0204h
MCASP4	02B4 0204h

Figure 14-5092. MCASP_XBUF1 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10297. MCASP_XBUF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.77 MCASP_XBUF2 Register

14.7.1.2.2.77.1 MCASP_XBUF2 Register (Offset = 208h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10298. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0208h
MCASP1	02B1 0208h
MCASP2	02B2 0208h
MCASP3	02B3 0208h
MCASP4	02B4 0208h

Figure 14-5093. MCASP_XBUF2 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10299. MCASP_XBUF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.78 MCASP_XBUF3 Register

14.7.1.2.2.78.1 MCASP_XBUF3 Register (Offset = 20Ch) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10300. Instance Table

Instance Name	Physical Address
MCASP0	02B0 020Ch
MCASP1	02B1 020Ch
MCASP2	02B2 020Ch
MCASP3	02B3 020Ch
MCASP4	02B4 020Ch

Figure 14-5094. MCASP_XBUF3 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10301. MCASP_XBUF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.79 MCASP_XBUF4 Register

14.7.1.2.2.79.1 MCASP_XBUF4 Register (Offset = 210h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10302. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0210h
MCASP1	02B1 0210h
MCASP2	02B2 0210h
MCASP3	02B3 0210h
MCASP4	02B4 0210h

Figure 14-5095. MCASP_XBUF4 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10303. MCASP_XBUF4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.80 MCASP_XBUF5 Register

14.7.1.2.2.80.1 MCASP_XBUF5 Register (Offset = 214h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10304. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0214h
MCASP1	02B1 0214h
MCASP2	02B2 0214h
MCASP3	02B3 0214h
MCASP4	02B4 0214h

Figure 14-5096. MCASP_XBUF5 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10305. MCASP_XBUF5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.81 MCASP_XBUF6 Register

14.7.1.2.2.81.1 MCASP_XBUF6 Register (Offset = 218h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10306. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0218h
MCASP1	02B1 0218h
MCASP2	02B2 0218h
MCASP3	02B3 0218h
MCASP4	02B4 0218h

Figure 14-5097. MCASP_XBUF6 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10307. MCASP_XBUF6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.82 MCASP_XBUF7 Register

14.7.1.2.2.82.1 MCASP_XBUF7 Register (Offset = 21Ch) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10308. Instance Table

Instance Name	Physical Address
MCASP0	02B0 021Ch
MCASP1	02B1 021Ch
MCASP2	02B2 021Ch
MCASP3	02B3 021Ch
MCASP4	02B4 021Ch

Figure 14-5098. MCASP_XBUF7 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10309. MCASP_XBUF7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.83 MCASP_XBUF8 Register

14.7.1.2.2.83.1 MCASP_XBUF8 Register (Offset = 220h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10310. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0220h
MCASP1	02B1 0220h
MCASP2	02B2 0220h
MCASP3	02B3 0220h
MCASP4	02B4 0220h

Figure 14-5099. MCASP_XBUF8 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10311. MCASP_XBUF8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.84 MCASP_XBUF9 Register

14.7.1.2.2.84.1 MCASP_XBUF9 Register (Offset = 224h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10312. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0224h
MCASP1	02B1 0224h
MCASP2	02B2 0224h
MCASP3	02B3 0224h
MCASP4	02B4 0224h

Figure 14-5100. MCASP_XBUF9 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10313. MCASP_XBUF9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.85 MCASP_XBUF10 Register

14.7.1.2.2.85.1 MCASP_XBUF10 Register (Offset = 228h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10314. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0228h
MCASP1	02B1 0228h
MCASP2	02B2 0228h
MCASP3	02B3 0228h
MCASP4	02B4 0228h

Figure 14-5101. MCASP_XBUF10 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10315. MCASP_XBUF10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.86 MCASP_XBUF11 Register

14.7.1.2.2.86.1 MCASP_XBUF11 Register (Offset = 22Ch) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10316. Instance Table

Instance Name	Physical Address
MCASP0	02B0 022Ch
MCASP1	02B1 022Ch
MCASP2	02B2 022Ch
MCASP3	02B3 022Ch
MCASP4	02B4 022Ch

Figure 14-5102. MCASP_XBUF11 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10317. MCASP_XBUF11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.87 MCASP_XBUF12 Register

14.7.1.2.2.87.1 MCASP_XBUF12 Register (Offset = 230h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10318. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0230h
MCASP1	02B1 0230h
MCASP2	02B2 0230h
MCASP3	02B3 0230h
MCASP4	02B4 0230h

Figure 14-5103. MCASP_XBUF12 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10319. MCASP_XBUF12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.88 MCASP_XBUF13 Register

14.7.1.2.2.88.1 MCASP_XBUF13 Register (Offset = 234h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10320. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0234h
MCASP1	02B1 0234h
MCASP2	02B2 0234h
MCASP3	02B3 0234h
MCASP4	02B4 0234h

Figure 14-5104. MCASP_XBUF13 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10321. MCASP_XBUF13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.89 MCASP_XBUF14 Register

14.7.1.2.2.89.1 MCASP_XBUF14 Register (Offset = 238h) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10322. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0238h
MCASP1	02B1 0238h
MCASP2	02B2 0238h
MCASP3	02B3 0238h
MCASP4	02B4 0238h

Figure 14-5105. MCASP_XBUF14 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10323. MCASP_XBUF14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.90 MCASP_XBUF15 Register

14.7.1.2.2.90.1 MCASP_XBUF15 Register (Offset = 23Ch) [reset = 0h]

The transmit buffers for the serializers (XBUF0) hold data from the transmit format unit. For transmit operations, the XBUF0 is an alias of the XRBUF in the serializer. Accessing XBUF0 registers not implemented on a specific device may cause improper device operation.

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Table 14-10324. Instance Table

Instance Name	Physical Address
MCASP0	02B0 023Ch
MCASP1	02B1 023Ch
MCASP2	02B2 023Ch
MCASP3	02B3 023Ch
MCASP4	02B4 023Ch

Figure 14-5106. MCASP_XBUF15 Name Register

31	30	29	28	27	26	25	24
XBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
XBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
XBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
XBUF							
R/W							
0h							

Table 14-10325. MCASP_XBUF15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XBUF	R/W	0h	Transmit buffers for serializers.

14.7.1.2.2.91 MCASP_RBUF0 Register

14.7.1.2.2.91.1 MCASP_RBUF0 Register (Offset = 280h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10326. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0280h
MCASP1	02B1 0280h
MCASP2	02B2 0280h
MCASP3	02B3 0280h
MCASP4	02B4 0280h

Figure 14-5107. MCASP_RBUF0 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10327. MCASP_RBUF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.92 MCASP_RBUF1 Register

14.7.1.2.2.92.1 MCASP_RBUF1 Register (Offset = 284h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10328. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0284h
MCASP1	02B1 0284h
MCASP2	02B2 0284h
MCASP3	02B3 0284h
MCASP4	02B4 0284h

Figure 14-5108. MCASP_RBUF1 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10329. MCASP_RBUF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.93 MCASP_RBUF2 Register

14.7.1.2.2.93.1 MCASP_RBUF2 Register (Offset = 288h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10330. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0288h
MCASP1	02B1 0288h
MCASP2	02B2 0288h
MCASP3	02B3 0288h
MCASP4	02B4 0288h

Figure 14-5109. MCASP_RBUF2 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10331. MCASP_RBUF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.94 MCASP_RBUF3 Register

14.7.1.2.2.94.1 MCASP_RBUF3 Register (Offset = 28Ch) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10332. Instance Table

Instance Name	Physical Address
MCASP0	02B0 028Ch
MCASP1	02B1 028Ch
MCASP2	02B2 028Ch
MCASP3	02B3 028Ch
MCASP4	02B4 028Ch

Figure 14-5110. MCASP_RBUF3 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10333. MCASP_RBUF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.95 MCASP_RBUF4 Register

14.7.1.2.2.95.1 MCASP_RBUF4 Register (Offset = 290h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10334. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0290h
MCASP1	02B1 0290h
MCASP2	02B2 0290h
MCASP3	02B3 0290h
MCASP4	02B4 0290h

Figure 14-5111. MCASP_RBUF4 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10335. MCASP_RBUF4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.96 MCASP_RBUF5 Register

14.7.1.2.2.96.1 MCASP_RBUF5 Register (Offset = 294h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10336. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0294h
MCASP1	02B1 0294h
MCASP2	02B2 0294h
MCASP3	02B3 0294h
MCASP4	02B4 0294h

Figure 14-5112. MCASP_RBUF5 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10337. MCASP_RBUF5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.97 MCASP_RBUF6 Register

14.7.1.2.2.97.1 MCASP_RBUF6 Register (Offset = 298h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10338. Instance Table

Instance Name	Physical Address
MCASP0	02B0 0298h
MCASP1	02B1 0298h
MCASP2	02B2 0298h
MCASP3	02B3 0298h
MCASP4	02B4 0298h

Figure 14-5113. MCASP_RBUF6 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10339. MCASP_RBUF6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.98 MCASP_RBUF7 Register

14.7.1.2.2.98.1 MCASP_RBUF7 Register (Offset = 29Ch) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10340. Instance Table

Instance Name	Physical Address
MCASP0	02B0 029Ch
MCASP1	02B1 029Ch
MCASP2	02B2 029Ch
MCASP3	02B3 029Ch
MCASP4	02B4 029Ch

Figure 14-5114. MCASP_RBUF7 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10341. MCASP_RBUF7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.99 MCASP_RBUF8 Register

14.7.1.2.2.99.1 MCASP_RBUF8 Register (Offset = 2A0h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10342. Instance Table

Instance Name	Physical Address
MCASP0	02B0 02A0h
MCASP1	02B1 02A0h
MCASP2	02B2 02A0h
MCASP3	02B3 02A0h
MCASP4	02B4 02A0h

Figure 14-5115. MCASP_RBUF8 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RBUF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RBUF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RBUF							
R/W							
0h							

Table 14-10343. MCASP_RBUF8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.100 MCASP_RBUF9 Register

14.7.1.2.2.100.1 MCASP_RBUF9 Register (Offset = 2A4h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10344. Instance Table

Instance Name	Physical Address
MCASP0	02B0 02A4h
MCASP1	02B1 02A4h
MCASP2	02B2 02A4h
MCASP3	02B3 02A4h
MCASP4	02B4 02A4h

Figure 14-5116. MCASP_RBUF9 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10345. MCASP_RBUF9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.101 MCASP_RBUF10 Register

14.7.1.2.2.101.1 MCASP_RBUF10 Register (Offset = 2A8h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

Return to Summary Table

Table 14-10346. Instance Table

Instance Name	Physical Address
MCASP0	02B0 02A8h
MCASP1	02B1 02A8h
MCASP2	02B2 02A8h
MCASP3	02B3 02A8h
MCASP4	02B4 02A8h

Figure 14-5117. MCASP_RBUF10 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RBUF							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RBUF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RBUF							
R/W							
0h							

Table 14-10347. MCASP_RBUF10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.102 MCASP_RBUF11 Register

14.7.1.2.2.102.1 MCASP_RBUF11 Register (Offset = 2ACh) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10348. Instance Table

Instance Name	Physical Address
MCASP0	02B0 02ACh
MCASP1	02B1 02ACh
MCASP2	02B2 02ACh
MCASP3	02B3 02ACh
MCASP4	02B4 02ACh

Figure 14-5118. MCASP_RBUF11 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10349. MCASP_RBUF11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.103 MCASP_RBUF12 Register

14.7.1.2.2.103.1 MCASP_RBUF12 Register (Offset = 2B0h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10350. Instance Table

Instance Name	Physical Address
MCASP0	02B0 02B0h
MCASP1	02B1 02B0h
MCASP2	02B2 02B0h
MCASP3	02B3 02B0h
MCASP4	02B4 02B0h

Figure 14-5119. MCASP_RBUF12 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10351. MCASP_RBUF12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.104 MCASP_RBUF13 Register

14.7.1.2.2.104.1 MCASP_RBUF13 Register (Offset = 2B4h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10352. Instance Table

Instance Name	Physical Address
MCASP0	02B0 02B4h
MCASP1	02B1 02B4h
MCASP2	02B2 02B4h
MCASP3	02B3 02B4h
MCASP4	02B4 02B4h

Figure 14-5120. MCASP_RBUF13 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10353. MCASP_RBUF13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.105 MCASP_RBUF14 Register

14.7.1.2.2.105.1 MCASP_RBUF14 Register (Offset = 2B8h) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10354. Instance Table

Instance Name	Physical Address
MCASP0	02B0 02B8h
MCASP1	02B1 02B8h
MCASP2	02B2 02B8h
MCASP3	02B3 02B8h
MCASP4	02B4 02B8h

Figure 14-5121. MCASP_RBUF14 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10355. MCASP_RBUF14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.106 MCASP_RBUF15 Register

14.7.1.2.2.106.1 MCASP_RBUF15 Register (Offset = 2BCh) [reset = 0h]

The receive buffers for the serializers (RBUF0) hold data from the serializer before the data goes to the receive format unit. For receive operations, the RBUF0 is an alias of the XRBUF0 in the serializer. Accessing XBUF registers not implemented on a specific device may cause improper device operation.

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Table 14-10356. Instance Table

Instance Name	Physical Address
MCASP0	02B0 02BCh
MCASP1	02B1 02BCh
MCASP2	02B2 02BCh
MCASP3	02B3 02BCh
MCASP4	02B4 02BCh

Figure 14-5122. MCASP_RBUF15 Name Register

31	30	29	28	27	26	25	24
RBUF							
R/W							
0h							
23	22	21	20	19	18	17	16
RBUF							
R/W							
0h							
15	14	13	12	11	10	9	8
RBUF							
R/W							
0h							
7	6	5	4	3	2	1	0
RBUF							
R/W							
0h							

Table 14-10357. MCASP_RBUF15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RBUF	R/W	0h	Receive buffers for serializers.

14.7.1.2.2.107 MCASP_WFIFOCTL Register

14.7.1.2.2.107.1 MCASP_WFIFOCTL Register (Offset = 1000h) [reset = 1004h]

The WNUMEVT and WNUMDMA values must be set prior to enabling the Write FIFO. If the Write FIFO is to be enabled, it must be enabled prior to taking the McASP out of reset

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Table 14-10358. Instance Table

Instance Name	Physical Address
MCASP0	02B0 1000h
MCASP1	02B1 1000h
MCASP2	02B2 1000h
MCASP3	02B3 1000h
MCASP4	02B4 1000h

Figure 14-5123. MCASP_WFIFOCTL Name Register

31	30	29	28	27	26	25	24
RESERVED127							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED127							WENA
R							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WNUMEVT							
R/W							
10h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WNUMDMA							
R/W							
4h							

Table 14-10359. MCASP_WFIFOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED127	R	0h	
16	WENA	R/W	0h	Write FIFO enable bit. 0 `Write FIFO is disabled. The WLVL bit in the Write FIFO status register (WFIFOSTS) is reset to 0 and pointers are initialized, that is, the Write FIFO is flushed.` 1 `Write FIFO is enabled. If Write FIFO is to be enabled, it must be enabled prior to taking McASP out of reset.`

Table 14-10359. MCASP_WFIFOCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	WNUMEVT	R/W	10h	Write word count per DMA event [32 bit]. When the Write FIFO has space for at least WNUMEVT words of data, then an AXEVT [transmit DMA event] is generated to the host/DMA controller. This value should be set to a non-zero integer multiple of the number of serializers enabled as transmitters. This value must be set prior to enabling the Write FIFO. 416h = 3 to 64 words from 3h to 416h. FFh = Reserved from 41h to FFh. 0 0 words 1 1 word 2 2 words 3 3 to 64 words from 3h to 40h. 65 Reserved from 41h to FFh.
7:0	WNUMDMA	R/W	4h	Write word count per transfer [32 bit words]. Upon a transmit DMA event from the McASP, WNUMDMA words are transferred from the Write FIFO to the McASP. This value must equal the number of McASP serializers used as transmitters. This value must be set prior to enabling the Write FIFO. FFh = Reserved from 11h to FFh. 0 0 words 1 1 word 2 2 words 3 3-16 words from 3h to 10h. 17 Reserved from 11h to FFh.

14.7.1.2.2.108 MCASP_WFIFOSTS Register

14.7.1.2.2.108.1 MCASP_WFIFOSTS Register (Offset = 1004h) [reset = 0h]

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Table 14-10360. Instance Table

Instance Name	Physical Address
MCASP0	02B0 1004h
MCASP1	02B1 1004h
MCASP2	02B2 1004h
MCASP3	02B3 1004h
MCASP4	02B4 1004h

Figure 14-5124. MCASP_WFIFOSTS Name Register

31	30	29	28	27	26	25	24
RESERVED128							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED128							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED128							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WLVL							
R							
0h							

Table 14-10361. MCASP_WFIFOSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED128	R	0h	

7:0	WLVL	R	0h	Write level [read-only]. Number of 32 bit words currently in the Write FIFO. 40h = 3 to 64 words currently in Write FIFO from 3h to 40h. FFh = Reserved from 41h to FFh.
				`0      0 words currently in Write FIFO.`
				`1      1 word currently in Write FIFO.`
				`2      2 words currently in Write FIFO.`
				`3      3 to 64 words currently in Write FIFO from 3h to 40h.`
				`65     Reserved from 41h to FFh.`

14.7.1.2.2.109 MCASP_RFIFOCTL Register

14.7.1.2.2.109.1 MCASP_RFIFOCTL Register (Offset = 1008h) [reset = 1004h]

The RNUMEVT and RNUMDMA values must be set prior to enabling the Read FIFO. If the Read FIFO is to be enabled, it must be enabled prior to taking the McASP out of reset

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Table 14-10362. Instance Table

Instance Name	Physical Address
MCASP0	02B0 1008h
MCASP1	02B1 1008h
MCASP2	02B2 1008h
MCASP3	02B3 1008h
MCASP4	02B4 1008h

Figure 14-5125. MCASP_RFIFOCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED129</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED129</td><td>RENA</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RNUMEVT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RNUMDMA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-10363. MCASP_RFIFOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED129	R	0h	
16	RENA	R/W	0h	Read FIFO enable bit. 0 `Read FIFO is disabled. The RLVL bit in the Read FIFO status register (RFIFOSTS) is reset to 0 and pointers are initialized, that is, the Read FIFO is flushed.` 1 `Read FIFO is enabled. If Read FIFO is to be enabled, it must be enabled prior to taking McASP out of reset.`

Table 14-10363. MCASP_RFIFOCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	RNUMEVT	R/W	10h	Read word count per DMA event [32 bit]. When the Read FIFO contains at least RNUMEVT words of data, then an AREVT [receive DMA event] is generated to the host/DMA controller. This value should be set to a non-zero integer multiple of the number of serializers enabled as receivers. This value must be set prior to enabling the Read FIFO. 416h = 3 to 64 words from 3h to 416h. FFh = Reserved from 41h = FFh. 0 0 words 1 1 word 2 2 words 3 3 to 64 words from 3h to 40h. 65 Reserved from 41h to FFh.
7:0	RNUMDMA	R/W	4h	Read word count per transfer [32 bit words]. Upon a receive DMA event from the McASP, the Read FIFO reads RNUMDMA words from the McASP. This value must equal the number of McASP serializers used as receivers. This value must be set prior to enabling the Read FIFO. 10h = 3 to 16 words from 3h to 10h. FFh = Reserved from 11h to FFh. 0 0 words 1 1 word 2 2 words 3 3 to 16 words from 3h to 10h. 17 Reserved from 11h to FFh.

14.7.1.2.2.110 MCASP_RFIFOSTS Register

14.7.1.2.2.110.1 MCASP_RFIFOSTS Register (Offset = 100Ch) [reset = 0h]

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Table 14-10364. Instance Table

Instance Name	Physical Address
MCASP0	02B0 100Ch
MCASP1	02B1 100Ch
MCASP2	02B2 100Ch
MCASP3	02B3 100Ch
MCASP4	02B4 100Ch

Figure 14-5126. MCASP_RFIFOSTS Name Register

31	30	29	28	27	26	25	24
RESERVED130							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED130							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED130							
R							
0h							
7	6	5	4	3	2	1	0
RLVL							
R							
0h							

Table 14-10365. MCASP_RFIFOSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED130	R	0h	
7:0	RLVL	R	0h	Read level [read-only]. Number of 32 bit words currently in the Read FIFO. 40h = 3 to 64 words currently in Read FIFO from 3h to 40h. FFh = Reserved from 41h to FFh. 0 0 words currently in Read FIFO. 1 1 word currently in Read FIFO. 2 2 words currently in Read FIFO. 3 3 to 64 words currently in Read FIFO from 3h to 40h. 65 Reserved from 41h to FFh.

14.7.1.3 atl

atl

14.7.1.3.1 atl Summaries

atl Summaries

Table 14-10366. ATL_MMR Registers, Base Address=0FEE 0000h, Length=1024

Offset	Length	Register Name	atl0 Physical Address
0h	32	ATL_MMR_REVISION	0FEE 0000h
200h	32	ATL_MMR_ATL0_PPMR	0FEE 0200h
204h	32	ATL_MMR_ATL0_BBSR	0FEE 0204h
208h	32	ATL_MMR_ATL0_ATLCR	0FEE 0208h
210h	32	ATL_MMR_ATL0_SWEN	0FEE 0210h
214h	32	ATL_MMR_ATL0_BWSMUX	0FEE 0214h
218h	32	ATL_MMR_ATL0_AWSMUX	0FEE 0218h
21Ch	32	ATL_MMR_ATL0_PCLKMUX	0FEE 021Ch
280h	32	ATL_MMR_ATL1_PPMR	0FEE 0280h
284h	32	ATL_MMR_ATL1_BBSR	0FEE 0284h
288h	32	ATL_MMR_ATL1_ATLCR	0FEE 0288h
290h	32	ATL_MMR_ATL1_SWEN	0FEE 0290h
294h	32	ATL_MMR_ATL1_BWSMUX	0FEE 0294h
298h	32	ATL_MMR_ATL1_AWSMUX	0FEE 0298h
29Ch	32	ATL_MMR_ATL1_PCLKMUX	0FEE 029Ch
300h	32	ATL_MMR_ATL2_PPMR	0FEE 0300h
304h	32	ATL_MMR_ATL2_BBSR	0FEE 0304h
308h	32	ATL_MMR_ATL2_ATLCR	0FEE 0308h
310h	32	ATL_MMR_ATL2_SWEN	0FEE 0310h
314h	32	ATL_MMR_ATL2_BWSMUX	0FEE 0314h
318h	32	ATL_MMR_ATL2_AWSMUX	0FEE 0318h
31Ch	32	ATL_MMR_ATL2_PCLKMUX	0FEE 031Ch
380h	32	ATL_MMR_ATL3_PPMR	0FEE 0380h
384h	32	ATL_MMR_ATL3_BBSR	0FEE 0384h
388h	32	ATL_MMR_ATL3_ATLCR	0FEE 0388h
390h	32	ATL_MMR_ATL3_SWEN	0FEE 0390h
394h	32	ATL_MMR_ATL3_BWSMUX	0FEE 0394h
398h	32	ATL_MMR_ATL3_AWSMUX	0FEE 0398h
39Ch	32	ATL_MMR_ATL3_PCLKMUX	0FEE 039Ch

14.7.1.3.2 atl Registers

atl Registers

14.7.1.3.2.1 ATL_MMR_REVISION Register

14.7.1.3.2.1.1 ATL_MMR_REVISION Register (Offset = 0h) [reset = A072100h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-10367. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0000h

Figure 14-5127. ATL_MMR_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNCTION			
R		R		R			
0h		0h		A07h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
A07h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
4h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-10368. ATL_MMR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	0h	PID register scheme Reset Source: mod_g_rst_n
29:28	RESERVED	R	0h	Reserved
27:16	FUNCTION	R	A07h	Module ID Reset Source: mod_g_rst_n
15:11	RTL	R	4h	RTL revision. Will vary depending on release. Reset Source: mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: mod_g_rst_n

14.7.1.3.2.2 ATL_MMR_ATL0_PPMR Register

14.7.1.3.2.2.1 ATL_MMR_ATL0_PPMR Register (Offset = 200h) [reset = 0h]

The PPM register is used by the Audio re-timing code. The DAC over-sampling clock will slow down or speed up by the PPM written to bits [8:0].

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Table 14-10369. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0200h

Figure 14-5128. ATL_MMR_ATL0_PPMR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PPM_SD	RESERVED						PPM_SET
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPM_SET							
R/W							
0h							

Table 14-10370. ATL_MMR_ATL0_PPMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	PPM_SD	R/W	0h	1 = Slow down 0 = Speed up Reset Source: mod_g_rst_n
14:9	RESERVED	NONE	0h	Reserved
8:0	PPM_SET	R/W	0h	This is the 9-bit parts-per-million value in the adjusting circuit. PPM adjustment = PPMSET/2^20 Reset Source: mod_g_rst_n

14.7.1.3.2.3 ATL_MMR_ATL0_BBSR Register

14.7.1.3.2.3.1 ATL_MMR_ATL0_BBSR Register (Offset = 204h) [reset = 0h]

The measuring circuit produces a 16-bit Sample Count. Its inputs are the Audio IIS Word Select (AWS) and the Baseband IIS Word Select (BWS) from their respective MCASP pins. The sample count is a read-only register.

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Table 14-10371. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0204h

Figure 14-5129. ATL_MMR_ATL0_BBSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SMP_CNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SMP_CNT							
R							
0h							

Table 14-10372. ATL_MMR_ATL0_BBSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SMP_CNT	R	0h	This is the 16-bit sample count from the measuring circuit Reset Source: mod_g_rst_n

14.7.1.3.2.4 ATL_MMR_ATL0_ATLCR Register

14.7.1.3.2.4.1 ATL_MMR_ATL0_ATLCR Register (Offset = 208h) [reset = 18h]

The modem Clock Divide Select bit is used during factory calibration of the radio to match latency between the analog and digital signal paths. The ATL Internal Divider divides down the ATL master clock to make ATCLK.

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Table 14-10373. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0208h

Figure 14-5130. ATL_MMR_ATL0_ATLCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		CLK_DIV_SEL	INT_DIV				
NONE		R/W	R/W				
0h		0h	18h				

Table 14-10374. ATL_MMR_ATL0_ATLCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	CLK_DIV_SEL	R/W	0h	0: MODCLK = AWS divided by 2^16 1: MODCLK = AWS divided by 2^12 Reset Source: mod_g_rst_n
4:0	INT_DIV	R/W	18h	Sets ratio of ATLPCLK to ATCLK Reset Source: mod_g_rst_n

14.7.1.3.2.5 ATL_MMR_ATL0_SWEN Register

14.7.1.3.2.5.1 ATL_MMR_ATL0_SWEN Register (Offset = 210h) [reset = 0h]

The software enable register is used to enable/disable the ATL.

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Table 14-10375. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0210h

Figure 14-5131. ATL_MMR_ATL0_SWEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
NONE							R/W
0h							0h

Table 14-10376. ATL_MMR_ATL0_SWEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE	R/W	0h	When disabled the ATL registers are forced to known states for simulation purposes. Runtime startup doesn't require initial values because measurement is relative to an arbitrary initial value. All registers are reset to zero except ATLCR.INT_DIV which is resets to 24 (divide-by-25, because zero is not a legal divide ratio.) Reset Source: mod_g_rst_n

14.7.1.3.2.6 ATL_MMR_ATL0_BWSMUX Register

14.7.1.3.2.6.1 ATL_MMR_ATL0_BWSMUX Register (Offset = 214h) [reset = 0h]

The Baseband IIS Word Select mux select control register

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Table 14-10377. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0214h

Figure 14-5132. ATL_MMR_ATL0_BWSMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SELECT			
NONE				R/W			
0h				0h			

Table 14-10378. ATL_MMR_ATL0_BWSMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	SELECT	R/W	0h	BWS input select: 0000: atl_io_port_bws[0] 0001: atl_io_port_bws[1] 0010: atl_io_port_bws[2] 0011: atl_io_port_bws[3] 0100: atl_io_port_bws[4] 0101: atl_io_port_bws[5] 0110: atl_io_port_bws[6] 0111: atl_io_port_bws[7] 1000: atl_io_port_bws[8] 1001: atl_io_port_bws[9] 1010: atl_io_port_bws[10] 1011: atl_io_port_bws[11] 1100: atl_io_port_bws[12] 1101: atl_io_port_bws[13] 1110: atl_io_port_bws[14] 1111: atl_io_port_bws[15] Reset Source: mod_g_rst_n

14.7.1.3.2.7 ATL_MMR_ATL0_AWSMUX Register

14.7.1.3.2.7.1 ATL_MMR_ATL0_AWSMUX Register (Offset = 218h) [reset = 0h]

The Audio IIS Word Select mux select control register

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Table 14-10379. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0218h

Figure 14-5133. ATL_MMR_ATL0_AWSMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SELECT			
NONE				R/W			
0h				0h			

Table 14-10380. ATL_MMR_ATL0_AWSMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	SELECT	R/W	0h	AWS input select: 0000: atl_io_port_aws[0] 0001: atl_io_port_aws[1] 0010: atl_io_port_aws[2] 0011: atl_io_port_aws[3] 0100: atl_io_port_aws[4] 0101: atl_io_port_aws[5] 0110: atl_io_port_aws[6] 0111: atl_io_port_aws[7] 1000: atl_io_port_aws[8] 1001: atl_io_port_aws[9] 1010: atl_io_port_aws[10] 1011: atl_io_port_aws[11] 1100: atl_io_port_aws[12] 1101: atl_io_port_aws[13] 1110: atl_io_port_aws[14] 1111: atl_io_port_aws[15] Reset Source: mod_g_rst_n

14.7.1.3.2.8 ATL_MMR_ATL0_PCLKMUX Register

14.7.1.3.2.8.1 ATL_MMR_ATL0_PCLKMUX Register (Offset = 21Ch) [reset = 0h]

ATL core input clock mux select control register

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Table 14-10381. Instance Table

Instance Name	Physical Address
ATL0	0FEE 021Ch

Figure 14-5134. ATL_MMR_ATL0_PCLKMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SELECT
NONE							R/W
0h							0h

Table 14-10382. ATL_MMR_ATL0_PCLKMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SELECT	R/W	0h	ATL[0-3] core clock select: 0: vbus_clk 1: atl_clk Reset Source: mod_g_rst_n

14.7.1.3.2.9 ATL_MMR_ATL1_PPMR Register

14.7.1.3.2.9.1 ATL_MMR_ATL1_PPMR Register (Offset = 280h) [reset = 0h]

The PPM register is used by the Audio re-timing code. The DAC over-sampling clock will slow down or speed up by the PPM written to bits [8:0].

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Table 14-10383. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0280h

Figure 14-5135. ATL_MMR_ATL1_PPMR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PPM_SD	RESERVED						PPM_SET
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
PPM_SET							
R/W							
0h							

Table 14-10384. ATL_MMR_ATL1_PPMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	PPM_SD	R/W	0h	1 = Slow down 0 = Speed up Reset Source: mod_g_rst_n
14:9	RESERVED	NONE	0h	Reserved
8:0	PPM_SET	R/W	0h	This is the 9-bit parts-per-million value in the adjusting circuit. PPM adjustment = PPMSET/2^20 Reset Source: mod_g_rst_n

14.7.1.3.2.10 ATL_MMR_ATL1_BBSR Register

14.7.1.3.2.10.1 ATL_MMR_ATL1_BBSR Register (Offset = 284h) [reset = 0h]

The measuring circuit produces a 16-bit Sample Count. Its inputs are the Audio IIS Word Select (AWS) and the Baseband IIS Word Select (BWS) from their respective MCASP pins. The sample count is a read-only register.

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Table 14-10385. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0284h

Figure 14-5136. ATL_MMR_ATL1_BBSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SMP_CNT							
R							
0h							
7	6	5	4	3	2	1	0
SMP_CNT							
R							
0h							

Table 14-10386. ATL_MMR_ATL1_BBSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SMP_CNT	R	0h	This is the 16-bit sample count from the measuring circuit Reset Source: mod_g_rst_n

14.7.1.3.2.11 ATL_MMR_ATL1_ATLCR Register

14.7.1.3.2.11.1 ATL_MMR_ATL1_ATLCR Register (Offset = 288h) [reset = 18h]

The modem Clock Divide Select bit is used during factory calibration of the radio to match latency between the analog and digital signal paths. The ATL Internal Divider divides down the ATL master clock to make ATCLK.

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Table 14-10387. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0288h

Figure 14-5137. ATL_MMR_ATL1_ATLCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_DIV_SEL	INT_DIV				
NONE		R/W	R/W				
0h		0h	18h				

Table 14-10388. ATL_MMR_ATL1_ATLCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	CLK_DIV_SEL	R/W	0h	0: MODCLK = AWS divided by 2^16 1: MODCLK = AWS divided by 2^12 Reset Source: mod_g_rst_n
4:0	INT_DIV	R/W	18h	Sets ratio of ATLPCLK to ATCLK Reset Source: mod_g_rst_n

14.7.1.3.2.12 ATL_MMR_ATL1_SWEN Register

14.7.1.3.2.12.1 ATL_MMR_ATL1_SWEN Register (Offset = 290h) [reset = 0h]

The software enable register is used to enable/disable the ATL.

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Table 14-10389. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0290h

Figure 14-5138. ATL_MMR_ATL1_SWEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
NONE							R/W
0h							0h

Table 14-10390. ATL_MMR_ATL1_SWEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE	R/W	0h	When disabled the ATL registers are forced to known states for simulation purposes. Runtime startup doesn't require initial values because measurement is relative to an arbitrary initial value. All registers are reset to zero except ATLCR.INT_DIV which is resets to 24 (divide-by-25, because zero is not a legal divide ratio.) Reset Source: mod_g_rst_n

14.7.1.3.2.13 ATL_MMR_ATL1_BWSMUX Register

14.7.1.3.2.13.1 ATL_MMR_ATL1_BWSMUX Register (Offset = 294h) [reset = 0h]

The Baseband IIS Word Select mux select control register

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Table 14-10391. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0294h

Figure 14-5139. ATL_MMR_ATL1_BWSMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SELECT			
NONE				R/W			
0h				0h			

Table 14-10392. ATL_MMR_ATL1_BWSMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	SELECT	R/W	0h	BWS input select: 0000: atl_io_port_bws[0] 0001: atl_io_port_bws[1] 0010: atl_io_port_bws[2] 0011: atl_io_port_bws[3] 0100: atl_io_port_bws[4] 0101: atl_io_port_bws[5] 0110: atl_io_port_bws[6] 0111: atl_io_port_bws[7] 1000: atl_io_port_bws[8] 1001: atl_io_port_bws[9] 1010: atl_io_port_bws[10] 1011: atl_io_port_bws[11] 1100: atl_io_port_bws[12] 1101: atl_io_port_bws[13] 1110: atl_io_port_bws[14] 1111: atl_io_port_bws[15] Reset Source: mod_g_rst_n

14.7.1.3.2.14 ATL_MMR_ATL1_AWSMUX Register

14.7.1.3.2.14.1 ATL_MMR_ATL1_AWSMUX Register (Offset = 298h) [reset = 0h]

The Audio IIS Word Select mux select control register

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Table 14-10393. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0298h

Figure 14-5140. ATL_MMR_ATL1_AWSMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SELECT			
NONE				R/W			
0h				0h			

Table 14-10394. ATL_MMR_ATL1_AWSMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	SELECT	R/W	0h	AWS input select: 0000: atl_io_port_aws[0] 0001: atl_io_port_aws[1] 0010: atl_io_port_aws[2] 0011: atl_io_port_aws[3] 0100: atl_io_port_aws[4] 0101: atl_io_port_aws[5] 0110: atl_io_port_aws[6] 0111: atl_io_port_aws[7] 1000: atl_io_port_aws[8] 1001: atl_io_port_aws[9] 1010: atl_io_port_aws[10] 1011: atl_io_port_aws[11] 1100: atl_io_port_aws[12] 1101: atl_io_port_aws[13] 1110: atl_io_port_aws[14] 1111: atl_io_port_aws[15] Reset Source: mod_g_rst_n

14.7.1.3.2.15 ATL_MMR_ATL1_PCLKMUX Register

14.7.1.3.2.15.1 ATL_MMR_ATL1_PCLKMUX Register (Offset = 29Ch) [reset = 0h]

ATL core input clock mux select control register

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Table 14-10395. Instance Table

Instance Name	Physical Address
ATL0	0FEE 029Ch

Figure 14-5141. ATL_MMR_ATL1_PCLKMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SELECT
NONE							R/W
0h							0h

Table 14-10396. ATL_MMR_ATL1_PCLKMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SELECT	R/W	0h	Non-functional Reset Source: mod_g_rst_n

14.7.1.3.2.16 ATL_MMR_ATL2_PPMR Register

14.7.1.3.2.16.1 ATL_MMR_ATL2_PPMR Register (Offset = 300h) [reset = 0h]

The PPM register is used by the Audio re-timing code. The DAC over-sampling clock will slow down or speed up by the PPM written to bits [8:0].

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Table 14-10397. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0300h

Figure 14-5142. ATL_MMR_ATL2_PPMR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PPM_SD	RESERVED						PPM_SET
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
PPM_SET							
R/W							
0h							

Table 14-10398. ATL_MMR_ATL2_PPMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	PPM_SD	R/W	0h	1 = Slow down 0 = Speed up Reset Source: mod_g_rst_n
14:9	RESERVED	NONE	0h	Reserved
8:0	PPM_SET	R/W	0h	This is the 9-bit parts-per-million value in the adjusting circuit. PPM adjustment = PPMSET/2^20 Reset Source: mod_g_rst_n

14.7.1.3.2.17 ATL_MMR_ATL2_BBSR Register

14.7.1.3.2.17.1 ATL_MMR_ATL2_BBSR Register (Offset = 304h) [reset = 0h]

The measuring circuit produces a 16-bit Sample Count. Its inputs are the Audio IIS Word Select (AWS) and the Baseband IIS Word Select (BWS) from their respective MCASP pins. The sample count is a read-only register.

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Table 14-10399. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0304h

Figure 14-5143. ATL_MMR_ATL2_BBSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SMP_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SMP_CNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10400. ATL_MMR_ATL2_BBSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SMP_CNT	R	0h	This is the 16-bit sample count from the measuring circuit Reset Source: mod_g_rst_n

14.7.1.3.2.18 ATL_MMR_ATL2_ATLCR Register

14.7.1.3.2.18.1 ATL_MMR_ATL2_ATLCR Register (Offset = 308h) [reset = 18h]

The modem Clock Divide Select bit is used during factory calibration of the radio to match latency between the analog and digital signal paths. The ATL Internal Divider divides down the ATL master clock to make ATCLK.

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Table 14-10401. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0308h

Figure 14-5144. ATL_MMR_ATL2_ATLCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_DIV_SEL	INT_DIV				
NONE		R/W	R/W				
0h		0h	18h				

Table 14-10402. ATL_MMR_ATL2_ATLCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	CLK_DIV_SEL	R/W	0h	0: MODCLK = AWS divided by 2^16 1: MODCLK = AWS divided by 2^12 Reset Source: mod_g_rst_n
4:0	INT_DIV	R/W	18h	Sets ratio of ATLPCLK to ATCLK Reset Source: mod_g_rst_n

14.7.1.3.2.19 ATL_MMR_ATL2_SWEN Register

14.7.1.3.2.19.1 ATL_MMR_ATL2_SWEN Register (Offset = 310h) [reset = 0h]

The software enable register is used to enable/disable the ATL.

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Table 14-10403. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0310h

Figure 14-5145. ATL_MMR_ATL2_SWEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
NONE							R/W
0h							0h

Table 14-10404. ATL_MMR_ATL2_SWEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE	R/W	0h	When disabled the ATL registers are forced to known states for simulation purposes. Runtime startup doesn't require initial values because measurement is relative to an arbitrary initial value. All registers are reset to zero except ATLCR.INT_DIV which is resets to 24 (divide-by-25, because zero is not a legal divide ratio.) Reset Source: mod_g_rst_n

14.7.1.3.2.20 ATL_MMR_ATL2_BWSMUX Register

14.7.1.3.2.20.1 ATL_MMR_ATL2_BWSMUX Register (Offset = 314h) [reset = 0h]

The Baseband IIS Word Select mux select control register

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Table 14-10405. Instance Table

Instance Name	**Physical Address**
ATL0	0FEE 0314h

Figure 14-5146. ATL_MMR_ATL2_BWSMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SELECT			
NONE				R/W			
0h				0h			

Table 14-10406. ATL_MMR_ATL2_BWSMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	SELECT	R/W	0h	BWS input select: 0000: atl_io_port_bws[0] 0001: atl_io_port_bws[1] 0010: atl_io_port_bws[2] 0011: atl_io_port_bws[3] 0100: atl_io_port_bws[4] 0101: atl_io_port_bws[5] 0110: atl_io_port_bws[6] 0111: atl_io_port_bws[7] 1000: atl_io_port_bws[8] 1001: atl_io_port_bws[9] 1010: atl_io_port_bws[10] 1011: atl_io_port_bws[11] 1100: atl_io_port_bws[12] 1101: atl_io_port_bws[13] 1110: atl_io_port_bws[14] 1111: atl_io_port_bws[15] Reset Source: mod_g_rst_n

14.7.1.3.2.21 ATL_MMR_ATL2_AWSMUX Register

14.7.1.3.2.21.1 ATL_MMR_ATL2_AWSMUX Register (Offset = 318h) [reset = 0h]

The Audio IIS Word Select mux select control register

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Table 14-10407. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0318h

Figure 14-5147. ATL_MMR_ATL2_AWSMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SELECT			
NONE				R/W			
0h				0h			

Table 14-10408. ATL_MMR_ATL2_AWSMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	SELECT	R/W	0h	AWS input select: 0000: atl_io_port_aws[0] 0001: atl_io_port_aws[1] 0010: atl_io_port_aws[2] 0011: atl_io_port_aws[3] 0100: atl_io_port_aws[4] 0101: atl_io_port_aws[5] 0110: atl_io_port_aws[6] 0111: atl_io_port_aws[7] 1000: atl_io_port_aws[8] 1001: atl_io_port_aws[9] 1010: atl_io_port_aws[10] 1011: atl_io_port_aws[11] 1100: atl_io_port_aws[12] 1101: atl_io_port_aws[13] 1110: atl_io_port_aws[14] 1111: atl_io_port_aws[15] Reset Source: mod_g_rst_n

14.7.1.3.2.22 ATL_MMR_ATL2_PCLKMUX Register

14.7.1.3.2.22.1 ATL_MMR_ATL2_PCLKMUX Register (Offset = 31Ch) [reset = 0h]

ATL core input clock mux select control register

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Table 14-10409. Instance Table

Instance Name	Physical Address
ATL0	0FEE 031Ch

Figure 14-5148. ATL_MMR_ATL2_PCLKMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SELECT
NONE							R/W
0h							0h

Table 14-10410. ATL_MMR_ATL2_PCLKMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SELECT	R/W	0h	Non-functional Reset Source: mod_g_rst_n

14.7.1.3.2.23 ATL_MMR_ATL3_PPMR Register

14.7.1.3.2.23.1 ATL_MMR_ATL3_PPMR Register (Offset = 380h) [reset = 0h]

The PPM register is used by the Audio re-timing code. The DAC over-sampling clock will slow down or speed up by the PPM written to bits [8:0].

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Table 14-10411. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0380h

Figure 14-5149. ATL_MMR_ATL3_PPMR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PPM_SD	RESERVED						PPM_SET
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
PPM_SET							
R/W							
0h							

Table 14-10412. ATL_MMR_ATL3_PPMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	PPM_SD	R/W	0h	1 = Slow down 0 = Speed up Reset Source: mod_g_rst_n
14:9	RESERVED	NONE	0h	Reserved
8:0	PPM_SET	R/W	0h	This is the 9-bit parts-per-million value in the adjusting circuit. PPM adjustment = PPMSET/2^20 Reset Source: mod_g_rst_n

14.7.1.3.2.24 ATL_MMR_ATL3_BBSR Register

14.7.1.3.2.24.1 ATL_MMR_ATL3_BBSR Register (Offset = 384h) [reset = 0h]

The measuring circuit produces a 16-bit Sample Count. Its inputs are the Audio IIS Word Select (AWS) and the Baseband IIS Word Select (BWS) from their respective MCASP pins. The sample count is a read-only register.

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Table 14-10413. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0384h

Figure 14-5150. ATL_MMR_ATL3_BBSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SMP_CNT							
R							
0h							
7	6	5	4	3	2	1	0
SMP_CNT							
R							
0h							

Table 14-10414. ATL_MMR_ATL3_BBSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SMP_CNT	R	0h	This is the 16-bit sample count from the measuring circuit Reset Source: mod_g_rst_n

14.7.1.3.2.25 ATL_MMR_ATL3_ATLCR Register

14.7.1.3.2.25.1 ATL_MMR_ATL3_ATLCR Register (Offset = 388h) [reset = 18h]

The modem Clock Divide Select bit is used during factory calibration of the radio to match latency between the analog and digital signal paths. The ATL Internal Divider divides down the ATL master clock to make ATCLK.

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Table 14-10415. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0388h

Figure 14-5151. ATL_MMR_ATL3_ATLCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		CLK_DIV_SEL	INT_DIV				
NONE		R/W	R/W				
0h		0h	18h				

Table 14-10416. ATL_MMR_ATL3_ATLCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	CLK_DIV_SEL	R/W	0h	0: MODCLK = AWS divided by 2^16 1: MODCLK = AWS divided by 2^12 Reset Source: mod_g_rst_n
4:0	INT_DIV	R/W	18h	Sets ratio of ATLPCLK to ATCLK Reset Source: mod_g_rst_n

14.7.1.3.2.26 ATL_MMR_ATL3_SWEN Register

14.7.1.3.2.26.1 ATL_MMR_ATL3_SWEN Register (Offset = 390h) [reset = 0h]

The software enable register is used to enable/disable the ATL.

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Table 14-10417. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0390h

Figure 14-5152. ATL_MMR_ATL3_SWEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
NONE							R/W
0h							0h

Table 14-10418. ATL_MMR_ATL3_SWEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE	R/W	0h	When disabled the ATL registers are forced to known states for simulation purposes. Runtime startup doesn't require initial values because measurement is relative to an arbitrary initial value. All registers are reset to zero except ATLCR.INT_DIV which is resets to 24 (divide-by-25, because zero is not a legal divide ratio.) Reset Source: mod_g_rst_n

14.7.1.3.2.27 ATL_MMR_ATL3_BWSMUX Register

14.7.1.3.2.27.1 ATL_MMR_ATL3_BWSMUX Register (Offset = 394h) [reset = 0h]

The Baseband IIS Word Select mux select control register

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Table 14-10419. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0394h

Figure 14-5153. ATL_MMR_ATL3_BWSMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SELECT			
NONE				R/W			
0h				0h			

Table 14-10420. ATL_MMR_ATL3_BWSMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	SELECT	R/W	0h	BWS input select: 0000: atl_io_port_bws[0] 0001: atl_io_port_bws[1] 0010: atl_io_port_bws[2] 0011: atl_io_port_bws[3] 0100: atl_io_port_bws[4] 0101: atl_io_port_bws[5] 0110: atl_io_port_bws[6] 0111: atl_io_port_bws[7] 1000: atl_io_port_bws[8] 1001: atl_io_port_bws[9] 1010: atl_io_port_bws[10] 1011: atl_io_port_bws[11] 1100: atl_io_port_bws[12] 1101: atl_io_port_bws[13] 1110: atl_io_port_bws[14] 1111: atl_io_port_bws[15] Reset Source: mod_g_rst_n

14.7.1.3.2.28 ATL_MMR_ATL3_AWSMUX Register

14.7.1.3.2.28.1 ATL_MMR_ATL3_AWSMUX Register (Offset = 398h) [reset = 0h]

The Audio IIS Word Select mux select control register

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Table 14-10421. Instance Table

Instance Name	Physical Address
ATL0	0FEE 0398h

Figure 14-5154. ATL_MMR_ATL3_AWSMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				SELECT			
NONE				R/W			
0h				0h			

Table 14-10422. ATL_MMR_ATL3_AWSMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	SELECT	R/W	0h	AWS input select: 0000: atl_io_port_aws[0] 0001: atl_io_port_aws[1] 0010: atl_io_port_aws[2] 0011: atl_io_port_aws[3] 0100: atl_io_port_aws[4] 0101: atl_io_port_aws[5] 0110: atl_io_port_aws[6] 0111: atl_io_port_aws[7] 1000: atl_io_port_aws[8] 1001: atl_io_port_aws[9] 1010: atl_io_port_aws[10] 1011: atl_io_port_aws[11] 1100: atl_io_port_aws[12] 1101: atl_io_port_aws[13] 1110: atl_io_port_aws[14] 1111: atl_io_port_aws[15] Reset Source: mod_g_rst_n

14.7.1.3.2.29 ATL_MMR_ATL3_PCLKMUX Register

14.7.1.3.2.29.1 ATL_MMR_ATL3_PCLKMUX Register (Offset = 39Ch) [reset = 0h]

ATL core input clock mux select control register

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Table 14-10423. Instance Table

Instance Name	Physical Address
ATL0	0FEE 039Ch

Figure 14-5155. ATL_MMR_ATL3_PCLKMUX Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SELECT
NONE							R/W
0h							0h

Table 14-10424. ATL_MMR_ATL3_PCLKMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SELECT	R/W	0h	Non-functional Reset Source: mod_g_rst_n

14.7.1.4 MLB

MLB

14.7.1.4.1 MLB Summaries

MLB Summaries

Table 14-10425. MLBSS_CFG Registers, Base Address=02F8 0000h, Length=512

Offset	Length	Register Name	MLB0 Physical Address
0h	32	MLBSS_CFG_PID	02F8 0000h
8h	32	MLBSS_CFG_STAT	02F8 0008h
Ch	32	MLBSS_CFG_DMA_CTRL	02F8 000Ch

Table 14-10426. MLBDIM_CFG Registers, Base Address=02F8 2000h, Length=1024

Offset	Length	Register Name	MLB0 Physical Address
0h	32	MLBDIM_CFG_MLBC0	02F8 2000h
8h	32	MLBDIM_CFG_MLBPC0	02F8 2008h
Ch	32	MLBDIM_CFG_MS0	02F8 200Ch
14h	32	MLBDIM_CFG_MS1	02F8 2014h
20h	32	MLBDIM_CFG_MSS	02F8 2020h
24h	32	MLBDIM_CFG_MSD	02F8 2024h
2Ch	32	MLBDIM_CFG_MIEN	02F8 202Ch
34h	32	MLBDIM_CFG_MLBPC2	02F8 2034h
38h	32	MLBDIM_CFG_MLBPC1	02F8 2038h
3Ch	32	MLBDIM_CFG_MLBC1	02F8 203Ch
80h	32	MLBDIM_CFG_HCTL	02F8 2080h
88h	32	MLBDIM_CFG_HCMR0	02F8 2088h
8Ch	32	MLBDIM_CFG_HCMR1	02F8 208Ch
90h	32	MLBDIM_CFG_HCER0	02F8 2090h
94h	32	MLBDIM_CFG_HCER1	02F8 2094h
98h	32	MLBDIM_CFG_HCBR0	02F8 2098h
9Ch	32	MLBDIM_CFG_HCBR1	02F8 209Ch
C0h	32	MLBDIM_CFG_MDAT0	02F8 20C0h
C4h	32	MLBDIM_CFG_MDAT1	02F8 20C4h
C8h	32	MLBDIM_CFG_MDAT2	02F8 20C8h
CCh	32	MLBDIM_CFG_MDAT3	02F8 20CCh
D0h	32	MLBDIM_CFG_MDWE0	02F8 20D0h
D4h	32	MLBDIM_CFG_MDWE1	02F8 20D4h
D8h	32	MLBDIM_CFG_MDWE2	02F8 20D8h
DCh	32	MLBDIM_CFG_MDWE3	02F8 20DCh
E0h	32	MLBDIM_CFG_MCTL	02F8 20E0h
E4h	32	MLBDIM_CFG_MADR	02F8 20E4h
FCh	32	MLBDIM_CFG_PID	02F8 20FCh
3C0h	32	MLBDIM_CFG_ACTL	02F8 23C0h
3D0h	32	MLBDIM_CFG_ACSR0	02F8 23D0h
3D4h	32	MLBDIM_CFG_ACSR1	02F8 23D4h
3D8h	32	MLBDIM_CFG_ACMR0	02F8 23D8h
3DCh	32	MLBDIM_CFG_ACMR1	02F8 23DCh

Table 14-10427. RAT Registers, Base Address=02F8 3000h, Length=4096

Offset	Length	Register Name	MLB0 Physical Address
0h	32	RAT_PID	02F8 3000h
4h	32	RAT_CONFIG	02F8 3004h
804h	32	RAT_DESTINATION_ID	02F8 3804h
820h	32	RAT_EXCEPTION_LOGGING_CONTROL	02F8 3820h
824h	32	RAT_EXCEPTION_LOGGING_HEADER0	02F8 3824h
828h	32	RAT_EXCEPTION_LOGGING_HEADER1	02F8 3828h
82Ch	32	RAT_EXCEPTION_LOGGING_DATA0	02F8 382Ch
830h	32	RAT_EXCEPTION_LOGGING_DATA1	02F8 3830h
834h	32	RAT_EXCEPTION_LOGGING_DATA2	02F8 3834h
838h	32	RAT_EXCEPTION_LOGGING_DATA3	02F8 3838h
840h	32	RAT_EXCEPTION_PEND_SET	02F8 3840h
844h	32	RAT_EXCEPTION_PEND_CLEAR	02F8 3844h
848h	32	RAT_EXCEPTION_ENABLE_SET	02F8 3848h
84Ch	32	RAT_EXCEPTION_ENABLE_CLEAR	02F8 384Ch
850h	32	RAT_EOI_REG	02F8 3850h
20h	32	RAT_REGION_CTRL_J	02F8 3020h + formula
24h	32	RAT_REGION_BASE_J	02F8 3024h + formula
28h	32	RAT_REGION_TRANS_L_J	02F8 3028h + formula
2Ch	32	RAT_REGION_TRANS_U_J	02F8 302Ch + formula

Table 14-10428. ECC_AGGR Registers, Base Address=072A 0000h, Length=1024

Offset	Length	Register Name	MLB0 Physical Address
0h	32	ECC_AGGR_REV	072A 0000h
8h	32	ECC_AGGR_VECTOR	072A 0008h
Ch	32	ECC_AGGR_STAT	072A 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	072A 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	072A 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	072A 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	072A 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	072A 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	072A 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	072A 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	072A 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	072A 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	072A 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	072A 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	072A 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	072A 020Ch

14.7.1.4.2 MLB Registers

MLB Registers

14.7.1.4.2.1 MLBSS_CFG_PID Register

14.7.1.4.2.1.1 MLBSS_CFG_PID Register (Offset = 0h) [reset = 68D09A00h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-10429. Instance Table

Instance Name	Physical Address
MLB0	02F8 0000h

Figure 14-5156. mlbss_cfg_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		8D0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
8D0h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
13h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-10430. mlbss_cfg_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: psrst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: psrst_n
27:16	MODULE_ID	R	8D0h	Module ID Reset Source: psrst_n
15:11	RTL	R	13h	RTL revision. Will vary depending on release. Reset Source: psrst_n
10:8	MAJOR	R	2h	Major revision Reset Source: psrst_n
7:6	CUSTOM	R	0h	Custom Reset Source: psrst_n
5:0	MINOR	R	0h	Minor revision Reset Source: psrst_n

14.7.1.4.2.2 MLBSS_CFG_STAT Register

14.7.1.4.2.2.1 MLBSS_CFG_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the mlbss

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Table 14-10431. Instance Table

Instance Name	Physical Address
MLB0	02F8 0008h

Figure 14-5157. mlbss_cfg_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_INIT_DONE	RESERVED
NONE						R	NONE
0h						0h	0h

Table 14-10432. mlbss_cfg_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_INIT_DONE	R	0h	0:Memory Initialization is in progress, 1:Memory Intialization Done Reset Source: psrst_n
0	RESERVED	NONE	0h	Reserved

14.7.1.4.2.3 MLBSS_CFG_DMA_CTRL Register

14.7.1.4.2.3.1 MLBSS_CFG_DMA_CTRL Register (Offset = Ch) [reset = 0h]

The DMA Control register provide control bits for the DMA Vbusp

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Table 14-10433. Instance Table

Instance Name	Physical Address
MLB0	02F8 000Ch

Figure 14-5158. mlbss_cfg_DMA_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PRIORITY		
NONE					R/W		
0h					0h		

Table 14-10434. mlbss_cfg_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PRIORITY	R/W	0h	DMA Vbusp priority Reset Source: psrst_n

14.7.1.4.2.4 MLBDIM_CFG_MLBC0 Register

14.7.1.4.2.4.1 MLBDIM_CFG_MLBC0 Register (Offset = 0h) [reset = 0h]

See reference [R1].

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Table 14-10435. Instance Table

Instance Name	Physical Address
MLB0	02F8 2000h

Figure 14-5159. mlbdim_cfg_MLBC0 Name Register

31	30	29	28	27	26	25	24
RSV4							
R							
0h							
23	22	21	20	19	18	17	16
RSV4						FCNT	
R						R/W	
0h						0h	
15	14	13	12	11	10	9	8
FCNT	CTLRETRY	RSV3	ASYRETRY	RSV2			
R/W	R/W	R	R/W	R			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
MLBLK	RSV1	MLBPEN	MLBCLK			RSV0	MLBEN
R	R	R/W	R/W			R	R/W
0h	0h	0h	0h			0h	0h

Table 14-10436. mlbdim_cfg_MLBC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RSV4	R	0h	Reserved Reset Source: prst_n
17:15	FCNT	R/W	0h	The number of frames per sub-buffer for synchronous channels. 000 - 1 frame per sub-buffer (Operation is the same as Standard mode) 001 - 2 frames per sub-buffer 010 - 4 frames per sub-buffer 011 - 8 frames per sub-buffer 100 - 16 frames per sub-buffer 101 - 32 frames per sub-buffer 110 - 64 frames per sub-buffer 111 - Reserved Reset Source: prst_n
14	CTLRETRY	R/W	0h	Control Tx packet retry. When set, a control packet that is flagged with a Break or ProtocolError by the receiver is retransmitted. When cleared, a control packet that is flagged with a Break or ProtocolError by the receiver is skipped. Reset Source: prst_n
13	RSV3	R	0h	Reserved Reset Source: prst_n
12	ASYRETRY	R/W	0h	Asynchronous Tx packet retry. When set, an asynchronous packet that is flagged with a Break or ProtocolError by the receiver is retransmitted. When cleared, an asynchronous packet that is flagged with a Break or ProtocolError by the receiver is skipped. Reset Source: prst_n
11:8	RSV2	R	0h	Reserved Reset Source: prst_n

Table 14-10436. mlbdim_cfg_MLBC0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	MLBLK	R	0h	MediaLB lock status. When set, indicates that the MediaLB block is synchronized to the incoming MediaLB frame. If MLBLK is clear (unlocked), MLBLK is set after FRAMESYNC is detected at the same position for three consecutive frames. If MLBLK is set (locked), MLBLK is cleared after not receiving FRAMESYNC at the expected time for two consecutive frames. While MLBLK is set, FRAMESYNC patterns occurring at locations other than the expected one are ignored. (read-only) Reset Source: prst_n
6	RSV1	R	0h	Reserved Reset Source: prst_n
5	MLBPEN	R/W	0h	MediaLB 6-pin enable. 0 - MediaLB 3-pin interface enabled 1 - MediaLB 6-pin interface enabled Reset Source: prst_n
4:2	MLBCLK	R/W	0h	MediaLB clock speed select. 000 - 256xFs (for MLBPEN = 0) 001 - 512xFs (for MLBPEN = 0) 010 - 1024xFs (for MLBPEN = 0) 011 - 2048xFs (for MLBPEN = 1) 100 - 3072xFs (for MLBPEN = 1) 101 - 4096xFs (for MLBPEN = 1) 110 - 6144xFs (for MLBPEN = 1) 111 - 8192xFs (for MLBPEN = 1) Reset Source: prst_n
1	RSV0	R	0h	Reserved Reset Source: prst_n
0	MLBEN	R/W	0h	MediaLB enable. When set, MediaLB clock, signal, and data are received and transmitted on the appropriate MediaLB pins. Reset Source: prst_n

14.7.1.4.2.5 MLBDIM_CFG_MLBPC0 Register

14.7.1.4.2.5.1 MLBDIM_CFG_MLBPC0 Register (Offset = 8h) [reset = 0h]

See reference [R1].

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Table 14-10437. Instance Table

Instance Name	Physical Address
MLB0	02F8 2008h

Figure 14-5160. mlbdim_cfg_MLBPC0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSV2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSV2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RSV2</td><td>MCLKHYS</td><td colspan="3">RSV1</td></tr>
<tr><td colspan="4">R</td><td>R/W</td><td colspan="3">R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RSV1</td><td>MLBCMRES</td><td>RSV0</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10438. mlbdim_cfg_MLBPC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RSV2	R	0h	Reserved Reset Source: prst_n
11	MCLKHYS	R/W	0h	MediaLB 6-pin clock hystersis enable. When set, enables hysteresis on the MediaLB clock. This value is driven on mlb_clk_hys_enable output pin and has no internal function. Reset Source: prst_n
10:2	RSV1	R	0h	Reserved Reset Source: prst_n
1	MLBCMRES	R/W	0h	MediaLB 6-pin common mode resistor enable. No longer used Reset Source: prst_n
0	RSV0	R	0h	Reserved Reset Source: prst_n

14.7.1.4.2.6 MLBDIM_CFG_MS0 Register

14.7.1.4.2.6.1 MLBDIM_CFG_MS0 Register (Offset = Ch) [reset = 0h]

See reference [R1].

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Table 14-10439. Instance Table

Instance Name	Physical Address
MLB0	02F8 200Ch

Figure 14-5161. mlbdim_cfg_MS0 Name Register

31	30	29	28	27	26	25	24
MCS							
R/W0TC							
0h							
23	22	21	20	19	18	17	16
MCS							
R/W0TC							
0h							
15	14	13	12	11	10	9	8
MCS							
R/W0TC							
0h							
7	6	5	4	3	2	1	0
MCS							
R/W0TC							
0h							

Table 14-10440. mlbdim_cfg_MS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCS	R/W0TC	0h	MediaLB channel status. Indicates the channel status for MediaLB channels 31 to 0. Channel status bits are set by hardware and cleared by software. Status is only set if the appropriate bits in the MIEN register are set. Reset Source: prst_n

14.7.1.4.2.7 MLBDIM_CFG_MS1 Register

14.7.1.4.2.7.1 MLBDIM_CFG_MS1 Register (Offset = 14h) [reset = 0h]

See reference [R1].

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Table 14-10441. Instance Table

Instance Name	Physical Address
MLB0	02F8 2014h

Figure 14-5162. mlbdim_cfg_MS1 Name Register

31	30	29	28	27	26	25	24
MCS							
R/W0TC							
0h							
23	22	21	20	19	18	17	16
MCS							
R/W0TC							
0h							
15	14	13	12	11	10	9	8
MCS							
R/W0TC							
0h							
7	6	5	4	3	2	1	0
MCS							
R/W0TC							
0h							

Table 14-10442. mlbdim_cfg_MS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MCS	R/W0TC	0h	MediaLB channel status. Indicates the channel status for MediaLB channels 63 to 32. Channel status bits are set by hardware and cleared by software. Status is only set if the appropriate bits in the MIEN register are set. Reset Source: prst_n

14.7.1.4.2.8 MLBDIM_CFG_MSS Register

14.7.1.4.2.8.1 MLBDIM_CFG_MSS Register (Offset = 20h) [reset = 0h]

See reference [R1].

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Table 14-10443. Instance Table

Instance Name	Physical Address
MLB0	02F8 2020h

Figure 14-5163. mlbdim_cfg_MSS Name Register

31	30	29	28	27	26	25	24
RSV0							
R							
0h							
23	22	21	20	19	18	17	16
RSV0							
R							
0h							
15	14	13	12	11	10	9	8
RSV0							
R							
0h							
7	6	5	4	3	2	1	0
RSV0		SERVREQ	SWSYSCMD	CSSYSCMD	ULKSYSCMD	LKSYSCMD	RSTSYSCMD
R		R/W	R/W0TC	R/W0TC	R/W0TC	R/W0TC	R/W0TC
0h		0h	0h	0h	0h	0h	0h

Table 14-10444. mlbdim_cfg_MSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RSV0	R	0h	Reserved Reset Source: prst_n
5	SERVREQ	R/W	0h	Service request enabled. When set, the MediaLB block responds with a "device present, request service" system response if a matching channel scan system command is detected. When cleared, the MediaLB block responds with a "device present" system response. Reset Source: prst_n
4	SWSYSCMD	R/W0TC	0h	Sowftware system command detected (in the system quadlet). Set by hardware, cleared by software. Data is stored in the MSD register for this command. Reset Source: prst_n
3	CSSYSCMD	R/W0TC	0h	Channel scan system command detected (in the system quadlet). Set by hardware, cleared by software. If the node address specified in Data quadlet matches the value in MLBC1.NDA, the device responds either "device present" or "device present, request service" system response in the next system quadlet. Reset Source: prst_n
2	ULKSYSCMD	R/W0TC	0h	Network unlock system command detected (in the system quadlet). Set by hardware, cleared by software. Reset Source: prst_n

Table 14-10444. mlbdim_cfg_MSS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LKSYSCMD	R/W0TC	0h	Network lock system command detected (in the system quadlet). Set by hardware, cleared by software. Reset Source: prst_n
0	RSTSYSCMD	R/W0TC	0h	Reset system command detected (in the system quadlet). Set by hardware, cleared by software. Reset Source: prst_n

14.7.1.4.2.9 MLBDIM_CFG_MSD Register

14.7.1.4.2.9.1 MLBDIM_CFG_MSD Register (Offset = 24h) [reset = 0h]

See reference [R1].

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Table 14-10445. Instance Table

Instance Name	Physical Address
MLB0	02F8 2024h

Figure 14-5164. mlbdim_cfg_MSD Name Register

31	30	29	28	27	26	25	24
SD3							
R							
0h							
23	22	21	20	19	18	17	16
SD2							
R							
0h							
15	14	13	12	11	10	9	8
SD1							
R							
0h							
7	6	5	4	3	2	1	0
SD0							
R							
0h							

Table 14-10446. mlbdim_cfg_MSD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SD3	R	0h	System data (byte 3) - MSB. Updated with MediaLB Data[31:24] when a MediaLB software system command is received in the system quadlet. If MSS.SWSYSCMD is already set, then SD3 is not updated. (read-only) Reset Source: prst_n
23:16	SD2	R	0h	System data (byte 2). Updated with MediaLB Data[23:16] when a MediaLB software system command is received in the system quadlet. If MSS.SWSYSCMD is already set, then SD2 is not updated. (readonly) Reset Source: prst_n
15:8	SD1	R	0h	System data (byte 1). Updated with MediaLB Data[15:8] when a MediaLB software system command is received in the system quadlet. If MSS.SWSYSCMD is already set, then SD1 is not updated. (read-only) Reset Source: prst_n
7:0	SD0	R	0h	System data (byte 0) - LSB. Updated with MediaLB Data[7:0] when a MediaLB software system command is received in the system quadlet. If MSS.SWSYSCMD is already set, then SD0 is not updated. (readonly) Reset Source: prst_n

14.7.1.4.2.10 MLBDIM_CFG_MIEN Register

14.7.1.4.2.10.1 MLBDIM_CFG_MIEN Register (Offset = 2Ch) [reset = 0h]

See reference [R1].

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Table 14-10447. Instance Table

Instance Name	Physical Address
MLB0	02F8 202Ch

Figure 14-5165. mlbdim_cfg_MIEN Name Register

31	30	29	28	27	26	25	24
RSV2		CTX_BREAK	CTX_PE	CTX_DONE	CRX_BREAK	CRX_PE	CRX_DONE
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RSV1	ATX_BREAK	ATX_PE	ATX_DONE	ARX_BREAK	ARX_PE	ARX_DONE	SYNC_PE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RSV0							
R/W							
0h							
7	6	5	4	3	2	1	0
RSV0						ISOC_BUFO	ISOC_PE
R/W						R/W	R/W
0h						0h	0h

Table 14-10448. mlbdim_cfg_MIEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSV2	R/W	0h	Reserved (write default value) Reset Source: prst_n
29	CTX_BREAK	R/W	0h	Control Tx break enable. When set, a ReceiverBreak response received from the receiver on a control Tx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
28	CTX_PE	R/W	0h	Control Tx protocol error enable. When set, a ProtocolError generated by the receiver on a control Tx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
27	CTX_DONE	R/W	0h	Control Tx packet done enable. When set, a packet transmitted with no errors on a control Tx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
26	CRX_BREAK	R/W	0h	Control Rx break enable. When set, a ControlBreak command received from the transmitter on a control Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
25	CRX_PE	R/W	0h	Control Rx protocol error enable. When set, a packet received with no errors on a control Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n

Table 14-10448. mlbdim_cfg_MIEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CRX_DONE	R/W	0h	Control Rx packet done enable. When set, a packet received with no errors on a control Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
23	RSV1	R/W	0h	Reserved (write default value) Reset Source: prst_n
22	ATX_BREAK	R/W	0h	Asynchronous Tx break enable. When set, a ReceiverBreak response received from the receiver on an asynchronous Tx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
21	ATX_PE	R/W	0h	Asynchronous Tx protocol error enable. When set, a ProtocolError generated by the receiver on an asynchronous Tx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
20	ATX_DONE	R/W	0h	Asynchronous Tx packet done enable. When set, a packet transmitted with no errors on an asynchronous Tx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
19	ARX_BREAK	R/W	0h	Asynchronous Rx break enable. When set, a AsyncBreak command received from the transmitter on an asynchronous Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
18	ARX_PE	R/W	0h	Asynchronous Rx protocol enable. When set, a ProtocolError detected on an asynchronous Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
17	ARX_DONE	R/W	0h	Asynchronous Rx packet done enable. When set, a packet received with no errors on an asynchronous Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
16	SYNC_PE	R/W	0h	Synchronous protocol error enable. When set, a ProtocolError detected on a synchronous Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n
15:2	RSV0	R/W	0h	Reserved (write default value) Reset Source: prst_n
1	ISOC_BUFO	R/W	0h	Isochronous Rx buffer overflow enable. When set, a buffer overflow on an isochronous Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. This occurs only when isochronous flow control is disabled. Reset Source: prst_n
0	ISOC_PE	R/W	0h	Isochronous Rx protocol error enable. When set, a ProtocolError detected on an isochronous Rx channel causes the appropriate channel bit in the MS0 or MS1 registers to be set. Reset Source: prst_n

14.7.1.4.2.11 MLBDIM_CFG_MLBPC2 Register

14.7.1.4.2.11.1 MLBDIM_CFG_MLBPC2 Register (Offset = 34h) [reset = 0h]

See reference [R1].

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Table 14-10449. Instance Table

Instance Name	Physical Address
MLB0	02F8 2034h

Figure 14-5166. mlbdim_cfg_MLBPC2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSV0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSV0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">UCFG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">UCFG</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10450. mlbdim_cfg_MLBPC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSV0	R	0h	Reserved Reset Source: prst_n
15:0	UCFG	R/W	0h	User Defined Configuration Register. This 16-bit register is output to the MediaLB physical interface (mlbp_user_cfg[15:0]) for additional control of external modules (i.e MediaLB 6-pin Analog module). Reset Source: prst_n

14.7.1.4.2.12 MLBDIM_CFG_MLBPC1 Register

14.7.1.4.2.12.1 MLBDIM_CFG_MLBPC1 Register (Offset = 38h) [reset = 0h]

See reference [R1].

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Table 14-10451. Instance Table

Instance Name	Physical Address
MLB0	02F8 2038h

Figure 14-5167. mlbdim_cfg_MLBPC1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSV0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSV0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RSV0</td><td colspan="4">CKRCVBIAS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SDXMTBIAS</td><td colspan="4">SDRCVBIAS</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-10452. mlbdim_cfg_MLBPC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RSV0	R	0h	Reserved Reset Source: prst_n
11:8	CKRCVBIAS	R/W	0h	Clock receiver bias control (for MediaLB 6-pin interface). This value is driven on mlb_clk_rx_bias_ctl[3:0] output pin and has no internal function. Reset Source: prst_n
7:4	SDXMTBIAS	R/W	0h	Signal/Data transmitter bias control (for MediaLB 6-pin interface). This value is driven on mlb_sig_data_tx_bias_ctl[3:0] output pin and has no internal function. Reset Source: prst_n
3:0	SDRCVBIAS	R/W	0h	Signal/Data reciever bias control (for MediaLB 6-pin interface). This value is driven on mlb_sig_data_rx_bias_ctl[3:0] output pin and has no internal function. Reset Source: prst_n

14.7.1.4.2.13 MLBDIM_CFG_MLBC1 Register

14.7.1.4.2.13.1 MLBDIM_CFG_MLBC1 Register (Offset = 3Ch) [reset = 0h]

See reference [R1].

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Table 14-10453. Instance Table

Instance Name	Physical Address
MLB0	02F8 203Ch

Figure 14-5168. mlbdim_cfg_MLBC1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSV1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSV1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NDA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CLKM</td><td>LOCK</td><td colspan="6">RSV0</td></tr>
<tr><td>R/W0TC</td><td>R/W0TC</td><td colspan="6">R</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-10454. mlbdim_cfg_MLBC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSV1	R	0h	Reserved Reset Source: prst_n
15:8	NDA	R/W	0h	Node device address. Used for system commands directed to individual MediaLB nodes. Reset Source: prst_n
7	CLKM	R/W0TC	0h	MediaLB clock missing status. Set when MediaLB clock is not toggling at the pin; cleared by software. Reset Source: prst_n
6	LOCK	R/W0TC	0h	MediaLB lock error status. Set when MediaLB is unlocked; cleared by software. Reset Source: prst_n
5:0	RSV0	R	0h	Reserved Reset Source: prst_n

14.7.1.4.2.14 MLBDIM_CFG_HCTL Register

14.7.1.4.2.14.1 MLBDIM_CFG_HCTL Register (Offset = 80h) [reset = 0h]

See reference [R1].

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Table 14-10455. Instance Table

Instance Name	Physical Address
MLB0	02F8 2080h

Figure 14-5169. mlbdim_cfg_HCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSV1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSV1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>EN</td><td colspan="7">RSV0</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RSV0</td><td>RST1</td><td>RST0</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10456. mlbdim_cfg_HCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSV1	R/W	0h	Reserved (write default value) Reset Source: prst_n
15	EN	R/W	0h	HBI enable: 1 = enabled, 0 = disabled Reset Source: prst_n
14:2	RSV0	R/W	0h	Reserved (write default value) Reset Source: prst_n
1	RST1	R/W	0h	AGU1 software reset: 1 = reset active, 0 = reset inactive Reset Source: prst_n
0	RST0	R/W	0h	AGU0 software reset: 1 = reset active, 0 = reset inactive Reset Source: prst_n

14.7.1.4.2.15 MLBDIM_CFG_HCMR0 Register

14.7.1.4.2.15.1 MLBDIM_CFG_HCMR0 Register (Offset = 88h) [reset = 0h]

See reference [R1].

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Table 14-10457. Instance Table

Instance Name	Physical Address
MLB0	02F8 2088h

Figure 14-5170. mlbdim_cfg_HCMR0 Name Register

31	30	29	28	27	26	25	24
CHM							
R/W							
0h							
23	22	21	20	19	18	17	16
CHM							
R/W							
0h							
15	14	13	12	11	10	9	8
CHM							
R/W							
0h							
7	6	5	4	3	2	1	0
CHM							
R/W							
0h							

Table 14-10458. mlbdim_cfg_HCMR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHM	R/W	0h	Bitwise channel mask bit [31:0]: 0 = masked, 1 = unmasked Reset Source: prst_n

14.7.1.4.2.16 MLBDIM_CFG_HCMR1 Register

14.7.1.4.2.16.1 MLBDIM_CFG_HCMR1 Register (Offset = 8Ch) [reset = 0h]

See reference [R1].

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Table 14-10459. Instance Table

Instance Name	Physical Address
MLB0	02F8 208Ch

Figure 14-5171. mlbdim_cfg_HCMR1 Name Register

31	30	29	28	27	26	25	24
CHM							
R/W							
0h							
23	22	21	20	19	18	17	16
CHM							
R/W							
0h							
15	14	13	12	11	10	9	8
CHM							
R/W							
0h							
7	6	5	4	3	2	1	0
CHM							
R/W							
0h							

Table 14-10460. mlbdim_cfg_HCMR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHM	R/W	0h	Bitwise channel mask bit [63:32]: 0 = masked, 1 = unmasked Reset Source: prst_n

14.7.1.4.2.17 MLBDIM_CFG_HCER0 Register

14.7.1.4.2.17.1 MLBDIM_CFG_HCER0 Register (Offset = 90h) [reset = 0h]

See reference [R1].

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Table 14-10461. Instance Table

Instance Name	Physical Address
MLB0	02F8 2090h

Figure 14-5172. mlbdim_cfg_HCER0 Name Register

31	30	29	28	27	26	25	24
CERR							
R/W0TC							
0h							
23	22	21	20	19	18	17	16
CERR							
R/W0TC							
0h							
15	14	13	12	11	10	9	8
CERR							
R/W0TC							
0h							
7	6	5	4	3	2	1	0
CERR							
R/W0TC							
0h							

Table 14-10462. mlbdim_cfg_HCER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CERR	R/W0TC	0h	Bitwise channel error bit[31:0] Reset Source: prst_n

14.7.1.4.2.18 MLBDIM_CFG_HCER1 Register

14.7.1.4.2.18.1 MLBDIM_CFG_HCER1 Register (Offset = 94h) [reset = 0h]

See reference [R1].

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Table 14-10463. Instance Table

Instance Name	Physical Address
MLB0	02F8 2094h

Figure 14-5173. mlbdim_cfg_HCER1 Name Register

31	30	29	28	27	26	25	24
CERR							
R/W0TC							
0h							
23	22	21	20	19	18	17	16
CERR							
R/W0TC							
0h							
15	14	13	12	11	10	9	8
CERR							
R/W0TC							
0h							
7	6	5	4	3	2	1	0
CERR							
R/W0TC							
0h							

Table 14-10464. mlbdim_cfg_HCER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CERR	R/W0TC	0h	Bitwise channel error bit[63:32] Reset Source: prst_n

14.7.1.4.2.19 MLBDIM_CFG_HCBR0 Register

14.7.1.4.2.19.1 MLBDIM_CFG_HCBR0 Register (Offset = 98h) [reset = 0h]

See reference [R1].

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Table 14-10465. Instance Table

Instance Name	Physical Address
MLB0	02F8 2098h

Figure 14-5174. mlbdim_cfg_HCBR0 Name Register

31	30	29	28	27	26	25	24
CHB							
R							
0h							
23	22	21	20	19	18	17	16
CHB							
R							
0h							
15	14	13	12	11	10	9	8
CHB							
R							
0h							
7	6	5	4	3	2	1	0
CHB							
R							
0h							

Table 14-10466. mlbdim_cfg_HCBR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHB	R	0h	Bitwise channel busy bit[31:0]: 0 = idle, 1 = busy Reset Source: prst_n

14.7.1.4.2.20 MLBDIM_CFG_HCBR1 Register

14.7.1.4.2.20.1 MLBDIM_CFG_HCBR1 Register (Offset = 9Ch) [reset = 0h]

See reference [R1].

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Table 14-10467. Instance Table

Instance Name	Physical Address
MLB0	02F8 209Ch

Figure 14-5175. mlbdim_cfg_HCBR1 Name Register

31	30	29	28	27	26	25	24
CHB							
R							
0h							
23	22	21	20	19	18	17	16
CHB							
R							
0h							
15	14	13	12	11	10	9	8
CHB							
R							
0h							
7	6	5	4	3	2	1	0
CHB							
R							
0h							

Table 14-10468. mlbdim_cfg_HCBR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHB	R	0h	Bitwise channel busy bit[63:32]: 0 = idle, 1 = busy Reset Source: prst_n

14.7.1.4.2.21 MLBDIM_CFG_MDAT0 Register

14.7.1.4.2.21.1 MLBDIM_CFG_MDAT0 Register (Offset = C0h) [reset = 0h]

See reference [R1].

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Table 14-10469. Instance Table

Instance Name	Physical Address
MLB0	02F8 20C0h

Figure 14-5176. mlbdim_cfg_MDAT0 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-10470. mlbdim_cfg_MDAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	CTR data - bits[31:0] of 128-bit entry or DBR data - bits[7:0] of 8-bit entry Reset Source: prst_n

14.7.1.4.2.22 MLBDIM_CFG_MDAT1 Register

14.7.1.4.2.22.1 MLBDIM_CFG_MDAT1 Register (Offset = C4h) [reset = 0h]

See reference [R1].

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Table 14-10471. Instance Table

Instance Name	Physical Address
MLB0	02F8 20C4h

Figure 14-5177. mlbdim_cfg_MDAT1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10472. mlbdim_cfg_MDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	CTR data - bits[63:32] of 128-bit entry Reset Source: prst_n

14.7.1.4.2.23 MLBDIM_CFG_MDAT2 Register

14.7.1.4.2.23.1 MLBDIM_CFG_MDAT2 Register (Offset = C8h) [reset = 0h]

See reference [R1].

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Table 14-10473. Instance Table

Instance Name	Physical Address
MLB0	02F8 20C8h

Figure 14-5178. mlbdim_cfg_MDAT2 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-10474. mlbdim_cfg_MDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	CTR data - bits[95:64] of 128-bit entry Reset Source: prst_n

14.7.1.4.2.24 MLBDIM_CFG_MDAT3 Register

14.7.1.4.2.24.1 MLBDIM_CFG_MDAT3 Register (Offset = CCh) [reset = 0h]

See reference [R1].

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Table 14-10475. Instance Table

Instance Name	Physical Address
MLB0	02F8 20CCh

Figure 14-5179. mlbdim_cfg_MDAT3 Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-10476. mlbdim_cfg_MDAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	CTR data - bits[127:96] of 128-bit entry Reset Source: prst_n

14.7.1.4.2.25 MLBDIM_CFG_MDWE0 Register

14.7.1.4.2.25.1 MLBDIM_CFG_MDWE0 Register (Offset = D0h) [reset = 0h]

See reference [R1].

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Table 14-10477. Instance Table

Instance Name	Physical Address
MLB0	02F8 20D0h

Figure 14-5180. mlbdim_cfg_MDWE0 Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 14-10478. mlbdim_cfg_MDWE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	Bitwise write enable for CTR data - bits[31:0] (0 = disabled, 1 = enabled) Reset Source: prst_n

14.7.1.4.2.26 MLBDIM_CFG_MDWE1 Register

14.7.1.4.2.26.1 MLBDIM_CFG_MDWE1 Register (Offset = D4h) [reset = 0h]

See reference [R1].

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Table 14-10479. Instance Table

Instance Name	Physical Address
MLB0	02F8 20D4h

Figure 14-5181. mlbdim_cfg_MDWE1 Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 14-10480. mlbdim_cfg_MDWE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	Bitwise write enable for CTR data - bits[63:32] (0 = disabled, 1 = enabled) Reset Source: prst_n

14.7.1.4.2.27 MLBDIM_CFG_MDWE2 Register

14.7.1.4.2.27.1 MLBDIM_CFG_MDWE2 Register (Offset = D8h) [reset = 0h]

See reference [R1].

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Table 14-10481. Instance Table

Instance Name	Physical Address
MLB0	02F8 20D8h

Figure 14-5182. mlbdim_cfg_MDWE2 Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 14-10482. mlbdim_cfg_MDWE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	Bitwise write enable for CTR data - bits[95:64] (0 = disabled, 1 = enabled) Reset Source: prst_n

14.7.1.4.2.28 MLBDIM_CFG_MDWE3 Register

14.7.1.4.2.28.1 MLBDIM_CFG_MDWE3 Register (Offset = DCh) [reset = 0h]

See reference [R1].

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Table 14-10483. Instance Table

Instance Name	Physical Address
MLB0	02F8 20DCh

Figure 14-5183. mlbdim_cfg_MDWE3 Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 14-10484. mlbdim_cfg_MDWE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	Bitwise write enable for CTR data - bits[127:96] (0 = disabled, 1 = enabled) Reset Source: prst_n

14.7.1.4.2.29 MLBDIM_CFG_MCTL Register

14.7.1.4.2.29.1 MLBDIM_CFG_MCTL Register (Offset = E0h) [reset = 0h]

See reference [R1].

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Table 14-10485. Instance Table

Instance Name	Physical Address
MLB0	02F8 20E0h

Figure 14-5184. mlbdim_cfg_MCTL Name Register

31	30	29	28	27	26	25	24
RSV0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSV0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSV0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSV0							XCMP
R/W							R/W0TC
0h							0h

Table 14-10486. mlbdim_cfg_MCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RSV0	R/W	0h	Reserved (write default value) Reset Source: prst_n
0	XCMP	R/W0TC	0h	Transfer complete (write 0 to clear) Reset Source: prst_n

14.7.1.4.2.30 MLBDIM_CFG_MADR Register

14.7.1.4.2.30.1 MLBDIM_CFG_MADR Register (Offset = E4h) [reset = 0h]

See reference [R1].

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Table 14-10487. Instance Table

Instance Name	Physical Address
MLB0	02F8 20E4h

Figure 14-5185. mlbdim_cfg_MADR Name Register

31	30	29	28	27	26	25	24
WNR	TB	RSV0					
R/W	R/W	R/W					
0h	0h	0h					
23	22	21	20	19	18	17	16
RSV0							
R/W							
0h							
15	14	13	12	11	10	9	8
RSV0		ADDR1					
R/W		R/W					
0h		0h					
7	6	5	4	3	2	1	0
ADDR0							
R/W							
0h							

Table 14-10488. mlbdim_cfg_MADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WNR	R/W	0h	Write-Not-Read selection (0 = read, 1 = write) Reset Source: prst_n
30	TB	R/W	0h	Target location bit (0 = selects CTR, 1 = selects DBR) Reset Source: prst_n
29:14	RSV0	R/W	0h	Reserved (write default value) Reset Source: prst_n
13:8	ADDR1	R/W	0h	DBR address of 8-bit entry - bits[13:8] Reset Source: prst_n
7:0	ADDR0	R/W	0h	CTR address of 128-bit entry or DBR address of 8-bit entry - bits[7:0] Reset Source: prst_n

14.7.1.4.2.31 MLBDIM_CFG_PID Register

14.7.1.4.2.31.1 MLBDIM_CFG_PID Register (Offset = FCh) [reset = 0h]

Microchip 3rd party MediaLB Device Interface Macro 2 soft IP core revision register.

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Table 14-10489. Instance Table

Instance Name	Physical Address
MLB0	02F8 20FCh

Figure 14-5186. mlbdim_cfg_PID Name Register

31	30	29	28	27	26	25	24
RSV0							
R							
0h							
23	22	21	20	19	18	17	16
RSV0							
R							
0h							
15	14	13	12	11	10	9	8
MAJOR							
R							
0h							
7	6	5	4	3	2	1	0
MINOR							
R							
0h							

Table 14-10490. mlbdim_cfg_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSV0	R	0h	Reserved Reset Source: prst_n
15:8	MAJOR	R	0h	Major revision Reset Source: prst_n
7:0	MINOR	R	0h	Minor revision Reset Source: prst_n

14.7.1.4.2.32 MLBDIM_CFG_ACTL Register

14.7.1.4.2.32.1 MLBDIM_CFG_ACTL Register (Offset = 3C0h) [reset = 0h]

See reference [R1].

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Table 14-10491. Instance Table

Instance Name	Physical Address
MLB0	02F8 23C0h

Figure 14-5187. mlbdim_cfg_ACTL Name Register

31	30	29	28	27	26	25	24
RSV1							
R/W							
0h							
23	22	21	20	19	18	17	16
RSV1							
R/W							
0h							
15	14	13	12	11	10	9	8
RSV1							
R/W							
0h							
7	6	5	4	3	2	1	0
RSV1			MPB	RSV0	DMAMODE	SMX	SCE
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-10492. mlbdim_cfg_ACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RSV1	R/W	0h	Reserved (write default value) Reset Source: prst_n
4	MPB	R/W	0h	Packet buffering mode: 0 = single-packet mode 1 = multiple-packet mode Reset Source: prst_n
3	RSV0	R/W	0h	Reserved (write default value) Reset Source: prst_n
2	DMAMODE	R/W	0h	DMA Mode: 0 = DMA Mode 0 1 = DMA Mode 1 Reset Source: prst_n
1	SMX	R/W	0h	AHB interrupt mux enable: 0 = ACSR0 generates an interrupt on ahb_int[0]; ACSR1 generates an interrupt on ahb_int[1] 1 = ACSR0 and ACSR1 generate an interrupts on ahb_int[0] only Reset Source: prst_n
0	SCE	R/W	0h	Software clear enable: 0 = Hardware clears interrupt after a ACSRn register read 1 = Software clears interrupt Reset Source: prst_n

14.7.1.4.2.33 MLBDIM_CFG_ACSR0 Register

14.7.1.4.2.33.1 MLBDIM_CFG_ACSR0 Register (Offset = 3D0h) [reset = 0h]

See reference [R1].

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Table 14-10493. Instance Table

Instance Name	Physical Address
MLB0	02F8 23D0h

Figure 14-5188. mlbdim_cfg_ACSR0 Name Register

31	30	29	28	27	26	25	24
CHS							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CHS							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CHS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CHS							
R/W1TC							
0h							

Table 14-10494. mlbdim_cfg_ACSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHS	R/W1TC	0h	Interrupt status for logical channels 31 to 0: 0 = None 1 = Interrupt Reset Source: prst_n

14.7.1.4.2.34 MLBDIM_CFG_ACSR1 Register

14.7.1.4.2.34.1 MLBDIM_CFG_ACSR1 Register (Offset = 3D4h) [reset = 0h]

See reference [R1].

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Table 14-10495. Instance Table

Instance Name	Physical Address
MLB0	02F8 23D4h

Figure 14-5189. mlbdim_cfg_ACSR1 Name Register

31	30	29	28	27	26	25	24
CHS							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CHS							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CHS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CHS							
R/W1TC							
0h							

Table 14-10496. mlbdim_cfg_ACSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHS	R/W1TC	0h	Interrupt status for logical channels 63 to 32: 0 = None 1 = Interrupt Reset Source: prst_n

14.7.1.4.2.35 MLBDIM_CFG_ACMR0 Register

14.7.1.4.2.35.1 MLBDIM_CFG_ACMR0 Register (Offset = 3D8h) [reset = 0h]

See reference [R1].

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Table 14-10497. Instance Table

Instance Name	Physical Address
MLB0	02F8 23D8h

Figure 14-5190. mlbdim_cfg_ACMR0 Name Register

31	30	29	28	27	26	25	24
CHM							
R/W							
0h							
23	22	21	20	19	18	17	16
CHM							
R/W							
0h							
15	14	13	12	11	10	9	8
CHM							
R/W							
0h							
7	6	5	4	3	2	1	0
CHM							
R/W							
0h							

Table 14-10498. mlbdim_cfg_ACMR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHM	R/W	0h	Bitwise channel mask bit[31:0]: 0 = Masked 1 = Unmasked Reset Source: prst_n

14.7.1.4.2.36 MLBDIM_CFG_ACMR1 Register

14.7.1.4.2.36.1 MLBDIM_CFG_ACMR1 Register (Offset = 3DCh) [reset = 0h]

See reference [R1].

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Table 14-10499. Instance Table

Instance Name	Physical Address
MLB0	02F8 23DCh

Figure 14-5191. mlbdim_cfg_ACMR1 Name Register

31	30	29	28	27	26	25	24
CHM							
R/W							
0h							
23	22	21	20	19	18	17	16
CHM							
R/W							
0h							
15	14	13	12	11	10	9	8
CHM							
R/W							
0h							
7	6	5	4	3	2	1	0
CHM							
R/W							
0h							

Table 14-10500. mlbdim_cfg_ACMR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CHM	R/W	0h	Bitwise channel mask bit[63:32]: 0 = Masked 1 = Unmasked Reset Source: prst_n

14.7.1.4.2.37 RAT_PID Register

14.7.1.4.2.37.1 RAT_PID Register (Offset = 0h) [reset = 66803100h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-10501. Instance Table

Instance Name	Physical Address
MLB0	02F8 3000h

Figure 14-5192. rat_pid Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		680h			
23	22	21	20	19	18	17	16
FUNC							
R							
680h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-10502. rat_pid Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: mod_g_rst_n
27:16	FUNC	R	680h	Module ID Reset Source: mod_g_rst_n
15:11	RTL	R	6h	RTL revision. Will vary depending on release. Reset Source: mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: mod_g_rst_n

14.7.1.4.2.38 RAT_CONFIG Register

14.7.1.4.2.38.1 RAT_CONFIG Register (Offset = 4h) [reset = 300140h]

The Config Register contains the configuration values for the module.

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Table 14-10503. Instance Table

Instance Name	Physical Address
MLB0	02F8 3004h

Figure 14-5193. rat_config Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
ADDR_WIDTH							
R							
30h							
15	14	13	12	11	10	9	8
ADDRS							
R							
1h							
7	6	5	4	3	2	1	0
REGIONS							
R							
40h							

Table 14-10504. rat_config Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	ADDR_WIDTH	R	30h	Number of address bits Reset Source: mod_g_rst_n
15:8	ADDRS	R	1h	Number of addresses Reset Source: mod_g_rst_n
7:0	REGIONS	R	40h	Number of regions Reset Source: mod_g_rst_n

14.7.1.4.2.39 RAT_DESTINATION_ID Register

14.7.1.4.2.39.1 RAT_DESTINATION_ID Register (Offset = 804h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 14-10505. Instance Table

Instance Name	Physical Address
MLB0	02F8 3804h

Figure 14-5194. rat_destination_id Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 14-10506. rat_destination_id Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID. Reset Source: mod_g_rst_n

14.7.1.4.2.40 RAT_EXCEPTION_LOGGING_CONTROL Register

14.7.1.4.2.40.1 RAT_EXCEPTION_LOGGING_CONTROL Register (Offset = 820h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 14-10507. Instance Table

Instance Name	Physical Address
MLB0	02F8 3820h

Figure 14-5195. rat_exception_logging_control Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 14-10508. rat_exception_logging_control Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set. Reset Source: mod_g_rst_n
0	DISABLE_F	R/W	0h	Disables logging when set. Reset Source: mod_g_rst_n

14.7.1.4.2.41 RAT_EXCEPTION_LOGGING_HEADER0 Register

14.7.1.4.2.41.1 RAT_EXCEPTION_LOGGING_HEADER0 Register (Offset = 824h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 14-10509. Instance Table

Instance Name	Physical Address
MLB0	02F8 3824h

Figure 14-5196. rat_exception_logging_header0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 14-10510. rat_exception_logging_header0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 4 = RAT. Reset Source: mod_g_rst_n
23:8	SRC_ID	R	0h	Source ID. Reset Source: mod_g_rst_n
7:0	DEST_ID	R	0h	Destination ID. Reset Source: mod_g_rst_n

14.7.1.4.2.42 RAT_EXCEPTION_LOGGING_HEADER1 Register

14.7.1.4.2.42.1 RAT_EXCEPTION_LOGGING_HEADER1 Register (Offset = 828h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 14-10511. Instance Table

Instance Name	Physical Address
MLB0	02F8 3828h

Figure 14-5197. rat_exception_logging_header1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-10512. rat_exception_logging_header1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group. Reset Source: mod_g_rst_n
23:16	CODE	R	0h	Code. 1 = Boundary crossing error. Reset Source: mod_g_rst_n
15:0	RESERVED	NONE	0h	Reserved

14.7.1.4.2.43 RAT_EXCEPTION_LOGGING_DATA0 Register

14.7.1.4.2.43.1 RAT_EXCEPTION_LOGGING_DATA0 Register (Offset = 82Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 14-10513. Instance Table

Instance Name	Physical Address
MLB0	02F8 382Ch

Figure 14-5198. rat_exception_logging_data0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 14-10514. rat_exception_logging_data0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits. Reset Source: mod_g_rst_n

14.7.1.4.2.44 RAT_EXCEPTION_LOGGING_DATA1 Register

14.7.1.4.2.44.1 RAT_EXCEPTION_LOGGING_DATA1 Register (Offset = 830h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 14-10515. Instance Table

Instance Name	Physical Address
MLB0	02F8 3830h

Figure 14-5199. rat_exception_logging_data1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 14-10516. rat_exception_logging_data1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 12 bits. Reset Source: mod_g_rst_n

14.7.1.4.2.45 RAT_EXCEPTION_LOGGING_DATA2 Register

14.7.1.4.2.45.1 RAT_EXCEPTION_LOGGING_DATA2 Register (Offset = 834h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 14-10517. Instance Table

Instance Name	Physical Address
MLB0	02F8 3834h

Figure 14-5200. rat_exception_logging_data2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 14-10518. rat_exception_logging_data2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write. Reset Source: mod_g_rst_n
12	READ	R	0h	Read. Reset Source: mod_g_rst_n
11	DEBUG	R	0h	Debug. Reset Source: mod_g_rst_n
10	CACHEABLE	R	0h	Cacheable. Reset Source: mod_g_rst_n
9	PRIV	R	0h	Priv. Reset Source: mod_g_rst_n
8	SECURE	R	0h	Secure. Reset Source: mod_g_rst_n
7:0	PRIV_ID	R	0h	Priv ID. Reset Source: mod_g_rst_n

14.7.1.4.2.46 RAT_EXCEPTION_LOGGING_DATA3 Register

14.7.1.4.2.46.1 RAT_EXCEPTION_LOGGING_DATA3 Register (Offset = 838h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

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Table 14-10519. Instance Table

Instance Name	Physical Address
MLB0	02F8 3838h

Figure 14-5201. rat_exception_logging_data3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">BYTECNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BYTECNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10520. rat_exception_logging_data3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count. Reset Source: mod_g_rst_n

14.7.1.4.2.47 RAT_EXCEPTION_PEND_SET Register

14.7.1.4.2.47.1 RAT_EXCEPTION_PEND_SET Register (Offset = 840h) [reset = 0h]

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

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Table 14-10521. Instance Table

Instance Name	Physical Address
MLB0	02F8 3840h

Figure 14-5202. rat_exception_pend_set Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 14-10522. rat_exception_pend_set Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal. Reset Source: mod_g_rst_n

14.7.1.4.2.48 RAT_EXCEPTION_PEND_CLEAR Register

14.7.1.4.2.48.1 RAT_EXCEPTION_PEND_CLEAR Register (Offset = 844h) [reset = 0h]

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

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Table 14-10523. Instance Table

Instance Name	Physical Address
MLB0	02F8 3844h

Figure 14-5203. rat_exception_pend_clear Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 14-10524. rat_exception_pend_clear Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal. Reset Source: mod_g_rst_n

14.7.1.4.2.49 RAT_EXCEPTION_ENABLE_SET Register

14.7.1.4.2.49.1 RAT_EXCEPTION_ENABLE_SET Register (Offset = 848h) [reset = 0h]

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

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Table 14-10525. Instance Table

Instance Name	Physical Address
MLB0	02F8 3848h

Figure 14-5204. rat_exception_enable_set Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-10526. rat_exception_enable_set Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SET	R/W1TS	0h	Write a 1 to set the exception interrupt enable signal. Reset Source: mod_g_rst_n

14.7.1.4.2.50 RAT_EXCEPTION_ENABLE_CLEAR Register

14.7.1.4.2.50.1 RAT_EXCEPTION_ENABLE_CLEAR Register (Offset = 84Ch) [reset = 0h]

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

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Table 14-10527. Instance Table

Instance Name	Physical Address
MLB0	02F8 384Ch

Figure 14-5205. rat_exception_enable_clear Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-10528. rat_exception_enable_clear Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_CLR	R/W1TC	0h	Write a 1 to clear the exception interrupt enable signal. Reset Source: mod_g_rst_n

14.7.1.4.2.51 RAT_EOI_REG Register

14.7.1.4.2.51.1 RAT_EOI_REG Register (Offset = 850h) [reset = 0h]

EOI Register

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Table 14-10529. Instance Table

Instance Name	Physical Address
MLB0	02F8 3850h

Figure 14-5206. rat_eoi_reg Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI_WR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10530. rat_eoi_reg Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register Reset Source: mod_g_rst_n

14.7.1.4.2.52 RAT_REGION_CTRL_J Register

14.7.1.4.2.52.1 RAT_REGION_CTRL_J Register (Offset = 20h) [reset = 0h]

The Control for Region a

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Offset = Base + (j * 10h); where j = 0 to 63d

Table 14-10531. Instance Table

Instance Name	Physical Address
MLB0	02F8 3020h + formula

Figure 14-5207. rat_REGION_ctrl_j Name Register

31	30	29	28	27	26	25	24
EN	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		SIZE					
NONE		R/W					
0h		0h					

Table 14-10532. rat_REGION_ctrl_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the Region Reset Source: mod_g_rst_n
30:6	RESERVED	NONE	0h	Reserved
5:0	SIZE	R/W	0h	Size of the Region in Address Bits. 0 = 1 byte, 1 = 2B, 2 = 4B, 3 = 8B, etc. up to 32 = 4GB. Reset Source: mod_g_rst_n

14.7.1.4.2.53 RAT_REGION_BASE_J Register

14.7.1.4.2.53.1 RAT_REGION_BASE_J Register (Offset = 24h) [reset = 0h]

The Base Address for Region a. This is the source address for matching to a region.

Return to Summary Table

Offset = Base + (j * 10h); where j = 0 to 63d

Table 14-10533. Instance Table

Instance Name	Physical Address
MLB0	02F8 3024h + formula

Figure 14-5208. rat_REGION_base_j Name Register

31	30	29	28	27	26	25	24
BASE							
R/W							
0h							
23	22	21	20	19	18	17	16
BASE							
R/W							
0h							
15	14	13	12	11	10	9	8
BASE							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE							
R/W							
0h							

Table 14-10534. rat_REGION_base_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size. Reset Source: mod_g_rst_n

14.7.1.4.2.54 RAT_REGION_TRANS_L_J Register

14.7.1.4.2.54.1 RAT_REGION_TRANS_L_J Register (Offset = 28h) [reset = 0h]

The Translated Lower Address Bits for Region a

Return to Summary Table

Offset = Base + (j * 10h); where j = 0 to 63d

Table 14-10535. Instance Table

Instance Name	Physical Address
MLB0	02F8 3028h + formula

Figure 14-5209. rat_REGION_trans_l_j Name Register

31	30	29	28	27	26	25	24
LOWER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOWER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOWER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOWER							
R/W							
0h							

Table 14-10536. rat_REGION_trans_l_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOWER	R/W	0h	Translated Lower Address Bits for the Region. It must be aligned to the programmed size. Reset Source: mod_g_rst_n

14.7.1.4.2.55 RAT_REGION_TRANS_U_J Register

14.7.1.4.2.55.1 RAT_REGION_TRANS_U_J Register (Offset = 2Ch) [reset = 0h]

The Translated Upper Address Bits for Region a

Return to Summary Table

Offset = Base + (j * 10h); where j = 0 to 63d

Table 14-10537. Instance Table

Instance Name	Physical Address
MLB0	02F8 302Ch + formula

Figure 14-5210. rat_REGION_trans_u_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
UPPER							
R/W							
0h							
7	6	5	4	3	2	1	0
UPPER							
R/W							
0h							

Table 14-10538. rat_REGION_trans_u_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	UPPER	R/W	0h	Translated Upper Address Bits for the Region Reset Source: mod_g_rst_n

14.7.1.4.2.56 ECC_AGGR_REV Register

14.7.1.4.2.56.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

Revision parameters

Return to Summary Table

Table 14-10539. Instance Table

Instance Name	Physical Address
MLB0	072A 0000h

Figure 14-5211. ecc_aggr_rev Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
1Dh					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-10540. ecc_aggr_rev Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	1Dh	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

14.7.1.4.2.57 ECC_AGGR_VECTOR Register

14.7.1.4.2.57.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

Return to Summary Table

Table 14-10541. Instance Table

Instance Name	Physical Address
MLB0	072A 0008h

Figure 14-5212. ecc_aggr_vector Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-10542. ecc_aggr_vector Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.1.4.2.58 ECC_AGGR_STAT Register

14.7.1.4.2.58.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

Return to Summary Table

Table 14-10543. Instance Table

Instance Name	Physical Address
MLB0	072A 000Ch

Figure 14-5213. ecc_aggr_stat Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1h							

Table 14-10544. ecc_aggr_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.1.4.2.59 ECC_AGGR_RESERVED_SVBUS_J Register

14.7.1.4.2.59.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Offset = Base + (j * 4h); where j = 0 to 7d

Table 14-10545. Instance Table

Instance Name	Physical Address
MLB0	072A 0010h + formula

Figure 14-5214. ecc_aggr_reserved_svbus_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-10546. ecc_aggr_reserved_svbus_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.1.4.2.60 ECC_AGGR_SEC_EOI_REG Register

14.7.1.4.2.60.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-10547. Instance Table

Instance Name	Physical Address
MLB0	072A 003Ch

Figure 14-5215. ecc_aggr_sec_eoi_reg Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-10548. ecc_aggr_sec_eoi_reg Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.1.4.2.61 ECC_AGGR_SEC_STATUS_REG0 Register

14.7.1.4.2.61.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-10549. Instance Table

Instance Name	Physical Address
MLB0	072A 0040h

Figure 14-5216. ecc_aggr_sec_status_reg0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							DBMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-10550. ecc_aggr_sec_status_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DBMEM_PEND	R/W1TS	0h	Interrupt Pending Status for dbmem_pend

14.7.1.4.2.62 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.7.1.4.2.62.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-10551. Instance Table

Instance Name	Physical Address
MLB0	072A 0080h

Figure 14-5217. ecc_aggr_sec_enable_set_reg0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							DBMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-10552. ecc_aggr_sec_enable_set_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DBMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dbmem_pend

14.7.1.4.2.63 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.7.1.4.2.63.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-10553. Instance Table

Instance Name	Physical Address
MLB0	072A 00C0h

Figure 14-5218. ecc_aggr_sec_enable_clr_reg0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							DBMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-10554. ecc_aggr_sec_enable_clr_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DBMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dbmem_pend

14.7.1.4.2.64 ECC_AGGR_DED_EOI_REG Register

14.7.1.4.2.64.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-10555. Instance Table

Instance Name	Physical Address
MLB0	072A 013Ch

Figure 14-5219. ecc_aggr_ded_eoi_reg Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-10556. ecc_aggr_ded_eoi_reg Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.1.4.2.65 ECC_AGGR_DED_STATUS_REG0 Register

14.7.1.4.2.65.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-10557. Instance Table

Instance Name	Physical Address
MLB0	072A 0140h

Figure 14-5220. ecc_aggr_ded_status_reg0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DBMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-10558. ecc_aggr_ded_status_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DBMEM_PEND	R/W1TS	0h	Interrupt Pending Status for dbmem_pend

14.7.1.4.2.66 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.7.1.4.2.66.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-10559. Instance Table

Instance Name	Physical Address
MLB0	072A 0180h

Figure 14-5221. ecc_aggr_ded_enable_set_reg0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DBMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-10560. ecc_aggr_ded_enable_set_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DBMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for dbmem_pend

14.7.1.4.2.67 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.7.1.4.2.67.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-10561. Instance Table

Instance Name	Physical Address
MLB0	072A 01C0h

Figure 14-5222. ecc_aggr_ded_enable_clr_reg0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							DBMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-10562. ecc_aggr_ded_enable_clr_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	DBMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for dbmem_pend

14.7.1.4.2.68 ECC_AGGR_AGGR_ENABLE_SET Register

14.7.1.4.2.68.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 14-10563. Instance Table

Instance Name	Physical Address
MLB0	072A 0200h

Figure 14-5223. ecc_aggr_aggr_enable_set Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-10564. ecc_aggr_aggr_enable_set Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.1.4.2.69 ECC_AGGR_AGGR_ENABLE_CLR Register

14.7.1.4.2.69.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-10565. Instance Table

Instance Name	Physical Address
MLB0	072A 0204h

Figure 14-5224. ecc_aggr_aggr_enable_clr Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10566. ecc_aggr_aggr_enable_clr Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.1.4.2.70 ECC_AGGR_AGGR_STATUS_SET Register

14.7.1.4.2.70.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-10567. Instance Table

Instance Name	Physical Address
MLB0	072A 0208h

Figure 14-5225. ecc_aggr_aggr_status_set Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-10568. ecc_aggr_aggr_status_set Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.1.4.2.71 ECC_AGGR_AGGR_STATUS_CLR Register

14.7.1.4.2.71.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-10569. Instance Table

Instance Name	Physical Address
MLB0	072A 020Ch

Figure 14-5226. ecc_aggr_aggr_status_clr Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-10570. ecc_aggr_aggr_status_clr Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.2 General Connectivity Peripherals Registers

14.7.2.1 GPIO

GPIO

14.7.2.1.1 GPIO Summaries

GPIO Summaries

Table 14-10571. GPIO Registers, Base Address=0060 0000h, Length=256

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	MCU_GPIO0 Physical Address
0h	32	GPIO_PID	0060 0000h	0060 1000h	0420 1000h
4h	32	GPIO_PCR	0060 0004h	0060 1004h	0420 1004h
8h	32	GPIO_BINTEN	0060 0008h	0060 1008h	0420 1008h
10h	32	GPIO_DIR01	0060 0010h	0060 1010h	0420 1010h
14h	32	GPIO_OUT_DATA01	0060 0014h	0060 1014h	0420 1014h
18h	32	GPIO_SET_DATA01	0060 0018h	0060 1018h	0420 1018h
1Ch	32	GPIO_CLR_DATA01	0060 001Ch	0060 101Ch	0420 101Ch
20h	32	GPIO_IN_DATA01	0060 0020h	0060 1020h	0420 1020h
24h	32	GPIO_SET_RIS_TRIG01	0060 0024h	0060 1024h	0420 1024h
28h	32	GPIO_CLR_RIS_TRIG01	0060 0028h	0060 1028h	0420 1028h
2Ch	32	GPIO_SET_FAL_TRIG01	0060 002Ch	0060 102Ch	0420 102Ch
30h	32	GPIO_CLR_FAL_TRIG01	0060 0030h	0060 1030h	0420 1030h
34h	32	GPIO_INTSTAT01	0060 0034h	0060 1034h	0420 1034h
38h	32	GPIO_DIR23	0060 0038h	0060 1038h	0420 1038h
3Ch	32	GPIO_OUT_DATA23	0060 003Ch	0060 103Ch	0420 103Ch
40h	32	GPIO_SET_DATA23	0060 0040h	0060 1040h	0420 1040h
44h	32	GPIO_CLR_DATA23	0060 0044h	0060 1044h	0420 1044h
48h	32	GPIO_IN_DATA23	0060 0048h	0060 1048h	0420 1048h
4Ch	32	GPIO_SET_RIS_TRIG23	0060 004Ch	0060 104Ch	0420 104Ch
50h	32	GPIO_CLR_RIS_TRIG23	0060 0050h	0060 1050h	0420 1050h
54h	32	GPIO_SET_FAL_TRIG23	0060 0054h	0060 1054h	0420 1054h
58h	32	GPIO_CLR_FAL_TRIG23	0060 0058h	0060 1058h	0420 1058h
5Ch	32	GPIO_INTSTAT23	0060 005Ch	0060 105Ch	0420 105Ch
60h	32	GPIO_DIR45	0060 0060h	0060 1060h	0420 1060h
64h	32	GPIO_OUT_DATA45	0060 0064h	0060 1064h	0420 1064h
68h	32	GPIO_SET_DATA45	0060 0068h	0060 1068h	0420 1068h
6Ch	32	GPIO_CLR_DATA45	0060 006Ch	0060 106Ch	0420 106Ch
70h	32	GPIO_IN_DATA45	0060 0070h	0060 1070h	0420 1070h
74h	32	GPIO_SET_RIS_TRIG45	0060 0074h	0060 1074h	0420 1074h
78h	32	GPIO_CLR_RIS_TRIG45	0060 0078h	0060 1078h	0420 1078h
7Ch	32	GPIO_SET_FAL_TRIG45	0060 007Ch	0060 107Ch	0420 107Ch
80h	32	GPIO_CLR_FAL_TRIG45	0060 0080h	0060 1080h	0420 1080h
84h	32	GPIO_INTSTAT45	0060 0084h	0060 1084h	0420 1084h
88h	32	GPIO_DIR67	0060 0088h	0060 1088h	0420 1088h
8Ch	32	GPIO_OUT_DATA67	0060 008Ch	0060 108Ch	0420 108Ch
90h	32	GPIO_SET_DATA67	0060 0090h	0060 1090h	0420 1090h
94h	32	GPIO_CLR_DATA67	0060 0094h	0060 1094h	0420 1094h
98h	32	GPIO_IN_DATA67	0060 0098h	0060 1098h	0420 1098h
9Ch	32	GPIO_SET_RIS_TRIG67	0060 009Ch	0060 109Ch	0420 109Ch

Table 14-10571. GPIO Registers, Base Address=0060 0000h, Length=256 (continued)

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	MCU_GPIO0 Physical Address
A0h	32	GPIO_CLR_RIS_TRIG67	0060 00A0h	0060 10A0h	0420 10A0h
A4h	32	GPIO_SET_FAL_TRIG67	0060 00A4h	0060 10A4h	0420 10A4h
A8h	32	GPIO_CLR_FAL_TRIG67	0060 00A8h	0060 10A8h	0420 10A8h
ACh	32	GPIO_INTSTAT67	0060 00ACh	0060 10ACh	0420 10ACh
B0h	32	GPIO_DIR8	0060 00B0h	0060 10B0h	0420 10B0h
B4h	32	GPIO_OUT_DATA8	0060 00B4h	0060 10B4h	0420 10B4h
B8h	32	GPIO_SET_DATA8	0060 00B8h	0060 10B8h	0420 10B8h
BCh	32	GPIO_CLR_DATA8	0060 00BCh	0060 10BCh	0420 10BCh
C0h	32	GPIO_IN_DATA8	0060 00C0h	0060 10C0h	0420 10C0h
C4h	32	GPIO_SET_RIS_TRIG8	0060 00C4h	0060 10C4h	0420 10C4h
C8h	32	GPIO_CLR_RIS_TRIG8	0060 00C8h	0060 10C8h	0420 10C8h
CCh	32	GPIO_SET_FAL_TRIG8	0060 00CCh	0060 10CCh	0420 10CCh
D0h	32	GPIO_CLR_FAL_TRIG8	0060 00D0h	0060 10D0h	0420 10D0h
D4h	32	GPIO_INTSTAT8	0060 00D4h	0060 10D4h	0420 10D4h

14.7.2.1.2 GPIO Registers

GPIO Registers

14.7.2.1.2.1 GPIO_PID Register

14.7.2.1.2.1.1 GPIO_PID Register (Offset = 0h) [reset = 44832905h]

GPIO Periperal ID Register

Return to Summary Table

Table 14-10572. Instance Table

Instance Name	Physical Address
GPIO0	0060 0000h
GPIO1	0060 1000h
MCU_GPIO0	0420 1000h

Figure 14-5227. GPIO_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		R		R			
1h		0h		483h			
23	22	21	20	19	18	17	16
FUNC							
R							
483h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
5h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		5h					

Table 14-10573. GPIO_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Current scheme Reset Source: mod_g_srst_n
29:28	RESERVED	R	0h	RESERVED
27:16	FUNC	R	483h	Function code assigned to TCP3 Reset Source: mod_g_srst_n
15:11	RTL	R	5h	RTL Version R code Reset Source: mod_g_srst_n
10:8	MAJOR	R	1h	Major revision X code Reset Source: mod_g_srst_n
7:6	CUSTOM	R	0h	Custom version code Reset Source: mod_g_srst_n
5:0	MINOR	R	5h	Minor revision Y code Reset Source: mod_g_srst_n

14.7.2.1.2.2 GPIO_PCR Register

14.7.2.1.2.2.1 GPIO_PCR Register (Offset = 4h) [reset = 1h]

Peripheral Control Register

Return to Summary Table

Table 14-10574. Instance Table

Instance Name	Physical Address
GPIO0	0060 0004h
GPIO1	0060 1004h
MCU_GPIO0	0420 1004h

Figure 14-5228. GPIO_PCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R	R
0h						0h	1h

Table 14-10575. GPIO_PCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R	0h	Used in conjunction with FREE bit to determine the emulation suspend mode. Reset Source: mod_g_srst_n
0	FREE	R	1h	For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend. Reset Source: mod_g_srst_n

14.7.2.1.2.3 GPIO_BINTEN Register

14.7.2.1.2.3.1 GPIO_BINTEN Register (Offset = 8h) [reset = 0h]

Bit Interrupt Enable Register

Return to Summary Table

Table 14-10576. Instance Table

Instance Name	Physical Address
GPIO0	0060 0008h
GPIO1	0060 1008h
MCU_GPIO0	0420 1008h

Figure 14-5229. GPIO_BINTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
EN							
R/W							
0h							
7	6	5	4	3	2	1	0
EN							
R/W							
0h							

Table 14-10577. GPIO_BINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	EN	R/W	0h	Per bank interrupt enable. 0 = disable, 1 = enable. Reset Source: mod_g_srst_n

14.7.2.1.2.4 GPIO_DIR01 Register

14.7.2.1.2.4.1 GPIO_DIR01 Register (Offset = 10h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-10578. Instance Table

Instance Name	Physical Address
GPIO0	0060 0010h
GPIO1	0060 1010h
MCU_GPIO0	0420 1010h

Figure 14-5230. GPIO_DIR01 Name Register

31	30	29	28	27	26	25	24
DIR1							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR1							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR0							
R/W							
FFFFh							

Table 14-10579. GPIO_DIR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR1	R/W	FFFFh	Direction of GPIO bank 1 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR0	R/W	FFFFh	Direction of GPIO bank 0 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.7.2.1.2.5 GPIO_OUT_DATA01 Register

14.7.2.1.2.5.1 GPIO_OUT_DATA01 Register (Offset = 14h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-10580. Instance Table

Instance Name	Physical Address
GPIO0	0060 0014h
GPIO1	0060 1014h
MCU_GPIO0	0420 1014h

Figure 14-5231. GPIO_OUT_DATA01 Name Register

31	30	29	28	27	26	25	24
OUT1							
R/W							
0h							

23	22	21	20	19	18	17	16
OUT1							
R/W							
0h							

15	14	13	12	11	10	9	8
OUT0							
R/W							
0h							

7	6	5	4	3	2	1	0
OUT0							
R/W							
0h							

Table 14-10581. GPIO_OUT_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT1	R/W	0h	Output drive state of GPIO bank 1 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT0	R/W	0h	Output drive state of GPIO bank 0 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.6 GPIO_SET_DATA01 Register

14.7.2.1.2.6.1 GPIO_SET_DATA01 Register (Offset = 18h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-10582. Instance Table

Instance Name	Physical Address
GPIO0	0060 0018h
GPIO1	0060 1018h
MCU_GPIO0	0420 1018h

Figure 14-5232. GPIO_SET_DATA01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SET1</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SET1</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SET0</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SET0</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10583. GPIO_SET_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET1	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 1 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET0	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 0 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.7 GPIO_CLR_DATA01 Register

14.7.2.1.2.7.1 GPIO_CLR_DATA01 Register (Offset = 1Ch) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-10584. Instance Table

Instance Name	Physical Address
GPIO0	0060 001Ch
GPIO1	0060 101Ch
MCU_GPIO0	0420 101Ch

Figure 14-5233. GPIO_CLR_DATA01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLR1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLR1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLR0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLR0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10585. GPIO_CLR_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR1	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR0	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.8 GPIO_IN_DATA01 Register

14.7.2.1.2.8.1 GPIO_IN_DATA01 Register (Offset = 20h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-10586. Instance Table

Instance Name	Physical Address
GPIO0	0060 0020h
GPIO1	0060 1020h
MCU_GPIO0	0420 1020h

Figure 14-5234. GPIO_IN_DATA01 Name Register

31	30	29	28	27	26	25	24
IN1							
R							
0h							
23	22	21	20	19	18	17	16
IN1							
R							
0h							
15	14	13	12	11	10	9	8
IN0							
R							
0h							
7	6	5	4	3	2	1	0
IN0							
R							
0h							

Table 14-10587. GPIO_IN_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN1	R	0h	Status of GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	IN0	R	0h	Status of GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.9 GPIO_SET_RIS_TRIG01 Register

14.7.2.1.2.9.1 GPIO_SET_RIS_TRIG01 Register (Offset = 24h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-10588. Instance Table

Instance Name	Physical Address
GPIO0	0060 0024h
GPIO1	0060 1024h
MCU_GPIO0	0420 1024h

Figure 14-5235. GPIO_SET_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24
SETRIS1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS0							
R/W1TS							
0h							

Table 14-10589. GPIO_SET_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS1	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	SETRIS0	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.10 GPIO_CLR_RIS_TRIG01 Register

14.7.2.1.2.10.1 GPIO_CLR_RIS_TRIG01 Register (Offset = 28h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-10590. Instance Table

Instance Name	Physical Address
GPIO0	0060 0028h
GPIO1	0060 1028h
MCU_GPIO0	0420 1028h

Figure 14-5236. GPIO_CLR_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24
CLRRIS1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS0							
R/W1TC							
0h							

Table 14-10591. GPIO_CLR_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS1	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS0	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.11 GPIO_SET_FAL_TRIG01 Register

14.7.2.1.2.11.1 GPIO_SET_FAL_TRIG01 Register (Offset = 2Ch) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-10592. Instance Table

Instance Name	Physical Address
GPIO0	0060 002Ch
GPIO1	0060 102Ch
MCU_GPIO0	0420 102Ch

Figure 14-5237. GPIO_SET_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24
SETFAL1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL0							
R/W1TS							
0h							

Table 14-10593. GPIO_SET_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL1	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	SETFAL0	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.12 GPIO_CLR_FAL_TRIG01 Register

14.7.2.1.2.12.1 GPIO_CLR_FAL_TRIG01 Register (Offset = 30h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-10594. Instance Table

Instance Name	Physical Address
GPIO0	0060 0030h
GPIO1	0060 1030h
MCU_GPIO0	0420 1030h

Figure 14-5238. GPIO_CLR_FAL_TRIG01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLRFAL1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLRFAL1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLRFAL0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLRFAL0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10595. GPIO_CLR_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL1	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL0	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 0 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.13 GPIO_INTSTAT01 Register

14.7.2.1.2.13.1 GPIO_INTSTAT01 Register (Offset = 34h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-10596. Instance Table

Instance Name	Physical Address
GPIO0	0060 0034h
GPIO1	0060 1034h
MCU_GPIO0	0420 1034h

Figure 14-5239. GPIO_INTSTAT01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">STAT1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">STAT1</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">STAT0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">STAT0</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10597. GPIO_INTSTAT01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT1	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT0	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.7.2.1.2.14 GPIO_DIR23 Register

14.7.2.1.2.14.1 GPIO_DIR23 Register (Offset = 38h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-10598. Instance Table

Instance Name	Physical Address
GPIO0	0060 0038h
GPIO1	0060 1038h
MCU_GPIO0	0420 1038h

Figure 14-5240. GPIO_DIR23 Name Register

31	30	29	28	27	26	25	24
DIR3							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR3							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR2							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR2							
R/W							
FFFFh							

Table 14-10599. GPIO_DIR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR3	R/W	FFFFh	Direction of GPIO bank 3 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR2	R/W	FFFFh	Direction of GPIO bank 2 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.7.2.1.2.15 GPIO_OUT_DATA23 Register

14.7.2.1.2.15.1 GPIO_OUT_DATA23 Register (Offset = 3Ch) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-10600. Instance Table

Instance Name	Physical Address
GPIO0	0060 003Ch
GPIO1	0060 103Ch
MCU_GPIO0	0420 103Ch

Figure 14-5241. GPIO_OUT_DATA23 Name Register

31	30	29	28	27	26	25	24
OUT3							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT3							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT2							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT2							
R/W							
0h							

Table 14-10601. GPIO_OUT_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT3	R/W	0h	Output drive state of GPIO bank 3 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT2	R/W	0h	Output drive state of GPIO bank 2 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.16 GPIO_SET_DATA23 Register

14.7.2.1.2.16.1 GPIO_SET_DATA23 Register (Offset = 40h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-10602. Instance Table

Instance Name	Physical Address
GPIO0	0060 0040h
GPIO1	0060 1040h
MCU_GPIO0	0420 1040h

Figure 14-5242. GPIO_SET_DATA23 Name Register

31	30	29	28	27	26	25	24
SET3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET2							
R/W1TS							
0h							

Table 14-10603. GPIO_SET_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET3	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 3 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET2	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 2 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.17 GPIO_CLR_DATA23 Register

14.7.2.1.2.17.1 GPIO_CLR_DATA23 Register (Offset = 44h) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-10604. Instance Table

Instance Name	Physical Address
GPIO0	0060 0044h
GPIO1	0060 1044h
MCU_GPIO0	0420 1044h

Figure 14-5243. GPIO_CLR_DATA23 Name Register

31	30	29	28	27	26	25	24
CLR3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR2							
R/W1TC							
0h							

Table 14-10605. GPIO_CLR_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR3	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR2	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.18 GPIO_IN_DATA23 Register

14.7.2.1.2.18.1 GPIO_IN_DATA23 Register (Offset = 48h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-10606. Instance Table

Instance Name	Physical Address
GPIO0	0060 0048h
GPIO1	0060 1048h
MCU_GPIO0	0420 1048h

Figure 14-5244. GPIO_IN_DATA23 Name Register

31	30	29	28	27	26	25	24
IN3							
R							
0h							
23	22	21	20	19	18	17	16
IN3							
R							
0h							
15	14	13	12	11	10	9	8
IN2							
R							
0h							
7	6	5	4	3	2	1	0
IN2							
R							
0h							

Table 14-10607. GPIO_IN_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN3	R	0h	Status of GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	IN2	R	0h	Status of GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.19 GPIO_SET_RIS_TRIG23 Register

14.7.2.1.2.19.1 GPIO_SET_RIS_TRIG23 Register (Offset = 4Ch) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-10608. Instance Table

Instance Name	Physical Address
GPIO0	0060 004Ch
GPIO1	0060 104Ch
MCU_GPIO0	0420 104Ch

Figure 14-5245. GPIO_SET_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24
SETRIS3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS2							
R/W1TS							
0h							

Table 14-10609. GPIO_SET_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS3	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	SETRIS2	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.20 GPIO_CLR_RIS_TRIG23 Register

14.7.2.1.2.20.1 GPIO_CLR_RIS_TRIG23 Register (Offset = 50h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-10610. Instance Table

Instance Name	Physical Address
GPIO0	0060 0050h
GPIO1	0060 1050h
MCU_GPIO0	0420 1050h

Figure 14-5246. GPIO_CLR_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24
CLRRIS3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS2							
R/W1TC							
0h							

Table 14-10611. GPIO_CLR_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS3	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS2	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.21 GPIO_SET_FAL_TRIG23 Register

14.7.2.1.2.21.1 GPIO_SET_FAL_TRIG23 Register (Offset = 54h) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-10612. Instance Table

Instance Name	Physical Address
GPIO0	0060 0054h
GPIO1	0060 1054h
MCU_GPIO0	0420 1054h

Figure 14-5247. GPIO_SET_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24
SETFAL3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL2							
R/W1TS							
0h							

Table 14-10613. GPIO_SET_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL3	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	SETFAL2	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.22 GPIO_CLR_FAL_TRIG23 Register

14.7.2.1.2.22.1 GPIO_CLR_FAL_TRIG23 Register (Offset = 58h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-10614. Instance Table

Instance Name	Physical Address
GPIO0	0060 0058h
GPIO1	0060 1058h
MCU_GPIO0	0420 1058h

Figure 14-5248. GPIO_CLR_FAL_TRIG23 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLRFAL3</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLRFAL3</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLRFAL2</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLRFAL2</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10615. GPIO_CLR_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL3	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL2	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 2 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.23 GPIO_INTSTAT23 Register

14.7.2.1.2.23.1 GPIO_INTSTAT23 Register (Offset = 5Ch) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-10616. Instance Table

Instance Name	Physical Address
GPIO0	0060 005Ch
GPIO1	0060 105Ch
MCU_GPIO0	0420 105Ch

Figure 14-5249. GPIO_INTSTAT23 Name Register

31	30	29	28	27	26	25	24
STAT3							
R/W1TC							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STAT3							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
STAT2							
R/W1TC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STAT2							
R/W1TC							
0h							

Table 14-10617. GPIO_INTSTAT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT3	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT2	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.7.2.1.2.24 GPIO_DIR45 Register

14.7.2.1.2.24.1 GPIO_DIR45 Register (Offset = 60h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-10618. Instance Table

Instance Name	Physical Address
GPIO0	0060 0060h
GPIO1	0060 1060h
MCU_GPIO0	0420 1060h

Figure 14-5250. GPIO_DIR45 Name Register

31	30	29	28	27	26	25	24
DIR5							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR5							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR4							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR4							
R/W							
FFFFh							

Table 14-10619. GPIO_DIR45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR5	R/W	FFFFh	Direction of GPIO bank 5 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR4	R/W	FFFFh	Direction of GPIO bank 4 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.7.2.1.2.25 GPIO_OUT_DATA45 Register

14.7.2.1.2.25.1 GPIO_OUT_DATA45 Register (Offset = 64h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-10620. Instance Table

Instance Name	Physical Address
GPIO0	0060 0064h
GPIO1	0060 1064h
MCU_GPIO0	0420 1064h

Figure 14-5251. GPIO_OUT_DATA45 Name Register

31	30	29	28	27	26	25	24
OUT5							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT5							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT4							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT4							
R/W							
0h							

Table 14-10621. GPIO_OUT_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT5	R/W	0h	Output drive state of GPIO bank 5 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT4	R/W	0h	Output drive state of GPIO bank 4 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.26 GPIO_SET_DATA45 Register

14.7.2.1.2.26.1 GPIO_SET_DATA45 Register (Offset = 68h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-10622. Instance Table

Instance Name	Physical Address
GPIO0	0060 0068h
GPIO1	0060 1068h
MCU_GPIO0	0420 1068h

Figure 14-5252. GPIO_SET_DATA45 Name Register

31	30	29	28	27	26	25	24
SET5							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET5							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET4							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET4							
R/W1TS							
0h							

Table 14-10623. GPIO_SET_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET5	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 5 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET4	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 4 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.27 GPIO_CLR_DATA45 Register

14.7.2.1.2.27.1 GPIO_CLR_DATA45 Register (Offset = 6Ch) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-10624. Instance Table

Instance Name	Physical Address
GPIO0	0060 006Ch
GPIO1	0060 106Ch
MCU_GPIO0	0420 106Ch

Figure 14-5253. GPIO_CLR_DATA45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLR5</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLR5</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLR4</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLR4</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10625. GPIO_CLR_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR5	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR4	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.28 GPIO_IN_DATA45 Register

14.7.2.1.2.28.1 GPIO_IN_DATA45 Register (Offset = 70h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-10626. Instance Table

Instance Name	Physical Address
GPIO0	0060 0070h
GPIO1	0060 1070h
MCU_GPIO0	0420 1070h

Figure 14-5254. GPIO_IN_DATA45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IN5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IN5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IN4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IN4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10627. GPIO_IN_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN5	R	0h	Status of GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	IN4	R	0h	Status of GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.29 GPIO_SET_RIS_TRIG45 Register

14.7.2.1.2.29.1 GPIO_SET_RIS_TRIG45 Register (Offset = 74h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-10628. Instance Table

Instance Name	Physical Address
GPIO0	0060 0074h
GPIO1	0060 1074h
MCU_GPIO0	0420 1074h

Figure 14-5255. GPIO_SET_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24
SETRIS5							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETRIS5							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETRIS4							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETRIS4							
R/W1TS							
0h							

Table 14-10629. GPIO_SET_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS5	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	SETRIS4	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.30 GPIO_CLR_RIS_TRIG45 Register

14.7.2.1.2.30.1 GPIO_CLR_RIS_TRIG45 Register (Offset = 78h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-10630. Instance Table

Instance Name	Physical Address
GPIO0	0060 0078h
GPIO1	0060 1078h
MCU_GPIO0	0420 1078h

Figure 14-5256. GPIO_CLR_RIS_TRIG45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CLRRIS5</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CLRRIS5</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CLRRIS4</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CLRRIS4</td></tr>
<tr><td colspan="8">R/W1TC</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10631. GPIO_CLR_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS5	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS4	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.31 GPIO_SET_FAL_TRIG45 Register

14.7.2.1.2.31.1 GPIO_SET_FAL_TRIG45 Register (Offset = 7Ch) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-10632. Instance Table

Instance Name	Physical Address
GPIO0	0060 007Ch
GPIO1	0060 107Ch
MCU_GPIO0	0420 107Ch

Figure 14-5257. GPIO_SET_FAL_TRIG45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SETFAL5</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SETFAL5</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SETFAL4</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SETFAL4</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10633. GPIO_SET_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL5	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	SETFAL4	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.32 GPIO_CLR_FAL_TRIG45 Register

14.7.2.1.2.32.1 GPIO_CLR_FAL_TRIG45 Register (Offset = 80h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-10634. Instance Table

Instance Name	Physical Address
GPIO0	0060 0080h
GPIO1	0060 1080h
MCU_GPIO0	0420 1080h

Figure 14-5258. GPIO_CLR_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24
CLRFAL5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL4							
R/W1TC							
0h							

Table 14-10635. GPIO_CLR_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL5	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL4	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 4 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.33 GPIO_INTSTAT45 Register

14.7.2.1.2.33.1 GPIO_INTSTAT45 Register (Offset = 84h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-10636. Instance Table

Instance Name	Physical Address
GPIO0	0060 0084h
GPIO1	0060 1084h
MCU_GPIO0	0420 1084h

Figure 14-5259. GPIO_INTSTAT45 Name Register

31	30	29	28	27	26	25	24
STAT5							
R/W1TC							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STAT5							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
STAT4							
R/W1TC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STAT4							
R/W1TC							
0h							

Table 14-10637. GPIO_INTSTAT45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT5	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT4	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.7.2.1.2.34 GPIO_DIR67 Register

14.7.2.1.2.34.1 GPIO_DIR67 Register (Offset = 88h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-10638. Instance Table

Instance Name	Physical Address
GPIO0	0060 0088h
GPIO1	0060 1088h
MCU_GPIO0	0420 1088h

Figure 14-5260. GPIO_DIR67 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DIR7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DIR7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DIR6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DIR6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-10639. GPIO_DIR67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR7	R/W	FFFFh	Direction of GPIO bank 7 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR6	R/W	FFFFh	Direction of GPIO bank 6 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.7.2.1.2.35 GPIO_OUT_DATA67 Register

14.7.2.1.2.35.1 GPIO_OUT_DATA67 Register (Offset = 8Ch) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-10640. Instance Table

Instance Name	Physical Address
GPIO0	0060 008Ch
GPIO1	0060 108Ch
MCU_GPIO0	0420 108Ch

Figure 14-5261. GPIO_OUT_DATA67 Name Register

31	30	29	28	27	26	25	24
OUT7							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT7							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT6							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT6							
R/W							
0h							

Table 14-10641. GPIO_OUT_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT7	R/W	0h	Output drive state of GPIO bank 7 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT6	R/W	0h	Output drive state of GPIO bank 6 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.36 GPIO_SET_DATA67 Register

14.7.2.1.2.36.1 GPIO_SET_DATA67 Register (Offset = 90h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-10642. Instance Table

Instance Name	Physical Address
GPIO0	0060 0090h
GPIO1	0060 1090h
MCU_GPIO0	0420 1090h

Figure 14-5262. GPIO_SET_DATA67 Name Register

31	30	29	28	27	26	25	24
SET7							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET7							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET6							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET6							
R/W1TS							
0h							

Table 14-10643. GPIO_SET_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET7	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 7 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET6	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 6 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.37 GPIO_CLR_DATA67 Register

14.7.2.1.2.37.1 GPIO_CLR_DATA67 Register (Offset = 94h) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-10644. Instance Table

Instance Name	Physical Address
GPIO0	0060 0094h
GPIO1	0060 1094h
MCU_GPIO0	0420 1094h

Figure 14-5263. GPIO_CLR_DATA67 Name Register

31	30	29	28	27	26	25	24
CLR7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR6							
R/W1TC							
0h							

Table 14-10645. GPIO_CLR_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR7	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR6	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.38 GPIO_IN_DATA67 Register

14.7.2.1.2.38.1 GPIO_IN_DATA67 Register (Offset = 98h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-10646. Instance Table

Instance Name	Physical Address
GPIO0	0060 0098h
GPIO1	0060 1098h
MCU_GPIO0	0420 1098h

Figure 14-5264. GPIO_IN_DATA67 Name Register

31	30	29	28	27	26	25	24
IN7							
R							
0h							
23	22	21	20	19	18	17	16
IN7							
R							
0h							
15	14	13	12	11	10	9	8
IN6							
R							
0h							
7	6	5	4	3	2	1	0
IN6							
R							
0h							

Table 14-10647. GPIO_IN_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN7	R	0h	Status of GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	IN6	R	0h	Status of GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.39 GPIO_SET_RIS_TRIG67 Register

14.7.2.1.2.39.1 GPIO_SET_RIS_TRIG67 Register (Offset = 9Ch) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-10648. Instance Table

Instance Name	Physical Address
GPIO0	0060 009Ch
GPIO1	0060 109Ch
MCU_GPIO0	0420 109Ch

Figure 14-5265. GPIO_SET_RIS_TRIG67 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SETRIS7</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SETRIS7</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SETRIS6</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SETRIS6</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10649. GPIO_SET_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS7	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	SETRIS6	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.40 GPIO_CLR_RIS_TRIG67 Register

14.7.2.1.2.40.1 GPIO_CLR_RIS_TRIG67 Register (Offset = A0h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-10650. Instance Table

Instance Name	Physical Address
GPIO0	0060 00A0h
GPIO1	0060 10A0h
MCU_GPIO0	0420 10A0h

Figure 14-5266. GPIO_CLR_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24
CLRRIS7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS6							
R/W1TC							
0h							

Table 14-10651. GPIO_CLR_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS7	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS6	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.41 GPIO_SET_FAL_TRIG67 Register

14.7.2.1.2.41.1 GPIO_SET_FAL_TRIG67 Register (Offset = A4h) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-10652. Instance Table

Instance Name	Physical Address
GPIO0	0060 00A4h
GPIO1	0060 10A4h
MCU_GPIO0	0420 10A4h

Figure 14-5267. GPIO_SET_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24
SETFAL7							
R/W1TS							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETFAL7							
R/W1TS							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETFAL6							
R/W1TS							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETFAL6							
R/W1TS							
0h							

Table 14-10653. GPIO_SET_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL7	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	SETFAL6	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.42 GPIO_CLR_FAL_TRIG67 Register

14.7.2.1.2.42.1 GPIO_CLR_FAL_TRIG67 Register (Offset = A8h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-10654. Instance Table

Instance Name	Physical Address
GPIO0	0060 00A8h
GPIO1	0060 10A8h
MCU_GPIO0	0420 10A8h

Figure 14-5268. GPIO_CLR_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24
CLRFAL7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL6							
R/W1TC							
0h							

Table 14-10655. GPIO_CLR_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL7	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL6	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 6 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.43 GPIO_INTSTAT67 Register

14.7.2.1.2.43.1 GPIO_INTSTAT67 Register (Offset = ACh) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-10656. Instance Table

Instance Name	Physical Address
GPIO0	0060 00ACh
GPIO1	0060 10ACh
MCU_GPIO0	0420 10ACh

Figure 14-5269. GPIO_INTSTAT67 Name Register

31	30	29	28	27	26	25	24
STAT7							
R/W1TC							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STAT7							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
STAT6							
R/W1TC							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STAT6							
R/W1TC							
0h							

Table 14-10657. GPIO_INTSTAT67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT7	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT6	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.7.2.1.2.44 GPIO_DIR8 Register

14.7.2.1.2.44.1 GPIO_DIR8 Register (Offset = B0h) [reset = FFFFFFFFh]

Direction Register

Return to Summary Table

Table 14-10658. Instance Table

Instance Name	Physical Address
GPIO0	0060 00B0h
GPIO1	0060 10B0h
MCU_GPIO0	0420 10B0h

Figure 14-5270. GPIO_DIR8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DIR8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DIR8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-10659. GPIO_DIR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	FFFFh	RESERVED
15:0	DIR8	R/W	FFFFh	Direction of GPIO bank 8 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

14.7.2.1.2.45 GPIO_OUT_DATA8 Register

14.7.2.1.2.45.1 GPIO_OUT_DATA8 Register (Offset = B4h) [reset = 0h]

Output Drive State Register

Return to Summary Table

Table 14-10660. Instance Table

Instance Name	Physical Address
GPIO0	0060 00B4h
GPIO1	0060 10B4h
MCU_GPIO0	0420 10B4h

Figure 14-5271. GPIO_OUT_DATA8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUT8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUT8</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10661. GPIO_OUT_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	OUT8	R/W	0h	Output drive state of GPIO bank 8 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.46 GPIO_SET_DATA8 Register

14.7.2.1.2.46.1 GPIO_SET_DATA8 Register (Offset = B8h) [reset = 0h]

Set Output Drive State Register

Return to Summary Table

Table 14-10662. Instance Table

Instance Name	Physical Address
GPIO0	0060 00B8h
GPIO1	0060 10B8h
MCU_GPIO0	0420 10B8h

Figure 14-5272. GPIO_SET_DATA8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SET8</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SET8</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10663. GPIO_SET_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	SET8	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 8 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.47 GPIO_CLR_DATA8 Register

14.7.2.1.2.47.1 GPIO_CLR_DATA8 Register (Offset = BCh) [reset = 0h]

Clear Output Drive State Register

Return to Summary Table

Table 14-10664. Instance Table

Instance Name	Physical Address
GPIO0	0060 00BCh
GPIO1	0060 10BCh
MCU_GPIO0	0420 10BCh

Figure 14-5273. GPIO_CLR_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CLR8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR8							
R/W1TC							
0h							

Table 14-10665. GPIO_CLR_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	CLR8	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. Reset Source: mod_g_srst_n

14.7.2.1.2.48 GPIO_IN_DATA8 Register

14.7.2.1.2.48.1 GPIO_IN_DATA8 Register (Offset = C0h) [reset = 0h]

Bank Status Register

Return to Summary Table

Table 14-10666. Instance Table

Instance Name	Physical Address
GPIO0	0060 00C0h
GPIO1	0060 10C0h
MCU_GPIO0	0420 10C0h

Figure 14-5274. GPIO_IN_DATA8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IN8</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IN8</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10667. GPIO_IN_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	IN8	R	0h	Status of GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.49 GPIO_SET_RIS_TRIG8 Register

14.7.2.1.2.49.1 GPIO_SET_RIS_TRIG8 Register (Offset = C4h) [reset = 0h]

Set Rising Edge Detection Register

Return to Summary Table

Table 14-10668. Instance Table

Instance Name	Physical Address
GPIO0	0060 00C4h
GPIO1	0060 10C4h
MCU_GPIO0	0420 10C4h

Figure 14-5275. GPIO_SET_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SETRIS8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS8							
R/W1TS							
0h							

Table 14-10669. GPIO_SET_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SETRIS8	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.50 GPIO_CLR_RIS_TRIG8 Register

14.7.2.1.2.50.1 GPIO_CLR_RIS_TRIG8 Register (Offset = C8h) [reset = 0h]

Clear Rising Edge Detection Register

Return to Summary Table

Table 14-10670. Instance Table

Instance Name	Physical Address
GPIO0	0060 00C8h
GPIO1	0060 10C8h
MCU_GPIO0	0420 10C8h

Figure 14-5276. GPIO_CLR_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLRRIS8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS8							
R/W1TC							
0h							

Table 14-10671. GPIO_CLR_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLRRIS8	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.51 GPIO_SET_FAL_TRIG8 Register

14.7.2.1.2.51.1 GPIO_SET_FAL_TRIG8 Register (Offset = CCh) [reset = 0h]

Set Falling Edge Detection Register

Return to Summary Table

Table 14-10672. Instance Table

Instance Name	Physical Address
GPIO0	0060 00CCh
GPIO1	0060 10CCh
MCU_GPIO0	0420 10CCh

Figure 14-5277. GPIO_SET_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SETFAL8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL8							
R/W1TS							
0h							

Table 14-10673. GPIO_SET_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SETFAL8	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.52 GPIO_CLR_FAL_TRIG8 Register

14.7.2.1.2.52.1 GPIO_CLR_FAL_TRIG8 Register (Offset = D0h) [reset = 0h]

Clear Falling Edge Detection Register

Return to Summary Table

Table 14-10674. Instance Table

Instance Name	Physical Address
GPIO0	0060 00D0h
GPIO1	0060 10D0h
MCU_GPIO0	0420 10D0h

Figure 14-5278. GPIO_CLR_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLRFAL8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL8							
R/W1TC							
0h							

Table 14-10675. GPIO_CLR_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLRFAL8	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 8 bits. Reset Source: mod_g_srst_n

14.7.2.1.2.53 GPIO_INTSTAT8 Register

14.7.2.1.2.53.1 GPIO_INTSTAT8 Register (Offset = D4h) [reset = 0h]

Bank Interrupt Status Register

Return to Summary Table

Table 14-10676. Instance Table

Instance Name	Physical Address
GPIO0	0060 00D4h
GPIO1	0060 10D4h
MCU_GPIO0	0420 10D4h

Figure 14-5279. GPIO_INTSTAT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAT8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT8							
R/W1TC							
0h							

Table 14-10677. GPIO_INTSTAT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	STAT8	R/W1TC	0h	Status of GPIO bank 8 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

14.7.2.2 I2C

I2C

14.7.2.2.1 I2C Summaries

I2C Summaries

Table 14-10678. I2C Registers, Base Address=2000 0000h, Length=256

Offset	Length	Register Name	I2C0 Physical Address	I2C1 Physical Address	I2C2 Physical Address
0h	32	I2C_REVNB_LO	2000 0000h	2001 0000h	2002 0000h
4h	32	I2C_REVNB_HI	2000 0004h	2001 0004h	2002 0004h
10h	32	I2C_SYSC	2000 0010h	2001 0010h	2002 0010h
20h	32	I2C_EOI	2000 0020h	2001 0020h	2002 0020h
24h	32	I2C_IRQSTATUS_RAW	2000 0024h	2001 0024h	2002 0024h
28h	32	I2C_IRQSTATUS	2000 0028h	2001 0028h	2002 0028h
2Ch	32	I2C_IRQENABLE_SET	2000 002Ch	2001 002Ch	2002 002Ch
30h	32	I2C_IRQENABLE_CLR	2000 0030h	2001 0030h	2002 0030h
34h	32	I2C_WE	2000 0034h	2001 0034h	2002 0034h
38h	32	I2C_DMARXENABLE_SET	2000 0038h	2001 0038h	2002 0038h
3Ch	32	I2C_DMATXENABLE_SET	2000 003Ch	2001 003Ch	2002 003Ch
40h	32	I2C_DMARXENABLE_CLR	2000 0040h	2001 0040h	2002 0040h
44h	32	I2C_DMATXENABLE_CLR	2000 0044h	2001 0044h	2002 0044h
48h	32	I2C_DMARXWAKE_EN	2000 0048h	2001 0048h	2002 0048h
4Ch	32	I2C_DMATXWAKE_EN	2000 004Ch	2001 004Ch	2002 004Ch
84h	32	I2C_IE	2000 0084h	2001 0084h	2002 0084h
88h	32	I2C_STAT	2000 0088h	2001 0088h	2002 0088h
90h	32	I2C_SYSS	2000 0090h	2001 0090h	2002 0090h
94h	32	I2C_BUF	2000 0094h	2001 0094h	2002 0094h
98h	32	I2C_CNT	2000 0098h	2001 0098h	2002 0098h
9Ch	32	I2C_DATA	2000 009Ch	2001 009Ch	2002 009Ch
A4h	32	I2C_CON	2000 00A4h	2001 00A4h	2002 00A4h
A8h	32	I2C_OA	2000 00A8h	2001 00A8h	2002 00A8h
ACh	32	I2C_SA	2000 00ACh	2001 00ACh	2002 00ACh
B0h	32	I2C_PSC	2000 00B0h	2001 00B0h	2002 00B0h
B4h	32	I2C_SCLL	2000 00B4h	2001 00B4h	2002 00B4h
B8h	32	I2C_SCLH	2000 00B8h	2001 00B8h	2002 00B8h
BCh	32	I2C_SYSTEST	2000 00BCh	2001 00BCh	2002 00BCh
C0h	32	I2C_BUFSTAT	2000 00C0h	2001 00C0h	2002 00C0h
C4h	32	I2C_OA1	2000 00C4h	2001 00C4h	2002 00C4h
C8h	32	I2C_OA2	2000 00C8h	2001 00C8h	2002 00C8h
CCh	32	I2C_OA3	2000 00CCh	2001 00CCh	2002 00CCh
D0h	32	I2C_ACTOA	2000 00D0h	2001 00D0h	2002 00D0h
D4h	32	I2C_SBLOCK	2000 00D4h	2001 00D4h	2002 00D4h

Table 14-10679. I2C Registers, Base Address=2000 0000h, Length=256

Offset	Length	Register Name	I2C3 Physical Address	I2C4 Physical Address	I2C5 Physical Address
0h	32	I2C_REVNB_LO	2003 0000h	2004 0000h	2005 0000h
4h	32	I2C_REVNB_HI	2003 0004h	2004 0004h	2005 0004h

Table 14-10679. I2C Registers, Base Address=2000 0000h, Length=256 (continued)

Offset	Length	Register Name	I2C3 Physical Address	I2C4 Physical Address	I2C5 Physical Address
10h	32	I2C_SYSC	2003 0010h	2004 0010h	2005 0010h
20h	32	I2C_EOI	2003 0020h	2004 0020h	2005 0020h
24h	32	I2C_IRQSTATUS_RAW	2003 0024h	2004 0024h	2005 0024h
28h	32	I2C_IRQSTATUS	2003 0028h	2004 0028h	2005 0028h
2Ch	32	I2C_IRQENABLE_SET	2003 002Ch	2004 002Ch	2005 002Ch
30h	32	I2C_IRQENABLE_CLR	2003 0030h	2004 0030h	2005 0030h
34h	32	I2C_WE	2003 0034h	2004 0034h	2005 0034h
38h	32	I2C_DMARXENABLE_SET	2003 0038h	2004 0038h	2005 0038h
3Ch	32	I2C_DMATXENABLE_SET	2003 003Ch	2004 003Ch	2005 003Ch
40h	32	I2C_DMARXENABLE_CLR	2003 0040h	2004 0040h	2005 0040h
44h	32	I2C_DMATXENABLE_CLR	2003 0044h	2004 0044h	2005 0044h
48h	32	I2C_DMARXWAKE_EN	2003 0048h	2004 0048h	2005 0048h
4Ch	32	I2C_DMATXWAKE_EN	2003 004Ch	2004 004Ch	2005 004Ch
84h	32	I2C_IE	2003 0084h	2004 0084h	2005 0084h
88h	32	I2C_STAT	2003 0088h	2004 0088h	2005 0088h
90h	32	I2C_SYSS	2003 0090h	2004 0090h	2005 0090h
94h	32	I2C_BUF	2003 0094h	2004 0094h	2005 0094h
98h	32	I2C_CNT	2003 0098h	2004 0098h	2005 0098h
9Ch	32	I2C_DATA	2003 009Ch	2004 009Ch	2005 009Ch
A4h	32	I2C_CON	2003 00A4h	2004 00A4h	2005 00A4h
A8h	32	I2C_OA	2003 00A8h	2004 00A8h	2005 00A8h
ACh	32	I2C_SA	2003 00ACh	2004 00ACh	2005 00ACh
B0h	32	I2C_PSC	2003 00B0h	2004 00B0h	2005 00B0h
B4h	32	I2C_SCLL	2003 00B4h	2004 00B4h	2005 00B4h
B8h	32	I2C_SCLH	2003 00B8h	2004 00B8h	2005 00B8h
BCh	32	I2C_SYSTEST	2003 00BCh	2004 00BCh	2005 00BCh
C0h	32	I2C_BUFSTAT	2003 00C0h	2004 00C0h	2005 00C0h
C4h	32	I2C_OA1	2003 00C4h	2004 00C4h	2005 00C4h
C8h	32	I2C_OA2	2003 00C8h	2004 00C8h	2005 00C8h
CCh	32	I2C_OA3	2003 00CCh	2004 00CCh	2005 00CCh
D0h	32	I2C_ACTOA	2003 00D0h	2004 00D0h	2005 00D0h
D4h	32	I2C_SBLOCK	2003 00D4h	2004 00D4h	2005 00D4h

Table 14-10680. I2C Registers, Base Address=2000 0000h, Length=256

Offset	Length	Register Name	I2C6 Physical Address	WKUP_I2C0 Physical Address
0h	32	I2C_REVNB_LO	2006 0000h	2B20 0000h
4h	32	I2C_REVNB_HI	2006 0004h	2B20 0004h
10h	32	I2C_SYSC	2006 0010h	2B20 0010h
20h	32	I2C_EOI	2006 0020h	2B20 0020h
24h	32	I2C_IRQSTATUS_RAW	2006 0024h	2B20 0024h
28h	32	I2C_IRQSTATUS	2006 0028h	2B20 0028h
2Ch	32	I2C_IRQENABLE_SET	2006 002Ch	2B20 002Ch
30h	32	I2C_IRQENABLE_CLR	2006 0030h	2B20 0030h
34h	32	I2C_WE	2006 0034h	2B20 0034h
38h	32	I2C_DMARXENABLE_SET	2006 0038h	2B20 0038h
3Ch	32	I2C_DMATXENABLE_SET	2006 003Ch	2B20 003Ch

Table 14-10680. I2C Registers, Base Address=2000 0000h, Length=256 (continued)

Offset	Length	Register Name	I2C6 Physical Address	WKUP_I2C0 Physical Address
40h	32	I2C_DMARXENABLE_CLR	2006 0040h	2B20 0040h
44h	32	I2C_DMATXENABLE_CLR	2006 0044h	2B20 0044h
48h	32	I2C_DMARXWAKE_EN	2006 0048h	2B20 0048h
4Ch	32	I2C_DMATXWAKE_EN	2006 004Ch	2B20 004Ch
84h	32	I2C_IE	2006 0084h	2B20 0084h
88h	32	I2C_STAT	2006 0088h	2B20 0088h
90h	32	I2C_SYSS	2006 0090h	2B20 0090h
94h	32	I2C_BUF	2006 0094h	2B20 0094h
98h	32	I2C_CNT	2006 0098h	2B20 0098h
9Ch	32	I2C_DATA	2006 009Ch	2B20 009Ch
A4h	32	I2C_CON	2006 00A4h	2B20 00A4h
A8h	32	I2C_OA	2006 00A8h	2B20 00A8h
ACh	32	I2C_SA	2006 00ACh	2B20 00ACh
B0h	32	I2C_PSC	2006 00B0h	2B20 00B0h
B4h	32	I2C_SCLL	2006 00B4h	2B20 00B4h
B8h	32	I2C_SCLH	2006 00B8h	2B20 00B8h
BCh	32	I2C_SYSTEST	2006 00BCh	2B20 00BCh
C0h	32	I2C_BUFSTAT	2006 00C0h	2B20 00C0h
C4h	32	I2C_OA1	2006 00C4h	2B20 00C4h
C8h	32	I2C_OA2	2006 00C8h	2B20 00C8h
CCh	32	I2C_OA3	2006 00CCh	2B20 00CCh
D0h	32	I2C_ACTOA	2006 00D0h	2B20 00D0h
D4h	32	I2C_SBLOCK	2006 00D4h	2B20 00D4h

14.7.2.2.2 I2C Registers

I2C Registers

14.7.2.2.2.1 I2C_REVNB_LO Register

14.7.2.2.2.1.1 I2C_REVNB_LO Register (Offset = 0h) [reset = 80Ch]

Revision Number register (Low)

Return to Summary Table

Table 14-10681. Instance Table

Instance Name	Physical Address
I2C0	2000 0000h
I2C1	2001 0000h
I2C2	2002 0000h
I2C3	2003 0000h
I2C4	2004 0000h
I2C5	2005 0000h
I2C6	2006 0000h
WKUP_I2C0	2B20 0000h

Figure 14-5280. I2C_REVNB_LO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">1h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">Ch</td></tr>
</table>

Table 14-10682. I2C_REVNB_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:11	RTL	R	1h	RTL version This field changes on bug fix, and resets to
10:8	MAJOR	R	0h	Major Revision This field changes when there is a major feature change This field does not change due to bug fix, or minor feature change
7:6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers 0 if non-custom
5:0	MINOR	R	Ch	Minor Revision This field changes when features are scaled up or down This field does not change due to bug fix, or major feature change

14.7.2.2.2.2 I2C_REVNB_HI Register

14.7.2.2.2.2.1 I2C_REVNB_HI Register (Offset = 4h) [reset = 5040h]

Revision Number register (High)

Return to Summary Table

Table 14-10683. Instance Table

Instance Name	Physical Address
I2C0	2000 0004h
I2C1	2001 0004h
I2C2	2002 0004h
I2C3	2003 0004h
I2C4	2004 0004h
I2C5	2005 0004h
I2C6	2006 0004h
WKUP_I2C0	2B20 0004h

Figure 14-5281. I2C_REVNB_HI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SCHEME		RESERVED		FUNC			
R		R		R			
1h		1h		40h			
7	6	5	4	3	2	1	0
FUNC							
R							
40h							

Table 14-10684. I2C_REVNB_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:14	SCHEME	R	1h	Used to distinguish between old Scheme and current Spare bit to encode future schemes
13:12	RESERVED	R	1h	Reads return 0x1
11:0	FUNC	R	40h	Function: Indicates a software compatible module family

14.7.2.2.2.3 I2C_SYSC Register

14.7.2.2.2.3.1 I2C_SYSC Register (Offset = 10h) [reset = 1h]

System Configuration register

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Table 14-10685. Instance Table

Instance Name	Physical Address
I2C0	2000 0010h
I2C1	2001 0010h
I2C2	2002 0010h
I2C3	2003 0010h
I2C4	2004 0010h
I2C5	2005 0010h
I2C6	2006 0010h
WKUP_I2C0	2B20 0010h

Figure 14-5282. I2C_SYSC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED1						CLKACTIVITY	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED			IDLEMODE		ENAWAKEUP	SRST	AUTOIDLE
R			R/W		R/W	R/W	R/W
0h			0h		0h	0h	1h

Table 14-10686. I2C_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED1	R	0h	Reserved
9:8	CLKACTIVITY	R/W	0h	Clock Activity selection bits
7:5	RESERVED	R	0h	Reads return 0
4:3	IDLEMODE	R/W	0h	Idle Mode selection bits
2	ENAWAKEUP	R/W	0h	Enable Wakeup control bit
1	SRST	R/W	0h	SoftReset bit
0	AUTOIDLE	R/W	1h	Autoidle bit

14.7.2.2.2.4 I2C_EOI Register

14.7.2.2.2.4.1 I2C_EOI Register (Offset = 20h) [reset = 0h]

End Of Interrupt number specification

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Table 14-10687. Instance Table

Instance Name	Physical Address
I2C0	2000 0020h
I2C1	2001 0020h
I2C2	2002 0020h
I2C3	2003 0020h
I2C4	2004 0020h
I2C5	2005 0020h
I2C6	2006 0020h
WKUP_I2C0	2B20 0020h

Figure 14-5283. I2C_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>LINE_NUMBER</td></tr>
<tr><td colspan="7">R</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-10688. I2C_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	LINE_NUMBER	W	0h	Software End Of Interrupt [EOI] control Write number of interrupt output

14.7.2.2.2.5 I2C_IRQSTATUS_RAW Register

14.7.2.2.2.5.1 I2C_IRQSTATUS_RAW Register (Offset = 24h) [reset = 0h]

Per-event raw interrupt status vector

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Table 14-10689. Instance Table

Instance Name	Physical Address
I2C0	2000 0024h
I2C1	2001 0024h
I2C2	2002 0024h
I2C3	2003 0024h
I2C4	2004 0024h
I2C5	2005 0024h
I2C6	2006 0024h
WKUP_I2C0	2B20 0024h

Figure 14-5284. I2C_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_11	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W	R/W	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10690. I2C_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_11	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ status
13	RDR	R/W	0h	Receive draining IRQ status
12	BB	R	0h	Bus busy statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as target IRQ status
8	BF	R/W	0h	Bus Free IRQ status
7	AERR	R/W	0h	Access Error IRQ status
6	STC	R/W	0h	Start Condition IRQ status
5	GC	R/W1C	0h	General call IRQ status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear

Table 14-10690. I2C_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R/W1C	0h	Transmit data ready IRQ status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W1C	0h	Receive data ready IRQ status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W1C	0h	Register access ready IRQ status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W1C	0h	No acknowledgement IRQ status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ status This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

14.7.2.2.2.6 I2C_IRQSTATUS Register

14.7.2.2.2.6.1 I2C_IRQSTATUS Register (Offset = 28h) [reset = 0h]

Per-event enabled interrupt status vector

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Table 14-10691. Instance Table

Instance Name	Physical Address
I2C0	2000 0028h
I2C1	2001 0028h
I2C2	2002 0028h
I2C3	2003 0028h
I2C4	2004 0028h
I2C5	2005 0028h
I2C6	2006 0028h
WKUP_I2C0	2B20 0028h

Figure 14-5285. I2C_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_11	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10692. I2C_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_11	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ enabled status
13	RDR	R/W	0h	Receive draining IRQ enabled status
12	BB	R	0h	Bus busy enabled statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun enabled statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow enabled statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as target IRQ enabled status
8	BF	R/W	0h	Bus Free IRQ enabled status
7	AERR	R/W	0h	Access Error IRQ enabled status
6	STC	R/W	0h	Start Condition IRQ enabled status
5	GC	R/W	0h	General call IRQ enabled status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear

Table 14-10692. I2C_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R/W	0h	Transmit data ready IRQ enabled status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W	0h	Receive data ready IRQ enabled status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W	0h	Register access ready IRQ enabled status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W	0h	No acknowledgement IRQ enabled status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ enabled status This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

14.7.2.2.2.7 I2C_IRQENABLE_SET Register

14.7.2.2.2.7.1 I2C_IRQENABLE_SET Register (Offset = 2Ch) [reset = 0h]

Per-event interrupt enable bit vector.

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Table 14-10693. Instance Table

Instance Name	Physical Address
I2C0	2000 002Ch
I2C1	2001 002Ch
I2C2	2002 002Ch
I2C3	2003 002Ch
I2C4	2004 002Ch
I2C5	2005 002Ch
I2C6	2006 002Ch
WKUP_I2C0	2B20 002Ch

Figure 14-5286. I2C_IRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_5	XDR_IE	RDR_IE	RESERVED1	ROVR	XUDF	ASS_IE	BF_IE
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10694. I2C_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_5	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED1	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable set
10	XUDF	R/W	0h	Transmit underflow enable set
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]
8	BF_IE	R/W	0h	Bus Free interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]

Table 14-10694. I2C_IRQENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AERR_IE	R/W	0h	Access Error interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]
6	STC_IE	R/W	0h	Start Condition interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

14.7.2.2.2.8 I2C_IRQENABLE_CLR Register

14.7.2.2.2.8.1 I2C_IRQENABLE_CLR Register (Offset = 30h) [reset = 0h]

Per-event interrupt clear bit vector.

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Table 14-10695. Instance Table

Instance Name	Physical Address
I2C0	2000 0030h
I2C1	2001 0030h
I2C2	2002 0030h
I2C3	2003 0030h
I2C4	2004 0030h
I2C5	2005 0030h
I2C6	2006 0030h
WKUP_I2C0	2B20 0030h

Figure 14-5287. I2C_IRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_5	XDR_IE	RDR_IE	RESERVED1	ROVR	XUDF	ASS_IE	BF_IE
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10696. I2C_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_5	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED1	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable clear
10	XUDF	R/W	0h	Transmit underflow enable clear
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]
8	BF_IE	R/W	0h	Bus Free interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]

Table 14-10696. I2C_IRQENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AERR_IE	R/W	0h	Access Error interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]
6	STC_IE	R/W	0h	Start Condition interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

14.7.2.2.2.9 I2C_WE Register

14.7.2.2.2.9.1 I2C_WE Register (Offset = 34h) [reset = 0h]

I2C wakeup enable vector (legacy).

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Table 14-10697. Instance Table

Instance Name	Physical Address
I2C0	2000 0034h
I2C1	2001 0034h
I2C2	2002 0034h
I2C3	2003 0034h
I2C4	2004 0034h
I2C5	2005 0034h
I2C6	2006 0034h
WKUP_I2C0	2B20 0034h

Figure 14-5288. I2C_WE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED3	ROVR	XUDF	AAS	BF
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	STC	GC	RESERVED1	DRDY	ARDY	NACK	AL
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10698. I2C_WE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED3	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as target IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED2	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED1	R	0h	Reserved

Table 14-10698. I2C_WE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

14.7.2.2.2.10 I2C_DMARXENABLE_SET Register

14.7.2.2.2.10.1 I2C_DMARXENABLE_SET Register (Offset = 38h) [reset = 0h]

Per-event DMA RX enable set.

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Table 14-10699. Instance Table

Instance Name	Physical Address
I2C0	2000 0038h
I2C1	2001 0038h
I2C2	2002 0038h
I2C3	2003 0038h
I2C4	2004 0038h
I2C5	2005 0038h
I2C6	2006 0038h
WKUP_I2C0	2B20 0038h

Figure 14-5289. I2C_DMARXENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							DMARX_ENABLE_SET
R							R/W
0h							0h

Table 14-10700. I2C_DMARXENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	DMARX_ENABLE_SET	R/W	0h	Receive DMA channel enable set

14.7.2.2.2.11 I2C_DMATXENABLE_SET Register

14.7.2.2.2.11.1 I2C_DMATXENABLE_SET Register (Offset = 3Ch) [reset = 0h]

Per-event DMA TX enable set.

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Table 14-10701. Instance Table

Instance Name	Physical Address
I2C0	2000 003Ch
I2C1	2001 003Ch
I2C2	2002 003Ch
I2C3	2003 003Ch
I2C4	2004 003Ch
I2C5	2005 003Ch
I2C6	2006 003Ch
WKUP_I2C0	2B20 003Ch

Figure 14-5290. I2C_DMATXENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							DMATX_ENABLE_SET
R							R/W
0h							0h

Table 14-10702. I2C_DMATXENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	DMATX_ENABLE_SET	R/W	0h	Transmit DMA channel enable set

14.7.2.2.2.12 I2C_DMARXENABLE_CLR Register

14.7.2.2.2.12.1 I2C_DMARXENABLE_CLR Register (Offset = 40h) [reset = 0h]

Per-event DMA RX enable clear.

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Table 14-10703. Instance Table

Instance Name	Physical Address
I2C0	2000 0040h
I2C1	2001 0040h
I2C2	2002 0040h
I2C3	2003 0040h
I2C4	2004 0040h
I2C5	2005 0040h
I2C6	2006 0040h
WKUP_I2C0	2B20 0040h

Figure 14-5291. I2C_DMARXENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							DMARX_ENABLE_CLEAR
R							R/W1C
0h							0h

Table 14-10704. I2C_DMARXENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	DMARX_ENABLE_CLEAR	R/W1C	0h	Receive DMA channel enable clear

14.7.2.2.2.13 I2C_DMATXENABLE_CLR Register

14.7.2.2.2.13.1 I2C_DMATXENABLE_CLR Register (Offset = 44h) [reset = 0h]

Per-event DMA TX enable clear.

Return to Summary Table

Table 14-10705. Instance Table

Instance Name	Physical Address
I2C0	2000 0044h
I2C1	2001 0044h
I2C2	2002 0044h
I2C3	2003 0044h
I2C4	2004 0044h
I2C5	2005 0044h
I2C6	2006 0044h
WKUP_I2C0	2B20 0044h

Figure 14-5292. I2C_DMATXENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							DMATX_ENABLE_CLEAR
R							R/W1C
0h							0h

Table 14-10706. I2C_DMATXENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	DMATX_ENABLE_CLEAR	R/W1C	0h	Transmit DMA channel enable clear

14.7.2.2.2.14 I2C_DMARXWAKE_EN Register

14.7.2.2.2.14.1 I2C_DMARXWAKE_EN Register (Offset = 48h) [reset = 0h]

Per-event DMA RX wakeup enable.

Return to Summary Table

Table 14-10707. Instance Table

Instance Name	Physical Address
I2C0	2000 0048h
I2C1	2001 0048h
I2C2	2002 0048h
I2C3	2003 0048h
I2C4	2004 0048h
I2C5	2005 0048h
I2C6	2006 0048h
WKUP_I2C0	2B20 0048h

Figure 14-5293. I2C_DMARXWAKE_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED3	ROVR	XUDF	AAS	BF
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	STC	GC	RESERVED1	DRDY	ARDY	NACK	AL
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10708. I2C_DMARXWAKE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED3	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as target IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED2	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED1	R	0h	Reserved

Table 14-10708. I2C_DMARXWAKE_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

14.7.2.2.2.15 I2C_DMATXWAKE_EN Register

14.7.2.2.2.15.1 I2C_DMATXWAKE_EN Register (Offset = 4Ch) [reset = 0h]

Per-event DMA TX wakeup enable.

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Table 14-10709. Instance Table

Instance Name	Physical Address
I2C0	2000 004Ch
I2C1	2001 004Ch
I2C2	2002 004Ch
I2C3	2003 004Ch
I2C4	2004 004Ch
I2C5	2005 004Ch
I2C6	2006 004Ch
WKUP_I2C0	2B20 004Ch

Figure 14-5294. I2C_DMATXWAKE_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED3	ROVR	XUDF	AAS	BF
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	STC	GC	RESERVED1	DRDY	ARDY	NACK	AL
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10710. I2C_DMATXWAKE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED3	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as target IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED2	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED1	R	0h	Reserved

Table 14-10710. I2C_DMATXWAKE_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

14.7.2.2.2.16 I2C_IE Register

14.7.2.2.2.16.1 I2C_IE Register (Offset = 84h) [reset = 0h]

I2C interrupt enable vector (legacy).

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Table 14-10711. Instance Table

Instance Name	Physical Address
I2C0	2000 0084h
I2C1	2001 0084h
I2C2	2002 0084h
I2C3	2003 0084h
I2C4	2004 0084h
I2C5	2005 0084h
I2C6	2006 0084h
WKUP_I2C0	2B20 0084h

Figure 14-5295. I2C_IE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_5	XDR_IE	RDR_IE	RESERVED1	ROVR	XUDF	ASS_IE	BF_IE
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10712. I2C_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_5	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED1	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable set
10	XUDF	R/W	0h	Transmit underflow enable set
9	ASS_IE	R/W	0h	Addressed as Target interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]
8	BF_IE	R/W	0h	Bus Free interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]

Table 14-10712. I2C_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AERR_IE	R/W	0h	Access Error interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]
6	STC_IE	R/W	0h	Start Condition interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

14.7.2.2.2.17 I2C_STAT Register

14.7.2.2.2.17.1 I2C_STAT Register (Offset = 88h) [reset = 0h]

I2C interrupt status vector (legacy).

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Table 14-10713. Instance Table

Instance Name	Physical Address
I2C0	2000 0088h
I2C1	2001 0088h
I2C2	2002 0088h
I2C3	2003 0088h
I2C4	2004 0088h
I2C5	2005 0088h
I2C6	2006 0088h
WKUP_I2C0	2B20 0088h

Figure 14-5296. I2C_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED_11	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10714. I2C_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED_11	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ status
13	RDR	R/W	0h	Receive draining IRQ status
12	BB	R	0h	Bus busy statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as target IRQ status
8	BF	R/W	0h	Bus Free IRQ status
7	AERR	R/W	0h	Access Error IRQ status
6	STC	R/W	0h	Start Condition IRQ status
5	GC	R/W	0h	General call IRQ status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear

Table 14-10714. I2C_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XRDY	R/W	0h	Transmit data ready IRQ status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W	0h	Receive data ready IRQ status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W	0h	Register access ready IRQ status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W	0h	No acknowledgement IRQ status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ status This bit is automatically set by the hardware when it loses the Arbitration in controller transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

14.7.2.2.2.18 I2C_SYSS Register

14.7.2.2.2.18.1 I2C_SYSS Register (Offset = 90h) [reset = 0h]

System Status register

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Table 14-10715. Instance Table

Instance Name	Physical Address
I2C0	2000 0090h
I2C1	2001 0090h
I2C2	2002 0090h
I2C3	2003 0090h
I2C4	2004 0090h
I2C5	2005 0090h
I2C6	2006 0090h
WKUP_I2C0	2B20 0090h

Figure 14-5297. I2C_SYSS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RDONE
R							R
0h							0h

Table 14-10716. I2C_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:1	RESERVED	R	0h	Reserved
0	RDONE	R	0h	Reset done bit

14.7.2.2.2.19 I2C_BUF Register

14.7.2.2.2.19.1 I2C_BUF Register (Offset = 94h) [reset = 0h]

Buffer Configuration register

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Table 14-10717. Instance Table

Instance Name	Physical Address
I2C0	2000 0094h
I2C1	2001 0094h
I2C2	2002 0094h
I2C3	2003 0094h
I2C4	2004 0094h
I2C5	2005 0094h
I2C6	2006 0094h
WKUP_I2C0	2B20 0094h

Figure 14-5298. I2C_BUF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RDMA_EN	RXFIFO_CLR	RXTRSH					
R/W	R/W	R/W					
0h	0h	0h					
7	6	5	4	3	2	1	0
XDMA_EN	TXFIFO_CLR	TXTRSH					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-10718. I2C_BUF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RDMA_EN	R/W	0h	Receive DMA channel enable
14	RXFIFO_CLR	R/W	0h	Receive FIFO clear
13:8	RXTRSH	R/W	0h	Threshold value for FIFO buffer in RX mode
7	XDMA_EN	R/W	0h	Transmit DMA channel enable
6	TXFIFO_CLR	R/W	0h	Transmit FIFO clear
5:0	TXTRSH	R/W	0h	Threshold value for FIFO buffer in TX mode

14.7.2.2.2.20 I2C_CNT Register

14.7.2.2.2.20.1 I2C_CNT Register (Offset = 98h) [reset = 0h]

Data counter register

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Table 14-10719. Instance Table

Instance Name	Physical Address
I2C0	2000 0098h
I2C1	2001 0098h
I2C2	2002 0098h
I2C3	2003 0098h
I2C4	2004 0098h
I2C5	2005 0098h
I2C6	2006 0098h
WKUP_I2C0	2B20 0098h

Figure 14-5299. I2C_CNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DCOUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DCOUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10720. I2C_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	DCOUNT	R/W	0h	Data count

14.7.2.2.2.21 I2C_DATA Register

14.7.2.2.2.21.1 I2C_DATA Register (Offset = 9Ch) [reset = 0h]

Data access register

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Table 14-10721. Instance Table

Instance Name	Physical Address
I2C0	2000 009Ch
I2C1	2001 009Ch
I2C2	2002 009Ch
I2C3	2003 009Ch
I2C4	2004 009Ch
I2C5	2005 009Ch
I2C6	2006 009Ch
WKUP_I2C0	2B20 009Ch

Figure 14-5300. I2C_DATA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10722. I2C_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RESERVED	R	0h	Reserved
7:0	DATA	R/W	0h	Transmit/Receive data FIFO endpoint

14.7.2.2.2.22 I2C_CON Register

14.7.2.2.2.22.1 I2C_CON Register (Offset = A4h) [reset = 0h]

I2C configuration register.

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Table 14-10723. Instance Table

Instance Name	Physical Address
I2C0	2000 00A4h
I2C1	2001 00A4h
I2C2	2002 00A4h
I2C3	2003 00A4h
I2C4	2004 00A4h
I2C5	2005 00A4h
I2C6	2006 00A4h
WKUP_I2C0	2B20 00A4h

Figure 14-5301. I2C_CON Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I2C_EN	RESERVED	OPMODE		STB	MST	TRX	XSA
R/W	R	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h
7	6	5	4	3	2	1	0
XOA0	XOA1	XOA2	XOA3	RESERVED1		STP	STT
R/W	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-10724. I2C_CON Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	I2C_EN	R/W	0h	I2C module enable
14	RESERVED	R	0h	Reserved
13:12	OPMODE	R/W	0h	Operation mode selection
11	STB	R/W	0h	Start byte mode [controller mode only]
10	MST	R/W	0h	Controller/target mode
9	TRX	R/W	0h	Transmitter/Receiver mode [controller mode only]
8	XSA	R/W	0h	Expand Target address
7	XOA0	R/W	0h	Expand Own address 0
6	XOA1	R/W	0h	Expand Own address 1
5	XOA2	R/W	0h	Expand Own address 2
4	XOA3	R/W	0h	Expand Own address 3
3:2	RESERVED1	R	0h	Reserved

Table 14-10724. I2C_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	STP	R/W	0h	Stop condition [controller mode only]
0	STT	R/W	0h	Start condition [controller mode only]

14.7.2.2.2.23 I2C_OA Register

14.7.2.2.2.23.1 I2C_OA Register (Offset = A8h) [reset = 0h]

Own address register

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Table 14-10725. Instance Table

Instance Name	Physical Address
I2C0	2000 00A8h
I2C1	2001 00A8h
I2C2	2002 00A8h
I2C3	2003 00A8h
I2C4	2004 00A8h
I2C5	2005 00A8h
I2C6	2006 00A8h
WKUP_I2C0	2B20 00A8h

Figure 14-5302. I2C_OA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">MCODE</td><td colspan="3">RESERVED</td><td colspan="2">OA</td></tr>
<tr><td colspan="3">R/W</td><td colspan="3">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="3">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10726. I2C_OA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	MCODE	R/W	0h	Controller Code
12:10	RESERVED	R	0h	Reserved
9:0	OA	R/W	0h	Own address

14.7.2.2.2.24 I2C_SA Register

14.7.2.2.2.24.1 I2C_SA Register (Offset = ACh) [reset = 3FFh]

Target address register

Return to Summary Table

Table 14-10727. Instance Table

Instance Name	Physical Address
I2C0	2000 00ACh
I2C1	2001 00ACh
I2C2	2002 00ACh
I2C3	2003 00ACh
I2C4	2004 00ACh
I2C5	2005 00ACh
I2C6	2006 00ACh
WKUP_I2C0	2B20 00ACh

Figure 14-5303. I2C_SA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						SA	
R						R/W	
0h						3FFh	
7	6	5	4	3	2	1	0
SA							
R/W							
3FFh							

Table 14-10728. I2C_SA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED	R	0h	Reserved
9:0	SA	R/W	3FFh	Target address

14.7.2.2.2.25 I2C_PSC Register

14.7.2.2.2.25.1 I2C_PSC Register (Offset = B0h) [reset = 0h]

I2C Clock Prescaler Register

Return to Summary Table

Table 14-10729. Instance Table

Instance Name	Physical Address
I2C0	2000 00B0h
I2C1	2001 00B0h
I2C2	2002 00B0h
I2C3	2003 00B0h
I2C4	2004 00B0h
I2C5	2005 00B0h
I2C6	2006 00B0h
WKUP_I2C0	2B20 00B0h

Figure 14-5304. I2C_PSC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PSC							
R/W							
0h							

Table 14-10730. I2C_PSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RESERVED	R	0h	Reserved
7:0	PSC	R/W	0h	Fast/Standard mode prescale sampling clock divider value 0x0: Divide by 1 0x1: Divide by 2 0xFF: Divide by 256

14.7.2.2.2.26 I2C_SCLL Register

14.7.2.2.2.26.1 I2C_SCLL Register (Offset = B4h) [reset = 0h]

I2C SCL Low Time Register.

Return to Summary Table

Table 14-10731. Instance Table

Instance Name	Physical Address
I2C0	2000 00B4h
I2C1	2001 00B4h
I2C2	2002 00B4h
I2C3	2003 00B4h
I2C4	2004 00B4h
I2C5	2005 00B4h
I2C6	2006 00B4h
WKUP_I2C0	2B20 00B4h

Figure 14-5305. I2C_SCLL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">HSSCLL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SCLL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10732. I2C_SCLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSSCLL	R/W	0h	High Speed mode SCL low time
7:0	SCLL	R/W	0h	Fast/Standard mode SCL low time

14.7.2.2.2.27 I2C_SCLH Register

14.7.2.2.2.27.1 I2C_SCLH Register (Offset = B8h) [reset = 0h]

I2C SCL High Time Register.

Return to Summary Table

Table 14-10733. Instance Table

Instance Name	Physical Address
I2C0	2000 00B8h
I2C1	2001 00B8h
I2C2	2002 00B8h
I2C3	2003 00B8h
I2C4	2004 00B8h
I2C5	2005 00B8h
I2C6	2006 00B8h
WKUP_I2C0	2B20 00B8h

Figure 14-5306. I2C_SCLH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">HSSCLH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SCLH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10734. I2C_SCLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSSCLH	R/W	0h	High Speed mode SCL high time
7:0	SCLH	R/W	0h	Fast/Standard mode SCL high time

14.7.2.2.2.28 I2C_SYSTEST Register

14.7.2.2.2.28.1 I2C_SYSTEST Register (Offset = BCh) [reset = 1E0h]

I2C System Test Register.

Return to Summary Table

Table 14-10735. Instance Table

Instance Name	Physical Address
I2C0	2000 00BCh
I2C1	2001 00BCh
I2C2	2002 00BCh
I2C3	2003 00BCh
I2C4	2004 00BCh
I2C5	2005 00BCh
I2C6	2006 00BCh
WKUP_I2C0	2B20 00BCh

Figure 14-5307. I2C_SYSTEST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ST_EN	FREE	TMODE		SSB	RESERVED		SCL_I_FUNC
R/W	R/W	R/W		R/W	R		R
0h	0h	0h		0h	0h		1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SCL_O_FUNC	SDA_I_FUNC	SDA_O_FUNC	SCCB_E_O	SCL_I	SCL_O	SDA_I	SDA_O
R	R	R	R/W	R	R/W	R	R/W
1h	1h	1h	0h	0h	0h	0h	0h

Table 14-10736. I2C_SYSTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	ST_EN	R/W	0h	System test enable
14	FREE	R/W	0h	Free running mode [on breakpoint]
13:12	TMODE	R/W	0h	Test mode select
11	SSB	R/W	0h	Set status bits
10:9	RESERVED	R	0h	Reserved
8	SCL_I_FUNC	R	1h	SCL line input value [functional mode]
7	SCL_O_FUNC	R	1h	SCL line output value [functional mode]
6	SDA_I_FUNC	R	1h	SDA line input value [functional mode]
5	SDA_O_FUNC	R	1h	SDA line output value [functional mode]
4	SCCB_E_O	R/W	0h	SCCB_E line sense output value
3	SCL_I	R	0h	SCL line sense input value
2	SCL_O	R/W	0h	SCL line drive output value

Table 14-10736. I2C_SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SDA_I	R	0h	SDA line sense input value
0	SDA_O	R/W	0h	SDA line drive output value

14.7.2.2.2.29 I2C_BUFSTAT Register

14.7.2.2.2.29.1 I2C_BUFSTAT Register (Offset = C0h) [reset = 8000h]

I2C Buffer Status Register.

Return to Summary Table

Table 14-10737. Instance Table

Instance Name	Physical Address
I2C0	2000 00C0h
I2C1	2001 00C0h
I2C2	2002 00C0h
I2C3	2003 00C0h
I2C4	2004 00C0h
I2C5	2005 00C0h
I2C6	2006 00C0h
WKUP_I2C0	2B20 00C0h

Figure 14-5308. I2C_BUFSTAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">FIFODEPTH</td><td colspan="6">RXSTAT</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">2h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TXSTAT</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-10738. I2C_BUFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:14	FIFODEPTH	R	2h	Internal FIFO buffers depth
13:8	RXSTAT	R	0h	RX Buffer Status
7:6	RESERVED	R	0h	Reserved
5:0	TXSTAT	R	0h	TX Buffer Status

14.7.2.2.2.30 I2C_OA1 Register

14.7.2.2.2.30.1 I2C_OA1 Register (Offset = C4h) [reset = 0h]

I2C Own Address 1 Register

Return to Summary Table

Table 14-10739. Instance Table

Instance Name	Physical Address
I2C0	2000 00C4h
I2C1	2001 00C4h
I2C2	2002 00C4h
I2C3	2003 00C4h
I2C4	2004 00C4h
I2C5	2005 00C4h
I2C6	2006 00C4h
WKUP_I2C0	2B20 00C4h

Figure 14-5309. I2C_OA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						OA1	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
OA1							
R/W							
0h							

Table 14-10740. I2C_OA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED	R	0h	Reserved
9:0	OA1	R/W	0h	Own address 1

14.7.2.2.2.31 I2C_OA2 Register

14.7.2.2.2.31.1 I2C_OA2 Register (Offset = C8h) [reset = 0h]

I2C Own Address 2 Register

Return to Summary Table

Table 14-10741. Instance Table

Instance Name	Physical Address
I2C0	2000 00C8h
I2C1	2001 00C8h
I2C2	2002 00C8h
I2C3	2003 00C8h
I2C4	2004 00C8h
I2C5	2005 00C8h
I2C6	2006 00C8h
WKUP_I2C0	2B20 00C8h

Figure 14-5310. I2C_OA2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						OA2	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
OA2							
R/W							
0h							

Table 14-10742. I2C_OA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED	R	0h	Reserved
9:0	OA2	R/W	0h	Own address 2

14.7.2.2.2.32 I2C_OA3 Register

14.7.2.2.2.32.1 I2C_OA3 Register (Offset = CCh) [reset = 0h]

I2C Own Address 3 Register

Return to Summary Table

Table 14-10743. Instance Table

Instance Name	Physical Address
I2C0	2000 00CCh
I2C1	2001 00CCh
I2C2	2002 00CCh
I2C3	2003 00CCh
I2C4	2004 00CCh
I2C5	2005 00CCh
I2C6	2006 00CCh
WKUP_I2C0	2B20 00CCh

Figure 14-5311. I2C_OA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">OA3</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OA3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10744. I2C_OA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:10	RESERVED	R	0h	Reserved
9:0	OA3	R/W	0h	Own address 3

14.7.2.2.2.33 I2C_ACTOA Register

14.7.2.2.2.33.1 I2C_ACTOA Register (Offset = D0h) [reset = 0h]

I2C Active Own Address Register.

Return to Summary Table

Table 14-10745. Instance Table

Instance Name	Physical Address
I2C0	2000 00D0h
I2C1	2001 00D0h
I2C2	2002 00D0h
I2C3	2003 00D0h
I2C4	2004 00D0h
I2C5	2005 00D0h
I2C6	2006 00D0h
WKUP_I2C0	2B20 00D0h

Figure 14-5312. I2C_ACTOA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>OA3_ACT</td><td>OA2_ACT</td><td>OA1_ACT</td><td>OA0_ACT</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10746. I2C_ACTOA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:4	RESERVED	R	0h	Reserved
3	OA3_ACT	R	0h	Own Address 3 active
2	OA2_ACT	R	0h	Own Address 2 active
1	OA1_ACT	R	0h	Own Address 1 active
0	OA0_ACT	R	0h	Own Address 0 active

14.7.2.2.2.34 I2C_SBLOCK Register

14.7.2.2.2.34.1 I2C_SBLOCK Register (Offset = D4h) [reset = 0h]

I2C Clock Blocking Enable Register.

Return to Summary Table

Table 14-10747. Instance Table

Instance Name	Physical Address
I2C0	2000 00D4h
I2C1	2001 00D4h
I2C2	2002 00D4h
I2C3	2003 00D4h
I2C4	2004 00D4h
I2C5	2005 00D4h
I2C6	2006 00D4h
WKUP_I2C0	2B20 00D4h

Figure 14-5313. I2C_SBLOCK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				OA3_EN	OA2_EN	OA1_EN	OA0_EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-10748. I2C_SBLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:4	RESERVED	R	0h	Reserved
3	OA3_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 3
2	OA2_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 2
1	OA1_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 1
0	OA0_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 0

14.7.2.3 MCSPI

MCSPI

14.7.2.3.1 MCSPI Summaries

MCSPI Summaries

Table 14-10749. MCSPI Registers, Base Address=2010 0000h, Length=1024

Offset	Length	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
0h	32	MCSPI_HL_REV	2010 0000h	2011 0000h	2012 0000h
4h	32	MCSPI_HL_HWINFO	2010 0004h	2011 0004h	2012 0004h
10h	32	MCSPI_HL_SYSCONFIG	2010 0010h	2011 0010h	2012 0010h
100h	32	MCSPI_REVISION	2010 0100h	2011 0100h	2012 0100h
110h	32	MCSPI_SYSCONFIG	2010 0110h	2011 0110h	2012 0110h
114h	32	MCSPI_SYSSTATUS	2010 0114h	2011 0114h	2012 0114h
118h	32	MCSPI_IRQSTATUS	2010 0118h	2011 0118h	2012 0118h
11Ch	32	MCSPI_IRQENABLE	2010 011Ch	2011 011Ch	2012 011Ch
120h	32	MCSPI_WAKEUPENABLE	2010 0120h	2011 0120h	2012 0120h
124h	32	MCSPI_SYST	2010 0124h	2011 0124h	2012 0124h
128h	32	MCSPI_MODULCTRL	2010 0128h	2011 0128h	2012 0128h
12Ch	32	MCSPI_CH0CONF	2010 012Ch	2011 012Ch	2012 012Ch
130h	32	MCSPI_CH0STAT	2010 0130h	2011 0130h	2012 0130h
134h	32	MCSPI_CH0CTRL	2010 0134h	2011 0134h	2012 0134h
138h	32	MCSPI_TX0	2010 0138h	2011 0138h	2012 0138h
13Ch	32	MCSPI_RX0	2010 013Ch	2011 013Ch	2012 013Ch
140h	32	MCSPI_CH1CONF	2010 0140h	2011 0140h	2012 0140h
144h	32	MCSPI_CH1STAT	2010 0144h	2011 0144h	2012 0144h
148h	32	MCSPI_CH1CTRL	2010 0148h	2011 0148h	2012 0148h
14Ch	32	MCSPI_TX1	2010 014Ch	2011 014Ch	2012 014Ch
150h	32	MCSPI_RX1	2010 0150h	2011 0150h	2012 0150h
154h	32	MCSPI_CH2CONF	2010 0154h	2011 0154h	2012 0154h
158h	32	MCSPI_CH2STAT	2010 0158h	2011 0158h	2012 0158h
15Ch	32	MCSPI_CH2CTRL	2010 015Ch	2011 015Ch	2012 015Ch
160h	32	MCSPI_TX2	2010 0160h	2011 0160h	2012 0160h
164h	32	MCSPI_RX2	2010 0164h	2011 0164h	2012 0164h
168h	32	MCSPI_CH3CONF	2010 0168h	2011 0168h	2012 0168h
16Ch	32	MCSPI_CH3STAT	2010 016Ch	2011 016Ch	2012 016Ch
170h	32	MCSPI_CH3CTRL	2010 0170h	2011 0170h	2012 0170h
174h	32	MCSPI_TX3	2010 0174h	2011 0174h	2012 0174h
178h	32	MCSPI_RX3	2010 0178h	2011 0178h	2012 0178h
17Ch	32	MCSPI_XFERLEVEL	2010 017Ch	2011 017Ch	2012 017Ch
180h	32	MCSPI_DAFTX	2010 0180h	2011 0180h	2012 0180h
1A0h	32	MCSPI_DAFRX	2010 01A0h	2011 01A0h	2012 01A0h

Table 14-10750. MCSPI Registers, Base Address=2010 0000h, Length=1024

Offset	Length	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address
0h	32	MCSPI_HL_REV	2013 0000h	2014 0000h
4h	32	MCSPI_HL_HWINFO	2013 0004h	2014 0004h

Table 14-10750. MCSPI Registers, Base Address=2010 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address
10h	32	MCSPI_HL_SYSCONFIG	2013 0010h	2014 0010h
100h	32	MCSPI_REVISION	2013 0100h	2014 0100h
110h	32	MCSPI_SYSCONFIG	2013 0110h	2014 0110h
114h	32	MCSPI_SYSSTATUS	2013 0114h	2014 0114h
118h	32	MCSPI_IRQSTATUS	2013 0118h	2014 0118h
11Ch	32	MCSPI_IRQENABLE	2013 011Ch	2014 011Ch
120h	32	MCSPI_WAKEUPENABLE	2013 0120h	2014 0120h
124h	32	MCSPI_SYST	2013 0124h	2014 0124h
128h	32	MCSPI_MODULCTRL	2013 0128h	2014 0128h
12Ch	32	MCSPI_CH0CONF	2013 012Ch	2014 012Ch
130h	32	MCSPI_CH0STAT	2013 0130h	2014 0130h
134h	32	MCSPI_CH0CTRL	2013 0134h	2014 0134h
138h	32	MCSPI_TX0	2013 0138h	2014 0138h
13Ch	32	MCSPI_RX0	2013 013Ch	2014 013Ch
140h	32	MCSPI_CH1CONF	2013 0140h	2014 0140h
144h	32	MCSPI_CH1STAT	2013 0144h	2014 0144h
148h	32	MCSPI_CH1CTRL	2013 0148h	2014 0148h
14Ch	32	MCSPI_TX1	2013 014Ch	2014 014Ch
150h	32	MCSPI_RX1	2013 0150h	2014 0150h
154h	32	MCSPI_CH2CONF	2013 0154h	2014 0154h
158h	32	MCSPI_CH2STAT	2013 0158h	2014 0158h
15Ch	32	MCSPI_CH2CTRL	2013 015Ch	2014 015Ch
160h	32	MCSPI_TX2	2013 0160h	2014 0160h
164h	32	MCSPI_RX2	2013 0164h	2014 0164h
168h	32	MCSPI_CH3CONF	2013 0168h	2014 0168h
16Ch	32	MCSPI_CH3STAT	2013 016Ch	2014 016Ch
170h	32	MCSPI_CH3CTRL	2013 0170h	2014 0170h
174h	32	MCSPI_TX3	2013 0174h	2014 0174h
178h	32	MCSPI_RX3	2013 0178h	2014 0178h
17Ch	32	MCSPI_XFERLEVEL	2013 017Ch	2014 017Ch
180h	32	MCSPI_DAFTX	2013 0180h	2014 0180h
1A0h	32	MCSPI_DAFRX	2013 01A0h	2014 01A0h

14.7.2.3.2 MCSPI Registers

MCSPI Registers

14.7.2.3.2.1 MCSPI_HL_REV Register

14.7.2.3.2.1.1 MCSPI_HL_REV Register (Offset = 0h) [reset = 40301A0Bh]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-10751. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0000h
MCSPI1	2011 0000h
MCSPI2	2012 0000h
MCSPI3	2013 0000h
MCSPI4	2014 0000h

Figure 14-5314. MCSPI_HL_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		RSVD		FUNC			
R		R		R			
1h		0h		30h			

23	22	21	20	19	18	17	16
FUNC							
R							
30h							

15	14	13	12	11	10	9	8
R_RTL					X_MAJOR		
R					R		
3h					2h		

7	6	5	4	3	2	1	0
CUSTOM		Y_MINOR					
R		R					
0h		Bh					

Table 14-10752. MCSPI_HL_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old scheme and current
29:28	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
27:16	FUNC	R	30h	Function indicates a software compatible module family If there is no level of software compatibility a new Func number [and hence REVISION] should be assigned
15:11	R_RTL	R	3h	RTL Version [R], maintained by IP design owner RTL follows a numbering such as XYRZ which are explained in this table R changes ONLY when: [1] PDS uploads occur which may have been due to spec changes [2] Bug fixes occur [3] Resets to '0' when X or Y changes Design team has an internal 'Z' [customer invisible] number which increments on every drop that happens due to DV and RTL updates Z resets to 0 when R increments
10:8	X_MAJOR	R	2h	Major Revision [X], maintained by IP specification owner X changes ONLY when: [1] There is a major feature addition An example would be adding Controller Mode to Utopia Level2 The Func field [or Class/Type in old PID format] will remain the same X does NOT change due to: [1] Bug fixes [2] Change in feature parameters
7:6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers

Table 14-10752. MCSPI_HL_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	Y_MINOR	R	Bh	Minor Revision [Y], maintained by IP specification owner Y changes ONLY when: [1] Features are scaled [up or down] Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available [2] When feature creeps from Is-Not list to Is list But this may not be the case once it sees silicon; in which case X will change Y does NOT change due to: [1] Bug fixes [2] Typos or clarifications [3] major functional/feature change/addition/ deletion Instead these changes may be reflected via R, S, X as applicable Spec owner maintains a customer-invisible number 'S' which changes due to: [1] Typos/clarifications [2] Bug documentation Note that this bug is not due to a spec change but due to implementation Nevertheless, the spec tracks the IP bugs An RTL release [say for silicon PG11] that occurs due to bug fix should document the corresponding spec number [XYS] in its release notes

14.7.2.3.2.2 MCSPI_HL_HWINFO Register

14.7.2.3.2.2.1 MCSPI_HL_HWINFO Register (Offset = 4h) [reset = 9h]

Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

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Table 14-10753. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0004h
MCSPI1	2011 0004h
MCSPI2	2012 0004h
MCSPI3	2013 0004h
MCSPI4	2014 0004h

Figure 14-5315. MCSPI_HL_HWINFO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RSVD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RSVD</td><td>RETMODE</td><td colspan="5">FFNBYTE</td><td>USEFIFO</td></tr>
<tr><td>R</td><td>R</td><td colspan="5">R</td><td>R</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">4h</td><td>1h</td></tr>
</table>

Table 14-10754. MCSPI_HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
6	RETMODE	R	0h	This bit field indicates whether the retention mode is supported using the pin PIRFFRET 0 `Retention mode disabled` 1 `Retention mode enabled`
5:1	FFNBYTE	R	4h	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account 1 `FIFO 16 bytes depth` 2 `FIFO 32 bytes depth` 4 `FIFO 64 bytes depth` 8 `FIFO 128 bytes depth` 10 `FIFO 256 bytes depth`

Table 14-10754. MCSPI_HL_HWINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	USEFIFO	R	1h	Use of a FIFO enable: This bit field indicates if a FIFO is integrated within controller design with its management 0 `FIFO not implemented in design` 1 `FIFO and its management implemented in design with depth defined by FFNBYTE generic`

14.7.2.3.2.3 MCSPI_HL_SYSCONFIG Register

14.7.2.3.2.3.1 MCSPI_HL_SYSCONFIG Register (Offset = 10h) [reset = 8h]

Clock management configuration

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Table 14-10755. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0010h
MCSPI1	2011 0010h
MCSPI2	2012 0010h
MCSPI3	2013 0010h
MCSPI4	2014 0010h

Figure 14-5316. MCSPI_HL_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD				IDLEMODE		FREEEMU	SOFTRESET
R				R/W		R/W	R/W
0h				2h		0h	0h

Table 14-10756. MCSPI_HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD	R	0h	Reserved
3:2	IDLEMODE	R/W	2h	Configuration of the local target state management mode By definition, target can handle read/write transaction as long as it is out of IDLE state 0 Force-idle mode: local target's IDLE state follows (acknowledges) the system's clock stop requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 1 No-idle mode: local target never enters IDLE state. Backup mode, for debug only. 2 Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events. 3 Smart-idle wake-up-capable mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state.

Table 14-10756. MCSPI_HL_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FREEEMU	R/W	0h	Sensitivity to emulation [debug] suspend input signal 0 `IP module is sensitive to emulation suspend.` 1 `IP module is not sensitive to emulation suspend.`
0	SOFTRESET	R/W	0h	Software reset [Optional] 0 `Reset done, no pending action` 1 `Initiate software reset`

14.7.2.3.2.4 MCSPI_REVISION Register

14.7.2.3.2.4.1 MCSPI_REVISION Register (Offset = 100h) [reset = 2Bh]

This register contains the hard coded RTL revision number.

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Table 14-10757. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0100h
MCSPI1	2011 0100h
MCSPI2	2012 0100h
MCSPI3	2013 0100h
MCSPI4	2014 0100h

Figure 14-5317. MCSPI_REVISION Name Register

31	30	29	28	27	26	25	24
RESERVED_13							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_13							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_13							
R							
0h							
7	6	5	4	3	2	1	0
REV							
R							
2Bh							

Table 14-10758. MCSPI_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_13	R	0h	Reads returns 0
7:0	REV	R	2Bh	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 10, 0x21 for 21

14.7.2.3.2.5 MCSPI_SYSCONFIG Register

14.7.2.3.2.5.1 MCSPI_SYSCONFIG Register (Offset = 110h) [reset = 15h]

This register allows controlling various parameters of the OCP interface.

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Table 14-10759. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0110h
MCSPI1	2011 0110h
MCSPI2	2012 0110h
MCSPI3	2013 0110h
MCSPI4	2014 0110h

Figure 14-5318. MCSPI_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_14							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_14							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_14						CLOCKACTIVITY	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED_15			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R			R/W		R/W	R/W	R/W
0h			2h		1h	0h	1h

Table 14-10760. MCSPI_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_14	R	0h	Reads returns 0
9:8	CLOCKACTIVITY	R/W	0h	Clocks activity during wake up mode period 0 `Interface and functional clocks may be switched off.` 1 `Interface clock is maintained. Functional clock may be switched off.` 2 `Functional clock is maintained. Interface clock may be switched off.` 3 `Interface and functional clocks are maintained.`
7:5	RESERVED_15	R	0h	Reads returns 0

Table 14-10760. MCSPI_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	SIDLEMODE	R/W	2h	Power management 0 If an IDLE request is detected, the MCSPI acknowledges it unconditionally and goes in inactive mode. Interrupt, DMA requests and wake-up lines are unconditionally deasserted and the module wake-up capability is deactivated even if the MCSPI_SYSCONFIG[2] ENAWAKEUP bit is set. 1 If an IDLE request is detected, the request is ignored and the module does not switch to wake-up mode, and keeps on behaving normally. 2 If an IDLE request is detected, the module will switch to wake-up mode based on its internal activity, and the wake-up capability can be used if the bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set. 3 Reserved - do not use.
2	ENAWAKEUP	R/W	1h	WakeUp feature control 0 Wake-up capability is disabled. 1 Wake-up capability is enabled.
1	SOFTRESET	R/W	0h	Software reset During reads it always returns 0 0 (write) Normal mode 1 (write) Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware.
0	AUTOIDLE	R/W	1h	Internal OCP Clock gating strategy 0 Interface clock is free-running. 1 Automatic interface clock gating strategy is applied, based on the configuration interface activity.

14.7.2.3.2.6 MCSPI_SYSSTATUS Register

14.7.2.3.2.6.1 MCSPI_SYSSTATUS Register (Offset = 114h) [reset = 1h]

This register provides status information about the module excluding the interrupt status information

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Table 14-10761. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0114h
MCSPI1	2011 0114h
MCSPI2	2012 0114h
MCSPI3	2013 0114h
MCSPI4	2014 0114h

Figure 14-5319. MCSPI_SYSSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_16							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_16							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_16							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_16							RESETDONE
R							R
0h							1h

Table 14-10762. MCSPI_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_16	R	0h	Reserved for module specific status information Read returns 0

0	RESETDONE	R	1h	Internal Reset Monitoring
				`0 Internal module reset is ongoing`
				`1 Reset completed`

14.7.2.3.2.7 MCSPI_IRQSTATUS Register

14.7.2.3.2.7.1 MCSPI_IRQSTATUS Register (Offset = 118h) [reset = 0h]

The interrupt status regroups all the status of the module internal events that can generate an interrupt

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Table 14-10763. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0118h
MCSPI1	2011 0118h
MCSPI2	2012 0118h
MCSPI3	2013 0118h
MCSPI4	2014 0118h

Figure 14-5320. MCSPI_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_8							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_8						EOW	WKS
R						R/W1TS	R/W1TS
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED_7	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED_9	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY
R	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_10	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY
R	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10764. MCSPI_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_8	R	0h	Reads returns 0

17	EOW	R/W1TS	0h	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT]
				`0 Event false`
				`1 Event status bit is reset`

16	WKS	R/W1TS	0h	Wake Up event in target mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]
				`0 Event status bit unchanged`
				`1 Event is pending`

15	RESERVED_7	R	0h	Reads returns 0

14	RX3_FULL	R/W1TS	0h	Receiver register is full or almost full Only when Channel 3 is enabled
				`0 Event status bit unchanged`
				`1 Event is pending`

Table 14-10764. MCSPI_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TX3_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Only when Channel 3 is enabled The transmitter register is empty [not updated by Host or DMA with new data] before its time slot assignment Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled 0 Event status bit unchanged 1 Event is pending
12	TX3_EMPTY	R/W1TS	0h	Transmitter register is empty or almost empty Note: Enabling the channel automatically rises this event 0 Event status bit unchanged 1 Event is pending
11	RESERVED_9	R	0h	Reads returns 0
10	RX2_FULL	R/W1TS	0h	Receiver register full or almost full Channel 2 0 Event status bit unchanged 1 Event is pending
9	TX2_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 2 0 Event status bit unchanged 1 Event is pending
8	TX2_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 2 0 Event status bit unchanged 1 Event is pending
7	RESERVED_10	R	0h	Reads returns 0
6	RX1_FULL	R/W1TS	0h	Receiver register full or almost full Channel 1 0 Event status bit unchanged 1 Event is pending
5	TX1_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 1 0 Event status bit unchanged 1 Event is pending
4	TX1_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 1 0 Event status bit unchanged 1 Event is pending
3	RX0_OVERFLOW	R/W1TS	0h	Receiver register overflow [target mode only] Channel 0 0 Event status bit unchanged 1 Event is pending
2	RX0_FULL	R/W1TS	0h	Receiver register full or almost full Channel 0 0 Event status bit unchanged 1 Event is pending
1	TX0_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 0 0 Event status bit unchanged 1 Event is pending
0	TX0_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 0 0 Event status bit unchanged 1 Event is pending

14.7.2.3.2.8 MCSPI_IRQENABLE Register

14.7.2.3.2.8.1 MCSPI_IRQENABLE Register (Offset = 11Ch) [reset = 0h]

This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.

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Table 14-10765. Instance Table

Instance Name	Physical Address
MCSPI0	2010 011Ch
MCSPI1	2011 011Ch
MCSPI2	2012 011Ch
MCSPI3	2013 011Ch
MCSPI4	2014 011Ch

Figure 14-5321. MCSPI_IRQENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED_5							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_5						EOW_ENABLE	WKE
R						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED_4	RX3_FULL_ENABLE	TX3_UNDERFLOW_ENABLE	TX3_EMPTY_ENABLE	RESERVED_6	RX2_FULL_ENABLE	TX2_UNDERFLOW_ENABLE	TX2_EMPTY_ENABLE
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_3	RX1_FULL_ENABLE	TX1_UNDERFLOW_ENABLE	TX1_EMPTY_ENABLE	RX0_OVERFLOW_ENABLE	RX0_FULL_ENABLE	TX0_UNDERFLOW_ENABLE	TX0_EMPTY_ENABLE
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10766. MCSPI_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_5	R	0h	Reads return 0
17	EOW_ENABLE	R/W	0h	End of Word count Interrupt Enable 0 Interrupt disabled 1 Interrupt enabled
16	WKE	R/W	0h	Wake Up event interrupt Enable in target mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 Interrupt disabled 1 Interrupt enabled
15	RESERVED_4	R	0h	Reads returns 0
14	RX3_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 3 0 Interrupt disabled 1 Interrupt enabled
13	TX3_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 3 0 Interrupt disabled 1 Interrupt enabled

Table 14-10766. MCSPI_IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	TX3_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch3 0 `Interrupt disabled` 1 `Interrupt enabled`
11	RESERVED_6	R	0h	Reads return 0
10	RX2_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
9	TX2_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
8	TX2_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 2 0 `Interrupt disabled` 1 `Interrupt enabled`
7	RESERVED_3	R	0h	Reads return 0
6	RX1_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
5	TX1_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
4	TX1_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 1 0 `Interrupt disabled` 1 `Interrupt enabled`
3	RX0_OVERFLOW_ENABLE	R/W	0h	Receiver register Overflow Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
2	RX0_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
1	TX0_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`
0	TX0_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 0 0 `Interrupt disabled` 1 `Interrupt enabled`

14.7.2.3.2.9 MCSPI_WAKEUPENABLE Register

14.7.2.3.2.9.1 MCSPI_WAKEUPENABLE Register (Offset = 120h) [reset = 0h]

The wakeup enable register allows to enable/disable the module internal sources of wakeup on event-by-event basis.

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Table 14-10767. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0120h
MCSPI1	2011 0120h
MCSPI2	2012 0120h
MCSPI3	2013 0120h
MCSPI4	2014 0120h

Figure 14-5322. MCSPI_WAKEUPENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED_18							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_18							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_18							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_18							WKEN
R							R/W
0h							0h

Table 14-10768. MCSPI_WAKEUPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_18	R	0h	Reads returns 0
0	WKEN	R/W	0h	WakeUp functionality in target mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 `The event is not allowed to wake-up the system, even if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUPis set.` 1 `The event is allowed to wake-up the system if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set.`

14.7.2.3.2.10 MCSPI_SYST Register

14.7.2.3.2.10.1 MCSPI_SYST Register (Offset = 124h) [reset = 0h]

This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.

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Table 14-10769. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0124h
MCSPI1	2011 0124h
MCSPI2	2012 0124h
MCSPI3	2013 0124h
MCSPI4	2014 0124h

Figure 14-5323. MCSPI_SYST Name Register

31	30	29	28	27	26	25	24
RESERVED_17							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_17							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_17				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10770. MCSPI_SYST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_17	R	0h	Reads returns 0
11	SSB	R/W	0h	Set status bit 0 No action. Writing 0 does not clear already set status bits. This bit must be cleared before trying to clear a status bit of the MCSPI_IRQSTATUS register. 1 Force to 1 all status bits of MCSPI_IRQSTATUS register. Writing 1 into this bit sets to 1 all status bits in the MCSPI_IRQSTATUS register.
10	SPIENDIR	R/W	0h	Set the direction of the SPIEN[3:0] lines and SPICLK line 0 Output (as in controller mode) 1 Input (as in peripheral mode)
9	SPIDATDIR1	R/W	0h	Set the direction of the SPIDAT[1] 0 Output 1 Input

Table 14-10770. MCSPI_SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SPIDATDIR0	R/W	0h	Set the direction of the SPIDAT[0] 0 Output 1 Input
7	WAKD	R/W	0h	SWAKEUP output [signal data value of internal signal to system] The signal is driven high or low according to the value written into this register bit 0 The pin is driven low. 1 The pin is driven high.
6	SPICLK	R/W	0h	SPICLK line [signal data value] If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the CLKSPI line [high or low], and a write into this bit has no effect If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the CLKSPI line is driven high or low according to the value written into this register
5	SPIDAT_1	R/W	0h	SPIDAT[1] line [signal data value] If MCSPI_SYST[SPIDATDIR1] = 0 [output mode direction], the SPIDAT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR1] = 1 [input mode direction], this bit returns the value on the SPIDAT[1] line [high or low], and a write into this bit has no effect
4	SPIDAT_0	R/W	0h	SPIDAT[0] line [signal data value] If MCSPI_SYST[SPIDATDIR0] = 0 [output mode direction], the SPIDAT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR0] = 1 [input mode direction], this bit returns the value on the SPIDAT[0] line [high or low], and a write into this bit has no effect
3	SPIEN_3	R/W	0h	SPIEN[3] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[3] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[3] line [high or low], and a write into this bit has no effect
2	SPIEN_2	R/W	0h	SPIEN[2] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[2] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[2] line [high or low], and a write into this bit has no effect
1	SPIEN_1	R/W	0h	SPIEN[1] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[1] line [high or low], and a write into this bit has no effect
0	SPIEN_0	R/W	0h	SPIEN[0] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[0] line [high or low], and a write into this bit has no effect

14.7.2.3.2.11 MCSPI_MODULCTRL Register

14.7.2.3.2.11.1 MCSPI_MODULCTRL Register (Offset = 128h) [reset = 4h]

This register is dedicated to the configuration of the serial port interface.

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Table 14-10771. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0128h
MCSPI1	2011 0128h
MCSPI2	2012 0128h
MCSPI3	2013 0128h
MCSPI4	2014 0128h

Figure 14-5324. MCSPI_MODULCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_11							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_11							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_11							FDAA
R							R/W
0h							0h
7	6	5	4	3	2	1	0
MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			0h	1h	0h	0h

Table 14-10772. MCSPI_MODULCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_11	R	0h	Reads returns 0
8	FDAA	R/W	0h	FIFO DMA Address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256 bit aligned address If this bit is set the enabled channel which uses the FIFO has its datas managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX[i] and MCSPI_RX[i] registers 0 `FIFO data managed by MCSPI_TX(i) and MCSPI_RX(i) registers.` 1 `FIFO data managed by MCSPI_DAFTX and MCSPI_DAFRX registers.`
7	MOA	R/W	0h	Multiple word ocp access: This register can only be used when a channel is enabled using a FIFO It allows the system to perform multiple SPI word access for a single 32-bit OCP word access This is possible for WL < 16 0 `Multiple word access disabled` 1 `Multiple word access enabled with FIFO`

Table 14-10772. MCSPI_MODULCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	INITDLY	R/W	0h	Initial spi delay for first transfer: This register is an option only available in SINGLE controller mode, The controller waits for a delay to transmit the first spi word after channel enabled and corresponding TX register filled This Delay is based on SPI output frequency clock, No clock output provided to the boundary and chip select is not active in 4 pin mode within this period 0 `No delay for first MCSPI transfer.` 1 `The controller wait 4 MCSPI bus clock` 2 `The controller wait 8 MCSPI bus clock` 3 `The controller wait 16 MCSPI bus clock` 4 `The controller wait 32 MCSPI bus clock`
3	SYSTEM_TEST	R/W	0h	Enables the system test mode 0 `Functional mode` 1 `System test mode (SYSTEST)`
2	MS	R/W	1h	Controller/ Target 0 `Controller - The module generates the SPICLK and SPIEN[3:0].` 1 `Peripheral - The module receives the SPICLK and SPIEN[3:0].`
1	PIN34	R/W	0h	Pin mode selection: This register is used to configure the SPI pin mode, in controller or target mode If asserted the controller only use SIMO,SOMI and SPICLK clock pin for spi transfers 0 `SPIEN is used as a chip-select.` 1 `SPIEN is not used. In this mode all related options to chip-select have no meaning.`
0	SINGLE	R/W	0h	Single channel / Multi Channel [controller mode only] 0 `More than one channel will be used in controller mode.` 1 `Only one channel will be used in controller mode. This bit must be set in Force SPIEN[i] mode.`

14.7.2.3.2.12 MCSPI_CH0CONF Register

14.7.2.3.2.12.1 MCSPI_CH0CONF Register (Offset = 12Ch) [reset = 60000h]

This register is dedicated to the configuration of the channel 0

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Table 14-10773. Instance Table

Instance Name	Physical Address
MCSPI0	2010 012Ch
MCSPI1	2011 012Ch
MCSPI2	2012 012Ch
MCSPI3	2013 012Ch
MCSPI4	2014 012Ch

Figure 14-5325. MCSPI_CH0CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS0		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
R/W	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-10774. MCSPI_CH0CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.

Table 14-10774. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:25	TCS0	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	SPIENSLV	R/W	0h	Channel 0 only and target mode only: SPI target select signal detection Reserved bits for other cases 0 Detection enabled only on SPIEN[0] 1 Detection enabled only on SPIEN[1] 2 Detection enabled only on SPIEN[2] 3 Detection enabled only on SPIEN[3]
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled

Table 14-10774. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

Table 14-10774. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 1 2 2 4 3 8 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.7.2.3.2.13 MCSPI_CH0STAT Register

14.7.2.3.2.13.1 MCSPI_CH0STAT Register (Offset = 130h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 0

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Table 14-10775. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0130h
MCSPI1	2011 0130h
MCSPI2	2012 0130h
MCSPI3	2013 0130h
MCSPI4	2014 0130h

Figure 14-5326. MCSPI_CH0STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10776. MCSPI_CH0STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 FIFO receive buffer is not full 1 FIFO receive buffer is full
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 FIFO receive buffer is not empty 1 FIFO receive buffer is empty
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 FIFO transmit buffer is not full 1 FIFO transmit buffer is full
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 FIFO transmit buffer is not empty 1 FIFO transmit buffer is empty

Table 14-10776. MCSPI_CH0STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus target and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.7.2.3.2.14 MCSPI_CH0CTRL Register

14.7.2.3.2.14.1 MCSPI_CH0CTRL Register (Offset = 134h) [reset = 0h]

This register is dedicated to enable the channel 0

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Table 14-10777. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0134h
MCSPI1	2011 0134h
MCSPI2	2012 0134h
MCSPI3	2013 0134h
MCSPI4	2014 0134h

Figure 14-5327. MCSPI_CH0CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EXTCLK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED_1</td><td>EN</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-10778. MCSPI_CH0CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.7.2.3.2.15 MCSPI_TX0 Register

14.7.2.3.2.15.1 MCSPI_TX0 Register (Offset = 138h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-10779. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0138h
MCSPI1	2011 0138h
MCSPI2	2012 0138h
MCSPI3	2013 0138h
MCSPI4	2014 0138h

Figure 14-5328. MCSPI_TX0 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 14-10780. MCSPI_TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 0 Data to transmit

14.7.2.3.2.16 MCSPI_RX0 Register

14.7.2.3.2.16.1 MCSPI_RX0 Register (Offset = 13Ch) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-10781. Instance Table

Instance Name	Physical Address
MCSPI0	2010 013Ch
MCSPI1	2011 013Ch
MCSPI2	2012 013Ch
MCSPI3	2013 013Ch
MCSPI4	2014 013Ch

Figure 14-5329. MCSPI_RX0 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-10782. MCSPI_RX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 0 Received Data

14.7.2.3.2.17 MCSPI_CH1CONF Register

14.7.2.3.2.17.1 MCSPI_CH1CONF Register (Offset = 140h) [reset = 60000h]

This register is dedicated to the configuration of the channel.

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Table 14-10783. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0140h
MCSPI1	2011 0140h
MCSPI2	2012 0140h
MCSPI3	2013 0140h
MCSPI4	2014 0140h

Figure 14-5330. MCSPI_CH1CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS1		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	22	21	20	19	18	17	16
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	14	13	12	11	10	9	8
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	6	5	4	3	2	1	0
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-10784. MCSPI_CH1CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.

Table 14-10784. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:25	TCS1	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 `0.5 clock cycle` 1 `1.5 clock cycles` 2 `2.5 clock cycles` 3 `3.5 clock cycles`
24	SBPOL	R/W	0h	Start bit polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 `Default MCSPI transfer length as specified by WL bit field` 1 `Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL`
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 `Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.` 1 `Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.`
19	TURBO	R/W	0h	Turbo mode 0 `Turbo is deactivated (recommended for single MCSPI word transfer).` 1 `Turbo is activated to maximize the throughput for multiple MCSPI words transfer.`
18	IS	R/W	1h	Input Select 0 `Data line 0 (SPIDAT[0]) selected for reception` 1 `Data line 1 (SPIDAT[1]) selected for reception`
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 `Data line 1 (SPIDAT[1]) selected for transmission` 1 `No transmission on Data Line1 (SPIDAT[1])`
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 `Data Line0 (SPIDAT[0]) selected for transmission` 1 `No transmission on data line 0 (SPIDAT[0])`
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 `DMA read request disabled` 1 `DMA read request enabled`
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 `DMA write request disabled` 1 `DMA write request enabled`

Table 14-10784. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

Table 14-10784. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 1 2 2 4 3 8 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.7.2.3.2.18 MCSPI_CH1STAT Register

14.7.2.3.2.18.1 MCSPI_CH1STAT Register (Offset = 144h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 1

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Table 14-10785. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0144h
MCSPI1	2011 0144h
MCSPI2	2012 0144h
MCSPI3	2013 0144h
MCSPI4	2014 0144h

Figure 14-5331. MCSPI_CH1STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10786. MCSPI_CH1STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0

6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status
				`0 FIFO receive buffer is not full`
				`1 FIFO receive buffer is full`

5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status
				`0 FIFO receive buffer is not empty`
				`1 FIFO receive buffer is empty`

4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status
				`0 FIFO transmit buffer is not full`
				`1 FIFO transmit buffer is full`

3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status
				`0 FIFO transmit buffer is not empty`
				`1 FIFO transmit buffer is empty`

Table 14-10786. MCSPI_CH1STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus target and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.7.2.3.2.19 MCSPI_CH1CTRL Register

14.7.2.3.2.19.1 MCSPI_CH1CTRL Register (Offset = 148h) [reset = 0h]

This register is dedicated to enable the channel 1

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Table 14-10787. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0148h
MCSPI1	2011 0148h
MCSPI2	2012 0148h
MCSPI3	2013 0148h
MCSPI4	2014 0148h

Figure 14-5332. MCSPI_CH1CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXTCLK							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							EN
R							R/W
0h							0h

Table 14-10788. MCSPI_CH1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.7.2.3.2.20 MCSPI_TX1 Register

14.7.2.3.2.20.1 MCSPI_TX1 Register (Offset = 14Ch) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-10789. Instance Table

Instance Name	Physical Address
MCSPI0	2010 014Ch
MCSPI1	2011 014Ch
MCSPI2	2012 014Ch
MCSPI3	2013 014Ch
MCSPI4	2014 014Ch

Figure 14-5333. MCSPI_TX1 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 14-10790. MCSPI_TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 1 Data to transmit

14.7.2.3.2.21 MCSPI_RX1 Register

14.7.2.3.2.21.1 MCSPI_RX1 Register (Offset = 150h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-10791. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0150h
MCSPI1	2011 0150h
MCSPI2	2012 0150h
MCSPI3	2013 0150h
MCSPI4	2014 0150h

Figure 14-5334. MCSPI_RX1 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-10792. MCSPI_RX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 1 Received Data

14.7.2.3.2.22 MCSPI_CH2CONF Register

14.7.2.3.2.22.1 MCSPI_CH2CONF Register (Offset = 154h) [reset = 60000h]

This register is dedicated to the configuration of the channel 2

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Table 14-10793. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0154h
MCSPI1	2011 0154h
MCSPI2	2012 0154h
MCSPI3	2013 0154h
MCSPI4	2014 0154h

Figure 14-5335. MCSPI_CH2CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS2		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-10794. MCSPI_CH2CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0

29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
				`0` `Clock granularity of power of 2`
				`1` `One clock cycle granularity`

28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
				`0` `The buffer is not used to receive data.`
				`1` `The buffer is used to receive data.`

27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
				`0` `The buffer is not used to transmit data.`
				`1` `The buffer is used to transmit data.`

Table 14-10794. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:25	TCS2	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 `0.5 clock cycle` 1 `1.5 clock cycles` 2 `2.5 clock cycles` 3 `3.5 clock cycles`
24	SBPOL	R/W	0h	Start bit polarity 0 `SPICLK is held low during the INACTIVE state` 1 `SPICLK is held high during the INACTIVE state`
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 `Default MCSPI transfer length as specified by WL bit field` 1 `Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL`
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 `Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.` 1 `Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.`
19	TURBO	R/W	0h	Turbo mode 0 `Turbo is deactivated (recommended for single MCSPI word transfer).` 1 `Turbo is activated to maximize the throughput for multiple MCSPI words transfer.`
18	IS	R/W	1h	Input Select 0 `Data line 0 (SPIDAT[0]) selected for reception` 1 `Data line 1 (SPIDAT[1]) selected for reception`
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 `Data line 1 (SPIDAT[1]) selected for transmission` 1 `No transmission on Data Line1 (SPIDAT[1])`
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 `Data Line0 (SPIDAT[0]) selected for transmission` 1 `No transmission on data line 0 (SPIDAT[0])`
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 `DMA read request disabled` 1 `DMA read request enabled`
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 `DMA write request disabled` 1 `DMA write request enabled`

Table 14-10794. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

Table 14-10794. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 1 2 2 4 3 8 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.7.2.3.2.23 MCSPI_CH2STAT Register

14.7.2.3.2.23.1 MCSPI_CH2STAT Register (Offset = 158h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 2

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Table 14-10795. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0158h
MCSPI1	2011 0158h
MCSPI2	2012 0158h
MCSPI3	2013 0158h
MCSPI4	2014 0158h

Figure 14-5336. MCSPI_CH2STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10796. MCSPI_CH2STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status 0 `FIFO receive buffer is not full` 1 `FIFO receive buffer is full`
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status 0 `FIFO receive buffer is not empty` 1 `FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status 0 `FIFO transmit buffer is not full` 1 `FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status 0 `FIFO transmit buffer is not empty` 1 `FIFO transmit buffer is empty`

Table 14-10796. MCSPI_CH2STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus target and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 `This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).` 1 `This flag is automatically set to one at the end of an MCSPI transfer.`
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 `Register is full.` 1 `Register is empty.`
0	RXS	R	0h	Channel "i" Receiver Register Status 0 `Register is empty.` 1 `Register is full.`

14.7.2.3.2.24 MCSPI_CH2CTRL Register

14.7.2.3.2.24.1 MCSPI_CH2CTRL Register (Offset = 15Ch) [reset = 0h]

This register is dedicated to enable the channel 2

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Table 14-10797. Instance Table

Instance Name	Physical Address
MCSPI0	2010 015Ch
MCSPI1	2011 015Ch
MCSPI2	2012 015Ch
MCSPI3	2013 015Ch
MCSPI4	2014 015Ch

Figure 14-5337. MCSPI_CH2CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EXTCLK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED_1</td><td>EN</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-10798. MCSPI_CH2CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.7.2.3.2.25 MCSPI_TX2 Register

14.7.2.3.2.25.1 MCSPI_TX2 Register (Offset = 160h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-10799. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0160h
MCSPI1	2011 0160h
MCSPI2	2012 0160h
MCSPI3	2013 0160h
MCSPI4	2014 0160h

Figure 14-5338. MCSPI_TX2 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 14-10800. MCSPI_TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 2 Data to transmit

14.7.2.3.2.26 MCSPI_RX2 Register

14.7.2.3.2.26.1 MCSPI_RX2 Register (Offset = 164h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-10801. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0164h
MCSPI1	2011 0164h
MCSPI2	2012 0164h
MCSPI3	2013 0164h
MCSPI4	2014 0164h

Figure 14-5339. MCSPI_RX2 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-10802. MCSPI_RX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 2 Received Data

14.7.2.3.2.27 MCSPI_CH3CONF Register

14.7.2.3.2.27.1 MCSPI_CH3CONF Register (Offset = 168h) [reset = 60000h]

This register is dedicated to the configuration of the channel 3

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Table 14-10803. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0168h
MCSPI1	2011 0168h
MCSPI2	2012 0168h
MCSPI3	2013 0168h
MCSPI4	2014 0168h

Figure 14-5340. MCSPI_CH3CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS3		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 14-10804. MCSPI_CH3CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	read returns 0

29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
				`0 Clock granularity of power of 2`
				`1 One clock cycle granularity`

28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
				`0 The buffer is not used to receive data.`
				`1 The buffer is used to receive data.`

27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
				`0 The buffer is not used to transmit data.`
				`1 The buffer is used to transmit data.`

Table 14-10804. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:25	TCS3	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled

Table 14-10804. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

Table 14-10804. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 1 2 2 4 3 8 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

14.7.2.3.2.28 MCSPI_CH3STAT Register

14.7.2.3.2.28.1 MCSPI_CH3STAT Register (Offset = 16Ch) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 3

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Table 14-10805. Instance Table

Instance Name	Physical Address
MCSPI0	2010 016Ch
MCSPI1	2011 016Ch
MCSPI2	2012 016Ch
MCSPI3	2013 016Ch
MCSPI4	2014 016Ch

Figure 14-5341. MCSPI_CH3STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10806. MCSPI_CH3STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0

6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status
				`0 FIFO receive buffer is not full`
				`1 FIFO receive buffer is full`

5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status
				`0 FIFO receive buffer is not empty`
				`1 FIFO receive buffer is empty`

4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status
				`0 FIFO transmit buffer is not full`
				`1 FIFO transmit buffer is full`

3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status
				`0 FIFO transmit buffer is not empty`
				`1 FIFO transmit buffer is empty`

Table 14-10806. MCSPI_CH3STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus target and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1 This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel "i" Transmitter Register Status 0 Register is full. 1 Register is empty.
0	RXS	R	0h	Channel "i" Receiver Register Status 0 Register is empty. 1 Register is full.

14.7.2.3.2.29 MCSPI_CH3CTRL Register

14.7.2.3.2.29.1 MCSPI_CH3CTRL Register (Offset = 170h) [reset = 0h]

This register is dedicated to enable the channel 3

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Table 14-10807. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0170h
MCSPI1	2011 0170h
MCSPI2	2012 0170h
MCSPI3	2013 0170h
MCSPI4	2014 0170h

Figure 14-5342. MCSPI_CH3CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EXTCLK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED_1</td><td>EN</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-10808. MCSPI_CH3CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

14.7.2.3.2.30 MCSPI_TX3 Register

14.7.2.3.2.30.1 MCSPI_TX3 Register (Offset = 174h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 14-10809. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0174h
MCSPI1	2011 0174h
MCSPI2	2012 0174h
MCSPI3	2013 0174h
MCSPI4	2014 0174h

Figure 14-5343. MCSPI_TX3 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 14-10810. MCSPI_TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 3 Data to transmit

14.7.2.3.2.31 MCSPI_RX3 Register

14.7.2.3.2.31.1 MCSPI_RX3 Register (Offset = 178h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 14-10811. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0178h
MCSPI1	2011 0178h
MCSPI2	2012 0178h
MCSPI3	2013 0178h
MCSPI4	2014 0178h

Figure 14-5344. MCSPI_RX3 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 14-10812. MCSPI_RX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 3 Received Data

14.7.2.3.2.32 MCSPI_XFERLEVEL Register

14.7.2.3.2.32.1 MCSPI_XFERLEVEL Register (Offset = 17Ch) [reset = 0h]

This register provides transfer levels needed while using FIFO buffer during transfer.

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Table 14-10813. Instance Table

Instance Name	Physical Address
MCSPI0	2010 017Ch
MCSPI1	2011 017Ch
MCSPI2	2012 017Ch
MCSPI3	2013 017Ch
MCSPI4	2014 017Ch

Figure 14-5345. MCSPI_XFERLEVEL Name Register

31	30	29	28	27	26	25	24
WCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
WCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
AFL							
R/W							
0h							
7	6	5	4	3	2	1	0
AEL							
R/W							
0h							

Table 14-10814. MCSPI_XFERLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WCNT	R/W	0h	Spi word counterThis register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO bufferWhen transfer had started, a read back in this register returns the current SPI word transfer index 0 Counter not used 1 One word FFFE 65534 MCSPI word FFFF 65535 MCSPI word
15:8	AFL	R/W	0h	Buffer Almost Full This register holds the programmable almost full level value used to determine almost full buffer condition If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n-1The size of this register is defined by the generic parameter FFNBYTE 0 1 byte 1 2 bytes FE 255bytes FF 256bytes

Table 14-10814. MCSPI_XFERLEVEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	AEL	R/W	0h	Buffer Almost EmptyThis register holds the programmable almost empty level value used to determine almost empty buffer condition If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with n-1 0 1 byte 1 2 bytes FE 255 bytes FF 256bytes

14.7.2.3.2.33 MCSPI_DAFTX Register

14.7.2.3.2.33.1 MCSPI_DAFTX Register (Offset = 180h) [reset = 0h]

This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_TX(i) register corresponding to the channel which have its FIFO enabled.

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Table 14-10815. Instance Table

Instance Name	Physical Address
MCSPI0	2010 0180h
MCSPI1	2011 0180h
MCSPI2	2012 0180h
MCSPI3	2013 0180h
MCSPI4	2014 0180h

Figure 14-5346. MCSPI_DAFTX Name Register

31	30	29	28	27	26	25	24
DAFTDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DAFTDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DAFTDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DAFTDATA							
R/W							
0h							

Table 14-10816. MCSPI_DAFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFTDATA	R/W	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

14.7.2.3.2.34 MCSPI_DAFRX Register

14.7.2.3.2.34.1 MCSPI_DAFRX Register (Offset = 1A0h) [reset = 0h]

This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_RX(i) register corresponding to the channel which have its FIFO enabled.

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Table 14-10817. Instance Table

Instance Name	Physical Address
MCSPI0	2010 01A0h
MCSPI1	2011 01A0h
MCSPI2	2012 01A0h
MCSPI3	2013 01A0h
MCSPI4	2014 01A0h

Figure 14-5347. MCSPI_DAFRX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DAFRDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10818. MCSPI_DAFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFRDATA	R	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

14.7.2.4 UART

UART

14.7.2.4.1 UART Summaries

UART Summaries

Table 14-10819. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	32	UART_DLL	0280 0000h	0281 0000h	0282 0000h
0h	32	UART_RHR	0280 0000h	0281 0000h	0282 0000h
0h	32	UART_THR	0280 0000h	0281 0000h	0282 0000h
4h	32	UART_DLH	0280 0004h	0281 0004h	0282 0004h
4h	32	UART_IER_CIR	0280 0004h	0281 0004h	0282 0004h
4h	32	UART_IER_IRDA	0280 0004h	0281 0004h	0282 0004h
4h	32	UART_IER_UART	0280 0004h	0281 0004h	0282 0004h
8h	32	UART_EFR	0280 0008h	0281 0008h	0282 0008h
8h	32	UART_FCR	0280 0008h	0281 0008h	0282 0008h
8h	32	UART_IIR_CIR	0280 0008h	0281 0008h	0282 0008h
8h	32	UART_IIR_IRDA	0280 0008h	0281 0008h	0282 0008h
8h	32	UART_IIR_UART	0280 0008h	0281 0008h	0282 0008h
Ch	32	UART_LCR	0280 000Ch	0281 000Ch	0282 000Ch
10h	32	UART_MCR	0280 0010h	0281 0010h	0282 0010h
10h	32	UART_XON1_ADDR1	0280 0010h	0281 0010h	0282 0010h
14h	32	UART_LSR_CIR	0280 0014h	0281 0014h	0282 0014h
14h	32	UART_LSR_IRDA	0280 0014h	0281 0014h	0282 0014h
14h	32	UART_LSR_UART	0280 0014h	0281 0014h	0282 0014h
14h	32	UART_XON2_ADDR2	0280 0014h	0281 0014h	0282 0014h
18h	32	UART_MSR	0280 0018h	0281 0018h	0282 0018h
18h	32	UART_TCR	0280 0018h	0281 0018h	0282 0018h
18h	32	UART_XOFF1	0280 0018h	0281 0018h	0282 0018h
1Ch	32	UART_SPR	0280 001Ch	0281 001Ch	0282 001Ch
1Ch	32	UART_TLR	0280 001Ch	0281 001Ch	0282 001Ch
1Ch	32	UART_XOFF2	0280 001Ch	0281 001Ch	0282 001Ch
20h	32	UART_MDR1	0280 0020h	0281 0020h	0282 0020h
24h	32	UART_MDR2	0280 0024h	0281 0024h	0282 0024h
28h	32	UART_SFLSR	0280 0028h	0281 0028h	0282 0028h
28h	32	UART_TXFLL	0280 0028h	0281 0028h	0282 0028h
2Ch	32	UART_RESUME	0280 002Ch	0281 002Ch	0282 002Ch
2Ch	32	UART_TXFLH	0280 002Ch	0281 002Ch	0282 002Ch
30h	32	UART_RXFLL	0280 0030h	0281 0030h	0282 0030h
30h	32	UART_SFREGL	0280 0030h	0281 0030h	0282 0030h
34h	32	UART_RXFLH	0280 0034h	0281 0034h	0282 0034h
34h	32	UART_SFREGH	0280 0034h	0281 0034h	0282 0034h
38h	32	UART_BLR	0280 0038h	0281 0038h	0282 0038h
38h	32	UART_UASR	0280 0038h	0281 0038h	0282 0038h
3Ch	32	UART_ACREG	0280 003Ch	0281 003Ch	0282 003Ch
40h	32	UART_SCR	0280 0040h	0281 0040h	0282 0040h

Table 14-10819. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
44h	32	UART_SSR	0280 0044h	0281 0044h	0282 0044h
48h	32	UART_EBLR	0280 0048h	0281 0048h	0282 0048h
50h	32	UART_MVR	0280 0050h	0281 0050h	0282 0050h
54h	32	UART_SYSC	0280 0054h	0281 0054h	0282 0054h
58h	32	UART_SYSS	0280 0058h	0281 0058h	0282 0058h
5Ch	32	UART_WER	0280 005Ch	0281 005Ch	0282 005Ch
60h	32	UART_CFPS	0280 0060h	0281 0060h	0282 0060h
64h	32	UART_RXFIFO_LVL	0280 0064h	0281 0064h	0282 0064h
68h	32	UART_TXFIFO_LVL	0280 0068h	0281 0068h	0282 0068h
6Ch	32	UART_IER2	0280 006Ch	0281 006Ch	0282 006Ch
70h	32	UART_ISR2	0280 0070h	0281 0070h	0282 0070h
74h	32	UART_FREQ_SEL	0280 0074h	0281 0074h	0282 0074h
78h	32	UART_ABAUD_1ST_CHAR	0280 0078h	0281 0078h	0282 0078h
7Ch	32	UART_BAUD_2ND_CHAR	0280 007Ch	0281 007Ch	0282 007Ch
80h	32	UART_MDR3	0280 0080h	0281 0080h	0282 0080h
84h	32	UART_TX_DMA_THRESHOLD	0280 0084h	0281 0084h	0282 0084h
88h	32	UART_MDR4	0280 0088h	0281 0088h	0282 0088h
8Ch	32	UART_EFR2	0280 008Ch	0281 008Ch	0282 008Ch
90h	32	UART_ECR	0280 0090h	0281 0090h	0282 0090h
94h	32	UART_TIMEGUARD	0280 0094h	0281 0094h	0282 0094h
98h	32	UART_TIMEOUTL	0280 0098h	0281 0098h	0282 0098h
9Ch	32	UART_TIMEOUTH	0280 009Ch	0281 009Ch	0282 009Ch
A0h	32	UART_SCCR	0280 00A0h	0281 00A0h	0282 00A0h
A4h	32	UART_ERHR	0280 00A4h	0281 00A4h	0282 00A4h
A4h	32	UART_ETHR	0280 00A4h	0281 00A4h	0282 00A4h
A8h	32	UART_MAR	0280 00A8h	0281 00A8h	0282 00A8h
ACh	32	UART_MMR	0280 00ACh	0281 00ACh	0282 00ACh
B0h	32	UART_MBR	0280 00B0h	0281 00B0h	0282 00B0h

Table 14-10820. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART_DLL	0283 0000h	0284 0000h	0285 0000h
0h	32	UART_RHR	0283 0000h	0284 0000h	0285 0000h
0h	32	UART_THR	0283 0000h	0284 0000h	0285 0000h
4h	32	UART_DLH	0283 0004h	0284 0004h	0285 0004h
4h	32	UART_IER_CIR	0283 0004h	0284 0004h	0285 0004h
4h	32	UART_IER_IRDA	0283 0004h	0284 0004h	0285 0004h
4h	32	UART_IER_UART	0283 0004h	0284 0004h	0285 0004h
8h	32	UART_EFR	0283 0008h	0284 0008h	0285 0008h
8h	32	UART_FCR	0283 0008h	0284 0008h	0285 0008h
8h	32	UART_IIR_CIR	0283 0008h	0284 0008h	0285 0008h
8h	32	UART_IIR_IRDA	0283 0008h	0284 0008h	0285 0008h
8h	32	UART_IIR_UART	0283 0008h	0284 0008h	0285 0008h
Ch	32	UART_LCR	0283 000Ch	0284 000Ch	0285 000Ch
10h	32	UART_MCR	0283 0010h	0284 0010h	0285 0010h

Table 14-10820. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
10h	32	UART_XON1_ADDR1	0283 0010h	0284 0010h	0285 0010h
14h	32	UART_LSR_CIR	0283 0014h	0284 0014h	0285 0014h
14h	32	UART_LSR_IRDA	0283 0014h	0284 0014h	0285 0014h
14h	32	UART_LSR_UART	0283 0014h	0284 0014h	0285 0014h
14h	32	UART_XON2_ADDR2	0283 0014h	0284 0014h	0285 0014h
18h	32	UART_MSR	0283 0018h	0284 0018h	0285 0018h
18h	32	UART_TCR	0283 0018h	0284 0018h	0285 0018h
18h	32	UART_XOFF1	0283 0018h	0284 0018h	0285 0018h
1Ch	32	UART_SPR	0283 001Ch	0284 001Ch	0285 001Ch
1Ch	32	UART_TLR	0283 001Ch	0284 001Ch	0285 001Ch
1Ch	32	UART_XOFF2	0283 001Ch	0284 001Ch	0285 001Ch
20h	32	UART_MDR1	0283 0020h	0284 0020h	0285 0020h
24h	32	UART_MDR2	0283 0024h	0284 0024h	0285 0024h
28h	32	UART_SFLSR	0283 0028h	0284 0028h	0285 0028h
28h	32	UART_TXFLL	0283 0028h	0284 0028h	0285 0028h
2Ch	32	UART_RESUME	0283 002Ch	0284 002Ch	0285 002Ch
2Ch	32	UART_TXFLH	0283 002Ch	0284 002Ch	0285 002Ch
30h	32	UART_RXFLL	0283 0030h	0284 0030h	0285 0030h
30h	32	UART_SFREGL	0283 0030h	0284 0030h	0285 0030h
34h	32	UART_RXFLH	0283 0034h	0284 0034h	0285 0034h
34h	32	UART_SFREGH	0283 0034h	0284 0034h	0285 0034h
38h	32	UART_BLR	0283 0038h	0284 0038h	0285 0038h
38h	32	UART_UASR	0283 0038h	0284 0038h	0285 0038h
3Ch	32	UART_ACREG	0283 003Ch	0284 003Ch	0285 003Ch
40h	32	UART_SCR	0283 0040h	0284 0040h	0285 0040h
44h	32	UART_SSR	0283 0044h	0284 0044h	0285 0044h
48h	32	UART_EBLR	0283 0048h	0284 0048h	0285 0048h
50h	32	UART_MVR	0283 0050h	0284 0050h	0285 0050h
54h	32	UART_SYSC	0283 0054h	0284 0054h	0285 0054h
58h	32	UART_SYSS	0283 0058h	0284 0058h	0285 0058h
5Ch	32	UART_WER	0283 005Ch	0284 005Ch	0285 005Ch
60h	32	UART_CFPS	0283 0060h	0284 0060h	0285 0060h
64h	32	UART_RXFIFO_LVL	0283 0064h	0284 0064h	0285 0064h
68h	32	UART_TXFIFO_LVL	0283 0068h	0284 0068h	0285 0068h
6Ch	32	UART_IER2	0283 006Ch	0284 006Ch	0285 006Ch
70h	32	UART_ISR2	0283 0070h	0284 0070h	0285 0070h
74h	32	UART_FREQ_SEL	0283 0074h	0284 0074h	0285 0074h
78h	32	UART_ABAUD_1ST_CHAR	0283 0078h	0284 0078h	0285 0078h
7Ch	32	UART_BAUD_2ND_CHAR	0283 007Ch	0284 007Ch	0285 007Ch
80h	32	UART_MDR3	0283 0080h	0284 0080h	0285 0080h
84h	32	UART_TX_DMA_THRESHOLD	0283 0084h	0284 0084h	0285 0084h
88h	32	UART_MDR4	0283 0088h	0284 0088h	0285 0088h
8Ch	32	UART_EFR2	0283 008Ch	0284 008Ch	0285 008Ch
90h	32	UART_ECR	0283 0090h	0284 0090h	0285 0090h
94h	32	UART_TIMEGUARD	0283 0094h	0284 0094h	0285 0094h
98h	32	UART_TIMEOUTL	0283 0098h	0284 0098h	0285 0098h

Table 14-10820. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
9Ch	32	UART_TIMEOUTH	0283 009Ch	0284 009Ch	0285 009Ch
A0h	32	UART_SCCR	0283 00A0h	0284 00A0h	0285 00A0h
A4h	32	UART_ERHR	0283 00A4h	0284 00A4h	0285 00A4h
A4h	32	UART_ETHR	0283 00A4h	0284 00A4h	0285 00A4h
A8h	32	UART_MAR	0283 00A8h	0284 00A8h	0285 00A8h
ACh	32	UART_MMR	0283 00ACh	0284 00ACh	0285 00ACh
B0h	32	UART_MBR	0283 00B0h	0284 00B0h	0285 00B0h

Table 14-10821. UART Registers, Base Address=0280 0000h, Length=512

Offset	Length	Register Name	UART6 Physical Address	WKUP_UART0 Physical Address
0h	32	UART_DLL	0286 0000h	2B30 0000h
0h	32	UART_RHR	0286 0000h	2B30 0000h
0h	32	UART_THR	0286 0000h	2B30 0000h
4h	32	UART_DLH	0286 0004h	2B30 0004h
4h	32	UART_IER_CIR	0286 0004h	2B30 0004h
4h	32	UART_IER_IRDA	0286 0004h	2B30 0004h
4h	32	UART_IER_UART	0286 0004h	2B30 0004h
8h	32	UART_EFR	0286 0008h	2B30 0008h
8h	32	UART_FCR	0286 0008h	2B30 0008h
8h	32	UART_IIR_CIR	0286 0008h	2B30 0008h
8h	32	UART_IIR_IRDA	0286 0008h	2B30 0008h
8h	32	UART_IIR_UART	0286 0008h	2B30 0008h
Ch	32	UART_LCR	0286 000Ch	2B30 000Ch
10h	32	UART_MCR	0286 0010h	2B30 0010h
10h	32	UART_XON1_ADDR1	0286 0010h	2B30 0010h
14h	32	UART_LSR_CIR	0286 0014h	2B30 0014h
14h	32	UART_LSR_IRDA	0286 0014h	2B30 0014h
14h	32	UART_LSR_UART	0286 0014h	2B30 0014h
14h	32	UART_XON2_ADDR2	0286 0014h	2B30 0014h
18h	32	UART_MSR	0286 0018h	2B30 0018h
18h	32	UART_TCR	0286 0018h	2B30 0018h
18h	32	UART_XOFF1	0286 0018h	2B30 0018h
1Ch	32	UART_SPR	0286 001Ch	2B30 001Ch
1Ch	32	UART_TLR	0286 001Ch	2B30 001Ch
1Ch	32	UART_XOFF2	0286 001Ch	2B30 001Ch
20h	32	UART_MDR1	0286 0020h	2B30 0020h
24h	32	UART_MDR2	0286 0024h	2B30 0024h
28h	32	UART_SFLSR	0286 0028h	2B30 0028h
28h	32	UART_TXFLL	0286 0028h	2B30 0028h
2Ch	32	UART_RESUME	0286 002Ch	2B30 002Ch
2Ch	32	UART_TXFLH	0286 002Ch	2B30 002Ch
30h	32	UART_RXFLL	0286 0030h	2B30 0030h
30h	32	UART_SFREGL	0286 0030h	2B30 0030h
34h	32	UART_RXFLH	0286 0034h	2B30 0034h
34h	32	UART_SFREGH	0286 0034h	2B30 0034h

Table 14-10821. UART Registers, Base Address=0280 0000h, Length=512 (continued)

Offset	Length	Register Name	UART6 Physical Address	WKUP_UART0 Physical Address
38h	32	UART_BLR	0286 0038h	2B30 0038h
38h	32	UART_UASR	0286 0038h	2B30 0038h
3Ch	32	UART_ACREG	0286 003Ch	2B30 003Ch
40h	32	UART_SCR	0286 0040h	2B30 0040h
44h	32	UART_SSR	0286 0044h	2B30 0044h
48h	32	UART_EBLR	0286 0048h	2B30 0048h
50h	32	UART_MVR	0286 0050h	2B30 0050h
54h	32	UART_SYSC	0286 0054h	2B30 0054h
58h	32	UART_SYSS	0286 0058h	2B30 0058h
5Ch	32	UART_WER	0286 005Ch	2B30 005Ch
60h	32	UART_CFPS	0286 0060h	2B30 0060h
64h	32	UART_RXFIFO_LVL	0286 0064h	2B30 0064h
68h	32	UART_TXFIFO_LVL	0286 0068h	2B30 0068h
6Ch	32	UART_IER2	0286 006Ch	2B30 006Ch
70h	32	UART_ISR2	0286 0070h	2B30 0070h
74h	32	UART_FREQ_SEL	0286 0074h	2B30 0074h
78h	32	UART_ABAUD_1ST_CHAR	0286 0078h	2B30 0078h
7Ch	32	UART_BAUD_2ND_CHAR	0286 007Ch	2B30 007Ch
80h	32	UART_MDR3	0286 0080h	2B30 0080h
84h	32	UART_TX_DMA_THRESHOLD	0286 0084h	2B30 0084h
88h	32	UART_MDR4	0286 0088h	2B30 0088h
8Ch	32	UART_EFR2	0286 008Ch	2B30 008Ch
90h	32	UART_ECR	0286 0090h	2B30 0090h
94h	32	UART_TIMEGUARD	0286 0094h	2B30 0094h
98h	32	UART_TIMEOUTL	0286 0098h	2B30 0098h
9Ch	32	UART_TIMEOUTH	0286 009Ch	2B30 009Ch
A0h	32	UART_SCCR	0286 00A0h	2B30 00A0h
A4h	32	UART_ERHR	0286 00A4h	2B30 00A4h
A4h	32	UART_ETHR	0286 00A4h	2B30 00A4h
A8h	32	UART_MAR	0286 00A8h	2B30 00A8h
ACh	32	UART_MMR	0286 00ACh	2B30 00ACh
B0h	32	UART_MBR	0286 00B0h	2B30 00B0h

14.7.2.4.2 UART Registers

UART Registers

14.7.2.4.2.1 UART_DLL Register

14.7.2.4.2.1.1 UART_DLL Register (Offset = 0h) [reset = 0h]

Divisor Latches Low Register

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Table 14-10822. Instance Table

Instance Name	Physical Address
UART0	0280 0000h
UART1	0281 0000h
UART2	0282 0000h
UART3	0283 0000h
UART4	0284 0000h
UART5	0285 0000h
UART6	0286 0000h
WKUP_UART0	2B30 0000h

Figure 14-5348. UART_DLL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLOCK_LSB							
R/W							
0h							

Table 14-10823. UART_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CLOCK_LSB	R/W	0h	Used to store the 8-bit LSB divisor value Reset Source: mod_g_arstn

14.7.2.4.2.2 UART_RHR Register

14.7.2.4.2.2.1 UART_RHR Register (Offset = 0h) [reset = 0h]

The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.

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Table 14-10824. Instance Table

Instance Name	Physical Address
UART0	0280 0000h
UART1	0281 0000h
UART2	0282 0000h
UART3	0283 0000h
UART4	0284 0000h
UART5	0285 0000h
UART6	0286 0000h
WKUP_UART0	2B30 0000h

Figure 14-5349. UART_RHR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RHR							
R							
0h							

Table 14-10825. UART_RHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RHR	R	0h	Receive holding register Reset Source: mod_g_arstn

14.7.2.4.2.3 UART_THR Register

14.7.2.4.2.3.1 UART_THR Register (Offset = 0h) [reset = 0h]

The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.

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Table 14-10826. Instance Table

Instance Name	Physical Address
UART0	0280 0000h
UART1	0281 0000h
UART2	0282 0000h
UART3	0283 0000h
UART4	0284 0000h
UART5	0285 0000h
UART6	0286 0000h
WKUP_UART0	2B30 0000h

Figure 14-5350. UART_THR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">THR</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10827. UART_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	THR	W	0h	TRANSMIT HOLDING REGISTER Reset Source: mod_g_arstn

14.7.2.4.2.4 UART_DLH Register

14.7.2.4.2.4.1 UART_DLH Register (Offset = 4h) [reset = 0h]

Divisor Latches High Register

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Table 14-10828. Instance Table

Instance Name	Physical Address
UART0	0280 0004h
UART1	0281 0004h
UART2	0282 0004h
UART3	0283 0004h
UART4	0284 0004h
UART5	0285 0004h
UART6	0286 0004h
WKUP_UART0	2B30 0004h

Figure 14-5351. UART_DLH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLOCK_MSB							
R/W							
0h							

Table 14-10829. UART_DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CLOCK_MSB	R/W	0h	Used to store the 8-bit MSB divisor value Reset Source: mod_g_arstn

14.7.2.4.2.5 UART_IER_CIR Register

14.7.2.4.2.5.1 UART_IER_CIR Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 14-10830. Instance Table

Instance Name	Physical Address
UART0	0280 0004h
UART1	0281 0004h
UART2	0282 0004h
UART3	0283 0004h
UART4	0284 0004h
UART5	0285 0004h
UART6	0286 0004h
WKUP_UART0	2B30 0004h

Figure 14-5352. UART_IER_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NOT_USED2		TX_STATUS_IT	NOT_USED1	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-10831. UART_IER_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	NOT_USED2	R/W	0h	Reset Source: mod_g_arstn
5	TX_STATUS_IT	R/W	0h	0 Disables the TX status interrupt. 1 Enables the TX status interrupt.
4	NOT_USED1	R/W	0h	Reset Source: mod_g_arstn
3	RX_OVERRUN_IT	R/W	0h	0 Disables the RX overrun interrupt. 1 Enables the RX overrun interrupt.
2	RX_STOP_IT	R/W	0h	0 Disables the receive stop interrupt. 1 Enables the receive stop interrupt.

Table 14-10831. UART_IER_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	THR_IT	R/W	0h	0 Disables the THR interrupt. 1 Enables the THR interrupt.
0	RHR_IT	R/W	0h	0 Disables the RHR interrupt. 1 Enables the RHR interrupt.

14.7.2.4.2.6 UART_IER_IRDA Register

14.7.2.4.2.6.1 UART_IER_IRDA Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 14-10832. Instance Table

Instance Name	Physical Address
UART0	0280 0004h
UART1	0281 0004h
UART2	0282 0004h
UART3	0283 0004h
UART4	0284 0004h
UART5	0285 0004h
UART6	0286 0004h
WKUP_UART0	2B30 0004h

Figure 14-5353. UART_IER_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10833. UART_IER_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EOF_IT	R/W	0h	0 `Disables the received EOF interrupt.` 1 `Enables the received EOF interrupt.`
6	LINE_STS_IT	R/W	0h	0 `Disables the receiver line status interrupt.` 1 `Enables the receiver line status interrupt.`
5	TX_STATUS_IT	R/W	0h	0 `Disables the TX status interrupt.` 1 `Enables the TX status interrupt.`

Table 14-10833. UART_IER_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	STS_FIFO_TRIG_IT	R/W	0h	0 Disables the status FIFO trigger level interrupt. 1 Enables the status FIFO trigger level interrupt.
3	RX_OVERRUN_IT	R/W	0h	0 Disables the RX overrun interrupt. 1 Enables the RX overrun interrupt.
2	LAST_RX_BYTE_IT	R/W	0h	0 Disables the last byte of frame in RX FIFO interrupt. 1 Enables the last byte of frame in RX FIFO interrupt.
1	THR_IT	R/W	0h	0 Disables the THR interrupt. 1 Enables the THR interrupt.
0	RHR_IT	R/W	0h	0 Disables the RHR interrupt. 1 Enables the RHR interrupt.

14.7.2.4.2.7 UART_IER_UART Register

14.7.2.4.2.7.1 UART_IER_UART Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.

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Table 14-10834. Instance Table

Instance Name	Physical Address
UART0	0280 0004h
UART1	0281 0004h
UART2	0282 0004h
UART3	0283 0004h
UART4	0284 0004h
UART5	0285 0004h
UART6	0286 0004h
WKUP_UART0	2B30 0004h

Figure 14-5354. UART_IER_UART Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10835. UART_IER_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7	CTS_IT	R/W	0h	0 Disables the CTS* interrupt 1 Enables the CTS* interrupt
6	RTS_IT	R/W	0h	0 Disables the RTS* interrupt 1 Enables the RTS* interrupt
5	XOFF_IT	R/W	0h	0 Disables the XOFF interrupt 1 Enables the XOFF interrupt

Table 14-10835. UART_IER_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SLEEP_MODE	R/W	0h	0 Disables sleep mode 1 Enables sleep mode (stop baud rate clock when the module is inactive)
3	MODEM_STS_IT	R/W	0h	0 Disables the modem status register interrupt 1 Enables the modem status register interrupt
2	LINE_STS_IT	R/W	0h	0 Disables the receiver line status interrupt 1 Enables the receiver line status interrupt
1	THR_IT	R/W	0h	0 Disables the THR interrupt 1 Enables the THR interrupt
0	RHR_IT	R/W	0h	0 Disables the RHR interrupt and time out interrupt. 1 Enables the RHR interrupt and time out interrupt.

14.7.2.4.2.8 UART_EFR Register

14.7.2.4.2.8.1 UART_EFR Register (Offset = 8h) [reset = 0h]

Enhanced Feature Register

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Table 14-10836. Instance Table

Instance Name	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
WKUP_UART0	2B30 0008h

Figure 14-5355. UART_EFR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 14-10837. UART_EFR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	AUTO_CTS_EN	R/W	0h	Auto-CTS enable bit. 0: Normal operation. 1: Auto-CTS flow control is enabled i.e. transmission is halted when the CTS* pin is high (inactive). Reset Source: mod_g_arstn
6	AUTO_RTS_EN	R/W	0h	Auto-RTS enable bit. 0: Normal operation. 1: Auto- RTS flow control is enabled i.e. RTS* pin goes high (inactive) when the receiver FIFO HALT trigger level, TCR[3:0], is reached, and goes low (active) when the receiver FIFO RESTORE transmission trigger level is reached. Reset Source: mod_g_arstn

Table 14-10837. UART_EFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SPECIAL_CHAR_DETECT	R/W	0h	0: Normal operation. 1: Special character detect enable. Received data is compared with XOFF2 data. If a match occurs the received data is transferred to RX FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected. Reset Source: mod_g_arstn
4	ENHANCED_EN	R/W	0h	Enhanced functions write enable bit. 0: Disables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. 1: Enables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. Reset Source: mod_g_arstn
3:0	SW_FLOW_CONTROL	R/W	0h	Combinations of Software flow control can be selected by programming bit 3 - bit 0. See Software Flow Control Options Reset Source: mod_g_arstn

14.7.2.4.2.9 UART_FCR Register

14.7.2.4.2.9.1 UART_FCR Register (Offset = 8h) [reset = 0h]

FIFO Control Register
Notes:
Bits 4 and 5 can only be written to when EFR[4] = 1
Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0)
Always make sure that the FIFO is empty when disabling or enabling the FIFO, or reset it if this can't be guaranteed.
See the Transmit FIFO Trigger section of the device TRM for FCR[5:4] setting restriction when SCR[6]=1
See the Recieve FIFO Trigger section of the device TRM for FCR[7:6] setting restriction when SCR[7]=1

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Table 14-10838. Instance Table

Instance Name	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
WKUP_UART0	2B30 0008h

Figure 14-5356. UART_FCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN
W		W		W	W	W	W
0h		0h		0h	0h	0h	0h

Table 14-10839. UART_FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:6	RX_FIFO_TRIG	W	0h	Sets the trigger level for the RX FIFO: If SCR[7] = 0 and TLR[7:4] = 0000: 00: 8 characters 01: 16 characters 10: 56 characters 11: 60 characters If SCR[7] = 0 and TLR[7:4] != 0000, RX_FIFO_TRIG is not considered. If SCR[7]=1, RX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1. Reset Source: mod_g_arstn

Table 14-10839. UART_FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	TX_FIFO_TRIG	W	0h	Sets the trigger level for the TX FIFO: If SCR[6] = 0 and TLR[3:0] = 0000: 00: 8 spaces 01: 16 spaces 10: 32 spaces 11: 56 spaces If SCR[6] = 0 and TLR[3:0] != 0000, TX_FIFO_TRIG is not considered. If SCR[6]=1, TX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1 Reset Source: mod_g_arstn
3	DMA_MODE	W	0h	This register is considered if SCR[0] = 0. 0 DMA_MODE 0 (No DMA) 1 DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)
2	TX_FIFO_CLEAR	W	0h	0 No change 1 Clears the transmit FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.
1	RX_FIFO_CLEAR	W	0h	0 No change 1 Clears the receive FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.
0	FIFO_EN	W	0h	0 Disables the transmit and receive FIFOs. The transmit and receive holding registers are one byte FIFOs. 1 : Enables the transmit and receive FIFOs.The transmit and receive holding registers are 64-bytes FIFOs.

14.7.2.4.2.10 UART_IIR_CIR Register

14.7.2.4.2.10.1 UART_IIR_CIR Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 14-10840. Instance Table

Instance Name	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
WKUP_UART0	2B30 0008h

Figure 14-5357. UART_IIR_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE		R	NONE	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-10841. UART_IIR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	TX_STATUS_IT	R	0h	`0 TX status interrupt inactive` `1 TX status interrupt active`
4	RESERVED	NONE	0h	Reserved
3	RX_OE_IT	R	0h	`0 RX overrun interrupt inactive` `1 RX overrun interrupt active`
2	RX_STOP_IT	R	0h	`0 Receive stop interrupt inactive` `1 Receive stop interrupt active`
1	THR_IT	R	0h	`0 THR interrupt inactive` `1 THR interrupt active`
0	RHR_IT	R	0h	`0 RHR interrupt inactive` `1 RHR interrupt active`

14.7.2.4.2.11 UART_IIR_IRDA Register

14.7.2.4.2.11.1 UART_IIR_IRDA Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 14-10842. Instance Table

Instance Name	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
WKUP_UART0	2B30 0008h

Figure 14-5358. UART_IIR_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10843. UART_IIR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EOF_IT	R	0h	0 Received EOF interrupt inactive 1 Received EOF interrupt active
6	LINE_STS_IT	R	0h	0 Receiver line status interrupt inactive 1 Receiver line status interrupt active
5	TX_STATUS_IT	R	0h	0 TX status interrupt inactive 1 TX status interrupt active
4	STS_FIFO_IT	R	0h	0 Status FIFO trigger level interrupt inactive 1 Status FIFO trigger level interrupt active
3	RX_OE_IT	R	0h	0 RX overrun interrupt inactive 1 RX overrun interrupt active

Table 14-10843. UART_IIR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RX_FIFO_LAST_BYTE_IT	R	0h	0 `Last byte of frame in RX FIFO interrupt inactive` 1 `Last byte of frame in RX FIFO interrupt active`
1	THR_IT	R	0h	0 `THR interrupt inactive` 1 `THR interrupt active`
0	RHR_IT	R	0h	0 `RHR interrupt inactive` 1 `RHR interrupt active`

14.7.2.4.2.12 UART_IIR_UART Register

14.7.2.4.2.12.1 UART_IIR_UART Register (Offset = 8h) [reset = 1h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 14-10844. Instance Table

Instance Name	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
WKUP_UART0	2B30 0008h

Figure 14-5359. UART_IIR_UART Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
FCR_MIRROR		IT_TYPE					IT_PENDING
R		R					R
0h		0h					1h

Table 14-10845. UART_IIR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:6	FCR_MIRROR	R	0h	Mirror the contents of FCR[0] on both bits. Reset Source: mod_g_arstn
5:1	IT_TYPE	R	0h	0 Modem Interrupt. Priority=4 1 THR interrupt. Priority=3 2 RHR interrupt. Priority=2 3 Receiver line status error. Priority=3 6 Rx timeout. Priority=2 8 Xoff/Special character. Priority=5 16 CTS, RTS, DSR change state from active (low) to inactive (high). Priority=6
0	IT_PENDING	R	1h	0 An interrupt is pending 1 No interrupt is pending

14.7.2.4.2.13 UART_LCR Register

14.7.2.4.2.13.1 UART_LCR Register (Offset = Ch) [reset = 0h]

LCR[6:0] define parameters of the transmission and reception. Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.

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Table 14-10846. Instance Table

Instance Name	Physical Address
UART0	0280 000Ch
UART1	0281 000Ch
UART2	0282 000Ch
UART3	0283 000Ch
UART4	0284 000Ch
UART5	0285 000Ch
UART6	0286 000Ch
WKUP_UART0	2B30 000Ch

Figure 14-5360. UART_LCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
DIV_EN	BREAK_EN	PARITY_TYPE 2	PARITY_TYPE 1	PARITY_EN	NB_STOP	CHAR_LENGTH	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-10847. UART_LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	DIV_EN	R/W	0h	0 Normal operating condition 1 Divisor latch enable. Allows to access to DLL, DLH and other registers (refer to the registers mapping)
6	BREAK_EN	R/W	0h	Break control bit. 0 Normal operating condition. 1 Forces the transmitter output to go low to alert the communication terminal

Table 14-10847. UART_LCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PARITY_TYPE2	R/W	0h	Selects the forced parity format [if LCR[3] = 1]. If LCR[5] = 1 and LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data. Reset Source: mod_g_arstn
4	PARITY_TYPE1	R/W	0h	0 Odd parity is generated (if LCR[3] = 1) 1 Even parity is generated (if LCR[3] = 1)
3	PARITY_EN	R/W	0h	0 No parity 1 A parity bit is generated during transmission and the receiver checks for received parity.
2	NB_STOP	R/W	0h	Specifies the number of stop bits: 0 1 stop bits (word length = 5, 6, 7, 8) 1 1.5 stop bits (word length = 5) in USART mode. 2 stop bits (word length = 6, 7, 8)
1:0	CHAR_LENGTH	R/W	0h	Specifies the word length to be transmitted or received. 0 5 bits 1 6 bits 2 7 bits 3 8 bits

14.7.2.4.2.14 UART_MCR Register

14.7.2.4.2.14.1 UART_MCR Register (Offset = 10h) [reset = 0h]

MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.

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Table 14-10848. Instance Table

Instance Name	Physical Address
UART0	0280 0010h
UART1	0281 0010h
UART2	0282 0010h
UART3	0283 0010h
UART4	0284 0010h
UART5	0285 0010h
UART6	0286 0010h
WKUP_UART0	2B30 0010h

Figure 14-5361. UART_MCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TCR_TLR	XON_EN	LOOPBACK_EN	CD_STS_CH	RI_STS_CH	RTS	DTR
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10849. UART_MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RESERVED	R	0h	
6	TCR_TLR	R/W	0h	0 No action 1 Enables access to the TCR and TLR registers.
5	XON_EN	R/W	0h	0 Disable 'XON any' function 1 Enable 'XON any' function
4	LOOPBACK_EN	R/W	0h	0 Normal operating mode 1 Enable local loopback mode (internal). In this mode the MCR[3:0] signals are looped back into MSR[7:4]. The transmit output is looped back to the receive input internally

Table 14-10849. UART_MCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CD_STS_CH	R/W	0h	0 `In loopback forces DCD* input high and IRQ outputs to inactive state.` 1 `In loopback forces DCD* input low and IRQ outputs to inactive state.`
2	RI_STS_CH	R/W	0h	0 `In loopback forces RI* input high.` 1 `In loopback forces RI* input low.`
1	RTS	R/W	0h	In loop back controls MSR[4]. If auto-RTS is enabled the RTS* output is controlled by hardware flow control. 0 `Force RTS* output to inactive (high).` 1 `Force RTS* output to active (low).`
0	DTR	R/W	0h	0 `Force DTR* output to inactive (high).` 1 `Force DTR* output to active (low).`

14.7.2.4.2.15 UART_XON1_ADDR1 Register

14.7.2.4.2.15.1 UART_XON1_ADDR1 Register (Offset = 10h) [reset = 0h]

XON1/ADDR1 Register

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Table 14-10850. Instance Table

Instance Name	Physical Address
UART0	0280 0010h
UART1	0281 0010h
UART2	0282 0010h
UART3	0283 0010h
UART4	0284 0010h
UART5	0285 0010h
UART6	0286 0010h
WKUP_UART0	2B30 0010h

Figure 14-5362. UART_XON1_ADDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XON_WORD1							
R/W							
0h							

Table 14-10851. UART_XON1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XON_WORD1	R/W	0h	Used to store the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes. Reset Source: mod_g_arstn

14.7.2.4.2.16 UART_LSR_CIR Register

14.7.2.4.2.16.1 UART_LSR_CIR Register (Offset = 14h) [reset = 81h]

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Table 14-10852. Instance Table

Instance Name	Physical Address
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
WKUP_UART0	2B30 0014h

Figure 14-5363. UART_LSR_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E
R	R	R	NONE				R
1h	0h	0h	0h				1h

Table 14-10853. UART_LSR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	THR_EMPTY	R	1h	0 `Transmit holding register (TX FIFO) is not empty` 1 `Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed`
6	RESERVED	R	0h	
5	RX_STOP	R	0h	The RX_STOP is generated based on the value set in the BOF Length register (EBLR). It is cleared on a single read of the LSR register 0 `Reception is on going or waiting for a new frame` 1 `Reception is completed`
4:1	RESERVED	NONE	0h	Reserved

Table 14-10853. UART_LSR_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RX_FIFO_E	R	1h	0 `No data in the receive FIFO` 1 `At least one data character in the RX FIFO`

14.7.2.4.2.17 UART_LSR_IRDA Register

14.7.2.4.2.17.1 UART_LSR_IRDA Register (Offset = 14h) [reset = 83h]

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Table 14-10854. Instance Table

Instance Name	Physical Address
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
WKUP_UART0	2B30 0014h

Figure 14-5364. UART_LSR_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E
R	R	R	R	R	R	R	R
1h	0h	0h	0h	0h	0h	1h	1h

Table 14-10855. UART_LSR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	THR_EMPTY	R	1h	0 `Transmit holding register (TX FIFO) is not empty` 1 `Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed`
6	STS_FIFO_FULL	R	0h	0 `Status FIFO not full` 1 `Status FIFO full`
5	RX_LAST_BYTE	R	0h	0 `The RX FIFO (RHR) does not contain the last byte of the frame to be read` 1 `The RX FIFO (RHR) contains the last byte of the frame to be read.This bit is only set when the last byte of a frame is available to be read. It is used to determine the frame boundary. It is cleared on a single read of the LSR register`

Table 14-10855. UART_LSR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	FRAME_TOO_LONG	R	0h	0 No frame-too-long error in frame 1 Frame-too-long error in the frame at the top of the STATUS FIFO, [next character to be read]. This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) has been received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected
3	ABORT	R	0h	0 No abort pattern error in frame 1 Abort pattern is received. SIR & MIR: Abort pattern. FIR: Illegal symbol
2	CRC	R	0h	0 No CRC error in frame 1 CRC error in the frame at the top of the STATUS FIFO (next character to be read)
1	STS_FIFO_E	R	1h	0 Status FIFO not empty 1 Status FIFO empty
0	RX_FIFO_E	R	1h	0 No data in the receive FIFO 1 At least one data character in the RX FIFO

14.7.2.4.2.18 UART_LSR_UART Register

14.7.2.4.2.18.1 UART_LSR_UART Register (Offset = 14h) [reset = 60h]

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Table 14-10856. Instance Table

Instance Name	Physical Address
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
WKUP_UART0	2B30 0014h

Figure 14-5365. UART_LSR_UART Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E
R	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-10857. UART_LSR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RX_FIFO_STS	R	0h	0 Normal operation 1 At least one parity error, framing error or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.
6	TX_SR_E	R	1h	0 Transmitter hold (TX FIFO) and shift registers are not empty. 1 Transmitter hold (TX FIFO) and shift registers are empty
5	TX_FIFO_E	R	1h	0 Transmit hold register (TX FIFO) is not empty 1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed.

Table 14-10857. UART_LSR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RX_BI	R	0h	0 No break condition 1 A break was detected while the data being read from the RX FIFO was being received. (i.e. RX input was low for one character + 1 bit time frame).
3	RX_FE	R	0h	0 No framing error in data being read from RX FIFO. 1 Framing error occurred in data being read from RX FIFO.(received data did not have a valid stop bit)
2	RX_PE	R	0h	0 No parity error in data being read from RX FIFO. 1 Parity error in data being read from RX FIFO
1	RX_OE	R	0h	0 No overrun error 1 Overrun error has occurred. Set when the character held in the receive shift register is not transferred to the RX FIFO. This case can occurs only when receive FIFO is full.
0	RX_FIFO_E	R	0h	0 No data in the receive FIFO 1 At least one data character in the RX FIFO

14.7.2.4.2.19 UART_XON2_ADDR2 Register

14.7.2.4.2.19.1 UART_XON2_ADDR2 Register (Offset = 14h) [reset = 0h]

XON2/ADDR2 Register

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Table 14-10858. Instance Table

Instance Name	Physical Address
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
WKUP_UART0	2B30 0014h

Figure 14-5366. UART_XON2_ADDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XON_WORD2							
R/W							
0h							

Table 14-10859. UART_XON2_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XON_WORD2	R/W	0h	Used to store the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes. Reset Source: mod_g_arstn

14.7.2.4.2.20 UART_MSR Register

14.7.2.4.2.20.1 UART_MSR Register (Offset = 18h) [reset = 0h]

This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.

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Table 14-10860. Instance Table

Instance Name	Physical Address
UART0	0280 0018h
UART1	0281 0018h
UART2	0282 0018h
UART3	0283 0018h
UART4	0284 0018h
UART5	0285 0018h
UART6	0286 0018h
WKUP_UART0	2B30 0018h

Figure 14-5367. UART_MSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10861. UART_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	NCD_STS	R	0h	This bit is the complement of the DCD* input. In loop-back mode it is equivalent to MCR[3] Reset Source: mod_g_arstn
6	NRI_STS	R	0h	This bit is the complement of the RI* input. In loop-back mode it is equivalent to MCR[2] Reset Source: mod_g_arstn
5	NDSR_STS	R	0h	This bit is the complement of the DSR* input. In loop-back mode, it is equivalent to MCR[0] Reset Source: mod_g_arstn
4	NCTS_STS	R	0h	This bit is the complement of the CTS* input. In loop-back mode it is equivalent to MCR[1] Reset Source: mod_g_arstn

Table 14-10861. UART_MSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DCD_STS	R	0h	Indicates that DCD* input [or MCR[3] in loop back] has changed. Cleared on a read. Reset Source: mod_g_arstn
2	RI_STS	R	0h	Indicates that RI* input [or MCR[2] in loop back] has changed state from low to high. Cleared on a read. Reset Source: mod_g_arstn
1	DSR_STS	R	0h	1 `Indicates that DSR* input (or MCR[0] in loop back) has changed state. Cleared on a read`
0	CTS_STS	R	0h	1 `Indicates that CTS* input (or MCR[1] in loop back) has changed state. Cleared on a read.`

14.7.2.4.2.21 UART_TCR Register

14.7.2.4.2.21.1 UART_TCR Register (Offset = 18h) [reset = Fh]

Transmission Control Register

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Table 14-10862. Instance Table

Instance Name	Physical Address
UART0	0280 0018h
UART1	0281 0018h
UART2	0282 0018h
UART3	0283 0018h
UART4	0284 0018h
UART5	0285 0018h
UART6	0286 0018h
WKUP_UART0	2B30 0018h

Figure 14-5368. UART_TCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			
R/W				R/W			
0h				Fh			

Table 14-10863. UART_TCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	RX_FIFO_TRIG_START	R/W	0h	RX FIFO trigger level to RESTORE transmission (0 - 60) Reset Source: mod_g_arstn
3:0	RX_FIFO_TRIG_HALT	R/W	Fh	RX FIFO trigger level to HALT transmission (0 - 60) Reset Source: mod_g_arstn

14.7.2.4.2.22 UART_XOFF1 Register

14.7.2.4.2.22.1 UART_XOFF1 Register (Offset = 18h) [reset = 0h]

XOFF1 Register

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Table 14-10864. Instance Table

Instance Name	Physical Address
UART0	0280 0018h
UART1	0281 0018h
UART2	0282 0018h
UART3	0283 0018h
UART4	0284 0018h
UART5	0285 0018h
UART6	0286 0018h
WKUP_UART0	2B30 0018h

Figure 14-5369. UART_XOFF1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XOFF_WORD1							
R/W							
0h							

Table 14-10865. UART_XOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XOFF_WORD1	R/W	0h	Used to store the 8-bit XOFF1 character in used in UART modes. Reset Source: mod_g_arstn

14.7.2.4.2.23 UART_SPR Register

14.7.2.4.2.23.1 UART_SPR Register (Offset = 1Ch) [reset = 0h]

This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

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Table 14-10866. Instance Table

Instance Name	Physical Address
UART0	0280 001Ch
UART1	0281 001Ch
UART2	0282 001Ch
UART3	0283 001Ch
UART4	0284 001Ch
UART5	0285 001Ch
UART6	0286 001Ch
WKUP_UART0	2B30 001Ch

Figure 14-5370. UART_SPR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SPR_WORD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10867. UART_SPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	SPR_WORD	R/W	0h	Scratchpad register Reset Source: mod_g_arstn

14.7.2.4.2.24 UART_TLR Register

14.7.2.4.2.24.1 UART_TLR Register (Offset = 1Ch) [reset = 0h]

Trigger Level Register

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Table 14-10868. Instance Table

Instance Name	Physical Address
UART0	0280 001Ch
UART1	0281 001Ch
UART2	0282 001Ch
UART3	0283 001Ch
UART4	0284 001Ch
UART5	0285 001Ch
UART6	0286 001Ch
WKUP_UART0	2B30 001Ch

Figure 14-5371. UART_TLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			
R/W				R/W			
0h				0h			

Table 14-10869. UART_TLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	RX_FIFO_TRIG_DMA	R/W	0h	Receive FIFO trigger level Reset Source: mod_g_arstn
3:0	TX_FIFO_TRIG_DMA	R/W	0h	Transmit FIFO trigger level Reset Source: mod_g_arstn

14.7.2.4.2.25 UART_XOFF2 Register

14.7.2.4.2.25.1 UART_XOFF2 Register (Offset = 1Ch) [reset = 0h]

XOFF2 Register

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Table 14-10870. Instance Table

Instance Name	Physical Address
UART0	0280 001Ch
UART1	0281 001Ch
UART2	0282 001Ch
UART3	0283 001Ch
UART4	0284 001Ch
UART5	0285 001Ch
UART6	0286 001Ch
WKUP_UART0	2B30 001Ch

Figure 14-5372. UART_XOFF2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XOFF_WORD2							
R/W							
0h							

Table 14-10871. UART_XOFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XOFF_WORD2	R/W	0h	Used to store the 8-bit XOFF2 character in used in UART modes. Reset Source: mod_g_arstn

14.7.2.4.2.26 UART_MDR1 Register

14.7.2.4.2.26.1 UART_MDR1 Register (Offset = 20h) [reset = 7h]

The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation.
Note: If the module is disabled by setting the MODE_SELECT field to 111, interrupt requests can still be generated unless disabled through the interrupt enable register (UART_IER). In this case, UART mode interrupts are visible. Reading the interrupt identification register (UART_IIR) shows UART mode interrupt flags.

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Table 14-10872. Instance Table

Instance Name	Physical Address
UART0	0280 0020h
UART1	0281 0020h
UART2	0282 0020h
UART3	0283 0020h
UART4	0284 0020h
UART5	0285 0020h
UART6	0286 0020h
WKUP_UART0	2B30 0020h

Figure 14-5373. UART_MDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		
R/W	R/W	R/W	R/W	R/W	R/W		
0h	0h	0h	0h	0h	7h		

Table 14-10873. UART_MDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	FRAME_END_MODE	R/W	0h	IrDA mode only. 0 `Frame-length method` 1 `Set EOT bit method`
6	SIP_MODE	R/W	0h	MIR/FIR modes only. 0 `Manual SIP mode: SIP is generated with the control of ACREG[3]` 1 `Automatic SIP mode: SIP is generated after each transmission.`

Table 14-10873. UART_MDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SCT	R/W	0h	Store and control the transmission 0 Starts the Infrared transmission as soon as a value is written to THR 1 Starts the Infrared transmission with the control of ACREG[2]. Note: before starting any transmission, there must be no reception on going.
4	SET_TXIR	R/W	0h	Used to configure the infrared transceiver. 0 No action if MDR2[7]=0. TXIR pin output is forced low if MDR2[7]=1 1 TXIR pin output is forced high (not dependant of MDR2[7] value).
3	IR_SLEEP	R/W	0h	0 IrDA/CIR sleep mode disabled 1 IrDA/CIR sleep mode enabled
2:0	MODE_SELECT	R/W	7h	0 UART 16x mode 1 SIR mode 2 UART 16x auto-baud 3 UART 13x mode 4 MIR mode 5 FIR mode 6 CIR mode 7 Disable (default state)

14.7.2.4.2.27 UART_MDR2 Register

14.7.2.4.2.27.1 UART_MDR2 Register (Offset = 24h) [reset = 0h]

IR-IrDA and IR-CIR modes only. MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0]. Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.

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Table 14-10874. Instance Table

Instance Name	Physical Address
UART0	0280 0024h
UART1	0281 0024h
UART2	0282 0024h
UART3	0283 0024h
UART4	0284 0024h
UART5	0285 0024h
UART6	0286 0024h
WKUP_UART0	2B30 0024h

Figure 14-5374. UART_MDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN
R/W	R/W	R/W		R/W	R/W		R
0h	0h	0h		0h	0h		0h

Table 14-10875. UART_MDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	SET_TXIR_ALT	R/W	0h	Provide alternate functionnality for MDR1[4] [SET_TXIR] 0 `Normal mode` 1 `Alternate mode for SET_TXIR`
6	IRRXINVERT	R/W	0h	Only for IR mode [IRDA & CIR]Invert RX pin inside the module before the voting or sampling system logic of the infra red block. This will not affect the RX path in UART Modem modes. 0 `inversion is performed` 1 `No inversion is performed`

Table 14-10875. UART_MDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	CIR_PULSE_MODE	R/W	0h	CIR Pulse modulation definition. It defines high level of the pulse width associated with a digit: 0 `Pulse width of 3 from 12 cycles` 1 `Pulse width of 4 from 12 cycles` 2 `Pulse width of 5 from 12 cycles` 3 `Pulse width of 6 from 12 cycles`
3	UART_PULSE	R/W	0h	UART mode only. Used to allow pulse shaping in UART mode. 0 `normal UART mode` 1 `UART mode with a pulse shaping`
2:1	STS_FIFO_TRIG	R/W	0h	Only for IR-IRDA mode. Frame Status FIFO Threshold select: 0 `1 entry` 1 `4 entries` 2 `7 entries` 3 `8 entries`
0	IRTX_UNDERRUN	R	0h	IRDA Transmission status interrupt.When the IIR[5] interrupt occurs, the meaning of the interrupt is : 0 `the last bit of the frame has been transmitted successfully without error.` 1 `an underrun has occurred. The last bit of the frame has been transmitted but with an underrun error present. The bit is reset to '0' when the RESUME register is read.`

14.7.2.4.2.28 UART_SFLSR Register

14.7.2.4.2.28.1 UART_SFLSR Register (Offset = 28h) [reset = 0h]

IrDA modes only. Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).

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Table 14-10876. Instance Table

Instance Name	Physical Address
UART0	0280 0028h
UART1	0281 0028h
UART2	0282 0028h
UART3	0283 0028h
UART4	0284 0028h
UART5	0285 0028h
UART6	0286 0028h
WKUP_UART0	2B30 0028h

Figure 14-5375. UART_SFLSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED5			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED0
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h

Table 14-10877. UART_SFLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED5	R	0h	
4	OE_ERROR	R	0h	1 `Overrun error in RX FIFO when frame at top of RX FIFO was received.`
3	FRAME_TOO_LONG_ERROR	R	0h	1 `Frame-length too long error in frame at top of RX FIFO.`
2	ABORT_DETECT	R	0h	1 `Abort pattern detected in frame at top of RX FIFO`

Table 14-10877. UART_SFLSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CRC_ERROR	R	0h	1 `CRC error in frame at top of RX FIFO. top of RX FIFO = Next frame to be read from RX FIFO`
0	RESERVED0	R	0h	

14.7.2.4.2.29 UART_TXFLL Register

14.7.2.4.2.29.1 UART_TXFLL Register (Offset = 28h) [reset = 0h]

IrDA modes only. The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 14-10878. Instance Table

Instance Name	Physical Address
UART0	0280 0028h
UART1	0281 0028h
UART2	0282 0028h
UART3	0283 0028h
UART4	0284 0028h
UART5	0285 0028h
UART6	0286 0028h
WKUP_UART0	2B30 0028h

Figure 14-5376. UART_TXFLL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
TXFLL							
W							
0h							

Table 14-10879. UART_TXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	TXFLL	W	0h	LSB register used to specify the frame length Reset Source: mod_g_arstn

14.7.2.4.2.30 UART_RESUME Register

14.7.2.4.2.30.1 UART_RESUME Register (Offset = 2Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only. This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

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Table 14-10880. Instance Table

Instance Name	Physical Address
UART0	0280 002Ch
UART1	0281 002Ch
UART2	0282 002Ch
UART3	0283 002Ch
UART4	0284 002Ch
UART5	0285 002Ch
UART6	0286 002Ch
WKUP_UART0	2B30 002Ch

Figure 14-5377. UART_RESUME Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESUME							
R							
0h							

Table 14-10881. UART_RESUME Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RESUME	R	0h	Dummy read to restart the TX or RX Reset Source: mod_g_arstn

14.7.2.4.2.31 UART_TXFLH Register

14.7.2.4.2.31.1 UART_TXFLH Register (Offset = 2Ch) [reset = 0h]

IrDA modes only. The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 14-10882. Instance Table

Instance Name	Physical Address
UART0	0280 002Ch
UART1	0281 002Ch
UART2	0282 002Ch
UART3	0283 002Ch
UART4	0284 002Ch
UART5	0285 002Ch
UART6	0286 002Ch
WKUP_UART0	2B30 002Ch

Figure 14-5378. UART_TXFLH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TXFLH</td></tr>
<tr><td colspan="3">R</td><td colspan="5">W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-10883. UART_TXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED	R	0h	
4:0	TXFLH	W	0h	MSB register used to specify the frame length Reset Source: mod_g_arstn

14.7.2.4.2.32 UART_RXFLL Register

14.7.2.4.2.32.1 UART_RXFLL Register (Offset = 30h) [reset = 0h]

IrDA modes only. The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 14-10884. Instance Table

Instance Name	Physical Address
UART0	0280 0030h
UART1	0281 0030h
UART2	0282 0030h
UART3	0283 0030h
UART4	0284 0030h
UART5	0285 0030h
UART6	0286 0030h
WKUP_UART0	2B30 0030h

Figure 14-5379. UART_RXFLL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RXFLL							
W							
0h							

Table 14-10885. UART_RXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	RXFLL	W	0h	LSB register used to specify the frame length in reception Reset Source: mod_g_arstn

14.7.2.4.2.33 UART_SFREGL Register

14.7.2.4.2.33.1 UART_SFREGL Register (Offset = 30h) [reset = 0h]

IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 14-10886. Instance Table

Instance Name	Physical Address
UART0	0280 0030h
UART1	0281 0030h
UART2	0282 0030h
UART3	0283 0030h
UART4	0284 0030h
UART5	0285 0030h
UART6	0286 0030h
WKUP_UART0	2B30 0030h

Figure 14-5380. UART_SFREGL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SFREGL							
R							
0h							

Table 14-10887. UART_SFREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	SFREGL	R	0h	LSB part of the frame length Reset Source: mod_g_arstn

14.7.2.4.2.34 UART_RXFLH Register

14.7.2.4.2.34.1 UART_RXFLH Register (Offset = 34h) [reset = 0h]

IrDA modes only. The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 14-10888. Instance Table

Instance Name	Physical Address
UART0	0280 0034h
UART1	0281 0034h
UART2	0282 0034h
UART3	0283 0034h
UART4	0284 0034h
UART5	0285 0034h
UART6	0286 0034h
WKUP_UART0	2B30 0034h

Figure 14-5381. UART_RXFLH Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">RXFLH</td></tr>
<tr><td colspan="4">R</td><td colspan="4">W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-10889. UART_RXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:4	RESERVED	R	0h	
3:0	RXFLH	W	0h	MSB register used to specify the frame length in reception Reset Source: mod_g_arstn

14.7.2.4.2.35 UART_SFREGH Register

14.7.2.4.2.35.1 UART_SFREGH Register (Offset = 34h) [reset = 0h]

IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 14-10890. Instance Table

Instance Name	Physical Address
UART0	0280 0034h
UART1	0281 0034h
UART2	0282 0034h
UART3	0283 0034h
UART4	0284 0034h
UART5	0285 0034h
UART6	0286 0034h
WKUP_UART0	2B30 0034h

Figure 14-5382. UART_SFREGH Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				SFREGH			
R				R			
0h				0h			

Table 14-10891. UART_SFREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:4	RESERVED	R	0h	
3:0	SFREGH	R	0h	MSB part of the frame length Reset Source: mod_g_arstn

14.7.2.4.2.36 UART_BLR Register

14.7.2.4.2.36.1 UART_BLR Register (Offset = 38h) [reset = 40h]

IrDA modes only. Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

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Table 14-10892. Instance Table

Instance Name	Physical Address
UART0	0280 0038h
UART1	0281 0038h
UART2	0282 0038h
UART3	0283 0038h
UART4	0284 0038h
UART5	0285 0038h
UART6	0286 0038h
WKUP_UART0	2B30 0038h

Figure 14-5383. UART_BLR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STS_FIFO_RESET	XBOF_TYPE	RESERVED					
R/W1TS	R/W	R					
0h	1h	0h					

Table 14-10893. UART_BLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	STS_FIFO_RESET	R/W1TS	0h	Status FIFO reset. This bit is self-clearing Reset Source: mod_g_arstn
6	XBOF_TYPE	R/W	1h	SIR xBOF select. 0 `0xFF` 1 `0xC0`
5:0	RESERVED	R	0h	

14.7.2.4.2.37 UART_UASR Register

14.7.2.4.2.37.1 UART_UASR Register (Offset = 38h) [reset = 0h]

UART Autobauding Status Register

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Table 14-10894. Instance Table

Instance Name	Physical Address
UART0	0280 0038h
UART1	0281 0038h
UART2	0282 0038h
UART3	0283 0038h
UART4	0284 0038h
UART5	0285 0038h
UART6	0286 0038h
WKUP_UART0	2B30 0038h

Figure 14-5384. UART_UASR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PARITY_TYPE		BIT_BY_CHAR	SPEED				
R		R	R				
0h		0h	0h				

Table 14-10895. UART_UASR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	PARITY_TYPE	R	0h	00 => No Parity identified. 01 => Parity space. 10 => Even Parity. 11 => Odd Parity Reset Source: mod_g_arstn
5	BIT_BY_CHAR	R	0h	0 => 7 bits character identified. 1 => 8 bits character identified Reset Source: mod_g_arstn
4:0	SPEED	R	0h	Used to report the speed identified. 00000 => No speed identified. 00001 => 115200 bauds. 00010 => 57600 bauds. 00011 => 38400 bauds. 00100 => 28800 bauds. 00101 => 19200 bauds. 00110 => 14400 bauds. 00111 => 9600 bauds. 01000 => 4800 bauds. 01001 => 2400 bauds. 01010 => 1200 bauds Reset Source: mod_g_arstn

14.7.2.4.2.38 UART_ACREG Register

14.7.2.4.2.38.1 UART_ACREG Register (Offset = 3Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only.

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Table 14-10896. Instance Table

Instance Name	Physical Address
UART0	0280 003Ch
UART1	0281 003Ch
UART2	0282 003Ch
UART3	0283 003Ch
UART4	0284 003Ch
UART5	0285 003Ch
UART6	0286 003Ch
WKUP_UART0	2B30 003Ch

Figure 14-5385. UART_ACREG Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN
R/W	R/W	R/W	R/W	R/W1TS	R/W1TS	R/W	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10897. UART_ACREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	PULSE_TYPE	R/W	0h	SIR pulse width select: 0 `3/16 of baud-rate pulse width` 1 `1.6us`
6	SD_MOD	R/W	0h	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers. 0 `SD pin is set to high` 1 `SD pin is set to low`
5	DIS_IR_RX	R/W	0h	0 `Normal operation (RX input automatically disabled during transmit but enabled outside of transmit operation).` 1 `Disables RX input (permanent state - independent of transmit).`

Table 14-10897. UART_ACREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DIS_TX_UNDERRUN	R/W	0h	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4]=1, garbage data is sent over TX line. 0 `Long stop bits cannot be transmitted, TX underrun is enabled` 1 `Long stop bits can be transmitted, TX underrun is disabled`
3	SEND_SIP	R/W1TS	0h	MIR/FIR Modes only.Send Serial Infrared Interaction Pulse [SIP] If this bit is set during a MIR/FIR transmission, the SIP will be send at the end of it.This bit automatically gets cleared at the end of the SIP transmission. 0 `No action` 1 `Send SIP pulse.`
2	SCTX_EN	R/W1TS	0h	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit the TX state machine starts frame transmission. This bit is self-clearing. Reset Source: mod_g_arstn
1	ABORT_EN	R/W	0h	Frame Abort. The LH can intentionally abort transmission of a frame by Writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If transmit FIFO is not empty and MDR1[5]=1, UART IrDA will start a new transfer with data of previous frame as soon as abort frame has been sent. Therefore, TX FIFO must be reset before sending an abort frame. Reset Source: mod_g_arstn
0	EOT_EN	R/W1TS	0h	EOT [end of transmission] bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit automatically gets cleared when the LH writes to the THR [TX FIFO]. Reset Source: mod_g_arstn

14.7.2.4.2.39 UART_SCR Register

14.7.2.4.2.39.1 UART_SCR Register (Offset = 40h) [reset = 0h]

Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.

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Table 14-10898. Instance Table

Instance Name	Physical Address
UART0	0280 0040h
UART1	0281 0040h
UART2	0282 0040h
UART3	0283 0040h
UART4	0284 0040h
UART5	0285 0040h
UART6	0286 0040h
WKUP_UART0	2B30 0040h

Figure 14-5386. UART_SCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2		DMA_MODE_CTL
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		0h

Table 14-10899. UART_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	RX_TRIG_GRANU1	R/W	0h	0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL. 1 ENABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL.
6	TX_TRIG_GRANU1	R/W	0h	0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER TX LEVEL. 1 Enables the granularity of 1 for trigger TX level.
5	DSR_IT	R/W	0h	0 DISABLES DSR* INTERRUPT. 1 ENABLES DSR* INTERRUPT.

Table 14-10899. UART_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RX_CTS_DSR_WAKE_UP_ENABLE	R/W	0h	0 DISABLES THE WAKE UP INTERRUPT AND CLEARS SSR[1]. 1 Waits for a falling edge of pins RX, CTS* or DSR* to generate an interrupt
3	TX_EMPTY_CTL_IT	R/W	0h	0 Normal mode for THR interrupt (See UART mode interrupts table). 1 THE THR INTERRUPT IS GENERATED WHEN TX FIFO AND TX SHIFT REGISTER ARE EMPTY.
2:1	DMA_MODE_2	R/W	0h	Used to specify the DMA mode valid if SCR[0] = 1 0 DMA mode 0 (no DMA) 1 DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX) 2 DMA mode 2 (UART_nDMA_REQ[0] in RX) 3 DMA mode 3 (UART_nDMA_REQ[0] in TX)
0	DMA_MODE_CTL	R/W	0h	0 The DMA_MODE is set with FCR[3] 1 The DMA_MODE is set with SCR[2:1]

14.7.2.4.2.40 UART_SSR Register

14.7.2.4.2.40.1 UART_SSR Register (Offset = 44h) [reset = 4h]

Note: Bit 1 is reset only when SCR[4] is reset to 0.

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Table 14-10900. Instance Table

Instance Name	Physical Address
UART0	0280 0044h
UART1	0281 0044h
UART2	0282 0044h
UART3	0283 0044h
UART4	0284 0044h
UART5	0285 0044h
UART6	0286 0044h
WKUP_UART0	2B30 0044h

Figure 14-5387. UART_SSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>DMA_COUNTER_RST</td><td>RX_CTS_DSR_WAKE_UP_STS</td><td>TX_FIFO_FULL</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10901. UART_SSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:3	RESERVED	R	0h	
2	DMA_COUNTER_RST	R/W	1h	0 The DMA counter will not be reset if the corresponding FIFO is reset (via FCR[1] or FCR[2]) 1 The DMA counter will be reset if corresponding FIFO is reset (via FCR[1] or FCR[2])
1	RX_CTS_DSR_WAKE_UP_STS	R	0h	0 No falling edge event on RX, CTS* and DSR* 1 A falling edge occurred on RX, CTS* or DSR*
0	TX_FIFO_FULL	R	0h	0 TX FIFO is not full 1 TX FIFO is full.

14.7.2.4.2.41 UART_EBLR Register

14.7.2.4.2.41.1 UART_EBLR Register (Offset = 48h) [reset = 0h]

IR-IrDA and IR-CIR modes only.
In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.
In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).
In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the UART_ACREG[5] to 1.
Note: If the RX_STOP interrupt occurs before a byte boundary, the remaining bits of the last byte are filled with 0s and passed into the RX FIFO.

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Table 14-10902. Instance Table

Instance Name	Physical Address
UART0	0280 0048h
UART1	0281 0048h
UART2	0282 0048h
UART3	0283 0048h
UART4	0284 0048h
UART5	0285 0048h
UART6	0286 0048h
WKUP_UART0	2B30 0048h

Figure 14-5388. UART_EBLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_24</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EBLR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10903. UART_EBLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	

Table 14-10903. UART_EBLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	EBLR	R/W	0h	IR-IRDA mode: This register allows to define up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt [IIR[2]]. 0x00: feature disabled. 0x01: generate RX_STOP interrupt after receiving one zero bit. ... 0xFF: generate RX_STOP interrupt after receiving 255 zero bits. Reset Source: mod_g_arstn

14.7.2.4.2.42 UART_MVR Register

14.7.2.4.2.42.1 UART_MVR Register (Offset = 50h) [reset = 47424E03h]

The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned Notes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification). For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8

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Table 14-10904. Instance Table

Instance Name	Physical Address
UART0	0280 0050h
UART1	0281 0050h
UART2	0282 0050h
UART3	0283 0050h
UART4	0284 0050h
UART5	0285 0050h
UART6	0286 0050h
WKUP_UART0	2B30 0050h

Figure 14-5389. UART_MVR Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		R		R			
1h		0h		742h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
742h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
9h					6h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		3h					

Table 14-10905. UART_MVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme revision number of module Reset Source: mod_g_arstn
29:28	RESERVED	R	0h	
27:16	FUNC	R	742h	Function revision number of module Reset Source: mod_g_arstn
15:11	RTL	R	9h	Rtl revision number of module Reset Source: mod_g_arstn
10:8	MAJOR	R	6h	Major revision number of the module. Reset Source: mod_g_arstn

Table 14-10905. UART_MVR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	CUSTOM	R	0h	Custom revision number of the module. Reset Source: mod_g_arstn
5:0	MINOR	R	3h	Minor revision number of the module. Reset Source: mod_g_arstn

14.7.2.4.2.43 UART_SYSC Register

14.7.2.4.2.43.1 UART_SYSC Register (Offset = 54h) [reset = 0h]

The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.

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Table 14-10906. Instance Table

Instance Name	Physical Address
UART0	0280 0054h
UART1	0281 0054h
UART2	0282 0054h
UART3	0283 0054h
UART4	0284 0054h
UART5	0285 0054h
UART6	0286 0054h
WKUP_UART0	2B30 0054h

Figure 14-5390. UART_SYSC Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R			R/W		R/W	W	R/W
0h			0h		0h	0h	0h

Table 14-10907. UART_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:5	RESERVED	R	0h	
4:3	IDLEMODE	R/W	0h	POWER MANAGEMENT REQ/ACK CONTROL REF: OCP DESIGN GUIDELINES VERSION 1.1 0 `Force idle. An idle request is acknowledged unconditionally` 1 `No-idle. An idle request is never acknowledged.` 2 `Smart idle. Acknowledgement to an idle request is given based in the internal activity of the module.` 3 `reserved`

Table 14-10907. UART_SYSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ENAWAKEUP	R/W	0h	WAKE UP FEATURE CONTROL 0 Wake up is disabled 1 Wake up capability is enabled
1	SOFTRESET	W	0h	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. During reads it always returns a 0. 0 Normal mode 1 The module is reset
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy 0 Clock is running 1 Automatic OCP clock gating strategy is applied, based on the OCP interface activity

14.7.2.4.2.44 UART_SYSS Register

14.7.2.4.2.44.1 UART_SYSS Register (Offset = 58h) [reset = 0h]

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Table 14-10908. Instance Table

Instance Name	Physical Address
UART0	0280 0058h
UART1	0281 0058h
UART2	0282 0058h
UART3	0283 0058h
UART4	0284 0058h
UART5	0285 0058h
UART6	0286 0058h
WKUP_UART0	2B30 0058h

Figure 14-5391. UART_SYSS Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							0h

Table 14-10909. UART_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:1	RESERVED	R	0h	
0	RESETDONE	R	0h	Internal Reset Monitoring 0 Internal Module Reset is ongoing 1 Reset completed

14.7.2.4.2.45 UART_WER Register

14.7.2.4.2.45.1 UART_WER Register (Offset = 5Ch) [reset = FFh]

The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.

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Table 14-10910. Instance Table

Instance Name	Physical Address
UART0	0280 005Ch
UART1	0281 005Ch
UART2	0282 005Ch
UART3	0283 005Ch
UART4	0284 005Ch
UART5	0285 005Ch
UART6	0286 005Ch
WKUP_UART0	2B30 005Ch

Figure 14-5392. UART_WER Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
EVENT_7_TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RI_ACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h

Table 14-10911. UART_WER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7	EVENT_7_TX_WAKEUP_EN	R/W	1h	0 Event is not allowed to wake up the system 1 EVENT CAN WAKE UP THE SYSTEM: Event can be: THR_IT or TX_DMA request and/or TX_SATUS_IT
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
5	EVENT_5_RHR_INTERRUPT	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system

Table 14-10911. UART_WER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EVENT_4_RX_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
3	EVENT_3_DCD_CD_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
2	EVENT_2_RI_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
1	EVENT_1_DSR_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
0	EVENT_0_CTS_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system

14.7.2.4.2.46 UART_CFPS Register

14.7.2.4.2.46.1 UART_CFPS Register (Offset = 60h) [reset = 69h]

Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.

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Table 14-10912. Instance Table

Instance Name	Physical Address
UART0	0280 0060h
UART1	0281 0060h
UART2	0282 0060h
UART3	0283 0060h
UART4	0284 0060h
UART5	0285 0060h
UART6	0286 0060h
WKUP_UART0	2B30 0060h

Figure 14-5393. UART_CFPS Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
CFPS							
R/W							
69h							

Table 14-10913. UART_CFPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	
7:0	CFPS	R/W	69h	System clock frequency prescaler at [12x multiple]. Examples for CFPS values are given in the table below. Target Freq [KHz] CFPS [decimal] Actual Freq[KHz] 30 133 30.08 32.75 122 32.79 36 111 36.04 36.7 109 36.69 38* 105 38.1 40 100 40 56.8 70 57.14 * configured at reset to this value Note: CFPS = 0 is not supported. Reset Source: mod_g_arstn

14.7.2.4.2.47 UART_RXFIFO_LVL Register

14.7.2.4.2.47.1 UART_RXFIFO_LVL Register (Offset = 64h) [reset = 0h]

Level of the RX FIFO

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Table 14-10914. Instance Table

Instance Name	Physical Address
UART0	0280 0064h
UART1	0281 0064h
UART2	0282 0064h
UART3	0283 0064h
UART4	0284 0064h
UART5	0285 0064h
UART6	0286 0064h
WKUP_UART0	2B30 0064h

Figure 14-5394. UART_RXFIFO_LVL Name Register

31	30	29	28	27	26	25	24
RESERVED24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED24							
R							
0h							
7	6	5	4	3	2	1	0
RXFIFO_LVL							
R							
0h							

Table 14-10915. UART_RXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	
7:0	RXFIFO_LVL	R	0h	Reset Source: mod_g_arstn

14.7.2.4.2.48 UART_TXFIFO_LVL Register

14.7.2.4.2.48.1 UART_TXFIFO_LVL Register (Offset = 68h) [reset = 0h]

Level of the TX FIFO

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Table 14-10916. Instance Table

Instance Name	Physical Address
UART0	0280 0068h
UART1	0281 0068h
UART2	0282 0068h
UART3	0283 0068h
UART4	0284 0068h
UART5	0285 0068h
UART6	0286 0068h
WKUP_UART0	2B30 0068h

Figure 14-5395. UART_TXFIFO_LVL Name Register

31	30	29	28	27	26	25	24
RESERVED24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED24							
R							
0h							
7	6	5	4	3	2	1	0
TXFIFO_LVL							
R							
0h							

Table 14-10917. UART_TXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	
7:0	TXFIFO_LVL	R	0h	Reset Source: mod_g_arstn

14.7.2.4.2.49 UART_IER2 Register

14.7.2.4.2.49.1 UART_IER2 Register (Offset = 6Ch) [reset = 0h]

Enables RX/TX FIFOs empty corresponding interrupts.

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Table 14-10918. Instance Table

Instance Name	Physical Address
UART0	0280 006Ch
UART1	0281 006Ch
UART2	0282 006Ch
UART3	0283 006Ch
UART4	0284 006Ch
UART5	0285 006Ch
UART6	0286 006Ch
WKUP_UART0	2B30 006Ch

Figure 14-5396. UART_IER2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>RHR_IT_DIS</td><td>EN_TXFIFO_EMPTY</td><td>EN_RXFIFO_EMPTY</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10919. UART_IER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:3	RESERVED	R	0h	
2	RHR_IT_DIS	R/W	0h	`0 Enables the RHR interrupt.` `1 Disables the RHR interrupt.`
1	EN_TXFIFO_EMPTY	R/W	0h	Enables[1]/DISABLES[00 EN_TXFIFO_EMPTY interrupt. Reset Source: mod_g_arstn
0	EN_RXFIFO_EMPTY	R/W	0h	Enables[1]/disables[0] EN_RXFIFO_EMPTY interrupt. Reset Source: mod_g_arstn

14.7.2.4.2.50 UART_ISR2 Register

14.7.2.4.2.50.1 UART_ISR2 Register (Offset = 70h) [reset = 3h]

Status of RX/TX FIFOs empty corresponding interrupts.

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Table 14-10920. Instance Table

Instance Name	Physical Address
UART0	0280 0070h
UART1	0281 0070h
UART2	0282 0070h
UART3	0283 0070h
UART4	0284 0070h
UART5	0285 0070h
UART6	0286 0070h
WKUP_UART0	2B30 0070h

Figure 14-5397. UART_ISR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TXFIFO_EMPTY_STS</td><td>RXFIFO_EMPTY_STS</td></tr>
<tr><td colspan="6">R</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-10921. UART_ISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:2	RESERVED	R	0h	
1	TXFIFO_EMPTY_STS	R/W1TC	1h	TXFIFO interrupt pending 0 `TXFIFO_EMPTY interrupt not pending.` 1 `TXFIFO_EMPTY interrupt pending.`
0	RXFIFO_EMPTY_STS	R/W1TC	1h	RXFIFO interrupt pending 0 `RXFIFO_EMPTY interrupt not pending.` 1 `RXFIFO_EMPTY interrupt pending.`

14.7.2.4.2.51 UART_FREQ_SEL Register

14.7.2.4.2.51.1 UART_FREQ_SEL Register (Offset = 74h) [reset = 1Ah]

Sample per bit value selector

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Table 14-10922. Instance Table

Instance Name	Physical Address
UART0	0280 0074h
UART1	0281 0074h
UART2	0282 0074h
UART3	0283 0074h
UART4	0284 0074h
UART5	0285 0074h
UART6	0286 0074h
WKUP_UART0	2B30 0074h

Figure 14-5398. UART_FREQ_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
FREQ_SEL							
R/W							
1Ah							

Table 14-10923. UART_FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	RESERVED
7:0	FREQ_SEL	R/W	1Ah	Sets the sample per bit if non default frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal or higher then 6. Reset Source: mod_g_arstn

14.7.2.4.2.52 UART_ABAUD_1ST_CHAR Register

14.7.2.4.2.52.1 UART_ABAUD_1ST_CHAR Register (Offset = 78h) [reset = 0h]

Unused

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Table 14-10924. Instance Table

Instance Name	Physical Address
UART0	0280 0078h
UART1	0281 0078h
UART2	0282 0078h
UART3	0283 0078h
UART4	0284 0078h
UART5	0285 0078h
UART6	0286 0078h
WKUP_UART0	2B30 0078h

Figure 14-5399. UART_ABAUD_1ST_CHAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-10925. UART_ABAUD_1ST_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	

14.7.2.4.2.53 UART_BAUD_2ND_CHAR Register

14.7.2.4.2.53.1 UART_BAUD_2ND_CHAR Register (Offset = 7Ch) [reset = 0h]

Unused

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Table 14-10926. Instance Table

Instance Name	Physical Address
UART0	0280 007Ch
UART1	0281 007Ch
UART2	0282 007Ch
UART3	0283 007Ch
UART4	0284 007Ch
UART5	0285 007Ch
UART6	0286 007Ch
WKUP_UART0	2B30 007Ch

Figure 14-5400. UART_BAUD_2ND_CHAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-10927. UART_BAUD_2ND_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	

14.7.2.4.2.54 UART_MDR3 Register

14.7.2.4.2.54.1 UART_MDR3 Register (Offset = 80h) [reset = 0h]

Mode definition register 3.

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Table 14-10928. Instance Table

Instance Name	Physical Address
UART0	0280 0080h
UART1	0281 0080h
UART2	0282 0080h
UART3	0283 0080h
UART4	0284 0080h
UART5	0285 0080h
UART6	0286 0080h
WKUP_UART0	2B30 0080h

Figure 14-5401. UART_MDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			DIR_EN	DIR_POL	SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-10929. UART_MDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	
7:5	RESERVED1	R	0h	Reserved
4	DIR_EN	R/W	0h	RS-485 External Transceiver Direction Enable Reset Source: mod_g_arstn
3	DIR_POL	R/W	0h	RS-485 External Transceiver Direction Polarity. 0 => TX: RTS=0, RX: RTS=1. 1 => TX: RTS=1, RX: RTS=0 Reset Source: mod_g_arstn
2	SET_DMA_TX_THRESHOLD	R/W	0h	Enable to set different TX DMA threshold then 64-trigger [usage of new register TX_DNA_THRESHOLD] Reset Source: mod_g_arstn
1	NONDEFAULT_FREQ	R/W	0h	Enables[1]/Disables[0] using NONDEFAULT fclk frequencies Reset Source: mod_g_arstn

Table 14-10929. UART_MDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DISABLE_CIR_RX_DEMOD	R/W	0h	Disables[1]/Enables[0] CIR RX demodulation 0 `Enables CIR RX demodulation` 1 `Disables CIR RX demodulation`

14.7.2.4.2.55 UART_TX_DMA_THRESHOLD Register

14.7.2.4.2.55.1 UART_TX_DMA_THRESHOLD Register (Offset = 84h) [reset = 0h]

Use to manually set the TX DMA threshold level. MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size). If not, 64-tx_trigger_level will be used w/o modifying the value of this register.

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Table 14-10930. Instance Table

Instance Name	Physical Address
UART0	0280 0084h
UART1	0281 0084h
UART2	0282 0084h
UART3	0283 0084h
UART4	0284 0084h
UART5	0285 0084h
UART6	0286 0084h
WKUP_UART0	2B30 0084h

Figure 14-5402. UART_TX_DMA_THRESHOLD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TX_DMA_THRESHOLD</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-10931. UART_TX_DMA_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	RESERVED
7:6	RESERVED	R	0h	Reserved
5:0	TX_DMA_THRESHOLD	R/W	0h	Use to manually set the TX DMA threshold level. Reset Source: mod_g_arstn

14.7.2.4.2.56 UART_MDR4 Register

14.7.2.4.2.56.1 UART_MDR4 Register (Offset = 88h) [reset = 0h]

Mode definition register 4

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Table 14-10932. Instance Table

Instance Name	Physical Address
UART0	0280 0088h
UART1	0281 0088h
UART2	0282 0088h
UART3	0283 0088h
UART4	0284 0088h
UART5	0285 0088h
UART6	0286 0088h
WKUP_UART0	2B30 0088h

Figure 14-5403. UART_MDR4 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	MODE9	FREQ_SEL_H			MODE		
R	R/W	R/W			R/W		
0h	0h	0h			0h		

Table 14-10933. UART_MDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	RESERVED	R	0h	
6	MODE9	R/W	0h	9-bit character length. When '1', overrides character length setting in LCR Reset Source: mod_g_arstn
5:3	FREQ_SEL_H	R/W	0h	Upper 3 bits of FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode Reset Source: mod_g_arstn

Table 14-10933. UART_MDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	MODE	R/W	0h	New modes [when set, overrides MDR1 modes] 0 disabled (no override) 1 reserved 2 Synchronous mode with external clock 3 Synchronous mode with generated clock 4 ISO 7816 mode T=0 5 ISO 7816 mode T=1 6 reserved 7 reserved

14.7.2.4.2.57 UART_EFR2 Register

14.7.2.4.2.57.1 UART_EFR2 Register (Offset = 8Ch) [reset = 0h]

Enhanced Features Register 2

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Table 14-10934. Instance Table

Instance Name	Physical Address
UART0	0280 008Ch
UART1	0281 008Ch
UART2	0282 008Ch
UART3	0283 008Ch
UART4	0284 008Ch
UART5	0285 008Ch
UART6	0286 008Ch
WKUP_UART0	2B30 008Ch

Figure 14-5404. UART_EFR2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
BROADCAST	TIMEOUT_BEHAVE	C8	C4	C2	MULTIDROP	RHR_OVERRUN	ENDIAN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10935. UART_EFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	BROADCAST	R/W	0h	Enables broadcast address matching in multi-drop address match mode Reset Source: mod_g_arstn
6	TIMEOUT_BEHAVE	R/W	0h	Specifies how timeout is measured 0 `timeout after at least one character has been received` 1 `periodic timeout even when no character has been received`
5	C8	R/W	0h	Value for ISO 7816 C8 pin for software control Reset Source: mod_g_arstn
4	C4	R/W	0h	Value for ISO 7816 C4 pin for software control Reset Source: mod_g_arstn

Table 14-10935. UART_EFR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	C2	R/W	0h	Value for ISO 7816 reset pin [software controllable] Reset Source: mod_g_arstn
2	MULTIDROP	R/W	0h	Enables parity Multi-drop mode [overrides LCR[5..3]] when '1' Reset Source: mod_g_arstn
1	RHR_OVERRUN	R/W	0h	RHR Overrun behaviour when buffer full 0 `data in RHR is not overwritten (standard)` 1 `data in RHR is overwritten when buffer full (and FIFO disabled)`
0	ENDIAN	R/W	0h	Endianness 0 `Little Endian (LSB First)` 1 `Big Endian (MSB First)`

14.7.2.4.2.58 UART_ECR Register

14.7.2.4.2.58.1 UART_ECR Register (Offset = 90h) [reset = 18h]

Enhanced Control register

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Table 14-10936. Instance Table

Instance Name	Physical Address
UART0	0280 0090h
UART1	0281 0090h
UART2	0282 0090h
UART3	0283 0090h
UART4	0284 0090h
UART5	0285 0090h
UART6	0286 0090h
WKUP_UART0	2B30 0090h

Figure 14-5405. UART_ECR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLEAR_TX_PE	TX_EN	RX_EN	TX_RST	RX_RST	A_MULTIDROP
R		W	R/W	R/W	W	W	W
0h		0h	1h	1h	0h	0h	0h

Table 14-10937. UART_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:6	RESERVED	R	0h	
5	CLEAR_TX_PE	W	0h	Write 1 to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only] Reset Source: mod_g_arstn

4	TX_EN	R/W	1h	Enables/Disables the transmitter
				`0 Transmitter is shut down`
				`1 Transmitter is working`

3	RX_EN	R/W	1h	Enables/Disables the receiver
				`0 Receiver is shut down`
				`1 Receiver is operating`

2	TX_RST	W	0h	Writing '1' resets the transmitter Reset Source: mod_g_arstn

Table 14-10937. UART_ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RX_RST	W	0h	Writing '1' resets the receiver Reset Source: mod_g_arstn
0	A_MULTIDROP	W	0h	In multi-drop mode, when written with the value '1' causes the next byte written into THR to be transmitted with the parity bit set, signaling an address Reset Source: mod_g_arstn

14.7.2.4.2.59 UART_TIMEGUARD Register

14.7.2.4.2.59.1 UART_TIMEGUARD Register (Offset = 94h) [reset = 0h]

Timeguard

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Table 14-10938. Instance Table

Instance Name	Physical Address
UART0	0280 0094h
UART1	0281 0094h
UART2	0282 0094h
UART3	0283 0094h
UART4	0284 0094h
UART5	0285 0094h
UART6	0286 0094h
WKUP_UART0	2B30 0094h

Figure 14-5406. UART_TIMEGUARD Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TIMEGUARD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10939. UART_TIMEGUARD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEGUARD	R/W	0h	Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when comunicating with slower devices Reset Source: mod_g_arstn

14.7.2.4.2.60 UART_TIMEOUTL Register

14.7.2.4.2.60.1 UART_TIMEOUTL Register (Offset = 98h) [reset = 0h]

Timeout lower byte

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Table 14-10940. Instance Table

Instance Name	Physical Address
UART0	0280 0098h
UART1	0281 0098h
UART2	0282 0098h
UART3	0283 0098h
UART4	0284 0098h
UART5	0285 0098h
UART6	0286 0098h
WKUP_UART0	2B30 0098h

Figure 14-5407. UART_TIMEOUTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_L							
R/W							
0h							

Table 14-10941. UART_TIMEOUTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEOUT_L	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Lower byte of the 16 bit value] Reset Source: mod_g_arstn

14.7.2.4.2.61 UART_TIMEOUTH Register

14.7.2.4.2.61.1 UART_TIMEOUTH Register (Offset = 9Ch) [reset = 0h]

Timeout higher byte

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Table 14-10942. Instance Table

Instance Name	Physical Address
UART0	0280 009Ch
UART1	0281 009Ch
UART2	0282 009Ch
UART3	0283 009Ch
UART4	0284 009Ch
UART5	0285 009Ch
UART6	0286 009Ch
WKUP_UART0	2B30 009Ch

Figure 14-5408. UART_TIMEOUTH Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_H							
R/W							
0h							

Table 14-10943. UART_TIMEOUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEOUT_H	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Higher byte of the 16 bit value] Reset Source: mod_g_arstn

14.7.2.4.2.62 UART_SCCR Register

14.7.2.4.2.62.1 UART_SCCR Register (Offset = A0h) [reset = 7h]

Smartcard (ISO7816) mode Control Register

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Table 14-10944. Instance Table

Instance Name	Physical Address
UART0	0280 00A0h
UART1	0281 00A0h
UART2	0282 00A0h
UART3	0283 00A0h
UART4	0284 00A0h
UART5	0285 00A0h
UART6	0286 00A0h
WKUP_UART0	2B30 00A0h

Figure 14-5409. UART_SCCR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
DSNACK	INACK	RESERVED			MAX_ITERATION		
R/W	R/W	R			R/W		
0h	0h	0h			7h		

Table 14-10945. UART_SCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	DSNACK	R/W	0h	Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error. The data will be loaded into the receiver FIFO and PE will be set when Reading it. Reset Source: mod_g_arstn
6	INACK	R/W	0h	Inhibit NACK when receiving, even if an error is received. The data will be loaded into the receiver FIFO and PE will be set when Reading it. Reset Source: mod_g_arstn
5:3	RESERVED	R	0h	

Table 14-10945. UART_SCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	MAX_ITERATION	R/W	7h	Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the USART transmitter will set parity error, stop and not continue until it is cleared. Reset Source: mod_g_arstn

14.7.2.4.2.63 UART_ERHR Register

14.7.2.4.2.63.1 UART_ERHR Register (Offset = A4h) [reset = 0h]

Extended Receive Holding Register

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Table 14-10946. Instance Table

Instance Name	Physical Address
UART0	0280 00A4h
UART1	0281 00A4h
UART2	0282 00A4h
UART3	0283 00A4h
UART4	0284 00A4h
UART5	0285 00A4h
UART6	0286 00A4h
WKUP_UART0	2B30 00A4h

Figure 14-5410. UART_ERHR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>ERHR</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ERHR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10947. UART_ERHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R	0h	
8:0	ERHR	R	0h	Extended Receive Holding Register - allows accessing the full 9bit RHR Reset Source: mod_g_arstn

14.7.2.4.2.64 UART_ETHR Register

14.7.2.4.2.64.1 UART_ETHR Register (Offset = A4h) [reset = 0h]

Extended Transmit Holding Register

Return to Summary Table

Table 14-10948. Instance Table

Instance Name	Physical Address
UART0	0280 00A4h
UART1	0281 00A4h
UART2	0282 00A4h
UART3	0283 00A4h
UART4	0284 00A4h
UART5	0285 00A4h
UART6	0286 00A4h
WKUP_UART0	2B30 00A4h

Figure 14-5411. UART_ETHR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>ETHR</td></tr>
<tr><td colspan="7">R</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ETHR</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10949. UART_ETHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R	0h	
8:0	ETHR	W	0h	Extended Transmit Holding Register - allows Writing the full 9bit RHR Reset Source: mod_g_arstn

14.7.2.4.2.65 UART_MAR Register

14.7.2.4.2.65.1 UART_MAR Register (Offset = A8h) [reset = 0h]

Multidrop Address Register

Return to Summary Table

Table 14-10950. Instance Table

Instance Name	Physical Address
UART0	0280 00A8h
UART1	0281 00A8h
UART2	0282 00A8h
UART3	0283 00A8h
UART4	0284 00A8h
UART5	0285 00A8h
UART6	0286 00A8h
WKUP_UART0	2B30 00A8h

Figure 14-5412. UART_MAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 14-10951. UART_MAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ADDRESS	R/W	0h	Multidrop match address value Reset Source: mod_g_arstn

14.7.2.4.2.66 UART_MMR Register

14.7.2.4.2.66.1 UART_MMR Register (Offset = ACh) [reset = 0h]

Multidrop Mask Register

Return to Summary Table

Table 14-10952. Instance Table

Instance Name	Physical Address
UART0	0280 00ACh
UART1	0281 00ACh
UART2	0282 00ACh
UART3	0283 00ACh
UART4	0284 00ACh
UART5	0285 00ACh
UART6	0286 00ACh
WKUP_UART0	2B30 00ACh

Figure 14-5413. UART_MMR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MASK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-10953. UART_MMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MASK	R/W	0h	Address match masking value ? Writing a 0 to a bit means that the corresponding address bit will be ignored in matching Reset Source: mod_g_arstn

14.7.2.4.2.67 UART_MBR Register

14.7.2.4.2.67.1 UART_MBR Register (Offset = B0h) [reset = 0h]

Multidrop Broadcast Address Register

Return to Summary Table

Table 14-10954. Instance Table

Instance Name	Physical Address
UART0	0280 00B0h
UART1	0281 00B0h
UART2	0282 00B0h
UART3	0283 00B0h
UART4	0284 00B0h
UART5	0285 00B0h
UART6	0286 00B0h
WKUP_UART0	2B30 00B0h

Figure 14-5414. UART_MBR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BROADCAST_ADDRESS							
R/W							
0h							

Table 14-10955. UART_MBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BROADCAST_ADDRESS	R/W	0h	Broadcast address for address matching Reset Source: mod_g_arstn

14.7.3 High-Speed Serial Interfaces Registers

14.7.3.1 CPSW

CPSW

14.7.3.1.1 CPSW Summaries

CPSW Summaries

Table 14-10956. CPSW3_ECC Registers, Base Address=0070 4000h, Length=1024

Offset	Length	Register Name	CPSW0 Physical Address
0h	32	CPSW3_ECC_ECC_REV	0070 4000h + formula
8h	32	CPSW3_ECC_ECC_VECTOR	0070 4008h + formula
Ch	32	CPSW3_ECC_ECC_STAT	0070 400Ch + formula
10h	32	CPSW3_ECC_ECC_RESERVED_SVBUS_J	0070 4010h + formula
3Ch	32	CPSW3_ECC_ECC_SEC_EOI_REG	0070 403Ch + formula
40h	32	CPSW3_ECC_ECC_SEC_STATUS_REG0	0070 4040h + formula
80h	32	CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0	0070 4080h + formula
C0h	32	CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0	0070 40C0h + formula
13Ch	32	CPSW3_ECC_ECC_DED_EOI_REG	0070 413Ch + formula
140h	32	CPSW3_ECC_ECC_DED_STATUS_REG0	0070 4140h + formula
180h	32	CPSW3_ECC_ECC_DED_ENABLE_SET_REG0	0070 4180h + formula
1C0h	32	CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0	0070 41C0h + formula
200h	32	CPSW3_ECC_ECC_AGGR_ENABLE_SET	0070 4200h + formula
204h	32	CPSW3_ECC_ECC_AGGR_ENABLE_CLR	0070 4204h + formula
208h	32	CPSW3_ECC_ECC_AGGR_STATUS_SET	0070 4208h + formula
20Ch	32	CPSW3_ECC_ECC_AGGR_STATUS_CLR	0070 420Ch + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152

Offset	Length	Register Name	CPSW0 Physical Address
0h	32	CPSW3_CPSW_NUSS_IDVER_REG	0800 0000h
4h	32	CPSW3_SYNCE_COUNT_REG	0800 0004h
8h	32	CPSW3_SYNCE_MUX_REG	0800 0008h
Ch	32	CPSW3_CONTROL_REG	0800 000Ch
1Ch	32	CPSW3_SUBSSYSTEM_STATUS_REG	0800 001Ch
20h	32	CPSW3_SUBSYSTEM_CONFIG_REG	0800 0020h
30h	32	CPSW3_RGMII1_STATUS_REG	0800 0030h
34h	32	CPSW3_RGMII2_STATUS_REG	0800 0034h
F00h	32	CPSW3_MDIO_MDIO_VERSION_REG	0800 0F00h + formula
F04h	32	CPSW3_MDIO_CONTROL_REG	0800 0F04h + formula
F08h	32	CPSW3_MDIO_ALIVE_REG	0800 0F08h + formula
F0Ch	32	CPSW3_MDIO_LINK_REG	0800 0F0Ch + formula
F10h	32	CPSW3_MDIO_LINK_INT_RAW_REG	0800 0F10h + formula
F14h	32	CPSW3_MDIO_LINK_INT_MASKED_REG	0800 0F14h + formula
F18h	32	CPSW3_MDIO_LINK_INT_MASK_SET_REG	0800 0F18h + formula
F1Ch	32	CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG	0800 0F1Ch + formula
F20h	32	CPSW3_MDIO_USER_INT_RAW_REG	0800 0F20h + formula
F24h	32	CPSW3_MDIO_USER_INT_MASKED_REG	0800 0F24h + formula
F28h	32	CPSW3_MDIO_USER_INT_MASK_SET_REG	0800 0F28h + formula
F2Ch	32	CPSW3_MDIO_USER_INT_MASK_CLEAR_REG	0800 0F2Ch + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
F30h	32	CPSW3_MDIO_MANUAL_IF_REG	0800 0F30h + formula
F34h	32	CPSW3_MDIO_POLL_REG	0800 0F34h + formula
F38h	32	CPSW3_MDIO_POLL_EN_REG	0800 0F38h + formula
F3Ch	32	CPSW3_MDIO_CLAUS45_REG	0800 0F3Ch + formula
F40h	32	CPSW3_MDIO_USER_ADDR0_REG	0800 0F40h + formula
F44h	32	CPSW3_MDIO_USER_ADDR1_REG	0800 0F44h + formula
1000h	32	CPSW3_INTD_REVISION	0800 1000h + formula
1010h	32	CPSW3_INTD_EOI_REG	0800 1010h + formula
1014h	32	CPSW3_INTD_INTR_VECTOR_REG	0800 1014h + formula
1100h	32	CPSW3_INTD_ENABLE_REG_OUT_PULSE_0	0800 1100h + formula
1300h	32	CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0	0800 1300h + formula
1500h	32	CPSW3_INTD_STATUS_REG_OUT_PULSE_0	0800 1500h + formula
1A80h	32	CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE	0800 1A80h + formula
20000h	32	CPSW3_CPSW_NU_CPSW_ID_VER_REG	0802 0000h + formula
20004h	32	CPSW3_CPSW_NU_CONTROL_REG	0802 0004h + formula
20010h	32	CPSW3_CPSW_NU_EM_CONTROL_REG	0802 0010h + formula
20014h	32	CPSW3_CPSW_NU_STAT_PORT_EN_REG	0802 0014h + formula
20018h	32	CPSW3_CPSW_NU_PTYPE_REG	0802 0018h + formula
2001Ch	32	CPSW3_CPSW_NU_SOFT_IDLE_REG	0802 001Ch + formula
20020h	32	CPSW3_CPSW_NU_THRU_RATE_REG	0802 0020h + formula
20024h	32	CPSW3_CPSW_NU_GAP_THRESH_REG	0802 0024h + formula
2002Ch	32	CPSW3_CPSW_NU_EEE_PRESCALE_REG	0802 002Ch + formula
20030h	32	CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG	0802 0030h + formula
20034h	32	CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG	0802 0034h + formula
20038h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG	0802 0038h + formula
2003Ch	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG	0802 003Ch + formula
20040h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG	0802 0040h + formula
20044h	32	CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG	0802 0044h + formula
20050h	32	CPSW3_CPSW_NU_VLAN_LTYPE_REG	0802 0050h + formula
20054h	32	CPSW3_CPSW_NU_EST_TS_DOMAIN_REG	0802 0054h + formula
20058h	32	CPSW3_CPSW_NU_CUT_THRESHOLD_REG	0802 0058h + formula
2005Ch	32	CPSW3_CPSW_NU_FREQUENCY_REG	0802 005Ch + formula
20060h	32	CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG	0802 0060h + formula
20100h	32	CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG	0802 0100h + formula
20104h	32	CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG	0802 0104h + formula
20108h	32	CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG	0802 0108h + formula
2010Ch	32	CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG	0802 010Ch + formula
20110h	32	CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG	0802 0110h + formula
20114h	32	CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG	0802 0114h + formula
20118h	32	CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG	0802 0118h + formula
2011Ch	32	CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG	0802 011Ch + formula
F80h	32	CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_J	0800 0F80h + formula
F84h	32	CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_J	0800 0F84h + formula
21004h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG	0802 1004h + formula
21008h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG	0802 1008h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
21010h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG	0802 1010h + formula
21014h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG	0802 1014h + formula
21018h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG	0802 1018h + formula
2101Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG	0802 101Ch + formula
21020h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG	0802 1020h + formula
21024h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG	0802 1024h + formula
21028h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG	0802 1028h + formula
21030h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG	0802 1030h + formula
21034h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG	0802 1034h + formula
21038h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG	0802 1038h + formula
21050h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG	0802 1050h + formula
21080h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_MAX_BLKS_REG	0802 1080h + formula
21120h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_J	0802 1120h + formula
21140h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_J	0802 1140h + formula
21160h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_J	0802 1160h + formula
21180h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG	0802 1180h + formula
21184h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG	0802 1184h + formula
21188h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG	0802 1188h + formula
2118Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG	0802 118Ch + formula
21190h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG	0802 1190h + formula
21194h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG	0802 1194h + formula
21198h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG	0802 1198h + formula
2119Ch	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG	0802 119Ch + formula
21300h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG	0802 1300h + formula
21304h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG	0802 1304h + formula
21320h	32	CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG	0802 1320h + formula
22000h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG	0802 2000h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
22004h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG	0802 2004h + formula
22008h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG	0802 2008h + formula
22010h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG	0802 2010h + formula
22014h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG	0802 2014h + formula
22018h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG	0802 2018h + formula
2201Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG	0802 201Ch + formula
22020h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG	0802 2020h + formula
22024h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG	0802 2024h + formula
22028h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG	0802 2028h + formula
22030h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG	0802 2030h + formula
22034h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG	0802 2034h + formula
22038h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG	0802 2038h + formula
22040h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG	0802 2040h + formula
22044h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG	0802 2044h + formula
22048h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG	0802 2048h + formula
22050h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG	0802 2050h + formula
22060h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG	0802 2060h + formula
22120h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_J	0802 2120h + formula
22140h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_J	0802 2140h + formula
22160h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_J	0802 2160h + formula
22180h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG	0802 2180h + formula
22184h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG	0802 2184h + formula
22188h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG	0802 2188h + formula
2218Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG	0802 218Ch + formula
22190h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG	0802 2190h + formula
22194h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG	0802 2194h + formula
22198h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG	0802 2198h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
2219Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG	0802 219Ch + formula
22300h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG	0802 2300h + formula
22304h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG	0802 2304h + formula
22308h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG	0802 2308h + formula
2230Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG	0802 230Ch + formula
22310h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG	0802 2310h + formula
22314h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG	0802 2314h + formula
22318h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG	0802 2318h + formula
2231Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG	0802 231Ch + formula
22320h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG	0802 2320h + formula
22330h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG	0802 2330h + formula
22334h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG	0802 2334h + formula
22338h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG	0802 2338h + formula
2233Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG	0802 233Ch + formula
22340h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG	0802 2340h + formula
22350h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_J	0802 2350h + formula
22370h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG	0802 2370h + formula
22380h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_J	0802 2380h + formula
223A0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG	0802 23A0h + formula
223A4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG	0802 23A4h + formula
223A8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG	0802 23A8h + formula
223ACh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG	0802 23ACh + formula
223B0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG	0802 23B0h + formula
223B4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG	0802 23B4h + formula
223B8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG	0802 23B8h + formula
223BCh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG	0802 23BCh + formula
223C0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG	0802 23C0h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
223C4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG	0802 23C4h + formula
23000h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG	0802 3000h + formula
23004h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG	0802 3004h + formula
23008h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG	0802 3008h + formula
23010h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG	0802 3010h + formula
23014h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG	0802 3014h + formula
23018h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG	0802 3018h + formula
2301Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG	0802 301Ch + formula
23020h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG	0802 3020h + formula
23024h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG	0802 3024h + formula
23028h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG	0802 3028h + formula
23030h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG	0802 3030h + formula
23034h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG	0802 3034h + formula
23038h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG	0802 3038h + formula
23040h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG	0802 3040h + formula
23044h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG	0802 3044h + formula
23048h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG	0802 3048h + formula
23050h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG	0802 3050h + formula
23060h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG	0802 3060h + formula
23120h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_J	0802 3120h + formula
23140h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_J	0802 3140h + formula
23160h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_J	0802 3160h + formula
23180h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG	0802 3180h + formula
23184h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG	0802 3184h + formula
23188h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG	0802 3188h + formula
2318Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG	0802 318Ch + formula
23190h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG	0802 3190h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
23194h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG	0802 3194h + formula
23198h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG	0802 3198h + formula
2319Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG	0802 319Ch + formula
23300h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG	0802 3300h + formula
23304h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG	0802 3304h + formula
23308h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG	0802 3308h + formula
2330Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG	0802 330Ch + formula
23310h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG	0802 3310h + formula
23314h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG	0802 3314h + formula
23318h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG	0802 3318h + formula
2331Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG	0802 331Ch + formula
23320h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG	0802 3320h + formula
23330h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG	0802 3330h + formula
23334h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG	0802 3334h + formula
23338h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG	0802 3338h + formula
2333Ch	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG	0802 333Ch + formula
23340h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG	0802 3340h + formula
23350h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_J	0802 3350h + formula
23370h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG	0802 3370h + formula
23380h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_J	0802 3380h + formula
233A0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG	0802 33A0h + formula
233A4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG	0802 33A4h + formula
233A8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG	0802 33A8h + formula
233ACh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG	0802 33ACh + formula
233B0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG	0802 33B0h + formula
233B4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG	0802 33B4h + formula
233B8h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG	0802 33B8h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
233BCh	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG	0802 33BCh + formula
233C0h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG	0802 33C0h + formula
233C4h	32	CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG	0802 33C4h + formula
32000h	32	CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_J	0803 2000h + formula
3A000h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_J	0803 A000h + formula
3A004h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_J	0803 A004h + formula
3A008h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_J	0803 A008h + formula
3A00Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_J	0803 A00Ch + formula
3A010h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_J	0803 A010h + formula
3A014h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_J	0803 A014h + formula
3A018h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_J	0803 A018h + formula
3A01Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_J	0803 A01Ch + formula
3A020h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_J	0803 A020h + formula
3A024h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_J	0803 A024h + formula
3A028h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_J	0803 A028h + formula
3A02Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_J	0803 A02Ch + formula
3A030h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_J	0803 A030h + formula
3A034h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_J	0803 A034h + formula
3A038h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_J	0803 A038h + formula
3A03Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_J	0803 A03Ch + formula
3A040h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_J	0803 A040h + formula
3A044h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_J	0803 A044h + formula
3A048h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_J	0803 A048h + formula
3A04Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_J	0803 A04Ch + formula
3A050h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_J	0803 A050h + formula
3A054h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_J	0803 A054h + formula
3A058h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_J	0803 A058h + formula
3A05Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_J	0803 A05Ch + formula
3A060h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_J	0803 A060h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
3A064h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_J	0803 A064h + formula
3A068h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_J	0803 A068h + formula
3A06Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_J	0803 A06Ch + formula
3A070h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_J	0803 A070h + formula
3A074h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_J	0803 A074h + formula
3A078h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_J	0803 A078h + formula
3A07Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_J	0803 A07Ch + formula
3A080h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_J	0803 A080h + formula
3A084h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_J	0803 A084h + formula
3A088h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_J	0803 A088h + formula
3A08Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_J	0803 A08Ch + formula
3A090h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_J	0803 A090h + formula
3A094h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_J	0803 A094h + formula
3A098h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_J	0803 A098h + formula
3A09Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_J	0803 A09Ch + formula
3A0A0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_J	0803 A0A0h + formula
3A0A4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_J	0803 A0A4h + formula
3A0A8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_J	0803 A0A8h + formula
3A0ACh	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_J	0803 A0ACh + formula
3A0B0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_J	0803 A0B0h + formula
3A0B4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_J	0803 A0B4h + formula
3A0B8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_J	0803 A0B8h + formula
3A0BCh	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_J	0803 A0BCh + formula
3A0C0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_J	0803 A0C0h + formula
3A0C4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_J	0803 A0C4h + formula
3A0C8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_J	0803 A0C8h + formula
3A0CCh	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_J	0803 A0CCh + formula
3A0D0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_J	0803 A0D0h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
3A0D4h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_J	0803 A0D4h + formula
3A0D8h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_J	0803 A0D8h + formula
3A0DCh	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_J	0803 A0DCh + formula
3A140h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_J	0803 A140h + formula
3A144h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_J	0803 A144h + formula
3A148h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_J	0803 A148h + formula
3A14Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_J	0803 A14Ch + formula
3A150h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_J	0803 A150h + formula
3A154h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_J	0803 A154h + formula
3A17Ch	32	CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_J	0803 A17Ch + formula
3A180h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_J_K	0803 A180h + formula
3A1A0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_J_K	0803 A1A0h + formula
3A1C0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_J_K	0803 A1C0h + formula
3A1E0h	32	CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_K	0803 A1E0h + formula
3D000h	32	CPSW3_CPSW_NU_CPTS_IDVER_REG	0803 D000h + formula
3D004h	32	CPSW3_CPSW_NU_CPTS_CONTROL_REG	0803 D004h + formula
3D008h	32	CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG	0803 D008h + formula
3D00Ch	32	CPSW3_CPSW_NU_CPTS_TS_PUSH_REG	0803 D00Ch + formula
3D010h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG	0803 D010h + formula
3D014h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG	0803 D014h + formula
3D018h	32	CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG	0803 D018h + formula
3D01Ch	32	CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG	0803 D01Ch + formula
3D020h	32	CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG	0803 D020h + formula
3D024h	32	CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG	0803 D024h + formula
3D028h	32	CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG	0803 D028h + formula
3D02Ch	32	CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG	0803 D02Ch + formula
3D030h	32	CPSW3_CPSW_NU_CPTS_EVENT_POP_REG	0803 D030h + formula
3D034h	32	CPSW3_CPSW_NU_CPTS_EVENT_0_REG	0803 D034h + formula
3D038h	32	CPSW3_CPSW_NU_CPTS_EVENT_1_REG	0803 D038h + formula
3D03Ch	32	CPSW3_CPSW_NU_CPTS_EVENT_2_REG	0803 D03Ch + formula
3D040h	32	CPSW3_CPSW_NU_CPTS_EVENT_3_REG	0803 D040h + formula
3D044h	32	CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG	0803 D044h + formula
3D048h	32	CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG	0803 D048h + formula
3D04Ch	32	CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG	0803 D04Ch + formula
3D050h	32	CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG	0803 D050h + formula
3D054h	32	CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG	0803 D054h + formula
3D058h	32	CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG	0803 D058h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
3D0D0h	32	CPSW3_CPSW_NU_CPTS_TS_CONFIG	0803 D0D0h + formula
3E000h	32	CPSW3_CPSW_NU_ALE_MOD_VER	0803 E000h + formula
3E004h	32	CPSW3_CPSW_NU_ALE_ALE_STATUS	0803 E004h + formula
3E008h	32	CPSW3_CPSW_NU_ALE_ALE_CONTROL	0803 E008h + formula
3E00Ch	32	CPSW3_CPSW_NU_ALE_ALE_CTRL2	0803 E00Ch + formula
3E010h	32	CPSW3_CPSW_NU_ALE_ALE_PRESCALE	0803 E010h + formula
3E014h	32	CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL	0803 E014h + formula
3E01Ch	32	CPSW3_CPSW_NU_ALE_ALE_NXT_HDR	0803 E01Ch + formula
3E020h	32	CPSW3_CPSW_NU_ALE_ALE_TBLCTL	0803 E020h + formula
3E034h	32	CPSW3_CPSW_NU_ALE_ALE_TBLW2	0803 E034h + formula
3E038h	32	CPSW3_CPSW_NU_ALE_ALE_TBLW1	0803 E038h + formula
3E03Ch	32	CPSW3_CPSW_NU_ALE_ALE_TBLW0	0803 E03Ch + formula
3E040h	32	CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_J	0803 E040h + formula
3E090h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER	0803 E090h + formula
3E094h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST	0803 E094h + formula
3E098h	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST	0803 E098h + formula
3E09Ch	32	CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG	0803 E09Ch + formula
3E0B4h	32	CPSW3_CPSW_NU_ALE_ALE_FAST_LUT	0803 E0B4h + formula
3E0B8h	32	CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG	0803 E0B8h + formula
3E0BCh	32	CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL	0803 E0BCh + formula
3E0FCh	32	CPSW3_CPSW_NU_ALE_EGRESSOP	0803 E0FCh + formula
3E100h	32	CPSW3_CPSW_NU_ALE_POLICECFG0	0803 E100h + formula
3E104h	32	CPSW3_CPSW_NU_ALE_POLICECFG1	0803 E104h + formula
3E108h	32	CPSW3_CPSW_NU_ALE_POLICECFG2	0803 E108h + formula
3E10Ch	32	CPSW3_CPSW_NU_ALE_POLICECFG3	0803 E10Ch + formula
3E110h	32	CPSW3_CPSW_NU_ALE_POLICECFG4	0803 E110h + formula
3E118h	32	CPSW3_CPSW_NU_ALE_POLICECFG6	0803 E118h + formula
3E11Ch	32	CPSW3_CPSW_NU_ALE_POLICECFG7	0803 E11Ch + formula
3E120h	32	CPSW3_CPSW_NU_ALE_POLICETBLCTL	0803 E120h + formula
3E124h	32	CPSW3_CPSW_NU_ALE_POLICECONTROL	0803 E124h + formula
3E128h	32	CPSW3_CPSW_NU_ALE_POLICETESTCTL	0803 E128h + formula
3E12Ch	32	CPSW3_CPSW_NU_ALE_POLICEHSTAT	0803 E12Ch + formula
3E134h	32	CPSW3_CPSW_NU_ALE_THREADMAPDEF	0803 E134h + formula
3E138h	32	CPSW3_CPSW_NU_ALE_THREADMAPCTL	0803 E138h + formula
3E13Ch	32	CPSW3_CPSW_NU_ALE_THREADMAPVAL	0803 E13Ch + formula
3D0E0h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_J	0803 D0E0h + formula
3D0E4h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_J	0803 D0E4h + formula
3D0E8h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_J	0803 D0E8h + formula
3D0ECh	32	CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_J	0803 D0ECh + formula
3D0F0h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_J	0803 D0F0h + formula
3D0F4h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_J	0803 D0F4h + formula
3D0F8h	32	CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_J	0803 D0F8h + formula

Table 14-10957. CPSW3 Registers, Base Address=0800 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
3D200h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_J	0803 D200h + formula
3D204h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_J	0803 D204h + formula
3D208h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_J	0803 D208h + formula
3D20Ch	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_J	0803 D20Ch + formula
3D210h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_J	0803 D210h + formula
3D214h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_J	0803 D214h + formula
3D218h	32	CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_J	0803 D218h + formula

14.7.3.1.2 CPSW Registers

CPSW Registers

14.7.3.1.2.1 CPSW3_ECC_ECC_REV Register

14.7.3.1.2.1.1 CPSW3_ECC_ECC_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-10958. Instance Table

Instance Name	Physical Address
CPSW0	0070 4000h + formula

Figure 14-5415. CPSW3_ECC_ECC_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-10959. CPSW3_ECC_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.3.1.2.2 CPSW3_ECC_ECC_VECTOR Register

14.7.3.1.2.2.1 CPSW3_ECC_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-10960. Instance Table

Instance Name	Physical Address
CPSW0	0070 4008h + formula

Figure 14-5416. CPSW3_ECC_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-10961. CPSW3_ECC_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.3.1.2.3 CPSW3_ECC_ECC_STAT Register

14.7.3.1.2.3.1 CPSW3_ECC_ECC_STAT Register (Offset = Ch) [reset = 8h]

Misc Status

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Table 14-10962. Instance Table

Instance Name	Physical Address
CPSW0	0070 400Ch + formula

Figure 14-5417. CPSW3_ECC_ECC_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
</table>

Table 14-10963. CPSW3_ECC_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	8h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.3.1.2.4 CPSW3_ECC_ECC_RESERVED_SVBUS_J Register

14.7.3.1.2.4.1 CPSW3_ECC_ECC_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-10964. Instance Table

Instance Name	Physical Address
CPSW0	0070 4010h + formula

Figure 14-5418. CPSW3_ECC_ECC_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-10965. CPSW3_ECC_ECC_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.3.1.2.5 CPSW3_ECC_ECC_SEC_EOI_REG Register

14.7.3.1.2.5.1 CPSW3_ECC_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-10966. Instance Table

Instance Name	Physical Address
CPSW0	0070 403Ch + formula

Figure 14-5419. CPSW3_ECC_ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-10967. CPSW3_ECC_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.3.1.2.6 CPSW3_ECC_ECC_SEC_STATUS_REG0 Register

14.7.3.1.2.6.1 CPSW3_ECC_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-10968. Instance Table

Instance Name	Physical Address
CPSW0	0070 4040h + formula

Figure 14-5420. CPSW3_ECC_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10969. CPSW3_ECC_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend

Table 14-10969. CPSW3_ECC_ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.7.3.1.2.7 CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register

14.7.3.1.2.7.1 CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-10970. Instance Table

Instance Name	Physical Address
CPSW0	0070 4080h + formula

Figure 14-5421. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10971. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend

Table 14-10971. CPSW3_ECC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.7.3.1.2.8 CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register

14.7.3.1.2.8.1 CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-10972. Instance Table

Instance Name	Physical Address
CPSW0	0070 40C0h + formula

Figure 14-5422. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10973. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend

Table 14-10973. CPSW3_ECC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.7.3.1.2.9 CPSW3_ECC_ECC_DED_EOI_REG Register

14.7.3.1.2.9.1 CPSW3_ECC_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-10974. Instance Table

Instance Name	Physical Address
CPSW0	0070 413Ch + formula

Figure 14-5423. CPSW3_ECC_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-10975. CPSW3_ECC_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.3.1.2.10 CPSW3_ECC_ECC_DED_STATUS_REG0 Register

14.7.3.1.2.10.1 CPSW3_ECC_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-10976. Instance Table

Instance Name	Physical Address
CPSW0	0070 4140h + formula

Figure 14-5424. CPSW3_ECC_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10977. CPSW3_ECC_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend

Table 14-10977. CPSW3_ECC_ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

14.7.3.1.2.11 CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register

14.7.3.1.2.11.1 CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-10978. Instance Table

Instance Name	Physical Address
CPSW0	0070 4180h + formula

Figure 14-5425. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10979. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend

Table 14-10979. CPSW3_ECC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

14.7.3.1.2.12 CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register

14.7.3.1.2.12.1 CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-10980. Instance Table

Instance Name	Physical Address
CPSW0	0070 41C0h + formula

Figure 14-5426. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-10981. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend

Table 14-10981. CPSW3_ECC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

14.7.3.1.2.13 CPSW3_ECC_ECC_AGGR_ENABLE_SET Register

14.7.3.1.2.13.1 CPSW3_ECC_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 14-10982. Instance Table

Instance Name	Physical Address
CPSW0	0070 4200h + formula

Figure 14-5427. CPSW3_ECC_ECC_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-10983. CPSW3_ECC_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.3.1.2.14 CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register

14.7.3.1.2.14.1 CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-10984. Instance Table

Instance Name	Physical Address
CPSW0	0070 4204h + formula

Figure 14-5428. CPSW3_ECC_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-10985. CPSW3_ECC_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.3.1.2.15 CPSW3_ECC_ECC_AGGR_STATUS_SET Register

14.7.3.1.2.15.1 CPSW3_ECC_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-10986. Instance Table

Instance Name	Physical Address
CPSW0	0070 4208h + formula

Figure 14-5429. CPSW3_ECC_ECC_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-10987. CPSW3_ECC_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.3.1.2.16 CPSW3_ECC_ECC_AGGR_STATUS_CLR Register

14.7.3.1.2.16.1 CPSW3_ECC_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-10988. Instance Table

Instance Name	Physical Address
CPSW0	0070 420Ch + formula

Figure 14-5430. CPSW3_ECC_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-10989. CPSW3_ECC_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.3.1.2.17 CPSW3_CPSW_NUSS_IDVER_REG Register

14.7.3.1.2.17.1 CPSW3_CPSW_NUSS_IDVER_REG Register (Offset = 0h) [reset = 6BA00103h]

ID Version Register

Return to Summary Table

Table 14-10990. Instance Table

Instance Name	Physical Address
CPSW0	0800 0000h

Figure 14-5431. CPSW3_CPSW_NUSS_IDVER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6BA0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IDENT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6BA0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJOR_VER</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MINOR_VER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
</table>

Table 14-10991. CPSW3_CPSW_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6BA0h	Identification value
15:11	RTL_VER	R	0h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	3h	Minor version value

14.7.3.1.2.18 CPSW3_SYNCE_COUNT_REG Register

14.7.3.1.2.18.1 CPSW3_SYNCE_COUNT_REG Register (Offset = 4h) [reset = 0h]

SyncE Count Register

Return to Summary Table

Table 14-10992. Instance Table

Instance Name	Physical Address
CPSW0	0800 0004h

Figure 14-5432. CPSW3_SYNCE_COUNT_REG Name Register

31	30	29	28	27	26	25	24
SYNCE_CNT							
R/W							
0h							
23	22	21	20	19	18	17	16
SYNCE_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
SYNCE_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNCE_CNT							
R/W							
0h							

Table 14-10993. CPSW3_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNCE_CNT	R/W	0h	Sync E Count Value

14.7.3.1.2.19 CPSW3_SYNCE_MUX_REG Register

14.7.3.1.2.19.1 CPSW3_SYNCE_MUX_REG Register (Offset = 8h) [reset = 0h]

SyncE Mux Register

Return to Summary Table

Table 14-10994. Instance Table

Instance Name	Physical Address
CPSW0	0800 0008h

Figure 14-5433. CPSW3_SYNCE_MUX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		SYNCE_SEL		SYNCE_PORT_SEL			
NONE		R/W		R/W			
0h		0h		0h			

Table 14-10995. CPSW3_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved

5:4	SYNCE_SEL	R/W	0h	Sync E Interface Select.
				`0h` `GMIIn_MRCLK_I input clock from selected port.`
				`1h` `RMII_MHZ_50_CLK (same for all ports).`
				`2h` `RGMIIn_RXC_I input clock from selected port.`
				`3h` `SERDESn_RXCLK from selected port.`

3:0	SYNCE_PORT_SEL	R/W	0h	Sync E Port Select This field selects the port that will be used for Synchronous Ethernet receive clock. The port interface is selected with synce_sel.
				`0h` `Port 1.`
				`1h` `Port 2.`
				`2h-Fh` `Reserved.`

14.7.3.1.2.20 CPSW3_CONTROL_REG Register

14.7.3.1.2.20.1 CPSW3_CONTROL_REG Register (Offset = Ch) [reset = 0h]

Control Register

Return to Summary Table

Table 14-10996. Instance Table

Instance Name	Physical Address
CPSW0	0800 000Ch

Figure 14-5434. CPSW3_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EEE_PHY_ONLY	EEE_EN
NONE						R/W	R/W
0h						0h	0h

Table 14-10997. CPSW3_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EEE_PHY_ONLY	R/W	0h	Energy Efficient Enable Phy Only Mode: 0h The low power indicate state includes gating off the CPPI_GCLK to the CPSW. 1h The low power indicate state does not gate the clock to the CPSW.
0	EEE_EN	R/W	0h	Energy Efficient Ethernet Enable: 0h EEE is disabled 1h EEE is enabled

14.7.3.1.2.21 CPSW3_SUBSSYSTEM_STATUS_REG Register

14.7.3.1.2.21.1 CPSW3_SUBSSYSTEM_STATUS_REG Register (Offset = 1Ch) [reset = 0h]

Subsystem Status Register

Return to Summary Table

Table 14-10998. Instance Table

Instance Name	Physical Address
CPSW0	0800 001Ch

Figure 14-5435. CPSW3_SUBSSYSTEM_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EEE_CLKSTOP_ACK
NONE							R
0h							0h

Table 14-10999. CPSW3_SUBSSYSTEM_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EEE_CLKSTOP_ACK	R	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

14.7.3.1.2.22 CPSW3_SUBSYSTEM_CONFIG_REG Register

14.7.3.1.2.22.1 CPSW3_SUBSYSTEM_CONFIG_REG Register (Offset = 20h) [reset = 30203h]

Subsystem Configuration Register

Return to Summary Table

Table 14-11000. Instance Table

Instance Name	Physical Address
CPSW0	0800 0020h

Figure 14-5436. CPSW3_SUBSYSTEM_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED				XGMII			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
XGMII				QSGMII	SGMII	RGMII	RMII
R				R	R	R	R
0h				0h	0h	1h	1h
15	14	13	12	11	10	9	8
RESERVED			NUM_GENF				
NONE			R				
0h			2h				
7	6	5	4	3	2	1	0
NUM_PORTS							
R							
3h							

Table 14-11001. CPSW3_SUBSYSTEM_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:20	XGMII	R	0h	The Number of XGMII Ports included in the CPSW_NUSS
19	QSGMII	R	0h	QSGMII is included in the CPSW_NUSS
18	SGMII	R	0h	SGMII is included in the CPSW_NUSS
17	RGMII	R	1h	RGMII is included in the CPSW_NUSS
16	RMII	R	1h	RMII is included in the CPSW_NUSS
15:13	RESERVED	NONE	0h	Reserved
12:8	NUM_GENF	R	2h	The number of CPTS GENF outputs
7:0	NUM_PORTS	R	3h	The total number of ports including the host port 0

14.7.3.1.2.23 CPSW3_RGMII1_STATUS_REG Register

14.7.3.1.2.23.1 CPSW3_RGMII1_STATUS_REG Register (Offset = 30h) [reset = 0h]

RGMII1 Status Register

Return to Summary Table

Table 14-11002. Instance Table

Instance Name	Physical Address
CPSW0	0800 0030h

Figure 14-5437. CPSW3_RGMII1_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
NONE				R	R		R
0h				0h	0h		0h

Table 14-11003. CPSW3_RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

3	FULLDUPLEX	R	0h	RGMII Port 1 full duplex:
				`0h Half-duplex`
				`1h Full-duplex`

2:1	SPEED	R	0h	RGMII Port 1 speed:
				`0h 10Mbps`
				`1h 100Mbps`
				`2h 1000Mbps`
				`3h Reserved`

0	LINK	R	0h	RGMII Port 1 link indicator:
				`0h Link is down,`
				`1h Link is up`

14.7.3.1.2.24 CPSW3_RGMII2_STATUS_REG Register

14.7.3.1.2.24.1 CPSW3_RGMII2_STATUS_REG Register (Offset = 34h) [reset = 0h]

RGMII2 Status Register

Return to Summary Table

Table 14-11004. Instance Table

Instance Name	Physical Address
CPSW0	0800 0034h

Figure 14-5438. CPSW3_RGMII2_STATUS_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>FULLDUPLEX</td><td colspan="2">SPEED</td><td>LINK</td></tr>
<tr><td colspan="4">NONE</td><td>R</td><td colspan="2">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-11005. CPSW3_RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

3	FULLDUPLEX	R	0h	RGMII Port 2 full dulex:
				`0h Half-duplex`
				`1h Full-duplex`

2:1	SPEED	R	0h	RGMII Port 2 speed:
				`0h 10Mbps`
				`1h 100Mbps`
				`2h 1000Mbps`
				`3h Reserved`

0	LINK	R	0h	RGMII Port 2 link indicator:
				`0h Link is down`
				`1h Link is up`

14.7.3.1.2.25 CPSW3_MDIO_MDIO_VERSION_REG Register

14.7.3.1.2.25.1 CPSW3_MDIO_MDIO_VERSION_REG Register (Offset = F00h) [reset = 71107h]

MDIO Version Register

Return to Summary Table

Table 14-11006. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F00h + formula

Figure 14-5439. CPSW3_MDIO_MDIO_VERSION_REG Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
0h		0h		7h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
7h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
2h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		7h					

Table 14-11007. CPSW3_MDIO_MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	0h	Scheme
29:28	BU	R	0h	bu
27:16	MODULE_ID	R	7h	Module ID
15:11	REVRTL	R	2h	RTL version
10:8	REVMAJ	R	1h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	7h	Minor version

14.7.3.1.2.26 CPSW3_MDIO_CONTROL_REG Register

14.7.3.1.2.26.1 CPSW3_MDIO_CONTROL_REG Register (Offset = F04h) [reset = 810000FFh]

MDIO Control Register

Return to Summary Table

Table 14-11008. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F04h + formula

Figure 14-5440. CPSW3_MDIO_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R	R/W	NONE	R				
1h	0h	0h	1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
NONE			R/W	R/W	R/W	R/W	NONE
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKDIV							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKDIV							
R/W							
FFh							

Table 14-11009. CPSW3_MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1h when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1h to this bit enables the MDIO state machine, writing a 0h disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	NONE	0h	Reserved
28:24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest useraccess channel that is available in the module and is currently set to 1h. This implies that MDIOUserAccess1 is the highest available user access channel.
23:21	RESERVED	NONE	0h	Reserved
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1h to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.

Table 14-11009. CPSW3_MDIO_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	FAULT	R/W	0h	Fault indicator. This bit is set to 1h if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1h to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1h to enable the physical layer fault detection.
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1h to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	NONE	0h	Reserved
15:0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. When clkdiv is set to 0h, MDCLK is disabled and output is driven to a high logic state. MDCLK frequency = clk frequency/(clkdiv+1).

14.7.3.1.2.27 CPSW3_MDIO_ALIVE_REG Register

14.7.3.1.2.27.1 CPSW3_MDIO_ALIVE_REG Register (Offset = F08h) [reset = 0h]

MDIO Alive Register

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Table 14-11010. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F08h + formula

Figure 14-5441. CPSW3_MDIO_ALIVE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ALIVE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ALIVE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ALIVE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ALIVE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11011. CPSW3_MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ALIVE	R/W	0h	MDIO Alive. Each of the 32-bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address. Writing a 1h to any bit will clear it, writing a 0h has no effect.

14.7.3.1.2.28 CPSW3_MDIO_LINK_REG Register

14.7.3.1.2.28.1 CPSW3_MDIO_LINK_REG Register (Offset = F0Ch) [reset = 0h]

MDIO Link Register

Return to Summary Table

Table 14-11012. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F0Ch + formula

Figure 14-5442. CPSW3_MDIO_LINK_REG Name Register

31	30	29	28	27	26	25	24
LINK							
R							
0h							
23	22	21	20	19	18	17	16
LINK							
R							
0h							
15	14	13	12	11	10	9	8
LINK							
R							
0h							
7	6	5	4	3	2	1	0
LINK							
R							
0h							

Table 14-11013. CPSW3_MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LINK	R	0h	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to 0h if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIOUserPhySel registers can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIOUserPhySel register. In State Change Mode the MLINK input pins are unused.

14.7.3.1.2.29 CPSW3_MDIO_LINK_INT_RAW_REG Register

14.7.3.1.2.29.1 CPSW3_MDIO_LINK_INT_RAW_REG Register (Offset = F10h) [reset = 0h]

MDIO Link Interrupt Raw Register

Return to Summary Table

Table 14-11014. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F10h + formula

Figure 14-5443. CPSW3_MDIO_LINK_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
NONE						R/W	
0h						0h	

Table 14-11015. CPSW3_MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTRAW	R/W	0h	MDIO link change event raw value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register. [0]LINKINTRAW and [1]LINKINTRAW correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set LINKINTRAW bits to a 1h which may be used for test purposes. MDIO link change event raw value. State Change Mode operation: The [0]LINKINTRAW bit will be asserted '1' when any bit (for any PHY) in the MDIOAlive or MDIOLink registers changes due to MDIO operations. The [1]LINKINTRAW bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the [0]LINKINTRAW bit to a 1h which may be used for test purposes.

14.7.3.1.2.30 CPSW3_MDIO_LINK_INT_MASKED_REG Register

14.7.3.1.2.30.1 CPSW3_MDIO_LINK_INT_MASKED_REG Register (Offset = F14h) [reset = 0h]

MDIO Link Interrupt Masked Register

Return to Summary Table

Table 14-11016. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F14h + formula

Figure 14-5444. CPSW3_MDIO_LINK_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
NONE						R/W	
0h						0h	

Table 14-11017. CPSW3_MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTMASKED	R/W	0h	MDIO link change interrupt masked value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding CPSW_MDIO_USER_PHY_SEL_REG_k[6] LINKINT_ENABLE bit was set. CPSW_MDIO_LINK_INT_MASKED_REG[0] LINKINTMASKED and [1] LINKINTMASKED correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1h will clear the interrupt and writing 0h has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values. MDIO link change interrupt masked value. State Change Mode operation: The [0] LINKINTMASKED bit will be asserted '1' when CPSW_MDIO_LINK_INT_RAW_REG[0] LINKINTRAW is asserted '1' and when the CPSW_MDIO_LINK_INT_MASK_SET_REG[0] LINKINTMASKSET bit is set to 1h. Writing a 1h will clear [0] LINKINTMASKED (and the MDIO_LINKINT[0] output) and writing 0h has no effect. The [1] LINKINTMASKED bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode).

14.7.3.1.2.31 CPSW3_MDIO_LINK_INT_MASK_SET_REG Register

14.7.3.1.2.31.1 CPSW3_MDIO_LINK_INT_MASK_SET_REG Register (Offset = F18h) [reset = 0h]

MDIO Link Interrupt Mask Set Register

Return to Summary Table

Table 14-11018. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F18h + formula

Figure 14-5445. CPSW3_MDIO_LINK_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASKSET
NONE							R/W
0h							0h

Table 14-11019. CPSW3_MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKSET	R/W	0h	MDIO link interrupt mask set. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask set. State Change Mode Operation: Writing this bit to 1h will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when [0] LINKINTRAW is asserted.

14.7.3.1.2.32 CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register

14.7.3.1.2.32.1 CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = F1Ch) [reset = 0h]

MDIO Link Interrupt Mask Clear Register

Return to Summary Table

Table 14-11020. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F1Ch + formula

Figure 14-5446. CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK CLR
NONE							R/W
0h							0h

Table 14-11021. CPSW3_MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKCLR	R/W	0h	MDIO link interrupt mask clear. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask clear. State Change Mode Operation: Writing this bit to 1h will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the [0] LINKINTRAW bit value.

14.7.3.1.2.33 CPSW3_MDIO_USER_INT_RAW_REG Register

14.7.3.1.2.33.1 CPSW3_MDIO_USER_INT_RAW_REG Register (Offset = F20h) [reset = 0h]

MDIO User Interrupt Raw Register

Return to Summary Table

Table 14-11022. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F20h + formula

Figure 14-5447. CPSW3_MDIO_USER_INT_RAW_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">USERINTRAW</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-11023. CPSW3_MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTRAW	R/W	0h	Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the userintraw bits to a 1h. This mode may be used for test purposes.

14.7.3.1.2.34 CPSW3_MDIO_USER_INT_MASKED_REG Register

14.7.3.1.2.34.1 CPSW3_MDIO_USER_INT_MASKED_REG Register (Offset = F24h) [reset = 0h]

MDIO User Interrupt Masked Register

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Table 14-11024. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F24h + formula

Figure 14-5448. CPSW3_MDIO_USER_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						USERINTMASKED	
NONE						R/W	
0h						0h	

Table 14-11025. CPSW3_MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKED	R/W	0h	Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1h. Writing a 1h will clear the interrupt and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED bits to a 1h. This mode may be used for test purposes.

14.7.3.1.2.35 CPSW3_MDIO_USER_INT_MASK_SET_REG Register

14.7.3.1.2.35.1 CPSW3_MDIO_USER_INT_MASK_SET_REG Register (Offset = F28h) [reset = 0h]

MDIO User Interrupt Mask Set Register

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Table 14-11026. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F28h + formula

Figure 14-5449. CPSW3_MDIO_USER_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKSET	
NONE						R/W	
0h						0h	

Table 14-11027. CPSW3_MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKSET	R/W	0h	MDIO user interrupt mask set for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0h. Writing a 0h to this register has no effect.

14.7.3.1.2.36 CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register

14.7.3.1.2.36.1 CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = F2Ch) [reset = 0h]

MDIO User Interrupt Mask Clear Register

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Table 14-11028. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F2Ch + formula

Figure 14-5450. CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
NONE						R/W	
0h						0h	

Table 14-11029. CPSW3_MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKCLR	R/W	0h	MDIO user command complete interrupt mask clear for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0h to this register has no effect.

14.7.3.1.2.37 CPSW3_MDIO_MANUAL_IF_REG Register

14.7.3.1.2.37.1 CPSW3_MDIO_MANUAL_IF_REG Register (Offset = F30h) [reset = 0h]

MDIO Manual Interface Register

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Table 14-11030. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F30h + formula

Figure 14-5451. CPSW3_MDIO_MANUAL_IF_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-11031. CPSW3_MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output. This value is the MDCLK_O output value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
1	MDIO_OE	R/W	0h	MDIO Output Enable. This value is inverted and output on the MDIO_OE_N output when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
0	MDIO_PIN	R/W	0h	MDIO Pin Value. This is the external MDIO data pin value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted '1'. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted '1' and MDIO_PIN is written with a 1h then MDIO_PIN should read a 1h if there are no external devices pulling the MDIO data line low.

14.7.3.1.2.38 CPSW3_MDIO_POLL_REG Register

14.7.3.1.2.38.1 CPSW3_MDIO_POLL_REG Register (Offset = F34h) [reset = 0h]

MDIO Poll Register

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Table 14-11032. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F34h + formula

Figure 14-5452. CPSW3_MDIO_POLL_REG Name Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANGEMODE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPG							
R/W							
0h							

Table 14-11033. CPSW3_MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	MDIO Manual Mode. When set 1h, the MDIO pins are directly controlled by software through the bits in the CPSW_MDIO_MANUAL_IF_REG register `1h Manual Mode.`

30	STATECHANGEMODE	R/W	0h	MDIO State Change Mode. When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations.
				`0h Normal Mode.`
				`1h State Change Mode.`

29:8	RESERVED	NONE	0h	Reserved
7:0	IPG	R/W	0h	Polling Inter Packet Gap Value. This value is the number of MDCLK_O clocks between each poll when polling is enabled.

14.7.3.1.2.39 CPSW3_MDIO_POLL_EN_REG Register

14.7.3.1.2.39.1 CPSW3_MDIO_POLL_EN_REG Register (Offset = F38h) [reset = FFFFFFFFh]

MDIO Poll Enable Register

Return to Summary Table

Table 14-11034. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F38h + formula

Figure 14-5453. CPSW3_MDIO_POLL_EN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">POLL_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFFFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">POLL_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFFFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">POLL_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFFFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">POLL_EN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFFFFFFFh</td></tr>
</table>

Table 14-11035. CPSW3_MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POLL_EN	R/W	FFFFFFFFh	MDIO Poll Enable. When set, the bit indicates that the associated PHY will be included in polling operations. When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set (regardless of the value of the preamble disable bit ([20] PREAMBLE) in the CPSW_MDIO_CONTROL_REG register. However, there does not have to be a PHY at address 31.

14.7.3.1.2.40 CPSW3_MDIO_CLAUS45_REG Register

14.7.3.1.2.40.1 CPSW3_MDIO_CLAUS45_REG Register (Offset = F3Ch) [reset = 0h]

MDIO Clause45 Register

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Table 14-11036. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F3Ch + formula

Figure 14-5454. CPSW3_MDIO_CLAUS45_REG Name Register

31	30	29	28	27	26	25	24
CLAUSE45							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAUSE45							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAUSE45							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAUSE45							
R/W							
0h							

Table 14-11037. CPSW3_MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAUSE45	R/W	0h	MDIO clause 45 mode. When a clause45 bit is cleared 0h, the PHY associated with the clause45 bit is operating in the clause 22 mode. When set 1h, the PHY associated with the clause45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on.

14.7.3.1.2.41 CPSW3_MDIO_USER_ADDR0_REG Register

14.7.3.1.2.41.1 CPSW3_MDIO_USER_ADDR0_REG Register (Offset = F40h) [reset = 0h]

MDIO Address 0 Register

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Table 14-11038. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F40h + formula

Figure 14-5455. CPSW3_MDIO_USER_ADDR0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
USER_ADDR0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
USER_ADDR0							
R/W							
0h							

Table 14-11039. CPSW3_MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR0	R/W	0h	MDIO User Address 0. In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIOUserAccess0 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess0 access.

14.7.3.1.2.42 CPSW3_MDIO_USER_ADDR1_REG Register

14.7.3.1.2.42.1 CPSW3_MDIO_USER_ADDR1_REG Register (Offset = F44h) [reset = 0h]

MDIO Address 1 Register

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Table 14-11040. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F44h + formula

Figure 14-5456. CPSW3_MDIO_USER_ADDR1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
USER_ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
USER_ADDR1							
R/W							
0h							

Table 14-11041. CPSW3_MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR1	R/W	0h	MDIO User Address 1. In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIOUserAccess1 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess1 access.

14.7.3.1.2.43 CPSW3_INTD_REVISION Register

14.7.3.1.2.43.1 CPSW3_INTD_REVISION Register (Offset = 1000h) [reset = 6690A200h]

Revision Register

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Table 14-11042. Instance Table

Instance Name	Physical Address
CPSW0	0800 1000h + formula

Figure 14-5457. CPSW3_INTD_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		690h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
690h							
15	14	13	12	11	10	9	8
RTLVER					MAJREV		
R					R		
14h					2h		
7	6	5	4	3	2	1	0
CUSTOM		MINREV					
R		R					
0h		0h					

Table 14-11043. CPSW3_INTD_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	BU
27:16	FUNCTION	R	690h	Module ID
15:11	RTLVER	R	14h	RTL revisions
10:8	MAJREV	R	2h	Major revision
7:6	CUSTOM	R	0h	Custom revision
5:0	MINREV	R	0h	Minor revision

14.7.3.1.2.44 CPSW3_INTD_EOI_REG Register

14.7.3.1.2.44.1 CPSW3_INTD_EOI_REG Register (Offset = 1010h) [reset = 0h]

End of Interrupt Register

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Table 14-11044. Instance Table

Instance Name	Physical Address
CPSW0	0800 1010h + formula

Figure 14-5458. CPSW3_INTD_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EOI_VECTOR							
R/W							
0h							

Table 14-11045. CPSW3_INTD_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	End of Interrupt Vector

14.7.3.1.2.45 CPSW3_INTD_INTR_VECTOR_REG Register

14.7.3.1.2.45.1 CPSW3_INTD_INTR_VECTOR_REG Register (Offset = 1014h) [reset = 0h]

Interrupt Vector Register

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Table 14-11046. Instance Table

Instance Name	Physical Address
CPSW0	0800 1014h + formula

Figure 14-5459. CPSW3_INTD_INTR_VECTOR_REG Name Register

31	30	29	28	27	26	25	24
INTR_VECTOR							
R							
0h							
23	22	21	20	19	18	17	16
INTR_VECTOR							
R							
0h							
15	14	13	12	11	10	9	8
INTR_VECTOR							
R							
0h							
7	6	5	4	3	2	1	0
INTR_VECTOR							
R							
0h							

Table 14-11047. CPSW3_INTD_INTR_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTR_VECTOR	R	0h	Interrupt Vector Register

14.7.3.1.2.46 CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register

14.7.3.1.2.46.1 CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register (Offset = 1100h) [reset = 0h]

Enable Register 0

Return to Summary Table

Table 14-11048. Instance Table

Instance Name	Physical Address
CPSW0	0800 1100h + formula

Figure 14-5460. CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA	ENABLE_OUT_PULSE_EN_MDIO_PENDA	ENABLE_OUT_PULSE_EN_EVNT_PENDA
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-11049. CPSW3_INTD_ENABLE_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_OUT_PULSE_EN_STAT_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVNT_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_evnt_penda

14.7.3.1.2.47 CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register

14.7.3.1.2.47.1 CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register (Offset = 1300h) [reset = 0h]

Enable Clear Register 0

Return to Summary Table

Table 14-11050. Instance Table

Instance Name	Physical Address
CPSW0	0800 1300h + formula

Figure 14-5461. CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	ENABLE_OUT_PULSE_EN_EVNT_PENDA_CLR
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-11051. CPSW3_INTD_ENABLE_CLR_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVNT_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_evnt_penda

14.7.3.1.2.48 CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register

14.7.3.1.2.48.1 CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register (Offset = 1500h) [reset = 0h]

Status Register 0

Return to Summary Table

Table 14-11052. Instance Table

Instance Name	Physical Address
CPSW0	0800 1500h + formula

Figure 14-5462. CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					STATUS_OUT_PULSE_STAT_PENDA	STATUS_OUT_PULSE_MDIO_PENDA	STATUS_OUT_PULSE_EVNT_PENDA
NONE					R	R	R
0h					0h	0h	0h

Table 14-11053. CPSW3_INTD_STATUS_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	STATUS_OUT_PULSE_STAT_PENDA	R	0h	Status for out_pulse_en_stat_penda
1	STATUS_OUT_PULSE_MDIO_PENDA	R	0h	Status for out_pulse_en_mdio_penda
0	STATUS_OUT_PULSE_EVNT_PENDA	R	0h	Status for out_pulse_en_evnt_penda

14.7.3.1.2.49 CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register

14.7.3.1.2.49.1 CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register (Offset = 1A80h) [reset = 0h]

Interrupt Vector for out_pulse

Return to Summary Table

Table 14-11054. Instance Table

Instance Name	Physical Address
CPSW0	0800 1A80h + formula

Figure 14-5463. CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Name Register

31	30	29	28	27	26	25	24
INTR_VECTOR_OUT_PULSE							
R							
0h							
23	22	21	20	19	18	17	16
INTR_VECTOR_OUT_PULSE							
R							
0h							
15	14	13	12	11	10	9	8
INTR_VECTOR_OUT_PULSE							
R							
0h							
7	6	5	4	3	2	1	0
INTR_VECTOR_OUT_PULSE							
R							
0h							

Table 14-11055. CPSW3_INTD_INTR_VECTOR_REG_OUT_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTR_VECTOR_OUT_PULSE	R	0h	Interrupt Vector

14.7.3.1.2.50 CPSW3_CPSW_NU_CPSW_ID_VER_REG Register

14.7.3.1.2.50.1 CPSW3_CPSW_NU_CPSW_ID_VER_REG Register (Offset = 20000h) [reset = 6BA80103h]

CPSW ID Version

Return to Summary Table

Table 14-11056. Instance Table

Instance Name	Physical Address
CPSW0	0802 0000h + formula

Figure 14-5464. CPSW3_CPSW_NU_CPSW_ID_VER_REG Name Register

31	30	29	28	27	26	25	24
IDENT							
R							
6BA8h							
23	22	21	20	19	18	17	16
IDENT							
R							
6BA8h							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_VER		
R					R		
0h					1h		
7	6	5	4	3	2	1	0
MINOR_VER							
R							
3h							

Table 14-11057. CPSW3_CPSW_NU_CPSW_ID_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6BA8h	Identification Value
15:11	RTL_VER	R	0h	RTL Version Value
10:8	MAJOR_VER	R	1h	Major Version Value
7:0	MINOR_VER	R	3h	Minor Version Value

14.7.3.1.2.51 CPSW3_CPSW_NU_CONTROL_REG Register

14.7.3.1.2.51.1 CPSW3_CPSW_NU_CONTROL_REG Register (Offset = 20004h) [reset = 0h]

CPSW Switch Control

Return to Summary Table

Table 14-11058. Instance Table

Instance Name	Physical Address
CPSW0	0802 0004h + formula

Figure 14-5465. CPSW3_CPSW_NU_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
ECC_CRC_MODE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				CUT_THRU_ENABLE	EST_ENABLE	IET_ENABLE	EEE_ENABLE
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P0_RX_PASS_CRC_ERR	P0_RX_PAD	P0_TX_CRC_REMOVE	P0_TX_CRC_TYPE	P8_PASS_PRI_TAGGED	P7_PASS_PRI_TAGGED	P6_PASS_PRI_TAGGED	P5_PASS_PRI_TAGGED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P4_PASS_PRI_TAGGED	P3_PASS_PRI_TAGGED	P2_PASS_PRI_TAGGED	P1_PASS_PRI_TAGGED	P0_PASS_PRI_TAGGED	P0_ENABLE	VLAN_AWARE	S_CN_SWITCH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11059. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_CRC_MODE	R/W	0h	ECC CRC Mode. 0h ECC errors induced through the ECC aggregator flip bits in the packet headers (not in packet data). 1h ECC errors induced through the ECC aggregator flip bits in the packet data (not in the packet headers).
30:20	RESERVED	NONE	0h	Reserved
19	CUT_THRU_ENABLE	R/W	0h	Cut Thru Enable. 0h Cut Thru disabled 1h Cut Thru enabled
18	EST_ENABLE	R/W	0h	Enhanced Scheduled Traffic enable (EST) 0h EST is disabled 1h EST is enabled
17	IET_ENABLE	R/W	0h	Interspersed Express Traffic enable (IET) 0h IET is disabled 1h IET is enabled
16	EEE_ENABLE	R/W	0h	Energy Efficient Ethernet enable 0h Energy Efficient Ethernet is disabled 1h Energy Efficient Ethernet is enabled

Table 14-11059. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	P0_RX_PASS_CRC_ERR	R/W	0h	Port 0 Pass Received CRC errors 0h Packets received with CRC errors on Port 0 are dropped. 1h Packets received with CRC errors on Port 0 are transferred to the destination ports.
14	P0_RX_PAD	R/W	0h	Port 0 Receive Short Packet Pad 0h Short packets are dropped. 1h Short packets are padded to 64-bytes (with pad and added CRC) if the CRC is not passed in. Short packets are dropped if the CRC is passed (in the Info0 word).
13	P0_TX_CRC_REMOVE	R/W	0h	Port 0 Transmit CRC remove. 0h Do not remove the CRC on Port 0 transmit (egress) packets. 1h Remove the CRC on all Port 0 transmit (egress) packets.
12	P0_TX_CRC_TYPE	R/W	0h	
11	P8_PASS_PRI_TAGGED	R/W	0h	Port 8 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P8_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
10	P7_PASS_PRI_TAGGED	R/W	0h	Port 7 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P7_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
9	P6_PASS_PRI_TAGGED	R/W	0h	Port 6 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P6_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
8	P5_PASS_PRI_TAGGED	R/W	0h	Port 5 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P5_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
7	P4_PASS_PRI_TAGGED	R/W	0h	Port 4 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P4_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
6	P3_PASS_PRI_TAGGED	R/W	0h	Port 3 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P3_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
5	P2_PASS_PRI_TAGGED	R/W	0h	Port 2 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P2_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.

Table 14-11059. CPSW3_CPSW_NU_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	P1_PASS_PRI_TAGGED	R/W	0h	Port 1 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port Enet_P1_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
3	P0_PASS_PRI_TAGGED	R/W	0h	Port 0 Pass Priority Tagged 0h Priority tagged packets have the zero VID replaced with the input port P0_PORT_VLAN[11:0] on ingress. 1h Priority tagged packets are processed unchanged.
2	P0_ENABLE	R/W	0h	Port 0 Enable 0h CPPI port (port 0) packet operations are disabled 1h CPPI port (port 0) packet operations are enabled
1	VLAN_AWARE	R/W	0h	VLAN Aware Mode: 0h CPSW_NU is in the VLAN unaware mode. 1h CPSW_NU is in the VLAN aware mode.
0	S_CN_SWITCH	R/W	0h	Service or Customer VLAN switch. 0h Customer switch. VLAN processing uses the inner_vlan_ltype. 1h Servide switch. VLAN processing uses the outer_vlan_ltype.

14.7.3.1.2.52 CPSW3_CPSW_NU_EM_CONTROL_REG Register

14.7.3.1.2.52.1 CPSW3_CPSW_NU_EM_CONTROL_REG Register (Offset = 20010h) [reset = 0h]

CPSW Emulation Control

Return to Summary Table

Table 14-11060. Instance Table

Instance Name	Physical Address
CPSW0	0802 0010h + formula

Figure 14-5466. CPSW3_CPSW_NU_EM_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-11061. CPSW3_CPSW_NU_EM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.7.3.1.2.53 CPSW3_CPSW_NU_STAT_PORT_EN_REG Register

14.7.3.1.2.53.1 CPSW3_CPSW_NU_STAT_PORT_EN_REG Register (Offset = 20014h) [reset = 0h]

CPSW Statistics Port Enable

Return to Summary Table

Table 14-11062. Instance Table

Instance Name	Physical Address
CPSW0	0802 0014h + formula

Figure 14-5467. CPSW3_CPSW_NU_STAT_PORT_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							P8_STAT_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11063. CPSW3_CPSW_NU_STAT_PORT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	P8_STAT_EN	R/W	0h	Port 8 Statistics Enable (if N > 8) 0h Port 8 statistics are not enabled 1h Port 8 statistics are enabled.
7	P7_STAT_EN	R/W	0h	Port 7 Statistics Enable (if N > 7) 0h Port 7 statistics are not enabled 1h Port 7 statistics are enabled.
6	P6_STAT_EN	R/W	0h	Port 6 Statistics Enable (if N > 6) 0h Port 6 statistics are not enabled 1h Port 6 statistics are enabled.
5	P5_STAT_EN	R/W	0h	Port 5 Statistics Enable (if N > 5) 0h Port 5 statistics are not enabled 1h Port 5 statistics are enabled.
4	P4_STAT_EN	R/W	0h	Port 4 Statistics Enable (if N > 4) 0h Port 4 statistics are not enabled 1h Port 4 statistics are enabled.
3	P3_STAT_EN	R/W	0h	Port 3 Statistics Enable (if N > 3) 0h Port 3 statistics are not enabled 1h Port 3 statistics are enabled.

Table 14-11063. CPSW3_CPSW_NU_STAT_PORT_EN_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2	P2_STAT_EN	R/W	0h	Port 2 Statistics Enable (if N > 2)
				`0h` `Port 2 statistics are not enabled`
				`1h` `Port 2 statistics are enabled.`

1	P1_STAT_EN	R/W	0h	Port 1 Statistics Enable
				`0h` `Port 1 statistics are not enabled`
				`1h` `Port 1 statistics are enabled.`

0	P0_STAT_EN	R/W	0h	Port 0 Statistics Enable
				`0h` `Port 0 statistics are not enabled`
				`1h` `Port 0 statistics are enabled.`

14.7.3.1.2.54 CPSW3_CPSW_NU_PTYPE_REG Register

14.7.3.1.2.54.1 CPSW3_CPSW_NU_PTYPE_REG Register (Offset = 20018h) [reset = 0h]

CPSW Transmit Priority Type

Return to Summary Table

Table 14-11064. Instance Table

Instance Name	Physical Address
CPSW0	0802 0018h + formula

Figure 14-5468. CPSW3_CPSW_NU_PTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							P8_PTYPE_ESC
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC	P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED				ESC_PRI_LD_VAL			
NONE				R/W			
0h				0h			

Table 14-11065. CPSW3_CPSW_NU_PTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	P8_PTYPE_ESC	R/W	0h	Port 8 Priority Type Escalate (if N > 8) 0h Port 8 priority type fixed 1h Port 8 priority type escalate
15	P7_PTYPE_ESC	R/W	0h	Port 7 Priority Type Escalate (if N > 7) 0h Port 7 priority type fixed 1h Port 7 priority type escalate
14	P6_PTYPE_ESC	R/W	0h	Port 6 Priority Type Escalate (if N > 6) 0h Port 6 priority type fixed 1h Port 6 priority type escalate
13	P5_PTYPE_ESC	R/W	0h	Port 5 Priority Type Escalate (if N > 5) 0h Port 5 priority type fixed 1h Port 5 priority type escalate
12	P4_PTYPE_ESC	R/W	0h	Port 4 Priority Type Escalate (if N > 4) 0h Port 4 priority type fixed 1h Port 4 priority type escalate
11	P3_PTYPE_ESC	R/W	0h	Port 3 Priority Type Escalate (if N > 3) 0h Port 3 priority type fixed 1h Port 3 priority type escalate

Table 14-11065. CPSW3_CPSW_NU_PTYPE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

10	P2_PTYPE_ESC	R/W	0h	Port 2 Priority Type Escalate (if N > 2)
				`0h      Port 2 priority type fixed`
				`1h      Port 2 priority type escalate`

9	P1_PTYPE_ESC	R/W	0h	Port 1 Priority Type Escalate
				`0h      Port 1 priority type fixed`
				`1h      Port 1 priority type escalate`

8	P0_PTYPE_ESC	R/W	0h	Port 0 Priority Type Escalate
				`0h      Port 0 priority type fixed`
				`1h      Port 0 priority type escalate`

7:5	RESERVED	NONE	0h	Reserved
4:0	ESC_PRI_LD_VAL	R/W	0h	Escalate Priority Load Value. When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority. The min value of ESC_PRI_LD_VAL = 2h.

14.7.3.1.2.55 CPSW3_CPSW_NU_SOFT_IDLE_REG Register

14.7.3.1.2.55.1 CPSW3_CPSW_NU_SOFT_IDLE_REG Register (Offset = 2001Ch) [reset = 0h]

CPSW Software Idle

Return to Summary Table

Table 14-11066. Instance Table

Instance Name	Physical Address
CPSW0	0802 001Ch + formula

Figure 14-5469. CPSW3_CPSW_NU_SOFT_IDLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_IDLE
NONE							R/W
0h							0h

Table 14-11067. CPSW3_CPSW_NU_SOFT_IDLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_IDLE	R/W	0h	Software Idle. 0h Not in Idle. 1h Command a MCU_CPSW0 software Idle. when set, no packets will be started to be unloaded from ports 0 through 4 receive unload. Packets that are currently being unloaded are unaffected.

14.7.3.1.2.56 CPSW3_CPSW_NU_THRU_RATE_REG Register

14.7.3.1.2.56.1 CPSW3_CPSW_NU_THRU_RATE_REG Register (Offset = 20020h) [reset = 3001h]

CPSW Thru Rate

Return to Summary Table

Table 14-11068. Instance Table

Instance Name	Physical Address
CPSW0	0802 0020h + formula

Figure 14-5470. CPSW3_CPSW_NU_THRU_RATE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">SL_RX_THRU_RATE</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">3h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">P0_RX_THRU_RATE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
</table>

Table 14-11069. CPSW3_CPSW_NU_THRU_RATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	SL_RX_THRU_RATE	R/W	3h	Ethernet Port Switch FIFO receive through rate. This register value is the maximum throughput of the Ethernet ports to the crossbar SCR. The default is one 8-byte word for every 3 VBUSP_GCLK periods maximum. The minimum value is 2. This is not a field that is intended to be changed by a user.
11:4	RESERVED	NONE	0h	Reserved
3:0	P0_RX_THRU_RATE	R/W	1h	CPPI FIFO (port 0) receive through rate. This register value is the maximum throughput of the CPPI FIFO (port 0) into the MCU_CPSW0. The minimum value is 1. This field is not intended to be changed by the user.

14.7.3.1.2.57 CPSW3_CPSW_NU_GAP_THRESH_REG Register

14.7.3.1.2.57.1 CPSW3_CPSW_NU_GAP_THRESH_REG Register (Offset = 20024h) [reset = Bh]

CPSW Transmit FIFO Short Gap Threshold

Return to Summary Table

Table 14-11070. Instance Table

Instance Name	Physical Address
CPSW0	0802 0024h + formula

Figure 14-5471. CPSW3_CPSW_NU_GAP_THRESH_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">GAP_THRESH</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">Bh</td></tr>
</table>

Table 14-11071. CPSW3_CPSW_NU_GAP_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	GAP_THRESH	R/W	Bh	Ethernet Port Short Gap Threshold. This is the Ethernet port associated FIFO transmit block usage value for triggering transmit short gap (when short gap is enabled).

14.7.3.1.2.58 CPSW3_CPSW_NU_EEE_PRESCALE_REG Register

14.7.3.1.2.58.1 CPSW3_CPSW_NU_EEE_PRESCALE_REG Register (Offset = 2002Ch) [reset = 0h]

CPSW Energy Efficient Ethernet Prescale Value

Return to Summary Table

Table 14-11072. Instance Table

Instance Name	Physical Address
CPSW0	0802 002Ch + formula

Figure 14-5472. CPSW3_CPSW_NU_EEE_PRESCALE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				EEE_PRESCALE			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
EEE_PRESCALE							
R/W							
0h							

Table 14-11073. CPSW3_CPSW_NU_EEE_PRESCALE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	EEE_PRESCALE	R/W	0h	Energy Efficient Ethernet Pre-scale count load value

14.7.3.1.2.59 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register

14.7.3.1.2.59.1 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register (Offset = 20030h) [reset = FFFFFFFFh]

CPSW PFC Tx Global Out Flow Threshold Set

Return to Summary Table

Table 14-11074. Instance Table

Instance Name	Physical Address
CPSW0	0802 0030h + formula

Figure 14-5473. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
Fh				Fh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI5				PRI4			
R/W				R/W			
Fh				Fh			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI3				PRI2			
R/W				R/W			
Fh				Fh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI1				PRI0			
R/W				R/W			
Fh				Fh			

Table 14-11075. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

14.7.3.1.2.60 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register

14.7.3.1.2.60.1 CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register (Offset = 20034h) [reset = 0h]

CPSW PFC Tx Global Out Flow Threshold Clear

Return to Summary Table

Table 14-11076. Instance Table

Instance Name	Physical Address
CPSW0	0802 0034h + formula

Figure 14-5474. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
0h				0h			

Table 14-11077. CPSW3_CPSW_NU_TX_G_OFLOW_THRESH_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

14.7.3.1.2.61 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register

14.7.3.1.2.61.1 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 20038h) [reset = FFFFFFFFh]

CPSW PFC Global Tx Buffer Threshold Set Low

Return to Summary Table

Table 14-11078. Instance Table

Instance Name	Physical Address
CPSW0	0802 0038h + formula

Figure 14-5475. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
PRI3							
R/W							
FFh							
23	22	21	20	19	18	17	16
PRI2							
R/W							
FFh							
15	14	13	12	11	10	9	8
PRI1							
R/W							
FFh							
7	6	5	4	3	2	1	0
PRI0							
R/W							
FFh							

Table 14-11079. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

14.7.3.1.2.62 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register

14.7.3.1.2.62.1 CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 2003Ch) [reset = FFFFFFFFh]

CPSW PFC Global Tx Buffer Threshold Set High

Return to Summary Table

Table 14-11080. Instance Table

Instance Name	Physical Address
CPSW0	0802 003Ch + formula

Figure 14-5476. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
PRI7							
R/W							
FFh							
23	22	21	20	19	18	17	16
PRI6							
R/W							
FFh							
15	14	13	12	11	10	9	8
PRI5							
R/W							
FFh							
7	6	5	4	3	2	1	0
PRI4							
R/W							
FFh							

Table 14-11081. CPSW3_CPSW_NU_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

14.7.3.1.2.63 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register

14.7.3.1.2.63.1 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 20040h) [reset = 0h]

CPSW PFC Global Tx Buffer Threshold Clear Low

Return to Summary Table

Table 14-11082. Instance Table

Instance Name	Physical Address
CPSW0	0802 0040h + formula

Figure 14-5477. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
PRI3							
R/W							
0h							
23	22	21	20	19	18	17	16
PRI2							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI1							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI0							
R/W							
0h							

Table 14-11083. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

14.7.3.1.2.64 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register

14.7.3.1.2.64.1 CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 20044h) [reset = 0h]

CPSW PFC Global Tx Buffer Threshold Clear High

Return to Summary Table

Table 14-11084. Instance Table

Instance Name	Physical Address
CPSW0	0802 0044h + formula

Figure 14-5478. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PRI7</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRI6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRI5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRI4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11085. CPSW3_CPSW_NU_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

14.7.3.1.2.65 CPSW3_CPSW_NU_VLAN_LTYPE_REG Register

14.7.3.1.2.65.1 CPSW3_CPSW_NU_VLAN_LTYPE_REG Register (Offset = 20050h) [reset = 88A88100h]

VLAN Length/type

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Table 14-11086. Instance Table

Instance Name	Physical Address
CPSW0	0802 0050h + formula

Figure 14-5479. CPSW3_CPSW_NU_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
VLAN_LTYPE_OUTER							
R/W							
88A8h							
23	22	21	20	19	18	17	16
VLAN_LTYPE_OUTER							
R/W							
88A8h							
15	14	13	12	11	10	9	8
VLAN_LTYPE_INNER							
R/W							
8100h							
7	6	5	4	3	2	1	0
VLAN_LTYPE_INNER							
R/W							
8100h							

Table 14-11087. CPSW3_CPSW_NU_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	VLAN_LTYPE_OUTER	R/W	88A8h	Outer VLAN LType
15:0	VLAN_LTYPE_INNER	R/W	8100h	Inner VLAN LType

14.7.3.1.2.66 CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register

14.7.3.1.2.66.1 CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register (Offset = 20054h) [reset = 0h]

Enhanced Scheduled Traffic Host Event Domain

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Table 14-11088. Instance Table

Instance Name	Physical Address
CPSW0	0802 0054h + formula

Figure 14-5480. CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EST_TS_DOMAIN							
R/W							
0h							

Table 14-11089. CPSW3_CPSW_NU_EST_TS_DOMAIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EST_TS_DOMAIN	R/W	0h	Enhanced Scheduled Traffic Host Event Domain. This value is used as the domain in the CPTS event to indicate that the event came from EST.

14.7.3.1.2.67 CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register

14.7.3.1.2.67.1 CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register (Offset = 20058h) [reset = 0h]

Cut-thru Threshold

Return to Summary Table

Table 14-11090. Instance Table

Instance Name	Physical Address
CPSW0	0802 0058h + formula

Figure 14-5481. CPSW3_CPSW_NU_CUT_THRESHOLD_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CUT_THRESH			
NONE				R/W			
0h				0h			

Table 14-11091. CPSW3_CPSW_NU_CUT_THRESHOLD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CUT_THRESH	R/W	0h	Cut_thru_threshold. This is not intended to be changed by software.

14.7.3.1.2.68 CPSW3_CPSW_NU_FREQUENCY_REG Register

14.7.3.1.2.68.1 CPSW3_CPSW_NU_FREQUENCY_REG Register (Offset = 2005Ch) [reset = 0h]

CPSW CPPI_CLK Frequency in Mhz

Return to Summary Table

Table 14-11092. Instance Table

Instance Name	Physical Address
CPSW0	0802 005Ch + formula

Figure 14-5482. CPSW3_CPSW_NU_FREQUENCY_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CPSW_FREQUENCY	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CPSW_FREQUENCY							
R/W							
0h							

Table 14-11093. CPSW3_CPSW_NU_FREQUENCY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	CPSW_FREQUENCY	R/W	0h	CPSW Frequency. This is the frequency in Mhz of the VBUSP_GCLK. The frequency is rounded to the nearest Mhz. This value is used in auto speed detection for cut-thru operations.

14.7.3.1.2.69 CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register

14.7.3.1.2.69.1 CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register (Offset = 20060h) [reset = 64h]

IET Hold Count Load Value for cut thru packets

Return to Summary Table

Table 14-11094. Instance Table

Instance Name	Physical Address
CPSW0	0802 0060h + formula

Figure 14-5483. CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IET_HOLD_CNT_LD_VAL							
R/W							
64h							

Table 14-11095. CPSW3_CPSW_NU_IET_HOLD_CNT_LD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	IET_HOLD_CNT_LD_VAL	R/W	64h	Cut-thru IET Hold Count Load Value. This value is loaded into counters to count the time that cut-thru packets are allowed to prempt traffic in advance in order to reduce cut-thru latency with IET operations. This is not intended to be changed by software.

14.7.3.1.2.70 CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register

14.7.3.1.2.70.1 CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register (Offset = 20100h) [reset = 7E8h]

Transmit Priority 0 Maximum Length

Return to Summary Table

Table 14-11096. Instance Table

Instance Name	Physical Address
CPSW0	0802 0100h + formula

Figure 14-5484. CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI0_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI0_MAXLEN							
R/W							
7E8h							

Table 14-11097. CPSW3_CPSW_NU_TX_PRI0_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI0_MAXLEN	R/W	7E8h	Transmit Priority 0 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on egress for all ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.7.3.1.2.71 CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register

14.7.3.1.2.71.1 CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register (Offset = 20104h) [reset = 7E8h]

Transmit Priority 1 Maximum Length

Return to Summary Table

Table 14-11098. Instance Table

Instance Name	Physical Address
CPSW0	0802 0104h + formula

Figure 14-5485. CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI1_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI1_MAXLEN							
R/W							
7E8h							

Table 14-11099. CPSW3_CPSW_NU_TX_PRI1_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI1_MAXLEN	R/W	7E8h	Transmit Priority 1 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.7.3.1.2.72 CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register

14.7.3.1.2.72.1 CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register (Offset = 20108h) [reset = 7E8h]

Transmit Priority 2 Maximum Length

Return to Summary Table

Table 14-11100. Instance Table

Instance Name	Physical Address
CPSW0	0802 0108h + formula

Figure 14-5486. CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI2_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI2_MAXLEN							
R/W							
7E8h							

Table 14-11101. CPSW3_CPSW_NU_TX_PRI2_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI2_MAXLEN	R/W	7E8h	Transmit Priority 2 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.7.3.1.2.73 CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register

14.7.3.1.2.73.1 CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register (Offset = 2010Ch) [reset = 7E8h]

Transmit Priority 3 Maximum Length

Return to Summary Table

Table 14-11102. Instance Table

Instance Name	Physical Address
CPSW0	0802 010Ch + formula

Figure 14-5487. CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI3_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI3_MAXLEN							
R/W							
7E8h							

Table 14-11103. CPSW3_CPSW_NU_TX_PRI3_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI3_MAXLEN	R/W	7E8h	Transmit Priority 3 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.7.3.1.2.74 CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register

14.7.3.1.2.74.1 CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register (Offset = 20110h) [reset = 7E8h]

Transmit Priority 4 Maximum Length

Return to Summary Table

Table 14-11104. Instance Table

Instance Name	Physical Address
CPSW0	0802 0110h + formula

Figure 14-5488. CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI4_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI4_MAXLEN							
R/W							
7E8h							

Table 14-11105. CPSW3_CPSW_NU_TX_PRI4_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI4_MAXLEN	R/W	7E8h	Transmit Priority 4 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.7.3.1.2.75 CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register

14.7.3.1.2.75.1 CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register (Offset = 20114h) [reset = 7E8h]

Transmit Priority 5 Maximum Length

Return to Summary Table

Table 14-11106. Instance Table

Instance Name	Physical Address
CPSW0	0802 0114h + formula

Figure 14-5489. CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		TX_PRI5_MAXLEN					
NONE		R/W					
0h		7E8h					
7	6	5	4	3	2	1	0
TX_PRI5_MAXLEN							
R/W							
7E8h							

Table 14-11107. CPSW3_CPSW_NU_TX_PRI5_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI5_MAXLEN	R/W	7E8h	Transmit Priority 5 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.7.3.1.2.76 CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register

14.7.3.1.2.76.1 CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register (Offset = 20118h) [reset = 7E8h]

Transmit Priority 6 Maximum Length

Return to Summary Table

Table 14-11108. Instance Table

Instance Name	Physical Address
CPSW0	0802 0118h + formula

Figure 14-5490. CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI6_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI6_MAXLEN							
R/W							
7E8h							

Table 14-11109. CPSW3_CPSW_NU_TX_PRI6_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI6_MAXLEN	R/W	7E8h	Transmit Priority 6 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.7.3.1.2.77 CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register

14.7.3.1.2.77.1 CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register (Offset = 2011Ch) [reset = 7E8h]

Transmit Priority 7 Maximum Length

Return to Summary Table

Table 14-11110. Instance Table

Instance Name	Physical Address
CPSW0	0802 011Ch + formula

Figure 14-5491. CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TX_PRI7_MAXLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">7E8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_PRI7_MAXLEN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E8h</td></tr>
</table>

Table 14-11111. CPSW3_CPSW_NU_TX_PRI7_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI7_MAXLEN	R/W	7E8h	Transmit Priority 7 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

14.7.3.1.2.78 CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_J Register

14.7.3.1.2.78.1 CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_J Register (Offset = F80h) [reset = 0h]

MDIO User Access Register

Return to Summary Table

Table 14-11112. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F80h + formula

Figure 14-5492. CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>GO</td><td>WRITE</td><td>ACK</td><td colspan="3">RESERVED</td><td colspan="2">REGADR</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="3">NONE</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">REGADR</td><td colspan="5">PHYADR</td></tr>
<tr><td colspan="3">R/W</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11113. CPSW3_MDIO_USER_GROUP_USER_ACCESS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go. Writing a 1h to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0h to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1h. If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1h causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28:26	RESERVED	NONE	0h	Reserved
25:21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.
20:16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.
15:0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

14.7.3.1.2.79 CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Register

14.7.3.1.2.79.1 CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Register (Offset = F84h) [reset = 0h]

MDIO User PHY Select Register

Return to Summary Table

Table 14-11114. Instance Table

Instance Name	Physical Address
CPSW0	0800 0F84h + formula

Figure 14-5493. CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W	R/W	NONE	R/W				
0h	0h	0h	0h				

Table 14-11115. CPSW3_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select. Set to 1h to determine link status using the MLINK pin. Default value is 0h which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1h to enable link change status interrupts for PHY address specified in [4-0] PHYADR_MON. Link change interrupts are disabled if this bit is set to 0h.
5	RESERVED	NONE	0h	Reserved
4:0	PHYADR_MON	R/W	0h	PHY address whose link status is monitored.

14.7.3.1.2.80 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register

14.7.3.1.2.80.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register (Offset = 21004h) [reset = 0h]

CPPI Port 0 Control

Return to Summary Table

Table 14-11116. Instance Table

Instance Name	Physical Address
CPSW0	0802 1004h + formula

Figure 14-5494. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CUT_THRU_MODE_ETH	RX_REMAP_DSCP_V6	RX_REMAP_DSCP_V4	RX_REMAP_VLAN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
7	6	5	4	3	2	1	0
RESERVED			RXTX_CHKSUM_EN	RESERVED	DSCP_IPV6_EN	DSCP_IPV4_EN	RX_CHECKSUM_EN
NONE			R/W	NONE	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-11117. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	CUT_THRU_MODE_ETH	R/W	0h	Port 0 Cut-Thru Mode. Packets always egress from the host port (CPPI egress) store-and- forward regardless of this bit setting. This bit determines how a receive port operates when the host port is in a cut-thru packet destination mask. 0h Force packets with the host port in the destination mask to be store-and-forward to all destination ports. 1h The host port operates similar to Ethernet ports. A cut-thru packet with the host in the destination mask will not force the packet to be store-and-forward unless the cut-thru packet is held off due to word counts or because another cut-thru packet on the host port priority.
18	RX_REMAP_DSCP_V6	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
17	RX_REMAP_DSCP_V4	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
16	RX_REMAP_VLAN	R/W	0h	Port 0 receive remap thread to VLAN.
15	RX_ECC_ERR_EN	R/W	0h	Port 0 receive ECC Error Enable. This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port 0 transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations

Table 14-11117. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:5	RESERVED	NONE	0h	Reserved
4	RXTX_CHKSUM_EN	R/W	0h	Port 0 Multihost Port0 Rx to TX Checksum Enable
3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	Port 0 IPv6 DSCP enable 0h IPV6 DSCP priority mapping is disabled 1h IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	Port 0 IPV4 DSCP enable 0h IPV4 DSCP priority mapping is disabled 1h IPV4 DSCP priority mapping is enabled
0	RX_CHECKSUM_EN	R/W	0h	Port 0 Receive (port 0 ingress) Checksum Enable 0h Port 0 receive checksum is disabled 1h Port 0 receive checksum is enabled

14.7.3.1.2.81 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register

14.7.3.1.2.81.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register (Offset = 21008h) [reset = 0h]

CPPI Port 0 Flow ID Offset

Return to Summary Table

Table 14-11118. Instance Table

Instance Name	Physical Address
CPSW0	0802 1008h + formula

Figure 14-5495. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">VALUE</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11119. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FLOW_ID_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	VALUE	R/W	0h	This value is added to the thread/Flow_ID in CPPI transmit PSI Info Word 0

14.7.3.1.2.82 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register

14.7.3.1.2.82.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register (Offset = 21010h) [reset = 1h]

CPPI Port 0 FIFO Block Usage Count

Return to Summary Table

Table 14-11120. Instance Table

Instance Name	Physical Address
CPSW0	0802 1010h + formula

Figure 14-5496. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TX_BLK_CNT</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RX_BLK_CNT</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-11121. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Port 0 Transmit Block Count Usage. This value is the number of blocks allocated to the FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT	R	1h	Port 0 Receive Block Count Usage. This value is the number of blocks allocated in the receive FIFO.

14.7.3.1.2.83 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register

14.7.3.1.2.83.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register (Offset = 21014h) [reset = 0h]

CPPI Port 0 VLAN

Return to Summary Table

Table 14-11122. Instance Table

Instance Name	Physical Address
CPSW0	0802 1014h + formula

Figure 14-5497. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">PORT_PRI</td><td>PORT_CFI</td><td colspan="4">PORT_VID</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PORT_VID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11123. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.7.3.1.2.84 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register

14.7.3.1.2.84.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register (Offset = 21018h) [reset = 76543210h]

CPPI Port 0 Tx Header Pri to Switch Pri Mapping

Return to Summary Table

Table 14-11124. Instance Table

Instance Name	Physical Address
CPSW0	0802 1018h + formula

Figure 14-5498. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-11125. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.

Table 14-11125. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.7.3.1.2.85 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register

14.7.3.1.2.85.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register (Offset = 2101Ch) [reset = 0h]

CPPI Port 0 Priority Control

Return to Summary Table

Table 14-11126. Instance Table

Instance Name	Physical Address
CPSW0	0802 101Ch + formula

Figure 14-5499. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>RX_PTYPE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11127. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority).
15:9	RESERVED	NONE	0h	Reserved

8	RX_PTYPE	R/W	0h	Receive Priority Type
				`0h` `Fixed priority`
				`1h` `Round Robin priority`

7:0	RESERVED	NONE	0h	Reserved

14.7.3.1.2.86 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register

14.7.3.1.2.86.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register (Offset = 21020h) [reset = 76543210h]

CPPI Port 0 RX Pkt Pri to Header Pri Map

Return to Summary Table

Table 14-11128. Instance Table

Instance Name	Physical Address
CPSW0	0802 1020h + formula

Figure 14-5500. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-11129. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.

Table 14-11129. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.7.3.1.2.87 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register

14.7.3.1.2.87.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register (Offset = 21024h) [reset = 5EEh]

CPPI Port 0 Receive Frame Max Length

Return to Summary Table

Table 14-11130. Instance Table

Instance Name	Physical Address
CPSW0	0802 1024h + formula

Figure 14-5501. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		RX_MAXLEN					
NONE		R/W					
0h		5EEh					
7	6	5	4	3	2	1	0
RX_MAXLEN							
R/W							
5EEh							

Table 14-11131. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_P0_RX_MAXLEN_REG are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN) when fifo_blk_size = 4. When fifo_blk_size = 1 the maximum value is 2024 (including VLAN).

14.7.3.1.2.88 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register

14.7.3.1.2.88.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register (Offset = 21028h) [reset = 1245678h]

CPPI Port 0 Transmit Block Sub Per Priority

Return to Summary Table

Table 14-11132. Instance Table

Instance Name	Physical Address
CPSW0	0802 1028h + formula

Figure 14-5502. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-11133. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 7 frames (value 0 means use all).
27:24	PRI6	R/W	1h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 6 frames (value 0 means use all).
23:20	PRI5	R/W	2h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 5 frames (value 0 means use all).
19:16	PRI4	R/W	4h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 4 frames (value 0 means use all).
15:12	PRI3	R/W	5h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 3 frames (value 0 means use all).
11:8	PRI2	R/W	6h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 2 frames (value 0 means use all).
7:4	PRI1	R/W	7h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 1 frames (value 0 means use all).

Table 14-11133. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_BLKS_PRI_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PRI0	R/W	8h	Number of transmit 1kB blocks (defined in TX_MAX_BLKS field of CPSW_PN_MAX_BLKS_REG_k) from TX port buffer to not use for priority 0 frames (value 0 means use all).

14.7.3.1.2.89 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register

14.7.3.1.2.89.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register (Offset = 21030h) [reset = 0h]

Port 0 EEE Idle to LPI counter

Return to Summary Table

Table 14-11134. Instance Table

Instance Name	Physical Address
CPSW0	0802 1030h + formula

Figure 14-5503. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11135. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Port 0 EEE Idle to LPI counter load value

14.7.3.1.2.90 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register

14.7.3.1.2.90.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register (Offset = 21034h) [reset = 0h]

Port 0 EEE LPI to wake counter

Return to Summary Table

Table 14-11136. Instance Table

Instance Name	Physical Address
CPSW0	0802 1034h + formula

Figure 14-5504. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11137. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Port 0 EEE LPI to wake counter load value

14.7.3.1.2.91 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register

14.7.3.1.2.91.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register (Offset = 21038h) [reset = 60h]

Port 0 EEE status

Return to Summary Table

Table 14-11138. Instance Table

Instance Name	Physical Address
CPSW0	0802 1038h + formula

Figure 14-5505. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 14-11139. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	CPPI port 0 transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	CPPI port 0 receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	CPPI port 0 transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	CPPI port 0 transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	CPPI port 0 transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	0h	CPPI port 0 receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.7.3.1.2.92 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register

14.7.3.1.2.92.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register (Offset = 21050h) [reset = 0h]

Port 0 FIFO Status

Return to Summary Table

Table 14-11140. Instance Table

Instance Name	Physical Address
CPSW0	0802 1050h + formula

Figure 14-5506. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_PRI_ACTIVE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11141. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_PRI_ACTIVE	R	0h	Port 0 Transmit FIFO Priority Active. Each bit indicates whether the corresponding FIFO priority has one or more queued packets on it or not. Note: For N=2 this field is always zero (there is no transmit FIFO).

14.7.3.1.2.93 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_MAX_BLKS_REG Register

14.7.3.1.2.93.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_MAX_BLKS_REG Register (Offset = 21080h) [reset = 1004h]

Port 0 FIFO Max Blocks

Return to Summary Table

Table 14-11142. Instance Table

Instance Name	Physical Address
CPSW0	0802 1080h + formula

Figure 14-5507. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_MAX_BLKS							
R/W							
10h							
7	6	5	4	3	2	1	0
RX_MAX_BLKS							
R/W							
4h							

Table 14-11143. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit FIFO maximum blocks
7:0	RX_MAX_BLKS	R/W	4h	Receive FIFO maximum blocks

14.7.3.1.2.94 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_J Register

14.7.3.1.2.94.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_J Register (Offset = 21120h) [reset = 0h]

CPPI Port 0 Receive IPV4/IPV6 DSCP Map N

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Table 14-11144. Instance Table

Instance Name	Physical Address
CPSW0	0802 1120h + formula

Figure 14-5508. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-11145. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved

Table 14-11145. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.7.3.1.2.95 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_J Register

14.7.3.1.2.95.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_J Register (Offset = 21140h) [reset = 0h]

CPPI Port 0 Rx Priority P Committed Information Rate

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Table 14-11146. Instance Table

Instance Name	Physical Address
CPSW0	0802 1140h + formula

Figure 14-5509. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_CIR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_CIR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_CIR							
R/W							
0h							

Table 14-11147. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N Committed Information Rate Count Value

14.7.3.1.2.96 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_J Register

14.7.3.1.2.96.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_J Register (Offset = 21160h) [reset = 0h]

CPPI Port 0 Rx Priority P Excess Information Rate

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Table 14-11148. Instance Table

Instance Name	Physical Address
CPSW0	0802 1160h + formula

Figure 14-5510. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 14-11149. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N EIR

14.7.3.1.2.97 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register

14.7.3.1.2.97.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register (Offset = 21180h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Destination Threshold Set Low

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Table 14-11150. Instance Table

Instance Name	Physical Address
CPSW0	0802 1180h + formula

Figure 14-5511. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-11151. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.7.3.1.2.98 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register

14.7.3.1.2.98.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register (Offset = 21184h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Destination Threshold Set High

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Table 14-11152. Instance Table

Instance Name	Physical Address
CPSW0	0802 1184h + formula

Figure 14-5512. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-11153. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.7.3.1.2.99 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register

14.7.3.1.2.99.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register (Offset = 21188h) [reset = 0h]

CPPI Port 0 Tx PFC Destination Threshold Clr Low

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Table 14-11154. Instance Table

Instance Name	Physical Address
CPSW0	0802 1188h + formula

Figure 14-5513. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-11155. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.7.3.1.2.100 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register

14.7.3.1.2.100.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register (Offset = 2118Ch) [reset = 0h]

CPPI Port 0 Tx PFC Destination Threshold Clr High

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Table 14-11156. Instance Table

Instance Name	Physical Address
CPSW0	0802 118Ch + formula

Figure 14-5514. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-11157. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.7.3.1.2.101 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register

14.7.3.1.2.101.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 21190h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Global Buffer Threshold Set Low

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Table 14-11158. Instance Table

Instance Name	Physical Address
CPSW0	0802 1190h + formula

Figure 14-5515. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-11159. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.7.3.1.2.102 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register

14.7.3.1.2.102.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 21194h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Global Buffer Threshold Set High

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Table 14-11160. Instance Table

Instance Name	Physical Address
CPSW0	0802 1194h + formula

Figure 14-5516. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-11161. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.7.3.1.2.103 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register

14.7.3.1.2.103.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 21198h) [reset = 0h]

CPPI Port 0 Tx PFC Global Buffer Threshold Clr Low

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Table 14-11162. Instance Table

Instance Name	Physical Address
CPSW0	0802 1198h + formula

Figure 14-5517. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-11163. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.7.3.1.2.104 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register

14.7.3.1.2.104.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2119Ch) [reset = 0h]

CPPI Port 0 Tx PFC Global Buffer Threshold Clr High

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Table 14-11164. Instance Table

Instance Name	Physical Address
CPSW0	0802 119Ch + formula

Figure 14-5518. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-11165. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.7.3.1.2.105 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register

14.7.3.1.2.105.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register (Offset = 21300h) [reset = 4030201h]

CPPI Port 0 CPPI Source ID A

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Table 14-11166. Instance Table

Instance Name	Physical Address
CPSW0	0802 1300h + formula

Figure 14-5519. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Name Register

31	30	29	28	27	26	25	24
PORT4							
R/W							
4h							
23	22	21	20	19	18	17	16
PORT3							
R/W							
3h							
15	14	13	12	11	10	9	8
PORT2							
R/W							
2h							
7	6	5	4	3	2	1	0
PORT1							
R/W							
1h							

Table 14-11167. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT4	R/W	4h	Port 4 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 4.
23:16	PORT3	R/W	3h	Port 3 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 3.
15:8	PORT2	R/W	2h	Port 2 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 2.
7:0	PORT1	R/W	1h	Port 1 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 1.

14.7.3.1.2.106 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register

14.7.3.1.2.106.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register (Offset = 21304h) [reset = 8070605h]

CPPI Port 0 CPPI Source ID B

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Table 14-11168. Instance Table

Instance Name	Physical Address
CPSW0	0802 1304h + formula

Figure 14-5520. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Name Register

31	30	29	28	27	26	25	24
PORT8							
R/W							
8h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PORT7							
R/W							
7h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PORT6							
R/W							
6h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PORT5							
R/W							
5h							

Table 14-11169. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_SRC_ID_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT8	R/W	8h	Port 8 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 8.
23:16	PORT7	R/W	7h	Port 7 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 7.
15:8	PORT6	R/W	6h	Port 6 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 6.
7:0	PORT5	R/W	5h	Port 5 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 5.

14.7.3.1.2.107 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register

14.7.3.1.2.107.1 CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register (Offset = 21320h) [reset = 0h]

CPPI Port 0 Host Blocks Priority

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Table 14-11170. Instance Table

Instance Name	Physical Address
CPSW0	0802 1320h + formula

Figure 14-5521. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI5				PRI4			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI3				PRI2			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI1				PRI0			
R/W				R/W			
0h				0h			

Table 14-11171. CPSW3_CPSW_NU_CPSW_NU_CPPI_P0_HOST_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Host Blocks
27:24	PRI6	R/W	0h	Priority 6 Host Blocks
23:20	PRI5	R/W	0h	Priority 5 Host Blocks
19:16	PRI4	R/W	0h	Priority 4 Host Blocks
15:12	PRI3	R/W	0h	Priority 3 Host Blocks
11:8	PRI2	R/W	0h	Priority 2 Host Blocks
7:4	PRI1	R/W	0h	Priority 1 Host Blocks
3:0	PRI0	R/W	0h	Priority 0 Host Blocks

14.7.3.1.2.108 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register

14.7.3.1.2.108.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register (Offset = 22000h) [reset = 0h]

Reserved

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Table 14-11172. Instance Table

Instance Name	Physical Address
CPSW0	0802 2000h + formula

Figure 14-5522. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-11173. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved register for memory map alignment

14.7.3.1.2.109 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register

14.7.3.1.2.109.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register (Offset = 22004h) [reset = 0h]

Enet Port N Control

Return to Summary Table

Table 14-11174. Instance Table

Instance Name	Physical Address
CPSW0	0802 2004h + formula

Figure 14-5523. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						EST_PORT_EN	IET_PORT_EN
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	TX_CUT_IET_HOLD_DIS	TX_LPI_CLKSTOP_EN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
NONE					R/W	R/W	NONE
0h					0h	0h	0h

Table 14-11175. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable. 0h EST is disabled on the port 1h EST is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
16	IET_PORT_EN	R/W	0h	Interspersed Express Traffic (IET) Port Enable. 0h IET is disabled on the port 1h IET is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
15	RX_ECC_ERR_EN	R/W	0h	Port N receive ECC Error Enable. This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port N transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations
13	TX_CUT_IET_HOLD_DIS	R/W	0h	Port N transmit IET hold due to cut-thru disable 0h Cut-thru packets to the port will cause premptable traffic to be prempted as early as possible minimizing cut-thru latency 1h Cut-thru packets to the port will be prempted as usual by the express MAC

Table 14-11175. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable. When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11:3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	IPV6 DSCP enable 0h `IPV6 DSCP priority mapping is disabled` 1h `IPV6 DSCP priority mapping is enabled`
1	DSCP_IPV4_EN	R/W	0h	IPV4 DSCP enable 0h `IPV4 DSCP priority mapping is disabled` 1h `IPV4 DSCP priority mapping is enabled`
0	RESERVED	NONE	0h	Reserved

14.7.3.1.2.110 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register

14.7.3.1.2.110.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register (Offset = 22008h) [reset = 1004h]

Enet Port N FIFO Max Blocks

Return to Summary Table

Table 14-11176. Instance Table

Instance Name	Physical Address
CPSW0	0802 2008h + formula

Figure 14-5524. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_MAX_BLKS							
R/W							
10h							
7	6	5	4	3	2	1	0
RX_MAX_BLKS							
R/W							
4h							

Table 14-11177. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit Max Blocks. The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive, when Fullduplex flow control is enabled (CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX = 1h) to allow for flow control runout.
7:0	RX_MAX_BLKS	R/W	4h	Receive Max Blocks. The maximum number of blocks allowed on the express and prempt receive FIFOs (transmit and receive FIFO's combined when fifo_oneram = 1)

14.7.3.1.2.111 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register

14.7.3.1.2.111.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register (Offset = 22010h) [reset = 1h]

Enet Port N FIFO Block Usage Count

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Table 14-11178. Instance Table

Instance Name	Physical Address
CPSW0	0802 2010h + formula

Figure 14-5525. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RX_BLK_CNT_P</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">TX_BLK_CNT</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">RX_BLK_CNT_E</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-11179. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO prempt receive queue. No blocks are allocated until the CPSW_CONTROL_REG[17] IET_ENABLE is set.
15:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage. This value is the number of blocks allocated to the port's FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO express receive queue.

14.7.3.1.2.112 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register

14.7.3.1.2.112.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register (Offset = 22014h) [reset = 0h]

Enet Port N VLAN

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Table 14-11180. Instance Table

Instance Name	Physical Address
CPSW0	0802 2014h + formula

Figure 14-5526. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W			R/W	R/W			
0h			0h	0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W							
0h							

Table 14-11181. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.7.3.1.2.113 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register

14.7.3.1.2.113.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register (Offset = 22018h) [reset = 76543210h]

Enet Port N Tx Header Pri to Switch Pri Mapping

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Table 14-11182. Instance Table

Instance Name	Physical Address
CPSW0	0802 2018h + formula

Figure 14-5527. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-11183. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	NONE	0h	Reserved

Table 14-11183. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.7.3.1.2.114 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register

14.7.3.1.2.114.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register (Offset = 2201Ch) [reset = 9000h]

Enet Port N Priority Control

Return to Summary Table

Table 14-11184. Instance Table

Instance Name	Physical Address
CPSW0	0802 201Ch + formula

Figure 14-5528. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">TX_HOST_BLKS_REM</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11185. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE	0h	Reserved

14.7.3.1.2.115 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register

14.7.3.1.2.115.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register (Offset = 22020h) [reset = 76543210h]

Enet Port N RX Pkt Pri to Header Pri Map

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Table 14-11186. Instance Table

Instance Name	Physical Address
CPSW0	0802 2020h + formula

Figure 14-5529. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-11187. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	NONE	0h	Reserved

Table 14-11187. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.7.3.1.2.116 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register

14.7.3.1.2.116.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register (Offset = 22024h) [reset = 5EEh]

Enet Port N Receive Frame Max Length

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Table 14-11188. Instance Table

Instance Name	Physical Address
CPSW0	0802 2024h + formula

Figure 14-5530. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		RX_MAXLEN					
NONE		R/W					
0h		5EEh					
7	6	5	4	3	2	1	0
RX_MAXLEN							
R/W							
5EEh							

Table 14-11189. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).

14.7.3.1.2.117 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register

14.7.3.1.2.117.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register (Offset = 22028h) [reset = 1245678h]

Enet Port N Transmit Block Sub Per Priority

Return to Summary Table

Table 14-11190. Instance Table

Instance Name	Physical Address
CPSW0	0802 2028h + formula

Figure 14-5531. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-11191. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

14.7.3.1.2.118 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register

14.7.3.1.2.118.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register (Offset = 22030h) [reset = 0h]

Enet Port N EEE Idle to LPI counter

Return to Summary Table

Table 14-11192. Instance Table

Instance Name	Physical Address
CPSW0	0802 2030h + formula

Figure 14-5532. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11193. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value

14.7.3.1.2.119 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register

14.7.3.1.2.119.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register (Offset = 22034h) [reset = 0h]

Enet Port N EEE LPI to wake counter

Return to Summary Table

Table 14-11194. Instance Table

Instance Name	Physical Address
CPSW0	0802 2034h + formula

Figure 14-5533. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11195. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value

14.7.3.1.2.120 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register

14.7.3.1.2.120.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register (Offset = 22038h) [reset = 62h]

Enet Port N EEE status

Return to Summary Table

Table 14-11196. Instance Table

Instance Name	Physical Address
CPSW0	0802 2038h + formula

Figure 14-5534. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	1h	0h

Table 14-11197. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.7.3.1.2.121 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register

14.7.3.1.2.121.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register (Offset = 22040h) [reset = 8h]

Enet Port N IET Control

Return to Summary Table

Table 14-11198. Instance Table

Instance Name	Physical Address
CPSW0	0802 2040h + formula

Figure 14-5535. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_PREMPT							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					MAC_ADDFRAGSIZE		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED				MAC_LINKFAIL	MAC_DISABLEVERIFY	MAC_HOLD	MAC_PENABLE
NONE				R/W	R/W	R/W	R/W
0h				1h	0h	0h	0h

Table 14-11199. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAC_PREMPT	R/W	0h	Mac Preempt Queue - Indicates which transmit FIFO queues are sent to the preempt MAC. Bit 0 indicates queue zero, bit 1 queue 1 and so on. Packets will be sent to the preempt MAC only when MAC_PENABLE is set, and when MAC_VERIFIED (from CPSW_PN_IET_STATUS_REG_k) or MAC_DISABLEVERIFY is set, and when IET_PORT_EN is set.
15:11	RESERVED	NONE	0h	Reserved
10:8	MAC_ADDFRAGSIZE	R/W	0h	Mac Fragment Size - An integer in the range 0:7 indicating, as a multiple of 64, the minimum additional length for nonfinal mPackets. 0 64 1 128 2 81 3 256 4 320 5 384 6 448 7 512
7:4	RESERVED	NONE	0h	Reserved
3	MAC_LINKFAIL	R/W	1h	Mac Link Fail - Link Fail Indicator to reset the verify state machine. This bit is reset high. Verify and response frames will be sent/allowed when this bit is cleared.

Table 14-11199. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MAC_DISABLEVERIFY	R/W	0h	Mac Disable Verify - Disables verification on the port when set. If this bit is set then packets will be sent to the preempt Mac when MAC_PENABLE is set (This is a forced mode with no IET verification).
1	MAC_HOLD	R/W	0h	Mac Hold - Hold Preemption on the port.
0	MAC_PENABLE	R/W	0h	Mac Preemption Enable - Port Preemption Enable. This takes effect only when IET_PORT_EN is set.

14.7.3.1.2.122 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register

14.7.3.1.2.122.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register (Offset = 22044h) [reset = 0h]

Enet Port N IET Status

Return to Summary Table

Table 14-11200. Instance Table

Instance Name	Physical Address
CPSW0	0802 2044h + formula

Figure 14-5536. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MAC_VERIFY_ERR	MAC_RESPOND_ERR	MAC_VERIFY_FAIL	MAC_VERIFIED
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-11201. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MAC_VERIFY_ERR	R	0h	Mac Received Verify Packet with Errors - Set when a verify packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
2	MAC_RESPOND_ERR	R	0h	Mac Received Respond Packet with Errors - Set when a respond packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
1	MAC_VERIFY_FAIL	R	0h	Mac Verification Failed - Indication that verification was unsuccessful.
0	MAC_VERIFIED	R	0h	Mac Verified - Indication that verification was successful.

14.7.3.1.2.123 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register

14.7.3.1.2.123.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register (Offset = 22048h) [reset = 1312D0h]

Enet Port N IET VERIFY

Return to Summary Table

Table 14-11202. Instance Table

Instance Name	Physical Address
CPSW0	0802 2048h + formula

Figure 14-5537. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
MAC_VERIFY_CNT							
R/W							
1312D0h							
15	14	13	12	11	10	9	8
MAC_VERIFY_CNT							
R/W							
1312D0h							
7	6	5	4	3	2	1	0
MAC_VERIFY_CNT							
R/W							
1312D0h							

Table 14-11203. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_IET_VERIFY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MAC_VERIFY_CNT	R/W	1312D0h	Mac Verify Timeout Count - The number of wireside clocks contained in the verify timeout counter. The default is 0x1312D0 (10ms at 125MHz in gig mode).

14.7.3.1.2.124 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register

14.7.3.1.2.124.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register (Offset = 22050h) [reset = FF00h]

Enet Port N FIFO STATUS

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Table 14-11204. Instance Table

Instance Name	Physical Address
CPSW0	0802 2050h + formula

Figure 14-5538. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED</td><td>EST_BUFACT</td><td>EST_ADD_ERR</td><td>EST_CNT_ERR</td></tr>
<tr><td colspan="5">NONE</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TX_E_MAC_ALLOW</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_PRI_ACTIVE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11205. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	EST_BUFACT	R	0h	EST RAM active buffer. Indicates the active 64-word fetch buffer when CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared to zero. Indicates the fetch RAM address MSB when bit [0] EST_ONEBUF is set to one.
17	EST_ADD_ERR	R	0h	EST Address Error. Indicates that the fetch RAM was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error. Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15:8	TX_E_MAC_ALLOW	R	FFh	EST transmit MAC allow. Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the prempt queue).
7:0	TX_PRI_ACTIVE	R	0h	EST Transmit Priority Active. Bus that indicates which priorities have packets (non-empty) at the time of the register read.

14.7.3.1.2.125 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register

14.7.3.1.2.125.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register (Offset = 22060h) [reset = 0h]

Enet Port N EST CONTROL

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Table 14-11206. Instance Table

Instance Name	Physical Address
CPSW0	0802 2060h + formula

Figure 14-5539. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED						EST_FILL_MARGIN	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
EST_FILL_MARGIN							
R/W							
0h							
15	14	13	12	11	10	9	8
EST_PREMPT_COMP							EST_FILL_EN
R/W							R/W
0h							0h
7	6	5	4	3	2	1	0
EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-11207. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin. Sets the fill margin required to ensure that the Ethernet wire is clear (including IPG) so that the timed EST express packet can egress at the required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended.
15:9	EST_PREMPT_COMP	R/W	0h	EST Prempt Comparison Value. When the count in a zero allow is less than or equal to this value in bytes (times 8), prempt packets are cleared from the wire. This is the prempt clear margin value.
8	EST_FILL_EN	R/W	0h	EST Fill Enable. Enable EST fill mode.
7:5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority. Selects the express priority that timestamp(s) will be generated on when CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI bit is set.
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority. When set, timestamp only enabled packets on the express priority selected by CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI bit field. When cleared to zero, express packet selection for timestamp is independent of priority.

Table 14-11207. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_EST_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only. Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI is also set then the timestamp is generated only on the first packet on CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI).
2	EST_TS_EN	R/W	0h	EST Timestamp Enable. Enable express timestamps (when CPSW_CONTROL_REG[18] EST_ENABLE and CPSW_PN_CONTROL_REG_k[17] EST_PORT_EN bits are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select. If CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the CPSW_PN_FIFO_STATUS_REG_k register, bit [18] EST_BUFACT.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer. When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The CPSW_PN_EST_CONTROL_REG_k[1] EST_BUFSEL bit selects the buffer to be used when bit [0] EST_ONEBUF is cleared to zero.

14.7.3.1.2.126 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_J Register

14.7.3.1.2.126.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_J Register (Offset = 22120h) [reset = 0h]

Enet Port N Receive IPV4/IPV6 DSCP Map M

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Table 14-11208. Instance Table

Instance Name	Physical Address
CPSW0	0802 2120h + formula

Figure 14-5540. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-11209. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved

Table 14-11209. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.7.3.1.2.127 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_J Register

14.7.3.1.2.127.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_J Register (Offset = 22140h) [reset = 0h]

Enet Port N Rx Priority P Committed Information Rate Value

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Table 14-11210. Instance Table

Instance Name	Physical Address
CPSW0	0802 2140h + formula

Figure 14-5541. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_CIR							
R/W							
0h							

Table 14-11211. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

14.7.3.1.2.128 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_J Register

14.7.3.1.2.128.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_J Register (Offset = 22160h) [reset = 0h]

Enet Port N Rx Priority P Excess Informatoin Rate Value

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Table 14-11212. Instance Table

Instance Name	Physical Address
CPSW0	0802 2160h + formula

Figure 14-5542. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 14-11213. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

14.7.3.1.2.129 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register

14.7.3.1.2.129.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register (Offset = 22180h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set Low

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Table 14-11214. Instance Table

Instance Name	Physical Address
CPSW0	0802 2180h + formula

Figure 14-5543. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-11215. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.7.3.1.2.130 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register

14.7.3.1.2.130.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register (Offset = 22184h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set High

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Table 14-11216. Instance Table

Instance Name	Physical Address
CPSW0	0802 2184h + formula

Figure 14-5544. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-11217. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.7.3.1.2.131 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register

14.7.3.1.2.131.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 22188h) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr Low

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Table 14-11218. Instance Table

Instance Name	**Physical Address**
CPSW0	0802 2188h + formula

Figure 14-5545. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-11219. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.7.3.1.2.132 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register

14.7.3.1.2.132.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 2218Ch) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr High

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Table 14-11220. Instance Table

Instance Name	Physical Address
CPSW0	0802 218Ch + formula

Figure 14-5546. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-11221. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.7.3.1.2.133 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register

14.7.3.1.2.133.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 22190h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set Low

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Table 14-11222. Instance Table

Instance Name	Physical Address
CPSW0	0802 2190h + formula

Figure 14-5547. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-11223. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.7.3.1.2.134 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register

14.7.3.1.2.134.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 22194h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set High

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Table 14-11224. Instance Table

Instance Name	Physical Address
CPSW0	0802 2194h + formula

Figure 14-5548. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-11225. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.7.3.1.2.135 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register

14.7.3.1.2.135.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 22198h) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr Low

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Table 14-11226. Instance Table

Instance Name	Physical Address
CPSW0	0802 2198h + formula

Figure 14-5549. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-11227. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.7.3.1.2.136 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register

14.7.3.1.2.136.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2219Ch) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr High

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Table 14-11228. Instance Table

Instance Name	Physical Address
CPSW0	0802 219Ch + formula

Figure 14-5550. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-11229. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.7.3.1.2.137 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register

14.7.3.1.2.137.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 22300h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values Low

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Table 14-11230. Instance Table

Instance Name	Physical Address
CPSW0	0802 2300h + formula

Figure 14-5551. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-11231. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

14.7.3.1.2.138 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register

14.7.3.1.2.138.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 22304h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values High

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Table 14-11232. Instance Table

Instance Name	Physical Address
CPSW0	0802 2304h + formula

Figure 14-5552. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-11233. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

14.7.3.1.2.139 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register

14.7.3.1.2.139.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register (Offset = 22308h) [reset = 0h]

Enet Port N Tx Pause Frame Source Address Low

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Table 14-11234. Instance Table

Instance Name	Physical Address
CPSW0	0802 2308h + formula

Figure 14-5553. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_15_8							
R/W							
0h							

Table 14-11235. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

14.7.3.1.2.140 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register

14.7.3.1.2.140.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register (Offset = 2230Ch) [reset = 0h]

Enet Port N Tx Pause Frame Source Address High

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Table 14-11236. Instance Table

Instance Name	Physical Address
CPSW0	0802 230Ch + formula

Figure 14-5554. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24
MACSRCADDR_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
MACSRCADDR_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_47_40							
R/W							
0h							

Table 14-11237. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

14.7.3.1.2.141 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register

14.7.3.1.2.141.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register (Offset = 22310h) [reset = 0h]

Enet Port N Time Sync Control

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Table 14-11238. Instance Table

Instance Name	Physical Address
CPSW0	0802 2310h + formula

Figure 14-5555. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_MSG_TYPE_EN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11239. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
15:12	RESERVED	NONE	0h	Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable

Table 14-11239. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

14.7.3.1.2.142 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register

14.7.3.1.2.142.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register (Offset = 22314h) [reset = 1E0000h]

Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

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Table 14-11240. Instance Table

Instance Name	Physical Address
CPSW0	0802 2314h + formula

Figure 14-5556. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		TS_SEQ_ID_OFFSET					
NONE		R/W					
0h		1Eh					
15	14	13	12	11	10	9	8
TS_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LTYPE1							
R/W							
0h							

Table 14-11241. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6h.
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1. This is the port's time sync LTYPE1 value.

14.7.3.1.2.143 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register

14.7.3.1.2.143.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register (Offset = 22318h) [reset = 0h]

Enet Port N Time Sync VLAN2 and VLAN2

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Table 14-11242. Instance Table

Instance Name	Physical Address
CPSW0	0802 2318h + formula

Figure 14-5557. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
TS_VLAN_LTYPE2							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_VLAN_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1							
R/W							
0h							

Table 14-11243. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for the port TX and RX time sync decode.
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for the port TX and RX time sync decode.

14.7.3.1.2.144 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register

14.7.3.1.2.144.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register (Offset = 2231Ch) [reset = 0h]

Enet Port N Time Sync Control and LTYPE 2

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Table 14-11244. Instance Table

Instance Name	Physical Address
CPSW0	0802 231Ch + formula

Figure 14-5558. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TS_LTYPE2							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LTYPE2							
R/W							
0h							

Table 14-11245. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable 0h Unicast disabled 1h Unicast enabled
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable 0h TTL must be 1h 1h TTL may be any value
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable 0h Disabled 1h Destination port number (decimal) 320 is enabled
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable 0h Disabled 1h Destination port number (decimal) 319 is enabled
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.132 is enabled

Table 14-11245. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.131 is enabled
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.130 is enabled
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.129 is enabled
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable 0h Disabled 1h Destination port number (decimal) 224.0.0.107 is enabled
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2. This is the time sync LTYPE1 value for port 1.

14.7.3.1.2.145 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register

14.7.3.1.2.145.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register (Offset = 22320h) [reset = 40000h]

Enet Port N Time Sync Control 2

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Table 14-11246. Instance Table

Instance Name	Physical Address
CPSW0	0802 2320h + formula

Figure 14-5559. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		TS_DOMAIN_OFFSET					
NONE		R/W					
0h		4h					
15	14	13	12	11	10	9	8
TS_MCAST_TYPE_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_MCAST_TYPE_EN							
R/W							
0h							

Table 14-11247. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

14.7.3.1.2.146 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register

14.7.3.1.2.146.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register (Offset = 22330h) [reset = 0h]

Enet Port N Mac Control

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Table 14-11248. Instance Table

Instance Name	Physical Address
CPSW0	0802 2330h + formula

Figure 14-5560. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							RX_CMF_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED	
R/W	NONE		R/W	R/W	R/W	NONE	
0h	0h		0h	0h	0h	0h	
7	6	5	4	3	2	1	0
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11249. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved

24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the CPSW_PN_MAC_CONTROL_REG_k register, regardless of the value of [24] RX_CMF_EN bit. Frames transferred to memory due to [24] RX_CMF_EN will have the control bit set in their EOP buffer descriptor.
				`0h` `MAC control frames are filtered (but acted upon if enabled).`
				`1h` `MAC control frames are transferred to memory.`

23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable. Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to CPSW_PN_MAC_CONTROL_REG_k[23] RX_CSF_EN will have the fragment or undersized bit set in their receive footer. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors.
				`0h` `Short frames are filtered.`
				`1h` `Short frames are transferred to memory.`

Table 14-11249. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable. Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is not set. 0h Frames containing errors are filtered. 1h Frames containing errors are transferred to memory.
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable When set this bit limits the number of short gap packets transmitted to 100ppm. The TX_SHORT_GAP_ENABLE bit must also be set. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable. Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the [4] TX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG_k register.
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable. Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the CPSW_PN_MAC_CONTROL_REG_k[3] RX_FLOW_EN bit in this register.
18	EXT_EN	R/W	0h	External Control Enable. Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the [0] FULLDUPLEX and [7] GIG bits in the CPSW_PN_MAC_CONTROL_REG_k register. The [0] FULLDUPLEX bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	R/W	0h	Gigabit Mode Force. This bit is used to force the Ethernet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.
15	IFCTL_A	R/W	0h	Determines the RMII link speed. 0h 10Mbps operation 0h 100Mbps operation
14:13	RESERVED	NONE	0h	Reserved
12	CRC_TYPE	R/W	0h	Port CRC Type. 0h Ethernet CRC 1h Castagnoli CRC
11	CMD_IDLE	R/W	0h	Command Idle. 0h Idle not commanded 1h Idle Commanded (read bit [31] IDLE in CPSW_PN_MAC_STATUS_REG_k register)
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable. 0h Transmit with a short IPG is disabled 1h Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.
9:8	RESERVED	NONE	0h	Reserved
7	GIG	R/W	0h	Gigabit Mode. 0h 10/100 mode 1h Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit.
6	TX_PACE	R/W	0h	Transmit Pacing Enable 0h Transmit Pacing Disabled 1h Transmit Pacing Enabled

Table 14-11249. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GMII_EN	R/W	0h	GMII Enable. 0h GMII RX and TX held in reset. 1h GMII RX and TX released from reset.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0h Transmit Flow Control Disabled. Full-duplex mode - Incoming pause frames are not acted upon. 1h Transmit Flow Control Enabled. Full-duplex mode - Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable. 0h Receive Flow Control Disabled Half-duplex mode - No flow control generated collisions are sent. Full-duplex mode - No outgoing pause frames are sent. 1h Receive Flow Control Enabled Half-duplex mode - Collisions are initiated when receive flow control is triggered. Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode. This bit must be set to allow writes to the CPSW_PN_MAC_BOFFTEST_REG_k and CPSW_PN_MAC_RX_PAUSETIMER_REG_k registers.
1	LOOPBACK	R/W	0h	Loop Back Mode. Loopback mode forces internal fullduplex mode regardless of whether the CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX bit is set or not. The [1] LOOPBACK bit should be changed only when [5] GMII_EN is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS). 0h Not looped back mode 1h Loop Back mode enabled
0	FULLDUPLEX	R/W	0h	Full Duplex mode. Gigabit mode forces fullduplex mode regardless of whether the [0] FULLDUPLEX bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit 0h Half duplex mode 1h Full duplex mode

14.7.3.1.2.147 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register

14.7.3.1.2.147.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register (Offset = 22334h) [reset = F0000000h]

Enet Port N Mac Status

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Table 14-11250. Instance Table

Instance Name	Physical Address
CPSW0	0802 2334h + formula

Figure 14-5561. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	P_IDLE	MAC_TX_IDLE	TORF	TORF_PRI		
R	R	R	R	R	R		
1h	1h	1h	1h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_PFC_FLOW_ACT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_PFC_FLOW_ACT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
NONE	R	R	R	R	NONE	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11251. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description

31	IDLE	R	1h	Enet IDLE. The Ethernet port (express and prempt) are in the Idle state (valid after an Idle command)
				`0h The port is not in the Idle state.`
				`1h The port is in the Idle state.`

30	E_IDLE	R	1h	Express MAC is Idle.
29	P_IDLE	R	1h	Prempt MAC is Idle.
28	MAC_TX_IDLE	R	1h	Mac Transmit Idle. Both Prempt and Express MAC Transmit are in Idle state. The transmit clock must be running for this to go idle.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 7h to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15:8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	NONE	0h	Reserved
6	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[19] EXT_RX_FLOW_EN input bit.

Table 14-11251. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[20] EXT_TX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG. This is the value of the [4] EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Fullduplex. This is the value of the [3] EXT_FULLDUPLEX input bit.
2	RESERVED	NONE	0h	Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

14.7.3.1.2.148 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register

14.7.3.1.2.148.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register (Offset = 22338h) [reset = 0h]

Enet Port N Mac Soft Reset

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Table 14-11252. Instance Table

Instance Name	Physical Address
CPSW0	0802 2338h + formula

Figure 14-5562. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFT_RESET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-11253. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Software reset. Writing a 1h to this bit causes the Ethernet Mac logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a 1h is read, the reset has not yet occurred. If a 0h is read then reset has occurred.

14.7.3.1.2.149 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register

14.7.3.1.2.149.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register (Offset = 2233Ch) [reset = 0h]

Enet Port N Mac Backoff Test

Return to Summary Table

Table 14-11254. Instance Table

Instance Name	Physical Address
CPSW0	0802 233Ch + formula

Figure 14-5563. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
NONE	R/W					R/W	
0h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RNDNUM							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COLL_COUNT				RESERVED		TX_BACKOFF	
R				NONE		R	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_BACKOFF							
R							
0h							

Table 14-11255. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:26	PACEVAL	R/W	0h	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce 'capture' effects improving overall network bandwidth.
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when CPSW_PN_MAC_CONTROL_REG_k[2] MTEST bit has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15:12	COLL_COUNT	R	0h	Collision Count.
11:10	RESERVED	NONE	0h	Reserved

Table 14-11255. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	TX_BACKOFF	R	0h	Backoff Count. This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.

14.7.3.1.2.150 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register

14.7.3.1.2.150.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 22340h) [reset = 0h]

Enet Port N 802.3 Receive Pause Timer

Return to Summary Table

Table 14-11256. Instance Table

Instance Name	Physical Address
CPSW0	0802 2340h + formula

Figure 14-5564. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RX_PAUSETIMER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RX_PAUSETIMER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11257. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.7.3.1.2.151 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_J Register

14.7.3.1.2.151.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_J Register (Offset = 22350h) [reset = 0h]

Enet Port N PFC Priority P Rx Pause Timer

Return to Summary Table

Table 14-11258. Instance Table

Instance Name	Physical Address
CPSW0	0802 2350h + formula

Figure 14-5565. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-11259. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	Rx Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

14.7.3.1.2.152 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register

14.7.3.1.2.152.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 22370h) [reset = 0h]

Enet Port N 802.3 Tx Pause Timer

Return to Summary Table

Table 14-11260. Instance Table

Instance Name	Physical Address
CPSW0	0802 2370h + formula

Figure 14-5566. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-11261. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.7.3.1.2.153 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_J Register

14.7.3.1.2.153.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_J Register (Offset = 22380h) [reset = 0h]

Enet Port N PFC Priority P Tx Pause Timer

Return to Summary Table

Table 14-11262. Instance Table

Instance Name	Physical Address
CPSW0	0802 2380h + formula

Figure 14-5567. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-11263. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	PFC Tx 'y' Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

14.7.3.1.2.154 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register

14.7.3.1.2.154.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register (Offset = 223A0h) [reset = 0h]

Enet Port N Emulation Control

Return to Summary Table

Table 14-11264. Instance Table

Instance Name	Physical Address
CPSW0	0802 23A0h + formula

Figure 14-5568. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>SOFT</td><td>FREE</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11265. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.7.3.1.2.155 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register

14.7.3.1.2.155.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register (Offset = 223A4h) [reset = Ch]

Enet Port N Tx Inter Packet Gap

Return to Summary Table

Table 14-11266. Instance Table

Instance Name	Physical Address
CPSW0	0802 23A4h + formula

Figure 14-5569. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_GAP							
R/W							
Ch							
7	6	5	4	3	2	1	0
TX_GAP							
R/W							
Ch							

Table 14-11267. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap GMII modes - This is the default gap value and only bits [8-0] are used. This can be increased from 12 to increase the gap between packets. XGMII mode - In 10 Gigabit mode this is the short gap rate and should be changed to 5000 (1388h) to get approximately 200ppm faster when short gap is triggered and enabled.

14.7.3.1.2.156 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register

14.7.3.1.2.156.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register (Offset = 223A8h) [reset = 204h]

Enet Port N Port Configuration

Return to Summary Table

Table 14-11268. Instance Table

Instance Name	Physical Address
CPSW0	0802 23A8h + formula

Figure 14-5570. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						IET	XGMII
NONE						R	R
0h						1h	0h
7	6	5	4	3	2	1	0
INTERVLAN_ROUTES							
R							
4h							

Table 14-11269. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	IET	R	1h	Intersperced Express Traffic (IET) is supported on this port when read high.
8	XGMII	R	0h	XGMII is supported on this port when set.
7:0	INTERVLAN_ROUTES	R	4h	This is the number of InterVLAN routes supported on this port (egress).

14.7.3.1.2.157 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register

14.7.3.1.2.157.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 223ACh) [reset = 0h]

Enet Port N Tx Egress InterVLAN Operation Pointer

Return to Summary Table

Table 14-11270. Instance Table

Instance Name	Physical Address
CPSW0	0802 23ACh + formula

Figure 14-5571. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					POINTER		
NONE					R/W		
0h					0h		

Table 14-11271. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

14.7.3.1.2.158 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register

14.7.3.1.2.158.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register (Offset = 223B0h) [reset = 0h]

Enet Port N Tx Egress InterVLAN A

Return to Summary Table

Table 14-11272. Instance Table

Instance Name	Physical Address
CPSW0	0802 23B0h + formula

Figure 14-5572. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24
DA_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
DA_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_47_40							
R/W							
0h							

Table 14-11273. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16 - DA byte 4 on wire
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24 - DA byte 3 on wire
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32 - DA byte 2 on wire
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40 - DA byte 1 on wire

14.7.3.1.2.159 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register

14.7.3.1.2.159.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register (Offset = 223B4h) [reset = 0h]

Enet Port N Tx Egress InterVLAN B

Return to Summary Table

Table 14-11274. Instance Table

Instance Name	Physical Address
CPSW0	0802 23B4h + formula

Figure 14-5573. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Name Register

31	30	29	28	27	26	25	24
SA_39_32							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_47_40							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_15_8							
R/W							
0h							

Table 14-11275. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32 - SA byte 2 on wire
23:16	SA_47_40	R/W	0h	Source Address bits 47:40 - SA byte 1 on wire
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0 - DA byte 6 on wire
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8 - DA byte 5 on wire

14.7.3.1.2.160 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register

14.7.3.1.2.160.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register (Offset = 223B8h) [reset = 0h]

Enet Port N Tx Egress InterVLAN C

Return to Summary Table

Table 14-11276. Instance Table

Instance Name	Physical Address
CPSW0	0802 23B8h + formula

Figure 14-5574. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24
SA_7_0							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_15_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SA_23_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SA_31_24							
R/W							
0h							

Table 14-11277. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0 - DA byte 6 on wire
23:16	SA_15_8	R/W	0h	Source Address bits 15:8 - DA byte 5 on wire
15:8	SA_23_16	R/W	0h	Source Address bits 23:16 - DA byte 4 on wire
7:0	SA_31_24	R/W	0h	Source Address bits 31:24 - DA byte 3 on wire

14.7.3.1.2.161 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register

14.7.3.1.2.161.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register (Offset = 223BCh) [reset = 0h]

Enet Port N Tx Egress InterVLAN D

Return to Summary Table

Table 14-11278. Instance Table

Instance Name	Physical Address
CPSW0	0802 23BCh + formula

Figure 14-5575. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VID							
R/W							
0h							

Table 14-11279. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

14.7.3.1.2.162 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register

14.7.3.1.2.162.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register (Offset = 223C0h) [reset = 0h]

Enet Port N Cut Thru Priority Enable

Return to Summary Table

Table 14-11280. Instance Table

Instance Name	Physical Address
CPSW0	0802 23C0h + formula

Figure 14-5576. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PRI_CUT_THRU_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PRI_CUT_THRU_EN							
R/W							
0h							

Table 14-11281. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_CUT_THRU_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RX_PRI_CUT_THRU_EN	R/W	0h	Receive Cut Thru Priority Enable
7:0	TX_PRI_CUT_THRU_EN	R/W	0h	Transmit Cut Thru Priority Enable

14.7.3.1.2.163 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register

14.7.3.1.2.163.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register (Offset = 223C4h) [reset = 0h]

Enet Port Speed

Return to Summary Table

Table 14-11282. Instance Table

Instance Name	Physical Address
CPSW0	0802 23C4h + formula

Figure 14-5577. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED			PORT_SPEED_CHANGED	RESERVED			
NONE			R	NONE			
0h			0h	0h			
15	14	13	12	11	10	9	8
PORT_AUTO_SPEED				RESERVED			PORT_SPEED_AUTO_EN
R				NONE			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
RESERVED				PORT_SPEED_MANUAL			
NONE				R/W			
0h				0h			

Table 14-11283. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_0_PN_PORT_SPEED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	PORT_SPEED_CHANGED	R	0h	Port Speed Changed
19:16	RESERVED	NONE	0h	Reserved
15:12	PORT_AUTO_SPEED	R	0h	Detected Auto Speed
11:9	RESERVED	NONE	0h	Reserved
8	PORT_SPEED_AUTO_EN	R/W	0h	Automatic Port Speed Enable
7:4	RESERVED	NONE	0h	Reserved
3:0	PORT_SPEED_MANUAL	R/W	0h	Manual Port Speed

14.7.3.1.2.164 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register

14.7.3.1.2.164.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register (Offset = 23000h) [reset = 0h]

Reserved

Return to Summary Table

Table 14-11284. Instance Table

Instance Name	Physical Address
CPSW0	0802 3000h + formula

Figure 14-5578. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 14-11285. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	Reserved register for memory map alignment

14.7.3.1.2.165 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register

14.7.3.1.2.165.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register (Offset = 23004h) [reset = 0h]

Enet Port N Control

Return to Summary Table

Table 14-11286. Instance Table

Instance Name	Physical Address
CPSW0	0802 3004h + formula

Figure 14-5579. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED						EST_PORT_EN	IET_PORT_EN
NONE						R/W	R/W
0h						0h	0h

15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	TX_CUT_IET_HOLD_DIS	TX_LPI_CLKSTOP_EN	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			

7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
NONE					R/W	R/W	NONE
0h					0h	0h	0h

Table 14-11287. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable. 0h EST is disabled on the port 1h EST is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
16	IET_PORT_EN	R/W	0h	Intersperced Express Traffic (IET) Port Enable. 0h IET is disabled on the port 1h IET is enabled on the port - Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
15	RX_ECC_ERR_EN	R/W	0h	Port N receive ECC Error Enable. This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port N transmit ECC Error Enable. This bit must be set to enable transmit ECC error operations
13	TX_CUT_IET_HOLD_DIS	R/W	0h	Port N transmit IET hold due to cut-thru disable 0h Cut-thru packets to the port will cause premptable traffic to be prempted as early as possible minimizing cut-thru latency 1h Cut-thru packets to the port will be prempted as usual by the express MAC

Table 14-11287. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable. When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11:3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	IPV6 DSCP enable 0h IPV6 DSCP priority mapping is disabled 1h IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	IPV4 DSCP enable 0h IPV4 DSCP priority mapping is disabled 1h IPV4 DSCP priority mapping is enabled
0	RESERVED	NONE	0h	Reserved

14.7.3.1.2.166 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register

14.7.3.1.2.166.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register (Offset = 23008h) [reset = 1004h]

Enet Port N FIFO Max Blocks

Return to Summary Table

Table 14-11288. Instance Table

Instance Name	Physical Address
CPSW0	0802 3008h + formula

Figure 14-5580. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_MAX_BLKS							
R/W							
10h							
7	6	5	4	3	2	1	0
RX_MAX_BLKS							
R/W							
4h							

Table 14-11289. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit Max Blocks. The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive, when Fullduplex flow control is enabled (CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX = 1h) to allow for flow control runout.
7:0	RX_MAX_BLKS	R/W	4h	Receive Max Blocks. The maximum number of blocks allowed on the express and prempt receive FIFOs (transmit and receive FIFO's combined when fifo_oneram = 1)

14.7.3.1.2.167 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register

14.7.3.1.2.167.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register (Offset = 23010h) [reset = 1h]

Enet Port N FIFO Block Usage Count

Return to Summary Table

Table 14-11290. Instance Table

Instance Name	Physical Address
CPSW0	0802 3010h + formula

Figure 14-5581. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		RX_BLK_CNT_P					
NONE		R					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT_E					
NONE		R					
0h		1h					

Table 14-11291. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO prempt receive queue. No blocks are allocated until the CPSW_CONTROL_REG[17] IET_ENABLE is set.
15:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage. This value is the number of blocks allocated to the port's FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO express receive queue.

14.7.3.1.2.168 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register

14.7.3.1.2.168.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register (Offset = 23014h) [reset = 0h]

Enet Port N VLAN

Return to Summary Table

Table 14-11292. Instance Table

Instance Name	Physical Address
CPSW0	0802 3014h + formula

Figure 14-5582. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">PORT_PRI</td><td>PORT_CFI</td><td colspan="4">PORT_VID</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PORT_VID</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11293. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

14.7.3.1.2.169 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register

14.7.3.1.2.169.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register (Offset = 23018h) [reset = 76543210h]

Enet Port N Tx Header Pri to Switch Pri Mapping

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Table 14-11294. Instance Table

Instance Name	Physical Address
CPSW0	0802 3018h + formula

Figure 14-5583. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-11295. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	NONE	0h	Reserved

Table 14-11295. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

14.7.3.1.2.170 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register

14.7.3.1.2.170.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register (Offset = 2301Ch) [reset = 9000h]

Enet Port N Priority Control

Return to Summary Table

Table 14-11296. Instance Table

Instance Name	Physical Address
CPSW0	0802 301Ch + formula

Figure 14-5584. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_FLOW_PRI</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">TX_HOST_BLKS_REM</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">9h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11297. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE	0h	Reserved

14.7.3.1.2.171 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register

14.7.3.1.2.171.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register (Offset = 23020h) [reset = 76543210h]

Enet Port N RX Pkt Pri to Header Pri Map

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Table 14-11298. Instance Table

Instance Name	Physical Address
CPSW0	0802 3020h + formula

Figure 14-5585. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 14-11299. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	NONE	0h	Reserved

Table 14-11299. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

14.7.3.1.2.172 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register

14.7.3.1.2.172.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register (Offset = 23024h) [reset = 5EEh]

Enet Port N Receive Frame Max Length

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Table 14-11300. Instance Table

Instance Name	Physical Address
CPSW0	0802 3024h + formula

Figure 14-5586. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		RX_MAXLEN					
NONE		R/W					
0h		5EEh					
7	6	5	4	3	2	1	0
RX_MAXLEN							
R/W							
5EEh							

Table 14-11301. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_PN_RX_MAXLEN_REG_k[13-0] RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).

14.7.3.1.2.173 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register

14.7.3.1.2.173.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register (Offset = 23028h) [reset = 1245678h]

Enet Port N Transmit Block Sub Per Priority

Return to Summary Table

Table 14-11302. Instance Table

Instance Name	Physical Address
CPSW0	0802 3028h + formula

Figure 14-5587. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 14-11303. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

14.7.3.1.2.174 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register

14.7.3.1.2.174.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register (Offset = 23030h) [reset = 0h]

Enet Port N EEE Idle to LPI counter

Return to Summary Table

Table 14-11304. Instance Table

Instance Name	Physical Address
CPSW0	0802 3030h + formula

Figure 14-5588. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11305. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value

14.7.3.1.2.175 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register

14.7.3.1.2.175.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register (Offset = 23034h) [reset = 0h]

Enet Port N EEE LPI to wake counter

Return to Summary Table

Table 14-11306. Instance Table

Instance Name	Physical Address
CPSW0	0802 3034h + formula

Figure 14-5589. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11307. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value

14.7.3.1.2.176 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register

14.7.3.1.2.176.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register (Offset = 23038h) [reset = 62h]

Enet Port N EEE status

Return to Summary Table

Table 14-11308. Instance Table

Instance Name	Physical Address
CPSW0	0802 3038h + formula

Figure 14-5590. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	1h	0h

Table 14-11309. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

14.7.3.1.2.177 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register

14.7.3.1.2.177.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register (Offset = 23040h) [reset = 8h]

Enet Port N IET Control

Return to Summary Table

Table 14-11310. Instance Table

Instance Name	Physical Address
CPSW0	0802 3040h + formula

Figure 14-5591. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MAC_PREMPT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MAC_ADDFRAGSIZE</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>MAC_LINKFAIL</td><td>MAC_DISABLEVERIFY</td><td>MAC_HOLD</td><td>MAC_PENABLE</td></tr>
<tr><td colspan="4">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td>1h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11311. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAC_PREMPT	R/W	0h	Mac Preempt Queue - Indicates which transmit FIFO queues are sent to the preempt MAC. Bit 0 indicates queue zero, bit 1 queue 1 and so on. Packets will be sent to the preempt MAC only when MAC_PENABLE is set, and when MAC_VERIFIED (from CPSW_PN_IET_STATUS_REG_k) or MAC_DISABLEVERIFY is set, and when IET_PORT_EN is set.
15:11	RESERVED	NONE	0h	Reserved
10:8	MAC_ADDFRAGSIZE	R/W	0h	Mac Fragment Size - An integer in the range 0:7 indicating, as a multiple of 64, the minimum additional length for nonfinal mPackets. 0 64 1 128 2 81 3 256 4 320 5 384 6 448 7 512
7:4	RESERVED	NONE	0h	Reserved
3	MAC_LINKFAIL	R/W	1h	Mac Link Fail - Link Fail Indicator to reset the verify state machine. This bit is reset high. Verify and response frames will be sent/allowed when this bit is cleared.

Table 14-11311. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MAC_DISABLEVERIFY	R/W	0h	Mac Disable Verify - Disables verification on the port when set. If this bit is set then packets will be sent to the preempt Mac when MAC_PENABLE is set (This is a forced mode with no IET verification).
1	MAC_HOLD	R/W	0h	Mac Hold - Hold Preemption on the port.
0	MAC_PENABLE	R/W	0h	Mac Preemption Enable - Port Preemption Enable. This takes effect only when IET_PORT_EN is set.

14.7.3.1.2.178 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register

14.7.3.1.2.178.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register (Offset = 23044h) [reset = 0h]

Enet Port N IET Status

Return to Summary Table

Table 14-11312. Instance Table

Instance Name	Physical Address
CPSW0	0802 3044h + formula

Figure 14-5592. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MAC_VERIFY_ERR	MAC_RESPOND_ERR	MAC_VERIFY_FAIL	MAC_VERIFIED
NONE				R	R	R	R
0h				0h	0h	0h	0h

Table 14-11313. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MAC_VERIFY_ERR	R	0h	Mac Received Verify Packet with Errors - Set when a verify packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
2	MAC_RESPOND_ERR	R	0h	Mac Received Respond Packet with Errors - Set when a respond packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
1	MAC_VERIFY_FAIL	R	0h	Mac Verification Failed - Indication that verification was unsuccessful.
0	MAC_VERIFIED	R	0h	Mac Verified - Indication that verification was successful.

14.7.3.1.2.179 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register

14.7.3.1.2.179.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register (Offset = 23048h) [reset = 1312D0h]

Enet Port N IET VERIFY

Return to Summary Table

Table 14-11314. Instance Table

Instance Name	Physical Address
CPSW0	0802 3048h + formula

Figure 14-5593. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MAC_VERIFY_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1312D0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MAC_VERIFY_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1312D0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MAC_VERIFY_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1312D0h</td></tr>
</table>

Table 14-11315. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_IET_VERIFY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	MAC_VERIFY_CNT	R/W	1312D0h	Mac Verify Timeout Count - The number of wireside clocks contained in the verify timeout counter. The default is 0x1312D0 (10ms at 125MHz in gig mode).

14.7.3.1.2.180 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register

14.7.3.1.2.180.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register (Offset = 23050h) [reset = FF00h]

Enet Port N FIFO STATUS

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Table 14-11316. Instance Table

Instance Name	Physical Address
CPSW0	0802 3050h + formula

Figure 14-5594. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE					R	R	R
0h					0h	0h	0h
15	14	13	12	11	10	9	8
TX_E_MAC_ALLOW							
R							
FFh							
7	6	5	4	3	2	1	0
TX_PRI_ACTIVE							
R							
0h							

Table 14-11317. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	EST_BUFACT	R	0h	EST RAM active buffer. Indicates the active 64-word fetch buffer when CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared to zero. Indicates the fetch RAM address MSB when bit [0] EST_ONEBUF is set to one.
17	EST_ADD_ERR	R	0h	EST Address Error. Indicates that the fetch RAM was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error. Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15:8	TX_E_MAC_ALLOW	R	FFh	EST transmit MAC allow. Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the prempt queue).
7:0	TX_PRI_ACTIVE	R	0h	EST Transmit Priority Active. Bus that indicates which priorities have packets (non-empty) at the time of the register read.

14.7.3.1.2.181 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register

14.7.3.1.2.181.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register (Offset = 23060h) [reset = 0h]

Enet Port N EST CONTROL

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Table 14-11318. Instance Table

Instance Name	Physical Address
CPSW0	0802 3060h + formula

Figure 14-5595. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED						EST_FILL_MARGIN	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EST_FILL_MARGIN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EST_PREMPT_COMP							EST_FILL_EN
R/W							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-11319. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin. Sets the fill margin required to ensure that the Ethernet wire is clear (including IPG) so that the timed EST express packet can egress at the required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended.
15:9	EST_PREMPT_COMP	R/W	0h	EST Prempt Comparison Value. When the count in a zero allow is less than or equal to this value in bytes (times 8), prempt packets are cleared from the wire. This is the prempt clear margin value.
8	EST_FILL_EN	R/W	0h	EST Fill Enable. Enable EST fill mode.
7:5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority. Selects the express priority that timestamp(s) will be generated on when CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI bit is set.
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority. When set, timestamp only enabled packets on the express priority selected by CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI bit field. When cleared to zero, express packet selection for timestamp is independent of priority.

Table 14-11319. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_EST_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only. Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If CPSW_PN_EST_CONTROL_REG_k[4] EST_TS_ONEPRI is also set then the timestamp is generated only on the first packet on CPSW_PN_EST_CONTROL_REG_k[7-5] ST_TS_PRI).
2	EST_TS_EN	R/W	0h	EST Timestamp Enable. Enable express timestamps (when CPSW_CONTROL_REG[18] EST_ENABLE and CPSW_PN_CONTROL_REG_k[17] EST_PORT_EN bits are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select. If CPSW_PN_EST_CONTROL_REG_k[0] EST_ONEBUF is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the CPSW_PN_FIFO_STATUS_REG_k register, bit [18] EST_BUFACT.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer. When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The CPSW_PN_EST_CONTROL_REG_k[1] EST_BUFSEL bit selects the buffer to be used when bit [0] EST_ONEBUF is cleared to zero.

14.7.3.1.2.182 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_J Register

14.7.3.1.2.182.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_J Register (Offset = 23120h) [reset = 0h]

Enet Port N Receive IPV4/IPV6 DSCP Map M

Return to Summary Table

Table 14-11320. Instance Table

Instance Name	Physical Address
CPSW0	0802 3120h + formula

Figure 14-5596. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 14-11321. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved

Table 14-11321. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_RX_DSCP_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

14.7.3.1.2.183 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_J Register

14.7.3.1.2.183.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_J Register (Offset = 23140h) [reset = 0h]

Enet Port N Rx Priority P Committed Information Rate Value

Return to Summary Table

Table 14-11322. Instance Table

Instance Name	Physical Address
CPSW0	0802 3140h + formula

Figure 14-5597. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_CIR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_CIR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_CIR							
R/W							
0h							

Table 14-11323. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

14.7.3.1.2.184 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_J Register

14.7.3.1.2.184.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_J Register (Offset = 23160h) [reset = 0h]

Enet Port N Rx Priority P Excess Informatoin Rate Value

Return to Summary Table

Table 14-11324. Instance Table

Instance Name	Physical Address
CPSW0	0802 3160h + formula

Figure 14-5598. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PRI_EIR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PRI_EIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PRI_EIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRI_EIR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11325. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

14.7.3.1.2.185 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register

14.7.3.1.2.185.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register (Offset = 23180h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set Low

Return to Summary Table

Table 14-11326. Instance Table

Instance Name	Physical Address
CPSW0	0802 3180h + formula

Figure 14-5599. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-11327. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.7.3.1.2.186 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register

14.7.3.1.2.186.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register (Offset = 23184h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set High

Return to Summary Table

Table 14-11328. Instance Table

Instance Name	Physical Address
CPSW0	0802 3184h + formula

Figure 14-5600. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-11329. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.7.3.1.2.187 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register

14.7.3.1.2.187.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 23188h) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr Low

Return to Summary Table

Table 14-11330. Instance Table

Instance Name	Physical Address
CPSW0	0802 3188h + formula

Figure 14-5601. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-11331. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.7.3.1.2.188 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register

14.7.3.1.2.188.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 2318Ch) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr High

Return to Summary Table

Table 14-11332. Instance Table

Instance Name	Physical Address
CPSW0	0802 318Ch + formula

Figure 14-5602. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PRI7</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PRI6</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PRI5</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">PRI4</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-11333. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.7.3.1.2.189 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register

14.7.3.1.2.189.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 23190h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set Low

Return to Summary Table

Table 14-11334. Instance Table

Instance Name	Physical Address
CPSW0	0802 3190h + formula

Figure 14-5603. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 14-11335. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

14.7.3.1.2.190 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register

14.7.3.1.2.190.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 23194h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set High

Return to Summary Table

Table 14-11336. Instance Table

Instance Name	Physical Address
CPSW0	0802 3194h + formula

Figure 14-5604. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 14-11337. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

14.7.3.1.2.191 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register

14.7.3.1.2.191.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 23198h) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr Low

Return to Summary Table

Table 14-11338. Instance Table

Instance Name	Physical Address
CPSW0	0802 3198h + formula

Figure 14-5605. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-11339. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

14.7.3.1.2.192 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register

14.7.3.1.2.192.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2319Ch) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr High

Return to Summary Table

Table 14-11340. Instance Table

Instance Name	Physical Address
CPSW0	0802 319Ch + formula

Figure 14-5606. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-11341. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

14.7.3.1.2.193 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register

14.7.3.1.2.193.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 23300h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values Low

Return to Summary Table

Table 14-11342. Instance Table

Instance Name	Physical Address
CPSW0	0802 3300h + formula

Figure 14-5607. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 14-11343. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

14.7.3.1.2.194 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register

14.7.3.1.2.194.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 23304h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values High

Return to Summary Table

Table 14-11344. Instance Table

Instance Name	Physical Address
CPSW0	0802 3304h + formula

Figure 14-5608. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 14-11345. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

14.7.3.1.2.195 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register

14.7.3.1.2.195.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register (Offset = 23308h) [reset = 0h]

Enet Port N Tx Pause Frame Source Address Low

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Table 14-11346. Instance Table

Instance Name	Physical Address
CPSW0	0802 3308h + formula

Figure 14-5609. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_15_8							
R/W							
0h							

Table 14-11347. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

14.7.3.1.2.196 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register

14.7.3.1.2.196.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register (Offset = 2330Ch) [reset = 0h]

Enet Port N Tx Pause Frame Source Address High

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Table 14-11348. Instance Table

Instance Name	Physical Address
CPSW0	0802 330Ch + formula

Figure 14-5610. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24
MACSRCADDR_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
MACSRCADDR_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_47_40							
R/W							
0h							

Table 14-11349. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

14.7.3.1.2.197 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register

14.7.3.1.2.197.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register (Offset = 23310h) [reset = 0h]

Enet Port N Time Sync Control

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Table 14-11350. Instance Table

Instance Name	Physical Address
CPSW0	0802 3310h + formula

Figure 14-5611. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_MSG_TYPE_EN							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11351. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
15:12	RESERVED	NONE	0h	Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable

Table 14-11351. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

14.7.3.1.2.198 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register

14.7.3.1.2.198.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register (Offset = 23314h) [reset = 1E0000h]

Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

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Table 14-11352. Instance Table

Instance Name	Physical Address
CPSW0	0802 3314h + formula

Figure 14-5612. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		TS_SEQ_ID_OFFSET					
NONE		R/W					
0h		1Eh					
15	14	13	12	11	10	9	8
TS_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LTYPE1							
R/W							
0h							

Table 14-11353. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6h.
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1. This is the port's time sync LTYPE1 value.

14.7.3.1.2.199 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register

14.7.3.1.2.199.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register (Offset = 23318h) [reset = 0h]

Enet Port N Time Sync VLAN2 and VLAN2

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Table 14-11354. Instance Table

Instance Name	Physical Address
CPSW0	0802 3318h + formula

Figure 14-5613. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
TS_VLAN_LTYPE2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_VLAN_LTYPE2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_VLAN_LTYPE1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_VLAN_LTYPE1							
R/W							
0h							

Table 14-11355. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for the port TX and RX time sync decode.
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for the port TX and RX time sync decode.

14.7.3.1.2.200 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register

14.7.3.1.2.200.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register (Offset = 2331Ch) [reset = 0h]

Enet Port N Time Sync Control and LTYPE 2

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Table 14-11356. Instance Table

Instance Name	Physical Address
CPSW0	0802 331Ch + formula

Figure 14-5614. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_LTYPE2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_LTYPE2							
R/W							
0h							

Table 14-11357. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved

24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable
				`0h` `Unicast disabled`
				`1h` `Unicast enabled`

23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable
				`0h` `TTL must be 1h`
				`1h` `TTL may be any value`

22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable
				`0h` `Disabled`
				`1h` `Destination port number (decimal) 320 is enabled`

21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable
				`0h` `Disabled`
				`1h` `Destination port number (decimal) 319 is enabled`

20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable
				`0h` `Disabled`
				`1h` `Destination port number (decimal) 224.0.1.132 is enabled`

Table 14-11357. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.131 is enabled
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.130 is enabled
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable 0h Disabled 1h Destination port number (decimal) 224.0.1.129 is enabled
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable 0h Disabled 1h Destination port number (decimal) 224.0.0.107 is enabled
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2. This is the time sync LTYPE1 value for port 1.

14.7.3.1.2.201 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register

14.7.3.1.2.201.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register (Offset = 23320h) [reset = 40000h]

Enet Port N Time Sync Control 2

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Table 14-11358. Instance Table

Instance Name	Physical Address
CPSW0	0802 3320h + formula

Figure 14-5615. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TS_DOMAIN_OFFSET					
NONE		R/W					
0h		4h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_MCAST_TYPE_EN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_MCAST_TYPE_EN							
R/W							
0h							

Table 14-11359. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

14.7.3.1.2.202 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register

14.7.3.1.2.202.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register (Offset = 23330h) [reset = 0h]

Enet Port N Mac Control

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Table 14-11360. Instance Table

Instance Name	Physical Address
CPSW0	0802 3330h + formula

Figure 14-5616. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							RX_CMF_EN
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED	
R/W	NONE		R/W	R/W	R/W	NONE	
0h	0h		0h	0h	0h	0h	
7	6	5	4	3	2	1	0
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11361. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the CPSW_PN_MAC_CONTROL_REG_k register, regardless of the value of [24] RX_CMF_EN bit. Frames transferred to memory due to [24] RX_CMF_EN will have the control bit set in their EOP buffer descriptor. 0h MAC control frames are filtered (but acted upon if enabled). 1h MAC control frames are transferred to memory.
23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable. Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to CPSW_PN_MAC_CONTROL_REG_k[23] RX_CSF_EN will have the fragment or undersized bit set in their receive footer. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors. 0h Short frames are filtered. 1h Short frames are transferred to memory.

Table 14-11361. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable. Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when CPSW_PN_MAC_CONTROL_REG_k[22] RX_CEF_EN is not set. 0h Frames containing errors are filtered. 1h Frames containing errors are transferred to memory.
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable When set this bit limits the number of short gap packets transmitted to 100ppm. The TX_SHORT_GAP_ENABLE bit must also be set. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable. Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the [4] TX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG_k register.
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable. Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the CPSW_PN_MAC_CONTROL_REG_k[3] RX_FLOW_EN bit in this register.
18	EXT_EN	R/W	0h	External Control Enable. Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the [0] FULLDUPLEX and [7] GIG bits in the CPSW_PN_MAC_CONTROL_REG_k register. The [0] FULLDUPLEX bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	R/W	0h	Gigabit Mode Force. This bit is used to force the Ethernet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.
15	IFCTL_A	R/W	0h	Determines the RMII link speed. 0h 10Mbps operation 0h 100Mbps operation
14:13	RESERVED	NONE	0h	Reserved
12	CRC_TYPE	R/W	0h	Port CRC Type. 0h Ethernet CRC 1h Castagnoli CRC
11	CMD_IDLE	R/W	0h	Command Idle. 0h Idle not commanded 1h Idle Commanded (read bit [31] IDLE in CPSW_PN_MAC_STATUS_REG_k register)
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable. 0h Transmit with a short IPG is disabled 1h Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.
9:8	RESERVED	NONE	0h	Reserved
7	GIG	R/W	0h	Gigabit Mode. 0h 10/100 mode 1h Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit.
6	TX_PACE	R/W	0h	Transmit Pacing Enable 0h Transmit Pacing Disabled 1h Transmit Pacing Enabled

Table 14-11361. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GMII_EN	R/W	0h	GMII Enable. 0h GMII RX and TX held in reset. 1h GMII RX and TX released from reset.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0h Transmit Flow Control Disabled. Full-duplex mode - Incoming pause frames are not acted upon. 1h Transmit Flow Control Enabled. Full-duplex mode - Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable. 0h Receive Flow Control Disabled Half-duplex mode - No flow control generated collisions are sent. Full-duplex mode - No outgoing pause frames are sent. 1h Receive Flow Control Enabled Half-duplex mode - Collisions are initiated when receive flow control is triggered. Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode. This bit must be set to allow writes to the CPSW_PN_MAC_BOFFTEST_REG_k and CPSW_PN_MAC_RX_PAUSETIMER_REG_k registers.
1	LOOPBACK	R/W	0h	Loop Back Mode. Loopback mode forces internal fullduplex mode regardless of whether the CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX bit is set or not. The [1] LOOPBACK bit should be changed only when [5] GMII_EN is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS). 0h Not looped back mode 1h Loop Back mode enabled
0	FULLDUPLEX	R/W	0h	Full Duplex mode. Gigabit mode forces fullduplex mode regardless of whether the [0] FULLDUPLEX bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit 0h Half duplex mode 1h Full duplex mode

14.7.3.1.2.203 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register

14.7.3.1.2.203.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register (Offset = 23334h) [reset = F0000000h]

Enet Port N Mac Status

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Table 14-11362. Instance Table

Instance Name	Physical Address
CPSW0	0802 3334h + formula

Figure 14-5617. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	P_IDLE	MAC_TX_IDLE	TORF	TORF_PRI		
R	R	R	R	R	R		
1h	1h	1h	1h	0h	0h		
23	22	21	20	19	18	17	16
TX_PFC_FLOW_ACT							
R							
0h							
15	14	13	12	11	10	9	8
RX_PFC_FLOW_ACT							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
NONE	R	R	R	R	NONE	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11363. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description

31	IDLE	R	1h	Enet IDLE. The Ethernet port (express and prempt) are in the Idle state (valid after an Idle command)
				`0h` `The port is not in the Idle state.`
				`1h` `The port is in the Idle state.`

30	E_IDLE	R	1h	Express MAC is Idle.
29	P_IDLE	R	1h	Prempt MAC is Idle.
28	MAC_TX_IDLE	R	1h	Mac Transmit Idle. Both Prempt and Express MAC Transmit are in Idle state. The transmit clock must be running for this to go idle.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 7h to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15:8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	NONE	0h	Reserved
6	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[19] EXT_RX_FLOW_EN input bit.

Table 14-11363. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG_k[20] EXT_TX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG. This is the value of the [4] EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Fullduplex. This is the value of the [3] EXT_FULLDUPLEX input bit.
2	RESERVED	NONE	0h	Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

14.7.3.1.2.204 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register

14.7.3.1.2.204.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register (Offset = 23338h) [reset = 0h]

Enet Port N Mac Soft Reset

Return to Summary Table

Table 14-11364. Instance Table

Instance Name	Physical Address
CPSW0	0802 3338h + formula

Figure 14-5618. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFT_RESET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-11365. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Software reset. Writing a 1h to this bit causes the Ethernet Mac logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a 1h is read, the reset has not yet occurred. If a 0h is read then reset has occurred.

14.7.3.1.2.205 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register

14.7.3.1.2.205.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register (Offset = 2333Ch) [reset = 0h]

Enet Port N Mac Backoff Test

Return to Summary Table

Table 14-11366. Instance Table

Instance Name	Physical Address
CPSW0	0802 333Ch + formula

Figure 14-5619. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
NONE	R/W					R/W	
0h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RNDNUM							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COLL_COUNT				RESERVED		TX_BACKOFF	
R				NONE		R	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_BACKOFF							
R							
0h							

Table 14-11367. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:26	PACEVAL	R/W	0h	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce 'capture' effects improving overall network bandwidth.
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when CPSW_PN_MAC_CONTROL_REG_k[2] MTEST bit has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15:12	COLL_COUNT	R	0h	Collision Count.
11:10	RESERVED	NONE	0h	Reserved

Table 14-11367. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	TX_BACKOFF	R	0h	Backoff Count. This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.

14.7.3.1.2.206 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register

14.7.3.1.2.206.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 23340h) [reset = 0h]

Enet Port N 802.3 Receive Pause Timer

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Table 14-11368. Instance Table

Instance Name	Physical Address
CPSW0	0802 3340h + formula

Figure 14-5620. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-11369. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.7.3.1.2.207 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_J Register

14.7.3.1.2.207.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_J Register (Offset = 23350h) [reset = 0h]

Enet Port N PFC Priority P Rx Pause Timer

Return to Summary Table

Table 14-11370. Instance Table

Instance Name	Physical Address
CPSW0	0802 3350h + formula

Figure 14-5621. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 14-11371. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	Rx Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

14.7.3.1.2.208 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register

14.7.3.1.2.208.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 23370h) [reset = 0h]

Enet Port N 802.3 Tx Pause Timer

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Table 14-11372. Instance Table

Instance Name	Physical Address
CPSW0	0802 3370h + formula

Figure 14-5622. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 14-11373. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

14.7.3.1.2.209 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_J Register

14.7.3.1.2.209.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_J Register (Offset = 23380h) [reset = 0h]

Enet Port N PFC Priority P Tx Pause Timer

Return to Summary Table

Table 14-11374. Instance Table

Instance Name	Physical Address
CPSW0	0802 3380h + formula

Figure 14-5623. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TX_PAUSETIMER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_PAUSETIMER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11375. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	PFC Tx 'y' Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

14.7.3.1.2.210 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register

14.7.3.1.2.210.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register (Offset = 233A0h) [reset = 0h]

Enet Port N Emulation Control

Return to Summary Table

Table 14-11376. Instance Table

Instance Name	Physical Address
CPSW0	0802 33A0h + formula

Figure 14-5624. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 14-11377. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

14.7.3.1.2.211 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register

14.7.3.1.2.211.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register (Offset = 233A4h) [reset = Ch]

Enet Port N Tx Inter Packet Gap

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Table 14-11378. Instance Table

Instance Name	Physical Address
CPSW0	0802 33A4h + formula

Figure 14-5625. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_GAP							
R/W							
Ch							
7	6	5	4	3	2	1	0
TX_GAP							
R/W							
Ch							

Table 14-11379. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap GMII modes - This is the default gap value and only bits [8-0] are used. This can be increased from 12 to increase the gap between packets. XGMII mode - In 10 Gigabit mode this is the short gap rate and should be changed to 5000 (1388h) to get approximately 200ppm faster when short gap is triggered and enabled.

14.7.3.1.2.212 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register

14.7.3.1.2.212.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register (Offset = 233A8h) [reset = 204h]

Enet Port N Port Configuration

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Table 14-11380. Instance Table

Instance Name	Physical Address
CPSW0	0802 33A8h + formula

Figure 14-5626. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						IET	XGMII
NONE						R	R
0h						1h	0h
7	6	5	4	3	2	1	0
INTERVLAN_ROUTES							
R							
4h							

Table 14-11381. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	IET	R	1h	Intersperced Express Traffic (IET) is supported on this port when read high.
8	XGMII	R	0h	XGMII is supported on this port when set.
7:0	INTERVLAN_ROUTES	R	4h	This is the number of InterVLAN routes supported on this port (egress).

14.7.3.1.2.213 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register

14.7.3.1.2.213.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 233ACh) [reset = 0h]

Enet Port N Tx Egress InterVLAN Operation Pointer

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Table 14-11382. Instance Table

Instance Name	Physical Address
CPSW0	0802 33ACh + formula

Figure 14-5627. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					POINTER		
NONE					R/W		
0h					0h		

Table 14-11383. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

14.7.3.1.2.214 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register

14.7.3.1.2.214.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register (Offset = 233B0h) [reset = 0h]

Enet Port N Tx Egress InterVLAN A

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Table 14-11384. Instance Table

Instance Name	Physical Address
CPSW0	0802 33B0h + formula

Figure 14-5628. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24
DA_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
DA_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_47_40							
R/W							
0h							

Table 14-11385. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16 - DA byte 4 on wire
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24 - DA byte 3 on wire
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32 - DA byte 2 on wire
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40 - DA byte 1 on wire

14.7.3.1.2.215 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register

14.7.3.1.2.215.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register (Offset = 233B4h) [reset = 0h]

Enet Port N Tx Egress InterVLAN B

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Table 14-11386. Instance Table

Instance Name	Physical Address
CPSW0	0802 33B4h + formula

Figure 14-5629. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Name Register

31	30	29	28	27	26	25	24
SA_39_32							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_47_40							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_15_8							
R/W							
0h							

Table 14-11387. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32 - SA byte 2 on wire
23:16	SA_47_40	R/W	0h	Source Address bits 47:40 - SA byte 1 on wire
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0 - DA byte 6 on wire
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8 - DA byte 5 on wire

14.7.3.1.2.216 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register

14.7.3.1.2.216.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register (Offset = 233B8h) [reset = 0h]

Enet Port N Tx Egress InterVLAN C

Return to Summary Table

Table 14-11388. Instance Table

Instance Name	Physical Address
CPSW0	0802 33B8h + formula

Figure 14-5630. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24
SA_7_0							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_15_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SA_23_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SA_31_24							
R/W							
0h							

Table 14-11389. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0 - DA byte 6 on wire
23:16	SA_15_8	R/W	0h	Source Address bits 15:8 - DA byte 5 on wire
15:8	SA_23_16	R/W	0h	Source Address bits 23:16 - DA byte 4 on wire
7:0	SA_31_24	R/W	0h	Source Address bits 31:24 - DA byte 3 on wire

14.7.3.1.2.217 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register

14.7.3.1.2.217.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register (Offset = 233BCh) [reset = 0h]

Enet Port N Tx Egress InterVLAN D

Return to Summary Table

Table 14-11390. Instance Table

Instance Name	Physical Address
CPSW0	0802 33BCh + formula

Figure 14-5631. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
VID							
R/W							
0h							

Table 14-11391. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

14.7.3.1.2.218 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register

14.7.3.1.2.218.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register (Offset = 233C0h) [reset = 0h]

Enet Port N Cut Thru Priority Enable

Return to Summary Table

Table 14-11392. Instance Table

Instance Name	Physical Address
CPSW0	0802 33C0h + formula

Figure 14-5632. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PRI_CUT_THRU_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PRI_CUT_THRU_EN							
R/W							
0h							

Table 14-11393. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_CUT_THRU_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RX_PRI_CUT_THRU_EN	R/W	0h	Receive Cut Thru Priority Enable
7:0	TX_PRI_CUT_THRU_EN	R/W	0h	Transmit Cut Thru Priority Enable

14.7.3.1.2.219 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register

14.7.3.1.2.219.1 CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register (Offset = 233C4h) [reset = 0h]

Enet Port Speed

Return to Summary Table

Table 14-11394. Instance Table

Instance Name	Physical Address
CPSW0	0802 33C4h + formula

Figure 14-5633. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RESERVED</td><td>PORT_SPEED_CHANGED</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">PORT_AUTO_SPEED</td><td colspan="3">RESERVED</td><td>PORT_SPEED_AUTO_EN</td></tr>
<tr><td colspan="4">R</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PORT_SPEED_MANUAL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-11395. CPSW3_CPSW_NU_CPSW_NU_ETH_MAC_1_PN_PORT_SPEED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	PORT_SPEED_CHANGED	R	0h	Port Speed Changed
19:16	RESERVED	NONE	0h	Reserved
15:12	PORT_AUTO_SPEED	R	0h	Detected Auto Speed
11:9	RESERVED	NONE	0h	Reserved
8	PORT_SPEED_AUTO_EN	R/W	0h	Automatic Port Speed Enable
7:4	RESERVED	NONE	0h	Reserved
3:0	PORT_SPEED_MANUAL	R/W	0h	Manual Port Speed

14.7.3.1.2.220 CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_J Register

14.7.3.1.2.220.1 CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_J Register (Offset = 32000h) [reset = 0h]

The Revision Register contains the ID and revision information.

Return to Summary Table

Table 14-11396. Instance Table

Instance Name	Physical Address
CPSW0	0803 2000h + formula

Figure 14-5634. CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		LOC					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOC							
R/W							
0h							

Table 14-11397. CPSW3_CPSW_NU_CPSW_NU_EST_FETCH_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	LOC	R/W	0h	RAM Location

14.7.3.1.2.221 CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_J Register

14.7.3.1.2.221.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_J Register (Offset = 3A000h) [reset = 0h]

Total number of good frames received

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Table 14-11398. Instance Table

Instance Name	Physical Address
CPSW0	0803 A000h + formula

Figure 14-5635. CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11399. CPSW3_CPSW_NU_CPSW_NU_STAT_RXGOODFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames received

14.7.3.1.2.222 CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_J Register

14.7.3.1.2.222.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_J Register (Offset = 3A004h) [reset = 0h]

Total number of good broadcast frames received

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Table 14-11400. Instance Table

Instance Name	Physical Address
CPSW0	0803 A004h + formula

Figure 14-5636. CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11401. CPSW3_CPSW_NU_CPSW_NU_STAT_RXBROADCASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames received

14.7.3.1.2.223 CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_J Register

14.7.3.1.2.223.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_J Register (Offset = 3A008h) [reset = 0h]

Total number of good multicast frames received

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Table 14-11402. Instance Table

Instance Name	Physical Address
CPSW0	0803 A008h + formula

Figure 14-5637. CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11403. CPSW3_CPSW_NU_CPSW_NU_STAT_RXMULTICASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames received

14.7.3.1.2.224 CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_J Register

14.7.3.1.2.224.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_J Register (Offset = 3A00Ch) [reset = 0h]

Total number of pause frames received

Return to Summary Table

Table 14-11404. Instance Table

Instance Name	Physical Address
CPSW0	0803 A00Ch + formula

Figure 14-5638. CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 14-11405. CPSW3_CPSW_NU_CPSW_NU_STAT_RXPAUSEFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames received

14.7.3.1.2.225 CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_J Register

14.7.3.1.2.225.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_J Register (Offset = 3A010h) [reset = 0h]

Total number of CRC errors frames received

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Table 14-11406. Instance Table

Instance Name	Physical Address
CPSW0	0803 A010h + formula

Figure 14-5639. CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11407. CPSW3_CPSW_NU_CPSW_NU_STAT_RXCRCERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of CRC errors frames received

14.7.3.1.2.226 CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_J Register

14.7.3.1.2.226.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_J Register (Offset = 3A014h) [reset = 0h]

Total number of alignment/code errors received

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Table 14-11408. Instance Table

Instance Name	Physical Address
CPSW0	0803 A014h + formula

Figure 14-5640. CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11409. CPSW3_CPSW_NU_CPSW_NU_STAT_RXALIGNCODEERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of alignment/code errors received

14.7.3.1.2.227 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_J Register

14.7.3.1.2.227.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_J Register (Offset = 3A018h) [reset = 0h]

Total number of oversized frames received

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Table 14-11410. Instance Table

Instance Name	Physical Address
CPSW0	0803 A018h + formula

Figure 14-5641. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11411. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOVERSIZEDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of oversized frames received

14.7.3.1.2.228 CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_J Register

14.7.3.1.2.228.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_J Register (Offset = 3A01Ch) [reset = 0h]

Total number of jabber frames received

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Table 14-11412. Instance Table

Instance Name	Physical Address
CPSW0	0803 A01Ch + formula

Figure 14-5642. CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11413. CPSW3_CPSW_NU_CPSW_NU_STAT_RXJABBERFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of jabber frames received

14.7.3.1.2.229 CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_J Register

14.7.3.1.2.229.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_J Register (Offset = 3A020h) [reset = 0h]

Total number of undersized frames received

Return to Summary Table

Table 14-11414. Instance Table

Instance Name	Physical Address
CPSW0	0803 A020h + formula

Figure 14-5643. CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11415. CPSW3_CPSW_NU_CPSW_NU_STAT_RXUNDERSIZEDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of undersized frames received

14.7.3.1.2.230 CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_J Register

14.7.3.1.2.230.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_J Register (Offset = 3A024h) [reset = 0h]

Total number of fragmented frames received

Return to Summary Table

Table 14-11416. Instance Table

Instance Name	Physical Address
CPSW0	0803 A024h + formula

Figure 14-5644. CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11417. CPSW3_CPSW_NU_CPSW_NU_STAT_RXFRAGMENTS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of fragmented frames received

14.7.3.1.2.231 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_J Register

14.7.3.1.2.231.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_J Register (Offset = 3A028h) [reset = 0h]

Total number of frames dropped by the ALE

Return to Summary Table

Table 14-11418. Instance Table

Instance Name	Physical Address
CPSW0	0803 A028h + formula

Figure 14-5645. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11419. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames dropped by the ALE

14.7.3.1.2.232 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_J Register

14.7.3.1.2.232.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_J Register (Offset = 3A02Ch) [reset = 0h]

Total number of overrun frames dropped by the ALE

Return to Summary Table

Table 14-11420. Instance Table

Instance Name	Physical Address
CPSW0	0803 A02Ch + formula

Figure 14-5646. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11421. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_OVERRUN_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE

14.7.3.1.2.233 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_J Register

14.7.3.1.2.233.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_J Register (Offset = 3A030h) [reset = 0h]

Total number of received bytes in good frames

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Table 14-11422. Instance Table

Instance Name	Physical Address
CPSW0	0803 A030h + formula

Figure 14-5647. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11423. CPSW3_CPSW_NU_CPSW_NU_STAT_RXOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of received bytes in good frames

14.7.3.1.2.234 CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_J Register

14.7.3.1.2.234.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_J Register (Offset = 3A034h) [reset = 0h]

Total number of good frames transmitted

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Table 14-11424. Instance Table

Instance Name	Physical Address
CPSW0	0803 A034h + formula

Figure 14-5648. CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11425. CPSW3_CPSW_NU_CPSW_NU_STAT_TXGOODFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames transmitted

14.7.3.1.2.235 CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_J Register

14.7.3.1.2.235.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_J Register (Offset = 3A038h) [reset = 0h]

Total number of good broadcast frames transmitted

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Table 14-11426. Instance Table

Instance Name	Physical Address
CPSW0	0803 A038h + formula

Figure 14-5649. CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11427. CPSW3_CPSW_NU_CPSW_NU_STAT_TXBROADCASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames transmitted

14.7.3.1.2.236 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_J Register

14.7.3.1.2.236.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_J Register (Offset = 3A03Ch) [reset = 0h]

Total number of good multicast frames transmitted

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Table 14-11428. Instance Table

Instance Name	Physical Address
CPSW0	0803 A03Ch + formula

Figure 14-5650. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11429. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTICASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames transmitted

14.7.3.1.2.237 CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_J Register

14.7.3.1.2.237.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_J Register (Offset = 3A040h) [reset = 0h]

Total number of pause frames transmitted

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Table 14-11430. Instance Table

Instance Name	Physical Address
CPSW0	0803 A040h + formula

Figure 14-5651. CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11431. CPSW3_CPSW_NU_CPSW_NU_STAT_TXPAUSEFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames transmitted

14.7.3.1.2.238 CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_J Register

14.7.3.1.2.238.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_J Register (Offset = 3A044h) [reset = 0h]

Total number of deferred frames transmitted

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Table 14-11432. Instance Table

Instance Name	Physical Address
CPSW0	0803 A044h + formula

Figure 14-5652. CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11433. CPSW3_CPSW_NU_CPSW_NU_STAT_TXDEFERREDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of deferred frames transmitted

14.7.3.1.2.239 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_J Register

14.7.3.1.2.239.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_J Register (Offset = 3A048h) [reset = 0h]

Total number of transmitted frames experiencing a collision

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Table 14-11434. Instance Table

Instance Name	Physical Address
CPSW0	0803 A048h + formula

Figure 14-5653. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11435. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCOLLISIONFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a collision

14.7.3.1.2.240 CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_J Register

14.7.3.1.2.240.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_J Register (Offset = 3A04Ch) [reset = 0h]

Total number of transmitted frames experiencing a single collision

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Table 14-11436. Instance Table

Instance Name	Physical Address
CPSW0	0803 A04Ch + formula

Figure 14-5654. CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11437. CPSW3_CPSW_NU_CPSW_NU_STAT_TXSINGLECOLLFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a single collision

14.7.3.1.2.241 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_J Register

14.7.3.1.2.241.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_J Register (Offset = 3A050h) [reset = 0h]

Total number of transmitted frames experiencing multiple collisions

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Table 14-11438. Instance Table

Instance Name	Physical Address
CPSW0	0803 A050h + formula

Figure 14-5655. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11439. CPSW3_CPSW_NU_CPSW_NU_STAT_TXMULTCOLLFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing multiple collisions

14.7.3.1.2.242 CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_J Register

14.7.3.1.2.242.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_J Register (Offset = 3A054h) [reset = 0h]

Total number of transmitted frames abandoned due to excessive collisions

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Table 14-11440. Instance Table

Instance Name	Physical Address
CPSW0	0803 A054h + formula

Figure 14-5656. CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11441. CPSW3_CPSW_NU_CPSW_NU_STAT_TXEXCESSIVECOLLISIONS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to excessive collisions

14.7.3.1.2.243 CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_J Register

14.7.3.1.2.243.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_J Register (Offset = 3A058h) [reset = 0h]

Total number of transmitted frames abandoned due to a late collision

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Table 14-11442. Instance Table

Instance Name	Physical Address
CPSW0	0803 A058h + formula

Figure 14-5657. CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11443. CPSW3_CPSW_NU_CPSW_NU_STAT_TXLATECOLLISIONS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to a late collision

14.7.3.1.2.244 CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_J Register

14.7.3.1.2.244.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_J Register (Offset = 3A05Ch) [reset = 0h]

Total number of receive inter-packet gap errors (10G only)

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Table 14-11444. Instance Table

Instance Name	Physical Address
CPSW0	0803 A05Ch + formula

Figure 14-5658. CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 14-11445. CPSW3_CPSW_NU_CPSW_NU_STAT_RXIPGERROR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of receive inter-packet gap errors (10G only)

14.7.3.1.2.245 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_J Register

14.7.3.1.2.245.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_J Register (Offset = 3A060h) [reset = 0h]

Total number of transmitted frames that experienced a carrier loss

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Table 14-11446. Instance Table

Instance Name	Physical Address
CPSW0	0803 A060h + formula

Figure 14-5659. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11447. CPSW3_CPSW_NU_CPSW_NU_STAT_TXCARRIERSENSEERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames that experienced a carrier loss

14.7.3.1.2.246 CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_J Register

14.7.3.1.2.246.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_J Register (Offset = 3A064h) [reset = 0h]

Total number of bytes in all good frames transmitted

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Table 14-11448. Instance Table

Instance Name	Physical Address
CPSW0	0803 A064h + formula

Figure 14-5660. CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11449. CPSW3_CPSW_NU_CPSW_NU_STAT_TXOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

14.7.3.1.2.247 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_J Register

14.7.3.1.2.247.1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_J Register (Offset = 3A068h) [reset = 0h]

Total number of 64-byte frames received and transmitted

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Table 14-11450. Instance Table

Instance Name	Physical Address
CPSW0	0803 A068h + formula

Figure 14-5661. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11451. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES64_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

14.7.3.1.2.248 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_J Register

14.7.3.1.2.248.1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_J Register (Offset = 3A06Ch) [reset = 0h]

Total number of frames of size 65 to 127 bytes received and transmitted

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Table 14-11452. Instance Table

Instance Name	Physical Address
CPSW0	0803 A06Ch + formula

Figure 14-5662. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11453. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES65T127_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

14.7.3.1.2.249 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_J Register

14.7.3.1.2.249.1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_J Register (Offset = 3A070h) [reset = 0h]

Total number of frames of size 128 to 255 bytes received and transmitted

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Table 14-11454. Instance Table

Instance Name	Physical Address
CPSW0	0803 A070h + formula

Figure 14-5663. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11455. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES128T255_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

14.7.3.1.2.250 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_J Register

14.7.3.1.2.250.1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_J Register (Offset = 3A074h) [reset = 0h]

Total number of frames of size 256 to 511 bytes received and transmitted

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Table 14-11456. Instance Table

Instance Name	Physical Address
CPSW0	0803 A074h + formula

Figure 14-5664. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11457. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES256T511_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted

14.7.3.1.2.251 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_J Register

14.7.3.1.2.251.1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_J Register (Offset = 3A078h) [reset = 0h]

Total number of frames of size 512 to 1023 bytes received and transmitted

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Table 14-11458. Instance Table

Instance Name	Physical Address
CPSW0	0803 A078h + formula

Figure 14-5665. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11459. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES512T1023_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted

14.7.3.1.2.252 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_J Register

14.7.3.1.2.252.1 CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_J Register (Offset = 3A07Ch) [reset = 0h]

Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

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Table 14-11460. Instance Table

Instance Name	Physical Address
CPSW0	0803 A07Ch + formula

Figure 14-5666. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11461. CPSW3_CPSW_NU_CPSW_NU_STAT_OCTETFRAMES1024TUP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

14.7.3.1.2.253 CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_J Register

14.7.3.1.2.253.1 CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_J Register (Offset = 3A080h) [reset = 0h]

Total number of bytes received and transmitted

Return to Summary Table

Table 14-11462. Instance Table

Instance Name	Physical Address
CPSW0	0803 A080h + formula

Figure 14-5667. CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11463. CPSW3_CPSW_NU_CPSW_NU_STAT_NETOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes received and transmitted

14.7.3.1.2.254 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_J Register

14.7.3.1.2.254.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_J Register (Offset = 3A084h) [reset = 0h]

Receive Bottom of FIFO Drop

Return to Summary Table

Table 14-11464. Instance Table

Instance Name	Physical Address
CPSW0	0803 A084h + formula

Figure 14-5668. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11465. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_BOTTOM_OF_FIFO_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Bottom of FIFO Drop

14.7.3.1.2.255 CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_J Register

14.7.3.1.2.255.1 CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_J Register (Offset = 3A088h) [reset = 0h]

Total number of dropped frames received due to portmask

Return to Summary Table

Table 14-11466. Instance Table

Instance Name	Physical Address
CPSW0	0803 A088h + formula

Figure 14-5669. CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11467. CPSW3_CPSW_NU_CPSW_NU_STAT_PORTMASK_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames received due to portmask

14.7.3.1.2.256 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_J Register

14.7.3.1.2.256.1 CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_J Register (Offset = 3A08Ch) [reset = 0h]

Receive Top of FIFO Drop

Return to Summary Table

Table 14-11468. Instance Table

Instance Name	Physical Address
CPSW0	0803 A08Ch + formula

Figure 14-5670. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11469. CPSW3_CPSW_NU_CPSW_NU_STAT_RX_TOP_OF_FIFO_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Top of FIFO Drop

14.7.3.1.2.257 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_J Register

14.7.3.1.2.257.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_J Register (Offset = 3A090h) [reset = 0h]

Total number of dropped frames due to ALE Rate Limiting

Return to Summary Table

Table 14-11470. Instance Table

Instance Name	Physical Address
CPSW0	0803 A090h + formula

Figure 14-5671. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11471. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_RATE_LIMIT_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting

14.7.3.1.2.258 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_J Register

14.7.3.1.2.258.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_J Register (Offset = 3A094h) [reset = 0h]

Total number of dropped frames due to ALE VID Ingress

Return to Summary Table

Table 14-11472. Instance Table

Instance Name	Physical Address
CPSW0	0803 A094h + formula

Figure 14-5672. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11473. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_VID_INGRESS_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress

14.7.3.1.2.259 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_J Register

14.7.3.1.2.259.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_J Register (Offset = 3A098h) [reset = 0h]

Total number of dropped frames due to DA=SA

Return to Summary Table

Table 14-11474. Instance Table

Instance Name	Physical Address
CPSW0	0803 A098h + formula

Figure 14-5673. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11475. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DA_EQ_SA_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA

14.7.3.1.2.260 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_J Register

14.7.3.1.2.260.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_J Register (Offset = 3A09Ch) [reset = 0h]

Total number of dropped frames due to ALE Block Mode

Return to Summary Table

Table 14-11476. Instance Table

Instance Name	Physical Address
CPSW0	0803 A09Ch + formula

Figure 14-5674. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11477. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_BLOCK_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode

14.7.3.1.2.261 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_J Register

14.7.3.1.2.261.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_J Register (Offset = 3A0A0h) [reset = 0h]

Total number of dropped frames due to ALE Secure Mode

Return to Summary Table

Table 14-11478. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0A0h + formula

Figure 14-5675. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11479. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_SECURE_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode

14.7.3.1.2.262 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_J Register

14.7.3.1.2.262.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_J Register (Offset = 3A0A4h) [reset = 0h]

Total number of dropped frames due to ALE Authentication

Return to Summary Table

Table 14-11480. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0A4h + formula

Figure 14-5676. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11481. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_AUTH_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication

14.7.3.1.2.263 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_J Register

14.7.3.1.2.263.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_J Register (Offset = 3A0A8h) [reset = 0h]

ALE Receive Unknown Unicast

Return to Summary Table

Table 14-11482. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0A8h + formula

Figure 14-5677. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11483. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast

14.7.3.1.2.264 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_J Register

14.7.3.1.2.264.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_J Register (Offset = 3A0ACh) [reset = 0h]

ALE Receive Unknown Unicast Bytecount

Return to Summary Table

Table 14-11484. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0ACh + formula

Figure 14-5678. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 14-11485. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_UNI_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount

14.7.3.1.2.265 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_J Register

14.7.3.1.2.265.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_J Register (Offset = 3A0B0h) [reset = 0h]

ALE Receive Unknown Multicast

Return to Summary Table

Table 14-11486. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0B0h + formula

Figure 14-5679. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							

23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							

15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							

7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11487. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast

14.7.3.1.2.266 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_J Register

14.7.3.1.2.266.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_J Register (Offset = 3A0B4h) [reset = 0h]

ALE Receive Unknown Multicast Bytecount

Return to Summary Table

Table 14-11488. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0B4h + formula

Figure 14-5680. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11489. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_MLT_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount

14.7.3.1.2.267 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_J Register

14.7.3.1.2.267.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_J Register (Offset = 3A0B8h) [reset = 0h]

ALE Receive Unknown Broadcast

Return to Summary Table

Table 14-11490. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0B8h + formula

Figure 14-5681. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11491. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast

14.7.3.1.2.268 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_J Register

14.7.3.1.2.268.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_J Register (Offset = 3A0BCh) [reset = 0h]

ALE Receive Unknown Broadcast Bytecount

Return to Summary Table

Table 14-11492. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0BCh + formula

Figure 14-5682. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11493. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_UNKN_BRD_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount

14.7.3.1.2.269 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_J Register

14.7.3.1.2.269.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_J Register (Offset = 3A0C0h) [reset = 0h]

ALE Policer Matched

Return to Summary Table

Table 14-11494. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0C0h + formula

Figure 14-5683. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 14-11495. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched

14.7.3.1.2.270 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_J Register

14.7.3.1.2.270.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_J Register (Offset = 3A0C4h) [reset = 0h]

ALE Policer Matched and Condition Red

Return to Summary Table

Table 14-11496. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0C4h + formula

Figure 14-5684. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11497. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_RED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Red

14.7.3.1.2.271 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_J Register

14.7.3.1.2.271.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_J Register (Offset = 3A0C8h) [reset = 0h]

ALE Policer Matched and Condition Yellow

Return to Summary Table

Table 14-11498. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0C8h + formula

Figure 14-5685. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11499. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_POL_MATCH_YELLOW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow

14.7.3.1.2.272 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_J Register

14.7.3.1.2.272.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_J Register (Offset = 3A0CCh) [reset = 0h]

ALE Multicast Source Address Drop

Return to Summary Table

Table 14-11500. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0CCh + formula

Figure 14-5686. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11501. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_MULT_SA_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Multicast Source Address drop

14.7.3.1.2.273 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_J Register

14.7.3.1.2.273.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_J Register (Offset = 3A0D0h) [reset = 0h]

ALE Dual VLAN Drop

Return to Summary Table

Table 14-11502. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0D0h + formula

Figure 14-5687. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11503. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_DUAL_VLAN_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Dual VLAN drop

14.7.3.1.2.274 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_J Register

14.7.3.1.2.274.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_J Register (Offset = 3A0D4h) [reset = 0h]

ALE Length Error Drop

Return to Summary Table

Table 14-11504. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0D4h + formula

Figure 14-5688. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11505. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_LEN_ERROR_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Length Error drop

14.7.3.1.2.275 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_J Register

14.7.3.1.2.275.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_J Register (Offset = 3A0D8h) [reset = 0h]

ALE IP Next Header Drop

Return to Summary Table

Table 14-11506. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0D8h + formula

Figure 14-5689. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11507. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IP_NEXT_HDR_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Next Header drop

14.7.3.1.2.276 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_J Register

14.7.3.1.2.276.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_J Register (Offset = 3A0DCh) [reset = 0h]

ALE IPV4 Frag Drop

Return to Summary Table

Table 14-11508. Instance Table

Instance Name	Physical Address
CPSW0	0803 A0DCh + formula

Figure 14-5690. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11509. CPSW3_CPSW_NU_CPSW_NU_STAT_ALE_IPV4_FRAG_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE IPV4 Fragment drop

14.7.3.1.2.277 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_J Register

14.7.3.1.2.277.1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_J Register (Offset = 3A140h) [reset = 0h]

IET Receive Assembly Error

Return to Summary Table

Table 14-11510. Instance Table

Instance Name	Physical Address
CPSW0	0803 A140h + formula

Figure 14-5691. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IET_RX_ASSEMBLY_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IET_RX_ASSEMBLY_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IET_RX_ASSEMBLY_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IET_RX_ASSEMBLY_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11511. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_ERROR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_ASSEMBLY_ERROR	R/W	0h	IET Receive Assembly Error

14.7.3.1.2.278 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_J Register

14.7.3.1.2.278.1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_J Register (Offset = 3A144h) [reset = 0h]

IET Receive Assembly Ok

Return to Summary Table

Table 14-11512. Instance Table

Instance Name	Physical Address
CPSW0	0803 A144h + formula

Figure 14-5692. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_ASSEMBLY_OK							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_RX_ASSEMBLY_OK							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_RX_ASSEMBLY_OK							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_OK							
R/W							
0h							

Table 14-11513. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_ASSEMBLY_OK_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_ASSEMBLY_OK	R/W	0h	IET Receive Assembly Ok

14.7.3.1.2.279 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_J Register

14.7.3.1.2.279.1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_J Register (Offset = 3A148h) [reset = 0h]

IET Receive Smd Error

Return to Summary Table

Table 14-11514. Instance Table

Instance Name	Physical Address
CPSW0	0803 A148h + formula

Figure 14-5693. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IET_RX_SMD_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IET_RX_SMD_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IET_RX_SMD_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IET_RX_SMD_ERROR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11515. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_SMD_ERROR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_SMD_ERROR	R/W	0h	IET Receive Smd Error

14.7.3.1.2.280 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_J Register

14.7.3.1.2.280.1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_J Register (Offset = 3A14Ch) [reset = 0h]

IET Receive Frag

Return to Summary Table

Table 14-11516. Instance Table

Instance Name	Physical Address
CPSW0	0803 A14Ch + formula

Figure 14-5694. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Name Register

31	30	29	28	27	26	25	24
IET_RX_FRAG							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_RX_FRAG							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_RX_FRAG							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_RX_FRAG							
R/W							
0h							

Table 14-11517. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_RX_FRAG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_RX_FRAG	R/W	0h	IET Receive Frag

14.7.3.1.2.281 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_J Register

14.7.3.1.2.281.1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_J Register (Offset = 3A150h) [reset = 0h]

IET Transmit Hold

Return to Summary Table

Table 14-11518. Instance Table

Instance Name	Physical Address
CPSW0	0803 A150h + formula

Figure 14-5695. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Name Register

31	30	29	28	27	26	25	24
IET_TX_HOLD							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_TX_HOLD							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_TX_HOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_TX_HOLD							
R/W							
0h							

Table 14-11519. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_HOLD_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_TX_HOLD	R/W	0h	IET Transmit Hold

14.7.3.1.2.282 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_J Register

14.7.3.1.2.282.1 CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_J Register (Offset = 3A154h) [reset = 0h]

IET Transmit Frag

Return to Summary Table

Table 14-11520. Instance Table

Instance Name	Physical Address
CPSW0	0803 A154h + formula

Figure 14-5696. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Name Register

31	30	29	28	27	26	25	24
IET_TX_FRAG							
R/W							
0h							
23	22	21	20	19	18	17	16
IET_TX_FRAG							
R/W							
0h							
15	14	13	12	11	10	9	8
IET_TX_FRAG							
R/W							
0h							
7	6	5	4	3	2	1	0
IET_TX_FRAG							
R/W							
0h							

Table 14-11521. CPSW3_CPSW_NU_CPSW_NU_STAT_IET_TX_FRAG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IET_TX_FRAG	R/W	0h	IET Transmit Frag

14.7.3.1.2.283 CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_J Register

14.7.3.1.2.283.1 CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_J Register (Offset = 3A17Ch) [reset = 0h]

Transmit Memory Protect CRC Error

Return to Summary Table

Table 14-11522. Instance Table

Instance Name	Physical Address
CPSW0	0803 A17Ch + formula

Figure 14-5697. CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-11523. CPSW3_CPSW_NU_CPSW_NU_STAT_TX_MEMORY_PROTECT_ERROR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COUNT	R/W	0h	Transmit Memory Protect CRC Error

14.7.3.1.2.284 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_J_K Register

14.7.3.1.2.284.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_J_K Register (Offset = 3A180h) [reset = 0h]

ENET Port n PRIORITY N Packet Count

Return to Summary Table

Table 14-11524. Instance Table

Instance Name	Physical Address
CPSW0	0803 A180h + formula

Figure 14-5698. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN							
R/W							
0h							

Table 14-11525. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN	R/W	0h	ENET TX Priority Packet Count

14.7.3.1.2.285 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_J_K Register

14.7.3.1.2.285.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_J_K Register (Offset = 3A1A0h) [reset = 0h]

ENET Port n PRIORITY N Packet Byte Count

Return to Summary Table

Table 14-11526. Instance Table

Instance Name	Physical Address
CPSW0	0803 A1A0h + formula

Figure 14-5699. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_BCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_BCNT							
R/W							
0h							

Table 14-11527. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Byte Count

14.7.3.1.2.286 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_J_K Register

14.7.3.1.2.286.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_J_K Register (Offset = 3A1C0h) [reset = 0h]

ENET Port n PRIORITY N Packet Drop Count

Return to Summary Table

Table 14-11528. Instance Table

Instance Name	Physical Address
CPSW0	0803 A1C0h + formula

Figure 14-5700. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_DROP							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_DROP							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP							
R/W							
0h							

Table 14-11529. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP	R/W	0h	ENET Port n PRIORITY N Packet Drop Count

14.7.3.1.2.287 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_K Register

14.7.3.1.2.287.1 CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_K Register (Offset = 3A1E0h) [reset = 0h]

ENET Port n PRIORITY N Packet Drop Byte Count

Return to Summary Table

Table 14-11530. Instance Table

Instance Name	Physical Address
CPSW0	0803 A1E0h + formula

Figure 14-5701. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							

Table 14-11531. CPSW3_CPSW_NU_CPSW_NU_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Drop Byte Count

14.7.3.1.2.288 CPSW3_CPSW_NU_CPTS_IDVER_REG Register

14.7.3.1.2.288.1 CPSW3_CPSW_NU_CPTS_IDVER_REG Register (Offset = 3D000h) [reset = 4E8A010Dh]

Identification and Version Register

Return to Summary Table

Table 14-11532. Instance Table

Instance Name	Physical Address
CPSW0	0803 D000h + formula

Figure 14-5702. CPSW3_CPSW_NU_CPTS_IDVER_REG Name Register

31	30	29	28	27	26	25	24
IDENT							
R							
4E8Ah							

23	22	21	20	19	18	17	16
IDENT							
R							
4E8Ah							

15	14	13	12	11	10	9	8
RTL_VER					MAJOR_VER		
R					R		
0h					1h		

7	6	5	4	3	2	1	0
MINOR_VER							
R							
Dh							

Table 14-11533. CPSW3_CPSW_NU_CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	4E8Ah	Identification value
15:11	RTL_VER	R	0h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	Dh	Minor version value

14.7.3.1.2.289 CPSW3_CPSW_NU_CPTS_CONTROL_REG Register

14.7.3.1.2.289.1 CPSW3_CPSW_NU_CPTS_CONTROL_REG Register (Offset = 3D004h) [reset = 4h]

Time Sync Control Register

Return to Summary Table

Table 14-11534. Instance Table

Instance Name	Physical Address
CPSW0	0803 D004h + formula

Figure 14-5703. CPSW3_CPSW_NU_CPTS_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">TS_SYNC_SEL</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td>TS_GENF_CLR_EN</td><td>TS_RX_NO_EVENT</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>HW8_TS_PUSH_EN</td><td>HW7_TS_PUSH_EN</td><td>HW6_TS_PUSH_EN</td><td>HW5_TS_PUSH_EN</td><td>HW4_TS_PUSH_EN</td><td>HW3_TS_PUSH_EN</td><td>HW2_TS_PUSH_EN</td><td>HW1_TS_PUSH_EN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>TS_PPM_DIR</td><td>TS_COMP_TOG</td><td>MODE</td><td>SEQUENCE_EN</td><td>TSTAMP_EN</td><td>TS_COMP_POLARITY</td><td>INT_TEST</td><td>CPTS_EN</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11535. CPSW3_CPSW_NU_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TS_SYNC_SEL	R/W	0h	TS_SYNC output time stamp counter bit select. 0h TS_SYNC disabled. 1h-Fh TS_SYNC is time stamp counter bits 31 (Fh) down to 17 (1h).
27:18	RESERVED	NONE	0h	Reserved
17	TS_GENF_CLR_EN	R/W	0h	GENF (and ESTF) Clear Enable. 0h A CPTS_GENFn output is not cleared when the associated CPSW_GENF_LENGTH_REG_l[31:0] is cleared to zero. 1h A CPTS_GENFn output is cleared when the associated CPSW_GENF_LENGTH_REG_l[31:0] is cleared to zero.
16	TS_RX_NO_EVENT	R/W	0h	Timestamp Ethernet Receive produces no events. 0h Ethernet receive timesync events enabled. 1h Ethernet receive timesync events disabled.
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable.
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable.
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable.
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable.
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable.

Table 14-11535. CPSW3_CPSW_NU_CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable.
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable.
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable.
7	TS_PPM_DIR	R/W	0h	PPM Correction Direction. 0h Increase the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG) by the PPM value. 1h Decrease the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG and) by the PPM value.
6	TS_COMP_TOG	R/W	0h	Time Stamp Compare Toggle mode. 0h TS_COMP is in non-toggle mode. 1h TS_COMP is in toggle mode.
5	MODE	R/W	0h	64-Bit Mode. 0h The time stamp is 32-bits with the upper 32-bits forced to zero. 1h The time stamp is 64-bits.
4	SEQUENCE_EN	R/W	0h	Sequence Enable. 0h The time stamp value increments with the selected RFTCLK 1h The time stamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc).
3	TSTAMP_EN	R/W	0h	Host Receive Time Stamp Enable. 0h Time stamps are disabled on received packets to host. 1h Time stamps enabled on received packets to host (PCIE_CPTS_CONTROL_REG[0] CPTS_EN must be set).
2	TS_COMP_POLARITY	R/W	1h	TS_COMP Polarity. 0h TS_COMP is asserted low. 1h TS_COMP is asserted high.
1	INT_TEST	R/W	0h	Interrupt Test. When set, this bit allows the raw interrupt to be written to facilitate interrupt test.
0	CPTS_EN	R/W	0h	Time Sync Enable. When disabled (cleared to zero), the RCLK domain is held in reset.

14.7.3.1.2.290 CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register

14.7.3.1.2.290.1 CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register (Offset = 3D008h) [reset = 0h]

RFTCLK Select Register

Return to Summary Table

Table 14-11536. Instance Table

Instance Name	Physical Address
CPSW0	0803 D008h + formula

Figure 14-5704. CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RFTCLK_SEL				
NONE			R/W				
0h			0h				

Table 14-11537. CPSW3_CPSW_NU_CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	RFTCLK_SEL	R/W	0h	Reference clock select. This bit field is used to control an external multiplexer that selects one out of 8 clocks for time sync reference. 0h Selects CPSWHSDIV_CLKOUT2 clock 1h Selects MAINHSDIV_CLKOUT3 clock 2h Selects MCU_CPTS0_RFT_CLK I/O pin 3h Selects CPTS0_RFT_CLK I/O pin 4h Selects MCU_EXT_REFCLK0 I/O pin 5h Selects EXT_REFCLK1 I/O pin 6h Selects PCIE0_TXI0_CLK clock 7h Selects PCIE1_TXI0_CLK clock The RFTCLK_SEL value can be written only when the [0] CPTS_EN and [3] TSTAMP_EN bits are cleared to zero in the CPSW_CPTS_CONTROL_REG register.

14.7.3.1.2.291 CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register

14.7.3.1.2.291.1 CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register (Offset = 3D00Ch) [reset = 0h]

Time Stamp Event Push Register

Return to Summary Table

Table 14-11538. Instance Table

Instance Name	Physical Address
CPSW0	0803 D00Ch + formula

Figure 14-5705. CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
NONE							W
0h							0h

Table 14-11539. CPSW3_CPSW_NU_CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PUSH	W	0h	Time stamp event push. When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads zero.

14.7.3.1.2.292 CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register

14.7.3.1.2.292.1 CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register (Offset = 3D010h) [reset = 0h]

Time Stamp Load Low Value Register

Return to Summary Table

Table 14-11540. Instance Table

Instance Name	Physical Address
CPSW0	0803 D010h + formula

Figure 14-5706. CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 14-11541. CPSW3_CPSW_NU_CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time stamp load low value

14.7.3.1.2.293 CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register

14.7.3.1.2.293.1 CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register (Offset = 3D014h) [reset = 0h]

Time Stamp Load Enable Register

Return to Summary Table

Table 14-11542. Instance Table

Instance Name	Physical Address
CPSW0	0803 D014h + formula

Figure 14-5707. CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
NONE							W
0h							0h

Table 14-11543. CPSW3_CPSW_NU_CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_LOAD_EN	W	0h	Time Stamp Load Enable. Writing a one to this bit enables the time stamp value to be written with the value in CPSW_CPTS_TS_LOAD_VAL_REG/ CPSW_CPTS_TS_LOAD_HIGH_VAL_REG. This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the time stamp (CPSW_CPTS_TS_LOAD_HIGH_VAL_REG) are forced to zero in 32-bit mode.

14.7.3.1.2.294 CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register

14.7.3.1.2.294.1 CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register (Offset = 3D018h) [reset = 0h]

Time Stamp Comparison Low Value Register

Return to Summary Table

Table 14-11544. Instance Table

Instance Name	Physical Address
CPSW0	0803 D018h + formula

Figure 14-5708. CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TS_COMP_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TS_COMP_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TS_COMP_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TS_COMP_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11545. CPSW3_CPSW_NU_CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_VAL	R/W	0h	Time Stamp Comparison Low Value. Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL.

14.7.3.1.2.295 CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register

14.7.3.1.2.295.1 CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register (Offset = 3D01Ch) [reset = 0h]

Time Stamp Comparison Length Register

Return to Summary Table

Table 14-11546. Instance Table

Instance Name	Physical Address
CPSW0	0803 D01Ch + formula

Figure 14-5709. CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TS_COMP_LENGTH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TS_COMP_LENGTH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TS_COMP_LENGTH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TS_COMP_LENGTH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11547. CPSW3_CPSW_NU_CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_LENGTH	R/W	0h	Time Stamp Comparison Length. Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the CPSW_GENF_COMP_LOW_REG_L[31-0] COMP_LOW and CPSW_GENF_COMP_HIGH_REG_L[31-0] COMP_HIGH registers are written.

14.7.3.1.2.296 CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register

14.7.3.1.2.296.1 CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register (Offset = 3D020h) [reset = 0h]

Interrupt Status Register Raw

Return to Summary Table

Table 14-11548. Instance Table

Instance Name	Physical Address
CPSW0	0803 D020h + formula

Figure 14-5710. CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_RAW
NONE							R/W
0h							0h

Table 14-11549. CPSW3_CPSW_NU_CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable). Writable when CPSW_CPTS_CONTROL_REG[1] INT_TEST = 1h A one in this bit indicates that there are one or more events in the event FIFO.

14.7.3.1.2.297 CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register

14.7.3.1.2.297.1 CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register (Offset = 3D024h) [reset = 0h]

Interrupt Status Register Masked

Return to Summary Table

Table 14-11550. Instance Table

Instance Name	Physical Address
CPSW0	0803 D024h + formula

Figure 14-5711. CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>TS_PEND</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-11551. CPSW3_CPSW_NU_CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

14.7.3.1.2.298 CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register

14.7.3.1.2.298.1 CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register (Offset = 3D028h) [reset = 0h]

Interrupt Enable Register

Return to Summary Table

Table 14-11552. Instance Table

Instance Name	Physical Address
CPSW0	0803 D028h + formula

Figure 14-5712. CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
NONE							R/W
0h							0h

Table 14-11553. CPSW3_CPSW_NU_CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

14.7.3.1.2.299 CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register

14.7.3.1.2.299.1 CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register (Offset = 3D02Ch) [reset = 0h]

Time Stamp Comparison Nudge Register

Return to Summary Table

Table 14-11554. Instance Table

Instance Name	Physical Address
CPSW0	0803 D02Ch + formula

Figure 14-5713. CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-11555. CPSW3_CPSW_NU_CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time stamp Comparison Nudge Value. This two's complement number is added to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH value to increase or decrease the TS_COMP length by the CPSW_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_CPTS_TS_COMP_NUDGE_REG value is cleared to zero when the nudge has occurred.

14.7.3.1.2.300 CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register

14.7.3.1.2.300.1 CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register (Offset = 3D030h) [reset = 0h]

Event Pop Register

Return to Summary Table

Table 14-11556. Instance Table

Instance Name	Physical Address
CPSW0	0803 D030h + formula

Figure 14-5714. CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
NONE							W
0h							0h

Table 14-11557. CPSW3_CPSW_NU_CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EVENT_POP	W	0h	Event Pop. When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read from the CPSW_CPTS_EVENT_0_REG to CPSW_CPTS_EVENT_3_REG registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.

14.7.3.1.2.301 CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register

14.7.3.1.2.301.1 CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register (Offset = 3D034h) [reset = 0h]

Event 0 Register

Return to Summary Table

Table 14-11558. Instance Table

Instance Name	Physical Address
CPSW0	0803 D034h + formula

Figure 14-5715. CPSW3_CPSW_NU_CPTS_EVENT_0_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 14-11559. CPSW3_CPSW_NU_CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp. The time stamp is valid for transmit, receive, and time stamp push event types. The time stamp value is not valid for counter roll event types.

14.7.3.1.2.302 CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register

14.7.3.1.2.302.1 CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register (Offset = 3D038h) [reset = 0h]

Event 1 Register

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Table 14-11560. Instance Table

Instance Name	Physical Address
CPSW0	0803 D038h + formula

Figure 14-5716. CPSW3_CPSW_NU_CPTS_EVENT_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
NONE		R	R				
0h		0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EVENT_TYPE				MESSAGE_TYPE			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SEQUENCE_ID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEQUENCE_ID							
R							
0h							

Table 14-11561. CPSW3_CPSW_NU_CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	PREMPT_QUEUE	R	0h	Prempt QUEUE
28:24	PORT_NUMBER	R	0h	Port Number. Indicates the port number (encoded) of an Ethernet event or the encoded hardware time stamp number.

23:20	EVENT_TYPE	R	0h	Time Sync Event Type
				`0h Time Stamp Push Event`
				`1h Time Stamp Rollover Event`
				`2h Time Stamp Half Rollover Event`
				`3h Hardware Time Stamp Push Event`
				`4h Ethernet Receive Event`
				`5h Ethernet Transmit Event`
				`6h Time Stamp Compare Event`
				`7h Host Transmit Event`
				`8h-Fh Reserved`

19:16	MESSAGE_TYPE	R	0h	Message type. The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
15:0	SEQUENCE_ID	R	0h	Sequence ID. The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

14.7.3.1.2.303 CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register

14.7.3.1.2.303.1 CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register (Offset = 3D03Ch) [reset = 0h]

Event 2 Register

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Table 14-11562. Instance Table

Instance Name	Physical Address
CPSW0	0803 D03Ch + formula

Figure 14-5717. CPSW3_CPSW_NU_CPTS_EVENT_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DOMAIN							
R							
0h							

Table 14-11563. CPSW3_CPSW_NU_CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DOMAIN	R	0h	Domain. The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

14.7.3.1.2.304 CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register

14.7.3.1.2.304.1 CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register (Offset = 3D040h) [reset = 0h]

Event 3 Register

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Table 14-11564. Instance Table

Instance Name	Physical Address
CPSW0	0803 D040h + formula

Figure 14-5718. CPSW3_CPSW_NU_CPTS_EVENT_3_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 14-11565. CPSW3_CPSW_NU_CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp. The time stamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode.

14.7.3.1.2.305 CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register

14.7.3.1.2.305.1 CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 3D044h) [reset = 0h]

Time Stamp Load High Value Register

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Table 14-11566. Instance Table

Instance Name	Physical Address
CPSW0	0803 D044h + formula

Figure 14-5719. CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 14-11567. CPSW3_CPSW_NU_CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time Stamp Load high Value. Writing the CPSW_CPTS_TS_LOAD_EN_REG[0] TS_LOAD_EN bit causes the value contained in this register to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode

14.7.3.1.2.306 CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register

14.7.3.1.2.306.1 CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 3D048h) [reset = 0h]

Time Stamp Comparison High Value Register

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Table 14-11568. Instance Table

Instance Name	Physical Address
CPSW0	0803 D048h + formula

Figure 14-5720. CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_HIGH_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_HIGH_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_HIGH_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL							
R/W							
0h							

Table 14-11569. CPSW3_CPSW_NU_CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_HIGH_VAL	R/W	0h	Time Stamp Comparison High Value. Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the [31-0]TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL and CPSW_CPTS_TS_COMP_HIGH_VAL_REG[31-0] TS_COMP_HIGH_VAL. This value is unused in 32-bit mode. The upper 32-bits in CPSW_CPTS_TS_COMP_HIGH_VAL_REG register should be written before the lower 32-bits in the CPSW_CPTS_TS_COMP_VAL_REG register.

14.7.3.1.2.307 CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register

14.7.3.1.2.307.1 CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register (Offset = 3D04Ch) [reset = 0h]

TS Add Value Register

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Table 14-11570. Instance Table

Instance Name	Physical Address
CPSW0	0803 D04Ch + formula

Figure 14-5721. CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADD_VAL		
NONE					R/W		
0h					0h		

Table 14-11571. CPSW3_CPSW_NU_CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADD_VAL	R/W	0h	The ts_add_value[2:0] is added to 1 to comprise the time stamp increment value. The time stamp increment value is added to the current time stamp (time_stamp[63:0]) on each RCLK. The time stamp increment value can be adjusted by nudge and ppm also. The CPSW_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL value may be non-zero in 64-bit mode only.

14.7.3.1.2.308 CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register

14.7.3.1.2.308.1 CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 3D050h) [reset = 0h]

Time Stamp PPM Low Value Register

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Table 14-11572. Instance Table

Instance Name	Physical Address
CPSW0	0803 D050h + formula

Figure 14-5722. CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_PPM_LOW_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_PPM_LOW_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_PPM_LOW_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL							
R/W							
0h							

Table 14-11573. CPSW3_CPSW_NU_CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_PPM_LOW_VAL	R/W	0h	Time Stamp PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen.

14.7.3.1.2.309 CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register

14.7.3.1.2.309.1 CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 3D054h) [reset = 0h]

Time Stamp PPM High Value Register

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Table 14-11574. Instance Table

Instance Name	Physical Address
CPSW0	0803 D054h + formula

Figure 14-5723. CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						TS_PPM_HIGH_VAL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TS_PPM_HIGH_VAL							
R/W							
0h							

Table 14-11575. CPSW3_CPSW_NU_CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TS_PPM_HIGH_VAL	R/W	0h	Time Stamp PPM High Value. This value should be written first (before the low value is written). The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).

14.7.3.1.2.310 CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register

14.7.3.1.2.310.1 CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register (Offset = 3D058h) [reset = 0h]

Time Stamp Nudge Value Register

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Table 14-11576. Instance Table

Instance Name	Physical Address
CPSW0	0803 D058h + formula

Figure 14-5724. CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TS_NUDGE_VAL							
R/W							
0h							

Table 14-11577. CPSW3_CPSW_NU_CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge Value. This two's complement number is added to the CPSW_CPTS_EVENT_0_REG[31-0] TIME_STAMP and CPSW_CPTS_EVENT_3_REG[[31-0] TIME_STAMP value to increase or decrease the time stamp value by the CPSW_CPTS_TS_NUDGE_VAL_REG[7-0] TS_NUDGE_VAL amount. The TS_NUDGE_VAL value is cleared to zero when the nudge has occurred. The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).

14.7.3.1.2.311 CPSW3_CPSW_NU_CPTS_TS_CONFIG Register

14.7.3.1.2.311.1 CPSW3_CPSW_NU_CPTS_TS_CONFIG Register (Offset = 3D0D0h) [reset = 2002h]

Time Stamp Configuration Read

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Table 14-11578. Instance Table

Instance Name	Physical Address
CPSW0	0803 D0D0h + formula

Figure 14-5725. CPSW3_CPSW_NU_CPTS_TS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EVNT_FIFO_DEPTH							
R							
20h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_GENF							
R							
2h							

Table 14-11579. CPSW3_CPSW_NU_CPTS_TS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	EVNT_FIFO_DEPTH	R	20h	The Event FIFO Depth
7:0	NUM_GENF	R	2h	The number of CPTS GENF outputs

14.7.3.1.2.312 CPSW3_CPSW_NU_ALE_MOD_VER Register

14.7.3.1.2.312.1 CPSW3_CPSW_NU_ALE_MOD_VER Register (Offset = 3E000h) [reset = 291105h]

The Module and Version Register identifies the module identifier and revision of the ALE_3g512ie module.

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Table 14-11580. Instance Table

Instance Name	Physical Address
CPSW0	0803 E000h + formula

Figure 14-5726. CPSW3_CPSW_NU_ALE_MOD_VER Name Register

31	30	29	28	27	26	25	24
MODULE_ID							
R							
29h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
29h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VERSION					MAJOR_REVISION		
R					R		
2h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM_REVISION		MINOR_REVISION					
R		R					
0h		5h					

Table 14-11581. CPSW3_CPSW_NU_ALE_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODULE_ID	R	29h	ALE_3g512ie module ID.
15:11	RTL_VERSION	R	2h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	5h	Minor Revision.

14.7.3.1.2.313 CPSW3_CPSW_NU_ALE_ALE_STATUS Register

14.7.3.1.2.313.1 CPSW3_CPSW_NU_ALE_ALE_STATUS Register (Offset = 3E004h) [reset = 80000400h]

The ALE status provides information on the ALE configuration and state. The ~iramdepth is used to determine how IPv6 entries are stored in the table. IPv6 entries are stored in two entries where IPv6 Entry hi is designated by the odd slice index and lo is designated by the even slice index. The slice index is above the ram depth like {SlixeIndex,RamIndex}. So for a 64 deep RAM index of 0x005, the Hi portion of the IPv6 entry is located at 0x005|0x040 and the Lo portion is located at 0x005&(~0x040).

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Table 14-11582. Instance Table

Instance Name	Physical Address
CPSW0	0803 E004h + formula

Figure 14-5727. CPSW3_CPSW_NU_ALE_ALE_STATUS Name Register

31	30	29	28	27	26	25	24
UREGANDREGMSK12	UREGANDREGMSK08	RESERVED					
R	R	NONE					
1h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POLCNTDIV8							
R							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMDEPTH128	RAMDEPTH32	RESERVED	KLUENTRIES				
R	R	NONE	R				
0h	0h	0h	0h				

Table 14-11583. CPSW3_CPSW_NU_ALE_ALE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UREGANDREGMSK12	R	1h	When set, the unregistered multicast field is a mask versus an index on 12 bit boundary in the ALE table.
30	UREGANDREGMSK08	R	0h	When set, the unregistered multicast field is a mask versus an index on 8 bit boundary in the ALE table.
29:16	RESERVED	NONE	0h	Reserved
15:8	POLCNTDIV8	R	4h	This is the number of Classifiers the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.
7	RAMDEPTH128	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both ramdepth128 and ramdepth32 are zero the depth is 64.
6	RAMDEPTH32	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both ramdepth128 and ramdepth32 are zero the depth is 64.
5	RESERVED	NONE	0h	Reserved
4:0	KLUENTRIES	R	0h	This is the number of table entries total divided by 1024. A value of 1 indicates 1024 table entries. A value of 8 indicates 8192 table entries.

14.7.3.1.2.314 CPSW3_CPSW_NU_ALE_ALE_CONTROL Register

14.7.3.1.2.314.1 CPSW3_CPSW_NU_ALE_ALE_CONTROL Register (Offset = 3E008h) [reset = 0h]

The ALE Control Register is used to set the ALE modes used for all ports.

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Table 14-11584. Instance Table

Instance Name	Physical Address
CPSW0	0803 E008h + formula

Figure 14-5728. CPSW3_CPSW_NU_ALE_ALE_CONTROL Name Register

31	30	29	28	27	26	25	24
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NOW	RESERVED			MIRROR_DP	
R/W	R/W	R/W	NONE			R/W	
0h	0h	0h	0h			0h	
23	22	21	20	19	18	17	16
UPD_BW_CTRL			RESERVED			MIRROR_TOP	
R/W			NONE			R/W	
0h			0h			0h	
15	14	13	12	11	10	9	8
UPD_STATIC	LRN_HOST_DST	UVLAN_NO_LEARN	MIRROR_MEN	MIRROR_DEN	MIRROR_SEN	RESERVED	EN_HOST_UNI_FLOOD
R/W	R/W	R/W	R/W	R/W	R/W	NONE	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
LEARN_NO_VLANID	ENABLE_VID0_MODE	ENABLE_OUI_DENY	ENABLE_BYPASS	BCAST_MCAST_CTL	ALE_VLAN_AWARE	ENABLE_AUTH_MODE	ENABLE_RATE_LIMIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11585. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_ALE	R/W	0h	Enable ALE 0 - Drop all packets 1 - Enable ALE packet processing
30	CLEAR_TABLE	R/W	0h	Clear ALE address table - Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.
29	AGE_OUT_NOW	R/W	0h	Age Out Address Table Now - Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.
28:26	RESERVED	NONE	0h	Reserved
25:24	MIRROR_DP	R/W	0h	Mirror Destination Port - This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the ~imirror_top port.

Table 14-11585. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:21	UPD_BW_CTRL	R/W	0h	The ~iupd_bw_ctrl field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the ~iupd_bw_ctrl can be programmed more aggressive. If the ~iupd_bw_ctrl is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. 0 - 350Mhz, 5M 1 - 359Mhz, 11M 2 - 367Mhz, 16M 3 - 375Mhz, 22M 4 - 384Mhz, 28M 5 - 392Mhz, 34M 6 - 400Mhz, 39M 7 - 409Mhz, 45M
20:18	RESERVED	NONE	0h	Reserved
17:16	MIRROR_TOP	R/W	0h	Mirror To Port - This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.
15	UPD_STATIC	R/W	0h	Update Static Entries - A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be '0' for most switch configurations.
14	LRN_HOST_DST	R/W	0h	Learn Host Destination - This field is set to only learn unicast packet source addresses that are destined to the host port. This bit is only valid for 3 port switches and allows the ALE table to only contain addresses the host port is concerned about. This bit is affectively disabled when ~ien_host_uni_flood is set since any unknown unicast is also sent to the host port for extended bridging operations.
13	UVLAN_NO_LEARN	R/W	0h	Unknown VLAN No Learn - This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.
12	MIRROR_MEN	R/W	0h	Mirror Match Entry Enable - This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the ~imirror_midx entry index will have that traffic also sent to the ~imirror_top port.
11	MIRROR_DEN	R/W	0h	Mirror Destination Port Enable - This field enables the destination port mirror option. When this bit is set any traffic destined for the ~imirror_dp port will have its transmit traffic also sent to the ~imirror_top port.
10	MIRROR_SEN	R/W	0h	Mirror Source Port Enable - This field enables the source port mirror option. When this bit is set any port with the ~ipX_mirror_sp set in the ALE Port Control registers set will have its received traffic also sent to the ~imirror_top port.
9	RESERVED	NONE	0h	Reserved
8	EN_HOST_UNI_FLOOD	R/W	0h	Unknown unicast packets flood to host 0 - unknown unicast packets are not sent to the host 1 - unknown unicast packets flood to host port as well as other ports
7	LEARN_NO_VLANID	R/W	0h	Learn No VID - 0 - VID is learned with the source address 1 - VID is not learned with the source address (source address is not tied to VID). Determines the entry type.
6	ENABLE_VID0_MODE	R/W	0h	Enable VLAN ID = 0 Mode 0 - Process the priority tagged packet with VID = PORT_VLAN[11:0]. 1 - Process the priority tagged packet with VID = 0.

Table 14-11585. CPSW3_CPSW_NU_ALE_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ENABLE_OUI_DENY	R/W	0h	Enable OUI Deny Mode - When set, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.
4	ENABLE_BYPASS	R/W	0h	ALE Bypass - When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port. 0 - no bypass 1 - bypass the ALE
3	BCAST_MCAST_CTL	R/W	0h	Rate Limit Transmit mode 0 - Broadcast and multicast rate limit counters are received port based 1 - Broadcast and multicast rate limit counters are transmit port based
2	ALE_VLAN_AWARE	R/W	0h	ALE VLAN Aware - Determines how traffic is forwarded using VLAN rules. 0 - Simple switch rules, packets forwarded to all ports for unknown destinations. 1 - VLAN Aware rules, packets forwarded based on VLAN members
1	ENABLE_AUTH_MODE	R/W	0h	Enable MAC Authorization Mode - Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set). 0 - The ALE is not in MAC authorization mode 1 - The ALE is in MAC authorization mode
0	ENABLE_RATE_LIMIT	R/W	0h	Enable Broadcast and Multicast Rate Limit 0 - Broadcast/Multicast rates not limited 1 - Broadcast/Multicast packet reception limited to the port control register rate limit fields.

14.7.3.1.2.315 CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register

14.7.3.1.2.315.1 CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register (Offset = 3E00Ch) [reset = 0h]

The ALE Control 2 Register is used to set the extended features used for all ports.

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Table 14-11586. Instance Table

Instance Name	Physical Address
CPSW0	0803 E00Ch + formula

Figure 14-5729. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Name Register

31	30	29	28	27	26	25	24
TRK_EN_DST	TRK_EN_SRC	TRK_EN_PRI	RESERVED	TRK_EN_IVLAN	RESERVED	TRK_EN_SIP	TRK_EN_DIP
R/W	R/W	R/W	NONE	R/W	NONE	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

23	22	21	20	19	18	17	16
DROP_BADLEN	NODROP_SRCMCST	DEFNOFRAG	DEFLMTNXTHDR	RESERVED	TRK_BASE		
R/W	R/W	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		

15	14	13	12	11	10	9	8
MULTIHOST	RESERVED						MIRROR_MIDX
R/W	NONE						R/W
0h	0h						0h

7	6	5	4	3	2	1	0
MIRROR_MIDX							
R/W							
0h							

Table 14-11587. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK_EN_DST	R/W	0h	Trunk Enable Destination Address - This field enables the destination MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
30	TRK_EN_SRC	R/W	0h	Trunk Enable Source Address - This field enables the source MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
29	TRK_EN_PRI	R/W	0h	Trunk Enable Priority - This field enables the VLAN Priority bits to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used.
28	RESERVED	NONE	0h	Reserved
27	TRK_EN_IVLAN	R/W	0h	Trunk Enable Inner VLAN - This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
26	RESERVED	NONE	0h	Reserved
25	TRK_EN_SIP	R/W	0h	Trunk Enable Source IP Address - This field enables the source IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.

Table 14-11587. CPSW3_CPSW_NU_ALE_ALE_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	TRK_EN_DIP	R/W	0h	Trunk Enable Destination IP Address - This field enables the destination IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
23	DROP_BADLEN	R/W	0h	Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.
22	NODROP_SRCMCST	R/W	0h	No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.
21	DEFNOFRAG	R/W	0h	Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.
20	DEFLMTNXTHDR	R/W	0h	Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the ~iALE_NXT_HDR register values.
19	RESERVED	NONE	0h	Reserved
18:16	TRK_BASE	R/W	0h	Trunk Base - This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the ~itrk_en_dst, ~itrk_en_src, ~itrk_en_pri and ~itrk_en_vlan are '0', this value is used as the distribution index. That is a '0' will select the 1st bit of an 'N' link trunk, a '1' will select the second, etc. Below is the distribution across the trunk links. The first number in the ~iitalic sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0 will go to the base port (0), hash result 1 will go to the highest port of the trunk group (2), hash result 2 will go to the middle port (1), etc. 1 - ~i00000000 2 - ~i01010101 3 - ~i02102102 4 - ~i03210321
15	MULTIHOST	R/W	0h	The ~multihost allows host traffic to be sent bact to the host if the DA is market for the host port.
14:9	RESERVED	NONE	0h	Reserved
8:0	MIRROR_MIDX	R/W	0h	Mirror Index - This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the ~imirror_top port. That is any VLAN, ONU or address with or withou VLAN can be selected for traffic mirroring.

14.7.3.1.2.316 CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register

14.7.3.1.2.316.1 CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register (Offset = 3E010h) [reset = 0h]

The ALE Prescale Register is used to set the Broadcast and Multicast rate limiting prescaler value.

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Table 14-11588. Instance Table

Instance Name	Physical Address
CPSW0	0803 E010h + formula

Figure 14-5730. CPSW3_CPSW_NU_ALE_ALE_PRESCALE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ALE_PRESCALE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ALE_PRESCALE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ALE_PRESCALE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11589. CPSW3_CPSW_NU_ALE_ALE_PRESCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	ALE_PRESCALE	R/W	0h	ALE Prescale - The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 0x10. The prescaler is off when the value is zero.

14.7.3.1.2.317 CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register

14.7.3.1.2.317.1 CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register (Offset = 3E014h) [reset = 0h]

The ALE Aging Control sets the aging interval which will cause periodic aging to occur. This value specifies the minimum time between aging starts.

Return to Summary Table

Table 14-11590. Instance Table

Instance Name	Physical Address
CPSW0	0803 E014h + formula

Figure 14-5731. CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Name Register

31	30	29	28	27	26	25	24
PRESCALE_2_DISABLE	PRESCALE_1_DISABLE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ALE_AGING_TIMER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ALE_AGING_TIMER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ALE_AGING_TIMER							
R/W							
0h							

Table 14-11591. CPSW3_CPSW_NU_ALE_ALE_AGING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESCALE_2_DISABLE	R/W	0h	ALE Prescaler 2 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
30	PRESCALE_1_DISABLE	R/W	0h	ALE Prescaler 1 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
29:24	RESERVED	NONE	0h	Reserved
23:0	ALE_AGING_TIMER	R/W	0h	ALE Aging Timer - This field specifies the number of clock cycles times 1,000,000 between aging operations.

14.7.3.1.2.318 CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register

14.7.3.1.2.318.1 CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register (Offset = 3E01Ch) [reset = 0h]

The ALE Next Header is used to limit the IPv6 Next header or IPv4 Protocol values found in the IP header. It is enabled via the ~iLmtNxtHdr bit in the VLAN entry. All four ~iip_nxt_hdr0-3 are compared when enabled, so if only one is required, set them all to the one value to be tested.

Return to Summary Table

Table 14-11592. Instance Table

Instance Name	Physical Address
CPSW0	0803 E01Ch + formula

Figure 14-5732. CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Name Register

31	30	29	28	27	26	25	24
IP_NXT_HDR3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IP_NXT_HDR2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IP_NXT_HDR1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IP_NXT_HDR0							
R/W							
0h							

Table 14-11593. CPSW3_CPSW_NU_ALE_ALE_NXT_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IP_NXT_HDR3	R/W	0h	The ~iip_nxt_hdr3 is the forth protocol or next header compared when enabled.
23:16	IP_NXT_HDR2	R/W	0h	The ~iip_nxt_hdr2 is the third protocol or next header compared when enabled.
15:8	IP_NXT_HDR1	R/W	0h	The ~iip_nxt_hdr1 is the second protocol or next header compared when enabled.
7:0	IP_NXT_HDR0	R/W	0h	The ~iip_nxt_hdr0 is the first protocol or next header compared when enabled.

14.7.3.1.2.319 CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register

14.7.3.1.2.319.1 CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register (Offset = 3E020h) [reset = 0h]

The ALE table control register is used to read or write that ALE table entries. After writing to this register any read or write to any ALE register will be stalled until the read or write operation completes.

Return to Summary Table

Table 14-11594. Instance Table

Instance Name	Physical Address
CPSW0	0803 E020h + formula

Figure 14-5733. CPSW3_CPSW_NU_ALE_ALE_TBLCTL Name Register

31	30	29	28	27	26	25	24
TABLEWR	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TABLEIDX
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
TABLEIDX							
R/W							
0h							

Table 14-11595. CPSW3_CPSW_NU_ALE_ALE_TBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TABLEWR	R/W	0h	Table Write - This bit is used to write the table words to the lookup table. 0 - Table Read Operation is performed. The contents of the ~b TABLEIDX entry will be read into the ~b ALE_TBLWx registers 1 - Table write operation is performed. This will take the current contents from the ~b ALE_TBLWx registers and write them to the table at the specified ~b TABLEIDX.
30:9	RESERVED	NONE	0h	Reserved
8:0	TABLEIDX	R/W	0h	The table index is used to determine which lookup table entry is read or written.

14.7.3.1.2.320 CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register

14.7.3.1.2.320.1 CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register (Offset = 3E034h) [reset = 0h]

The ALE Table Word 2 is the most significant word of an ALE table entry.

Return to Summary Table

Table 14-11596. Instance Table

Instance Name	Physical Address
CPSW0	0803 E034h + formula

Figure 14-5734. CPSW3_CPSW_NU_ALE_ALE_TBLW2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TABLEWRD2						
NONE	R/W						
0h	0h						

Table 14-11597. CPSW3_CPSW_NU_ALE_ALE_TBLW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	TABLEWRD2	R/W	0h	Table Entry bits [70:64]

14.7.3.1.2.321 CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register

14.7.3.1.2.321.1 CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register (Offset = 3E038h) [reset = 0h]

The ALE Table Word 1 is the middle word of an ALE table entry.

Return to Summary Table

Table 14-11598. Instance Table

Instance Name	Physical Address
CPSW0	0803 E038h + formula

Figure 14-5735. CPSW3_CPSW_NU_ALE_ALE_TBLW1 Name Register

31	30	29	28	27	26	25	24
TABLEWRD1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TABLEWRD1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TABLEWRD1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TABLEWRD1							
R/W							
0h							

Table 14-11599. CPSW3_CPSW_NU_ALE_ALE_TBLW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD1	R/W	0h	Table Entry bits [63:32]

14.7.3.1.2.322 CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register

14.7.3.1.2.322.1 CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register (Offset = 3E03Ch) [reset = 0h]

The ALE Table Word 0 is the least significant word of an ALE table entry.

Return to Summary Table

Table 14-11600. Instance Table

Instance Name	Physical Address
CPSW0	0803 E03Ch + formula

Figure 14-5736. CPSW3_CPSW_NU_ALE_ALE_TBLW0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TABLEWRD0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TABLEWRD0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TABLEWRD0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TABLEWRD0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11601. CPSW3_CPSW_NU_ALE_ALE_TBLW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD0	R/W	0h	Table Entry bits [31:0]

14.7.3.1.2.323 CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_J Register

14.7.3.1.2.323.1 CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_J Register (Offset = 3E040h) [reset = 0h]

The ALE Port Control Register sets the port specific modes of operation.

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Table 14-11602. Instance Table

Instance Name	Physical Address
CPSW0	0803 E040h + formula

Figure 14-5737. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Name Register

31	30	29	28	27	26	25	24
I0_REG_P0_BCAST_LIMIT							
R/W							
0h							
23	22	21	20	19	18	17	16
I0_REG_P0_MCAST_LIMIT							
R/W							
0h							
15	14	13	12	11	10	9	8
I0_REG_P0_DROP_DOUBLE_VLAN	I0_REG_P0_DROP_DUAL_VLAN	I0_REG_P0_MACONLY_CAF	I0_REG_P0_DIS_PAUTHMOD	I0_REG_P0_MACONLY	I0_REG_P0_TRUNKEN	I0_REG_P0_TRUNKNUM	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
7	6	5	4	3	2	1	0
I0_REG_P0_MIRROR_SP	RESERVED	I0_REG_P0_NO_SA_UPDATE	I0_REG_P0_NO_LEARN	I0_REG_P0_VID_INGRESS_CHECK	I0_REG_P0_DROP_UN_TAGGED	I0_REG_P0_PORTSTATE	
R/W	NONE	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-11603. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	I0_REG_P0_BCAST_LIMIT	R/W	0h	Broadcast Packet Rate Limit. Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23:16	I0_REG_P0_MCAST_LIMIT	R/W	0h	Multicast Packet Rate Limit. Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.The Iy_REG_Py_MCAST_LIMIT bit field is the number of Multicast packets that will be forwarded per CPSW_ALE_PRESCALE time.
15	I0_REG_P0_DROP_DOUBLE_VLAN	R/W	0h	Drop Double VLAN. When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.
14	I0_REG_P0_DROP_DUAL_VLAN	R/W	0h	Drop Dual VLAN - When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.

Table 14-11603. CPSW3_CPSW_NU_ALE_I0_ALE_PORTCTL0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	I0_REG_P0_MACONLY_CAF	R/W	0h	Mac Only Copy All Frames. When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with Iy_REG_Py_MACONLY set.
12	I0_REG_P0_DIS_PAUTHMOD	R/W	0h	Disable Port authorization. When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.
11	I0_REG_P0_MACONLY	R/W	0h	MAC Only. When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the Iy_REG_Py_MACONLY bit set and the Iy_REG_Py_NO_LEARN also set. If Iy_REG_Py_MACONLY bit is set and the Iy_REG_Py_NO_LEARN is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that The host can broadcast to all ports including MacOnly ports in this mode.
10	I0_REG_P0_TRUNKEN	R/W	0h	Trunk Enable. This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the Iy_REG_Py_TRUNKEN its set and having the same Iy_REG_Py_TRUNKNUM will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never trasnmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry.
9:8	I0_REG_P0_TRUNKNUM	R/W	0h	Trunk Number. This field is used as the trunk number when the Iy_REG_Py_TRUNKEN is also set. Ports with the same trunk number that have the Iy_REG_Py_TRUNKEN also set will have traffic distributed within the trunk based on the result of the hash function descrived above.
7	I0_REG_P0_MIRROR_SP	R/W	0h	Mirror Source Port. This field enables the source port mirror option. When this bit is set any traffic received on the port with the Iy_REG_Py_MIRROR_SP bit set will have its received traffic also sent to the MIRROR_TOP port.
6	RESERVED	NONE	0h	Reserved
5	I0_REG_P0_NO_SA_UPDATE	R/W	0h	No Source Address Update. When set will not update the source addresses for this port.
4	I0_REG_P0_NO_LEARN	R/W	0h	No Learn. When set will not learn the source addresses for this port.
3	I0_REG_P0_VID_INGRESS_CHECK	R/W	0h	VLAN Ingress Check. When set if a packet received is not a member of the VLAN, the packet will be dropped.
2	I0_REG_P0_DROP_UN_TAGGED	R/W	0h	If Drop Untagged. When set will drop packets without a VLAN tag.

1:0	I0_REG_P0_PORTSTATE	R/W	0h	Port State. Defines the current port state used for lookup operations.
				`0h Disabled`
				`1h Blocked`
				`2h Learning`
				`3h Forwarding`

14.7.3.1.2.324 CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register

14.7.3.1.2.324.1 CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register (Offset = 3E090h) [reset = 0h]

The ALE Unknown VLAN Member Mask Register is used to specify the member list for unknown VLAN ID.

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Table 14-11604. Instance Table

Instance Name	Physical Address
CPSW0	0803 E090h + formula

Figure 14-5738. CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_MEMBER_LIST		
NONE					R/W		
0h					0h		

Table 14-11605. CPSW3_CPSW_NU_ALE_ALE_UVLAN_MEMBER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_MEMBER_LIST	R/W	0h	Unknown VLAN Member List - Each bit represents the port member status for unknown VLANs.

14.7.3.1.2.325 CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register

14.7.3.1.2.325.1 CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register (Offset = 3E094h) [reset = 0h]

The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is used to specify which egress ports unregistered multicast addresses egress for the unregistered VLAN ID.

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Table 14-11606. Instance Table

Instance Name	Physical Address
CPSW0	0803 E094h + formula

Figure 14-5739. CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_UNREG_MCAST_FLOOD_MASK		
NONE					R/W		
0h					0h		

Table 14-11607. CPSW3_CPSW_NU_ALE_ALE_UVLAN_URCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_UNREG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Unregister Multicast Flood Mask - Each bit represents the port to which unregistered multicast are sent for unregistered VLANs.

14.7.3.1.2.326 CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register

14.7.3.1.2.326.1 CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register (Offset = 3E098h) [reset = 0h]

The ALE Unknown VLAN Registered Multicast Flood Mask Register is used to specify which egress ports registered multicast addresses egress for the unregistered VLAN ID.

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Table 14-11608. Instance Table

Instance Name	Physical Address
CPSW0	0803 E098h + formula

Figure 14-5740. CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_REG_MCAST_FLOOD_MASK		
NONE					R/W		
0h					0h		

Table 14-11609. CPSW3_CPSW_NU_ALE_ALE_UVLAN_RMCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_REG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Register Multicast Flood Mask - Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs.

14.7.3.1.2.327 CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register

14.7.3.1.2.327.1 CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register (Offset = 3E09Ch) [reset = 0h]

The ALE Unknown VLAN force Untagged Egress Mask Register is used to specify which egress ports the VLAN ID will be removed.

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Table 14-11610. Instance Table

Instance Name	Physical Address
CPSW0	0803 E09Ch + formula

Figure 14-5741. CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_FORCE_UNTAGGED_EGRESS		
NONE					R/W		
0h					0h		

Table 14-11611. CPSW3_CPSW_NU_ALE_ALE_UVLAN_UNTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_FORCE_UNTAGGED_EGRESS	R/W	0h	Unknown VLAN Force Untagged Egress Mask - Each bit represents the port where the VLAN will be removed for unregistered VLANs.

14.7.3.1.2.328 CPSW3_CPSW_NU_ALE_ALE_FAST_LUT Register

14.7.3.1.2.328.1 CPSW3_CPSW_NU_ALE_ALE_FAST_LUT Register (Offset = 3E0B4h) [reset = 0h]

The Fast LUT registers allows the ports to be placed in Fast LUT mode.

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Table 14-11612. Instance Table

Instance Name	Physical Address
CPSW0	0803 E0B4h + formula

Figure 14-5742. CPSW3_CPSW_NU_ALE_ALE_FAST_LUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					FAST_LUT		
NONE					R/W		
0h					0h		

Table 14-11613. CPSW3_CPSW_NU_ALE_ALE_FAST_LUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FAST_LUT	R/W	0h	The ~Fast_LUT field allows any port to be Fast_LUT mode, which will cause all lookup operations to start based on DA/SA and VLAN only. That is any data beyong the first 32 are not used in the lookup process.

14.7.3.1.2.329 CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register

14.7.3.1.2.329.1 CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register (Offset = 3E0B8h) [reset = 0h]

The ALE Statistic Output Diagnostic Register allows the output statistics to diagnose the SW counters. This register is for diagnostice only.

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Table 14-11614. Instance Table

Instance Name	Physical Address
CPSW0	0803 E0B8h + formula

Figure 14-5743. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
PBCAST_DIAG	RESERVED					PORT_DIAG	
R/W	NONE					R/W	
0h	0h					0h	

7	6	5	4	3	2	1	0
RESERVED				STAT_DIAG			
NONE				R/W			
0h				0h			

Table 14-11615. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	PBCAST_DIAG	R/W	0h	When set and the ~iport_diag is set to zero, will allow all ports to see the same stat diagnostic increment.
14:10	RESERVED	NONE	0h	Reserved
9:8	PORT_DIAG	R/W	0h	The port selected that a received packet will cause the selected error to increment
7:4	RESERVED	NONE	0h	Reserved

Table 14-11615. CPSW3_CPSW_NU_ALE_ALE_STAT_DIAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	STAT_DIAG	R/W	0h	When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port. 0: Disabled 1: Destination Equal Source Drop Stat will count 2: VLAN Ingress Check Drop Stat will count 3: Source Multicast Drop Stat will count 4: Dual VLAN Drop Stat will count 5: Ether Type length error Drop Stat will count 6: Next Hop Limit Drop Stat will count 7: IPv4 Fragment Drop Stat will count 8: Classifier Hit Stat will count 9: Classifier Red Drop Stat will count 10: Classifier Yellow Drop Stat will count 11: ALE Overflow Drop Stat will count 12: Rate Limit Drop Stat will count 13: Blocked Address Drop Stat will count 14: Secure Address Drop Stat will count 15: Authorization Drop Stat will count.

14.7.3.1.2.330 CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register

14.7.3.1.2.330.1 CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register (Offset = 3E0BCh) [reset = 0h]

The ALE OAM Control allows ports to be put into OAM Loopback, only non-supervisor packet are looped back to the source port.

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Table 14-11616. Instance Table

Instance Name	Physical Address
CPSW0	0803 E0BCh + formula

Figure 14-5744. CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OAM_LB_CTRL		
NONE					R/W		
0h					0h		

Table 14-11617. CPSW3_CPSW_NU_ALE_ALE_OAM_LB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OAM_LB_CTRL	R/W	0h	The ~ioam_lb_ctrl allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an egressop of 0xFF which swaps the source and destination address. BPDUs will still flow through as normal so that OAM can be remotly requested and disabled.

14.7.3.1.2.331 CPSW3_CPSW_NU_ALE_EGRESSOP Register

14.7.3.1.2.331.1 CPSW3_CPSW_NU_ALE_EGRESSOP Register (Offset = 3E0FCh) [reset = 0h]

The Egress Operation register allows enabled classifiers with any match like IPSA or IPDA match to use the CPSW Egress Packet Operations Inter VLAN Routing sub functions. If the packet was destined for the host or is destined to any port without any errors, but matches a clasifier that has a programmed egress opcode, it will be forwarded to the destination ports where the destination ports will use the thier egress opcode entry to modify the packet. InterVLAN Routing and mirroring need to be understood, they are orthogonal functions. Care must be taken not to violate VLAN rules as this can redirect packets based on classifier matches.

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Table 14-11618. Instance Table

Instance Name	Physical Address
CPSW0	0803 E0FCh + formula

Figure 14-5745. CPSW3_CPSW_NU_ALE_EGRESSOP Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">EGRESS_OP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">EGRESS_TRK</td><td>TTL_CHECK</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">DEST_PORTS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-11619. CPSW3_CPSW_NU_ALE_EGRESSOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EGRESS_OP	R/W	0h	The Egress Operation defines the operation performed by the CPSW Egress Packet Operations 0: NOP : 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load. 0xff: Swap SA and DA of packet, this is intended to allow OAM diagnostics for a link.
23:21	EGRESS_TRK	R/W	0h	The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.
20	TTL_CHECK	R/W	0h	The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.
19:3	RESERVED	NONE	0h	Reserved

Table 14-11619. CPSW3_CPSW_NU_ALE_EGRESSOP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DEST_PORTS	R/W	0h	The Destination Ports is a list of the ports the classified packet will be set to. If a destination is a Trunk, all the port bits for that trunck must be set.

14.7.3.1.2.332 CPSW3_CPSW_NU_ALE_POLICECFG0 Register

14.7.3.1.2.332.1 CPSW3_CPSW_NU_ALE_POLICECFG0 Register (Offset = 3E100h) [reset = 0h]

The Policing Config 0 holds the port, frame priority and ONU address index as well as match enables for port, frame priority and ONU address matching.

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Table 14-11620. Instance Table

Instance Name	Physical Address
CPSW0	0803 E100h + formula

Figure 14-5746. CPSW3_CPSW_NU_ALE_POLICECFG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PORT_MEN</td><td>TRUNKID</td><td colspan="3">RESERVED</td><td colspan="2">PORT_NUM</td><td>RESERVED</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="3">NONE</td><td colspan="2">R/W</td><td>NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td>PRI_MEN</td><td colspan="3">PRI_VAL</td></tr>
<tr><td colspan="4">NONE</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>ONU_MEN</td><td colspan="6">RESERVED</td><td>ONU_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ONU_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11621. CPSW3_CPSW_NU_ALE_POLICECFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PORT_MEN	R/W	0h	Port Match Enable - Enabled port match for the selected policing/classifier entry
30	TRUNKID	R/W	0h	Trunk ID - When set indicates the port number is a trunk group.
29:27	RESERVED	NONE	0h	Reserved
26:25	PORT_NUM	R/W	0h	Port Number - Specifies the port address to match for the selected policing/classifier entry
24:20	RESERVED	NONE	0h	Reserved
19	PRI_MEN	R/W	0h	Priority Match Enable - Enables frame priority match for the selected policing/classifier entry
18:16	PRI_VAL	R/W	0h	Priority Value - Specifies the frame priority to match for the selected policing/classifier entry
15	ONU_MEN	R/W	0h	OUI Match Enable - Enables frame ONU address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	ONU_INDEX	R/W	0h	OUI Table Entry Index - Specifies the ALE ONU address lookup table index to match for the selected policing/classifier entry

14.7.3.1.2.333 CPSW3_CPSW_NU_ALE_POLICECFG1 Register

14.7.3.1.2.333.1 CPSW3_CPSW_NU_ALE_POLICECFG1 Register (Offset = 3E104h) [reset = 0h]

The Policing Config 1 holds the match enable/match index for the L2 Destination and L2 source addresses

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Table 14-11622. Instance Table

Instance Name	Physical Address
CPSW0	0803 E104h + formula

Figure 14-5747. CPSW3_CPSW_NU_ALE_POLICECFG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DST_MEN</td><td colspan="6">RESERVED</td><td>DST_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DST_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>SRC_MEN</td><td colspan="6">RESERVED</td><td>SRC_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SRC_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11623. CPSW3_CPSW_NU_ALE_POLICECFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DST_MEN	R/W	0h	Destination Address Match Enable - Enables frame L2 destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	DST_INDEX	R/W	0h	Destination Address Table Entry Index - Specifies the ALE L2 destination address lookup table index to match for the selected policing/classifier entry
15	SRC_MEN	R/W	0h	Source Address Match Enable - Enables frame L2 source address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	SRC_INDEX	R/W	0h	Source Address Table Entry Index - Specifies the ALE L2 source address lookup table index to match for the selected policing/classifier entry

14.7.3.1.2.334 CPSW3_CPSW_NU_ALE_POLICECFG2 Register

14.7.3.1.2.334.1 CPSW3_CPSW_NU_ALE_POLICECFG2 Register (Offset = 3E108h) [reset = 0h]

The Policing Config 2 holds the match enable/match index for the Outer VLAN and Inner VLAN addresses

Return to Summary Table

Table 14-11624. Instance Table

Instance Name	Physical Address
CPSW0	0803 E108h + formula

Figure 14-5748. CPSW3_CPSW_NU_ALE_POLICECFG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>OVLAN_MEN</td><td colspan="6">RESERVED</td><td>OVLAN_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OVLAN_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>IVLAN_MEN</td><td colspan="6">RESERVED</td><td>IVLAN_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IVLAN_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11625. CPSW3_CPSW_NU_ALE_POLICECFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVLAN_MEN	R/W	0h	Outer VLAN Match Enable - Enables frame Outer VLAN address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	OVLAN_INDEX	R/W	0h	Outer VLAN Table Entry Index - Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/ classifier entry Note this index assumes the VLANID is in the packet, it does not use the port VLAN if the packet in untagged or priority tagged.
15	IVLAN_MEN	R/W	0h	Inner VLAN Match Enable - Enables frame Inner VLAN address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	IVLAN_INDEX	R/W	0h	Inner VLAN Table Entry Index - Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/ classifier entry Note this index assumes the VLANID is in the packet, it does not use the port VLAN if the packet in untagged or priority tagged.

14.7.3.1.2.335 CPSW3_CPSW_NU_ALE_POLICECFG3 Register

14.7.3.1.2.335.1 CPSW3_CPSW_NU_ALE_POLICECFG3 Register (Offset = 3E10Ch) [reset = 0h]

The Policing Config 3 holds the match enable/match index for the Ether Type and IP Source address

Return to Summary Table

Table 14-11626. Instance Table

Instance Name	Physical Address
CPSW0	0803 E10Ch + formula

Figure 14-5749. CPSW3_CPSW_NU_ALE_POLICECFG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>ETHERTYPE_MEN</td><td colspan="6">RESERVED</td><td>ETHERTYPE_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ETHERTYPE_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>IPSRC_MEN</td><td colspan="6">RESERVED</td><td>IPSRC_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IPSRC_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11627. CPSW3_CPSW_NU_ALE_POLICECFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ETHERTYPE_MEN	R/W	0h	EtherType Match Enable - Enables frame Ether Type match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	ETHERTYPE_INDEX	R/W	0h	EtherType Table Entry Index - Specifies the ALE Ether Type lookup table index to match for the selected policing/classifier entry
15	IPSRC_MEN	R/W	0h	IP Source Address Match Enable - Enables frame IP Source address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	IPSRC_INDEX	R/W	0h	IP Source Address Table Entry Index - Specifies the ALE IP Source address lookup table index to match for the selected policing/classifier entry

14.7.3.1.2.336 CPSW3_CPSW_NU_ALE_POLICECFG4 Register

14.7.3.1.2.336.1 CPSW3_CPSW_NU_ALE_POLICECFG4 Register (Offset = 3E110h) [reset = 0h]

The Policing Config 4 holds the match enable/match index for the IP Destination address

Return to Summary Table

Table 14-11628. Instance Table

Instance Name	Physical Address
CPSW0	0803 E110h + formula

Figure 14-5750. CPSW3_CPSW_NU_ALE_POLICECFG4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>IPDST_MEN</td><td colspan="6">RESERVED</td><td>IPDST_INDEX</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IPDST_INDEX</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11629. CPSW3_CPSW_NU_ALE_POLICECFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPDST_MEN	R/W	0h	IP Destination Address Match Enable - Enables frame IP Destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	IPDST_INDEX	R/W	0h	IP Destination Address Table Entry Index - Specifies the ALE IP Destination address lookup table index to match for the selected policing/classifier entry
15:0	RESERVED	NONE	0h	Reserved

14.7.3.1.2.337 CPSW3_CPSW_NU_ALE_POLICECFG6 Register

14.7.3.1.2.337.1 CPSW3_CPSW_NU_ALE_POLICECFG6 Register (Offset = 3E118h) [reset = 0h]

The PIR counter is a 37 bit internal counter where ~ipir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED at LUT time. If the counter is negative the packet will be marked RED, else it can be YELLOW or GREEN based on the CIR counter. If only this counter is used (aka cir_idle_inc_val==0) Packet are marked RED or GREEN based on PIR counter only.

Return to Summary Table

Table 14-11630. Instance Table

Instance Name	Physical Address
CPSW0	0803 E118h + formula

Figure 14-5751. CPSW3_CPSW_NU_ALE_POLICECFG6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PIR_IDLE_INC_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PIR_IDLE_INC_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PIR_IDLE_INC_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PIR_IDLE_INC_VAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11631. CPSW3_CPSW_NU_ALE_POLICECFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR_IDLE_INC_VAL	R/W	0h	Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED.

14.7.3.1.2.338 CPSW3_CPSW_NU_ALE_POLICECFG7 Register

14.7.3.1.2.338.1 CPSW3_CPSW_NU_ALE_POLICECFG7 Register (Offset = 3E11Ch) [reset = 0h]

The CIR counter is a 37 bit internal counter where ~icir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED or YELLOW at LUT time. If the counter is positive the packet will be marked GREEN, else it can be YELLOW or RED based on the PIR counter. If only this counter is used (aka pir_idle_inc_val==0) Packet are marked YELLOW or GREEN based on CIR counter only.

Return to Summary Table

Table 14-11632. Instance Table

Instance Name	Physical Address
CPSW0	0803 E11Ch + formula

Figure 14-5752. CPSW3_CPSW_NU_ALE_POLICECFG7 Name Register

31	30	29	28	27	26	25	24
CIR_IDLE_INC_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
CIR_IDLE_INC_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
CIR_IDLE_INC_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
CIR_IDLE_INC_VAL							
R/W							
0h							

Table 14-11633. CPSW3_CPSW_NU_ALE_POLICECFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR_IDLE_INC_VAL	R/W	0h	Committed Information Idle Increment Value - The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW.

14.7.3.1.2.339 CPSW3_CPSW_NU_ALE_POLICETBLCTL Register

14.7.3.1.2.339.1 CPSW3_CPSW_NU_ALE_POLICETBLCTL Register (Offset = 3E120h) [reset = 0h]

The Policing Table Control is used to read or write the selected policing/classifier entry. The selected policing/classifier entry is only read or written after this register is written based on the value of the ~iwrite_enable bit.

Return to Summary Table

Table 14-11634. Instance Table

Instance Name	Physical Address
CPSW0	0803 E120h + formula

Figure 14-5753. CPSW3_CPSW_NU_ALE_POLICETBLCTL Name Register

31	30	29	28	27	26	25	24
WRITE_ENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			POL_TBL_IDX				
NONE			R/W				
0h			0h				

Table 14-11635. CPSW3_CPSW_NU_ALE_POLICETBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRITE_ENABLE	R/W	0h	Write Enable - Setting this bit will write the POLICECFG0-7 to the ~ipol_tbl_idx selected policing/classifier entry. Clearing this bit will read the ~ipol_tbl_idx selected policing/classifier entry into the POLICECFG0-7 registers.
30:5	RESERVED	NONE	0h	Reserved
4:0	POL_TBL_IDX	R/W	0h	Policer Entry Index - This field specifies the policing/classifier entry to be read or written. When writing to this field without setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be loaded into the POLICECFG0-7 registers. When writing to this field with setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be updated from the POLICECFG0-7 registers.

14.7.3.1.2.340 CPSW3_CPSW_NU_ALE_POLICECONTROL Register

14.7.3.1.2.340.1 CPSW3_CPSW_NU_ALE_POLICECONTROL Register (Offset = 3E124h) [reset = 0h]

The Control Enables color marking as well as internal ALE packet dropping rules.

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Table 14-11636. Instance Table

Instance Name	Physical Address
CPSW0	0803 E124h + formula

Figure 14-5754. CPSW3_CPSW_NU_ALE_POLICECONTROL Name Register

31	30	29	28	27	26	25	24
POLICING_EN	RESERVED	RED_DROP_EN	YELLOW_DROP_EN	RESERVED	YELLOWTHRESH		
R/W	NONE	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		
23	22	21	20	19	18	17	16
POLMCHMODE		PRIORITY_THREAD_EN	MAC_ONLY_DEF_DIS	RESERVED			
R/W		R/W	R/W	NONE			
0h		0h	0h	0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 14-11637. CPSW3_CPSW_NU_ALE_POLICECONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLICING_EN	R/W	0h	Policing Enable - Enables the policing to color the packets, this also enables red or yellow drop capabilities.
30	RESERVED	NONE	0h	Reserved
29	RED_DROP_EN	R/W	0h	RED Drop Enable - Enables the ALE to drop the red colored packets.
28	YELLOW_DROP_EN	R/W	0h	WELLOW Drop Enable - Enables the ALE to drop yellow packets based on the ~iyellowthresh value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature.
27	RESERVED	NONE	0h	Reserved
26:24	YELLOWTHRESH	R/W	0h	Yellow Threshold - When set enables a portion of the yellow packets to be dropped based on the ~iyellow_drop_en enable. 0-100% 1=50% 2-33% 3-25% 4=20% 5-17% 6-14% 7-13%

Table 14-11637. CPSW3_CPSW_NU_ALE_POLICECONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	POLMCHMODE	R/W	0h	Policing Match Mode - This field determines what happens to packets that fail to hit any policing/classifier entry. 0 - No Hit packets are marked GREEN 1 - No Hit packets are marked YELLOW 2 - No Hit packets are marked RED 3 - No Hit packets are marked based on policing/classifier entry=0 state.
21	PRIORITY_THREAD_EN	R/W	0h	Priority Thread Enable - This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.
20	MAC_ONLY_DEF_DIS	R/W	0h	MAC Only Default Disable - This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}. If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.
19:0	RESERVED	NONE	0h	Reserved

14.7.3.1.2.341 CPSW3_CPSW_NU_ALE_POLICETESTCTL Register

14.7.3.1.2.341.1 CPSW3_CPSW_NU_ALE_POLICETESTCTL Register (Offset = 3E128h) [reset = 0h]

The Policing Test Control enables the ability to determine which policing entry has been hit and whether they reported a red or yellow rate condition.

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Table 14-11638. Instance Table

Instance Name	Physical Address
CPSW0	0803 E128h + formula

Figure 14-5755. CPSW3_CPSW_NU_ALE_POLICETESTCTL Name Register

31	30	29	28	27	26	25	24
POL_CLRALL_HIT	POL_CLRALL_REDHIT	POL_CLRALL_YELLOWHIT	POL_CLRSEL_ALL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			POL_TEST_IDX				
NONE			R/W				
0h			0h				

Table 14-11639. CPSW3_CPSW_NU_ALE_POLICETESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_CLRALL_HIT	R/W	0h	Policer Clear - This bit clears all the policing/classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit.
30	POL_CLRALL_REDHIT	R/W	0h	Policer Clear RED - This bit clears all the policing/classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.
29	POL_CLRALL_YELLOWHIT	R/W	0h	Policer Clear YELLOW - This bit clears all the policing/classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition.
28	POL_CLRSEL_ALL	R/W	0h	Police Clear Selected - This bit clears the selected policing/classifier hit, redhit and yellowhit bits. This bit is self clearing.
27:5	RESERVED	NONE	0h	Reserved
4:0	POL_TEST_IDX	R/W	0h	Policer Test Index - This field selects which policing/classifier hit bits will be read or written.

14.7.3.1.2.342 CPSW3_CPSW_NU_ALE_POLICEHSTAT Register

14.7.3.1.2.342.1 CPSW3_CPSW_NU_ALE_POLICEHSTAT Register (Offset = 3E12Ch) [reset = 0h]

The policing hit status is a read only register that reads the hit bits of the selected policing/classifier.

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Table 14-11640. Instance Table

Instance Name	Physical Address
CPSW0	0803 E12Ch + formula

Figure 14-5756. CPSW3_CPSW_NU_ALE_POLICEHSTAT Name Register

31	30	29	28	27	26	25	24
POL_HIT	POL_REDHIT	POL_YELLOW HIT	RESERVED				
R	R	R	NONE				
0h	0h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 14-11641. CPSW3_CPSW_NU_ALE_POLICEHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_HIT	R	0h	Policer Hit - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit by a packet seen on any port that matches the policing/classifier entry match.
30	POL_REDHIT	R	0h	Policer Hit RED - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a RED condition by a packet seen on any port that matches the policing/classifier entry match.
29	POL_YELLOWHIT	R	0h	Policer Hit YELLOW - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/classifier entry match.
28:0	RESERVED	NONE	0h	Reserved

14.7.3.1.2.343 CPSW3_CPSW_NU_ALE_THREADMAPDEF Register

14.7.3.1.2.343.1 CPSW3_CPSW_NU_ALE_THREADMAPDEF Register (Offset = 3E134h) [reset = 0h]

The THREAD Mapping Default Value register is used to set the default thread ID when no classifier is matched,

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Table 14-11642. Instance Table

Instance Name	Physical Address
CPSW0	0803 E134h + formula

Figure 14-5757. CPSW3_CPSW_NU_ALE_THREADMAPDEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DEFTHREAD_EN	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED		DEFTHREADVAL					
NONE		R/W					
0h		0h					

Table 14-11643. CPSW3_CPSW_NU_ALE_THREADMAPDEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DEFTHREAD_EN	R/W	0h	Default Tread Enable - When set the switch will use the ~idefthreadval for the host interface thread ID if no classifier is matched. If clear the switch will generate its own thread ID based on port and priority if there is no classifier match.
14:6	RESERVED	NONE	0h	Reserved
5:0	DEFTHREADVAL	R/W	0h	Default Thread Value - This field specifies the default thread ID value.

14.7.3.1.2.344 CPSW3_CPSW_NU_ALE_THREADMAPCTL Register

14.7.3.1.2.344.1 CPSW3_CPSW_NU_ALE_THREADMAPCTL Register (Offset = 3E138h) [reset = 0h]

The THREAD Mapping Control register allows the highest matched classifier to return a particular thread ID for traffic sent to the host. This allows particular classifier matched traffic to be placed an a particular hosts queue.

Return to Summary Table

Table 14-11644. Instance Table

Instance Name	Physical Address
CPSW0	0803 E138h + formula

Figure 14-5758. CPSW3_CPSW_NU_ALE_THREADMAPCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			CLASSINDEX				
NONE			R/W				
0h			0h				

Table 14-11645. CPSW3_CPSW_NU_ALE_THREADMAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	CLASSINDEX	R/W	0h	Classifier Index - This is the classifier index entry that the thread enable and thread value will be read or written by the ~bTHREADMAPVAL register.

14.7.3.1.2.345 CPSW3_CPSW_NU_ALE_THREADMAPVAL Register

14.7.3.1.2.345.1 CPSW3_CPSW_NU_ALE_THREADMAPVAL Register (Offset = 3E13Ch) [reset = 0h]

The THREAD Mapping Value register is used to set the thread ID for a particular classifier entry.

Return to Summary Table

Table 14-11646. Instance Table

Instance Name	Physical Address
CPSW0	0803 E13Ch + formula

Figure 14-5759. CPSW3_CPSW_NU_ALE_THREADMAPVAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_EN	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED		THREADVAL					
NONE		R/W					
0h		0h					

Table 14-11647. CPSW3_CPSW_NU_ALE_THREADMAPVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	THREAD_EN	R/W	0h	Thread Enable - When set the switch will use the ~ithreadval for the selected classifier match. If clear the the thread ID will be determined by the ~bTHREADMAPDEF register settings.
14:6	RESERVED	NONE	0h	Reserved
5:0	THREADVAL	R/W	0h	Thread Value - This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.

14.7.3.1.2.346 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_J Register

14.7.3.1.2.346.1 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_J Register (Offset = 3D0E0h) [reset = 0h]

Time Stamp Generate Function Comparison Low Value

Return to Summary Table

Table 14-11648. Instance Table

Instance Name	Physical Address
CPSW0	0803 D0E0h + formula

Figure 14-5760. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 14-11649. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_GENF_COMP_HIGH_REG_I and CPSW_GENF_COMP_LOW_REG_I should only be written when the CPSW_GENF_LENGTH_REG_I[31-0] LENGTH value is zero.

14.7.3.1.2.347 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_J Register

14.7.3.1.2.347.1 CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_J Register (Offset = 3D0E4h) [reset = 0h]

Time Stamp Generate Function Comparison high Value

Return to Summary Table

Table 14-11650. Instance Table

Instance Name	Physical Address
CPSW0	0803 D0E4h + formula

Figure 14-5761. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 14-11651. CPSW3_CPSW_NU_CPTS_TS_GENF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits. The CPSW_GENF_COMP_HIGH_REG_I and CPSW_GENF_COMP_LOW_REG_I should only be written when the CPSW_GENF_LENGTH_REG_I[31-0] LENGTH value is zero.

14.7.3.1.2.348 CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_J Register

14.7.3.1.2.348.1 CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_J Register (Offset = 3D0E8h) [reset = 0h]

Time Stamp Generate Function Control

Return to Summary Table

Table 14-11652. Instance Table

Instance Name	Physical Address
CPSW0	0803 D0E8h + formula

Figure 14-5762. CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PPM_DIR	POLARITY_INV
NONE						R/W	R/W
0h						0h	0h

Table 14-11653. CPSW3_CPSW_NU_CPTS_TS_GENF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction. 0h A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.
0	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert 0h The output TS_GENFn signal asserts low 1h The output TS_GENFn signal asserts high

14.7.3.1.2.349 CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_J Register

14.7.3.1.2.349.1 CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_J Register (Offset = 3D0ECh) [reset = 0h]

Time Stamp Generate Function Length Value

Return to Summary Table

Table 14-11654. Instance Table

Instance Name	Physical Address
CPSW0	0803 D0ECh + formula

Figure 14-5763. CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 14-11655. CPSW3_CPSW_NU_CPTS_TS_GENF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value

14.7.3.1.2.350 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_J Register

14.7.3.1.2.350.1 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_J Register (Offset = 3D0F0h) [reset = 0h]

Time Stamp Generate Function PPM Low Value

Return to Summary Table

Table 14-11656. Instance Table

Instance Name	Physical Address
CPSW0	0803 D0F0h + formula

Figure 14-5764. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 14-11657. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

14.7.3.1.2.351 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_J Register

14.7.3.1.2.351.1 CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_J Register (Offset = 3D0F4h) [reset = 0h]

Time Stamp Generate Function PPM High Value

Return to Summary Table

Table 14-11658. Instance Table

Instance Name	Physical Address
CPSW0	0803 D0F4h + formula

Figure 14-5765. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PPM_HIGH	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PPM_HIGH							
R/W							
0h							

Table 14-11659. CPSW3_CPSW_NU_CPTS_TS_GENF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value. This value should be written first (before the low value is written).

14.7.3.1.2.352 CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_J Register

14.7.3.1.2.352.1 CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_J Register (Offset = 3D0F8h) [reset = 0h]

Time Stamp Generate Function Nudge Value

Return to Summary Table

Table 14-11660. Instance Table

Instance Name	Physical Address
CPSW0	0803 D0F8h + formula

Figure 14-5766. CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 14-11661. CPSW3_CPSW_NU_CPTS_TS_GENF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_GENF_NUDGE_REG_l[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_GENF_NUDGE_REG_l value is cleared to zero when the nudge has occurred.

14.7.3.1.2.353 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_J Register

14.7.3.1.2.353.1 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_J Register (Offset = 3D200h) [reset = 0h]

Time Stamp ESTF Generate Function Comparison Low Value

Return to Summary Table

Table 14-11662. Instance Table

Instance Name	Physical Address
CPSW0	0803 D200h + formula

Figure 14-5767. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 14-11663. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	ESTFn comparison value lower 32-bits. This value should be written after the upper 32-bits. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

14.7.3.1.2.354 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_J Register

14.7.3.1.2.354.1 CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_J Register (Offset = 3D204h) [reset = 0h]

Time Stamp ESTF Generate Function Comparison high Value

Return to Summary Table

Table 14-11664. Instance Table

Instance Name	Physical Address
CPSW0	0803 D204h + formula

Figure 14-5768. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 14-11665. CPSW3_CPSW_NU_CPTS_TS_ESTF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	ESTFn comparison value upper 32-bits. This value should be written before the lower 32-bits are written. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

14.7.3.1.2.355 CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_J Register

14.7.3.1.2.355.1 CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_J Register (Offset = 3D208h) [reset = 0h]

Time Stamp ESTF Generate Function Control

Return to Summary Table

Table 14-11666. Instance Table

Instance Name	Physical Address
CPSW0	0803 D208h + formula

Figure 14-5769. CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
NONE						R/W	R/W
0h						0h	0h

Table 14-11667. CPSW3_CPSW_NU_CPTS_TS_ESTF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 2) Polarity Invert. 0h The output TS_ESTFn signal asserts low 1h The output TS_ESTFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 2) PPM Direction. 0h A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

14.7.3.1.2.356 CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_J Register

14.7.3.1.2.356.1 CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_J Register (Offset = 3D20Ch) [reset = 0h]

Time Stamp ESTF Generate Function Length Value

Return to Summary Table

Table 14-11668. Instance Table

Instance Name	Physical Address
CPSW0	0803 D20Ch + formula

Figure 14-5770. CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 14-11669. CPSW3_CPSW_NU_CPTS_TS_ESTF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function Length Value.

14.7.3.1.2.357 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_J Register

14.7.3.1.2.357.1 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_J Register (Offset = 3D210h) [reset = 0h]

Time Stamp ESTF Generate Function PPM Low Value

Return to Summary Table

Table 14-11670. Instance Table

Instance Name	Physical Address
CPSW0	0803 D210h + formula

Figure 14-5771. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PPM_LOW							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PPM_LOW							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPM_LOW							
R/W							
0h							

Table 14-11671. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

14.7.3.1.2.358 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_J Register

14.7.3.1.2.358.1 CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_J Register (Offset = 3D214h) [reset = 0h]

Time Stamp ESTF Generate Function PPM High Value

Return to Summary Table

Table 14-11672. Instance Table

Instance Name	Physical Address
CPSW0	0803 D214h + formula

Figure 14-5772. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PPM_HIGH	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PPM_HIGH							
R/W							
0h							

Table 14-11673. CPSW3_CPSW_NU_CPTS_TS_ESTF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function PPM High Value. This value should be written first (before the low value is written).

14.7.3.1.2.359 CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_J Register

14.7.3.1.2.359.1 CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_J Register (Offset = 3D218h) [reset = 0h]

Time Stamp ESTF Generate Function Nudge Value

Return to Summary Table

Table 14-11674. Instance Table

Instance Name	Physical Address
CPSW0	0803 D218h + formula

Figure 14-5773. CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUDGE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11675. CPSW3_CPSW_NU_CPTS_TS_ESTF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Time Stamp ESTFn (n = 1 to 2) Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_ESTF_NUDGE_REG_l[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_ESTF_NUDGE_REG_l value is cleared to zero when the nudge has occurred.

14.7.3.2 USB

USB

14.7.3.2.1 USB Summaries

USB Summaries

Table 14-11676. USB2SS_USB2SS_DEBUG_TRACE Registers, Base Address=0070 3000h, Length=512

Offset	Length	Register Name	USB0 Physical Address
80h	32	USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL	0070 3080h
0h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_J	0070 3000h + formula
4h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_J	0070 3004h + formula
8h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_J	0070 3008h + formula
Ch	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_J	0070 300Ch + formula
10h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_J	0070 3010h + formula
14h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_J	0070 3014h + formula
18h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_J	0070 3018h + formula
1Ch	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_J	0070 301Ch + formula
20h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_J	0070 3020h + formula
24h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_J	0070 3024h + formula
28h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_J	0070 3028h + formula
2Ch	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_J	0070 302Ch + formula
30h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_J	0070 3030h + formula
34h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_J	0070 3034h + formula
38h	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_J	0070 3038h + formula
3Ch	32	USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_J	0070 303Ch + formula

Table 14-11677. USB2SS_USB2SS_CFG Registers, Base Address=0F90 0000h, Length=2048

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_USB2SS_CFG_REVISION	0F90 0000h
4h	32	USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL	0F90 0004h
8h	32	USB2SS_USB2SS_CFG_PHY_CONFIG	0F90 0008h
Ch	32	USB2SS_USB2SS_CFG_PHY_TEST	0F90 000Ch
14h	32	USB2SS_USB2SS_CFG_CORE_STAT	0F90 0014h
18h	32	USB2SS_USB2SS_CFG_HOST_VBUS_CTRL	0F90 0018h
1Ch	32	USB2SS_USB2SS_CFG_MODE_CONTROL	0F90 001Ch
30h	32	USB2SS_USB2SS_CFG_WAKEUP_CONFIG	0F90 0030h
34h	32	USB2SS_USB2SS_CFG_WAKEUP_STAT	0F90 0034h
38h	32	USB2SS_USB2SS_CFG_OVERRIDE_CONFIG	0F90 0038h
430h	32	USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW	0F90 0430h
434h	32	USB2SS_USB2SS_CFG_IRQ_MISC_STATUS	0F90 0434h
438h	32	USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET	0F90 0438h
43Ch	32	USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR	0F90 043Ch
440h	32	USB2SS_USB2SS_CFG_IRQ_MISC_EOI	0F90 0440h
490h	32	USB2SS_USB2SS_CFG_INTR_TEST	0F90 0490h
614h	32	USB2SS_USB2SS_CFG_VBUS_FILTER	0F90 0614h
618h	32	USB2SS_USB2SS_CFG_VBUS_STAT	0F90 0618h
708h	32	USB2SS_USB2SS_CFG_DEBUG_CFG	0F90 0708h

Table 14-11677. USB2SS_USB2SS_CFG Registers, Base Address=0F90 0000h, Length=2048 (continued)

Offset	Length	Register Name	USB0 Physical Address
70Ch	32	USB2SS_USB2SS_CFG_DEBUG_DATA	0F90 070Ch
714h	32	USB2SS_USB2SS_CFG_HOST_HUB_CTRL	0F90 0714h

Table 14-11678. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_PHY2_AFE_TX_REG0	0F90 8000h
4h	32	USB2SS_PHY2_AFE_TX_REG1	0F90 8004h
8h	32	USB2SS_PHY2_AFE_TX_REG2	0F90 8008h
Ch	32	USB2SS_PHY2_AFE_TX_REG3	0F90 800Ch
10h	32	USB2SS_PHY2_AFE_TX_REG4	0F90 8010h
14h	32	USB2SS_PHY2_AFE_TX_REG5	0F90 8014h
18h	32	USB2SS_PHY2_AFE_TX_REG6	0F90 8018h
1Ch	32	USB2SS_PHY2_AFE_TX_REG7	0F90 801Ch
20h	32	USB2SS_PHY2_AFE_TX_REG8	0F90 8020h
24h	32	USB2SS_PHY2_AFE_TX_REG9	0F90 8024h
28h	32	USB2SS_PHY2_AFE_TX_REG10	0F90 8028h
2Ch	32	USB2SS_PHY2_AFE_TX_REG11	0F90 802Ch
30h	32	USB2SS_PHY2_AFE_TX_REG12	0F90 8030h
34h	32	USB2SS_PHY2_AFE_RX_REG0	0F90 8034h
38h	32	USB2SS_PHY2_AFE_RX_REG1	0F90 8038h
3Ch	32	USB2SS_PHY2_AFE_RX_REG2	0F90 803Ch
40h	32	USB2SS_PHY2_AFE_RX_REG3	0F90 8040h
44h	32	USB2SS_PHY2_AFE_RX_REG4	0F90 8044h
48h	32	USB2SS_PHY2_AFE_RX_REG5	0F90 8048h
4Ch	32	USB2SS_PHY2_AFE_RX_REG6	0F90 804Ch
50h	32	USB2SS_PHY2_AFE_TX_REG13	0F90 8050h
54h	32	USB2SS_PHY2_AFE_TX_REG14	0F90 8054h
58h	32	USB2SS_PHY2_AFE_RX_REG7	0F90 8058h
5Ch	32	USB2SS_PHY2_AFE_RX_REG8	0F90 805Ch
60h	32	USB2SS_PHY2_AFE_UNUSED_REG0	0F90 8060h
64h	32	USB2SS_PHY2_AFE_UNUSED_REG1	0F90 8064h
80h	32	USB2SS_PHY2_AFE_BG_REG0	0F90 8080h
84h	32	USB2SS_PHY2_AFE_BG_REG1	0F90 8084h
88h	32	USB2SS_PHY2_AFE_BG_REG2	0F90 8088h
8Ch	32	USB2SS_PHY2_AFE_BG_REG3	0F90 808Ch
90h	32	USB2SS_PHY2_AFE_CALIB_REG0	0F90 8090h
94h	32	USB2SS_PHY2_AFE_BC_REG0	0F90 8094h
98h	32	USB2SS_PHY2_AFE_BC_REG1	0F90 8098h
9Ch	32	USB2SS_PHY2_AFE_BC_REG2	0F90 809Ch
A0h	32	USB2SS_PHY2_AFE_BC_REG3	0F90 80A0h
A4h	32	USB2SS_PHY2_AFE_BC_REG4	0F90 80A4h
A8h	32	USB2SS_PHY2_AFE_BC_REG5	0F90 80A8h
ACh	32	USB2SS_PHY2_AFE_BC_REG6	0F90 80ACh
B0h	32	USB2SS_PHY2_AFE_PLL_REG0	0F90 80B0h
B4h	32	USB2SS_PHY2_AFE_PLL_REG1	0F90 80B4h
B8h	32	USB2SS_PHY2_AFE_PLL_REG2	0F90 80B8h

Table 14-11678. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
BCh	32	USB2SS_PHY2_AFE_PLL_REG3	0F90 80BCh
C0h	32	USB2SS_PHY2_AFE_PLL_REG4	0F90 80C0h
C4h	32	USB2SS_PHY2_AFE_PLL_REG5	0F90 80C4h
C8h	32	USB2SS_PHY2_AFE_BG_REG4	0F90 80C8h
CCh	32	USB2SS_PHY2_AFE_CALIB_REG1	0F90 80CCh
D0h	32	USB2SS_PHY2_AFE_BC_REG7	0F90 80D0h
D4h	32	USB2SS_PHY2_AFE_PLL_REG6	0F90 80D4h
D8h	32	USB2SS_PHY2_AFE_UNUSED_REG2	0F90 80D8h
DCh	32	USB2SS_PHY2_AFE_UNUSED_REG3	0F90 80DCh
100h	32	USB2SS_PHY2_PLL_REG0	0F90 8100h
104h	32	USB2SS_PHY2_PLL_REG1	0F90 8104h
108h	32	USB2SS_PHY2_PLL_REG2	0F90 8108h
10Ch	32	USB2SS_PHY2_PLL_REG3	0F90 810Ch
110h	32	USB2SS_PHY2_PLL_REG4	0F90 8110h
114h	32	USB2SS_PHY2_PLL_REG5	0F90 8114h
118h	32	USB2SS_PHY2_PLL_REG6	0F90 8118h
11Ch	32	USB2SS_PHY2_PLL_REG7	0F90 811Ch
120h	32	USB2SS_PHY2_PLL_REG8	0F90 8120h
124h	32	USB2SS_PHY2_PLL_REG9	0F90 8124h
128h	32	USB2SS_PHY2_PLL_REG10	0F90 8128h
12Ch	32	USB2SS_PHY2_PLL_REG11	0F90 812Ch
130h	32	USB2SS_PHY2_PLL_REG12	0F90 8130h
134h	32	USB2SS_PHY2_PLL_REG13	0F90 8134h
138h	32	USB2SS_PHY2_PLL_REG14	0F90 8138h
13Ch	32	USB2SS_PHY2_PLL_UNUSED_REG0	0F90 813Ch
140h	32	USB2SS_PHY2_PLL_UNUSED_REG1	0F90 8140h
144h	32	USB2SS_PHY2_PLL_REG15	0F90 8144h
148h	32	USB2SS_PHY2_PLL_REG16	0F90 8148h
14Ch	32	USB2SS_PHY2_PLL_UNUSED_REG2	0F90 814Ch
180h	32	USB2SS_PHY2_CALIB_REG0	0F90 8180h
184h	32	USB2SS_PHY2_CALIB_REG1	0F90 8184h
188h	32	USB2SS_PHY2_BC_REG0	0F90 8188h
18Ch	32	USB2SS_PHY2_BC_REG1	0F90 818Ch
190h	32	USB2SS_PHY2_BC_REG2	0F90 8190h
194h	32	USB2SS_PHY2_BC_REG3	0F90 8194h
198h	32	USB2SS_PHY2_BC_REG4	0F90 8198h
19Ch	32	USB2SS_PHY2_BC_REG5	0F90 819Ch
1A0h	32	USB2SS_PHY2_BC_REG6	0F90 81A0h
1A4h	32	USB2SS_PHY2_BC_REG7	0F90 81A4h
1A8h	32	USB2SS_PHY2_TED_REG0	0F90 81A8h
1ACh	32	USB2SS_PHY2_TED_REG1	0F90 81ACh
1B0h	32	USB2SS_PHY2_TED_REG2	0F90 81B0h
1B4h	32	USB2SS_PHY2_CALIB_REG2	0F90 81B4h
1B8h	32	USB2SS_PHY2_CALIB_REG3	0F90 81B8h
1BCh	32	USB2SS_PHY2_BC_REG8	0F90 81BCh
1C0h	32	USB2SS_PHY2_BC_REG9	0F90 81C0h
1C4h	32	USB2SS_PHY2_BC_REG10	0F90 81C4h

Table 14-11678. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
1C8h	32	USB2SS_PHY2_BC_REG11	0F90 81C8h
1CCh	32	USB2SS_PHY2_BC_REG12	0F90 81CCh
1D0h	32	USB2SS_PHY2_TED_REG3	0F90 81D0h
1D4h	32	USB2SS_PHY2_TED_REG4	0F90 81D4h
1D8h	32	USB2SS_PHY2_DIG_UNUSED_REG0	0F90 81D8h
1DCh	32	USB2SS_PHY2_DIG_UNUSED_REG1	0F90 81DCh
1E0h	32	USB2SS_PHY2_DIG_UNUSED_REG2	0F90 81E0h
1E4h	32	USB2SS_PHY2_DIG_UNUSED_REG3	0F90 81E4h
1E8h	32	USB2SS_PHY2_INTERRUPT_REG1	0F90 81E8h
1ECh	32	USB2SS_PHY2_INTERRUPT_REG2	0F90 81ECh
200h	32	USB2SS_PHY2_RX_REG0	0F90 8200h
204h	32	USB2SS_PHY2_RX_REG1	0F90 8204h
208h	32	USB2SS_PHY2_TX_REG0	0F90 8208h
20Ch	32	USB2SS_PHY2_TX_REG1	0F90 820Ch
210h	32	USB2SS_PHY2_CDR_REG0	0F90 8210h
214h	32	USB2SS_PHY2_CDR_REG1	0F90 8214h
218h	32	USB2SS_PHY2_CDR_REG2	0F90 8218h
21Ch	32	USB2SS_PHY2_CDR_REG3	0F90 821Ch
220h	32	USB2SS_PHY2_CDR_REG4	0F90 8220h
224h	32	USB2SS_PHY2_CDR_REG5	0F90 8224h
228h	32	USB2SS_PHY2_CDR_REG6	0F90 8228h
22Ch	32	USB2SS_PHY2_CDR_REG7	0F90 822Ch
230h	32	USB2SS_PHY2_CDR_REG8	0F90 8230h
234h	32	USB2SS_PHY2_RX_REG2	0F90 8234h
238h	32	USB2SS_PHY2_RX_REG3	0F90 8238h
23Ch	32	USB2SS_PHY2_RX_REG4	0F90 823Ch
240h	32	USB2SS_PHY2_RX_REG5	0F90 8240h
244h	32	USB2SS_PHY2_RX_REG6	0F90 8244h
248h	32	USB2SS_PHY2_RX_REG7	0F90 8248h
24Ch	32	USB2SS_PHY2_TX_REG2	0F90 824Ch
250h	32	USB2SS_PHY2_TX_REG3	0F90 8250h
254h	32	USB2SS_PHY2_TX_REG4	0F90 8254h
258h	32	USB2SS_PHY2_CDR_REG9	0F90 8258h
25Ch	32	USB2SS_PHY2_CDR_REG10	0F90 825Ch
260h	32	USB2SS_PHY2_CDR_REG11	0F90 8260h
264h	32	USB2SS_PHY2_CDR_RE12	0F90 8264h
268h	32	USB2SS_PHY2_DIG_TXRX_UNUSED_REG0	0F90 8268h
26Ch	32	USB2SS_PHY2_DIG_TXRX_UNUSED_REG1	0F90 826Ch
270h	32	USB2SS_PHY2_DIG_TXRX_UNUSED_REG2	0F90 8270h
274h	32	USB2SS_PHY2_DIG_TXRX_UNUSED_REG3	0F90 8274h
280h	32	USB2SS_PHY2_UTMI_REG0	0F90 8280h
284h	32	USB2SS_PHY2_UTMI_REG1	0F90 8284h
288h	32	USB2SS_PHY2_UTMI_REG2	0F90 8288h
28Ch	32	USB2SS_PHY2_UTMI_REG3	0F90 828Ch
290h	32	USB2SS_PHY2_UTMI_REG4	0F90 8290h
294h	32	USB2SS_PHY2_UTMI_REG5	0F90 8294h
298h	32	USB2SS_PHY2_UTMI_REG6	0F90 8298h

Table 14-11678. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
29Ch	32	USB2SS_PHY2_UTMI_REG7	0F90 829Ch
2A0h	32	USB2SS_PHY2_UTMI_REG8	0F90 82A0h
2A4h	32	USB2SS_PHY2_UTMI_REG9	0F90 82A4h
2A8h	32	USB2SS_PHY2_UTMI_REG10	0F90 82A8h
2ACh	32	USB2SS_PHY2_UTMI_REG11	0F90 82ACh
2B0h	32	USB2SS_PHY2_UTMI_REG12	0F90 82B0h
2B4h	32	USB2SS_PHY2_UTMI_REG13	0F90 82B4h
2B8h	32	USB2SS_PHY2_UTMI_REG14	0F90 82B8h
2BCh	32	USB2SS_PHY2_UTMI_REG15	0F90 82BCh
2C0h	32	USB2SS_PHY2_UTMI_REG16	0F90 82C0h
2C4h	32	USB2SS_PHY2_UTMI_REG17	0F90 82C4h
2C8h	32	USB2SS_PHY2_UTMI_REG18	0F90 82C8h
2CCh	32	USB2SS_PHY2_UTMI_REG19	0F90 82CCh
2D0h	32	USB2SS_PHY2_UTMI_REG20	0F90 82D0h
2D4h	32	USB2SS_PHY2_UTMI_REG21	0F90 82D4h
2D8h	32	USB2SS_PHY2_UTMI_REG22	0F90 82D8h
2DCh	32	USB2SS_PHY2_UTMI_REG23	0F90 82DCh
2E0h	32	USB2SS_PHY2_UTMI_REG24	0F90 82E0h
2E4h	32	USB2SS_PHY2_UTMI_REG25	0F90 82E4h
2E8h	32	USB2SS_PHY2_UTMI_REG26	0F90 82E8h
2ECh	32	USB2SS_PHY2_UTMI_REG27	0F90 82ECh
2F0h	32	USB2SS_PHY2_UTMI_REG28	0F90 82F0h
2F4h	32	USB2SS_PHY2_UTMI_REG29	0F90 82F4h
2F8h	32	USB2SS_PHY2_UTMI_REG30	0F90 82F8h
2FCh	32	USB2SS_PHY2_UTMI_UNUSED_REG0	0F90 82FCh
300h	32	USB2SS_PHY2_UTMI_UNUSED_REG1	0F90 8300h
304h	32	USB2SS_PHY2_UTMI_UNUSED_REG2	0F90 8304h
308h	32	USB2SS_PHY2_UTMI_UNUSED_REG3	0F90 8308h
30Ch	32	USB2SS_PHY2_UTMI_REG31	0F90 830Ch
310h	32	USB2SS_PHY2_UTMI_REG32	0F90 8310h
314h	32	USB2SS_PHY2_UTMI_REG33	0F90 8314h
318h	32	USB2SS_PHY2_UTMI_REG34	0F90 8318h
31Ch	32	USB2SS_PHY2_UTMI_REG35	0F90 831Ch
320h	32	USB2SS_PHY2_UTMI_REG36	0F90 8320h
324h	32	USB2SS_PHY2_UTMI_REG37	0F90 8324h
328h	32	USB2SS_PHY2_UTMI_REG38	0F90 8328h
32Ch	32	USB2SS_PHY2_UTMI_REG39	0F90 832Ch
330h	32	USB2SS_PHY2_UTMI_REG40	0F90 8330h
334h	32	USB2SS_PHY2_UTMI_REG41	0F90 8334h
338h	32	USB2SS_PHY2_UTMI_REG42	0F90 8338h
33Ch	32	USB2SS_PHY2_UTMI_REG43	0F90 833Ch
340h	32	USB2SS_PHY2_UTMI_REG44	0F90 8340h
344h	32	USB2SS_PHY2_UTMI_REG45	0F90 8344h
348h	32	USB2SS_PHY2_UTMI_REG46	0F90 8348h
34Ch	32	USB2SS_PHY2_UTMI_REG47	0F90 834Ch
350h	32	USB2SS_PHY2_UTMI_REG48	0F90 8350h
354h	32	USB2SS_PHY2_UTMI_REG49	0F90 8354h

Table 14-11678. USB2SS_PHY2 Registers, Base Address=0F90 8000h, Length=1024 (continued)

Offset	Length	Register Name	USB0 Physical Address
358h	32	USB2SS_PHY2_UTMI_REG50	0F90 8358h
35Ch	32	USB2SS_PHY2_UTMI_REG51	0F90 835Ch
360h	32	USB2SS_PHY2_UTMI_REG52	0F90 8360h
364h	32	USB2SS_PHY2_UTMI_REG53	0F90 8364h
368h	32	USB2SS_PHY2_UTMI_REG54	0F90 8368h
36Ch	32	USB2SS_PHY2_UTMI_REG55	0F90 836Ch
370h	32	USB2SS_PHY2_UTMI_REG56	0F90 8370h
374h	32	USB2SS_PHY2_UTMI_REG57	0F90 8374h
378h	32	USB2SS_PHY2_UTMI_REG58	0F90 8378h
37Ch	32	USB2SS_PHY2_UTMI_REG59	0F90 837Ch
380h	32	USB2SS_PHY2_UTMI_UNUSED_REG6	0F90 8380h
384h	32	USB2SS_PHY2_UTMI_UNUSED_REG7	0F90 8384h

Table 14-11679. ECC_AGGR Registers, Base Address=0F98 0000h, Length=1024

Offset	Length	Register Name	USB0 Physical Address
0h	32	ECC_AGGR_REV	0F98 0000h
8h	32	ECC_AGGR_VECTOR	0F98 0008h
Ch	32	ECC_AGGR_STAT	0F98 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0F98 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0F98 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0F98 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0F98 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0F98 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0F98 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0F98 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0F98 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0F98 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0F98 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0F98 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0F98 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0F98 020Ch

Table 14-11680. USB2SS_CAP Registers, Base Address=3100 0000h, Length=32

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_CAP_CAPLENGTH	3100 0000h
4h	32	USB2SS_CAP_HCSPARAMS1	3100 0004h
8h	32	USB2SS_CAP_HCSPARAMS2	3100 0008h
Ch	32	USB2SS_CAP_HCSPARAMS3	3100 000Ch
10h	32	USB2SS_CAP_HCCPARAMS1	3100 0010h
14h	32	USB2SS_CAP_DBOFF	3100 0014h
18h	32	USB2SS_CAP_RTSOFF	3100 0018h
1Ch	32	USB2SS_CAP_HCCPARAMS2	3100 001Ch

Table 14-11681. USB2SS_OPER Registers, Base Address=3100 0020h, Length=64

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_OPER_USBCMD	3100 0020h
4h	32	USB2SS_OPER_USBSTS	3100 0024h
8h	32	USB2SS_OPER_PAGESIZE	3100 0028h
14h	32	USB2SS_OPER_DNCTRL	3100 0034h
18h	32	USB2SS_OPER_CRCR_LO	3100 0038h
1Ch	32	USB2SS_OPER_CRCR_HI	3100 003Ch
30h	32	USB2SS_OPER_DCBAAP_LO	3100 0050h
34h	32	USB2SS_OPER_DCBAAP_HI	3100 0054h
38h	32	USB2SS_OPER_CONFIG	3100 0058h

Table 14-11682. USB2SS_PORT Registers, Base Address=3100 0420h, Length=32

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_PORT_XHCI_PORT_20_PORTSC_20	3100 0420h + formula
4h	32	USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20	3100 0424h + formula
8h	32	USB2SS_PORT_XHCI_PORT_20_PORTLI_20	3100 0428h + formula
Ch	32	USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20	3100 042Ch + formula
14h	32	USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30	3100 0434h + formula
18h	32	USB2SS_PORT_XHCI_PORT_30_PORTLI_30	3100 0438h + formula
1Ch	32	USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30	3100 043Ch + formula

Table 14-11683. USB2SS_RUNTIME Registers, Base Address=3100 0440h, Length=32

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_RUNTIME_MFINDEX	3100 0440h
4h	32	USB2SS_RUNTIME_RSVDZ	3100 0444h

Table 14-11684. USB2SS_INTR Registers, Base Address=3100 0460h, Length=64

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_INTR_XHCI_INTR_IMAN_J	3100 0460h + formula
4h	32	USB2SS_INTR_XHCI_INTR_IMOD_J	3100 0464h + formula
8h	32	USB2SS_INTR_XHCI_INTR_ERSTSZ_J	3100 0468h + formula
Ch	32	USB2SS_INTR_XHCI_INTR_RSVDP_J	3100 046Ch + formula
10h	32	USB2SS_INTR_XHCI_INTR_ERSTBA_LO_J	3100 0470h + formula
14h	32	USB2SS_INTR_XHCI_INTR_ERSTBA_HI_J	3100 0474h + formula
18h	32	USB2SS_INTR_XHCI_INTR_ERDP_LO_J	3100 0478h + formula
1Ch	32	USB2SS_INTR_XHCI_INTR_ERDP_HI_J	3100 047Ch + formula

Table 14-11685. USB2SS_DBARR Registers, Base Address=3100 0560h, Length=512

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_DBARR_XHCI_DB_DB_J	3100 0560h + formula

Table 14-11686. USB2SS_EXTCAP Registers, Base Address=3100 0960h, Length=16

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_EXTCAP_USBLEGSUP	3100 0960h
4h	32	USB2SS_EXTCAP_USBLEGCTLSTS	3100 0964h

Table 14-11687. USB2SS_SUPPRTCAP2 Registers, Base Address=3100 0970h, Length=16

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_SUPPRTCAP2_SUPTPRT2_DW0	3100 0970h
4h	32	USB2SS_SUPPRTCAP2_SUPTPRT2_DW1	3100 0974h
8h	32	USB2SS_SUPPRTCAP2_SUPTPRT2_DW2	3100 0978h
Ch	32	USB2SS_SUPPRTCAP2_SUPTPRT2_DW3	3100 097Ch

Table 14-11688. USB2SS_SUPPRTCAP3 Registers, Base Address=3100 0980h, Length=32

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_SUPPRTCAP3_SUPTPRT3_DW0	3100 0980h
4h	32	USB2SS_SUPPRTCAP3_SUPTPRT3_DW1	3100 0984h
8h	32	USB2SS_SUPPRTCAP3_SUPTPRT3_DW2	3100 0988h
Ch	32	USB2SS_SUPPRTCAP3_SUPTPRT3_DW3	3100 098Ch

Table 14-11689. USB2SS_GBL Registers, Base Address=3100 C100h, Length=2048

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_GBL_GSBUSCFG0	3100 C100h
4h	32	USB2SS_GBL_GSBUSCFG1	3100 C104h
8h	32	USB2SS_GBL_GTXTHRCFG	3100 C108h
Ch	32	USB2SS_GBL_GRXTHRCFG	3100 C10Ch
10h	32	USB2SS_GBL_GCTL	3100 C110h
14h	32	USB2SS_GBL_GPMSTS	3100 C114h
18h	32	USB2SS_GBL_GSTS	3100 C118h
1Ch	32	USB2SS_GBL_GUCTL1	3100 C11Ch
20h	32	USB2SS_GBL_GSNPSID	3100 C120h
24h	32	USB2SS_GBL_GGPIO	3100 C124h
28h	32	USB2SS_GBL_GUID	3100 C128h
2Ch	32	USB2SS_GBL_GUCTL	3100 C12Ch
30h	32	USB2SS_GBL_GBUSERRADDRLO	3100 C130h
34h	32	USB2SS_GBL_GBUSERRADDRHI	3100 C134h
38h	32	USB2SS_GBL_GPRTBIMAPLO	3100 C138h
3Ch	32	USB2SS_GBL_GPRTBIMAPHI	3100 C13Ch
40h	32	USB2SS_GBL_GHWPARAMS0	3100 C140h
44h	32	USB2SS_GBL_GHWPARAMS1	3100 C144h
48h	32	USB2SS_GBL_GHWPARAMS2	3100 C148h
4Ch	32	USB2SS_GBL_GHWPARAMS3	3100 C14Ch
50h	32	USB2SS_GBL_GHWPARAMS4	3100 C150h
54h	32	USB2SS_GBL_GHWPARAMS5	3100 C154h
58h	32	USB2SS_GBL_GHWPARAMS6	3100 C158h
5Ch	32	USB2SS_GBL_GHWPARAMS7	3100 C15Ch
60h	32	USB2SS_GBL_GDBGFIFOSPACE	3100 C160h
64h	32	USB2SS_GBL_GDBGLTSSM	3100 C164h
68h	32	USB2SS_GBL_GDBGLNMCC	3100 C168h
6Ch	32	USB2SS_GBL_GDBGBMU	3100 C16Ch
70h	32	USB2SS_GBL_GDBGLSPMUX_HST	3100 C170h
74h	32	USB2SS_GBL_GDBGLSP	3100 C174h
78h	32	USB2SS_GBL_GDBGEPINFO0	3100 C178h

Table 14-11689. USB2SS_GBL Registers, Base Address=3100 C100h, Length=2048 (continued)

Offset	Length	Register Name	USB0 Physical Address
7Ch	32	USB2SS_GBL_GDBGEPINFO1	3100 C17Ch
80h	32	USB2SS_GBL_GPRTBIMAP_HSLO	3100 C180h
84h	32	USB2SS_GBL_GPRTBIMAP_HSHI	3100 C184h
88h	32	USB2SS_GBL_GPRTBIMAP_FSLO	3100 C188h
8Ch	32	USB2SS_GBL_GPRTBIMAP_FSHI	3100 C18Ch
94h	32	USB2SS_GBL_RESERVED_94	3100 C194h
98h	32	USB2SS_GBL_RESERVED_98	3100 C198h
9Ch	32	USB2SS_GBL_GUCTL2	3100 C19Ch
500h	32	USB2SS_GBL_GHWPARAMS8	3100 C600h
50Ch	32	USB2SS_GBL_GUCTL3	3100 C60Ch
510h	32	USB2SS_GBL_GTXFIFOPRIDEV	3100 C610h
518h	32	USB2SS_GBL_GTXFIFOPRIHST	3100 C618h
51Ch	32	USB2SS_GBL_GRXFIFOPRIHST	3100 C61Ch
524h	32	USB2SS_GBL_GDMAHLRATIO	3100 C624h
530h	32	USB2SS_GBL_GFLADJ	3100 C630h
100h	32	USB2SS_GBL_GPHY_GUSB2PHYCFG	3100 C200h + formula
140h	32	USB2SS_GBL_GI2C_GUSB2I2CCTL	3100 C240h + formula
180h	32	USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI	3100 C280h + formula
1C0h	32	USB2SS_GBL_GPIPE_GUSB3PIPECTL	3100 C2C0h + formula
200h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0	3100 C300h + formula
204h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1	3100 C304h + formula
208h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2	3100 C308h + formula
20Ch	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3	3100 C30Ch + formula
210h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4	3100 C310h + formula
214h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5	3100 C314h + formula
218h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6	3100 C318h + formula
21Ch	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7	3100 C31Ch + formula
220h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8	3100 C320h + formula
224h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9	3100 C324h + formula
228h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10	3100 C328h + formula
22Ch	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11	3100 C32Ch + formula
230h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12	3100 C330h + formula
234h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13	3100 C334h + formula
238h	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14	3100 C338h + formula
23Ch	32	USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15	3100 C33Ch + formula
280h	32	USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0	3100 C380h + formula
284h	32	USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1	3100 C384h + formula
288h	32	USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2	3100 C388h + formula
300h	32	USB2SS_GBL_GEVNT_GEVNTADRLO_J	3100 C400h + formula
304h	32	USB2SS_GBL_GEVNT_GEVNTADRHI_J	3100 C404h + formula
308h	32	USB2SS_GBL_GEVNT_GEVNTSIZ_J	3100 C408h + formula
30Ch	32	USB2SS_GBL_GEVNT_GEVNTCOUNT_J	3100 C40Ch + formula
540h	32	USB2SS_GBL_GRHB_GUSB2RHBCTL	3100 C640h + formula

Table 14-11690. USB2SS_DEV Registers, Base Address=3100 C700h, Length=2048

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_DEV_DCFG	3100 C700h
4h	32	USB2SS_DEV_DCTL	3100 C704h
8h	32	USB2SS_DEV_DEVTEN	3100 C708h
Ch	32	USB2SS_DEV_DSTS	3100 C70Ch
10h	32	USB2SS_DEV_DGCMDPAR	3100 C710h
14h	32	USB2SS_DEV_DGCMD	3100 C714h
20h	32	USB2SS_DEV_DALEPENA	3100 C720h
24h	32	USB2SS_DEV_DEV_RESERVED_RSVD_J	3100 C724h + formula
100h	32	USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_J	3100 C800h + formula
104h	32	USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_J	3100 C804h + formula
108h	32	USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_J	3100 C808h + formula
10Ch	32	USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_J	3100 C80Ch + formula
300h	32	USB2SS_DEV_DEV_INTR_DEV_IMOD_J	3100 CA00h + formula

Table 14-11691. USB2SS_LINK Registers, Base Address=3100 D000h, Length=128

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_LINK_LINK_LU1LFPSRXTIM	3100 D000h + formula
20h	32	USB2SS_LINK_LINK_LINK_SETTINGS	3100 D020h + formula
24h	32	USB2SS_LINK_LINK_LLUCTL	3100 D024h + formula
28h	32	USB2SS_LINK_LINK_LPTMDPDELAY	3100 D028h + formula

Table 14-11692. USB2SS_DEBUG Registers, Base Address=3100 D800h, Length=512

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_DEBUG_DEBUG_U3RHBDBG	3100 D800h + formula

Table 14-11693. USB2SS_DEBUG_RAM0 Registers, Base Address=3104 0000h, Length=65536

Offset	Length	Register Name	USB0 Physical Address
0h	32	USB2SS_DEBUG_RAM0_RAM0_J	3104 0000h + formula

14.7.3.2.2 USB Registers

USB Registers

14.7.3.2.2.1 USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL Register

14.7.3.2.2.1.1 USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL Register (Offset = 80h) [reset = 0h]

Debug trace control register

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Table 14-11694. Instance Table

Instance Name	Physical Address
USB0	0070 3080h

Figure 14-5774. USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD				EN_OUT_EP14	EN_OUT_EP15	EN_IN_EP14	EN_IN_EP15
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-11695. USB2SS_USB2SS_DEBUG_TRACE_TRACE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD	R	0h	Reserved bits Reset Source: cfg_srst_n
3	EN_OUT_EP14	R/W	0h	Debug trace enable for OUT Endpoint 14 Reset Source: cfg_srst_n
2	EN_OUT_EP15	R/W	0h	Debug trace enable for OUT Endpoint 15 Reset Source: cfg_srst_n
1	EN_IN_EP14	R/W	0h	Debug trace enable for IN Endpoint 14 Reset Source: cfg_srst_n
0	EN_IN_EP15	R/W	0h	Debug trace enable for IN Endpoint 15 Reset Source: cfg_srst_n

14.7.3.2.2.2 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_J Register

14.7.3.2.2.2.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_J Register (Offset = 0h) [reset = 0h]

TRB0 Word 0.

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Table 14-11696. Instance Table

Instance Name	Physical Address
USB0	0070 3000h + formula

Figure 14-5775. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_j Name Register

31	30	29	28	27	26	25	24
RSVD2		SID					
R/W		R/W					
0h		0h					
23	22	21	20	19	18	17	16
SID							
R/W							
0h							
15	14	13	12	11	10	9	8
SID		RSVD1		IOC	ISP_IMI	TRBCTL	
R/W		R/W		R/W	R/W	R/W	
0h		0h		0h	0h	0h	
7	6	5	4	3	2	1	0
TRBCTL				CSP	CHN	LST	HWO
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-11697. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
29:14	SID	R/W	0h	Stream ID / SOF Number Reset Source: cfg_srst_n
13:12	RSVD1	R/W	0h	Reserved bits Reset Source: cfg_srst_n
11	IOC	R/W	0h	Interrupt on Complete Reset Source: cfg_srst_n
10	ISP_IMI	R/W	0h	Interrupt on Short Packet / Interrupt on Missed ISOC Reset Source: cfg_srst_n
9:4	TRBCTL	R/W	0h	Indicates the type of TRB Reset Source: cfg_srst_n
3	CSP	R/W	0h	Continue on Short Packet Reset Source: cfg_srst_n
2	CHN	R/W	0h	Chain buffers Reset Source: cfg_srst_n
1	LST	R/W	0h	Indicates this is the last TRB in a list Reset Source: cfg_srst_n

Table 14-11697. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HWO	R/W	0h	Hardware Owner of Descriptor Reset Source: cfg_srst_n

14.7.3.2.2.3 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_J Register

14.7.3.2.2.3.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_J Register (Offset = 4h) [reset = 0h]

TRB0 Word 1.

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Table 14-11698. Instance Table

Instance Name	Physical Address
USB0	0070 3004h + formula

Figure 14-5776. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_j Name Register

31	30	29	28	27	26	25	24
TRBSTS				RSVD2	SPR	PCM1	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
23	22	21	20	19	18	17	16
RESERVED	BUFSIZ						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
BUFSIZ							
R/W							
0h							
7	6	5	4	3	2	1	0
BUFSIZ							
R/W							
0h							

Table 14-11699. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TRBSTS	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
27	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
26	SPR	R/W	0h	Short packet received/Reserved bits Reset Source: cfg_srst_n
25:24	PCM1	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
23	RESERVED	NONE	0h	Reserved
22:0	BUFSIZ	R/W	0h	Buffer Size Reset Source: cfg_srst_n

14.7.3.2.2.4 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_J Register

14.7.3.2.2.4.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_J Register (Offset = 8h) [reset = 0h]

TRB0 Word 2.

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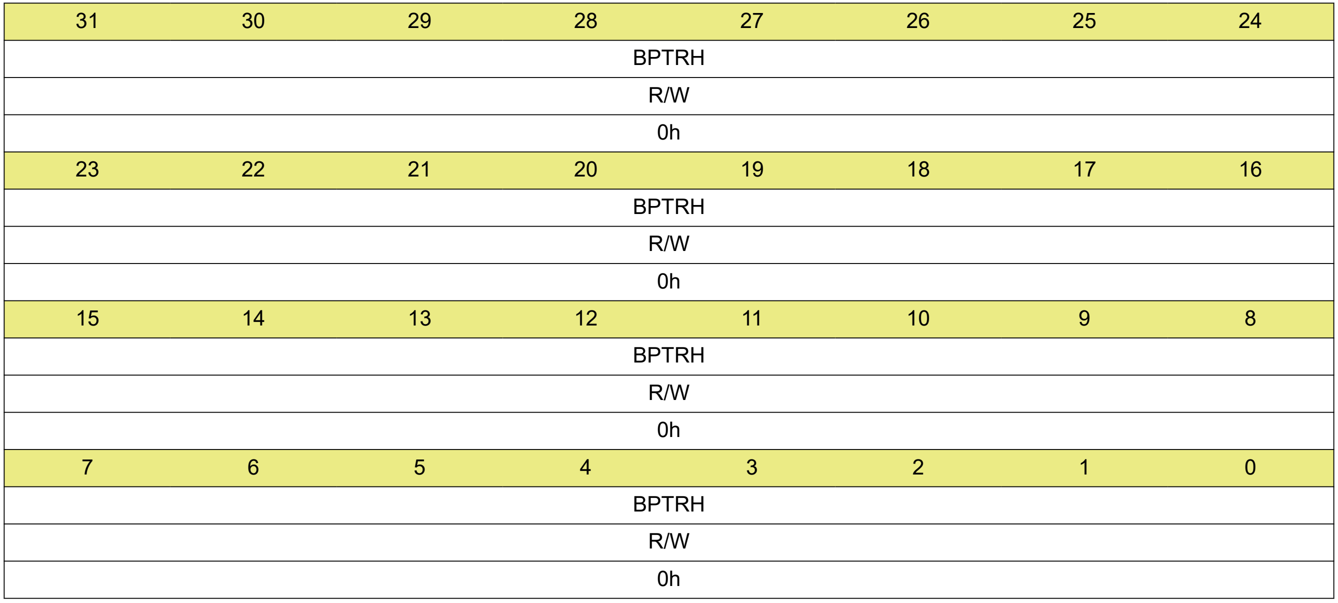
Table 14-11700. Instance Table

Instance Name	Physical Address
USB0	0070 3008h + formula

Figure 14-5777. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_j Name Register



31	30	29	28	27	26	25	24
BPTRH							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRH							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRH							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRH							
R/W							
0h							

Table 14-11701. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRH	R/W	0h	Buffer Pointer High Reset Source: cfg_srst_n

14.7.3.2.2.5 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_J Register

14.7.3.2.2.5.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_J Register (Offset = Ch) [reset = 0h]

TRB0 Word 3.

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Table 14-11702. Instance Table

Instance Name	Physical Address
USB0	0070 300Ch + formula

Figure 14-5778. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_j Name Register

31	30	29	28	27	26	25	24
BPTRL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BPTRL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BPTRL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BPTRL							
R/W							
0h							

Table 14-11703. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB0_W3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRL	R/W	0h	Buffer Pointer Low Reset Source: cfg_srst_n

14.7.3.2.2.6 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_J Register

14.7.3.2.2.6.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_J Register (Offset = 10h) [reset = 0h]

TRB1 Word 0.

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Table 14-11704. Instance Table

Instance Name	Physical Address
USB0	0070 3010h + formula

Figure 14-5779. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_j Name Register

31	30	29	28	27	26	25	24
RSVD2		SID					
R/W		R/W					
0h		0h					
23	22	21	20	19	18	17	16
SID							
R/W							
0h							
15	14	13	12	11	10	9	8
SID		RSVD1		IOC	ISP_IMI	TRBCTL	
R/W		R/W		R/W	R/W	R/W	
0h		0h		0h	0h	0h	
7	6	5	4	3	2	1	0
TRBCTL				CSP	CHN	LST	HWO
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-11705. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
29:14	SID	R/W	0h	Stream ID / SOF Number Reset Source: cfg_srst_n
13:12	RSVD1	R/W	0h	Reserved bits Reset Source: cfg_srst_n
11	IOC	R/W	0h	Interrupt on Complete Reset Source: cfg_srst_n
10	ISP_IMI	R/W	0h	Interrupt on Short Packet / Interrupt on Missed ISOC Reset Source: cfg_srst_n
9:4	TRBCTL	R/W	0h	Indicates the type of TRB Reset Source: cfg_srst_n
3	CSP	R/W	0h	Continue on Short Packet Reset Source: cfg_srst_n
2	CHN	R/W	0h	Chain buffers Reset Source: cfg_srst_n
1	LST	R/W	0h	Indicates this is the last TRB in a list Reset Source: cfg_srst_n

Table 14-11705. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HWO	R/W	0h	Hardware Owner of Descriptor Reset Source: cfg_srst_n

14.7.3.2.2.7 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_J Register

14.7.3.2.2.7.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_J Register (Offset = 14h) [reset = 0h]

TRB1 Word 1.

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Table 14-11706. Instance Table

Instance Name	Physical Address
USB0	0070 3014h + formula

Figure 14-5780. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_j Name Register

31	30	29	28	27	26	25	24
TRBSTS				RSVD2	SPR	PCM1	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
23	22	21	20	19	18	17	16
RESERVED	BUFSIZ						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
BUFSIZ							
R/W							
0h							
7	6	5	4	3	2	1	0
BUFSIZ							
R/W							
0h							

Table 14-11707. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TRBSTS	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
27	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
26	SPR	R/W	0h	Short packet received/Reserved bits Reset Source: cfg_srst_n
25:24	PCM1	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
23	RESERVED	NONE	0h	Reserved
22:0	BUFSIZ	R/W	0h	Buffer Size Reset Source: cfg_srst_n

14.7.3.2.2.8 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_J Register

14.7.3.2.2.8.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_J Register (Offset = 18h) [reset = 0h]

TRB1 Word 2.

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Table 14-11708. Instance Table

Instance Name	Physical Address
USB0	0070 3018h + formula

Figure 14-5781. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_j Name Register

31	30	29	28	27	26	25	24
BPTRH							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRH							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRH							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRH							
R/W							
0h							

Table 14-11709. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRH	R/W	0h	Buffer Pointer High Reset Source: cfg_srst_n

14.7.3.2.2.9 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_J Register

14.7.3.2.2.9.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_J Register (Offset = 1Ch) [reset = 0h]

TRB1 Word 3.

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Table 14-11710. Instance Table

Instance Name	Physical Address
USB0	0070 301Ch + formula

Figure 14-5782. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_j Name Register

31	30	29	28	27	26	25	24
BPTRL							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRL							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRL							
R/W							
0h							

Table 14-11711. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB1_W3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRL	R/W	0h	Buffer Pointer Low Reset Source: cfg_srst_n

14.7.3.2.2.10 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_J Register

14.7.3.2.2.10.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_J Register (Offset = 20h) [reset = 0h]

TRB2 Word 0.

Return to Summary Table

Table 14-11712. Instance Table

Instance Name	Physical Address
USB0	0070 3020h + formula

Figure 14-5783. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_j Name Register

31	30	29	28	27	26	25	24
RSVD2		SID					
R/W		R/W					
0h		0h					
23	22	21	20	19	18	17	16
SID							
R/W							
0h							
15	14	13	12	11	10	9	8
SID		RSVD1		IOC	ISP_IMI	TRBCTL	
R/W		R/W		R/W	R/W	R/W	
0h		0h		0h	0h	0h	
7	6	5	4	3	2	1	0
TRBCTL				CSP	CHN	LST	HWO
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-11713. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
29:14	SID	R/W	0h	Stream ID / SOF Number Reset Source: cfg_srst_n
13:12	RSVD1	R/W	0h	Reserved bits Reset Source: cfg_srst_n
11	IOC	R/W	0h	Interrupt on Complete Reset Source: cfg_srst_n
10	ISP_IMI	R/W	0h	Interrupt on Short Packet / Interrupt on Missed ISOC Reset Source: cfg_srst_n
9:4	TRBCTL	R/W	0h	Indicates the type of TRB Reset Source: cfg_srst_n
3	CSP	R/W	0h	Continue on Short Packet Reset Source: cfg_srst_n
2	CHN	R/W	0h	Chain buffers Reset Source: cfg_srst_n
1	LST	R/W	0h	Indicates this is the last TRB in a list Reset Source: cfg_srst_n

Table 14-11713. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HWO	R/W	0h	Hardware Owner of Descriptor Reset Source: cfg_srst_n

14.7.3.2.2.11 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_J Register

14.7.3.2.2.11.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_J Register (Offset = 24h) [reset = 0h]

TRB2 Word 1.

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Table 14-11714. Instance Table

Instance Name	Physical Address
USB0	0070 3024h + formula

Figure 14-5784. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_j Name Register

31	30	29	28	27	26	25	24
TRBSTS				RSVD2	SPR	PCM1	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
23	22	21	20	19	18	17	16
RESERVED	BUFSIZ						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
BUFSIZ							
R/W							
0h							
7	6	5	4	3	2	1	0
BUFSIZ							
R/W							
0h							

Table 14-11715. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TRBSTS	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
27	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
26	SPR	R/W	0h	Short packet received/Reserved bits Reset Source: cfg_srst_n
25:24	PCM1	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
23	RESERVED	NONE	0h	Reserved
22:0	BUFSIZ	R/W	0h	Buffer Size Reset Source: cfg_srst_n

14.7.3.2.2.12 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_J Register

14.7.3.2.2.12.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_J Register (Offset = 28h) [reset = 0h]

TRB2 Word 2.

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Table 14-11716. Instance Table

Instance Name	Physical Address
USB0	0070 3028h + formula

Figure 14-5785. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BPTRH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BPTRH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BPTRH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BPTRH</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11717. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRH	R/W	0h	Buffer Pointer High Reset Source: cfg_srst_n

14.7.3.2.2.13 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_J Register

14.7.3.2.2.13.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_J Register (Offset = 2Ch) [reset = 0h]

TRB2 Word 3.

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Table 14-11718. Instance Table

Instance Name	Physical Address
USB0	0070 302Ch + formula

Figure 14-5786. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_j Name Register

31	30	29	28	27	26	25	24
BPTRL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BPTRL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BPTRL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BPTRL							
R/W							
0h							

Table 14-11719. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB2_W3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRL	R/W	0h	Buffer Pointer Low Reset Source: cfg_srst_n

14.7.3.2.2.14 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_J Register

14.7.3.2.2.14.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_J Register (Offset = 30h) [reset = 0h]

TRB3 Word 0.

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Table 14-11720. Instance Table

Instance Name	Physical Address
USB0	0070 3030h + formula

Figure 14-5787. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_j Name Register

31	30	29	28	27	26	25	24
RSVD2		SID					
R/W		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SID							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SID		RSVD1		IOC	ISP_IMI	TRBCTL	
R/W		R/W		R/W	R/W	R/W	
0h		0h		0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRBCTL				CSP	CHN	LST	HWO
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-11721. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
29:14	SID	R/W	0h	Stream ID / SOF Number Reset Source: cfg_srst_n
13:12	RSVD1	R/W	0h	Reserved bits Reset Source: cfg_srst_n
11	IOC	R/W	0h	Interrupt on Complete Reset Source: cfg_srst_n
10	ISP_IMI	R/W	0h	Interrupt on Short Packet / Interrupt on Missed ISOC Reset Source: cfg_srst_n
9:4	TRBCTL	R/W	0h	Indicates the type of TRB Reset Source: cfg_srst_n
3	CSP	R/W	0h	Continue on Short Packet Reset Source: cfg_srst_n
2	CHN	R/W	0h	Chain buffers Reset Source: cfg_srst_n
1	LST	R/W	0h	Indicates this is the last TRB in a list Reset Source: cfg_srst_n

Table 14-11721. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HWO	R/W	0h	Hardware Owner of Descriptor Reset Source: cfg_srst_n

14.7.3.2.2.15 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_J Register

14.7.3.2.2.15.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_J Register (Offset = 34h) [reset = 0h]

TRB3 Word 1.

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Table 14-11722. Instance Table

Instance Name	Physical Address
USB0	0070 3034h + formula

Figure 14-5788. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_j Name Register

31	30	29	28	27	26	25	24
TRBSTS				RSVD2	SPR	PCM1	
R/W				R/W	R/W	R/W	
0h				0h	0h	0h	
23	22	21	20	19	18	17	16
RESERVED	BUFSIZ						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
BUFSIZ							
R/W							
0h							
7	6	5	4	3	2	1	0
BUFSIZ							
R/W							
0h							

Table 14-11723. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TRBSTS	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
27	RSVD2	R/W	0h	Reserved bits Reset Source: cfg_srst_n
26	SPR	R/W	0h	Short packet received/Reserved bits Reset Source: cfg_srst_n
25:24	PCM1	R/W	0h	Packet Count M1 Reset Source: cfg_srst_n
23	RESERVED	NONE	0h	Reserved
22:0	BUFSIZ	R/W	0h	Buffer Size Reset Source: cfg_srst_n

14.7.3.2.2.16 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_J Register

14.7.3.2.2.16.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_J Register (Offset = 38h) [reset = 0h]

TRB3 Word 2.

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Table 14-11724. Instance Table

Instance Name	Physical Address
USB0	0070 3038h + formula

Figure 14-5789. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_j Name Register

31	30	29	28	27	26	25	24
BPTRH							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRH							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRH							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRH							
R/W							
0h							

Table 14-11725. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRH	R/W	0h	Buffer Pointer High Reset Source: cfg_srst_n

14.7.3.2.2.17 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_J Register

14.7.3.2.2.17.1 USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_J Register (Offset = 3Ch) [reset = 0h]

TRB3 Word 3.

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Table 14-11726. Instance Table

Instance Name	Physical Address
USB0	0070 303Ch + formula

Figure 14-5790. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_j Name Register

31	30	29	28	27	26	25	24
BPTRL							
R/W							
0h							
23	22	21	20	19	18	17	16
BPTRL							
R/W							
0h							
15	14	13	12	11	10	9	8
BPTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
BPTRL							
R/W							
0h							

Table 14-11727. USB2SS_USB2SS_DEBUG_TRACE_EP_TRB3_W3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BPTRL	R/W	0h	Buffer Pointer Low Reset Source: cfg_srst_n

14.7.3.2.2.18 USB2SS_USB2SS_CFG_REVISION Register

14.7.3.2.2.18.1 USB2SS_USB2SS_CFG_REVISION Register (Offset = 0h) [reset = 68214900h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-11728. Instance Table

Instance Name	Physical Address
USB0	0F90 0000h

Figure 14-5791. USB2SS_USB2SS_CFG_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		821h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
821h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
9h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-11729. USB2SS_USB2SS_CFG_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: cfg_srst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: cfg_srst_n
27:16	MODULE_ID	R	821h	Module ID Reset Source: cfg_srst_n
15:11	RTL	R	9h	RTL revision. Will vary depending on release. Reset Source: cfg_srst_n
10:8	MAJOR	R	1h	Major revision Reset Source: cfg_srst_n
7:6	CUSTOM	R	0h	Custom Reset Source: cfg_srst_n
5:0	MINOR	R	0h	Minor revision Reset Source: cfg_srst_n

14.7.3.2.2.19 USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL Register

14.7.3.2.2.19.1 USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL Register (Offset = 4h) [reset = 10000h]

This register contains bits for indicating overcurrent condition on VBUS to Controller

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Table 14-11730. Instance Table

Instance Name	Physical Address
USB0	0F90 0004h

Figure 14-5792. USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL Name Register

31	30	29	28	27	26	25	24
RSVD3							
R							
0h							
23	22	21	20	19	18	17	16
RSVD3							OVERCURRENT_N
R							R/W
0h							1h
15	14	13	12	11	10	9	8
RSVD2							OVERCURRENT_SEL
R							R/W
0h							0h
7	6	5	4	3	2	1	0
RSVD1							
R							
0h							

Table 14-11731. USB2SS_USB2SS_CFG_OVERCURRENT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RSVD3	R	0h	Reserved bits Reset Source: cfg_srst_n
16	OVERCURRENT_N	R/W	1h	Overcurrent indicator to the Controller Reset Source: cfg_srst_n
15:9	RSVD2	R	0h	Reserved bits Reset Source: cfg_srst_n
8	OVERCURRENT_SEL	R/W	0h	Overcurrent MMR select. Has to be written before setting pwrup_rst_n bit. 1 - overcurrent MMR bit is used, 0 - port_overcurrent_n input is used Reset Source: cfg_srst_n
7:0	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n

14.7.3.2.2.20 USB2SS_USB2SS_CFG_PHY_CONFIG Register

14.7.3.2.2.20.1 USB2SS_USB2SS_CFG_PHY_CONFIG Register (Offset = 8h) [reset = 2h]

Wrapper register containing static settings. All bits in this register directly drive the USB2 PHY inputs. Please refer to USB2 PHY user guide for more information.

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Table 14-11732. Instance Table

Instance Name	Physical Address
USB0	0F90 0008h

Figure 14-5793. USB2SS_USB2SS_CFG_PHY_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED31_9							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_9							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED31_9							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED31_9			RESERVED4_3		VBUS_SEL		LANE_REVERSE
R			R/W		R/W		R/W
0h			0h		1h		0h

Table 14-11733. USB2SS_USB2SS_CFG_PHY_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED31_9	R	0h	Reserved bits
4:3	RESERVED4_3	R/W	0h	Reserved bits
2:1	VBUS_SEL	R/W	1h	This register directly drives the vbus_sel[1:0] input to the PHY. VBUS select - 00: VBUS = 5.25V/3.3V, 01: VBUS/3 external divider is active, so VBUS could be upto 11V. Reset Source: cfg_srst_n
0	LANE_REVERSE	R/W	0h	This register directly drives the lane_reverse input to USB2 PHY. Lane reverse selection. When set, this bit indicates that D+ and D- lines have to be swapped. Reset Source: cfg_srst_n

14.7.3.2.2.21 USB2SS_USB2SS_CFG_PHY_TEST Register

14.7.3.2.2.21.1 USB2SS_USB2SS_CFG_PHY_TEST Register (Offset = Ch) [reset = 0h]

Register containing PLL bypass select, BIST control and status

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Table 14-11734. Instance Table

Instance Name	Physical Address
USB0	0F90 000Ch

Figure 14-5794. USB2SS_USB2SS_CFG_PHY_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED31_18							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED31_18						BIST_MODE	BIST_ERROR_COUNT
R						R/W	R
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIST_ERROR_COUNT							BIST_ERROR
R							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_COMPLETE	BIST_ON	BIST_MODE_EN	BIST_MODE_SEL				RESERVED0
R	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 14-11735. USB2SS_USB2SS_CFG_PHY_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED31_18	R	0h	Reserved bits
17	BIST_MODE	R/W	0h	Set for bist mode. This is used for overriding PHY ports for BIST. Reset Source: cfg_srst_n
16:9	BIST_ERROR_COUNT	R	0h	Number of bytes that have errors while running BIST. The count resets when bist_on is set. Reset Source: cfg_srst_n
8	BIST_ERROR	R	0h	If set, this bit indicates that BIST completed with error. Reset Source: cfg_srst_n
7	BIST_COMPLETE	R	0h	If set, this bit indicates that the BIST operation is completed. Reset Source: cfg_srst_n
6	BIST_ON	R/W	0h	Setting this bit starts the BIST operation. Reset Source: cfg_srst_n
5	BIST_MODE_EN	R/W	0h	BIST Mode Enable. 0 = BIST not enabled, 1 = BIST enabled Reset Source: cfg_srst_n
4:1	BIST_MODE_SEL	R/W	0h	BIST Mode Selection. bist_mode_sel[3]: 0 = 8-bit interface, 1 = 16-bit interface; bist_mode_sel[2]: 0 = error injection disabled, 1 = error injection enabled; bist_mode_sel[1]: 0 = device mode, 1 = host mode; bist_mode_sel[0]: 0 = High Speed mode, 1 = Full Speed mode. Reset Source: cfg_srst_n

Table 14-11735. USB2SS_USB2SS_CFG_PHY_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED0	R/W	0h	Reserved bits

14.7.3.2.2.22 USB2SS_USB2SS_CFG_CORE_STAT Register

14.7.3.2.2.22.1 USB2SS_USB2SS_CFG_CORE_STAT Register (Offset = 14h) [reset = 27E8h]

Register containing miscellaneous status bits from the core

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Table 14-11736. Instance Table

Instance Name	Physical Address
USB0	0F90 0014h

Figure 14-5795. USB2SS_USB2SS_CFG_CORE_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RSVD1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RSVD1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RSVD1</td><td>HUB_VBUS_CTRL</td><td colspan="2">OPERATIONAL_MODE</td><td colspan="4">HOST_CURRENT_BELT</td></tr>
<tr><td>R</td><td>R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">2h</td><td colspan="4">7E8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">HOST_CURRENT_BELT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7E8h</td></tr>
</table>

Table 14-11737. USB2SS_USB2SS_CFG_CORE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n
14	HUB_VBUS_CTRL	R	0h	Indicates whether core is asking for VBUS to be turned on in host mode. Reset Source: cfg_srst_n
13:12	OPERATIONAL_MODE	R	2h	Indicates current operational mode of Controller. This directly reflects the value programmed into GCTL.PRTCAPDIR Controller register. 2'b01 - Host, 2'b10 - Device. Reset Source: cfg_srst_n
11:0	HOST_CURRENT_BELT	R	7E8h	Indicates minimum of all received device BELT values and the BELT value set by the Set Latency Tolerance Value command. Reset Source: cfg_srst_n

14.7.3.2.2.23 USB2SS_USB2SS_CFG_HOST_VBUS_CTRL Register

14.7.3.2.2.23.1 USB2SS_USB2SS_CFG_HOST_VBUS_CTRL Register (Offset = 18h) [reset = 0h]

Register containing software bit for overriding drive VBUS

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Table 14-11738. Instance Table

Instance Name	Physical Address
USB0	0F90 0018h

Figure 14-5796. USB2SS_USB2SS_CFG_HOST_VBUS_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>DRV_VBUS_OVERRIDE</td><td>DRV_VBUS_OVERRIDE_VAL</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11739. USB2SS_USB2SS_CFG_HOST_VBUS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DRV_VBUS_OVERRIDE	R/W	0h	Setting this bit enables drive VBUS override. Drive VBUS output reflects drv_vbus_override_val field value. Reset Source: cfg_srst_n
0	DRV_VBUS_OVERRIDE_VAL	R/W	0h	Drive VBUS output override value. Reset Source: cfg_srst_n

14.7.3.2.2.24 USB2SS_USB2SS_CFG_MODE_CONTROL Register

14.7.3.2.2.24.1 USB2SS_USB2SS_CFG_MODE_CONTROL Register (Offset = 1Ch) [reset = 0h]

Register containing software bit for indicating DRD mode is determined

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Table 14-11740. Instance Table

Instance Name	Physical Address
USB0	0F90 001Ch

Figure 14-5797. USB2SS_USB2SS_CFG_MODE_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MODE_VALID
NONE							R/W
0h							0h

Table 14-11741. USB2SS_USB2SS_CFG_MODE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MODE_VALID	R/W	0h	For DRD applications, software sets this bit when the role is determined based on connect event and ID value from GPIO. Software clears this bit when a disconnect event happens and role is no longer valid. Software can also set this once during initialization for fixed role applications. Reset Source: cfg_srst_n

14.7.3.2.2.25 USB2SS_USB2SS_CFG_WAKEUP_CONFIG Register

14.7.3.2.2.25.1 USB2SS_USB2SS_CFG_WAKEUP_CONFIG Register (Offset = 30h) [reset = 0h]

Register containing low power mode wakeup enables

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Table 14-11742. Instance Table

Instance Name	Physical Address
USB0	0F90 0030h

Figure 14-5798. USB2SS_USB2SS_CFG_WAKEUP_CONFIG Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	22	21	20	19	18	17	16
RSVD1							
R							
0h							
15	14	13	12	11	10	9	8
RSVD1							
R							
0h							
7	6	5	4	3	2	1	0
RSVD1				OVERCURRENT_WAKEUP_EN	LINESTATE_WAKEUP_EN	SESSVALID_WAKEUP_EN	VBUSVALID_WAKEUP_EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-11743. USB2SS_USB2SS_CFG_WAKEUP_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n
3	OVERCURRENT_WAKEUP_EN	R/W	0h	overcurrent event wakeup enable Reset Source: cfg_srst_n
2	LINESTATE_WAKEUP_EN	R/W	0h	linestate event wakeup enable Reset Source: cfg_srst_n
1	SESSVALID_WAKEUP_EN	R/W	0h	SESSVALID event wakeup enable Reset Source: cfg_srst_n
0	VBUSVALID_WAKEUP_EN	R/W	0h	VBUSVALID event wakeup enable Reset Source: cfg_srst_n

14.7.3.2.2.26 USB2SS_USB2SS_CFG_WAKEUP_STAT Register

14.7.3.2.2.26.1 USB2SS_USB2SS_CFG_WAKEUP_STAT Register (Offset = 34h) [reset = 0h]

Register containing low power mode status bits. The status bits are set when the corresponding wakeup event happens and the corresponding enable in WAKEUP_CONFIG MMR is set. In addition, these bits are only set if clockstop request from PSC is active in order to ensure that these are captured only during low power mode and not during regular operation. These bits can only be set by hardware and once set, they can only be cleared by software by setting wakeup_stat_clear field.

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Table 14-11744. Instance Table

Instance Name	Physical Address
USB0	0F90 0034h

Figure 14-5799. USB2SS_USB2SS_CFG_WAKEUP_STAT Name Register

31	30	29	28	27	26	25	24
RSVD1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSVD1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSVD1	OVERCURRENT_N_WAKEUP_CURRENT	OVERCURRENT_N_WAKEUP_PREV	LINESTATE_WAKEUP_CURRENT		LINESTATE_WAKEUP_PREV		SESSVALID_WAKEUP_CURRENT
R	R	R	R		R		R
0h	0h	0h	0h		0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SESSVALID_WAKEUP_PREV	VBUSVALID_WAKEUP_CURRENT	VBUSVALID_WAKEUP_PREV	OVERCURRENT_N_WAKEUP_STAT	LINESTATE_WAKEUP_STAT	SESSVALID_WAKEUP_STAT	VBUSVALID_WAKEUP_STAT	WAKEUP_STAT_CLEAR
R	R	R	R	R	R	R	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11745. USB2SS_USB2SS_CFG_WAKEUP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n
14	OVERCURRENT_N_WAKEUP_CURRENT	R	0h	overcurrent_n current value during wakeup event Reset Source: cfg_srst_n
13	OVERCURRENT_N_WAKEUP_PREV	R	0h	overcurrent_n previous value during wakeup event Reset Source: cfg_srst_n
12:11	LINESTATE_WAKEUP_CURRENT	R	0h	Linestate current value during wakeup event Reset Source: cfg_srst_n
10:9	LINESTATE_WAKEUP_PREV	R	0h	Linestate previous value during wakeup event Reset Source: cfg_srst_n
8	SESSVALID_WAKEUP_CURRENT	R	0h	SESSVALID current value during wakeup event Reset Source: cfg_srst_n

Table 14-11745. USB2SS_USB2SS_CFG_WAKEUP_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SESSVALID_WAKEUP_PREV	R	0h	SESSVALID previous value during wakeup event Reset Source: cfg_srst_n
6	VBUSVALID_WAKEUP_CURRENT	R	0h	VBUSVALID current value during wakeup event Reset Source: cfg_srst_n
5	VBUSVALID_WAKEUP_PREV	R	0h	VBUSVALID previous value during wakeup event Reset Source: cfg_srst_n
4	OVERCURRENT_N_WAKEUP_STAT	R	0h	overcurrent_n event wakeup status. This is only looking for change on port_overcurrent_n input and does not include overcurrent MMR. This is because wakeup is required only for a port event and for any software write to happen, SOC should already have been awake. Also SOC may be tying off port_overcurrent_n, so this event may never trigger. Reset Source: cfg_srst_n
3	LINESTATE_WAKEUP_STAT	R	0h	linestate event wakeup status Reset Source: cfg_srst_n
2	SESSVALID_WAKEUP_STAT	R	0h	SESSVALID event wakeup status Reset Source: cfg_srst_n
1	VBUSVALID_WAKEUP_STAT	R	0h	VBUSVALID event wakeup status Reset Source: cfg_srst_n
0	WAKEUP_STAT_CLEAR	R/W1TC	0h	Clears all the *_wakeup_stat bits in this register Reset Source: cfg_srst_n

14.7.3.2.2.27 USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Register

14.7.3.2.2.27.1 USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Register (Offset = 38h) [reset = 0h]

Register containing various overrides

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Table 14-11746. Instance Table

Instance Name	Physical Address
USB0	0F90 0038h

Figure 14-5800. USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Name Register

31	30	29	28	27	26	25	24
PHY_HVM_EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							XCVRSEL_HVM_OVERRIDE_VAL
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
XCVRSEL_HVM_OVERRIDE_VAL	TERMSEL_HVM_OVERRIDE_VAL	OPMODE_HVM_OVERRIDE_VAL		DMPULLDOWN_HVM_OVERRIDE_VAL	DPPULLDOWN_HVM_OVERRIDE_VAL	RESERVED	
R/W	R/W	R/W		R/W	R/W	NONE	
0h	0h	0h		0h	0h	0h	
7	6	5	4	3	2	1	0
SUSPEND_OVERRIDE_VAL	SUSPEND_OVERRIDE_SEL	TXBITSTUFFEN_OVERRIDE_VAL	TXBITSTUFFEN_OVERRIDE_SEL	SESSVALID_OVERRIDE_VAL	SESSVALID_OVERRIDE_SEL	VBUSVALID_OVERRIDE_VAL	VBUSVALID_OVERRIDE_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11747. USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_HVM_EN	R/W	0h	Enable PHY HVM overrides. Reset Source: cfg_srst_n
30:17	RESERVED	NONE	0h	Reserved
16:15	XCVRSEL_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY xcvr input. The value in this field is applied to PHY xcvrsel input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n
14	TERMSEL_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY termsel input. The value in this field is applied to PHY termsel input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n
13:12	OPMODE_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY opmode input. The value in this field is applied to PHY opmode input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n

Table 14-11747. USB2SS_USB2SS_CFG_OVERRIDE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DMPULLDOWN_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY dmpulldown input. The value in this field is applied to PHY dmpulldown input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n
10	DPPULLDOWN_HVM_OVERRIDE_VAL	R/W	0h	Override value for PHY dppulldown input. The value in this field is applied to PHY dppulldown input if phy_hvm_en bit in this register is set. Reset Source: cfg_srst_n
9:8	RESERVED	NONE	0h	Reserved
7	SUSPEND_OVERRIDE_VAL	R/W	0h	Suspend override value. 0 - suspendm is asserted and clockstop idle term indicates idle, 1 - suspendm is deasserted and clockstop idle term indicates non-idle. Reset Source: cfg_srst_n
6	SUSPEND_OVERRIDE_SEL	R/W	0h	Suspend override selector. This has to be set to override utmi_suspend_n from Controller that goes to clockstop idle. This does not affect suspend going to PHY. Only purpose of this is to ease clockstop interface DV. Reset Source: cfg_srst_n
5	TXBITSTUFFEN_OVERRIDE_VAL	R/W	0h	TXBITSTUFFENABLE override value Reset Source: cfg_srst_n
4	TXBITSTUFFEN_OVERRIDE_SEL	R/W	0h	TXBITSTUFFENABLE override selector. This has to be set to override TXBITSTUFFENABLE to PHY. Reset Source: cfg_srst_n
3	SESSVALID_OVERRIDE_VAL	R/W	0h	SESSVALID override value. 1 - Session is valid, 0 - Session is not valid Reset Source: cfg_srst_n
2	SESSVALID_OVERRIDE_SEL	R/W	0h	SESSVALID override selector. This has to be set to override sessvalid from PHY to Controller. Reset Source: cfg_srst_n
1	VBUSVALID_OVERRIDE_VAL	R/W	0h	VBUSVALID override value. 1 - VBUS is valid, 0 - VBUS is not valid Reset Source: cfg_srst_n
0	VBUSVALID_OVERRIDE_SEL	R/W	0h	VBUSVALID override selector. This has to be set to override vbusvalid from PHY to Controller. Reset Source: cfg_srst_n

14.7.3.2.2.28 USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW Register

14.7.3.2.2.28.1 USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW Register (Offset = 430h) [reset = 0h]

The IRQ_STATUS_RAW_MISC register allows the usbss interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-11748. Instance Table

Instance Name	Physical Address
USB0	0F90 0430h

Figure 14-5801. USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED31_23							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_23	VBUSVALID_CHANGE	RESERVED21	SESSVALID_CHANGE	RESERVED19_0			
R	R/W1TS	R	R/W1TS	R			
0h	0h	0h	0h	0h			
15	14	13	12	11	10	9	8
RESERVED19_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED19_0							
R							
0h							

Table 14-11749. USB2SS_USB2SS_CFG_IRQ_MISC_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED31_23	R	0h	Reserved bits
22	VBUSVALID_CHANGE	R/W1TS	0h	Set when VBUSVALID changes state Reset Source: cfg_srst_n
21	RESERVED21	R	0h	Reserved bits
20	SESSVALID_CHANGE	R/W1TS	0h	Set when SESSVALID changes state Reset Source: cfg_srst_n
19:0	RESERVED19_0	R	0h	Reserved bits

14.7.3.2.2.29 USB2SS_USB2SS_CFG_IRQ_MISC_STATUS Register

14.7.3.2.2.29.1 USB2SS_USB2SS_CFG_IRQ_MISC_STATUS Register (Offset = 434h) [reset = 0h]

The IRQ_STATUS_MISC register allows the usbss interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-11750. Instance Table

Instance Name	Physical Address
USB0	0F90 0434h

Figure 14-5802. USB2SS_USB2SS_CFG_IRQ_MISC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED31_23							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_23	VBUSVALID_CHANGE	RESERVED21	SESSVALID_CHANGE	RESERVED19_0			
R	R/W1TC	R	R/W1TC	R			
0h	0h	0h	0h	0h			
15	14	13	12	11	10	9	8
RESERVED19_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED19_0							
R							
0h							

Table 14-11751. USB2SS_USB2SS_CFG_IRQ_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED31_23	R	0h	Reserved bits
22	VBUSVALID_CHANGE	R/W1TC	0h	Set when VBUSVALID changes state Reset Source: cfg_srst_n
21	RESERVED21	R	0h	Reserved bits
20	SESSVALID_CHANGE	R/W1TC	0h	Set when SESSVALID changes state Reset Source: cfg_srst_n
19:0	RESERVED19_0	R	0h	Reserved bits

14.7.3.2.2.30 USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET Register

14.7.3.2.2.30.1 USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET Register (Offset = 438h) [reset = 0h]

The IRQ_ENABLE_SET_MISC register allows the usbss interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-11752. Instance Table

Instance Name	Physical Address
USB0	0F90 0438h

Figure 14-5803. USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED31_23</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED31_23</td><td>VBUSVALID_CHANGE</td><td>RESERVED21</td><td>SESSVALID_CHANGE</td><td colspan="4">RESERVED19_0</td></tr>
<tr><td>R</td><td>R/W1TS</td><td>R</td><td>R/W1TS</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED19_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED19_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11753. USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED31_23	R	0h	Reserved bits
22	VBUSVALID_CHANGE	R/W1TS	0h	Event enable Reset Source: cfg_srst_n
21	RESERVED21	R	0h	Reserved bits
20	SESSVALID_CHANGE	R/W1TS	0h	Event enable Reset Source: cfg_srst_n
19:0	RESERVED19_0	R	0h	Reserved bits

14.7.3.2.2.31 USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR Register

14.7.3.2.2.31.1 USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR Register (Offset = 43Ch) [reset = 0h]

The IRQ_ENABLE_CLR_MISC register allows the usbss interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-11754. Instance Table

Instance Name	Physical Address
USB0	0F90 043Ch

Figure 14-5804. USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED31_23							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_23	VBUSVALID_CHANGE	RESERVED21	SESSVALID_CHANGE	RESERVED19_0			
R	R/W1TC	R	R/W1TC	R			
0h	0h	0h	0h	0h			
15	14	13	12	11	10	9	8
RESERVED19_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED19_0							
R							
0h							

Table 14-11755. USB2SS_USB2SS_CFG_IRQ_MISC_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED31_23	R	0h	Reserved bits
22	VBUSVALID_CHANGE	R/W1TC	0h	Event enable Reset Source: cfg_srst_n
21	RESERVED21	R	0h	Reserved bits
20	SESSVALID_CHANGE	R/W1TC	0h	Event enable Reset Source: cfg_srst_n
19:0	RESERVED19_0	R	0h	Reserved bits

14.7.3.2.2.32 USB2SS_USB2SS_CFG_IRQ_MISC_EOI Register

14.7.3.2.2.32.1 USB2SS_USB2SS_CFG_IRQ_MISC_EOI Register (Offset = 440h) [reset = 0h]

EOI vector for re-triggering interrupts

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Table 14-11756. Instance Table

Instance Name	Physical Address
USB0	0F90 0440h

Figure 14-5805. USB2SS_USB2SS_CFG_IRQ_MISC_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							R/W
0h							0h

Table 14-11757. USB2SS_USB2SS_CFG_IRQ_MISC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	R/W	0h	EOI vector for misc interrupt. Has to be written to 0 after ISR services misc interrupt. Reset Source: cfg_srst_n

14.7.3.2.2.33 USB2SS_USB2SS_CFG_INTR_TEST Register

14.7.3.2.2.33.1 USB2SS_USB2SS_CFG_INTR_TEST Register (Offset = 490h) [reset = 0h]

Register for overriding various Controller interrupts for easy activation during DV. NOTE: This is only for internal purposes and should NOT be used during functional operation.

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Table 14-11758. Instance Table

Instance Name	Physical Address
USB0	0F90 0490h

Figure 14-5806. USB2SS_USB2SS_CFG_INTR_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							HOST_SYSTEM_ERR_TEST
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
IRQ_TEST							
R/W							
0h							

Table 14-11759. USB2SS_USB2SS_CFG_INTR_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	HOST_SYSTEM_ERR_TEST	R/W	0h	Test for host system error interrupt. Set 1 to cause host_system_error_intr to trigger and clear this bit to clear the interrupt condition. Reset Source: cfg_srst_n
7:0	IRQ_TEST	R/W	0h	Test for irq interrupts from core. Each bit sets corresponding irq_intr bit. Set 1 to each bit based on whether that interrupt needs to trigger and clear the bit in ISR to clear interrupt condition. Reset Source: cfg_srst_n

14.7.3.2.2.34 USB2SS_USB2SS_CFG_VBUS_FILTER Register

14.7.3.2.2.34.1 USB2SS_USB2SS_CFG_VBUS_FILTER Register (Offset = 614h) [reset = 104h]

The vbus comparator signals may be filtered by controlling these register values.

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Table 14-11760. Instance Table

Instance Name	Physical Address
USB0	0F90 0614h

Figure 14-5807. USB2SS_USB2SS_CFG_VBUS_FILTER Name Register

31	30	29	28	27	26	25	24
RESERVED31_9							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_9							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED31_9							SESSVALID_BYPASS
R							R/W
0h							1h
7	6	5	4	3	2	1	0
SESSVALID_THRESH		RESERVED5_3			VBUSVALID_BYPASS	VBUSVALID_THRESH	
R/W		R			R/W	R/W	
0h		0h			1h	0h	

Table 14-11761. USB2SS_USB2SS_CFG_VBUS_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED31_9	R	0h	Reserved bits
8	SESSVALID_BYPASS	R/W	1h	0= use filter, 1= bypass filter Reset Source: cfg_srst_n
7:6	SESSVALID_THRESH	R/W	0h	00= 1us,01= 100us,10= 5ms,11= 50ms. 4 utmi_clk latency for sessvalid Reset Source: cfg_srst_n
5:3	RESERVED5_3	R	0h	Reserved bits
2	VBUSVALID_BYPASS	R/W	1h	0= use filter, 1= bypass filter for vbusvalid Reset Source: cfg_srst_n
1:0	VBUSVALID_THRESH	R/W	0h	00= 1us,01= 100us,10= 5ms,11= 50ms. 4 utmi_clk latency for vbusvalid Reset Source: cfg_srst_n

14.7.3.2.2.35 USB2SS_USB2SS_CFG_VBUS_STAT Register

14.7.3.2.2.35.1 USB2SS_USB2SS_CFG_VBUS_STAT Register (Offset = 618h) [reset = 0h]

Status bits of VBUS detected signals after filter.

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Table 14-11762. Instance Table

Instance Name	Physical Address
USB0	0F90 0618h

Figure 14-5808. USB2SS_USB2SS_CFG_VBUS_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED31_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED31_3							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED31_3					SESSVALID	RESERVED1_1	VBUSVALID
R					R	R	R
0h					0h	0h	0h

Table 14-11763. USB2SS_USB2SS_CFG_VBUS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED31_3	R	0h	Reserved bits
2	SESSVALID	R	0h	Filtered SESSVALID Reset Source: cfg_srst_n
1	RESERVED1_1	R	0h	Reserved bits
0	VBUSVALID	R	0h	Filtered VBUSVALID Reset Source: cfg_srst_n

14.7.3.2.2.36 USB2SS_USB2SS_CFG_DEBUG_CFG Register

14.7.3.2.2.36.1 USB2SS_USB2SS_CFG_DEBUG_CFG Register (Offset = 708h) [reset = 0h]

Configuration of debug data for observation. 0x0 or 0x7 = debug outputs are tied low, 0x1 = debug outputs are UTMI interface signals, 0x2 = debug outputs are Controller debug[31:0] output 0x3 = debug outputs are Controller debug[63:32] output, 0x4 = debug outputs are clk_gate_ctrl and debug[66:64] Controller outputs, 0x5 = debug outputs are controller logic_analyzer_trace[31:0], 0x6 = debug outputs are controller logic_analyzer_trace[63:32]

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Table 14-11764. Instance Table

Instance Name	Physical Address
USB0	0F90 0708h

Figure 14-5809. USB2SS_USB2SS_CFG_DEBUG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED31_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED31_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED31_3							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED31_3					SEL		
R					R/W		
0h					0h		

Table 14-11765. USB2SS_USB2SS_CFG_DEBUG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED31_3	R	0h	Reserved
2:0	SEL	R/W	0h	selection of observed local signals Reset Source: cfg_srst_n

14.7.3.2.2.37 USB2SS_USB2SS_CFG_DEBUG_DATA Register

14.7.3.2.2.37.1 USB2SS_USB2SS_CFG_DEBUG_DATA Register (Offset = 70Ch) [reset = 0h]

Debug data

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Table 14-11766. Instance Table

Instance Name	Physical Address
USB0	0F90 070Ch

Figure 14-5810. USB2SS_USB2SS_CFG_DEBUG_DATA Name Register

31	30	29	28	27	26	25	24
VAL							
R							
0h							
23	22	21	20	19	18	17	16
VAL							
R							
0h							
15	14	13	12	11	10	9	8
VAL							
R							
0h							
7	6	5	4	3	2	1	0
VAL							
R							
0h							

Table 14-11767. USB2SS_USB2SS_CFG_DEBUG_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R	0h	tmp Reset Source: cfg_srst_n

14.7.3.2.2.38 USB2SS_USB2SS_CFG_HOST_HUB_CTRL Register

14.7.3.2.2.38.1 USB2SS_USB2SS_CFG_HOST_HUB_CTRL Register (Offset = 714h) [reset = 2h]

The HOST_HUB_CTRL Register is a collection of various input signals that control the xHC controllers Host or Hub interfaces. These signals are used regardless if a Host or Hub is implemented or not.

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Table 14-11768. Instance Table

Instance Name	Physical Address
USB0	0F90 0714h

Figure 14-5811. USB2SS_USB2SS_CFG_HOST_HUB_CTRL Name Register

31	30	29	28	27	26	25	24
RSVD3							
R							
0h							
23	22	21	20	19	18	17	16
RSVD3							
R							
0h							
15	14	13	12	11	10	9	8
RSVD3						BUS_FILTER_BYPASS	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
BUS_FILTER_BYPASS		HUB_PORT_PERM_ATTACH	RSVD2			HOST_PORT_POWER_CONTROL_PRESENT	RSVD1
R/W		R/W	R			R/W	R
0h		0h	0h			1h	0h

Table 14-11769. USB2SS_USB2SS_CFG_HOST_HUB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RSVD3	R	0h	Reserved bits Reset Source: cfg_srst_n
9:6	BUS_FILTER_BYPASS	R/W	0h	Bus Filter Bypass bit [0]: bypass the filter for vbusvalid bit bit [2]: bypass the filter for sessvalid Reset Source: cfg_srst_n
5	HUB_PORT_PERM_ATTACH	R/W	0h	Indicates if the device attached to a downstream port is permanently attached or not. Bit 6 is the USB2 port and bit 7 is the SS port. 0 - Not permanently attached 1 - Permanently attached Reset Source: cfg_srst_n
4:2	RSVD2	R	0h	Reserved bits Reset Source: cfg_srst_n
1	HOST_PORT_POWER_CONTROL_PRESENT	R/W	1h	This port defines the bit [3] of Capability Parameters (HCCPARAMS). Change the PPC value through the pin Port Power Control (PPC). This indicates whether the host controller implementation includes port power control. 0 - Indicates that the port does not have port power switches. 1 - Indicates that the port has port power switches. Reset Source: cfg_srst_n

Table 14-11769. USB2SS_USB2SS_CFG_HOST_HUB_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RSVD1	R	0h	Reserved bits Reset Source: cfg_srst_n

14.7.3.2.2.39 USB2SS_PHY2_AFE_TX_REG0 Register

14.7.3.2.2.39.1 USB2SS_PHY2_AFE_TX_REG0 Register (Offset = 0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11770. Instance Table

Instance Name	Physical Address
USB0	0F90 8000h

Figure 14-5812. USB2SS_PHY2_AFE_TX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG0	BF_6_2					BF_1	BF_0
R/W	R/W					R/W	R/W
0h	0h					0h	0h

Table 14-11771. USB2SS_PHY2_AFE_TX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:2	BF_6_2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	BF_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.40 USB2SS_PHY2_AFE_TX_REG1 Register

14.7.3.2.2.40.1 USB2SS_PHY2_AFE_TX_REG1 Register (Offset = 4h) [reset = 0h]

HS TX trimming

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Table 14-11772. Instance Table

Instance Name	Physical Address
USB0	0F90 8004h

Figure 14-5813. USB2SS_PHY2_AFE_TX_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>TX_ANA_REG1</td><td colspan="6">BF_6_1</td><td>BF_0</td></tr>
<tr><td>R/W</td><td colspan="6">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
</table>

Table 14-11773. USB2SS_PHY2_AFE_TX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG1	R/W	0h	0 SCALE1 VALUE IS 0, 1 SCALE1 VALUE IS 0.5 Reset Source: usb2_sync_preset_n

Table 14-11773. USB2SS_PHY2_AFE_TX_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:1	BF_6_1	R/W	0h	000000 BOOST CODE VALUE IS 0, 000001 BOOST CODE VALUE IS 1, 000010 BOOST CODE VALUE IS 2, 00011 BOOST CODE VALUE IS 3, 000100 BOOST CODE VALUE IS 4, 000101 BOOST CODE VALUE IS 5, 000110 BOOST CODE VALUE IS 6, 000111 BOOST CODE VALUE IS 7, 001000 BOOST CODE VALUE IS 8, 001001 BOOST CODE VALUE IS 9, 001010 BOOST CODE VALUE IS 10, 001011 BOOST CODE VALUE IS 11, 001100 BOOST CODE VALUE IS 12, 001101 BOOST CODE VALUE IS 13, 001110 BOOST CODE VALUE IS 14, 001111 BOOST CODE VALUE IS 15, 010000 BOOST CODE VALUE IS 16, 010001 BOOST CODE VALUE IS 17, 010010 BOOST CODE VALUE IS 18, 010011 BOOST CODE VALUE IS 19, 010100 BOOST CODE VALUE IS 20, 010101 BOOST CODE VALUE IS 21, 010110 BOOST CODE VALUE IS 22, 010111 BOOST CODE VALUE IS 23, 011000 BOOST CODE VALUE IS 24, 011001 BOOST CODE VALUE IS 24, 011010 BOOST CODE VALUE IS 26, 011011 BOOST CODE VALUE IS 27, 011100 BOOST CODE VALUE IS 28, 011101 BOOST CODE VALUE IS 29, 011110 BOOST CODE VALUE IS 30, 011111 BOOST CODE VALUE IS 31, 100000 BOOST CODE VALUE IS 16, 100001 BOOST CODE VALUE IS 17, 100010 BOOST CODE VALUE IS 18, 100011 BOOST CODE VALUE IS 19, 100100 BOOST CODE VALUE IS 20, 100101 BOOST CODE VALUE IS 21, 100110 BOOST CODE VALUE IS 22, 100111 BOOST CODE VALUE IS 23, 101000 BOOST CODE VALUE IS 24 , 101001 BOOST CODE VALUE IS 24, 101010 BOOST CODE VALUE IS 26, 101011 BOOST CODE VALUE IS 27, 101100 BOOST CODE VALUE IS 28, 101101 BOOST CODE VALUE IS 29, 101110 BOOST CODE VALUE IS 30, 101111 BOOST CODE VALUE IS 31, 110000 BOOST CODE VALUE IS 32, 110001 BOOST CODE VALUE IS 33, 110010 BOOST CODE VALUE IS 34, 110011 BOOST CODE VALUE IS 35, 110100 BOOST CODE VALUE IS 36, 110101 BOOST CODE VALUE IS 37, 110110 BOOST CODE VALUE IS 38, 110111 BOOST CODE VALUE IS 39, 111000 BOOST CODE VALUE IS 40, 111001 BOOST CODE VALUE IS 41, 111010 BOOST CODE VALUE IS 42, 111011 BOOST CODE VALUE IS 43, 111100 BOOST CODE VALUE IS 44, 111101 BOOST CODE VALUE IS 45, 111110 BOOST CODE VALUE IS 46, 111111 BOOST CODE VALUE IS 47. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	0 Default BOOST CODE = 8, 1 BOOST CODE can be controlled by BITS [6:1]. Reset Source: usb2_sync_preset_n

14.7.3.2.2.41 USB2SS_PHY2_AFE_TX_REG2 Register

14.7.3.2.2.41.1 USB2SS_PHY2_AFE_TX_REG2 Register (Offset = 8h) [reset = 0h]

HS TX trimming

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Table 14-11774. Instance Table

Instance Name	Physical Address
USB0	0F90 8008h

Figure 14-5814. USB2SS_PHY2_AFE_TX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG2	BF_6	BF_5_1					BF_0
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-11775. USB2SS_PHY2_AFE_TX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11775. USB2SS_PHY2_AFE_TX_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:1	BF_5_1	R/W	0h	00000 DEEMP CODE VALUE IS 0, 00001 DEEMP CODE VALUE IS 1, 00010 DEEMP CODE VALUE IS 2, 00011 DEEMP CODE VALUE IS 3, 00100 DEEMP CODE VALUE IS 4, 00101 DEEMP CODE VALUE IS 5, 00110 DEEMP CODE VALUE IS 6, 00111 DEEMP CODE VALUE IS 7, 01000 DEEMP CODE VALUE IS 8, 01001 DEEMP CODE VALUE IS 9, 01010 DEEMP CODE VALUE IS 10, 01011 DEEMP CODE VALUE IS 11, 01100 DEEMP CODE VALUE IS 12, 01101 DEEMP CODE VALUE IS 13, 01110 DEEMP CODE VALUE IS 14, 01111 DEEMP CODE VALUE IS 15, 10000 DEEMP CODE VALUE IS 8, 10001 DEEMP CODE VALUE IS 9, 10010 DEEMP CODE VALUE IS 10, 10011 DEEMP CODE VALUE IS 11, 10100 DEEMP CODE VALUE IS 12, 10101 DEEMP CODE VALUE IS 13, 10110 DEEMP CODE VALUE IS 14, 10111 DEEMP CODE VALUE IS 15, 11000 DEEMP CODE VALUE IS 16, 11001 DEEMP CODE VALUE IS 17, 11010 DEEMP CODE VALUE IS 18, 11011 DEEMP CODE VALUE IS 19, 11100 DEEMP CODE VALUE IS 20, 11101 DEEMP CODE VALUE IS 21, 11110 DEEMP CODE VALUE IS 22, 11111 DEEMP CODE VALUE IS 23. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	0 Default DEEMP CODE = 8, 1 DEEMP CODE can be controlled by BITS 5:1. Reset Source: usb2_sync_preset_n

14.7.3.2.2.42 USB2SS_PHY2_AFE_TX_REG3 Register

14.7.3.2.2.42.1 USB2SS_PHY2_AFE_TX_REG3 Register (Offset = Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11776. Instance Table

Instance Name	Physical Address
USB0	0F90 800Ch

Figure 14-5815. USB2SS_PHY2_AFE_TX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG3			BF_4_1				BF_0
R/W			R/W				R/W
0h			0h				0h

Table 14-11777. USB2SS_PHY2_AFE_TX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	TX_ANA_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	BF_4_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.43 USB2SS_PHY2_AFE_TX_REG4 Register

14.7.3.2.2.43.1 USB2SS_PHY2_AFE_TX_REG4 Register (Offset = 10h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11778. Instance Table

Instance Name	Physical Address
USB0	0F90 8010h

Figure 14-5816. USB2SS_PHY2_AFE_TX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG4	BF_6	BF_5	BF_4_1				BF_0
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 14-11779. USB2SS_PHY2_AFE_TX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BF_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	BF_4_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.44 USB2SS_PHY2_AFE_TX_REG5 Register

14.7.3.2.2.44.1 USB2SS_PHY2_AFE_TX_REG5 Register (Offset = 14h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11780. Instance Table

Instance Name	Physical Address
USB0	0F90 8014h

Figure 14-5817. USB2SS_PHY2_AFE_TX_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_TX_REG5	BF_6_1						BF_0
R/W	R/W						R/W
0h	0h						0h

Table 14-11781. USB2SS_PHY2_AFE_TX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	AFE_TX_REG5	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6:1	BF_6_1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BF_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.45 USB2SS_PHY2_AFE_TX_REG6 Register

14.7.3.2.2.45.1 USB2SS_PHY2_AFE_TX_REG6 Register (Offset = 18h) [reset = 0h]

LSTX rise time trimming

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Table 14-11782. Instance Table

Instance Name	Physical Address
USB0	0F90 8018h

Figure 14-5818. USB2SS_PHY2_AFE_TX_REG6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_ANA_REG6</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11783. USB2SS_PHY2_AFE_TX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG6	R/W	0h	Bit 7 = unused. Bbits 6:3= 0000 Typical LSTx rise time = 375ns, 0001 Typical LSTx rise time =215ns, 0010 Typical LSTx rise time =215ns, 0011 Typical LSTx rise time =150ns, 0100 Typical LSTx rise time =215ns, 0101 Typical LSTx rise time =150ns, 0110 Typical LSTx rise time =150ns, 0111 Typical LSTx rise time =115ns, 1000 Typical LSTx rise time =150ns, 1001 Typical LSTx rise time =115ns, 1010 Typical LSTx rise time =115ns, 1011 Typical LSTx rise time =94ns, 1100 Typical LSTx rise time =115ns, 1101 Typical LSTx rise time =94ns, 1110 Typical LSTx rise time =94ns, 1111 Typical LSTx rise time =79ns. Bit 6= 0 Typical LSTx rise time is set to default value of 150ns, 1 LSTX RISE TIME IS DETERMINED BY BITS 6:2. Bits 1:0 = reserved. Reset Source: usb2_sync_preset_n

14.7.3.2.2.46 USB2SS_PHY2_AFE_TX_REG7 Register

14.7.3.2.2.46.1 USB2SS_PHY2_AFE_TX_REG7 Register (Offset = 1Ch) [reset = 0h]

FSTX rise time trimming

Return to Summary Table

Table 14-11784. Instance Table

Instance Name	Physical Address
USB0	0F90 801Ch

Figure 14-5819. USB2SS_PHY2_AFE_TX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG7							
R/W							
0h							

Table 14-11785. USB2SS_PHY2_AFE_TX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG7	R/W	0h	Bits 7:5= reserved. Bits 4:1= 0000 Typical FSTx rise time = 16.6ns, 0001 Typical FSTx rise time =16.1ns, 0010 Typical FSTx rise time =15.6ns, 0011 Typical FSTx rise time =15.2ns, 0100 Typical FSTx rise time =14.7ns, 0101 Typical FSTx rise time =14.3ns, 0110 Typical FSTx rise time =13.9ns, 0111 Typical FSTx rise time =13.6ns, 1000 Typical FSTx rise time =13.2ns, 1001 Typical FSTx rise time =12.9ns, 1010 Typical FSTx rise time =12.6ns, 1011 Typical FSTx rise time =12.3ns, 1100 Typical FSTx rise time =12.0ns, 1101 Typical FSTx rise time =11.7ns, 1110 Typical FSTx rise time =11.5ns, 1111 Typical FSTx rise time =11.2ns. Bit 0= 0 FSTx rise time at typical corner is set to default value of 12ns, 1 FSTX RISE TIME IS DETERMINED BY BITS 4:1. Reset Source: usb2_sync_preset_n

14.7.3.2.2.47 USB2SS_PHY2_AFE_TX_REG8 Register

14.7.3.2.2.47.1 USB2SS_PHY2_AFE_TX_REG8 Register (Offset = 20h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11786. Instance Table

Instance Name	Physical Address
USB0	0F90 8020h

Figure 14-5820. USB2SS_PHY2_AFE_TX_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG8							
R/W							
0h							

Table 14-11787. USB2SS_PHY2_AFE_TX_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG8	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.48 USB2SS_PHY2_AFE_TX_REG9 Register

14.7.3.2.2.48.1 USB2SS_PHY2_AFE_TX_REG9 Register (Offset = 24h) [reset = 0h]

Register AFE_TX_REG9

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Table 14-11788. Instance Table

Instance Name	Physical Address
USB0	0F90 8024h

Figure 14-5821. USB2SS_PHY2_AFE_TX_REG9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_ANA_REG9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11789. USB2SS_PHY2_AFE_TX_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG9	R/W	0h	Bits 7:4= 0000 Typical LSTx fall time = 450ns, 0001 Typical LSTx fall time = 225ns, 0010 Typical LSTx fall time =150ns, 0011 Typical LSTx fall time =225ns, 0100 Typical LSTx fall time =150ns, 0101 Typical LSTx fall time =150ns, 0110 Typical LSTx fall time =112ns, 0111 Typical LSTx fall time =150ns, 1000 Typical LSTx fall time =112ns, 1001 Typical LSTx fall time =112ns, 1010 Typical LSTx fall time =90ns, 1011 Typical LSTx fall time =112ns, 1100 Typical LSTx fall time =90ns, 1101 Typical LSTx fall time =90ns, 1110 Typical LSTx fall time =75ns, 1111 Typical LSTx fall time = 150ns. bit 3 = 0 LSTX FALL TIME IS DETERMINED BY DESIGN, 1 LSTX FALL TIME IS DETERMINED BY BITS 7:4. Bits 2:1= reserved. Reset Source: usb2_sync_preset_n

14.7.3.2.2.49 USB2SS_PHY2_AFE_TX_REG10 Register

14.7.3.2.2.49.1 USB2SS_PHY2_AFE_TX_REG10 Register (Offset = 28h) [reset = 0h]

FSTX fall time trimming

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Table 14-11790. Instance Table

Instance Name	Physical Address
USB0	0F90 8028h

Figure 14-5822. USB2SS_PHY2_AFE_TX_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG10							
R/W							
0h							

Table 14-11791. USB2SS_PHY2_AFE_TX_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG10	R/W	0h	Bits 7:5= reserved. Bits 4:1= 0000 Typical FSTx fall time = 16.6ns, 0001 Typical FSTx fall time =16.1ns, 0010 Typical FSTx fall time =15.6ns, 0011 Typical FSTx fall time =15.2ns, 0100 Typical FSTx fall time =14.7ns, 0101 Typical FSTx fall time =14.3ns, 0110 Typical FSTx fall time =13.9ns, 0111 Typical FSTx fall time =13.6ns, 1000 Typical FSTx fall time =13.2ns, 1001 Typical FSTx fall time =12.9ns, 1010 Typical FSTx fall time =12.6ns, 1011 Typical FSTx fall time =12.3ns, 1100 Typical FSTx fall time =12ns, 1101 Typical FSTx fall time =11.7, 1110 Typical FSTx fall time =11.5ns, 1111 Typical FSTx fall time =11.2ns. bit 0 = 0 Typical FSTx fall time set to default value of 12ns, 1 FSTX fall TIME IS DETERMINED BY BITS 4:1. Reset Source: usb2_sync_preset_n

14.7.3.2.2.50 USB2SS_PHY2_AFE_TX_REG11 Register

14.7.3.2.2.50.1 USB2SS_PHY2_AFE_TX_REG11 Register (Offset = 2Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11792. Instance Table

Instance Name	Physical Address
USB0	0F90 802Ch

Figure 14-5823. USB2SS_PHY2_AFE_TX_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG11							
R/W							
0h							

Table 14-11793. USB2SS_PHY2_AFE_TX_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG11	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.51 USB2SS_PHY2_AFE_TX_REG12 Register

14.7.3.2.2.51.1 USB2SS_PHY2_AFE_TX_REG12 Register (Offset = 30h) [reset = 0h]

Register AFE_TX_REG12

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Table 14-11794. Instance Table

Instance Name	Physical Address
USB0	0F90 8030h

Figure 14-5824. USB2SS_PHY2_AFE_TX_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG12	BF_6	BF_5	BF_4	BF_3	BF_2	BF_1_0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 14-11795. USB2SS_PHY2_AFE_TX_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TX_ANA_REG12	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	BF_6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BF_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BF_4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	BF_3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	BF_2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11795. USB2SS_PHY2_AFE_TX_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	BF_1_0	R/W	0h	00- SCALE2 set to 0, 01- SCALE2 set to 1, 10- SCALE2 set to 1, 11- SCALE2 set to 2 Reset Source: usb2_sync_preset_n

14.7.3.2.2.52 USB2SS_PHY2_AFE_RX_REG0 Register

14.7.3.2.2.52.1 USB2SS_PHY2_AFE_RX_REG0 Register (Offset = 34h) [reset = 0h]

Trim the squelch threshold

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Table 14-11796. Instance Table

Instance Name	Physical Address
USB0	0F90 8034h

Figure 14-5825. USB2SS_PHY2_AFE_RX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG0							
R/W							
0h							

Table 14-11797. USB2SS_PHY2_AFE_RX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG0	R/W	0h	Bits 7:6= reserved. Bits 5:0= 000000 keep squelch threshold at default value, 100000 increade squelch threshold by 5mv, 110000 increade squelch threshold by 10mv, 111000 increade squelch threshold by 15mv, 000001 reduce squelch threshold by 5mv, 000011 reduce squelch threshold by 10mv, 000111 reduce squelch threshold by 15mv. Reset Source: usb2_sync_preset_n

14.7.3.2.2.53 USB2SS_PHY2_AFE_RX_REG1 Register

14.7.3.2.2.53.1 USB2SS_PHY2_AFE_RX_REG1 Register (Offset = 38h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11798. Instance Table

Instance Name	Physical Address
USB0	0F90 8038h

Figure 14-5826. USB2SS_PHY2_AFE_RX_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RX_ANA_REG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11799. USB2SS_PHY2_AFE_RX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.54 USB2SS_PHY2_AFE_RX_REG2 Register

14.7.3.2.2.54.1 USB2SS_PHY2_AFE_RX_REG2 Register (Offset = 3Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11800. Instance Table

Instance Name	Physical Address
USB0	0F90 803Ch

Figure 14-5827. USB2SS_PHY2_AFE_RX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG2							
R/W							
0h							

Table 14-11801. USB2SS_PHY2_AFE_RX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG2	R/W	0h	reserved Reset Source: usb2_sync_preset_n

14.7.3.2.2.55 USB2SS_PHY2_AFE_RX_REG3 Register

14.7.3.2.2.55.1 USB2SS_PHY2_AFE_RX_REG3 Register (Offset = 40h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11802. Instance Table

Instance Name	Physical Address
USB0	0F90 8040h

Figure 14-5828. USB2SS_PHY2_AFE_RX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_ANA_REG3							
R/W							
0h							

Table 14-11803. USB2SS_PHY2_AFE_RX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.56 USB2SS_PHY2_AFE_RX_REG4 Register

14.7.3.2.2.56.1 USB2SS_PHY2_AFE_RX_REG4 Register (Offset = 44h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11804. Instance Table

Instance Name	Physical Address
USB0	0F90 8044h

Figure 14-5829. USB2SS_PHY2_AFE_RX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG4							
R/W							
0h							

Table 14-11805. USB2SS_PHY2_AFE_RX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.57 USB2SS_PHY2_AFE_RX_REG5 Register

14.7.3.2.2.57.1 USB2SS_PHY2_AFE_RX_REG5 Register (Offset = 48h) [reset = 0h]

Single ended receivers threshold trimming

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Table 14-11806. Instance Table

Instance Name	Physical Address
USB0	0F90 8048h

Figure 14-5830. USB2SS_PHY2_AFE_RX_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG5							
R/W							
0h							

Table 14-11807. USB2SS_PHY2_AFE_RX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG5	R/W	0h	Bits 7:3= reserved. Bits 2:1= 01 Switching thresholds for single ended receivers increased by 100mV, 10 Switching thresholds for single ended receivers reduced by 100mV. Bit 0= 0 Default Switching Thresholds for Single ended receivers, 1 SERx Switching Thresholds are controlled by bits [2:1]. Reset Source: usb2_sync_preset_n

14.7.3.2.2.58 USB2SS_PHY2_AFE_RX_REG6 Register

14.7.3.2.2.58.1 USB2SS_PHY2_AFE_RX_REG6 Register (Offset = 4Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11808. Instance Table

Instance Name	Physical Address
USB0	0F90 804Ch

Figure 14-5831. USB2SS_PHY2_AFE_RX_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG6							
R/W							
0h							

Table 14-11809. USB2SS_PHY2_AFE_RX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG6	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.59 USB2SS_PHY2_AFE_TX_REG13 Register

14.7.3.2.2.59.1 USB2SS_PHY2_AFE_TX_REG13 Register (Offset = 50h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11810. Instance Table

Instance Name	Physical Address
USB0	0F90 8050h

Figure 14-5832. USB2SS_PHY2_AFE_TX_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG13							
R							
0h							

Table 14-11811. USB2SS_PHY2_AFE_TX_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG13	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.60 USB2SS_PHY2_AFE_TX_REG14 Register

14.7.3.2.2.60.1 USB2SS_PHY2_AFE_TX_REG14 Register (Offset = 54h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11812. Instance Table

Instance Name	Physical Address
USB0	0F90 8054h

Figure 14-5833. USB2SS_PHY2_AFE_TX_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_ANA_REG14							
R							
0h							

Table 14-11813. USB2SS_PHY2_AFE_TX_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_ANA_REG14	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.61 USB2SS_PHY2_AFE_RX_REG7 Register

14.7.3.2.2.61.1 USB2SS_PHY2_AFE_RX_REG7 Register (Offset = 58h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-11814. Instance Table

Instance Name	Physical Address
USB0	0F90 8058h

Figure 14-5834. USB2SS_PHY2_AFE_RX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_ANA_REG7							
R							
0h							

Table 14-11815. USB2SS_PHY2_AFE_RX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG7	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.62 USB2SS_PHY2_AFE_RX_REG8 Register

14.7.3.2.2.62.1 USB2SS_PHY2_AFE_RX_REG8 Register (Offset = 5Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11816. Instance Table

Instance Name	Physical Address
USB0	0F90 805Ch

Figure 14-5835. USB2SS_PHY2_AFE_RX_REG8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RX_ANA_REG8</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11817. USB2SS_PHY2_AFE_RX_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_ANA_REG8	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.63 USB2SS_PHY2_AFE_UNUSED_REG0 Register

14.7.3.2.2.63.1 USB2SS_PHY2_AFE_UNUSED_REG0 Register (Offset = 60h) [reset = 0h]

AFE_UNUSED_REG0

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Table 14-11818. Instance Table

Instance Name	Physical Address
USB0	0F90 8060h

Figure 14-5836. USB2SS_PHY2_AFE_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_UNUSED_REG0							
R/W							
0h							

Table 14-11819. USB2SS_PHY2_AFE_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_UNUSED_REG0	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.64 USB2SS_PHY2_AFE_UNUSED_REG1 Register

14.7.3.2.2.64.1 USB2SS_PHY2_AFE_UNUSED_REG1 Register (Offset = 64h) [reset = 0h]

AFE_UNUSED_REG1

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Table 14-11820. Instance Table

Instance Name	Physical Address
USB0	0F90 8064h

Figure 14-5837. USB2SS_PHY2_AFE_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_UNUSED_REG1							
R/W							
0h							

Table 14-11821. USB2SS_PHY2_AFE_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_UNUSED_REG1	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.65 USB2SS_PHY2_AFE_BG_REG0 Register

14.7.3.2.2.65.1 USB2SS_PHY2_AFE_BG_REG0 Register (Offset = 80h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11822. Instance Table

Instance Name	Physical Address
USB0	0F90 8080h

Figure 14-5838. USB2SS_PHY2_AFE_BG_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG0							
R/W							
0h							

Table 14-11823. USB2SS_PHY2_AFE_BG_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.66 USB2SS_PHY2_AFE_BG_REG1 Register

14.7.3.2.2.66.1 USB2SS_PHY2_AFE_BG_REG1 Register (Offset = 84h) [reset = 0h]

BG bias current trimming

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Table 14-11824. Instance Table

Instance Name	Physical Address
USB0	0F90 8084h

Figure 14-5839. USB2SS_PHY2_AFE_BG_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BG_ANA_REG1							
R/W							
0h							

Table 14-11825. USB2SS_PHY2_AFE_BG_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG1	R/W	0h	Bits 7:6= 00- PLL charge pump bias current 5uA, 01- PLL charge pump bias current 4uA, 10- PLL charge pump bias current 6uA, 11- PLL charge pump bias current 5uA. Bits 5:4= 00- PLL DAC bias bias current bias current 5uA, 01- PLL DAC bias bias current bias current 4uA, 10- PLL DAC bias current current 6uA, 11- PLL DAC bias current current 5uA. Bits 3:2= 00- PLL DAC cascode bias current current 5uA, 01- PLL DAC cascode bias current current 4uA, 10- PLL DAC cascode bias current current 6uA, 11- PLL DAC cascode bias current current 5uA. Bits 1:0= 00- OTG block bias current 5uA, 01- OTG block bias current 6uA, 10- OTG block bias current 6uA, 11- OTG block bias current 5uA. Reset Source: usb2_sync_preset_n

14.7.3.2.2.67 USB2SS_PHY2_AFE_BG_REG2 Register

14.7.3.2.2.67.1 USB2SS_PHY2_AFE_BG_REG2 Register (Offset = 88h) [reset = 0h]

BG bias current trimming

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Table 14-11826. Instance Table

Instance Name	Physical Address
USB0	0F90 8088h

Figure 14-5840. USB2SS_PHY2_AFE_BG_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG2							
R/W							
0h							

Table 14-11827. USB2SS_PHY2_AFE_BG_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG2	R/W	0h	Bits 7:5= 000 High speed receiver bias 5uA, 100 High speed receiver bias 1uA, 001 High speed receiver bias 4uA, 010 High speed receiver bias 6uA, 101 High speed receiver bias 2uA. Bits 4:2= 000 Trasmission Envelope Detector bias current 5uA, 100 Trasmission Envelope Detector bias current 1uA, 001 Trasmission Envelope Detector bias current 4uA, 101 Trasmission Envelope Detector bias current 6uA, 101 Trasmission Envelope Detector bias current 2uA. Bits 1:0=00 PLL LDO bias current 5uA, 01 PLL LDO bias current 6uA, 10 PLL LDO bias current 4uA, 11 PLL LDO bias current 5uA Reset Source: usb2_sync_preset_n

14.7.3.2.2.68 USB2SS_PHY2_AFE_BG_REG3 Register

14.7.3.2.2.68.1 USB2SS_PHY2_AFE_BG_REG3 Register (Offset = 8Ch) [reset = 2h]

Register AFE_BG_REG3

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Table 14-11828. Instance Table

Instance Name	Physical Address
USB0	0F90 808Ch

Figure 14-5841. USB2SS_PHY2_AFE_BG_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_ANA_REG3							
R/W							
2h							

Table 14-11829. USB2SS_PHY2_AFE_BG_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG3	R/W	2h	Bits 7:6= reserved, Bits 5:4= 00 [Default] BG_OK_CORE Generated Internally, 01 BG_OK_CORE Generated Internally, 10 Force BG_OK_CORE =0, 11 Force BG_OK_CORE =1. Bits 3:0=0000 Invalid state, 0001 Higher start sense voltage, weaker start-up pull down, 0010 Default start sense voltage, 0100 Low start sense voltage, strong start-up pull down, 1000 Lowest start sense voltage, strongest start-up pull down. Reset Source: usb2_sync_preset_n

14.7.3.2.2.69 USB2SS_PHY2_AFE_CALIB_REG0 Register

14.7.3.2.2.69.1 USB2SS_PHY2_AFE_CALIB_REG0 Register (Offset = 90h) [reset = 0h]

Calibration resistance trimming

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Table 14-11830. Instance Table

Instance Name	Physical Address
USB0	0F90 8090h

Figure 14-5842. USB2SS_PHY2_AFE_CALIB_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_ANA_REG0							
R/W							
0h							

Table 14-11831. USB2SS_PHY2_AFE_CALIB_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CALIB_ANA_REG0	R/W	0h	Bits 5:0= 000000 Calibrate termination resistor to default value, 000001 Calibrate termination resistor by -%5 to default value, 000011 Calibrate termination resistor by -%10 to default value, 000111 Calibrate termination resistor by - %15 to default value, 001000 Calibrate termination resistor by +5% to default value, 011000 Calibrate termination resistor by +10% to default value, 111000 Calibrate termination resistor by +15% to default value. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.7.3.2.2.70 USB2SS_PHY2_AFE_BC_REG0 Register

14.7.3.2.2.70.1 USB2SS_PHY2_AFE_BC_REG0 Register (Offset = 94h) [reset = 0h]

register AFE_BC_REG0

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Table 14-11832. Instance Table

Instance Name	Physical Address
USB0	0F90 8094h

Figure 14-5843. USB2SS_PHY2_AFE_BC_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BC_ANA_REG0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11833. USB2SS_PHY2_AFE_BC_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved

Table 14-11833. USB2SS_PHY2_AFE_BC_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	BC_ANA_REG0	R/W	0h	Bit 0= 0 Battery_charging_DAC_RES_CALIB CODE CANNOT BE CONTROLLED BY ANALOG TEST BITS, 1 Battery_charging_DAC_RES_CALIB CODE CAN BE CONTROLLED BY ANALOG TEST BITS. Bits 5:1= 00000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 0, 00001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 1, 00010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 2, 00011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 3, 00100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 4, 00101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 5, 00110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 6, 00111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 7, 01000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 8, 01001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 9, 01010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 10, 01011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 11, 01100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 12, 01101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 13, 01110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 14, 01111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 15, 10000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 16, 10001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 17, 10010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 18, 10011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 19, 10100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 20, 10101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 21, 10110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 22, 10111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 23, 11000 Battery_charging_DAC_RES_CALIB CODE FORCED TO 24, 11001 Battery_charging_DAC_RES_CALIB CODE FORCED TO 24, 11010 Battery_charging_DAC_RES_CALIB CODE FORCED TO 26, 11011 Battery_charging_DAC_RES_CALIB CODE FORCED TO 27, 11100 Battery_charging_DAC_RES_CALIB CODE FORCED TO 28, 11101 Battery_charging_DAC_RES_CALIB CODE FORCED TO 29, 11110 Battery_charging_DAC_RES_CALIB CODE FORCED TO 30, 11111 Battery_charging_DAC_RES_CALIB CODE FORCED TO 31. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.7.3.2.2.71 USB2SS_PHY2_AFE_BC_REG1 Register

14.7.3.2.2.71.1 USB2SS_PHY2_AFE_BC_REG1 Register (Offset = 98h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11834. Instance Table

Instance Name	Physical Address
USB0	0F90 8098h

Figure 14-5844. USB2SS_PHY2_AFE_BC_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BC_ANA_REG1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11835. USB2SS_PHY2_AFE_BC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.72 USB2SS_PHY2_AFE_BC_REG2 Register

14.7.3.2.2.72.1 USB2SS_PHY2_AFE_BC_REG2 Register (Offset = 9Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11836. Instance Table

Instance Name	Physical Address
USB0	0F90 809Ch

Figure 14-5845. USB2SS_PHY2_AFE_BC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG2							
R/W							
0h							

Table 14-11837. USB2SS_PHY2_AFE_BC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.73 USB2SS_PHY2_AFE_BC_REG3 Register

14.7.3.2.2.73.1 USB2SS_PHY2_AFE_BC_REG3 Register (Offset = A0h) [reset = 0h]

Register AFE_BC_REG3

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Table 14-11838. Instance Table

Instance Name	Physical Address
USB0	0F90 80A0h

Figure 14-5846. USB2SS_PHY2_AFE_BC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BC_ANA_REG3							
R/W							
0h							

Table 14-11839. USB2SS_PHY2_AFE_BC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG3	R/W	0h	Bit 0= 0 Do not overdrive SESS_VLD comparator enable signal, 1 Overdrive SESS_VLD comparator enable signal. Bit 1= 0 SESS_VLD comparator disabled, 1 SESS_VLD comparator enabled. Bit 2= 0 Do not overdrive VBUS_VLD comparator enable signal, 1 Overdrive VBUS_VLD comparator enable signal. Bit 3= 0 VBUS_VLD comparator disabled, 1 VBUS_VLD comparator enabled. Bit 4= 0 Do not overdrive ID comparator enable signal, 1 Overdrive ID comparator enable signal. Bit 5= 0 ID comparator disabled, 1 ID comparator enabled. Bits 7:6= reserved. Reset Source: usb2_sync_preset_n

14.7.3.2.2.74 USB2SS_PHY2_AFE_BC_REG4 Register

14.7.3.2.2.74.1 USB2SS_PHY2_AFE_BC_REG4 Register (Offset = A4h) [reset = 0h]

Register AFE_BC_REG4

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Table 14-11840. Instance Table

Instance Name	Physical Address
USB0	0F90 80A4h

Figure 14-5847. USB2SS_PHY2_AFE_BC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG4							
R/W							
0h							

Table 14-11841. USB2SS_PHY2_AFE_BC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG4	R/W	0h	Bits 2:0= reserved. Bit 3= 0- VBUS_VLD comparator output low, 1- VBUS_VLD comparator output high. Bit 4= 0- Do not overdrive VBUS_VLD comparator output, 1- Overdrive VBUS_VLD comparator output. Bit 5= 0- SESS_VLD comparator output low, 1- SESS_VLD comparator output high. Bit 6= 0- Do not overdrive SESS_VLD comparator output, 1- Overdrive SESS_VLD comparator output. Bit 7= 0- ID comparator output low, 1- ID comparator output high. Reset Source: usb2_sync_preset_n

14.7.3.2.2.75 USB2SS_PHY2_AFE_BC_REG5 Register

14.7.3.2.2.75.1 USB2SS_PHY2_AFE_BC_REG5 Register (Offset = A8h) [reset = 0h]

Register AFE_BC_REG5

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Table 14-11842. Instance Table

Instance Name	Physical Address
USB0	0F90 80A8h

Figure 14-5848. USB2SS_PHY2_AFE_BC_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG5							
R/W							
0h							

Table 14-11843. USB2SS_PHY2_AFE_BC_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG5	R/W	0h	Bit 0= 0- Do not overdrive ID comparator output, 1- Overdrive ID comparator output. Bit 1= 0 Do not overdrive VBUS_DIV signal, 1- Overdrive VBUS_DIV signal. Bit 2= 0- VBUS_DIV signal low, 1- VBUS_DIV signal high. Bits 7:3= reserved. Reset Source: usb2_sync_preset_n

14.7.3.2.2.76 USB2SS_PHY2_AFE_BC_REG6 Register

14.7.3.2.2.76.1 USB2SS_PHY2_AFE_BC_REG6 Register (Offset = ACh) [reset = 0h]

Register AFE_BC_REG6

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Table 14-11844. Instance Table

Instance Name	Physical Address
USB0	0F90 80ACh

Figure 14-5849. USB2SS_PHY2_AFE_BC_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG6							
R/W							
0h							

Table 14-11845. USB2SS_PHY2_AFE_BC_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG6	R/W	0h	register AFE_BC_REG6 Reset Source: usb2_sync_preset_n

14.7.3.2.2.77 USB2SS_PHY2_AFE_PLL_REG0 Register

14.7.3.2.2.77.1 USB2SS_PHY2_AFE_PLL_REG0 Register (Offset = B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11846. Instance Table

Instance Name	Physical Address
USB0	0F90 80B0h

Figure 14-5850. USB2SS_PHY2_AFE_PLL_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG0							
R/W							
0h							

Table 14-11847. USB2SS_PHY2_AFE_PLL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.78 USB2SS_PHY2_AFE_PLL_REG1 Register

14.7.3.2.2.78.1 USB2SS_PHY2_AFE_PLL_REG1 Register (Offset = B4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11848. Instance Table

Instance Name	Physical Address
USB0	0F90 80B4h

Figure 14-5851. USB2SS_PHY2_AFE_PLL_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG1							
R/W							
0h							

Table 14-11849. USB2SS_PHY2_AFE_PLL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.79 USB2SS_PHY2_AFE_PLL_REG2 Register

14.7.3.2.2.79.1 USB2SS_PHY2_AFE_PLL_REG2 Register (Offset = B8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11850. Instance Table

Instance Name	Physical Address
USB0	0F90 80B8h

Figure 14-5852. USB2SS_PHY2_AFE_PLL_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG2							
R/W							
0h							

Table 14-11851. USB2SS_PHY2_AFE_PLL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.80 USB2SS_PHY2_AFE_PLL_REG3 Register

14.7.3.2.2.80.1 USB2SS_PHY2_AFE_PLL_REG3 Register (Offset = BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11852. Instance Table

Instance Name	Physical Address
USB0	0F90 80BCh

Figure 14-5853. USB2SS_PHY2_AFE_PLL_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG3							
R/W							
0h							

Table 14-11853. USB2SS_PHY2_AFE_PLL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG3	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.81 USB2SS_PHY2_AFE_PLL_REG4 Register

14.7.3.2.2.81.1 USB2SS_PHY2_AFE_PLL_REG4 Register (Offset = C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11854. Instance Table

Instance Name	Physical Address
USB0	0F90 80C0h

Figure 14-5854. USB2SS_PHY2_AFE_PLL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG4							
R/W							
0h							

Table 14-11855. USB2SS_PHY2_AFE_PLL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG4	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.82 USB2SS_PHY2_AFE_PLL_REG5 Register

14.7.3.2.2.82.1 USB2SS_PHY2_AFE_PLL_REG5 Register (Offset = C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11856. Instance Table

Instance Name	Physical Address
USB0	0F90 80C4h

Figure 14-5855. USB2SS_PHY2_AFE_PLL_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AFE_PLL_REG5							
R/W							
0h							

Table 14-11857. USB2SS_PHY2_AFE_PLL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	AFE_PLL_REG5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.83 USB2SS_PHY2_AFE_BG_REG4 Register

14.7.3.2.2.83.1 USB2SS_PHY2_AFE_BG_REG4 Register (Offset = C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11858. Instance Table

Instance Name	Physical Address
USB0	0F90 80C8h

Figure 14-5856. USB2SS_PHY2_AFE_BG_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BG_ANA_REG4							
R							
0h							

Table 14-11859. USB2SS_PHY2_AFE_BG_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BG_ANA_REG4	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.84 USB2SS_PHY2_AFE_CALIB_REG1 Register

14.7.3.2.2.84.1 USB2SS_PHY2_AFE_CALIB_REG1 Register (Offset = CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11860. Instance Table

Instance Name	Physical Address
USB0	0F90 80CCh

Figure 14-5857. USB2SS_PHY2_AFE_CALIB_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CALIB_ANA_REG1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11861. USB2SS_PHY2_AFE_CALIB_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CALIB_ANA_REG1	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.85 USB2SS_PHY2_AFE_BC_REG7 Register

14.7.3.2.2.85.1 USB2SS_PHY2_AFE_BC_REG7 Register (Offset = D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11862. Instance Table

Instance Name	Physical Address
USB0	0F90 80D0h

Figure 14-5858. USB2SS_PHY2_AFE_BC_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_ANA_REG7							
R							
0h							

Table 14-11863. USB2SS_PHY2_AFE_BC_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BC_ANA_REG7	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.86 USB2SS_PHY2_AFE_PLL_REG6 Register

14.7.3.2.2.86.1 USB2SS_PHY2_AFE_PLL_REG6 Register (Offset = D4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11864. Instance Table

Instance Name	Physical Address
USB0	0F90 80D4h

Figure 14-5859. USB2SS_PHY2_AFE_PLL_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_ANA_REG6							
R							
0h							

Table 14-11865. USB2SS_PHY2_AFE_PLL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PLL_ANA_REG6	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.87 USB2SS_PHY2_AFE_UNUSED_REG2 Register

14.7.3.2.2.87.1 USB2SS_PHY2_AFE_UNUSED_REG2 Register (Offset = D8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11866. Instance Table

Instance Name	Physical Address
USB0	0F90 80D8h

Figure 14-5860. USB2SS_PHY2_AFE_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-11867. USB2SS_PHY2_AFE_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.88 USB2SS_PHY2_AFE_UNUSED_REG3 Register

14.7.3.2.2.88.1 USB2SS_PHY2_AFE_UNUSED_REG3 Register (Offset = DCh) [reset = 0h]

AFE_UNUSED_REG3

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Table 14-11868. Instance Table

Instance Name	Physical Address
USB0	0F90 80DCh

Figure 14-5861. USB2SS_PHY2_AFE_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-11869. USB2SS_PHY2_AFE_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.89 USB2SS_PHY2_PLL_REG0 Register

14.7.3.2.2.89.1 USB2SS_PHY2_PLL_REG0 Register (Offset = 100h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11870. Instance Table

Instance Name	Physical Address
USB0	0F90 8100h

Figure 14-5862. USB2SS_PHY2_PLL_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INITIAL_WAIT_TIME							
R/W							
0h							

Table 14-11871. USB2SS_PHY2_PLL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INITIAL_WAIT_TIME	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.90 USB2SS_PHY2_PLL_REG1 Register

14.7.3.2.2.90.1 USB2SS_PHY2_PLL_REG1 Register (Offset = 104h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11872. Instance Table

Instance Name	Physical Address
USB0	0F90 8104h

Figure 14-5863. USB2SS_PHY2_PLL_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RST_FDBK_DIV_DELAY_VALUE					RST_FDBK_DIV_DELAY_EN	FBDIV_EN	INITIAL_WAIT_TIME_EN
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-11873. USB2SS_PHY2_PLL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	RST_FDBK_DIV_DELAY_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RST_FDBK_DIV_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	FBDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	INITIAL_WAIT_TIME_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.91 USB2SS_PHY2_PLL_REG2 Register

14.7.3.2.2.91.1 USB2SS_PHY2_PLL_REG2 Register (Offset = 108h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11874. Instance Table

Instance Name	Physical Address
USB0	0F90 8108h

Figure 14-5864. USB2SS_PHY2_PLL_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	VCO_SETTLING_TIME_EN	VCO_SETTLING_TIME					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-11875. USB2SS_PHY2_PLL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6	VCO_SETTLING_TIME_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	VCO_SETTLING_TIME	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.92 USB2SS_PHY2_PLL_REG3 Register

14.7.3.2.2.92.1 USB2SS_PHY2_PLL_REG3 Register (Offset = 10Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11876. Instance Table

Instance Name	Physical Address
USB0	0F90 810Ch

Figure 14-5865. USB2SS_PHY2_PLL_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FBDIV_VALUE							
R/W							
0h							

Table 14-11877. USB2SS_PHY2_PLL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FBDIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.93 USB2SS_PHY2_PLL_REG4 Register

14.7.3.2.2.93.1 USB2SS_PHY2_PLL_REG4 Register (Offset = 110h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11878. Instance Table

Instance Name	Physical Address
USB0	0F90 8110h

Figure 14-5866. USB2SS_PHY2_PLL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED	PLL_LOCK_TIME_15	PD_PFD_VALUE	PD_PFD_EN	PLL_LOCK_EN	PLL_LOCK_VALUE	COARSEDONE_EN	COARSEDONE_VALUE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11879. USB2SS_PHY2_PLL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
6	PLL_LOCK_TIME_15	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PD_PFD_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PD_PFD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_LOCK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	PLL_LOCK_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	COARSEDONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11879. USB2SS_PHY2_PLL_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COARSEDONE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.94 USB2SS_PHY2_PLL_REG5 Register

14.7.3.2.2.94.1 USB2SS_PHY2_PLL_REG5 Register (Offset = 114h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11880. Instance Table

Instance Name	Physical Address
USB0	0F90 8114h

Figure 14-5867. USB2SS_PHY2_PLL_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
STARTLOOP_EN_4_0	STARTLOOP_EN_5	STARTLOOP_5	STARTLOOP_4_0				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 14-11881. USB2SS_PHY2_PLL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	STARTLOOP_EN_4_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	STARTLOOP_EN_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	STARTLOOP_5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	STARTLOOP_4_0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.95 USB2SS_PHY2_PLL_REG6 Register

14.7.3.2.2.95.1 USB2SS_PHY2_PLL_REG6 Register (Offset = 118h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11882. Instance Table

Instance Name	Physical Address
USB0	0F90 8118h

Figure 14-5868. USB2SS_PHY2_PLL_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	COARSE_CODE_SEL	LSB_ERROR_0P5	BIG_JUMP_EN	VCO_CNT_WINDOW_VALUE	VCO_CNT_WINDOW_EN	RST_FDBK_DIV_VALUE	RST_FDBK_DIV_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11883. USB2SS_PHY2_PLL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	COARSE_CODE_SEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	LSB_ERROR_0P5	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIG_JUMP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VCO_CNT_WINDOW_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	VCO_CNT_WINDOW_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RST_FDBK_DIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11883. USB2SS_PHY2_PLL_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RST_FDBK_DIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.96 USB2SS_PHY2_PLL_REG7 Register

14.7.3.2.2.96.1 USB2SS_PHY2_PLL_REG7 Register (Offset = 11Ch) [reset = 0h]

refclock selection

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Table 14-11884. Instance Table

Instance Name	Physical Address
USB0	0F90 811Ch

Figure 14-5869. USB2SS_PHY2_PLL_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			REFCLK_SEL				REFCLK_SEL_EN
R/W			R/W				R/W
0h			0h				0h

Table 14-11885. USB2SS_PHY2_PLL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
4:1	REFCLK_SEL	R/W	0h	0000 Refclock selection for 9.6 MHz, 0001 Refclock selection for 10 MHz, 0010 Refclock selection for 12 MHz, 0011 Refclock selection for 19.2 MHz, 0100 Refclock selection for 20 MHz, 0101 Refclock selection for 24 MHz, 0110 Refclock selection for 25 MHz, 0111 Refclock selection for 26 MHz, 1000 Refclock selection for 38.4 MHz, 1001 Refclock selection for 40 MHz, 1010 Refclock selection for 48 MHz, 1011 Refclock selection for 50 MHz, 1100 Refclock selection for 52 MHz, 1101 Refclock selection for 9.6 MHz, 1110 Refclock selection for 9.6 MHz, 1111 Refclock selection for 9.6 MHz. Reset Source: usb2_sync_preset_n
0	REFCLK_SEL_EN	R/W	0h	0 PLLREFSEL Value not taken from PLL_REG7[4:1], 1 PLLREFSEL Value taken from PLL_REG7[4:1]. Reset Source: usb2_sync_preset_n

14.7.3.2.2.97 USB2SS_PHY2_PLL_REG8 Register

14.7.3.2.2.97.1 USB2SS_PHY2_PLL_REG8 Register (Offset = 120h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11886. Instance Table

Instance Name	Physical Address
USB0	0F90 8120h

Figure 14-5870. USB2SS_PHY2_PLL_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COARSE_CODE							
R/W							
0h							

Table 14-11887. USB2SS_PHY2_PLL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COARSE_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.98 USB2SS_PHY2_PLL_REG9 Register

14.7.3.2.2.98.1 USB2SS_PHY2_PLL_REG9 Register (Offset = 124h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11888. Instance Table

Instance Name	Physical Address
USB0	0F90 8124h

Figure 14-5871. USB2SS_PHY2_PLL_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COARSE_CODE	V2I_CODE_EN	V2I_CODE					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-11889. USB2SS_PHY2_PLL_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	COARSE_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	V2I_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	V2I_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.99 USB2SS_PHY2_PLL_REG10 Register

14.7.3.2.2.99.1 USB2SS_PHY2_PLL_REG10 Register (Offset = 128h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11890. Instance Table

Instance Name	Physical Address
USB0	0F90 8128h

Figure 14-5872. USB2SS_PHY2_PLL_REG10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>UNUSED</td><td colspan="5">IPDIV_VALUE</td><td>IPDIV_EN</td><td>COARSE_CODE_EN</td></tr>
<tr><td>R/W</td><td colspan="5">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="5">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11891. USB2SS_PHY2_PLL_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6:2	IPDIV_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	IPDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	COARSE_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.100 USB2SS_PHY2_PLL_REG11 Register

14.7.3.2.2.100.1 USB2SS_PHY2_PLL_REG11 Register (Offset = 12Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11892. Instance Table

Instance Name	Physical Address
USB0	0F90 812Ch

Figure 14-5873. USB2SS_PHY2_PLL_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_STANDBY	PLL_STANDBY_EN	PLL_PD	PLL_PD_EN	PLL_PSO_DEL	PLL_PSO_DEL_EN	PLL_PSO	PLL_PSO_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11893. USB2SS_PHY2_PLL_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_STANDBY	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	PLL_STANDBY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PLL_PD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_PD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_PSO_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	PLL_PSO_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11893. USB2SS_PHY2_PLL_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PLL_PSO	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_PSO_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.101 USB2SS_PHY2_PLL_REG12 Register

14.7.3.2.2.101.1 USB2SS_PHY2_PLL_REG12 Register (Offset = 130h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11894. Instance Table

Instance Name	Physical Address
USB0	0F90 8130h

Figure 14-5874. USB2SS_PHY2_PLL_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED		PLL_LDO_REF_EN	PLL_LDO_REF_EN_EN	PLL_LDO_CORE_EN	PLL_LDO_CORE_EN_EN	PLL_PD_ANA	PLL_PD_ANA_EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-11895. USB2SS_PHY2_PLL_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
5	PLL_LDO_REF_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_LDO_REF_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_LDO_CORE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	PLL_LDO_CORE_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	PLL_PD_ANA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11895. USB2SS_PHY2_PLL_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL_PD_ANA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.102 USB2SS_PHY2_PLL_REG13 Register

14.7.3.2.2.102.1 USB2SS_PHY2_PLL_REG13 Register (Offset = 134h) [reset = 0h]

PLL clockon test mode

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Table 14-11896. Instance Table

Instance Name	Physical Address
USB0	0F90 8134h

Figure 14-5875. USB2SS_PHY2_PLL_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_CLKON	PLL_LDO_REF_CORE						PLL_LDO_REF_CORE_EN
R/W	R/W						R/W
0h	0h						0h

Table 14-11897. USB2SS_PHY2_PLL_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_CLKON	R/W	0h	0 pll clock is not always running, 1 pll clock is always running. Reset Source: usb2_sync_preset_n
6:1	PLL_LDO_REF_CORE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_LDO_REF_CORE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.103 USB2SS_PHY2_PLL_REG14 Register

14.7.3.2.2.103.1 USB2SS_PHY2_PLL_REG14 Register (Offset = 138h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11898. Instance Table

Instance Name	Physical Address
USB0	0F90 8138h

Figure 14-5876. USB2SS_PHY2_PLL_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_LDO_CNT_THRESHOLD			PLL_LDO_CNT_THRESHOLD_EN	PLL_LDO_ISO_CNT_THRESHOLD			PLL_LDO_ISO_CNT_THRESHOLD_EN
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 14-11899. USB2SS_PHY2_PLL_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	PLL_LDO_CNT_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_LDO_CNT_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	PLL_LDO_ISO_CNT_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PLL_LDO_ISO_CNT_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.104 USB2SS_PHY2_PLL_UNUSED_REG0 Register

14.7.3.2.2.104.1 USB2SS_PHY2_PLL_UNUSED_REG0 Register (Offset = 13Ch) [reset = 0h]

unused

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Table 14-11900. Instance Table

Instance Name	Physical Address
USB0	0F90 813Ch

Figure 14-5877. USB2SS_PHY2_PLL_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-11901. USB2SS_PHY2_PLL_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.105 USB2SS_PHY2_PLL_UNUSED_REG1 Register

14.7.3.2.2.105.1 USB2SS_PHY2_PLL_UNUSED_REG1 Register (Offset = 140h) [reset = 0h]

unused

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Table 14-11902. Instance Table

Instance Name	Physical Address
USB0	0F90 8140h

Figure 14-5878. USB2SS_PHY2_PLL_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-11903. USB2SS_PHY2_PLL_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.106 USB2SS_PHY2_PLL_REG15 Register

14.7.3.2.2.106.1 USB2SS_PHY2_PLL_REG15 Register (Offset = 144h) [reset = 0h]

Coarse_code values

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Table 14-11904. Instance Table

Instance Name	Physical Address
USB0	0F90 8144h

Figure 14-5879. USB2SS_PHY2_PLL_REG15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_LOCK	COARSEDONE	VCO_CNT_WIN	RST_FDBK_DIV	UNUSED	PD_PFD	STARTLOOP	COARSE_CODE_8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11905. USB2SS_PHY2_PLL_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_LOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	COARSEDONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	VCO_CNT_WIN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RST_FDBK_DIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
2	PD_PFD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	STARTLOOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11905. USB2SS_PHY2_PLL_REG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COARSE_CODE_8	R	0h	0 MSB of coarse_code for PLL VCO. Reset Source: usb2_sync_preset_n

14.7.3.2.2.107 USB2SS_PHY2_PLL_REG16 Register

14.7.3.2.2.107.1 USB2SS_PHY2_PLL_REG16 Register (Offset = 148h) [reset = 0h]

Coarse_code values

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Table 14-11906. Instance Table

Instance Name	Physical Address
USB0	0F90 8148h

Figure 14-5880. USB2SS_PHY2_PLL_REG16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COARSE_CODE							
R							
0h							

Table 14-11907. USB2SS_PHY2_PLL_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COARSE_CODE	R	0h	01011010 8 LSBs of coarse code for PLL VCO Reset Source: usb2_sync_preset_n

14.7.3.2.2.108 USB2SS_PHY2_PLL_UNUSED_REG2 Register

14.7.3.2.2.108.1 USB2SS_PHY2_PLL_UNUSED_REG2 Register (Offset = 14Ch) [reset = 0h]

unused

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Table 14-11908. Instance Table

Instance Name	Physical Address
USB0	0F90 814Ch

Figure 14-5881. USB2SS_PHY2_PLL_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-11909. USB2SS_PHY2_PLL_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.109 USB2SS_PHY2_CALIB_REG0 Register

14.7.3.2.2.109.1 USB2SS_PHY2_CALIB_REG0 Register (Offset = 180h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11910. Instance Table

Instance Name	Physical Address
USB0	0F90 8180h

Figure 14-5882. USB2SS_PHY2_CALIB_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CLK	CALIB_CLK_EN	COMP_OUT	INIT_WAIT_OVR				INIT_WAIT_OVR_EN
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 14-11911. USB2SS_PHY2_CALIB_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_CLK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CALIB_CLK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	COMP_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	INIT_WAIT_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	INIT_WAIT_OVR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.110 USB2SS_PHY2_CALIB_REG1 Register

14.7.3.2.2.110.1 USB2SS_PHY2_CALIB_REG1 Register (Offset = 184h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11912. Instance Table

Instance Name	Physical Address
USB0	0F90 8184h

Figure 14-5883. USB2SS_PHY2_CALIB_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	CALIB_CODE						CALIB_CODE_EN
R/W	R/W						R/W
0h	0h						0h

Table 14-11913. USB2SS_PHY2_CALIB_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6:1	CALIB_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_CODE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.111 USB2SS_PHY2_BC_REG0 Register

14.7.3.2.2.111.1 USB2SS_PHY2_BC_REG0 Register (Offset = 188h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11914. Instance Table

Instance Name	Physical Address
USB0	0F90 8188h

Figure 14-5884. USB2SS_PHY2_BC_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED				ADP_EN	ADP_EN_EN	ID_PULLUP	ID_PULLUP_EN
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 14-11915. USB2SS_PHY2_BC_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
3	ADP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	ADP_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ID_PULLUP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ID_PULLUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.112 USB2SS_PHY2_BC_REG1 Register

14.7.3.2.2.112.1 USB2SS_PHY2_BC_REG1 Register (Offset = 18Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11916. Instance Table

Instance Name	Physical Address
USB0	0F90 818Ch

Figure 14-5885. USB2SS_PHY2_BC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ADP_SOURCE_I_EN	ADP_SOURCE_I_EN_CTRL	ADP_SINK_I_EN	ADP_SINK_I_EN_CTRL	ADP_SENSE_EN	ADP_SENSE_EN_CTRL	ADP_PROBE_EN	ADP_PROBE_EN_CTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11917. USB2SS_PHY2_BC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	ADP_SOURCE_I_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ADP_SOURCE_I_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	ADP_SINK_I_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	ADP_SINK_I_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	ADP_SENSE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	ADP_SENSE_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11917. USB2SS_PHY2_BC_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ADP_PROBE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ADP_PROBE_EN_CTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.113 USB2SS_PHY2_BC_REG2 Register

14.7.3.2.2.113.1 USB2SS_PHY2_BC_REG2 Register (Offset = 190h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11918. Instance Table

Instance Name	Physical Address
USB0	0F90 8190h

Figure 14-5886. USB2SS_PHY2_BC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IDM_SINK_EN_VALUE	IDM_SINK_EN_CNTRL	IDP_SINK_EN_VALUE	IDP_SINK_EN_CNTRL	IDP_SRC_EN_VALUE	IDP_SRC_EN_CNTRL	BC_EN_VALUE	BC_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11919. USB2SS_PHY2_BC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	IDM_SINK_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	IDM_SINK_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	IDP_SINK_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	IDP_SINK_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	IDP_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	IDP_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11919. USB2SS_PHY2_BC_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	BC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.114 USB2SS_PHY2_BC_REG3 Register

14.7.3.2.2.114.1 USB2SS_PHY2_BC_REG3 Register (Offset = 194h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11920. Instance Table

Instance Name	Physical Address
USB0	0F90 8194h

Figure 14-5887. USB2SS_PHY2_BC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DM_VDAT_REF_COMP_EN_VALUE	DM_VDAT_REF_COMP_EN_CNTRL	DP_VDAT_REF_COMP_EN_VALUE	DP_VDAT_REF_COMP_EN_CNTRL	VDP_SRC_EN_VALUE	VDP_SRC_EN_CNTRL	VDM_SRC_EN_VALUE	VDM_SRC_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11921. USB2SS_PHY2_BC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DM_VDAT_REF_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DM_VDAT_REF_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DP_VDAT_REF_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DP_VDAT_REF_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VDP_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	VDP_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11921. USB2SS_PHY2_BC_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VDM_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	VDM_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.115 USB2SS_PHY2_BC_REG4 Register

14.7.3.2.2.115.1 USB2SS_PHY2_BC_REG4 Register (Offset = 198h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11922. Instance Table

Instance Name	Physical Address
USB0	0F90 8198h

Figure 14-5888. USB2SS_PHY2_BC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_A_REF_EN_VALUE	RID_A_REF_EN_CNTRL	RID_FLOAT_REF_EN_VALUE	RID_FLOAT_REF_EN_CNTRL	RID_NONFLOAT_COMP_EN_VALUE	RID_NONFLOAT_COMP_EN_CNTRL	RID_FLOAT_COMP_EN_VALUE	RID_FLOAT_COMP_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11923. USB2SS_PHY2_BC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_A_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_A_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_FLOAT_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_FLOAT_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_NONFLOAT_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RID_NONFLOAT_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11923. USB2SS_PHY2_BC_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RID_FLOAT_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RID_FLOAT_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.116 USB2SS_PHY2_BC_REG5 Register

14.7.3.2.2.116.1 USB2SS_PHY2_BC_REG5 Register (Offset = 19Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11924. Instance Table

Instance Name	Physical Address
USB0	0F90 819Ch

Figure 14-5889. USB2SS_PHY2_BC_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_B_C_COMP_EN_VALUE	RID_B_C_COMP_EN_CNTRL	RID_A_COMP_EN_VALUE	RID_A_COMP_EN_CNTRL	RID_C_REF_EN_VALUE	RID_C_REF_EN_CNTRL	RID_B_REF_EN_VALUE	RID_B_REF_EN_CNTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11925. USB2SS_PHY2_BC_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_B_C_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_B_C_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_A_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_A_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_C_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RID_C_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11925. USB2SS_PHY2_BC_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RID_B_REF_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RID_B_REF_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.117 USB2SS_PHY2_BC_REG6 Register

14.7.3.2.2.117.1 USB2SS_PHY2_BC_REG6 Register (Offset = 1A0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11926. Instance Table

Instance Name	Physical Address
USB0	0F90 81A0h

Figure 14-5890. USB2SS_PHY2_BC_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BC_DELAY_VALUE					BC_DELAY_EN	DM_VLGC_COMP_EN_VALUE	DM_VLGC_COMP_EN_CNTRL
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-11927. USB2SS_PHY2_BC_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	BC_DELAY_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	BC_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DM_VLGC_COMP_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DM_VLGC_COMP_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.118 USB2SS_PHY2_BC_REG7 Register

14.7.3.2.2.118.1 USB2SS_PHY2_BC_REG7 Register (Offset = 1A4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11928. Instance Table

Instance Name	Physical Address
USB0	0F90 81A4h

Figure 14-5891. USB2SS_PHY2_BC_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_NONFLOAT_SRC_EN_VALUE	RID_NONFLOAT_SRC_EN_CNTRL	RID_FLOAT_SRC_EN_VALUE	RID_FLOAT_SRC_EN_CNTRL	RESET_CNTRL	DM_CURRENT_SRC_EN_VALUE	DM_CURRENT_SRC_EN_CNTRL	UNUSED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11929. USB2SS_PHY2_BC_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_NONFLOAT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_NONFLOAT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_FLOAT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_FLOAT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RESET_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DM_CURRENT_SRC_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11929. USB2SS_PHY2_BC_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DM_CURRENT_SRC_EN_CNTRL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.119 USB2SS_PHY2_TED_REG0 Register

14.7.3.2.2.119.1 USB2SS_PHY2_TED_REG0 Register (Offset = 1A8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11930. Instance Table

Instance Name	Physical Address
USB0	0F90 81A8h

Figure 14-5892. USB2SS_PHY2_TED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALIB_CODE_UP_EN	DELAY_VALUE		DELAY_EN	CALIB_DONE	CALIIB_DONE_EN	COMP_OUT_DOWN_INV	COMP_OUT_UP_INV
R/W	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h

Table 14-11931. USB2SS_PHY2_TED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_CODE_UP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:5	DELAY_VALUE	R/W	0h	Delay is 8us Reset Source: usb2_sync_preset_n
4	DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CALIB_DONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIIB_DONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	COMP_OUT_DOWN_INV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11931. USB2SS_PHY2_TED_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COMP_OUT_UP_INV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.120 USB2SS_PHY2_TED_REG1 Register

14.7.3.2.2.120.1 USB2SS_PHY2_TED_REG1 Register (Offset = 1ACh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11932. Instance Table

Instance Name	Physical Address
USB0	0F90 81ACh

Figure 14-5893. USB2SS_PHY2_TED_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CALIB_CODE_DOWN</td><td colspan="4">CALIB_CODE_UP</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-11933. USB2SS_PHY2_TED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_DOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	CALIB_CODE_UP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.121 USB2SS_PHY2_TED_REG2 Register

14.7.3.2.2.121.1 USB2SS_PHY2_TED_REG2 Register (Offset = 1B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11934. Instance Table

Instance Name	Physical Address
USB0	0F90 81B0h

Figure 14-5894. USB2SS_PHY2_TED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			CALIB_MODE_DN	CALIB_MODE_DN_EN	CALIB_MODE_UP	CALIB_MODE_UP_EN	CALIB_CODE_DN_EN
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-11935. USB2SS_PHY2_TED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
4	CALIB_MODE_DN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CALIB_MODE_DN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_MODE_UP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CALIB_MODE_UP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_CODE_DN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.122 USB2SS_PHY2_CALIB_REG2 Register

14.7.3.2.2.122.1 USB2SS_PHY2_CALIB_REG2 Register (Offset = 1B4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11936. Instance Table

Instance Name	Physical Address
USB0	0F90 81B4h

Figure 14-5895. USB2SS_PHY2_CALIB_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">UNUSED</td><td>CALIB_CMP</td><td>CALIB_PD</td><td>CALIB_CLOCK</td><td>CALIB_DONE</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-11937. USB2SS_PHY2_CALIB_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
3	CALIB_CMP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CALIB_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.123 USB2SS_PHY2_CALIB_REG3 Register

14.7.3.2.2.123.1 USB2SS_PHY2_CALIB_REG3 Register (Offset = 1B8h) [reset = 0h]

Resistor calibration code

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Table 14-11938. Instance Table

Instance Name	Physical Address
USB0	0F90 81B8h

Figure 14-5896. USB2SS_PHY2_CALIB_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED			BG_UNIT_RES_CALIB				
R			R				
0h			0h				

Table 14-11939. USB2SS_PHY2_CALIB_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
4:0	BG_UNIT_RES_CALIB	R	0h	Resistor calibration code from the calibration block Reset Source: usb2_sync_preset_n

14.7.3.2.2.124 USB2SS_PHY2_BC_REG8 Register

14.7.3.2.2.124.1 USB2SS_PHY2_BC_REG8 Register (Offset = 1BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11940. Instance Table

Instance Name	Physical Address
USB0	0F90 81BCh

Figure 14-5897. USB2SS_PHY2_BC_REG8 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>DCD_COMP</td><td>ADP_SENSE</td><td>ADP_PROBE</td><td>BVALID</td><td>VBUSVALID</td><td>IDDIG</td><td colspan="2">UNUSED</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td colspan="2">R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-11941. USB2SS_PHY2_BC_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DCD_COMP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ADP_SENSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	ADP_PROBE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VBUSVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	IDDIG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.125 USB2SS_PHY2_BC_REG9 Register

14.7.3.2.2.125.1 USB2SS_PHY2_BC_REG9 Register (Offset = 1C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11942. Instance Table

Instance Name	Physical Address
USB0	0F90 81C0h

Figure 14-5898. USB2SS_PHY2_BC_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_DM_VDAT_REF_COMP_EN	O_DP_VDAT_REF_COMP_EN	O_VDM_SRC_EN	O_VDP_SRC_EN	O_IDM_SINK_EN	O_IDP_SINK_EN	O_IDP_SRC_EN	O_BC_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11943. USB2SS_PHY2_BC_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_DM_VDAT_REF_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_DP_VDAT_REF_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_VDM_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_VDP_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_IDM_SINK_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_IDP_SINK_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11943. USB2SS_PHY2_BC_REG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	O_IDP_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_BC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.126 USB2SS_PHY2_BC_REG10 Register

14.7.3.2.2.126.1 USB2SS_PHY2_BC_REG10 Register (Offset = 1C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11944. Instance Table

Instance Name	Physical Address
USB0	0F90 81C4h

Figure 14-5899. USB2SS_PHY2_BC_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_RID_B_C_COMP_EN	O_RID_A_COMP_EN	O_RID_C_REF_EN	O_RID_B_REF_EN	O_RID_A_REF_EN	O_RID_FLOAT_REF_EN	O_RID_NONFLOAT_SRC_EN	O_RID_FLOAT_SRC_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11945. USB2SS_PHY2_BC_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_RID_B_C_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_RID_A_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_RID_C_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_RID_B_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_RID_A_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_RID_FLOAT_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11945. USB2SS_PHY2_BC_REG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	O_RID_NONFLOAT_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_RID_FLOAT_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.127 USB2SS_PHY2_BC_REG11 Register

14.7.3.2.2.127.1 USB2SS_PHY2_BC_REG11 Register (Offset = 1C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11946. Instance Table

Instance Name	Physical Address
USB0	0F90 81C8h

Figure 14-5900. USB2SS_PHY2_BC_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_IDM_SRC_EN	I_AFE_RXDP_ANA	I_AFE_RXDM_ANA	I_RID_B_C_COMP_STS	I_RID_A_COMP_STS	I_DM_VDAT_REF_COMP_STS	I_DP_VDAT_REF_COMP_STS	O_DM_VLGC_COMP_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11947. USB2SS_PHY2_BC_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_IDM_SRC_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	I_AFE_RXDP_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	I_AFE_RXDM_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	I_RID_B_C_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	I_RID_A_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	I_DM_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11947. USB2SS_PHY2_BC_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	I_DP_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_DM_VLGC_COMP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.128 USB2SS_PHY2_BC_REG12 Register

14.7.3.2.2.128.1 USB2SS_PHY2_BC_REG12 Register (Offset = 1CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11948. Instance Table

Instance Name	Physical Address
USB0	0F90 81CCh

Figure 14-5901. USB2SS_PHY2_BC_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RID_GND_COMP_STS	RID_FLOAT_COMP_STS	RID_C_COMP_STS	RID_B_COMP_STS	RID_A_COMP_STS	DM_VLGC_COMP_STS	DM_VDAT_REF_COMP_STS	DP_VDAT_REF_COMP_STS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11949. USB2SS_PHY2_BC_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RID_GND_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RID_FLOAT_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RID_C_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RID_B_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RID_A_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DM_VLGC_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11949. USB2SS_PHY2_BC_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DM_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DP_VDAT_REF_COMP_STS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.129 USB2SS_PHY2_TED_REG3 Register

14.7.3.2.2.129.1 USB2SS_PHY2_TED_REG3 Register (Offset = 1D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11950. Instance Table

Instance Name	Physical Address
USB0	0F90 81D0h

Figure 14-5902. USB2SS_PHY2_TED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_CODE_DOWN				COMPARATOR_DOWN	CALIB_DONE_DOWN	UNUSED	
R				R	R	R	
0h				0h	0h	0h	

Table 14-11951. USB2SS_PHY2_TED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	COMPARATOR_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_DONE_DOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.130 USB2SS_PHY2_TED_REG4 Register

14.7.3.2.2.130.1 USB2SS_PHY2_TED_REG4 Register (Offset = 1D4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11952. Instance Table

Instance Name	Physical Address
USB0	0F90 81D4h

Figure 14-5903. USB2SS_PHY2_TED_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALIB_CODE_UP				COMPARATOR_UP	CALIB_DONE_UP	UNUSED	
R				R	R	R	
0h				0h	0h	0h	

Table 14-11953. USB2SS_PHY2_TED_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	CALIB_CODE_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	COMPARATOR_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_DONE_UP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1:0	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.131 USB2SS_PHY2_DIG_UNUSED_REG0 Register

14.7.3.2.2.131.1 USB2SS_PHY2_DIG_UNUSED_REG0 Register (Offset = 1D8h) [reset = 0h]

UNUSED

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Table 14-11954. Instance Table

Instance Name	Physical Address
USB0	0F90 81D8h

Figure 14-5904. USB2SS_PHY2_DIG_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
GLITCH_FILTER_EN	UNUSED						
R/W	R/W						
0h	0h						

Table 14-11955. USB2SS_PHY2_DIG_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	GLITCH_FILTER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.132 USB2SS_PHY2_DIG_UNUSED_REG1 Register

14.7.3.2.2.132.1 USB2SS_PHY2_DIG_UNUSED_REG1 Register (Offset = 1DCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11956. Instance Table

Instance Name	Physical Address
USB0	0F90 81DCh

Figure 14-5905. USB2SS_PHY2_DIG_UNUSED_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">UNUSED</td><td colspan="2">THRESHOLD_OVR_VALUE_MSB</td><td>THRESHOLD_OVR_EN</td></tr>
<tr><td colspan="5">R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-11957. USB2SS_PHY2_DIG_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
2:1	THRESHOLD_OVR_VALUE_MSB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	THRESHOLD_OVR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.133 USB2SS_PHY2_DIG_UNUSED_REG2 Register

14.7.3.2.2.133.1 USB2SS_PHY2_DIG_UNUSED_REG2 Register (Offset = 1E0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11958. Instance Table

Instance Name	Physical Address
USB0	0F90 81E0h

Figure 14-5906. USB2SS_PHY2_DIG_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
THRESHOLD_OVR_VALUE_LSB							
R/W							
0h							

Table 14-11959. USB2SS_PHY2_DIG_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	THRESHOLD_OVR_VALUE_LSB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.134 USB2SS_PHY2_DIG_UNUSED_REG3 Register

14.7.3.2.2.134.1 USB2SS_PHY2_DIG_UNUSED_REG3 Register (Offset = 1E4h) [reset = 0h]

UNUSED

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Table 14-11960. Instance Table

Instance Name	Physical Address
USB0	0F90 81E4h

Figure 14-5907. USB2SS_PHY2_DIG_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-11961. USB2SS_PHY2_DIG_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.135 USB2SS_PHY2_INTERRUPT_REG1 Register

14.7.3.2.2.135.1 USB2SS_PHY2_INTERRUPT_REG1 Register (Offset = 1E8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11962. Instance Table

Instance Name	Physical Address
USB0	0F90 81E8h

Figure 14-5908. USB2SS_PHY2_INTERRUPT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IRSR	ISR	UNUSED					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-11963. USB2SS_PHY2_INTERRUPT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	IRSR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ISR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.136 USB2SS_PHY2_INTERRUPT_REG2 Register

14.7.3.2.2.136.1 USB2SS_PHY2_INTERRUPT_REG2 Register (Offset = 1ECh) [reset = 1h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11964. Instance Table

Instance Name	Physical Address
USB0	0F90 81ECh

Figure 14-5909. USB2SS_PHY2_INTERRUPT_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED							IMR
R/W							R/W
0h							1h

Table 14-11965. USB2SS_PHY2_INTERRUPT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:1	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n
0	IMR	R/W	1h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.137 USB2SS_PHY2_RX_REG0 Register

14.7.3.2.2.137.1 USB2SS_PHY2_RX_REG0 Register (Offset = 200h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11966. Instance Table

Instance Name	Physical Address
USB0	0F90 8200h

Figure 14-5910. USB2SS_PHY2_RX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSLS_NO_EOP_TIMEOUT			FSLS_TIMEOUT_EN	HS_SYNC_DET_BITS	FS_EOP_SE0_THRESHOLD		FS_EOP_SE0_EN
R/W			R/W	R/W	R/W		R/W
0h			0h	0h	0h		0h

Table 14-11967. USB2SS_PHY2_RX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:5	FSLS_NO_EOP_TIMEOUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	FSLS_TIMEOUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_SYNC_DET_BITS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	FS_EOP_SE0_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_EOP_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.138 USB2SS_PHY2_RX_REG1 Register

14.7.3.2.2.138.1 USB2SS_PHY2_RX_REG1 Register (Offset = 204h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11968. Instance Table

Instance Name	Physical Address
USB0	0F90 8204h

Figure 14-5911. USB2SS_PHY2_RX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LS_EOP_SE0_THRESHOLD						LS_EOP_SE0_EN	FS_NO_EOP_TIMEOUT_EN
R/W						R/W	R/W
0h						0h	0h

Table 14-11969. USB2SS_PHY2_RX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	LS_EOP_SE0_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	LS_EOP_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_NO_EOP_TIMEOUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.139 USB2SS_PHY2_TX_REG0 Register

14.7.3.2.2.139.1 USB2SS_PHY2_TX_REG0 Register (Offset = 208h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11970. Instance Table

Instance Name	Physical Address
USB0	0F90 8208h

Figure 14-5912. USB2SS_PHY2_TX_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED				FS_PREAMBLE_EN	SOF_EXTENSION		SOF_EXTENSION_EN
R/W				R/W	R/W		R/W
0h				0h	0h		0h

Table 14-11971. USB2SS_PHY2_TX_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
3	FS_PREAMBLE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	SOF_EXTENSION	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SOF_EXTENSION_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.140 USB2SS_PHY2_TX_REG1 Register

14.7.3.2.2.140.1 USB2SS_PHY2_TX_REG1 Register (Offset = 20Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11972. Instance Table

Instance Name	Physical Address
USB0	0F90 820Ch

Figure 14-5913. USB2SS_PHY2_TX_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PREAMBLE_VALUE							
R/W							
0h							

Table 14-11973. USB2SS_PHY2_TX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PREAMBLE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.141 USB2SS_PHY2_CDR_REG0 Register

14.7.3.2.2.141.1 USB2SS_PHY2_CDR_REG0 Register (Offset = 210h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11974. Instance Table

Instance Name	Physical Address
USB0	0F90 8210h

Figure 14-5914. USB2SS_PHY2_CDR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED		PLL_CLKDIV		PLL_CLKDIV_EN	SQUELCH_DELAY		SQUELCH_DELAY_EN
R/W		R/W		R/W	R/W		R/W
0h		0h		0h	0h		0h

Table 14-11975. USB2SS_PHY2_CDR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
5:4	PLL_CLKDIV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	PLL_CLKDIV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	SQUELCH_DELAY	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SQUELCH_DELAY_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.142 USB2SS_PHY2_CDR_REG1 Register

14.7.3.2.2.142.1 USB2SS_PHY2_CDR_REG1 Register (Offset = 214h) [reset = 0h]

dynamic calib controls

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Table 14-11976. Instance Table

Instance Name	Physical Address
USB0	0F90 8214h

Figure 14-5915. USB2SS_PHY2_CDR_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED	CALIB_COMP_OUT	CALIB_SPC_THRESHOLD			CALIB_SPC_THRESHOLD_EN	CALIB_ITERATION	DYNAMIC_CALIB_EN
R/W	R/W	R/W			R/W	R/W	R/W
0h	0h	0h			0h	0h	0h

Table 14-11977. USB2SS_PHY2_CDR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	CALIB_COMP_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:3	CALIB_SPC_THRESHOLD	R/W	0h	000 The time interval between succesive calibrations is 0us, 001 The time interval between succesive calibrations is 1us, 010 The time interval between succesive calibrations is 2us, 011 The time interval between succesive calibrations is 3us, 100 The time interval between succesive calibrations is 4us, 101 The time interval between succesive calibrations is 5us, 110 The time interval between succesive calibrations is 6us, 111 The time interval between succesive calibrations is 7us. Reset Source: usb2_sync_preset_n
2	CALIB_SPC_THRESHOLD_EN	R/W	0h	0 The time interval between succesive calibrations is taken as 5us by default, 1 The time interval between succesive calibrations is taken from CDR_REG1[5:3] Reset Source: usb2_sync_preset_n

Table 14-11977. USB2SS_PHY2_CDR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CALIB_ITERATION	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DYNAMIC_CALIB_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.143 USB2SS_PHY2_CDR_REG2 Register

14.7.3.2.2.143.1 USB2SS_PHY2_CDR_REG2 Register (Offset = 218h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11978. Instance Table

Instance Name	Physical Address
USB0	0F90 8218h

Figure 14-5916. USB2SS_PHY2_CDR_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	HSRX_EN_DEL	HSRX_EN_DEL_EN	HSRX_EN	HSRX_EN_EN	CALIB_CLOCK	CALIB_CLOCK_EN	CALIB_OUT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11979. USB2SS_PHY2_CDR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	HSRX_EN_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSRX_EN_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSRX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSRX_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CALIB_CLOCK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CALIB_CLOCK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11979. USB2SS_PHY2_CDR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CALIB_OUT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.144 USB2SS_PHY2_CDR_REG3 Register

14.7.3.2.2.144.1 USB2SS_PHY2_CDR_REG3 Register (Offset = 21Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11980. Instance Table

Instance Name	Physical Address
USB0	0F90 821Ch

Figure 14-5917. USB2SS_PHY2_CDR_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_ACTIVE	CALIB_DONE	CALIB_CODE					
R/W	R/W	R/W					
0h	0h	0h					

Table 14-11981. USB2SS_PHY2_CDR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_ACTIVE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CALIB_DONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	CALIB_CODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.145 USB2SS_PHY2_CDR_REG4 Register

14.7.3.2.2.145.1 USB2SS_PHY2_CDR_REG4 Register (Offset = 220h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11982. Instance Table

Instance Name	Physical Address
USB0	0F90 8220h

Figure 14-5918. USB2SS_PHY2_CDR_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLK_GATE_VALUE	CLK_GATE_EN	CLK_GATE_SQ_MASK	LATENCY_THRESHOLD		LATENCY_THRESHOLD_EN	DECISION_ERROR_EN	FILTER_EN
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	0h

Table 14-11983. USB2SS_PHY2_CDR_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLK_GATE_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CLK_GATE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	CLK_GATE_SQ_MASK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	LATENCY_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	LATENCY_THRESHOLD_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DECISION_ERROR_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11983. USB2SS_PHY2_CDR_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FILTER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.146 USB2SS_PHY2_CDR_REG5 Register

14.7.3.2.2.146.1 USB2SS_PHY2_CDR_REG5 Register (Offset = 224h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11984. Instance Table

Instance Name	Physical Address
USB0	0F90 8224h

Figure 14-5919. USB2SS_PHY2_CDR_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED					SAMPLE_5X_EN	SMALL_PULSE	SMALL_PULSE_EN
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-11985. USB2SS_PHY2_CDR_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
2	SAMPLE_5X_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	SMALL_PULSE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SMALL_PULSE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.147 USB2SS_PHY2_CDR_REG6 Register

14.7.3.2.2.147.1 USB2SS_PHY2_CDR_REG6 Register (Offset = 228h) [reset = 0h]

unused

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Table 14-11986. Instance Table

Instance Name	Physical Address
USB0	0F90 8228h

Figure 14-5920. USB2SS_PHY2_CDR_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-11987. USB2SS_PHY2_CDR_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.148 USB2SS_PHY2_CDR_REG7 Register

14.7.3.2.2.148.1 USB2SS_PHY2_CDR_REG7 Register (Offset = 22Ch) [reset = 0h]

unused

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Table 14-11988. Instance Table

Instance Name	Physical Address
USB0	0F90 822Ch

Figure 14-5921. USB2SS_PHY2_CDR_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-11989. USB2SS_PHY2_CDR_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.149 USB2SS_PHY2_CDR_REG8 Register

14.7.3.2.2.149.1 USB2SS_PHY2_CDR_REG8 Register (Offset = 230h) [reset = 0h]

unused

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Table 14-11990. Instance Table

Instance Name	Physical Address
USB0	0F90 8230h

Figure 14-5922. USB2SS_PHY2_CDR_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-11991. USB2SS_PHY2_CDR_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.150 USB2SS_PHY2_RX_REG2 Register

14.7.3.2.2.150.1 USB2SS_PHY2_RX_REG2 Register (Offset = 234h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11992. Instance Table

Instance Name	Physical Address
USB0	0F90 8234h

Figure 14-5923. USB2SS_PHY2_RX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EB_ERROR	CDR_ERROR	SYNC_DETECTED	EOP_DETECTED	HS_EOP_CONDITION	NORMAL_EOP	ALIGNMENT_ERROR	NO_EOP
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-11993. USB2SS_PHY2_RX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EB_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	CDR_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SYNC_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_EOP_CONDITION	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	NORMAL_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-11993. USB2SS_PHY2_RX_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ALIGNMENT_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	NO_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.151 USB2SS_PHY2_RX_REG3 Register

14.7.3.2.2.151.1 USB2SS_PHY2_RX_REG3 Register (Offset = 238h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11994. Instance Table

Instance Name	Physical Address
USB0	0F90 8238h

Figure 14-5924. USB2SS_PHY2_RX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS_EOP_DETECTED	SE0_VALIDATED	LSFS_EOP_DETECTED	BIT_UNSTUFF_ERROR	RX_STATE_BITUNSTUFF			START_FLAG
R	R	R	R	R			R
0h	0h	0h	0h	0h			0h

Table 14-11995. USB2SS_PHY2_RX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SE0_VALIDATED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	LSFS_EOP_DETECTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIT_UNSTUFF_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	RX_STATE_BITUNSTUFF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	START_FLAG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.152 USB2SS_PHY2_RX_REG4 Register

14.7.3.2.2.152.1 USB2SS_PHY2_RX_REG4 Register (Offset = 23Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-11996. Instance Table

Instance Name	Physical Address
USB0	0F90 823Ch

Figure 14-5925. USB2SS_PHY2_RX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RXACTIVE_REG	DEASSERT_RXACTIVE_REG	UNUSED					
R	R	R					
0h	0h	0h					

Table 14-11997. USB2SS_PHY2_RX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RXACTIVE_REG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DEASSERT_RXACTIVE_REG	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.153 USB2SS_PHY2_RX_REG5 Register

14.7.3.2.2.153.1 USB2SS_PHY2_RX_REG5 Register (Offset = 240h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-11998. Instance Table

Instance Name	Physical Address
USB0	0F90 8240h

Figure 14-5926. USB2SS_PHY2_RX_REG5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SIE_CNT_UPPER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-11999. USB2SS_PHY2_RX_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	SIE_CNT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.154 USB2SS_PHY2_RX_REG6 Register

14.7.3.2.2.154.1 USB2SS_PHY2_RX_REG6 Register (Offset = 244h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12000. Instance Table

Instance Name	Physical Address
USB0	0F90 8244h

Figure 14-5927. USB2SS_PHY2_RX_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CNT_UPPER							
R							
0h							

Table 14-12001. USB2SS_PHY2_RX_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PHY_CNT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.155 USB2SS_PHY2_RX_REG7 Register

14.7.3.2.2.155.1 USB2SS_PHY2_RX_REG7 Register (Offset = 248h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-12002. Instance Table

Instance Name	Physical Address
USB0	0F90 8248h

Figure 14-5928. USB2SS_PHY2_RX_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PHY_CNT_LOWER				SIE_CNT_LOWER			
R				R			
0h				0h			

Table 14-12003. USB2SS_PHY2_RX_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	PHY_CNT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	SIE_CNT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.156 USB2SS_PHY2_TX_REG2 Register

14.7.3.2.2.156.1 USB2SS_PHY2_TX_REG2 Register (Offset = 24Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12004. Instance Table

Instance Name	Physical Address
USB0	0F90 824Ch

Figure 14-5929. USB2SS_PHY2_TX_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_HS_STATE				EOP_TRANSMITTED	HS_BITSTUFF_EN	RESUME_EOP	REMOTE_WAKEUP
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-12005. USB2SS_PHY2_TX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	TX_HS_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	EOP_TRANSMITTED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HS_BITSTUFF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RESUME_EOP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	REMOTE_WAKEUP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.157 USB2SS_PHY2_TX_REG3 Register

14.7.3.2.2.157.1 USB2SS_PHY2_TX_REG3 Register (Offset = 250h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12006. Instance Table

Instance Name	Physical Address
USB0	0F90 8250h

Figure 14-5930. USB2SS_PHY2_TX_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_LSFS_STATE				PD_STATE			PREAMBLE_SENT
R				R			R
0h				0h			0h

Table 14-12007. USB2SS_PHY2_TX_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	TX_LSFS_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:1	PD_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	PREAMBLE_SENT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.158 USB2SS_PHY2_TX_REG4 Register

14.7.3.2.2.158.1 USB2SS_PHY2_TX_REG4 Register (Offset = 254h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12008. Instance Table

Instance Name	Physical Address
USB0	0F90 8254h

Figure 14-5931. USB2SS_PHY2_TX_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED						LSFS_BITSTUFF_EN	LS_KEEP_ALIVE
R						R	R
0h						0h	0h

Table 14-12009. USB2SS_PHY2_TX_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
1	LSFS_BITSTUFF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	LS_KEEP_ALIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.159 USB2SS_PHY2_CDR_REG9 Register

14.7.3.2.2.159.1 USB2SS_PHY2_CDR_REG9 Register (Offset = 258h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12010. Instance Table

Instance Name	Physical Address
USB0	0F90 8258h

Figure 14-5932. USB2SS_PHY2_CDR_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED					I_ANA_COMP_OUT	SAMPLER_CALIB_DONE	ANA_CALIB_ACTIVE
R					R	R	R
0h					0h	0h	0h

Table 14-12011. USB2SS_PHY2_CDR_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:3	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
2	I_ANA_COMP_OUT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	SAMPLER_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ANA_CALIB_ACTIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.160 USB2SS_PHY2_CDR_REG10 Register

14.7.3.2.2.160.1 USB2SS_PHY2_CDR_REG10 Register (Offset = 25Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12012. Instance Table

Instance Name	Physical Address
USB0	0F90 825Ch

Figure 14-5933. USB2SS_PHY2_CDR_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED		CALIB_CODE					
R		R					
0h		0h					

Table 14-12013. USB2SS_PHY2_CDR_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
5:0	CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.161 USB2SS_PHY2_CDR_REG11 Register

14.7.3.2.2.161.1 USB2SS_PHY2_CDR_REG11 Register (Offset = 260h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12014. Instance Table

Instance Name	Physical Address
USB0	0F90 8260h

Figure 14-5934. USB2SS_PHY2_CDR_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SMALL_PULSE				O_HSRX_REC_DICISION_ERROR	O_ANA_CLK_GATE	RECEIVE_START	I_ANA_TED_SQUELCH
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-12015. USB2SS_PHY2_CDR_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	SMALL_PULSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_HSRX_REC_DICISION_ERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_ANA_CLK_GATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RECEIVE_START	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	I_ANA_TED_SQUELCH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.162 USB2SS_PHY2_CDR_RE12 Register

14.7.3.2.2.162.1 USB2SS_PHY2_CDR_RE12 Register (Offset = 264h) [reset = 0h]

unused

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Table 14-12016. Instance Table

Instance Name	Physical Address
USB0	0F90 8264h

Figure 14-5935. USB2SS_PHY2_CDR_RE12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-12017. USB2SS_PHY2_CDR_RE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.163 USB2SS_PHY2_DIG_TXRX_UNUSED_REG0 Register

14.7.3.2.2.163.1 USB2SS_PHY2_DIG_TXRX_UNUSED_REG0 Register (Offset = 268h) [reset = 0h]

UNUSED

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Table 14-12018. Instance Table

Instance Name	Physical Address
USB0	0F90 8268h

Figure 14-5936. USB2SS_PHY2_DIG_TXRX_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-12019. USB2SS_PHY2_DIG_TXRX_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.164 USB2SS_PHY2_DIG_TXRX_UNUSED_REG1 Register

14.7.3.2.2.164.1 USB2SS_PHY2_DIG_TXRX_UNUSED_REG1 Register (Offset = 26Ch) [reset = 0h]

UNUSED

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Table 14-12020. Instance Table

Instance Name	Physical Address
USB0	0F90 826Ch

Figure 14-5937. USB2SS_PHY2_DIG_TXRX_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-12021. USB2SS_PHY2_DIG_TXRX_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.165 USB2SS_PHY2_DIG_TXRX_UNUSED_REG2 Register

14.7.3.2.2.165.1 USB2SS_PHY2_DIG_TXRX_UNUSED_REG2 Register (Offset = 270h) [reset = 0h]

UNUSED

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Table 14-12022. Instance Table

Instance Name	Physical Address
USB0	0F90 8270h

Figure 14-5938. USB2SS_PHY2_DIG_TXRX_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-12023. USB2SS_PHY2_DIG_TXRX_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.166 USB2SS_PHY2_DIG_TXRX_UNUSED_REG3 Register

14.7.3.2.2.166.1 USB2SS_PHY2_DIG_TXRX_UNUSED_REG3 Register (Offset = 274h) [reset = 0h]

UNUSED

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Table 14-12024. Instance Table

Instance Name	Physical Address
USB0	0F90 8274h

Figure 14-5939. USB2SS_PHY2_DIG_TXRX_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-12025. USB2SS_PHY2_DIG_TXRX_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	UNUSED Reset Source: usb2_sync_preset_n

14.7.3.2.2.167 USB2SS_PHY2_UTMI_REG0 Register

14.7.3.2.2.167.1 USB2SS_PHY2_UTMI_REG0 Register (Offset = 280h) [reset = 0h]

register UTMI_REG0

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Table 14-12026. Instance Table

Instance Name	Physical Address
USB0	0F90 8280h

Figure 14-5940. USB2SS_PHY2_UTMI_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">LOOPBACK_SEL</td><td>LOOPBACK_EN</td><td colspan="4">BIST_MODE_SEL</td><td>BIST_EN</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>0h</td></tr>
</table>

Table 14-12027. USB2SS_PHY2_UTMI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	LOOPBACK_SEL	R/W	0h	00 Loopback mode selection = 00 : Reserved, 01 Loopback mode selection = 01 : LS, 10 Loopback mode selection = 10 : FS, 11 Loopback mode selection = 11 : HS Reset Source: usb2_sync_preset_n
5	LOOPBACK_EN	R/W	0h	0 Loopback mode selection is taken from primary input port-loopback[1:0], 1 Loopback mode selection is taken from UTMI_REG0[7:6]. Reset Source: usb2_sync_preset_n
4:1	BIST_MODE_SEL	R/W	0h	0 BIST for 8 bit, 1 BIST for 16 bit, 0 Error injection disabled, 1 Error injection enabled, 0 BIST for device mode, 1 BIST for host mode, 0 BIST for HS mode, 1 BIST for FS mode. Reset Source: usb2_sync_preset_n
0	BIST_EN	R/W	0h	0 BIST control signals taken from primary input BIST related ports, 1 BIST signals taken from UTMI REG0[4:1], UTMI_REG1[7:6], UTMI_REG5[7:6] Reset Source: usb2_sync_preset_n

14.7.3.2.2.168 USB2SS_PHY2_UTMI_REG1 Register

14.7.3.2.2.168.1 USB2SS_PHY2_UTMI_REG1 Register (Offset = 284h) [reset = 0h]

bist error injection, soft resets

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Table 14-12028. Instance Table

Instance Name	Physical Address
USB0	0F90 8284h

Figure 14-5941. USB2SS_PHY2_UTMI_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_ERR		BIST_SOFT_RST	TX_LSFS_SOFT_RST	TX_HS_SOFT_RST	CLKDIV_SOFT_RST	CALIB_SOFT_RST	PHY_SOFT_RST
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-12029. USB2SS_PHY2_UTMI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_ERR	R/W	0h	00 Introduce error on first packet, bist error injection = 00, 01 Introduce error on second packet,bist error injection = 01, 10 Introduce error on third packet, bist error injection = 10, 11 Introduce error on last packet, bist error injection = 11. Reset Source: usb2_sync_preset_n
5	BIST_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	TX_LSFS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TX_HS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	CLKDIV_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	CALIB_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12029. USB2SS_PHY2_UTMI_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.169 USB2SS_PHY2_UTMI_REG2 Register

14.7.3.2.2.169.1 USB2SS_PHY2_UTMI_REG2 Register (Offset = 288h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12030. Instance Table

Instance Name	Physical Address
USB0	0F90 8288h

Figure 14-5942. USB2SS_PHY2_UTMI_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_CNTRL_SOFT_RST	SHIFT_REG_SOFT_RST	BITUNSTUFF_SOFT_RST	NRZI_DEC_SOFT_RST	EOP_DET_SOFT_RST	SYNC_DET_SOFT_RST	LSFS_DLL_SOFT_RST	RX_HS_SOFT_RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12031. USB2SS_PHY2_UTMI_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RX_CNTRL_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SHIFT_REG_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BITUNSTUFF_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	NRZI_DEC_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	EOP_DET_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	SYNC_DET_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12031. USB2SS_PHY2_UTMI_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LSFS_DLL_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	RX_HS_SOFT_RST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.170 USB2SS_PHY2_UTMI_REG3 Register

14.7.3.2.2.170.1 USB2SS_PHY2_UTMI_REG3 Register (Offset = 28Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12032. Instance Table

Instance Name	Physical Address
USB0	0F90 828Ch

Figure 14-5943. USB2SS_PHY2_UTMI_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HS_RX_ERR	LS_LINESTATE_FIL_EN	FS_LINESTATE_FIL_CNT					FS_LINESTATE_FIL_EN
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-12033. USB2SS_PHY2_UTMI_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_RX_ERR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	LS_LINESTATE_FIL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:1	FS_LINESTATE_FIL_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	FS_LINESTATE_FIL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.171 USB2SS_PHY2_UTMI_REG4 Register

14.7.3.2.2.171.1 USB2SS_PHY2_UTMI_REG4 Register (Offset = 290h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12034. Instance Table

Instance Name	Physical Address
USB0	0F90 8290h

Figure 14-5944. USB2SS_PHY2_UTMI_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LS_LINESTATE_FIL_CNT							
R/W							
0h							

Table 14-12035. USB2SS_PHY2_UTMI_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	LS_LINESTATE_FIL_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.172 USB2SS_PHY2_UTMI_REG5 Register

14.7.3.2.2.172.1 USB2SS_PHY2_UTMI_REG5 Register (Offset = 294h) [reset = 0h]

BIST, hsrx data

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Table 14-12036. Instance Table

Instance Name	Physical Address
USB0	0F90 8294h

Figure 14-5945. USB2SS_PHY2_UTMI_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_MODE_EN	BIST_ON	HSTX_BOOST_DEAMP_OFF	HSTX_BOOST	HS_SAMP	HS_SAMP_EN	HSRX	HSRX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12037. USB2SS_PHY2_UTMI_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	BIST_MODE_EN	R/W	0h	0 BIST mode en is taken from primary input port- bist_mode_en, 1 bist_mode_en is turned on. Reset Source: usb2_sync_preset_n
6	BIST_ON	R/W	0h	0 BIST on is taken from primary input port- bist_on, 1 bist_on is enabled. Reset Source: usb2_sync_preset_n
5	HSTX_BOOST_DEAMP_OFF	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_BOOST	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HS_SAMP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HS_SAMP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12037. USB2SS_PHY2_UTMI_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HSRX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSRX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.173 USB2SS_PHY2_UTMI_REG6 Register

14.7.3.2.2.173.1 USB2SS_PHY2_UTMI_REG6 Register (Offset = 298h) [reset = 0h]

vbusvalid control, hs drive en threshold

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Table 14-12038. Instance Table

Instance Name	Physical Address
USB0	0F90 8298h

Figure 14-5946. USB2SS_PHY2_UTMI_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBUSVALID_CNTRL	VBUSVALID_L3_DEV_EN	HS_DRVEN_THRESHOLD					HS_DRVEN_TH_EN
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-12039. USB2SS_PHY2_UTMI_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	VBUSVALID_CNTRL	R/W	0h	0 vbusvalid comparator is not enabled in L3 device Powered Off state, 1 vbusvalid comparator is enabled in L3 device Powered Off state Reset Source: usb2_sync_preset_n
6	VBUSVALID_L3_DEV_EN	R/W	0h	0 Vbusvalid comparator output comes on vbusvalid primary output port, 1 Sessvalid comparator output comes on vbusvalid primary output port. Reset Source: usb2_sync_preset_n
5:1	HS_DRVEN_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HS_DRVEN_TH_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.174 USB2SS_PHY2_UTMI_REG7 Register

14.7.3.2.2.174.1 USB2SS_PHY2_UTMI_REG7 Register (Offset = 29Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12040. Instance Table

Instance Name	Physical Address
USB0	0F90 829Ch

Figure 14-5947. USB2SS_PHY2_UTMI_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HSTX_BC_MODE	HSTX_BC_EN	HSTX_CHIRP_MODE	HSTX_CHIRP_EN	HSTX_EN_DEL	HSTX_EN_DEL_EN	HSTX	HSTX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12041. USB2SS_PHY2_UTMI_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HSTX_BC_MODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HSTX_BC_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSTX_CHIRP_MODE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_CHIRP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSTX_EN_DEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HSTX_EN_DEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12041. USB2SS_PHY2_UTMI_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HSTX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.175 USB2SS_PHY2_UTMI_REG8 Register

14.7.3.2.2.175.1 USB2SS_PHY2_UTMI_REG8 Register (Offset = 2A0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12042. Instance Table

Instance Name	Physical Address
USB0	0F90 82A0h

Figure 14-5948. USB2SS_PHY2_UTMI_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HS_TERM	HS_TERM_EN	HSTX_DATA	HSTX_DATA_EN	HSTX_DRV	HSTX_DRV_EN	HSTX_PREDRV	HSTX_PREDRV_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12043. USB2SS_PHY2_UTMI_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_TERM	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HS_TERM_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSTX_DATA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSTX_DATA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	HSTX_DRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HSTX_DRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12043. USB2SS_PHY2_UTMI_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HSTX_PREDRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_PREDRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.176 USB2SS_PHY2_UTMI_REG9 Register

14.7.3.2.2.176.1 USB2SS_PHY2_UTMI_REG9 Register (Offset = 2A4h) [reset = 0h]

hs delay values

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Table 14-12044. Instance Table

Instance Name	Physical Address
USB0	0F90 82A4h

Figure 14-5949. USB2SS_PHY2_UTMI_REG9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CLKOFF_EN</td><td colspan="3">SDC_SPACE</td><td>SDC_SPACE_EN</td><td colspan="2">HSTX_EN_DEL_TH</td><td>HSTX_EN_DEL_TH_EN</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td></tr>
</table>

Table 14-12045. USB2SS_PHY2_UTMI_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLKOFF_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:4	SDC_SPACE	R/W	0h	000- The time between successive resistor calibration is 0ms, 001- The time between successive resistor calibration is 500ms, 010- The time between successive resistor calibration is 1000ms, 011- The time between successive resistor calibration is1500ms, 100- The time between successive resistor calibration is 2000ms, 101- The time between successive resistor calibration is 2500ms, 110- The time between successive resistor calibration is 3000ms, 111- The time between successive resistor calibration is 3500ms. Reset Source: usb2_sync_preset_n
3	SDC_SPACE_EN	R/W	0h	0- The time between successive resistor calibration taken as 1s by default, 1- The time between successive resistor calibration taken from UTMI_REG9[6:4]. Reset Source: usb2_sync_preset_n
2:1	HSTX_EN_DEL_TH	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12045. USB2SS_PHY2_UTMI_REG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HSTX_EN_DEL_TH_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.177 USB2SS_PHY2_UTMI_REG10 Register

14.7.3.2.2.177.1 USB2SS_PHY2_UTMI_REG10 Register (Offset = 2A8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12046. Instance Table

Instance Name	Physical Address
USB0	0F90 82A8h

Figure 14-5950. USB2SS_PHY2_UTMI_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_CLKON	PLL_CLKON_EN	BG_PD_BG_OK	BG_PD_BG_OK_EN	LSFS_SERX	LSFS_SERX_EN	LSFS_RX	LSFS_RX_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12047. USB2SS_PHY2_UTMI_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	PLL_CLKON	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	PLL_CLKON_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BG_PD_BG_OK	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BG_PD_BG_OK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	LSFS_SERX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	LSFS_SERX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12047. USB2SS_PHY2_UTMI_REG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LSFS_RX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	LSFS_RX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.178 USB2SS_PHY2_UTMI_REG11 Register

14.7.3.2.2.178.1 USB2SS_PHY2_UTMI_REG11 Register (Offset = 2ACh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12048. Instance Table

Instance Name	Physical Address
USB0	0F90 82ACh

Figure 14-5951. USB2SS_PHY2_UTMI_REG11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CLEAN_LINESTATE_SERX_MASK_EN</td><td>SERX_MASK_EN</td><td colspan="2">SERX_MASK_THRESHOLD</td><td>LSFS_TX</td><td>LSFS_TX_EN</td><td>FSLS_EDGESEL</td><td>FSLS_EDGESEL_EN</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12049. USB2SS_PHY2_UTMI_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CLEAN_LINESTATE_SERX_MASK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SERX_MASK_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	SERX_MASK_THRESHOLD	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	LSFS_TX	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	LSFS_TX_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	FSLS_EDGESEL	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12049. USB2SS_PHY2_UTMI_REG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FSLS_EDGESEL_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.179 USB2SS_PHY2_UTMI_REG12 Register

14.7.3.2.2.179.1 USB2SS_PHY2_UTMI_REG12 Register (Offset = 2B0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12050. Instance Table

Instance Name	Physical Address
USB0	0F90 82B0h

Figure 14-5952. USB2SS_PHY2_UTMI_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SERX_BIAS_EN		FSLS_TX_DATA	FSLS_TX_DATA_EN	FSLS_TX_SE0	FSLS_TX_SE0_EN	FSLS_TX_DRV	FSLS_TX_DRV_EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-12051. USB2SS_PHY2_UTMI_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SERX_BIAS_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	FSLS_TX_DATA	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	FSLS_TX_DATA_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	FSLS_TX_SE0	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	FSLS_TX_SE0_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	FSLS_TX_DRV	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12051. USB2SS_PHY2_UTMI_REG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FSLS_TX_DRV_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.180 USB2SS_PHY2_UTMI_REG13 Register

14.7.3.2.2.180.1 USB2SS_PHY2_UTMI_REG13 Register (Offset = 2B4h) [reset = 0h]

serial mode

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Table 14-12052. Instance Table

Instance Name	Physical Address
USB0	0F90 82B4h

Figure 14-5953. USB2SS_PHY2_UTMI_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSLS_SERIALMODE_PULLUP2	FSLS_SERIALMODE_PULLUP2_EN	DM_PULLDOWN	DM_PULLDOWN_EN	DP_PULLDOWN	DP_PULLDOWN_EN	LANE_REVERSE	LANE_REVERSE_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12053. USB2SS_PHY2_UTMI_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FSLS_SERIALMODE_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	FSLS_SERIALMODE_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DM_PULLDOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DM_PULLDOWN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DP_PULLDOWN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DP_PULLDOWN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12053. USB2SS_PHY2_UTMI_REG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LANE_REVERSE	R/W	0h	0- Polarity inversion of DP/DM is not done, 1- Polarity inversion of DP/DM is done Reset Source: usb2_sync_preset_n
0	LANE_REVERSE_EN	R/W	0h	0- Lane Reverse Value is taken from primary input portlane_reverse, 1- Lane Reverse Value taken from UTMI_REG13[1] Reset Source: usb2_sync_preset_n

14.7.3.2.2.181 USB2SS_PHY2_UTMI_REG14 Register

14.7.3.2.2.181.1 USB2SS_PHY2_UTMI_REG14 Register (Offset = 2B8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12054. Instance Table

Instance Name	Physical Address
USB0	0F90 82B8h

Figure 14-5954. USB2SS_PHY2_UTMI_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DM_PULLUP2	DM_PULLUP2_EN	DP_PULLUP2	DP_PULLUP2_EN	DM_PULLUP1	DM_PULLUP1_EN	DP_PULLUP1	DP_PULLUP1_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12055. USB2SS_PHY2_UTMI_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DM_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	DM_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	DP_PULLUP2	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	DP_PULLUP2_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DM_PULLUP1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DM_PULLUP1_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12055. USB2SS_PHY2_UTMI_REG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DP_PULLUP1	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	DP_PULLUP1_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.182 USB2SS_PHY2_UTMI_REG15 Register

14.7.3.2.2.182.1 USB2SS_PHY2_UTMI_REG15 Register (Offset = 2BCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-12056. Instance Table

Instance Name	Physical Address
USB0	0F90 82BCh

Figure 14-5955. USB2SS_PHY2_UTMI_REG15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXVALID_GATE_THRESHOLD_FS		TXVALID_GATE_THRESHOLD_HS		TED_EN_VALUE	TED_EN_CNT	ED_EN_VALUE	ED_EN_CNT
R/W		R/W		R/W	R/W	R/W	R/W
0h		0h		0h	0h	0h	0h

Table 14-12057. USB2SS_PHY2_UTMI_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	TXVALID_GATE_THRESHOLD_FS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	TXVALID_GATE_THRESHOLD_HS	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TED_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	TED_EN_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	ED_EN_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	ED_EN_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.183 USB2SS_PHY2_UTMI_REG16 Register

14.7.3.2.2.183.1 USB2SS_PHY2_UTMI_REG16 Register (Offset = 2C0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-12058. Instance Table

Instance Name	Physical Address
USB0	0F90 82C0h

Figure 14-5956. USB2SS_PHY2_UTMI_REG16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED							
R/W							
0h							

Table 14-12059. USB2SS_PHY2_UTMI_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.184 USB2SS_PHY2_UTMI_REG17 Register

14.7.3.2.2.184.1 USB2SS_PHY2_UTMI_REG17 Register (Offset = 2C4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-12060. Instance Table

Instance Name	Physical Address
USB0	0F90 82C4h

Figure 14-5957. USB2SS_PHY2_UTMI_REG17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SQUELCH_COUNT_IDLE		SQUELCH_COUNT_IDLE_EN	TX_SQ_CNT				TX_SQ_CNT_EN
R/W		R/W	R/W				R/W
0h		0h	0h				0h

Table 14-12061. USB2SS_PHY2_UTMI_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	SQUELCH_COUNT_IDLE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SQUELCH_COUNT_IDLE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:1	TX_SQ_CNT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	TX_SQ_CNT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.185 USB2SS_PHY2_UTMI_REG18 Register

14.7.3.2.2.185.1 USB2SS_PHY2_UTMI_REG18 Register (Offset = 2C8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12062. Instance Table

Instance Name	Physical Address
USB0	0F90 82C8h

Figure 14-5958. USB2SS_PHY2_UTMI_REG18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SLEEP_VALUE	SLEEP_EN	BIST_POWERUP	BIST_POWERUP_EN	POWERUP_EN	UNUSED	CLIPPER_EN	CLIPPER_EN_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12063. USB2SS_PHY2_UTMI_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	SLEEP_VALUE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	SLEEP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	BIST_POWERUP	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	BIST_POWERUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	POWERUP_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12063. USB2SS_PHY2_UTMI_REG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLIPPER_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CLIPPER_EN_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.186 USB2SS_PHY2_UTMI_REG19 Register

14.7.3.2.2.186.1 USB2SS_PHY2_UTMI_REG19 Register (Offset = 2CCh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12064. Instance Table

Instance Name	Physical Address
USB0	0F90 82CCh

Figure 14-5959. USB2SS_PHY2_UTMI_REG19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED							TED_SW_EN
R/W							R/W
0h							0h

Table 14-12065. USB2SS_PHY2_UTMI_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:1	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
0	TED_SW_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.187 USB2SS_PHY2_UTMI_REG20 Register

14.7.3.2.2.187.1 USB2SS_PHY2_UTMI_REG20 Register (Offset = 2D0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12066. Instance Table

Instance Name	Physical Address
USB0	0F90 82D0h

Figure 14-5960. USB2SS_PHY2_UTMI_REG20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HOSTDISCON_RST_REG	HOSTDISCON_RST_REG_EN	CALIB_RST_DT					CALIB_RST_DT_EN
R/W	R/W	R/W					R/W
0h	0h	0h					0h

Table 14-12067. USB2SS_PHY2_UTMI_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HOSTDISCON_RST_REG	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	HOSTDISCON_RST_REG_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:1	CALIB_RST_DT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	CALIB_RST_DT_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.188 USB2SS_PHY2_UTMI_REG21 Register

14.7.3.2.2.188.1 USB2SS_PHY2_UTMI_REG21 Register (Offset = 2D4h) [reset = 0h]

Register UTMI_REG21

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Table 14-12068. Instance Table

Instance Name	Physical Address
USB0	0F90 82D4h

Figure 14-5961. USB2SS_PHY2_UTMI_REG21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CALIB_TRIGER_POSEDGE	AUTO_CAL_ENABLE	ABSVALID	ABSVALID_EN	VBUSVALID	VBUSVALID_EN	SUSPENDM	SUSPENDM_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12069. USB2SS_PHY2_UTMI_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CALIB_TRIGER_POSEDGE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	AUTO_CAL_ENABLE	R/W	0h	0- Dynamic resistor calibration is disabled, 1- Dynamic resistor calibration is enabled Reset Source: usb2_sync_preset_n
5	ABSVALID	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	ABSVALID_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	VBUSVALID	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	VBUSVALID_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12069. USB2SS_PHY2_UTMI_REG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SUSPENDM	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SUSPENDM_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.189 USB2SS_PHY2_UTMI_REG22 Register

14.7.3.2.2.189.1 USB2SS_PHY2_UTMI_REG22 Register (Offset = 2D8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12070. Instance Table

Instance Name	Physical Address
USB0	0F90 82D8h

Figure 14-5962. USB2SS_PHY2_UTMI_REG22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BCCALIB_OFFSET							
R/W							
0h							

Table 14-12071. USB2SS_PHY2_UTMI_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BCCALIB_OFFSET	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.190 USB2SS_PHY2_UTMI_REG23 Register

14.7.3.2.2.190.1 USB2SS_PHY2_UTMI_REG23 Register (Offset = 2DCh) [reset = 0h]

hscalib code offset

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Table 14-12072. Instance Table

Instance Name	Physical Address
USB0	0F90 82DCh

Figure 14-5963. USB2SS_PHY2_UTMI_REG23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSCALIB_OFFSET							
R/W							
0h							

Table 14-12073. USB2SS_PHY2_UTMI_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	HSCALIB_OFFSET	R/W	0h	Bit 0= 0- Final resistor calibration code going to HSTX is not offsetted, 1- Offset given by bits [6:2] is considered for computation of final resistor code going to HSTX. Bit 1= 0- ADD the offset given in bits [6:2] to the resistor calibration code before giving the code to HSTX, 1- Subtract the offset given in bits [6:2] from the reistor calibration code before giving code to HSTX. Bits 6:2= 00000 Programmable offset value for hs resistor calib code -HS OFFSET. Bit 7= reserved Reset Source: usb2_sync_preset_n

14.7.3.2.2.191 USB2SS_PHY2_UTMI_REG24 Register

14.7.3.2.2.191.1 USB2SS_PHY2_UTMI_REG24 Register (Offset = 2E0h) [reset = 0h]

fscalib code offset

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Table 14-12074. Instance Table

Instance Name	Physical Address
USB0	0F90 82E0h

Figure 14-5964. USB2SS_PHY2_UTMI_REG24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSCALIB_OFFSET							
R/W							
0h							

Table 14-12075. USB2SS_PHY2_UTMI_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FSCALIB_OFFSET	R/W	0h	Bit 0= 0- Final resistor calibration code going to FSTX is not offsetted, 1- Offset given by bits [6:2] is used for computation of final resistor code going to FSTX. Bit 1= 0- ADD the offset given in bits [6:2] to the Resistor calibration code before giving the code to FSTX, 1- Subtract the offset given in bits [6:2] from the Resistor calibration code before giving code to FSTX. Bits 6:2= 00000 Programmable offset value for fs resistor calib code - FS OFFSET. Bit 7= reserved. Reset Source: usb2_sync_preset_n

14.7.3.2.2.192 USB2SS_PHY2_UTMI_REG25 Register

14.7.3.2.2.192.1 USB2SS_PHY2_UTMI_REG25 Register (Offset = 2E4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12076. Instance Table

Instance Name	Physical Address
USB0	0F90 82E4h

Figure 14-5965. USB2SS_PHY2_UTMI_REG25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED	HSCALIB						
R/W	R/W						
0h	0h						

Table 14-12077. USB2SS_PHY2_UTMI_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	HSCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.193 USB2SS_PHY2_UTMI_REG26 Register

14.7.3.2.2.193.1 USB2SS_PHY2_UTMI_REG26 Register (Offset = 2E8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12078. Instance Table

Instance Name	Physical Address
USB0	0F90 82E8h

Figure 14-5966. USB2SS_PHY2_UTMI_REG26 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>UNUSED</td><td colspan="7">FSCALIB</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-12079. USB2SS_PHY2_UTMI_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	FSCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.194 USB2SS_PHY2_UTMI_REG27 Register

14.7.3.2.2.194.1 USB2SS_PHY2_UTMI_REG27 Register (Offset = 2ECh) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12080. Instance Table

Instance Name	Physical Address
USB0	0F90 82ECh

Figure 14-5967. USB2SS_PHY2_UTMI_REG27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	BCCALIB						
R/W	R/W						
0h	0h						

Table 14-12081. USB2SS_PHY2_UTMI_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:0	BCCALIB	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.195 USB2SS_PHY2_UTMI_REG28 Register

14.7.3.2.2.195.1 USB2SS_PHY2_UTMI_REG28 Register (Offset = 2F0h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12082. Instance Table

Instance Name	Physical Address
USB0	0F90 82F0h

Figure 14-5968. USB2SS_PHY2_UTMI_REG28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CDR_EB_WR_RESET	UNUSED						SERX_EN_CNTRL_OPMODE01
R/W	R/W						R/W
0h	0h						0h

Table 14-12083. USB2SS_PHY2_UTMI_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CDR_EB_WR_RESET	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:1	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	SERX_EN_CNTRL_OPMODE01	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.196 USB2SS_PHY2_UTMI_REG29 Register

14.7.3.2.2.196.1 USB2SS_PHY2_UTMI_REG29 Register (Offset = 2F4h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12084. Instance Table

Instance Name	Physical Address
USB0	0F90 82F4h

Figure 14-5969. USB2SS_PHY2_UTMI_REG29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UNUSED		PLL_STANDALONE	PLL_STANDALONE_EN	SPARE_OUT			
R/W		R/W	R/W	R/W			
0h		0h	0h	0h			

Table 14-12085. USB2SS_PHY2_UTMI_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	UNUSED	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	PLL_STANDALONE	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	PLL_STANDALONE_EN	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	SPARE_OUT	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.197 USB2SS_PHY2_UTMI_REG30 Register

14.7.3.2.2.197.1 USB2SS_PHY2_UTMI_REG30 Register (Offset = 2F8h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12086. Instance Table

Instance Name	Physical Address
USB0	0F90 82F8h

Figure 14-5970. USB2SS_PHY2_UTMI_REG30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	PLL_480_CLOCK_GATE_OVR	SCAN_ATS_HS_CLOCK_GATE_OVR	VCO_PLL_CLOCK_GATE_OVR	DIG_DIV_REFCLOCK_GATE_OVR	FB_CLOCK_GATE_OVR	ANA_DIV_REFCLOCK_GATE_OVR	HS_CLOCK_GATE_OVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12087. USB2SS_PHY2_UTMI_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n
6	PLL_480_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	SCAN_ATS_HS_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	VCO_PLL_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	DIG_DIV_REFCLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	FB_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12087. USB2SS_PHY2_UTMI_REG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ANA_DIV_REFCLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HS_CLOCK_GATE_OVR	R/W	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.198 USB2SS_PHY2_UTMI_UNUSED_REG0 Register

14.7.3.2.2.198.1 USB2SS_PHY2_UTMI_UNUSED_REG0 Register (Offset = 2FCh) [reset = 0h]

unused

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Table 14-12088. Instance Table

Instance Name	Physical Address
USB0	0F90 82FCh

Figure 14-5971. USB2SS_PHY2_UTMI_UNUSED_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-12089. USB2SS_PHY2_UTMI_UNUSED_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.199 USB2SS_PHY2_UTMI_UNUSED_REG1 Register

14.7.3.2.2.199.1 USB2SS_PHY2_UTMI_UNUSED_REG1 Register (Offset = 300h) [reset = 0h]

unused

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Table 14-12090. Instance Table

Instance Name	Physical Address
USB0	0F90 8300h

Figure 14-5972. USB2SS_PHY2_UTMI_UNUSED_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-12091. USB2SS_PHY2_UTMI_UNUSED_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.200 USB2SS_PHY2_UTMI_UNUSED_REG2 Register

14.7.3.2.2.200.1 USB2SS_PHY2_UTMI_UNUSED_REG2 Register (Offset = 304h) [reset = 0h]

unused

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Table 14-12092. Instance Table

Instance Name	Physical Address
USB0	0F90 8304h

Figure 14-5973. USB2SS_PHY2_UTMI_UNUSED_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-12093. USB2SS_PHY2_UTMI_UNUSED_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.201 USB2SS_PHY2_UTMI_UNUSED_REG3 Register

14.7.3.2.2.201.1 USB2SS_PHY2_UTMI_UNUSED_REG3 Register (Offset = 308h) [reset = 0h]

unused

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Table 14-12094. Instance Table

Instance Name	Physical Address
USB0	0F90 8308h

Figure 14-5974. USB2SS_PHY2_UTMI_UNUSED_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R/W							
0h							

Table 14-12095. USB2SS_PHY2_UTMI_UNUSED_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R/W	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.202 USB2SS_PHY2_UTMI_REG31 Register

14.7.3.2.2.202.1 USB2SS_PHY2_UTMI_REG31 Register (Offset = 30Ch) [reset = 0h]

bist

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Table 14-12096. Instance Table

Instance Name	Physical Address
USB0	0F90 830Ch

Figure 14-5975. USB2SS_PHY2_UTMI_REG31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED						BIST_ERROR	BIST_COMPLETE
R						R	R
0h						0h	0h

Table 14-12097. USB2SS_PHY2_UTMI_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:2	UNUSED	R	0h	UNUSED Reset Source: usb2_sync_preset_n
1	BIST_ERROR	R	0h	0- BIST resulted in no Error, 1- BIST resulted in Error Reset Source: usb2_sync_preset_n
0	BIST_COMPLETE	R	0h	0- BIST is Not complete, 1- BIST is Complete Reset Source: usb2_sync_preset_n

14.7.3.2.2.203 USB2SS_PHY2_UTMI_REG32 Register

14.7.3.2.2.203.1 USB2SS_PHY2_UTMI_REG32 Register (Offset = 310h) [reset = 0h]

bist error count

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Table 14-12098. Instance Table

Instance Name	Physical Address
USB0	0F90 8310h

Figure 14-5976. USB2SS_PHY2_UTMI_REG32 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_ERR_COUNT							
R							
0h							

Table 14-12099. USB2SS_PHY2_UTMI_REG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BIST_ERR_COUNT	R	0h	00000000 Number of bytes that resulted in error while running BIST Reset Source: usb2_sync_preset_n

14.7.3.2.2.204 USB2SS_PHY2_UTMI_REG33 Register

14.7.3.2.2.204.1 USB2SS_PHY2_UTMI_REG33 Register (Offset = 314h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12100. Instance Table

Instance Name	Physical Address
USB0	0F90 8314h

Figure 14-5977. USB2SS_PHY2_UTMI_REG33 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BG_POWERGOOD	AFE_HSRX_DIFF_DATA	HSRX_EN	HSRX_SAMPLER_ENABLE	CHIRP_MODE_EN	HSTX_EN	HSTX_EN_DELAYED	HSTX_BOOST_DEAMP_OFF
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12101. USB2SS_PHY2_UTMI_REG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	BG_POWERGOOD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	AFE_HSRX_DIFF_DATA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	HSRX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	HSRX_SAMPLER_ENABLE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	CHIRP_MODE_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	HSTX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12101. USB2SS_PHY2_UTMI_REG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HSTX_EN_DELAYED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HSTX_BOOST_DEAMP_OFF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.205 USB2SS_PHY2_UTMI_REG34 Register

14.7.3.2.2.205.1 USB2SS_PHY2_UTMI_REG34 Register (Offset = 318h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12102. Instance Table

Instance Name	Physical Address
USB0	0F90 8318h

Figure 14-5978. USB2SS_PHY2_UTMI_REG34 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_DPRPU1_EN	O_DMRPU1_EN	O_DPRPU2_EN	O_DMRPU2_EN	O_DPRPD_EN	O_DMRPD_EN	O_OTGC_ID_PULLUP_EN	O_FS_EDGE_SEL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12103. USB2SS_PHY2_UTMI_REG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_DPRPU1_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_DMRPU1_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_DPRPU2_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_DMRPU2_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_DPRPD_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_DMRPD_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12103. USB2SS_PHY2_UTMI_REG34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	O_OTGC_ID_PULLUP_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_FS_EDGE_SEL	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.206 USB2SS_PHY2_UTMI_REG35 Register

14.7.3.2.2.206.1 USB2SS_PHY2_UTMI_REG35 Register (Offset = 31Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12104. Instance Table

Instance Name	Physical Address
USB0	0F90 831Ch

Figure 14-5979. USB2SS_PHY2_UTMI_REG35 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
I_AFE_LSFSRX_ANA	O_LSFSTX_EN	O_LSFSDRV_EN	O_LSFS_DDI	O_ASSERT_SEZERO	O_LSFSRX_EN	O_SERX_EN	O_SERX_BIAS_EN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12105. USB2SS_PHY2_UTMI_REG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	I_AFE_LSFSRX_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_LSFSTX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_LSFSDRV_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_LSFS_DDI	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_ASSERT_SEZERO	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_LSFSRX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12105. USB2SS_PHY2_UTMI_REG35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	O_SERX_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_SERX_BIAS_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.207 USB2SS_PHY2_UTMI_REG36 Register

14.7.3.2.2.207.1 USB2SS_PHY2_UTMI_REG36 Register (Offset = 320h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12106. Instance Table

Instance Name	Physical Address
USB0	0F90 8320h

Figure 14-5980. USB2SS_PHY2_UTMI_REG36 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
O_PLL_PSO	O_PLL_PSO_DELAY	O_PLL_PD	O_PLL_IPDIV				
R	R	R	R				
0h	0h	0h	0h				

Table 14-12107. USB2SS_PHY2_UTMI_REG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_PLL_PSO	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_PLL_PSO_DELAY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_PLL_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	O_PLL_IPDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.208 USB2SS_PHY2_UTMI_REG37 Register

14.7.3.2.2.208.1 USB2SS_PHY2_UTMI_REG37 Register (Offset = 324h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12108. Instance Table

Instance Name	Physical Address
USB0	0F90 8324h

Figure 14-5981. USB2SS_PHY2_UTMI_REG37 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">O_PLL_FBDIV_VALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12109. USB2SS_PHY2_UTMI_REG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	O_PLL_FBDIV_VALUE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.209 USB2SS_PHY2_UTMI_REG38 Register

14.7.3.2.2.209.1 USB2SS_PHY2_UTMI_REG38 Register (Offset = 328h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12110. Instance Table

Instance Name	**Physical Address**
USB0	0F90 8328h

Figure 14-5982. USB2SS_PHY2_UTMI_REG38 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
O_PLL_STANDBY	O_PLL_LDO_CORE_EN	O_PLL_LDO_REF_EN	O_AFE_SUSPENDM	O_OTGC_VBUSVALID_EN	O_OTGC_ABSVALID_EN	O_AFE_CLIPPER_EN	O_PLL_LDO_ISOLATION_CNTRL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12111. USB2SS_PHY2_UTMI_REG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	O_PLL_STANDBY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	O_PLL_LDO_CORE_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_PLL_LDO_REF_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_AFE_SUSPENDM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	O_OTGC_VBUSVALID_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_OTGC_ABSVALID_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12111. USB2SS_PHY2_UTMI_REG38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	O_AFE_CLIPPER_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_PLL_LDO_ISOLATION_CNTRL	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.210 USB2SS_PHY2_UTMI_REG39 Register

14.7.3.2.2.210.1 USB2SS_PHY2_UTMI_REG39 Register (Offset = 32Ch) [reset = 0h]

unused

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Table 14-12112. Instance Table

Instance Name	Physical Address
USB0	0F90 832Ch

Figure 14-5983. USB2SS_PHY2_UTMI_REG39 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-12113. USB2SS_PHY2_UTMI_REG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.211 USB2SS_PHY2_UTMI_REG40 Register

14.7.3.2.2.211.1 USB2SS_PHY2_UTMI_REG40 Register (Offset = 330h) [reset = 0h]

unused

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Table 14-12114. Instance Table

Instance Name	Physical Address
USB0	0F90 8330h

Figure 14-5984. USB2SS_PHY2_UTMI_REG40 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-12115. USB2SS_PHY2_UTMI_REG40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.212 USB2SS_PHY2_UTMI_REG41 Register

14.7.3.2.2.212.1 USB2SS_PHY2_UTMI_REG41 Register (Offset = 334h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12116. Instance Table

Instance Name	Physical Address
USB0	0F90 8334h

Figure 14-5985. USB2SS_PHY2_UTMI_REG41 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>I_TED_SQUELCH_ANA</td><td>I_USB2_RESCAL_CALIB_DONE</td><td colspan="6">HS_CALIB_CODE</td></tr>
<tr><td>R</td><td>R</td><td colspan="6">R</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-12117. USB2SS_PHY2_UTMI_REG41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	I_TED_SQUELCH_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	I_USB2_RESCAL_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	HS_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.213 USB2SS_PHY2_UTMI_REG42 Register

14.7.3.2.2.213.1 USB2SS_PHY2_UTMI_REG42 Register (Offset = 338h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12118. Instance Table

Instance Name	Physical Address
USB0	0F90 8338h

Figure 14-5986. USB2SS_PHY2_UTMI_REG42 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS_SOF	ALL_CALIB_DONE	FS_CALIB_CODE					
R	R	R					
0h	0h	0h					

Table 14-12119. USB2SS_PHY2_UTMI_REG42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	HS_SOF	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	ALL_CALIB_DONE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	FS_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.214 USB2SS_PHY2_UTMI_REG43 Register

14.7.3.2.2.214.1 USB2SS_PHY2_UTMI_REG43 Register (Offset = 33Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12120. Instance Table

Instance Name	Physical Address
USB0	0F90 833Ch

Figure 14-5987. USB2SS_PHY2_UTMI_REG43 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LS_MODE	FS_MODE_PRE	BC_CALIB_CODE					
R	R	R					
0h	0h	0h					

Table 14-12121. USB2SS_PHY2_UTMI_REG43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LS_MODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	FS_MODE_PRE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	BC_CALIB_CODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.215 USB2SS_PHY2_UTMI_REG44 Register

14.7.3.2.2.215.1 USB2SS_PHY2_UTMI_REG44 Register (Offset = 340h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12122. Instance Table

Instance Name	Physical Address
USB0	0F90 8340h

Figure 14-5988. USB2SS_PHY2_UTMI_REG44 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RSTN_REFCLOCK	RSTN_HS_CLOCK	RSTN_HS_TX_CLOCK	RSTN_BYTE_CLOCK	RSTN_SIECLOCK	RSTN_CLKDIV	RSTN_CALIB_CLKDIV	UDC_RSTN_CDR_ASYNC
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12123. USB2SS_PHY2_UTMI_REG44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RSTN_REFCLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RSTN_HS_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RSTN_HS_TX_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RSTN_BYTE_CLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RSTN_SIECLOCK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RSTN_CLKDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12123. USB2SS_PHY2_UTMI_REG44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RSTN_CALIB_CLKDIV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	UDC_RSTN_CDR_ASYNC	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.216 USB2SS_PHY2_UTMI_REG45 Register

14.7.3.2.2.216.1 USB2SS_PHY2_UTMI_REG45 Register (Offset = 344h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12124. Instance Table

Instance Name	Physical Address
USB0	0F90 8344h

Figure 14-5989. USB2SS_PHY2_UTMI_REG45 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UDC_CALIB_RSTN	UDC_APB_RSTN	O_RSTN_CDR_ASYNC	O_PLL_CALIB_RSTN	BIST_MODE_RSTN	O_USB2_CALIB_RSTN	UDC_BC_CALIB_RSTN	GLOBAL_RESETN
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12125. USB2SS_PHY2_UTMI_REG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UDC_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	UDC_APB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	O_RSTN_CDR_ASYNC	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	O_PLL_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	BIST_MODE_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	O_USB2_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12125. USB2SS_PHY2_UTMI_REG45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UDC_BC_CALIB_RSTN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	GLOBAL_RESETN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.217 USB2SS_PHY2_UTMI_REG46 Register

14.7.3.2.2.217.1 USB2SS_PHY2_UTMI_REG46 Register (Offset = 348h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12126. Instance Table

Instance Name	Physical Address
USB0	0F90 8348h

Figure 14-5990. USB2SS_PHY2_UTMI_REG46 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED	RECOVERY_CNT_EN	CLEAN_LINESTATE		BC_STATE_MACHINE_STATUS			
R	R	R		R			
0h	0h	0h		0h			

Table 14-12127. USB2SS_PHY2_UTMI_REG46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n
6	RECOVERY_CNT_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:4	CLEAN_LINESTATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3:0	BC_STATE_MACHINE_STATUS	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.218 USB2SS_PHY2_UTMI_REG47 Register

14.7.3.2.2.218.1 USB2SS_PHY2_UTMI_REG47 Register (Offset = 34Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-12128. Instance Table

Instance Name	Physical Address
USB0	0F90 834Ch

Figure 14-5991. USB2SS_PHY2_UTMI_REG47 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FILTER_CNT_EN	HOST_OPMODE		DEV_OPMODE		I_DED_ANA	HS_HOSTDISCONNECT	LSFS_HOSTDISCONNECT
R	R		R		R	R	R
0h	0h		0h		0h	0h	0h

Table 14-12129. USB2SS_PHY2_UTMI_REG47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FILTER_CNT_EN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6:5	HOST_OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	DEV_OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	I_DED_ANA	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	HS_HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	LSFS_HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.219 USB2SS_PHY2_UTMI_REG48 Register

14.7.3.2.2.219.1 USB2SS_PHY2_UTMI_REG48 Register (Offset = 350h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12130. Instance Table

Instance Name	Physical Address
USB0	0F90 8350h

Figure 14-5992. USB2SS_PHY2_UTMI_REG48 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_TX_STATE		DATA_CNT_TX					
R		R					
0h		0h					

Table 14-12131. USB2SS_PHY2_UTMI_REG48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_TX_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	DATA_CNT_TX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.220 USB2SS_PHY2_UTMI_REG49 Register

14.7.3.2.2.220.1 USB2SS_PHY2_UTMI_REG49 Register (Offset = 354h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12132. Instance Table

Instance Name	Physical Address
USB0	0F90 8354h

Figure 14-5993. USB2SS_PHY2_UTMI_REG49 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BIST_RX_STATE		DATA_CNT_RX					
R		R					
0h		0h					

Table 14-12133. USB2SS_PHY2_UTMI_REG49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	BIST_RX_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5:0	DATA_CNT_RX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.221 USB2SS_PHY2_UTMI_REG50 Register

14.7.3.2.2.221.1 USB2SS_PHY2_UTMI_REG50 Register (Offset = 358h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

Return to Summary Table

Table 14-12134. Instance Table

Instance Name	Physical Address
USB0	0F90 8358h

Figure 14-5994. USB2SS_PHY2_UTMI_REG50 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BIST_TOP_STATE				INC_DATA_CNT_TX	INC_DATA_CNT_RX	O_BG_PD	O_BG_PD_BG_OK
R				R	R	R	R
0h				0h	0h	0h	0h

Table 14-12135. USB2SS_PHY2_UTMI_REG50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	BIST_TOP_STATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	INC_DATA_CNT_TX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	INC_DATA_CNT_RX	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	O_BG_PD	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	O_BG_PD_BG_OK	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.222 USB2SS_PHY2_UTMI_REG51 Register

14.7.3.2.2.222.1 USB2SS_PHY2_UTMI_REG51 Register (Offset = 35Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12136. Instance Table

Instance Name	Physical Address
USB0	0F90 835Ch

Figure 14-5995. USB2SS_PHY2_UTMI_REG51 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
POWERDOWN		RESET	SUSPENDM	TERMSELECT	DATABUS16_8	DPPULLDOWN	DMPULLDOWN
R		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-12137. USB2SS_PHY2_UTMI_REG51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	POWERDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RESET	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	SUSPENDM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	TERMSELECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	DATABUS16_8	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	DPPULLDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12137. USB2SS_PHY2_UTMI_REG51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMPULLDOWN	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.223 USB2SS_PHY2_UTMI_REG52 Register

14.7.3.2.2.223.1 USB2SS_PHY2_UTMI_REG52 Register (Offset = 360h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12138. Instance Table

Instance Name	Physical Address
USB0	0F90 8360h

Figure 14-5996. USB2SS_PHY2_UTMI_REG52 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
LANE_REVERSE	TXBITSTUFFENABLE	TXBITSTUFFENABLEH	XCVRSELECT		LINESTATE		HOSTDISCONNECT
R	R	R	R		R		R
0h	0h	0h	0h		0h		0h

Table 14-12139. USB2SS_PHY2_UTMI_REG52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LANE_REVERSE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TXBITSTUFFENABLE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TXBITSTUFFENABLEH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:3	XCVRSELECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2:1	LINESTATE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
0	HOSTDISCONNECT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.224 USB2SS_PHY2_UTMI_REG53 Register

14.7.3.2.2.224.1 USB2SS_PHY2_UTMI_REG53 Register (Offset = 364h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12140. Instance Table

Instance Name	Physical Address
USB0	0F90 8364h

Figure 14-5997. USB2SS_PHY2_UTMI_REG53 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FSLSSERIALMODE	TX_ENABLE_N	TX_DAT	TX_SE0	SLEEPM	UNUSED	OPMODE	
R	R	R	R	R	R	R	
0h	0h	0h	0h	0h	0h	0h	

Table 14-12141. USB2SS_PHY2_UTMI_REG53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FSLSSERIALMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TX_ENABLE_N	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TX_DAT	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	TX_SE0	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	SLEEPM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12141. USB2SS_PHY2_UTMI_REG53 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	OPMODE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.225 USB2SS_PHY2_UTMI_REG54 Register

14.7.3.2.2.225.1 USB2SS_PHY2_UTMI_REG54 Register (Offset = 368h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12142. Instance Table

Instance Name	Physical Address
USB0	0F90 8368h

Figure 14-5998. USB2SS_PHY2_UTMI_REG54 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_DP	RX_DM	RX_RCV	UNUSED				
R	R	R	R				
0h	0h	0h	0h				

Table 14-12143. USB2SS_PHY2_UTMI_REG54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RX_DP	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	RX_DM	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	RX_RCV	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4:0	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.226 USB2SS_PHY2_UTMI_REG55 Register

14.7.3.2.2.226.1 USB2SS_PHY2_UTMI_REG55 Register (Offset = 36Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12144. Instance Table

Instance Name	Physical Address
USB0	0F90 836Ch

Figure 14-5999. USB2SS_PHY2_UTMI_REG55 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TXVALIDH	TXVALID	TXREADY	RXVALIDH	RXVALID	RXACTIVE	RXERROR	UNUSED
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12145. USB2SS_PHY2_UTMI_REG55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	TXVALIDH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
6	TXVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
5	TXREADY	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
4	RXVALIDH	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
3	RXVALID	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
2	RXACTIVE	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n
1	RXERROR	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

Table 14-12145. USB2SS_PHY2_UTMI_REG55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	UNUSED	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.227 USB2SS_PHY2_UTMI_REG56 Register

14.7.3.2.2.227.1 USB2SS_PHY2_UTMI_REG56 Register (Offset = 370h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12146. Instance Table

Instance Name	Physical Address
USB0	0F90 8370h

Figure 14-6000. USB2SS_PHY2_UTMI_REG56 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAIN_UPPER							
R							
0h							

Table 14-12147. USB2SS_PHY2_UTMI_REG56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAIN_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.228 USB2SS_PHY2_UTMI_REG57 Register

14.7.3.2.2.228.1 USB2SS_PHY2_UTMI_REG57 Register (Offset = 374h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12148. Instance Table

Instance Name	Physical Address
USB0	0F90 8374h

Figure 14-6001. USB2SS_PHY2_UTMI_REG57 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAIN_LOWER							
R							
0h							

Table 14-12149. USB2SS_PHY2_UTMI_REG57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAIN_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.229 USB2SS_PHY2_UTMI_REG58 Register

14.7.3.2.2.229.1 USB2SS_PHY2_UTMI_REG58 Register (Offset = 378h) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12150. Instance Table

Instance Name	Physical Address
USB0	0F90 8378h

Figure 14-6002. USB2SS_PHY2_UTMI_REG58 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAOUT_UPPER							
R							
0h							

Table 14-12151. USB2SS_PHY2_UTMI_REG58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAOUT_UPPER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.230 USB2SS_PHY2_UTMI_REG59 Register

14.7.3.2.2.230.1 USB2SS_PHY2_UTMI_REG59 Register (Offset = 37Ch) [reset = 0h]

This is a reserved register or field. It should not be written or read, and the value should be ignored.

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Table 14-12152. Instance Table

Instance Name	Physical Address
USB0	0F90 837Ch

Figure 14-6003. USB2SS_PHY2_UTMI_REG59 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATAOUT_LOWER							
R							
0h							

Table 14-12153. USB2SS_PHY2_UTMI_REG59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATAOUT_LOWER	R	0h	This is a reserved register or field. It should not be written or read, and the value should be ignored. Reset Source: usb2_sync_preset_n

14.7.3.2.2.231 USB2SS_PHY2_UTMI_UNUSED_REG6 Register

14.7.3.2.2.231.1 USB2SS_PHY2_UTMI_UNUSED_REG6 Register (Offset = 380h) [reset = 0h]

UNUSED

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Table 14-12154. Instance Table

Instance Name	Physical Address
USB0	0F90 8380h

Figure 14-6004. USB2SS_PHY2_UTMI_UNUSED_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-12155. USB2SS_PHY2_UTMI_UNUSED_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.232 USB2SS_PHY2_UTMI_UNUSED_REG7 Register

14.7.3.2.2.232.1 USB2SS_PHY2_UTMI_UNUSED_REG7 Register (Offset = 384h) [reset = 0h]

UNUSED

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Table 14-12156. Instance Table

Instance Name	Physical Address
USB0	0F90 8384h

Figure 14-6005. USB2SS_PHY2_UTMI_UNUSED_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
UNUSED							
R							
0h							

Table 14-12157. USB2SS_PHY2_UTMI_UNUSED_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	UNUSED	R	0h	unused Reset Source: usb2_sync_preset_n

14.7.3.2.2.233 ECC_AGGR_REV Register

14.7.3.2.2.233.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-12158. Instance Table

Instance Name	Physical Address
USB0	0F98 0000h

Figure 14-6006. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-12159. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.3.2.2.234 ECC_AGGR_VECTOR Register

14.7.3.2.2.234.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12160. Instance Table

Instance Name	Physical Address
USB0	0F98 0008h

Figure 14-6007. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-12161. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.3.2.2.235 ECC_AGGR_STAT Register

14.7.3.2.2.235.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 2h]

Misc Status

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Table 14-12162. Instance Table

Instance Name	Physical Address
USB0	0F98 000Ch

Figure 14-6008. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-12163. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	2h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.3.2.2.236 ECC_AGGR_RESERVED_SVBUS_J Register

14.7.3.2.2.236.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-12164. Instance Table

Instance Name	Physical Address
USB0	0F98 0010h + formula

Figure 14-6009. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-12165. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.3.2.2.237 ECC_AGGR_SEC_EOI_REG Register

14.7.3.2.2.237.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-12166. Instance Table

Instance Name	Physical Address
USB0	0F98 003Ch

Figure 14-6010. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12167. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.3.2.2.238 ECC_AGGR_SEC_STATUS_REG0 Register

14.7.3.2.2.238.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12168. Instance Table

Instance Name	Physical Address
USB0	0F98 0040h

Figure 14-6011. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_PEND	RAMECC_PEND
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12169. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for mem_ctrl_ram0_pend
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.7.3.2.2.239 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.7.3.2.2.239.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12170. Instance Table

Instance Name	Physical Address
USB0	0F98 0080h

Figure 14-6012. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_ENABLE_SET	RAMECC_ENABLE_SET
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12171. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_ctrl_ram0_pend
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.7.3.2.2.240 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.7.3.2.2.240.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12172. Instance Table

Instance Name	Physical Address
USB0	0F98 00C0h

Figure 14-6013. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_ENABLE_CLR	RAMECC_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12173. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_ctrl_ram0_pend
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.7.3.2.2.241 ECC_AGGR_DED_EOI_REG Register

14.7.3.2.2.241.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-12174. Instance Table

Instance Name	Physical Address
USB0	0F98 013Ch

Figure 14-6014. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12175. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.3.2.2.242 ECC_AGGR_DED_STATUS_REG0 Register

14.7.3.2.2.242.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12176. Instance Table

Instance Name	Physical Address
USB0	0F98 0140h

Figure 14-6015. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_PEND	RAMECC_PEND
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12177. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for mem_ctrl_ram0_pend
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.7.3.2.2.243 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.7.3.2.2.243.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12178. Instance Table

Instance Name	Physical Address
USB0	0F98 0180h

Figure 14-6016. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>MEM_CTRL_RAM0_ENABLE_SET</td><td>RAMECC_ENABLE_SET</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12179. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_ctrl_ram0_pend
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.7.3.2.2.244 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.7.3.2.2.244.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12180. Instance Table

Instance Name	Physical Address
USB0	0F98 01C0h

Figure 14-6017. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_CTRL_RAM0_ENABLE_CLR	RAMECC_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12181. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_CTRL_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_ctrl_ram0_pend
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.7.3.2.2.245 ECC_AGGR_AGGR_ENABLE_SET Register

14.7.3.2.2.245.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12182. Instance Table

Instance Name	Physical Address
USB0	0F98 0200h

Figure 14-6018. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12183. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.3.2.2.246 ECC_AGGR_AGGR_ENABLE_CLR Register

14.7.3.2.2.246.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12184. Instance Table

Instance Name	Physical Address
USB0	0F98 0204h

Figure 14-6019. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12185. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.3.2.2.247 ECC_AGGR_AGGR_STATUS_SET Register

14.7.3.2.2.247.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12186. Instance Table

Instance Name	Physical Address
USB0	0F98 0208h

Figure 14-6020. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-12187. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.3.2.2.248 ECC_AGGR_AGGR_STATUS_CLR Register

14.7.3.2.2.248.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12188. Instance Table

Instance Name	Physical Address
USB0	0F98 020Ch

Figure 14-6021. ECC_AGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12189. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.3.2.2.249 USB2SS_CAP_CAPLENGTH Register

14.7.3.2.2.249.1 USB2SS_CAP_CAPLENGTH Register (Offset = 0h) [reset = 1100020h]

Capability Registers Length Host Controller Operational Registers = Base address + CAPLENGTH where CAPLENGTH is DWC_USB3_HOST_CAP_REG_LEN whose default value is 20h.

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Table 14-12190. Instance Table

Instance Name	Physical Address
USB0	3100 0000h

Figure 14-6022. USB2SS_CAP_CAPLENGTH Name Register

31	30	29	28	27	26	25	24
HCIVERSION							
R							
110h							
23	22	21	20	19	18	17	16
HCIVERSION							
R							
110h							
15	14	13	12	11	10	9	8
RESERVED_15_8							
R							
0h							
7	6	5	4	3	2	1	0
CAPLENGTH							
R							
20h							

Table 14-12191. USB2SS_CAP_CAPLENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HCIVERSION	R	110h	HC Interface Version Number [HCIVERSION] Reset Source: rst_mod_g_rst_n
15:8	RESERVED_15_8	R	0h	Reserved
7:0	CAPLENGTH	R	20h	Capability Registers Length [CAPLENGTH] Reset Source: rst_mod_g_rst_n

14.7.3.2.2.250 USB2SS_CAP_HCSPARAMS1 Register

14.7.3.2.2.250.1 USB2SS_CAP_HCSPARAMS1 Register (Offset = 4h) [reset = 1000840h]

Structural Parameters 1 Register For register definitions, refer to the xHCI specification.

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Table 14-12192. Instance Table

Instance Name	Physical Address
USB0	3100 0004h

Figure 14-6023. USB2SS_CAP_HCSPARAMS1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MAXPORTS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">RESERVED_23_19</td><td colspan="3">MAXINTRS</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">8h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MAXINTRS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MAXSLOTS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">40h</td></tr>
</table>

Table 14-12193. USB2SS_CAP_HCSPARAMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAXPORTS	R	1h	Number of Ports [MaxPorts] - Number of ports implemented is defined by the parameter [DWC_USB3_HOST_NUM_U2_ROOT_PORTS + DWC_USB3_HOST_NUM_U3_ROOT_PORTS] - Number of ports enabled is controlled by the controller input signals host_num_u2_port[3:0]+host_num_u3_port[3:0] Note: In USB 2.0-only mode, the host_num_u3_port signal is zero. Reset Source: rst_mod_g_rst_n
23:19	RESERVED_23_19	R	0h	Reserved
18:8	MAXINTRS	R	8h	Number of Interrupters [MaxIntrs] Defined by the configurable parameter DWC_USB3_HOST_NUM_INTERRUPTER_SUPT Reset Source: rst_mod_g_rst_n
7:0	MAXSLOTS	R	40h	Number of device slots [MaxSlots] Defined by configurable parameter DWC_USB3_NUM_DEVICE_SUPT Reset Source: rst_mod_g_rst_n

14.7.3.2.2.251 USB2SS_CAP_HCSPARAMS2 Register

14.7.3.2.2.251.1 USB2SS_CAP_HCSPARAMS2 Register (Offset = 8h) [reset = 140000F1h]

Structural Parameters 2 Register For register definitions, refer to the xHCI specification.

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Table 14-12194. Instance Table

Instance Name	Physical Address
USB0	3100 0008h

Figure 14-6024. USB2SS_CAP_HCSPARAMS2 Name Register

31	30	29	28	27	26	25	24
MAXSCRATCHPADBUFS					SPR	MAXSCRATCHPADBUFS_HI	
R					R	R	
2h					1h	0h	
23	22	21	20	19	18	17	16
MAXSCRATCHPADBUFS_HI			RESERVED_20_8				
R			R				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED_20_8							
R							
0h							
7	6	5	4	3	2	1	0
ERSTMAX				IST			
R				R			
Fh				1h			

Table 14-12195. USB2SS_CAP_HCSPARAMS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	MAXSCRATCHPADBUFS	R	2h	Max Scratchpad Bufs Lo The value is calculated based on chosen configuration parameter values. Possible values are 1-4. Reset Source: rst_mod_g_rst_n
26	SPR	R	1h	Scratchpad Restore [SPR] Reset Source: rst_mod_g_rst_n
25:21	MAXSCRATCHPADBUFS_HI	R	0h	Max Scratchpad Bufs HI The controller automatically updates this field. Reset Source: rst_mod_g_rst_n
20:8	RESERVED_20_8	R	0h	Reserved
7:4	ERSTMAX	R	Fh	Event Ring Segment Table Max [ERST Max] Reset Source: rst_mod_g_rst_n
3:0	IST	R	1h	Isochronous Scheduling Threshold [IST] Reset Source: rst_mod_g_rst_n

14.7.3.2.2.252 USB2SS_CAP_HCSPARAMS3 Register

14.7.3.2.2.252.1 USB2SS_CAP_HCSPARAMS3 Register (Offset = Ch) [reset = 7FF000Ah]

Structural Parameters 3 Register For register definitions, refer to the xHCI specification.

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Table 14-12196. Instance Table

Instance Name	Physical Address
USB0	3100 000Ch

Figure 14-6025. USB2SS_CAP_HCSPARAMS3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">U2_DEVICE_EXIT_LAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">U2_DEVICE_EXIT_LAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_15_8</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">U1_DEVICE_EXIT_LAT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Ah</td></tr>
</table>

Table 14-12197. USB2SS_CAP_HCSPARAMS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	U2_DEVICE_EXIT_LAT	R	7FFh	U2 Device Exit Latency Reset Source: rst_mod_g_rst_n
15:8	RESERVED_15_8	R	0h	Reserved
7:0	U1_DEVICE_EXIT_LAT	R	Ah	U1 Device Exit Latency Reset Source: rst_mod_g_rst_n

14.7.3.2.2.253 USB2SS_CAP_HCCPARAMS1 Register

14.7.3.2.2.253.1 USB2SS_CAP_HCCPARAMS1 Register (Offset = 10h) [reset = 258FE6Dh]

Capability Parameters 1 Register For register definitions, refer to the xHCI specification.

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Table 14-12198. Instance Table

Instance Name	Physical Address
USB0	3100 0010h

Figure 14-6026. USB2SS_CAP_HCCPARAMS1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">XECP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">258h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">XECP</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">258h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAXPSASIZE</td><td>CFC</td><td>SEC</td><td>SPC</td><td>PAE</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">Fh</td><td>1h</td><td>1h</td><td>1h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NSS</td><td>LTC</td><td>LHRC</td><td>PIND</td><td>PPC</td><td>CSZ</td><td>BNC</td><td>AC64</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td>0h</td><td>1h</td><td>1h</td><td>0h</td><td>1h</td><td>1h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-12199. USB2SS_CAP_HCCPARAMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XECP	R	258h	xHCI Extended Capabilities Pointer [xECP] Based on configuration, controller automatically updates it. Refer to <workspace>/src/DWC_usb3_params.v for details on DWC_USB3_HC_XECP. Reset Source: rst_mod_g_rst_n
15:12	MAXPSASIZE	R	Fh	Maximum Primary Stream Array Size [MaxPSASize] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
11	CFC	R	1h	Contiguous Frame ID Capability [CFC] Reset Source: rst_mod_g_rst_n
10	SEC	R	1h	Stopped EDLTA Capability [SEC] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
9	SPC	R	1h	Short Packet Capability [SPC] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
8	PAE	R	0h	Parse All Event Data [PAE] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-12199. USB2SS_CAP_HCCPARAMS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	NSS	R	0h	No Secondary SID Support [NSS] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
6	LTC	R	1h	Latency Tolerance Messaging Capability [LTC] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
5	LHRC	R	1h	Light HC Reset Capability For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
4	PIND	R	0h	Port Indicators [PIND] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
3	PPC	R	1h	Port Power Control For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	CSZ	R	1h	Context Size [CSZ] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1	BNC	R	0h	BW Negotiation Capability [BNC] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	AC64	R	1h	64-bit Addressing Capability [AC64] For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.254 USB2SS_CAP_DBOFF Register

14.7.3.2.2.254.1 USB2SS_CAP_DBOFF Register (Offset = 14h) [reset = 560h]

Doorbell Offset Register For register definitions, refer to the xHCI specification.

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Table 14-12200. Instance Table

Instance Name	Physical Address
USB0	3100 0014h

Figure 14-6027. USB2SS_CAP_DBOFF Name Register

31	30	29	28	27	26	25	24
DOORBELL_ARRAY_OFFSET							
R							
158h							
23	22	21	20	19	18	17	16
DOORBELL_ARRAY_OFFSET							
R							
158h							
15	14	13	12	11	10	9	8
DOORBELL_ARRAY_OFFSET							
R							
158h							
7	6	5	4	3	2	1	0
DOORBELL_ARRAY_OFFSET						RESERVED_1_0	
R						R	
158h						0h	

Table 14-12201. USB2SS_CAP_DBOFF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	DOORBELL_ARRAY_OFFSET	R	158h	Doorbell Array Offset - RO Based on configuration, the controller automatically updates it. For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1:0	RESERVED_1_0	R	0h	Reserved

14.7.3.2.2.255 USB2SS_CAP_RTSOFF Register

14.7.3.2.2.255.1 USB2SS_CAP_RTSOFF Register (Offset = 18h) [reset = 440h]

Runtime Register Space Offset Register

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Table 14-12202. Instance Table

Instance Name	Physical Address
USB0	3100 0018h

Figure 14-6028. USB2SS_CAP_RTSOFF Name Register

31	30	29	28	27	26	25	24
RUNTIME_REG_SPACE_OFFSET							
R							
22h							
23	22	21	20	19	18	17	16
RUNTIME_REG_SPACE_OFFSET							
R							
22h							
15	14	13	12	11	10	9	8
RUNTIME_REG_SPACE_OFFSET							
R							
22h							
7	6	5	4	3	2	1	0
RUNTIME_REG_SPACE_OFFSET			RESERVED_4_0				
R			R				
22h			0h				

Table 14-12203. USB2SS_CAP_RTSOFF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RUNTIME_REG_SPACE_OFFSET	R	22h	Runtime Register Space Offset Based on configuration, the controller automatically updates it. For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
4:0	RESERVED_4_0	R	0h	Reserved

14.7.3.2.2.256 USB2SS_CAP_HCCPARAMS2 Register

14.7.3.2.2.256.1 USB2SS_CAP_HCCPARAMS2 Register (Offset = 1Ch) [reset = 2Fh]

Host Controller Capability Parameters 2 For register definitions, refer to the xHCI specification.

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Table 14-12204. Instance Table

Instance Name	Physical Address
USB0	3100 001Ch

Figure 14-6029. USB2SS_CAP_HCCPARAMS2 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_6							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_6							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_6							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_6		CIC	LEC	CTC	FSC	CMC	U3C
R		R	R	R	R	R	R
0h		1h	0h	1h	1h	1h	1h

Table 14-12205. USB2SS_CAP_HCCPARAMS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_31_6	R	0h	Reserved
5	CIC	R	1h	Configuration Information Capability [CIC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
4	LEC	R	0h	Large ESIT Payload Capability [LEC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
3	CTC	R	1h	Compliance Transition Capability [CTC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	FSC	R	1h	Force Save Context Capability [FSC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1	CMC	R	1h	Configure Endpoint Command Max Exit Latency Too Large Capability [CMC] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-12205. USB2SS_CAP_HCCPARAMS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	U3C	R	1h	U3 Entry Capability [U3C] For a description of this standard USB register field, see the eXtensible Host Controller I nterface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.257 USB2SS_OPER_USBCMD Register

14.7.3.2.2.257.1 USB2SS_OPER_USBCMD Register (Offset = 0h) [reset = 0h]

USB Command Register For a description of this standard USB register field see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12206. Instance Table

Instance Name	Physical Address
USB0	3100 0020h

Figure 14-6030. USB2SS_OPER_USBCMD Name Register

31	30	29	28	27	26	25	24
RESERVED_31_14							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_14							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_31_14		CME	RESERVED_12	EU3S	EWE	CRS	CSS
R		R/W	R	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LHCRST	RESERVED_6_4			HSEE	INTE	HCRST	R_S
R/W	R			R/W	R/W	R/W	R/W
0h	0h			0h	0h	0h	0h

Table 14-12207. USB2SS_OPER_USBCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_31_14	R	0h	Reserved
13	CME	R/W	0h	CEM Enable For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
12	RESERVED_12	R	0h	Reserved
11	EU3S	R/W	0h	EU3S For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
10	EWE	R/W	0h	EWE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
9	CRS	R/W	0h	Controller Restore State This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'. Note: When read, this field always returns '0'. Reset Source: rst_mod_g_rst_n

Table 14-12207. USB2SS_OPER_USBCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CSS	R/W	0h	Controller Save State This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'. Note: When read, this field always returns '0'. Reset Source: rst_mod_g_rst_n
7	LHCRST	R/W	0h	Light Host Controller Reset For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. The following bits reset the internal logic of the host controller. Under soft reset, some CSR accesses may fail [Timeout]. - HCRST - LHCRST Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
6:4	RESERVED_6_4	R	0h	Reserved
3	HSEE	R/W	0h	HSEE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	INTE	R/W	0h	INTE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1	HCRST	R/W	0h	HCRST The following bits reset the internal logic of the host controller. Under soft reset, some CSR accesses may fail [Timeout]. - HCRST - LHCRST Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
0	R_S	R/W	0h	R_S For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Due to side-effects this reguster field is not recommended for Bit-Bash testing. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.258 USB2SS_OPER_USBSTS Register

14.7.3.2.2.258.1 USB2SS_OPER_USBSTS Register (Offset = 4h) [reset = 801h]

USB Status Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12208. Instance Table

Instance Name	Physical Address
USB0	3100 0024h

Figure 14-6031. USB2SS_OPER_USBSTS Name Register

31	30	29	28	27	26	25	24
RESERVED_31_13							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_13							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_13			HCE	CNR	SRE	RSS	SSS
R			R	R	R/W1TC	R	R
0h			0h	1h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_7_5			PCD	EINT	HSE	RESERVED_1	HCH
R			R/W1TC	R/W1TC	R/W1TC	R	R
0h			0h	0h	0h	0h	1h

Table 14-12209. USB2SS_OPER_USBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_31_13	R	0h	Reserved
12	HCE	R	0h	Host Controller Error [HCE] - RO Default = 0. '0' = No internal xHC error conditions exist and '1' = Internal xHC error condition. This flag must be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC. Refer to section 4.24.1 of the Databook for more information. Reset Source: rst_mod_g_rst_n
11	CNR	R	1h	Controller Not Ready [CNR] - RO Default = '1'. '0' = Ready and '1' = Not Ready. Software must not write to thes Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag remains cleared ['0'] until the next Chip Hardware Reset. Reset Source: rst_mod_g_rst_n
10	SRE	R/W1TC	0h	Save/Restore Error This bit is currently not supported. Reset Source: rst_mod_g_rst_n
9	RSS	R	0h	Restore State Status This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the restore process, it completes the command by setting DSTS.RSS to '0'. Reset Source: rst_mod_g_rst_n

Table 14-12209. USB2SS_OPER_USBSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SSS	R	0h	Save State Status This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to '0'. Reset Source: rst_mod_g_rst_n
7:5	RESERVED_7_5	R	0h	Reserved
4	PCD	R/W1TC	0h	Reset Value for PCD Reset Source: rst_mod_g_rst_n
3	EINT	R/W1TC	0h	Reset Value for EINT Reset Source: rst_mod_g_rst_n
2	HSE	R/W1TC	0h	HSE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.. Reset Source: rst_mod_g_rst_n
1	RESERVED_1	R	0h	Reserved
0	HCH	R	1h	HCH For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.259 USB2SS_OPER_PAGESIZE Register

14.7.3.2.2.259.1 USB2SS_OPER_PAGESIZE Register (Offset = 8h) [reset = 1h]

Page Size Register Bit Definitions Use this register to enable or disable the reporting of specific USB Device Notification Transaction Packets being received. A Notification Enable (Nx, where x = 0 to 15) flag is defined for each of the 16 possible device notification types. If a flag is set for a specific notification type, a Device Notification Event is generated when the respective notification packet is received. After reset, all notifications are disabled. Refer to section 6.4.2.7 of the Databook for more information. This register is written as a Dword. Byte writes produce undefined results.

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Table 14-12210. Instance Table

Instance Name	Physical Address
USB0	3100 0028h

Figure 14-6032. USB2SS_OPER_PAGESIZE Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
PAGE_SIZE							
R							
1h							
7	6	5	4	3	2	1	0
PAGE_SIZE							
R							
1h							

Table 14-12211. USB2SS_OPER_PAGESIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:0	PAGE_SIZE	R	1h	PAGE_SIZE Reset Source: rst_mod_g_rst_n

14.7.3.2.2.260 USB2SS_OPER_DNCTRL Register

14.7.3.2.2.260.1 USB2SS_OPER_DNCTRL Register (Offset = 14h) [reset = 0h]

Device Notification Register Bit Definitions For a description of this standard USB register field see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12212. Instance Table

Instance Name	Physical Address
USB0	3100 0034h

Figure 14-6033. USB2SS_OPER_DNCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
N0_N15							
R/W							
0h							
7	6	5	4	3	2	1	0
N0_N15							
R/W							
0h							

Table 14-12213. USB2SS_OPER_DNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:0	N0_N15	R/W	0h	N0_N15 For a description of this standard USB register field see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.261 USB2SS_OPER_CRCR_LO Register

14.7.3.2.2.261.1 USB2SS_OPER_CRCR_LO Register (Offset = 18h) [reset = 0h]

CRCR_LO For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12214. Instance Table

Instance Name	Physical Address
USB0	3100 0038h

Figure 14-6034. USB2SS_OPER_CRCR_LO Name Register

31	30	29	28	27	26	25	24
CMD_RING_PNTR							
W							
0h							
23	22	21	20	19	18	17	16
CMD_RING_PNTR							
W							
0h							
15	14	13	12	11	10	9	8
CMD_RING_PNTR							
W							
0h							
7	6	5	4	3	2	1	0
CMD_RING_PNTR		RESERVED_5_4		CRR	CA	CS	RCS
W		R		R	W	W	W
0h		0h		0h	0h	0h	0h

Table 14-12215. USB2SS_OPER_CRCR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	CMD_RING_PNTR	W	0h	CMD_RING_PNTR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
5:4	RESERVED_5_4	R	0h	Reserved
3	CRR	R	0h	CRR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	CA	W	0h	CA For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1	CS	W	0h	CS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	RCS	W	0h	RCS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.262 USB2SS_OPER_CRCR_HI Register

14.7.3.2.2.262.1 USB2SS_OPER_CRCR_HI Register (Offset = 1Ch) [reset = 0h]

CRCR_HI

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Table 14-12216. Instance Table

Instance Name	Physical Address
USB0	3100 003Ch

Figure 14-6035. USB2SS_OPER_CRCR_HI Name Register

31	30	29	28	27	26	25	24
CMD_RING_PNTR							
W							
0h							
23	22	21	20	19	18	17	16
CMD_RING_PNTR							
W							
0h							
15	14	13	12	11	10	9	8
CMD_RING_PNTR							
W							
0h							
7	6	5	4	3	2	1	0
CMD_RING_PNTR							
W							
0h							

Table 14-12217. USB2SS_OPER_CRCR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMD_RING_PNTR	W	0h	COMMAND_RING_POINTER Reading this field always returns '0'. For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.263 USB2SS_OPER_DCBAAP_LO Register

14.7.3.2.2.263.1 USB2SS_OPER_DCBAAP_LO Register (Offset = 30h) [reset = 0h]

DCBAAP_LO

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Table 14-12218. Instance Table

Instance Name	Physical Address
USB0	3100 0050h

Figure 14-6036. USB2SS_OPER_DCBAAP_LO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DEVICE_CONTEXT_BAAP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DEVICE_CONTEXT_BAAP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DEVICE_CONTEXT_BAAP</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">DEVICE_CONTEXT_BAAP</td><td colspan="6">RESERVED_5_0</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-12219. USB2SS_OPER_DCBAAP_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	DEVICE_CONTEXT_BAAP	R/W	0h	DEVICE_CONTEXT_BAAP For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
5:0	RESERVED_5_0	R	0h	Reserved

14.7.3.2.2.264 USB2SS_OPER_DCBAAP_HI Register

14.7.3.2.2.264.1 USB2SS_OPER_DCBAAP_HI Register (Offset = 34h) [reset = 0h]

DCBAAP_HI For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12220. Instance Table

Instance Name	Physical Address
USB0	3100 0054h

Figure 14-6037. USB2SS_OPER_DCBAAP_HI Name Register

31	30	29	28	27	26	25	24
DEVICE_CONTEXT_BAAP							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVICE_CONTEXT_BAAP							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVICE_CONTEXT_BAAP							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVICE_CONTEXT_BAAP							
R/W							
0h							

Table 14-12221. USB2SS_OPER_DCBAAP_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVICE_CONTEXT_BAAP	R/W	0h	DEVICE_CONTEXT_BAAP Reset Source: rst_mod_g_rst_n

14.7.3.2.2.265 USB2SS_OPER_CONFIG Register

14.7.3.2.2.265.1 USB2SS_OPER_CONFIG Register (Offset = 38h) [reset = 0h]

Configure Register Bit Definitions This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST). The initial conditions of a port are described in section 4.19 of the Databook.

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Table 14-12222. Instance Table

Instance Name	Physical Address
USB0	3100 0058h

Figure 14-6038. USB2SS_OPER_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_31_10							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_10							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_10						CIE	U3E
R						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
MAXSLOTSEN							
R/W							
0h							

Table 14-12223. USB2SS_OPER_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_31_10	R	0h	Reserved
9	CIE	R/W	0h	Configuration Information Enable For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
8	U3E	R/W	0h	U3 Entry Enable For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	MAXSLOTSEN	R/W	0h	MAXSLOTSEN For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.266 USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register

14.7.3.2.2.266.1 USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register (Offset = 0h) [reset = 2A0h]

Port Status and Control Register Bit Definitions The PORTSC Register Access fails (Timeout) if the UTMI/ULPI clock is not running or one of the following bits is asserted. - PR - ORC

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Table 14-12224. Instance Table

Instance Name	Physical Address
USB0	3100 0420h + formula

Figure 14-6039. USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Name Register

31	30	29	28	27	26	25	24
RESERVED_31	DR	RESERVED_29_28		WOE	WDE	WCE	CAS
R	R	R		R/W	R/W	R/W	R
0h	0h	0h		0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED_23	PLC	PRC	OCC	RESERVED_19	PEC	CSC	LWS
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PIC		PORTSPEED				PP	PLS
R/W		R				R/W	R/W
0h		0h				1h	5h
7	6	5	4	3	2	1	0
PLS			PR	OCA	RESERVED_2	PED	CCS
R/W			R/W1TS	R	R	R/W1TC	R
5h			0h	0h	0h	0h	0h

Table 14-12225. USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_31	R	0h	Reserved For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Programming this field with random data will cause side effect i.e. Register Access will fail [Timeout] if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.
30	DR	R	0h	Reset Value For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
29:28	RESERVED_29_28	R	0h	Reserved
27	WOE	R/W	0h	WOE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
26	WDE	R/W	0h	WDE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-12225. USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	WCE	R/W	0h	WCE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
24	CAS	R	0h	Cold Attach Status For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
23	RESERVED_23	R	0h	Reserved For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.
22	PLC	R/W1TC	0h	PLC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
21	PRC	R/W1TC	0h	PRC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Programming this field with random data will cause side effect. Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
20	OCC	R/W1TC	0h	OCC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
19	RESERVED_19	R/W1TC	0h	WRC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.
18	PEC	R/W1TC	0h	PEC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
17	CSC	R/W1TC	0h	CSC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
16	LWS	R/W	0h	LWS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:14	PIC	R/W	0h	PIC For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
13:10	PORTSPEED	R	0h	PORTSPEED For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
9	PP	R/W	1h	PP For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-12225. USB2SS_PORT_XHCI_PORT_20_PORTSC_20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:5	PLS	R/W	5h	PLS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
4	PR	R/W1TS	0h	PR set_register_field_attribute DWC_usb3_map/ DWC_usb3_block_Host_Cntrl_Port_Reg_Set/PORTSC_20_REGS/ PORTSC_20/PR VolatileMemory 1 Programming this field with random data will cause side effect. Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
3	OCA	R	0h	OCA For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2	RESERVED_2	R	0h	Reserved
1	PED	R/W1TC	0h	PED For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	CCS	R	0h	CCS For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.267 USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Register

14.7.3.2.2.267.1 USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Register (Offset = 4h) [reset = 0h]

USB3 Port Power Management Status and Control Register Bit Definitions This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST). Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

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Table 14-12226. Instance Table

Instance Name	Physical Address
USB0	3100 0424h + formula

Figure 14-6040. USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Name Register

31	30	29	28	27	26	25	24
PRTTSTCTRL				RESERVED_27_17			
R/W				R			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED_27_17							HLE
R							R/W
0h							0h
15	14	13	12	11	10	9	8
L1DSLOT							
R/W							
0h							
7	6	5	4	3	2	1	0
HIRD				RWE	L1S		
R/W				R/W	R		
0h				0h	0h		

Table 14-12227. USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRTTSTCTRL	R/W	0h	Port Test Control For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
27:17	RESERVED_27_17	R	0h	Reserved
16	HLE	R/W	0h	Port Test Control For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	L1DSLOT	R/W	0h	L1DSLOT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

Table 14-12227. USB2SS_PORT_XHCI_PORT_20_PORTPMSC_20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	HIRD	R/W	0h	Host Initiated Resume Duration [HIRD] - RW. Default = '0'. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it [the xHC] initiates an exit from L1. The HIRD value is encoded as follows: Value Description 0h 50us. [default] 1h 125us. 2h 200us. Fh 1.175 ms. The value of 0000b is interpreted as 50us. Each incrementing value up adds 75us. to the previous value. For example, 0001b is 125us, 0010b is 200us and so on. Based on this rule, the maximum value resume drive time is at encoding value 1111b which represents 1.2ms. Note that the HIRD field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 for more information on HIRD use. Refer to Section 4.1 of the USB2 LPM spec for more information on the use of the HIRD field. Reset Source: rst_mod_g_rst_n
3	RWE	R/W	0h	RWE Port Test Control For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
2:0	L1S	R	0h	L1 Status [L1S] - RO. Default = 0. This field is used by software to determine whether an L1-based suspend request [LMP transaction] was successful, specifically: Value Meaning 0 Invalid - This field is ignored by software. - 1 Success - Port successfully transitioned to L1 [ACK] - 2 Not Yet - Device is unable to enter L1 at this time [NYET] - 3 Not Supported -Device does not support L1 transitions [STALL] - 4 Timeout/Error -Device failed to respond to the LPM Transaction or an error occurred - 5-7 Reserved The value of this field is only valid when the port resides in the L0 or L1 state [PLS = '0' or '2']. Refer to section 4.23.5.1.1 for more information. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.268 USB2SS_PORT_XHCI_PORT_20_PORTLI_20 Register

14.7.3.2.2.268.1 USB2SS_PORT_XHCI_PORT_20_PORTLI_20 Register (Offset = 8h) [reset = 0h]

Port Link Info Register Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

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Table 14-12228. Instance Table

Instance Name	Physical Address
USB0	3100 0428h + formula

Figure 14-6041. USB2SS_PORT_XHCI_PORT_20_PORTLI_20 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-12229. USB2SS_PORT_XHCI_PORT_20_PORTLI_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved

14.7.3.2.2.269 USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Register

14.7.3.2.2.269.1 USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Register (Offset = Ch) [reset = 0h]

USB2 Port Hardware LPM Control Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12230. Instance Table

Instance Name	Physical Address
USB0	3100 042Ch + formula

Figure 14-6042. USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED_31_14</td><td colspan="4">HIRDD</td><td colspan="2">L1_TIMEOUT</td></tr>
<tr><td colspan="2">R</td><td colspan="4">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="4">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">L1_TIMEOUT</td><td colspan="2">HIRDM</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12231. USB2SS_PORT_XHCI_PORT_20_PORTHLPMC_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_31_14	R	0h	Reserved For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.
13:10	HIRDD	R/W	0h	PORTHLPMC_20 HIRDD Reset Source: rst_mod_g_rst_n
9:2	L1_TIMEOUT	R/W	0h	PORTHLPMC_20 L1_TIMEOUT. For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
1:0	HIRDM	R/W	0h	Host Initiated Resume Duration Mode [HIRDM] - RWS. Default = 0h. Indicates which HIRD value must be used. The following are permissible values: Value Description 0 Initiate L1 using HIRD only on timeout. [default] 1 Initiate L1 using HIRDD on timeout. If rejected by device, initiate L1 using HIRD. 3-2 Reserved. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.270 USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30 Register

14.7.3.2.2.270.1 USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30 Register (Offset = 14h) [reset = 0h]

USB3 Port Power Management Status and Control Register Bit Definitions This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST). Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

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Table 14-12232. Instance Table

Instance Name	Physical Address
USB0	3100 0434h + formula

Figure 14-6043. USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_17</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED_31_17</td><td>FLA</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">U2_TIMEOUT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">U1_TIMEOUT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12233. USB2SS_PORT_XHCI_PORT_30_PORTPMSC_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_31_17	R	0h	Reserved
16	FLA	R/W	0h	FLA For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	U2_TIMEOUT	R/W	0h	U2_TIMEOUT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	U1_TIMEOUT	R/W	0h	U1_TIMEOUT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.271 USB2SS_PORT_XHCI_PORT_30_PORTLI_30 Register

14.7.3.2.2.271.1 USB2SS_PORT_XHCI_PORT_30_PORTLI_30 Register (Offset = 18h) [reset = 0h]

Port Link Info Register Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

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Table 14-12234. Instance Table

Instance Name	Physical Address
USB0	3100 0438h + formula

Figure 14-6044. USB2SS_PORT_XHCI_PORT_30_PORTLI_30 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LINK_ERROR_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LINK_ERROR_COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12235. USB2SS_PORT_XHCI_PORT_30_PORTLI_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:0	LINK_ERROR_COUNT	R	0h	LINK_ERROR_COUNT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.272 USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30 Register

14.7.3.2.2.272.1 USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30 Register (Offset = 1Ch) [reset = 0h]

USB2 Port Hardware LPM Control Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12236. Instance Table

Instance Name	Physical Address
USB0	3100 043Ch + formula

Figure 14-6045. USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-12237. USB2SS_PORT_XHCI_PORT_30_PORTHLPMC_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0.

14.7.3.2.2.273 USB2SS_RUNTIME_MFINDEX Register

14.7.3.2.2.273.1 USB2SS_RUNTIME_MFINDEX Register (Offset = 0h) [reset = 0h]

Microframe Index Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12238. Instance Table

Instance Name	Physical Address
USB0	3100 0440h

Figure 14-6046. USB2SS_RUNTIME_MFINDEX Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_14</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED_31_14</td><td colspan="6">MICROFRAME_INDEX</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MICROFRAME_INDEX</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12239. USB2SS_RUNTIME_MFINDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED_31_14	R	0h	Reserved
13:0	MICROFRAME_INDEX	R	0h	MICROFRAME_INDEX For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.274 USB2SS_RUNTIME_RSVDZ Register

14.7.3.2.2.274.1 USB2SS_RUNTIME_RSVDZ Register (Offset = 4h) [reset = 0h]

RsvdZ For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12240. Instance Table

Instance Name	Physical Address
USB0	3100 0444h

Figure 14-6047. USB2SS_RUNTIME_RSVDZ Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-12241. USB2SS_RUNTIME_RSVDZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved

14.7.3.2.2.275 USB2SS_INTR_XHCI_INTR_IMAN_J Register

14.7.3.2.2.275.1 USB2SS_INTR_XHCI_INTR_IMAN_J Register (Offset = 0h) [reset = 0h]

Interrupter Management Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12242. Instance Table

Instance Name	Physical Address
USB0	3100 0460h + formula

Figure 14-6048. USB2SS_INTR_XHCI_INTR_IMAN_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_31_2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED_31_2</td><td>IE</td><td>IP</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12243. USB2SS_INTR_XHCI_INTR_IMAN_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_31_2	R	0h	Reserved
1	IE	R/W	0h	IE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
0	IP	R/W1TC	0h	IP Interrupt Pending For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.276 USB2SS_INTR_XHCI_INTR_IMOD_J Register

14.7.3.2.2.276.1 USB2SS_INTR_XHCI_INTR_IMOD_J Register (Offset = 4h) [reset = FA0h]

Interrupter Moderation Register The software may use this register to pace (or even out) the delivery of interrupts to the host CPU. This register provides a guaranteed inter-interrupt delay between interrupts asserted by the xHC, regardless of USB traffic conditions. To independently validate configuration settings, software may use the following algorithm to convert the inter-interrupt Interval value to the common 'interrupts/sec' performance metric.

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Table 14-12244. Instance Table

Instance Name	Physical Address
USB0	3100 0464h + formula

Figure 14-6049. USB2SS_INTR_XHCI_INTR_IMOD_j Name Register

31	30	29	28	27	26	25	24
IMODC							
R/W							
0h							
23	22	21	20	19	18	17	16
IMODC							
R/W							
0h							
15	14	13	12	11	10	9	8
IMODI							
R/W							
FA0h							
7	6	5	4	3	2	1	0
IMODI							
R/W							
FA0h							

Table 14-12245. USB2SS_INTR_XHCI_INTR_IMOD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IMODC	R/W	0h	Interrupt Moderation Counter [IMODC] - RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to '0', and stops. The associated interrupt is signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	IMODI	R/W	FA0h	Interrupt Moderation Interval [IMODI] - RW. Default = '4000' [~1ms]. Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic and interrupts is generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.277 USB2SS_INTR_XHCI_INTR_ERSTSZ_J Register

14.7.3.2.2.277.1 USB2SS_INTR_XHCI_INTR_ERSTSZ_J Register (Offset = 8h) [reset = 0h]

Event Ring Segment Table Size Register Bit Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12246. Instance Table

Instance Name	Physical Address
USB0	3100 0468h + formula

Figure 14-6050. USB2SS_INTR_XHCI_INTR_ERSTSZ_j Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
ERS_TABLE_SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
ERS_TABLE_SIZE							
R/W							
0h							

Table 14-12247. USB2SS_INTR_XHCI_INTR_ERSTSZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:0	ERS_TABLE_SIZE	R/W	0h	ERS_TABLE_SIZE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.278 USB2SS_INTR_XHCI_INTR_RSVDP_J Register

14.7.3.2.2.278.1 USB2SS_INTR_XHCI_INTR_RSVDP_J Register (Offset = Ch) [reset = 0h]

RsvdP

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Table 14-12248. Instance Table

Instance Name	Physical Address
USB0	3100 046Ch + formula

Figure 14-6051. USB2SS_INTR_XHCI_INTR_RSVDP_j Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-12249. USB2SS_INTR_XHCI_INTR_RSVDP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved

14.7.3.2.2.279 USB2SS_INTR_XHCI_INTR_ERSTBA_LO_J Register

14.7.3.2.2.279.1 USB2SS_INTR_XHCI_INTR_ERSTBA_LO_J Register (Offset = 10h) [reset = 0h]

ERSTBA_LO

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Table 14-12250. Instance Table

Instance Name	Physical Address
USB0	3100 0470h + formula

Figure 14-6052. USB2SS_INTR_XHCI_INTR_ERSTBA_LO_j Name Register

31	30	29	28	27	26	25	24
ERS_TABLE_BAR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ERS_TABLE_BAR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ERS_TABLE_BAR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERS_TABLE_BAR		RESERVED_5_0					
R/W		R					
0h		0h					

Table 14-12251. USB2SS_INTR_XHCI_INTR_ERSTBA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	ERS_TABLE_BAR	R/W	0h	ERS_TABLE_BAR Reset Source: rst_mod_g_rst_n
5:0	RESERVED_5_0	R	0h	Reserved

14.7.3.2.2.280 USB2SS_INTR_XHCI_INTR_ERSTBA_HI_J Register

14.7.3.2.2.280.1 USB2SS_INTR_XHCI_INTR_ERSTBA_HI_J Register (Offset = 14h) [reset = 0h]

ERSTBA_HI

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Table 14-12252. Instance Table

Instance Name	Physical Address
USB0	3100 0474h + formula

Figure 14-6053. USB2SS_INTR_XHCI_INTR_ERSTBA_HI_j Name Register

31	30	29	28	27	26	25	24
ERS_TABLE_BAR							
R/W							
0h							
23	22	21	20	19	18	17	16
ERS_TABLE_BAR							
R/W							
0h							
15	14	13	12	11	10	9	8
ERS_TABLE_BAR							
R/W							
0h							
7	6	5	4	3	2	1	0
ERS_TABLE_BAR							
R/W							
0h							

Table 14-12253. USB2SS_INTR_XHCI_INTR_ERSTBA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERS_TABLE_BAR	R/W	0h	ERS_TABLE_BAR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.281 USB2SS_INTR_XHCI_INTR_ERDP_LO_J Register

14.7.3.2.2.281.1 USB2SS_INTR_XHCI_INTR_ERDP_LO_J Register (Offset = 18h) [reset = 0h]

ERDP_LO For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12254. Instance Table

Instance Name	Physical Address
USB0	3100 0478h + formula

Figure 14-6054. USB2SS_INTR_XHCI_INTR_ERDP_LO_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ERD_PNTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ERD_PNTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ERD_PNTR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ERD_PNTR</td><td>EHB</td><td colspan="3">DESI</td></tr>
<tr><td colspan="4">R/W</td><td>R/W1TC</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-12255. USB2SS_INTR_XHCI_INTR_ERDP_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	ERD_PNTR	R/W	0h	ERD_PNTR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
3	EHB	R/W1TC	0h	HC OS Owned SemaphoreERS_TABLE_SIZEHC BIOS Owned Semaphore USB SMI Enable SMI on Host System Error Enable - SMI on OS Ownership Enable - SMI on PCI Command Enable - SMI on BAR Enable - SMI on Event Interrupt - SMI on Host System Error - SMI on OS Ownership Change - SMI on PCI Command - SMI on BAR - Compatible Port Count - HC OS Owned Semaphore - HC BIOS Owned Semaphore - USB SMI Enable - SMI on Host System Error Enable - SMI on OS Ownership Enable - SMI on PCI Command Enable - SMI on BAR Enable - SMI on Event Interrupt - SMI on Host System Error - SMI on OS Ownership Change - SMI on PCI Command - SMI on BAR - Compatible Port Count Reset Source: rst_mod_g_rst_n
2:0	DESI	R/W	0h	DESI - For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.282 USB2SS_INTR_XHCI_INTR_ERDP_HI_J Register

14.7.3.2.2.282.1 USB2SS_INTR_XHCI_INTR_ERDP_HI_J Register (Offset = 1Ch) [reset = 0h]

ERDP_HI

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Table 14-12256. Instance Table

Instance Name	Physical Address
USB0	3100 047Ch + formula

Figure 14-6055. USB2SS_INTR_XHCI_INTR_ERDP_HI_j Name Register

31	30	29	28	27	26	25	24
ERD_PNTR							
R/W							
0h							
23	22	21	20	19	18	17	16
ERD_PNTR							
R/W							
0h							
15	14	13	12	11	10	9	8
ERD_PNTR							
R/W							
0h							
7	6	5	4	3	2	1	0
ERD_PNTR							
R/W							
0h							

Table 14-12257. USB2SS_INTR_XHCI_INTR_ERDP_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ERD_PNTR	R/W	0h	ERD_PNTR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.283 USB2SS_DBARR_XHCI_DB_DB_J Register

14.7.3.2.2.283.1 USB2SS_DBARR_XHCI_DB_DB_J Register (Offset = 0h) [reset = 0h]

Doorbell Register Bit Field Definitions For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0. Programming this field with random data will cause side effect i.e. Register Access will fail (Timeout) if the pipe clock is not running or reset is asserted . Bit Bash register testing is not recommended.

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Table 14-12258. Instance Table

Instance Name	Physical Address
USB0	3100 0560h + formula

Figure 14-6056. USB2SS_DBARR_XHCI_DB_DB_j Name Register

31	30	29	28	27	26	25	24
DB_STREAM_ID							
R/W							
0h							
23	22	21	20	19	18	17	16
DB_STREAM_ID							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_15_8							
R							
0h							
7	6	5	4	3	2	1	0
DB_TARGET							
R/W							
0h							

Table 14-12259. USB2SS_DBARR_XHCI_DB_DB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DB_STREAM_ID	R/W	0h	DB_STREAM_ID For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	RESERVED_15_8	R	0h	Reserved
7:0	DB_TARGET	R/W	0h	DB_TARGET For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.284 USB2SS_EXTCAP_USBLEGSUP Register

14.7.3.2.2.284.1 USB2SS_EXTCAP_USBLEGSUP Register (Offset = 0h) [reset = 401h]

USBLEGSUP

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Table 14-12260. Instance Table

Instance Name	Physical Address
USB0	3100 0960h

Figure 14-6057. USB2SS_EXTCAP_USBLEGSUP Name Register

31	30	29	28	27	26	25	24
RESERVED_31_25							HC_OS_OWNED
R							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_23_17							HC_BIOS_OWNED
R							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NEXT_CAPABILITY_POINTER							
R							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAPABILITY_ID							
R							
1h							

Table 14-12261. USB2SS_EXTCAP_USBLEGSUP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED_31_25	R	0h	Reserved
24	HC_OS_OWNED	R/W	0h	HC_OS_OWNED SEMAPHORE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
23:17	RESERVED_23_17	R	0h	Reserved
16	HC_BIOS_OWNED	R/W	0h	HC_BIOS_OWNED SEMAPHORE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	NEXT_CAPABILITY_POINTER	R	4h	NEXT_CAPABILITY_POINTER For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	CAPABILITY_ID	R	1h	CAPABILITY_ID set_register_field_attribute DWC_usb3_map/ DWC_usb3_block_HC_Extended_Capability_Register/ USBLEGSUP/CAPABILITY_ID RegisterResetValue 0x1 For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.285 USB2SS_EXTCAP_USBLEGCTLSTS Register

14.7.3.2.2.285.1 USB2SS_EXTCAP_USBLEGCTLSTS Register (Offset = 4h) [reset = 0h]

USBLEGCTLSTS

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Table 14-12262. Instance Table

Instance Name	Physical Address
USB0	3100 0964h

Figure 14-6058. USB2SS_EXTCAP_USBLEGCTLSTS Name Register

31	30	29	28	27	26	25	24
SMI_ON_BAR	SMI_ON_PCI	SMI_ON_OS	RESERVED_28_21				
R/W1TC	R/W1TC	R/W1TC	R				
0h	0h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_28_21			SMI_ON_HOST	RESERVED_19_17			SMI_ON_EVENT
R			R	R			R
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SMI_ON_BAR_E	SMI_ON_PCI_E	SMI_ON_OS_E	RESERVED_12_5				
R/W	R/W	R/W	R				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_12_5			SMI_ON_HOST_E	RESERVED_3_1			USB_SMI_ENABLE
R			R/W	R			R/W
0h			0h	0h			0h

Table 14-12263. USB2SS_EXTCAP_USBLEGCTLSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SMI_ON_BAR	R/W1TC	0h	SMI_ON_BAR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
30	SMI_ON_PCI	R/W1TC	0h	SMI_ON_PCI COMMAND For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
29	SMI_ON_OS	R/W1TC	0h	SMI_ON_OS OWNERSHIP CHANGE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
28:21	RESERVED_28_21	R	0h	Reserved
20	SMI_ON_HOST	R	0h	SMI_ON_HOST SYSTEM ERROR For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
19:17	RESERVED_19_17	R	0h	Reserved

Table 14-12263. USB2SS_EXTCAP_USBLEGCTLSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SMI_ON_EVENT	R	0h	SMI_ON_EVENT INTERRUPT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15	SMI_ON_BAR_E	R/W	0h	SMI_ON_BAR ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
14	SMI_ON_PCI_E	R/W	0h	SMI_ON_PCI COMMAND ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
13	SMI_ON_OS_E	R/W	0h	SMI_ON_OS OWNERSHIP ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
12:5	RESERVED_12_5	R	0h	Reserved
4	SMI_ON_HOST_E	R/W	0h	SMI_ON_HOST SYSTEM ERROR ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
3:1	RESERVED_3_1	R	0h	Reserved
0	USB_SMI_ENABLE	R/W	0h	USB_SMI_ENABLE For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.286 USB2SS_SUPPRTCAP2_SUPTPRT2_DW0 Register

14.7.3.2.2.286.1 USB2SS_SUPPRTCAP2_SUPTPRT2_DW0 Register (Offset = 0h) [reset = 2000002h]

SUPTPRT2_DW0

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Table 14-12264. Instance Table

Instance Name	Physical Address
USB0	3100 0970h

Figure 14-6059. USB2SS_SUPPRTCAP2_SUPTPRT2_DW0 Name Register

31	30	29	28	27	26	25	24
MAJOR_REVISION							
R							
2h							
23	22	21	20	19	18	17	16
MINOR_REVISION							
R							
0h							
15	14	13	12	11	10	9	8
NEXT_CAPABILITY_POINTER							
R							
0h							
7	6	5	4	3	2	1	0
CAPABILITY_ID							
R							
2h							

Table 14-12265. USB2SS_SUPPRTCAP2_SUPTPRT2_DW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAJOR_REVISION	R	2h	MAJOR_REVISION Reset Source: rst_mod_g_rst_n
23:16	MINOR_REVISION	R	0h	MINOR_REVISION Reset Source: rst_mod_g_rst_n
15:8	NEXT_CAPABILITY_POINTER	R	0h	NEXT_CAPABILITY_POINTER Reset Source: rst_mod_g_rst_n
7:0	CAPABILITY_ID	R	2h	CAPABILITY_ID For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.287 USB2SS_SUPPRTCAP2_SUPTPRT2_DW1 Register

14.7.3.2.2.287.1 USB2SS_SUPPRTCAP2_SUPTPRT2_DW1 Register (Offset = 4h) [reset = 20425355h]

Register SUPTPRT2_DW1

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Table 14-12266. Instance Table

Instance Name	Physical Address
USB0	3100 0974h

Figure 14-6060. USB2SS_SUPPRTCAP2_SUPTPRT2_DW1 Name Register

31	30	29	28	27	26	25	24
NAME_STRING							
R							
20425355h							
23	22	21	20	19	18	17	16
NAME_STRING							
R							
20425355h							
15	14	13	12	11	10	9	8
NAME_STRING							
R							
20425355h							
7	6	5	4	3	2	1	0
NAME_STRING							
R							
20425355h							

Table 14-12267. USB2SS_SUPPRTCAP2_SUPTPRT2_DW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NAME_STRING	R	20425355h	NAME_STRING For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.288 USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Register

14.7.3.2.2.288.1 USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Register (Offset = 8h) [reset = 180101h]

xHCI Supported Protocol Capability_ Data Word 2 For a description of other register fields, see section 7.2 of the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12268. Instance Table

Instance Name	Physical Address
USB0	3100 0978h

Figure 14-6061. USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Name Register

31	30	29	28	27	26	25	24
PSIC				MHD			RESERVED_24_21
R				R			R
0h				0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24_21			BLC	HLC	IHI	HSO	RESERVED
R			R	R	R	R	NONE
0h			1h	1h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COMPATIBLE_PORT_COUNT							
R							
1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMPATIBLE_PORT_OFFSET							
R							
1h							

Table 14-12269. USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PSIC	R	0h	PSIC Reset Source: rst_mod_g_rst_n
27:25	MHD	R	0h	Hub Depth For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
24:21	RESERVED_24_21	R	0h	Reserved
20	BLC	R	1h	BESL LPM Capability. When this bit is set to: - 1: The ports described by this xHCI Supported Protocol Capability applies BESL timing to the BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. - 0: The ports described by this xHCI Supported Protocol Capability applies HIRD timing to the BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. Reset Source: rst_mod_g_rst_n
19	HLC	R	1h	Compatible Port Offset. Compatible Port Count Refer to Table 7-3 in the Databook. Reset Source: rst_mod_g_rst_n
18	IHI	R	0h	IHI Reset Source: rst_mod_g_rst_n

Table 14-12269. USB2SS_SUPPRTCAP2_SUPTPRT2_DW2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	HSO	R	0h	HSO Reset Source: rst_mod_g_rst_n
16	RESERVED	NONE	0h	Reserved
15:8	COMPATIBLE_PORT_COUNT	R	1h	COMPATIBLE_PORT_COUNT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	COMPATIBLE_PORT_OFFSET	R	1h	COMPATIBLE_PORT_OFFSET For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.289 USB2SS_SUPPRTCAP2_SUPTPRT2_DW3 Register

14.7.3.2.2.289.1 USB2SS_SUPPRTCAP2_SUPTPRT2_DW3 Register (Offset = Ch) [reset = 0h]

Register SUPTPRT2_DW3

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Table 14-12270. Instance Table

Instance Name	Physical Address
USB0	3100 097Ch

Figure 14-6062. USB2SS_SUPPRTCAP2_SUPTPRT2_DW3 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_5							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_5							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_5							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_5			PROTCL_SLT_TY				
R			R				
0h			0h				

Table 14-12271. USB2SS_SUPPRTCAP2_SUPTPRT2_DW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED_31_5	R	0h	Reserved
4:0	PROTCL_SLT_TY	R	0h	Protocol Slot Type Reset Source: rst_mod_g_rst_n

14.7.3.2.2.290 USB2SS_SUPPRTCAP3_SUPTPRT3_DW0 Register

14.7.3.2.2.290.1 USB2SS_SUPPRTCAP3_SUPTPRT3_DW0 Register (Offset = 0h) [reset = 0h]

Register SUPTPRT3_DW0

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Table 14-12272. Instance Table

Instance Name	Physical Address
USB0	3100 0980h

Figure 14-6063. USB2SS_SUPPRTCAP3_SUPTPRT3_DW0 Name Register

31	30	29	28	27	26	25	24
MAJOR_REVISION							
R							
0h							
23	22	21	20	19	18	17	16
MINOR_REVISION							
R							
0h							
15	14	13	12	11	10	9	8
NEXT_CAPABILITY_POINTER							
R							
0h							
7	6	5	4	3	2	1	0
CAPABILITY_ID							
R							
0h							

Table 14-12273. USB2SS_SUPPRTCAP3_SUPTPRT3_DW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MAJOR_REVISION	R	0h	MAJOR_REVISION For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
23:16	MINOR_REVISION	R	0h	MINOR_REVISION For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
15:8	NEXT_CAPABILITY_POINTER	R	0h	NEXT_CAPABILITY_POINTER For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	CAPABILITY_ID	R	0h	CAPABILITY_ID For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.291 USB2SS_SUPPRTCAP3_SUPTPRT3_DW1 Register

14.7.3.2.2.291.1 USB2SS_SUPPRTCAP3_SUPTPRT3_DW1 Register (Offset = 4h) [reset = 0h]

Register SUPTPRT3_DW1

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Table 14-12274. Instance Table

Instance Name	Physical Address
USB0	3100 0984h

Figure 14-6064. USB2SS_SUPPRTCAP3_SUPTPRT3_DW1 Name Register

31	30	29	28	27	26	25	24
NAME_STRING							
R							
0h							
23	22	21	20	19	18	17	16
NAME_STRING							
R							
0h							
15	14	13	12	11	10	9	8
NAME_STRING							
R							
0h							
7	6	5	4	3	2	1	0
NAME_STRING							
R							
0h							

Table 14-12275. USB2SS_SUPPRTCAP3_SUPTPRT3_DW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NAME_STRING	R	0h	NAME_STRING For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.292 USB2SS_SUPPRTCAP3_SUPTPRT3_DW2 Register

14.7.3.2.2.292.1 USB2SS_SUPPRTCAP3_SUPTPRT3_DW2 Register (Offset = 8h) [reset = 102h]

SUPTPRT3_DW2 For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus (USB) Specification 3.0.

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Table 14-12276. Instance Table

Instance Name	Physical Address
USB0	3100 0988h

Figure 14-6065. USB2SS_SUPPRTCAP3_SUPTPRT3_DW2 Name Register

31	30	29	28	27	26	25	24
PSIC				MHD			RESERVED
R				R			NONE
0h				0h			0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
COMPATIBLE_PORT_COUNT							
R							
1h							
7	6	5	4	3	2	1	0
COMPATIBLE_PORT_OFFSET							
R							
2h							

Table 14-12277. USB2SS_SUPPRTCAP3_SUPTPRT3_DW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PSIC	R	0h	PSIC Reset Source: rst_mod_g_rst_n
27:25	MHD	R	0h	Hub Depth For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
24:16	RESERVED	NONE	0h	Reserved
15:8	COMPATIBLE_PORT_COUNT	R	1h	COMPATIBLE_PORT_COUNT For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n
7:0	COMPATIBLE_PORT_OFFSET	R	2h	COMPATIBLE_PORT_OFFSET For a description of this standard USB register field, see the eXtensible Host Controller Interface for Universal Serial Bus [USB] Specification 3.0. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.293 USB2SS_SUPPRTCAP3_SUPTPRT3_DW3 Register

14.7.3.2.2.293.1 USB2SS_SUPPRTCAP3_SUPTPRT3_DW3 Register (Offset = Ch) [reset = 0h]

SUPTPRT3_DW3

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Table 14-12278. Instance Table

Instance Name	Physical Address
USB0	3100 098Ch

Figure 14-6066. USB2SS_SUPPRTCAP3_SUPTPRT3_DW3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_31_5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED_31_5</td><td colspan="5">PROTCL_SLT_TY</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-12279. USB2SS_SUPPRTCAP3_SUPTPRT3_DW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED_31_5	R	0h	Reserved
4:0	PROTCL_SLT_TY	R	0h	Protocol Slot Type Reset Source: rst_mod_g_rst_n

14.7.3.2.2.294 USB2SS_GBL_GSBUSCFG0 Register

14.7.3.2.2.294.1 USB2SS_GBL_GSBUSCFG0 Register (Offset = 0h) [reset = 6h]

Global SoC Bus Configuration Register 0 This register configures system bus DMA options for the initiator bus, which may be configured as AHB, AXI, or Native. Options include burst length and cache type (bufferable/ posted, cacheable/snoop, and so on). The application can program this register upon power-on, or a change in mode of operation after the DMA engine is halted. xHCI Register Power-On Value: If you are using a standard xHCI host driver, make sure to set the register's power-on value during coreConsultant configuration (DWC_USB3_GSBUSCFG0_INIT parameter) because the standard xHCI driver does not access this register. For more details on this register, refer to the following sections: - "Usage of Global SoC Bus Configuration Register 0 (GSBUSCFG0)" section in the Programming Guide - "System Bus Interface" section in the Databook

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Table 14-12280. Instance Table

Instance Name	Physical Address
USB0	3100 C100h

Figure 14-6067. USB2SS_GBL_GSBUSCFG0 Name Register

31	30	29	28	27	26	25	24
DATRDREQINFO				DESRDREQINFO			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
DATWRREQINFO				DESWRREQINFO			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED_15_12				DATBIGEND	DESBIGEND	RESERVED_9_8	
R				R/W	R/W	R	
0h				0h	0h	0h	
7	6	5	4	3	2	1	0
INCR256BRSTENA	INCR128BRSTENA	INCR64BRSTENA	INCR32BRSTENA	INCR16BRSTENA	INCR8BRSTENA	INCR4BRSTENA	INCRBRSTENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	1h	0h

Table 14-12281. USB2SS_GBL_GSBUSCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	DATRDREQINFO	R/W	0h	DATRDREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Data Read [DatRdReqInfo] Input to BUS-GM. Reset Source: rst_mod_g_rst_n
27:24	DESRDREQINFO	R/W	0h	DESRDREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Read [DesRdReqInfo]. Input to BUS-GM. Reset Source: rst_mod_g_rst_n
23:20	DATWRREQINFO	R/W	0h	DATWRREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Data Write [DatWrReqInfo]. Input to BUS-GM. Reset Source: rst_mod_g_rst_n
19:16	DESWRREQINFO	R/W	0h	DESWRREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Write [DesWrReqInfo] Input to BUS-GM. Reset Source: rst_mod_g_rst_n
15:12	RESERVED_15_12	R	0h	Reserved for future use

Table 14-12281. USB2SS_GBL_GSBUSCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DATBIGEND	R/W	0h	Data Access is Big Endian This bit controls the endian mode for data accesses. - Little-endian [default]. - Big-endian. In big-endian mode, DMA access [both read and write] for packet data a Byte Invariant Big-Endian mode [see "Little-Endian and Big-Endian" section in the User Guide]. Note: Since AXI requires byte invariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate. See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI initiator [DWC_USB3_MBUS_TYPE=1], this bit must be set to zero. Reset Source: rst_mod_g_rst_n
10	DESBIGEND	R/W	0h	Descriptor Access is Big Endian This bit controls the endian mode for descriptor accesses. - Little-endian [default] - Big-endian In big-endian mode, DMA access [both read and write] for descriptors uses a Byte Invariant Big-Endian mode [see "Little-Endian and Big-Endian" section in the User Guide. Data is considered as 'embedded data' in the descriptors in the following cases: - Device mode: The buffer pointer of a Setup TRB points to the Setup TRB itself. - Host mode: The Immediate Data [IDT] bit in a Transfer TRB is set to 1. In device mode, if the system uses different endian modes for descriptor and data, software must not use 'embedded' data. In host mode, if the system uses different endian modes for data and descriptors, the controller treats 'embedded data' as descriptor [not as data] in terms of endian mode handling. If this is not the expectation of the system, the software must manipulate the 'embedded data' accordingly. Note: Since AXI requires byte invariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate. See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI initiator [DWC_USB3_MBUS_TYPE=1], this bit must be set to zero. Reset Source: rst_mod_g_rst_n
9:8	RESERVED_9_8	R	0h	Reserved
7	INCR256BRSTENA	R/W	0h	INCR256 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to 1, the AHB/AXI initiator uses INCR to do the 256-beat burst. Reset Source: rst_mod_g_rst_n
6	INCR128BRSTENA	R/W	0h	INCR128 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to 1, the AHB/AXI initiator uses INCR to do the 128-beat burst. Reset Source: rst_mod_g_rst_n
5	INCR64BRSTENA	R/W	0h	INCR64 Burst Type Enable - Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to 1, the AHB/AXI initiator uses INCR to do the 64-beat burst. Reset Source: rst_mod_g_rst_n
4	INCR32BRSTENA	R/W	0h	INCR32 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to 1, the AHB/AXI initiator uses INCR to do the 32-beat burst. Reset Source: rst_mod_g_rst_n
3	INCR16BRSTENA	R/W	0h	INCR16 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to '1', the AHB/AXI initiator uses INCR to do the 16-beat burst. Reset Source: rst_mod_g_rst_n
2	INCR8BRSTENA	R/W	1h	INCR8 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software set this bit to "1", the AHB/AXI initiator uses INCR to do the 8-beat burst. Reset Source: rst_mod_g_rst_n

Table 14-12281. USB2SS_GBL_GSBUSCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INCR4BRSTENA	R/W	1h	INCR4 Burst Type Enable Input to BUS-GM. For the AXI configuration, when this bit is enabled the controller is allowed to do bursts of beat length 1, 2, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers. Reset Source: rst_mod_g_rst_n
0	INCRBRSTENA	R/W	0h	Undefined Length INCR Burst Type Enable [INCRBrstEna] Input to BUS-GM. This bit determines the set of burst lengths the initiator interface uses. It works in conjunction with the GSBUSCFG0[7:1] enables [INCR256/128/64/32/16/8/4]. 0: INCRX burst mode HBURST [for AHB configurations] and ARLEN/AWLEN [for AXI configurations] do not use INCR except in case of non-aligned burst transfers. In the case of address-aligned transfers, they use only the following burst lengths: - 1 - 2, 4 [if GSBUSCFG0.INCR4BrstEna = 1] - 8 [if GSBUSCFG0.INCR8BrstEna = 1] - 16 [if GSBUSCFG0.INCR16BrstEna = 1] - 32 [if GSBUSCFG0.INCR32BrstEna = 1] - 64 [if GSBUSCFG0.INCR64BrstEna = 1] - 128 [if GSBUSCFG0.INCR128BrstEna = 1] - 256 [if GSBUSCFG0.INCR256BrstEna = 1] Note: - In case of non-address-aligned transfers, INCR may get generated at the beginning and end of the transfers to align the address boundaries, even though INCR is disabled. - In AHB mode, if INCRX burst mode is enabled, but none of the supported INCRx bursts bits are enabled, then the controller will perform [undefined length] INCR bursts. 1: INCR [undefined length] burst mode - AHB configurations: HBURST uses SINGLE or INCR of any length with handling 1KB boundary breakup. - AXI configurations: ARLEN/AWLEN uses any length less than or equal to the largest-enabled burst length of INCR32/64/128/256. For cache line-aligned applications, this bit is typically set to 0 to ensure that the initiator interface uses only power-of-2 burst lengths [as enabled via GSBUSCFG0[7:0]]. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.295 USB2SS_GBL_GSBUSCFG1 Register

14.7.3.2.2.295.1 USB2SS_GBL_GSBUSCFG1 Register (Offset = 4h) [reset = 300h]

Global SoC Bus Configuration Register 1 xHCI Register Power-On Value: If you are using a standard xHCI host driver, make sure to set the register's power-on value during coreConsultant configuration (DWC_USB3_GSBUSCFG1_INIT parameter) because the standard xHCI driver does not access this register. For more details on this register, refer to "System Bus Interface" section in the Databook.

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Table 14-12282. Instance Table

Instance Name	Physical Address
USB0	3100 C104h

Figure 14-6068. USB2SS_GBL_GSBUSCFG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_13</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_31_13</td><td>EN1KPAGE</td><td colspan="4">PIPETRANSLIMIT</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_7_0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12283. USB2SS_GBL_GSBUSCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_31_13	R	0h	Reserved
12	EN1KPAGE	R/W	0h	1k Page Boundary Enable By default [this bit is disabled] the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI initiator [DMA data] breaks transfers at the 1k page boundary. Reset Source: rst_mod_g_rst_n
11:8	PIPETRANSLIMIT	R/W	3h	AXI Pipelined Transfers Burst Request Limit The field controls the number of outstanding pipelined transfer requests the AXI initiator pushes to the AXI target. When the AXI initiator reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: - 'h0: 1 request - 'h1: 2 requests - 'h2: 3 requests - 'h3: 4 requests - ... - 'hF: 16 requests Reset Source: rst_mod_g_rst_n
7:0	RESERVED_7_0	R	0h	Reserved

14.7.3.2.2.296 USB2SS_GBL_GTXTHRCFG Register

14.7.3.2.2.296.1 USB2SS_GBL_GTXTHRCFG Register (Offset = 8h) [reset = 0h]

Global Tx Threshold Control Register For more information on - Using this register, refer to "Packet Threshold and Burst Features for High Latency Systems" section in the Databook. - Selecting values for the fields of this register, see the "TX/RX Data FIFO Sizes and TX/RX Threshold Control Register Settings" section in the User Guide. Note: - GTXTHRCFG register is not applicable for Debug Target. - GTXTHRCFG register is not applicable in USB 2.0-only mode.

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Table 14-12284. Instance Table

Instance Name	Physical Address
USB0	3100 C108h

Figure 14-6069. USB2SS_GBL_GTXTHRCFG Name Register

31	30	29	28	27	26	25	24
RESERVED_31	RESERVED_30	USBTXPKTCNTSEL	RESERVED_28	USBTXPKTCNT			
R	R	R/W	R	R/W			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
USBMAXTXBURSTSIZE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_15	RESERVED_14	RESERVED_13_11			RESERVED_10_0		
R	R	R			R		
0h	0h	0h			0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_10_0							
R							
0h							

Table 14-12285. USB2SS_GBL_GTXTHRCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_31	R	0h	Reserved
30	RESERVED_30	R	0h	Reserved
29	USBTXPKTCNTSEL	R/W	0h	USB Transmit Packet Count Enable This field enables/disables the USB transmission multi-packet thresholding: - 0: USB transmission multi-packet thresholding is disabled. the controller can start transmission on the USB after the entire [one full] packet has been fetched into the corresponding TXFIFO. - 1: USB transmission multi-packet thresholding is enabled. The controller can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction [burst] are already in the corresponding TXFIFO. This mode is valid in both host and device modes. It is only used for SuperSpeed operation. Reset Source: rst_mod_g_rst_n
28	RESERVED_28	R	0h	Reserved

Table 14-12285. USB2SS_GBL_GTXTHRCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:24	USBTXPKTCNT	R/W	0h	USB Transmit Packet Count This field specifies the number of packets that must be in the TXFIFO before the controller can start transmission for the corresponding USB transaction [burst]. This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15. Note: - In device mode, if device controller does not have the TRBs for the number of packets or if it cannot fetch the TRBs because of high latency or switching between other endpoints, then it does not wait for the threshold number of packets. The threshold number of packets will be honored only when the TRBs are available in the controller for the number of packets before it starts the data fetch. - This field must be less than or equal to the USB Maximum TX Burst Size field. Reset Source: rst_mod_g_rst_n
23:16	USBMAXTXBURSTSIZE	R/W	0h	USB Maximum TX Burst Size When UsbTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the controller can do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. User can program a smaller value to this field to limit the TX burst size that the controller can do. Host mode: It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints. Device mode: This value is not used in device mode, but users need to program a value when using the TX threshold feature to make sure that the value programmed in UsbTxPktCnt is less than this value. Valid values are from 1 to 16. Reset Source: rst_mod_g_rst_n
15	RESERVED_15	R	0h	Reserved_15
14	RESERVED_14	R	0h	Reserved1[Rsvd/Rs] Register field must write only 0 by the application. The read value must be treated as X [unknown].
13:11	RESERVED_13_11	R	0h	Reserved [Rsvd/Rs] The register field must write only 0 by the application. The read value must be treated as X [unknown].
10:0	RESERVED_10_0	R	0h	Reserved for future use

14.7.3.2.2.297 USB2SS_GBL_GRXTHRCFG Register

14.7.3.2.2.297.1 USB2SS_GBL_GRXTHRCFG Register (Offset = Ch) [reset = 0h]

Global Rx Threshold Control Register In a normal case, a Tx burst starts as soon as one packet is prefetched. an Rx burst starts as soon as 1-packet space is available. This works well as long as the system bus is faster than the USB 3.0 bus (a 1024-bytes packet takes ~2.2 microseconds on the USB bus in SS mode). If the system bus latency is larger than 2.2 microseconds to access a 1024-byte packet, then starting a burst on 1-packet condition leads to an early abort of the burst causing unnecessary performance reduction. To avoid underrun and overrun during the burst, in a high-latency bus system (like USB), threshold and burst size control is provided through GTXTHRCFG and GRXTHRCFG registers. Bit [29] of the GTXTHRCFG and GRXTHRCFG registers enables this feature. For more information on - Using this register, refer to "Packet Threshold and Burst Features for High Latency Systems" section in the Databook. - Selecting values for the fields of this register, see the "TX/RX Data FIFO Sizes and TX/RX Threshold Control Register Settings" section in the User Guide. Note: - GRXTHRCFG register is not applicable for Debug Target. - There is an issue when ACK TP with NumP=0 followed by ACK TP with NumP=1 without ERDY TP sent by the device controller during a burst bulk OUT transfer. This may cause third-party USB 3.0 host controllers to keep waiting for the ERDY TP. The USB 3.0 specification states that "When an endpoint is not in a flow control condition, it shall not send an ERDY TP unless the endpoint is a Bulk endpoint that supports streams." In this case, after the device sent the ACK TP (nump=1), the endpoint was not in the flow control, so it did not send an ERDY. The device would have sent ERDY if the next OUT packet was not received. When the next OUT packet was received, at that time there was enough buffer space to accept it, so the device accepted the packet by informing host that it is not no longer in the flow control. The Host should wait for the responses for all the OUT packets to return and then decide if the endpoint is still in flow control or not. The USB 3.1 specification supersedes all the USB 3.0 specification. The errata states that "If the host continues, or resumes, transactions to an endpoint, the endpoint shall re-evaluate its flow control state and respond appropriately." However, there are no ECNs on the USB 3.0 for this issue. To work around this issue, the Global Rx Threshold mode must be disable by setting GRXTHRCFG.UsbRxPktCntSel=0. Instead, software can program the DCFG.NUMP mode (where fixed NUMP is transmitted always) instead of the RX threshold based nump mode to prevent the device from sending ACK TP with NumP=0. The NUMP in the ACK TP is the minimum value of (DCFG.NUMP, bMaxBurstSize) for each endpoint.

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Table 14-12286. Instance Table

Instance Name	Physical Address
USB0	3100 C10Ch

Figure 14-6070. USB2SS_GBL_GRXTHRCFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED_31_30</td><td>USBRXPKTCNTSEL</td><td>RESERVED_28</td><td colspan="4">USBRXPKTCNT</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td>R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">USBMAXRXBURSTSIZE</td><td colspan="3">RESERVED_18_16</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED_15</td><td colspan="2">RESERVED_14_13</td><td colspan="5">RESVISOCOUTSPC</td></tr>
<tr><td>R</td><td colspan="2">R</td><td colspan="5">R/W</td></tr>
<tr><td>0h</td><td colspan="2">0h</td><td colspan="5">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESVISOCOUTSPC</td></tr>
<tr><td colspan="8">R/W</td></tr>
</table>

Figure 14-6070. USB2SS_GBL_GRXTHRCFG Name Register (continued)

0h

Table 14-12287. USB2SS_GBL_GRXTHRCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_31_30	R	0h	Reserved
29	USBRXPKTCNTSEL	R/W	0h	USB Receive Packet Count Enable This field enables/disables the USB reception multi-packet thresholding: - 0: The controller can only start reception on the USB when the RX FIFO has space for at least one packet. - 1: The controller can only start reception on the USB when the RX FIFO has space for at least UsbRxPktCnt amount of packets. This mode is valid in both host and device mode. It is only used for SuperSpeed. In device mode, - Setting this bit to 1 also enables the functionality of reporting NUMP in the ACK TP based on the RX FIFO space instead of reporting a fixed NUMP derived from DCFG.NUMP for non-control endpoints. - If you are using external buffer control [EBC] feature, disable this mode by setting UsbRxPktCntSel to 0. Reset Source: rst_mod_g_rst_n
28	RESERVED_28	R	0h	Reserved
27:24	USBRXPKTCNT	R/W	0h	USB Receive Packet Count In host mode, this field specifies the space [in terms of the number of packets] that must be available in the RX FIFO before the controller can start the corresponding USB RX transaction [burst]. In device mode, this field specifies the space [in terms of the number of packets] that must be available in the RX FIFO before the controller can send ERDY for a flow-controlled endpoint. This field is valid only when the USB Receive Packet Count Enable field is set to 1. The valid values for this field are from 1 to 15. Note: This field must be less than or equal to the USB Maximum Receive Burst Size field. Reset Source: rst_mod_g_rst_n
23:19	USBMAXRXBURSTSIZE	R/W	0h	USB Maximum Receive Burst Size In host mode, this field specifies the Maximum Bulk IN burst the DWC_usb3 controller can perform. When the system bus is slower than the USB, RX FIFO can overrun during a long burst. You can program a smaller value to this field to limit the RX burst size that the controller can perform. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints in the host mode. In device mode, this field specifies the NUMP value that is sent in ERDY for an OUT endpoint. The programmed value should not exceed the RXFIFO size. This field is valid only when UsbRxPktCntSel is one. The valid values for this field are from 1 to 16. Reset Source: rst_mod_g_rst_n
18:16	RESERVED_18_16	R	0h	Reserved
15	RESERVED_15	R	0h	Reserved
14:13	RESERVED_14_13	R	0h	Reserved

Table 14-12287. USB2SS_GBL_GRXTHRCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:0	RESVISOCOUTSPC	R/W	0h	Space reserved in Rx FIFO for ISOC OUT In host mode, this field is not applicable and must be programmed to 0. In device mode, this value represents the amount of space to be reserved for ISOC OUT packets. The value to be programmed should be chosen so as to ensure that non ISOC packets are not completely dropped. If no space needs to be reserved for ISOC OUT packets, program this field to 0. This field is valid only in device mode. The maximum configurable depth of RX FIFO is 8192. Therefore, this field is 13 bits wide. The value of space reserved is in terms of DWC_USB3_MDWIDTH. For SS, the space reservation is always rounded off to the nearest packet boundary. Therefore, it is always recommended to program a value corresponding to MPS or its multiples. For HS/FS, the space reservation is the actual value. Note: For SS, reserve space for ISOC when the Rx FIFO space can accommodate two MPS or more. Otherwise, this may result in degraded performance for non-ISOC packets. If the space is entirely allocated for ISOC, the non-ISOC packets will be completely dropped. To help you decide during the time of configuring the controller, refer to the "Device-Mode Receive Path" section in the Databook. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.298 USB2SS_GBL_GCTL Register

14.7.3.2.2.298.1 USB2SS_GBL_GCTL Register (Offset = 10h) [reset = 2001h]

Global Core Control Register Refer to <workspace>/src/DWC_usb3_params.v for details on DWC_USB3_GCTL_INIT. Note: When Hibernation is not enabled, you can write any value to GblHibernationEn. It always returns 0 when read.

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Table 14-12288. Instance Table

Instance Name	Physical Address
USB0	3100 C110h

Figure 14-6071. USB2SS_GBL_GCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PWRDNSCALE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="5">PWRDNSCALE</td><td>MASTERFILTBYPASS</td><td>BYPSSETADDR</td><td>U2RSTECN</td></tr>
<tr><td colspan="5">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">FRMSCLDWN</td><td colspan="2">PRTCAPDIR</td><td>CORESOFTRESET</td><td>SOFITPSYNC</td><td>U1U2TIMERSCALE</td><td>DEBUGATTACH</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">2h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RAMCLKSEL</td><td colspan="2">SCALEDOWN</td><td>DISSCRAMBLE</td><td>U2EXIT_LFPS</td><td>GBLHIBERNATIONEN</td><td>DSBLCLKGTNG</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td></tr>
</table>

Table 14-12289. USB2SS_GBL_GCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	PWRDNSCALE	R/W	0h	Power Down Scale [PwrDnScale] The USB3 suspend_clk input replaces pipe3_rx_pclk as a clock source to a small part of the USB3 controller that operates when the SS PHY is in its lowest power [P3] state, and therefore does not provide a clock. The Power Down Scale field specifies how many suspend_clk periods fit into a 16 kHz clock period. When performing the division, round up the remainder. For example, when using an 8-bit/16-bit/32-bit PHY and 25-MHz Suspend clock, Power Down Scale = 25000 kHz/16 kHz = 13'd1563 [rounder up] Note: - Minimum Suspend clock frequency is 32 kHz - Maximum Suspend clock frequency is 125 MHz The LTSSM uses Suspend clock for 12-ms and 100-ms timers during suspend mode. According to the USB 3.0 specification, the accuracy on these timers is 0% to +50%. - 12 ms + 0~+50% accuracy = 18 ms [Range is 12 ms - 18 ms] - 100 ms + 0~+50% accuracy = 150 ms [Range is 100 ms - 150 ms]. The suspend clock accuracy requirement is: - [12,000/62.5] * [GCTL[31:19]] * actual suspend_clk_period must be between 12,000 and 18,000 - [100,0000/62.5] * [GCTL[31:19]] * actual suspend_clk_period must be between 100,000 and 150,000 For example, if your suspend_clk frequency varies from 7.5 MHz to 10.5MHz, then the value needs to programmed is: Power Down Scale = 10500/16 = 657 [rounded up. and fastest frequency used]. Reset Source: rst_mod_g_rst_n

Table 14-12289. USB2SS_GBL_GCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	MASTERFILTBYPASS	R/W	0h	Initiator Filter Bypass When this bit is set to 1'b1, irrespective of the parameter DWC_USB3_EN_BUS_FILTERS chosen, all the filters in the DWC_usb3_filter module are bypassed. The double synchronizers to mac_clk preceding the filters are also bypassed. For enabling the filters, this bit must be 1'b0. Reset Source: rst_mod_g_rst_n
17	BYPSSETADDR	R/W	0h	Bypass SetAddress in Device Mode. When BYPSSETADDR bit is set, the device controller uses the value in the DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, you can use this feature to avoid sending an actual SET ADDRESS control transfer on the USB, and make the device controller respond to a new address. When the xHCI Debug capability is enabled and this bit is set, the Debug Target immediately enters the configured state without requiring the Debug Host to send a SetAddress or SetConfig request. Note: You can set this bit for simulation purposes only. In the actual hardware, this bit must be set to 1'b0. Reset Source: rst_mod_g_rst_n
16	U2RSTECN	R/W	0h	U2RSTECN If the SuperSpeed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode. For each attempt, the device checks receiver termination eight times. From 2.60a release, this bit controls whether to check for Rx.Detect eight times or one time for every attempt. Device controller on USB 2.0 reset checks for receiver termination eight times per attempt if this bit is set to zero, or only once per attempt if the bit is set to one. Note: This bit is applicable only in device mode. Reset Source: rst_mod_g_rst_n
15:14	FRMSCLDWN	R/W	0h	FRMSCLDWN This field scales down device view of a SOF/ USOF/ITP duration. For SS/HS mode: - Value of 2'h3 implements interval to be 15.625 us - Value of 2'h2 implements interval to be 31.25 us - Value of 2'h1 implements interval to be 62.5 us - Value of 2'h0 implements interval to be 125us For FS mode, the scale-down value is multiplied by 8. When xHCI Debug Capability is enabled, this field also scales down the MaxPacketSize of the IN and OUT bulk endpoint to allow more traffic during simulation. It can only be changed from a non-zero value during simulation. - 2'h0: 1024 bytes - 2'h1: 512 bytes - 2'h2: 256 bytes - 2'h3: 128 bytes Reset Source: rst_mod_g_rst_n
13:12	PRTCAPDIR	R/W	2h	PRTCAPDIR: Port Capability Direction [PrtCapDir] - 2'b01: for Host configurations - 2'b10: for Device configurations Note: For static Host-only/Device-only applications, use DRD Host or DRD Device mode. The combination of GCTL.PrtCapDir=2'b11 with SRP and HNP/RSP disabled is not recommended for these applications. The sequence for switching modes in DRD configuration is as follows: Switching from Device to Host: 1. Reset the controller using GCTL[11] [CoreSoftReset]. 2. Set GCTL[13:12] [PrtCapDir] to 2'b01 [Host mode]. 3. Reset the host using USBCMD.HCRESET. Switching from Host to Device: 1. Reset the controller using GCTL[11] [CoreSoftReset]. 2. Set GCTL[13:12] [PrtCapDir] to 2'b10 [Device mode]. 3. Reset the device by setting DCTL[30] [CSftRst]. Reset Source: rst_mod_g_rst_n

Table 14-12289. USB2SS_GBL_GCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CORESOFTRESET	R/W	0h	Core Soft Reset [CoreSoftReset] - 1'b0 - No soft reset - 1'b1 - Soft reset to controller Clears the interrupts and all the CSRs except the following registers: - GCTL - GUCTL - GSTS - GSNPSID - GGPIO - GUID - GUSB2PHYCFGn registers - GUSB3PIPECTLn registers - DCFG - DCTL - DEVTEN - DSTS When you reset PHYs [using GUBS3PHYCFG or GUSB3PIPECTL registers], you must keep the controller in reset state until PHY clocks are stable. This controls the bus, ram, and mac domain resets. Refer to the "Reset Generation" section in the Databook. Note: This bit is for debug purposes only. Use USBCMD.HCRESET in xHCI Mode and DCTL.SoftReset in device mode for soft reset. Programming this field with random data will reset the internal logic of the host controller. Due to this side effect Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
10	SOFITPSYNC	R/W	0h	SOFITPSYNC If this bit is set to '0' operating in host mode, the controller keeps the UTMI/ULPI PHY on the first port in a non-suspended state whenever there is a SuperSpeed port that is not in Rx.Detect, SS.Disable and U3. If this bit is set to '1' operating in host mode, the controller keeps the UTMI/ULPI PHY on the first port in a non-suspended state whenever the other non-SuperSpeed ports are not in a suspended state. This feature is useful because it saves power by suspending UTMI/ULPI when SuperSpeed only is active, and it helps resolve when the PHY does not transmit a host resume unless it is placed in suspend state. This bit must be programmed as a part of initialization at power-on reset, and must not be dynamically changed afterwards. Note: - USB2PHYCFGn[6].PhySusp eventually decides to put the UTMI/ULPI PHY in to suspend state. In addition, when this bit is set to '1', the controller generates ITP from the ref_clk based counter. Otherwise, ITP and SOF are generated from utmi/ulpi_clk[0] based counter. To program the reference clock period inside the controller, refer to GUCTL[31:22].REFCLKPER. - This feature is valid in Host and DRD configurations and used only in Host mode operation. - If you never use this feature or the GFLADJ.GFLADJ_REFCLK_LPM_SEL, the minimum frequency for the ref_clk can be as low as 32KHz. You can connect the suspend_clk [as low as 32 KHz] to the ref_clk. - If you plan to enable hardware-based LPM or software-based LPM [PORTPMSC. HLE=1], then you cannot use this feature. Turn off this feature by setting this bit to '0' and use the GFLADJ.GFLADJ_REFCLK_LPM_SEL feature. - If you set this bit to '1', the GUSB2PHYCFG.U2_FREECLK_EXISTS bit and the DWC_USB3_FREECLK_USB2_EXIST parameter must be set to '0'. Program this bit to 0 if the controller is intended to be operated in USB 3.0 mode. Reset Source: rst_mod_g_rst_n
9	U1U2TIMERSCALE	R/W	0h	Disable U1/U2 timer Scaledown [U1U2TimerScale]. If set to '1' along with GCTL[5:4] [ScaleDown] = 2'bX1, disables the scale down of U1/U2 inactive timer values. This is for simulation mode only. Reset Source: rst_mod_g_rst_n
8	DEBUGATTACH	R/W	0h	Debug Attach When this bit is set, - SS Link proceeds directly to the Polling link state [after RUN/STOP in the DCTL register is asserted] without checking remote termination. - Link LFPS polling timeout is infinite. - Polling timeout during TS1 is infinite [in case link is waiting for TXEQ to finish]. Reset Source: rst_mod_g_rst_n

Table 14-12289. USB2SS_GBL_GCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	RAMCLKSEL	R/W	0h	RAM Clock Select [RAMClkSel] - 2'b00: bus clock - 2'b01: pipe clock [Only used in device mode] - 2'b10: In device mode , pipe/2 clock.In Host mode, controller switches ram_clk between pipe/2 clock, mac2_clk and bus_clk based on the status of the U2/U3 ports - 2'b11: In device mode, selects mac2_clk as ram_clk [when 8-bit UTMI or ULPI used. Not supported in 16-bit UTMI mode] In Host mode, controller switches ram_clk between pipe_clk, mac2_clk and bus_clk based on the status of the U2/U3 ports. In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00. For more information on how to select the RAM clock, see the "Clock Generation and Clock Tree Synthesis [CTS] Requirements" section in the Databook. Note: - In device mode, if you set RAMClkSel to 2'b11 [mac2_clk], the controller internally switches the ram_clk to bus_clk when the link state changes to Suspend [L2 or L3], and switches the ram_clk back to mac2_clk when the link state changes to resume or U2. - In host mode, if a value of 2/3 is chosen, then controller switches ram_clk between bus_clk, mac2_clk and pipe_clk, pipe_clk/2, based on the state of the U2/U3 ports. For example, if only the U2 port is active and the U3 ports are suspended, then the ram_clk is switched to mac2_clk. When only the U3 ports are active and the U2 ports are suspended, the controller internally switches the ram_clk to pipe3 clock and when all U2 and U3 ports are suspended, it switches the ram_clk to bus_clk. This allows decoupling the ram_clk from the bus_clk, and depending on the bandwidth requirement allows the bus_clk to be run at a lower frequency than the ram_clk requirements. The bus_clk frequency still cannot be less than 60MHz in host mode, and this is not verified. A value of 2 can be chosen only if the pipe data width is 8 or 16 bits. In this case the when the ram_clk is switched to pipe_clk, it uses pipe_clk/2 instead of pipe_clk. If a value of 3 is chosen for RAMClkSel, then when ram_clk is switched to pipe_clk, then pipe_clk is used without any divider. - In device mode, when RAMClkSel != 2'b00, the bus_clk_early frequency can be a minimum of 1 MHz. This is tested in simulation and also in hardware with Linux, Microsoft Windows 8, and MCCI Windows7 host drivers. Only control and non periodic transfers are supported when bus_clk is 1 MHz. For periodic applications, the bus_clk_early minimum frequency is higher depending on your application and SoC bus. Even though 1 MHz has been tested with standard host drivers, Synopsys recommends 5 MHz minimum for ASIC designs to provide a margin or at least have a backup option to increase the bus_clk frequency to 5 MHz if needed. Programming this field with random data will cause side effect. Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
5:4	SCALEDOWN	R/W	0h	Scale-Down Mode [ScaleDown] When Scale-Down mode is enabled for simulation, the controller uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes - 2'b00: Disables all scale-downs. Actual timing values are used. - 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include Speed enumeration, HNP/SRP, and Host mode suspend and resume - 2'b10: Enables scale-down of Device mode suspend and resume timing values only. - 2'b11: Enables bit 0 and bit 1 scale-down timing values. SS Mode - 2'b00: Disables all scale-downs. Actual timing values are used. - 2'b01: Enables scaled down SS timing and repeat values including: [1] Number of TxEq training sequences reduce to 8. [2] LFPS polling burst time reduce to 256 nS. [3] LFPS warm reset receive reduce to 30 uS. Refer to the rtl_vip_scaledown_mapping.xls file under <workspace>/sim/SoC_sim directory for the complete list. - 2'b10: No TxEq training sequences are sent. Overrides Bit 4. - 2'b11: Enables bit 0 and bit 1 scale-down timing values. Reset Source: rst_mod_g_rst_n

Table 14-12289. USB2SS_GBL_GCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DISSCRAMBLE	R/W	0h	Disable Scrambling [DisScramble] Transmit request to Link Partner on next transition to Recovery or Polling. Reset Source: rst_mod_g_rst_n
2	U2EXIT_LFPS	R/W	0h	U2EXIT_LFPS If this bit is, - 0: the link treats 248ns LFPS as a valid U2 exit. - 1: the link waits for 8us of LFPS before it detects a valid U2 exit. This bit is added to improve interoperability with a third-party host/device controller. This host/device controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the host/device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the host/device can stay in U2 while ignoring this glitch from the host/device controller. This bit is applicable for both host and device controller. This bit is added to improve interoperability with a third party host controller. This host controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the device can stay in U2 while ignoring this glitch from the host controller. Reset Source: rst_mod_g_rst_n
1	GBLHIBERNATIONEN	R	0h	GblHibernationEn This bit enables hibernation at the global level. If hibernation is not enabled through this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any controller state. In addition, the PMUs never drive the PHY interfaces and let the controller continue to drive the PHY interfaces. Reset Source: rst_mod_g_rst_n
0	DSBLCLKGTNG	R/W	1h	Disable Clock Gating [DsblClkGtng] This bit is set to 1 and the controller is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.299 USB2SS_GBL_GPMSTS Register

14.7.3.2.2.299.1 USB2SS_GBL_GPMSTS Register (Offset = 14h) [reset = 0h]

Global Power Management Status Register This debug register gives information on which event caused the hibernation exit. It provides internal status and state machine information, and is for Synopsys use only for debugging purposes. This register is not applicable in USB 2.0-only mode.

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Table 14-12290. Instance Table

Instance Name	Physical Address
USB0	3100 C114h

Figure 14-6072. USB2SS_GBL_GPMSTS Name Register

31	30	29	28	27	26	25	24
PORTSEL				RESERVED_27_17			
W				R			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED_27_17							U3WAKEUP
R							R
0h							0h
15	14	13	12	11	10	9	8
U3WAKEUP				RESERVED_10_11		U2WAKEUP	
R				R		R	
0h				0h		0h	
7	6	5	4	3	2	1	0
U2WAKEUP							
R							
0h							

Table 14-12291. USB2SS_GBL_GPMSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PORTSEL	W	0h	Global Power Management Status Register, PortSel This field selects the port number. Reset Source: rst_mod_g_rst_n
27:17	RESERVED_27_17	R	0h	Reserved
16:12	U3WAKEUP	R	0h	U3Wakeup This field gives the following USB 3.0 port wakeup conditions: - Bit [12]: Overcurrent Detected - Bit [13]: Resume Detected - Bit [14]: Connect Detected - Bit [15]: Disconnect Detected - Bit [16]: Last Connection State Reset Source: rst_mod_g_rst_n
11:10	RESERVED_10_11	R	0h	Reserved
9:0	U2WAKEUP	R	0h	U2Wakeup This field indicates the following USB 2.0 port wakeup conditions: - Bit [0]: Overcurrent Detected - Bit [1]: Resume Detected - Bit [2]: Connect Detected - Bit [3]: Disconnect Detected - Bit [4]: Last Connection State - Bit [5]: ID Change Detected - Bit [6]: SRP Request Detected - Bit [7]: ULPI Interrupt Detected - Bit [8]: USB Reset Detected - Bit [9]: Resume Detected Changed Reset Source: rst_mod_g_rst_n

14.7.3.2.2.300 USB2SS_GBL_GSTS Register

14.7.3.2.2.300.1 USB2SS_GBL_GSTS Register (Offset = 18h) [reset = 7E800000h]

Global Status Register

Return to Summary Table

Table 14-12292. Instance Table

Instance Name	Physical Address
USB0	3100 C118h

Figure 14-6073. USB2SS_GBL_GSTS Name Register

<table>
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<tr><td colspan="8">CBELT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">7E8h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">CBELT</td><td colspan="4">RESERVED_19_12</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">7E8h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED_19_12</td><td>SSIC_IP</td><td>OTG_IP</td><td>BC_IP</td><td>ADP_IP</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
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<tr><td>HOST_IP</td><td>DEVICE_IP</td><td>CSRTIMEOUT</td><td>BUSERRADDR VLD</td><td colspan="2">RESERVED_3_2</td><td colspan="2">CURMOD</td></tr>
<tr><td>R</td><td>R</td><td>R/W1TC</td><td>R/W1TC</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12293. USB2SS_GBL_GSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	CBELT	R	7E8h	Current BELT Value In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command. Reset Source: rst_mod_g_rst_n
19:12	RESERVED_19_12	R	0h	Reserved
11	SSIC_IP	R	0h	This field is not used. Reset Source: rst_mod_g_rst_n
10	OTG_IP	R	0h	This field is not used. Reset Source: rst_mod_g_rst_n
9	BC_IP	R	0h	Battery Charger Interrupt Pending This field indicates that there is a pending interrupt pertaining to BC in BCEVT register. Reset Source: rst_mod_g_rst_n
8	ADP_IP	R	0h	This field is not used. Reset Source: rst_mod_g_rst_n
7	HOST_IP	R	0h	Host Interrupt Pending: This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue. Reset Source: rst_mod_g_rst_n
6	DEVICE_IP	R	0h	Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral [device] operation in the Device event queue. Reset Source: rst_mod_g_rst_n

Table 14-12293. USB2SS_GBL_GSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CSRTIMEOUT	R/W1TC	0h	CSR Timeout When this bit is 1'b1, it indicates that the software performed a write or read to a controller register that could not be completed within DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles [default: h1FFFF]. Reset Source: rst_mod_g_rst_n
4	BUSERRADDRVLD	R/W1TC	0h	Bus Error Address Valid [BusErrAddrVld] Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error. Note: Only supported in AHB and AXI configurations. Reset Source: rst_mod_g_rst_n
3:2	RESERVED_3_2	R	0h	Reserved
1:0	CURMOD	R	0h	Current Mode of Operation [CurMod] Indicates the current mode of operation: - 2'b00: Device mode - 2'b01: Host mode Reset Source: rst_mod_g_rst_n

14.7.3.2.2.301 USB2SS_GBL_GUCTL1 Register

14.7.3.2.2.301.1 USB2SS_GBL_GUCTL1 Register (Offset = 1Ch) [reset = 198Bh]

Global User Control Register 1

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Table 14-12294. Instance Table

Instance Name	Physical Address
USB0	3100 C11Ch

Figure 14-6074. USB2SS_GBL_GUCTL1 Name Register

31	30	29	28	27	26	25	24
DEV_DECOUPLE_L1L2_EVT	DS_RXDET_MAX_TOUT_CTRL	FILTER_SE0_FSLS_EOP	TX_IPGAP_LINECHECK_DIS	DEV_TRB_OUT_SPR_IND	DEV_FORCE_20_CLK_FOR_30_CLK	P3_IN_U2	DEV_L1_EXIT_BY_HW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
IP_GAP_ADD_ON			DEV_LSP_TAIL_LOCK_DIS	NAK_PER_ENH_FS	NAK_PER_ENH_HS	PARKMODE_DISABLE_SS	PARKMODE_DISABLE_HS
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PARKMODE_DISABLE_FSLS	RESERVED_14_13		DISUSB2REFCLKGTNG	DISREFCLKGTNG	RESUME_OPMODE_HS_HOST	DEV_HS_NYET_BULK_SPR	L1_SUSP_THRLD_EN_FOR_HOST
R/W	R		R	R	R/W	R/W	R/W
0h	0h		1h	1h	0h	0h	1h
7	6	5	4	3	2	1	0
L1_SUSP_THRLD_FOR_HOST				HC_ERRATA_ENABLE	HC_PARCHK_DISABLE	OVRLD_L1_SUSP_COM	LOA_FILTER_EN
R/W				R/W	R/W	R/W	R/W
8h				1h	0h	1h	1h

Table 14-12295. USB2SS_GBL_GUCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DEV_DECOUPLE_L1L2_EVT	R/W	0h	DEV_DECOUPLE_L1L2_EVT - 0: Default behavior, no change in device events L1/L2U3 events are not decoupled [old behavior of v2.90a and before] - 1: Feature enabled, L1 and L2 events are separated when operating in 2.0 mode. Separate event enable bits for L1 suspend and wake events. This bit is applicable for device mode only. If this feature is enabled, L1 suspend and wake events have individual controls to enable/mask them. Enable this feature if you want to get L1 [LPM] events separtely and not combined with L2 events when operating in 2.0 speeds. Reset Source: rst_mod_g_rst_n
30	DS_RXDET_MAX_TOUT_CTRL	R/W	0h	DS_RXDET_MAX_TOUT_CTRL This bit is used to control the tRxDetectTimeoutDFP timer for the SuperSpeed link. - 0: Default behavior. 12ms is used as tRxDetectTimeoutDFP. - 1: 120ms is used as the tRxDetectTimeoutDFP. This bit is used only in host mode. For more details, refer to ECN020 for USB 3.0 Specification. Reset Source: rst_mod_g_rst_n

Table 14-12295. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	FILTER_SE0_FSLS_EOP	R/W	0h	FILTER_SE0_FSLS_EOP - 0: Default behavior, no change in Linestate check for SE0 detection in FS/LS - 1: Feature enabled, FS/LS SE0 is filtered for 2 clocks for detecting EOP This bit is applicable for FS/LS operation. If this feature is enabled, then SE0 on the linestate is validated for 2 consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode: FS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM handshake, the controller will ignore single SE0 glitch on the linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS. Host mode: FS/LS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the controller will ignore single SE0 glitch on the linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if the LineState has SE0 glitches during transmission. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n
28	TX_IPGAP_LINECHECK_DIS	R/W	0h	TX_IPGAP_LINECHECK_DIS - 0: Default behavior, no change in Linestate check - 1: Feature enabled, 2.0 MAC disables Linestate check during HS transmit This bit is applicable for HS operation of u2mac. If this feature is enabled, then the 2.0 mac operating in HS ignores the UTMI/ULPI Linestate during the transmit of a token [during token-to-token and token-to-data IPGAP]. When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the Linestate during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then for device LPM handshake, the controller will ignore the linestate after TX and wait for fixed clocks [40 bit times equivalent] after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap between [tkn to tkn/data] is added by 40 bit times of TXENDDELAY, and linestate is ignored during this 40 bit times delay. Enable this bit if the LineState will not reflect the expected line state [J] during transmission. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n
27	DEV_TRB_OUT_SPR_IND	R/W	0h	DEV_TRB_OUT_SPR_IND - 0: Default behavior, no change in TRB status dword - 1: Feature enabled, OUT TRB status indicates Short Packet This bit is applicable for device mode only [and ignored in host mode]. If the device application [software/hardware] wants to know if a short packet was received for an OUT in the TRB status itself, then this feature can be enabled, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the {trbstatus, RSVD, SPR, PCM1, bufsize} dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n

Table 14-12295. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	DEV_FORCE_20_CLK_FOR_30_CLK	R/W	0h	DEV_FORCE_20_CLK_FOR_30_CLK - 0: Default behavior, Uses 3.0 clock when operating in 2.0 mode - 1: Feature enabled This bit is applicable [and to be set] for device mode [DCFG.Speed != SS] only. In the 3.0 device controller, if the controller is programmed to operate in 2.0 only [that is, Device Speed is programmed to 2.0 speeds in DCFG[Speed]], then setting this bit makes the internal 2.0 [utmi/ulpi] clock to be routed as the 3.0 [pipe] clock. Enabling this feature allows the pipe3 clock to be not-running when forcibly operating in 2.0 device mode. Note: - When using this feature, all pipe3 inputs must be in inactive mode. In particular, the pipe3 clocks must not be running and the pipe3_phystatus_async must be tied to 0. This bit should not be set if the controller is programmed to operate in SuperSpeed mode [even when it falls back to 2.0]. - This bit is quasi-static, that is, it must not be changed during operation. - If the parameter "DWC_USB3_REMOVE_PIPE_CLK_MUX_FOR_20_MODE" is enabled, then muxing 2.0 clock/signals to pipe_clk/signals have to be done outside the controller for this feature to work. Reset Source: rst_mod_g_rst_n
25	P3_IN_U2	R/W	0h	P3_IN_U2 - 0: Default behavior, When SuperSpeed link is in U2, PowerState P2 is attempted on the PIPE Interface. - 1: When SuperSpeed link is in U2, PowerState P3 is attempted if GUSB3PIPECTL[17] is set. Setting this bit enables P3 Power State when the SuperSpeed link is in U2. Another Power Saving option. Check with your PHY vendor before enabling this option.When setting this bit to 1 to enable P3 in P2, GUSB3PIPECTL[27] should be set to 0 to make sure that the U2 exit is attempted in P0. This bit should be set only when GCTL.SOFITPSYNC=1 or GFLADJ.GFLADJ_REFCLK_LPM_SEL=1. Reset Source: rst_mod_g_rst_n
24	DEV_L1_EXIT_BY_HW	R/W	0h	DEV_L1_EXIT_BY_HW - 0: Default behavior, disables device L1 hardware exit logic - 1: feature enabled This bit is applicable for device mode [2.0] only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wakeup signaling to resume after going into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This hardware remote wake feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control - When control transfers are in progress, the LPM will be rejected [NYET response]. Only after control transfers are completed [either with ACK/STALL], LPM will be accepted - For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote-wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. - When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests thru L1. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n
23:21	IP_GAP_ADD_ON	R/W	0h	This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC. This should be programmed to a non zero value only in case where you need to increase the default inter packet delay calculations in the USB 2.0 MAC module DWC_usb3_u2mac.v Reset Source: rst_mod_g_rst_n

Table 14-12295. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DEV_LSP_TAIL_LOCK_DIS	R/W	0h	DEV_LSP_TAIL_LOCK_DIS - 0: Default behavior, enables device lsp lock logic for tail TRB update - 1: Fix disabled This is a bug fix for STAR 9000716195 that affects the CSP mode for OUT endpoints in device mode. The issue is that tail TRB index is not synchronized with the cache Scratchpad bytecount update. If the fast-forward request comes in-between the bytecount update on a newly fetched TRB and the tail-index write update in TPF, the RDP works on an incorrect tail index and misses the byte count decrement for the newly fetched TRB in the fast-forwarding process. This fix needs to be present all the times. Reset Source: rst_mod_g_rst_n
19	NAK_PER_ENH_FS	R/W	0h	NAK_PER_ENH_FS - 1: Enables performance enhancement for FS async endpoints in the presence of NAKs - 0: Enhancement not applied If a periodic endpoint is present , and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other Full Speed bulk endpoint which is ACked by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints [bulk/ control] and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your FullSpeed application. Setting this bit will only control, and is only required for Full Speed transfers. Reset Source: rst_mod_g_rst_n
18	NAK_PER_ENH_HS	R/W	0h	NAK_PER_ENH_HS - 1: Enables performance enhancement for HS async endpoints in the presence of NAKs - 0: Enhancement not applied If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in decrease in performance of other High Speed bulk endpoint which is ACked by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints [bulk/ control] and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your HighSpeed application. Setting this bit will only control, and is only required for High Speed transfers. Reset Source: rst_mod_g_rst_n
17	PARKMODE_DISABLE_SS	R/W	0h	PARKMODE_DISABLE_SS This bit is used only in host mode, and is for debug purpose only. When this bit is set to '1' all SS bus instances in park mode are disabled. Reset Source: rst_mod_g_rst_n
16	PARKMODE_DISABLE_HS	R/W	0h	PARKMODE_DISABLE_HS This bit is used only in host mode. When this bit is set to '1' all HS bus instances park mode are disabled. To improve performance in park mode, the xHCI scheduler queues in three requests of 4 packets each for High Speed asynchronous endpoints in a micro-frame. But if a device is slow and if it NAKs more than 3 times, then it is rescheduled only in the next micro-frame. This could decrease the performance of a slow device even further. In a few high speed devices [such as Sandisk Cruzer Blade 4GB VID:1921, PID:21863 and Flex Drive VID:3744, PID:8552] when an IN request is sent within 900ns of the ACK of the previous packet, these devices send a NAK. When connected to these devices, if required, the software can disable the park mode if you see performance drop in your system. When park mode is disabled, pipelining of multiple packet is disabled and instead one packet at a time is requested by the scheduler. This allows up to 12 NAKs in a micro-frame and improves performance of these slow devices. Reset Source: rst_mod_g_rst_n
15	PARKMODE_DISABLE_FSLS	R/W	0h	PARKMODE_DISABLE_FSLS This bit is used only in host mode, and is for debug purpose only. When this bit is set to '1' all FS/LS bus instances in park mode disabled. Reset Source: rst_mod_g_rst_n

Table 14-12295. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	RESERVED_14_13	R	0h	Reserved
12	DISUSB2REFCLKGTNG	R	1h	Disable ref_clk gating for 2.0 PHY [DisUSB2RefClkGtng] If ref_clk gating is disabled, then the ref_clk input cannot be turned off to the USB 2.0 PHY and controller. This is independent of the GCTL[DisClkGtng] setting. - 1'b0: ref_clk gating enabled for USB 2.0 PHY - 1'b1: ref_clk gating disabled for USB 2.0 PHY Reset Source: rst_mod_g_rst_n
11	DISREFCLKGTNG	R	1h	Disable ref_clk gating [DisRefClkGtng] If the ref_clk gating is disabled then input ref_clk cannot be turned off to SSPHY and controller. This is independent of GCTL[DisClkGtng] setting. - 1'b0: ref_clk gating Enabled for SSPHY - 1'b1: ref_clk gating Disabled for SSPHY Reset Source: rst_mod_g_rst_n
10	RESUME_OPMODE_HS_HOST	R/W	0h	RESUME_OPMODE_HS_HOST This bit is used only in host mode, and is for USB 2.0 opmode behavior in HS Resume. - When this bit is set to '1', the UTMI/ULPI opmode will be changed to "normal" along with HS terminations after EOR. This option is to support certain legacy UTMI/ULPI PHYs. - When this bit is set to '0', the UTMI/ULPI opmode will be changed to "normal" 2us after HS terminations change after EOR. This is the default behavior. Reset Source: rst_mod_g_rst_n
9	DEV_HS_NYET_BULK_SPR	R/W	0h	DEV_HS_NYET_BULK_SPR - 0: Default behavior, no change in device response - 1: Feature enabled, HS bulk OUT short packet gets NYET response This bit is applicable for device mode only [and ignored in host mode] to be used in 2.0 operation. If this bit is set, the device controller sends NYET response instead of ACK response for a successfully received bulk OUT short packet. If NYET is sent after receiving short packet, then the host would PING before sending the next OUT. this improves the performance as well as clears up the buffer/cache on the host side. Internal to the device controller, short packet [SPR=1] processing takes some time, and during this time, the USB is flow controlled. With NYET response instead of ACK on short packet, the host does not send another OUT-DATA without pinging in HS mode. This bit is quasi-static, that is, it must not be changed during device operation. Reset Source: rst_mod_g_rst_n
8	L1_SUSP_THRLD_EN_FOR_HOST	R/W	1h	L1_SUSP_THRLD_EN_FOR_HOST This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals [see "LPM Interface Signals" table in the Databook] as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: - The HIRD/BESL value used is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. - The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: - The HIRD/BESL value used is less than the value in L1_SUSP_THRLD_FOR_HOST field. - The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0. Reset Source: rst_mod_g_rst_n
7:4	L1_SUSP_THRLD_FOR_HOST	R/W	8h	L1_SUSP_THRLD_FOR_HOST This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit. Reset Source: rst_mod_g_rst_n
3	HC_ERRATA_ENABLE	R/W	1h	Host ELD Enable [HELDEn] When this bit is set to 1, it enables the Exit Latency Delta [ELD] support defined in the xHCI 1.0 Errata. This bit is used only in the host mode. This bit has to be set to 1 in Host mode. Reset Source: rst_mod_g_rst_n

Table 14-12295. USB2SS_GBL_GUCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	HC_PARCHK_DISABLE	R/W	0h	Host Parameter Check Disable [HParChkDisable] When this bit is set to '0' [by default], the xHC checks that the input slot/EP context fields comply to the xHCI Specification. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating 'PARAMETER ERROR'. When the bit is set to '1', the xHC does not perform parameter checks and does not generate 'PARAMETER ERROR' completion code. Reset Source: rst_mod_g_rst_n
1	OVRLD_L1_SUSP_COM	R/W	1h	OVRLD_L1_SUSP_COM If this bit is set, the utmi_l1_suspend_com_n is overloaded with the utmi_sleep_n signal. This bit is usually set if the PHY stops the port clock during L1 sleep condition. Note: The recommended connection for the SUSPENDM/ SLEEPM signals to the PHY with respect to this bit is as follows. For non-zero ports: Connect: - utmi_sleep_n[n] to SLEEPM[n] - [utmi_suspend_n[n] & utmi_l1_suspend_n[n]] to SUSPENDM[n] - USB2 PHYCLK[n] to utmi_clk[n] GUCTL1.OVRLD_L1_SUSP_COM impacts only Port0. For Port0: For Synopsys PHY, GUSB2PHYCFGn.U2_FREECLK_EXISTS=1. With this connection, the PHY keeps PLL active so that FREECLK is always available irrespective of suspend/sleep. - Connect USB2 PHY COMMONONN to 0. - Connect utmi_sleep_n[0] to SLEEPM[0]. - Connect [utmi_suspend_n[0] & utmi_l1_suspend_n[0]] to SUSPENDM[0]. - Connect USB2 PHY FREECLK to utmi_clk[0]. - Leave utmi_suspend_com_n, utmi_l1_suspend_com_n unconnected. - GUCTL1.OVRLD_L1_SUSP_COM can be set to any value. For Third Party PHY, GUSB2PHYCFGn.U2_FREECLK_EXISTS=0. With this connection the PHY can shut off all the clocks when the required conditions are met [like, GUSB2PHYCFGn[8,6], GUCTL1[1], GFLADJ[23], GCTL[10], Suspend condition, HW LPM enable etc]. - Connect -utmi_suspend_com_n to SUSPENDM[0] [or equivalent]. - Connect -utmi_l1_suspend_com_n to SLEEPM[0] [or equivalent]. - Connect PHYCLK0 [first port clock] to utmi_clk[0]. - Leave utmi_suspend_n[0], utmi_l1_suspend_ n[0], utmi_sleep_n[0] unconnected. - Set GUCTL1.OVRLD_L1_SUSP_COM to 1'b1. Reset Source: rst_mod_g_rst_n
0	LOA_FILTER_EN	R/W	1h	LOA_FILTER_EN If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables. Note: This bit is valid only in host mode. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.302 USB2SS_GBL_GSNPSID Register

14.7.3.2.2.302.1 USB2SS_GBL_GSNPSID Register (Offset = 20h) [reset = 5533330Bh]

Global Synopsys ID Register This is a read-only register that contains the release number of the controller.

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Table 14-12296. Instance Table

Instance Name	Physical Address
USB0	3100 C120h

Figure 14-6075. USB2SS_GBL_GSNPSID Name Register

31	30	29	28	27	26	25	24
SYNOPSYSID							
R							
5533330Bh							
23	22	21	20	19	18	17	16
SYNOPSYSID							
R							
5533330Bh							
15	14	13	12	11	10	9	8
SYNOPSYSID							
R							
5533330Bh							
7	6	5	4	3	2	1	0
SYNOPSYSID							
R							
5533330Bh							

Table 14-12297. USB2SS_GBL_GSNPSID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNOPSYSID	R	5533330Bh	Synopsys ID - SynopsysID[31:16] indicates Core Identification Number. 0x5533 is ASCII for U3 [DWC_usb3]. - SynopsysID[15:0] indicates the release number. Current Release is 3.30a. Software uses this register to configure release-specific features in the driver. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.303 USB2SS_GBL_GGPIO Register

14.7.3.2.2.303.1 USB2SS_GBL_GGPIO Register (Offset = 24h) [reset = 0h]

Global General Purpose Input/Output Register The application can use this register for general purpose input and output ports or for debugging.

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Table 14-12298. Instance Table

Instance Name	Physical Address
USB0	3100 C124h

Figure 14-6076. USB2SS_GBL_GGPIO Name Register

31	30	29	28	27	26	25	24
GPO							
R/W							
0h							
23	22	21	20	19	18	17	16
GPO							
R/W							
0h							
15	14	13	12	11	10	9	8
GPI							
R							
0h							
7	6	5	4	3	2	1	0
GPI							
R							
0h							

Table 14-12299. USB2SS_GBL_GGPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GPO	R/W	0h	General Purpose Output The value of this field is driven out on the gp_out[15:0] output port. Reset Source: rst_mod_g_rst_n
15:0	GPI	R	0h	General Purpose Input The read value of this field reflects the gp_in[15:0] input signal value. Note: Register bit-bash test should not check for reset value of this field since its not predictable. depends on the gp_in port. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.304 USB2SS_GBL_GUID Register

14.7.3.2.2.304.1 USB2SS_GBL_GUID Register (Offset = 28h) [reset = 0h]

Global User ID Register This is a read/write register containing the User ID. The power-on value for this register is specified as the User Identification Register. Power-on value during coreConsultant configuration (parameter DWC_USB3_USERID). This register can be used in the following ways: - To store the version or revision of your system. - To store hardware configurations that are outside the controller. - As a scratch register.

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Table 14-12300. Instance Table

Instance Name	Physical Address
USB0	3100 C128h

Figure 14-6077. USB2SS_GBL_GUID Name Register

31	30	29	28	27	26	25	24
USERID							
R/W							
0h							
23	22	21	20	19	18	17	16
USERID							
R/W							
0h							
15	14	13	12	11	10	9	8
USERID							
R/W							
0h							
7	6	5	4	3	2	1	0
USERID							
R/W							
0h							

Table 14-12301. USB2SS_GBL_GUID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USERID	R/W	0h	USERID Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.305 USB2SS_GBL_GUCTL Register

14.7.3.2.2.305.1 USB2SS_GBL_GUCTL Register (Offset = 2Ch) [reset = C800010h]

Global User Control Register: This register provides a few options for the software to control the controller behavior in the Host mode. Most of the options are used to improve host inter-operability with different devices.

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Table 14-12302. Instance Table

Instance Name	Physical Address
USB0	3100 C12Ch

Figure 14-6078. USB2SS_GBL_GUCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">REFCLKPER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">32h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">REFCLKPER</td><td>NOEXTRDL</td><td colspan="3">RESERVED_20_18</td><td>SPRSCTRLTRANSEN</td><td>RESBWHSEPS</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td colspan="3">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">32h</td><td>0h</td><td colspan="3">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED_15</td><td>USBHSTINAUTORETRYEN</td><td>ENOVERLAPCHK</td><td>EXTCAPSUPPTEN</td><td>INSRTEXTRFSBODI</td><td colspan="2">DTCT</td><td>DTFT</td></tr>
<tr><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DTFT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">10h</td></tr>
</table>

Table 14-12303. USB2SS_GBL_GUCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	REFCLKPER	R/W	32h	REFCLKPER This field indicates in terms of nano seconds the period of ref_clk. The default value of this register is set to 'h8 [8ns/125 MHz]. This field needs to be updated during power-on initialization, if GCTL.SOFITPSYNC or GFLADJ.GFLADJ_REFCLK_LPM_SEL is set to '1'. The programmable maximum value is 62ns, and the minimum value is 8ns. You must use a reference clock with a period that is an integer multiple, so that ITP can meet the jitter margin of 32ns. The allowable ref_clk frequencies whose period is not integer multiples are 16/17/19.2/24/39.7MHz. This field must not be set to '0' at any time. If you never plan to use this feature, then set this field to 'h8, the default value. Reset Source: rst_mod_g_rst_n

Table 14-12303. USB2SS_GBL_GUCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NOEXTRDL	R/W	0h	No Extra Delay Between SOF and the First Packet[NoExtrDl] Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host must wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. - 1'b0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. - 1'b1: Host doesn't wait after a SOF before it sends the first USB packet. Reset Source: rst_mod_g_rst_n
20:18	RESERVED_20_18	R	0h	Reserved
17	SPRSCTRLTRANSEN	R/W	0h	Sparse Control Transaction Enable Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames. Reset Source: rst_mod_g_rst_n
16	RESBWHSEPS	R/W	0h	Reserving 85% Bandwidth for HS Periodic EPs [ResBwHSEPS] By default, HC reserves 800f the bandwidth for periodic EPs. If this bit is set, the bandwidth is relaxed to 85% to accommodate two high speed, high bandwidth ISOC EPs. USB 2.0 required 800andwidth allocated for ISOC traffic. If two High-bandwidth ISOC devices [HD Webcams] are connected, and if each requires 1024-bytes X 3 packets per Micro-Frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 paylod per Micro-Frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode. Reset Source: rst_mod_g_rst_n
15	RESERVED_15	R	0h	Reserved
14	USBHSTINAUTORETRYEN	R/W	0h	Host IN Auto Retry [USBHstInAutoRetryEn] When set, this field enables the Auto Retry feature. For IN transfers [non-isochronous] that encounter data packets with CRC errors or internal overrun scenarios, the auto retry feature causes the Host controller to reply to the device with a non-terminating retry ACK [that is, an ACK transaction packet with Retry = 1 and NumP != 0]. If the Auto Retry feature is disabled [default], the controller will respond with a terminating retry ACK [that is, an ACK transaction packet with Retry = 1 and NumP = 0]. - 1'b0: Auto Retry Disabled - 1'b1: Auto Retry Enabled Note: When enabling Auto Retry feature, if the system latency is large enough to cause the internal PSQ full [PSQ can be full as the result of messages not being processed because of pending fetches before flushing the TxQ due to NRDY/ERDY conditions], then the host controller can generate a transaction error. Reset Source: rst_mod_g_rst_n
13	ENOVERLAPCHK	R/W	0h	Enable Check for LFPS Overlap During Remote Ux Exit: If this bit is set to, - 1'b1: The SuperSpeed link when exiting U1/U2/U3 waits for either the remote link LFPS or TS1/TS2 training symbols before it confirms that the LFPS handshake is complete. This is done to handle the case where the LFPS glitch causes the link to start exiting from the low power state. Looking for the LFPS overlap makes sure that the link partner also sees the LFPS. - 1'b0: When the link exists U1/U2/U3 because of a remote exit, it does not look for an LFPS overlap. Reset Source: rst_mod_g_rst_n

Table 14-12303. USB2SS_GBL_GUCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	EXTCAPSUPPTEN	R/W	0h	External Extended Capability Support Enable [ExtCapSuptEN] When set, this field enables extended capabilities to be implemented outside the controller. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in "Debug Capability" returns 16. A read to the first DWORD of the last internal extended capability [the "xHCI Supported Protocol Capability for USB 3.0" when the Debug Capability is not enabled] returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability [for example, at address N+16 where N is the address of this DWORD]. If enabled, an external address decoder that snoops the xHC target interface must be implemented. If it sees an access to N+16 or greater, the target access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer field. This indicates there are no more capabilities. Reset Source: rst_mod_g_rst_n
11	INSRTEXTRFSBODI	R/W	0h	Insert Extra Delay Between FS Bulk OUT Transactions [InsrtExtrFSBODI]. Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. - 1'b0: Host doesn't insert extra delay between consecutive Bulk OUT transactions to a FS Endpoint. - 1'b1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. Note: Setting this bit to one will reduce the Bulk OUT transfer performance for most of the FS devices. Reset Source: rst_mod_g_rst_n
10:9	DTCT	R/W	0h	Device Timeout Coarse Tuning [DTCT] This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The controller first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: - 2'b00: 0 usec -> use DTFT value instead - 2'b01: 500 usec - 2'b10: 1.5 msec - 2'b11: 6.5 msec Note: When the system latency is larger than the programmed DTCT/DTFT value, if the host controller is not able to accept certain transactions on the bus [because of system bus delays], the controller may not release header credits which in turn can cause the host to report a transaction error. Therefore, program this value to be larger than your system delay. Reset Source: rst_mod_g_rst_n
8:0	DTFT	R/W	10h	Device Timeout Fine Tuning [DTFT] This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For the DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. The minimum value of DTFT is 2. For example, if the mac3_clk is 125 MHz clk [8 ns period], this is calculated as follows: [DTFT value] * 256 * [8 ns] Quick Reference: - if DTFT = 0x2, 2*256*8 = 4usec timeout - if DTFT = 0x5, 5*256*8 = 10usec timeout - if DTFT = 0xA, 10*256*8 = 20usec timeout - if DTFT = 0x10, 16*256*8 = 32usec timeout - if DTFT = 0x19, 25*256*8 = 51usec timeout - if DTFT = 0x31, 49*256*8 = 100usec timeout - if DTFT = 0x62, 98*256*8 = 200usec timeout Note: When the system latency is larger than the programmed DTCT/DTFT value, if the host controller is not able to accept certain transactions on the bus [because of system bus delays], the controller may not release header credits which in turn can cause the host to report a transaction error. Therefore, program this value to be larger than your system delay. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.306 USB2SS_GBL_GBUSERRADDRLO Register

14.7.3.2.2.306.1 USB2SS_GBL_GBUSERRADDRLO Register (Offset = 30h) [reset = 0h]

Gobal SoC Bus Error Address Register - Low This is an alternate register for the GBUSERRADDR register.

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Table 14-12304. Instance Table

Instance Name	Physical Address
USB0	3100 C130h

Figure 14-6079. USB2SS_GBL_GBUSERRADDRLO Name Register

31	30	29	28	27	26	25	24
BUSERRADDR							
R							
0h							
23	22	21	20	19	18	17	16
BUSERRADDR							
R							
0h							
15	14	13	12	11	10	9	8
BUSERRADDR							
R							
0h							
7	6	5	4	3	2	1	0
BUSERRADDR							
R							
0h							

Table 14-12305. USB2SS_GBL_GBUSERRADDRLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUSERRADDR	R	0h	Bus Address - Low [BusAddrLo] This register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the controller. Note: Only supported in AHB and AXI configurations. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.307 USB2SS_GBL_GBUSERRADDRHI Register

14.7.3.2.2.307.1 USB2SS_GBL_GBUSERRADDRHI Register (Offset = 34h) [reset = 0h]

Gobal SoC Bus Error Address Register - High This is an alternate register for the GBUSERRADDR register.

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Table 14-12306. Instance Table

Instance Name	Physical Address
USB0	3100 C134h

Figure 14-6080. USB2SS_GBL_GBUSERRADDRHI Name Register

31	30	29	28	27	26	25	24
BUSERRADDR							
R							
0h							
23	22	21	20	19	18	17	16
BUSERRADDR							
R							
0h							
15	14	13	12	11	10	9	8
BUSERRADDR							
R							
0h							
7	6	5	4	3	2	1	0
BUSERRADDR							
R							
0h							

Table 14-12307. USB2SS_GBL_GBUSERRADDRHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUSERRADDR	R	0h	Bus Address - High [BusAddrHi] This register contains the higher 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the controller. Note: Only supported in AHB and AXI configurations. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.308 USB2SS_GBL_GPRTBIMAPLO Register

14.7.3.2.2.308.1 USB2SS_GBL_GPRTBIMAPLO Register (Offset = 38h) [reset = 0h]

Global SS Port to Bus Instance Mapping Register - Low This is an alternate register for the GPRTBIMAP register. Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. For a configuration with number of USB 3.0 ports same as number of SS Bus Instances, do not remap during debug session. If you remap for some reason, then the debug host must be connected to a port which has a dedicated SS Bus Instance. For example, if DWC_USB3_NUM_U3_ROOT_PORTS =3 and DWC_USB3_NUM_SS_USB_INSTANCES=3, and software maps the first SS port to the first SS BI and the second/third port to the second BI, then the debug host can be connected to the first port only. Note: For reset values, refer to the corresponding values in the GPRTBIMAP register.

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Table 14-12308. Instance Table

Instance Name	Physical Address
USB0	3100 C138h

Figure 14-6081. USB2SS_GBL_GPRTBIMAPLO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">BINUM8</td><td colspan="4">BINUM7</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">BINUM6</td><td colspan="4">BINUM5</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BINUM4</td><td colspan="4">BINUM3</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">BINUM2</td><td colspan="4">BINUM1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-12309. USB2SS_GBL_GPRTBIMAPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	BINUM8	R	0h	BINUM8: SS USB Instance Number for Port 8. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
27:24	BINUM7	R	0h	BINUM7: SS USB Instance Number for Port 7. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM6	R	0h	BINUM6: SS USB Instance Number for Port 6. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM5	R	0h	BINUM5: SS USB Instance Number for Port 5. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-12309. USB2SS_GBL_GPRTBIMAPLO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	BINUM4	R	0h	BINUM4: SS USB Instance Number for Port 4. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
11:8	BINUM3	R	0h	BINUM3: SS USB Instance Number for Port 3. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
7:4	BINUM2	R	0h	BINUM2: SS USB Instance Number for Port 2. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM1	R/W	0h	BINUM1: SS USB Instance Number for Port 1. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.309 USB2SS_GBL_GPRTBIMAPHI Register

14.7.3.2.2.309.1 USB2SS_GBL_GPRTBIMAPHI Register (Offset = 3Ch) [reset = 0h]

Global SS Port to Bus Instance Mapping Register - High This is an alternate register for the GPRTBIMAP register. For a configuration with number of USB 3.0 ports same as number of SS Bus Instances, do not remap during debug session. If you remap for some reason, then the debug host must be connected to a port which has a dedicated SS Bus Instance. For example, if DWC_USB3_NUM_U3_ROOT_PORTS =3 and DWC_USB3_NUM_SS_USB_INSTANCES=3, and software maps the first SS port to the first SS BI and the second/third port to the second BI, then the debug host can be connected to the first port only. Note: For reset values, refer to the corresponding values in the GPRTBIMAP register.

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Table 14-12310. Instance Table

Instance Name	Physical Address
USB0	3100 C13Ch

Figure 14-6082. USB2SS_GBL_GPRTBIMAPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_31_28				BINUM15			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
BINUM14				BINUM13			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
BINUM12				BINUM11			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
BINUM10				BINUM9			
R				R			
0h				0h			

Table 14-12311. USB2SS_GBL_GPRTBIMAPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_31_28	R	0h	Reserved
27:24	BINUM15	R	0h	BINUM15: SS USB Instance Number for Port 15. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM14	R	0h	BINUM14: SS USB Instance Number for Port 14. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM13	R	0h	BINUM13: SS USB Instance Number for Port 13. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM12	R	0h	BINUM12: SS USB Instance Number for Port 12. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
11:8	BINUM11	R	0h	BINUM11: SS USB Instance Number for Port 11. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-12311. USB2SS_GBL_GPRTBIMAPHI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	BINUM10	R	0h	BINUM10: SS USB Instance Number for Port 10. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM9	R	0h	BINUM9: SS USB Instance Number for Port 9. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.310 USB2SS_GBL_GHWPARAMS0 Register

14.7.3.2.2.310.1 USB2SS_GBL_GHWPARAMS0 Register (Offset = 40h) [reset = 4020400Ah]

This register contains the hardware configuration options

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Table 14-12312. Instance Table

Instance Name	Physical Address
USB0	3100 C140h

Figure 14-6083. USB2SS_GBL_GHWPARAMS0 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS0_31_24							
R							
40h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS0_23_16							
R							
20h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GHWPARAMS0_15_8							
R							
40h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS0_7_6		GHWPARAMS0_5_3			GHWPARAMS0_2_0		
R		R			R		
0h		1h			2h		

Table 14-12313. USB2SS_GBL_GHWPARAMS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GHWPARAMS0_31_24	R	40h	DWC_USB3_AWIDTH Reset Source: rst_mod_g_rst_n
23:16	GHWPARAMS0_23_16	R	20h	DWC_USB3_SDWIDTH Reset Source: rst_mod_g_rst_n
15:8	GHWPARAMS0_15_8	R	40h	DWC_USB3_MDWIDTH Reset Source: rst_mod_g_rst_n
7:6	GHWPARAMS0_7_6	R	0h	DWC_USB3_SBUS_TYPE Reset Source: rst_mod_g_rst_n
5:3	GHWPARAMS0_5_3	R	1h	DWC_USB3_MBUS_TYPE Reset Source: rst_mod_g_rst_n
2:0	GHWPARAMS0_2_0	R	2h	DWC_USB3_MODE Reset Source: rst_mod_g_rst_n

14.7.3.2.2.311 USB2SS_GBL_GHWPARAMS1 Register

14.7.3.2.2.311.1 USB2SS_GBL_GHWPARAMS1 Register (Offset = 44h) [reset = 1A4493Bh]

This register contains the hardware configuration options

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Table 14-12314. Instance Table

Instance Name	Physical Address
USB0	3100 C144h

Figure 14-6084. USB2SS_GBL_GHWPARAMS1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>GHWPARAMS1_31</td><td>GHWPARAMS1_30</td><td>GHWPARAMS1_29</td><td>GHWPARAMS1_28</td><td>GHWPARAMS1_27</td><td>GHWPARAMS1_26</td><td colspan="2">GHWPARAMS1_25_24</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td colspan="2">R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>GHWPARAMS1_23</td><td colspan="2">GHWPARAMS1_22_21</td><td colspan="5">GHWPARAMS1_20_15</td></tr>
<tr><td>R</td><td colspan="2">R</td><td colspan="5">R</td></tr>
<tr><td>1h</td><td colspan="2">1h</td><td colspan="5">8h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>GHWPARAMS1_20_15</td><td colspan="3">GHWPARAMS1_14_12</td><td colspan="3">GHWPARAMS1_11_9</td><td>GHWPARAMS1_8_6</td></tr>
<tr><td>R</td><td colspan="3">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td>8h</td><td colspan="3">4h</td><td colspan="3">4h</td><td>4h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">GHWPARAMS1_8_6</td><td colspan="3">GHWPARAMS1_5_3</td><td colspan="3">GHWPARAMS1_2_0</td></tr>
<tr><td colspan="2">R</td><td colspan="3">R</td><td colspan="3">R</td></tr>
<tr><td colspan="2">4h</td><td colspan="3">7h</td><td colspan="3">3h</td></tr>
</table>

Table 14-12315. USB2SS_GBL_GHWPARAMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GHWPARAMS1_31	R	0h	DWC_USB3_EN_DBC Reset Source: rst_mod_g_rst_n
30	GHWPARAMS1_30	R	0h	DWC_USB3_RM_OPT_FEATURES Reset Source: rst_mod_g_rst_n
29	GHWPARAMS1_29	R	0h	Reserved1 Reset Source: rst_mod_g_rst_n
28	GHWPARAMS1_28	R	0h	DWC_USB3_RAM_BUS_CLKS_SYNC Reset Source: rst_mod_g_rst_n
27	GHWPARAMS1_27	R	0h	DWC_USB3_MAC_RAM_CLKS_SYNC Reset Source: rst_mod_g_rst_n
26	GHWPARAMS1_26	R	0h	DWC_USB3_MAC_PHY_CLKS_SYNC Reset Source: rst_mod_g_rst_n
25:24	GHWPARAMS1_25_24	R	1h	DWC_USB3_EN_PWROPT Reset Source: rst_mod_g_rst_n
23	GHWPARAMS1_23	R	1h	DWC_USB3_SPRAM_TYP Reset Source: rst_mod_g_rst_n

Table 14-12315. USB2SS_GBL_GHWPARAMS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:21	GHWPARAMS1_22_21	R	1h	DWC_USB3_NUM_RAMS Reset Source: rst_mod_g_rst_n
20:15	GHWPARAMS1_20_15	R	8h	DWC_USB3_DEVICE_NUM_INT For details on DWC_USB3_DEVICE_NUM_INT, refer to <workspace>/src/DWC_usb3_params.v file. Reset Source: rst_mod_g_rst_n
14:12	GHWPARAMS1_14_12	R	4h	DWC_USB3_ASPACEWIDTH Reset Source: rst_mod_g_rst_n
11:9	GHWPARAMS1_11_9	R	4h	DWC_USB3_REQINFOWIDTH Reset Source: rst_mod_g_rst_n
8:6	GHWPARAMS1_8_6	R	4h	DWC_USB3_DATAINFOWIDTH Reset Source: rst_mod_g_rst_n
5:3	GHWPARAMS1_5_3	R	7h	DWC_USB3_BURSTWIDTH-1 Reset Source: rst_mod_g_rst_n
2:0	GHWPARAMS1_2_0	R	3h	DWC_USB3_IDWIDTH-1 Reset Source: rst_mod_g_rst_n

14.7.3.2.2.312 USB2SS_GBL_GHWPARAMS2 Register

14.7.3.2.2.312.1 USB2SS_GBL_GHWPARAMS2 Register (Offset = 48h) [reset = 0h]

This register contains the hardware configuration options

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Table 14-12316. Instance Table

Instance Name	Physical Address
USB0	3100 C148h

Figure 14-6085. USB2SS_GBL_GHWPARAMS2 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS2_31_0							
R							
0h							
23	22	21	20	19	18	17	16
GHWPARAMS2_31_0							
R							
0h							
15	14	13	12	11	10	9	8
GHWPARAMS2_31_0							
R							
0h							
7	6	5	4	3	2	1	0
GHWPARAMS2_31_0							
R							
0h							

Table 14-12317. USB2SS_GBL_GHWPARAMS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GHWPARAMS2_31_0	R	0h	DWC_USB3_USERID Reset Source: rst_mod_g_rst_n

14.7.3.2.2.313 USB2SS_GBL_GHWPARAMS3 Register

14.7.3.2.2.313.1 USB2SS_GBL_GHWPARAMS3 Register (Offset = 4Ch) [reset = 10420084h]

This register contains the hardware configuration options

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Table 14-12318. Instance Table

Instance Name	Physical Address
USB0	3100 C14Ch

Figure 14-6086. USB2SS_GBL_GHWPARAMS3 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS3_31	GHWPARAMS3_30_23						
R	R						
0h	20h						

23	22	21	20	19	18	17	16
GHWPARAMS3_30_23	GHWPARAMS3_22_18					GHWPARAMS3_17_12	
R	R					R	
20h	10h					20h	

15	14	13	12	11	10	9	8
GHWPARAMS3_17_12				GHWPARAMS3_11	GHWPARAMS3_10	GHWPARAMS3_9_8	
R				R	R	R	
20h				0h	0h	0h	

7	6	5	4	3	2	1	0
GHWPARAMS3_7_6		GHWPARAMS3_5_4		GHWPARAMS3_3_2		GHWPARAMS3_1_0	
R		R		R		R	
2h		0h		1h		0h	

Table 14-12319. USB2SS_GBL_GHWPARAMS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GHWPARAMS3_31	R	0h	Reserved Reset Source: rst_mod_g_rst_n
30:23	GHWPARAMS3_30_23	R	20h	DWC_USB3_CACHE_TOTAL_XFER_RESOURCES Reset Source: rst_mod_g_rst_n
22:18	GHWPARAMS3_22_18	R	10h	DWC_USB3_NUM_IN_EPS Reset Source: rst_mod_g_rst_n
17:12	GHWPARAMS3_17_12	R	20h	DWC_USB3_NUM_EPS Reset Source: rst_mod_g_rst_n
11	GHWPARAMS3_11	R	0h	DWC_USB3_ULPI_CARKIT Reset Source: rst_mod_g_rst_n
10	GHWPARAMS3_10	R	0h	DWC_USB3_VENDOR_CTL_INTERFACE Reset Source: rst_mod_g_rst_n
9:8	GHWPARAMS3_9_8	R	0h	Reserved Reset Source: rst_mod_g_rst_n
7:6	GHWPARAMS3_7_6	R	2h	DWC_USB3_HSPHY_DWIDTH Reset Source: rst_mod_g_rst_n

Table 14-12319. USB2SS_GBL_GHWPARAMS3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	GHWPARAMS3_5_4	R	0h	DWC_USB3_FSPHY_INTERFACE Reset Source: rst_mod_g_rst_n
3:2	GHWPARAMS3_3_2	R	1h	DWC_USB3_HSPHY_INTERFACE Reset Source: rst_mod_g_rst_n
1:0	GHWPARAMS3_1_0	R	0h	DWC_USB3_SSPHY_INTERFACE Reset Source: rst_mod_g_rst_n

14.7.3.2.2.314 USB2SS_GBL_GHWPARAMS4 Register

14.7.3.2.2.314.1 USB2SS_GBL_GHWPARAMS4 Register (Offset = 50h) [reset = 47A22004h]

This register contains the hardware configuration options

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Table 14-12320. Instance Table

Instance Name	Physical Address
USB0	3100 C150h

Figure 14-6087. USB2SS_GBL_GHWPARAMS4 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS4_31_28				GHWPARAMS4_27_24			
R				R			
4h				7h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS4_23	GHWPARAMS4_22	GHWPARAMS4_21	GHWPARAMS4_20_17				GHWPARAMS4_16_13
R	R	R	R				R
1h	0h	1h	1h				1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GHWPARAMS4_16_13			GHWPARAMS4_12	GHWPARAMS4_11	GHWPARAMS4_10_9		GHWPARAMS4_8_7
R			R	R	R		R
1h			0h	0h	0h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS4_8_7	GHWPARAMS4_6	GHWPARAMS4_5_0					
R	R	R					
0h	0h	4h					

Table 14-12321. USB2SS_GBL_GHWPARAMS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	GHWPARAMS4_31_28	R	4h	DWC_USB3_BMU_LSP_DEPTH Reset Source: rst_mod_g_rst_n
27:24	GHWPARAMS4_27_24	R	7h	DWC_USB3_BMU_PTL_DEPTH-1 Reset Source: rst_mod_g_rst_n
23	GHWPARAMS4_23	R	1h	DWC_USB3_EN_ISOC_SUPT Reset Source: rst_mod_g_rst_n
22	GHWPARAMS4_22	R	0h	Reserved Reset Source: rst_mod_g_rst_n
21	GHWPARAMS4_21	R	1h	DWC_USB3_EXT_BUFF_CONTROL Reset Source: rst_mod_g_rst_n
20:17	GHWPARAMS4_20_17	R	1h	DWC_USB3_NUM_SS_USB_INSTANCES Reset Source: rst_mod_g_rst_n
16:13	GHWPARAMS4_16_13	R	1h	DWC_USB3_HIBER_SCRATCHBUFS Number of external scratchpad buffers the controller requires to save its internal state in the device mode. Each buffer is assumed to be 4KB. The scratchpad buffer array must have this many buffer pointers. Reset Source: rst_mod_g_rst_n

Table 14-12321. USB2SS_GBL_GHWPARAMS4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	GHWPARAMS4_12	R	0h	Reserved Reset Source: rst_mod_g_rst_n
11	GHWPARAMS4_11	R	0h	Reserved Reset Source: rst_mod_g_rst_n
10:9	GHWPARAMS4_10_9	R	0h	Reserved Reset Source: rst_mod_g_rst_n
8:7	GHWPARAMS4_8_7	R	0h	Reserved Reset Source: rst_mod_g_rst_n
6	GHWPARAMS4_6	R	0h	Reserved Reset Source: rst_mod_g_rst_n
5:0	GHWPARAMS4_5_0	R	4h	DWC_USB3_CACHE_TRBS_PER_TRANSFER Reset Source: rst_mod_g_rst_n

14.7.3.2.2.315 USB2SS_GBL_GHWPARAMS5 Register

14.7.3.2.2.315.1 USB2SS_GBL_GHWPARAMS5 Register (Offset = 54h) [reset = 4202088h]

This register contains the hardware configuration options

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Table 14-12322. Instance Table

Instance Name	Physical Address
USB0	3100 C154h

Figure 14-6088. USB2SS_GBL_GHWPARAMS5 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS5_31_28				GHWPARAMS5_27_22			
R				R			
0h				10h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS5_27_22		GHWPARAMS5_21_16					
R		R					
10h		20h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GHWPARAMS5_15_10						GHWPARAMS5_9_4	
R						R	
8h						8h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS5_9_4				GHWPARAMS5_3_0			
R				R			
8h				8h			

Table 14-12323. USB2SS_GBL_GHWPARAMS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	GHWPARAMS5_31_28	R	0h	Reserved Reset Source: rst_mod_g_rst_n
27:22	GHWPARAMS5_27_22	R	10h	DWC_USB3_DFQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n
21:16	GHWPARAMS5_21_16	R	20h	DWC_USB3_DWQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n
15:10	GHWPARAMS5_15_10	R	8h	DWC_USB3_TXQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n
9:4	GHWPARAMS5_9_4	R	8h	DWC_USB3_RXQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n
3:0	GHWPARAMS5_3_0	R	8h	DWC_USB3_BMU_BUSGM_DEPTH Reset Source: rst_mod_g_rst_n

14.7.3.2.2.316 USB2SS_GBL_GHWPARAMS6 Register

14.7.3.2.2.316.1 USB2SS_GBL_GHWPARAMS6 Register (Offset = 58h) [reset = 1C268020h]

This register contains the hardware configuration options

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Table 14-12324. Instance Table

Instance Name	Physical Address
USB0	3100 C158h

Figure 14-6089. USB2SS_GBL_GHWPARAMS6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">GHWPARAMS6_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C26h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GHWPARAMS6_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C26h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>BUSFLTRSSUPPORT</td><td>BCSUPPORT</td><td>OTG_SS_SUPPORT</td><td>ADPSUPPORT</td><td>HNPSUPPORT</td><td>SRPSUPPORT</td><td colspan="2">GHWPARAMS6_9_8</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td colspan="2">R</td></tr>
<tr><td>1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>GHWPARAMS6_7</td><td>GHWPARAMS6_6</td><td colspan="6">GHWPARAMS6_5_0</td></tr>
<tr><td>R</td><td>R</td><td colspan="6">R</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">20h</td></tr>
</table>

Table 14-12325. USB2SS_GBL_GHWPARAMS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GHWPARAMS6_31_16	R	1C26h	DWC_USB3_RAM0_DEPTH Reset Source: rst_mod_g_rst_n
15	BUSFLTRSSUPPORT	R	1h	DWC_USB3_EN_BUS_FILTERS Reset Source: rst_mod_g_rst_n
14	BCSUPPORT	R	0h	DWC_USB3_EN_BC Reset Source: rst_mod_g_rst_n
13	OTG_SS_SUPPORT	R	0h	Reserved Reset Source: rst_mod_g_rst_n
12	ADPSUPPORT	R	0h	DWC_USB3_EN_ADP Reset Source: rst_mod_g_rst_n
11	HNPSUPPORT	R	0h	Reserved Reset Source: rst_mod_g_rst_n
10	SRPSUPPORT	R	0h	Reserved Reset Source: rst_mod_g_rst_n
9:8	GHWPARAMS6_9_8	R	0h	Reserved Reset Source: rst_mod_g_rst_n
7	GHWPARAMS6_7	R	0h	DWC_USB3_EN_FPGA Reset Source: rst_mod_g_rst_n

Table 14-12325. USB2SS_GBL_GHWPARAMS6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	GHWPARAMS6_6	R	0h	DWC_USB3_EN_DBG_PORTS Reset Source: rst_mod_g_rst_n
5:0	GHWPARAMS6_5_0	R	20h	DWC_USB3_PSQ_FIFO_DEPTH Reset Source: rst_mod_g_rst_n

14.7.3.2.2.317 USB2SS_GBL_GHWPARAMS7 Register

14.7.3.2.2.317.1 USB2SS_GBL_GHWPARAMS7 Register (Offset = 5Ch) [reset = 0h]

This register contains the hardware configuration options

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Table 14-12326. Instance Table

Instance Name	Physical Address
USB0	3100 C15Ch

Figure 14-6090. USB2SS_GBL_GHWPARAMS7 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS7_31_16							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GHWPARAMS7_31_16							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GHWPARAMS7_15_0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GHWPARAMS7_15_0							
R							
0h							

Table 14-12327. USB2SS_GBL_GHWPARAMS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GHWPARAMS7_31_16	R	0h	DWC_USB3_RAM2_DEPTH Reset Source: rst_mod_g_rst_n
15:0	GHWPARAMS7_15_0	R	0h	DWC_USB3_RAM1_DEPTH Reset Source: rst_mod_g_rst_n

14.7.3.2.2.318 USB2SS_GBL_GDBGFIFOSPACE Register

14.7.3.2.2.318.1 USB2SS_GBL_GDBGFIFOSPACE Register (Offset = 60h) [reset = C0000h]

Global Debug Queue/FIFO Space Available Register Bit Bash test should not be done on this debug register.

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Table 14-12328. Instance Table

Instance Name	Physical Address
USB0	3100 C160h

Figure 14-6091. USB2SS_GBL_GDBGFIFOSPACE Name Register

31	30	29	28	27	26	25	24
SPACE_AVAILABLE							
R							
Ch							
23	22	21	20	19	18	17	16
SPACE_AVAILABLE							
R							
Ch							
15	14	13	12	11	10	9	8
RESERVED_15_9							FIFO_QUEUE_SELECT
R							R/W
0h							0h
7	6	5	4	3	2	1	0
FIFO_QUEUE_SELECT							
R/W							
0h							

Table 14-12329. USB2SS_GBL_GDBGFIFOSPACE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SPACE_AVAILABLE	R	Ch	SPACE_AVAILABLE Reset Source: rst_mod_g_rst_n
15:9	RESERVED_15_9	R	0h	Reserved
8:0	FIFO_QUEUE_SELECT	R/W	0h	FIFO/Queue Select [or] Port-Select - FIFO/Queue Select[8:5] indicates the FIFO/Queue Type - FIFO/Queue Select[4:0] indicates the FIFO/Queue Number For example, 9'b0_0010_0001 refers to RxFIFO_1 and 9'b0_0101_1110 refers to TxReqQ_30. - 9'b0_0001_1111 to 9'b0_0000_0000: TxFIFO_31 to TxFIFO_0 - 9'b0_0011_1111 to 9'b0_0010_0000: RxFIFO_31 to RxFIFO_0 - 9'b0_0101_1111 to 9'b0_0100_0000: TxReqQ_31 to TxReqQ_0 - 9'b0_0111_1111 to 9'b0_0110_0000: RxReqQ_31 to RxReqQ_0 - 9'b0_1001_1111 to 9'b0_1000_0000: RxInfoQ_31 to RxInfoQ_0 - 9'b0_1010_0000: DescFetchQ_0 [for backwards compatibility] - 9'b0_1010_0001: EventQ_0 [for backwards compatibility] - 9'b0_1010_0010: ProtocolStatusQ_0 - 9'b0_1101_1111 to 9'b0_1110_0000: DescFetchQ_31 to DescFetchQ_0 - 9'b0_1111_1111 to 9'b0_1110_0000: WriteBack/EventQ_31 to WriteBack/EventQ_0 - 9'b1_0000_0111 to 9'b1_0000_0000: AuxEventQ_7 to AuxEventQ_0 [if EN_SEPARATE_DESC_QUEUES=1] Port-Select[3:0] selects the port-number when accessing GDBGLTSSM register. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.319 USB2SS_GBL_GDBGLTSSM Register

14.7.3.2.2.319.1 USB2SS_GBL_GDBGLTSSM Register (Offset = 64h) [reset = 41010440h]

Global Debug LTSSM Register In multi-port host configuration, the port-number is defined by Port-Select[3:0] field in the GDBGFIFOSPACE register. Note: - GDBGLTSSM register is not applicable for USB 2.0-only mode. - Bit Bash test should not be done on this debug register.

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Table 14-12330. Instance Table

Instance Name	Physical Address
USB0	3100 C164h

Figure 14-6092. USB2SS_GBL_GDBGLTSSM Name Register

31	30	29	28	27	26	25	24
RESERVED_31_31	RXELECIDLE	X3_XS_SWAPPING	X3_DS_HOST_SHUTDOWN	PRTDIRECTION	LTDBTIMEOUT	LTDBLINKSTATE	
R	R	R	R	R	R	R	
0h	1h	0h	0h	0h	0h	4h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LTDBLINKSTATE		LTDBSUBSTATE				ELASTICBUFFERMODE	TXELECLDLE
R		R				R	R
4h		0h				0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RXPOLARITY	TXDETRXLOOPBACK	LTDBPHYCMDSTATE			POWERDOWN		RXEQTRAIN
R	R	R			R		R
0h	0h	0h			2h		0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXDEEMPHASIS		LTDBCLKSTATE			TXSWING	RXTERMINATION	TXONESZEROS
R		R			R	R	R
1h		0h			0h	0h	0h

Table 14-12331. USB2SS_GBL_GDBGLTSSM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_31_31	R	0h	Reserved
30	RXELECIDLE	R	1h	RxElecidle For description of RxElecIdle, see table 5-4, "Status Interface Signals" of the PIPE3 Specification. Reset Source: rst_mod_g_rst_n
29	X3_XS_SWAPPING	R	0h	Reserved Reset Source: rst_mod_g_rst_n
28	X3_DS_HOST_SHUTDOWN	R	0h	Reserved Reset Source: rst_mod_g_rst_n
27	PRTDIRECTION	R	0h	Reserved Reset Source: rst_mod_g_rst_n
26	LTDBTIMEOUT	R	0h	LTDB Timeout [LTDBTimeout] Reset Source: rst_mod_g_rst_n
25:22	LTDBLINKSTATE	R	4h	LTDB Link State [LTDBLinkState] Reset Source: rst_mod_g_rst_n

Table 14-12331. USB2SS_GBL_GDBGLTSSM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:18	LTDBSUBSTATE	R	0h	LTDB Sub-State [LTDBSubState] Reset Source: rst_mod_g_rst_n
17	ELASTICBUFFERMODE	R	0h	Elastic Buffer Mode [ElasticBufferMode] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
16	TXELECLDLE	R	1h	Tx Elec Idle [TxElecIdle] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
15	RXPOLARITY	R	0h	Rx Polarity [RxPolarity] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
14	TXDETRXLOOPBACK	R	0h	Tx Detect Rx/Loopback [TxDetRxLoopback] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
13:11	LTDBPHYCMDSTATE	R	0h	LTSSM PHY command State [LTDBPhyCmdState] - 000: PHY_IDLE [PHY command state is in IDLE. No PHY request pending] - 001: PHY_DET [Request to start Receiver detection] - 010: PHY_DET_3 [Wait for Phy_Status [Receiver detection]] - 011: PHY_PWR_DLY [Delay Pipe3_PowerDown P0 -> P1/P2/P3 request] - 100: PHY_PWR_A [Delay for internal logic] - 101: PHY_PWR_B [Wait for Phy_Status[Power state change request]] Reset Source: rst_mod_g_rst_n
10:9	POWERDOWN	R	2h	POWERDOWN [PowerDown] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
8	RXEQTRAIN	R	0h	RxEq Train For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
7:6	TXDEEMPHASIS	R	1h	TXDEEMPHASIS [TxDeemphasis] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
5:3	LTDBCLKSTATE	R	0h	LTSSM Clock State [LTDBClkState] In multi-port host configuration, the port number is defined by Port-Select[3:0] field in the GDBGFIFOSPACE register. Note: GDBGLTSSM register is not applicable for USB 2.0-only mode. - 000: CLK_NORM [PHY is in non-P3 state and PCLK is running] - 001: CLK_TO_P3 [P3 entry request to PHY]. - 010: CLK_WAIT1 [Wait for Phy_Status [P3 request]]. - 011: CLK_P3 [PHY is in P3 and PCLK is not running]. - 100: CLK_TO_P0 [P3 exit request to PHY]. - 101: CLK_WAIT2 [Wait for Phy_Status [P3 exit request]] Reset Source: rst_mod_g_rst_n
2	TXSWING	R	0h	Tx Swing [TxSwing] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n
1	RXTERMINATION	R	0h	Rx Termination [RxTermination] For details on DWC_USB3_PIPE_RXTERM_RESET_VAL, refer to <workspace>/src/DWC_usb3_params.v Reset Source: rst_mod_g_rst_n
0	TXONESZEROS	R	0h	Tx Ones/Zeros [TxOnesZeros] For field definition, refer to Table 5-3 of the PIPE3 specification. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.320 USB2SS_GBL_GDBGLNMCC Register

14.7.3.2.2.320.1 USB2SS_GBL_GDBGLNMCC Register (Offset = 68h) [reset = 0h]

Global Debug LNMCC Register Bit Bash test should not be done on this debug register.

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Table 14-12332. Instance Table

Instance Name	Physical Address
USB0	3100 C168h

Figure 14-6093. USB2SS_GBL_GDBGLNMCC Name Register

31	30	29	28	27	26	25	24
RESERVED_31_9							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_9							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_9							LNMCC_BERC
R							R
0h							0h
7	6	5	4	3	2	1	0
LNMCC_BERC							
R							
0h							

Table 14-12333. USB2SS_GBL_GDBGLNMCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_31_9	R	0h	Reserved
8:0	LNMCC_BERC	R	0h	This field indicates the bit error rate information for the port selected in the GDBGFIFOSPACE.PortSelect field. This field is for debug purposes only. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.321 USB2SS_GBL_GDBGBMU Register

14.7.3.2.2.321.1 USB2SS_GBL_GDBGBMU Register (Offset = 6Ch) [reset = 0h]

Global Debug BMU Register Bit Bash test should not be done on this debug register.

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Table 14-12334. Instance Table

Instance Name	Physical Address
USB0	3100 C16Ch

Figure 14-6094. USB2SS_GBL_GDBGBMU Name Register

31	30	29	28	27	26	25	24
BMU_BCU							
R							
0h							
23	22	21	20	19	18	17	16
BMU_BCU							
R							
0h							
15	14	13	12	11	10	9	8
BMU_BCU							
R							
0h							
7	6	5	4	3	2	1	0
BMU_DCU				BMU_CCU			
R				R			
0h				0h			

Table 14-12335. USB2SS_GBL_GDBGBMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	BMU_BCU	R	0h	BMU_BCU Debug information Reset Source: rst_mod_g_rst_n
7:4	BMU_DCU	R	0h	BMU_DCU Debug information Reset Source: rst_mod_g_rst_n
3:0	BMU_CCU	R	0h	BMU_CCU Debug information Reset Source: rst_mod_g_rst_n

14.7.3.2.2.322 USB2SS_GBL_GDBGLSPMUX_HST Register

14.7.3.2.2.322.1 USB2SS_GBL_GDBGLSPMUX_HST Register (Offset = 70h) [reset = 3F0000h]

Global Debug LSP MUX Register - Host This register is for internal use only. If DWC_USB3_PRESERVE_LOGIC_ANALYZER_SELECT is enabled during controller configuration, then the default values readout is X (Undefined). Bit Bash test should not be done on this debug register.

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Table 14-12336. Instance Table

Instance Name	**Physical Address**
USB0	3100 C170h

Figure 14-6095. USB2SS_GBL_GDBGLSPMUX_HST Name Register

31	30	29	28	27	26	25	24
RESERVED_31_24							
R							
0h							
23	22	21	20	19	18	17	16
LOGIC_ANALYZER_TRACE							
R/W							
3Fh							
15	14	13	12	11	10	9	8
RESERVED_15_14		HOSTSELECT					
R		R/W					
0h		0h					
7	6	5	4	3	2	1	0
HOSTSELECT							
R/W							
0h							

Table 14-12337. USB2SS_GBL_GDBGLSPMUX_HST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_31_24	R	0h	Reserved
23:16	LOGIC_ANALYZER_TRACE	R/W	3Fh	logic_analyzer_trace Port MUX Select Currently only bits[21:16] are used. For details on how the mux controls the debug traces, refer to the "assign logic_analyzer_trace =" code section in the DWC_usb3.v file. A value of 6'h3F drives 0s on the logic_analyzer_trace signal. If you plan to OR [instead using a mux] this signal with other trace signals in your system to generate a common trace signal, you can use this feature. Reset Source: rst_mod_g_rst_n
15:14	RESERVED_15_14	R	0h	Reserved
13:0	HOSTSELECT	R/W	0h	Device LSP Select Selects the LSP debug information presented in the GDBGLSP register in host mode. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.323 USB2SS_GBL_GDBGLSP Register

14.7.3.2.2.323.1 USB2SS_GBL_GDBGLSP Register (Offset = 74h) [reset = 0h]

Global Debug LSP Register This register is for internal debug purposes only. This register is for internal use only. If DWC_USB3_PRESERVE_LOGIC_ANALYZER_SELECT is enabled during controller configuration, then the default values readout is X (Undefined). Bit Bash test should not be done on this debug register.

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Table 14-12338. Instance Table

Instance Name	Physical Address
USB0	3100 C174h

Figure 14-6096. USB2SS_GBL_GDBGLSP Name Register

31	30	29	28	27	26	25	24
LSPDEBUG							
R							
0h							
23	22	21	20	19	18	17	16
LSPDEBUG							
R							
0h							
15	14	13	12	11	10	9	8
LSPDEBUG							
R							
0h							
7	6	5	4	3	2	1	0
LSPDEBUG							
R							
0h							

Table 14-12339. USB2SS_GBL_GDBGLSP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LSPDEBUG	R	0h	LSP Debug Information Reset Source: rst_mod_g_rst_n

14.7.3.2.2.324 USB2SS_GBL_GDBGEPINFO0 Register

14.7.3.2.2.324.1 USB2SS_GBL_GDBGEPINFO0 Register (Offset = 78h) [reset = 0h]

Global Debug Endpoint Information Register 0 This register is for internal use only. If DWC_USB3_PRESERVE_LOGIC_ANALYZER_SELECT is enabled during controller configuration, then the default values readout is X (Undefined). Bit Bash test should not be done on this debug register.

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Table 14-12340. Instance Table

Instance Name	Physical Address
USB0	3100 C178h

Figure 14-6097. USB2SS_GBL_GDBGEPINFO0 Name Register

31	30	29	28	27	26	25	24
EPDEBUG							
R							
0h							
23	22	21	20	19	18	17	16
EPDEBUG							
R							
0h							
15	14	13	12	11	10	9	8
EPDEBUG							
R							
0h							
7	6	5	4	3	2	1	0
EPDEBUG							
R							
0h							

Table 14-12341. USB2SS_GBL_GDBGEPINFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPDEBUG	R	0h	Endpoint Debug Information, bits[31:0] Reset Source: rst_mod_g_rst_n

14.7.3.2.2.325 USB2SS_GBL_GDBGEPINFO1 Register

14.7.3.2.2.325.1 USB2SS_GBL_GDBGEPINFO1 Register (Offset = 7Ch) [reset = 800000h]

Global Debug Endpoint Information Register 1 This register is for internal use only. If DWC_USB3_PRESERVE_LOGIC_ANALYZER_SELECT is enabled during controller configuration, then the default values readout is X (Undefined). Bit Bash test should not be done on this debug register.

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Table 14-12342. Instance Table

Instance Name	Physical Address
USB0	3100 C17Ch

Figure 14-6098. USB2SS_GBL_GDBGEPINFO1 Name Register

31	30	29	28	27	26	25	24
EPDEBUG							
R							
800000h							
23	22	21	20	19	18	17	16
EPDEBUG							
R							
800000h							
15	14	13	12	11	10	9	8
EPDEBUG							
R							
800000h							
7	6	5	4	3	2	1	0
EPDEBUG							
R							
800000h							

Table 14-12343. USB2SS_GBL_GDBGEPINFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPDEBUG	R	800000h	Endpoint Debug Information, bits[63:32] Reset Source: rst_mod_g_rst_n

14.7.3.2.2.326 USB2SS_GBL_GPRTBIMAP_HSLO Register

14.7.3.2.2.326.1 USB2SS_GBL_GPRTBIMAP_HSLO Register (Offset = 80h) [reset = 0h]

Global High-Speed Port to Bus Instance Mapping Register - Low This is an alternate register for the GPRTBIMAP_HS register. - Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. Note: For reset values, refer to the corresponding values in the GPRTBIMAP_HS register.

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Table 14-12344. Instance Table

Instance Name	Physical Address
USB0	3100 C180h

Figure 14-6099. USB2SS_GBL_GPRTBIMAP_HSLO Name Register

31	30	29	28	27	26	25	24
BINUM8				BINUM7			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BINUM6				BINUM5			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BINUM4				BINUM3			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BINUM2				BINUM1			
R				R/W			
0h				0h			

Table 14-12345. USB2SS_GBL_GPRTBIMAP_HSLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	BINUM8	R	0h	BINUM8: HS USB Instance Number for Port 8. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
27:24	BINUM7	R	0h	BINUM7: HS USB Instance Number for Port 7. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM6	R	0h	BINUM6 USB Instance Number for Port 6. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM5	R	0h	BINUM5: HS USB Instance Number for Port 5. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM4	R	0h	BINUM4: HS USB Instance Number for Port 4. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
11:8	BINUM3	R	0h	BINUM3: HS USB Instance Number for Port 3. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-12345. USB2SS_GBL_GPRTBIMAP_HSLO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	BINUM2	R	0h	BINUM2: HS USB Instance Number for Port 2. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM1	R/W	0h	BINUM1: HS USB Instance Number for Port 1. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.327 USB2SS_GBL_GPRTBIMAP_HSHI Register

14.7.3.2.2.327.1 USB2SS_GBL_GPRTBIMAP_HSHI Register (Offset = 84h) [reset = 0h]

Global High-Speed Port to Bus Instance Mapping Register - High This is an alternate register for the GPRTBIMAP_HS register. - Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. Note: For reset values, refer to the corresponding values in the GPRTBIMAP register.

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Table 14-12346. Instance Table

Instance Name	Physical Address
USB0	3100 C184h

Figure 14-6100. USB2SS_GBL_GPRTBIMAP_HSHI Name Register

31	30	29	28	27	26	25	24
RESERVED_31_28				BINUM15			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
BINUM14				BINUM13			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
BINUM12				BINUM11			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
BINUM10				BINUM9			
R				R			
0h				0h			

Table 14-12347. USB2SS_GBL_GPRTBIMAP_HSHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_31_28	R	0h	Reserved
27:24	BINUM15	R	0h	BINUM15: HS USB Instance Number for Port 15. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM14	R	0h	BINUM14: HS USB Instance Number for Port 14. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM13	R	0h	BINUM13: HS USB Instance Number for Port 13. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM12	R	0h	BINUM12: HS USB Instance Number for Port 12. SApplication-programmable ID field. Reset Source: rst_mod_g_rst_n
11:8	BINUM11	R	0h	BINUM11: HS USB Instance Number for 11. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
7:4	BINUM10	R	0h	BINUM10: HS USB Instance Number for Port 10. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-12347. USB2SS_GBL_GPRTBIMAP_HSHI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	BINUM9	R	0h	BINUM9: HS USB Instance Number for Port 9. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.328 USB2SS_GBL_GPRTBIMAP_FSLO Register

14.7.3.2.2.328.1 USB2SS_GBL_GPRTBIMAP_FSLO Register (Offset = 88h) [reset = 0h]

Global Full-Speed Port to Bus Instance Mapping Register - Low This is an alternate register for the GPRTBIMAP_FS register. - Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. Note: For reset values, refer to the corresponding values in the GPRTBIMAP_FS register.

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Table 14-12348. Instance Table

Instance Name	Physical Address
USB0	3100 C188h

Figure 14-6101. USB2SS_GBL_GPRTBIMAP_FSLO Name Register

31	30	29	28	27	26	25	24
BINUM8				BINUM7			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
BINUM6				BINUM5			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
BINUM4				BINUM3			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
BINUM2				BINUM1			
R				R/W			
0h				0h			

Table 14-12349. USB2SS_GBL_GPRTBIMAP_FSLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	BINUM8	R	0h	BINUM8: FS USB Instance Number for Port 8. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
27:24	BINUM7	R	0h	BINUM7: FS USB Instance Number for Port 7. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
23:20	BINUM6	R	0h	BINUM6: FS USB Instance Number for Port 6. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
19:16	BINUM5	R	0h	BINUM5: FS USB Instance Number for Port 5. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
15:12	BINUM4	R	0h	BINUM4: FS USB Instance Number for Port 4. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
11:8	BINUM3	R	0h	BINUM3: FS USB Instance Number for Port 3. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

Table 14-12349. USB2SS_GBL_GPRTBIMAP_FSLO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	BINUM2	R	0h	BINUM2: FS USB Instance Number for Port 2. Application-programmable ID field. Reset Source: rst_mod_g_rst_n
3:0	BINUM1	R/W	0h	BINUM1: FS USB Instance Number for Port 1. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.329 USB2SS_GBL_GPRTBIMAP_FSHI Register

14.7.3.2.2.329.1 USB2SS_GBL_GPRTBIMAP_FSHI Register (Offset = 8Ch) [reset = 0h]

Global Full-Speed Port to Bus Instance Mapping Register - High This is an alternate register for the GPRTBIMAP_FS register. - Register fields are read-write with respect to number of port instantiated. writeAsRead constraint is added to limit side effects for unused fields. Note: For reset values, refer to the corresponding values in the GPRTBIMAP_FS register.

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Table 14-12350. Instance Table

Instance Name	Physical Address
USB0	3100 C18Ch

Figure 14-6102. USB2SS_GBL_GPRTBIMAP_FSHI Name Register

31	30	29	28	27	26	25	24
RESERVED_31_28				BINUM15			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
BINUM14				BINUM13			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
BINUM12				BINUM11			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
BINUM10				BINUM9			
R				R			
0h				0h			

Table 14-12351. USB2SS_GBL_GPRTBIMAP_FSHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED_31_28	R	0h	Reserved
27:24	BINUM15	R	0h	BINUM15: FS USB Instance Number for Port 15. Application-programmable ID field Reset Source: rst_mod_g_rst_n
23:20	BINUM14	R	0h	BINUM14: FS USB Instance Number for Port 14. Application-programmable ID field Reset Source: rst_mod_g_rst_n
19:16	BINUM13	R	0h	BINUM13: FS USB Instance Number for Port 13. Application-programmable ID field Reset Source: rst_mod_g_rst_n
15:12	BINUM12	R	0h	BINUM12: FS USB Instance Number for Port 12. Application-programmable ID field Reset Source: rst_mod_g_rst_n
11:8	BINUM11	R	0h	BINUM11: FS USB Instance Number for Port 11. Application-programmable ID field Reset Source: rst_mod_g_rst_n
7:4	BINUM10	R	0h	BINUM10: FS USB Instance Number for Port 10. Application-programmable ID field Reset Source: rst_mod_g_rst_n

Table 14-12351. USB2SS_GBL_GPRTBIMAP_FSHI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	BINUM9	R	0h	BINUM9: FS USB Instance Number for Port 9. Application-programmable ID field. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.330 USB2SS_GBL_RESERVED_94 Register

14.7.3.2.2.330.1 USB2SS_GBL_RESERVED_94 Register (Offset = 94h) [reset = 0h]

Future Reserved Register at offset 0x94

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Table 14-12352. Instance Table

Instance Name	Physical Address
USB0	3100 C194h

Figure 14-6103. USB2SS_GBL_RESERVED_94 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-12353. USB2SS_GBL_RESERVED_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Future use Register field

14.7.3.2.2.331 USB2SS_GBL_RESERVED_98 Register

14.7.3.2.2.331.1 USB2SS_GBL_RESERVED_98 Register (Offset = 98h) [reset = 0h]

Future Reserved Register at offset 0x98

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Table 14-12354. Instance Table

Instance Name	Physical Address
USB0	3100 C198h

Figure 14-6104. USB2SS_GBL_RESERVED_98 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-12355. USB2SS_GBL_RESERVED_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Field for future use

14.7.3.2.2.332 USB2SS_GBL_GUCTL2 Register

14.7.3.2.2.332.1 USB2SS_GBL_GUCTL2 Register (Offset = 9Ch) [reset = 0h]

Global User Control Register 2: This register provides a few options for the software to control the controller behavior in the Host and device mode. Most of the options are used to improve inter-operability with different hosts and devices.

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Table 14-12356. Instance Table

Instance Name	Physical Address
USB0	3100 C19Ch

Figure 14-6105. USB2SS_GBL_GUCTL2 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_26						EN_HP_PM_TIMER	
R/W						R/W	
0h						0h	
23	22	21	20	19	18	17	16
EN_HP_PM_TIMER					NOLOWPWRDUR		
R/W					R/W		
0h					0h		
15	14	13	12	11	10	9	8
NOLOWPWRDUR	RST_ACTBITLATER	RESERVED_13	ENABLEEPCACHEEVICT	DISABLECFC	RXPINGDURATION		
R/W	R/W	R	R/W	R/W	R/W		
0h	0h	0h	0h	0h	0h		
7	6	5	4	3	2	1	0
RXPINGDURATION			TXPINGDURATION				
R/W			R/W				
0h			0h				

Table 14-12357. USB2SS_GBL_GUCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED_31_26	R/W	0h	Reserved
25:19	EN_HP_PM_TIMER	R/W	0h	This register field is used to set new HP and PM timers. - To enable PM timer, set GUCTL2[19] bit as 1. - To enable HP timer, set GUCTL2[20] bit as 1. Default value of HP timer is 4us when HP PM timer is not enabled. when new HP timer is enabled default value is 12us. Use GUCTL2[25:21] to specify HP timer value in microseconds. Reset Source: rst_mod_g_rst_n

Table 14-12357. USB2SS_GBL_GUCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:15	NOLOWPWRDUR	R/W	0h	No Low Power Duration [NOLOWPWRDUR] This bit is applicable for device mode only and is ignored in host mode. After starting a transfer on a SS ISOC endpoint, the application must program these bits to prevent the device to lose frame synchronization over a period of time. Based on this count-down counter, the device will wake itself from U1/U2 low power states. After entering to U0 state and receiving two ITPs [which will sync-up the host and the device], U1/U2 low power entry is allowed. Each count represents the duration in terms of milliseconds. For example, a value of 3 represents 3ms. Note: - To disable this feature, set this field to 4'b0. - These bits are applicable only in device mode and ignored in host mode. - Some xHCI hosts do not send ITPs when performing ISOC transfers when the link enters U1/U2 low power states. This causes the device to lose frame synchronization over a period of time resulting in ISOC packets being dropped. Reset Source: rst_mod_g_rst_n
14	RST_ACTBITLATER	R/W	0h	Enable clearing of the command active bit for the ENDXFER command after the command execution is completed. This bit is valid in device mode only. Reset Source: rst_mod_g_rst_n
13	RESERVED_13	R	0h	Reserved for future use
12	ENABLEEPCACHEEVICT	R/W	0h	Enable Evicting Endpoint cache after Flow Control for bulk endpoints. In 3.00a release, a performance enhancement was done to keep the non-stream capable bulk IN endpoint in cache after flow control. Setting this bit will disable this enhancement. This should be set only for debug purpose. Reset Source: rst_mod_g_rst_n
11	DISABLECFC	R/W	0h	Disable xHCI Errata Feature Contiguous Frame ID Capability This field controls the xHCI Errata feature Contiguous FrameID capability. When set, the xHCI HCCPARAMS1 bit 11 will be set to 0 indicating that CFC is not supported. Disable this feature only if your application cannot tolerate Misssed Service Error events for Isoc transfers, and your system latencies are large to cause Missed Service errors even if the software is following the Isochronous Thresholding rules. Reset Source: rst_mod_g_rst_n
10:5	RXPINGDURATION	R/W	0h	Recieve Ping Maximum Duration This field is relevant to Host mode and controls the maximum duration of received LFPS to be treated as a Ping LFPS. The Max duration of the Ping LFPS is controlled by programming this value and is in terms of 8 ns granularity. Eg: A value of 32 indicates 256 ns. Reset Source: rst_mod_g_rst_n
4:0	TXPINGDURATION	R/W	0h	Transmit Ping Maximum Duration This field is relevant to Device mode and controls the maximum duration for which the controller should instruct the PHY to transmit a Ping LFPS. The duration of the Ping LFPS is controlled by programming this value and is in terms of 8 ns granularity. Eg: A value of 13 indicates 104 ns. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.333 USB2SS_GBL_GHWPARAMS8 Register

14.7.3.2.2.333.1 USB2SS_GBL_GHWPARAMS8 Register (Offset = 500h) [reset = 660h]

This register contains the hardware configuration options

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Table 14-12358. Instance Table

Instance Name	Physical Address
USB0	3100 C600h

Figure 14-6106. USB2SS_GBL_GHWPARAMS8 Name Register

31	30	29	28	27	26	25	24
GHWPARAMS8_32_0							
R							
660h							
23	22	21	20	19	18	17	16
GHWPARAMS8_32_0							
R							
660h							
15	14	13	12	11	10	9	8
GHWPARAMS8_32_0							
R							
660h							
7	6	5	4	3	2	1	0
GHWPARAMS8_32_0							
R							
660h							

Table 14-12359. USB2SS_GBL_GHWPARAMS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GHWPARAMS8_32_0	R	660h	DWC_USB3_DCACHE_DEPTH_INFO Reset Source: rst_mod_g_rst_n

14.7.3.2.2.334 USB2SS_GBL_GUCTL3 Register

14.7.3.2.2.334.1 USB2SS_GBL_GUCTL3 Register (Offset = 50Ch) [reset = 0h]

Global User Control Register 3 This register provides a few options for the software to control the controller behavior in the Host mode. Most of the options are used to improve host inter-operability with different devices.

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Table 14-12360. Instance Table

Instance Name	Physical Address
USB0	3100 C60Ch

Figure 14-6107. USB2SS_GBL_GUCTL3 Name Register

31	30	29	28	27	26	25	24
RESERVED_31_17							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_17							SCH_PING_EARLY
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_15_0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_15_0							
R/W							
0h							

Table 14-12361. USB2SS_GBL_GUCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_31_17	R/W	0h	Reserved
16	SCH_PING_EARLY	R/W	0h	Enable SuperSpeed Ping Transaction Packet scheduling early in the microframe. This bit is valid in Host mode only. Reset Source: rst_mod_g_rst_n
15:0	RESERVED_15_0	R/W	0h	Reserved

14.7.3.2.2.335 USB2SS_GBL_GTXFIFOPRIDEV Register

14.7.3.2.2.335.1 USB2SS_GBL_GTXFIFOPRIDEV Register (Offset = 510h) [reset = 0h]

Global Device TX FIFO DMA Priority Register This register specifies the relative DMA priority level among the Device TXFIFOs (one per IN endpoint). Each register bit[n] controls the priority (1: high, 0: low) of each TXFIFO[n]. When multiple TXFIFOs compete for DMA service at a given time (that is, multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: - 1. High-priority TXFIFOs are granted access using round-robin arbitration - 2. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. When configuring periodic IN endpoints, software must set register bit[n]=1, where n is the TXFIFO assignment. This ensures that the DMA for isochronous or interrupt IN endpoints are prioritized over bulk or control IN endpoints. This register is present only when the controller is configured to operate in the device mode (includes DRD mode). The register size corresponds to the number of Device IN endpoints. Note - Since the device mode uses only one RXFIFO, there is no Device RXFIFO DMA Priority Register.

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Table 14-12362. Instance Table

Instance Name	Physical Address
USB0	3100 C610h

Figure 14-6108. USB2SS_GBL_GTXFIFOPRIDEV Name Register

31	30	29	28	27	26	25	24
RESERVED_31_N							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_31_N							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GTXFIFOPRIDEV							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GTXFIFOPRIDEV							
R/W							
0h							

Table 14-12363. USB2SS_GBL_GTXFIFOPRIDEV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_N	R	0h	Reserved
15:0	GTXFIFOPRIDEV	R/W	0h	Device TxFIFO priority Reset Source: rst_mod_g_rst_n

14.7.3.2.2.336 USB2SS_GBL_GTXFIFOPRIHST Register

14.7.3.2.2.336.1 USB2SS_GBL_GTXFIFOPRIHST Register (Offset = 518h) [reset = 0h]

Global Host TX FIFO DMA Priority Register This register specifies the relative DMA priority level among the Host TXFIFOs (one per USB bus instance) within the associated speed group (SS or HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of TXFIFO[n] within a speed group. When multiple TXFIFOs compete for DMA service at a given time (i.e., multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: - 1. Among the FIFOs in the same speed group (SS or HS/FSLS): a. High-priority TXFIFOs are granted access using round-robin arbitration b. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). - 2. The TX DMA arbiter prioritizes the SS speed group or HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the controller is configured to operate in the host mode (includes DRD mode). The register size corresponds to the number of configured USB bus instances. for example, in the default configuration, there are 3 USB bus instances (1 SS, 1 HS, and 1 FSLS).

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Table 14-12364. Instance Table

Instance Name	Physical Address
USB0	3100 C618h

Figure 14-6109. USB2SS_GBL_GTXFIFOPRIHST Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_16							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_16					GTXFIFOPRIHST		
R					R/W		
0h					0h		

Table 14-12365. USB2SS_GBL_GTXFIFOPRIHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_31_16	R	0h	Reserved
2:0	GTXFIFOPRIHST	R/W	0h	Host TxFIFO priority Reset Source: rst_mod_g_rst_n

14.7.3.2.2.337 USB2SS_GBL_GRXFIFOPRIHST Register

14.7.3.2.2.337.1 USB2SS_GBL_GRXFIFOPRIHST Register (Offset = 51Ch) [reset = 0h]

Global Host RX FIFO DMA Priority Register This register specifies the relative DMA priority level among the Host RXFIFOs (one per USB bus instance) within the associated speed group (SS or HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of RXFIFO[n] within a speed group. When multiple RXFIFOs compete for DMA service at a given time (i.e., multiple RXQs contain RX DMA requests and their corresponding RXFIFOs have data available), the RX DMA arbiter grants access on a packet-basis in the following manner: - 1. Among the FIFOs in the same speed group (SS or HS/FSLS): a. High-priority RXFIFOs are granted access using round-robin arbitration b. Low-priority RXFIFOs are granted access using round-robin arbitration only after high-priority RXFIFOs have no further processing to do (that is, either the RXQs are empty or the corresponding RXFIFOs do not have the required data). - 2. The RX DMA arbiter prioritizes the SS speed group or HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the controller is configured to operate in the host mode (includes DRD mode). The register size corresponds to the number of configured USB bus instances. for example, in the default configuration, there are 3 USB bus instances (1 SS, 1 HS, and 1 FSLS).

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Table 14-12366. Instance Table

Instance Name	Physical Address
USB0	3100 C61Ch

Figure 14-6110. USB2SS_GBL_GRXFIFOPRIHST Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_31_16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED_31_16</td><td colspan="3">GRXFIFOPRIHST</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-12367. USB2SS_GBL_GRXFIFOPRIHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_31_16	R	0h	Reserved
2:0	GRXFIFOPRIHST	R/W	0h	Host RxFIFO priority Reset Source: rst_mod_g_rst_n

14.7.3.2.2.338 USB2SS_GBL_GDMAHLRATIO Register

14.7.3.2.2.338.1 USB2SS_GBL_GDMAHLRATIO Register (Offset = 524h) [reset = 0h]

Global Host FIFO DMA High-Low Priority Ratio Register This register specifies the relative priority of the SS FIFOs with respect to the HS/FSLS FIFOs. The DMA arbiter prioritizes the HS/FSLS round-robin arbiter group every DMA High-Low Priority Ratio grants as indicated in the register separately for TX and RX. To illustrate, consider that all FIFOs are requesting access simultaneously, and the ratio is 4. SS gets priority for 4 packets, HS/FSLS gets priority for 1 packet, SS gets priority for 4 packets, HS/FSLS gets priority for 1 packet, and so on. If FIFOs from both speed groups are not requesting access simultaneously then, - if SS got grants 4 out of the last 4 times, then HS/FSLS get the priority on any future request. - if HS/FSLS got the grant last time, SS gets the priority on the next request. - if there is a valid request on either SS or HS/FSLS, a grant is always awarded. there is no idle. This register is present if the controller is configured to operate in host mode (includes DRD).

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Table 14-12368. Instance Table

Instance Name	Physical Address
USB0	3100 C624h

Figure 14-6111. USB2SS_GBL_GDMAHLRATIO Name Register

31	30	29	28	27	26	25	24
RESERVED_31_13							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_13							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_13			HSTRXFIFO				
R			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED_7_5			HSTTXFIFO				
R			R/W				
0h			0h				

Table 14-12369. USB2SS_GBL_GDMAHLRATIO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_31_13	R	0h	Reserved
12:8	HSTRXFIFO	R/W	0h	Host RXFIFO DMA High-Low Priority Reset Source: rst_mod_g_rst_n
7:5	RESERVED_7_5	R	0h	Reserved
4:0	HSTTXFIFO	R/W	0h	Host TXFIFO DMA High-Low Priority Reset Source: rst_mod_g_rst_n

14.7.3.2.2.339 USB2SS_GBL_GFLADJ Register

14.7.3.2.2.339.1 USB2SS_GBL_GFLADJ Register (Offset = 530h) [reset = 0h]

Global Frame Length Adjustment Register This register provides options for the software to control the controller behavior with respect to SOF (Start of Frame) and ITP (Isochronous Timestamp Packet) timers and frame timer functionality. It provides an option to override the fladj_30mhz_reg sideband signal. In addition, it enables running SOF or ITP frame timer counters completely from the ref_clk. This facilitates hardware LPM in host mode with the SOF or ITP counters being run from the ref_clk signal.

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Table 14-12370. Instance Table

Instance Name	Physical Address
USB0	3100 C630h

Figure 14-6112. USB2SS_GBL_GFLADJ Name Register

31	30	29	28	27	26	25	24
GFLADJ_REFCLK_240MHZDECR_PLS1	GFLADJ_REFCLK_240MHZ_DECR						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GFLADJ_REFCLK_LPM_SEL	RESERVED_22	GFLADJ_REFCLK_FLADJ					
R/W	R	R/W					
0h	0h	0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GFLADJ_REFCLK_FLADJ							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GFLADJ_30MHZ_SDBND_SEL	RESERVED_6	GFLADJ_30MHZ					
R/W	R	R/W					
0h	0h	0h					

Table 14-12371. USB2SS_GBL_GFLADJ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GFLADJ_REFCLK_240MHZDECR_PLS1	R/W	0h	GFLADJ_REFCLK_240MHZDECR_PLS1 This field indicates that the decrement value that the controller applies for each ref_clk must be GFLADJ_REFCLK_240MHZ_DECR and GFLADJ_REFCLK_240MHZ_DECR +1 alternatively on each ref_clk. Set this bit to a '1' only if GFLADJ_REFCLK_LPM_SEL is set to '1' and the fractional component of 240/ref_frequency is greater than or equal to 0.5. Examples: If the ref_clk is 19.2 MHz then - GUCTL.REF_CLK_PERIOD = 52 - GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = [240/19.2] = 12.5 - GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 1 If the ref_clk is 24 MHz then - GUCTL.REF_CLK_PERIOD = 41 - GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = [240/24] = 10 - GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 0 Reset Source: rst_mod_g_rst_n

Table 14-12371. USB2SS_GBL_GFLADJ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30:24	GFLADJ_REFCLK_240MHZ_DECR	R/W	0h	This field indicates the decrement value that the controller applies for each ref_clk in order to derive a frame timer in terms of a 240-MHz clock. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to '1'. The value is derived as follows: GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency Examples: If the ref_clk is 24 MHz then - GUCTL.REF_CLK_PERIOD = 41 - GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/24 = 10 If the ref_clk is 48 MHz then - GUCTL.REF_CLK_PERIOD = 20 - GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/48 = 5 If the ref_clk is 17 MHz then - GUCTL.REF_CLK_PERIOD = 58 - GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/17 = 14 Reset Source: rst_mod_g_rst_n
23	GFLADJ_REFCLK_LPM_SEL	R/W	0h	This bit enables the functionality of running SOF/ITP counters on the ref_clk. This bit must not be set to '1' if GCTL.SOFITPSYNC bit is set to '1'. Similarly, if GFLADJ_REFCLK_LPM_SEL set to '1', GCTL.SOFITPSYNC must not be set to '1'. In device mode, setting this bit to '1' enables SOF tracking using ref_clk. When GFLADJ_REFCLK_LPM_SEL is set to '1' the overloading of the suspend control of the USB 2.0 first port PHY [UTMI/ULPI] with USB 3.0 port states is removed. For example, for Synopsys PHY, the COMMONONN signal can be tied to '1'. Note that the ref_clk frequencies supported in this mode are 16/17/19.2/20/24/39.7/40 MHz. The utmi_clk[0] signal of the controller must be connected to the FREECLK of the PHY. Note: If you set this bit to '1', the GUSB2PHYCFG.U2_FREECLK_EXISTS bit must be set to '0'. Reset Source: rst_mod_g_rst_n
22	RESERVED_22	R	0h	Reserved for future use
21:8	GFLADJ_REFCLK_FLADJ	R/W	0h	This field indicates the frame length adjustment to be applied when SOF/ITP counter is running on the ref_clk. This register value is used to adjust the ITP interval when GCTL[SOFITPSYNC] is set to '1'. SOF and ITP interval when GLADJ.GFLADJ_REFCLK_LPM_SEL is set to '1'. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to '1' or GCTL.SOFITPSYNC is set to '1'. The value is derived as follows: FLADJ_REF_CLK_FLADJ=[[125000/ref_clk_period_integer]-[125000/ref_clk_period]] * ref_clk_period where - the ref_clk_period_integer is the integer value of the ref_clk period got by truncating the decimal [fractional] value that is programmed in the GUCTL.REF_CLK_PERIOD field. - the ref_clk_period is the ref_clk period including the fractional value. Examples: If the ref_clk is 24 MHz then - GUCTL.REF_CLK_PERIOD = 41 - GFLADJ.GLADJ_REFCLK_FLADJ = [[125000/41]-[125000/41.6666]]*41.6666 = 2032 [ignoring the fractional value] If the ref_clk is 48 MHz then - GUCTL.REF_CLK_PERIOD = 20 - GFLADJ.GLADJ_REFCLK_FLADJ = [[125000/20]-[125000/20.8333]]*20.8333 = 5208 [ignoring the fractional value] Reset Source: rst_mod_g_rst_n
7	GFLADJ_30MHZ_SDBND_SEL	R/W	0h	GFLADJ_30MHZ_SDBND_SEL This field selects whether to use the input signal fladj_30mhz_reg or the GFLADJ.GFLADJ_30MHZ to adjust the frame length for the SOF/ITP. When this bit is set to, - 1, the controller uses the register field GFLADJ.GFLADJ_30MHZ value - 0, the controller uses the input signal fladj_30mhz_reg value Reset Source: rst_mod_g_rst_n
6	RESERVED_6	R	0h	Reserved for future use

Table 14-12371. USB2SS_GBL_GFLADJ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GFLADJ_30MHZ	R/W	0h	GFLADJ_30MHZ This field indicates the value that is used for frame length adjustment instead of considering from the sideband input signal fladj_30mhz_reg. This enables post-silicon frame length adjustment in case the input signal fladj_30mhz_reg is connected to a wrong value or is not valid. For details on how to set this value, refer to section 5.2.4, "Frame Length Adjustment Register [FLADJ]," of the xHCI Specification. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.340 USB2SS_GBL_GPHY_GUSB2PHYCFG Register

14.7.3.2.2.340.1 USB2SS_GBL_GPHY_GUSB2PHYCFG Register (Offset = 100h) [reset = 102400h]

Global USB2 PHY Configuration Register The application must program this register before starting any transactions on either the SoC bus or the USB. In Device-only configurations, only one register is needed. In Host mode, per-port registers are implemented.

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Table 14-12372. Instance Table

Instance Name	Physical Address
USB0	3100 C200h + formula

Figure 14-6113. USB2SS_GBL_GPHY_GUSB2PHYCFG Name Register

31	30	29	28	27	26	25	24
PHYSOFTRST	U2_FREECLK_EXISTS	ULPI_LPM_WITH_OPMODE_CHK	HSIC_CON_WIDTH_ADJ		INV_SEL_HSIC	OVRD_FSLS_DISC_TIME	LSTRD
R/W	R/W	R/W	R		R	R/W	R/W
0h	0h	0h	0h		0h	0h	0h
23	22	21	20	19	18	17	16
LSTRD		LSIPD			ULPIEXTVBUSINDIACTOR	ULPIEXTVBUSDRV	RESERVED_16
R/W		R/W			R/W	R/W	R
0h		2h			0h	0h	0h
15	14	13	12	11	10	9	8
ULPIAUTORES	RESERVED_14	USBTRDTIM				XCVRDLY	ENBLSLPM
R/W	R	R/W				R/W	R/W
0h	0h	9h				0h	0h
7	6	5	4	3	2	1	0
PHYSEL	SUSPENDUSB20	FSINTF	ULPI_UTMI_SEL	PHYIF	TOUTCAL		
W	R/W	R	R	R/W	R/W		
0h	0h	0h	0h	0h	0h		

Table 14-12373. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHYSOFTRST	R/W	0h	UTMI PHY Soft Reset [PHYSoftRst] Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI because ULPI PHYs are reset via their FunctionControl.Reset register, and the controller automatically writes to this register when the controller is reset [vcc_reset_n, USBCMD.HCRST, DCTL.SoftReset, or GCTL.SoftReset] Reset Source: rst_mod_g_rst_n
30	U2_FREECLK_EXISTS	R/W	0h	U2_FREECLK_EXISTS Specifies whether your USB 2.0 PHY provides a free-running PHY clock, which is active when the clock control input is active. If your USB 2.0 PHY provides a free-running PHY clock, it must be connected to the utmi_clk[0] input. The remaining utmi_clk[n] must be connected to the respective port clocks. The controller uses the Port-0 clock for generating the internal mac2 clock. - 1'b0: USB 2.0 free clock does not exist - 1'b1: USB 2.0 free clock exists Note: When the controller is configured as device-only [DWC_USB3_MODE = 0], do not set this bit to 1. Reset Source: rst_mod_g_rst_n

Table 14-12373. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	ULPI_LPM_WITH_OPMODE_CHK	R/W	0h	ULPI_LPM_WITH_OPMODE_CHK Support the LPM over ULPI without NOPID token to the ULPI PHY. If this bit is set, the ULPI PHY is expected to qualify the EXT PID with OPMODE=2'b00 for LPM and not treat it as a NOPID. Check with your PHY vendor about your PHY behavior. This bit is valid only when the DWC_USB3_HSPHY_INTERFACE parameter is 2 or 3. - 1'b0: A NOPID is sent before sending an EXTPID for LPM. - 1'b1: An EXTPID is sent without previously sending a NOPID. Note: This bit is valid only in host mode. This bit should be '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
28:27	HSIC_CON_WIDTH_ADJ	R	0h	HSIC_CON_WIDTH_ADJ This bit is used in the HSIC device mode of operation. By default, the connect duration for the HSIC device controller is thrice the strobe period. You can change this duration to 4, 5, or 6 times the strobe period by setting the value of this field to 1, 2, or 3. This value is added to the default connect duration. Reset Source: rst_mod_g_rst_n
26	INV_SEL_HSIC	R	0h	INV_SEL_HSIC The application driver uses this bit to control the HSIC enable/disable function. When set to '1', this bit overrides and functionally inverts the "if_select_hsic" input signal. If {INV_SEL_HSIC, if_select_hsic} is: - 00: HSIC Capability is disabled. - 01: HSIC Capability is enabled. - 10: HSIC Capability is enabled. - 11: HSIC Capability is disabled. If the controller operates as non-HSIC-capable, it can only connect to non-HSIC-capable PHYs. If it operates as HSIC-capable, it can connect to HSIC-capable PHYs. This bit is reserved if the DWC_USB3_ENABLE_HSIC parameter is set to '0'. When selecting the HSIC feature, set the host side to HSIC mode first, then set the device mode side. If the device side is set to HSIC mode first and if the host does not see a connection in HSIC mode, then you must de-select the device HSIC mode and select it again using the if_select_hsic setting or register bit GUSB2PHYCFGn[26] to ensure that the device can connect to the host. Reset Source: rst_mod_g_rst_n
25	OVRD_FSLS_DISC_TIME	R/W	0h	Overriding the FS/LS disconnect time to 32us. - If this value is 0, the FS/LS disconnect time is set to 2.5us as per the USB specification. - If this value is non-0, the disconnect detection time is set to 32us. Normally, this value is set to 0. However, if the USB 2.0 PHYs introduce noise on the UTMI linestate and cause SE0 glitches longer than 2.5us, then a false disconnect condition may get triggered. To avoid interoperability issues with these PHYs, this bit can be set to 1. Reset Source: rst_mod_g_rst_n
24:22	LSTRD	R/W	0h	LS Turnaround Time [LSTRDTIM] This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: - 0: 2 bit times - 1: 2.5 bit times - 2: 3 bit times - 3: 3.5 bit times - 4: 4 bit times - 5: 4.5 bit times - 6: 5 bit times - 7: 5.5 bit times Note: - This field is applicable only in Host mode. - For normal operation [to work with most LS devices], set the default value of this field to 3'h0 [2 bit times]. - The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the Open LS mouse requires 3 bit times of inter-packet gap to work correctly. - Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY's TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay [~1 LS bit time] from the device's delay requirement. Reset Source: rst_mod_g_rst_n

Table 14-12373. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:19	LSIPD	R/W	2h	LS Inter-Packet Time [LSIPD] This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows: - 0: 2 bit times - 1: 2.5 bit times - 2: 3 bit times - 3: 3.5 bit times - 4: 4 bit times - 5: 4.5 bit times - 6: 5 bit times - 7: 5.5 bit times Note: - This field is applicable only in Host mode. - For normal operation [to work with most LS devices], set the default value of this field to 3'h2 [3 bit times]. - The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly. - Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY's TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay [~1 LS bit time] from the device's delay requirement. Reset Source: rst_mod_g_rst_n
18	ULPIEXTVBUSINDIACTOR	R/W	0h	ULPI External VBUS Indicator [ULPIExtVbusIndicator] Indicates the ULPI PHY VBUS over-current indicator. - 1'b0: PHY uses an internal VBUS valid comparator. - 1'b1: PHY uses an external VBUS valid comparator. Valid only when RTL parameter DWC_USB3_HSPHY_INTERFACE = 2 or 3 Reset Source: rst_mod_g_rst_n
17	ULPIEXTVBUSDRV	R/W	0h	ULPI External VBUS Drive [ULPIExtVbusDrv] Selects supply source to drive 5V on VBUS, in the ULPI PHY. - 1'b0: PHY drives VBUS with internal charge pump [default]. - 1'b1: PHY drives VBUS with an external supply. [Only when RTL parameter DWC_USB3_HSPHY_INTERFACE = 2 or 3] Reset Source: rst_mod_g_rst_n
16	RESERVED_16	R	0h	Reserved
15	ULPIAUTORES	R/W	0h	ULPI Auto Resume [ULPIAutoRes] Sets the AutoResume bit in Interface Control register on the ULPI PHY. - 1'b0: PHY does not use the AutoResume feature. - 1'b1: PHY uses the AutoResume feature. Valid only when RTL parameter DWC_USB3_HSPHY_INTERFACE = 2 or 3 Reset Source: rst_mod_g_rst_n
14	RESERVED_14	R	0h	Reserved
13:10	USBTRDTIM	R/W	9h	USB 2.0 Turnaround Time [USBTrdTim] Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller [PFC] to fetch data from the DFIFO [SPRAM]. The following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: - 4'h5: When the MAC interface is 16-bit UTMI+. - 4'h9: When the MAC interface is 8-bit UTMI+/ULPI. If SoC bus clock is less than 60 MHz, and USB turnaround time is not critical, this field can be set to a larger value. Note: This field is valid only in device mode. Reset Source: rst_mod_g_rst_n
9	XCVRDLY	R/W	0h	Transceiver Delay: Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal [for HS] and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay [of approximately 2.5 us] is introduced from the time when the Transceiver Select is set to 2'b00 [HS] to the time the TxValid is driven to 0 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. Note: - If you enable the hibernation feature when the device controller comes out of power-off, you must re-initialize this bit with the appropriate value because the controller does not save and restore this bit value during hibernation. - This bit is valid only in device mode. Reset Source: rst_mod_g_rst_n

Table 14-12373. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ENBLSLPM	R/W	0h	Enable utmi_sleep_n and utmi_l1_suspend_n [EnblSlpM] The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the L1 state. - 1'b0: utmi_sleep_n and utmi_l1_suspend_n assertion from the controller is not transferred to the external PHY. - 1'b1: utmi_sleep_n and utmi_l1_suspend_n assertion from the controller is transferred to the external PHY. Note: This bit must be set high for Port0 if Synopsys PHY is used. Note: In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk [utmi_clk/ulpi_clk] is gated off, the command will not get completed. Reset Source: rst_mod_g_rst_n
7	PHYSEL	W	0h	USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select The application uses this bit to select a high-speed PHY or a full-speed transceiver. - 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY. This bit is always 0, with Write Only access. - 1'b1: USB 1.1 full-speed serial transceiver. This bit is always 1, with Write Only access. If both interface types are selected in coreConsultant [that is, parameters' values are not zero], the application uses this bit to select the active interface is active, with Read-Write bit access. Note: USB 1.1 full-serial transceiver is not supported. This bit always reads as 1'b0. Reset Source: rst_mod_g_rst_n
6	SUSPENDUSB20	R/W	0h	Suspend USB2.0 HS/FS/LS PHY [SusPHY] When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. For DRD configurations, it is recommended that this bit is set to 0 during coreConsultant configuration. If it is set to 1, then the application must clear this bit after power-on reset. Application needs to set it to 1 after the controller initialization completes. For all other configurations, this bit can be set to 1 during controller configuration. Note: - In host mode, on reset, this bit is set to 1. Software can override this bit after reset. - In device mode, before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. If you issue a command without disabling this bit when the device is in L2 state and if mac2_clk [utmi_clk/ulpi_clk] is gated off, the command will not get completed. Reset Source: rst_mod_g_rst_n
5	FSINTF	R	0h	Full-Speed Serial Interface Select [FSIntf] The application uses this bit to select a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. - 1'b0: 6-pin unidirectional full-speed serial interface. This bit is set to 0 with Read Only access. - 1'b1: 3-pin bidirectional full-speed serial interface. This bit is set to 0 with Read Only access. Note: USB 1.1 full-speed serial interface is not supported. This bit always reads as 1'b0. Reset Source: rst_mod_g_rst_n
4	ULPI_UTMI_SEL	R	0h	ULPI or UTMI+ Select [ULPI_UTMI_Sel] The application uses this bit to select a UTMI+ or ULPI Interface. - 1'b0: UTMI+ Interface - 1'b1: ULPI Interface This bit is writable only if UTMI+ and ULPI is specified for High-Speed PHY Interface[s] in coreConsultant configuration [DWC_USB3_HSPHY_INTERFACE = 3]. Otherwise, this bit is read-only and the value depends on the interface selected through DWC_USB3_HSPHY_INTERFACE. Reset Source: rst_mod_g_rst_n

Table 14-12373. USB2SS_GBL_GPHY_GUSB2PHYCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PHYIF	R/W	0h	PHY Interface [PHYIf] If UTMI+ is selected, the application uses this bit to configure the controller to support a UTMI+ PHY with an 8- or 16-bit interface. - 1'b0: 8 bits - 1'b1: 16 bits ULPI Mode: 1'b0 Note: - All the enabled 2.0 ports must have the same clock frequency as Port0 clock frequency [utmi_clk[0]]. - The UTMI 8-bit and 16-bit modes cannot be used together for different ports at the same time [that is, all the ports must be in 8-bit mode, or all of them must be in 16-bit mode, at a time]. - If any of the USB 2.0 ports is selected as ULPI port for operation, then all the USB 2.0 ports must be operating at 60 MHz. Reset Source: rst_mod_g_rst_n
2:0	TOUTCAL	R/W	0h	HS/FS Timeout Calibration [TOutCal] The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor. this factor is added to the high-speed/full-speed interpacket timeout duration in the controller to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 [inclusive] bit times. The USB standard timeout value for full-speed operation is 16 to 18 [inclusive] bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: - One 30-MHz PHY clock = 16 bit times - One 60-MHz PHY clock = 8 bit times Full-speed operation: - One 30-MHz PHY clock = 0.4 bit times - One 60-MHz PHY clock = 0.2 bit times - One 48-MHz PHY clock = 0.25 bit times Reset Source: rst_mod_g_rst_n

14.7.3.2.2.341 USB2SS_GBL_GI2C_GUSB2I2CCTL Register

14.7.3.2.2.341.1 USB2SS_GBL_GI2C_GUSB2I2CCTL Register (Offset = 140h) [reset = 0h]

Reserved Register

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Table 14-12374. Instance Table

Instance Name	Physical Address
USB0	3100 C240h + formula

Figure 14-6114. USB2SS_GBL_GI2C_GUSB2I2CCTL Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-12375. USB2SS_GBL_GI2C_GUSB2I2CCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved for future use

14.7.3.2.2.342 USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Register

14.7.3.2.2.342.1 USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Register (Offset = 180h) [reset = 0h]

Global USB 2.0 ULPI PHY Vendor Control Register The application uses this register to access the PHY registers. This register is always implemented when the ULPI PHY Interface is enabled during coreConsultant configuration (parameter DWC_USB3_HSPHY_INTERFACE = 2 or 3). For an ULPI PHY, the controller uses the ULPI interface for PHY register access. The application sets the Vendor Control register for PHY register access and times the PHY register access. The application polls the VStatus Done bit in this register for the completion of the PHY register access. In Device-only configurations, only one register is needed. In Host mode, per-port registers are implemented.

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Table 14-12376. Instance Table

Instance Name	Physical Address
USB0	3100 C280h + formula

Figure 14-6115. USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RESERVED_31_27</td><td>DISUIPIDRVR</td><td>NEWREGREQ</td><td>VSTSDONE</td></tr>
<tr><td colspan="5">R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>VSTSBSY</td><td>REGWR</td><td colspan="6">REGADDR</td></tr>
<tr><td>R</td><td>R</td><td colspan="6">R</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">EXTREGADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">REGDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12377. USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED_31_27	R	0h	Reserved
26	DISUIPIDRVR	R	0h	DISUIPIDRVR Reset Source: rst_mod_g_rst_n
25	NEWREGREQ	R	0h	New Register Request The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n [1'b0] on the UTMI interface. Reset Source: rst_mod_g_rst_n
24	VSTSDONE	R	0h	VSTSDONE Reset Source: rst_mod_g_rst_n
23	VSTSBSY	R	0h	VSTSBSY Reset Source: rst_mod_g_rst_n
22	REGWR	R	0h	Register Write The application sets this bit for register writes and clears it for register reads. Note: This bit is applicable for ULPI register read/write access only. Reset Source: rst_mod_g_rst_n

Table 14-12377. USB2SS_GBL_GULPI_GUSB2PHYACC_ULPI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:16	REGADDR	R	0h	Register Address The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. Note: These bits are applicable for ULPI only. Reset Source: rst_mod_g_rst_n
15:8	EXTREGADDR	R	0h	EXTREGADDR Reset Source: rst_mod_g_rst_n
7:0	REGDATA	R	0h	REGDATA Reset Source: rst_mod_g_rst_n

14.7.3.2.2.343 USB2SS_GBL_GPIPE_GUSB3PIPECTL Register

14.7.3.2.2.343.1 USB2SS_GBL_GPIPE_GUSB3PIPECTL Register (Offset = 1C0h) [reset = 10C8002h]

Global USB 3.0 PIPE Control Register The application uses this register to configure the USB3 PHY and PIPE interface. Device-only configuration requires only one register. In Host mode, registers are implemented for each port. For more details on GUSB3PIPECTL(#n) bits, refer to section "GUSB3PIPECTLn Register" in the User Guide. Note: - GUSB3PIPECTLn registers are not applicable for USB 2.0-only mode.

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Table 14-12378. Instance Table

Instance Name	Physical Address
USB0	3100 C2C0h + formula

Figure 14-6116. USB2SS_GBL_GPIPE_GUSB3PIPECTL Name Register

31	30	29	28	27	26	25	24
PHYSOFTRST	HSTPRTCMPL	U2P3OK	DISRXDETP3	UX_EXIT_IN_PX	PING_ENHANCEMENT_EN	U1U2EXITFAIL_TO_RECOV	REQUEST_P1P2P3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h
23	22	21	20	19	18	17	16
STARTRXDETU3RXDET	DISRXDETU3RXDET	DELAYP1P2P3			DELAYP1TRANS	SUSPENDENABLE	DATWIDTH
W	R/W	R/W			R/W	R/W	R
0h	0h	1h			1h	0h	1h
15	14	13	12	11	10	9	8
DATWIDTH	ABORTRXDETINU2	SKIPRXDET	LFPSP0ALGN	P3P2TRANOK	P3EXSIGP2	LFPSFILTER	RX_DETECT_TO_POLLING_LFPS_CONTROL
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SSICEN	TX_SWING	TX_MARGIN			SS_TX_DE_EMPHASIS		ELASTIC_BUFFER_MODE
R/W	R/W	R/W			R/W		R/W
0h	0h	0h			1h		0h

Table 14-12379. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHYSOFTRST	R/W	0h	USB3 PHY Soft Reset After setting this bit to '1', the software needs to clear this bit. For more information, refer to Figure "Software Resets and PHY Clock Sequencing and Requirements" in the Databook. Reset Source: rst_mod_g_rst_n

Table 14-12379. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	HSTPRTCMPL	R/W	0h	HstPrtCmpl This feature tests the PIPE PHY compliance patterns without having to have a test fixture on the USB 3.0 cable. This bit enables placing the SS port link into a compliance state. By default, this bit must be set to 1'b0. In compliance lab testing, the SS port link enters compliance after failing the first polling sequence after power on. Set this bit to 0, when you run compliance tests. The sequence for using this functionality is as follows: - 1. Disconnect any plugged in devices. - 2. Perform USBCMD.HCRST or power-on-chip reset. - 3. Set PORTSC.PLS=0xA. - 4. Set PORTSC.PP=0. - 5. Set GUSB3PIPECTL. HstPrtCmpl=1. This places the link into compliance state. To advance the compliance pattern, follow this sequence [toggle the set GUSB3PIPECTL. HstPrtCmpl]: - 1. Set GUSB3PIPECTL.HstPrtCmpl=0. - 2. Set GUSB3PIPECTL.HstPrtCmpl=1. This advances the link to the next compliance pattern. To exit from the compliance state perform USBCMD.HCRST or power-on-chip reset. Reset Source: rst_mod_g_rst_n
29	U2P3OK	R/W	0h	P3 OK for SSInactive [SSIP3ok] - 0: During link state SS.Inactive, put PHY in P2 [Default] - 1: During link state SS.Inactive, put PHY in P3. Reset Source: rst_mod_g_rst_n
28	DISRXDETP3	R/W	0h	Disabled receiver detection in P3 [DisRxDetP3] - 0: If PHY is in P3 and controller needs to perform receiver detection, The controller performs receiver detection in P3. [Default] - 1: If PHY is in P3 and controller needs to perform receiver detection, The controller changes the PHY power state to P2 and then performs receiver detection. After receiver detection, the cores changes PHY power state to P3. Reset Source: rst_mod_g_rst_n
27	UX_EXIT_IN_PX	R/W	0h	Ux Exit in Px [Ux_exit_in_Px] - 0: The controller does U1/U2/U3 exit in PHY power state P0 [default behavior]. - 1: The controller does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
26	PING_ENHANCEMENT_EN	R/W	0h	Ping Enhancement Enable [ping_enhancement_en] When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns [one mac3_clk]. This field is valid for the downstream port only. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
25	U1U2EXITFAIL_TO_RECOV	R/W	0h	U1U2exitfail to Recovery [u1u2exitfail_to_recov] When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake. Reset Source: rst_mod_g_rst_n
24	REQUEST_P1P2P3	R/W	1h	Always Request P1/P2/P3 for U1/U2/U3 [request_p1p2p3] When set, the controller always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit [remotely initiated, or locally initiated] happens, the controller does not request P1/P2/P3 power state change. Note: This bit must be set to '1' for Synopsys PHY. For third-party SS PHY, check with your PHY vendor. Reset Source: rst_mod_g_rst_n

Table 14-12379. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	STARTRXDETU3RXDET	W	0h	Start Receiver Detection in U3/Rx.Detect [StartRxdetU3RxDet] If DWC_USB3_GUSB3PIPECTL_INIT[22] is set, and the link is in either U3 or Rx.Detect state, the controller starts receiver detection on the rising edge of this bit. This can only be used for Downstream ports. This bit must be set to '0' for Upstream ports. This feature must not be enabled for normal operation. If have to use this feature, contact Synopsys. Reset Source: rst_mod_g_rst_n
22	DISRXDETU3RXDET	R/W	0h	Disable Receiver Detection in U3/Rx.Det When set, the controller does not handle receiver detection in either U3 or Rx.Detect states. DWC_USB3_GUSB3PIPECTL_INIT[23] must be used to start receiver detection manually. This bit can only be used for the downstream port. This bit must be set to "0" for Upstream ports. This feature must not be enabled for normal operation. If you have to use this feature, contact Synopsys. Reset Source: rst_mod_g_rst_n
21:19	DELAYP1P2P3	R/W	1h	Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until [DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8] 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality. Reset Source: rst_mod_g_rst_n
18	DELAYP1TRANS	R/W	1h	Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. - 1'b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIdle is 1 and pipe3_RxValid is 0 - 1'b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIdle and pipe3_RxValid. Note: - If you are using Synopsys PHY, contact Synopsys Customer Support for recommendation on setting this bit because it is node dependent. - If you are using a third-party SS PHY, check with your PHY vendor for recommendation on setting this bit. Reset Source: rst_mod_g_rst_n
17	SUSPENDENABLE	R/W	0h	Suspend USB3.0 SS PHY [Suspend_en] When set, and if Suspend conditions are valid, the USB 3.0 PHY enters Suspend mode. For DRD configurations, it is recommended that this bit is set to '0' during coreConsultant configuration. If it is set to '1', then the application must clear this bit after power-on reset. Application needs to set it to '1' after the controller initialization is completed. For all other configurations, this bit can be set to '1' during controller configuration. Reset Source: rst_mod_g_rst_n
16:15	DATWIDTH	R	1h	PIPE Data Width [DatWidth] - 2'b00: 32 bits - 2'b01: 16 bits One clock after reset, these bits receive the value seen on the pipe3_DataBusWidth. The simulation testbench uses the coreConsultant parameter to configure the VIP. These bits in the coreConsultant parameter must match your PHY data width and the pipe3_DataBusWidth port. Note: 8-bit data width is not supported. Reset Source: rst_mod_g_rst_n
14	ABORTRXDETINU2	R/W	0h	Abort Rx Detect in U2 [AbortRxDetInU2] When set and the link state is U2, the controller will abort receiver detection if it receives U2 exit LFPS from the remote link partner. This bit is for the downstream port only. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
13	SKIPRXDET	R/W	0h	Skip Rx Detect: When set, the controller skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation. Reset Source: rst_mod_g_rst_n

Table 14-12379. USB2SS_GBL_GPIPE_GUSB3PIPECTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	LFPSP0ALGN	R/W	0h	LFPS P0 Align: When set, - The controller deasserts LFPS transmission on the clock edge that it requests Phy power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. - The controller requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state. Currently, this bit is only used in USB 3.0 HUB with Synopsys PHY. For other USB 3.0 Host, Device, and DRD cores, this bit is not required. Reset Source: rst_mod_g_rst_n
11	P3P2TRANOK	R/W	0h	P3 P2 Transitions OK [P3P2TranOK] When set, the controller transitions directly from Phy power state P2 to P3 or from state P3 to P2. When not set, P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE3 Specification. According to the PIPE3 Specification, any direct transition between P3 and P2 is illegal. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
10	P3EXSIGP2	R/W	0h	P3 Exit Signal in P2 [P3ExSigP2] When this bit is set, the controller always changes the PHY power state to P2, before attempting a U3 exit handshake. This bit is used only for some non-Synopsys PHYs that cannot do LFPS in P3. Note: This bit is used by third-party SS PHY. It must be set to '0' for Synopsys PHY. Reset Source: rst_mod_g_rst_n
9	LFPSFILTER	R/W	0h	LFPS Filter [LFPSFilt] When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted. Reset Source: rst_mod_g_rst_n
8	RX_DETECT_TO_POLLING_LFPS_CONTROL	R/W	0h	RX_DETECT to Polling.LFPS Control - 1'b0 [Default]: Enables a 400us delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. - 1'b1: Disables the 400us delay to start Polling LFPS after RX_DETECT. During controller certification with third party PHY it is observed that the PHY is not able to meet the Tx AC common mode voltage active [VTX-CM-ACPP_ACTIVE <100mv] if the link starts polling within 80us from the time rx.detect is performed. To meet this VTX-CM-ACPP_ACTIVE specification, the polling must be delayed further. If the PHY does not have issue then they can set this bit to 1 which allows polling to start within 80us. Reset Source: rst_mod_g_rst_n
7	SSICEN	R/W	0h	This field is not used. Reset Source: rst_mod_g_rst_n
6	TX_SWING	R/W	0h	Tx Swing [TxSwing] Refer to the PIPE3 specification. Reset Source: rst_mod_g_rst_n
5:3	TX_MARGIN	R/W	0h	Tx Margin[2:0] [TxMargin] Refer to Table 5-3 of the PIPE3 Specification. Reset Source: rst_mod_g_rst_n
2:1	SS_TX_DE_EMPHASIS	R/W	1h	Tx Deemphasis [TxDeemphasis] The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode. [Refer to Table 5-3 of the PIPE3 specification.] Reset Source: rst_mod_g_rst_n
0	ELASTIC_BUFFER_MODE	R/W	0h	Elastic Buffer Mode [ElasticBufferMode] [Refer to Table 5-3 of the PIPE3 specification.] Reset Source: rst_mod_g_rst_n

14.7.3.2.2.344 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0 Register

14.7.3.2.2.344.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0 Register (Offset = 200h) [reset = 593000Ch]

Global Transmit FIFO Size Register This register specifies the RAM start address and depth (both in MDWIDTH-bit words) for each implemented TxFIFO. The number of TxFIFOs depends on the configuration parameters including the number of Device IN Endpoints, number of Host Bus Instances, and presence of Debug Capability. The register default values for each mode are assigned in coreConsultant based on the maximum packet size, number of packets to be buffered, speed of host bus instance, bus latency, and mode of operation (host, device, or, DBC). Upon reset and mode transitions, hardware automatically programs these registers to the default values. Consequently, there is typically no need for the software to modify the pre-defined default values. For the debug capability mode, the currently mapped EP0 IN and EP1 IN TxFIFO numbers can be read from the GFIFOPRIDBC register. For more details on the usage of the GTXFIFOSIZn and GRXFIFOSIZn registers for different modes of operation, refer to "Memory Requirements" chapter in the Databook.

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Table 14-12380. Instance Table

Instance Name	Physical Address
USB0	3100 C300h + formula

Figure 14-6117. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TXFSTADDR_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">593h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TXFSTADDR_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">593h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TXFDEP_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">Ch</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TXFDEP_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">Ch</td></tr>
</table>

Table 14-12381. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	593h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	Ch	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.345 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1 Register

14.7.3.2.2.345.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1 Register (Offset = 204h) [reset = 59F0209h]

Register GTXFIFOSIZ 1

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Table 14-12382. Instance Table

Instance Name	Physical Address
USB0	3100 C304h + formula

Figure 14-6118. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
59Fh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
59Fh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-12383. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	59Fh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TXFDEP_N Reset Source: rst_mod_g_rst_n

14.7.3.2.2.346 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2 Register

14.7.3.2.2.346.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2 Register (Offset = 208h) [reset = 7A80209h]

Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words.

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Table 14-12384. Instance Table

Instance Name	Physical Address
USB0	3100 C308h + formula

Figure 14-6119. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TXFSTADDR_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7A8h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TXFSTADDR_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7A8h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TXFDEP_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">209h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TXFDEP_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">209h</td></tr>
</table>

Table 14-12385. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	7A8h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.347 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3 Register

14.7.3.2.2.347.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3 Register (Offset = 20Ch) [reset = 9B10209h]

Register GTXFIFOSIZ 3

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Table 14-12386. Instance Table

Instance Name	Physical Address
USB0	3100 C30Ch + formula

Figure 14-6120. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
9B1h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
9B1h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-12387. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	9B1h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TXFDEP_N: TxFIFO Depth [TxFDep_n] This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.348 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4 Register

14.7.3.2.2.348.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4 Register (Offset = 210h) [reset = BBA0209h]

Register GTXFIFOSIZ 4

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Table 14-12388. Instance Table

Instance Name	Physical Address
USB0	3100 C310h + formula

Figure 14-6121. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
BBAh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
BBAh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-12389. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	BBAh	TXFSTADDR_N Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TXFDEP_N: TxFIFO Depth [TxFDep_n] This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.349 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5 Register

14.7.3.2.2.349.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5 Register (Offset = 214h) [reset = DC30209h]

Register GTXFIFOSIZ 5

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Table 14-12390. Instance Table

Instance Name	Physical Address
USB0	3100 C314h + formula

Figure 14-6122. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
DC3h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
DC3h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-12391. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	DC3h	Transmit FIFOn RAM Start Address Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.350 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6 Register

14.7.3.2.2.350.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6 Register (Offset = 218h) [reset = FCC0209h]

Register GTXFIFOSIZ 6

Return to Summary Table

Table 14-12392. Instance Table

Instance Name	Physical Address
USB0	3100 C318h + formula

Figure 14-6123. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
FCCh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
FCCh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
209h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
209h							

Table 14-12393. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	FCCh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.351 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7 Register

14.7.3.2.2.351.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7 Register (Offset = 21Ch) [reset = 11D50209h]

Register GTXFIFOSIZ 7

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Table 14-12394. Instance Table

Instance Name	Physical Address
USB0	3100 C31Ch + formula

Figure 14-6124. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
11D5h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXFSTADDR_N							
R/W							
11D5h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXFDEP_N							
R/W							
209h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXFDEP_N							
R/W							
209h							

Table 14-12395. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	11D5h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	209h	TXFDEP_N This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.352 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8 Register

14.7.3.2.2.352.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8 Register (Offset = 220h) [reset = 13DE0105h]

Register GTXFIFOSIZ 8

Return to Summary Table

Table 14-12396. Instance Table

Instance Name	Physical Address
USB0	3100 C320h + formula

Figure 14-6125. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
13DEh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
13DEh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-12397. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	13DEh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.353 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9 Register

14.7.3.2.2.353.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9 Register (Offset = 224h) [reset = 14E30105h]

Register GTXFIFOSIZ 9

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Table 14-12398. Instance Table

Instance Name	Physical Address
USB0	3100 C324h + formula

Figure 14-6126. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
14E3h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXFSTADDR_N							
R/W							
14E3h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXFDEP_N							
R/W							
105h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXFDEP_N							
R/W							
105h							

Table 14-12399. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	14E3h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.354 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10 Register

14.7.3.2.2.354.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10 Register (Offset = 228h) [reset = 15E80105h]

GTXFIFOSIZ 10

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Table 14-12400. Instance Table

Instance Name	Physical Address
USB0	3100 C328h + formula

Figure 14-6127. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
15E8h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
15E8h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-12401. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	15E8h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TXFDEP_N: TxFIFO Depth [TxFDep_n] This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.355 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11 Register

14.7.3.2.2.355.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11 Register (Offset = 22Ch) [reset = 16ED0105h]

Register GTXFIFOSIZ 11

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Table 14-12402. Instance Table

Instance Name	Physical Address
USB0	3100 C32Ch + formula

Figure 14-6128. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
16EDh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXFSTADDR_N							
R/W							
16EDh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXFDEP_N							
R/W							
105h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXFDEP_N							
R/W							
105h							

Table 14-12403. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	16EDh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.356 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12 Register

14.7.3.2.2.356.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12 Register (Offset = 230h) [reset = 17F20105h]

GTXFIFOSIZ 12

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Table 14-12404. Instance Table

Instance Name	Physical Address
USB0	3100 C330h + formula

Figure 14-6129. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
17F2h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
17F2h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-12405. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	17F2h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TxFIFO Depth This field contains the depth of TxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 32,768 For more information, see "Integrating the Controller" chapter in the User Guide. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.357 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13 Register

14.7.3.2.2.357.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13 Register (Offset = 234h) [reset = 18F70105h]

Register GTXFIFOSIZ 13

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Table 14-12406. Instance Table

Instance Name	Physical Address
USB0	3100 C334h + formula

Figure 14-6130. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
18F7h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
18F7h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-12407. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	18F7h	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TXFDEP_N Reset Source: rst_mod_g_rst_n

14.7.3.2.2.358 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14 Register

14.7.3.2.2.358.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14 Register (Offset = 238h) [reset = 19FC0105h]

Register GTXFIFOSIZ 14

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Table 14-12408. Instance Table

Instance Name	Physical Address
USB0	3100 C338h + formula

Figure 14-6131. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
19FCh							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
19FCh							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-12409. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	19FCh	Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TXFDEP_N Reset Source: rst_mod_g_rst_n

14.7.3.2.2.359 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15 Register

14.7.3.2.2.359.1 USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15 Register (Offset = 23Ch) [reset = 1B010105h]

Register GTXFIFOSIZ 15

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Table 14-12410. Instance Table

Instance Name	Physical Address
USB0	3100 C33Ch + formula

Figure 14-6132. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15 Name Register

31	30	29	28	27	26	25	24
TXFSTADDR_N							
R/W							
1B01h							
23	22	21	20	19	18	17	16
TXFSTADDR_N							
R/W							
1B01h							
15	14	13	12	11	10	9	8
TXFDEP_N							
R/W							
105h							
7	6	5	4	3	2	1	0
TXFDEP_N							
R/W							
105h							

Table 14-12411. USB2SS_GBL_GTXFIFO_GTXFIFOSIZ15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TXFSTADDR_N	R/W	1B01h	TXFSTADDR_N Reset Source: rst_mod_g_rst_n
15:0	TXFDEP_N	R/W	105h	TXFDEP_N Reset Source: rst_mod_g_rst_n

14.7.3.2.2.360 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0 Register

14.7.3.2.2.360.1 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0 Register (Offset = 280h) [reset = 38A0209h]

Global Receive FIFO Size Register This register specifies the RAM start address and depth (both in MDWIDTH-bit words) for each implemented RxFIFO. The number of RxFIFOs depends on the configuration parameters including the number of Host Bus Instances and presence of Debug Capability. device mode requires only one RxFIFO. The register default values for each mode are assigned in coreConsultant based on the maximum packet size, number of packets to be buffered, speed of the host bus instance, bus latency, and mode of operation (host, device, or DBC). Upon reset and mode transitions, hardware automatically programs these registers to the default values. Consequently, there is typically no need for the software to modify the pre-defined default values. For the debug capability mode, the currently mapped RxFIFO number can be read from the GFIFOPRIDBC register. For more details on the usage of the GTXFIFOSIZn and GRXFIFOSIZn registers for different modes of operation, refer to "Memory Requirements" chapter in the Databook.

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Table 14-12412. Instance Table

Instance Name	Physical Address
USB0	3100 C380h + formula

Figure 14-6133. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RXFSTADDR_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">38Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RXFSTADDR_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">38Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RXFDEP_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">209h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RXFDEP_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">209h</td></tr>
</table>

Table 14-12413. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RXFSTADDR_N	R/W	38Ah	RxFIFOn RAM Start Address [RxFStAddr_n] This field contains the memory start address for RxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	RXFDEP_N	R/W	209h	RxFIFO Depth [RxFDep_n] This field contains the depth of RxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 16,384 Reset Source: rst_mod_g_rst_n

14.7.3.2.2.361 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1 Register

14.7.3.2.2.361.1 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1 Register (Offset = 284h) [reset = 5930000h]

Register

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Table 14-12414. Instance Table

Instance Name	Physical Address
USB0	3100 C384h + formula

Figure 14-6134. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RXFSTADDR_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">593h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RXFSTADDR_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">593h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RXFDEP_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RXFDEP_N</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12415. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RXFSTADDR_N	R/W	593h	RXFSTADDR_N Reset Source: rst_mod_g_rst_n
15:0	RXFDEP_N	R/W	0h	RxFIFO Depth This field contains the depth of RxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 16,384 Reset Source: rst_mod_g_rst_n

14.7.3.2.2.362 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2 Register

14.7.3.2.2.362.1 USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2 Register (Offset = 288h) [reset = 5930000h]

Register

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Table 14-12416. Instance Table

Instance Name	Physical Address
USB0	3100 C388h + formula

Figure 14-6135. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2 Name Register

31	30	29	28	27	26	25	24
RXFSTADDR_N							
R/W							
593h							
23	22	21	20	19	18	17	16
RXFSTADDR_N							
R/W							
593h							
15	14	13	12	11	10	9	8
RXFDEP_N							
R/W							
0h							
7	6	5	4	3	2	1	0
RXFDEP_N							
R/W							
0h							

Table 14-12417. USB2SS_GBL_GRXFIFO_GRXFIFOSIZ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RXFSTADDR_N	R/W	593h	RAM Start Address This field contains the memory start address for RxFIFOn in MDWIDTH-bit words. Reset Source: rst_mod_g_rst_n
15:0	RXFDEP_N	R/W	0h	RxFIFO Depth This field contains the depth of RxFIFOn in MDWIDTH-bit words. - Minimum value: 32 - Maximum value: 16,384 Reset Source: rst_mod_g_rst_n

14.7.3.2.2.363 USB2SS_GBL_GEVNT_GEVNTADRLO_J Register

14.7.3.2.2.363.1 USB2SS_GBL_GEVNT_GEVNTADRLO_J Register (Offset = 300h) [reset = 0h]

Global Event Buffer Address (Low) Register This is an alternate register for the GEVNTADRn register.

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Table 14-12418. Instance Table

Instance Name	Physical Address
USB0	3100 C400h + formula

Figure 14-6136. USB2SS_GBL_GEVNT_GEVNTADRLO_j Name Register

31	30	29	28	27	26	25	24
EVNTADRLO							
R/W							
0h							
23	22	21	20	19	18	17	16
EVNTADRLO							
R/W							
0h							
15	14	13	12	11	10	9	8
EVNTADRLO							
R/W							
0h							
7	6	5	4	3	2	1	0
EVNTADRLO							
R/W							
0h							

Table 14-12419. USB2SS_GBL_GEVNT_GEVNTADRLO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EVNTADRLO	R/W	0h	Event Buffer Address [EvntAdrLo] Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.364 USB2SS_GBL_GEVNT_GEVNTADRHI_J Register

14.7.3.2.2.364.1 USB2SS_GBL_GEVNT_GEVNTADRHI_J Register (Offset = 304h) [reset = 0h]

Global Event Buffer Address (High) Register This is an alternate register for the GEVNTADRn register.

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Table 14-12420. Instance Table

Instance Name	Physical Address
USB0	3100 C404h + formula

Figure 14-6137. USB2SS_GBL_GEVNT_GEVNTADRHI_j Name Register

31	30	29	28	27	26	25	24
EVNTADRHI							
R/W							
0h							
23	22	21	20	19	18	17	16
EVNTADRHI							
R/W							
0h							
15	14	13	12	11	10	9	8
EVNTADRHI							
R/W							
0h							
7	6	5	4	3	2	1	0
EVNTADRHI							
R/W							
0h							

Table 14-12421. USB2SS_GBL_GEVNT_GEVNTADRHI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EVNTADRHI	R/W	0h	Event Buffer Address [EvntAdrHi] Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.365 USB2SS_GBL_GEVNT_GEVNTSIZ_J Register

14.7.3.2.2.365.1 USB2SS_GBL_GEVNT_GEVNTSIZ_J Register (Offset = 308h) [reset = 0h]

Global Event Buffer Size Register This register holds the Event Buffer Size and the Event Interrupt Mask bit. During power-on initialization, software must initialize the size with the number of bytes allocated for the Event Buffer. The Event Interrupt Mask will mask the interrupt, but events are still queued. After configuration, software must preserve the Event Buffer Size value when changing the Event Interrupt Mask.

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Table 14-12422. Instance Table

Instance Name	Physical Address
USB0	3100 C408h + formula

Figure 14-6138. USB2SS_GBL_GEVNT_GEVNTSIZ_j Name Register

31	30	29	28	27	26	25	24
EVNTINTRPTMASK	RESERVED_30_16						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_30_16							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EVENTSIZ							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVENTSIZ							
R/W							
0h							

Table 14-12423. USB2SS_GBL_GEVNT_GEVNTSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVNTINTRPTMASK	R/W	0h	Event Interrupt Mask [EvntIntMask]. When set to '1', this prevents the interrupt from being generated. However, even when the mask is set, the events are queued. Reset Source: rst_mod_g_rst_n
30:16	RESERVED_30_16	R	0h	Reserved
15:0	EVENTSIZ	R/W	0h	Event Buffer Size in bytes [EVNTSiz] Holds the size of the Event Buffer in bytes. must be a multiple of four. This is programmed by software once during initialization. The minimum size of the event buffer is 32 bytes. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.366 USB2SS_GBL_GEVNT_GEVNTCOUNT_J Register

14.7.3.2.2.366.1 USB2SS_GBL_GEVNT_GEVNTCOUNT_J Register (Offset = 30Ch) [reset = 0h]

Global Event Buffer Count Register This register holds the number of valid bytes in the Event Buffer. During initialization, software must initialize the count by writing 0 to the Event Count field. Each time the hardware writes a new event to the Event Buffer, it increments this count. Most events are four bytes, but some events may span over multiple four byte entries. Whenever the count is greater than zero and if enabled, conditions for interrupt moderation are satisfied, the hardware raises the corresponding interrupt line (depending on the EvntIntMask bit in the GEVNTSIZn register). On an interrupt, software processes one or more events out of the Event Buffer. Afterwards, software must write the Event Count field with the number of bytes it processed. If Interrupt Moderation is enabled, then software needs to clear EVNT_HANDLER_BUSY bit. Clock crossing delays may result in the continuous assertion of the interrupt after software acknowledges the last event. Therefore, when the interrupt line is asserted, software must read the GEVNTCOUNT register and only process events if the GEVNTCOUNT is greater than 0.

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Table 14-12424. Instance Table

Instance Name	Physical Address
USB0	3100 C40Ch + formula

Figure 14-6139. USB2SS_GBL_GEVNT_GEVNTCOUNT_j Name Register

31	30	29	28	27	26	25	24
EVNT_HANDLER_BUSY	RESERVED_30_16						
R/W	R						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED_30_16							
R							
0h							
15	14	13	12	11	10	9	8
EVNTCOUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
EVNTCOUNT							
R/W							
0h							

Table 14-12425. USB2SS_GBL_GEVNT_GEVNTCOUNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVNT_HANDLER_BUSY	R/W	0h	Event Handler Busy Device software event handler busy indication. The controller sets this bit when the interrupt line is asserted due to pending events. Software clears this bit [with 1'b1] when it has finished processing the events [along with updating the EVNTCOUNT in this register]. The controller does not raise the interrupt line for a new event unless this bit is cleared. Note: When Interrupt moderation is disabled [that is, DEVICE_IMODI = 0], this bit is ignored. Reset Source: rst_mod_g_rst_n
30:16	RESERVED_30_16	R	0h	Reserved

Table 14-12425. USB2SS_GBL_GEVNT_GEVNTCOUNT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	EVNTCOUNT	R/W	0h	Event Count [EVNTCount] When read, returns the number of valid events in the Event Buffer [in bytes]. When written, hardware decrements the count by the value written. When Interrupt moderation is enabled [that is, DEVICE_IMODI!= 0], the interrupt line gets de-asserted when the first write happens on this register to decrement the count. When Interrupt moderation is disabled [that is, DEVICE_IMODI = 0], the Interrupt line continues to get asserted until the event count becomes zero [no-moderation behavior]. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.367 USB2SS_GBL_GRHB_GUSB2RHBCTL Register

14.7.3.2.2.367.1 USB2SS_GBL_GRHB_GUSB2RHBCTL Register (Offset = 540h) [reset = 0h]

Global USB 2.0 Root Hub Control Register The application must program this register before starting any transactions on the USB if a non-default value is desired. In Host mode, per-port registers are implemented.

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Table 14-12426. Instance Table

Instance Name	Physical Address
USB0	3100 C640h + formula

Figure 14-6140. USB2SS_GBL_GRHB_GUSB2RHBCTL Name Register

31	30	29	28	27	26	25	24
RESERVED_31_4							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_4							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_4				OVRD_L1TIMEOUT			
R				R/W			
0h				0h			

Table 14-12427. USB2SS_GBL_GRHB_GUSB2RHBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_31_4	R	0h	Reserved
3:0	OVRD_L1TIMEOUT	R/W	0h	Overriding the driver programmed L1TIMEOUT value. If this value is 0, the L1 Timeout value is taken from the xHCI PORTHLPMC register. If this value is non-0, then this will override the L1 Timeout value programmed in the xHCI PORTHLPMC register. In that case the actual L1 Timeout would be 2 ^ <OVRD_L1TIMEOUT-1> * 8us. [1=8us, 2=16us, 3=32us etc] Reset Source: rst_mod_g_rst_n

14.7.3.2.2.368 USB2SS_DEV_DCFG Register

14.7.3.2.2.368.1 USB2SS_DEV_DCFG Register (Offset = 0h) [reset = 80800h]

Device Configuration Register. This register configures the controller in Device mode after power-on or after certain control commands or enumeration. Do not make changes to this register after initial programming.

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Table 14-12428. Instance Table

Instance Name	Physical Address
USB0	3100 C700h

Figure 14-6141. USB2SS_DEV_DCFG Name Register

31	30	29	28	27	26	25	24
RESERVED_31_25							RESERVED_24
R							R
0h							0h
23	22	21	20	19	18	17	16
IGNSTRMPP	LPMCAP	NUMP					INTRNUM
R/W	R/W	R/W					R/W
0h	0h	4h					0h
15	14	13	12	11	10	9	8
INTRNUM				RESERVED_10_11		DEVADDR	
R/W				R		R/W	
0h				2h		0h	
7	6	5	4	3	2	1	0
DEVADDR					DEVSPD		
R/W					R/W		
0h					0h		

Table 14-12429. USB2SS_DEV_DCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED_31_25	R	0h	Reserved
24	RESERVED_24	R	0h	reserved
23	IGNSTRMPP	R/W	0h	IgnoreStreamPP This bit only affects stream-capable bulk endpoints. When this bit is set to '0' and the controller receives a Data Packet with the Packet Pending [PP] bit set to 0 for OUT endpoints, or it receives an ACK with the NumP field set to 0 and PP set to 0 for IN endpoints, the controller attempts to search for another stream [CStream] to initiate to the host. However, there are two situations where this behavior is not optimal: - When the host is setting PP=0 even though it has not finished the stream, or - When the endpoint on the device is configured with one transfer resource and therefore does not have any other streams to initiate to the host. When this bit is set to '1', the controller ignores the Packet Pending bit for the purposes of stream selection and does not search for another stream when it receives DP[PP=0] or ACK[NumP=0, PP=0]. This can enhance the performance when the device system bus bandwidth is low or the host responds to the controller's ERDY transmission very quickly. Reset Source: rst_mod_g_rst_n
22	LPMCAP	R/W	0h	LPM Capable The application uses this bit to control the LPM capabilities of the DWC_usb3 controller. If the controller operates as a non-LPM-capable device, it cannot respond to LPM transactions. - 1'b0: LPM capability is not enabled. - 1'b1: LPM capability is enabled. Reset Source: rst_mod_g_rst_n

Table 14-12429. USB2SS_DEV_DCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:17	NUMP	R/W	4h	Number of Receive Buffers. This bit indicates the number of receive buffers to be reported in the ACK TP. The DWC_usb3 controller uses this field for non-control endpoints if GRXTHRCFG.UsbRxPktCntSel is set to '0'. The application can program this value based on RxFIFO size, buffer sizes programmed in descriptors, and system latency. For an OUT endpoint, this field controls the number of receive buffers reported in the NumP field of the ACK TP transmitted by the controller. Note: This bit is used in host mode when Debug Capability is enabled. Reset Source: rst_mod_g_rst_n
16:12	INTRNUM	R/W	0h	Interrupt number Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts [see DEVT] are generated. Reset Source: rst_mod_g_rst_n
11:10	RESERVED_10_11	R	2h	Reserved
9:3	DEVADDR	R/W	0h	Device Address. The application must perform the following: - Program this field after every SetAddress request. - Reset this field to zero after USB reset. Reset Source: rst_mod_g_rst_n
2:0	DEVSPD	R/W	0h	Device Speed. Indicates the speed at which the application requires the controller to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the controller is connected. - 3'b100: SuperSpeed [USB 3.0 PHY clock is 125 MHz or 250 MHz] - 3'b000: High-speed [USB 2.0 PHY clock is 30 MHz or 60 MHz] - 3'b001: Full-speed [USB 2.0 PHY clock is 30 MHz or 60 MHz] 0 `HighSpe` 1 `FullSpeed` 4 `SuperSpeed`

14.7.3.2.2.369 USB2SS_DEV_DCTL Register

14.7.3.2.2.369.1 USB2SS_DEV_DCTL Register (Offset = 4h) [reset = F00000h]

Device Control Register Note: When Hibernation is not enabled using GCTL.GblHibernationEn field, - you can write any value to CSS, CRS, L1HibernationEn, and KeepConnect fields - L1HibernationEn, and KeepConnect fields always return 0 when read in this hibernation-disabled state

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Table 14-12430. Instance Table

Instance Name	Physical Address
USB0	3100 C704h

Figure 14-6142. USB2SS_DEV_DCTL Name Register

31	30	29	28	27	26	25	24
RUN_STOP	CSFTRST	RESERVED_29	HIRDTHRES				
R/W	R/W1TS	R	R/W				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
LPM_NYET_THRES				KEEPCONNECT	L1HIBERNATIONEN	CRS	CSS
R/W				W	W	R/W	R/W
Fh				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED_15_13			INITU2ENA	ACCEPTU2ENA	INITU1ENA	ACCEPTU1ENA	ULSTCHNGREQ
R			R/W	R/W	R/W	R/W	W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ULSTCHNGREQ				TSTCTL			RESERVED_0
W				R/W			R
0h				0h			0h

Table 14-12431. USB2SS_DEV_DCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RUN_STOP	R/W	0h	Run/Stop The software writes 1 to this bit to start the device controller operation. To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the controller is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: - After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. - The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared is specified in the Note below. If the software attempts a connect after the soft disconnect or detects a disconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stop bit. - When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller. For more details, see "Low Power Operation" section of the Databook. Note: The following is the minimum duration under various conditions for which the soft disconnect [SftDiscon] bit must be set for the USB host to detect a device disconnect: 30ms: - For SuperSpeed, when the device state is Suspended, Idle, Transmit, or Receive. 10ms: - For high-speed, when the device state is Suspended, Idle, or not Idle/Suspended [performing transactions] - For full-speed/ low-speed, when the device state is Suspended, Idle, or not Idle/ Supended [performing transactions] To accommodate clock jitter, it is recommended that the application add extra delay to the specified minimum duration. Reset Source: rst_mod_g_rst_n
30	CSFTRST	R/W1TS	0h	Core Soft Reset Resets the all clock domains as follows: - This bit clears the interrupts and all the CSRs except GSTS, GSNPSID, GGPIO, GUID, GUSB2PHYCFGn registers, GUSB3PIPECTLn registers, DCFG, DCTL, DEVTEN, and DSTS registers. - All module state machines [except the SoC Bus Target Unit] are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. - Any transactions on the SoC bus Initiator are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the controller. This is a self-clearing bit. the controller clears this bit after all necessary logic is reset in the controller, which may take several clocks depending on the current state of the controller. Once this bit is cleared, the software must wait at least 3 PHY clocks before accessing the PHY domain [synchronization delay]. Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation. Note: Programming this field with random data causes side effect . Bit Bash register testing is not recommended. Reset Source: rst_mod_g_rst_n
29	RESERVED_29	R	0h	Reserved1

Table 14-12431. USB2SS_DEV_DCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28:24	HIRDTHRES	R/W	0h	HIRD Threshold [HIRD_Thres] The controller asserts output signals utmi_l1_suspend_n and utmi_sleep_n [see "LPM Interface Signals" table in the Databook] on the basis of this signal: The controller asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: - HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] - HIRD_Thres[4] is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: - If the HIRD value is less than HIRD_Thres[3:0] or - HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation. Reset Source: rst_mod_g_rst_n
23:20	LPM_NYET_THRES	R/W	Fh	LPM NYET Threshold When LPM Errata is enabled: Bits [23:20]: LPM NYET Response Threshold [LPM_NYET_thres] Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. - DCFG.LPMCap is 1'b0 - The controller always responds with Timeout [that is, no response]. - DCFG.LPMCap is 1'b1 - The controller responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: - There are no PID or CRC5 errors in both the EXT token and the LPM token [if not true, inactivity results in a timeout ERROR]. - No data is pending in the TxFIFO and RxFIFO is empty [else NYET]. - The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0] Reset Source: rst_mod_g_rst_n
19	KEEPCONNECT	W	0h	Keep Connect When '1', this bit enables the save and restore programming model by preventing the controller from disconnecting from the host when DCTL.RunStop is set to '0'. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device controller disconnects from the host when DCTL.RunStop is set to '0'. This bit indicates whether to preserve this behavior ['0'], or if the controller must not disconnect when RunStop is set to 0 ['1']. This bit also prevents the LTSSM from automatically going to U0/L0 when the host requests resume from U3/L2. Note: If Hibernation is disabled, that is, GCTL[1].GblHibernationEn = 0, this bit is tied to zero. Reset Source: rst_mod_g_rst_n
18	L1HIBERNATIONEN	W	0h	L1HibernationEn When this bit is set along with KeepConnect, the device controller generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The controller does not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1. Note: If Hibernation is disabled, that is, GCTL[1].GblHibernationEn = 0, this bit is tied to zero. Reset Source: rst_mod_g_rst_n
17	CRS	R/W	0h	Controller Restore State [CRS] This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'. Note: When read, this field always returns '0'. Reset Source: rst_mod_g_rst_n
16	CSS	R/W	0h	Controller Save State [CSS] This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'. Note: When read, this field always returns '0'. Reset Source: rst_mod_g_rst_n
15:13	RESERVED_15_13	R	0h	Reserved

Table 14-12431. USB2SS_DEV_DCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	INITU2ENA	R/W	0h	Initiate U2 Enable - 1'b0: May not initiate U2 [default] - 1'b1: May initiate U2 On USB reset, hardware clears this bit to 0. Software sets this bit after receiving SetFeature[U2_ENABLE], and clears this bit when ClearFeature[U2_ENABLE] is received. If DCTL[11] [AcceptU2Ena] is 0, the link immediately exits U2 state. Reset Source: rst_mod_g_rst_n
11	ACCEPTU2ENA	R/W	0h	Accept U2 Enable - 1'b0: Reject U2 except when Force_LinkPM_Accept bit is set [default] - 1'b1: Controller accepts transition to U2 state if nothing is pending on the application side. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving a SetConfiguration command. Reset Source: rst_mod_g_rst_n
10	INITU1ENA	R/W	0h	Initiate U1 Enable - 1'b0: May not initiate U1 [default]. - 1'b1: May initiate U1. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving SetFeature[U1_ENABLE], and clears this bit when ClearFeature[U1_ENABLE] is received. If DCTL[9] [AcceptU1Ena] is 0, the link immediately exits U1 state. Reset Source: rst_mod_g_rst_n
9	ACCEPTU1ENA	R/W	0h	Accept U1 Enable - 1'b0: Controller rejects U1 except when Force_LinkPM_Accept bit is set [default] - 1'b1: Controller accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving a SetConfiguration command. Reset Source: rst_mod_g_rst_n
8:5	ULSTCHNGREQ	W	0h	ULSTCHNGREQ Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the controller. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Refer to the USB 3.0 specification. Alternatively, you can force the local link directly into compliance mode, by resetting the SS link with the RUN/STOP bit set to zero. If you then write '10' to the USB/Link State Change field and '1' to RUN/STOP, the link goes to compliance mode. Once you are in compliance, you may alternately write zero and '10' to this field to advance the compliance pattern. In SS mode: - Value Requested Link State Transition/Action - 0 No Action - 4 SS.Disabled - 5 Rx.Detect - 6 SS.Inactive - 8 U3 exit request - 10 Compliance - Others: Reserved In HS/FS/LS mode: - ValueRequested USB state transition - 8 Remote wakeup request - Others: Reserved The Remote wakeup request must be issued 2us after the device goes into suspend state [DSTS[21:18] is 3 - refer to Table "Fields for Register: DSTS"]. Note: After coming out of hibernation, software must write 8 [Recovery] into this field to confirm exit from the suspended state. Reset Source: rst_mod_g_rst_n
4:1	TSTCTL	R/W	0h	Test Control - 4'b000: Test mode disabled - 4'b001: Test_J mode - 4'b010: Test_K mode - 4'b011: Test_SE0_NAK mode - 4'b100: Test_Packet mode - 4'b101: Test_Force_Enable - Others: Reserved Reset Source: rst_mod_g_rst_n
0	RESERVED_0	R	0h	Reserved

14.7.3.2.2.370 USB2SS_DEV_DEVTEN Register

14.7.3.2.2.370.1 USB2SS_DEV_DEVTEN Register (Offset = 8h) [reset = 0h]

Device Event Enable Register This register controls the generation of device-specific events (see "Event Buffer Content for Device-Specific Events (DEVT)" section). If an enable bit is set to 0, the event will not be generated.

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Table 14-12432. Instance Table

Instance Name	Physical Address
USB0	3100 C708h

Figure 14-6143. USB2SS_DEV_DEVTEN Name Register

31	30	29	28	27	26	25	24
RESERVED_31_17							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_17							ECCERREN
R							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED_15	L1WKUPEVTEN	RESERVED	VENDEVTSTRCVDEN	RESERVED_11	RESERVED_10	ERRTICERREVTEN	L1SUSPEN
R	R/W	NONE	R/W	R	R	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOFTEVTEN	U3L2L1SUSPEN	HIBERNATIONREQEVTEN	WKUPEVTEN	ULSTCNGEN	CONNECTDONEEVTEN	USBRSTEVTEN	DISSCONNEVTEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12433. USB2SS_DEV_DEVTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_31_17	R	0h	Reserved
16	ECCERREN	R	0h	ECC Error Enable. If this bit is set to 1, the controller reports an ECC error to the software when an uncorrectable ECC occurs internally. Reset Source: rst_mod_g_rst_n
15	RESERVED_15	R	0h	Reserved
14	L1WKUPEVTEN	R/W	0h	L1 Resume Detected Event Enable. Note: If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for L1 Resume Detected Event Enable. Reset Source: rst_mod_g_rst_n
13	RESERVED	NONE	0h	Reserved
12	VENDEVTSTRCVDEN	R/W	0h	Vendor Device Test LMP Received Event [VndrDevTstRcvedEn] Reset Source: rst_mod_g_rst_n
11	RESERVED_11	R	0h	Reserved
10	RESERVED_10	R	0h	Reserved
9	ERRTICERREVTEN	R/W	0h	Erratic Error Event Enable Reset Source: rst_mod_g_rst_n

Table 14-12433. USB2SS_DEV_DEVTEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	L1SUSPEN	R/W	0h	L1 Suspend Event Enable Note: Only if GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, this bit is for L1 Suspend Event Enable. Reset Source: rst_mod_g_rst_n
7	SOFTEVTEN	R/W	0h	Start of [u]frame Reset Source: rst_mod_g_rst_n
6	U3L2L1SUSPEN	R/W	0h	U3/L2 or U3/L2L1 Suspend Event Enable. Note: - If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for U3/L2 Suspend Event Enable. - If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is not enabled, then this bit is for U3/L2L1 Suspend Event Enable. Reset Source: rst_mod_g_rst_n
5	HIBERNATIONREQEVTEN	R/W	0h	This bit enables/disables the generation of the Hibernation Request Event. Reset Source: rst_mod_g_rst_n
4	WKUPEVTEN	R/W	0h	U3/L2 or U3/L2L1 Resume Detected Event Enable. Note: - If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for U3/L2 Resume Detected Event Enable. - If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is not enabled, then this bit is for U3/L2L1 Resume Detected Event Enable. Reset Source: rst_mod_g_rst_n
3	ULSTCNGEN	R/W	0h	USB/Link State Change Event Enable Reset Source: rst_mod_g_rst_n
2	CONNECTDONEEVTEN	R/W	0h	Connection Done Enable Reset Source: rst_mod_g_rst_n
1	USBRSTEVTEN	R/W	0h	USB Reset Enable Reset Source: rst_mod_g_rst_n
0	DISSCONNEVTEN	R/W	0h	Disconnect Detected Event Enable Reset Source: rst_mod_g_rst_n

14.7.3.2.2.371 USB2SS_DEV_DSTS Register

14.7.3.2.2.371.1 USB2SS_DEV_DSTS Register (Offset = Ch) [reset = 520004h]

Device Status Register This register indicates the status of the device controller with respect to USB-related events. Note: When Hibernation is not enabled, RSS and SSS fields always return 0 when read.

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Table 14-12434. Instance Table

Instance Name	Physical Address
USB0	3100 C70Ch

Figure 14-6144. USB2SS_DEV_DSTS Name Register

31	30	29	28	27	26	25	24
RESERVED_31_30		DCNRD	SRE	RESERVED_27_26		RSS	SSS
R		R	R/W1TC	R		R	R
0h		0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
COREIDLE	DEVCTRLHLT	USBLNKST				RXFIFOEMPTY	SOFFN
R	R	R				R	R
0h	1h	4h				1h	0h
15	14	13	12	11	10	9	8
SOFFN							
R							
0h							
7	6	5	4	3	2	1	0
SOFFN					CONNECTSPD		
R					R		
0h					4h		

Table 14-12435. USB2SS_DEV_DSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_31_30	R	0h	Reserved
29	DCNRD	R	0h	Device Controller Not Ready The bit indicates that the controller is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to '1' and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when DWC_USB3_EN_PWROPT is set to 2 and GCTL[1].GblHibernationEn =1. Reset Source: rst_mod_g_rst_n
28	SRE	R/W1TC	0h	Save Restore Error. Currently not supported. Reset Source: rst_mod_g_rst_n
27:26	RESERVED_27_26	R	0h	Reserved
25	RSS	R	0h	RSS Restore State Status This bit is similar to the USBSTS.RSS in host mode. When the controller finishes the restore process, it completes the command by setting DSTS.RSS to '0'. Reset Source: rst_mod_g_rst_n
24	SSS	R	0h	SSS Save State Status This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to '0'. Reset Source: rst_mod_g_rst_n

Table 14-12435. USB2SS_DEV_DSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	COREIDLE	R	0h	Core Idle The bit indicates that the controller finished transferring all RxFIFO data to system memory, Writing out all completed descriptors, and all Event Counts are zero. Note: While testing for Reset values, mask out the read value. This bit represents the changing state of the controller and does not hold a static value. Reset Source: rst_mod_g_rst_n
22	DEVCTRLHLT	R	1h	Device Controller Halted This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The controller sets this bit to 1 when, after SW sets Run/Stop to 0, the controller is idle and the lower layer finishes the disconnect process. When Halted=1, the controller does not generate Device events. Note: - The controller does not set this bit to 1 if GEVNTCOUNTn has some valid value. Software needs to acknowledge the events that are generated [by Writing to GEVNTCOUNTn] while it is waiting for this bit to be set to 1. - When Interrupt Moderation is enabled, there could be delay in raising the interrupt line when the event count is non-zero. Software should read the GEVNTCOUNT register directly and acknowledge them. Reset Source: rst_mod_g_rst_n
21:18	USBLNKST	R	4h	USBLNKST. USB/Link State In SS mode: LTSSM State - 4'h0: U0 - 4'h1: U1 - 4'h2: U2 - 4'h3: U3 - 4'h4: SS_DIS - 4'h5: RX_DET - 4'h6: SS_INACT - 4'h7: POLL - 4'h8: RECOV - 4'h9: HRESET - 4'ha: CMPLY - 4'hb: LPBK - 4'hf: Resume/Reset In HS/FS/LS mode: - 4'h0: On state - 4'h2: Sleep [L1] state - 4'h3: Suspend [L2] state - 4'h4: Disconnected state [Default state] - 4'h5: Early Suspend state [valid only when Hibernation is disabled, GCTL[1].GblHibernationEn = 0] - 4'he: Reset [valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1] - 4'hf: Resume [valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1] The link state Resume/Reset indicates that the controller received a resume or USB reset request from the host while the link was in hibernation. Software must write '8' [Recovery] to the DCTL.ULStChngReq field to acknowledge the resume/reset request. When Hibernation is enabled, GCTL[1].GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL[31].Run/Stop set to '1' and DSTS[29].DCNRD = 0. The Early Suspend link state is an early indication of device suspend in HS/FS. The link state changes to Early Suspend after detecting bus idle for 3ms. - In HS operation, this is an indication that the USB bus [that is, LineState] has been in idle [SE0] for 3ms. However, it does not confirm whether the next process is Suspend or Reset. The device checks the bus again after pull up enable delay and if the line state indicates Suspend [full speed J], then the device waits for an additional time [~3ms] to indicate the actual Suspend state. - In FS operation, this is an indication that the USB bus [that is, LineState] has been in idle [J] for 3ms. The device waits for an additional time [~3ms of Idle] to indicate the actual Suspend state. Reset Source: rst_mod_g_rst_n
17	RXFIFOEMPTY	R	1h	RxFIFO Empty. Reset Source: rst_mod_g_rst_n
16:3	SOFFN	R	0h	Frame/Microframe Number of the Received SOF. When the controller is operating at SuperSpeed, - [16:3] indicates the uframe/ITP number When the controller is operating at high-speed, - [16:6] indicates the frame number - [5:3] indicates the microframe number When the controller is operating at full-speed, - [16:14] is not used. Software can ignore these 3 bits - [13:3] indicates the frame number Note: After power-on reset, the controller generates the microframe number internally for every 125us if the USB host has not issued SOF/ITP yet. During P3 state, the duration of SOFFN is based on the suspend_clk frequency. Reset Source: rst_mod_g_rst_n

Table 14-12435. USB2SS_DEV_DSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	CONNECTSPD	R	4h	Connected Speed [ConnectSpd] Indicates the speed at which the DWC_usb3 controller has come up after speed detection through a chirp sequence. - 3'b100: SuperSpeed [PHY clock is running at 125 or 250 MHz] - 3'b000: High-speed [PHY clock is running at 30 or 60 MHz] - 3'b001: Full-speed [PHY clock is running at 30 or 60 MHz] Low-speed is not supported for devices using a UTMI+ PHY. 0 `HighSpeed` 1 `FullSpeed` 4 `SuperSpeed`

14.7.3.2.2.372 USB2SS_DEV_DGCMDPAR Register

14.7.3.2.2.372.1 USB2SS_DEV_DGCMDPAR Register (Offset = 10h) [reset = 0h]

Device Generic Command Parameter Register This register indicates the device command parameter. This must be programmed before or along with the device command. The available device commands are listed in DGCMD register.

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Table 14-12436. Instance Table

Instance Name	Physical Address
USB0	3100 C710h

Figure 14-6145. USB2SS_DEV_DGCMDPAR Name Register

31	30	29	28	27	26	25	24
PARAMETER							
R/W							
0h							
23	22	21	20	19	18	17	16
PARAMETER							
R/W							
0h							
15	14	13	12	11	10	9	8
PARAMETER							
R/W							
0h							
7	6	5	4	3	2	1	0
PARAMETER							
R/W							
0h							

Table 14-12437. USB2SS_DEV_DGCMDPAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PARAMETER	R/W	0h	PARAMETER Reset Source: rst_mod_g_rst_n

14.7.3.2.2.373 USB2SS_DEV_DGCMD Register

14.7.3.2.2.373.1 USB2SS_DEV_DGCMD Register (Offset = 14h) [reset = 0h]

Device Generic Command Register This register enables software to program the controller using a single generic command interface to send link management packets and notifications. This register contains command, control, and status fields relevant to the current generic command, while the DGCMDPAR register provides the command parameter.

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Table 14-12438. Instance Table

Instance Name	Physical Address
USB0	3100 C714h

Figure 14-6146. USB2SS_DEV_DGCMD Name Register

31	30	29	28	27	26	25	24
RESERVED_31_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_16							
R							
0h							
15	14	13	12	11	10	9	8
CMDSTATUS				RESERVED_11	CMDACT	RESERVED_9	CMDIOC
R				R	R/W1TS	R	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
CMDTYP							
R/W							
0h							

Table 14-12439. USB2SS_DEV_DGCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_31_16	R	0h	Reserved
15:12	CMDSTATUS	R	0h	Command Status - 1: CmdErr: Indicates that the device controller encountered an error while processing the command. - 0: Indicates command success Reset Source: rst_mod_g_rst_n
11	RESERVED_11	R	0h	Reserved
10	CMDACT	R/W1TS	0h	Command Active The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command. Reset Source: rst_mod_g_rst_n
9	RESERVED_9	R	0h	Reserved
8	CMDIOC	R/W	0h	Command Interrupt on Complete When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to '1' if the DCTL.RunStop field is '0'. Reset Source: rst_mod_g_rst_n

Table 14-12439. USB2SS_DEV_DGCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	CMDTYP	R/W	0h	CMDTYP Generic Command Type Specifies the type of generic command the software driver is requesting the controller to perform. - 02h: Set Periodic Parameters - 04h: Set Scratchpad Buffer Array Address Lo - 05h: Set Scratchpad Buffer Array Address Hi - 07h: Transmit Device Notification - 09h: Selected FIFO Flush - 0Ah: All FIFO Flush - 0Ch: Set Endpoint NRDY - 10h: Run SoC Bus LoopBack Test - 11h: Restart After Disconnect All other values are reserved. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.374 USB2SS_DEV_DALEPENA Register

14.7.3.2.2.374.1 USB2SS_DEV_DALEPENA Register (Offset = 20h) [reset = 0h]

Device Active USB Endpoint Enable Register. This register indicates whether a USB endpoint is active in a given configuration or interface.

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Table 14-12440. Instance Table

Instance Name	Physical Address
USB0	3100 C720h

Figure 14-6147. USB2SS_DEV_DALEPENA Name Register

31	30	29	28	27	26	25	24
USBACTEP							
R/W							
0h							
23	22	21	20	19	18	17	16
USBACTEP							
R/W							
0h							
15	14	13	12	11	10	9	8
USBACTEP							
R/W							
0h							
7	6	5	4	3	2	1	0
USBACTEP							
R/W							
0h							

Table 14-12441. USB2SS_DEV_DALEPENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USBACTEP	R/W	0h	USBACTEP USB Active Endpoints [USBActEP] This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0.15 and OUT endpoints 0.15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: - Bit[0]: USB EP0-OUT - Bit[1]: USB EP0-IN - Bit[2]: USB EP1-OUT - Bit[3]: USB EP1-IN The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints [resources] after USBReset. Hardware clears these bits for all endpoints [other than EP0-OUT and EP0-IN] after detecting a USB reset event. After receiving SetConfiguration and SetInterface requests, the application must program endpoint registers accordingly and set these bits. For more information, see "Flexible Endpoint Mapping" section in the Databook. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.375 USB2SS_DEV_DEV_RESERVED_RSVD_J Register

14.7.3.2.2.375.1 USB2SS_DEV_DEV_RESERVED_RSVD_J Register (Offset = 24h) [reset = 0h]

Reserved

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Table 14-12442. Instance Table

Instance Name	Physical Address
USB0	3100 C724h + formula

Figure 14-6148. USB2SS_DEV_DEV_RESERVED_RSVD_j Name Register

31	30	29	28	27	26	25	24
RESERVED_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_31_0							
R							
0h							

Table 14-12443. USB2SS_DEV_DEV_RESERVED_RSVD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_31_0	R	0h	Reserved

14.7.3.2.2.376 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_J Register

14.7.3.2.2.376.1 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_J Register (Offset = 100h) [reset = 0h]

Device Physical Endpoint-n Command Parameter 2 Register (DEPCMDPAR2n) This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

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Table 14-12444. Instance Table

Instance Name	Physical Address
USB0	3100 C800h + formula

Figure 14-6149. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_j Name Register

31	30	29	28	27	26	25	24
PARAMETER							
R/W							
0h							
23	22	21	20	19	18	17	16
PARAMETER							
R/W							
0h							
15	14	13	12	11	10	9	8
PARAMETER							
R/W							
0h							
7	6	5	4	3	2	1	0
PARAMETER							
R/W							
0h							

Table 14-12445. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PARAMETER	R/W	0h	PARAMETER Reset Source: rst_mod_g_rst_n

14.7.3.2.2.377 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_J Register

14.7.3.2.2.377.1 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_J Register (Offset = 104h) [reset = 0h]

Device Physical Endpoint-n Command Parameter 1 Register (DEPCMDPAR1n)

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Table 14-12446. Instance Table

Instance Name	Physical Address
USB0	3100 C804h + formula

Figure 14-6150. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PARAMETER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PARAMETER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PARAMETER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PARAMETER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12447. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PARAMETER	R/W	0h	PARAMETER Reset Source: rst_mod_g_rst_n

14.7.3.2.2.378 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_J Register

14.7.3.2.2.378.1 USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_J Register (Offset = 108h) [reset = 0h]

Device Physical Endpoint-n Command Parameter 0 Register (DEPCMDPAR0n)

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Table 14-12448. Instance Table

Instance Name	Physical Address
USB0	3100 C808h + formula

Figure 14-6151. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_j Name Register

31	30	29	28	27	26	25	24
PARAMETER							
R/W							
0h							
23	22	21	20	19	18	17	16
PARAMETER							
R/W							
0h							
15	14	13	12	11	10	9	8
PARAMETER							
R/W							
0h							
7	6	5	4	3	2	1	0
PARAMETER							
R/W							
0h							

Table 14-12449. USB2SS_DEV_DEPCMDPAR_EP_DEPCMDPAR0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PARAMETER	R/W	0h	PARAMETER Reset Source: rst_mod_g_rst_n

14.7.3.2.2.379 USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_J Register

14.7.3.2.2.379.1 USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_J Register (Offset = 10Ch) [reset = 0h]

Device Physical Endpoint-n Command Register This register enables software to issue physical endpoint-specific commands. This register contains command, control, and status fields relevant to the current generic command, while the DEPCMDPAR[2:0]n registers provide command parameters and return status information. Several fields (including Command Type) are write-only, so their read values are undefined. After power-on, prior to issuing the first endpoint command, the read value of this register is undefined. In particular, the CmdAct bit may be set after power-on. In this case, it is safe to issue an endpoint command.

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Table 14-12450. Instance Table

Instance Name	Physical Address
USB0	3100 C80Ch + formula

Figure 14-6152. USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_j Name Register

31	30	29	28	27	26	25	24
COMMANDPARAM							
R/W							
0h							
23	22	21	20	19	18	17	16
COMMANDPARAM							
R/W							
0h							
15	14	13	12	11	10	9	8
CMDSTATUS				HIPRI_FORCERM	CMDACT	RESERVED_9	CMDIOC
R/W				R/W	R/W	R	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_7_4				CMDTYP			
R				R/W			
0h				0h			

Table 14-12451. USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COMMANDPARAM	R/W	0h	Command Parameters or Event Parameters Command Parameters [CommandParam], when this register is written: For Start Transfer command: - [31:16]: StreamID. The USB StreamID assigned to this transfer For Start Transfer command applied to an isochronous endpoint - [31:16]: StartMicroFramNum: Indicates the [micro]frame number to which the first TRB applies. For Update Transfer, End Transfer, and Start New Configuration commands - [22:16]: Transfer Resource Index [XferRscIdx]. The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command. Event Parameters [EventParam], when this register is read. Refer to bits [31:16] in Table "Device Endpoint-n Events: DEPEVT". Reset Source: rst_mod_g_rst_n
15:12	CMDSTATUS	R/W	0h	Command Completion Status [CmdStatus] Additional information about the completion of this command is available in this field. The information is in the same format as bits 15:12 of the Endpoint Command Complete event, see "Device Endpoint-n Events: DEPEVT" table in the Programming Guide. Reset Source: rst_mod_g_rst_n

Table 14-12451. USB2SS_DEV_DEPCMDPAR_EP_DEPCMD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	HIPRI_FORCERM	R/W	0h	HighPriority/ForceRM [HiPri_ForceRM] - HighPriority: Only valid for Start Transfer command - ForceRM: Only valid for End Transfer command - ClearPendIN: Only valid for Clear Stall command . Software sets this bit to clear any pending IN transaction [on that endpoint] stuck at the lower layers when a Clear Stall command is issued. Reset Source: rst_mod_g_rst_n
10	CMDACT	R/W	0h	Command Active [CmdAct] Software sets this bit to 1 to enable the device endpoint controller to execute the generic command. The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place. Reset Source: rst_mod_g_rst_n
9	RESERVED_9	R	0h	Reserved
8	CMDIOC	R/W	0h	CMDIOC Command Interrupt on Complete [CmdIOC] When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to 1 if the DCTL.RunStop field is 0. Reset Source: rst_mod_g_rst_n
7:4	RESERVED_7_4	R	0h	Reserved
3:0	CMDTYP	R/W	0h	Command Type Specifies the type of command the software driver is requesting the controller to perform. - 00h: Reserved - 01h: Set Endpoint Configuration - -64 or 96-bit Parameter - 02h: Set Endpoint Transfer Resource Configuration - 32-bit Parameter - 03h: Get Endpoint State - No Parameter Needed - 04h: Set Stall - No Parameter Needed - 05h: Clear Stall [see Set Stall] - No Parameter Needed - 06h: Start Transfer - 64-bit Parameter - 07h: Update Transfer - No Parameter Needed - 08h: End Transfer - No Parameter Needed - 09h: Start New Configuration - No Parameter Needed Reset Source: rst_mod_g_rst_n

14.7.3.2.2.380 USB2SS_DEV_DEV_INTR_DEV_IMOD_J Register

14.7.3.2.2.380.1 USB2SS_DEV_DEV_INTR_DEV_IMOD_J Register (Offset = 300h) [reset = 0h]

Device Interrupt Moderation Register (DEV_IMOD) This register controls the Interrupt Moderation feature that allows the device software to throttle the interrupt rate. Key Functions: - Interrupt Moderation is enabled only when the IMOD Interval is programmed to a non-zero value. - Interrupt is asserted whenever the IMOD (down) counter is 0, EVNT_HANDLER_BUSY is 0, and there are pending events (that is, event count is non-zero) - GEVNTCOUNT[EVNT_HANDLER_BUSY] is set by hardware when interrupt is asserted, and cleared by software when interrupt processing is completed. - The Interrupt line is de-asserted after the first write to the event count. - IMOD counter is loaded with IMOD interval whenever the Interrupt line is de-asserted.

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Table 14-12452. Instance Table

Instance Name	Physical Address
USB0	3100 CA00h + formula

Figure 14-6153. USB2SS_DEV_DEV_INTR_DEV_IMOD_j Name Register

31	30	29	28	27	26	25	24
DEVICE_IMODC							
R/W							
0h							
23	22	21	20	19	18	17	16
DEVICE_IMODC							
R/W							
0h							
15	14	13	12	11	10	9	8
DEVICE_IMODI							
R/W							
0h							
7	6	5	4	3	2	1	0
DEVICE_IMODI							
R/W							
0h							

Table 14-12453. USB2SS_DEV_DEV_INTR_DEV_IMOD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DEVICE_IMODC	R/W	0h	Interrupt Moderation Down Counter Loaded with the DEVICE_IMODI value, whenever the hardware interrupt[n] line is de-asserted from the asserted state, counts down to 0, and stops. The interrupt[n] is signaled whenever this counter is 0, EVNT_HANDLER_BUSY is 0, and there are pending events [that is, event count is non-zero]. This counter may be directly written by software at any time to alter the interrupt rate. Reset Source: rst_mod_g_rst_n
15:0	DEVICE_IMODI	R/W	0h	Moderation Interval [DEVICE_IMODI] This field holds the minimum inter-interrupt interval between events. The interval is specified in terms of 250ns increments. A value of 0 disables the interrupt throttling logic and interrupts are generated immediately if event count becomes non-zero. In scaledown simulation mode, 4 ram clocks are used to time 250ns. Reset Source: rst_mod_g_rst_n

14.7.3.2.2.381 USB2SS_LINK_LINK_LU1LFPSRXTIM Register

14.7.3.2.2.381.1 USB2SS_LINK_LINK_LU1LFPSRXTIM Register (Offset = 0h) [reset = 1F1Fh]

U1/U2 LFPS Rx Timer Register - Link Layer Register for U1/U2 LFPS RX Timers. - This register is common for all SS ports.

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Table 14-12454. Instance Table

Instance Name	Physical Address
USB0	3100 D000h + formula

Figure 14-6154. USB2SS_LINK_LINK_LU1LFPSRXTIM Name Register

31	30	29	28	27	26	25	24
RESERVED_16_31							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED_16_31							
R/W							
0h							
15	14	13	12	11	10	9	8
U1U2_LFPS_EXIT_RX_CLK							
R/W							
1Fh							
7	6	5	4	3	2	1	0
U1U2_EXIT_RSP_RX_CLK							
R/W							
1Fh							

Table 14-12455. USB2SS_LINK_LINK_LU1LFPSRXTIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_16_31	R/W	0h	Reserved
15:8	U1U2_LFPS_EXIT_RX_CLK	R/W	1Fh	Programmable U1U2 LFPS EXIT RX CLKS - Applicable to Remote Partner initiated Ux exit: Time to recognize valid Ux exit request from the remote partner. - This field is encoded as the pipe clk [8ns] count for the LFPS. -- 1: 8ns -- 2: 16ns -- 3: 24ns, and so on Reset Source: rst_mod_g_rst_n
7:0	U1U2_EXIT_RSP_RX_CLK	R/W	1Fh	Programmable U1U2 EXIT RESP RX CLKS - Applicable to locally initiated Ux exit: Minimum LFPS reception from remote to consider Ux exit handshake is successful. - This field is encoded as the pipe clk [8ns] count for the LFPS. -- 1: 8ns -- 2: 16ns -- 3: 24ns, and so on Reset Source: rst_mod_g_rst_n

14.7.3.2.2.382 USB2SS_LINK_LINK_LINK_SETTINGS Register

14.7.3.2.2.382.1 USB2SS_LINK_LINK_LINK_SETTINGS Register (Offset = 20h) [reset = 45900000h]

Link Setting Register - Link Layer User Control Register for enabling Link/PHY-specific options. - This register is common for all SS ports.

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Table 14-12456. Instance Table

Instance Name	Physical Address
USB0	3100 D020h + formula

Figure 14-6155. USB2SS_LINK_LINK_LINK_SETTINGS Name Register

31	30	29	28	27	26	25	24
RESERVED_31	U1_RESID_TIMER_US			RESERVED_27	PM_LC_TIMER_US		
R/W	R/W			R/W	R/W		
0h	4h			0h	5h		
23	22	21	20	19	18	17	16
PM_ENTRY_TIMER_US				RESERVED_0_19			
R/W				R/W			
9h				0h			
15	14	13	12	11	10	9	8
RESERVED_0_19							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_0_19							
R/W							
0h							

Table 14-12457. USB2SS_LINK_LINK_LINK_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_31	R/W	0h	Reserved
30:28	U1_RESID_TIMER_US	R/W	4h	Programmable U1 MIN RESIDENCY TIMER This field specifies U1 MIN RESIDENCY TIMER value in us. Set to 0 to disable the timer. Reset Source: rst_mod_g_rst_n
27	RESERVED_27	R/W	0h	Reserved
26:24	PM_LC_TIMER_US	R/W	5h	Programmable PM_LC_TIMER This field specifies PM_LC_TIMER value in us. Reset Source: rst_mod_g_rst_n
23:20	PM_ENTRY_TIMER_US	R/W	9h	Programmable PM_ENTRY_TIMER This field specifies PM_ENTRY_TIMER value in us. Reset Source: rst_mod_g_rst_n
19:0	RESERVED_0_19	R/W	0h	Reserved

14.7.3.2.2.383 USB2SS_LINK_LINK_LLUCTL Register

14.7.3.2.2.383.1 USB2SS_LINK_LINK_LLUCTL Register (Offset = 24h) [reset = 800080h]

Link User Control Register - Link Layer User Control Register for enabling Link/PHY-specific options. - This register is common for all SS ports.

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Table 14-12458. Instance Table

Instance Name	Physical Address
USB0	3100 D024h + formula

Figure 14-6156. USB2SS_LINK_LINK_LLUCTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">RESERVED_30_31</td><td>SUPPORT_P4_PG</td><td>SUPPORT_P4</td><td colspan="4">RESERVED_24_27</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>DISRXDET_LTSSM_TIMER_OVRRD</td><td colspan="7">RESERVED_13_22</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>1h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_13_22</td><td>U2P3CPMOK</td><td>EN_RESET_PIPE_AFTER_PHY_MUX</td><td colspan="3">RESERVED_8_10</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td>R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MASK_PIPE_RESET</td><td>RESERVED_6</td><td>NO_UX_EXIT_P0_TRANS</td><td colspan="5">RESERVED_0_4</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="5">R/W</td></tr>
<tr><td>1h</td><td>0h</td><td>0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-12459. USB2SS_LINK_LINK_LLUCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_30_31	R/W	0h	Reserved
29	SUPPORT_P4_PG	R/W	0h	PHY P4 Power gate mode [PG] is enabled. Set this bit if the PHY supports PG mode in P4. This bit is used only for Synopsys PHY. Reset Source: rst_mod_g_rst_n
28	SUPPORT_P4	R/W	0h	Support PHY P3.CPM and P4 Power States. When this bit is set, the controller puts the PHY in P3.CPM or P4 in certain states. This bit is used only for Synopsys PHY. Reset Source: rst_mod_g_rst_n
27:24	RESERVED_24_27	R/W	0h	Reserved
23	DISRXDET_LTSSM_TIMER_OVRRD	R/W	1h	DisRxDet_LTSSM_Timer_Ovrrd. When DisRxDetU3RxDet is asserted in Polling or U1, the timeout expires immediately. Reset Source: rst_mod_g_rst_n
22:13	RESERVED_13_22	R/W	0h	Reserved

Table 14-12459. USB2SS_LINK_LINK_LLUCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	U2P3CPMOK	R/W	0h	P3CPM OK for U2/SSInactive [U2P3CPMok] - 0: During link state U2/SS.Inactive, put PHY in P2 [Default] - 1: During link state U2/SS.Inactive, put PHY in P3CPM. Note: For a port, if both GUCTL1[25]=1 and LUCTL[12]=1, LUCTL[12]=1 takes priority. Reset Source: rst_mod_g_rst_n
11	EN_RESET_PIPE_AFTER_PHY_MUX	R/W	0h	en_reset_pipe_after_phy_mux. The controller issues USB 3.0 PHY reset after DisRxDetU3RxDet is de-asserted. Reset Source: rst_mod_g_rst_n
10:8	RESERVED_8_10	R/W	0h	Reserved
7	MASK_PIPE_RESET	R/W	1h	Mask pipe reset. If this bit is set, controller blocks pipe_reset_n from going to the PHY when DisRxDetU3RxDet=1. Reset Source: rst_mod_g_rst_n
6	RESERVED_6	R/W	0h	Reserved
5	NO_UX_EXIT_P0_TRANS	R/W	0h	no_ux_exit_p0_trans. Link LTSSM detects Ux_exit LFPS when P0 transition is on-going by default. If this bit is set, Link LTSSM may miss Ux_exit LFPS when P0 transition is happening. Reset Source: rst_mod_g_rst_n
4:0	RESERVED_0_4	R/W	0h	Reserved

14.7.3.2.2.384 USB2SS_LINK_LINK_LPTMDPDELAY Register

14.7.3.2.2.384.1 USB2SS_LINK_LINK_LPTMDPDELAY Register (Offset = 28h) [reset = C00h]

Link Datapath Delay Register - Link Layer Timer Register for P3CPM/P4 Residency. - This register is common for all SS ports.

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Table 14-12460. Instance Table

Instance Name	Physical Address
USB0	3100 D028h + formula

Figure 14-6157. USB2SS_LINK_LINK_LPTMDPDELAY Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_22_31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">RESERVED_22_31</td><td colspan="6">P3CPMP4_RESIDENCY</td></tr>
<tr><td colspan="2">R/W</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">P3CPMP4_RESIDENCY</td><td colspan="2">RESERVED_0_9</td></tr>
<tr><td colspan="6">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">3h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED_0_9</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12461. USB2SS_LINK_LINK_LPTMDPDELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED_22_31	R/W	0h	Reserved
21:10	P3CPMP4_RESIDENCY	R/W	3h	p3cpmp4 residency timer value. Minimum number of suspend_clk periods that the controller needs to stay in P3.CPM or P4 before exiting P3.CPM or P4. This field is used only for Synopsys PHY. Reset Source: rst_mod_g_rst_n
9:0	RESERVED_0_9	R/W	0h	Reserved

14.7.3.2.2.385 USB2SS_DEBUG_DEBUG_U3RHBDBG Register

14.7.3.2.2.385.1 USB2SS_DEBUG_DEBUG_U3RHBDBG Register (Offset = 0h) [reset = 0h]

U3 Root Hub Debug Register

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Table 14-12462. Instance Table

Instance Name	Physical Address
USB0	3100 D800h + formula

Figure 14-6158. USB2SS_DEBUG_DEBUG_U3RHBDBG Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				TPCFG_TOUT_CTRL	RESERVED_0_2		
R				R/W	R		
0h				0h	0h		

Table 14-12463. USB2SS_DEBUG_DEBUG_U3RHBDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_1	R	0h	Reserved_1
3	TPCFG_TOUT_CTRL	R/W	0h	tpcfg_tout_ctrl This bit controls the USB 3.0 port configuration timeout duration. - 1: The port configuration timeout counter resets when the link is not in U0. - 0: The port configuration timeout counter does not reset if the link enters recovery or exits U0. Reset Source: rst_mod_g_rst_n
2:0	RESERVED_0_2	R	0h	Reserved_0_2

14.7.3.2.2.386 USB2SS_DEBUG_RAM0_RAM0_J Register

14.7.3.2.2.386.1 USB2SS_DEBUG_RAM0_RAM0_J Register (Offset = 0h) [reset = 0h]

RAM0 memory region accessible through config interface for debug purpose only.

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Table 14-12464. Instance Table

Instance Name	Physical Address
USB0	3104 0000h + formula

Figure 14-6159. USB2SS_DEBUG_RAM0_RAM0_j Name Register

31	30	29	28	27	26	25	24
MEM							
R/W							
0h							
23	22	21	20	19	18	17	16
MEM							
R/W							
0h							
15	14	13	12	11	10	9	8
MEM							
R/W							
0h							
7	6	5	4	3	2	1	0
MEM							
R/W							
0h							

Table 14-12465. USB2SS_DEBUG_RAM0_RAM0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEM	R/W	0h	Memory location Reset Source: rst_mod_g_rst_n

14.7.4 Memory Interfaces Registers

14.7.4.1 FSS0

FSS0

14.7.4.1.1 FSS0 Summaries

FSS0 Summaries

Table 14-12466. ECC_AGGR Registers, Base Address=0071 6000h, Length=1024

Offset	Length	Register Name	FSS0 Physical Address
0h	32	ECC_AGGR_REV	0071 6000h
8h	32	ECC_AGGR_VECTOR	0071 6008h
Ch	32	ECC_AGGR_STAT	0071 600Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 6010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 603Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 6040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 6080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 60C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 613Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 6140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 6180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 61C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 6200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 6204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 6208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 620Ch

Table 14-12467. ECC_AGGR Registers, Base Address=0071 7000h, Length=1024

Offset	Length	Register Name	FSS0 Physical Address
0h	32	ECC_AGGR_REV	0071 7000h
8h	32	ECC_AGGR_VECTOR	0071 7008h
Ch	32	ECC_AGGR_STAT	0071 700Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0071 7010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0071 703Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0071 7040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0071 7080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0071 70C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0071 713Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0071 7140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0071 7180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0071 71C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0071 7200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0071 7204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0071 7208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0071 720Ch

Table 14-12468. FSS_GENREGS Registers, Base Address=0FC0 0000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS_GENREGS_REVISION	0FC0 0000h

Table 14-12469. FSS0_FSAS_GENREGS Registers, Base Address=0FC1 0000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS0_FSAS_GENREGS_REVISION	0FC1 0000h
4h	32	FSS0_FSAS_GENREGS_SYSCONFIG	0FC1 0004h
80h	32	FSS0_FSAS_GENREGS_DP_ERR_INJ_CTRL	0FC1 0080h
10h	32	FSS0_FSAS_GENREGS_IRQ_EOI	0FC1 0010h + formula
14h	32	FSS0_FSAS_GENREGS_IRQ_STATUS_RAW	0FC1 0014h + formula
18h	32	FSS0_FSAS_GENREGS_IRQ_STATUS	0FC1 0018h + formula
1Ch	32	FSS0_FSAS_GENREGS_IRQ_ENABLE_SET	0FC1 001Ch + formula
20h	32	FSS0_FSAS_GENREGS_IRQ_ENABLE_CLR	0FC1 0020h + formula
30h	32	FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J	0FC1 0030h + formula
34h	32	FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J	0FC1 0034h + formula
70h	32	FSS0_FSAS_GENREGS_ERR_ECC_BLOCK_ADR	0FC1 0070h + formula
74h	32	FSS0_FSAS_GENREGS_ERR_ECC_TYPE	0FC1 0074h + formula
78h	32	FSS0_FSAS_GENREGS_ERR_WRT_TYPE	0FC1 0078h + formula

Table 14-12470. FSAS_OTFA_REGS Registers, Base Address=0FC2 0000h, Length=4096

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSAS_OTFA_REGS_REVID	0FC2 0000h
4h	32	FSAS_OTFA_REGS_SCFG	0FC2 0004h
8h	32	FSAS_OTFA_REGS_ISR	0FC2 0008h
Ch	32	FSAS_OTFA_REGS_IS	0FC2 000Ch
10h	32	FSAS_OTFA_REGS_IES	0FC2 0010h
14h	32	FSAS_OTFA_REGS_IEC	0FC2 0014h
18h	32	FSAS_OTFA_REGS_CCFG	0FC2 0018h
1Ch	32	FSAS_OTFA_REGS_CSTATUS	0FC2 001Ch
220h	32	FSAS_OTFA_REGS_IRQADDINFO0	0FC2 0220h
224h	32	FSAS_OTFA_REGS_IRQADDINFO1	0FC2 0224h
228h	32	FSAS_OTFA_REGS_MACCACHEINFO	0FC2 0228h
22Ch	32	FSAS_OTFA_REGS_RMWRMCNT	0FC2 022Ch
20h	32	FSAS_OTFA_REGS_RG_RGCFG_J	0FC2 0020h + formula
24h	32	FSAS_OTFA_REGS_RG_RGMACST_J	0FC2 0024h + formula
28h	32	FSAS_OTFA_REGS_RG_RGST_J	0FC2 0028h + formula
2Ch	32	FSAS_OTFA_REGS_RG_RGSI_J	0FC2 002Ch + formula
30h	32	FSAS_OTFA_REGS_RG_RKEYE_J_K	0FC2 0030h + formula
50h	32	FSAS_OTFA_REGS_RG_RKEYEP_J_K	0FC2 0050h + formula
70h	32	FSAS_OTFA_REGS_RG_RKEYA_J_K	0FC2 0070h + formula
80h	32	FSAS_OTFA_REGS_RG_RKEYAP_J_K	0FC2 0080h + formula
90h	32	FSAS_OTFA_REGS_RG_RIV_J_K	0FC2 0090h + formula

Table 14-12471. OSPI_FLASH_CFG Registers, Base Address=0FC4 0000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	OSPI_FLASH_CFG_CONFIG_REG	0FC4 0000h

Table 14-12471. OSPI_FLASH_CFG Registers, Base Address=0FC4 0000h, Length=256 (continued)

Offset	Length	Register Name	FSS0 Physical Address
4h	32	OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG	0FC4 0004h
8h	32	OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG	0FC4 0008h
Ch	32	OSPI_FLASH_CFG_DEV_DELAY_REG	0FC4 000Ch
10h	32	OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG	0FC4 0010h
14h	32	OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG	0FC4 0014h
18h	32	OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG	0FC4 0018h
1Ch	32	OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG	0FC4 001Ch
20h	32	OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG	0FC4 0020h
24h	32	OSPI_FLASH_CFG_REMAP_ADDR_REG	0FC4 0024h
28h	32	OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG	0FC4 0028h
2Ch	32	OSPI_FLASH_CFG_SRAM_FILL_REG	0FC4 002Ch
30h	32	OSPI_FLASH_CFG_TX_THRESH_REG	0FC4 0030h
34h	32	OSPI_FLASH_CFG_RX_THRESH_REG	0FC4 0034h
38h	32	OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG	0FC4 0038h
3Ch	32	OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG	0FC4 003Ch
40h	32	OSPI_FLASH_CFG_IRQ_STATUS_REG	0FC4 0040h
44h	32	OSPI_FLASH_CFG_IRQ_MASK_REG	0FC4 0044h
50h	32	OSPI_FLASH_CFG_LOWER_WR_PROT_REG	0FC4 0050h
54h	32	OSPI_FLASH_CFG_UPPER_WR_PROT_REG	0FC4 0054h
58h	32	OSPI_FLASH_CFG_WR_PROT_CTRL_REG	0FC4 0058h
60h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG	0FC4 0060h
64h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG	0FC4 0064h
68h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG	0FC4 0068h
6Ch	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG	0FC4 006Ch
70h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG	0FC4 0070h
74h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG	0FC4 0074h
78h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG	0FC4 0078h
7Ch	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG	0FC4 007Ch
80h	32	OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG	0FC4 0080h
8Ch	32	OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG	0FC4 008Ch
90h	32	OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG	0FC4 0090h
94h	32	OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG	0FC4 0094h
A0h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG	0FC4 00A0h
A4h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG	0FC4 00A4h
A8h	32	OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG	0FC4 00A8h
ACh	32	OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG	0FC4 00ACh
B0h	32	OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG	0FC4 00B0h
B4h	32	OSPI_FLASH_CFG_PHY_CONFIGURATION_REG	0FC4 00B4h
B8h	32	OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG	0FC4 00B8h
BCh	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG	0FC4 00BCh

Table 14-12471. OSPI_FLASH_CFG Registers, Base Address=0FC4 0000h, Length=256 (continued)

Offset	Length	Register Name	FSS0 Physical Address
C0h	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG	0FC4 00C0h
E0h	32	OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG	0FC4 00E0h
E4h	32	OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG	0FC4 00E4h
FCh	32	OSPI_FLASH_CFG_MODULE_ID_REG	0FC4 00FCh

Table 14-12472. OSPI_CFG Registers, Base Address=0FC4 4000h, Length=512

Offset	Length	Register Name	FSS0 Physical Address
0h	32	OSPI_CFG_PID	0FC4 4000h
4h	32	OSPI_CFG_CTRL	0FC4 4004h
8h	32	OSPI_CFG_STAT	0FC4 4008h
20h	32	OSPI_CFG_EOI	0FC4 4020h

Table 14-12473. FSS0_FOTA_GENREGS Registers, Base Address=0FC6 0000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS0_FOTA_GENREGS_FOTA_INIT	0FC6 0000h
4h	32	FSS0_FOTA_GENREGS_FOTA_CTRL	0FC6 0004h
8h	32	FSS0_FOTA_GENREGS_FOTA_ERR_INFO	0FC6 0008h
10h	32	FSS0_FOTA_GENREGS_FOTA_GP0	0FC6 0010h
14h	32	FSS0_FOTA_GENREGS_FOTA_GP1	0FC6 0014h
18h	32	FSS0_FOTA_GENREGS_FOTA_ADDR	0FC6 0018h
1Ch	32	FSS0_FOTA_GENREGS_FOTA_CNT	0FC6 001Ch
20h	32	FSS0_FOTA_GENREGS_STS_IRQ_EOI	0FC6 0020h + formula
24h	32	FSS0_FOTA_GENREGS_STS_IRQ_STATUS_RAW	0FC6 0024h + formula
28h	32	FSS0_FOTA_GENREGS_STS_IRQ_STATUS	0FC6 0028h + formula
2Ch	32	FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_SET	0FC6 002Ch + formula
30h	32	FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_CLR	0FC6 0030h + formula
40h	32	FSS0_FOTA_GENREGS_ERR_STS_IRQ_EOI	0FC6 0040h + formula
44h	32	FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS_RAW	0FC6 0044h + formula
48h	32	FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS	0FC6 0048h + formula
4Ch	32	FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_SET	0FC6 004Ch + formula
50h	32	FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_CLR	0FC6 0050h + formula

Table 14-12474. FSS0_PDMEM_GENREGS Registers, Base Address=0FC6 1000h, Length=2048

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS0_PDMEM_GENREGS_LOC_J	0FC6 1000h + formula

Table 14-12475. FSS0_IMEM_GENREGS Registers, Base Address=0FC6 2000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS0_IMEM_GENREGS_LOC_J	0FC6 2000h + formula

Table 14-12476. FSS0_WBUF_GENREGS Registers, Base Address=0FC6 3000h, Length=512

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS0_WBUF_GENREGS_LOC_J	0FC6 3000h + formula

Table 14-12477. DAT_REG1 Registers, Base Address=6000 0000h, Length=134217728

Offset	Length	Register Name	FSS0 Physical Address
0h	32	DAT_REG1_HPB_DATA_MEM_J	6000 0000h + formula

Table 14-12478. DAT_REG0 Registers, Base Address=0004 0000 0000h, Length=4294967296

Offset	Length	Register Name	FSS0 Physical Address
0h	32	DAT_REG0_HPB_DATA_MEM_J	0004 0000 0000h + formula

Table 14-12479. DAT_REG3 Registers, Base Address=0005 0000 0000h, Length=4294967296

Offset	Length	Register Name	FSS0 Physical Address
0h	32	DAT_REG3_HPB_DATA_MEM_J	0005 0000 0000h + formula

14.7.4.1.2 FSS0 Registers

FSS0 Registers

14.7.4.1.2.1 ECC_AGGR_REV Register

14.7.4.1.2.1.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-12480. Instance Table

Instance Name	Physical Address
FSS0	0071 7000h

Figure 14-6160. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
7h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-12481. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.4.1.2.2 ECC_AGGR_VECTOR Register

14.7.4.1.2.2.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12482. Instance Table

Instance Name	Physical Address
FSS0	0071 7008h

Figure 14-6161. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 14-12483. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.4.1.2.3 ECC_AGGR_STAT Register

14.7.4.1.2.3.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

Return to Summary Table

Table 14-12484. Instance Table

Instance Name	Physical Address
FSS0	0071 700Ch

Figure 14-6162. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-12485. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.4.1.2.4 ECC_AGGR_RESERVED_SVBUS_J Register

14.7.4.1.2.4.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to Summary Table

Table 14-12486. Instance Table

Instance Name	Physical Address
FSS0	0071 7010h + formula

Figure 14-6163. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-12487. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.4.1.2.5 ECC_AGGR_SEC_EOI_REG Register

14.7.4.1.2.5.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-12488. Instance Table

Instance Name	Physical Address
FSS0	0071 703Ch

Figure 14-6164. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12489. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.1.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

14.7.4.1.2.6.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-12490. Instance Table

Instance Name	Physical Address
FSS0	0071 7040h

Figure 14-6165. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_PEND
NONE							R/W1TS
0h							0h

Table 14-12491. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.7.4.1.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.7.4.1.2.7.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-12492. Instance Table

Instance Name	Physical Address
FSS0	0071 7080h

Figure 14-6166. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-12493. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.7.4.1.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.7.4.1.2.8.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12494. Instance Table

Instance Name	Physical Address
FSS0	0071 70C0h

Figure 14-6167. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-12495. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.7.4.1.2.9 ECC_AGGR_DED_EOI_REG Register

14.7.4.1.2.9.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-12496. Instance Table

Instance Name	Physical Address
FSS0	0071 713Ch

Figure 14-6168. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12497. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.1.2.10 ECC_AGGR_DED_STATUS_REG0 Register

14.7.4.1.2.10.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-12498. Instance Table

Instance Name	Physical Address
FSS0	0071 7140h

Figure 14-6169. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_PEND
NONE							R/W1TS
0h							0h

Table 14-12499. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.7.4.1.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.7.4.1.2.11.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12500. Instance Table

Instance Name	Physical Address
FSS0	0071 7180h

Figure 14-6170. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-12501. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.7.4.1.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.7.4.1.2.12.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12502. Instance Table

Instance Name	Physical Address
FSS0	0071 71C0h

Figure 14-6171. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-12503. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.7.4.1.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

14.7.4.1.2.13.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12504. Instance Table

Instance Name	Physical Address
FSS0	0071 7200h

Figure 14-6172. ECC_AGGR_AGGR_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12505. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.4.1.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

14.7.4.1.2.14.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 14-12506. Instance Table

Instance Name	Physical Address
FSS0	0071 7204h

Figure 14-6173. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12507. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.4.1.2.15 ECC_AGGR_AGGR_STATUS_SET Register

14.7.4.1.2.15.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-12508. Instance Table

Instance Name	Physical Address
FSS0	0071 7208h

Figure 14-6174. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-12509. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.4.1.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

14.7.4.1.2.16.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12510. Instance Table

Instance Name	Physical Address
FSS0	0071 720Ch

Figure 14-6175. ECC_AGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12511. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.4.1.2.17 ECC_AGGR_REV Register

14.7.4.1.2.17.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-12512. Instance Table

Instance Name	Physical Address
FSS0	0071 7000h

Figure 14-6176. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-12513. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.4.1.2.18 ECC_AGGR_VECTOR Register

14.7.4.1.2.18.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12514. Instance Table

Instance Name	Physical Address
FSS0	0071 7008h

Figure 14-6177. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-12515. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.4.1.2.19 ECC_AGGR_STAT Register

14.7.4.1.2.19.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-12516. Instance Table

Instance Name	Physical Address
FSS0	0071 700Ch

Figure 14-6178. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-12517. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.4.1.2.20 ECC_AGGR_RESERVED_SVBUS_J Register

14.7.4.1.2.20.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-12518. Instance Table

Instance Name	Physical Address
FSS0	0071 7010h + formula

Figure 14-6179. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-12519. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.4.1.2.21 ECC_AGGR_SEC_EOI_REG Register

14.7.4.1.2.21.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-12520. Instance Table

Instance Name	Physical Address
FSS0	0071 703Ch

Figure 14-6180. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12521. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.1.2.22 ECC_AGGR_SEC_STATUS_REG0 Register

14.7.4.1.2.22.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-12522. Instance Table

Instance Name	Physical Address
FSS0	0071 7040h

Figure 14-6181. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_PEND
NONE							R/W1TS
0h							0h

Table 14-12523. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.7.4.1.2.23 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.7.4.1.2.23.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-12524. Instance Table

Instance Name	Physical Address
FSS0	0071 7080h

Figure 14-6182. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-12525. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.7.4.1.2.24 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.7.4.1.2.24.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-12526. Instance Table

Instance Name	Physical Address
FSS0	0071 70C0h

Figure 14-6183. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-12527. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.7.4.1.2.25 ECC_AGGR_DED_EOI_REG Register

14.7.4.1.2.25.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-12528. Instance Table

Instance Name	Physical Address
FSS0	0071 713Ch

Figure 14-6184. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12529. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.1.2.26 ECC_AGGR_DED_STATUS_REG0 Register

14.7.4.1.2.26.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-12530. Instance Table

Instance Name	Physical Address
FSS0	0071 7140h

Figure 14-6185. ECC_AGGR_DED_STATUS_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>RAMECC_PEND</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12531. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

14.7.4.1.2.27 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.7.4.1.2.27.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-12532. Instance Table

Instance Name	Physical Address
FSS0	0071 7180h

Figure 14-6186. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>RAMECC_ENABLE_SET</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12533. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

14.7.4.1.2.28 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.7.4.1.2.28.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12534. Instance Table

Instance Name	Physical Address
FSS0	0071 71C0h

Figure 14-6187. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>RAMECC_ENABLE_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12535. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

14.7.4.1.2.29 ECC_AGGR_AGGR_ENABLE_SET Register

14.7.4.1.2.29.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12536. Instance Table

Instance Name	Physical Address
FSS0	0071 7200h

Figure 14-6188. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12537. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.4.1.2.30 ECC_AGGR_AGGR_ENABLE_CLR Register

14.7.4.1.2.30.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12538. Instance Table

Instance Name	Physical Address
FSS0	0071 7204h

Figure 14-6189. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12539. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.4.1.2.31 ECC_AGGR_AGGR_STATUS_SET Register

14.7.4.1.2.31.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12540. Instance Table

Instance Name	Physical Address
FSS0	0071 7208h

Figure 14-6190. ECC_AGGR_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12541. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.4.1.2.32 ECC_AGGR_AGGR_STATUS_CLR Register

14.7.4.1.2.32.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12542. Instance Table

Instance Name	Physical Address
FSS0	0071 720Ch

Figure 14-6191. ECC_AGGR_AGGR_STATUS_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12543. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.4.1.2.33 FSS_GENREGS_REVISION Register

14.7.4.1.2.33.1 FSS_GENREGS_REVISION Register (Offset = 0h) [reset = 68502200h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-12544. Instance Table

Instance Name	Physical Address
FSS0	0FC0 0000h

Figure 14-6192. FSS_GENREGS_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6850h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6850h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">4h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-12545. FSS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field Reset Source: vbus_mod_g_rst_n
15:11	REVRTL	R	4h	RTL revision. Will vary depending on release. Reset Source: vbus_mod_g_rst_n
10:8	REVMAJ	R	2h	Major revision Reset Source: vbus_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_mod_g_rst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.34 FSS0_FSAS_GENREGS_REVISION Register

14.7.4.1.2.34.1 FSS0_FSAS_GENREGS_REVISION Register (Offset = 0h) [reset = 68502200h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-12546. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0000h

Figure 14-6193. FSS0_FSAS_GENREGS_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6850h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6850h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">4h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-12547. FSS0_FSAS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field Reset Source: vbus_mod_g_rst_n
15:11	REVRTL	R	4h	RTL revision. Will vary depending on release. Reset Source: vbus_mod_g_rst_n
10:8	REVMAJ	R	2h	Major revision Reset Source: vbus_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_mod_g_rst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.35 FSS0_FSAS_GENREGS_SYSCONFIG Register

14.7.4.1.2.35.1 FSS0_FSAS_GENREGS_SYSCONFIG Register (Offset = 4h) [reset = 5000h]

Controls various parameters of the cotroller state.

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Table 14-12548. Instance Table

Instance Name	**Physical Address**
FSS0	0FC1 0004h

Figure 14-6194. FSS0_FSAS_GENREGS_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					HW_RW_DELAY_COUNT		
NONE					R/W		
0h					Ah		
15	14	13	12	11	10	9	8
HW_RW_DELAY_COUNT					HW_RW_DELAY_EN	DP_EN	OSPI_32B_DISABLE_MODE
R/W					R/W	R/W	R/W
Ah					0h	0h	0h
7	6	5	4	3	2	1	0
DISXIP	OSPI_DDR_DISABLE_MODE	RESERVED		ECC_DISABLE_ADR	FSS_AES_EN_IPCFG	RESERVED	ECC_EN
R/W	R/W	NONE		R/W	R	NONE	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-12549. FSS0_FSAS_GENREGS_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:11	HW_RW_DELAY_COUNT	R/W	Ah	Delay for switching between reads and writes Reset Source: vbus_mod_g_rst_n
10	HW_RW_DELAY_EN	R/W	0h	Enable delay when switching between reads and writes to avoid read-write collision for sensitive logic. Reset Source: vbus_mod_g_rst_n
9	DP_EN	R/W	0h	0 Safety double pumping disabled. 1 Safety double pumping enabled Reset Source: vbus_mod_g_rst_n
8	OSPI_32B_DISABLE_MODE	R/W	0h	0 OSPI 32bit mode enabled. 1 OSPI 32bit mode disabled Reset Source: vbus_mod_g_rst_n
7	DISXIP	R/W	0h	This field is used to disable XIP prefetching. 0 XIP Prefetch Enabled. 1 XIP prefetch disabled Please note that this is referring to prefetching feature that is useful for linear accesses associated with XIP. This is NOT referring to XIP features implemented in flash Controller or memory device. Reset Source: vbus_mod_g_rst_n
6	OSPI_DDR_DISABLE_MODE	R/W	0h	0 OSPI DDR mode enabled. 1 OSPI DDR mode disabled Reset Source: vbus_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved

Table 14-12549. FSS0_FSAS_GENREGS_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ECC_DISABLE_ADR	R/W	0h	0 Block address within ECC calculation, 1 Block address not within ECC calculation Reset Source: vbus_mod_g_rst_n
2	FSS_AES_EN_IPCFG	R	0h	1 select security, 0 disable security Reset Source: vbus_mod_g_rst_n
1	RESERVED	NONE	0h	Reserved
0	ECC_EN	R/W	0h	0 ECC disabled. 1 ECC enabled Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.36 FSS0_FSAS_GENREGS_DP_ERR_INJ_CTRL Register

14.7.4.1.2.36.1 FSS0_FSAS_GENREGS_DP_ERR_INJ_CTRL Register (Offset = 80h) [reset = 0h]

This register is used to setup double pumping error injection. Only one error injection enable field has to be set in this register at a given time. After error injection is enabled, a read must be issued to a valid flash address in order to trigger the error. Once triggered, the error will be reported using IRQ.STATUS register dp_cmd_err/dp_ret_err fields and corresponding interrupt fsas_ecc_intr_err_pend/fsas_ecc_intr_err_req will be generated if enabled.

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Table 14-12550. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0080h

Figure 14-6195. FSS0_FSAS_GENREGS_DP_ERR_INJ_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
BIT_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED			RET_NFIRST_LAST	EN_DUPL_RET	EN_ORIG_RET	EN_DUPL_CMD	EN_ORIG_CMD
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-12551. FSS0_FSAS_GENREGS_DP_ERR_INJ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	BIT_SEL	R/W	0h	Bit select for injecting error on command or read return fields. For command error, only 0 through 47 are valid values for bit select. For read return error, only 0 through 166 are valid values for bit select. Reset Source: vbus_mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved
4	RET_NFIRST_LAST	R/W	0h	1'b0 - Inject on first read return phase, 1'b1 - Inject on last read return phase Reset Source: vbus_mod_g_rst_n
3	EN_DUPL_RET	R/W	0h	Enable error injection on duplicate read return fields. Reset Source: vbus_mod_g_rst_n
2	EN_ORIG_RET	R/W	0h	Enable error injection on original read return fields. Reset Source: vbus_mod_g_rst_n
1	EN_DUPL_CMD	R/W	0h	Enable error injection on duplicate command fields. Reset Source: vbus_mod_g_rst_n

Table 14-12551. FSS0_FSAS_GENREGS_DP_ERR_INJ_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN_ORIG_CMD	R/W	0h	Enable error injection on original command fields. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.37 FSS0_FSAS_GENREGS_IRQ_EOI Register

14.7.4.1.2.37.1 FSS0_FSAS_GENREGS_IRQ_EOI Register (Offset = 10h) [reset = 0h]

The End of Interrupt (EOI) Register allows the CPU to acknowledge completion of fsas_ecc_intr_err_req pulse interrupt. When this register is written to 1'b0, INTD logic used for converting fsas_ecc_intr_err_pend level interrupt to pulse will be re-armed. That is, if interrupt sources remain after writing this register to 1'b0, another pulse interrupt will be triggered by INTD. Conversely, if this register is not written to 1'b0 after fsas_ecc_intr_err_req pulse interrupt is received, then another pulse interrupt will not be received as INTD has not been re-armed. This register will be reset one cycle after it has been written to. Please note that the reason for writing 1'b0 is because there is only one interrupt (no interrupt aggregation) associated with this EOI and the INTD vector associated with this interrupt is 1'b0.

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Table 14-12552. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0010h + formula

Figure 14-6196. FSS0_FSAS_GENREGS_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							W
0h							0h

Table 14-12553. FSS0_FSAS_GENREGS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	W	0h	Write 1'b0 to acknowledge fsas_ecc_intr_err_req pulse interrupt. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.38 FSS0_FSAS_GENREGS_IRQ_STATUS_RAW Register

14.7.4.1.2.38.1 FSS0_FSAS_GENREGS_IRQ_STATUS_RAW Register (Offset = 14h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources associated with each bit in this register to be manually set when writing a 1 to a specific bit. This register corresponds to fsas_ecc_intr_err_pend (level) and fsas_ecc_intr_err_req (pulse) interrupt outputs. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-12554. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0014h + formula

Figure 14-6197. FSS0_FSAS_GENREGS_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DP_RET_ERROR	DP_CMD_ERROR	ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 14-12555. FSS0_FSAS_GENREGS_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DP_RET_ERROR	R/W1TS	0h	Safety double pumping read return error Reset Source: vbus_mod_g_rst_n
3	DP_CMD_ERROR	R/W1TS	0h	Safety double pumping command error Reset Source: vbus_mod_g_rst_n
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	An ECC error occurred on 2 bits and was not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	An ECC error occurred on only 1 bit and was corrected Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.39 FSS0_FSAS_GENREGS_IRQ_STATUS Register

14.7.4.1.2.39.1 FSS0_FSAS_GENREGS_IRQ_STATUS Register (Offset = 18h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources associated with each bit in this register to be manually cleared when writing a 1 to a specific bit. This register corresponds to fsas_ecc_intr_err_pend (level) and fsas_ecc_intr_err_req (pulse) interrupt outputs. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-12556. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0018h + formula

Figure 14-6198. FSS0_FSAS_GENREGS_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DP_RET_ERROR	DP_CMD_ERROR	ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-12557. FSS0_FSAS_GENREGS_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DP_RET_ERROR	R/W1TC	0h	Safety double pumping read return error Reset Source: vbus_mod_g_rst_n
3	DP_CMD_ERROR	R/W1TC	0h	Safety double pumping command error Reset Source: vbus_mod_g_rst_n
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	An ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. corrected Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.40 FSS0_FSAS_GENREGS_IRQ_ENABLE_SET Register

14.7.4.1.2.40.1 FSS0_FSAS_GENREGS_IRQ_ENABLE_SET Register (Offset = 1Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources associated with each bit in this register to be manually enabled when writing a 1 to a specific bit. This register corresponds to fsas_ecc_intr_err_pend (level) and fsas_ecc_intr_err_req (pulse) interrupt outputs. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-12558. Instance Table

Instance Name	Physical Address
FSS0	0FC1 001Ch + formula

Figure 14-6199. FSS0_FSAS_GENREGS_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DP_RET_ERROR	DP_CMD_ERROR	ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 14-12559. FSS0_FSAS_GENREGS_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DP_RET_ERROR	R/W1TS	0h	Safety double pumping read return error Reset Source: vbus_mod_g_rst_n
3	DP_CMD_ERROR	R/W1TS	0h	Safety double pumping command error Reset Source: vbus_mod_g_rst_n
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. corrected Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.41 FSS0_FSAS_GENREGS_IRQ_ENABLE_CLR Register

14.7.4.1.2.41.1 FSS0_FSAS_GENREGS_IRQ_ENABLE_CLR Register (Offset = 20h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources associated with each bit in this register to be manually disabled when writing a 1 to a specific bit. This register corresponds to fsas_ecc_intr_err_pend (level) and fsas_ecc_intr_err_req (pulse) interrupt outputs. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-12560. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0020h + formula

Figure 14-6200. FSS0_FSAS_GENREGS_IRQ_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DP_RET_ERROR	DP_CMD_ERROR	ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-12561. FSS0_FSAS_GENREGS_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DP_RET_ERROR	R/W1TC	0h	Safety double pumping read return error Reset Source: vbus_mod_g_rst_n
3	DP_CMD_ERROR	R/W1TC	0h	Safety double pumping command error Reset Source: vbus_mod_g_rst_n
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. corrected Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.42 FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J Register

14.7.4.1.2.42.1 FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J Register (Offset = 30h) [reset = 0h]

This defines the start of the ECC region in 4KBytes steps.

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Table 14-12562. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0030h + formula

Figure 14-6201. FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">R_START</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_START</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_START</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12563. FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START	R/W	0h	This defines the start of the ECC region in 4KBytes steps. Address start = {start[19:0], 0x000} 0x0 means the start is 0x0000_0000 0x1 means the start is 0x0000_1000 0xA means the start is 0x0000_A000 Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.43 FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J Register

14.7.4.1.2.43.1 FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J Register (Offset = 34h) [reset = 0h]

This defines the size of the ECC region in 4KBytes steps.

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Table 14-12564. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0034h + formula

Figure 14-6202. FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE							
R/W							
0h							

Table 14-12565. FSS0_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE	R/W	0h	This defines the size of the ECC region in 4KBytes steps 0x0 means the size is zero and disabled 0x1 means the size is 4KBytes 0xA means the size is 40KBytes 0xF_FFFF means the size is 4GBytes Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.44 FSS0_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register

14.7.4.1.2.44.1 FSS0_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register (Offset = 70h) [reset = 0h]

The ERR_ECC_BLOCK_ADR register holds the current top of stack ECC error block address, this is only valid when the ecc_err_valid is set

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Table 14-12566. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0070h + formula

Figure 14-6203. FSS0_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Name Register

31	30	29	28	27	26	25	24
ECC_ERROR_BLOCK_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ERROR_BLOCK_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ERROR_BLOCK_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ERROR_BLOCK_ADDR			RESERVED				
R			NONE				
0h			0h				

Table 14-12567. FSS0_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	ECC_ERROR_BLOCK_ADDR	R	0h	ECC 32 byte aligned block address Reset Source: vbus_mod_g_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.7.4.1.2.45 FSS0_FSAS_GENREGS_ERR_ECC_TYPE Register

14.7.4.1.2.45.1 FSS0_FSAS_GENREGS_ERR_ECC_TYPE Register (Offset = 74h) [reset = 0h]

The ERR_ECC_TYPE register holds the current top of stack ECC error info, this is only valid when the ecc_err_valid is set

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Table 14-12568. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0074h + formula

Figure 14-6204. FSS0_FSAS_GENREGS_ERR_ECC_TYPE Name Register

31	30	29	28	27	26	25	24
ECC_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		ECC_ERR_ADR	ECC_ERR_MAC	ECC_ERR_DA1	ECC_ERR_DA0	ECC_ERR_DED	ECC_ERR_SEC
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-12569. FSS0_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_ERR_VALID	R/W1TC	0h	When set indicates that there is valid ECC error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:6	RESERVED	NONE	0h	Reserved
5	ECC_ERR_ADR	R	0h	When set indicates that there was a single error detected within the address field. Bits 0 and 1 in this register indicate whether it is single or double error. Reset Source: vbus_mod_g_rst_n
4	ECC_ERR_MAC	R	0h	When set indicates that there was a single error detected within the MAC field. Bits 0 and 1 in this register indicate whether it is single or double error. Reset Source: vbus_mod_g_rst_n
3	ECC_ERR_DA1	R	0h	When set indicates that there was a single error detected within the High Data word, which is bits 127 through 64 of the data word. Bits 0 and 1 in this register indicate whether it is single or double error. Reset Source: vbus_mod_g_rst_n
2	ECC_ERR_DA0	R	0h	When set indicates that there was a single error detected within the Low Data word, which is bits 63 through 0 of the data word. Bits 0 and 1 in this register indicate whether it is single or double error. Reset Source: vbus_mod_g_rst_n

Table 14-12569. FSS0_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ECC_ERR_DED	R	0h	When set indicates that there was a double error detected for the block Reset Source: vbus_mod_g_rst_n
0	ECC_ERR_SEC	R	0h	When set indicates that there was a single error detected for the block. The fields that had single error are reported by bits 2 through 5 in this register. It is possible that single error is reported in multiple fields since the ECCM inputs are partitioned into four partitions and ECC code is separate for each partition. It is also possible that none of the fields report single error even though ecc_err_sec bit is set. This can happen if single bit error occurred on the ECC code. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.46 FSS0_FSAS_GENREGS_ERR_WRT_TYPE Register

14.7.4.1.2.46.1 FSS0_FSAS_GENREGS_ERR_WRT_TYPE Register (Offset = 78h) [reset = 0h]

The ERR_WRT_TYPE register holds the current top of stack write error info. this is only valid when the wrt_err_valid is set

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Table 14-12570. Instance Table

Instance Name	Physical Address
FSS0	0FC1 0078h + formula

Figure 14-6205. FSS0_FSAS_GENREGS_ERR_WRT_TYPE Name Register

31	30	29	28	27	26	25	24
WRT_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRT_ERR_BEN	WRT_ERR_ADR	WRT_ERR_ROUTEID			
NONE		R	R	R			
0h		0h	0h	0h			
7	6	5	4	3	2	1	0
WRT_ERR_ROUTEID							
R							
0h							

Table 14-12571. FSS0_FSAS_GENREGS_ERR_WRT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRT_ERR_VALID	R/W1TC	0h	When set indicates that there is valid write error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:14	RESERVED	NONE	0h	Reserved
13	WRT_ERR_BEN	R	0h	When set indicates that there was a write error due to a non-contiguous byte enables or because write byte count was not 32-byte multiple. Please note that this bit will always be set when wrt_err_valid bit is set. There is no write error if byte count is 32-byte multiple and if byte-enables are all set. Reset Source: vbus_mod_g_rst_n
12	WRT_ERR_ADR	R	0h	When set indicates that there was a write error due to a non-aligned address. Please note that this bit can only be set if address was 16-byte multiple but not 32-byte multiple. For example, an address of 0x10 or 0x30 for writes will cause this bit to get set. Reset Source: vbus_mod_g_rst_n
11:0	WRT_ERR_ROUTEID	R	0h	Indicates the Route ID for the Initiator that caused the write error Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.47 FSAS_OTFA_REGS_REVID Register

14.7.4.1.2.47.1 FSAS_OTFA_REGS_REVID Register (Offset = 0h) [reset = 47500101h]

Revision

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Table 14-12572. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0000h

Figure 14-6206. FSAS_OTFA_REGS_REVID Name Register

31	30	29	28	27	26	25	24
REVID							
R							
47500101h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REVID							
R							
47500101h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVID							
R							
47500101h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVID							
R							
47500101h							

Table 14-12573. FSAS_OTFA_REGS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REVID	R	47500101h	REVID Reset Source: rst_modg_rst_n

14.7.4.1.2.48 FSAS_OTFA_REGS_SCFG Register

14.7.4.1.2.48.1 FSAS_OTFA_REGS_SCFG Register (Offset = 4h) [reset = 2h]

SysConfig

Return to Summary Table

Table 14-12574. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0004h

Figure 14-6207. FSAS_OTFA_REGS_SCFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						IDLE_MODE	
NONE						R/W	
0h						2h	

Table 14-12575. FSAS_OTFA_REGS_SCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	IDLE_MODE	R/W	2h	IDLE MODE Reset Source: rst_modg_rst_n

14.7.4.1.2.49 FSAS_OTFA_REGS_ISR Register

14.7.4.1.2.49.1 FSAS_OTFA_REGS_ISR Register (Offset = 8h) [reset = 0h]

IRQSTATUS_RAW

Return to Summary Table

Table 14-12576. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0008h

Figure 14-6208. FSAS_OTFA_REGS_ISR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 14-12577. FSAS_OTFA_REGS_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.7.4.1.2.50 FSAS_OTFA_REGS_IS Register

14.7.4.1.2.50.1 FSAS_OTFA_REGS_IS Register (Offset = Ch) [reset = 0h]

IRQSTATUS

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Table 14-12578. Instance Table

Instance Name	Physical Address
FSS0	0FC2 000Ch

Figure 14-6209. FSAS_OTFA_REGS_IS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAC_ERR</td><td colspan="4">WRT_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REGION_BV</td><td colspan="4">CTR_WKV</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-12579. FSAS_OTFA_REGS_IS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.7.4.1.2.51 FSAS_OTFA_REGS_IES Register

14.7.4.1.2.51.1 FSAS_OTFA_REGS_IES Register (Offset = 10h) [reset = 0h]

IRQENABLE_SET

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Table 14-12580. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0010h

Figure 14-6210. FSAS_OTFA_REGS_IES Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 14-12581. FSAS_OTFA_REGS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.7.4.1.2.52 FSAS_OTFA_REGS_IEC Register

14.7.4.1.2.52.1 FSAS_OTFA_REGS_IEC Register (Offset = 14h) [reset = 0h]

IRQENABLE_CLR

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Table 14-12582. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0014h

Figure 14-6211. FSAS_OTFA_REGS_IEC Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAC_ERR</td><td colspan="4">WRT_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REGION_BV</td><td colspan="4">CTR_WKV</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-12583. FSAS_OTFA_REGS_IEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.7.4.1.2.53 FSAS_OTFA_REGS_CCFG Register

14.7.4.1.2.53.1 FSAS_OTFA_REGS_CCFG Register (Offset = 18h) [reset = 0h]

CryptoCfg

Return to Summary Table

Table 14-12584. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0018h

Figure 14-6212. FSAS_OTFA_REGS_CCFG Name Register

31	30	29	28	27	26	25	24
MASTER_EN_RD	RESERVED						
R/W	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
FE_PROC_EN	RESERVED		MAC_LSB_ALIGN_EN	MAC_SIZE		ERROR_RESP_EN	OTFA_WAIT
R/W	NONE		R/W	R/W		R/W	R/W
0h	0h		0h	0h		0h	0h

7	6	5	4	3	2	1	0
RESERVED	CACHE_ENABLE	CACHE_EVICT_MODE	KEY_SIZE	RD_WRT_OPT			
NONE	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 14-12585. FSAS_OTFA_REGS_CCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MASTER_EN_RD	R/W	0h	This register controls the enabling the functionality of this IP Disabled and Bypass mode active Reset Source: rst_modg_rst_n
30:16	RESERVED	NONE	0h	Reserved
15	FE_PROC_EN	R/W	0h	Setting this register to 1'b1 enables performance enhancement that performs AES computations on command rather than read return. Reset Source: rst_modg_rst_n
14:13	RESERVED	NONE	0h	Reserved
12	MAC_LSB_ALIGN_EN	R/W	0h	This register is used to enable MAC to be always lsb aligned. For legacy behavior with 4-byte MAC, this register can be retained at 1'b0. However for MAC sizes 8 through 16-bytes, only 1'b1 is supported for this register. Retaining this register at 1'b0 for MAC sizes 8 through 16-bytes results in undefined behavior. Reset Source: rst_modg_rst_n
11:10	MAC_SIZE	R/W	0h	This register defines the MAC size. 2'b00: 4-bytes, 2'b01: 8-bytes, 2'b10: 12-bytes, 2'b11: 16-bytes. Reset Source: rst_modg_rst_n
9	ERROR_RESP_EN	R/W	0h	This register controls the enabling the the ocp error response for mac errors Reset Source: rst_modg_rst_n

Table 14-12585. FSAS_OTFA_REGS_CCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OTFA_WAIT	R/W	0h	This register allows the ability to stop accepting any new transactions from getting accepted and allow the current transactions to complete Reset Source: rst_modg_rst_n
7	RESERVED	NONE	0h	Reserved
6	CACHE_ENABLE	R/W	0h	MAC cache enable Reset Source: rst_modg_rst_n
5	CACHE_EVICT_MODE	R/W	0h	cache evict mode Reset Source: rst_modg_rst_n
4	KEY_SIZE	R/W	0h	Key Size, 0 128 Bit 1 256 Bit Reset Source: rst_modg_rst_n
3:0	RD_WRT_OPT	R/W	0h	This register defines the static allocation of the AES cores to read transactions. The remainder will be allocated to write transactions Reset Source: rst_modg_rst_n

14.7.4.1.2.54 FSAS_OTFA_REGS_CSTATUS Register

14.7.4.1.2.54.1 FSAS_OTFA_REGS_CSTATUS Register (Offset = 1Ch) [reset = 0h]

CryptoStatus

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Table 14-12586. Instance Table

Instance Name	Physical Address
FSS0	0FC2 001Ch

Figure 14-6213. FSAS_OTFA_REGS_CSTATUS Name Register

31	30	29	28	27	26	25	24
BUSY	CRYPTO_BUSY	RD_STALL_EVENT_CNT					
R	R	R/W1TC					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_STALL_EVENT_CNT							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRT_STALL_EVENT_CNT					
NONE		R/W1TC					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRT_STALL_EVENT_CNT							
R/W1TC							
0h							

Table 14-12587. FSAS_OTFA_REGS_CSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BUSY	R	0h	0 No transactions are active, crypto or none crypto 1 One or more transactions are active, crypto or none crypto Reset Source: rst_modg_rst_n
30	CRYPTO_BUSY	R	0h	0 No transactions are active, crypto or none crypto 1 One or more transactions are active, crypto or none crypto Reset Source: rst_modg_rst_n
29:16	RD_STALL_EVENT_CNT	R/W1TC	0h	rd stall event do to lack of eng Reset Source: rst_modg_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	WRT_STALL_EVENT_CNT	R/W1TC	0h	wrt stall event do to lack of eng Reset Source: rst_modg_rst_n

14.7.4.1.2.55 FSAS_OTFA_REGS_IRQADDINFO0 Register

14.7.4.1.2.55.1 FSAS_OTFA_REGS_IRQADDINFO0 Register (Offset = 220h) [reset = 0h]

IRQAdditionalInfo0

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Table 14-12588. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0220h

Figure 14-6214. FSAS_OTFA_REGS_IRQADDINFO0 Name Register

31	30	29	28	27	26	25	24
IRQ_MADDR							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IRQ_MADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IRQ_MADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IRQ_MADDR							
R							
0h							

Table 14-12589. FSAS_OTFA_REGS_IRQADDINFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IRQ_MADDR	R	0h	Initiator Address which caused the event Reset Source: rst_modg_rst_n

14.7.4.1.2.56 FSAS_OTFA_REGS_IRQADDINFO1 Register

14.7.4.1.2.56.1 FSAS_OTFA_REGS_IRQADDINFO1 Register (Offset = 224h) [reset = 0h]

IRQAdditionalInfo1

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Table 14-12590. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0224h

Figure 14-6215. FSAS_OTFA_REGS_IRQADDINFO1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">IRQ_MLEN</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">IRQ_MLEN</td><td colspan="3">IRQ_MSEQ</td><td colspan="3">IRQ_MCMD</td></tr>
<tr><td colspan="2">R</td><td colspan="3">R</td><td colspan="3">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IRQ_MID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12591. FSAS_OTFA_REGS_IRQADDINFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:14	IRQ_MLEN	R	0h	Initiator LENGTH which caused the event Reset Source: rst_modg_rst_n
13:11	IRQ_MSEQ	R	0h	Initiator SEQ which caused the event Reset Source: rst_modg_rst_n
10:8	IRQ_MCMD	R	0h	Initiator CMD which caused the event Reset Source: rst_modg_rst_n
7:0	IRQ_MID	R	0h	Initiator TAG ID which caused the event Reset Source: rst_modg_rst_n

14.7.4.1.2.57 FSAS_OTFA_REGS_MACCACHEINFO Register

14.7.4.1.2.57.1 FSAS_OTFA_REGS_MACCACHEINFO Register (Offset = 228h) [reset = 0h]

MACCacheInfo

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Table 14-12592. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0228h

Figure 14-6216. FSAS_OTFA_REGS_MACCACHEINFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CACHE_MISS_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
CACHE_MISS_EVENT_CNT							
R							
0h							

Table 14-12593. FSAS_OTFA_REGS_MACCACHEINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CACHE_MISS_EVENT_CNT	R	0h	MAC Cache Miss event cnt Reset Source: rst_modg_rst_n

14.7.4.1.2.58 FSAS_OTFA_REGS_RMWRMCNT Register

14.7.4.1.2.58.1 FSAS_OTFA_REGS_RMWRMCNT Register (Offset = 22Ch) [reset = 0h]

RMWRMCnt

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Table 14-12594. Instance Table

Instance Name	Physical Address
FSS0	0FC2 022Ch

Figure 14-6217. FSAS_OTFA_REGS_RMWRMCNT Name Register

31	30	29	28	27	26	25	24
RM_EVENT_CNT							
R							
0h							
23	22	21	20	19	18	17	16
RM_EVENT_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RMW_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
RMW_EVENT_CNT							
R							
0h							

Table 14-12595. FSAS_OTFA_REGS_RMWRMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RM_EVENT_CNT	R	0h	RM event cnt Reset Source: rst_modg_rst_n
15:0	RMW_EVENT_CNT	R	0h	RMW event cnt Reset Source: rst_modg_rst_n

14.7.4.1.2.59 FSAS_OTFA_REGS_RG_RGCFG_J Register

14.7.4.1.2.59.1 FSAS_OTFA_REGS_RG_RGCFG_J Register (Offset = 20h) [reset = 0h]

RegionCfg

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Table 14-12596. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0020h + formula

Figure 14-6218. FSAS_OTFA_REGS_RG_RGCFG_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>WRT_PROTECT</td><td colspan="2">MAC_MODE</td><td colspan="2">AES_MODE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12597. FSAS_OTFA_REGS_RG_RGCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.7.4.1.2.60 FSAS_OTFA_REGS_RG_RGMACST_J Register

14.7.4.1.2.60.1 FSAS_OTFA_REGS_RG_RGMACST_J Register (Offset = 24h) [reset = 0h]

RegionMacStart

Return to Summary Table

Table 14-12598. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0024h + formula

Figure 14-6219. FSAS_OTFA_REGS_RG_RGMACST_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START							
R/W							
0h							

Table 14-12599. FSAS_OTFA_REGS_RG_RGMACST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.1.2.61 FSAS_OTFA_REGS_RG_RGST_J Register

14.7.4.1.2.61.1 FSAS_OTFA_REGS_RG_RGST_J Register (Offset = 28h) [reset = 0h]

RegionStart

Return to Summary Table

Table 14-12600. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0028h + formula

Figure 14-6220. FSAS_OTFA_REGS_RG_RGST_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START							
R/W							
0h							

Table 14-12601. FSAS_OTFA_REGS_RG_RGST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.1.2.62 FSAS_OTFA_REGS_RG_RGSI_J Register

14.7.4.1.2.62.1 FSAS_OTFA_REGS_RG_RGSI_J Register (Offset = 2Ch) [reset = 0h]

RegionSize

Return to Summary Table

Table 14-12602. Instance Table

Instance Name	Physical Address
FSS0	0FC2 002Ch + formula

Figure 14-6221. FSAS_OTFA_REGS_RG_RGSI_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">R_SIZE</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_SIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_SIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12603. FSAS_OTFA_REGS_RG_RGSI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.1.2.63 FSAS_OTFA_REGS_RG_RKEYE_J_K Register

14.7.4.1.2.63.1 FSAS_OTFA_REGS_RG_RKEYE_J_K Register (Offset = 30h) [reset = 0h]

RegionKeyE

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Table 14-12604. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0030h + formula

Figure 14-6222. FSAS_OTFA_REGS_RG_RKEYE_j_k Name Register

31	30	29	28	27	26	25	24
R_KEY_E							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E							
R/W							
0h							

Table 14-12605. FSAS_OTFA_REGS_RG_RKEYE_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.1.2.64 FSAS_OTFA_REGS_RG_RKEYEP_J_K Register

14.7.4.1.2.64.1 FSAS_OTFA_REGS_RG_RKEYEP_J_K Register (Offset = 50h) [reset = 0h]

RegionKeyEP

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Table 14-12606. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0050h + formula

Figure 14-6223. FSAS_OTFA_REGS_RG_RKEYEP_j_k Name Register

31	30	29	28	27	26	25	24
R_KEY_EP							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP							
R/W							
0h							

Table 14-12607. FSAS_OTFA_REGS_RG_RKEYEP_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.1.2.65 FSAS_OTFA_REGS_RG_RKEYA_J_K Register

14.7.4.1.2.65.1 FSAS_OTFA_REGS_RG_RKEYA_J_K Register (Offset = 70h) [reset = 0h]

RegionKeyA

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Table 14-12608. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0070h + formula

Figure 14-6224. FSAS_OTFA_REGS_RG_RKEYA_j_k Name Register

31	30	29	28	27	26	25	24
R_KEY_A							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A							
R/W							
0h							

Table 14-12609. FSAS_OTFA_REGS_RG_RKEYA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.1.2.66 FSAS_OTFA_REGS_RG_RKEYAP_J_K Register

14.7.4.1.2.66.1 FSAS_OTFA_REGS_RG_RKEYAP_J_K Register (Offset = 80h) [reset = 0h]

RegionKeyAP

Return to Summary Table

Table 14-12610. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0080h + formula

Figure 14-6225. FSAS_OTFA_REGS_RG_RKEYAP_j_k Name Register

31	30	29	28	27	26	25	24
R_KEY_AP							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP							
R/W							
0h							

Table 14-12611. FSAS_OTFA_REGS_RG_RKEYAP_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.1.2.67 FSAS_OTFA_REGS_RG_RIV_J_K Register

14.7.4.1.2.67.1 FSAS_OTFA_REGS_RG_RIV_J_K Register (Offset = 90h) [reset = 0h]

RegionIV

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Table 14-12612. Instance Table

Instance Name	Physical Address
FSS0	0FC2 0090h + formula

Figure 14-6226. FSAS_OTFA_REGS_RG_RIV_j_k Name Register

31	30	29	28	27	26	25	24
R_IV							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_IV							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_IV							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_IV							
R/W							
0h							

Table 14-12613. FSAS_OTFA_REGS_RG_RIV_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.1.2.68 OSPI_FLASH_CFG_CONFIG_REG Register

14.7.4.1.2.68.1 OSPI_FLASH_CFG_CONFIG_REG Register (Offset = 0h) [reset = 80780081h]

Octal-SPI Configuration Register

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Table 14-12614. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0000h

Figure 14-6227. OSPI_FLASH_CFG_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
IDLE_FLD	DUAL_BYTE_OPCODE_EN_FLD	CRC_ENABLE_FLD	CONFIG_RESV2_FLD			PIPELINE_PHY_FLD	ENABLE_DTR_PROTOCOL_FLD
R	R/W	R/W	R			R/W	R/W
1h	0h	0h	0h			0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ENABLE_AHB_DECODER_FLD	MSTR_BAUD_DIV_FLD				ENTER_XIP_MODE_IMM_FLD	ENTER_XIP_MODE_FLD	ENB_AHB_ADDR_REMAP_FLD
R/W	R/W				R/W	R/W	R/W
0h	Fh				0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENB_DMA_IF_FLD	WR_PROT_FLASH_FLD	PERIPH_CS_LINES_FLD				PERIPH_SEL_DEC_FLD	ENB_LEGACY_IP_MODE_FLD
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ENB_DIR_ACC_CTLR_FLD	RESET_CFG_FLD	RESET_PIN_FLD	HOLD_PIN_FLD	PHY_MODE_ENABLE_FLD	SEL_CLK_PHASE_FLD	SEL_CLK_POL_FLD	ENB_SPI_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	1h

Table 14-12615. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE_FLD	R	1h	Serial interface and low level SPI pipeline is IDLE: This is a STATUS read-only bit. Note this is a retimed signal, so there will be some inherent delay on the generation of this status signal.
30	DUAL_BYTE_OPCODE_EN_FLD	R/W	0h	Dual-byte Opcode Mode enable bit This bit is to be set in case the target Flash Device supports dual byte opcode [i.e. Macronix MX25]. It is applicable for Octal I/O Mode or Protocol only so should be set back to low if the device is configured to work in another SPI Mode. If enabled, the supplementing bytes are taken from Opcode Extension Register [Lower] and from Opcode Extension Register [Upper].
29	CRC_ENABLE_FLD	R/W	0h	CRC enable bit This bit is to be set in case the target Flash Device supports CRC [Macronix MX25]. It is applicable for Octal DDR Protocol only so should be set back to low if the device is configured to work in another SPI Mode.
28:26	CONFIG_RESV2_FLD	R	0h	Reserved
25	PIPELINE_PHY_FLD	R/W	0h	Pipeline PHY Mode enable: This bit is relevant only for configuration with PHY Module. It should be asserted to 1 between consecutive PHY pipeline reads transfers and de-asserted to 0 otherwise.
24	ENABLE_DTR_PROTOCOL_FLD	R/W	0h	Enable DTR Protocol: This bit should be set if device is configured to work in DTR protocol.

Table 14-12615. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ENABLE_AHB_DECODER_FLD	R/W	0h	Enable AHB Decoder: Value=0 : Active target is selected based on Peripheral Chip Select Lines [bits [13:10]]. Value=1 Active target is selected based on actual AHB address [the partition for each device is calculated with respect to bits [28:21] of Device Size Configuration Register]
22:19	MSTR_BAUD_DIV_FLD	R/W	Fh	Initiator Mode Baud Rate Divisor: SPI baud rate = [initiator reference clock] baud_rate_divisor
18	ENTER_XIP_MODE_IMM_FLD	R/W	0h	Enter XIP Mode immediately: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : Operate the device in XIP mode immediately Use this register when the external device wakes up in XIP mode [as per the contents of its non- volatile configuration register]. The controller will assume the next READ instruction will be passed to the device as an XIP instruction, and therefore will not require the READ opcode to be transferred. Note: To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only after the next READ instruction is executed. Software therefore should ensure that at least one READ instruction is requested after resetting this bit in order to be sure that XIP mode is exited.
17	ENTER_XIP_MODE_FLD	R/W	0h	Enter XIP Mode on next READ: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : If XIP is disabled, then setting to ?1? will inform the controller that the device is ready to enter XIP on the next READ instruction. The controller will therefore send the appropriate command sequence, including mode bits to cause the device to enter XIP mode. Use this register after the controller has ensured the FLASH device has been configured to be ready to enter XIP mode. Note : To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only AFTER the next READ instruction is executed. Software should therefore ensure that at least one READ instruction is requested after resetting this bit before it can be sure XIP mode in the device is exited.
16	ENB_AHB_ADDR_REMAP_FLD	R/W	0h	Enable AHB Address Re-mapping: [Direct Access Mode Only] When set to 1, the incoming AHB address will be adapted and sent to the FLASH device as [address + N], where N is the value stored in the remap address register.
15	ENB_DMA_IF_FLD	R/W	0h	Enable DMA Peripheral Interface: Set to 1 to enable the DMA handshaking logic. When enabled the controller will trigger DMA transfer requests via the DMA peripheral interface. Set to 0 to disable
14	WR_PROT_FLASH_FLD	R/W	0h	Write Protect Flash Pin: Set to drive the Write Protect pin of the FLASH device. This is resynchronized to the generated memory clock as necessary.
13:10	PERIPH_CS_LINES_FLD	R/W	0h	Peripheral Chip Select Lines: Peripheral chip select lines If pdec = 0, ss[3:0] are output thus: ss[3:0] n_ss_out[3:0] xxx0 1110 xx01 1101 x011 1011 0111 0111 1111 1111 [no peripheral selected] else ss[3:0] directly drives n_ss_out[3:0]
9	PERIPH_SEL_DEC_FLD	R/W	0h	Peripheral select decode: 0 : only 1 of 4 selects n_ss_out[3:0] is active 1 : allow external 4-to-16 decode [n_ss_out = ss]
8	ENB_LEGACY_IP_MODE_FLD	R/W	0h	Legacy IP Mode Enable: 0 : Use Direct Access Controller/Indirect Access Controller 1 : legacy Mode is enabled. In this mode, any write to the controller via the AHB interface is serialized and sent to the FLASH device. Any valid AHB read will pop the internal RX-FIFO, retrieving data that was forwarded by the external FLASH device on the SPI lines,4,2 or 1 byte transfers are permitted and controlled via the HSIZE input.
7	ENB_DIR_ACC_CTLR_FLD	R/W	1h	Enable Direct Access Controller: 0 : disable the Direct Access Controller once current transfer of the data word [FF_W] is complete. 1 : enable the Direct Access Controller When the Direct Access Controller and Indirect Access Controller are both disabled, all AHB requested are completed with an error response.

Table 14-12615. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESET_CFG_FLD	R/W	0h	RESET pin configuration: 0 = RESET feature on DQ3 pin of the device 1 = RESET feature on dedicated pin of the device [controlling of 5th bit influences on reset_out output]
5	RESET_PIN_FLD	R/W	0h	Set to drive the RESET pin of the FLASH device and reset for de-activation of the RESET pin feature
4	HOLD_PIN_FLD	R/W	0h	Set to drive the HOLD pin of the FLASH device and reset for de-activation of the HOLD pin feature
3	PHY_MODE_ENABLE_FLD	R/W	0h	PHY mode enable: When enabled, the controller is informed that PHY Module is to be used for handling SPI transfers. This bit is relevant only for configuration with PHY Module.
2	SEL_CLK_PHASE_FLD	R/W	0h	Select Clock Phase: Selects whether the clock is in an active or inactive phase outside the SPI word. 0 : the SPI clock is active outside the word 1 : the SPI clock is inactive outside the word
1	SEL_CLK_POL_FLD	R/W	0h	Clock polarity outside SPI word: 0 : the SPI clock is quiescent low 1 : the SPI clock is quiescent high
0	ENB_SPI_FLD	R/W	1h	Octal-SPI Enable: 0 : disable the Octal-SPI, once current transfer of the data word [FF_W] is complete. 1 : enable the Octal-SPI, when spi_enable = 0, all output enables are inactive and all pins are set to input mode.

14.7.4.1.2.69 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register

14.7.4.1.2.69.1 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register (Offset = 4h) [reset = 3h]

Device Read Instruction Configuration Register

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Table 14-12616. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0004h

Figure 14-6228. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RD_INSTR_RESV5_FLD</td><td colspan="5">DUMMY_RD_CLK_CYCLES_FLD</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">RD_INSTR_RESV4_FLD</td><td>MODE_BIT_ENABLE_FLD</td><td colspan="2">RD_INSTR_RESV3_FLD</td><td colspan="2">DATA_XFER_TYPE_EXT_MODE_FLD</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RD_INSTR_RESV2_FLD</td><td colspan="2">ADDR_XFER_TYPE_STD_MODE_FLD</td><td>RD_INSTR_RESV1_FLD</td><td>DDR_EN_FLD</td><td colspan="2">INSTR_TYPE_FLD</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R/W</td><td>R</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RD_OPCODE_NON_XIP_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">3h</td></tr>
</table>

Table 14-12617. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RD_INSTR_RESV5_FLD	R	0h	Reserved
28:24	DUMMY_RD_CLK_CYCLES_FLD	R/W	0h	Dummy Read Clock Cycles: Number of dummy clock cycles required by device for read instruction.
23:21	RD_INSTR_RESV4_FLD	R	0h	Reserved
20	MODE_BIT_ENABLE_FLD	R/W	0h	Mode Bit Enable: Set this field to 1 to ensure that the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
19:18	RD_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	RD_INSTR_RESV2_FLD	R	0h	Reserved
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11	RD_INSTR_RESV1_FLD	R	0h	Reserved

Table 14-12617. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DDR_EN_FLD	R/W	0h	DDR Enable: This is to inform that opcode from rd_opcode_non_xip_fld is compliant with one of the DDR READ Commands
9:8	INSTR_TYPE_FLD	R/W	0h	Instruction Type: 0 : Use Standard SPI mode [instruction always shifted into the device on DQ0 only] 1 : Use DIO-SPI mode [Instructions, Address and Data always sent on DQ0 and DQ1] 2 : Use QIO-SPI mode [Instructions, Address and Data always sent on DQ0, DQ1, DQ2 and DQ3] 3 : Use Octal-IO-SPI mode [Instructions, Address and Data always sent on DQ[7:0]]
7:0	RD_OPCODE_NON_XIP_FLD	R/W	3h	Read Opcode in non-XIP mode: Read Opcode to use when not in XIP mode

14.7.4.1.2.70 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register

14.7.4.1.2.70.1 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register (Offset = 8h) [reset = 2h]

Device Write Instruction Configuration Register

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Table 14-12618. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0008h

Figure 14-6229. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">WR_INSTR_RESV4_FLD</td><td colspan="5">DUMMY_WR_CLK_CYCLES_FLD</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WR_INSTR_RESV3_FLD</td><td colspan="2">DATA_XFER_TYPE_EXT_MODE_FLD</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">WR_INSTR_RESV2_FLD</td><td colspan="2">ADDR_XFER_TYPE_STD_MODE_FLD</td><td colspan="3">WR_INSTR_RESV1_FLD</td><td>WEL_DIS_FLD</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WR_OPCODE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-12619. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	WR_INSTR_RESV4_FLD	R	0h	Reserved
28:24	DUMMY_WR_CLK_CYCLES_FLD	R/W	0h	Dummy Write Clock Cycles: Number of dummy clock cycles required by device for write instruction.
23:18	WR_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	WR_INSTR_RESV2_FLD	R	0h	Reserved
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11:9	WR_INSTR_RESV1_FLD	R	0h	Reserved
8	WEL_DIS_FLD	R/W	0h	WEL Disable: This is to turn off automatic issuing of WEL Command before write operation for DAC or INDAC
7:0	WR_OPCODE_FLD	R/W	2h	Write Opcode

14.7.4.1.2.71 OSPI_FLASH_CFG_DEV_DELAY_REG Register

14.7.4.1.2.71.1 OSPI_FLASH_CFG_DEV_DELAY_REG Register (Offset = Ch) [reset = 0h]

Octal-SPI Device Delay Register: This register is used to introduce relative delays into the generation of the master output signals. All timings are defined in cycles of the SPI REFERENCE CLOCK/ext_clk, defined in this table as SPI master ref clock.

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Table 14-12620. Instance Table

Instance Name	Physical Address
FSS0	0FC4 000Ch

Figure 14-6230. OSPI_FLASH_CFG_DEV_DELAY_REG Name Register

31	30	29	28	27	26	25	24
D_NSS_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
D_BTWN_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
D_AFTER_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
D_INIT_FLD							
R/W							
0h							

Table 14-12621. OSPI_FLASH_CFG_DEV_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	D_NSS_FLD	R/W	0h	Clock Delay for Chip Select Deassert: Delay in initiator reference clocks for the length that the initiator mode chip select outputs are de-asserted between transactions. The minimum delay is always SCLK period to ensure the chip select is never re-asserted within an SCLK period.
23:16	D_BTWN_FLD	R/W	0h	Clock Delay for Chip Select Deactivation: Delay in initiator reference clocks between one chip select being de-activated and the activation of another. This is used to ensure a quiet period between the selection of two different targets and requires the transmit FIFO to be empty.
15:8	D_AFTER_FLD	R/W	0h	Clock Delay for Last Transaction Bit: Delay in initiator reference clocks between last bit of current transaction and deasserting the device chip select [n_ss_out]. By default, the chip select will be deasserted on the cycle following the completion of the current transaction.
7:0	D_INIT_FLD	R/W	0h	Clock Delay with n_ss_out: Delay in initiator reference clocks between setting n_ss_out low and first bit transfer.

14.7.4.1.2.72 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register

14.7.4.1.2.72.1 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register (Offset = 10h) [reset = 1h]

Read Data Capture Register

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Table 14-12622. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0010h

Figure 14-6231. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RD_DATA_RESV3_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RD_DATA_RESV3_FLD</td><td colspan="4">DDR_READ_DELAY_FLD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RD_DATA_RESV2_FLD</td><td>DQS_ENABLE_FLD</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RD_DATA_RESV1_FLD</td><td>SAMPLE_EDGE_SEL_FLD</td><td colspan="4">DELAY_FLD</td><td>BYPASS_FLD</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>1h</td></tr>
</table>

Table 14-12623. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RD_DATA_RESV3_FLD	R	0h	Reserved
19:16	DDR_READ_DELAY_FLD	R/W	0h	DDR read delay: Delay the transmitted data by the programmed number of ref_clk cycles.This field is only relevant when DDR Read Command is executed. Otherwise can be ignored.
15:9	RD_DATA_RESV2_FLD	R	0h	Reserved
8	DQS_ENABLE_FLD	R/W	0h	DQS enable bit: If enabled, signal from DQS input is driven into RX DLL and is used for data capturing in PHY Mode rather than internally generated gated ref_clk..
7:6	RD_DATA_RESV1_FLD	R	0h	Reserved
5	SAMPLE_EDGE_SEL_FLD	R/W	0h	Sample edge selection: Choose edge on which data outputs from flash memory will be sampled
4:1	DELAY_FLD	R/W	0h	Read Delay: Delay the read data capturing logic by the programmed number of ref_clk cycles
0	BYPASS_FLD	R/W	1h	Bypass the adapted loopback clock circuit

14.7.4.1.2.73 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register

14.7.4.1.2.73.1 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register (Offset = 14h) [reset = 101002h]

Device Size Configuration Register

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Table 14-12624. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0014h

Figure 14-6232. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DEV_SIZE_RESV_FLD			MEM_SIZE_ON_CS3_FLD		MEM_SIZE_ON_CS2_FLD		MEM_SIZE_ON_CS1_FLD
R			R/W		R/W		R/W
0h			0h		0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MEM_SIZE_ON_CS1_FLD	MEM_SIZE_ON_CS0_FLD		BYTES_PER_SUBSECTOR_FLD				
R/W	R/W		R/W				
0h	0h		10h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BYTES_PER_DEVICE_PAGE_FLD							
R/W							
100h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BYTES_PER_DEVICE_PAGE_FLD				NUM_ADDR_BYTES_FLD			
R/W				R/W			
100h				2h			

Table 14-12625. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	DEV_SIZE_RESV_FLD	R	0h	Reserved
28:27	MEM_SIZE_ON_CS3_FLD	R/W	0h	Size of Flash Device connected to CS[3] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
26:25	MEM_SIZE_ON_CS2_FLD	R/W	0h	Size of Flash Device connected to CS[2] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
24:23	MEM_SIZE_ON_CS1_FLD	R/W	0h	Size of Flash Device connected to CS[1] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
22:21	MEM_SIZE_ON_CS0_FLD	R/W	0h	Size of Flash Device connected to CS[0] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
20:16	BYTES_PER_SUBSECTOR_FLD	R/W	10h	Number of bytes per Block. This is required by the controller for performing the write protection logic. The number of bytes per block must be a power of 2 number.
15:4	BYTES_PER_DEVICE_PAGE_FLD	R/W	100h	Number of bytes per device page. This is required by the controller for performing FLASH writes up to and across page boundaries.
3:0	NUM_ADDR_BYTES_FLD	R/W	2h	Number of address bytes. A value of 0 indicates 1 byte.

14.7.4.1.2.74 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register

14.7.4.1.2.74.1 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register (Offset = 18h) [reset = 80h]

SRAM Partition Configuration Register

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Table 14-12626. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0018h

Figure 14-6233. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Name Register

31	30	29	28	27	26	25	24
SRAM_PARTITION_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_PARTITION_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_PARTITION_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
80h							

Table 14-12627. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	SRAM_PARTITION_RESV_FLD	R	0h	Reserved
7:0	ADDR_FLD	R/W	80h	Indirect Read Partition Size: Defines the size of the indirect read partition in the SRAM, in units of SRAM locations. By default, half of the SRAM is reserved for indirect read operation, and half for indirect write. The size of this register will scale with the depth of the SRAM.

14.7.4.1.2.75 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register

14.7.4.1.2.75.1 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register (Offset = 1Ch) [reset = 0h]

Indirect AHB Address Trigger Register

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Table 14-12628. Instance Table

Instance Name	Physical Address
FSS0	0FC4 001Ch

Figure 14-6234. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-12629. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the base address that will be used by the AHB controller. When the incoming AHB read access address matches a range of addresses from this trigger address to the trigger address + 15, then the AHB request will be completed by fetching data from the Indirect Controllers SRAM.

14.7.4.1.2.76 OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register

14.7.4.1.2.76.1 OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register (Offset = 20h) [reset = 0h]

DMA Peripheral Configuration Register

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Table 14-12630. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0020h

Figure 14-6235. OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DMA_PERIPH_RESV2_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DMA_PERIPH_RESV2_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DMA_PERIPH_RESV2_FLD				NUM_BURST_REQ_BYTES_FLD			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DMA_PERIPH_RESV1_FLD				NUM_SINGLE_REQ_BYTES_FLD			
R				R/W			
0h				0h			

Table 14-12631. OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	DMA_PERIPH_RESV2_FLD	R	0h	Reserved
11:8	NUM_BURST_REQ_BYTES_FLD	R/W	0h	Number of Burst Bytes: Number of bytes in a burst type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.
7:4	DMA_PERIPH_RESV1_FLD	R	0h	Reserved
3:0	NUM_SINGLE_REQ_BYTES_FLD	R/W	0h	Number of Single Bytes: Number of bytes in a single type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.

14.7.4.1.2.77 OSPI_FLASH_CFG_REMAP_ADDR_REG Register

14.7.4.1.2.77.1 OSPI_FLASH_CFG_REMAP_ADDR_REG Register (Offset = 24h) [reset = 0h]

Remap Address Register

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Table 14-12632. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0024h

Figure 14-6236. OSPI_FLASH_CFG_REMAP_ADDR_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VALUE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VALUE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VALUE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VALUE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12633. OSPI_FLASH_CFG_REMAP_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This register is used to remap an incoming AHB address to a different address used by the FLASH device.

14.7.4.1.2.78 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register

14.7.4.1.2.78.1 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register (Offset = 28h) [reset = 200h]

Mode Bit Configuration Register

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Table 14-12634. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0028h

Figure 14-6237. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RX_CRC_DATA_LOW_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CRC_DATA_UP_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_OUT_ENABLE_FLD	MODE_BIT_RESV1_FLD				CHUNK_SIZE_FLD		
R/W	R				R/W		
0h	0h				2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MODE_FLD							
R/W							
0h							

Table 14-12635. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RX_CRC_DATA_LOW_FLD	R	0h	RX CRC data [lower] The first CRC byte returned after RX data chunk.
23:16	RX_CRC_DATA_UP_FLD	R	0h	RX CRC data [upper] The second CRC byte returned after RX data chunk.
15	CRC_OUT_ENABLE_FLD	R/W	0h	CRC# output enable bit When enabled, the controller expects the Flash Device to toggle CRC data on both SPI clock edges in CRC->CRC# sequence and calculates CRC compliance accordingly.
14:11	MODE_BIT_RESV1_FLD	R	0h	Reserved
10:8	CHUNK_SIZE_FLD	R/W	2h	It defines size of chunk after which CRC data is expected to show up on the SPI interface for write and read data transfers.
7:0	MODE_FLD	R/W	0h	These are the 8 mode bits that are sent to the device following the address bytes if mode bit transmission has been enabled.

14.7.4.1.2.79 OSPI_FLASH_CFG_SRAM_FILL_REG Register

14.7.4.1.2.79.1 OSPI_FLASH_CFG_SRAM_FILL_REG Register (Offset = 2Ch) [reset = 0h]

SRAM Fill Register

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Table 14-12636. Instance Table

Instance Name	Physical Address
FSS0	0FC4 002Ch

Figure 14-6238. OSPI_FLASH_CFG_SRAM_FILL_REG Name Register

31	30	29	28	27	26	25	24
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_FILL_INDAC_READ_FLD							
R							
0h							
7	6	5	4	3	2	1	0
SRAM_FILL_INDAC_READ_FLD							
R							
0h							

Table 14-12637. OSPI_FLASH_CFG_SRAM_FILL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SRAM_FILL_INDAC_WRITE_FLD	R	0h	SRAM Fill Level [Indirect Write Partition]: Identifies the current fill level of the SRAM Indirect Write partition
15:0	SRAM_FILL_INDAC_READ_FLD	R	0h	SRAM Fill Level [Indirect Read Partition]: Identifies the current fill level of the SRAM Indirect Read partition

14.7.4.1.2.80 OSPI_FLASH_CFG_TX_THRESH_REG Register

14.7.4.1.2.80.1 OSPI_FLASH_CFG_TX_THRESH_REG Register (Offset = 30h) [reset = 1h]

TX Threshold Register

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Table 14-12638. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0030h

Figure 14-6239. OSPI_FLASH_CFG_TX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
TX_THRESH_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
TX_THRESH_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
TX_THRESH_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
TX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 14-12639. OSPI_FLASH_CFG_TX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	TX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small TX FIFO not full interrupt is generated

14.7.4.1.2.81 OSPI_FLASH_CFG_RX_THRESH_REG Register

14.7.4.1.2.81.1 OSPI_FLASH_CFG_RX_THRESH_REG Register (Offset = 34h) [reset = 1h]

RX Threshold Register

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Table 14-12640. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0034h

Figure 14-6240. OSPI_FLASH_CFG_RX_THRESH_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RX_THRESH_RESV_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_THRESH_RESV_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RX_THRESH_RESV_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RX_THRESH_RESV_FLD</td><td colspan="5">LEVEL_FLD</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">1h</td></tr>
</table>

Table 14-12641. OSPI_FLASH_CFG_RX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small RX FIFO not empty interrupt is generated

14.7.4.1.2.82 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register

14.7.4.1.2.82.1 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register (Offset = 38h) [reset = 10005h]

Write Completion Control Register: This register defines how the controller will poll the device following a write transfer

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Table 14-12642. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0038h

Figure 14-6241. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Name Register

31	30	29	28	27	26	25	24
POLL_REP_DELAY_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
POLL_COUNT_FLD							
R/W							
1h							
15	14	13	12	11	10	9	8
ENABLE_POLLING_EXP_FLD	DISABLE_POLLING_FLD	POLLING_POLARITY_FLD	WR_COMP_CTRL_RESV1_FLD		POLLING_BIT_INDEX_FLD		
R/W	R/W	R/W	R		R/W		
0h	0h	0h	0h		0h		
7	6	5	4	3	2	1	0
OPCODE_FLD							
R/W							
5h							

Table 14-12643. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	POLL_REP_DELAY_FLD	R/W	0h	Defines additional delay for maintain Chip Select de-asserted during auto-polling phase
23:16	POLL_COUNT_FLD	R/W	1h	Defines the number of times the controller should expect to see a true result from the polling in successive reads of the device register.
15	ENABLE_POLLING_EXP_FLD	R/W	0h	Set to '1' for enabling auto-polling expiration.
14	DISABLE_POLLING_FLD	R/W	0h	This switches off the automatic polling function
13	POLLING_POLARITY_FLD	R/W	0h	Defines the polling polarity. If '1', then the write transfer to the device will be complete if the polled bit is equal to '1'. If '0', then the write transfer to the device will be complete if the polled bit is equal to '0'.
12:11	WR_COMP_CTRL_RESV1_FLD	R	0h	Reserved
10:8	POLLING_BIT_INDEX_FLD	R/W	0h	Defines the bit index that should be polled. A value of 010 means that bit 2 of the returned data will be polled for.A value of 111 means that bit 7 of the returned data will be polled for.
7:0	OPCODE_FLD	R/W	5h	Defines the opcode that should be issued by the controller when it is automatically polling for device program completion. This command is issued followed all device write operations. By default, this will poll the standard device STATUS register using opcode 0x05

14.7.4.1.2.83 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register

14.7.4.1.2.83.1 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register (Offset = 3Ch) [reset = FFFFFFFFh]

Polling Expiration Register

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Table 14-12644. Instance Table

Instance Name	Physical Address
FSS0	0FC4 003Ch

Figure 14-6242. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Name Register

31	30	29	28	27	26	25	24
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							

Table 14-12645. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NO_OF_POLLS_BEF_EXP_FLD	R/W	FFFFFFFFh	Number of polls cycles before expiration

14.7.4.1.2.84 OSPI_FLASH_CFG_IRQ_STATUS_REG Register

14.7.4.1.2.84.1 OSPI_FLASH_CFG_IRQ_STATUS_REG Register (Offset = 40h) [reset = 0h]

Interrupt Status Register: The status fields in this register are set when the described event occurs and the interrupt is enabled in the mask register. When any of these bit fields are set, the interrupt output is asserted high. The fields are each cleared by writing a 1 to the field. Note that bit fields 6 thru 10 are only valid when legacy SPI mode is active.

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Table 14-12646. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0040h

Figure 14-6243. OSPI_FLASH_CFG_IRQ_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IRQ_STAT_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_STAT_RESV_FLD				ECC_FAIL_FLD	TX_CRC_CHUNK_BRK_FLD	RX_CRC_DATA_VAL_FLD	RX_CRC_DATA_ERR_FLD
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_STAT_RESV1_FLD	STIG_REQ_INT_FLD	POLL_EXP_INT_FLD	INDRD_SRAM_FULL_FLD	RX_FIFO_FULL_FLD	RX_FIFO_NOT_EMPTY_FLD	TX_FIFO_FULL_FLD	TX_FIFO_NOT_FULL_FLD
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_FLD	INDIRECT_XFER_LEVEL_BREACH_FLD	ILLEGAL_ACCESS_DET_FLD	PROT_WR_ATTEMPT_FLD	INDIRECT_READ_REJECT_FLD	INDIRECT_OP_DONE_FLD	UNDERFLOW_DET_FLD	MODE_M_FAIL_FLD
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12647. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_STAT_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_FLD	R/W1TC	0h	ECC failure This interrupt informs the system that Flash Device reported ECC error.
18	TX_CRC_CHUNK_BRK_FLD	R/W1TC	0h	TX CRC chunk was broken This interrupt informs the system that program page SPI transfer was discontinued somewhere inside the chunk.
17	RX_CRC_DATA_VAL_FLD	R/W1TC	0h	RX CRC data valid New RX CRC data was captured from Flash Device
16	RX_CRC_DATA_ERR_FLD	R/W1TC	0h	RX CRC data error CRC data from Flash Device does not correspond to the one dynamically calculated by the controller.
15	IRQ_STAT_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_INT_FLD	R/W1TC	0h	The controller is ready for getting another STIG request.
13	POLL_EXP_INT_FLD	R/W1TC	0h	The maximum number of programmed polls cycles is expired
12	INDRD_SRAM_FULL_FLD	R/W1TC	0h	Indirect Read Partition overflow: Indirect Read Partition of SRAM is full and unable to immediately complete indirect operation

Table 14-12647. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_FIFO_FULL_FLD	R/W1TC	0h	Small RX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full 1 : FIFO is full
10	RX_FIFO_NOT_EMPTY_FLD	R/W1TC	0h	Small RX FIFO not empty: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has less than RX THRESHOLD entries, 1 : FIFO has >= THRESHOLD entries
9	TX_FIFO_FULL_FLD	R/W1TC	0h	Small TX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full, 1 : FIFO is full
8	TX_FIFO_NOT_FULL_FLD	R/W1TC	0h	Small TX FIFO not full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has >= THRESHOLD entries, 1 : FIFO has less than THRESHOLD entries
7	RECV_OVERFLOW_FLD	R/W1TC	0h	Receive Overflow: This should only occur in Legacy SPI mode. Set if an attempt is made to push the RX FIFO when it is full. This bit is reset only by a system reset and cleared only when this register is read. If a new push to the RX FIFO occurs coincident with a register read this flag will remain set. 0 : no overflow has been detected. 1 : an overflow has occurred.
6	INDIRECT_XFER_LEVEL_BREACH_FLD	R/W1TC	0h	Indirect Transfer Watermark Level Breached
5	ILLEGAL_ACCESS_DET_FLD	R/W1TC	0h	Illegal AHB access has been detected. AHB wrapping bursts and the use of SPLIT/RETRY accesses will cause this error interrupt to trigger.
4	PROT_WR_ATTEMPT_FLD	R/W1TC	0h	Write to protected area was attempted and rejected.
3	INDIRECT_READ_REJECT_FLD	R/W1TC	0h	Indirect operation was requested but could not be accepted. Two indirect operations already in storage.
2	INDIRECT_OP_DONE_FLD	R/W1TC	0h	Indirect Operation Complete: Controller has completed last triggered indirect operation
1	UNDERFLOW_DET_FLD	R/W1TC	0h	Underflow Detected: 0 : no underflow has been detected 1 : underflow is detected and an attempt to transfer data is made when the small TX FIFO is empty. This may occur when AHB write data is being supplied too slowly to keep up with the requested write operation This bit is reset only by a system reset and cleared only when the register is read.
0	MODE_M_FAIL_FLD	R/W1TC	0h	Mode M Failure: Mode M failure indicates the voltage on pin n_ss_in is inconsistent with the SPI mode. Set =1 if n_ss_in is low in initiator mode [multi-initiator contention]. These conditions will clear the spi_enable bit and disable the SPI. This bit is reset only by a system reset and cleared only when this register is read. 0 : no mode fault has been detected 1 : a mode fault has occurred

14.7.4.1.2.85 OSPI_FLASH_CFG_IRQ_MASK_REG Register

14.7.4.1.2.85.1 OSPI_FLASH_CFG_IRQ_MASK_REG Register (Offset = 44h) [reset = 0h]

Interrupt Mask: 0 : the interrupt for the corresponding interrupt status register bit is disabled. 1 : the interrupt for the corresponding interrupt status register bit is enabled.

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Table 14-12648. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0044h

Figure 14-6244. OSPI_FLASH_CFG_IRQ_MASK_REG Name Register

31	30	29	28	27	26	25	24
IRQ_MASK_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_MASK_RESV_FLD				ECC_FAIL_MASK_FLD	TX_CRC_CHUNK_BRK_MASK_FLD	RX_CRC_DATA_VAL_MASK_FLD	RX_CRC_DATA_ERR_MASK_FLD
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_MASK_RESV1_FLD	STIG_REQ_MASK_FLD	POLL_EXP_INT_MASK_FLD	INDRD_SRAM_FULL_MASK_FLD	RX_FIFO_FULL_MASK_FLD	RX_FIFO_NOT_EMPTY_MASK_FLD	TX_FIFO_FULL_MASK_FLD	TX_FIFO_NOT_FULL_MASK_FLD
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_MASK_FLD	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	ILLEGAL_ACCESS_DET_MASK_FLD	PROT_WR_ATTEMPT_MASK_FLD	INDIRECT_READ_REJECT_MASK_FLD	INDIRECT_OP_DONE_MASK_FLD	UNDERFLOW_DET_MASK_FLD	MODE_M_FAIL_MASK_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12649. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_MASK_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_MASK_FLD	R/W	0h	ECC failure Mask
18	TX_CRC_CHUNK_BRK_MASK_FLD	R/W	0h	TX CRC chunk was broken Mask
17	RX_CRC_DATA_VAL_MASK_FLD	R/W	0h	RX CRC data valid Mask
16	RX_CRC_DATA_ERR_MASK_FLD	R/W	0h	RX CRC data error Mask
15	IRQ_MASK_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_MASK_FLD	R/W	0h	STIG request completion Mask
13	POLL_EXP_INT_MASK_FLD	R/W	0h	Polling expiration detected Mask
12	INDRD_SRAM_FULL_MASK_FLD	R/W	0h	Indirect Read Partition overflow mask
11	RX_FIFO_FULL_MASK_FLD	R/W	0h	Small RX FIFO full Mask

Table 14-12649. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_FIFO_NOT_EMPTY_MASK_FLD	R/W	0h	Small RX FIFO not empty Mask
9	TX_FIFO_FULL_MASK_FLD	R/W	0h	Small TX FIFO full Mask
8	TX_FIFO_NOT_FULL_MASK_FLD	R/W	0h	Small TX FIFO not full Mask
7	RECV_OVERFLOW_MASK_FLD	R/W	0h	Receive Overflow Mask
6	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	R/W	0h	Transfer Watermark Breach Mask
5	ILLEGAL_ACCESS_DET_MASK_FLD	R/W	0h	Illegal Access Detected Mask
4	PROT_WR_ATTEMPT_MASK_FLD	R/W	0h	Protected Area Write Attempt Mask
3	INDIRECT_READ_REJECT_MASK_FLD	R/W	0h	Indirect Read Reject Mask
2	INDIRECT_OP_DONE_MASK_FLD	R/W	0h	Indirect Complete Mask
1	UNDERFLOW_DET_MASK_FLD	R/W	0h	Underflow Detected Mask
0	MODE_M_FAIL_MASK_FLD	R/W	0h	Mode M Failure Mask

14.7.4.1.2.86 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register

14.7.4.1.2.86.1 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register (Offset = 50h) [reset = 0h]

Lower Write Protection Register

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Table 14-12650. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0050h

Figure 14-6245. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 14-12651. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the lower block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

14.7.4.1.2.87 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register

14.7.4.1.2.87.1 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register (Offset = 54h) [reset = 0h]

Upper Write Protection Register

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Table 14-12652. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0054h

Figure 14-6246. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 14-12653. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the upper block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

14.7.4.1.2.88 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register

14.7.4.1.2.88.1 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register (Offset = 58h) [reset = 0h]

Write Protection Control Register

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Table 14-12654. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0058h

Figure 14-6247. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Name Register

31	30	29	28	27	26	25	24
WR_PROT_CTRL_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
WR_PROT_CTRL_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
WR_PROT_CTRL_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
WR_PROT_CTRL_RESV_FLD						ENB_FLD	INV_FLD
R						R/W	R/W
0h						0h	0h

Table 14-12655. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	WR_PROT_CTRL_RESV_FLD	R	0h	Reserved
1	ENB_FLD	R/W	0h	Write Protection Enable Bit: When set to 1, any AHB write access with an address within the protection region defined in the lower and upper write protection registers is rejected. An AHB error response is generated and an interrupt source triggered. When set to 0, the protection region is disabled.
0	INV_FLD	R/W	0h	Write Protection Inversion Bit: When set to 1, the protection region defined in the lower and upper write protection registers is inverted meaning it is the region that the system is permitted to write to. When set to 0, the protection region defined in the lower and upper write protection registers is the region that the system is not permitted to write to.

14.7.4.1.2.89 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register

14.7.4.1.2.89.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register (Offset = 60h) [reset = 0h]

Indirect Read Transfer Control Register

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Table 14-12656. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0060h

Figure 14-6248. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_RD_XFER_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
INDIR_RD_XFER_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
INDIR_RD_XFER_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	RD_QUEUED_FLD	SRAM_FULL_FLD	RD_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R/W1TC	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 14-12657. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_RD_XFER_RESV_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	RD_QUEUED_FLD	R	0h	Two indirect read operations have been queued
3	SRAM_FULL_FLD	R/W1TC	0h	SRAM Full: SRAM full and unable to immediately complete an indirect operation. Write a 1 to this field to clear it.; indirect operation [status]
2	RD_STATUS_FLD	R	0h	Indirect Read Status: Indirect read operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Read: Writing a 1 to this bit will cancel all ongoing indirect read operations.
0	START_FLD	W	0h	Start Indirect Read: Writing a 1 to this bit will trigger an indirect read operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect read operation.

14.7.4.1.2.90 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register

14.7.4.1.2.90.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register (Offset = 64h) [reset = 0h]

Indirect Read Transfer Watermark Register

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Table 14-12658. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0064h

Figure 14-6249. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
0h							

Table 14-12659. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	0h	Watermark Value: This represents the minimum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level passes the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all zeroes.

14.7.4.1.2.91 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register

14.7.4.1.2.91.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register (Offset = 68h) [reset = 0h]

Indirect Read Transfer Start Address Register

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Table 14-12660. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0068h

Figure 14-6250. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-12661. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the start address from which the indirect access will commence its READ operation.

14.7.4.1.2.92 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register

14.7.4.1.2.92.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register (Offset = 6Ch) [reset = 0h]

Indirect Read Transfer Number Bytes Register

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Table 14-12662. Instance Table

Instance Name	Physical Address
FSS0	0FC4 006Ch

Figure 14-6251. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-12663. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.7.4.1.2.93 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register

14.7.4.1.2.93.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register (Offset = 70h) [reset = 0h]

Indirect Write Transfer Control Register

Return to Summary Table

Table 14-12664. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0070h

Figure 14-6252. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
23	22	21	20	19	18	17	16
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
15	14	13	12	11	10	9	8
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
7	6	5	4	3	2	1	0
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	WR_QUEUED_FLD	INDIR_WR_XFER_RESV1_FLD	WR_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 14-12665. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_WR_XFER_RESV2_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	WR_QUEUED_FLD	R	0h	Two indirect write operations have been queued
3	INDIR_WR_XFER_RESV1_FLD	R	0h	Reserved
2	WR_STATUS_FLD	R	0h	Indirect Write Status: Indirect write operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Write: Writing a 1 to this bit will cancel all ongoing indirect write operations.
0	START_FLD	W	0h	Start Indirect Write: Writing a 1 to this bit will trigger an indirect write operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect write operation.

14.7.4.1.2.94 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register

14.7.4.1.2.94.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register (Offset = 74h) [reset = FFFFFFFFh]

Indirect Write Transfer Watermark Register

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Table 14-12666. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0074h

Figure 14-6253. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
FFFFFFFFh							

Table 14-12667. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	FFFFFFFFh	Watermark Value: This represents the maximum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level falls below the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all ones.

14.7.4.1.2.95 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register

14.7.4.1.2.95.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register (Offset = 78h) [reset = 0h]

Indirect Write Transfer Start Address Register

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Table 14-12668. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0078h

Figure 14-6254. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-12669. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Start of Indirect Access: This is the start address from which the indirect access will commence its READ operation.

14.7.4.1.2.96 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register

14.7.4.1.2.96.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register (Offset = 7Ch) [reset = 0h]

Indirect Write Transfer Number Bytes Register

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Table 14-12670. Instance Table

Instance Name	Physical Address
FSS0	0FC4 007Ch

Figure 14-6255. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-12671. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	Indirect Number of Bytes: This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.7.4.1.2.97 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register

14.7.4.1.2.97.1 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register (Offset = 80h) [reset = 4h]

Indirect Trigger Address Range Register

Return to Summary Table

Table 14-12672. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0080h

Figure 14-6256. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IND_RANGE_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IND_RANGE_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IND_RANGE_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IND_RANGE_RESV1_FLD</td><td colspan="4">IND_RANGE_WIDTH_FLD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-12673. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IND_RANGE_RESV1_FLD	R	0h	Reserved
3:0	IND_RANGE_WIDTH_FLD	R/W	4h	This is the address offset of Indirect Trigger Address Register.

14.7.4.1.2.98 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register

14.7.4.1.2.98.1 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register (Offset = 8Ch) [reset = 0h]

Flash Command Control Memory Register

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Table 14-12674. Instance Table

Instance Name	Physical Address
FSS0	0FC4 008Ch

Figure 14-6257. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Name Register

31	30	29	28	27	26	25	24
FLASH_COMMAND_CTRL_MEM_RESV1_FLD			MEM_BANK_ADDR_FLD				
R			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MEM_BANK_ADDR_FLD				FLASH_COMMAND_CTRL_MEM_RESV2_FLD	NB_OF_STIG_READ_BYTES_FLD		
R/W				R	R/W		
0h				0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MEM_BANK_READ_DATA_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FLASH_COMMAND_CTRL_MEM_RESV3_FLD						MEM_BANK_REQ_IN_PROGRESS_FLD	TRIGGER_MEM_BANK_REQ_FLD
R						R	W
0h						0h	0h

Table 14-12675. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	FLASH_COMMAND_CTRL_MEM_RESV1_FLD	R	0h	Reserved
28:20	MEM_BANK_ADDR_FLD	R/W	0h	The address of the Memory Bank which data will be read from.
19	FLASH_COMMAND_CTRL_MEM_RESV2_FLD	R	0h	Reserved
18:16	NB_OF_STIG_READ_BYTES_FLD	R/W	0h	It defines the number of read bytes for the extended STIG.
15:8	MEM_BANK_READ_DATA_FLD	R	0h	Last requested data from the STIG Memory Bank.
7:2	FLASH_COMMAND_CTRL_MEM_RESV3_FLD	R	0h	Reserved
1	MEM_BANK_REQ_IN_PROGRESS_FLD	R	0h	Memory Bank data request in progress.
0	TRIGGER_MEM_BANK_REQ_FLD	W	0h	Trigger the Memory Bank data request.

14.7.4.1.2.99 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register

14.7.4.1.2.99.1 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register (Offset = 90h) [reset = 0h]

Flash Command Control Register

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Table 14-12676. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0090h

Figure 14-6258. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Name Register

31	30	29	28	27	26	25	24
CMD_OPCODE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ENB_READ_DATA_FLD	NUM_RD_DATA_BYTES_FLD			ENB_COMD_ADDR_FLD	ENB_MODE_BIT_FLD	NUM_ADDR_BYTES_FLD	
R/W	R/W			R/W	R/W	R/W	
0h	0h			0h	0h	0h	
15	14	13	12	11	10	9	8
ENB_WRITE_DATA_FLD	NUM_WR_DATA_BYTES_FLD			NUM_DUMMY_CYCLES_FLD			
R/W	R/W			R/W			
0h	0h			0h			
7	6	5	4	3	2	1	0
NUM_DUMMY_CYCLES_FLD	FLASH_CMD_CTRL_RESV1_FLD				STIG_MEM_BANK_EN_FLD	CMD_EXEC_STATUS_FLD	CMD_EXEC_FLD
R/W	R				R/W	R	W
0h	0h				0h	0h	0h

Table 14-12677. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CMD_OPCODE_FLD	R/W	0h	Command Opcode: The command opcode field should be setup before triggering the command. For example, 0x20 maps to SubSector Erase. Writing to the execute field [bit 0] of this register launches the command. NOTE : Using this approach to issue commands to the device will make use of the instruction type of the device instruction configuration register. If this field is set to 2'b00, then the command opcode, command address, command dummy bytes and command data will all be transferred in a serial fashion. If this field is set to 2'b01, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0 and DQ1 pins. If this field is set to 2'b10, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0, DQ1, DQ2 and DQ3 pins.
23	ENB_READ_DATA_FLD	R/W	0h	Read Data Enable: Set to 1 if the command specified in the command opcode field [bits 31:24] requires read data bytes to be received from the device.
22:20	NUM_RD_DATA_BYTES_FLD	R/W	0h	Number of Read Data Bytes: Up to 8 data bytes may be read using this command. Set to 0 for 1 byte and 7 for 8 bytes.
19	ENB_COMD_ADDR_FLD	R/W	0h	Command Address Enable: Set to 1 if the command specified in bits 31:24 requires an address. This should be setup before triggering the command via Writing a 1 to the execute field.

Table 14-12677. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	ENB_MODE_BIT_FLD	R/W	0h	Mode Bit Enable: Set to 1 to ensure the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
17:16	NUM_ADDR_BYTES_FLD	R/W	0h	Number of Address Bytes: Set to the number of address bytes required [the address itself is programmed in the FLASH COMMAND ADDRESS REGISTERS]. This should be setup before triggering the command via bit 0 of this register. 2'b00 : 1 address byte 2'b01 : 2 address bytes 2'b10 : 3 address bytes 2'b11 : 4 address bytes
15	ENB_WRITE_DATA_FLD	R/W	0h	Write Data Enable: Set to 1 if the command specified in the command opcode field requires write data bytes to be sent to the device.
14:12	NUM_WR_DATA_BYTES_FLD	R/W	0h	Number of Write Data Bytes: Up to 8 Data bytes may be written using this command Set to 0 for 1 byte, 7 for 8 bytes.
11:7	NUM_DUMMY_CYCLES_FLD	R/W	0h	Number of Dummy cycles: Set to the number of dummy cycles required. This should be setup before triggering the command via the execute field of this register.
6:3	FLASH_CMD_CTRL_RESV1_FLD	R	0h	Reserved
2	STIG_MEM_BANK_EN_FLD	R/W	0h	STIG Memory Bank enable bit.
1	CMD_EXEC_STATUS_FLD	R	0h	Command execution in progress.
0	CMD_EXEC_FLD	W	0h	Execute the command.

14.7.4.1.2.100 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register

14.7.4.1.2.100.1 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register (Offset = 94h) [reset = 0h]

Flash Command Address Register

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Table 14-12678. Instance Table

Instance Name	Physical Address
FSS0	0FC4 0094h

Figure 14-6259. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-12679. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Command Address: This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the address used by the command specified in the opcode field [bits 31:24] of the Flash Command Control register.

14.7.4.1.2.101 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register

14.7.4.1.2.101.1 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register (Offset = A0h) [reset = 0h]

Flash Command Read Data Register (Lower)

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Table 14-12680. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00A0h

Figure 14-6260. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12681. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the flash device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.7.4.1.2.102 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register

14.7.4.1.2.102.1 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register (Offset = A4h) [reset = 0h]

Flash Command Read Data Register (Upper)

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Table 14-12682. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00A4h

Figure 14-6261. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R							
0h							

Table 14-12683. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the FLASH device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.7.4.1.2.103 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register

14.7.4.1.2.103.1 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register (Offset = A8h) [reset = 0h]

Flash Command Write Data Register (Lower)

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Table 14-12684. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00A8h

Figure 14-6262. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 14-12685. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Lower Byte: This is the command write data lower byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

14.7.4.1.2.104 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register

14.7.4.1.2.104.1 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register (Offset = ACh) [reset = 0h]

Flash Command Write Data Register (Upper)

Return to Summary Table

Table 14-12686. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00ACh

Figure 14-6263. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 14-12687. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Upper Byte: This is the command write data upper byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

14.7.4.1.2.105 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register

14.7.4.1.2.105.1 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register (Offset = B0h) [reset = 0h]

Polling Flash Status Register

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Table 14-12688. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00B0h

Figure 14-6264. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Name Register

31	30	29	28	27	26	25	24
DEVICE_STATUS_RSVD_FLD2							
R							
0h							
23	22	21	20	19	18	17	16
DEVICE_STATUS_RSVD_FLD2				DEVICE_STATUS_NB_DUMMY			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
DEVICE_STATUS_RSVD_FLD1							DEVICE_STATUS_VALID_FLD
R							R
0h							0h
7	6	5	4	3	2	1	0
DEVICE_STATUS_FLD							
R							
0h							

Table 14-12689. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	DEVICE_STATUS_RSVD_FLD2	R	0h	Reserved
19:16	DEVICE_STATUS_NB_DUMMY	R/W	0h	Number of dummy cycles for auto-polling
15:9	DEVICE_STATUS_RSVD_FLD1	R	0h	Reserved
8	DEVICE_STATUS_VALID_FLD	R	0h	Device Status Valid: This should be set when value in bits from 7 to 0 is valid.
7:0	DEVICE_STATUS_FLD	R	0h	Defines actual Status Register of Device

14.7.4.1.2.106 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register

14.7.4.1.2.106.1 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register (Offset = B4h) [reset = 40000000h]

PHY Configuration Register

Return to Summary Table

Table 14-12690. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00B4h

Figure 14-6265. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PHY_CONFIG_RESYNC_FLD</td><td>PHY_CONFIG_RESET_FLD</td><td>PHY_CONFIG_RX_DLL_BYPASS_FLD</td><td colspan="5">PHY_CONFIG_RESV2_FLD</td></tr>
<tr><td>W</td><td>W</td><td>R/W</td><td colspan="5">R</td></tr>
<tr><td>0h</td><td>1h</td><td>0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PHY_CONFIG_RESV2_FLD</td><td colspan="7">PHY_CONFIG_TX_DLL_DELAY_FLD</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_CONFIG_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PHY_CONFIG_RESV1_FLD</td><td colspan="7">PHY_CONFIG_RX_DLL_DELAY_FLD</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-12691. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_CONFIG_RESYNC_FLD	W	0h	This bit is used for re-synchronisation delay lines to update them with values from TX DLL Delay and RX DLL Delay fields.
30	PHY_CONFIG_RESET_FLD	W	1h	DLL Reset bit: This bit is used for reset of Delay Lines by software.
29	PHY_CONFIG_RX_DLL_BYPASS_FLD	R/W	0h	RX DLL Bypass: This field determines id RX DLL is bypassed.
28:23	PHY_CONFIG_RESV2_FLD	R	0h	Reserved
22:16	PHY_CONFIG_TX_DLL_DELAY_FLD	R/W	0h	TX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and spi_clk.
15:7	PHY_CONFIG_RESV1_FLD	R	0h	Reserved
6:0	PHY_CONFIG_RX_DLL_DELAY_FLD	R/W	0h	RX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and rx_dll_clk.

14.7.4.1.2.107 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register

14.7.4.1.2.107.1 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register (Offset = B8h) [reset = 800000h]

PHY DLL Master Control Register

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Table 14-12692. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00B8h

Figure 14-6266. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">PHY_MASTER_CONTROL_RESV3_FLD</td><td>PHY_MASTER_LOCK_MODE_FLD</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PHY_MASTER_BYPASS_MODE_FLD</td><td colspan="3">PHY_MASTER_PHASE_DETECT_SELECTOR_FLD</td><td>PHY_MASTER_CONTROL_RESV2_FLD</td><td colspan="3">PHY_MASTER_NB_INDICATIONS_FLD</td></tr>
<tr><td>R/W</td><td colspan="3">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td>1h</td><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHY_MASTER_CONTROL_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>PHY_MASTER_CONTROL_RESV1_FLD</td><td colspan="7">PHY_MASTER_INITIAL_DELAY_FLD</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-12693. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	PHY_MASTER_CONTROL_RESV3_FLD	R	0h	Reserved
24	PHY_MASTER_LOCK_MODE_FLD	R/W	0h	Determines if the initiator delay line locks on a full cycle or half cycle of delay.
23	PHY_MASTER_BYPASS_MODE_FLD	R/W	1h	Controls the bypass mode of the initiator and target DLLs.
22:20	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD	R/W	0h	Selects the number of delay elements to be inserted between the phase detect flip-flops.
19	PHY_MASTER_CONTROL_RESV2_FLD	R	0h	Reserved
18:16	PHY_MASTER_NB_INDICATIONS_FLD	R/W	0h	Holds the number of consecutive increment or decrement indications.
15:7	PHY_MASTER_CONTROL_RESV1_FLD	R	0h	Reserved
6:0	PHY_MASTER_INITIAL_DELAY_FLD	R/W	0h	This value is the initial delay value for the DLL.

14.7.4.1.2.108 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register

14.7.4.1.2.108.1 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register (Offset = BCh) [reset = 0h]

DLL Observable Register Lower

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Table 14-12694. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00BCh

Figure 14-6267. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD						
R	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD					DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD		DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD
R					R		R
0h					0h		0h

Table 14-12695. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD	R	0h	Holds the state of the cumulative dll_lock_inc register.
23:16	DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD	R	0h	Holds the state of the cumulative dll_lock_dec register.
15	DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	R	0h	This bit indicates that lock of loopback is done.
14:8	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD	R	0h	Reports the DLL encoder value from the initiator DLL to the target DLLs.
7:3	DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD	R	0h	Reports the number of increments or decrements required for the initiator DLL to complete the locking process.
2:1	DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD	R	0h	Defines the mode in which the DLL has achieved the lock.
0	DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD	R	0h	Indicates status of DLL.

14.7.4.1.2.109 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register

14.7.4.1.2.109.1 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register (Offset = C0h) [reset = 0h]

DLL Observable Register Upper

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Table 14-12696. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00C0h

Figure 14-6268. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_UPPER_RESV2_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DLL_OBSERVABLE_UPPER_RESV2_FLD	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DLL_OBSERVABLE_UPPER_RESV1_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLL_OBSERVABLE_UPPER_RESV1_FLD	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD						
R	R						
0h	0h						

Table 14-12697. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	DLL_OBSERVABLE_UPPER_RESV2_FLD	R	0h	Reserved
22:16	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the TX delay line for this slice.
15:7	DLL_OBSERVABLE_UPPER_RESV1_FLD	R	0h	Reserved
6:0	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the RX delay line for this slice.

14.7.4.1.2.110 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register

14.7.4.1.2.110.1 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register (Offset = E0h) [reset = 13EDFA00h]

Opcode Extension Register (Lower)

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Table 14-12698. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00E0h

Figure 14-6269. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Name Register

31	30	29	28	27	26	25	24
EXT_READ_OPCODE_FLD							
R/W							
13h							
23	22	21	20	19	18	17	16
EXT_WRITE_OPCODE_FLD							
R/W							
EDh							
15	14	13	12	11	10	9	8
EXT_POLL_OPCODE_FLD							
R/W							
FAh							
7	6	5	4	3	2	1	0
EXT_STIG_OPCODE_FLD							
R/W							
0h							

Table 14-12699. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EXT_READ_OPCODE_FLD	R/W	13h	Supplement byte of any Read Opcode
23:16	EXT_WRITE_OPCODE_FLD	R/W	EDh	Supplement byte of any Write Opcode
15:8	EXT_POLL_OPCODE_FLD	R/W	FAh	Supplement byte of any Polling Opcode
7:0	EXT_STIG_OPCODE_FLD	R/W	0h	Supplement byte of any STIG Opcode

14.7.4.1.2.111 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register

14.7.4.1.2.111.1 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register (Offset = E4h) [reset = 6F90000h]

Opcode Extension Register (Upper)

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Table 14-12700. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00E4h

Figure 14-6270. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Name Register

31	30	29	28	27	26	25	24
WEL_OPCODE_FLD							
R/W							
6h							
23	22	21	20	19	18	17	16
EXT_WEL_OPCODE_FLD							
R/W							
F9h							
15	14	13	12	11	10	9	8
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							

Table 14-12701. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WEL_OPCODE_FLD	R/W	6h	First byte of any WEL Opcode
23:16	EXT_WEL_OPCODE_FLD	R/W	F9h	Supplement byte of any WEL Opcode
15:0	OPCODE_EXT_UPPER_RESV1_FLD	R	0h	Reserved

14.7.4.1.2.112 OSPI_FLASH_CFG_MODULE_ID_REG Register

14.7.4.1.2.112.1 OSPI_FLASH_CFG_MODULE_ID_REG Register (Offset = FCh) [reset = 3000300h]

Module ID Register

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Table 14-12702. Instance Table

Instance Name	Physical Address
FSS0	0FC4 00FCh

Figure 14-6271. OSPI_FLASH_CFG_MODULE_ID_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FIX_PATCH_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MODULE_ID_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">MODULE_ID_RESV_FLD</td><td colspan="2">CONF_FLD</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12703. OSPI_FLASH_CFG_MODULE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	FIX_PATCH_FLD	R	3h	Fix/path number related to revision described by 3 LSBs of this register
23:8	MODULE_ID_FLD	R	3h	Module/Revision ID number
7:2	MODULE_ID_RESV_FLD	R	0h	Reserved
1:0	CONF_FLD	R	0h	Configuration ID number: 0 : OCTAL + PHY Configuration 1 : OCTAL Configuration 2 : QUAD + PHY Configuration 3 : QUAD Configuration

14.7.4.1.2.113 OSPI_CFG_PID Register

14.7.4.1.2.113.1 OSPI_CFG_PID Register (Offset = 0h) [reset = 68748100h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-12704. Instance Table

Instance Name	Physical Address
FSS0	0FC4 4000h

Figure 14-6272. OSPI_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		874h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
874h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-12705. OSPI_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: psrst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: psrst_n
27:16	MODULE_ID	R	874h	Module ID Reset Source: psrst_n
15:11	RTL	R	10h	RTL revision. Will vary depending on release. Reset Source: psrst_n
10:8	MAJOR	R	1h	Major revision Reset Source: psrst_n
7:6	CUSTOM	R	0h	Custom Reset Source: psrst_n
5:0	MINOR	R	0h	Minor revision Reset Source: psrst_n

14.7.4.1.2.114 OSPI_CFG_CTRL Register

14.7.4.1.2.114.1 OSPI_CFG_CTRL Register (Offset = 4h) [reset = 0h]

The Control Register contains general control bits for the ospi

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Table 14-12706. Instance Table

Instance Name	Physical Address
FSS0	0FC4 4004h

Figure 14-6273. OSPI_CFG_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PIPELINE_MODE_FLUSH	RESERVED		
NONE				R/W	NONE		
0h				0h	0h		

Table 14-12707. OSPI_CFG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PIPELINE_MODE_FLUSH	R/W	0h	1 - Flush Cadence Flash Controller FIFO by forcin gAHB SEL low. 0 - AHB Sel to Cadence Controller is 1 Reset Source: psrst_n
2:0	RESERVED	NONE	0h	Reserved

14.7.4.1.2.115 OSPI_CFG_STAT Register

14.7.4.1.2.115.1 OSPI_CFG_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the ospi

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Table 14-12708. Instance Table

Instance Name	Physical Address
FSS0	0FC4 4008h

Figure 14-6274. OSPI_CFG_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_INIT_DONE	RESERVED
NONE						R	NONE
0h						0h	0h

Table 14-12709. OSPI_CFG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_INIT_DONE	R	0h	0:Memory Initialization is in progress, 1:Memory Intialization Done Reset Source: psrst_n
0	RESERVED	NONE	0h	Reserved

14.7.4.1.2.116 OSPI_CFG_EOI Register

14.7.4.1.2.116.1 OSPI_CFG_EOI Register (Offset = 20h) [reset = 0h]

End of Interrupt Register

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Table 14-12710. Instance Table

Instance Name	Physical Address
FSS0	0FC4 4020h

Figure 14-6275. OSPI_CFG_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI							
W							
0h							

Table 14-12711. OSPI_CFG_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI	W	0h	Write with bit position of targetted interrupt. (E.g. Ext TS is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt Reset Source: psrst_n

14.7.4.1.2.117 FSS0_FOTA_GENREGS_FOTA_INIT Register

14.7.4.1.2.117.1 FSS0_FOTA_GENREGS_FOTA_INIT Register (Offset = 0h) [reset = 15h]

This register is used to initialize FOTA logic including M8051EW MCU

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Table 14-12712. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0000h

Figure 14-6276. FSS0_FOTA_GENREGS_FOTA_INIT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		MCU_STALL_EN	FUNC_MODE	PDMEM_INIT_DONE	MEMACCESS	CLKDIS	RESET
NONE		R/W	R/W	R	R/W	R/W	R/W
0h		0h	1h	0h	1h	0h	1h

Table 14-12713. FSS0_FOTA_GENREGS_FOTA_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	MCU_STALL_EN	R/W	0h	Reserved field. This field SHALL be retained at 0, which is the default value. Reset Source: vbus_mod_g_rst_n
4	FUNC_MODE	R/W	1h	This bit is used for selection functional or debug mode. 1'b1 - M8051EW uses functional mode for regular operation. 1'b0 - M8051EW uses debug mode for debug using JTAG. Reset Source: vbus_mod_g_rst_n
3	PDMEM_INIT_DONE	R	0h	This bit indicates that FOTA program/data memory RAM initialization is done. Until this bit is set, access to program/data memory should not be performed by software. Reset Source: vbus_mod_g_rst_n
2	MEMACCESS	R/W	1h	This bit provides SOC CPU access to program/data memory and internal memory through FSS config interface when set. If clear, these M8051EW memories are not accessible through config interface and is fully under the control of M8051EW. Software has to ensure that M8051EW is in reset by setting bit 0 of this register when memaccess is set. Reset Source: vbus_mod_g_rst_n

Table 14-12713. FSS0_FOTA_GENREGS_FOTA_INIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLKDIS	R/W	0h	This bit holds M8051EW core clock gated when set to 1'b1. Clock to M8051EW is enabled at reset. SOC software sets this bit to put M8051EW and other FOTA logic in low power state when not used by enabling clock gating. Reset Source: vbus_mod_g_rst_n
0	RESET	R/W	1h	This bit holds M8051EW core in reset when set to 1'b1. System firmware clears this bit after setting up program and data memories. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.118 FSS0_FOTA_GENREGS_FOTA_CTRL Register

14.7.4.1.2.118.1 FSS0_FOTA_GENREGS_FOTA_CTRL Register (Offset = 4h) [reset = 0h]

This register is used to start M8051EW firmware.

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Table 14-12714. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0004h

Figure 14-6277. FSS0_FOTA_GENREGS_FOTA_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GO
NONE							R/W1TS
0h							0h

Table 14-12715. FSS0_FOTA_GENREGS_FOTA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GO	R/W1TS	0h	SOC CPU sets this bit to indicate to M8051EW firmware that it can start the next FOTA page write. Once go is set, SOC software has to ensure that it is set again only after receiving an interrupt (completion or error) from M8051EW. If this requirement is not followed, it could result in M8051EW firmware repeating the FOTA write erroneously. A write to this register causes an indirect write to ESFR space for M8051EW. Firmware polls until ESFR GO bit is set and then starts the FOTA write sequence. This bit is cleared by hardware when the MCU has acknowledged GO through a write to the GO_ACK ESFR bit. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.119 FSS0_FOTA_GENREGS_FOTA_ERR_INFO Register

14.7.4.1.2.119.1 FSS0_FOTA_GENREGS_FOTA_ERR_INFO Register (Offset = 8h) [reset = 0h]

This register contains information from FOTA logic used when servicing fsas_fota_stat_err_pend/ fsas_fota_stat_err_req interrupt. This information is used in conjunction with FOTA interrupt status register ERR_STS_IRQ_STATUS_RAW. Software is expected to clear the fields in this register as it is not auto cleared by hardware.

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Table 14-12716. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0008h

Figure 14-6278. FSS0_FOTA_GENREGS_FOTA_ERR_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							MCU_ERR_CODE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
MCU_ERR_CODE				DAT_ERR_SSTATUS			DAT_ERR_RSTATUS
R/W				R/W			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
DAT_ERR_RSTATUS		CFG_ERR_SSTATUS			CFG_ERR_RSTATUS		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-12717. FSS0_FOTA_GENREGS_FOTA_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:12	MCU_ERR_CODE	R/W	0h	This field contains error code reported by M8051EW firmware when ERR_STS_IRQ_STATUS_RAW.mcu_err is set. Error codes are software defined. Example encoding: 5'd0 - Flash error encountered during auto status polling, 5'd1 - Auto polling timeout error as status read from flash did not occur within expected time, 5'd2 - FOTA write timeout error where auto polling by M8051EW has indicated that flash write is still in progress after auto polling expiry time programmed in firmware, 5'd3 to 5'd31 - Reserved for future use. Reset Source: vbus_mod_g_rst_n
11:9	DAT_ERR_SSTATUS	R/W	0h	This field contains read error status code when ERR_STS_IRQ_STATUS_RAW.dat_read_err interrupt flag is set Reset Source: vbus_mod_g_rst_n
8:6	DAT_ERR_RSTATUS	R/W	0h	This field contains read error status code when ERR_STS_IRQ_STATUS_RAW.dat_read_err interrupt flag is set Reset Source: vbus_mod_g_rst_n
5:3	CFG_ERR_SSTATUS	R/W	0h	This field contains read error status code when ERR_STS_IRQ_STATUS_RAW.cfg_read_err interrupt flag is set Reset Source: vbus_mod_g_rst_n

Table 14-12717. FSS0_FOTA_GENREGS_FOTA_ERR_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	CFG_ERR_RSTATUS	R/W	0h	This field contains read error status code when ERR_STS_IRQ_STATUS_RAW.cfg_read_err interrupt flag is set Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.120 FSS0_FOTA_GENREGS_FOTA_GP0 Register

14.7.4.1.2.120.1 FSS0_FOTA_GENREGS_FOTA_GP0 Register (Offset = 10h) [reset = 0h]

FOTA general purpose 0 register. SOC CPU can write to this register to pass information to M8051EW firmware through ESFR space.

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Table 14-12718. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0010h

Figure 14-6279. FSS0_FOTA_GENREGS_FOTA_GP0 Name Register

31	30	29	28	27	26	25	24
VAL3							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL2							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL1							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL0							
R/W							
0h							

Table 14-12719. FSS0_FOTA_GENREGS_FOTA_GP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	VAL3	R/W	0h	General purpose 0 register val3. Reset Source: vbus_mod_g_rst_n
23:16	VAL2	R/W	0h	General purpose 0 register val2. Reset Source: vbus_mod_g_rst_n
15:8	VAL1	R/W	0h	General purpose 0 register val1. Reset Source: vbus_mod_g_rst_n
7:0	VAL0	R/W	0h	General purpose 0 register val0. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.121 FSS0_FOTA_GENREGS_FOTA_GP1 Register

14.7.4.1.2.121.1 FSS0_FOTA_GENREGS_FOTA_GP1 Register (Offset = 14h) [reset = 0h]

FOTA general purpose 1 register. M8051EW can write to this register to pass information to SOC CPU through ESFR space. Interpretation for this register is software defined and can be made context dependent if required.

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Table 14-12720. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0014h

Figure 14-6280. FSS0_FOTA_GENREGS_FOTA_GP1 Name Register

31	30	29	28	27	26	25	24
VAL3							
R							
0h							
23	22	21	20	19	18	17	16
VAL2							
R							
0h							
15	14	13	12	11	10	9	8
VAL1							
R							
0h							
7	6	5	4	3	2	1	0
VAL0							
R							
0h							

Table 14-12721. FSS0_FOTA_GENREGS_FOTA_GP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	VAL3	R	0h	General purpose 1 register val3. Reset Source: vbus_mod_g_rst_n
23:16	VAL2	R	0h	General purpose 1 register val2. Reset Source: vbus_mod_g_rst_n
15:8	VAL1	R	0h	General purpose 1 register val1. Reset Source: vbus_mod_g_rst_n
7:0	VAL0	R	0h	General purpose 1 register val0. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.122 FSS0_FOTA_GENREGS_FOTA_ADDR Register

14.7.4.1.2.122.1 FSS0_FOTA_GENREGS_FOTA_ADDR Register (Offset = 18h) [reset = 0h]

FOTA operation write address register. SOC can write to this register to preload address for FOTA write instead of having 8051 firmware to setup address. Writing this register causes an indirect write to MCU_DAT_ADDR0-MCU_DAT_ADDR3 ESFR registers that are used by the VBUSM initiator as address for the FOTA write operation. Preloading these ESFR registers through this register removes the burden from 8051 firmware and reduces 8051 code size.

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Table 14-12722. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0018h

Figure 14-6281. FSS0_FOTA_GENREGS_FOTA_ADDR Name Register

31	30	29	28	27	26	25	24
VAL3							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL2							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL1							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL0							
R/W							
0h							

Table 14-12723. FSS0_FOTA_GENREGS_FOTA_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	VAL3	R/W	0h	FOTA write address bits 31:24 Reset Source: vbus_mod_g_rst_n
23:16	VAL2	R/W	0h	FOTA write address bits 23:16 Reset Source: vbus_mod_g_rst_n
15:8	VAL1	R/W	0h	FOTA write address bits 15:8 Reset Source: vbus_mod_g_rst_n
7:0	VAL0	R/W	0h	FOTA write address bits 7:0 Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.123 FSS0_FOTA_GENREGS_FOTA_CNT Register

14.7.4.1.2.123.1 FSS0_FOTA_GENREGS_FOTA_CNT Register (Offset = 1Ch) [reset = 0h]

FOTA operation write byte count. SOC can write to this register to preload byte count based on the page size of the flash memory used. Writing this register causes an indirect write to MCU_DAT_CNT0-MCU_DAT_CNT1 ESFR registers that are used by the VBUSM initiator as the overall byte count for the FOTA write operation. VBUSM initiator performs the required number of 32-byte writes to match this overall byte count. Preloading these ESFR registers through this register removes the burden from 8051 firmware and reduces 8051 code size.

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Table 14-12724. Instance Table

Instance Name	Physical Address
FSS0	0FC6 001Ch

Figure 14-6282. FSS0_FOTA_GENREGS_FOTA_CNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">VAL1</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VAL0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12725. FSS0_FOTA_GENREGS_FOTA_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	VAL1	R/W	0h	FOTA write byte count bits 9:8 Reset Source: vbus_mod_g_rst_n
7:0	VAL0	R/W	0h	FOTA write byte count bits 7:0 Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.124 FSS0_FOTA_GENREGS_STS_IRQ_EOI Register

14.7.4.1.2.124.1 FSS0_FOTA_GENREGS_STS_IRQ_EOI Register (Offset = 20h) [reset = 0h]

The End of Interrupt (EOI) Register allows the CPU to acknowledge completion of fsas_fota_stat_intr_req pulse interrupt. When this register is written to 1'b0, INTD logic used for converting fsas_ecc_intr_err_pend level interrupt to pulse will be re-armed. That is, if interrupt sources remain after writing this register to 1'b0, another pulse interrupt will be triggered by INTD. Conversely, if this register is not written to 1'b0 after fsas_fota_stat_intr_req pulse interrupt is received, then another pulse interrupt will not be received as INTD has not been re-armed. This register will be reset one cycle after it has been written to. Please note that the reason for writing 1'b0 is because there is only one interrupt (no interrupt aggregation) associated with this EOI and the INTD vector associated with this interrupt is 1'b0.

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Table 14-12726. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0020h + formula

Figure 14-6283. FSS0_FOTA_GENREGS_STS_IRQ_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_VECTOR</td></tr>
<tr><td colspan="7">NONE</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12727. FSS0_FOTA_GENREGS_STS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	W	0h	Write 1'b0 to acknowledge fsas_fota_stat_intr_req pulse interrupt. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.125 FSS0_FOTA_GENREGS_STS_IRQ_STATUS_RAW Register

14.7.4.1.2.125.1 FSS0_FOTA_GENREGS_STS_IRQ_STATUS_RAW Register (Offset = 24h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources to be manually set when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_intr_pend/fsas_fota_stat_intr_req interrupt output. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-12728. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0024h + formula

Figure 14-6284. FSS0_FOTA_GENREGS_STS_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FOTA_DONE
NONE							R/W1TS
0h							0h

Table 14-12729. FSS0_FOTA_GENREGS_STS_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FOTA_DONE	R/W1TS	0h	FOTA done raw status flag Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.126 FSS0_FOTA_GENREGS_STS_IRQ_STATUS Register

14.7.4.1.2.126.1 FSS0_FOTA_GENREGS_STS_IRQ_STATUS Register (Offset = 28h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources to be manually cleared when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_intr_pend/fsas_fota_stat_intr_req interrupt output. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-12730. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0028h + formula

Figure 14-6285. FSS0_FOTA_GENREGS_STS_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FOTA_DONE
NONE							R/W1TC
0h							0h

Table 14-12731. FSS0_FOTA_GENREGS_STS_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FOTA_DONE	R/W1TC	0h	FOTA done status flag Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.127 FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_SET Register

14.7.4.1.2.127.1 FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_SET Register (Offset = 2Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources to be manually enabled when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_intr_pend/fsas_fota_stat_intr_req interrupt output. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-12732. Instance Table

Instance Name	Physical Address
FSS0	0FC6 002Ch + formula

Figure 14-6286. FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FOTA_DONE
NONE							R/W1TS
0h							0h

Table 14-12733. FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FOTA_DONE	R/W1TS	0h	FOTA done enable set Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.128 FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_CLR Register

14.7.4.1.2.128.1 FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_CLR Register (Offset = 30h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources to be manually disabled when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_intr_pend/fsas_fota_stat_intr_req interrupt output. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-12734. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0030h + formula

Figure 14-6287. FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FOTA_DONE
NONE							R/W1TC
0h							0h

Table 14-12735. FSS0_FOTA_GENREGS_STS_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FOTA_DONE	R/W1TC	0h	FOTA done enable clear Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.129 FSS0_FOTA_GENREGS_ERR_STS_IRQ_EOI Register

14.7.4.1.2.129.1 FSS0_FOTA_GENREGS_ERR_STS_IRQ_EOI Register (Offset = 40h) [reset = 0h]

The End of Interrupt (EOI) Register allows the CPU to acknowledge completion of fsas_fota_stat_err_req pulse interrupt. When this register is written to 1'b0, INTD logic used for converting fsas_ecc_intr_err_pend level interrupt to pulse will be re-armed. That is, if interrupt sources remain after writing this register to 1'b0, another pulse interrupt will be triggered by INTD. Conversely, if this register is not written to 1'b0 after fsas_fota_stat_err_req pulse interrupt is received, then another pulse interrupt will not be received as INTD has not been re-armed. This register will be reset one cycle after it has been written to. Please note that the reason for writing 1'b0 is because there is only one interrupt (no interrupt aggregation) associated with this EOI and the INTD vector associated with this interrupt is 1'b0.

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Table 14-12736. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0040h + formula

Figure 14-6288. FSS0_FOTA_GENREGS_ERR_STS_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							W
0h							0h

Table 14-12737. FSS0_FOTA_GENREGS_ERR_STS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	W	0h	Write 1'b0 to acknowledge fsas_fota_stat_err_req pulse interrupt. Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.130 FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS_RAW Register

14.7.4.1.2.130.1 FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS_RAW Register (Offset = 44h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources to be manually set when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_err_pend/fsas_fota_stat_err_req interrupt output. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-12738. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0044h + formula

Figure 14-6289. FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MCU_ERR	DAT_WRITE_ERR	DAT_READ_ERR	CFG_WRITE_ERR	CFG_READ_ERR	RESERVED	
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	NONE	
0h	0h	0h	0h	0h	0h	0h	

Table 14-12739. FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	MCU_ERR	R/W1TS	0h	MCU error raw status flag. This is used to communicate error conditions encountered by 8051 firmware to SOC CPU. Error code is captured in FOTA_ERR_INFO.mcu_err_code field. If 8051 firmware runs into any error conditions, it sets the FOTA_ERR_STAT.mcu_err ESFR bit to 1'b1 and writes the corresponding error code into FOTA_ERR_STAT.mcu_err_code field. This causes an indirect writes to STATUS_RAW.mcu_err MMR and FOTA_ERR_INFO.mcu_err_code MMR. M8051EW firmware defines the error codes that result in this error. Please refer to FOTA_ERR_INFO.mcu_err_code MMR description for suggested encoding. Reset Source: vbus_mod_g_rst_n
5	DAT_WRITE_ERR	R/W1TS	0h	Data interface write status error raw status flag. This error flag gets set when M8051EW performs a data write and error status is returned. The CBA error status code received is stored in FOTA_ERR_INFO.dat_err_sstatus register. Reset Source: vbus_mod_g_rst_n

Table 14-12739. FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DAT_READ_ERR	R/W1TS	0h	Data interface read status error raw status flag. This error flag gets set when M8051EW performs a data read and error status is returned. The CBA error status code received is stored in FOTA_ERR_INFO.dat_err_rstatus register. Reset Source: vbus_mod_g_rst_n
3	CFG_WRITE_ERR	R/W1TS	0h	Config interface write status error raw status flag. This error flag gets set when M8051EW performs a configuration write and error status is returned. The CBA error status code received is stored in FOTA_ERR_INFO.cfg_err_sstatus register. Reset Source: vbus_mod_g_rst_n
2	CFG_READ_ERR	R/W1TS	0h	Config interface read status error raw status flag. This error flag gets set when M8051EW performs a configuration read and error status is returned. The CBA error status code received is stored in FOTA_ERR_INFO.cfg_err_rstatus register. Reset Source: vbus_mod_g_rst_n
1:0	RESERVED	NONE	0h	Reserved

14.7.4.1.2.131 FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS Register

14.7.4.1.2.131.1 FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS Register (Offset = 48h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources to be manually cleared when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_err_pend/fsas_fota_stat_err_req interrupt output. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

Return to Summary Table

Table 14-12740. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0048h + formula

Figure 14-6290. FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MCU_ERR	DAT_WRITE_ERR	DAT_READ_ERR	CFG_WRITE_ERR	CFG_READ_ERR	RESERVED	
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE	
0h	0h	0h	0h	0h	0h	0h	

Table 14-12741. FSS0_FOTA_GENREGS_ERR_STS_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	MCU_ERR	R/W1TC	0h	MCU error status flag Reset Source: vbus_mod_g_rst_n
5	DAT_WRITE_ERR	R/W1TC	0h	Data interface write status error status flag Reset Source: vbus_mod_g_rst_n
4	DAT_READ_ERR	R/W1TC	0h	Data interface read status error status flag Reset Source: vbus_mod_g_rst_n
3	CFG_WRITE_ERR	R/W1TC	0h	Config interface write status error status flag Reset Source: vbus_mod_g_rst_n
2	CFG_READ_ERR	R/W1TC	0h	Config interface read status error status flag Reset Source: vbus_mod_g_rst_n
1:0	RESERVED	NONE	0h	Reserved

14.7.4.1.2.132 FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_SET Register

14.7.4.1.2.132.1 FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_SET Register (Offset = 4Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources to be manually enabled when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_err_pend/fsas_fota_stat_err_req interrupt output. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

Return to Summary Table

Table 14-12742. Instance Table

Instance Name	Physical Address
FSS0	0FC6 004Ch + formula

Figure 14-6291. FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MCU_ERR	DAT_WRITE_ERR	DAT_READ_ERR	CFG_WRITE_ERR	CFG_READ_ERR	RESERVED	
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	NONE	
0h	0h	0h	0h	0h	0h	0h	

Table 14-12743. FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	MCU_ERR	R/W1TS	0h	MCU error enable set Reset Source: vbus_mod_g_rst_n
5	DAT_WRITE_ERR	R/W1TS	0h	Data interface write status error enable set Reset Source: vbus_mod_g_rst_n
4	DAT_READ_ERR	R/W1TS	0h	Data interface read status error enable set Reset Source: vbus_mod_g_rst_n
3	CFG_WRITE_ERR	R/W1TS	0h	Config interface write status error enable set Reset Source: vbus_mod_g_rst_n
2	CFG_READ_ERR	R/W1TS	0h	Config interface read status error enable set Reset Source: vbus_mod_g_rst_n
1:0	RESERVED	NONE	0h	Reserved

14.7.4.1.2.133 FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_CLR Register

14.7.4.1.2.133.1 FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_CLR Register (Offset = 50h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources to be manually disabled when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_err_pend/fsas_fota_stat_err_req interrupt output. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-12744. Instance Table

Instance Name	Physical Address
FSS0	0FC6 0050h + formula

Figure 14-6292. FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MCU_ERR	DAT_WRITE_ERR	DAT_READ_ERR	CFG_WRITE_ERR	CFG_READ_ERR	RESERVED	
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE	
0h	0h	0h	0h	0h	0h	0h	

Table 14-12745. FSS0_FOTA_GENREGS_ERR_STS_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	MCU_ERR	R/W1TC	0h	MCU error enable clear Reset Source: vbus_mod_g_rst_n
5	DAT_WRITE_ERR	R/W1TC	0h	Data interface write status error enable clear Reset Source: vbus_mod_g_rst_n
4	DAT_READ_ERR	R/W1TC	0h	Data interface read status error enable clear Reset Source: vbus_mod_g_rst_n
3	CFG_WRITE_ERR	R/W1TC	0h	Config interface write status error enable clear Reset Source: vbus_mod_g_rst_n
2	CFG_READ_ERR	R/W1TC	0h	Config interface read status error enable clear Reset Source: vbus_mod_g_rst_n
1:0	RESERVED	NONE	0h	Reserved

14.7.4.1.2.134 FSS0_PDMEM_GENREGS_LOC_J Register

14.7.4.1.2.134.1 FSS0_PDMEM_GENREGS_LOC_J Register (Offset = 0h) [reset = 0h]

M8051EW program and external data memory array

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Table 14-12746. Instance Table

Instance Name	Physical Address
FSS0	0FC6 1000h + formula

Figure 14-6293. FSS0_PDMEM_GENREGS_LOC_j Name Register

31	30	29	28	27	26	25	24
VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL							
R/W							
0h							

Table 14-12747. FSS0_PDMEM_GENREGS_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R/W	0h	Value of element in program and external data memory Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.135 FSS0_IMEM_GENREGS_LOC_J Register

14.7.4.1.2.135.1 FSS0_IMEM_GENREGS_LOC_J Register (Offset = 0h) [reset = 0h]

M8051EW Internal Data Memory array

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Table 14-12748. Instance Table

Instance Name	Physical Address
FSS0	0FC6 2000h + formula

Figure 14-6294. FSS0_IMEM_GENREGS_LOC_j Name Register

31	30	29	28	27	26	25	24
VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL							
R/W							
0h							

Table 14-12749. FSS0_IMEM_GENREGS_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R/W	0h	Value of element in internal data memory Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.136 FSS0_WBUF_GENREGS_LOC_J Register

14.7.4.1.2.136.1 FSS0_WBUF_GENREGS_LOC_J Register (Offset = 0h) [reset = 0h]

FOTA write buffer array

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Table 14-12750. Instance Table

Instance Name	Physical Address
FSS0	0FC6 3000h + formula

Figure 14-6295. FSS0_WBUF_GENREGS_LOC_j Name Register

31	30	29	28	27	26	25	24
VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL							
R/W							
0h							

Table 14-12751. FSS0_WBUF_GENREGS_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R/W	0h	Value of element in FOTA write buffer Reset Source: vbus_mod_g_rst_n

14.7.4.1.2.137 DAT_REG1_HPB_DATA_MEM_J Register

14.7.4.1.2.137.1 DAT_REG1_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS boot data region1

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Table 14-12752. Instance Table

Instance Name	Physical Address
FSS0	6000 0000h + formula

Figure 14-6296. DAT_REG1_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HPB_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HPB_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HPB_DATA							
R/W							
0h							

Table 14-12753. DAT_REG1_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1 Reset Source: rst_mod_g_rst_n

14.7.4.1.2.138 DAT_REG0_HPB_DATA_MEM_J Register

14.7.4.1.2.138.1 DAT_REG0_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS data region0

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Table 14-12754. Instance Table

Instance Name	Physical Address
FSS0	0004 0000 0000h + formula

Figure 14-6297. DAT_REG0_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-12755. DAT_REG0_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region0 Reset Source: rst_mod_g_rst_n

14.7.4.1.2.139 DAT_REG3_HPB_DATA_MEM_J Register

14.7.4.1.2.139.1 DAT_REG3_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS bypass data region3

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Table 14-12756. Instance Table

Instance Name	Physical Address
FSS0	0005 0000 0000h + formula

Figure 14-6298. DAT_REG3_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-12757. DAT_REG3_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1 Reset Source: rst_mod_g_rst_n

14.7.4.2 FSS1

FSS1

14.7.4.2.1 FSS1 Summaries

FSS1 Summaries

Table 14-12758. FSS_GENREGS Registers, Base Address=0FC8 0000h, Length=256

Offset	Length	Register Name	FSS1 Physical Address
0h	32	FSS_GENREGS_REVISION	0FC8 0000h
4h	32	FSS_GENREGS_SYSCONFIG	0FC8 0004h
10h	32	FSS_GENREGS_IRQ_EOI	0FC8 0010h + formula
14h	32	FSS_GENREGS_IRQ_STATUS_RAW	0FC8 0014h + formula
18h	32	FSS_GENREGS_IRQ_STATUS	0FC8 0018h + formula
1Ch	32	FSS_GENREGS_IRQ_ENABLE_SET	0FC8 001Ch + formula
20h	32	FSS_GENREGS_IRQ_ENABLE_CLR	0FC8 0020h + formula
30h	32	FSS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J	0FC8 0030h + formula
34h	32	FSS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J	0FC8 0034h + formula
70h	32	FSS_GENREGS_ERR_ECC_BLOCK_ADR	0FC8 0070h + formula
74h	32	FSS_GENREGS_ERR_ECC_TYPE	0FC8 0074h + formula
78h	32	FSS_GENREGS_ERR_WRT_TYPE	0FC8 0078h + formula

14.7.4.2.2 FSS1 Registers

FSS1 Registers

14.7.4.2.2.1 FSS_GENREGS_REVISION Register

14.7.4.2.2.1.1 FSS_GENREGS_REVISION Register (Offset = 0h) [reset = 68501101h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-12759. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0000h

Figure 14-6299. FSS_GENREGS_REVISION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6850h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6850h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">2h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-12760. FSS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field Reset Source: vbus_mod_g_rst_n
15:11	REVRTL	R	2h	RTL revision. Will vary depending on release. Reset Source: vbus_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: vbus_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_mod_g_rst_n
5:0	REVMIN	R	1h	Minor revision Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.2 FSS_GENREGS_SYSCONFIG Register

14.7.4.2.2.2.1 FSS_GENREGS_SYSCONFIG Register (Offset = 4h) [reset = 0h]

Controls various parameters of the cotroller state.

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Table 14-12761. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0004h

Figure 14-6300. FSS_GENREGS_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							OSPI_32B_DISABLE_MODE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
DISXIP	OSPI_DDR_DISABLE_MODE	RESERVED		ECC_DISABLE_ADR	FSS_AES_EN_IPCFG	HB_OSPI	ECC_EN
R/W	R/W	NONE		R/W	R	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-12762. FSS_GENREGS_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	OSPI_32B_DISABLE_MODE	R/W	0h	0 OSPI 32bit mode enabled. 1 OSPI 32bit mode disabled Reset Source: vbus_mod_g_rst_n
7	DISXIP	R/W	0h	0 XIP Prefetch Enabled. 1 XIP prefetch disabled Reset Source: vbus_mod_g_rst_n
6	OSPI_DDR_DISABLE_MODE	R/W	0h	0 OSPI DDR mode enabled. 1 OSPI DDR mode disabled Reset Source: vbus_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	ECC_DISABLE_ADR	R/W	0h	0 Block address within ECC calculation, 1 Block address not within ECC calculation Reset Source: vbus_mod_g_rst_n
2	FSS_AES_EN_IPCFG	R	0h	1 select security, 0 disable security Reset Source: vbus_mod_g_rst_n
1	HB_OSPI	R/W	0h	1 select hb path. 0 select ospi path Reset Source: vbus_mod_g_rst_n
0	ECC_EN	R/W	0h	0 ECC disabled. 1 ECC enabled Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.3 FSS_GENREGS_IRQ_EOI Register

14.7.4.2.2.3.1 FSS_GENREGS_IRQ_EOI Register (Offset = 10h) [reset = 0h]

The End of Interrupt (EOI) MISC Register allows the CPU to acknowledge completion of an interrupt by writing to the EOI for MISC interrupt sources. An eoi_write signal will be generated and another interrupt will be triggered if interrupt sources remain. This register will be reset one cycle after it has been written to.

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Table 14-12763. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0010h + formula

Figure 14-6301. FSS_GENREGS_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							R/W
0h							0h

Table 14-12764. FSS_GENREGS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	R/W	0h	Write with bit position of targeted interrupt. (E.g. Ext FSS ECC is bit 0). Upon write, level interrupt will clear and if un-serviced will issue another pulse interrupt Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.4 FSS_GENREGS_IRQ_STATUS_RAW Register

14.7.4.2.2.4.1 FSS_GENREGS_IRQ_STATUS_RAW Register (Offset = 14h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-12765. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0014h + formula

Figure 14-6302. FSS_GENREGS_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-12766. FSS_GENREGS_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.5 FSS_GENREGS_IRQ_STATUS Register

14.7.4.2.2.5.1 FSS_GENREGS_IRQ_STATUS Register (Offset = 18h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-12767. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0018h + formula

Figure 14-6303. FSS_GENREGS_IRQ_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>ECC_WRITE_NONALIGN</td><td>ECC_ERROR_2BIT</td><td>ECC_ERROR_1BIT</td></tr>
<tr><td colspan="5">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12768. FSS_GENREGS_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.6 FSS_GENREGS_IRQ_ENABLE_SET Register

14.7.4.2.2.6.1 FSS_GENREGS_IRQ_ENABLE_SET Register (Offset = 1Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

Return to Summary Table

Table 14-12769. Instance Table

Instance Name	Physical Address
FSS1	0FC8 001Ch + formula

Figure 14-6304. FSS_GENREGS_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-12770. FSS_GENREGS_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.7 FSS_GENREGS_IRQ_ENABLE_CLR Register

14.7.4.2.2.7.1 FSS_GENREGS_IRQ_ENABLE_CLR Register (Offset = 20h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-12771. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0020h + formula

Figure 14-6305. FSS_GENREGS_IRQ_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>ECC_WRITE_NONALIGN</td><td>ECC_ERROR_2BIT</td><td>ECC_ERROR_1BIT</td></tr>
<tr><td colspan="5">NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12772. FSS_GENREGS_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.8 FSS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J Register

14.7.4.2.2.8.1 FSS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J Register (Offset = 30h) [reset = 0h]

This defines the start of the ECC region in 4KBytes steps.

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Table 14-12773. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0030h + formula

Figure 14-6306. FSS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START							
R/W							
0h							

Table 14-12774. FSS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START	R/W	0h	This defines the start of the ECC region in 4KBytes steps. Address start = {start[19:0], 0x000} 0x0 means the start is 0x0000_0000 0x1 means the start is 0x0000_1000 0xA means the start is 0x0000_A000 Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.9 FSS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J Register

14.7.4.2.2.9.1 FSS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J Register (Offset = 34h) [reset = 0h]

This defines the size of the ECC region in 4KBytes steps.

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Table 14-12775. Instance Table

Instance Name	**Physical Address**
FSS1	0FC8 0034h + formula

Figure 14-6307. FSS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R_SIZE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_SIZE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_SIZE							
R/W							
0h							

Table 14-12776. FSS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE	R/W	0h	This defines the size of the ECC region in 4KBytes steps 0x0 means the size is zero and disabled 0x1 means the size is 4KBytes 0xA means the size is 40KBytes 0xF_FFFF means the size is 4GBytes Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.10 FSS_GENREGS_ERR_ECC_BLOCK_ADR Register

14.7.4.2.2.10.1 FSS_GENREGS_ERR_ECC_BLOCK_ADR Register (Offset = 70h) [reset = 0h]

The ERR_ECC_BLOCK_ADR register holds the current top of stack ECC error block address, this is only valid when the ecc_err_valid is set

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Table 14-12777. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0070h + formula

Figure 14-6308. FSS_GENREGS_ERR_ECC_BLOCK_ADR Name Register

31	30	29	28	27	26	25	24
ECC_ERROR_BLOCK_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ERROR_BLOCK_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ERROR_BLOCK_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ERROR_BLOCK_ADDR			RESERVED				
R			NONE				
0h			0h				

Table 14-12778. FSS_GENREGS_ERR_ECC_BLOCK_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	ECC_ERROR_BLOCK_ADDR	R	0h	ECC 32 byte aligned block address Reset Source: vbus_mod_g_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.7.4.2.2.11 FSS_GENREGS_ERR_ECC_TYPE Register

14.7.4.2.2.11.1 FSS_GENREGS_ERR_ECC_TYPE Register (Offset = 74h) [reset = 0h]

The ERR_ECC_TYPE register holds the current top of stack ECC error info, this is only valid when the ecc_err_valid is set

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Table 14-12779. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0074h + formula

Figure 14-6309. FSS_GENREGS_ERR_ECC_TYPE Name Register

31	30	29	28	27	26	25	24
ECC_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECC_ERR_ADR	ECC_ERR_MAC	ECC_ERR_DA1	ECC_ERR_DA0	ECC_ERR_DED	ECC_ERR_SEC
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 14-12780. FSS_GENREGS_ERR_ECC_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_ERR_VALID	R/W1TC	0h	When set indicates that there is valid ECC error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:6	RESERVED	NONE	0h	Reserved
5	ECC_ERR_ADR	R	0h	When set indicates that there was a single error detected within the address field Reset Source: vbus_mod_g_rst_n
4	ECC_ERR_MAC	R	0h	When set indicates that there was a single error detected within the MAC field Reset Source: vbus_mod_g_rst_n
3	ECC_ERR_DA1	R	0h	When set indicates that there was a single error detected within the High Data word Reset Source: vbus_mod_g_rst_n
2	ECC_ERR_DA0	R	0h	When set indicates that there was a single error detected within the Low Data word Reset Source: vbus_mod_g_rst_n
1	ECC_ERR_DED	R	0h	When set indicates that there was a double error detected for the block Reset Source: vbus_mod_g_rst_n

Table 14-12780. FSS_GENREGS_ERR_ECC_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECC_ERR_SEC	R	0h	hen set indicates that there was a single error detected for the block Reset Source: vbus_mod_g_rst_n

14.7.4.2.2.12 FSS_GENREGS_ERR_WRT_TYPE Register

14.7.4.2.2.12.1 FSS_GENREGS_ERR_WRT_TYPE Register (Offset = 78h) [reset = 0h]

The ERR_WRT_TYPE register holds the current top of stack write error info. this is only valid when the wrt_err_valid is set

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Table 14-12781. Instance Table

Instance Name	Physical Address
FSS1	0FC8 0078h + formula

Figure 14-6310. FSS_GENREGS_ERR_WRT_TYPE Name Register

31	30	29	28	27	26	25	24
WRT_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRT_ERR_BEN	WRT_ERR_ADR	WRT_ERR_ROUTEID			
NONE		R	R	R			
0h		0h	0h	0h			
7	6	5	4	3	2	1	0
WRT_ERR_ROUTEID							
R							
0h							

Table 14-12782. FSS_GENREGS_ERR_WRT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRT_ERR_VALID	R/W1TC	0h	When set indicates that there is valid write error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:14	RESERVED	NONE	0h	Reserved
13	WRT_ERR_BEN	R	0h	When set indicates that there was a write error due to a non-contiguous byte enables Reset Source: vbus_mod_g_rst_n
12	WRT_ERR_ADR	R	0h	When set indicates that there was a write error due to a non-aligned address Reset Source: vbus_mod_g_rst_n
11:0	WRT_ERR_ROUTEID	R	0h	Indicates the Route ID for the Initiator that caused the write error Reset Source: vbus_mod_g_rst_n

14.7.4.3 OSPI1

OSPI1

14.7.4.3.1 OSPI1 Summaries

OSPI1 Summaries

Table 14-12783. ECC_AGGR Registers, Base Address=0072 3000h, Length=1024

Offset	Length	Register Name	FSS1_OSPI_0 Physical Address
0h	32	ECC_AGGR_REV	0072 3000h
8h	32	ECC_AGGR_VECTOR	0072 3008h
Ch	32	ECC_AGGR_STAT	0072 300Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0072 3010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0072 303Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0072 3040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0072 3080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0072 30C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0072 313Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0072 3140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0072 3180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0072 31C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0072 3200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0072 3204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0072 3208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0072 320Ch

Table 14-12784. OSPI_FLASH_CFG Registers, Base Address=0FCC 0000h, Length=256

Offset	Length	Register Name	FSS1_OSPI_0 Physical Address
0h	32	OSPI_FLASH_CFG_CONFIG_REG	0FCC 0000h
4h	32	OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG	0FCC 0004h
8h	32	OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG	0FCC 0008h
Ch	32	OSPI_FLASH_CFG_DEV_DELAY_REG	0FCC 000Ch
10h	32	OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG	0FCC 0010h
14h	32	OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG	0FCC 0014h
18h	32	OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG	0FCC 0018h
1Ch	32	OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG	0FCC 001Ch
20h	32	OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG	0FCC 0020h
24h	32	OSPI_FLASH_CFG_REMAP_ADDR_REG	0FCC 0024h
28h	32	OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG	0FCC 0028h
2Ch	32	OSPI_FLASH_CFG_SRAM_FILL_REG	0FCC 002Ch
30h	32	OSPI_FLASH_CFG_TX_THRESH_REG	0FCC 0030h
34h	32	OSPI_FLASH_CFG_RX_THRESH_REG	0FCC 0034h
38h	32	OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG	0FCC 0038h
3Ch	32	OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG	0FCC 003Ch
40h	32	OSPI_FLASH_CFG_IRQ_STATUS_REG	0FCC 0040h
44h	32	OSPI_FLASH_CFG_IRQ_MASK_REG	0FCC 0044h
50h	32	OSPI_FLASH_CFG_LOWER_WR_PROT_REG	0FCC 0050h
54h	32	OSPI_FLASH_CFG_UPPER_WR_PROT_REG	0FCC 0054h

Table 14-12784. OSPI_FLASH_CFG Registers, Base Address=0FCC 0000h, Length=256 (continued)

Offset	Length	Register Name	FSS1_OSPI_0 Physical Address
58h	32	OSPI_FLASH_CFG_WR_PROT_CTRL_REG	0FCC 0058h
60h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG	0FCC 0060h
64h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG	0FCC 0064h
68h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG	0FCC 0068h
6Ch	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG	0FCC 006Ch
70h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG	0FCC 0070h
74h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG	0FCC 0074h
78h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG	0FCC 0078h
7Ch	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG	0FCC 007Ch
80h	32	OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG	0FCC 0080h
8Ch	32	OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG	0FCC 008Ch
90h	32	OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG	0FCC 0090h
94h	32	OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG	0FCC 0094h
A0h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG	0FCC 00A0h
A4h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG	0FCC 00A4h
A8h	32	OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG	0FCC 00A8h
ACh	32	OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG	0FCC 00ACh
B0h	32	OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG	0FCC 00B0h
B4h	32	OSPI_FLASH_CFG_PHY_CONFIGURATION_REG	0FCC 00B4h
B8h	32	OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG	0FCC 00B8h
BCh	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG	0FCC 00BCh
C0h	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG	0FCC 00C0h
E0h	32	OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG	0FCC 00E0h
E4h	32	OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG	0FCC 00E4h
FCh	32	OSPI_FLASH_CFG_MODULE_ID_REG	0FCC 00FCh

Table 14-12785. OSPI_CFG Registers, Base Address=0FCC 4000h, Length=512

Offset	Length	Register Name	FSS1_OSPI_0 Physical Address
0h	32	OSPI_CFG_PID	0FCC 4000h
4h	32	OSPI_CFG_CTRL	0FCC 4004h
8h	32	OSPI_CFG_STAT	0FCC 4008h
20h	32	OSPI_CFG_EOI	0FCC 4020h

14.7.4.3.2 OSPI1 Registers

OSPI1 Registers

14.7.4.3.2.1 ECC_AGGR_REV Register

14.7.4.3.2.1.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

Revision parameters

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Table 14-12786. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3000h

Figure 14-6311. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
1Dh					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-12787. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	1Dh	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

14.7.4.3.2.2 ECC_AGGR_VECTOR Register

14.7.4.3.2.2.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12788. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3008h

Figure 14-6312. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12789. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.4.3.2.3 ECC_AGGR_STAT Register

14.7.4.3.2.3.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-12790. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 300Ch

Figure 14-6313. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_RAMS							
R							
1h							

Table 14-12791. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.4.3.2.4 ECC_AGGR_RESERVED_SVBUS_J Register

14.7.4.3.2.4.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-12792. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3010h + formula

Figure 14-6314. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-12793. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.4.3.2.5 ECC_AGGR_SEC_EOI_REG Register

14.7.4.3.2.5.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-12794. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 303Ch

Figure 14-6315. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12795. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.3.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

14.7.4.3.2.6.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12796. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3040h

Figure 14-6316. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 14-12797. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.7.4.3.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.7.4.3.2.7.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12798. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3080h

Figure 14-6317. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-12799. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.7.4.3.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.7.4.3.2.8.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12800. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 30C0h

Figure 14-6318. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-12801. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.7.4.3.2.9 ECC_AGGR_DED_EOI_REG Register

14.7.4.3.2.9.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-12802. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 313Ch

Figure 14-6319. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12803. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.3.2.10 ECC_AGGR_DED_STATUS_REG0 Register

14.7.4.3.2.10.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12804. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3140h

Figure 14-6320. ECC_AGGR_DED_STATUS_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SRAM_PEND</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12805. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

14.7.4.3.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.7.4.3.2.11.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12806. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3180h

Figure 14-6321. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-12807. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

14.7.4.3.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.7.4.3.2.12.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12808. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 31C0h

Figure 14-6322. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-12809. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

14.7.4.3.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

14.7.4.3.2.13.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12810. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3200h

Figure 14-6323. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12811. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.4.3.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

14.7.4.3.2.14.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12812. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3204h

Figure 14-6324. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12813. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.4.3.2.15 ECC_AGGR_AGGR_STATUS_SET Register

14.7.4.3.2.15.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12814. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 3208h

Figure 14-6325. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-12815. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.4.3.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

14.7.4.3.2.16.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12816. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0072 320Ch

Figure 14-6326. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-12817. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.4.3.2.17 OSPI_FLASH_CFG_CONFIG_REG Register

14.7.4.3.2.17.1 OSPI_FLASH_CFG_CONFIG_REG Register (Offset = 0h) [reset = 80780081h]

Octal-SPI Configuration Register

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Table 14-12818. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0000h

Figure 14-6327. OSPI_FLASH_CFG_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
IDLE_FLD	DUAL_BYTE_OPCODE_EN_FLD	CRC_ENABLE_FLD	CONFIG_RESV2_FLD			PIPELINE_PHY_FLD	ENABLE_DTR_PROTOCOL_FLD
R	R/W	R/W	R			R/W	R/W
1h	0h	0h	0h			0h	0h
23	22	21	20	19	18	17	16
ENABLE_AHB_DECODER_FLD	MSTR_BAUD_DIV_FLD				ENTER_XIP_MODE_IMM_FLD	ENTER_XIP_MODE_FLD	ENB_AHB_ADDR_REMAP_FLD
R/W	R/W				R/W	R/W	R/W
0h	Fh				0h	0h	0h
15	14	13	12	11	10	9	8
ENB_DMA_IF_FLD	WR_PROT_FLASH_FLD	PERIPH_CS_LINES_FLD				PERIPH_SEL_DEC_FLD	ENB_LEGACY_IP_MODE_FLD
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h
7	6	5	4	3	2	1	0
ENB_DIR_ACC_CTLR_FLD	RESET_CFG_FLD	RESET_PIN_FLD	HOLD_PIN_FLD	PHY_MODE_ENABLE_FLD	SEL_CLK_PHASE_FLD	SEL_CLK_POL_FLD	ENB_SPI_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	1h

Table 14-12819. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE_FLD	R	1h	Serial interface and low level SPI pipeline is IDLE: This is a STATUS read-only bit. Note this is a retimed signal, so there will be some inherent delay on the generation of this status signal.
30	DUAL_BYTE_OPCODE_EN_FLD	R/W	0h	Dual-byte Opcode Mode enable bit This bit is to be set in case the target Flash Device supports dual byte opcode [i.e. Macronix MX25]. It is applicable for Octal I/O Mode or Protocol only so should be set back to low if the device is configured to work in another SPI Mode. If enabled, the supplementing bytes are taken from Opcode Extension Register [Lower] and from Opcode Extension Register [Upper].
29	CRC_ENABLE_FLD	R/W	0h	CRC enable bit This bit is to be set in case the target Flash Device supports CRC [Macronix MX25]. It is applicable for Octal DDR Protocol only so should be set back to low if the device is configured to work in another SPI Mode.
28:26	CONFIG_RESV2_FLD	R	0h	Reserved
25	PIPELINE_PHY_FLD	R/W	0h	Pipeline PHY Mode enable: This bit is relevant only for configuration with PHY Module. It should be asserted to 1 between consecutive PHY pipeline reads transfers and de-asserted to 0 otherwise.
24	ENABLE_DTR_PROTOCOL_FLD	R/W	0h	Enable DTR Protocol: This bit should be set if device is configured to work in DTR protocol.

Table 14-12819. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ENABLE_AHB_DECODER_FLD	R/W	0h	Enable AHB Decoder: Value=0 : Active target is selected based on Peripheral Chip Select Lines [bits [13:10]]. Value=1 Active target is selected based on actual AHB address [the partition for each device is calculated with respect to bits [28:21] of Device Size Configuration Register]
22:19	MSTR_BAUD_DIV_FLD	R/W	Fh	Initiator Mode Baud Rate Divisor: SPI baud rate = [initiator reference clock] baud_rate_divisor
18	ENTER_XIP_MODE_IMM_FLD	R/W	0h	Enter XIP Mode immediately: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : Operate the device in XIP mode immediately Use this register when the external device wakes up in XIP mode [as per the contents of its non- volatile configuration register]. The controller will assume the next READ instruction will be passed to the device as an XIP instruction, and therefore will not require the READ opcode to be transferred. Note: To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only after the next READ instruction is executed. Software therefore should ensure that at least one READ instruction is requested after resetting this bit in order to be sure that XIP mode is exited.
17	ENTER_XIP_MODE_FLD	R/W	0h	Enter XIP Mode on next READ: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : If XIP is disabled, then setting to ?1? will inform the controller that the device is ready to enter XIP on the next READ instruction. The controller will therefore send the appropriate command sequence, including mode bits to cause the device to enter XIP mode. Use this register after the controller has ensured the FLASH device has been configured to be ready to enter XIP mode. Note : To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only AFTER the next READ instruction is executed. Software should therefore ensure that at least one READ instruction is requested after resetting this bit before it can be sure XIP mode in the device is exited.
16	ENB_AHB_ADDR_REMAP_FLD	R/W	0h	Enable AHB Address Re-mapping: [Direct Access Mode Only] When set to 1, the incoming AHB address will be adapted and sent to the FLASH device as [address + N], where N is the value stored in the remap address register.
15	ENB_DMA_IF_FLD	R/W	0h	Enable DMA Peripheral Interface: Set to 1 to enable the DMA handshaking logic. When enabled the controller will trigger DMA transfer requests via the DMA peripheral interface. Set to 0 to disable
14	WR_PROT_FLASH_FLD	R/W	0h	Write Protect Flash Pin: Set to drive the Write Protect pin of the FLASH device. This is resynchronized to the generated memory clock as necessary.
13:10	PERIPH_CS_LINES_FLD	R/W	0h	Peripheral Chip Select Lines: Peripheral chip select lines If pdec = 0, ss[3:0] are output thus: ss[3:0] n_ss_out[3:0] xxx0 1110 xx01 1101 x011 1011 0111 0111 1111 1111 [no peripheral selected] else ss[3:0] directly drives n_ss_out[3:0]
9	PERIPH_SEL_DEC_FLD	R/W	0h	Peripheral select decode: 0 : only 1 of 4 selects n_ss_out[3:0] is active 1 : allow external 4-to-16 decode [n_ss_out = ss]
8	ENB_LEGACY_IP_MODE_FLD	R/W	0h	Legacy IP Mode Enable: 0 : Use Direct Access Controller/Indirect Access Controller 1 : legacy Mode is enabled. In this mode, any write to the controller via the AHB interface is serialized and sent to the FLASH device. Any valid AHB read will pop the internal RX-FIFO, retrieving data that was forwarded by the external FLASH device on the SPI lines,4,2 or 1 byte transfers are permitted and controlled via the HSIZE input.
7	ENB_DIR_ACC_CTLR_FLD	R/W	1h	Enable Direct Access Controller: 0 : disable the Direct Access Controller once current transfer of the data word [FF_W] is complete. 1 : enable the Direct Access Controller When the Direct Access Controller and Indirect Access Controller are both disabled, all AHB requested are completed with an error response.

Table 14-12819. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESET_CFG_FLD	R/W	0h	RESET pin configuration: 0 = RESET feature on DQ3 pin of the device 1 = RESET feature on dedicated pin of the device [controlling of 5th bit influences on reset_out output]
5	RESET_PIN_FLD	R/W	0h	Set to drive the RESET pin of the FLASH device and reset for de-activation of the RESET pin feature
4	HOLD_PIN_FLD	R/W	0h	Set to drive the HOLD pin of the FLASH device and reset for de-activation of the HOLD pin feature
3	PHY_MODE_ENABLE_FLD	R/W	0h	PHY mode enable: When enabled, the controller is informed that PHY Module is to be used for handling SPI transfers. This bit is relevant only for configuration with PHY Module.
2	SEL_CLK_PHASE_FLD	R/W	0h	Select Clock Phase: Selects whether the clock is in an active or inactive phase outside the SPI word. 0 : the SPI clock is active outside the word 1 : the SPI clock is inactive outside the word
1	SEL_CLK_POL_FLD	R/W	0h	Clock polarity outside SPI word: 0 : the SPI clock is quiescent low 1 : the SPI clock is quiescent high
0	ENB_SPI_FLD	R/W	1h	Octal-SPI Enable: 0 : disable the Octal-SPI, once current transfer of the data word [FF_W] is complete. 1 : enable the Octal-SPI, when spi_enable = 0, all output enables are inactive and all pins are set to input mode.

14.7.4.3.2.18 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register

14.7.4.3.2.18.1 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register (Offset = 4h) [reset = 3h]

Device Read Instruction Configuration Register

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Table 14-12820. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0004h

Figure 14-6328. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RD_INSTR_RESV5_FLD			DUMMY_RD_CLK_CYCLES_FLD				
R			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_INSTR_RESV4_FLD			MODE_BIT_ENABLE_FLD	RD_INSTR_RESV3_FLD		DATA_XFER_TYPE_EXT_MODE_FLD	
R			R/W	R		R/W	
0h			0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_INSTR_RESV2_FLD		ADDR_XFER_TYPE_STD_MODE_FLD		RD_INSTR_RESV1_FLD	DDR_EN_FLD	INSTR_TYPE_FLD	
R		R/W		R	R/W	R/W	
0h		0h		0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RD_OPCODE_NON_XIP_FLD							
R/W							
3h							

Table 14-12821. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RD_INSTR_RESV5_FLD	R	0h	Reserved
28:24	DUMMY_RD_CLK_CYCLES_FLD	R/W	0h	Dummy Read Clock Cycles: Number of dummy clock cycles required by device for read instruction.
23:21	RD_INSTR_RESV4_FLD	R	0h	Reserved
20	MODE_BIT_ENABLE_FLD	R/W	0h	Mode Bit Enable: Set this field to 1 to ensure that the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
19:18	RD_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	RD_INSTR_RESV2_FLD	R	0h	Reserved
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11	RD_INSTR_RESV1_FLD	R	0h	Reserved

Table 14-12821. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DDR_EN_FLD	R/W	0h	DDR Enable: This is to inform that opcode from rd_opcode_non_xip_fld is compliant with one of the DDR READ Commands
9:8	INSTR_TYPE_FLD	R/W	0h	Instruction Type: 0 : Use Standard SPI mode [instruction always shifted into the device on DQ0 only] 1 : Use DIO-SPI mode [Instructions, Address and Data always sent on DQ0 and DQ1] 2 : Use QIO-SPI mode [Instructions, Address and Data always sent on DQ0, DQ1, DQ2 and DQ3] 3 : Use Octal-IO-SPI mode [Instructions, Address and Data always sent on DQ[7:0]]
7:0	RD_OPCODE_NON_XIP_FLD	R/W	3h	Read Opcode in non-XIP mode: Read Opcode to use when not in XIP mode

14.7.4.3.2.19 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register

14.7.4.3.2.19.1 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register (Offset = 8h) [reset = 2h]

Device Write Instruction Configuration Register

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Table 14-12822. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0008h

Figure 14-6329. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">WR_INSTR_RESV4_FLD</td><td colspan="5">DUMMY_WR_CLK_CYCLES_FLD</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WR_INSTR_RESV3_FLD</td><td colspan="2">DATA_XFER_TYPE_EXT_MODE_FLD</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">WR_INSTR_RESV2_FLD</td><td colspan="2">ADDR_XFER_TYPE_STD_MODE_FLD</td><td colspan="3">WR_INSTR_RESV1_FLD</td><td>WEL_DIS_FLD</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WR_OPCODE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-12823. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	WR_INSTR_RESV4_FLD	R	0h	Reserved
28:24	DUMMY_WR_CLK_CYCLES_FLD	R/W	0h	Dummy Write Clock Cycles: Number of dummy clock cycles required by device for write instruction.
23:18	WR_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	WR_INSTR_RESV2_FLD	R	0h	Reserved
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11:9	WR_INSTR_RESV1_FLD	R	0h	Reserved
8	WEL_DIS_FLD	R/W	0h	WEL Disable: This is to turn off automatic issuing of WEL Command before write operation for DAC or INDAC
7:0	WR_OPCODE_FLD	R/W	2h	Write Opcode

14.7.4.3.2.20 OSPI_FLASH_CFG_DEV_DELAY_REG Register

14.7.4.3.2.20.1 OSPI_FLASH_CFG_DEV_DELAY_REG Register (Offset = Ch) [reset = 0h]

Octal-SPI Device Delay Register: This register is used to introduce relative delays into the generation of the master output signals. All timings are defined in cycles of the SPI REFERENCE CLOCK/ext_clk, defined in this table as SPI master ref clock.

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Table 14-12824. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 000Ch

Figure 14-6330. OSPI_FLASH_CFG_DEV_DELAY_REG Name Register

31	30	29	28	27	26	25	24
D_NSS_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
D_BTWN_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
D_AFTER_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
D_INIT_FLD							
R/W							
0h							

Table 14-12825. OSPI_FLASH_CFG_DEV_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	D_NSS_FLD	R/W	0h	Clock Delay for Chip Select Deassert: Delay in initiator reference clocks for the length that the initiator mode chip select outputs are de-asserted between transactions. The minimum delay is always SCLK period to ensure the chip select is never re-asserted within an SCLK period.
23:16	D_BTWN_FLD	R/W	0h	Clock Delay for Chip Select Deactivation: Delay in initiator reference clocks between one chip select being de-activated and the activation of another. This is used to ensure a quiet period between the selection of two different targets and requires the transmit FIFO to be empty.
15:8	D_AFTER_FLD	R/W	0h	Clock Delay for Last Transaction Bit: Delay in initiator reference clocks between last bit of current transaction and deasserting the device chip select [n_ss_out]. By default, the chip select will be deasserted on the cycle following the completion of the current transaction.
7:0	D_INIT_FLD	R/W	0h	Clock Delay with n_ss_out: Delay in initiator reference clocks between setting n_ss_out low and first bit transfer.

14.7.4.3.2.21 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register

14.7.4.3.2.21.1 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register (Offset = 10h) [reset = 1h]

Read Data Capture Register

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Table 14-12826. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0010h

Figure 14-6331. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RD_DATA_RESV3_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RD_DATA_RESV3_FLD</td><td colspan="4">DDR_READ_DELAY_FLD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RD_DATA_RESV2_FLD</td><td>DQS_ENABLE_FLD</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RD_DATA_RESV1_FLD</td><td>SAMPLE_EDGE_SEL_FLD</td><td colspan="4">DELAY_FLD</td><td>BYPASS_FLD</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>1h</td></tr>
</table>

Table 14-12827. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RD_DATA_RESV3_FLD	R	0h	Reserved
19:16	DDR_READ_DELAY_FLD	R/W	0h	DDR read delay: Delay the transmitted data by the programmed number of ref_clk cycles.This field is only relevant when DDR Read Command is executed. Otherwise can be ignored.
15:9	RD_DATA_RESV2_FLD	R	0h	Reserved
8	DQS_ENABLE_FLD	R/W	0h	DQS enable bit: If enabled, signal from DQS input is driven into RX DLL and is used for data capturing in PHY Mode rather than internally generated gated ref_clk..
7:6	RD_DATA_RESV1_FLD	R	0h	Reserved
5	SAMPLE_EDGE_SEL_FLD	R/W	0h	Sample edge selection: Choose edge on which data outputs from flash memory will be sampled
4:1	DELAY_FLD	R/W	0h	Read Delay: Delay the read data capturing logic by the programmed number of ref_clk cycles
0	BYPASS_FLD	R/W	1h	Bypass the adapted loopback clock circuit

14.7.4.3.2.22 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register

14.7.4.3.2.22.1 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register (Offset = 14h) [reset = 101002h]

Device Size Configuration Register

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Table 14-12828. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0014h

Figure 14-6332. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DEV_SIZE_RESV_FLD			MEM_SIZE_ON_CS3_FLD		MEM_SIZE_ON_CS2_FLD		MEM_SIZE_ON_CS1_FLD
R			R/W		R/W		R/W
0h			0h		0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MEM_SIZE_ON_CS1_FLD	MEM_SIZE_ON_CS0_FLD		BYTES_PER_SUBSECTOR_FLD				
R/W	R/W		R/W				
0h	0h		10h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BYTES_PER_DEVICE_PAGE_FLD							
R/W							
100h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BYTES_PER_DEVICE_PAGE_FLD				NUM_ADDR_BYTES_FLD			
R/W				R/W			
100h				2h			

Table 14-12829. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	DEV_SIZE_RESV_FLD	R	0h	Reserved
28:27	MEM_SIZE_ON_CS3_FLD	R/W	0h	Size of Flash Device connected to CS[3] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
26:25	MEM_SIZE_ON_CS2_FLD	R/W	0h	Size of Flash Device connected to CS[2] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
24:23	MEM_SIZE_ON_CS1_FLD	R/W	0h	Size of Flash Device connected to CS[1] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
22:21	MEM_SIZE_ON_CS0_FLD	R/W	0h	Size of Flash Device connected to CS[0] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb.
20:16	BYTES_PER_SUBSECTOR_FLD	R/W	10h	Number of bytes per Block. This is required by the controller for performing the write protection logic. The number of bytes per block must be a power of 2 number.
15:4	BYTES_PER_DEVICE_PAGE_FLD	R/W	100h	Number of bytes per device page. This is required by the controller for performing FLASH writes up to and across page boundaries.
3:0	NUM_ADDR_BYTES_FLD	R/W	2h	Number of address bytes. A value of 0 indicates 1 byte.

14.7.4.3.2.23 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register

14.7.4.3.2.23.1 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register (Offset = 18h) [reset = 80h]

SRAM Partition Configuration Register

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Table 14-12830. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0018h

Figure 14-6333. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Name Register

31	30	29	28	27	26	25	24
SRAM_PARTITION_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_PARTITION_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_PARTITION_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
80h							

Table 14-12831. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	SRAM_PARTITION_RESV_FLD	R	0h	Reserved
7:0	ADDR_FLD	R/W	80h	Indirect Read Partition Size: Defines the size of the indirect read partition in the SRAM, in units of SRAM locations. By default, half of the SRAM is reserved for indirect read operation, and half for indirect write. The size of this register will scale with the depth of the SRAM.

14.7.4.3.2.24 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register

14.7.4.3.2.24.1 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register (Offset = 1Ch) [reset = 0h]

Indirect AHB Address Trigger Register

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Table 14-12832. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 001Ch

Figure 14-6334. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-12833. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the base address that will be used by the AHB controller. When the incoming AHB read access address matches a range of addresses from this trigger address to the trigger address + 15, then the AHB request will be completed by fetching data from the Indirect Controllers SRAM.

14.7.4.3.2.25 OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register

14.7.4.3.2.25.1 OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register (Offset = 20h) [reset = 0h]

DMA Peripheral Configuration Register

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Table 14-12834. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0020h

Figure 14-6335. OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DMA_PERIPH_RESV2_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DMA_PERIPH_RESV2_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DMA_PERIPH_RESV2_FLD				NUM_BURST_REQ_BYTES_FLD			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DMA_PERIPH_RESV1_FLD				NUM_SINGLE_REQ_BYTES_FLD			
R				R/W			
0h				0h			

Table 14-12835. OSPI_FLASH_CFG_DMA_PERIPH_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	DMA_PERIPH_RESV2_FLD	R	0h	Reserved
11:8	NUM_BURST_REQ_BYTES_FLD	R/W	0h	Number of Burst Bytes: Number of bytes in a burst type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.
7:4	DMA_PERIPH_RESV1_FLD	R	0h	Reserved
3:0	NUM_SINGLE_REQ_BYTES_FLD	R/W	0h	Number of Single Bytes: Number of bytes in a single type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.

14.7.4.3.2.26 OSPI_FLASH_CFG_REMAP_ADDR_REG Register

14.7.4.3.2.26.1 OSPI_FLASH_CFG_REMAP_ADDR_REG Register (Offset = 24h) [reset = 0h]

Remap Address Register

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Table 14-12836. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0024h

Figure 14-6336. OSPI_FLASH_CFG_REMAP_ADDR_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-12837. OSPI_FLASH_CFG_REMAP_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This register is used to remap an incoming AHB address to a different address used by the FLASH device.

14.7.4.3.2.27 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register

14.7.4.3.2.27.1 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register (Offset = 28h) [reset = 200h]

Mode Bit Configuration Register

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Table 14-12838. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0028h

Figure 14-6337. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RX_CRC_DATA_LOW_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RX_CRC_DATA_UP_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CRC_OUT_ENABLE_FLD</td><td colspan="4">MODE_BIT_RESV1_FLD</td><td colspan="3">CHUNK_SIZE_FLD</td></tr>
<tr><td>R/W</td><td colspan="4">R</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MODE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12839. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RX_CRC_DATA_LOW_FLD	R	0h	RX CRC data [lower] The first CRC byte returned after RX data chunk.
23:16	RX_CRC_DATA_UP_FLD	R	0h	RX CRC data [upper] The second CRC byte returned after RX data chunk.
15	CRC_OUT_ENABLE_FLD	R/W	0h	CRC# output enable bit When enabled, the controller expects the Flash Device to toggle CRC data on both SPI clock edges in CRC->CRC# sequence and calculates CRC compliance accordingly.
14:11	MODE_BIT_RESV1_FLD	R	0h	Reserved
10:8	CHUNK_SIZE_FLD	R/W	2h	It defines size of chunk after which CRC data is expected to show up on the SPI interface for write and read data transfers.
7:0	MODE_FLD	R/W	0h	These are the 8 mode bits that are sent to the device following the address bytes if mode bit transmission has been enabled.

14.7.4.3.2.28 OSPI_FLASH_CFG_SRAM_FILL_REG Register

14.7.4.3.2.28.1 OSPI_FLASH_CFG_SRAM_FILL_REG Register (Offset = 2Ch) [reset = 0h]

SRAM Fill Register

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Table 14-12840. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 002Ch

Figure 14-6338. OSPI_FLASH_CFG_SRAM_FILL_REG Name Register

31	30	29	28	27	26	25	24
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_FILL_INDAC_READ_FLD							
R							
0h							
7	6	5	4	3	2	1	0
SRAM_FILL_INDAC_READ_FLD							
R							
0h							

Table 14-12841. OSPI_FLASH_CFG_SRAM_FILL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SRAM_FILL_INDAC_WRITE_FLD	R	0h	SRAM Fill Level [Indirect Write Partition]: Identifies the current fill level of the SRAM Indirect Write partition
15:0	SRAM_FILL_INDAC_READ_FLD	R	0h	SRAM Fill Level [Indirect Read Partition]: Identifies the current fill level of the SRAM Indirect Read partition

14.7.4.3.2.29 OSPI_FLASH_CFG_TX_THRESH_REG Register

14.7.4.3.2.29.1 OSPI_FLASH_CFG_TX_THRESH_REG Register (Offset = 30h) [reset = 1h]

TX Threshold Register

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Table 14-12842. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0030h

Figure 14-6339. OSPI_FLASH_CFG_TX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
TX_THRESH_RESV_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_THRESH_RESV_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TX_THRESH_RESV_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 14-12843. OSPI_FLASH_CFG_TX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	TX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small TX FIFO not full interrupt is generated

14.7.4.3.2.30 OSPI_FLASH_CFG_RX_THRESH_REG Register

14.7.4.3.2.30.1 OSPI_FLASH_CFG_RX_THRESH_REG Register (Offset = 34h) [reset = 1h]

RX Threshold Register

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Table 14-12844. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0034h

Figure 14-6340. OSPI_FLASH_CFG_RX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
RX_THRESH_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
RX_THRESH_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
RX_THRESH_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
RX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 14-12845. OSPI_FLASH_CFG_RX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small RX FIFO not empty interrupt is generated

14.7.4.3.2.31 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register

14.7.4.3.2.31.1 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register (Offset = 38h) [reset = 10005h]

Write Completion Control Register: This register defines how the controller will poll the device following a write transfer

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Table 14-12846. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0038h

Figure 14-6341. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">POLL_REP_DELAY_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">POLL_COUNT_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>ENABLE_POLLING_EXP_FLD</td><td>DISABLE_POLLING_FLD</td><td>POLLING_POLARITY_FLD</td><td colspan="2">WR_COMP_CTRL_RESV1_FLD</td><td colspan="3">POLLING_BIT_INDEX_FLD</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OPCODE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">5h</td></tr>
</table>

Table 14-12847. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	POLL_REP_DELAY_FLD	R/W	0h	Defines additional delay for maintain Chip Select de-asserted during auto-polling phase
23:16	POLL_COUNT_FLD	R/W	1h	Defines the number of times the controller should expect to see a true result from the polling in successive reads of the device register.
15	ENABLE_POLLING_EXP_FLD	R/W	0h	Set to '1' for enabling auto-polling expiration.
14	DISABLE_POLLING_FLD	R/W	0h	This switches off the automatic polling function
13	POLLING_POLARITY_FLD	R/W	0h	Defines the polling polarity. If '1', then the write transfer to the device will be complete if the polled bit is equal to '1'. If '0', then the write transfer to the device will be complete if the polled bit is equal to '0'.
12:11	WR_COMP_CTRL_RESV1_FLD	R	0h	Reserved
10:8	POLLING_BIT_INDEX_FLD	R/W	0h	Defines the bit index that should be polled. A value of 010 means that bit 2 of the returned data will be polled for.A value of 111 means that bit 7 of the returned data will be polled for.
7:0	OPCODE_FLD	R/W	5h	Defines the opcode that should be issued by the controller when it is automatically polling for device program completion. This command is issued followed all device write operations. By default, this will poll the standard device STATUS register using opcode 0x05

14.7.4.3.2.32 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register

14.7.4.3.2.32.1 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register (Offset = 3Ch) [reset = FFFFFFFFh]

Polling Expiration Register

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Table 14-12848. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 003Ch

Figure 14-6342. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Name Register

31	30	29	28	27	26	25	24
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							

Table 14-12849. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NO_OF_POLLS_BEF_EXP_FLD	R/W	FFFFFFFFh	Number of polls cycles before expiration

14.7.4.3.2.33 OSPI_FLASH_CFG_IRQ_STATUS_REG Register

14.7.4.3.2.33.1 OSPI_FLASH_CFG_IRQ_STATUS_REG Register (Offset = 40h) [reset = 0h]

Interrupt Status Register: The status fields in this register are set when the described event occurs and the interrupt is enabled in the mask register. When any of these bit fields are set, the interrupt output is asserted high. The fields are each cleared by writing a 1 to the field. Note that bit fields 6 thru 10 are only valid when legacy SPI mode is active.

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Table 14-12850. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0040h

Figure 14-6343. OSPI_FLASH_CFG_IRQ_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IRQ_STAT_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_STAT_RESV_FLD				ECC_FAIL_FLD	TX_CRC_CHUNK_BRK_FLD	RX_CRC_DATA_VAL_FLD	RX_CRC_DATA_ERR_FLD
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_STAT_RESV1_FLD	STIG_REQ_INT_FLD	POLL_EXP_INT_FLD	INDRD_SRAM_FULL_FLD	RX_FIFO_FULL_FLD	RX_FIFO_NOT_EMPTY_FLD	TX_FIFO_FULL_FLD	TX_FIFO_NOT_FULL_FLD
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_FLD	INDIRECT_XFER_LEVEL_BREACH_FLD	ILLEGAL_ACCESS_DET_FLD	PROT_WR_ATTEMPT_FLD	INDIRECT_READ_REJECT_FLD	INDIRECT_OP_DONE_FLD	UNDERFLOW_DET_FLD	MODE_M_FAIL_FLD
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12851. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_STAT_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_FLD	R/W1TC	0h	ECC failure This interrupt informs the system that Flash Device reported ECC error.
18	TX_CRC_CHUNK_BRK_FLD	R/W1TC	0h	TX CRC chunk was broken This interrupt informs the system that program page SPI transfer was discontinued somewhere inside the chunk.
17	RX_CRC_DATA_VAL_FLD	R/W1TC	0h	RX CRC data valid New RX CRC data was captured from Flash Device
16	RX_CRC_DATA_ERR_FLD	R/W1TC	0h	RX CRC data error CRC data from Flash Device does not correspond to the one dynamically calculated by the controller.
15	IRQ_STAT_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_INT_FLD	R/W1TC	0h	The controller is ready for getting another STIG request.
13	POLL_EXP_INT_FLD	R/W1TC	0h	The maximum number of programmed polls cycles is expired
12	INDRD_SRAM_FULL_FLD	R/W1TC	0h	Indirect Read Partition overflow: Indirect Read Partition of SRAM is full and unable to immediately complete indirect operation

Table 14-12851. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_FIFO_FULL_FLD	R/W1TC	0h	Small RX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full 1 : FIFO is full
10	RX_FIFO_NOT_EMPTY_FLD	R/W1TC	0h	Small RX FIFO not empty: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has less than RX THRESHOLD entries, 1 : FIFO has >= THRESHOLD entries
9	TX_FIFO_FULL_FLD	R/W1TC	0h	Small TX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full, 1 : FIFO is full
8	TX_FIFO_NOT_FULL_FLD	R/W1TC	0h	Small TX FIFO not full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has >= THRESHOLD entries, 1 : FIFO has less than THRESHOLD entries
7	RECV_OVERFLOW_FLD	R/W1TC	0h	Receive Overflow: This should only occur in Legacy SPI mode. Set if an attempt is made to push the RX FIFO when it is full. This bit is reset only by a system reset and cleared only when this register is read. If a new push to the RX FIFO occurs coincident with a register read this flag will remain set. 0 : no overflow has been detected. 1 : an overflow has occurred.
6	INDIRECT_XFER_LEVEL_BREACH_FLD	R/W1TC	0h	Indirect Transfer Watermark Level Breached
5	ILLEGAL_ACCESS_DET_FLD	R/W1TC	0h	Illegal AHB access has been detected. AHB wrapping bursts and the use of SPLIT/RETRY accesses will cause this error interrupt to trigger.
4	PROT_WR_ATTEMPT_FLD	R/W1TC	0h	Write to protected area was attempted and rejected.
3	INDIRECT_READ_REJECT_FLD	R/W1TC	0h	Indirect operation was requested but could not be accepted. Two indirect operations already in storage.
2	INDIRECT_OP_DONE_FLD	R/W1TC	0h	Indirect Operation Complete: Controller has completed last triggered indirect operation
1	UNDERFLOW_DET_FLD	R/W1TC	0h	Underflow Detected: 0 : no underflow has been detected 1 : underflow is detected and an attempt to transfer data is made when the small TX FIFO is empty. This may occur when AHB write data is being supplied too slowly to keep up with the requested write operation This bit is reset only by a system reset and cleared only when the register is read.
0	MODE_M_FAIL_FLD	R/W1TC	0h	Mode M Failure: Mode M failure indicates the voltage on pin n_ss_in is inconsistent with the SPI mode. Set =1 if n_ss_in is low in initiator mode [multi-initiator contention]. These conditions will clear the spi_enable bit and disable the SPI. This bit is reset only by a system reset and cleared only when this register is read. 0 : no mode fault has been detected 1 : a mode fault has occurred

14.7.4.3.2.34 OSPI_FLASH_CFG_IRQ_MASK_REG Register

14.7.4.3.2.34.1 OSPI_FLASH_CFG_IRQ_MASK_REG Register (Offset = 44h) [reset = 0h]

Interrupt Mask: 0 : the interrupt for the corresponding interrupt status register bit is disabled. 1 : the interrupt for the corresponding interrupt status register bit is enabled.

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Table 14-12852. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0044h

Figure 14-6344. OSPI_FLASH_CFG_IRQ_MASK_REG Name Register

31	30	29	28	27	26	25	24
IRQ_MASK_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_MASK_RESV_FLD				ECC_FAIL_MASK_FLD	TX_CRC_CHUNK_BRK_MASK_FLD	RX_CRC_DATA_VAL_MASK_FLD	RX_CRC_DATA_ERR_MASK_FLD
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_MASK_RESV1_FLD	STIG_REQ_MASK_FLD	POLL_EXP_INT_MASK_FLD	INDRD_SRAM_FULL_MASK_FLD	RX_FIFO_FULL_MASK_FLD	RX_FIFO_NOT_EMPTY_MASK_FLD	TX_FIFO_FULL_MASK_FLD	TX_FIFO_NOT_FULL_MASK_FLD
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_MASK_FLD	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	ILLEGAL_ACCESS_DET_MASK_FLD	PROT_WR_ATTEMPT_MASK_FLD	INDIRECT_READ_REJECT_MASK_FLD	INDIRECT_OP_DONE_MASK_FLD	UNDERFLOW_DET_MASK_FLD	MODE_M_FAIL_MASK_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12853. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_MASK_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_MASK_FLD	R/W	0h	ECC failure Mask
18	TX_CRC_CHUNK_BRK_MASK_FLD	R/W	0h	TX CRC chunk was broken Mask
17	RX_CRC_DATA_VAL_MASK_FLD	R/W	0h	RX CRC data valid Mask
16	RX_CRC_DATA_ERR_MASK_FLD	R/W	0h	RX CRC data error Mask
15	IRQ_MASK_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_MASK_FLD	R/W	0h	STIG request completion Mask
13	POLL_EXP_INT_MASK_FLD	R/W	0h	Polling expiration detected Mask
12	INDRD_SRAM_FULL_MASK_FLD	R/W	0h	Indirect Read Partition overflow mask
11	RX_FIFO_FULL_MASK_FLD	R/W	0h	Small RX FIFO full Mask

Table 14-12853. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_FIFO_NOT_EMPTY_MASK_FLD	R/W	0h	Small RX FIFO not empty Mask
9	TX_FIFO_FULL_MASK_FLD	R/W	0h	Small TX FIFO full Mask
8	TX_FIFO_NOT_FULL_MASK_FLD	R/W	0h	Small TX FIFO not full Mask
7	RECV_OVERFLOW_MASK_FLD	R/W	0h	Receive Overflow Mask
6	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	R/W	0h	Transfer Watermark Breach Mask
5	ILLEGAL_ACCESS_DET_MASK_FLD	R/W	0h	Illegal Access Detected Mask
4	PROT_WR_ATTEMPT_MASK_FLD	R/W	0h	Protected Area Write Attempt Mask
3	INDIRECT_READ_REJECT_MASK_FLD	R/W	0h	Indirect Read Reject Mask
2	INDIRECT_OP_DONE_MASK_FLD	R/W	0h	Indirect Complete Mask
1	UNDERFLOW_DET_MASK_FLD	R/W	0h	Underflow Detected Mask
0	MODE_M_FAIL_MASK_FLD	R/W	0h	Mode M Failure Mask

14.7.4.3.2.35 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register

14.7.4.3.2.35.1 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register (Offset = 50h) [reset = 0h]

Lower Write Protection Register

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Table 14-12854. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0050h

Figure 14-6345. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 14-12855. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the lower block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

14.7.4.3.2.36 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register

14.7.4.3.2.36.1 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register (Offset = 54h) [reset = 0h]

Upper Write Protection Register

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Table 14-12856. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0054h

Figure 14-6346. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 14-12857. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the upper block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

14.7.4.3.2.37 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register

14.7.4.3.2.37.1 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register (Offset = 58h) [reset = 0h]

Write Protection Control Register

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Table 14-12858. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0058h

Figure 14-6347. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Name Register

31	30	29	28	27	26	25	24
WR_PROT_CTRL_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
WR_PROT_CTRL_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
WR_PROT_CTRL_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
WR_PROT_CTRL_RESV_FLD						ENB_FLD	INV_FLD
R						R/W	R/W
0h						0h	0h

Table 14-12859. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	WR_PROT_CTRL_RESV_FLD	R	0h	Reserved
1	ENB_FLD	R/W	0h	Write Protection Enable Bit: When set to 1, any AHB write access with an address within the protection region defined in the lower and upper write protection registers is rejected. An AHB error response is generated and an interrupt source triggered. When set to 0, the protection region is disabled.
0	INV_FLD	R/W	0h	Write Protection Inversion Bit: When set to 1, the protection region defined in the lower and upper write protection registers is inverted meaning it is the region that the system is permitted to write to. When set to 0, the protection region defined in the lower and upper write protection registers is the region that the system is not permitted to write to.

14.7.4.3.2.38 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register

14.7.4.3.2.38.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register (Offset = 60h) [reset = 0h]

Indirect Read Transfer Control Register

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Table 14-12860. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0060h

Figure 14-6348. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_RD_XFER_RESV_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INDIR_RD_XFER_RESV_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INDIR_RD_XFER_RESV_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	RD_QUEUED_FLD	SRAM_FULL_FLD	RD_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R/W1TC	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 14-12861. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_RD_XFER_RESV_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	RD_QUEUED_FLD	R	0h	Two indirect read operations have been queued
3	SRAM_FULL_FLD	R/W1TC	0h	SRAM Full: SRAM full and unable to immediately complete an indirect operation. Write a 1 to this field to clear it.; indirect operation [status]
2	RD_STATUS_FLD	R	0h	Indirect Read Status: Indirect read operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Read: Writing a 1 to this bit will cancel all ongoing indirect read operations.
0	START_FLD	W	0h	Start Indirect Read: Writing a 1 to this bit will trigger an indirect read operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect read operation.

14.7.4.3.2.39 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register

14.7.4.3.2.39.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register (Offset = 64h) [reset = 0h]

Indirect Read Transfer Watermark Register

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Table 14-12862. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0064h

Figure 14-6349. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
0h							

Table 14-12863. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	0h	Watermark Value: This represents the minimum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level passes the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all zeroes.

14.7.4.3.2.40 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register

14.7.4.3.2.40.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register (Offset = 68h) [reset = 0h]

Indirect Read Transfer Start Address Register

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Table 14-12864. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0068h

Figure 14-6350. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADDR_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADDR_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ADDR_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADDR_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12865. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the start address from which the indirect access will commence its READ operation.

14.7.4.3.2.41 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register

14.7.4.3.2.41.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register (Offset = 6Ch) [reset = 0h]

Indirect Read Transfer Number Bytes Register

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Table 14-12866. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 006Ch

Figure 14-6351. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-12867. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.7.4.3.2.42 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register

14.7.4.3.2.42.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register (Offset = 70h) [reset = 0h]

Indirect Write Transfer Control Register

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Table 14-12868. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0070h

Figure 14-6352. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
23	22	21	20	19	18	17	16
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
15	14	13	12	11	10	9	8
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
7	6	5	4	3	2	1	0
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	WR_QUEUED_FLD	INDIR_WR_XFER_RESV1_FLD	WR_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 14-12869. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_WR_XFER_RESV2_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	WR_QUEUED_FLD	R	0h	Two indirect write operations have been queued
3	INDIR_WR_XFER_RESV1_FLD	R	0h	Reserved
2	WR_STATUS_FLD	R	0h	Indirect Write Status: Indirect write operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Write: Writing a 1 to this bit will cancel all ongoing indirect write operations.
0	START_FLD	W	0h	Start Indirect Write: Writing a 1 to this bit will trigger an indirect write operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect write operation.

14.7.4.3.2.43 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register

14.7.4.3.2.43.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register (Offset = 74h) [reset = FFFFFFFFh]

Indirect Write Transfer Watermark Register

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Table 14-12870. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0074h

Figure 14-6353. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
FFFFFFFFh							

Table 14-12871. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	FFFFFFFFh	Watermark Value: This represents the maximum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level falls below the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all ones.

14.7.4.3.2.44 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register

14.7.4.3.2.44.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register (Offset = 78h) [reset = 0h]

Indirect Write Transfer Start Address Register

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Table 14-12872. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0078h

Figure 14-6354. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-12873. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Start of Indirect Access: This is the start address from which the indirect access will commence its READ operation.

14.7.4.3.2.45 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register

14.7.4.3.2.45.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register (Offset = 7Ch) [reset = 0h]

Indirect Write Transfer Number Bytes Register

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Table 14-12874. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 007Ch

Figure 14-6355. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 14-12875. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	Indirect Number of Bytes: This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.7.4.3.2.46 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register

14.7.4.3.2.46.1 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register (Offset = 80h) [reset = 4h]

Indirect Trigger Address Range Register

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Table 14-12876. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0080h

Figure 14-6356. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">IND_RANGE_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">IND_RANGE_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">IND_RANGE_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">IND_RANGE_RESV1_FLD</td><td colspan="4">IND_RANGE_WIDTH_FLD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-12877. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IND_RANGE_RESV1_FLD	R	0h	Reserved
3:0	IND_RANGE_WIDTH_FLD	R/W	4h	This is the address offset of Indirect Trigger Address Register.

14.7.4.3.2.47 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register

14.7.4.3.2.47.1 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register (Offset = 8Ch) [reset = 0h]

Flash Command Control Memory Register

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Table 14-12878. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 008Ch

Figure 14-6357. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">FLASH_COMMAND_CTRL_MEM_RESV1_FLD</td><td colspan="5">MEM_BANK_ADDR_FLD</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">MEM_BANK_ADDR_FLD</td><td>FLASH_COMMAND_CTRL_MEM_RESV2_FLD</td><td colspan="3">NB_OF_STIG_READ_BYTES_FLD</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MEM_BANK_READ_DATA_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">FLASH_COMMAND_CTRL_MEM_RESV3_FLD</td><td>MEM_BANK_REQ_IN_PROGRESS_FLD</td><td>TRIGGER_MEM_BANK_REQ_FLD</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12879. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	FLASH_COMMAND_CTRL_MEM_RESV1_FLD	R	0h	Reserved
28:20	MEM_BANK_ADDR_FLD	R/W	0h	The address of the Memory Bank which data will be read from.
19	FLASH_COMMAND_CTRL_MEM_RESV2_FLD	R	0h	Reserved
18:16	NB_OF_STIG_READ_BYTES_FLD	R/W	0h	It defines the number of read bytes for the extended STIG.
15:8	MEM_BANK_READ_DATA_FLD	R	0h	Last requested data from the STIG Memory Bank.
7:2	FLASH_COMMAND_CTRL_MEM_RESV3_FLD	R	0h	Reserved
1	MEM_BANK_REQ_IN_PROGRESS_FLD	R	0h	Memory Bank data request in progress.
0	TRIGGER_MEM_BANK_REQ_FLD	W	0h	Trigger the Memory Bank data request.

14.7.4.3.2.48 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register

14.7.4.3.2.48.1 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register (Offset = 90h) [reset = 0h]

Flash Command Control Register

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Table 14-12880. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0090h

Figure 14-6358. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Name Register

31	30	29	28	27	26	25	24
CMD_OPCODE_FLD							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ENB_READ_DATA_FLD	NUM_RD_DATA_BYTES_FLD			ENB_COMD_ADDR_FLD	ENB_MODE_BIT_FLD	NUM_ADDR_BYTES_FLD	
R/W	R/W			R/W	R/W	R/W	
0h	0h			0h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENB_WRITE_DATA_FLD	NUM_WR_DATA_BYTES_FLD			NUM_DUMMY_CYCLES_FLD			
R/W	R/W			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_DUMMY_CYCLES_FLD	FLASH_CMD_CTRL_RESV1_FLD				STIG_MEM_BANK_EN_FLD	CMD_EXEC_STATUS_FLD	CMD_EXEC_FLD
R/W	R				R/W	R	W
0h	0h				0h	0h	0h

Table 14-12881. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CMD_OPCODE_FLD	R/W	0h	Command Opcode: The command opcode field should be setup before triggering the command. For example, 0x20 maps to SubSector Erase. Writing to the execute field [bit 0] of this register launches the command. NOTE : Using this approach to issue commands to the device will make use of the instruction type of the device instruction configuration register. If this field is set to 2'b00, then the command opcode, command address, command dummy bytes and command data will all be transferred in a serial fashion. If this field is set to 2'b01, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0 and DQ1 pins. If this field is set to 2'b10, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0, DQ1, DQ2 and DQ3 pins.
23	ENB_READ_DATA_FLD	R/W	0h	Read Data Enable: Set to 1 if the command specified in the command opcode field [bits 31:24] requires read data bytes to be received from the device.
22:20	NUM_RD_DATA_BYTES_FLD	R/W	0h	Number of Read Data Bytes: Up to 8 data bytes may be read using this command. Set to 0 for 1 byte and 7 for 8 bytes.
19	ENB_COMD_ADDR_FLD	R/W	0h	Command Address Enable: Set to 1 if the command specified in bits 31:24 requires an address. This should be setup before triggering the command via Writing a 1 to the execute field.

Table 14-12881. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	ENB_MODE_BIT_FLD	R/W	0h	Mode Bit Enable: Set to 1 to ensure the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
17:16	NUM_ADDR_BYTES_FLD	R/W	0h	Number of Address Bytes: Set to the number of address bytes required [the address itself is programmed in the FLASH COMMAND ADDRESS REGISTERS]. This should be setup before triggering the command via bit 0 of this register. 2'b00 : 1 address byte 2'b01 : 2 address bytes 2'b10 : 3 address bytes 2'b11 : 4 address bytes
15	ENB_WRITE_DATA_FLD	R/W	0h	Write Data Enable: Set to 1 if the command specified in the command opcode field requires write data bytes to be sent to the device.
14:12	NUM_WR_DATA_BYTES_FLD	R/W	0h	Number of Write Data Bytes: Up to 8 Data bytes may be written using this command Set to 0 for 1 byte, 7 for 8 bytes.
11:7	NUM_DUMMY_CYCLES_FLD	R/W	0h	Number of Dummy cycles: Set to the number of dummy cycles required. This should be setup before triggering the command via the execute field of this register.
6:3	FLASH_CMD_CTRL_RESV1_FLD	R	0h	Reserved
2	STIG_MEM_BANK_EN_FLD	R/W	0h	STIG Memory Bank enable bit.
1	CMD_EXEC_STATUS_FLD	R	0h	Command execution in progress.
0	CMD_EXEC_FLD	W	0h	Execute the command.

14.7.4.3.2.49 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register

14.7.4.3.2.49.1 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register (Offset = 94h) [reset = 0h]

Flash Command Address Register

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Table 14-12882. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 0094h

Figure 14-6359. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 14-12883. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Command Address: This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the address used by the command specified in the opcode field [bits 31:24] of the Flash Command Control register.

14.7.4.3.2.50 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register

14.7.4.3.2.50.1 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register (Offset = A0h) [reset = 0h]

Flash Command Read Data Register (Lower)

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Table 14-12884. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00A0h

Figure 14-6360. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R							
0h							

Table 14-12885. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the flash device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.7.4.3.2.51 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register

14.7.4.3.2.51.1 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register (Offset = A4h) [reset = 0h]

Flash Command Read Data Register (Upper)

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Table 14-12886. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00A4h

Figure 14-6361. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R							
0h							

Table 14-12887. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the FLASH device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.7.4.3.2.52 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register

14.7.4.3.2.52.1 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register (Offset = A8h) [reset = 0h]

Flash Command Write Data Register (Lower)

Return to Summary Table

Table 14-12888. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00A8h

Figure 14-6362. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 14-12889. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Lower Byte: This is the command write data lower byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

14.7.4.3.2.53 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register

14.7.4.3.2.53.1 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register (Offset = ACh) [reset = 0h]

Flash Command Write Data Register (Upper)

Return to Summary Table

Table 14-12890. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00ACh

Figure 14-6363. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12891. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Upper Byte: This is the command write data upper byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

14.7.4.3.2.54 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register

14.7.4.3.2.54.1 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register (Offset = B0h) [reset = 0h]

Polling Flash Status Register

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Table 14-12892. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00B0h

Figure 14-6364. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Name Register

31	30	29	28	27	26	25	24
DEVICE_STATUS_RSVD_FLD2							
R							
0h							
23	22	21	20	19	18	17	16
DEVICE_STATUS_RSVD_FLD2				DEVICE_STATUS_NB_DUMMY			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
DEVICE_STATUS_RSVD_FLD1							DEVICE_STATUS_VALID_FLD
R							R
0h							0h
7	6	5	4	3	2	1	0
DEVICE_STATUS_FLD							
R							
0h							

Table 14-12893. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	DEVICE_STATUS_RSVD_FLD2	R	0h	Reserved
19:16	DEVICE_STATUS_NB_DUMMY	R/W	0h	Number of dummy cycles for auto-polling
15:9	DEVICE_STATUS_RSVD_FLD1	R	0h	Reserved
8	DEVICE_STATUS_VALID_FLD	R	0h	Device Status Valid: This should be set when value in bits from 7 to 0 is valid.
7:0	DEVICE_STATUS_FLD	R	0h	Defines actual Status Register of Device

14.7.4.3.2.55 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register

14.7.4.3.2.55.1 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register (Offset = B4h) [reset = 40000000h]

PHY Configuration Register

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Table 14-12894. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00B4h

Figure 14-6365. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Name Register

31	30	29	28	27	26	25	24
PHY_CONFIG_RESYNC_FLD	PHY_CONFIG_RESET_FLD	PHY_CONFIG_RX_DLL_BYPASS_FLD	PHY_CONFIG_RESV2_FLD				
W	W	R/W	R				
0h	1h	0h	0h				
23	22	21	20	19	18	17	16
PHY_CONFIG_RESV2_FLD	PHY_CONFIG_TX_DLL_DELAY_FLD						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
PHY_CONFIG_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
PHY_CONFIG_RESV1_FLD	PHY_CONFIG_RX_DLL_DELAY_FLD						
R	R/W						
0h	0h						

Table 14-12895. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_CONFIG_RESYNC_FLD	W	0h	This bit is used for re-synchronisation delay lines to update them with values from TX DLL Delay and RX DLL Delay fields.
30	PHY_CONFIG_RESET_FLD	W	1h	DLL Reset bit: This bit is used for reset of Delay Lines by software.
29	PHY_CONFIG_RX_DLL_BYPASS_FLD	R/W	0h	RX DLL Bypass: This field determines id RX DLL is bypassed.
28:23	PHY_CONFIG_RESV2_FLD	R	0h	Reserved
22:16	PHY_CONFIG_TX_DLL_DELAY_FLD	R/W	0h	TX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and spi_clk.
15:7	PHY_CONFIG_RESV1_FLD	R	0h	Reserved
6:0	PHY_CONFIG_RX_DLL_DELAY_FLD	R/W	0h	RX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and rx_dll_clk.

14.7.4.3.2.56 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register

14.7.4.3.2.56.1 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register (Offset = B8h) [reset = 800000h]

PHY DLL Master Control Register

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Table 14-12896. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00B8h

Figure 14-6366. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
PHY_MASTER_CONTROL_RESV3_FLD							PHY_MASTER_LOCK_MODE_FLD
R							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MASTER_BYPASS_MODE_FLD	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD			PHY_MASTER_CONTROL_RESV2_FLD	PHY_MASTER_NB_INDICATIONS_FLD		
R/W	R/W			R	R/W		
1h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_MASTER_CONTROL_RESV1_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_CONTROL_RESV1_FLD	PHY_MASTER_INITIAL_DELAY_FLD						
R	R/W						
0h	0h						

Table 14-12897. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	PHY_MASTER_CONTROL_RESV3_FLD	R	0h	Reserved
24	PHY_MASTER_LOCK_MODE_FLD	R/W	0h	Determines if the initiator delay line locks on a full cycle or half cycle of delay.
23	PHY_MASTER_BYPASS_MODE_FLD	R/W	1h	Controls the bypass mode of the initiator and target DLLs.
22:20	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD	R/W	0h	Selects the number of delay elements to be inserted between the phase detect flip-flops.
19	PHY_MASTER_CONTROL_RESV2_FLD	R	0h	Reserved
18:16	PHY_MASTER_NB_INDICATIONS_FLD	R/W	0h	Holds the number of consecutive increment or decrement indications.
15:7	PHY_MASTER_CONTROL_RESV1_FLD	R	0h	Reserved
6:0	PHY_MASTER_INITIAL_DELAY_FLD	R/W	0h	This value is the initial delay value for the DLL.

14.7.4.3.2.57 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register

14.7.4.3.2.57.1 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register (Offset = BCh) [reset = 0h]

DLL Observable Register Lower

Return to Summary Table

Table 14-12898. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00BCh

Figure 14-6367. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD					DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD		DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD
R					R		R
0h					0h		0h

Table 14-12899. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD	R	0h	Holds the state of the cumulative dll_lock_inc register.
23:16	DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD	R	0h	Holds the state of the cumulative dll_lock_dec register.
15	DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	R	0h	This bit indicates that lock of loopback is done.
14:8	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD	R	0h	Reports the DLL encoder value from the initiator DLL to the target DLLs.
7:3	DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD	R	0h	Reports the number of increments or decrements required for the initiator DLL to complete the locking process.
2:1	DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD	R	0h	Defines the mode in which the DLL has achieved the lock.
0	DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD	R	0h	Indicates status of DLL.

14.7.4.3.2.58 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register

14.7.4.3.2.58.1 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register (Offset = C0h) [reset = 0h]

DLL Observable Register Upper

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Table 14-12900. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00C0h

Figure 14-6368. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DLL_OBSERVABLE_UPPER_RESV2_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>DLL_OBSERVABLE_UPPER_RESV2_FLD</td><td colspan="7">DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DLL_OBSERVABLE_UPPER_RESV1_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>DLL_OBSERVABLE_UPPER_RESV1_FLD</td><td colspan="7">DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
</table>

Table 14-12901. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	DLL_OBSERVABLE_UPPER_RESV2_FLD	R	0h	Reserved
22:16	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the TX delay line for this slice.
15:7	DLL_OBSERVABLE_UPPER_RESV1_FLD	R	0h	Reserved
6:0	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the RX delay line for this slice.

14.7.4.3.2.59 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register

14.7.4.3.2.59.1 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register (Offset = E0h) [reset = 13EDFA00h]

Opcode Extension Register (Lower)

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Table 14-12902. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00E0h

Figure 14-6369. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Name Register

31	30	29	28	27	26	25	24
EXT_READ_OPCODE_FLD							
R/W							
13h							
23	22	21	20	19	18	17	16
EXT_WRITE_OPCODE_FLD							
R/W							
EDh							
15	14	13	12	11	10	9	8
EXT_POLL_OPCODE_FLD							
R/W							
FAh							
7	6	5	4	3	2	1	0
EXT_STIG_OPCODE_FLD							
R/W							
0h							

Table 14-12903. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EXT_READ_OPCODE_FLD	R/W	13h	Supplement byte of any Read Opcode
23:16	EXT_WRITE_OPCODE_FLD	R/W	EDh	Supplement byte of any Write Opcode
15:8	EXT_POLL_OPCODE_FLD	R/W	FAh	Supplement byte of any Polling Opcode
7:0	EXT_STIG_OPCODE_FLD	R/W	0h	Supplement byte of any STIG Opcode

14.7.4.3.2.60 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register

14.7.4.3.2.60.1 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register (Offset = E4h) [reset = 6F90000h]

Opcode Extension Register (Upper)

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Table 14-12904. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00E4h

Figure 14-6370. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Name Register

31	30	29	28	27	26	25	24
WEL_OPCODE_FLD							
R/W							
6h							
23	22	21	20	19	18	17	16
EXT_WEL_OPCODE_FLD							
R/W							
F9h							
15	14	13	12	11	10	9	8
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							

Table 14-12905. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WEL_OPCODE_FLD	R/W	6h	First byte of any WEL Opcode
23:16	EXT_WEL_OPCODE_FLD	R/W	F9h	Supplement byte of any WEL Opcode
15:0	OPCODE_EXT_UPPER_RESV1_FLD	R	0h	Reserved

14.7.4.3.2.61 OSPI_FLASH_CFG_MODULE_ID_REG Register

14.7.4.3.2.61.1 OSPI_FLASH_CFG_MODULE_ID_REG Register (Offset = FCh) [reset = 3000300h]

Module ID Register

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Table 14-12906. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 00FCh

Figure 14-6371. OSPI_FLASH_CFG_MODULE_ID_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FIX_PATCH_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MODULE_ID_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">MODULE_ID_RESV_FLD</td><td colspan="2">CONF_FLD</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12907. OSPI_FLASH_CFG_MODULE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	FIX_PATCH_FLD	R	3h	Fix/path number related to revision described by 3 LSBs of this register
23:8	MODULE_ID_FLD	R	3h	Module/Revision ID number
7:2	MODULE_ID_RESV_FLD	R	0h	Reserved
1:0	CONF_FLD	R	0h	Configuration ID number: 0 : OCTAL + PHY Configuration 1 : OCTAL Configuration 2 : QUAD + PHY Configuration 3 : QUAD Configuration

14.7.4.3.2.62 OSPI_CFG_PID Register

14.7.4.3.2.62.1 OSPI_CFG_PID Register (Offset = 0h) [reset = 68747900h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-12908. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 4000h

Figure 14-6372. OSPI_CFG_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">874h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">874h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">Fh</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-12909. OSPI_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: psrst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: psrst_n
27:16	MODULE_ID	R	874h	Module ID Reset Source: psrst_n
15:11	RTL	R	Fh	RTL revision. Will vary depending on release. Reset Source: psrst_n
10:8	MAJOR	R	1h	Major revision Reset Source: psrst_n
7:6	CUSTOM	R	0h	Custom Reset Source: psrst_n
5:0	MINOR	R	0h	Minor revision Reset Source: psrst_n

14.7.4.3.2.63 OSPI_CFG_CTRL Register

14.7.4.3.2.63.1 OSPI_CFG_CTRL Register (Offset = 4h) [reset = 0h]

The Control Register contains general control bits for the ospi

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Table 14-12910. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 4004h

Figure 14-6373. OSPI_CFG_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PIPELINE_MODE_FLUSH	RESERVED		
NONE				R/W	NONE		
0h				0h	0h		

Table 14-12911. OSPI_CFG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PIPELINE_MODE_FLUSH	R/W	0h	1 - Flush Cadence Flash Controller FIFO by forcin gAHB SEL low. 0 - AHB Sel to Cadence Controller is 1 Reset Source: psrst_n
2:0	RESERVED	NONE	0h	Reserved

14.7.4.3.2.64 OSPI_CFG_STAT Register

14.7.4.3.2.64.1 OSPI_CFG_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the ospi

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Table 14-12912. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 4008h

Figure 14-6374. OSPI_CFG_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>MEM_INIT_DONE</td><td>RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12913. OSPI_CFG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_INIT_DONE	R	0h	0:Memory Initialization is in progress, 1:Memory Intialization Done Reset Source: psrst_n
0	RESERVED	NONE	0h	Reserved

14.7.4.3.2.65 OSPI_CFG_EOI Register

14.7.4.3.2.65.1 OSPI_CFG_EOI Register (Offset = 20h) [reset = 0h]

End of Interrupt Register

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Table 14-12914. Instance Table

Instance Name	Physical Address
FSS1_OSPI_0	0FCC 4020h

Figure 14-6375. OSPI_CFG_EOI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">EOI</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-12915. OSPI_CFG_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI	W	0h	Write with bit position of targetted interrupt. (E.g. Ext TS is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt Reset Source: psrst_n

14.7.4.4 FSS_HYPERBUS1P0_0

FSS_HYPERBUS1P0_0

14.7.4.4.1 FSS_HYPERBUS1P0_0 Summaries

FSS_HYPERBUS1P0_0 Summaries

Table 14-12916. ECC_AGGR Registers, Base Address=0072 2000h, Length=1024

Offset	Length	Register Name	FSS1_HYPERBUS1P0_0 Physical Address
0h	32	ECC_AGGR_REV	0072 2000h
8h	32	ECC_AGGR_VECTOR	0072 2008h
Ch	32	ECC_AGGR_STAT	0072 200Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0072 2010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0072 203Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0072 2040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0072 2080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0072 20C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0072 213Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0072 2140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0072 2180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0072 21C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0072 2200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0072 2204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0072 2208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0072 220Ch

Table 14-12917. HYPERBUS_SYSCFG Registers, Base Address=0FC3 0000h, Length=256

Offset	Length	Register Name	FSS1_HYPERBUS1P0_0 Physical Address
0h	32	HYPERBUS_SYSCFG_REVISION_REG	0FC3 0000h
4h	32	HYPERBUS_SYSCFG_DLL_STAT_REG	0FC3 0004h
8h	32	HYPERBUS_SYSCFG_RAM_STAT_REG	0FC3 0008h

Table 14-12918. HYPERBUS_CORE Registers, Base Address=0FC3 4000h, Length=256

Offset	Length	Register Name	FSS1_HYPERBUS1P0_0 Physical Address
0h	32	HYPERBUS_CORE_CSR	0FC3 4000h
4h	32	HYPERBUS_CORE_IER	0FC3 4004h
8h	32	HYPERBUS_CORE_ISR	0FC3 4008h
10h	32	HYPERBUS_CORE_MBAR_J	0FC3 4010h + formula
20h	32	HYPERBUS_CORE_MCR_J	0FC3 4020h + formula
30h	32	HYPERBUS_CORE_MTR_J	0FC3 4030h + formula
40h	32	HYPERBUS_CORE_GPOR	0FC3 4040h
44h	32	HYPERBUS_CORE_WPR	0FC3 4044h
48h	32	HYPERBUS_CORE_LBR	0FC3 4048h

14.7.4.4.2 FSS_HYPERBUS1P0_0 Registers

FSS_HYPERBUS1P0_0 Registers

14.7.4.4.2.1 ECC_AGGR_REV Register

14.7.4.4.2.1.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

Revision parameters

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Table 14-12919. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2000h

Figure 14-6376. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
1Dh					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-12920. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	1Dh	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

14.7.4.4.2.2 ECC_AGGR_VECTOR Register

14.7.4.4.2.2.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-12921. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2008h

Figure 14-6377. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 14-12922. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.4.4.2.3 ECC_AGGR_STAT Register

14.7.4.4.2.3.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = Fh]

Misc Status

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Table 14-12923. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 200Ch

Figure 14-6378. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					Fh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
Fh							

Table 14-12924. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	Fh	Indicates the number of RAMS serviced by the ECC aggregator

14.7.4.4.2.4 ECC_AGGR_RESERVED_SVBUS_J Register

14.7.4.4.2.4.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-12925. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2010h + formula

Figure 14-6379. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 14-12926. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.4.4.2.5 ECC_AGGR_SEC_EOI_REG Register

14.7.4.4.2.5.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-12927. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 203Ch

Figure 14-6380. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12928. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.4.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

14.7.4.4.2.6.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12929. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2040h

Figure 14-6381. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIFO_PEND	MEM_AR_FIFO_PEND	MEM_AWID1_FIFO_PEND	MEM_WID1_FIFO_PEND	MEM_AW1_FIFO_PEND	MEM_AWID0_FIFO_PEND	MEM_WID0_FIFO_PEND
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MEM_AW0_FIFO_PEND	MEM_RX_FIFO_PEND	MEM_RDAT_FIFO_PEND	MEM_BDAT1_FIFO_PEND	MEM_BDAT0_FIFO_PEND	MEM_WDAT1_FIFO_PEND	MEM_WDAT0_FIFO_PEND	MEM_ADR_FIFO_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12930. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	MEM_ARID_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_arid_fifo_pend
13	MEM_AR_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_awid1_fifo_pend
11	MEM_WID1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_awid0_fifo_pend
8	MEM_WID0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_aw0_fifo_pend
6	MEM_RX_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_rx_fifo_pend
5	MEM_RDAT_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_wdat1_fifo_pend

Table 14-12930. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MEM_WDAT0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_adr_fifo_pend

14.7.4.4.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.7.4.4.2.7.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12931. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2080h

Figure 14-6382. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIFO_ENABLE_SET	MEM_AR_FIFO_ENABLE_SET	MEM_AWID1_FIFO_ENABLE_SET	MEM_WID1_FIFO_ENABLE_SET	MEM_AW1_FIFO_ENABLE_SET	MEM_AWID0_FIFO_ENABLE_SET	MEM_WID0_FIFO_ENABLE_SET
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MEM_AW0_FIFO_ENABLE_SET	MEM_RX_FIFO_ENABLE_SET	MEM_RDAT_FIFO_ENABLE_SET	MEM_BDAT1_FIFO_ENABLE_SET	MEM_BDAT0_FIFO_ENABLE_SET	MEM_WDAT1_FIFO_ENABLE_SET	MEM_WDAT0_FIFO_ENABLE_SET	MEM_ADR_FIFO_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12932. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	MEM_ARID_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_arid_fifo_pend
13	MEM_AR_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_awid1_fifo_pend
11	MEM_WID1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_awid0_fifo_pend
8	MEM_WID0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_aw0_fifo_pend
6	MEM_RX_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_rx_fifo_pend

Table 14-12932. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MEM_RDAT_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_wdat1_fifo_pend
1	MEM_WDAT0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_adr_fifo_pend

14.7.4.4.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.7.4.4.2.8.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12933. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 20C0h

Figure 14-6383. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIFO_ENABLE_CLR	MEM_AR_FIFO_ENABLE_CLR	MEM_AWID1_FIFO_ENABLE_CLR	MEM_WID1_FIFO_ENABLE_CLR	MEM_AW1_FIFO_ENABLE_CLR	MEM_AWID0_FIFO_ENABLE_CLR	MEM_WID0_FIFO_ENABLE_CLR
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MEM_AW0_FIFO_ENABLE_CLR	MEM_RX_FIFO_ENABLE_CLR	MEM_RDAT_FIFO_ENABLE_CLR	MEM_BDAT1_FIFO_ENABLE_CLR	MEM_BDAT0_FIFO_ENABLE_CLR	MEM_WDAT1_FIFO_ENABLE_CLR	MEM_WDAT0_FIFO_ENABLE_CLR	MEM_ADR_FIFO_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12934. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	MEM_ARID_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_arid_fifo_pend
13	MEM_AR_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_awid1_fifo_pend
11	MEM_WID1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_awid0_fifo_pend
8	MEM_WID0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_aw0_fifo_pend
6	MEM_RX_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_rx_fifo_pend

Table 14-12934. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MEM_RDAT_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_wdat1_fifo_pend
1	MEM_WDAT0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_adr_fifo_pend

14.7.4.4.2.9 ECC_AGGR_DED_EOI_REG Register

14.7.4.4.2.9.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-12935. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 213Ch

Figure 14-6384. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-12936. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.4.2.10 ECC_AGGR_DED_STATUS_REG0 Register

14.7.4.4.2.10.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-12937. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2140h

Figure 14-6385. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIFO_PEND	MEM_AR_FIFO_PEND	MEM_AWID1_FIFO_PEND	MEM_WID1_FIFO_PEND	MEM_AW1_FIFO_PEND	MEM_AWID0_FIFO_PEND	MEM_WID0_FIFO_PEND
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MEM_AW0_FIFO_PEND	MEM_RX_FIFO_PEND	MEM_RDAT_FIFO_PEND	MEM_BDAT1_FIFO_PEND	MEM_BDAT0_FIFO_PEND	MEM_WDAT1_FIFO_PEND	MEM_WDAT0_FIFO_PEND	MEM_ADR_FIFO_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12938. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	MEM_ARID_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_arid_fifo_pend
13	MEM_AR_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_awid1_fifo_pend
11	MEM_WID1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_awid0_fifo_pend
8	MEM_WID0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_aw0_fifo_pend
6	MEM_RX_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_rx_fifo_pend
5	MEM_RDAT_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_wdat1_fifo_pend

Table 14-12938. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MEM_WDAT0_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_PEND	R/W1TS	0h	Interrupt Pending Status for mem_adr_fifo_pend

14.7.4.4.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.7.4.4.2.11.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-12939. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2180h

Figure 14-6386. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIFO_ENABLE_SET	MEM_AR_FIFO_ENABLE_SET	MEM_AWID1_FIFO_ENABLE_SET	MEM_WID1_FIFO_ENABLE_SET	MEM_AW1_FIFO_ENABLE_SET	MEM_AWID0_FIFO_ENABLE_SET	MEM_WID0_FIFO_ENABLE_SET
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MEM_AW0_FIFO_ENABLE_SET	MEM_RX_FIFO_ENABLE_SET	MEM_RDAT_FIFO_ENABLE_SET	MEM_BDAT1_FIFO_ENABLE_SET	MEM_BDAT0_FIFO_ENABLE_SET	MEM_WDAT1_FIFO_ENABLE_SET	MEM_WDAT0_FIFO_ENABLE_SET	MEM_ADR_FIFO_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12940. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	MEM_ARID_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_arid_fifo_pend
13	MEM_AR_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_awid1_fifo_pend
11	MEM_WID1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_awid0_fifo_pend
8	MEM_WID0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_aw0_fifo_pend
6	MEM_RX_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_rx_fifo_pend

Table 14-12940. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MEM_RDAT_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_wdat1_fifo_pend
1	MEM_WDAT0_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mem_adr_fifo_pend

14.7.4.4.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.7.4.4.2.12.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-12941. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 21C0h

Figure 14-6387. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIFO_ENABLE_CLR	MEM_AR_FIFO_ENABLE_CLR	MEM_AWID1_FIFO_ENABLE_CLR	MEM_WID1_FIFO_ENABLE_CLR	MEM_AW1_FIFO_ENABLE_CLR	MEM_AWID0_FIFO_ENABLE_CLR	MEM_WID0_FIFO_ENABLE_CLR
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MEM_AW0_FIFO_ENABLE_CLR	MEM_RX_FIFO_ENABLE_CLR	MEM_RDAT_FIFO_ENABLE_CLR	MEM_BDAT1_FIFO_ENABLE_CLR	MEM_BDAT0_FIFO_ENABLE_CLR	MEM_WDAT1_FIFO_ENABLE_CLR	MEM_WDAT0_FIFO_ENABLE_CLR	MEM_ADR_FIFO_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-12942. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	MEM_ARID_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_arid_fifo_pend
13	MEM_AR_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_awid1_fifo_pend
11	MEM_WID1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_awid0_fifo_pend
8	MEM_WID0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_aw0_fifo_pend
6	MEM_RX_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_rx_fifo_pend

Table 14-12942. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MEM_RDAT_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_wdat1_fifo_pend
1	MEM_WDAT0_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mem_adr_fifo_pend

14.7.4.4.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

14.7.4.4.2.13.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-12943. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2200h

Figure 14-6388. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-12944. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.4.4.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

14.7.4.4.2.14.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-12945. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2204h

Figure 14-6389. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-12946. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.4.4.2.15 ECC_AGGR_AGGR_STATUS_SET Register

14.7.4.4.2.15.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-12947. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 2208h

Figure 14-6390. ECC_AGGR_AGGR_STATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-12948. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.4.4.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

14.7.4.4.2.16.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-12949. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0072 220Ch

Figure 14-6391. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-12950. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.4.4.2.17 HYPERBUS_SYSCFG_REVISION_REG Register

14.7.4.4.2.17.1 HYPERBUS_SYSCFG_REVISION_REG Register (Offset = 0h) [reset = 6860E900h]

The Revision Register contains the major and minor revisions for the module

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Table 14-12951. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 0000h

Figure 14-6392. HYPERBUS_SYSCFG_REVISION_REG Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6860h							
23	22	21	20	19	18	17	16
MODID							
R							
6860h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
1Dh					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-12952. HYPERBUS_SYSCFG_REVISION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6860h	Module ID field Reset Source: rst_n
15:11	REVRTL	R	1Dh	RTL revision. Will vary depending on release Reset Source: rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: rst_n

14.7.4.4.2.18 HYPERBUS_SYSCFG_DLL_STAT_REG Register

14.7.4.4.2.18.1 HYPERBUS_SYSCFG_DLL_STAT_REG Register (Offset = 4h) [reset = 0h]

DLL status register

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Table 14-12953. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 0004h

Figure 14-6393. HYPERBUS_SYSCFG_DLL_STAT_REG Name Register

31	30	29	28	27	26	25	24
RSVD04							
R							
0h							
23	22	21	20	19	18	17	16
RSVD04							
R							
0h							
15	14	13	12	11	10	9	8
RSVD04					MDLL_CODE		
R					R		
0h					0h		
7	6	5	4	3	2	1	0
MDLL_CODE						SDL_LOCK	MDLL_LOCK
R						R	R
0h						0h	0h

Table 14-12954. HYPERBUS_SYSCFG_DLL_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RSVD04	R	0h	Reserved Reset Source: rst_n
10:2	MDLL_CODE	R	0h	MDLL code. The target delay line length that is currently enabled is determined by the MDLL code value Reset Source: rst_n
1	SDL_LOCK	R	0h	SDL lock. When this bit is set, it indicates that the target delay line in the MDLL is locked. Reset Source: rst_n
0	MDLL_LOCK	R	0h	MDLL lock. When this bit is set, it indicates that the initiator delay line in the MDLL is locked. Reset Source: rst_n

14.7.4.4.2.19 HYPERBUS_SYSCFG_RAM_STAT_REG Register

14.7.4.4.2.19.1 HYPERBUS_SYSCFG_RAM_STAT_REG Register (Offset = 8h) [reset = 0h]

RAM status register

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Table 14-12955. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 0008h

Figure 14-6394. HYPERBUS_SYSCFG_RAM_STAT_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>INIT_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12956. HYPERBUS_SYSCFG_RAM_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	INIT_DONE	R	0h	FIFO RAM initialization done. When this bit is set, t indicates that all the FIFO RAM auto initialization is complete. Software should check that this bit is set before initiating transactions to the external memory Reset Source: rst_n

14.7.4.4.2.20 HYPERBUS_CORE_CSR Register

14.7.4.4.2.20.1 HYPERBUS_CORE_CSR Register (Offset = 0h) [reset = 0h]

Controller Status Register to access the internal status of HyperBus Memory Controller IP

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Table 14-12957. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4000h

Figure 14-6395. HYPERBUS_CORE_CSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="5">RFU3</td><td>WRSTOERR</td><td>WTRSERR</td><td>WDECERR</td></tr>
<tr><td colspan="5">R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RFU2</td><td>WACT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RFU1</td><td>RDSSTALL</td><td>RRSTOERR</td><td>RTRSERR</td><td>RDECERR</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RFU0</td><td>RACT</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12958. HYPERBUS_CORE_CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RFU3	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
26	WRSTOERR	R	0h	Write RSTO error. This bit indicates whether HyperBus memory is under reset state in the latest write operation.When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.0-Normal operation,1- HyperBus memory is under reset Reset Source: mod_g_rst_n
25	WTRSERR	R	0h	Write Transaction Error. This bit indicates whether AXI protocol is acceptable by HyperBus Memory Controller IP in the latest write transaction.When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.0-Normal operation,1- This protocol is not supported Reset Source: mod_g_rst_n
24	WDECERR	R	0h	Write Decode Error. This bit indicates whether access address is acceptable in the latest write transaction.When this bit is set, HyperBus Memory Controller IP responds by AXI DECERR.0-Normal operation. 1- Access address is not reachable Reset Source: mod_g_rst_n
23:17	RFU2	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n

Table 14-12958. HYPERBUS_CORE_CSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	WACT	R	0h	Write is Active. This bit indicates whether write transaction is in progress or not.0- Write is idle,1 - Write is active.When receiving write request on write address channel, this bit becomes 1. When retrieving response signaling on write response channel, this bit becomes 0. Reset Source: mod_g_rst_n
15:12	RFU1	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
11	RDSSTALL	R	0h	RDS Stall. This bit indicates whether read data transfer from HyperBus memory is stalled [RDS remains LOW] in the latest read transaction.When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR. Reset Source: mod_g_rst_n
10	RRSTOERR	R	0h	Read RSTO error. This bit indicates whether HyperBus memory is under reset state in the latest read operation.When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.0 -Normal operation, 1 -HyperBus memory is under reset Reset Source: mod_g_rst_n
9	RTRSERR	R	0h	Read Transaction Error. This bit indicates whether AXI protocol is acceptable by HyperBus Memory Controller IP in the latest read transaction.When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.0- Normal operation,1- This protocol is not supported Reset Source: mod_g_rst_n
8	RDECERR	R	0h	Read Decode Error. This bit indicates whether access address is acceptable in the latest read transaction.When this bit is set, HyperBus Memory Controller IP responds by AXI DECERR.0 -Normal operation,1- Access address is not reachable Reset Source: mod_g_rst_n
7:1	RFU0	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
0	RACT	R	0h	Read is Active. This bit indicates whether read transaction is in progress or not. 0 - Read is idle, 1-Read is active. When receiving read request on read address channel, this bit becomes 1. When retrieving all requested data on read data channel, this bit becomes 0 Reset Source: mod_g_rst_n

14.7.4.4.2.21 HYPERBUS_CORE_IER Register

14.7.4.4.2.21.1 HYPERBUS_CORE_IER Register (Offset = 4h) [reset = 0h]

HyperBus Memory Controller IP outputs optional interrupt signal by condition enabled by this register

Return to Summary Table

Table 14-12959. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4004h

Figure 14-6396. HYPERBUS_CORE_IER Name Register

31	30	29	28	27	26	25	24
INTP	RFU4						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RFU4							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RFU4							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RFU4							RPCINTE
R							R/W
0h							0h

Table 14-12960. HYPERBUS_CORE_IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INTP	R/W	0h	Interrupt Polarity Control. This bit is used to choose the polarity of optional interrupt signal [IENOn].0 -IENOn signal is active low.1 -IENOn signal is active high. [Reversed mode.] Reset Source: mod_g_rst_n
30:1	RFU4	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
0	RPCINTE	R/W	0h	HyperBus Memory Interrupt Enable.0 - Disable interrupt.1 - Enable interrupt by INT# signal of HyperBus memory. Reset Source: mod_g_rst_n

14.7.4.4.2.22 HYPERBUS_CORE_ISR Register

14.7.4.4.2.22.1 HYPERBUS_CORE_ISR Register (Offset = 8h) [reset = 0h]

Interrupt status register

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Table 14-12961. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4008h

Figure 14-6397. HYPERBUS_CORE_ISR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RFU5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RFU5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RFU5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RFU5</td><td>RPCINTS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-12962. HYPERBUS_CORE_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RFU5	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
0	RPCINTS	R	0h	HyperBus Memory Interrupt.0 -No interrupt.1 - This bit displays interrupt from INT# signal of HyperBus memory. Reset Source: mod_g_rst_n

14.7.4.4.2.23 HYPERBUS_CORE_MBAR_J Register

14.7.4.4.2.23.1 HYPERBUS_CORE_MBAR_J Register (Offset = 10h) [reset = 0h]

Memory Base Address Register for device connected to CS#

Return to Summary Table

Table 14-12963. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4010h + formula

Figure 14-6398. HYPERBUS_CORE_MBAR_j Name Register

31	30	29	28	27	26	25	24
A_MSB							
R/W							
0h							
23	22	21	20	19	18	17	16
A_LSB							
R							
0h							
15	14	13	12	11	10	9	8
A_LSB							
R							
0h							
7	6	5	4	3	2	1	0
A_LSB							
R							
0h							

Table 14-12964. HYPERBUS_CORE_MBAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	A_MSB	R/W	0h	MSB 8 bit of the base address of addressable region to HyperBus memory Reset Source: mod_g_rst_n
23:0	A_LSB	R	0h	Since register can be set in 16M bytes boundary, lower 24 bit is fixed to 0, if read, this field will always return 0 Reset Source: mod_g_rst_n

14.7.4.4.2.24 HYPERBUS_CORE_MCR_J Register

14.7.4.4.2.24.1 HYPERBUS_CORE_MCR_J Register (Offset = 20h) [reset = 3h]

Memory configuration register for CS#

Return to Summary Table

Table 14-12965. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4020h + formula

Figure 14-6399. HYPERBUS_CORE_MCR_j Name Register

31	30	29	28	27	26	25	24
MAXEN	RFU8				MAXLEN		
R/W	R				R/W		
0h	0h				0h		
23	22	21	20	19	18	17	16
MAXLEN						TCMO	ACS
R/W						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RFU7							
R							
0h							
7	6	5	4	3	2	1	0
RFU7		CRT	DEVTYPE	RFU6		WRAPSIZE	
R		R/W	R/W	R		R/W	
0h		0h	0h	0h		3h	

Table 14-12966. HYPERBUS_CORE_MCR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAXEN	R/W	0h	Maximum length Enable 0: No configurable CS# low time 1: Configurable CS# low time When this bit 1, CS# low time can be configurable by MAXLEN bit. Reset Source: mod_g_rst_n
30:27	RFU8	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
26:18	MAXLEN	R/W	0h	Maximum Length,This bit indicates maximum read/write transaction length to memory. This bit is ignored when MAXEN bit is 0. 000000000: 2 Byte [1 HyperBus CK] 000000001: 4 Byte [2 HyperBus CK] 000000010: 6 Byte [3 HyperBus CK] 111111111: 1024 Byte [512 HyperBus CK] Reset Source: mod_g_rst_n
17	TCMO	R/W	0h	True Continuous Merge Option. 0 : No merging WRAP and INCR. 1 : Merging WRAP and INCR. Note that this function can be used with the HyperFlash with specific function. Please confirm whether it is corresponding HyperFlash before enabling this function. When HyperBus memory doesnt accept the 8-bit boundary address, and a wrapping burst access with ARSIZE=0 and ARADDR0=1 is used, this bit must not be set to 1. Reset Source: mod_g_rst_n

Table 14-12966. HYPERBUS_CORE_MCR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	ACS	R/W	0h	Asymmetry Cache Support. 0 : No asymmetry cache system support. 1 : Asymmetry cache system support. This function should be disabled if the HyperBus memory itself supports the asymmetry cache system. Reset Source: mod_g_rst_n
15:6	RFU7	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
5	CRT	R/W	0h	Configuration Register Target. 0: Memory space 1: CR space . This bit indicates whether the read or write operation accesses the memory or CR space. This bit is mapped to CA-46 bit in HyperRAM. When using HyperFlash, Reset Source: mod_g_rst_n
4	DEVTYPE	R/W	0h	Device Type. 0: HyperFlash,1: HyperRAM. Device type for control target Reset Source: mod_g_rst_n
3:2	RFU6	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
1:0	WRAPSIZE	R/W	3h	Wrap Size.The wrap burst length of HyperBus memory. This bit is ignored when the asymmetry cache support bit is 0. When the asymmetry cache support is 1, this bit should be set the same as wrap size of configuration register in HyperBus memory. 00 :Reserved. 01 :64 Bytes. 10 :16 Bytes. 11 :32 Bytes. Reset Source: mod_g_rst_n

14.7.4.4.2.25 HYPERBUS_CORE_MTR_J Register

14.7.4.4.2.25.1 HYPERBUS_CORE_MTR_J Register (Offset = 30h) [reset = 1h]

CS# Memory Timing Register

Return to Summary Table

Table 14-12967. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4030h + formula

Figure 14-6400. HYPERBUS_CORE_MTR_j Name Register

31	30	29	28	27	26	25	24
RCSHI				WCSHI			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RCSS				WCSS			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RCSH				WCSH			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RFU12				LTCY			
R				R/W			
0h				1h			

Table 14-12968. HYPERBUS_CORE_MTR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RCSHI	R/W	0h	Read Chip Select High Between Operations. This bit indicates CS# high time for read between operations. 0x0 corresponds to 1.5 clock cycle, 0xF corresponds to 16.5 clock cycle. Reset Source: mod_g_rst_n
27:24	WCSHI	R/W	0h	Write Chip Select High Between Operations. This bit indicates CS# high time for write between operations. 0x0 corresponds to 1.5 clock cycle, 0xF corresponds to 16.5 clock cycle. Reset Source: mod_g_rst_n
23:20	RCSS	R/W	0h	Read Chip Select Setup to next CK rising edge. This bit indicates CS# setup time for read from CS# assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle. Reset Source: mod_g_rst_n
19:16	WCSS	R/W	0h	Write Chip Select Setup to next CK rising edge. This bit indicates CS# setup time for write from CS# assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle Reset Source: mod_g_rst_n
15:12	RCSH	R/W	0h	Read Chip Select Hold after CK falling edge. This bit indicates CS# hold time for read to CS# de-assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle. Reset Source: mod_g_rst_n

Table 14-12968. HYPERBUS_CORE_MTR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	WCSH	R/W	0h	Write Chip Select Hold after CK falling edge. This bit indicates CS# hold time for write to CS# de-assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponding to 16 clock cycle Reset Source: mod_g_rst_n
7:4	RFU12	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
3:0	LTCY	R/W	1h	Latency Cycle. Only uses in HyperRAM. This bit indicates initial latency code for read/write access. This bit is ignored when MCRX.DEVTYPE is 0 [HyperFlash]. 0000 - 5 clock latency 0001 - 6 clock latency 0010 - Reserved 1101 - Reserved 1110 - 3 clock latency 1111 - 4 clock latency Reset Source: mod_g_rst_n

14.7.4.4.2.26 HYPERBUS_CORE_GPOR Register

14.7.4.4.2.26.1 HYPERBUS_CORE_GPOR Register (Offset = 40h) [reset = 0h]

General Purpose Output Register

Return to Summary Table

Table 14-12969. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4040h

Figure 14-6401. HYPERBUS_CORE_GPOR Name Register

31	30	29	28	27	26	25	24
RFU14							
R							
0h							
23	22	21	20	19	18	17	16
RFU14							
R							
0h							
15	14	13	12	11	10	9	8
RFU14							
R							
0h							
7	6	5	4	3	2	1	0
RFU14						GPO	
R						R/W	
0h						0h	

Table 14-12970. HYPERBUS_CORE_GPOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RFU14	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
1:0	GPO	R/W	0h	General Purpose Output interface. 0: Output signal polarity is LOW. 1: Output signal polarity is HIGH. Reset Source: mod_g_rst_n

14.7.4.4.2.27 HYPERBUS_CORE_WPR Register

14.7.4.4.2.27.1 HYPERBUS_CORE_WPR Register (Offset = 44h) [reset = 0h]

Write Protection Register

Return to Summary Table

Table 14-12971. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4044h

Figure 14-6402. HYPERBUS_CORE_WPR Name Register

31	30	29	28	27	26	25	24
RFU15							
R							
0h							
23	22	21	20	19	18	17	16
RFU15							
R							
0h							
15	14	13	12	11	10	9	8
RFU15							
R							
0h							
7	6	5	4	3	2	1	0
RFU15							WP
R							R/W
0h							0h

Table 14-12972. HYPERBUS_CORE_WPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RFU15	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
0	WP	R/W	0h	Write Protection Control. 0 : Not Protected. WP# signal is HIGH. 1 : Protected. WP# signal is LOW. Reset Source: mod_g_rst_n

14.7.4.4.2.28 HYPERBUS_CORE_LBR Register

14.7.4.4.2.28.1 HYPERBUS_CORE_LBR Register (Offset = 48h) [reset = 0h]

Loop Back Register

Return to Summary Table

Table 14-12973. Instance Table

Instance Name	Physical Address
FSS1_HYPERBUS1P0_0	0FC3 4048h

Figure 14-6403. HYPERBUS_CORE_LBR Name Register

31	30	29	28	27	26	25	24
RFU16							
R							
0h							
23	22	21	20	19	18	17	16
RFU16							
R							
0h							
15	14	13	12	11	10	9	8
RFU16							
R							
0h							
7	6	5	4	3	2	1	0
RFU16							LOOPBACK
R							R/W
0h							0h

Table 14-12974. HYPERBUS_CORE_LBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RFU16	R	0h	This field is reserved for future use Reset Source: mod_g_rst_n
0	LOOPBACK	R/W	0h	The write transaction data written on AXI bus is looped back as the read data from RPC bus. The loop-back is performed between W DAT FIFO and R DAT FIFO in AXI interface controller. 0 :Disable loopback. 1 :Enable loopback. Reset Source: mod_g_rst_n

14.7.4.5 FSS_FSAS_0

FSS_FSAS_0

14.7.4.5.1 FSS_FSAS_0 Summaries

FSS_FSAS_0 Summaries

Table 14-12975. FSS_FSAS_GENREGS Registers, Base Address=0FC9 0000h, Length=256

Offset	Length	Register Name	FSS1_FSAS_0 Physical Address
4h	32	FSS_FSAS_GENREGS_SYSCONFIG	0FC9 0004h
8h	32	FSS_FSAS_GENREGS_FRAG_ADR	0FC9 0008h
Ch	32	FSS_FSAS_GENREGS_FRAG_CTL	0FC9 000Ch
10h	32	FSS_FSAS_GENREGS_IRQ_EOI	0FC9 0010h + formula
14h	32	FSS_FSAS_GENREGS_IRQ_STATUS_RAW	0FC9 0014h + formula
18h	32	FSS_FSAS_GENREGS_IRQ_STATUS	0FC9 0018h + formula
1Ch	32	FSS_FSAS_GENREGS_IRQ_ENABLE_SET	0FC9 001Ch + formula
20h	32	FSS_FSAS_GENREGS_IRQ_ENABLE_CLR	0FC9 0020h + formula
30h	32	FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J	0FC9 0030h + formula
34h	32	FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J	0FC9 0034h + formula
70h	32	FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR	0FC9 0070h + formula
74h	32	FSS_FSAS_GENREGS_ERR_ECC_TYPE	0FC9 0074h + formula
78h	32	FSS_FSAS_GENREGS_ERR_WRT_TYPE	0FC9 0078h + formula

Table 14-12976. FSS_FSAS_OTFA_REGS Registers, Base Address=0FCA 0000h, Length=4096

Offset	Length	Register Name	FSS1_FSAS_0 Physical Address
0h	32	FSS_FSAS_OTFA_REGS_REVID	0FCA 0000h
4h	32	FSS_FSAS_OTFA_REGS_SCFG	0FCA 0004h
8h	32	FSS_FSAS_OTFA_REGS_ISR	0FCA 0008h
Ch	32	FSS_FSAS_OTFA_REGS_IS	0FCA 000Ch
10h	32	FSS_FSAS_OTFA_REGS_IES	0FCA 0010h
14h	32	FSS_FSAS_OTFA_REGS_IEC	0FCA 0014h
18h	32	FSS_FSAS_OTFA_REGS_CCFG	0FCA 0018h
1Ch	32	FSS_FSAS_OTFA_REGS_CSTATUS	0FCA 001Ch
20h	32	FSS_FSAS_OTFA_REGS_RGCFG0	0FCA 0020h
24h	32	FSS_FSAS_OTFA_REGS_RGMACST0	0FCA 0024h
28h	32	FSS_FSAS_OTFA_REGS_RGST0	0FCA 0028h
2Ch	32	FSS_FSAS_OTFA_REGS_RGSI0	0FCA 002Ch
30h	32	FSS_FSAS_OTFA_REGS_RKEYE00	0FCA 0030h
34h	32	FSS_FSAS_OTFA_REGS_RKEYE01	0FCA 0034h
38h	32	FSS_FSAS_OTFA_REGS_RKEYE02	0FCA 0038h
3Ch	32	FSS_FSAS_OTFA_REGS_RKEYE03	0FCA 003Ch
40h	32	FSS_FSAS_OTFA_REGS_RKEYE04	0FCA 0040h
44h	32	FSS_FSAS_OTFA_REGS_RKEYE05	0FCA 0044h
48h	32	FSS_FSAS_OTFA_REGS_RKEYE06	0FCA 0048h
4Ch	32	FSS_FSAS_OTFA_REGS_RKEYE07	0FCA 004Ch
50h	32	FSS_FSAS_OTFA_REGS_RKEYEP00	0FCA 0050h
54h	32	FSS_FSAS_OTFA_REGS_RKEYEP01	0FCA 0054h
58h	32	FSS_FSAS_OTFA_REGS_RKEYEP02	0FCA 0058h

Table 14-12976. FSS_FSAS_OTFA_REGS Registers, Base Address=0FCA 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS1_FSAS_0 Physical Address
5Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP03	0FCA 005Ch
60h	32	FSS_FSAS_OTFA_REGS_RKEYEP04	0FCA 0060h
64h	32	FSS_FSAS_OTFA_REGS_RKEYEP05	0FCA 0064h
68h	32	FSS_FSAS_OTFA_REGS_RKEYEP06	0FCA 0068h
6Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP07	0FCA 006Ch
70h	32	FSS_FSAS_OTFA_REGS_RKEYA00	0FCA 0070h
74h	32	FSS_FSAS_OTFA_REGS_RKEYA01	0FCA 0074h
78h	32	FSS_FSAS_OTFA_REGS_RKEYA02	0FCA 0078h
7Ch	32	FSS_FSAS_OTFA_REGS_RKEYA03	0FCA 007Ch
80h	32	FSS_FSAS_OTFA_REGS_RKEYAP00	0FCA 0080h
84h	32	FSS_FSAS_OTFA_REGS_RKEYAP01	0FCA 0084h
88h	32	FSS_FSAS_OTFA_REGS_RKEYAP02	0FCA 0088h
8Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP03	0FCA 008Ch
90h	32	FSS_FSAS_OTFA_REGS_RIV00	0FCA 0090h
94h	32	FSS_FSAS_OTFA_REGS_RIV01	0FCA 0094h
98h	32	FSS_FSAS_OTFA_REGS_RIV02	0FCA 0098h
9Ch	32	FSS_FSAS_OTFA_REGS_RIV03	0FCA 009Ch
A0h	32	FSS_FSAS_OTFA_REGS_RGCFG1	0FCA 00A0h
A4h	32	FSS_FSAS_OTFA_REGS_RGMACST1	0FCA 00A4h
A8h	32	FSS_FSAS_OTFA_REGS_RGST1	0FCA 00A8h
ACh	32	FSS_FSAS_OTFA_REGS_RGSI1	0FCA 00ACh
B0h	32	FSS_FSAS_OTFA_REGS_RKEYE10	0FCA 00B0h
B4h	32	FSS_FSAS_OTFA_REGS_RKEYE11	0FCA 00B4h
B8h	32	FSS_FSAS_OTFA_REGS_RKEYE12	0FCA 00B8h
BCh	32	FSS_FSAS_OTFA_REGS_RKEYE13	0FCA 00BCh
C0h	32	FSS_FSAS_OTFA_REGS_RKEYE14	0FCA 00C0h
C4h	32	FSS_FSAS_OTFA_REGS_RKEYE15	0FCA 00C4h
C8h	32	FSS_FSAS_OTFA_REGS_RKEYE16	0FCA 00C8h
CCh	32	FSS_FSAS_OTFA_REGS_RKEYE17	0FCA 00CCh
D0h	32	FSS_FSAS_OTFA_REGS_RKEYEP10	0FCA 00D0h
D4h	32	FSS_FSAS_OTFA_REGS_RKEYEP11	0FCA 00D4h
D8h	32	FSS_FSAS_OTFA_REGS_RKEYEP12	0FCA 00D8h
DCh	32	FSS_FSAS_OTFA_REGS_RKEYEP13	0FCA 00DCh
E0h	32	FSS_FSAS_OTFA_REGS_RKEYEP14	0FCA 00E0h
E4h	32	FSS_FSAS_OTFA_REGS_RKEYEP15	0FCA 00E4h
E8h	32	FSS_FSAS_OTFA_REGS_RKEYEP16	0FCA 00E8h
ECh	32	FSS_FSAS_OTFA_REGS_RKEYEP17	0FCA 00ECh
F0h	32	FSS_FSAS_OTFA_REGS_RKEYA10	0FCA 00F0h
F4h	32	FSS_FSAS_OTFA_REGS_RKEYA11	0FCA 00F4h
F8h	32	FSS_FSAS_OTFA_REGS_RKEYA12	0FCA 00F8h
FCh	32	FSS_FSAS_OTFA_REGS_RKEYA13	0FCA 00FCh
100h	32	FSS_FSAS_OTFA_REGS_RKEYAP10	0FCA 0100h
104h	32	FSS_FSAS_OTFA_REGS_RKEYAP11	0FCA 0104h
108h	32	FSS_FSAS_OTFA_REGS_RKEYAP12	0FCA 0108h
10Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP13	0FCA 010Ch
110h	32	FSS_FSAS_OTFA_REGS_RIV10	0FCA 0110h

Table 14-12976. FSS_FSAS_OTFA_REGS Registers, Base Address=0FCA 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS1_FSAS_0 Physical Address
114h	32	FSS_FSAS_OTFA_REGS_RIV11	0FCA 0114h
118h	32	FSS_FSAS_OTFA_REGS_RIV12	0FCA 0118h
11Ch	32	FSS_FSAS_OTFA_REGS_RIV13	0FCA 011Ch
120h	32	FSS_FSAS_OTFA_REGS_RGCFG2	0FCA 0120h
124h	32	FSS_FSAS_OTFA_REGS_RGMACST2	0FCA 0124h
128h	32	FSS_FSAS_OTFA_REGS_RGST2	0FCA 0128h
12Ch	32	FSS_FSAS_OTFA_REGS_RGSI2	0FCA 012Ch
130h	32	FSS_FSAS_OTFA_REGS_RKEYE20	0FCA 0130h
134h	32	FSS_FSAS_OTFA_REGS_RKEYE21	0FCA 0134h
138h	32	FSS_FSAS_OTFA_REGS_RKEYE22	0FCA 0138h
13Ch	32	FSS_FSAS_OTFA_REGS_RKEYE23	0FCA 013Ch
140h	32	FSS_FSAS_OTFA_REGS_RKEYE24	0FCA 0140h
144h	32	FSS_FSAS_OTFA_REGS_RKEYE25	0FCA 0144h
148h	32	FSS_FSAS_OTFA_REGS_RKEYE26	0FCA 0148h
14Ch	32	FSS_FSAS_OTFA_REGS_RKEYE27	0FCA 014Ch
150h	32	FSS_FSAS_OTFA_REGS_RKEYEP20	0FCA 0150h
154h	32	FSS_FSAS_OTFA_REGS_RKEYEP21	0FCA 0154h
158h	32	FSS_FSAS_OTFA_REGS_RKEYEP22	0FCA 0158h
15Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP23	0FCA 015Ch
160h	32	FSS_FSAS_OTFA_REGS_RKEYEP24	0FCA 0160h
164h	32	FSS_FSAS_OTFA_REGS_RKEYEP25	0FCA 0164h
168h	32	FSS_FSAS_OTFA_REGS_RKEYEP26	0FCA 0168h
16Ch	32	FSS_FSAS_OTFA_REGS_RKEYEP27	0FCA 016Ch
170h	32	FSS_FSAS_OTFA_REGS_RKEYA20	0FCA 0170h
174h	32	FSS_FSAS_OTFA_REGS_RKEYA21	0FCA 0174h
178h	32	FSS_FSAS_OTFA_REGS_RKEYA22	0FCA 0178h
17Ch	32	FSS_FSAS_OTFA_REGS_RKEYA23	0FCA 017Ch
180h	32	FSS_FSAS_OTFA_REGS_RKEYAP20	0FCA 0180h
184h	32	FSS_FSAS_OTFA_REGS_RKEYAP21	0FCA 0184h
188h	32	FSS_FSAS_OTFA_REGS_RKEYAP22	0FCA 0188h
18Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP23	0FCA 018Ch
190h	32	FSS_FSAS_OTFA_REGS_RIV20	0FCA 0190h
194h	32	FSS_FSAS_OTFA_REGS_RIV21	0FCA 0194h
198h	32	FSS_FSAS_OTFA_REGS_RIV22	0FCA 0198h
19Ch	32	FSS_FSAS_OTFA_REGS_RIV23	0FCA 019Ch
1A0h	32	FSS_FSAS_OTFA_REGS_RGCFG3	0FCA 01A0h
1A4h	32	FSS_FSAS_OTFA_REGS_RGMACST3	0FCA 01A4h
1A8h	32	FSS_FSAS_OTFA_REGS_RGST3	0FCA 01A8h
1ACh	32	FSS_FSAS_OTFA_REGS_RGSI3	0FCA 01ACh
1B0h	32	FSS_FSAS_OTFA_REGS_RKEYE30	0FCA 01B0h
1B4h	32	FSS_FSAS_OTFA_REGS_RKEYE31	0FCA 01B4h
1B8h	32	FSS_FSAS_OTFA_REGS_RKEYE32	0FCA 01B8h
1BCh	32	FSS_FSAS_OTFA_REGS_RKEYE33	0FCA 01BCh
1C0h	32	FSS_FSAS_OTFA_REGS_RKEYE34	0FCA 01C0h
1C4h	32	FSS_FSAS_OTFA_REGS_RKEYE35	0FCA 01C4h
1C8h	32	FSS_FSAS_OTFA_REGS_RKEYE36	0FCA 01C8h

Table 14-12976. FSS_FSAS_OTFA_REGS Registers, Base Address=0FCA 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSS1_FSAS_0 Physical Address
1CCh	32	FSS_FSAS_OTFA_REGS_RKEYE37	0FCA 01CCh
1D0h	32	FSS_FSAS_OTFA_REGS_RKEYEP30	0FCA 01D0h
1D4h	32	FSS_FSAS_OTFA_REGS_RKEYEP31	0FCA 01D4h
1D8h	32	FSS_FSAS_OTFA_REGS_RKEYEP32	0FCA 01D8h
1DCh	32	FSS_FSAS_OTFA_REGS_RKEYEP33	0FCA 01DCh
1E0h	32	FSS_FSAS_OTFA_REGS_RKEYEP34	0FCA 01E0h
1E4h	32	FSS_FSAS_OTFA_REGS_RKEYEP35	0FCA 01E4h
1E8h	32	FSS_FSAS_OTFA_REGS_RKEYEP36	0FCA 01E8h
1ECh	32	FSS_FSAS_OTFA_REGS_RKEYEP37	0FCA 01ECh
1F0h	32	FSS_FSAS_OTFA_REGS_RKEYA30	0FCA 01F0h
1F4h	32	FSS_FSAS_OTFA_REGS_RKEYA31	0FCA 01F4h
1F8h	32	FSS_FSAS_OTFA_REGS_RKEYA32	0FCA 01F8h
1FCh	32	FSS_FSAS_OTFA_REGS_RKEYA33	0FCA 01FCh
200h	32	FSS_FSAS_OTFA_REGS_RKEYAP30	0FCA 0200h
204h	32	FSS_FSAS_OTFA_REGS_RKEYAP31	0FCA 0204h
208h	32	FSS_FSAS_OTFA_REGS_RKEYAP32	0FCA 0208h
20Ch	32	FSS_FSAS_OTFA_REGS_RKEYAP33	0FCA 020Ch
210h	32	FSS_FSAS_OTFA_REGS_RIV30	0FCA 0210h
214h	32	FSS_FSAS_OTFA_REGS_RIV31	0FCA 0214h
218h	32	FSS_FSAS_OTFA_REGS_RIV32	0FCA 0218h
21Ch	32	FSS_FSAS_OTFA_REGS_RIV33	0FCA 021Ch
220h	32	FSS_FSAS_OTFA_REGS_IRQADDINFO0	0FCA 0220h
224h	32	FSS_FSAS_OTFA_REGS_IRQADDINFO1	0FCA 0224h
228h	32	FSS_FSAS_OTFA_REGS_MACCACHEINFO	0FCA 0228h
22Ch	32	FSS_FSAS_OTFA_REGS_RMWRMCNT	0FCA 022Ch

Table 14-12977. FSS_DAT_REG1 Registers, Base Address=6800 0000h, Length=134217728

Offset	Length	Register Name	FSS1_FSAS_0 Physical Address
0h	32	FSS_DAT_REG1_HPB_DATA_MEM_J	6800 0000h + formula

Table 14-12978. FSS_DAT_REG0 Registers, Base Address=0002 0000 0000h, Length=4294967296

Offset	Length	Register Name	FSS1_FSAS_0 Physical Address
0h	32	FSS_DAT_REG0_HPB_DATA_MEM_J	0002 0000 0000h + formula

Table 14-12979. FSS_DAT_REG3 Registers, Base Address=0003 0000 0000h, Length=4294967296

Offset	Length	Register Name	FSS1_FSAS_0 Physical Address
0h	32	FSS_DAT_REG3_HPB_DATA_MEM_J	0003 0000 0000h + formula

14.7.4.5.2 FSS_FSAS_0 Registers

FSS_FSAS_0 Registers

14.7.4.5.2.1 FSS_FSAS_GENREGS_SYSCONFIG Register

14.7.4.5.2.1.1 FSS_FSAS_GENREGS_SYSCONFIG Register (Offset = 4h) [reset = 0h]

Controls various parameters of the cotroller state.

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Table 14-12980. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0004h

Figure 14-6404. FSS_FSAS_GENREGS_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							OSPI_32B_DISABLE_MODE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
DISXIP	OSPI_DDR_DISABLE_MODE	RESERVED		ECC_DISABLE_ADR	FSS_AES_EN_IPCFG	RESERVED	ECC_EN
R/W	R/W	NONE		R/W	R	NONE	R/W
0h	0h	0h		0h	0h	0h	0h

Table 14-12981. FSS_FSAS_GENREGS_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	OSPI_32B_DISABLE_MODE	R/W	0h	0 OSPI 32bit mode enabled. 1 OSPI 32bit mode disabled Reset Source: vbus_mod_g_rst_n
7	DISXIP	R/W	0h	0 XIP Prefetch Enabled. 1 XIP prefetch disabled Reset Source: vbus_mod_g_rst_n
6	OSPI_DDR_DISABLE_MODE	R/W	0h	0 OSPI DDR mode enabled. 1 OSPI DDR mode disabled Reset Source: vbus_mod_g_rst_n
5:4	RESERVED	NONE	0h	Reserved
3	ECC_DISABLE_ADR	R/W	0h	0 Block address within ECC calculation, 1 Block address not within ECC calculation Reset Source: vbus_mod_g_rst_n
2	FSS_AES_EN_IPCFG	R	0h	1 select security, 0 disable security Reset Source: vbus_mod_g_rst_n
1	RESERVED	NONE	0h	Reserved
0	ECC_EN	R/W	0h	0 ECC disabled. 1 ECC enabled Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.2 FSS_FSAS_GENREGS_FRAG_ADR Register

14.7.4.5.2.2.1 FSS_FSAS_GENREGS_FRAG_ADR Register (Offset = 8h) [reset = 0h]

This FRAG_ADR is the address of a request that frag_hi or frag_lo boundary occurs

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Table 14-12982. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0008h

Figure 14-6405. FSS_FSAS_GENREGS_FRAG_ADR Name Register

31	30	29	28	27	26	25	24
FRAG_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
FRAG_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
FRAG_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
FRAG_ADDR							
R/W							
0h							

Table 14-12983. FSS_FSAS_GENREGS_FRAG_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAG_ADDR	R/W	0h	This address is used to determine the boundary of frag_hi and flag_lo Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.3 FSS_FSAS_GENREGS_FRAG_CTL Register

14.7.4.5.2.3.1 FSS_FSAS_GENREGS_FRAG_CTL Register (Offset = Ch) [reset = 3h]

The FRAG_CTL determins which frag region is fragmented

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Table 14-12984. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 000Ch

Figure 14-6406. FSS_FSAS_GENREGS_FRAG_CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>FRAG_HI</td><td>FRAG_LO</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-12985. FSS_FSAS_GENREGS_FRAG_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	FRAG_HI	R/W	1h	When set any address greater than or equal to frag_addr will be fragmented to 16 bits Reset Source: vbus_mod_g_rst_n
0	FRAG_LO	R/W	1h	When set any address less than frag_addr will be fragmented to 16 bits Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.4 FSS_FSAS_GENREGS_IRQ_EOI Register

14.7.4.5.2.4.1 FSS_FSAS_GENREGS_IRQ_EOI Register (Offset = 10h) [reset = 0h]

The End of Interrupt (EOI) MISC Register allows the CPU to acknowledge completion of an interrupt by writing to the EOI for MISC interrupt sources. An eoi_write signal will be generated and another interrupt will be triggered if interrupt sources remain. This register will be reset one cycle after it has been written to.

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Table 14-12986. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0010h + formula

Figure 14-6407. FSS_FSAS_GENREGS_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							R/W
0h							0h

Table 14-12987. FSS_FSAS_GENREGS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	R/W	0h	Write with bit position of targeted interrupt. (E.g. Ext FSS ECC is bit 0). Upon write, level interrupt will clear and if un-serviced will issue another pulse interrupt Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.5 FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register

14.7.4.5.2.5.1 FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register (Offset = 14h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-12988. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0014h + formula

Figure 14-6408. FSS_FSAS_GENREGS_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-12989. FSS_FSAS_GENREGS_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.6 FSS_FSAS_GENREGS_IRQ_STATUS Register

14.7.4.5.2.6.1 FSS_FSAS_GENREGS_IRQ_STATUS Register (Offset = 18h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-12990. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0018h + formula

Figure 14-6409. FSS_FSAS_GENREGS_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-12991. FSS_FSAS_GENREGS_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.7 FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register

14.7.4.5.2.7.1 FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register (Offset = 1Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-12992. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 001Ch + formula

Figure 14-6410. FSS_FSAS_GENREGS_IRQ_ENABLE_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>ECC_WRITE_NONALIGN</td><td>ECC_ERROR_2BIT</td><td>ECC_ERROR_1BIT</td></tr>
<tr><td colspan="5">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-12993. FSS_FSAS_GENREGS_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.8 FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register

14.7.4.5.2.8.1 FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register (Offset = 20h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-12994. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0020h + formula

Figure 14-6411. FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-12995. FSS_FSAS_GENREGS_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B Reset Source: vbus_mod_g_rst_n
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable Reset Source: vbus_mod_g_rst_n
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. correctable Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.9 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J Register

14.7.4.5.2.9.1 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J Register (Offset = 30h) [reset = 0h]

This defines the start of the ECC region in 4KBytes steps.

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Table 14-12996. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0030h + formula

Figure 14-6412. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START							
R/W							
0h							

Table 14-12997. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START	R/W	0h	This defines the start of the ECC region in 4KBytes steps. Address start = {start[19:0], 0x000} 0x0 means the start is 0x0000_0000 0x1 means the start is 0x0000_1000 0xA means the start is 0x0000_A000 Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.10 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J Register

14.7.4.5.2.10.1 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J Register (Offset = 34h) [reset = 0h]

This defines the size of the ECC region in 4KBytes steps.

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Table 14-12998. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0034h + formula

Figure 14-6413. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE							
R/W							
0h							

Table 14-12999. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE	R/W	0h	This defines the size of the ECC region in 4KBytes steps 0x0 means the size is zero and disabled 0x1 means the size is 4KBytes 0xA means the size is 40KBytes 0xF_FFFF means the size is 4GBytes Note the offset + size should be <= 4GBytes, wrap around is not supported. Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.11 FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register

14.7.4.5.2.11.1 FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register (Offset = 70h) [reset = 0h]

The ERR_ECC_BLOCK_ADR register holds the current top of stack ECC error block address, this is only valid when the ecc_err_valid is set

Return to Summary Table

Table 14-13000. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0070h + formula

Figure 14-6414. FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Name Register

31	30	29	28	27	26	25	24
ECC_ERROR_BLOCK_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ERROR_BLOCK_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ERROR_BLOCK_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ERROR_BLOCK_ADDR			RESERVED				
R			NONE				
0h			0h				

Table 14-13001. FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	ECC_ERROR_BLOCK_ADDR	R	0h	ECC 32 byte aligned block address Reset Source: vbus_mod_g_rst_n
4:0	RESERVED	NONE	0h	Reserved

14.7.4.5.2.12 FSS_FSAS_GENREGS_ERR_ECC_TYPE Register

14.7.4.5.2.12.1 FSS_FSAS_GENREGS_ERR_ECC_TYPE Register (Offset = 74h) [reset = 0h]

The ERR_ECC_TYPE register holds the current top of stack ECC error info, this is only valid when the ecc_err_valid is set

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Table 14-13002. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0074h + formula

Figure 14-6415. FSS_FSAS_GENREGS_ERR_ECC_TYPE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>ECC_ERR_VALID</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W1TC</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>ECC_ERR_ADR</td><td>ECC_ERR_MAC</td><td>ECC_ERR_DA1</td><td>ECC_ERR_DA0</td><td>ECC_ERR_DED</td><td>ECC_ERR_SEC</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13003. FSS_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_ERR_VALID	R/W1TC	0h	When set indicates that there is valid ECC error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:6	RESERVED	NONE	0h	Reserved
5	ECC_ERR_ADR	R	0h	When set indicates that there was a single error detected within the address field Reset Source: vbus_mod_g_rst_n
4	ECC_ERR_MAC	R	0h	When set indicates that there was a single error detected within the MAC field Reset Source: vbus_mod_g_rst_n
3	ECC_ERR_DA1	R	0h	When set indicates that there was a single error detected within the High Data word Reset Source: vbus_mod_g_rst_n
2	ECC_ERR_DA0	R	0h	When set indicates that there was a single error detected within the Low Data word Reset Source: vbus_mod_g_rst_n
1	ECC_ERR_DED	R	0h	When set indicates that there was a double error detected for the block Reset Source: vbus_mod_g_rst_n

Table 14-13003. FSS_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECC_ERR_SEC	R	0h	hen set indicates that there was a single error detected for the block Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.13 FSS_FSAS_GENREGS_ERR_WRT_TYPE Register

14.7.4.5.2.13.1 FSS_FSAS_GENREGS_ERR_WRT_TYPE Register (Offset = 78h) [reset = 0h]

The ERR_WRT_TYPE register holds the current top of stack write error info. this is only valid when the wrt_err_valid is set

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Table 14-13004. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FC9 0078h + formula

Figure 14-6416. FSS_FSAS_GENREGS_ERR_WRT_TYPE Name Register

31	30	29	28	27	26	25	24
WRT_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRT_ERR_BEN	WRT_ERR_ADR	WRT_ERR_ROUTEID			
NONE		R	R	R			
0h		0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRT_ERR_ROUTEID							
R							
0h							

Table 14-13005. FSS_FSAS_GENREGS_ERR_WRT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRT_ERR_VALID	R/W1TC	0h	When set indicates that there is valid write error information available, Writing a one to this register will pop the top of the stack Reset Source: vbus_mod_g_rst_n
30:14	RESERVED	NONE	0h	Reserved
13	WRT_ERR_BEN	R	0h	When set indicates that there was a write error due to a non-contiguous byte enables Reset Source: vbus_mod_g_rst_n
12	WRT_ERR_ADR	R	0h	When set indicates that there was a write error due to a non-aligned address Reset Source: vbus_mod_g_rst_n
11:0	WRT_ERR_ROUTEID	R	0h	Indicates the Route ID for the Initiator that caused the write error Reset Source: vbus_mod_g_rst_n

14.7.4.5.2.14 FSS_FSAS_OTFA_REGS_REVID Register

14.7.4.5.2.14.1 FSS_FSAS_OTFA_REGS_REVID Register (Offset = 0h) [reset = 47500100h]

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Table 14-13006. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0000h

Figure 14-6417. FSS_FSAS_OTFA_REGS_REVID Name Register

31	30	29	28	27	26	25	24
REVID							
R							
47500100h							
23	22	21	20	19	18	17	16
REVID							
R							
47500100h							
15	14	13	12	11	10	9	8
REVID							
R							
47500100h							
7	6	5	4	3	2	1	0
REVID							
R							
47500100h							

Table 14-13007. FSS_FSAS_OTFA_REGS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REVID	R	47500100h	REVID Reset Source: rst_modg_rst_n

14.7.4.5.2.15 FSS_FSAS_OTFA_REGS_SCFG Register

14.7.4.5.2.15.1 FSS_FSAS_OTFA_REGS_SCFG Register (Offset = 4h) [reset = 2h]

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Table 14-13008. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0004h

Figure 14-6418. FSS_FSAS_OTFA_REGS_SCFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						IDLE_MODE	
NONE						R/W	
0h						2h	

Table 14-13009. FSS_FSAS_OTFA_REGS_SCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	IDLE_MODE	R/W	2h	IDLE MODE Reset Source: rst_modg_rst_n

14.7.4.5.2.16 FSS_FSAS_OTFA_REGS_ISR Register

14.7.4.5.2.16.1 FSS_FSAS_OTFA_REGS_ISR Register (Offset = 8h) [reset = 0h]

IRQSTATUS_RAW

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Table 14-13010. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0008h

Figure 14-6419. FSS_FSAS_OTFA_REGS_ISR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAC_ERR</td><td colspan="4">WRT_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REGION_BV</td><td colspan="4">CTR_WKV</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13011. FSS_FSAS_OTFA_REGS_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.7.4.5.2.17 FSS_FSAS_OTFA_REGS_IS Register

14.7.4.5.2.17.1 FSS_FSAS_OTFA_REGS_IS Register (Offset = Ch) [reset = 0h]

IRQSTATUS

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Table 14-13012. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 000Ch

Figure 14-6420. FSS_FSAS_OTFA_REGS_IS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAC_ERR</td><td colspan="4">WRT_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REGION_BV</td><td colspan="4">CTR_WKV</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13013. FSS_FSAS_OTFA_REGS_IS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.7.4.5.2.18 FSS_FSAS_OTFA_REGS_IES Register

14.7.4.5.2.18.1 FSS_FSAS_OTFA_REGS_IES Register (Offset = 10h) [reset = 0h]

IRQENABLE_SET

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Table 14-13014. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0010h

Figure 14-6421. FSS_FSAS_OTFA_REGS_IES Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAC_ERR</td><td colspan="4">WRT_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REGION_BV</td><td colspan="4">CTR_WKV</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13015. FSS_FSAS_OTFA_REGS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.7.4.5.2.19 FSS_FSAS_OTFA_REGS_IEC Register

14.7.4.5.2.19.1 FSS_FSAS_OTFA_REGS_IEC Register (Offset = 14h) [reset = 0h]

IRQENABLE_CLR

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Table 14-13016. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0014h

Figure 14-6422. FSS_FSAS_OTFA_REGS_IEC Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">MAC_ERR</td><td colspan="4">WRT_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REGION_BV</td><td colspan="4">CTR_WKV</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13017. FSS_FSAS_OTFA_REGS_IEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	MAC error Reset Source: rst_modg_rst_n
11:8	WRT_ERR	R/W	0h	Write error Reset Source: rst_modg_rst_n
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region Reset Source: rst_modg_rst_n
3:0	CTR_WKV	R/W	0h	AES mode 0 enabled region violated Wrt Once Per Wrt Key rule Reset Source: rst_modg_rst_n

14.7.4.5.2.20 FSS_FSAS_OTFA_REGS_CCFG Register

14.7.4.5.2.20.1 FSS_FSAS_OTFA_REGS_CCFG Register (Offset = 18h) [reset = 0h]

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Table 14-13018. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0018h

Figure 14-6423. FSS_FSAS_OTFA_REGS_CCFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>MASTER_EN_RD</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td>ERROR_RESP_EN</td><td>OTFA_WAIT</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>CACHE_ENABLE</td><td>CACHE_EVICT_MODE</td><td>KEY_SIZE</td><td colspan="4">RD_WRT_OPT</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13019. FSS_FSAS_OTFA_REGS_CCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MASTER_EN_RD	R/W	0h	This register controls the enabling the functionality of this IP Disabled and Bypass mode active Reset Source: rst_modg_rst_n
30:10	RESERVED	NONE	0h	Reserved
9	ERROR_RESP_EN	R/W	0h	This register controls the enabling the the ocp error response for mac errors Reset Source: rst_modg_rst_n
8	OTFA_WAIT	R/W	0h	This register allows the ability to stop accepting any new transactions from getting accepted and allow the current transactions to complete Reset Source: rst_modg_rst_n
7	RESERVED	NONE	0h	Reserved
6	CACHE_ENABLE	R/W	0h	MAC cache enable Reset Source: rst_modg_rst_n
5	CACHE_EVICT_MODE	R/W	0h	cache evict mode Reset Source: rst_modg_rst_n
4	KEY_SIZE	R/W	0h	Key Size, 0 128 Bit 1 256 Bit Reset Source: rst_modg_rst_n

Table 14-13019. FSS_FSAS_OTFA_REGS_CCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RD_WRT_OPT	R/W	0h	This register defines the static allocation of the AES cores to read transactions. The remainder will be allocated to write transactions Reset Source: rst_modg_rst_n

14.7.4.5.2.21 FSS_FSAS_OTFA_REGS_CSTATUS Register

14.7.4.5.2.21.1 FSS_FSAS_OTFA_REGS_CSTATUS Register (Offset = 1Ch) [reset = 0h]

CryptoStatus

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Table 14-13020. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 001Ch

Figure 14-6424. FSS_FSAS_OTFA_REGS_CSTATUS Name Register

31	30	29	28	27	26	25	24
BUSY	CRYPTO_BUSY	RD_STALL_EVENT_CNT					
R	R	R/W1TC					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_STALL_EVENT_CNT							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRT_STALL_EVENT_CNT					
NONE		R/W1TC					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRT_STALL_EVENT_CNT							
R/W1TC							
0h							

Table 14-13021. FSS_FSAS_OTFA_REGS_CSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BUSY	R	0h	0 No transactions are active, crypto or none crypto 1 One or more transactions are active, crypto or none crypto Reset Source: rst_modg_rst_n
30	CRYPTO_BUSY	R	0h	0 No transactions are active, crypto or none crypto 1 One or more transactions are active, crypto or none crypto Reset Source: rst_modg_rst_n
29:16	RD_STALL_EVENT_CNT	R/W1TC	0h	rd stall event do to lack of eng Reset Source: rst_modg_rst_n
15:14	RESERVED	NONE	0h	Reserved
13:0	WRT_STALL_EVENT_CNT	R/W1TC	0h	wrt stall event do to lack of eng Reset Source: rst_modg_rst_n

14.7.4.5.2.22 FSS_FSAS_OTFA_REGS_RGCFG0 Register

14.7.4.5.2.22.1 FSS_FSAS_OTFA_REGS_RGCFG0 Register (Offset = 20h) [reset = 0h]

RegionCfg0

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Table 14-13022. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0020h

Figure 14-6425. FSS_FSAS_OTFA_REGS_RGCFG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT0	MAC_MODE0		AES_MODE0	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-13023. FSS_FSAS_OTFA_REGS_RGCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT0	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE0	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE0	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.7.4.5.2.23 FSS_FSAS_OTFA_REGS_RGMACST0 Register

14.7.4.5.2.23.1 FSS_FSAS_OTFA_REGS_RGMACST0 Register (Offset = 24h) [reset = 0h]

RegionMacStart0

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Table 14-13024. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0024h

Figure 14-6426. FSS_FSAS_OTFA_REGS_RGMACST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START0							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START0							
R/W							
0h							

Table 14-13025. FSS_FSAS_OTFA_REGS_RGMACST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START0	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.24 FSS_FSAS_OTFA_REGS_RGST0 Register

14.7.4.5.2.24.1 FSS_FSAS_OTFA_REGS_RGST0 Register (Offset = 28h) [reset = 0h]

RegionStart0

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Table 14-13026. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0028h

Figure 14-6427. FSS_FSAS_OTFA_REGS_RGST0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R_START0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_START0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_START0							
R/W							
0h							

Table 14-13027. FSS_FSAS_OTFA_REGS_RGST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START0	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.25 FSS_FSAS_OTFA_REGS_RGSI0 Register

14.7.4.5.2.25.1 FSS_FSAS_OTFA_REGS_RGSI0 Register (Offset = 2Ch) [reset = 0h]

RegionSize0

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Table 14-13028. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 002Ch

Figure 14-6428. FSS_FSAS_OTFA_REGS_RGSI0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE0			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE0							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE0							
R/W							
0h							

Table 14-13029. FSS_FSAS_OTFA_REGS_RGSI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE0	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.26 FSS_FSAS_OTFA_REGS_RKEYE00 Register

14.7.4.5.2.26.1 FSS_FSAS_OTFA_REGS_RKEYE00 Register (Offset = 30h) [reset = 0h]

RegionKeyE00

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Table 14-13030. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0030h

Figure 14-6429. FSS_FSAS_OTFA_REGS_RKEYE00 Name Register

31	30	29	28	27	26	25	24
R_KEY_E00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E00							
R/W							
0h							

Table 14-13031. FSS_FSAS_OTFA_REGS_RKEYE00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E00	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.27 FSS_FSAS_OTFA_REGS_RKEYE01 Register

14.7.4.5.2.27.1 FSS_FSAS_OTFA_REGS_RKEYE01 Register (Offset = 34h) [reset = 0h]

RegionKeyE01

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Table 14-13032. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0034h

Figure 14-6430. FSS_FSAS_OTFA_REGS_RKEYE01 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_E01</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_E01</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_E01</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_E01</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13033. FSS_FSAS_OTFA_REGS_RKEYE01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E01	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.28 FSS_FSAS_OTFA_REGS_RKEYE02 Register

14.7.4.5.2.28.1 FSS_FSAS_OTFA_REGS_RKEYE02 Register (Offset = 38h) [reset = 0h]

RegionKeyE02

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Table 14-13034. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0038h

Figure 14-6431. FSS_FSAS_OTFA_REGS_RKEYE02 Name Register

31	30	29	28	27	26	25	24
R_KEY_E02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E02							
R/W							
0h							

Table 14-13035. FSS_FSAS_OTFA_REGS_RKEYE02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E02	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.29 FSS_FSAS_OTFA_REGS_RKEYE03 Register

14.7.4.5.2.29.1 FSS_FSAS_OTFA_REGS_RKEYE03 Register (Offset = 3Ch) [reset = 0h]

RegionKeyE03

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Table 14-13036. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 003Ch

Figure 14-6432. FSS_FSAS_OTFA_REGS_RKEYE03 Name Register

31	30	29	28	27	26	25	24
R_KEY_E03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E03							
R/W							
0h							

Table 14-13037. FSS_FSAS_OTFA_REGS_RKEYE03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E03	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.30 FSS_FSAS_OTFA_REGS_RKEYE04 Register

14.7.4.5.2.30.1 FSS_FSAS_OTFA_REGS_RKEYE04 Register (Offset = 40h) [reset = 0h]

RegionKeyE04

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Table 14-13038. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0040h

Figure 14-6433. FSS_FSAS_OTFA_REGS_RKEYE04 Name Register

31	30	29	28	27	26	25	24
R_KEY_E04							
R/W							
0h							

23	22	21	20	19	18	17	16
R_KEY_E04							
R/W							
0h							

15	14	13	12	11	10	9	8
R_KEY_E04							
R/W							
0h							

7	6	5	4	3	2	1	0
R_KEY_E04							
R/W							
0h							

Table 14-13039. FSS_FSAS_OTFA_REGS_RKEYE04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E04	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.31 FSS_FSAS_OTFA_REGS_RKEYE05 Register

14.7.4.5.2.31.1 FSS_FSAS_OTFA_REGS_RKEYE05 Register (Offset = 44h) [reset = 0h]

RegionKeyE05

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Table 14-13040. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0044h

Figure 14-6434. FSS_FSAS_OTFA_REGS_RKEYE05 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_E05</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_E05</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_E05</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_E05</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13041. FSS_FSAS_OTFA_REGS_RKEYE05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E05	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.32 FSS_FSAS_OTFA_REGS_RKEYE06 Register

14.7.4.5.2.32.1 FSS_FSAS_OTFA_REGS_RKEYE06 Register (Offset = 48h) [reset = 0h]

RegionKeyE06

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Table 14-13042. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0048h

Figure 14-6435. FSS_FSAS_OTFA_REGS_RKEYE06 Name Register

31	30	29	28	27	26	25	24
R_KEY_E06							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_E06							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_E06							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_E06							
R/W							
0h							

Table 14-13043. FSS_FSAS_OTFA_REGS_RKEYE06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E06	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.33 FSS_FSAS_OTFA_REGS_RKEYE07 Register

14.7.4.5.2.33.1 FSS_FSAS_OTFA_REGS_RKEYE07 Register (Offset = 4Ch) [reset = 0h]

RegionKeyE07

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Table 14-13044. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 004Ch

Figure 14-6436. FSS_FSAS_OTFA_REGS_RKEYE07 Name Register

31	30	29	28	27	26	25	24
R_KEY_E07							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E07							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E07							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E07							
R/W							
0h							

Table 14-13045. FSS_FSAS_OTFA_REGS_RKEYE07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E07	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.34 FSS_FSAS_OTFA_REGS_RKEYEP00 Register

14.7.4.5.2.34.1 FSS_FSAS_OTFA_REGS_RKEYEP00 Register (Offset = 50h) [reset = 0h]

RegionKeyEP00

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Table 14-13046. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0050h

Figure 14-6437. FSS_FSAS_OTFA_REGS_RKEYEP00 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP00							
R/W							
0h							

Table 14-13047. FSS_FSAS_OTFA_REGS_RKEYEP00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP00	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.35 FSS_FSAS_OTFA_REGS_RKEYEP01 Register

14.7.4.5.2.35.1 FSS_FSAS_OTFA_REGS_RKEYEP01 Register (Offset = 54h) [reset = 0h]

RegionKeyEP01

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Table 14-13048. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0054h

Figure 14-6438. FSS_FSAS_OTFA_REGS_RKEYEP01 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP01							
R/W							
0h							

Table 14-13049. FSS_FSAS_OTFA_REGS_RKEYEP01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP01	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.36 FSS_FSAS_OTFA_REGS_RKEYEP02 Register

14.7.4.5.2.36.1 FSS_FSAS_OTFA_REGS_RKEYEP02 Register (Offset = 58h) [reset = 0h]

RegionKeyEP02

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Table 14-13050. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0058h

Figure 14-6439. FSS_FSAS_OTFA_REGS_RKEYEP02 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP02							
R/W							
0h							

Table 14-13051. FSS_FSAS_OTFA_REGS_RKEYEP02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP02	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.37 FSS_FSAS_OTFA_REGS_RKEYEP03 Register

14.7.4.5.2.37.1 FSS_FSAS_OTFA_REGS_RKEYEP03 Register (Offset = 5Ch) [reset = 0h]

RegionKeyEP03

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Table 14-13052. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 005Ch

Figure 14-6440. FSS_FSAS_OTFA_REGS_RKEYEP03 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP03							
R/W							
0h							

Table 14-13053. FSS_FSAS_OTFA_REGS_RKEYEP03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP03	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.38 FSS_FSAS_OTFA_REGS_RKEYEP04 Register

14.7.4.5.2.38.1 FSS_FSAS_OTFA_REGS_RKEYEP04 Register (Offset = 60h) [reset = 0h]

RegionKeyEP04

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Table 14-13054. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0060h

Figure 14-6441. FSS_FSAS_OTFA_REGS_RKEYEP04 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP04							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP04							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP04							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP04							
R/W							
0h							

Table 14-13055. FSS_FSAS_OTFA_REGS_RKEYEP04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP04	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.39 FSS_FSAS_OTFA_REGS_RKEYEP05 Register

14.7.4.5.2.39.1 FSS_FSAS_OTFA_REGS_RKEYEP05 Register (Offset = 64h) [reset = 0h]

RegionKeyEP05

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Table 14-13056. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0064h

Figure 14-6442. FSS_FSAS_OTFA_REGS_RKEYEP05 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP05							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP05							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP05							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP05							
R/W							
0h							

Table 14-13057. FSS_FSAS_OTFA_REGS_RKEYEP05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP05	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.40 FSS_FSAS_OTFA_REGS_RKEYEP06 Register

14.7.4.5.2.40.1 FSS_FSAS_OTFA_REGS_RKEYEP06 Register (Offset = 68h) [reset = 0h]

RegionKeyEP06

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Table 14-13058. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0068h

Figure 14-6443. FSS_FSAS_OTFA_REGS_RKEYEP06 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP06							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP06							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP06							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP06							
R/W							
0h							

Table 14-13059. FSS_FSAS_OTFA_REGS_RKEYEP06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP06	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.41 FSS_FSAS_OTFA_REGS_RKEYEP07 Register

14.7.4.5.2.41.1 FSS_FSAS_OTFA_REGS_RKEYEP07 Register (Offset = 6Ch) [reset = 0h]

RegionKeyEP07

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Table 14-13060. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 006Ch

Figure 14-6444. FSS_FSAS_OTFA_REGS_RKEYEP07 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP07							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_EP07							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_EP07							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_EP07							
R/W							
0h							

Table 14-13061. FSS_FSAS_OTFA_REGS_RKEYEP07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP07	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.42 FSS_FSAS_OTFA_REGS_RKEYA00 Register

14.7.4.5.2.42.1 FSS_FSAS_OTFA_REGS_RKEYA00 Register (Offset = 70h) [reset = 0h]

RegionKeyA00

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Table 14-13062. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0070h

Figure 14-6445. FSS_FSAS_OTFA_REGS_RKEYA00 Name Register

31	30	29	28	27	26	25	24
R_KEY_A00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A00							
R/W							
0h							

Table 14-13063. FSS_FSAS_OTFA_REGS_RKEYA00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A00	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.43 FSS_FSAS_OTFA_REGS_RKEYA01 Register

14.7.4.5.2.43.1 FSS_FSAS_OTFA_REGS_RKEYA01 Register (Offset = 74h) [reset = 0h]

RegionKeyA01

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Table 14-13064. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0074h

Figure 14-6446. FSS_FSAS_OTFA_REGS_RKEYA01 Name Register

31	30	29	28	27	26	25	24
R_KEY_A01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A01							
R/W							
0h							

Table 14-13065. FSS_FSAS_OTFA_REGS_RKEYA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A01	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.44 FSS_FSAS_OTFA_REGS_RKEYA02 Register

14.7.4.5.2.44.1 FSS_FSAS_OTFA_REGS_RKEYA02 Register (Offset = 78h) [reset = 0h]

RegionKeyA02

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Table 14-13066. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0078h

Figure 14-6447. FSS_FSAS_OTFA_REGS_RKEYA02 Name Register

31	30	29	28	27	26	25	24
R_KEY_A02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A02							
R/W							
0h							

Table 14-13067. FSS_FSAS_OTFA_REGS_RKEYA02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A02	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.45 FSS_FSAS_OTFA_REGS_RKEYA03 Register

14.7.4.5.2.45.1 FSS_FSAS_OTFA_REGS_RKEYA03 Register (Offset = 7Ch) [reset = 0h]

RegionKeyA03

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Table 14-13068. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 007Ch

Figure 14-6448. FSS_FSAS_OTFA_REGS_RKEYA03 Name Register

31	30	29	28	27	26	25	24
R_KEY_A03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A03							
R/W							
0h							

Table 14-13069. FSS_FSAS_OTFA_REGS_RKEYA03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A03	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.46 FSS_FSAS_OTFA_REGS_RKEYAP00 Register

14.7.4.5.2.46.1 FSS_FSAS_OTFA_REGS_RKEYAP00 Register (Offset = 80h) [reset = 0h]

RegionKeyAP00

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Table 14-13070. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0080h

Figure 14-6449. FSS_FSAS_OTFA_REGS_RKEYAP00 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP00							
R/W							
0h							

Table 14-13071. FSS_FSAS_OTFA_REGS_RKEYAP00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP00	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.47 FSS_FSAS_OTFA_REGS_RKEYAP01 Register

14.7.4.5.2.47.1 FSS_FSAS_OTFA_REGS_RKEYAP01 Register (Offset = 84h) [reset = 0h]

RegionKeyAP01

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Table 14-13072. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0084h

Figure 14-6450. FSS_FSAS_OTFA_REGS_RKEYAP01 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP01							
R/W							
0h							

Table 14-13073. FSS_FSAS_OTFA_REGS_RKEYAP01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP01	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.48 FSS_FSAS_OTFA_REGS_RKEYAP02 Register

14.7.4.5.2.48.1 FSS_FSAS_OTFA_REGS_RKEYAP02 Register (Offset = 88h) [reset = 0h]

RegionKeyAP02

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Table 14-13074. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0088h

Figure 14-6451. FSS_FSAS_OTFA_REGS_RKEYAP02 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP02							
R/W							
0h							

Table 14-13075. FSS_FSAS_OTFA_REGS_RKEYAP02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP02	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.49 FSS_FSAS_OTFA_REGS_RKEYAP03 Register

14.7.4.5.2.49.1 FSS_FSAS_OTFA_REGS_RKEYAP03 Register (Offset = 8Ch) [reset = 0h]

RegionKeyAP03

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Table 14-13076. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 008Ch

Figure 14-6452. FSS_FSAS_OTFA_REGS_RKEYAP03 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP03							
R/W							
0h							

Table 14-13077. FSS_FSAS_OTFA_REGS_RKEYAP03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP03	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.50 FSS_FSAS_OTFA_REGS_RIV00 Register

14.7.4.5.2.50.1 FSS_FSAS_OTFA_REGS_RIV00 Register (Offset = 90h) [reset = 0h]

RegionIV00

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Table 14-13078. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0090h

Figure 14-6453. FSS_FSAS_OTFA_REGS_RIV00 Name Register

31	30	29	28	27	26	25	24
R_IV00							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV00							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV00							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV00							
R/W							
0h							

Table 14-13079. FSS_FSAS_OTFA_REGS_RIV00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV00	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.51 FSS_FSAS_OTFA_REGS_RIV01 Register

14.7.4.5.2.51.1 FSS_FSAS_OTFA_REGS_RIV01 Register (Offset = 94h) [reset = 0h]

RegionIV01

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Table 14-13080. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0094h

Figure 14-6454. FSS_FSAS_OTFA_REGS_RIV01 Name Register

31	30	29	28	27	26	25	24
R_IV01							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV01							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV01							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV01							
R/W							
0h							

Table 14-13081. FSS_FSAS_OTFA_REGS_RIV01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV01	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.52 FSS_FSAS_OTFA_REGS_RIV02 Register

14.7.4.5.2.52.1 FSS_FSAS_OTFA_REGS_RIV02 Register (Offset = 98h) [reset = 0h]

RegionIV02

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Table 14-13082. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0098h

Figure 14-6455. FSS_FSAS_OTFA_REGS_RIV02 Name Register

31	30	29	28	27	26	25	24
R_IV02							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV02							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV02							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV02							
R/W							
0h							

Table 14-13083. FSS_FSAS_OTFA_REGS_RIV02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV02	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.53 FSS_FSAS_OTFA_REGS_RIV03 Register

14.7.4.5.2.53.1 FSS_FSAS_OTFA_REGS_RIV03 Register (Offset = 9Ch) [reset = 0h]

RegionIV03

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Table 14-13084. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 009Ch

Figure 14-6456. FSS_FSAS_OTFA_REGS_RIV03 Name Register

31	30	29	28	27	26	25	24
R_IV03							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV03							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV03							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV03							
R/W							
0h							

Table 14-13085. FSS_FSAS_OTFA_REGS_RIV03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV03	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.54 FSS_FSAS_OTFA_REGS_RGCFG1 Register

14.7.4.5.2.54.1 FSS_FSAS_OTFA_REGS_RGCFG1 Register (Offset = A0h) [reset = 0h]

RegionCfg1

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Table 14-13086. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00A0h

Figure 14-6457. FSS_FSAS_OTFA_REGS_RGCFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT1	MAC_MODE1		AES_MODE1	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-13087. FSS_FSAS_OTFA_REGS_RGCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT1	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE1	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE1	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.7.4.5.2.55 FSS_FSAS_OTFA_REGS_RGMACST1 Register

14.7.4.5.2.55.1 FSS_FSAS_OTFA_REGS_RGMACST1 Register (Offset = A4h) [reset = 0h]

RegionMacStart1

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Table 14-13088. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00A4h

Figure 14-6458. FSS_FSAS_OTFA_REGS_RGMACST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				M_START1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
M_START1							
R/W							
0h							
7	6	5	4	3	2	1	0
M_START1							
R/W							
0h							

Table 14-13089. FSS_FSAS_OTFA_REGS_RGMACST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START1	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.56 FSS_FSAS_OTFA_REGS_RGST1 Register

14.7.4.5.2.56.1 FSS_FSAS_OTFA_REGS_RGST1 Register (Offset = A8h) [reset = 0h]

RegionStart1

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Table 14-13090. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00A8h

Figure 14-6459. FSS_FSAS_OTFA_REGS_RGST1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R_START1			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_START1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_START1							
R/W							
0h							

Table 14-13091. FSS_FSAS_OTFA_REGS_RGST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START1	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.57 FSS_FSAS_OTFA_REGS_RGSI1 Register

14.7.4.5.2.57.1 FSS_FSAS_OTFA_REGS_RGSI1 Register (Offset = ACh) [reset = 0h]

RegionSize1

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Table 14-13092. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00ACh

Figure 14-6460. FSS_FSAS_OTFA_REGS_RGSI1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE1							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE1							
R/W							
0h							

Table 14-13093. FSS_FSAS_OTFA_REGS_RGSI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE1	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.58 FSS_FSAS_OTFA_REGS_RKEYE10 Register

14.7.4.5.2.58.1 FSS_FSAS_OTFA_REGS_RKEYE10 Register (Offset = B0h) [reset = 0h]

RegionKeyE10

Return to Summary Table

Table 14-13094. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00B0h

Figure 14-6461. FSS_FSAS_OTFA_REGS_RKEYE10 Name Register

31	30	29	28	27	26	25	24
R_KEY_E10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E10							
R/W							
0h							

Table 14-13095. FSS_FSAS_OTFA_REGS_RKEYE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E10	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.59 FSS_FSAS_OTFA_REGS_RKEYE11 Register

14.7.4.5.2.59.1 FSS_FSAS_OTFA_REGS_RKEYE11 Register (Offset = B4h) [reset = 0h]

RegionKeyE11

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Table 14-13096. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00B4h

Figure 14-6462. FSS_FSAS_OTFA_REGS_RKEYE11 Name Register

31	30	29	28	27	26	25	24
R_KEY_E11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E11							
R/W							
0h							

Table 14-13097. FSS_FSAS_OTFA_REGS_RKEYE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E11	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.60 FSS_FSAS_OTFA_REGS_RKEYE12 Register

14.7.4.5.2.60.1 FSS_FSAS_OTFA_REGS_RKEYE12 Register (Offset = B8h) [reset = 0h]

RegionKeyE12

Return to Summary Table

Table 14-13098. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00B8h

Figure 14-6463. FSS_FSAS_OTFA_REGS_RKEYE12 Name Register

31	30	29	28	27	26	25	24
R_KEY_E12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E12							
R/W							
0h							

Table 14-13099. FSS_FSAS_OTFA_REGS_RKEYE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E12	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.61 FSS_FSAS_OTFA_REGS_RKEYE13 Register

14.7.4.5.2.61.1 FSS_FSAS_OTFA_REGS_RKEYE13 Register (Offset = BCh) [reset = 0h]

RegionKeyE13

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Table 14-13100. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00BCh

Figure 14-6464. FSS_FSAS_OTFA_REGS_RKEYE13 Name Register

31	30	29	28	27	26	25	24
R_KEY_E13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E13							
R/W							
0h							

Table 14-13101. FSS_FSAS_OTFA_REGS_RKEYE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E13	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.62 FSS_FSAS_OTFA_REGS_RKEYE14 Register

14.7.4.5.2.62.1 FSS_FSAS_OTFA_REGS_RKEYE14 Register (Offset = C0h) [reset = 0h]

RegionKeyE14

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Table 14-13102. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00C0h

Figure 14-6465. FSS_FSAS_OTFA_REGS_RKEYE14 Name Register

31	30	29	28	27	26	25	24
R_KEY_E14							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E14							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E14							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E14							
R/W							
0h							

Table 14-13103. FSS_FSAS_OTFA_REGS_RKEYE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E14	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.63 FSS_FSAS_OTFA_REGS_RKEYE15 Register

14.7.4.5.2.63.1 FSS_FSAS_OTFA_REGS_RKEYE15 Register (Offset = C4h) [reset = 0h]

RegionKeyE15

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Table 14-13104. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00C4h

Figure 14-6466. FSS_FSAS_OTFA_REGS_RKEYE15 Name Register

31	30	29	28	27	26	25	24
R_KEY_E15							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E15							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E15							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E15							
R/W							
0h							

Table 14-13105. FSS_FSAS_OTFA_REGS_RKEYE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E15	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.64 FSS_FSAS_OTFA_REGS_RKEYE16 Register

14.7.4.5.2.64.1 FSS_FSAS_OTFA_REGS_RKEYE16 Register (Offset = C8h) [reset = 0h]

RegionKeyE16

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Table 14-13106. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00C8h

Figure 14-6467. FSS_FSAS_OTFA_REGS_RKEYE16 Name Register

31	30	29	28	27	26	25	24
R_KEY_E16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_E16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_E16							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_E16							
R/W							
0h							

Table 14-13107. FSS_FSAS_OTFA_REGS_RKEYE16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E16	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.65 FSS_FSAS_OTFA_REGS_RKEYE17 Register

14.7.4.5.2.65.1 FSS_FSAS_OTFA_REGS_RKEYE17 Register (Offset = CCh) [reset = 0h]

RegionKeyE17

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Table 14-13108. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00CCh

Figure 14-6468. FSS_FSAS_OTFA_REGS_RKEYE17 Name Register

31	30	29	28	27	26	25	24
R_KEY_E17							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_E17							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_E17							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_E17							
R/W							
0h							

Table 14-13109. FSS_FSAS_OTFA_REGS_RKEYE17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E17	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.66 FSS_FSAS_OTFA_REGS_RKEYEP10 Register

14.7.4.5.2.66.1 FSS_FSAS_OTFA_REGS_RKEYEP10 Register (Offset = D0h) [reset = 0h]

RegionKeyEP10

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Table 14-13110. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00D0h

Figure 14-6469. FSS_FSAS_OTFA_REGS_RKEYEP10 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP10							
R/W							
0h							

Table 14-13111. FSS_FSAS_OTFA_REGS_RKEYEP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP10	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.67 FSS_FSAS_OTFA_REGS_RKEYEP11 Register

14.7.4.5.2.67.1 FSS_FSAS_OTFA_REGS_RKEYEP11 Register (Offset = D4h) [reset = 0h]

RegionKeyEP11

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Table 14-13112. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00D4h

Figure 14-6470. FSS_FSAS_OTFA_REGS_RKEYEP11 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP11							
R/W							
0h							

Table 14-13113. FSS_FSAS_OTFA_REGS_RKEYEP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP11	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.68 FSS_FSAS_OTFA_REGS_RKEYEP12 Register

14.7.4.5.2.68.1 FSS_FSAS_OTFA_REGS_RKEYEP12 Register (Offset = D8h) [reset = 0h]

RegionKeyEP12

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Table 14-13114. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00D8h

Figure 14-6471. FSS_FSAS_OTFA_REGS_RKEYEP12 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP12							
R/W							
0h							

Table 14-13115. FSS_FSAS_OTFA_REGS_RKEYEP12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP12	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.69 FSS_FSAS_OTFA_REGS_RKEYEP13 Register

14.7.4.5.2.69.1 FSS_FSAS_OTFA_REGS_RKEYEP13 Register (Offset = DCh) [reset = 0h]

RegionKeyEP13

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Table 14-13116. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00DCh

Figure 14-6472. FSS_FSAS_OTFA_REGS_RKEYEP13 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP13							
R/W							
0h							

Table 14-13117. FSS_FSAS_OTFA_REGS_RKEYEP13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP13	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.70 FSS_FSAS_OTFA_REGS_RKEYEP14 Register

14.7.4.5.2.70.1 FSS_FSAS_OTFA_REGS_RKEYEP14 Register (Offset = E0h) [reset = 0h]

RegionKeyEP14

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Table 14-13118. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00E0h

Figure 14-6473. FSS_FSAS_OTFA_REGS_RKEYEP14 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP14							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP14							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP14							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP14							
R/W							
0h							

Table 14-13119. FSS_FSAS_OTFA_REGS_RKEYEP14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP14	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.71 FSS_FSAS_OTFA_REGS_RKEYEP15 Register

14.7.4.5.2.71.1 FSS_FSAS_OTFA_REGS_RKEYEP15 Register (Offset = E4h) [reset = 0h]

RegionKeyEP15

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Table 14-13120. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00E4h

Figure 14-6474. FSS_FSAS_OTFA_REGS_RKEYEP15 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP15							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP15							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP15							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP15							
R/W							
0h							

Table 14-13121. FSS_FSAS_OTFA_REGS_RKEYEP15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP15	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.72 FSS_FSAS_OTFA_REGS_RKEYEP16 Register

14.7.4.5.2.72.1 FSS_FSAS_OTFA_REGS_RKEYEP16 Register (Offset = E8h) [reset = 0h]

RegionKeyEP16

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Table 14-13122. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00E8h

Figure 14-6475. FSS_FSAS_OTFA_REGS_RKEYEP16 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP16							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP16							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP16							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP16							
R/W							
0h							

Table 14-13123. FSS_FSAS_OTFA_REGS_RKEYEP16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP16	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.73 FSS_FSAS_OTFA_REGS_RKEYEP17 Register

14.7.4.5.2.73.1 FSS_FSAS_OTFA_REGS_RKEYEP17 Register (Offset = ECh) [reset = 0h]

RegionKeyEP17

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Table 14-13124. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00ECh

Figure 14-6476. FSS_FSAS_OTFA_REGS_RKEYEP17 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP17							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP17							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP17							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP17							
R/W							
0h							

Table 14-13125. FSS_FSAS_OTFA_REGS_RKEYEP17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP17	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.74 FSS_FSAS_OTFA_REGS_RKEYA10 Register

14.7.4.5.2.74.1 FSS_FSAS_OTFA_REGS_RKEYA10 Register (Offset = F0h) [reset = 0h]

RegionKeyA10

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Table 14-13126. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00F0h

Figure 14-6477. FSS_FSAS_OTFA_REGS_RKEYA10 Name Register

31	30	29	28	27	26	25	24
R_KEY_A10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A10							
R/W							
0h							

Table 14-13127. FSS_FSAS_OTFA_REGS_RKEYA10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A10	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.75 FSS_FSAS_OTFA_REGS_RKEYA11 Register

14.7.4.5.2.75.1 FSS_FSAS_OTFA_REGS_RKEYA11 Register (Offset = F4h) [reset = 0h]

RegionKeyA11

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Table 14-13128. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00F4h

Figure 14-6478. FSS_FSAS_OTFA_REGS_RKEYA11 Name Register

31	30	29	28	27	26	25	24
R_KEY_A11							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A11							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A11							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A11							
R/W							
0h							

Table 14-13129. FSS_FSAS_OTFA_REGS_RKEYA11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A11	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.76 FSS_FSAS_OTFA_REGS_RKEYA12 Register

14.7.4.5.2.76.1 FSS_FSAS_OTFA_REGS_RKEYA12 Register (Offset = F8h) [reset = 0h]

RegionKeyA12

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Table 14-13130. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00F8h

Figure 14-6479. FSS_FSAS_OTFA_REGS_RKEYA12 Name Register

31	30	29	28	27	26	25	24
R_KEY_A12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A12							
R/W							
0h							

Table 14-13131. FSS_FSAS_OTFA_REGS_RKEYA12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A12	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.77 FSS_FSAS_OTFA_REGS_RKEYA13 Register

14.7.4.5.2.77.1 FSS_FSAS_OTFA_REGS_RKEYA13 Register (Offset = FCh) [reset = 0h]

RegionKeyA13

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Table 14-13132. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 00FCh

Figure 14-6480. FSS_FSAS_OTFA_REGS_RKEYA13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_A13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_A13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_A13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_A13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13133. FSS_FSAS_OTFA_REGS_RKEYA13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A13	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.78 FSS_FSAS_OTFA_REGS_RKEYAP10 Register

14.7.4.5.2.78.1 FSS_FSAS_OTFA_REGS_RKEYAP10 Register (Offset = 100h) [reset = 0h]

RegionKeyAP10

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Table 14-13134. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0100h

Figure 14-6481. FSS_FSAS_OTFA_REGS_RKEYAP10 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP10							
R/W							
0h							

Table 14-13135. FSS_FSAS_OTFA_REGS_RKEYAP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP10	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.79 FSS_FSAS_OTFA_REGS_RKEYAP11 Register

14.7.4.5.2.79.1 FSS_FSAS_OTFA_REGS_RKEYAP11 Register (Offset = 104h) [reset = 0h]

RegionKeyAP11

Return to Summary Table

Table 14-13136. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0104h

Figure 14-6482. FSS_FSAS_OTFA_REGS_RKEYAP11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_AP11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_AP11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_AP11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_AP11</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13137. FSS_FSAS_OTFA_REGS_RKEYAP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP11	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.80 FSS_FSAS_OTFA_REGS_RKEYAP12 Register

14.7.4.5.2.80.1 FSS_FSAS_OTFA_REGS_RKEYAP12 Register (Offset = 108h) [reset = 0h]

RegionKeyAP12

Return to Summary Table

Table 14-13138. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0108h

Figure 14-6483. FSS_FSAS_OTFA_REGS_RKEYAP12 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP12							
R/W							
0h							

Table 14-13139. FSS_FSAS_OTFA_REGS_RKEYAP12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP12	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.81 FSS_FSAS_OTFA_REGS_RKEYAP13 Register

14.7.4.5.2.81.1 FSS_FSAS_OTFA_REGS_RKEYAP13 Register (Offset = 10Ch) [reset = 0h]

RegionKeyAP13

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Table 14-13140. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 010Ch

Figure 14-6484. FSS_FSAS_OTFA_REGS_RKEYAP13 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP13							
R/W							
0h							

Table 14-13141. FSS_FSAS_OTFA_REGS_RKEYAP13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP13	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.82 FSS_FSAS_OTFA_REGS_RIV10 Register

14.7.4.5.2.82.1 FSS_FSAS_OTFA_REGS_RIV10 Register (Offset = 110h) [reset = 0h]

RegionIV10

Return to Summary Table

Table 14-13142. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0110h

Figure 14-6485. FSS_FSAS_OTFA_REGS_RIV10 Name Register

31	30	29	28	27	26	25	24
R_IV10							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV10							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV10							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV10							
R/W							
0h							

Table 14-13143. FSS_FSAS_OTFA_REGS_RIV10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV10	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.83 FSS_FSAS_OTFA_REGS_RIV11 Register

14.7.4.5.2.83.1 FSS_FSAS_OTFA_REGS_RIV11 Register (Offset = 114h) [reset = 0h]

RegionIV11

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Table 14-13144. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0114h

Figure 14-6486. FSS_FSAS_OTFA_REGS_RIV11 Name Register

31	30	29	28	27	26	25	24
R_IV11							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_IV11							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_IV11							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_IV11							
R/W							
0h							

Table 14-13145. FSS_FSAS_OTFA_REGS_RIV11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV11	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.84 FSS_FSAS_OTFA_REGS_RIV12 Register

14.7.4.5.2.84.1 FSS_FSAS_OTFA_REGS_RIV12 Register (Offset = 118h) [reset = 0h]

RegionIV12

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Table 14-13146. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0118h

Figure 14-6487. FSS_FSAS_OTFA_REGS_RIV12 Name Register

31	30	29	28	27	26	25	24
R_IV12							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV12							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV12							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV12							
R/W							
0h							

Table 14-13147. FSS_FSAS_OTFA_REGS_RIV12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV12	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.85 FSS_FSAS_OTFA_REGS_RIV13 Register

14.7.4.5.2.85.1 FSS_FSAS_OTFA_REGS_RIV13 Register (Offset = 11Ch) [reset = 0h]

RegionIV13

Return to Summary Table

Table 14-13148. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 011Ch

Figure 14-6488. FSS_FSAS_OTFA_REGS_RIV13 Name Register

31	30	29	28	27	26	25	24
R_IV13							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV13							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV13							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV13							
R/W							
0h							

Table 14-13149. FSS_FSAS_OTFA_REGS_RIV13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV13	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.86 FSS_FSAS_OTFA_REGS_RGCFG2 Register

14.7.4.5.2.86.1 FSS_FSAS_OTFA_REGS_RGCFG2 Register (Offset = 120h) [reset = 0h]

RegionCfg2

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Table 14-13150. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0120h

Figure 14-6489. FSS_FSAS_OTFA_REGS_RGCFG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT2	MAC_MODE2		AES_MODE2	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 14-13151. FSS_FSAS_OTFA_REGS_RGCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT2	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE2	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE2	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.7.4.5.2.87 FSS_FSAS_OTFA_REGS_RGMACST2 Register

14.7.4.5.2.87.1 FSS_FSAS_OTFA_REGS_RGMACST2 Register (Offset = 124h) [reset = 0h]

RegionMacStart2

Return to Summary Table

Table 14-13152. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0124h

Figure 14-6490. FSS_FSAS_OTFA_REGS_RGMACST2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">M_START2</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">M_START2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">M_START2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13153. FSS_FSAS_OTFA_REGS_RGMACST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START2	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.88 FSS_FSAS_OTFA_REGS_RGST2 Register

14.7.4.5.2.88.1 FSS_FSAS_OTFA_REGS_RGST2 Register (Offset = 128h) [reset = 0h]

RegionStart2

Return to Summary Table

Table 14-13154. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0128h

Figure 14-6491. FSS_FSAS_OTFA_REGS_RGST2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START2							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START2							
R/W							
0h							

Table 14-13155. FSS_FSAS_OTFA_REGS_RGST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START2	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.89 FSS_FSAS_OTFA_REGS_RGSI2 Register

14.7.4.5.2.89.1 FSS_FSAS_OTFA_REGS_RGSI2 Register (Offset = 12Ch) [reset = 0h]

RegionSize2

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Table 14-13156. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 012Ch

Figure 14-6492. FSS_FSAS_OTFA_REGS_RGSI2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE2							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE2							
R/W							
0h							

Table 14-13157. FSS_FSAS_OTFA_REGS_RGSI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE2	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.90 FSS_FSAS_OTFA_REGS_RKEYE20 Register

14.7.4.5.2.90.1 FSS_FSAS_OTFA_REGS_RKEYE20 Register (Offset = 130h) [reset = 0h]

RegionKeyE20

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Table 14-13158. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0130h

Figure 14-6493. FSS_FSAS_OTFA_REGS_RKEYE20 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_E20</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_E20</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_E20</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_E20</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13159. FSS_FSAS_OTFA_REGS_RKEYE20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E20	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.91 FSS_FSAS_OTFA_REGS_RKEYE21 Register

14.7.4.5.2.91.1 FSS_FSAS_OTFA_REGS_RKEYE21 Register (Offset = 134h) [reset = 0h]

RegionKeyE21

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Table 14-13160. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0134h

Figure 14-6494. FSS_FSAS_OTFA_REGS_RKEYE21 Name Register

31	30	29	28	27	26	25	24
R_KEY_E21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E21							
R/W							
0h							

Table 14-13161. FSS_FSAS_OTFA_REGS_RKEYE21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E21	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.92 FSS_FSAS_OTFA_REGS_RKEYE22 Register

14.7.4.5.2.92.1 FSS_FSAS_OTFA_REGS_RKEYE22 Register (Offset = 138h) [reset = 0h]

RegionKeyE22

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Table 14-13162. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0138h

Figure 14-6495. FSS_FSAS_OTFA_REGS_RKEYE22 Name Register

31	30	29	28	27	26	25	24
R_KEY_E22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E22							
R/W							
0h							

Table 14-13163. FSS_FSAS_OTFA_REGS_RKEYE22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E22	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.93 FSS_FSAS_OTFA_REGS_RKEYE23 Register

14.7.4.5.2.93.1 FSS_FSAS_OTFA_REGS_RKEYE23 Register (Offset = 13Ch) [reset = 0h]

RegionKeyE23

Return to Summary Table

Table 14-13164. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 013Ch

Figure 14-6496. FSS_FSAS_OTFA_REGS_RKEYE23 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_E23</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_E23</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_E23</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_E23</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13165. FSS_FSAS_OTFA_REGS_RKEYE23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E23	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.94 FSS_FSAS_OTFA_REGS_RKEYE24 Register

14.7.4.5.2.94.1 FSS_FSAS_OTFA_REGS_RKEYE24 Register (Offset = 140h) [reset = 0h]

RegionKeyE24

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Table 14-13166. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0140h

Figure 14-6497. FSS_FSAS_OTFA_REGS_RKEYE24 Name Register

31	30	29	28	27	26	25	24
R_KEY_E24							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E24							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E24							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E24							
R/W							
0h							

Table 14-13167. FSS_FSAS_OTFA_REGS_RKEYE24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E24	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.95 FSS_FSAS_OTFA_REGS_RKEYE25 Register

14.7.4.5.2.95.1 FSS_FSAS_OTFA_REGS_RKEYE25 Register (Offset = 144h) [reset = 0h]

RegionKeyE25

Return to Summary Table

Table 14-13168. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0144h

Figure 14-6498. FSS_FSAS_OTFA_REGS_RKEYE25 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_E25</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_E25</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_E25</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_E25</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13169. FSS_FSAS_OTFA_REGS_RKEYE25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E25	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.96 FSS_FSAS_OTFA_REGS_RKEYE26 Register

14.7.4.5.2.96.1 FSS_FSAS_OTFA_REGS_RKEYE26 Register (Offset = 148h) [reset = 0h]

RegionKeyE26

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Table 14-13170. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0148h

Figure 14-6499. FSS_FSAS_OTFA_REGS_RKEYE26 Name Register

31	30	29	28	27	26	25	24
R_KEY_E26							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E26							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E26							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E26							
R/W							
0h							

Table 14-13171. FSS_FSAS_OTFA_REGS_RKEYE26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E26	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.97 FSS_FSAS_OTFA_REGS_RKEYE27 Register

14.7.4.5.2.97.1 FSS_FSAS_OTFA_REGS_RKEYE27 Register (Offset = 14Ch) [reset = 0h]

RegionKeyE27

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Table 14-13172. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 014Ch

Figure 14-6500. FSS_FSAS_OTFA_REGS_RKEYE27 Name Register

31	30	29	28	27	26	25	24
R_KEY_E27							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E27							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E27							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E27							
R/W							
0h							

Table 14-13173. FSS_FSAS_OTFA_REGS_RKEYE27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E27	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.98 FSS_FSAS_OTFA_REGS_RKEYEP20 Register

14.7.4.5.2.98.1 FSS_FSAS_OTFA_REGS_RKEYEP20 Register (Offset = 150h) [reset = 0h]

RegionKeyEP20

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Table 14-13174. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0150h

Figure 14-6501. FSS_FSAS_OTFA_REGS_RKEYEP20 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP20							
R/W							
0h							

Table 14-13175. FSS_FSAS_OTFA_REGS_RKEYEP20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP20	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.99 FSS_FSAS_OTFA_REGS_RKEYEP21 Register

14.7.4.5.2.99.1 FSS_FSAS_OTFA_REGS_RKEYEP21 Register (Offset = 154h) [reset = 0h]

RegionKeyEP21

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Table 14-13176. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0154h

Figure 14-6502. FSS_FSAS_OTFA_REGS_RKEYEP21 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP21							
R/W							
0h							

Table 14-13177. FSS_FSAS_OTFA_REGS_RKEYEP21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP21	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.100 FSS_FSAS_OTFA_REGS_RKEYEP22 Register

14.7.4.5.2.100.1 FSS_FSAS_OTFA_REGS_RKEYEP22 Register (Offset = 158h) [reset = 0h]

RegionKeyEP22

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Table 14-13178. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0158h

Figure 14-6503. FSS_FSAS_OTFA_REGS_RKEYEP22 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP22							
R/W							
0h							

Table 14-13179. FSS_FSAS_OTFA_REGS_RKEYEP22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP22	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.101 FSS_FSAS_OTFA_REGS_RKEYEP23 Register

14.7.4.5.2.101.1 FSS_FSAS_OTFA_REGS_RKEYEP23 Register (Offset = 15Ch) [reset = 0h]

RegionKeyEP23

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Table 14-13180. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 015Ch

Figure 14-6504. FSS_FSAS_OTFA_REGS_RKEYEP23 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP23							
R/W							
0h							

Table 14-13181. FSS_FSAS_OTFA_REGS_RKEYEP23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP23	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.102 FSS_FSAS_OTFA_REGS_RKEYEP24 Register

14.7.4.5.2.102.1 FSS_FSAS_OTFA_REGS_RKEYEP24 Register (Offset = 160h) [reset = 0h]

RegionKeyEP24

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Table 14-13182. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0160h

Figure 14-6505. FSS_FSAS_OTFA_REGS_RKEYEP24 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP24							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP24							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP24							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP24							
R/W							
0h							

Table 14-13183. FSS_FSAS_OTFA_REGS_RKEYEP24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP24	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.103 FSS_FSAS_OTFA_REGS_RKEYEP25 Register

14.7.4.5.2.103.1 FSS_FSAS_OTFA_REGS_RKEYEP25 Register (Offset = 164h) [reset = 0h]

RegionKeyEP25

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Table 14-13184. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0164h

Figure 14-6506. FSS_FSAS_OTFA_REGS_RKEYEP25 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP25							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP25							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP25							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP25							
R/W							
0h							

Table 14-13185. FSS_FSAS_OTFA_REGS_RKEYEP25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP25	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.104 FSS_FSAS_OTFA_REGS_RKEYEP26 Register

14.7.4.5.2.104.1 FSS_FSAS_OTFA_REGS_RKEYEP26 Register (Offset = 168h) [reset = 0h]

RegionKeyEP26

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Table 14-13186. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0168h

Figure 14-6507. FSS_FSAS_OTFA_REGS_RKEYEP26 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP26							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP26							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP26							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP26							
R/W							
0h							

Table 14-13187. FSS_FSAS_OTFA_REGS_RKEYEP26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP26	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.105 FSS_FSAS_OTFA_REGS_RKEYEP27 Register

14.7.4.5.2.105.1 FSS_FSAS_OTFA_REGS_RKEYEP27 Register (Offset = 16Ch) [reset = 0h]

RegionKeyEP27

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Table 14-13188. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 016Ch

Figure 14-6508. FSS_FSAS_OTFA_REGS_RKEYEP27 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP27							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP27							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP27							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP27							
R/W							
0h							

Table 14-13189. FSS_FSAS_OTFA_REGS_RKEYEP27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP27	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.106 FSS_FSAS_OTFA_REGS_RKEYA20 Register

14.7.4.5.2.106.1 FSS_FSAS_OTFA_REGS_RKEYA20 Register (Offset = 170h) [reset = 0h]

RegionKeyA20

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Table 14-13190. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0170h

Figure 14-6509. FSS_FSAS_OTFA_REGS_RKEYA20 Name Register

31	30	29	28	27	26	25	24
R_KEY_A20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A20							
R/W							
0h							

Table 14-13191. FSS_FSAS_OTFA_REGS_RKEYA20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A20	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.107 FSS_FSAS_OTFA_REGS_RKEYA21 Register

14.7.4.5.2.107.1 FSS_FSAS_OTFA_REGS_RKEYA21 Register (Offset = 174h) [reset = 0h]

RegionKeyA21

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Table 14-13192. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0174h

Figure 14-6510. FSS_FSAS_OTFA_REGS_RKEYA21 Name Register

31	30	29	28	27	26	25	24
R_KEY_A21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A21							
R/W							
0h							

Table 14-13193. FSS_FSAS_OTFA_REGS_RKEYA21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A21	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.108 FSS_FSAS_OTFA_REGS_RKEYA22 Register

14.7.4.5.2.108.1 FSS_FSAS_OTFA_REGS_RKEYA22 Register (Offset = 178h) [reset = 0h]

RegionKeyA22

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Table 14-13194. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0178h

Figure 14-6511. FSS_FSAS_OTFA_REGS_RKEYA22 Name Register

31	30	29	28	27	26	25	24
R_KEY_A22							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A22							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A22							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A22							
R/W							
0h							

Table 14-13195. FSS_FSAS_OTFA_REGS_RKEYA22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A22	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.109 FSS_FSAS_OTFA_REGS_RKEYA23 Register

14.7.4.5.2.109.1 FSS_FSAS_OTFA_REGS_RKEYA23 Register (Offset = 17Ch) [reset = 0h]

RegionKeyA23

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Table 14-13196. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 017Ch

Figure 14-6512. FSS_FSAS_OTFA_REGS_RKEYA23 Name Register

31	30	29	28	27	26	25	24
R_KEY_A23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A23							
R/W							
0h							

Table 14-13197. FSS_FSAS_OTFA_REGS_RKEYA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A23	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.110 FSS_FSAS_OTFA_REGS_RKEYAP20 Register

14.7.4.5.2.110.1 FSS_FSAS_OTFA_REGS_RKEYAP20 Register (Offset = 180h) [reset = 0h]

RegionKeyAP20

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Table 14-13198. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0180h

Figure 14-6513. FSS_FSAS_OTFA_REGS_RKEYAP20 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP20							
R/W							
0h							

Table 14-13199. FSS_FSAS_OTFA_REGS_RKEYAP20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP20	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.111 FSS_FSAS_OTFA_REGS_RKEYAP21 Register

14.7.4.5.2.111.1 FSS_FSAS_OTFA_REGS_RKEYAP21 Register (Offset = 184h) [reset = 0h]

RegionKeyAP21

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Table 14-13200. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0184h

Figure 14-6514. FSS_FSAS_OTFA_REGS_RKEYAP21 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP21							
R/W							
0h							

Table 14-13201. FSS_FSAS_OTFA_REGS_RKEYAP21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP21	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.112 FSS_FSAS_OTFA_REGS_RKEYAP22 Register

14.7.4.5.2.112.1 FSS_FSAS_OTFA_REGS_RKEYAP22 Register (Offset = 188h) [reset = 0h]

RegionKeyAP22

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Table 14-13202. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0188h

Figure 14-6515. FSS_FSAS_OTFA_REGS_RKEYAP22 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_AP22							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_AP22							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_AP22							
R/W							
0h							

Table 14-13203. FSS_FSAS_OTFA_REGS_RKEYAP22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP22	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.113 FSS_FSAS_OTFA_REGS_RKEYAP23 Register

14.7.4.5.2.113.1 FSS_FSAS_OTFA_REGS_RKEYAP23 Register (Offset = 18Ch) [reset = 0h]

RegionKeyAP23

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Table 14-13204. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 018Ch

Figure 14-6516. FSS_FSAS_OTFA_REGS_RKEYAP23 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP23							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_KEY_AP23							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_KEY_AP23							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_KEY_AP23							
R/W							
0h							

Table 14-13205. FSS_FSAS_OTFA_REGS_RKEYAP23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP23	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.114 FSS_FSAS_OTFA_REGS_RIV20 Register

14.7.4.5.2.114.1 FSS_FSAS_OTFA_REGS_RIV20 Register (Offset = 190h) [reset = 0h]

RegionIV20

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Table 14-13206. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0190h

Figure 14-6517. FSS_FSAS_OTFA_REGS_RIV20 Name Register

31	30	29	28	27	26	25	24
R_IV20							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV20							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV20							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV20							
R/W							
0h							

Table 14-13207. FSS_FSAS_OTFA_REGS_RIV20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV20	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.115 FSS_FSAS_OTFA_REGS_RIV21 Register

14.7.4.5.2.115.1 FSS_FSAS_OTFA_REGS_RIV21 Register (Offset = 194h) [reset = 0h]

RegionIV21

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Table 14-13208. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0194h

Figure 14-6518. FSS_FSAS_OTFA_REGS_RIV21 Name Register

31	30	29	28	27	26	25	24
R_IV21							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV21							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV21							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV21							
R/W							
0h							

Table 14-13209. FSS_FSAS_OTFA_REGS_RIV21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV21	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.116 FSS_FSAS_OTFA_REGS_RIV22 Register

14.7.4.5.2.116.1 FSS_FSAS_OTFA_REGS_RIV22 Register (Offset = 198h) [reset = 0h]

RegionIV22

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Table 14-13210. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0198h

Figure 14-6519. FSS_FSAS_OTFA_REGS_RIV22 Name Register

31	30	29	28	27	26	25	24
R_IV22							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R_IV22							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_IV22							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_IV22							
R/W							
0h							

Table 14-13211. FSS_FSAS_OTFA_REGS_RIV22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV22	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.117 FSS_FSAS_OTFA_REGS_RIV23 Register

14.7.4.5.2.117.1 FSS_FSAS_OTFA_REGS_RIV23 Register (Offset = 19Ch) [reset = 0h]

RegionIV23

Return to Summary Table

Table 14-13212. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 019Ch

Figure 14-6520. FSS_FSAS_OTFA_REGS_RIV23 Name Register

31	30	29	28	27	26	25	24
R_IV23							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV23							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV23							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV23							
R/W							
0h							

Table 14-13213. FSS_FSAS_OTFA_REGS_RIV23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV23	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.118 FSS_FSAS_OTFA_REGS_RGCFG3 Register

14.7.4.5.2.118.1 FSS_FSAS_OTFA_REGS_RGCFG3 Register (Offset = 1A0h) [reset = 0h]

RegionCfg3

Return to Summary Table

Table 14-13214. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01A0h

Figure 14-6521. FSS_FSAS_OTFA_REGS_RGCFG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>WRT_PROTECT3</td><td colspan="2">MAC_MODE3</td><td colspan="2">AES_MODE3</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-13215. FSS_FSAS_OTFA_REGS_RGCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT3	R/W	0h	WRT protect Reset Source: rst_modg_rst_n
3:2	MAC_MODE3	R/W	0h	MAC mode Reset Source: rst_modg_rst_n
1:0	AES_MODE3	R/W	0h	AES mode Reset Source: rst_modg_rst_n

14.7.4.5.2.119 FSS_FSAS_OTFA_REGS_RGMACST3 Register

14.7.4.5.2.119.1 FSS_FSAS_OTFA_REGS_RGMACST3 Register (Offset = 1A4h) [reset = 0h]

RegionMacStart3

Return to Summary Table

Table 14-13216. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01A4h

Figure 14-6522. FSS_FSAS_OTFA_REGS_RGMACST3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">M_START3</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">M_START3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">M_START3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13217. FSS_FSAS_OTFA_REGS_RGMACST3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START3	R/W	0h	This defines the start of the mac buffer in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.120 FSS_FSAS_OTFA_REGS_RGST3 Register

14.7.4.5.2.120.1 FSS_FSAS_OTFA_REGS_RGST3 Register (Offset = 1A8h) [reset = 0h]

RegionStart3

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Table 14-13218. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01A8h

Figure 14-6523. FSS_FSAS_OTFA_REGS_RGST3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">R_START3</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_START3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_START3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13219. FSS_FSAS_OTFA_REGS_RGST3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START3	R/W	0h	This defines the start of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.121 FSS_FSAS_OTFA_REGS_RGSI3 Register

14.7.4.5.2.121.1 FSS_FSAS_OTFA_REGS_RGSI3 Register (Offset = 1ACh) [reset = 0h]

RegionSize3

Return to Summary Table

Table 14-13220. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01ACh

Figure 14-6524. FSS_FSAS_OTFA_REGS_RGSI3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">R_SIZE3</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_SIZE3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_SIZE3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13221. FSS_FSAS_OTFA_REGS_RGSI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE3	R/W	0h	This defines the size of the crypto region in 4KBytes steps Reset Source: rst_modg_rst_n

14.7.4.5.2.122 FSS_FSAS_OTFA_REGS_RKEYE30 Register

14.7.4.5.2.122.1 FSS_FSAS_OTFA_REGS_RKEYE30 Register (Offset = 1B0h) [reset = 0h]

RegionKeyE30

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Table 14-13222. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01B0h

Figure 14-6525. FSS_FSAS_OTFA_REGS_RKEYE30 Name Register

31	30	29	28	27	26	25	24
R_KEY_E30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E30							
R/W							
0h							

Table 14-13223. FSS_FSAS_OTFA_REGS_RKEYE30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E30	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.123 FSS_FSAS_OTFA_REGS_RKEYE31 Register

14.7.4.5.2.123.1 FSS_FSAS_OTFA_REGS_RKEYE31 Register (Offset = 1B4h) [reset = 0h]

RegionKeyE31

Return to Summary Table

Table 14-13224. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01B4h

Figure 14-6526. FSS_FSAS_OTFA_REGS_RKEYE31 Name Register

31	30	29	28	27	26	25	24
R_KEY_E31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E31							
R/W							
0h							

Table 14-13225. FSS_FSAS_OTFA_REGS_RKEYE31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E31	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.124 FSS_FSAS_OTFA_REGS_RKEYE32 Register

14.7.4.5.2.124.1 FSS_FSAS_OTFA_REGS_RKEYE32 Register (Offset = 1B8h) [reset = 0h]

RegionKeyE32

Return to Summary Table

Table 14-13226. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01B8h

Figure 14-6527. FSS_FSAS_OTFA_REGS_RKEYE32 Name Register

31	30	29	28	27	26	25	24
R_KEY_E32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E32							
R/W							
0h							

Table 14-13227. FSS_FSAS_OTFA_REGS_RKEYE32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E32	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.125 FSS_FSAS_OTFA_REGS_RKEYE33 Register

14.7.4.5.2.125.1 FSS_FSAS_OTFA_REGS_RKEYE33 Register (Offset = 1BCh) [reset = 0h]

RegionKeyE33

Return to Summary Table

Table 14-13228. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01BCh

Figure 14-6528. FSS_FSAS_OTFA_REGS_RKEYE33 Name Register

31	30	29	28	27	26	25	24
R_KEY_E33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E33							
R/W							
0h							

Table 14-13229. FSS_FSAS_OTFA_REGS_RKEYE33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E33	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.126 FSS_FSAS_OTFA_REGS_RKEYE34 Register

14.7.4.5.2.126.1 FSS_FSAS_OTFA_REGS_RKEYE34 Register (Offset = 1C0h) [reset = 0h]

RegionKeyE34

Return to Summary Table

Table 14-13230. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01C0h

Figure 14-6529. FSS_FSAS_OTFA_REGS_RKEYE34 Name Register

31	30	29	28	27	26	25	24
R_KEY_E34							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E34							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E34							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E34							
R/W							
0h							

Table 14-13231. FSS_FSAS_OTFA_REGS_RKEYE34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E34	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.127 FSS_FSAS_OTFA_REGS_RKEYE35 Register

14.7.4.5.2.127.1 FSS_FSAS_OTFA_REGS_RKEYE35 Register (Offset = 1C4h) [reset = 0h]

RegionKeyE35

Return to Summary Table

Table 14-13232. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01C4h

Figure 14-6530. FSS_FSAS_OTFA_REGS_RKEYE35 Name Register

31	30	29	28	27	26	25	24
R_KEY_E35							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E35							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E35							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E35							
R/W							
0h							

Table 14-13233. FSS_FSAS_OTFA_REGS_RKEYE35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E35	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.128 FSS_FSAS_OTFA_REGS_RKEYE36 Register

14.7.4.5.2.128.1 FSS_FSAS_OTFA_REGS_RKEYE36 Register (Offset = 1C8h) [reset = 0h]

RegionKeyE36

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Table 14-13234. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01C8h

Figure 14-6531. FSS_FSAS_OTFA_REGS_RKEYE36 Name Register

31	30	29	28	27	26	25	24
R_KEY_E36							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E36							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E36							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E36							
R/W							
0h							

Table 14-13235. FSS_FSAS_OTFA_REGS_RKEYE36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E36	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.129 FSS_FSAS_OTFA_REGS_RKEYE37 Register

14.7.4.5.2.129.1 FSS_FSAS_OTFA_REGS_RKEYE37 Register (Offset = 1CCh) [reset = 0h]

RegionKeyE37

Return to Summary Table

Table 14-13236. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01CCh

Figure 14-6532. FSS_FSAS_OTFA_REGS_RKEYE37 Name Register

31	30	29	28	27	26	25	24
R_KEY_E37							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E37							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E37							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E37							
R/W							
0h							

Table 14-13237. FSS_FSAS_OTFA_REGS_RKEYE37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E37	R/W	0h	Key E Reset Source: rst_modg_rst_n

14.7.4.5.2.130 FSS_FSAS_OTFA_REGS_RKEYEP30 Register

14.7.4.5.2.130.1 FSS_FSAS_OTFA_REGS_RKEYEP30 Register (Offset = 1D0h) [reset = 0h]

RegionKeyEP30

Return to Summary Table

Table 14-13238. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01D0h

Figure 14-6533. FSS_FSAS_OTFA_REGS_RKEYEP30 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP30							
R/W							
0h							

Table 14-13239. FSS_FSAS_OTFA_REGS_RKEYEP30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP30	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.131 FSS_FSAS_OTFA_REGS_RKEYEP31 Register

14.7.4.5.2.131.1 FSS_FSAS_OTFA_REGS_RKEYEP31 Register (Offset = 1D4h) [reset = 0h]

RegionKeyEP31

Return to Summary Table

Table 14-13240. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01D4h

Figure 14-6534. FSS_FSAS_OTFA_REGS_RKEYEP31 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP31							
R/W							
0h							

Table 14-13241. FSS_FSAS_OTFA_REGS_RKEYEP31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP31	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.132 FSS_FSAS_OTFA_REGS_RKEYEP32 Register

14.7.4.5.2.132.1 FSS_FSAS_OTFA_REGS_RKEYEP32 Register (Offset = 1D8h) [reset = 0h]

RegionKeyEP32

Return to Summary Table

Table 14-13242. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01D8h

Figure 14-6535. FSS_FSAS_OTFA_REGS_RKEYEP32 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP32							
R/W							
0h							

Table 14-13243. FSS_FSAS_OTFA_REGS_RKEYEP32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP32	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.133 FSS_FSAS_OTFA_REGS_RKEYEP33 Register

14.7.4.5.2.133.1 FSS_FSAS_OTFA_REGS_RKEYEP33 Register (Offset = 1DCh) [reset = 0h]

RegionKeyEP33

Return to Summary Table

Table 14-13244. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01DCh

Figure 14-6536. FSS_FSAS_OTFA_REGS_RKEYEP33 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP33							
R/W							
0h							

Table 14-13245. FSS_FSAS_OTFA_REGS_RKEYEP33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP33	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.134 FSS_FSAS_OTFA_REGS_RKEYEP34 Register

14.7.4.5.2.134.1 FSS_FSAS_OTFA_REGS_RKEYEP34 Register (Offset = 1E0h) [reset = 0h]

RegionKeyEP34

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Table 14-13246. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01E0h

Figure 14-6537. FSS_FSAS_OTFA_REGS_RKEYEP34 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP34							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP34							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP34							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP34							
R/W							
0h							

Table 14-13247. FSS_FSAS_OTFA_REGS_RKEYEP34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP34	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.135 FSS_FSAS_OTFA_REGS_RKEYEP35 Register

14.7.4.5.2.135.1 FSS_FSAS_OTFA_REGS_RKEYEP35 Register (Offset = 1E4h) [reset = 0h]

RegionKeyEP35

Return to Summary Table

Table 14-13248. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01E4h

Figure 14-6538. FSS_FSAS_OTFA_REGS_RKEYEP35 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP35							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP35							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP35							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP35							
R/W							
0h							

Table 14-13249. FSS_FSAS_OTFA_REGS_RKEYEP35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP35	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.136 FSS_FSAS_OTFA_REGS_RKEYEP36 Register

14.7.4.5.2.136.1 FSS_FSAS_OTFA_REGS_RKEYEP36 Register (Offset = 1E8h) [reset = 0h]

RegionKeyEP36

Return to Summary Table

Table 14-13250. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01E8h

Figure 14-6539. FSS_FSAS_OTFA_REGS_RKEYEP36 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP36							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP36							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP36							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP36							
R/W							
0h							

Table 14-13251. FSS_FSAS_OTFA_REGS_RKEYEP36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP36	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.137 FSS_FSAS_OTFA_REGS_RKEYEP37 Register

14.7.4.5.2.137.1 FSS_FSAS_OTFA_REGS_RKEYEP37 Register (Offset = 1ECh) [reset = 0h]

RegionKeyEP37

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Table 14-13252. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01ECh

Figure 14-6540. FSS_FSAS_OTFA_REGS_RKEYEP37 Name Register

31	30	29	28	27	26	25	24
R_KEY_EP37							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP37							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP37							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP37							
R/W							
0h							

Table 14-13253. FSS_FSAS_OTFA_REGS_RKEYEP37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP37	R/W	0h	Key EP Reset Source: rst_modg_rst_n

14.7.4.5.2.138 FSS_FSAS_OTFA_REGS_RKEYA30 Register

14.7.4.5.2.138.1 FSS_FSAS_OTFA_REGS_RKEYA30 Register (Offset = 1F0h) [reset = 0h]

RegionKeyA30

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Table 14-13254. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01F0h

Figure 14-6541. FSS_FSAS_OTFA_REGS_RKEYA30 Name Register

31	30	29	28	27	26	25	24
R_KEY_A30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A30							
R/W							
0h							

Table 14-13255. FSS_FSAS_OTFA_REGS_RKEYA30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A30	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.139 FSS_FSAS_OTFA_REGS_RKEYA31 Register

14.7.4.5.2.139.1 FSS_FSAS_OTFA_REGS_RKEYA31 Register (Offset = 1F4h) [reset = 0h]

RegionKeyA31

Return to Summary Table

Table 14-13256. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01F4h

Figure 14-6542. FSS_FSAS_OTFA_REGS_RKEYA31 Name Register

31	30	29	28	27	26	25	24
R_KEY_A31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A31							
R/W							
0h							

Table 14-13257. FSS_FSAS_OTFA_REGS_RKEYA31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A31	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.140 FSS_FSAS_OTFA_REGS_RKEYA32 Register

14.7.4.5.2.140.1 FSS_FSAS_OTFA_REGS_RKEYA32 Register (Offset = 1F8h) [reset = 0h]

RegionKeyA32

Return to Summary Table

Table 14-13258. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01F8h

Figure 14-6543. FSS_FSAS_OTFA_REGS_RKEYA32 Name Register

31	30	29	28	27	26	25	24
R_KEY_A32							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A32							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A32							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A32							
R/W							
0h							

Table 14-13259. FSS_FSAS_OTFA_REGS_RKEYA32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A32	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.141 FSS_FSAS_OTFA_REGS_RKEYA33 Register

14.7.4.5.2.141.1 FSS_FSAS_OTFA_REGS_RKEYA33 Register (Offset = 1FCh) [reset = 0h]

RegionKeyA33

Return to Summary Table

Table 14-13260. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 01FCh

Figure 14-6544. FSS_FSAS_OTFA_REGS_RKEYA33 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_A33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_A33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_A33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_A33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13261. FSS_FSAS_OTFA_REGS_RKEYA33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A33	R/W	0h	Key A Reset Source: rst_modg_rst_n

14.7.4.5.2.142 FSS_FSAS_OTFA_REGS_RKEYAP30 Register

14.7.4.5.2.142.1 FSS_FSAS_OTFA_REGS_RKEYAP30 Register (Offset = 200h) [reset = 0h]

RegionKeyAP30

Return to Summary Table

Table 14-13262. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0200h

Figure 14-6545. FSS_FSAS_OTFA_REGS_RKEYAP30 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP30							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP30							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP30							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP30							
R/W							
0h							

Table 14-13263. FSS_FSAS_OTFA_REGS_RKEYAP30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP30	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.143 FSS_FSAS_OTFA_REGS_RKEYAP31 Register

14.7.4.5.2.143.1 FSS_FSAS_OTFA_REGS_RKEYAP31 Register (Offset = 204h) [reset = 0h]

RegionKeyAP31

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Table 14-13264. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0204h

Figure 14-6546. FSS_FSAS_OTFA_REGS_RKEYAP31 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP31							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP31							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP31							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP31							
R/W							
0h							

Table 14-13265. FSS_FSAS_OTFA_REGS_RKEYAP31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP31	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.144 FSS_FSAS_OTFA_REGS_RKEYAP32 Register

14.7.4.5.2.144.1 FSS_FSAS_OTFA_REGS_RKEYAP32 Register (Offset = 208h) [reset = 0h]

RegionKeyAP32

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Table 14-13266. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0208h

Figure 14-6547. FSS_FSAS_OTFA_REGS_RKEYAP32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_KEY_AP32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_KEY_AP32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_KEY_AP32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_KEY_AP32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13267. FSS_FSAS_OTFA_REGS_RKEYAP32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP32	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.145 FSS_FSAS_OTFA_REGS_RKEYAP33 Register

14.7.4.5.2.145.1 FSS_FSAS_OTFA_REGS_RKEYAP33 Register (Offset = 20Ch) [reset = 0h]

RegionKeyAP33

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Table 14-13268. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 020Ch

Figure 14-6548. FSS_FSAS_OTFA_REGS_RKEYAP33 Name Register

31	30	29	28	27	26	25	24
R_KEY_AP33							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP33							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP33							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP33							
R/W							
0h							

Table 14-13269. FSS_FSAS_OTFA_REGS_RKEYAP33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP33	R/W	0h	Key AP Reset Source: rst_modg_rst_n

14.7.4.5.2.146 FSS_FSAS_OTFA_REGS_RIV30 Register

14.7.4.5.2.146.1 FSS_FSAS_OTFA_REGS_RIV30 Register (Offset = 210h) [reset = 0h]

RegionIV30

Return to Summary Table

Table 14-13270. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0210h

Figure 14-6549. FSS_FSAS_OTFA_REGS_RIV30 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_IV30</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_IV30</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_IV30</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_IV30</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13271. FSS_FSAS_OTFA_REGS_RIV30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV30	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.147 FSS_FSAS_OTFA_REGS_RIV31 Register

14.7.4.5.2.147.1 FSS_FSAS_OTFA_REGS_RIV31 Register (Offset = 214h) [reset = 0h]

RegionIV31

Return to Summary Table

Table 14-13272. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0214h

Figure 14-6550. FSS_FSAS_OTFA_REGS_RIV31 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_IV31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_IV31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_IV31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_IV31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13273. FSS_FSAS_OTFA_REGS_RIV31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV31	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.148 FSS_FSAS_OTFA_REGS_RIV32 Register

14.7.4.5.2.148.1 FSS_FSAS_OTFA_REGS_RIV32 Register (Offset = 218h) [reset = 0h]

RegionIV32

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Table 14-13274. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0218h

Figure 14-6551. FSS_FSAS_OTFA_REGS_RIV32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_IV32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_IV32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_IV32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_IV32</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13275. FSS_FSAS_OTFA_REGS_RIV32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV32	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.149 FSS_FSAS_OTFA_REGS_RIV33 Register

14.7.4.5.2.149.1 FSS_FSAS_OTFA_REGS_RIV33 Register (Offset = 21Ch) [reset = 0h]

RegionIV33

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Table 14-13276. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 021Ch

Figure 14-6552. FSS_FSAS_OTFA_REGS_RIV33 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">R_IV33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">R_IV33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">R_IV33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">R_IV33</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13277. FSS_FSAS_OTFA_REGS_RIV33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV33	R/W	0h	IV Reset Source: rst_modg_rst_n

14.7.4.5.2.150 FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register

14.7.4.5.2.150.1 FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register (Offset = 220h) [reset = 0h]

IRQAdditionalInfo0

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Table 14-13278. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0220h

Figure 14-6553. FSS_FSAS_OTFA_REGS_IRQADDINFO0 Name Register

31	30	29	28	27	26	25	24
IRQ_MADDR							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_MADDR							
R							
0h							
15	14	13	12	11	10	9	8
IRQ_MADDR							
R							
0h							
7	6	5	4	3	2	1	0
IRQ_MADDR							
R							
0h							

Table 14-13279. FSS_FSAS_OTFA_REGS_IRQADDINFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IRQ_MADDR	R	0h	Initiator Address which caused the event Reset Source: rst_modg_rst_n

14.7.4.5.2.151 FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register

14.7.4.5.2.151.1 FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register (Offset = 224h) [reset = 0h]

IRQAdditionalInfo1

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Table 14-13280. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0224h

Figure 14-6554. FSS_FSAS_OTFA_REGS_IRQADDINFO1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">IRQ_MLEN</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">IRQ_MLEN</td><td colspan="3">IRQ_MSEQ</td><td colspan="3">IRQ_MCMD</td></tr>
<tr><td colspan="2">R</td><td colspan="3">R</td><td colspan="3">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">IRQ_MID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13281. FSS_FSAS_OTFA_REGS_IRQADDINFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:14	IRQ_MLEN	R	0h	Initiator LENGTH which caused the event Reset Source: rst_modg_rst_n
13:11	IRQ_MSEQ	R	0h	Initiator SEQ which caused the event Reset Source: rst_modg_rst_n
10:8	IRQ_MCMD	R	0h	Initiator CMD which caused the event Reset Source: rst_modg_rst_n
7:0	IRQ_MID	R	0h	Initiator TAG ID which caused the event Reset Source: rst_modg_rst_n

14.7.4.5.2.152 FSS_FSAS_OTFA_REGS_MACCACHEINFO Register

14.7.4.5.2.152.1 FSS_FSAS_OTFA_REGS_MACCACHEINFO Register (Offset = 228h) [reset = 0h]

MACCacheInfo

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Table 14-13282. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 0228h

Figure 14-6555. FSS_FSAS_OTFA_REGS_MACCACHEINFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CACHE_MISS_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
CACHE_MISS_EVENT_CNT							
R							
0h							

Table 14-13283. FSS_FSAS_OTFA_REGS_MACCACHEINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CACHE_MISS_EVENT_CNT	R	0h	MAC Cache Miss event cnt Reset Source: rst_modg_rst_n

14.7.4.5.2.153 FSS_FSAS_OTFA_REGS_RMWRMCNT Register

14.7.4.5.2.153.1 FSS_FSAS_OTFA_REGS_RMWRMCNT Register (Offset = 22Ch) [reset = 0h]

RMWRMCnt

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Table 14-13284. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0FCA 022Ch

Figure 14-6556. FSS_FSAS_OTFA_REGS_RMWRMCNT Name Register

31	30	29	28	27	26	25	24
RM_EVENT_CNT							
R							
0h							
23	22	21	20	19	18	17	16
RM_EVENT_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RMW_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
RMW_EVENT_CNT							
R							
0h							

Table 14-13285. FSS_FSAS_OTFA_REGS_RMWRMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RM_EVENT_CNT	R	0h	RM event cnt Reset Source: rst_modg_rst_n
15:0	RMW_EVENT_CNT	R	0h	RMW event cnt Reset Source: rst_modg_rst_n

14.7.4.5.2.154 FSS_DAT_REG1_HPB_DATA_MEM_J Register

14.7.4.5.2.154.1 FSS_DAT_REG1_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS boot data region1

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Table 14-13286. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	6800 0000h + formula

Figure 14-6557. FSS_DAT_REG1_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HPB_DATA							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HPB_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HPB_DATA							
R/W							
0h							

Table 14-13287. FSS_DAT_REG1_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1 Reset Source: rst_mod_g_rst_n

14.7.4.5.2.155 FSS_DAT_REG0_HPB_DATA_MEM_J Register

14.7.4.5.2.155.1 FSS_DAT_REG0_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS data region0

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Table 14-13288. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0002 0000 0000h + formula

Figure 14-6558. FSS_DAT_REG0_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-13289. FSS_DAT_REG0_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region0 Reset Source: rst_mod_g_rst_n

14.7.4.5.2.156 FSS_DAT_REG3_HPB_DATA_MEM_J Register

14.7.4.5.2.156.1 FSS_DAT_REG3_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS bypass data region3

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Table 14-13290. Instance Table

Instance Name	Physical Address
FSS1_FSAS_0	0003 0000 0000h + formula

Figure 14-6559. FSS_DAT_REG3_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 14-13291. FSS_DAT_REG3_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1 Reset Source: rst_mod_g_rst_n

14.7.4.6 MMCSD

MMCSD

14.7.4.6.1 MMCSD Summaries

MMCSD Summaries

Table 14-13292. MMCSD_ECC_AGGR_RXMEM Registers, Base Address=0070 8000h, Length=1024

Offset	Length	Register Name	MMCSD0 Physical Address
0h	32	MMCSD_ECC_AGGR_RXMEM_REV	0070 8000h
8h	32	MMCSD_ECC_AGGR_RXMEM_VECTOR	0070 8008h
Ch	32	MMCSD_ECC_AGGR_RXMEM_STAT	0070 800Ch
10h	32	MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS	0070 8010h
3Ch	32	MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG	0070 803Ch
40h	32	MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0	0070 8040h
80h	32	MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0	0070 8080h
C0h	32	MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0	0070 80C0h
13Ch	32	MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG	0070 813Ch
140h	32	MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0	0070 8140h
180h	32	MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0	0070 8180h
1C0h	32	MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0	0070 81C0h
200h	32	MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET	0070 8200h
204h	32	MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR	0070 8204h
208h	32	MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET	0070 8208h
20Ch	32	MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR	0070 820Ch

Table 14-13293. MMCSD_ECC_AGGR_TXMEM Registers, Base Address=0070 9000h, Length=1024

Offset	Length	Register Name	MMCSD0 Physical Address
0h	32	MMCSD_ECC_AGGR_TXMEM_REV	0070 9000h
8h	32	MMCSD_ECC_AGGR_TXMEM_VECTOR	0070 9008h
Ch	32	MMCSD_ECC_AGGR_TXMEM_STAT	0070 900Ch
10h	32	MMCSD_ECC_AGGR_TXMEM_RESERVED_SVBUS	0070 9010h
3Ch	32	MMCSD_ECC_AGGR_TXMEM_SEC_EOI_REG	0070 903Ch
40h	32	MMCSD_ECC_AGGR_TXMEM_SEC_STATUS_REG0	0070 9040h
80h	32	MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_SET_REG0	0070 9080h
C0h	32	MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_CLR_REG0	0070 90C0h
13Ch	32	MMCSD_ECC_AGGR_TXMEM_DED_EOI_REG	0070 913Ch
140h	32	MMCSD_ECC_AGGR_TXMEM_DED_STATUS_REG0	0070 9140h
180h	32	MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_SET_REG0	0070 9180h
1C0h	32	MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_CLR_REG0	0070 91C0h
200h	32	MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_SET	0070 9200h
204h	32	MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_CLR	0070 9204h
208h	32	MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_SET	0070 9208h

Table 14-13293. MMCSD_ECC_AGGR_TXMEM Registers, Base Address=0070 9000h, Length=1024 (continued)

Offset	Length	Register Name	MMCSD0 Physical Address
20Ch	32	MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_CLR	0070 920Ch

Table 14-13294. MMCSD_CTL_CFG Registers, Base Address=0FA0 0000h, Length=4096

Offset	Length	Register Name	MMCSD0 Physical Address
0h	16	MMCSD_CTL_CFG_SDMA_SYS_ADDR_LO	0FA0 0000h
2h	16	MMCSD_CTL_CFG_SDMA_SYS_ADDR_HI	0FA0 0002h
4h	16	MMCSD_CTL_CFG_BLOCK_SIZE	0FA0 0004h
6h	16	MMCSD_CTL_CFG_BLOCK_COUNT	0FA0 0006h
8h	16	MMCSD_CTL_CFG_ARGUMENT1_LO	0FA0 0008h
Ah	16	MMCSD_CTL_CFG_ARGUMENT1_HI	0FA0 000Ah
Ch	16	MMCSD_CTL_CFG_TRANSFER_MODE	0FA0 000Ch
Eh	16	MMCSD_CTL_CFG_COMMAND	0FA0 000Eh
10h	16	MMCSD_CTL_CFG_RESPONSE	0FA0 0010h
20h	32	MMCSD_CTL_CFG_DATA_PORT	0FA0 0020h
24h	32	MMCSD_CTL_CFG_PRESENTSTATE	0FA0 0024h
28h	8	MMCSD_CTL_CFG_HOST_CONTROL1	0FA0 0028h
29h	8	MMCSD_CTL_CFG_POWER_CONTROL	0FA0 0029h
2Ah	8	MMCSD_CTL_CFG_BLOCK_GAP_CONTROL	0FA0 002Ah
2Bh	8	MMCSD_CTL_CFG_WAKEUP_CONTROL	0FA0 002Bh
2Ch	16	MMCSD_CTL_CFG_CLOCK_CONTROL	0FA0 002Ch
2Eh	8	MMCSD_CTL_CFG_TIMEOUT_CONTROL	0FA0 002Eh
2Fh	8	MMCSD_CTL_CFG_SOFTWARE_RESET	0FA0 002Fh
30h	16	MMCSD_CTL_CFG_NORMAL_INTR_STS	0FA0 0030h
32h	16	MMCSD_CTL_CFG_ERROR_INTR_STS	0FA0 0032h
34h	16	MMCSD_CTL_CFG_NORMAL_INTR_STS_ENA	0FA0 0034h
36h	16	MMCSD_CTL_CFG_ERROR_INTR_STS_ENA	0FA0 0036h
38h	16	MMCSD_CTL_CFG_NORMAL_INTR_SIG_ENA	0FA0 0038h
3Ah	16	MMCSD_CTL_CFG_ERROR_INTR_SIG_ENA	0FA0 003Ah
3Ch	16	MMCSD_CTL_CFG_AUTOCMD_ERR_STS	0FA0 003Ch
3Eh	16	MMCSD_CTL_CFG_HOST_CONTROL2	0FA0 003Eh
40h	64	MMCSD_CTL_CFG_CAPABILITIES	0FA0 0040h
48h	64	MMCSD_CTL_CFG_MAX_CURRENT_CAP	0FA0 0048h
50h	16	MMCSD_CTL_CFG_FORCE_EVNT_ACMD_ERR_STS	0FA0 0050h
52h	16	MMCSD_CTL_CFG_FORCE_EVNT_ERR_INT_STS	0FA0 0052h
54h	8	MMCSD_CTL_CFG_ADMA_ERR_STATUS	0FA0 0054h
58h	64	MMCSD_CTL_CFG_ADMA_SYS_ADDRESS	0FA0 0058h
60h	16	MMCSD_CTL_CFG_PRESET_VALUE0	0FA0 0060h
62h	16	MMCSD_CTL_CFG_PRESET_VALUE1	0FA0 0062h
64h	16	MMCSD_CTL_CFG_PRESET_VALUE2	0FA0 0064h
66h	16	MMCSD_CTL_CFG_PRESET_VALUE3	0FA0 0066h
68h	16	MMCSD_CTL_CFG_PRESET_VALUE4	0FA0 0068h
6Ah	16	MMCSD_CTL_CFG_PRESET_VALUE5	0FA0 006Ah
6Ch	16	MMCSD_CTL_CFG_PRESET_VALUE6	0FA0 006Ch
6Eh	16	MMCSD_CTL_CFG_PRESET_VALUE7	0FA0 006Eh
72h	16	MMCSD_CTL_CFG_PRESET_VALUE8	0FA0 0072h

Table 14-13294. MMCSD_CTL_CFG Registers, Base Address=0FA0 0000h, Length=4096 (continued)

Offset	Length	Register Name	MMCSD0 Physical Address
74h	16	MMCSD_CTL_CFG_PRESET_VALUE10	0FA0 0074h
78h	64	MMCSD_CTL_CFG_ADMA3_DESC_ADDRESS	0FA0 0078h
80h	16	MMCSD_CTL_CFG_UHS2_BLOCK_SIZE	0FA0 0080h
84h	32	MMCSD_CTL_CFG_UHS2_BLOCK_COUNT	0FA0 0084h
88h	8	MMCSD_CTL_CFG_UHS2_COMMAND_PKT	0FA0 0088h
9Ch	16	MMCSD_CTL_CFG_UHS2_XFER_MODE	0FA0 009Ch
9Eh	16	MMCSD_CTL_CFG_UHS2_COMMAND	0FA0 009Eh
A0h	8	MMCSD_CTL_CFG_UHS2_RESPONSE	0FA0 00A0h
B4h	8	MMCSD_CTL_CFG_UHS2_MESSAGE_SELECT	0FA0 00B4h
B8h	32	MMCSD_CTL_CFG_UHS2_MESSAGE	0FA0 00B8h
BCh	16	MMCSD_CTL_CFG_UHS2_DEVICE_INTR_STATUS	0FA0 00BCh
BEh	8	MMCSD_CTL_CFG_UHS2_DEVICE_SELECT	0FA0 00BEh
BFh	8	MMCSD_CTL_CFG_UHS2_DEVICE_INT_CODE	0FA0 00BFh
C0h	16	MMCSD_CTL_CFG_UHS2_SOFTWARE_RESET	0FA0 00C0h
C2h	16	MMCSD_CTL_CFG_UHS2_TIMER_CONTROL	0FA0 00C2h
C4h	32	MMCSD_CTL_CFG_UHS2_ERR_INTR_STS	0FA0 00C4h
C8h	32	MMCSD_CTL_CFG_UHS2_ERR_INTR_STS_ENA	0FA0 00C8h
CCh	32	MMCSD_CTL_CFG_UHS2_ERR_INTR_SIG_ENA	0FA0 00CCh
E0h	16	MMCSD_CTL_CFG_UHS2_SETTINGS_PTR	0FA0 00E0h
E2h	16	MMCSD_CTL_CFG_UHS2_CAPABILITIES_PTR	0FA0 00E2h
E4h	16	MMCSD_CTL_CFG_UHS2_TEST_PTR	0FA0 00E4h
E6h	16	MMCSD_CTL_CFG_SHARED_BUS_CTRL_PTR	0FA0 00E6h
E8h	16	MMCSD_CTL_CFG_VENDOR_SPECFIC_PTR	0FA0 00E8h
F4h	32	MMCSD_CTL_CFG_BOOT_TIMEOUT_CONTROL	0FA0 00F4h
F8h	32	MMCSD_CTL_CFG_VENDOR_REGISTER	0FA0 00F8h
FCh	16	MMCSD_CTL_CFG_SLOT_INT_STS	0FA0 00FCh
FEh	16	MMCSD_CTL_CFG_HOST_CONTROLLER_VER	0FA0 00FEh
100h	32	MMCSD_CTL_CFG_UHS2_GEN_SETTINGS	0FA0 0100h
104h	32	MMCSD_CTL_CFG_UHS2_PHY_SETTINGS	0FA0 0104h
108h	64	MMCSD_CTL_CFG_UHS2_LNK_TRN_SETTINGS	0FA0 0108h
110h	32	MMCSD_CTL_CFG_UHS2_GEN_CAP	0FA0 0110h
114h	32	MMCSD_CTL_CFG_UHS2_PHY_CAP	0FA0 0114h
118h	64	MMCSD_CTL_CFG_UHS2_LNK_TRN_CAP	0FA0 0118h
120h	32	MMCSD_CTL_CFG_FORCE_UHSII_ERR_INT_STS	0FA0 0120h
200h	32	MMCSD_CTL_CFG_CQ_VERSION	0FA0 0200h
204h	32	MMCSD_CTL_CFG_CQ_CAPABILITIES	0FA0 0204h
208h	32	MMCSD_CTL_CFG_CQ_CONFIG	0FA0 0208h
20Ch	32	MMCSD_CTL_CFG_CQ_CONTROL	0FA0 020Ch
210h	32	MMCSD_CTL_CFG_CQ_INTR_STS	0FA0 0210h
214h	32	MMCSD_CTL_CFG_CQ_INTR_STS_ENA	0FA0 0214h
218h	32	MMCSD_CTL_CFG_CQ_INTR_SIG_ENA	0FA0 0218h
21Ch	32	MMCSD_CTL_CFG_CQ_INTR_COALESCING	0FA0 021Ch
220h	32	MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR	0FA0 0220h
224h	32	MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR_UPBITS	0FA0 0224h
228h	32	MMCSD_CTL_CFG_CQ_TASK_DOOR_BELL	0FA0 0228h
22Ch	32	MMCSD_CTL_CFG_CQ_TASK_COMP_NOTIF	0FA0 022Ch
230h	32	MMCSD_CTL_CFG_CQ_DEV_QUEUE_STATUS	0FA0 0230h

Table 14-13294. MMCSD_CTL_CFG Registers, Base Address=0FA0 0000h, Length=4096 (continued)

Offset	Length	Register Name	MMCSD0 Physical Address
234h	32	MMCSD_CTL_CFG_CQ_DEV_PENDING_TASKS	0FA0 0234h
238h	32	MMCSD_CTL_CFG_CQ_TASK_CLEAR	0FA0 0238h
240h	32	MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG1	0FA0 0240h
244h	32	MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG2	0FA0 0244h
248h	32	MMCSD_CTL_CFG_CQ_DCMD_RESPONSE	0FA0 0248h
250h	32	MMCSD_CTL_CFG_CQ_RESP_ERR_MASK	0FA0 0250h
254h	32	MMCSD_CTL_CFG_CQ_TASK_ERR_INFO	0FA0 0254h
258h	32	MMCSD_CTL_CFG_CQ_CMD_RESP_INDEX	0FA0 0258h
25Ch	32	MMCSD_CTL_CFG_CQ_CMD_RESP_ARG	0FA0 025Ch
260h	32	MMCSD_CTL_CFG_CQ_ERROR_TASK_ID	0FA0 0260h

Table 14-13295. MMCSD_SS_CFG Registers, Base Address=0FA0 8000h, Length=1024

Offset	Length	Register Name	MMCSD0 Physical Address
0h	32	MMCSD_SS_CFG_SS_ID_REV_REG	0FA0 8000h
10h	32	MMCSD_SS_CFG_CTL_CFG_1_REG	0FA0 8010h
14h	32	MMCSD_SS_CFG_CTL_CFG_2_REG	0FA0 8014h
18h	32	MMCSD_SS_CFG_CTL_CFG_3_REG	0FA0 8018h
1Ch	32	MMCSD_SS_CFG_CTL_CFG_4_REG	0FA0 801Ch
20h	32	MMCSD_SS_CFG_CTL_CFG_5_REG	0FA0 8020h
24h	32	MMCSD_SS_CFG_CTL_CFG_6_REG	0FA0 8024h
28h	32	MMCSD_SS_CFG_CTL_CFG_7_REG	0FA0 8028h
2Ch	32	MMCSD_SS_CFG_CTL_CFG_8_REG	0FA0 802Ch
30h	32	MMCSD_SS_CFG_CTL_CFG_9_REG	0FA0 8030h
34h	32	MMCSD_SS_CFG_CTL_CFG_10_REG	0FA0 8034h
38h	32	MMCSD_SS_CFG_CTL_CFG_11_REG	0FA0 8038h
3Ch	32	MMCSD_SS_CFG_CTL_CFG_12_REG	0FA0 803Ch
40h	32	MMCSD_SS_CFG_CTL_CFG_13_REG	0FA0 8040h
44h	32	MMCSD_SS_CFG_CTL_CFG_14_REG	0FA0 8044h
60h	32	MMCSD_SS_CFG_CTL_STAT_1_REG	0FA0 8060h
64h	32	MMCSD_SS_CFG_CTL_STAT_2_REG	0FA0 8064h
68h	32	MMCSD_SS_CFG_CTL_STAT_3_REG	0FA0 8068h
6Ch	32	MMCSD_SS_CFG_CTL_STAT_4_REG	0FA0 806Ch
70h	32	MMCSD_SS_CFG_CTL_STAT_5_REG	0FA0 8070h
74h	32	MMCSD_SS_CFG_CTL_STAT_6_REG	0FA0 8074h
100h	32	MMCSD_SS_CFG_PHY_CTRL_1_REG	0FA0 8100h
104h	32	MMCSD_SS_CFG_PHY_CTRL_2_REG	0FA0 8104h
108h	32	MMCSD_SS_CFG_PHY_CTRL_3_REG	0FA0 8108h
10Ch	32	MMCSD_SS_CFG_PHY_CTRL_4_REG	0FA0 810Ch
110h	32	MMCSD_SS_CFG_PHY_CTRL_5_REG	0FA0 8110h
114h	32	MMCSD_SS_CFG_PHY_CTRL_6_REG	0FA0 8114h
130h	32	MMCSD_SS_CFG_PHY_STAT_1_REG	0FA0 8130h
134h	32	MMCSD_SS_CFG_PHY_STAT_2_REG	0FA0 8134h

14.7.4.6.2 MMCSD Registers

MMCSD Registers

14.7.4.6.2.1 MMCSD_ECC_AGGR_RXMEM_REV Register

14.7.4.6.2.1.1 MMCSD_ECC_AGGR_RXMEM_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-13296. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8000h

Figure 14-6560. MMCSD_ECC_AGGR_RXMEM_REV Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6a0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6a0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-13297. MMCSD_ECC_AGGR_RXMEM_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6a0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.4.6.2.2 MMCSD_ECC_AGGR_RXMEM_VECTOR Register

14.7.4.6.2.2.1 MMCSD_ECC_AGGR_RXMEM_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-13298. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8008h

Figure 14-6561. MMCSD_ECC_AGGR_RXMEM_VECTOR Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13299. MMCSD_ECC_AGGR_RXMEM_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.4.6.2.3 MMCSD_ECC_AGGR_RXMEM_STAT Register

14.7.4.6.2.3.1 MMCSD_ECC_AGGR_RXMEM_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-13300. Instance Table

Instance Name	Physical Address
MMCSD0	0070 800Ch

Figure 14-6562. MMCSD_ECC_AGGR_RXMEM_STAT Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
8	7	6	5	4	3	2	1
NUM_RAMS							
R							
1h							

Table 14-13301. MMCSD_ECC_AGGR_RXMEM_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.4.6.2.4 MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS Register

14.7.4.6.2.4.1 MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-13302. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8010h

Figure 14-6563. MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS Name Register

32	31	30	29	28	27	26	25
DATA							
R/W							
0h							
24	23	22	21	20	19	18	17
DATA							
R/W							
0h							
16	15	14	13	12	11	10	9
DATA							
R/W							
0h							
8	7	6	5	4	3	2	1
DATA							
R/W							
0h							

Table 14-13303. MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.4.6.2.5 MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG Register

14.7.4.6.2.5.1 MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-13304. Instance Table

Instance Name	Physical Address
MMCSD0	0070 803Ch

Figure 14-6564. MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-13305. MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.6.2.6 MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0 Register

14.7.4.6.2.6.1 MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-13306. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8040h

Figure 14-6565. MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-13307. MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for rxmem_pend

14.7.4.6.2.7 MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0 Register

14.7.4.6.2.7.1 MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-13308. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8080h

Figure 14-6566. MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-13309. MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rxmem_pend

14.7.4.6.2.8 MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0 Register

14.7.4.6.2.8.1 MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-13310. Instance Table

Instance Name	Physical Address
MMCSD0	0070 80C0h

Figure 14-6567. MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-13311. MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rxmem_pend

14.7.4.6.2.9 MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG Register

14.7.4.6.2.9.1 MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-13312. Instance Table

Instance Name	Physical Address
MMCSD0	0070 813Ch

Figure 14-6568. MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-13313. MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.6.2.10 MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0 Register

14.7.4.6.2.10.1 MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-13314. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8140h

Figure 14-6569. MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-13315. MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for rxmem_pend

14.7.4.6.2.11 MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0 Register

14.7.4.6.2.11.1 MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-13316. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8180h

Figure 14-6570. MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-13317. MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rxmem_pend

14.7.4.6.2.12 MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0 Register

14.7.4.6.2.12.1 MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-13318. Instance Table

Instance Name	Physical Address
MMCSD0	0070 81C0h

Figure 14-6571. MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-13319. MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rxmem_pend

14.7.4.6.2.13 MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET Register

14.7.4.6.2.13.1 MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-13320. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8200h

Figure 14-6572. MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13321. MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.4.6.2.14 MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR Register

14.7.4.6.2.14.1 MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-13322. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8204h

Figure 14-6573. MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-13323. MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.4.6.2.15 MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET Register

14.7.4.6.2.15.1 MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-13324. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8208h

Figure 14-6574. MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-13325. MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.4.6.2.16 MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR Register

14.7.4.6.2.16.1 MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-13326. Instance Table

Instance Name	Physical Address
MMCSD0	0070 820Ch

Figure 14-6575. MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-13327. MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.4.6.2.17 MMCSD_ECC_AGGR_TXMEM_REV Register

14.7.4.6.2.17.1 MMCSD_ECC_AGGR_TXMEM_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-13328. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9000h

Figure 14-6576. MMCSD_ECC_AGGR_TXMEM_REV Name Register

32	31	30	29	28	27	26	25
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6a0h			
24	23	22	21	20	19	18	17
MODULE_ID							
R							
6a0h							
16	15	14	13	12	11	10	9
REVRTL					REVMAJ		
R					R		
7h					2h		
8	7	6	5	4	3	2	1
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-13329. MMCSD_ECC_AGGR_TXMEM_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6a0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.4.6.2.18 MMCSD_ECC_AGGR_TXMEM_VECTOR Register

14.7.4.6.2.18.1 MMCSD_ECC_AGGR_TXMEM_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-13330. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9008h

Figure 14-6577. MMCSD_ECC_AGGR_TXMEM_VECTOR Name Register

32	31	30	29	28	27	26	25
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
24	23	22	21	20	19	18	17
RD_SVBUS_ADDRESS							
R/W							
0h							
16	15	14	13	12	11	10	9
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
8	7	6	5	4	3	2	1
ECC_VECTOR							
R/W							
0h							

Table 14-13331. MMCSD_ECC_AGGR_TXMEM_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.4.6.2.19 MMCSD_ECC_AGGR_TXMEM_STAT Register

14.7.4.6.2.19.1 MMCSD_ECC_AGGR_TXMEM_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-13332. Instance Table

Instance Name	Physical Address
MMCSD0	0070 900Ch

Figure 14-6578. MMCSD_ECC_AGGR_TXMEM_STAT Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
8	7	6	5	4	3	2	1
NUM_RAMS							
R							
1h							

Table 14-13333. MMCSD_ECC_AGGR_TXMEM_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.4.6.2.20 MMCSD_ECC_AGGR_TXMEM_RESERVED_SVBUS Register

14.7.4.6.2.20.1 MMCSD_ECC_AGGR_TXMEM_RESERVED_SVBUS Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-13334. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9010h

Figure 14-6579. MMCSD_ECC_AGGR_TXMEM_RESERVED_SVBUS Name Register

32	31	30	29	28	27	26	25
DATA							
R/W							
0h							
24	23	22	21	20	19	18	17
DATA							
R/W							
0h							
16	15	14	13	12	11	10	9
DATA							
R/W							
0h							
8	7	6	5	4	3	2	1
DATA							
R/W							
0h							

Table 14-13335. MMCSD_ECC_AGGR_TXMEM_RESERVED_SVBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.4.6.2.21 MMCSD_ECC_AGGR_TXMEM_SEC_EOI_REG Register

14.7.4.6.2.21.1 MMCSD_ECC_AGGR_TXMEM_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-13336. Instance Table

Instance Name	Physical Address
MMCSD0	0070 903Ch

Figure 14-6580. MMCSD_ECC_AGGR_TXMEM_SEC_EOI_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-13337. MMCSD_ECC_AGGR_TXMEM_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.6.2.22 MMCSD_ECC_AGGR_TXMEM_SEC_STATUS_REG0 Register

14.7.4.6.2.22.1 MMCSD_ECC_AGGR_TXMEM_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-13338. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9040h

Figure 14-6581. MMCSD_ECC_AGGR_TXMEM_SEC_STATUS_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-13339. MMCSD_ECC_AGGR_TXMEM_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.7.4.6.2.23 MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_SET_REG0 Register

14.7.4.6.2.23.1 MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-13340. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9080h

Figure 14-6582. MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_SET_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-13341. MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.7.4.6.2.24 MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_CLR_REG0 Register

14.7.4.6.2.24.1 MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-13342. Instance Table

Instance Name	Physical Address
MMCSD0	0070 90C0h

Figure 14-6583. MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_CLR_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-13343. MMCSD_ECC_AGGR_TXMEM_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.7.4.6.2.25 MMCSD_ECC_AGGR_TXMEM_DED_EOI_REG Register

14.7.4.6.2.25.1 MMCSD_ECC_AGGR_TXMEM_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-13344. Instance Table

Instance Name	Physical Address
MMCSD0	0070 913Ch

Figure 14-6584. MMCSD_ECC_AGGR_TXMEM_DED_EOI_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-13345. MMCSD_ECC_AGGR_TXMEM_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.4.6.2.26 MMCSD_ECC_AGGR_TXMEM_DED_STATUS_REG0 Register

14.7.4.6.2.26.1 MMCSD_ECC_AGGR_TXMEM_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-13346. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9140h

Figure 14-6585. MMCSD_ECC_AGGR_TXMEM_DED_STATUS_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							TXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-13347. MMCSD_ECC_AGGR_TXMEM_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for txmem_pend

14.7.4.6.2.27 MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_SET_REG0 Register

14.7.4.6.2.27.1 MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-13348. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9180h

Figure 14-6586. MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_SET_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							TXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-13349. MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for txmem_pend

14.7.4.6.2.28 MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_CLR_REG0 Register

14.7.4.6.2.28.1 MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-13350. Instance Table

Instance Name	Physical Address
MMCSD0	0070 91C0h

Figure 14-6587. MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_CLR_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							TXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-13351. MMCSD_ECC_AGGR_TXMEM_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for txmem_pend

14.7.4.6.2.29 MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_SET Register

14.7.4.6.2.29.1 MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-13352. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9200h

Figure 14-6588. MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_SET Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13353. MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.4.6.2.30 MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_CLR Register

14.7.4.6.2.30.1 MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-13354. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9204h

Figure 14-6589. MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13355. MMCSD_ECC_AGGR_TXMEM_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.4.6.2.31 MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_SET Register

14.7.4.6.2.31.1 MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-13356. Instance Table

Instance Name	Physical Address
MMCSD0	0070 9208h

Figure 14-6590. MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_SET Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-13357. MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.4.6.2.32 MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_CLR Register

14.7.4.6.2.32.1 MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-13358. Instance Table

Instance Name	Physical Address
MMCSD0	0070 920Ch

Figure 14-6591. MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_CLR Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WD</td><td colspan="2">R/WD</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-13359. MMCSD_ECC_AGGR_TXMEM_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.4.6.2.33 MMCSD_CTL_CFG_SDMA_SYS_ADDR_LO Register

14.7.4.6.2.33.1 MMCSD_CTL_CFG_SDMA_SYS_ADDR_LO Register (Offset = 0h) [reset = 0h]

This register contains the Lower 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

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Table 14-13360. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0000h

Figure 14-6592. MMCSD_CTL_CFG_SDMA_SYS_ADDR_LO Name Register

16	15	14	13	12	11	10	9
SDMA_ADDRESS							
R/W							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDMA_ADDRESS							
R/W							
0h							

Table 14-13361. MMCSD_CTL_CFG_SDMA_SYS_ADDR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SDMA_ADDRESS	R/W	0h	When Host Version 4 Enable is set to 0 in the Host Control 2 register,DMA uses this register as system address in only 32-bit addressing mode. Auto CMD23 cannot be used with SDMA. When Host Version 4 Enable is set to 1, SDMA uses ADMA System Address register [05Fh-058h] instead of using this register to support both 32-bit and 64-bit addressing. This register is re-assigned to 32-bit Block Count and then SDMA may use Auto CMD23.[1] SDMA System Address [Host Version 4 Enable = 0] This register contains the system memory address for a SDMA transfer in 32-bit addressing mode. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing [i.e., after a transaction has stopped]. Reading this register during SDMA transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data posi- tion can be read from this register. The SDMA transfer waits at the every boundary specified by the SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register [003h] is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. [2] 32-bit Block Count [Host Version 4 Enable = 1] Host Controller Version 4.10 re-defines this register as 32-bit Block Count [Refer to Section 1.15 for more details about block count extension]. In version 4.00, this register may be used as 32-bit block count only for Auto CMD23 to set the argument of the CMD23 while executing Auto CMD23. The Host Controller would decrement the block count of this register every block transfer and data transfer stops when the count reaches zero. This register should be accessed only when no transaction is executing. Reading this register during data transfers may return invalid value. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.34 MMCSD_CTL_CFG_SDMA_SYS_ADDR_HI Register

14.7.4.6.2.34.1 MMCSD_CTL_CFG_SDMA_SYS_ADDR_HI Register (Offset = 2h) [reset = 0h]

This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

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Table 14-13362. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0002h

Figure 14-6593. MMCSD_CTL_CFG_SDMA_SYS_ADDR_HI Name Register

16	15	14	13	12	11	10	9
SDMA_ADDRESS							
R/W							
0h							
8	7	6	5	4	3	2	1
SDMA_ADDRESS							
R/W							
0h							

Table 14-13363. MMCSD_CTL_CFG_SDMA_SYS_ADDR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SDMA_ADDRESS	R/W	0h	This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.35 MMCSD_CTL_CFG_BLOCK_SIZE Register

14.7.4.6.2.35.1 MMCSD_CTL_CFG_BLOCK_SIZE Register (Offset = 4h) [reset = 0h]

This register is used to configure the number of bytes in a data block

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Table 14-13364. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0004h

Figure 14-6594. MMCSD_CTL_CFG_BLOCK_SIZE Name Register

16	15	14	13	12	11	10	9
RESERVED	SDMA_BUF_SIZE			XFER_BLK_SIZE			
NONE	R/W			R/W			
0h	0h			0h			
8	7	6	5	4	3	2	1
XFER_BLK_SIZE							
R/W							
0h							

Table 14-13365. MMCSD_CTL_CFG_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:12	SDMA_BUF_SIZE	R/W	0h	To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the HC generates the DMA Interrupt to request the HD to update the System Address register. These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. 7 6 5 4 3 2 1 0
11:0	XFER_BLK_SIZE	R/W	0h	This field specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. It can be accessed only if no transaction is executing [i.e after a transaction has stopped]. Read operations during transfer return an invalid value and write operations shall be ignored. 2048 512 2 1 0

14.7.4.6.2.36 MMCSD_CTL_CFG_BLOCK_COUNT Register

14.7.4.6.2.36.1 MMCSD_CTL_CFG_BLOCK_COUNT Register (Offset = 6h) [reset = 0h]

This register is used to configure the number of data blocks

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Table 14-13366. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0006h

Figure 14-6595. MMCSD_CTL_CFG_BLOCK_COUNT Name Register

16	15	14	13	12	11	10	9
XFER_BLK_CNT							
R/W							
0h							
8	7	6	5	4	3	2	1
XFER_BLK_CNT							
R/W							
0h							

Table 14-13367. MMCSD_CTL_CFG_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description

15:0	XFER_BLK_CNT	R/W	0h	Host Controller Version 4.10 extends block count to 32-bit [Refer to Section 1.15].Selection of either 16-bit Block Count register or 32-bit Block Count register is defined as follows: [1] If Host Version 4 Enable in the Host Control 2 register is set to 0 or 16-bit Block Count register is set to non-zero, 16-bit Block Count register is selected [2] If Host Version 4 Enable is set to 1 and 16-bit Block Count register is set to zero, 32-bit Block Count register is selected.Use of 16-bit/32-bit Block Count register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1 and the maximum block count.The Host Controller decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0 results in no data blocks is transferred.This register should be accessed only when no transaction is executing [i.e., after transactions are stopped]. During data transfer,read operations on this register may return an invalid value and write operations are ignored.
				`65535`
				`3`
				`2`
				`1`
				`0`

14.7.4.6.2.37 MMCSD_CTL_CFG_ARGUMENT1_LO Register

14.7.4.6.2.37.1 MMCSD_CTL_CFG_ARGUMENT1_LO Register (Offset = 8h) [reset = 0h]

This register contains Lower bits of SD Command Argument

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Table 14-13368. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0008h

Figure 14-6596. MMCSD_CTL_CFG_ARGUMENT1_LO Name Register

16	15	14	13	12	11	10	9
CMD_ARG1							
R/W							
0h							
8	7	6	5	4	3	2	1
CMD_ARG1							
R/W							
0h							

Table 14-13369. MMCSD_CTL_CFG_ARGUMENT1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_ARG1	R/W	0h	The SD Command Argument is specified as bit23-8 of Command-Format. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.38 MMCSD_CTL_CFG_ARGUMENT1_HI Register

14.7.4.6.2.38.1 MMCSD_CTL_CFG_ARGUMENT1_HI Register (Offset = Ah) [reset = 0h]

This register contains higher bits of SD Command Argument

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Table 14-13370. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 000Ah

Figure 14-6597. MMCSD_CTL_CFG_ARGUMENT1_HI Name Register

16	15	14	13	12	11	10	9
CMD_ARG1							
R/W							
0h							
8	7	6	5	4	3	2	1
CMD_ARG1							
R/W							
0h							

Table 14-13371. MMCSD_CTL_CFG_ARGUMENT1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_ARG1	R/W	0h	The SD Command Argument is specified as bit39-24 of Command-Format. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.39 MMCSD_CTL_CFG_TRANSFER_MODE Register

14.7.4.6.2.39.1 MMCSD_CTL_CFG_TRANSFER_MODE Register (Offset = Ch) [reset = 0h]

This register is used to control the operations of data transfers

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Table 14-13372. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 000Ch

Figure 14-6598. MMCSD_CTL_CFG_TRANSFER_MODE Name Register

16	15	14	13	12	11	10	9
RESERVED							RESP_INTR_DIS
NONE							R/W
0h							0h
8	7	6	5	4	3	2	1
RESP_ERR_CHK_ENA	RESP_TYPE	MULTI_BLK_SEL	DATA_XFER_DIR	AUTO_CMD_ENA		BLK_CNT_ENA	DMA_ENA
R/W	R/W	R/W	R/W	R/W		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-13373. MMCSD_CTL_CFG_TRANSFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	NONE	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error,sets this bit to 0 and waits Command Complete Interrupt and then checks the response register. If Host Controller checks response error, sets this bit to 1 and sets Response Error Check Enable to 1. Command Complete Interrupt is disabled by this bit regardless of Command Complete Signal Enable. 1 Disable Response Interrupt 0 Enable Response Interrupt
7	RESP_ERR_CHK_ENA	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.If Host Driver checks response error, this bit is set to 0 and Response Interrupt Disable is set to 0.If Host Controller checks response error, sets this bit to 1 and sets Response Interrupt Disable to 1. Response Type R1 / R5 selects either R1 or R5 response type. If an error is detected, Response Error Interrupt is generated in the Response Error Interrupt Status register. 1 Enable Response Error Check 0 Disable Response Error Check
6	RESP_TYPE	R/W	0h	When response error check is enabled, this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1 .Bit31 OUT_OF_RANGE .Bit30 ADDRESS_ERROR .Bit29 BLOCK_LEN_ERROR .Bit26 WP_VIOLATION .Bit25 CARD_IS_LOCKED .Bit23 COM_CRC_ERROR .Bit21 CARD_ECC_FAILED .Bit20 CC_ERROR .Bit19 ERROR Response Flags Checked in R5 .Bit07 COM_CRC_ERROR .Bit03 ERROR .Bit01 FUNCTION_NUMBER .Bit00 OUT_OF_RANGE 1 SDIO 0 Memory

Table 14-13373. MMCSD_CTL_CFG_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MULTI_BLK_SEL	R/W	0h	This bit enables multiple block data transfers. 1 Multiple Block transfer 0 Single Block transfer
4	DATA_XFER_DIR	R/W	0h	This bit defines the direction of data transfers. 1 Read from Card to Host 0 Write from Host to Card
3:2	AUTO_CMD_ENA	R/W	0h	There are three methods to stop Multiple-block read and write operation. [1] Auto CMD12 Enable: Multiple-block read and write commands for memory require CMD12 to stop the operation. When this field is set to 01b, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the Auto CMD Error Status register. The Host Driver shall not set this bit if the command does not require CMD12. When Host Version 4 Enable =0, CMD12 is issued when 16-bit Block Count is expired. When Host Version 4 Enable =1, CMD12 is issued when 16-bit Block Count or 32-bit Block Count is expired. [2] Auto CMD23 Enable: When this bit field is set to 10b, the Host Controller issues a CMD23 automatically before issuing a command specified in the Command register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23. The following conditions are required to use the Auto CMD23. Auto CMD23 Supported [Host Controller Version is 3.00 or later]. A memory card that supports CMD23 [SCR[33]=1]. If DMA is used, it shall be ADMA. Only when CMD18 or CMD25 is issued. Auto CMD23 can be used with or without ADMA. By writing the Command register, the Host Controller issues a CMD23 first and then issues a command specified by the Command Index in Com-mand register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the Auto CMD Error Status register.32-bit block count value for CMD23 is set to 32-bit Block Count [SDMA System Address] register. [3] Auto CMD Auto Select [Version 4.10] As CMD23 is optional for SD memory card except UHS 104 card, if card supports CMD23, Auto CMD 23 should be used instead of Auto CMD12. Host Controller Version 4.10 defines this Auto CMD Auto Select mode. Selection of Auto CMD depends on setting of CMD23 Enable in the Host Control 2 register which indicates whether card supports CMD23. If CMD23 Enable =1, Auto CMD23 is used and if CMD23 Enable =0, Auto CMD12 is used. In case of Version 4.10 or later, use of Auto CMD Auto Select is recommended rather than use of Auto CMD12 Enable or Auto CMD23 Enable. 3 2 1 0
1	BLK_CNT_ENA	R/W	0h	This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. 1 Enable Block count 0 Disable Block count
0	DMA_ENA	R/W	0h	DMA can be enabled only if DMA Support bit in the Capabilities register is set. If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register [00Fh]. 1 DMA mode is Enabled 0 DMA mode is Disabled

14.7.4.6.2.40 MMCSD_CTL_CFG_COMMAND Register

14.7.4.6.2.40.1 MMCSD_CTL_CFG_COMMAND Register (Offset = Eh) [reset = 0h]

This register is used to program the Command for host controller

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Table 14-13374. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 000Eh

Figure 14-6599. MMCSD_CTL_CFG_COMMAND Name Register

16	15	14	13	12	11	10	9
RESERVED		CMD_INDEX					
NONE		R/W					
0h		0h					
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
CMD_TYPE		DATA_PRESENT	CMD_INDEX_CHK_ENA	CMD_CRC_CHK_ENA	SUB_CMD	RESP_TYPE_SEL	
R/W		R/W	R/W	R/W	R/W	R/W	
0h		0h	0h	0h	0h	0h	

Table 14-13375. MMCSD_CTL_CFG_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	NONE	0h	Reserved
13:8	CMD_INDEX	R/W	0h	This bit shall be set to the command number [CMD0-63, ACMD0-63]. Reset Source: vbus_amod_g_rst_n
7:6	CMD_TYPE	R/W	0h	There are three types of special commands. Suspend, Resume andAbort. These bits shall bet set to 00b for all other commands. Suspend Command: If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state. and the HD shall restart the transfer by setting Continue Request in the Block Gap Control Register. Resume Command: The HD re-starts the data transfer by restoring the registers in the range of 000-00Dh. The HC shall check for busy before starting write transfers. Abort Command: If this command is set when exe- cuting a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a writetransfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset. 3 2 1 0
5	DATA_PRESENT	R/W	0h	This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. If is set to 0 for the following: 1. Commands using only CMD line [ex. CMD52]. 2. Commands with no data transferbut using busy signal on DAT[0]line [R1b or R5b ex. CMD38]. 3. Resume Command. 1 Data present 0 Data not Present

Table 14-13375. MMCSD_CTL_CFG_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CMD_INDEX_CHK_ENA	R/W	0h	If this bit is set to 1, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 `Enable Command Index Check` 0 `Disable Command Index Check`
3	CMD_CRC_CHK_ENA	R/W	0h	If this bit is set to 1, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. 1 `Enable Command CRC Check` 0 `Disable Command CRC Check`
2	SUB_CMD	R/W	0h	This bit is added from Version 4.10 to distinguish a main command or sub command [Refer to Section 1.17]. When issuing a main command, this bit is set to 0 and when issuing a sub command, this bit is set to 1. Setting of this bit is checked by Sub Command Status in the Present State register.Host Driver manages whether main or sub command. Host Controller does not refer to this bit to issue a command. 1 `Sub Command` 0 `Main Command`
1:0	RESP_TYPE_SEL	R/W	0h	Response Type Select. 3 2 1 0

14.7.4.6.2.41 MMCSD_CTL_CFG_RESPONSE Register

14.7.4.6.2.41.1 MMCSD_CTL_CFG_RESPONSE Register (Offset = 10h) [reset = 0h]

This register is used to store responses from SD Cards

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Table 14-13376. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0010h

Figure 14-6600. MMCSD_CTL_CFG_RESPONSE Name Register

16	15	14	13	12	11	10	9
CMD_RESP							
R							
0h							
8	7	6	5	4	3	2	1
CMD_RESP							
R							
0h							

Table 14-13377. MMCSD_CTL_CFG_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMD_RESP	R	0h	R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.42 MMCSD_CTL_CFG_DATA_PORT Register

14.7.4.6.2.42.1 MMCSD_CTL_CFG_DATA_PORT Register (Offset = 20h) [reset = 0h]

This register is used to access internal buffer

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Table 14-13378. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0020h

Figure 14-6601. MMCSD_CTL_CFG_DATA_PORT Name Register

32	31	30	29	28	27	26	25
BUF_RD_DATA							
R/W							
0h							
24	23	22	21	20	19	18	17
BUF_RD_DATA							
R/W							
0h							
16	15	14	13	12	11	10	9
BUF_RD_DATA							
R/W							
0h							
8	7	6	5	4	3	2	1
BUF_RD_DATA							
R/W							
0h							

Table 14-13379. MMCSD_CTL_CFG_DATA_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BUF_RD_DATA	R/W	0h	The Host Controller Buffer can be accessed through this 32-bit Data Port Register. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.43 MMCSD_CTL_CFG_PRESENTSTATE Register

14.7.4.6.2.43.1 MMCSD_CTL_CFG_PRESENTSTATE Register (Offset = 24h) [reset = 1F00000h]

The Host Driver can get status of the Host Controller from this 32-bit read-only register

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Table 14-13380. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0024h

Figure 14-6602. MMCSD_CTL_CFG_PRESENTSTATE Name Register

32	31	30	29	28	27	26	25
UHS2_IF_DETECTION	UHS2_IF_LANE_SYNC	UHS2_DORMANT	SUB_COMMAND_STS	CMD_NOT_ISS_BY_ERR	RESERVED		SDIF_CMDIN
R	R	R	R	R	NONE		R
0h	0h	0h	0h	0h	0h		1h
24	23	22	21	20	19	18	17
SDIF_DAT3IN	SDIF_DAT2IN	SDIF_DAT1IN	SDIF_DAT0IN	WRITE_PROTECT	CARD_DETECT	CARD_STATE_STABLE	CARD_INSERTED
R	R	R	R	R	R	R	R
1h	1h	1h	1h	0h	0h	0h	0h
16	15	14	13	12	11	10	9
RESERVED				BUF_RD_ENA	BUF_WR_ENA	RD_XFER_ACTIVE	WR_XFER_ACTIVE
NONE				R	R	R	R
0h				0h	0h	0h	0h
8	7	6	5	4	3	2	1
SDIF_DAT7IN	SDIF_DAT6IN	SDIF_DAT5IN	SDIF_DAT4IN	RETUNING_REQ	DATA_LINE_ACTIVE	INHIBIT_DAT	INHIBIT_CMD
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13381. MMCSD_CTL_CFG_PRESENTSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UHS2_IF_DETECTION	R	0h	This status indicates whether a card supports UHS-II IF. This status is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 regis-ter. UHS-II interface initialization is activated by setting SD Clock Enable in the Clock Control reg-ister. Host Controller drives STB.L on D0 lanefrom EIDL state and waits for receiving STB.L on D1 lane. This bit is set to 1 if STB.L is detected on D1 lane. Host Controller shall compensate latency from setting SD Clock Enable to output STB.L on D0 lane when reading this status [Refer to Figure 3-35 about details of this method]. This bit may be read any time after setting SD Clock Enable for faster UHS-II IF detection but Host Driver shall check this status at least 200us period from set- ting SD Clock Enable until detecting UHS-II IF. After UHS-II IF is detected, this bit is cleared by when EIDL is detected on D0 lane, UHS-II Inter-face Enable is set to 0 or Host full reset is exe-cuted. '0' UHS-II IF is not detected '1' UHS-II IF is detected Reset Source: vbus_amod_g_rst_n

Table 14-13381. MMCSD_CTL_CFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	UHS2_IF_LANE_SYNC	R	0h	This status indicates whether lane is synchronized in UHS-II mode. This status is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 register. On detecting UHS-II Interface [D31=1], Host Controller provides SYN LSS on D0 lane and waits for receiving SYN LSS on D1 lane. If SYN LSS is detected on D1 lane, Host Controller pro-vides LIDL LSS on D0 lane and waits for receiving LIDL LSS on D1 lane. In case of Version 4.00, this bit indicates comple-tion of Device PHY Initialization by detecting LIDL LSS on D1 lane.From Version 4.10, Host Controller may imple-ment a specific PHY verification method and PHY Initialization Failure can be indicated by keeping this bit to 0 even LIDL LSS is detected on D1 lane.Host Driver detects PHY Initialization Failure by timeout.This bit is cleared by when D0 lane is set to EIDL,UHS-II Interface Enable is set to 0 or executes Host full reset. 1 `UHS-II PHY is initialized` 0 `UHS-II PHY is not initialized`
29	UHS2_DORMANT	R	0h	This status indicates whether UHS-II lanes enterDormant state. This function is enabled by setting UHS-II Interface Enable to 1 in the Host Control 2 register. On issuing GO_DORMAT_STATE com-mand, Go Dormant Command [111b]; is set to Command type in the UHS-II Command register.This command type acts as a trigger to enterlanes into dormant state. Host Controller provides STB.H and EIDL on D0 lane and waits for receiv-ing STB.H and EIDL on D1 lane. This bit is set to 1 after the time of T_DMT_ENTRY [750 RCLK cycle] or more from detecting EIDL on D1 lane. RCLK may be stopped in dormant state, by setting SD Clock Enable to 0 in the Clock Control register while In Dormant State bit is set to 1. On writingClock Control register with setting SD Clock Enable to 1, Host Controller wakes lanes to exit Dormant State and In Dormant State is set to 0. In case of the card enters Hibernate Mode [RCLK is stopped], Host Driver may turn off VDD1 by clearing SD Bus Power for VDD1 bit in the Power Control register. Host Controller shall turn off VDD1 after stopping RCLK. This bit is cleared by when Host Controller drives STB.L on D0 lane, UHS-II Interface Enable is set to 0 or executesHost full reset. 1 `In DORMANT state` 0 `Not in DORMANT state`
28	SUB_COMMAND_STS	R	0h	The Command register and Response register are commonly used for main command and sub command. This status is used to distinguish which response error statuses, main command or sub command, indicated in the Error Interrupt Status register or in the UHS-II Error Interrupt Status register. Refer to Section 1.17 about details of response error statuses. Just before reading of this register, the Sub Command Flag of the Command register or the UHS-II Command register is copied to this status. This status is effective not only when Response Error interrupt is generated but also when data error interrupt is generated with Command Not Issued by Error [D27 of this register] or Auto CMD Error interrupt is generated with Command Not Issued by Error by Auto CMD12 in the Auto CMD Error Status register. 1 - Sub Command Status 0 - Main Command Status Reset Source: vbus_amod_g_rst_n
27	CMD_NOT_ISS_BY_ERR	R	0h	Setting of this status indicates that a command cannot be issued due to an error except Auto CMD12 error. [Equivalent error status by Auto CMD12 error is defined as Command Not Issued By Auto CMD12 Error in the Auto CMD Error Status register.] This status is set to 1 when Host Controller cannot issue a command after setting Command register or UHS-II Command register.Refer to Section 3.10 about 2L-HD error case inUHS-II mode.Sub Command Status [D28] indicates which command is not issued [main or sub]. 1 - Command cannot be issued 0 - No error for issuing a command Reset Source: vbus_amod_g_rst_n
26:25	RESERVED	NONE	0h	Reserved

Table 14-13381. MMCSD_CTL_CFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	SDIF_CMDIN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
23	SDIF_DAT3IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[3]. Reset Source: vbus_amod_g_rst_n
22	SDIF_DAT2IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[2]. Reset Source: vbus_amod_g_rst_n
21	SDIF_DAT1IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[1]. Reset Source: vbus_amod_g_rst_n
20	SDIF_DAT0IN	R	1h	This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. Reset Source: vbus_amod_g_rst_n
19	WRITE_PROTECT	R	0h	The Write Protect Switch is supported for memory and combo cards.This bit reflects the SDWP# pin. 1 `Write enabled (SDWP# = 0)` 0 `Write protected (SDWP# = 1)`
18	CARD_DETECT	R	0h	This bit reflects the inverse value of the SDCD# pin. '0' No Card present [SDCD# = 1] '1' Card present [SDCD# = 0] Reset Source: vbus_amod_g_rst_n
17	CARD_STATE_STABLE	R	0h	This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1,it means the Card Detect Pin Level is stable. The Software Reset For All in the Software Reset Register shall not affect this bit. '0' Reset of Debouncing '1' No Card or Inserted Reset Source: vbus_amod_g_rst_n
16	CARD_INSERTED	R	0h	This bit indicates whether a card has been inserted. Changing from 0 to 1 generates a Card Insertion interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal Interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear SD Bus Power in the Power Control register and SD Clock Enable in the Clock control register. In addition the HD should clear the HC by the Software Reset For All in Software register. The card detect is active regardless of the SD Bus Power. '0' Reset or Debouncing or No Card '1' Card Inserted Reset Source: vbus_amod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11	BUF_RD_ENA	R	0h	This status is used for non-DMA read transfers.This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 1 `Read Enable` 0 `Read Disable`

Table 14-13381. MMCSD_CTL_CFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	BUF_WR_ENA	R	0h	This status is used for non-DMA write transfers.This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. 1 `Write Enable` 0 `Write Disable`
9	RD_XFER_ACTIVE	R	0h	This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: After the end bit of the read command. When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: When the last data block as specified by block length is transferred to the system. When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. '0' No valid data '1' Transferring data 1 `Transferring data` 0 `No valid data`
8	WR_XFER_ACTIVE	R	0h	This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: After the end bit of the write command. When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: After getting the CRC status of the last data block as specified by the transfer count [Single or Multiple] After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 1 `Transferring data` 0 `No valid data`
7	SDIF_DAT7IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
6	SDIF_DAT6IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
5	SDIF_DAT5IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
4	SDIF_DAT4IN	R	0h	This status is used to check DAT line level to recover from errors, and for debugging. Reset Source: vbus_amod_g_rst_n
3	RETUNING_REQ	R	0h	Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 [using fixed sampling clock]. 1 `Sampling clock needs re-tuning` 0 `Fixed or well tuned sampling clock`

Table 14-13381. MMCSD_CTL_CFG_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

2	DATA_LINE_ACTIVE	R	0h	This bit indicates whether one of the DAT line on SD bus is in use.
				`1 DAT line active`
				`0 DAT line inactive`

1	INHIBIT_DAT	R	0h	This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit [DAT] [ex. R1b, R5b type]. Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal interrupt status register. Note: The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. '0' Can issue command which uses the DAT line '1' Cannot issue command which uses the DATline Reset Source: vbus_amod_g_rst_n
0	INHIBIT_CMD	R	0h	SD Mode If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register [00Fh] is written. This bit is cleared when the command response is received. Even if the Command Inhibit [DAT] is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 gener- ates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issuethe command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Com- mand Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 opera- tion, Host Controller shall manage to issue two commands: CMD12 and a command set by Com-mand register. UHS-II Mode This bit is 0 means that a command packet can be issued by the Host Controller. While this bit is set to 1, which means the Host Controller is not ready to issue a next command, Host Driver shall not write the registers from UHS-II BlockSize [Offset 080h] to the UHS-II Command [Offset 09Eh]. Changing from 1 to 0 generates a Command Complete Interrupt in the Normal Interrupt Status-register. 1- Host Controller is not ready to issue a com-mand 0 - Host Controller is ready to issue a command Version 4.10 adds a new control to prevent error statuses from overwriting by receipt of a next com-mand. This status keeps indicating 1 while any of response error statuses is set to 1 [as described in Section 1.17], Command Not Issued by Error in this register is set to 1 or Command Not Issued by Auto CMD12 Error in the Auto CMD Error Status register is set to 1. Software Reset For CMD Lineis used to clear the error statuses above and this status. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.44 MMCSD_CTL_CFG_HOST_CONTROL1 Register

14.7.4.6.2.44.1 MMCSD_CTL_CFG_HOST_CONTROL1 Register (Offset = 28h) [reset = 0h]

This register is used to program DMA modes, LED Control, Data Transfer Width, High Speed Enable, Card detect test level and signal selection

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Table 14-13382. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0028h

Figure 14-6603. MMCSD_CTL_CFG_HOST_CONTROL1 Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
CD_SIG_SEL	CD_TEST_LEVEL	EXT_DATA_WIDTH	DMA_SELECT		HIGH_SPEED_ENA	DATA_WIDTH	LED_CONTROL
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0h	0h	0h	0h		0h	0h	0h

Table 14-13383. MMCSD_CTL_CFG_HOST_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CD_SIG_SEL	R/W	0h	This bit selects source for card detection. '0' SDCD# is selected [for normal use] '1' The card detect test level is selected Reset Source: vbus_amod_g_rst_n
6	CD_TEST_LEVEL	R/W	0h	This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. Generates [card ins or card removal] interrupt when the normal int sts enable bit is set. '0' No Card '1' Card Inserted Reset Source: vbus_amod_g_rst_n
5	EXT_DATA_WIDTH	R/W	0h	This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilities register. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register.This bit is not effective when multiple devices are installed on a bus slot [Slot Type is set to 10b in the Capabilities register]. In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register. 1 8-bit bus width 0 Bus width is selected by data transfer width

Table 14-13383. MMCSD_CTL_CFG_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	DMA_SELECT	R/W	0h	This field is used to select DMA type. The Host Driver shall check support of DMA modes by referring the Capabilities register. Selected DMA is enabled by DMA Enable of the Transfer Mode register in SD mode and DMA Enable of UHS-II Transfer Mode register in UHS-II mode. [1] Up to Version 3.00 When Host Version 4 Enable is set to 0, setting of this field is compatible to Host Controller Version 3.00.SDMA is initiated by writing to the Command register when this field is set to 00b and the SDMA System Address regis-ter [32-bit] is used. SDMA does not support 64-bit address-ing.ADMA2 is initiated by writing to the Command register when this field is set to 10b or 11b. Lower 32-bit of the ADMA Sys-tem Address register is used when this field is set to 10b and 64-bit of the ADMA System Address register is used when this field is set to 11b. Support of 64-bit System Addressing is indicated by 64-bit System Address Support for V3 in the Capabilities register. 64-bit AMDA2 uses 96-bit Descriptor. 00 - SDMA is selected 01 - 32-bit Address ADMA1 is selected 10 -32-bit Address ADMA2 is selected 11 - 64-bit Address ADMA2 is selected [Optional] [2] Version 4.00 or later When Host Version 4 Enable is set to 1, setting of this field is changed as follows. SDMA is initiated by Host Driver writes to the Command reg-ister when this field is set to 00b.ADMA2 is initiated by Host Driver writes to the Command register when this field is set to 10b or 11b and by ADMA3 sets to the ADMA System Address register when this field is set to 11b. ADMA3 is initiated by Host Driver writes to the ADMA3 IDAddress register when this field is set to 11b. 00 - SDMA is selected 01 - Not Used [New assignment is not allowed] 10 - ADMA2 is selected [AMDA3 is not supported or dis-abled] 11 - ADMA2 or ADMA3 is selected Support of 64-bit DMA and 128-bit Descriptor is indicated by 64-bit System Address Support for V4 in the Capabilities register. If the support bit is set to 1, all supported DMAs [depends on Support, ADMA2 Support and ADMA3 Sup-port] shall support 64-bit addressing. 64-bit Addressing in the Host Controller 2 register selects either 32-bit or 64-bit system addressing of DMAs. Reset Source: vbus_amod_g_rst_n
2	HIGH_SPEED_ENA	R/W	0h	This bit is optional. Before setting this bit, the HD shall check the High Speed Support in the capabilities register. If this bit is set to 0 [default], the HC outputs CMD line and DAT lines at the falling edge of the SD clock [up to 25 MHz/20MHz for MMC]. If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock [up to 50 MHz for SD/52MHz for MMC]/ 208Mhz [for SD3.0] If Preset Value Enable in the Host Control 2 register is set to 1, Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. This bit is not effective in UHS-II mode. 1 0
1	DATA_WIDTH	R/W	0h	This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. This bit is not effective in UHS-II mode. 1 0
0	LED_CONTROL	R/W	0h	This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. 1 0

14.7.4.6.2.45 MMCSD_CTL_CFG_POWER_CONTROL Register

14.7.4.6.2.45.1 MMCSD_CTL_CFG_POWER_CONTROL Register (Offset = 29h) [reset = 0h]

This register is used to program the SD Bus power and voltage level

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Table 14-13384. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0029h

Figure 14-6604. MMCSD_CTL_CFG_POWER_CONTROL Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
UHS2_VOLTAGE			UHS2_POWER	SD_BUS_VOLTAGE			SD_BUS_POWER
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 14-13385. MMCSD_CTL_CFG_POWER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	UHS2_VOLTAGE	R/W	0h	This field determines supply voltage range to VDD2. This field can be set to 101b if 1.8V VDD2 Support in the Capabilities register is set to 1. '000' VDD2 Not supported '001'- '011' Reserved '100' Reserved for 1.2V '101' 1.8V '110' Not Used '111' Not Used Reset Source: vbus_amod_g_rst_n

4	UHS2_POWER	R/W	0h	Setting this bit enables providing VDD2. '0' Power Off '1' Power On
				`1 Power On`
				`0 Power Off`

3:1	SD_BUS_VOLTAGE	R/W	0h	By setting these bits, the HD selects the voltage level for the SD card. Before setting this register, the HD shall check the voltage support bits in the capabilities register. If an unsupported voltage is selected, the Host System shall not supply SD bus voltage. '000'- '100' Reserved '101' 1.8V '110' 3.0V '111' 3.3V 7 6 5 0

0	SD_BUS_POWER	R/W	0h	Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. If this bit is cleared, the Host Control-ler should immediately stop driving CMD and DAT[3:0] [tri-state], and drive SDCLK to low level [Refer to Section 2.2.14]. If card is connectedto Host Controller, Host Controller shall set these lines to low before stopping to supply VDD1.In UHS-II mode, before clearing this bit, Host Driver shall clear SD Clock Enable and before stopping to sup-ply VDD1, Host Controller shall set DAT[2] to low if DAT[2] is used as out-of band interrupt.
				`1 Power On`
				`0 Power Off`

14.7.4.6.2.46 MMCSD_CTL_CFG_BLOCK_GAP_CONTROL Register

14.7.4.6.2.46.1 MMCSD_CTL_CFG_BLOCK_GAP_CONTROL Register (Offset = 2Ah) [reset = 80h]

This register is used to program the block gap request, read wait control and interrupt at block gap

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Table 14-13386. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 002Ah

Figure 14-6605. MMCSD_CTL_CFG_BLOCK_GAP_CONTROL Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
BOOT_ACK_ENA	ALT_BOOT_MODE	BOOT_ENABLE	SPI_MODE	INTRPT_AT_BLK_GAP	RDWAIT_CTRL	CONTINUE	STOP_AT_BLK_GAP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	0h

Table 14-13387. MMCSD_CTL_CFG_BLOCK_GAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOT_ACK_ENA	R/W	1h	To check for the boot acknowledge in boot operation. 1 `Wait for boot ack from eMMC card` 0 `Will not wait for boot ack from eMMC card`
6	ALT_BOOT_MODE	R/W	0h	To start boot code access in alternative mode. 1 `To start alternative boot code access` 0 `To stop alternative boot code access`
5	BOOT_ENABLE	R/W	0h	To start boot code access. 1 `To start boot code access` 0 `To stop boot code access`
4	SPI_MODE	R/W	0h	SPI mode enable bit. 1 `SPI Mode` 0 `SD Mode`
3	INTRPT_AT_BLK_GAP	R/W	0h	This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. Reset Source: vbus_amod_g_rst_n
2	RDWAIT_CTRL	R/W	0h	The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported. In UHS-II mode, Read Wait is disabled and DAT[2] line is used for Interrupt Signal from UHS-II Card. 1 `Enable Read-Wait Control` 0 `Disable Read-Wait Control`

Table 14-13387. MMCSD_CTL_CFG_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CONTINUE	R/W	0h	This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0 and set this bit to restart the transfer. The Host Controller automatically clears this bit when the transaction re-starts. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. In SD mode, this bit is cleared in either of the following cases: [1] In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. [2] In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts. Therefore it is not necessary for Host driver to set this bit to 0. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. '0' Ignore '1' Restart 1 `Restart` 0 `Ignore`
0	STOP_AT_BLK_GAP	R/W	0h	This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers. Until the transfer complete is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The HC shall honour Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1. In case of write transfers in which the HD writes data to the Buffer Data Port register, the HD shall set this bit after all block data is written. If this bit is set to 1, the HD shall not write data to Buffer data port register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit [DAT] in the Present State register. In case of UHS-II, a transaction can be stopped at the boundary of DATA Burst [Flow Control basis]. Host Control-ler waits for sending Flow Control MSG until Continue Request is set to 1. '0' Transfer '1' Stop 1 `Stop` 0 `Transfer`

14.7.4.6.2.47 MMCSD_CTL_CFG_WAKEUP_CONTROL Register

14.7.4.6.2.47.1 MMCSD_CTL_CFG_WAKEUP_CONTROL Register (Offset = 2Bh) [reset = 0h]

This register is used to program the wakeup functionality

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Table 14-13388. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 002Bh

Figure 14-6606. MMCSD_CTL_CFG_WAKEUP_CONTROL Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
RESERVED					CARD_REMOVAL	CARD_INSERTION	CARD_INTERRUPT
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-13389. MMCSD_CTL_CFG_WAKEUP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	CARD_REMOVAL	R/W	0h	This bit enables wakeup event via Card removal assertion in the Normal Interrupt Status register.FN_WUS [Wake up Support] in CIS does not affect this bit. 1 `Enable wakeup event via Card removal` 0 `Disable wakeup event`
1	CARD_INSERTION	R/W	0h	This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.FN_WUS [Wake up Support] in CIS does not affect this bit. 1 `Enable wakeup event via Card Insertion` 0 `Disable wakeup event`
0	CARD_INTERRUPT	R/W	0h	This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register.This bit can be set to 1 if FN_WUS [Wake Up Support] in CIS is set to 1. 1 `Enable wakeup event via Card Interrupt` 0 `Disable wakeup event`

14.7.4.6.2.48 MMCSD_CTL_CFG_CLOCK_CONTROL Register

14.7.4.6.2.48.1 MMCSD_CTL_CFG_CLOCK_CONTROL Register (Offset = 2Ch) [reset = 0h]

This register is used to program the Clock frequency select, generator select, Clock enable, Internal Clock state fields This register controls SDCLK in SD Mode and RCLK in UHS-II mode.

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Table 14-13390. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 002Ch

Figure 14-6607. MMCSD_CTL_CFG_CLOCK_CONTROL Name Register

16	15	14	13	12	11	10	9
SDCLK_FRQSEL							
R/W							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDCLK_FRQSEL_UPBITS		CLKGEN_SEL	RESERVED	PLL_ENA	SD_CLK_ENA	INT_CLK_STABLE	INT_CLK_ENA
R/W		R/W	NONE	R/W	R/W	R	R/W
0h		0h	0h	0h	0h	0h	0h

Table 14-13391. MMCSD_CTL_CFG_CLOCK_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	SDCLK_FRQSEL	R/W	0h	This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the capabilities register. Only the following settings are allowed. [1] 8-bit Divided Clock Mode 80h - base clock divided by 256 40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32 08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock[10MHz-63MHz] Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register. [1] 25 MHz divider value. [2] 400 KHz divider value. The frequency of the SDCLK is set by the following formula: Clock Frequency = [Baseclock] / divisor. Thus choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. Maximum Frequency for SD = 50Mhz [base clock] Maximum Frequency for MMC = 52Mhz [base clock] Minimum Frequency = 195.3125Khz [50Mhz / 256], same calculation for MMC also. [2] 10-bit Divided Clock Mode Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to10 bits and all divider values shall be supported. 3FFh --1/2046 Divided Clock N -------1/2N Divided Clock [Duty 50%] 002h -- 1/4 Divided Clock 001h ---1/2 Divided Clock 000h --- Base Clock [10MHz-254MHz] Reset Source: vbus_amod_g_rst_n
7:6	SDCLK_FRQSEL_UPBITS	R/W	0h	Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select. Reset Source: vbus_amod_g_rst_n

Table 14-13391. MMCSD_CTL_CFG_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLKGEN_SEL	R/W	0h	This bit is used to select the clock generator mode in SDCLK Frequency Select. If the Programmable Clock Mode is supported [non-zero value is set to Clock Multiplier in the Capabilities register], this bit attribute is RW, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers. '0' Divided Clock Mode '1' Programmable Clock Mode 1 Programmable Clock Mode 0 Divided Clock Mode
4	RESERVED	NONE	0h	Reserved
3	PLL_ENA	R/W	0h	This bit is added from Version 4.10 for Host Controller using PLL. This feature allows Host Controller to initialize clock generator in two steps: by Internal Clock Enable and PLL Enable and to minimize output latency [ex. SDCLK/RCLK, D0lane] from SD Clock Enable. There are two modes to keep Host Drivers compatibility. In both modes, PLL Locked timing is indicated by Internal Clock Stable. [1] When Host Version 4 Enable =0 [Host Driver Version 3, which does not support this bit] or this bit is not implemented,Internal Clock Enable [or SD Clock Enable] may activate PLL [exit low power mode and start locking clock]. [2] When Host Version 4 Enable =1 [Host Driver Version 4],Internal Clock Enable is set before setting this bit and then setting this bit may activate PLL [exit low power mode and start locking clock]. 1 PLL is enabled 0 PLL is in low power mode
2	SD_CLK_ENA	R/W	0h	The HC shall stop SDCLK when writing this bit to 0. SDCLK frequency Select can be changed when this bit is 0. Then, the HC shall maintain the same clock frequency until SDCLK is stopped [Stop at SDCLK = 0]. If the HC detects the No Card state, this bit shall be cleared. 1 0
1	INT_CLK_STABLE	R	0h	This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. Note: This is useful when using PLL for a clock oscillator that requires setup time. 1 0
0	INT_CLK_ENA	R/W	0h	This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the HC shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection. 1 0

14.7.4.6.2.49 MMCSD_CTL_CFG_TIMEOUT_CONTROL Register

14.7.4.6.2.49.1 MMCSD_CTL_CFG_TIMEOUT_CONTROL Register (Offset = 2Eh) [reset = 0h]

The register sets the Data Timeout counter value

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Table 14-13392. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 002Eh

Figure 14-6608. MMCSD_CTL_CFG_TIMEOUT_CONTROL Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
RESERVED				COUNTER_VALUE			
NONE				R/W			
0h				0h			

Table 14-13393. MMCSD_CTL_CFG_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	NONE	0h	Reserved
3:0	COUNTER_VALUE	R/W	0h	This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sdclockTMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable [in the Error Interrupt Status Enable register]. 1111 - Reserved 1110 - TMCLK * 2^27 ------------------- -------------------- 0001 - TMCLK * 2^14 0000 - TMCLK * 2^13 Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.50 MMCSD_CTL_CFG_SOFTWARE_RESET Register

14.7.4.6.2.50.1 MMCSD_CTL_CFG_SOFTWARE_RESET Register (Offset = 2Fh) [reset = 0h]

This register is used to program the software reset for data, command and for all

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Table 14-13394. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 002Fh

Figure 14-6609. MMCSD_CTL_CFG_SOFTWARE_RESET Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
RESERVED					SWRST_FOR_ DAT	SWRST_FOR_ CMD	SWRST_FOR_ ALL
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-13395. MMCSD_CTL_CFG_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	SWRST_FOR_DAT	R/W	0h	Only part of data circuit is reset. The following registers and bits are cleared by this bit: Buffer Data Port Register: Buffer is cleared and Initialized. Present State register: Buffer read Enable, Buffer write Enable, Read Transfer Active, Write Transfer Active, DAT Line Active, Command Inhibit [DAT]. Block Gap Control register: Continue Request, Stop At Block Gap Request. Normal Interrupt Status register: Buffer Read Ready, Buffer Write Ready, Block Gap Event, Transfer Complete. 1 0
1	SWRST_FOR_CMD	R/W	0h	Software Reset For CMD Line Only part of command circuit is reset to be able to issue a command. From Version 4.10, this bit is also used to initialize UHS-II command circuit. This reset is effective only command issuing circuit [including response error statuses related to Com-mand Inhibit [CMD] control] and does not affect data transfer circuit. Host Controller can continue data transfer even this reset is executed during handling of sub com- mand response errors. The following registers and bits are cleared by this bit: Present State register Command Inhibit [CMD] Normal Interrupt Status register Command Complete Error Interrupt Status [from Version 4.10] Response error statuses related to Com-mand Inhibit [CMD] 1 0
0	SWRST_FOR_ALL	R/W	0h	This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD. 1 0

14.7.4.6.2.51 MMCSD_CTL_CFG_NORMAL_INTR_STS Register

14.7.4.6.2.51.1 MMCSD_CTL_CFG_NORMAL_INTR_STS Register (Offset = 30h) [reset = 0h]

This register gives the status of all the interrupts

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Table 14-13396. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0030h

Figure 14-6610. MMCSD_CTL_CFG_NORMAL_INTR_STS Name Register

16	15	14	13	12	11	10	9
ERROR_INTR	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTR
R	R/W1TC	R/W1TC	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
CARD_REM	CARD_INS	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13397. MMCSD_CTL_CFG_NORMAL_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ERROR_INTR	R	0h	If any of the bits in the Error Interrupt Status Register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. In UHS-II mode is enabled, if any of the bits in the UHS-II Error Interrupt Status register are set, this bit is also set. '0' No error '1' Error 1 Error interrupt is generated 0 No Interrupt
14	BOOT_COMPLETE	R/W1TC	0h	This status is set if the boot operation gets terminated. '0' Boot operation is not terminated '1' Boot operation is terminated 1 Boot Terminate interrupt is generated 0 No Interrupt
13	RCV_BOOT_ACK	R/W1TC	0h	This status is set if the boot acknowledge is received from device. '0' Boot ack not recieved '1' Boot ack is recieved 1 Boot acknowledge is received 0 No Interrupt
12	RETUNING_EVENT	R	0h	This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer [not large block count] can be completed without re-tuning.In UHS-II mode, this bit is not effective '0' Re-tuning not required '1' Re-tuning should be performed Reset Source: vbus_amod_g_rst_n
11	INTC	R	0h	This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor. Reset Source: vbus_amod_g_rst_n
10	INTB	R	0h	This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor. Reset Source: vbus_amod_g_rst_n

Table 14-13397. MMCSD_CTL_CFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	INTA	R	0h	This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor. NOTE : INT_A, INT_B, and INT_C are to be implemented based on the Application Requirements. By default these are not implemented as there is no specific requirement from Customers. Reset Source: vbus_amod_g_rst_n

8	CARD_INTR	R	0h	When this status has been set and the Host Driver needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status Enable register may be set to 0 in order to clear the card interrupt status latched in the Host Controller and to stop driv-ing the interrupt signal to the Host System.After completion of the card interrupt service [It should reset interrupt factors in the SD card and the interrupt signal may not be asserted],set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt fac-tor. [1] DAT[1] Interrupt Input in SD Mode In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt sig-nal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the inter-rupt to the Host System. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of UHS-I mode, switching time of Interrupt Period is relaxed for 2 clock cycles. Then Host Controller needs to delay start of interrupt sampling at least 2 clocks and should sample interrupt while Interrupt Period is sta-ble. [2] DAT[2] Interrupt Input in UHS-II Mode When Card Inserted in the Present State reg-ister and SD Bus Power for VDD1 in the Power Control register are set to 1, Host Con-troller configures DAT[2] as Interrupt Input and enables pull-up of DAT[2]. DAT[2] interrupt is asynchronous to RCLK, low level sensitive and 3.3V signal level. DAT[2] interrupt is masked by setting Card Interrupt Status Enable to 0 in the Normal Interrupt register.When either Card Inserted or SD Bus Power for VDD1 is set to 0, Host Controller sets DAT[2] to low. Only point to point connection is allowed between Host and Card. [3] INT MSG in UHS-II Mode INT MSG is enabled by setting INT MSG Enable in the UHS-II Device Select register. DAT[2] and INT MSG interrupt sources are ORed and indicated to Card Interrupt. If any bit in the UHS-II Device Interrupt Status regis- ter is set to 1, INT MSG interrupt is generated. INT MSG interrupt is cleared by writing a cor-respondent bit to 1 in the UHS-II Device Inter-rupt Status register. Masking DAT[2] interrupt also disables INT MSG interupt due to Card Interrupt Status Enable is set to 0. SDIO Ver-sion 4.00 does not support INT MSG. '0' No Card Interrupt '1' Generate Card Interrupt
				`1 Card interrupt is generated`
				`0 No Interrupt`

7	CARD_REM	R/W1TC	0h	This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. '0' Card State Stable or Debouncing '1' Card Removed
				`1 Card removal interrupt is generated`
				`0 No Interrupt`

6	CARD_INS	R/W1TC	0h	This status is set if the Card Inserted in the Present State register changes from 0 to 1.When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. '0' Card State Stable or Debouncing '1' Card Inserted
				`1 Card insertion interrupt is generated`
				`0 No Interrupt`

Table 14-13397. MMCSD_CTL_CFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	BUF_RD_READY	R/W1TC	0h	This status is set if the Buffer Read Enable changes from 0 to 1. Buffer Read Ready is set to 1 for every CMD19 execution in tuning procedure.In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' Not ready to read buffer, '1' Ready to read buffer 1 `Buffer Read Ready interrupt is generated` 0 `No Interrupt`
4	BUF_WR_READY	R/W1TC	0h	This status is set if the Buffer Write Enable changes from 0 to 1.In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' Not ready to write to buffer, '1' Ready to write to buffer 1 `Buffer Write Ready interrupt is generated` 0 `No Interrupt`
3	DMA_INTERRUPT	R/W1TC	0h	This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser. '0' No DMA Interrupt '1' DMA Interrupt is generated 1 `DMA interrupt is generated` 0 `No Interrupt`
2	BLK_GAP_EVENT	R/W1TC	0h	If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set. Read Transaction: This bit is set at the falling edge of the DAT Line Active Status [When the transaction is stopped at SD Bus timing. The Read Wait must be supported inorder to use this function]. Write Transaction: This bit is set at the falling edge of Write Transfer Active Status [After getting CRC status at SD Bus timing]. In UHS-II mode, this bit is set at FC [Flow Control] unit basis. '0' No Block Gap Event '1' Transaction stopped at Block Gap 1 `Block Gap Event is generated` 0 `No Interrupt`

Table 14-13397. MMCSD_CTL_CFG_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XFER_COMPLETE	R/W1TC	0h	This bit is set when a read / write transaction is completed. SD Mode Read Transaction: This bit is set at the falling edge of Read Transfer Active Status. There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length [After the last data has been read to the Host Sys- tem]. The second is when data has stopped at the block gap and completed the data transfer by setting the Stop At Block Gap Request in the Block Gap Control Register [After valid data has been read to the Host System]. Write Transaction: This bit is set at the falling edge of the DAT Line Active Status. There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control Register and data transfers completed. [After valid data is written to the SD card and the busy signal is released]. Note: Transfer Complete has higher priority than Data Time-out Error. If both bits are set to 1, the data transfer can be considered complete. Note: While performing tuning procedure [Execute Tuning is set to 1], Transfer Complete is not set to 1 Command with Busy: This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit[DAT] in the Present State register.UHS-I mode While performing tuning procedure [Execute Tuning is set to 1], Transfer Complete is not set to 1. '0' No Data Transfer Complete, '1' Data Transfer Complete UHS-II Mode This interrupt is generated in following twocases: [a] EBSY Completion [for EBSY supported commands] When EBSY Wait in the UHS-II Transfer Mode register is set to 1, this bit is set when EBSY packet has been received, and all valid data have been sent to system memory in case of read operation. [b] Stop and Continue during DCMD Data Transfer When Stop At Block Gap Request in the Block Gap Control register is set to 1 and data transfer is stopped at the Flow Control. Following is for both SD mode and UHS-II mode. The table below shows that Transfer Com-plete has higher priority than Data Timeout Error. If both bits are set to 1, execution of a command can be considered to be completed. 1 - Command execution is completed 0 - Not complete 1 Transfer complete interrupt is generated 0 No Interrupt
0	CMD_COMPLETE	R/W1TC	0h	SD Mode This bit is set when we get the end bit of the command response [Except Auto CMD12 and Auto CMD23] Note: Command Time-out Error has higher priority than Command Complete. If both are set to 1, it can be considered that the response was not received correctly. Version 4.00 defines response check function for R1 and R5. If Response Interrupt Disable in the Transfer Mode register is set to 1, gen-eration of this interrupt is prohibited regardless of Command Complete Signal Enable. UHS-II Mode If Response Interrupt Disable is set to 0 in the UHS-II Transfer Mode register, this interrupt is generated when response packet is received.If Response Interrupt Disable is set to 1 in the UHS-II Transfer Mode register, generation of this interrupt is prohibited regardless of Com-mand Complete Signal Enable. '0' No Command Complete, '1' Command Complete 1 Command complete interrupt is generated 0 No Interrupt

14.7.4.6.2.52 MMCSD_CTL_CFG_ERROR_INTR_STS Register

14.7.4.6.2.52.1 MMCSD_CTL_CFG_ERROR_INTR_STS Register (Offset = 32h) [reset = 0h]

This register gives the status of the error interrupts

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Table 14-13398. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0032h

Figure 14-6611. MMCSD_CTL_CFG_ERROR_INTR_STS Name Register

16	15	14	13	12	11	10	9
RESERVED			HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13399. MMCSD_CTL_CFG_ERROR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12	HOST	R/W1TC	0h	Occurs when detecting ERROR in m_hresp[dma transaction] 1 Host Error 0 No Error
11	RESP	R/W1TC	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1.If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. 1 Response Error 0 No Error
10	TUNING	R/W1TC	0h	This bit is set when an unrecoverable error is detected in a tuning circuit except during tuning procedure [Occurrence of an error during tuning procedure is indicated by Sampling Select]. By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning.To reset tuning circuit, Sampling Clock shall be set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Turning Error, the Host Driver should discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from tuning circuit error. 1 Tuning Error 0 No Error
9	ADMA	R/W1TC	0h	This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. 1 ADMA Error 0 No Error

Table 14-13399. MMCSD_CTL_CFG_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	AUTO_CMD	R/W1TC	0h	Auto CMD12 and Auto CMD23 use this error status.This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared with clearing of this bit [another implementation is also allowed]. 1 `Auto CMD Error` 0 `No Error`
7	CURR_LIMIT	R/W1TC	0h	By setting the SD Bus Power bit in the Power Control Register, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function. 1 `Power Fail` 0 `No Error`
6	DATA_ENDBIT	R/W1TC	0h	Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 1 `Data Endbit Error` 0 `No Error`
5	DATA_CRC	R/W1TC	0h	Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010. 1 `Data CRC Error` 0 `No Error`
4	DATA_TIMEOUT	R/W1TC	0h	Occurs when detecting one of following timeout conditions: 1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout. 1 `Data Timeout Error` 0 `No Error`
3	CMD_INDEX	R/W1TC	0h	Occurs if a Command Index error occurs in the Command Response. 1 `Command Index Error` 0 `No Error`
2	CMD_ENDBIT	R/W1TC	0h	Occurs when detecting that the end bit of a command response is 0. 1 `Command End bit Error` 0 `No Error`
1	CMD_CRC	R/W1TC	0h	Command CRC Error is generated in two cases. 1. If a response is returned and the Command Time-out Error is set to 0, this bit is set to 1 when detecting a CRT error in the command response 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command [Stop driving CMD line] and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. 1 `Command CRC Error` 0 `No Error`
0	CMD_TIMEOUT	R/W1TC	0h	Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case Command CRC Error shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. 1 `Command Timeout Error` 0 `No Error`

14.7.4.6.2.53 MMCSD_CTL_CFG_NORMAL_INTR_STS_ENA Register

14.7.4.6.2.53.1 MMCSD_CTL_CFG_NORMAL_INTR_STS_ENA Register (Offset = 34h) [reset = 0h]

This register is used to enable the normal interrupt status register fields

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Table 14-13400. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0034h

Figure 14-6612. MMCSD_CTL_CFG_NORMAL_INTR_STS_ENA Name Register

16	15	14	13	12	11	10	9
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13401. MMCSD_CTL_CFG_NORMAL_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	The HC shall control error Interrupts using the Error Interrupt Status Enable register. Reset Source: vbus_amod_g_rst_n
14	BOOT_COMPLETE	R/W	0h	'0' Masked '1' Enabled 1 0
13	RCV_BOOT_ACK	R/W	0h	'0' Masked '1' Enabled 1 0
12	RETUNING_EVENT	R/W	0h	0 - Masked 1 - Enabled 1 0
11	INTC	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts. 1 0
10	INTB	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts. 1 0
9	INTA	R/W	0h	If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts. 1 0

Table 14-13401. MMCSD_CTL_CFG_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CARD_INTERRUPT	R/W	0h	If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The HD may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. By setting this bit to 0, interrupt input should be masked by implementation so that the interrupt Input is not affected by external signal in any state [ex. floating]. 1 0
7	CARD_REMOVAL	R/W	0h	'0' Masked '1' Enabled 1 0
6	CARD_INSERTION	R/W	0h	'0' Masked '1' Enabled 1 0
5	BUF_RD_READY	R/W	0h	'0' Masked '1' Enabled 1 0
4	BUF_WR_READY	R/W	0h	'0' Masked '1' Enabled 1 0
3	DMA_INTERRUPT	R/W	0h	'0' Masked, '1' Enabled 1 0
2	BLK_GAP_EVENT	R/W	0h	'0' Masked '1' Enabled 1 0
1	XFER_COMPLETE	R/W	0h	'0' Masked '1' Enabled 1 0
0	CMD_COMPLETE	R/W	0h	'0' Masked '1' Enabled 1 0

14.7.4.6.2.54 MMCSD_CTL_CFG_ERROR_INTR_STS_ENA Register

14.7.4.6.2.54.1 MMCSD_CTL_CFG_ERROR_INTR_STS_ENA Register (Offset = 36h) [reset = 0h]

This register is used to enable the Error Interrupt Status register fields

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Table 14-13402. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0036h

Figure 14-6613. MMCSD_CTL_CFG_ERROR_INTR_STS_ENA Name Register

16	15	14	13	12	11	10	9
RESERVED	VENDOR_SPECIFIC		HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13403. MMCSD_CTL_CFG_ERROR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:13	VENDOR_SPECIFIC	R/W	0h	N/A Reset Source: vbus_amod_g_rst_n
12	HOST	R/W	0h	'0' Masked '1' Enabled 1 0
11	RESP	R/W	0h	'0' Masked '1' Enabled 1 0
10	TUNING	R/W	0h	'0' Masked '1' Enabled 1 0
9	ADMA	R/W	0h	'0' Masked '1' Enabled 1 0
8	AUTO_CMD	R/W	0h	'0' Masked '1' Enabled 1 0
7	CURR_LIMIT	R/W	0h	'0' Masked '1' Enabled 1 0
6	DATA_ENDBIT	R/W	0h	'0' Masked '1' Enabled 1 0
5	DATA_CRC	R/W	0h	'0' Masked '1' Enabled 1 0

Table 14-13403. MMCSD_CTL_CFG_ERROR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DATA_TIMEOUT	R/W	0h	'0' Masked '1' Enabled 1 0
3	CMD_INDEX	R/W	0h	'0' Masked '1' Enabled 1 0
2	CMD_ENDBIT	R/W	0h	'0' Masked '1' Enabled 1 0
1	CMD_CRC	R/W	0h	'0' Masked '1' Enabled 1 0
0	CMD_TIMEOUT	R/W	0h	'0' Masked '1' Enabled 1 0

14.7.4.6.2.55 MMCSD_CTL_CFG_NORMAL_INTR_SIG_ENA Register

14.7.4.6.2.55.1 MMCSD_CTL_CFG_NORMAL_INTR_SIG_ENA Register (Offset = 38h) [reset = 0h]

This register is used to enable the Normal Interrupt Signal register

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Table 14-13404. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0038h

Figure 14-6614. MMCSD_CTL_CFG_NORMAL_INTR_SIG_ENA Name Register

16	15	14	13	12	11	10	9
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
CARD_REMOVAL	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13405. MMCSD_CTL_CFG_NORMAL_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	The HD shall control error Interrupts using the Error Interrupt Signal Enable register. Reset Source: vbus_amod_g_rst_n
14	BOOT_COMPLETE	R/W	0h	'0' Masked '1' Enabled 1 0
13	RCV_BOOT_ACK	R/W	0h	'0' Masked '1' Enabled 1 0
12	RETUNING_EVENT	R/W	0h	'0' Masked '1' Enabled 1 0
11	INTC	R/W	0h	'0' Masked '1' Enabled 1 0
10	INTB	R/W	0h	'0' Masked '1' Enabled 1 0
9	INTA	R/W	0h	'0' Masked '1' Enabled 1 0
8	CARD_INTERRUPT	R/W	0h	'0' Masked '1' Enabled 1 0
7	CARD_REMOVAL	R/W	0h	'0' Masked '1' Enabled 1 0

Table 14-13405. MMCSD_CTL_CFG_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CARD_INSERTION	R/W	0h	'0' Masked '1' Enabled 1 0
5	BUF_RD_READY	R/W	0h	'0' Masked '1' Enabled 1 0
4	BUF_WR_READY	R/W	0h	'0' Masked '1' Enabled 1 0
3	DMA_INTERRUPT	R/W	0h	'0' Masked '1' Enabled 1 0
2	BLK_GAP_EVENT	R/W	0h	'0' Masked '1' Enabled 1 0
1	XFER_COMPLETE	R/W	0h	'0' Masked '1' Enabled 1 0
0	CMD_COMPLETE	R/W	0h	'0' Masked '1' Enabled 1 0

14.7.4.6.2.56 MMCSD_CTL_CFG_ERROR_INTR_SIG_ENA Register

14.7.4.6.2.56.1 MMCSD_CTL_CFG_ERROR_INTR_SIG_ENA Register (Offset = 3Ah) [reset = 0h]

This register is used to enable Error Interrupt Signal register

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Table 14-13406. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 003Ah

Figure 14-6615. MMCSD_CTL_CFG_ERROR_INTR_SIG_ENA Name Register

16	15	14	13	12	11	10	9
RESERVED	VENDOR_SPECIFIC		HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13407. MMCSD_CTL_CFG_ERROR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:13	VENDOR_SPECIFIC	R/W	0h	N/A Reset Source: vbus_amod_g_rst_n
12	HOST	R/W	0h	'0' Masked '1' Enabled 1 0
11	RESP	R/W	0h	'0' Masked '1' Enabled 1 0
10	TUNING	R/W	0h	'0' Masked '1' Enabled 1 0
9	ADMA	R/W	0h	'0' Masked '1' Enabled 1 0
8	AUTO_CMD	R/W	0h	'0' Masked '1' Enabled 1 0
7	CURR_LIMIT	R/W	0h	'0' Masked '1' Enabled 1 0
6	DATA_ENDBIT	R/W	0h	'0' Masked '1' Enabled 1 0
5	DATA_CRC	R/W	0h	'0' Masked '1' Enabled 1 0

Table 14-13407. MMCSD_CTL_CFG_ERROR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DATA_TIMEOUT	R/W	0h	'0' Masked '1' Enabled 1 0
3	CMD_INDEX	R/W	0h	'0' Masked '1' Enabled 1 0
2	CMD_ENDBIT	R/W	0h	'0' Masked '1' Enabled 1 0
1	CMD_CRC	R/W	0h	'0' Masked '1' Enabled 1 0
0	CMD_TIMEOUT	R/W	0h	'0' Masked '1' Enabled 1 0

14.7.4.6.2.57 MMCSD_CTL_CFG_AUTOCMD_ERR_STS Register

14.7.4.6.2.57.1 MMCSD_CTL_CFG_AUTOCMD_ERR_STS Register (Offset = 3Ch) [reset = 0h]

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD 23

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Table 14-13408. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 003Ch

Figure 14-6616. MMCSD_CTL_CFG_AUTOCMD_ERR_STS Name Register

16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
CMD_NOT_ISSUED	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD12_NOT_EXEC
R	NONE	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13409. MMCSD_CTL_CFG_AUTOCMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7	CMD_NOT_ISSUED	R	0h	Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error [D04- D01] in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. 1 `Not Issued` 0 `No Error`
6	RESERVED	NONE	0h	Reserved
5	RESP	R	0h	This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or Auto CMD23. This status should be ignored if any bit of D00 to D04 is set to 1. 1 `Auto Command Response Error` 0 `No Error`
4	INDEX	R	0h	Occurs if the Command Index error occurs in response to a command. 1 `Auto Command Index Error` 0 `No Error`
3	ENDBIT	R	0h	Occurs when detecting that the end bit of command response is 0. 1 `Auto Command End Bit Error` 0 `No Error`
2	CRC	R	0h	Occurs when detecting a CRC error in the command response. 1 `Auto Command CRC Error` 0 `No Error`
1	TIMEOUT	R	0h	Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command.If this bit is set to 1, the other error status bits [D04 - D02] are meaningless. 1 `Auto Command Timeout Error` 0 `No Error`

Table 14-13409. MMCSD_CTL_CFG_AUTOCMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ACMD12_NOT_EXEC	R	0h	If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1, other error status bits [D04 - D01] are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23 1 `Not Executed` 0 `No Error`

14.7.4.6.2.58 MMCSD_CTL_CFG_HOST_CONTROL2 Register

14.7.4.6.2.58.1 MMCSD_CTL_CFG_HOST_CONTROL2 Register (Offset = 3Eh) [reset = 0h]

This register is used to program UHS Select Mode,UHS Select Mode,Driver Strength Select,Execute Tuning,Sampling Clock Select,Asynchronous Interrupt Enable and Preset value enable

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Table 14-13410. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 003Eh

Figure 14-6617. MMCSD_CTL_CFG_HOST_CONTROL2 Name Register

16	15	14	13	12	11	10	9
PRESET_VALUE_ENA	ASYNCH_INTR_ENA	BIT64_ADDRESSING	HOST_VER40_ENA	CMD23_ENA	ADMA2_LEN_MODE	DRIVER_STRENGTH2	UHS2_INTF_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SAMPLING_CLK_SELECT	EXECUTE_TUNING	DRIVER_STRENGTH1		V1P8_SIGNAL_ENA	UHS_MODE_SELECT		
R/W	R/W	R/W		R/W	R/W		
0h	0h	0h		0h	0h		

Table 14-13411. MMCSD_CTL_CFG_HOST_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PRESET_VALUE_ENA	R/W	0h	Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic. This bit enables the functions defined in the Preset Value registers. If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers. 1 `Automatic Selection by Preset Value are Enabled` 0 `SDCLK and Driver Strength are controlled by Host Driver`
14	ASYNCH_INTR_ENA	R/W	0h	This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode [and zero is set to Interrupt Pin Select in the Shared Bus Control register]. If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 1 `Asynchronous Interrupt enabled` 0 `Asynchronous Interrupt disabled`
13	BIT64_ADDRESSING	R/W	0h	This field is effective when Host Version 4.00 Enable is set to 1. Host Controller selects either of 32-bit or 64-bit addressing modes to access system memory. Whether 32-bit or 64-bit is determined by OS installed in a host system. Host Driver sets this bit depends on addressing mode of installed OS. Refer to 64-bit System Address Support in the Capabilities register. . 1 `64 bit addressing` 0 `32 bit addressing`

Table 14-13411. MMCSD_CTL_CFG_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	HOST_VER40_ENA	R/W	0h	This bit selects either Version 3.00 compatible mode or Ver4.mode. In Version 4.00, support of 64-bit System Addressing is modified. All DMAs support 64-bit System Addressing. UHS-II supported Host Driver shall enable this bit. In Version 4.10, supported 32-bit Block Count for all operations. Functions of following fields are modified. SDMA Address SDMA uses ADMA System Address register [05Fh-058h] instead of SDMA System Address register [Offset 003-000h] ADMA2 / ADMA3 Selection ADMA3 is selected by DMA Select in the Host Control 1 regis-ter. 64bit ADMA Descriptor Size 128bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1. Selection of 32-bit / 64-bit System Addressing Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register instead of DMA Select in the Host Control 1 register. 32-bit Block Count SDMA System Address register [003h-000h] is modified to 32-bit Block Count register. 1 `Version 4 Mode` 0 `Version 3.00 Compatible Mode`
11	CMD23_ENA	R/W	0h	In memory card initialization, Host Driver Version 4.10 checks whether card supports CMD23 by checking a bit SCR[33]. If the card supports CMD23 [SCR[33]=1], this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 datatransfer. Refer to Auto CMD Enable in the Transfer Mode regis-ter. 1 `CMD23 Enable` 0 `CMD23 Disable`
10	ADMA2_LEN_MODE	R/W	0h	This bit selects one of ADMA2 Length Modes either 16-bit or 26-bit. 1 `26-bit Data Length Mode` 0 `16-bit Data Length Mode`
9	DRIVER_STRENGTH2	R/W	0h	This is the programmed Drive STrength output and Bit[2] of the sdhccore_drivestrength value. Reset Source: vbus_amod_g_rst_n
8	UHS2_INTF_ENABLE	R/W	0h	This bit is used to enable UHS-II Interface. Before trying to start UHS-II initialization, this bit shall be set to 1. Before trying to start SD mode initialization, this bit shall be set to 0. This bit is used to enable UHS-II IF Detection, Lane Synchroni-zation and In Dormant State in the Present State register, and to select clock source of either SD mode or UHS-II mode. Host Controller shall not leave unused SD 4-bit Interface lines [CLK, CMD and DAT[3:2]] floating in UHS-II mode by using pull-up or driving to low. When DAT[2] is used as interrupt input in UHS-II mode, DAT[2] of Host Controller is set to input and then DAT[2] of SDIO card is set to output to avoid conflict. '0' 4-bit SD Interface enabled '1' UHS-II Interface enabled 1 `UHS-II Interface enabled` 0 `4-bit SD Interface enabled`
7	SAMPLING_CLK_SELECT	R/W	0h	This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. 1 `Tuned clock is used to sample data` 0 `Fixed clock is used to sample data`
6	EXECUTE_TUNING	R/W	0h	This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. '0' Not Tuned or Tuning Completed '1' Execute Tuning Reset Source: vbus_amod_g_rst_n

Table 14-13411. MMCSD_CTL_CFG_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	DRIVER_STRENGTH1	R/W	0h	Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the Capabilities register. This bit depends on setting of Preset Value Enable. If Preset Value Enable = 0, this field is set by Host Driver. If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers. 3 2 1 0
3	V1P8_SIGNAL_ENA	R/W	0h	This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms. Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling [One of support bits is set to 1: SDR50, SDR104 or DDR50 in the Capabilities register] and the card or device supports UHS-I. '0' 3.3V Signalling, '1' 1.8V Signalling 1 1.8V Signalling 0 3.3V Signalling
2:0	UHS_MODE_SELECT	R/W	0h	This field is used to select one of UHS-I modes or UHS-II mode.In case of UHS-I mode, this field is effective when 1.8V Signal-ing Enable is set to 1. In case of UHS-II mode, 1.8V Signaling Enable shall be set to 0. Setting of this field is used to select one of preset values in UHS-I or UHS-II mode. If Preset Value Enable in the Host Control 2 register is set to 1,Host Controller sets SDCLK/RCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more detail. 7 6 5 4 3 2 1 0

14.7.4.6.2.59 MMCSD_CTL_CFG_CAPABILITIES Register

14.7.4.6.2.59.1 MMCSD_CTL_CFG_CAPABILITIES Register (Offset = 40h) [reset = 180004073DECC7F4h]

This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initializa-tion.

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Table 14-13412. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0040h

Figure 14-6618. MMCSD_CTL_CFG_CAPABILITIES Name Register

63	62	61	60	59	58	57	
HS400_SUPPORT	RESERVED		VDD2_1P8_SUPPORT	ADMA3_SUPPORT	RESERVED	SPI_BLK_MODE	SPI_SUPPORT
R	NONE		R	R	NONE	R	R
0h	1h		1h	1h	1h	0h	0h
56	55	54	53	52	51	50	49
CLOCK_MULTIPLIER							
R							
0h							
48	47	46	45	44	43	42	41
RETUNING_MODES		TUNING_FOR_SDR50	RESERVED	RETUNING_TIMER_CNT			
R		R	NONE	R			
0h		0h	1h	4h			
40	39	38	37	36	35	34	33
RESERVED	DRIVERD_SUPPORT	DRIVERC_SUPPORT	DRIVERA_SUPPORT	UHS2_SUPPORT	DDR50_SUPPORT	SDR104_SUPPORT	SDR50_SUPPORT
NONE	R	R	R	R	R	R	R
1h	0h	0h	0h	0h	1h	1h	1h
16	15	14	13	12	11	10	9
BASE_CLK_FREQ							
R							
c8h							
8	7	6	5	4	3	2	1
TIMEOUT_CLK_UNIT	RESERVED	TIMEOUT_CLK_FREQ					
R	NONE	R					
0h	0h	1h					

Table 14-13413. MMCSD_CTL_CFG_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
63	HS400_SUPPORT	R	0h	1 HS400 is Supported 0 HS400 is Not Supported 1 HS400 Mode is Supported 0 HS400 Mode is not Supported
62:61	RESERVED	NONE	1h	Reserved
60	VDD2_1P8_SUPPORT	R	1h	This field indicates that support of VDD2 on Host system. 1 1.8V VDD2 is Supported 0 1.8V VDD2 is not Supported

Table 14-13413. MMCSD_CTL_CFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

59	ADMA3_SUPPORT	R	1h	This field indicates that support of ADMA3 on Host Controller.
				`1 ADMA3 is Supported`
				`0 ADMA3 is not Supported`

58	RESERVED	NONE	1h	Reserved

57	SPI_BLK_MODE	R	0h	This field indicates whether SPI Block Mode is supported or not.
				`1 SPI Block Mode is Supported`
				`0 SPI Block Mode is not Supported`

56	SPI_SUPPORT	R	0h	This field indicates whether SPI Mode is supported or not.
				`1 SPI Mode is Supported`
				`0 SPI Mode is not Supported`

55:48	CLOCK_MULTIPLIER	R	0h	This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator. 'FF' Clock Multiplier M = 256 --------- '02' Clock Multiplier M = 3 '01' Clock Multiplier M = 2 '00' Clock Multiplier is Not Supported. Reset Source: vbus_amod_g_rst_n

47:46	RETUNING_MODES	R	0h	This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver. '00' Mode 1 '01' Mode 2 '10' Mode 3 '11' Reserved. There are two re-tuning timings:Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.
				`3 Reserved`
				`2 Mode 3`
				`1 Mode 2`
				`0 Mode 1`

45	TUNING_FOR_SDR50	R	0h	If this bit is set to 1, this Host Controller requires tuning to operate SDR50. [Tuning is always required to operate SDR104]. '0' '1'
				`1 SDR50 requires tuning`
				`0 SDR50 does not require tuning`

44	RESERVED	NONE	1h	Reserved
43:40	RETUNING_TIMER_CNT	R	4h	This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. 0h - Get information via other source 1h = 1 seconds 2h = 2 seconds 3h = 4 seconds 4h = 8 seconds ------ n = 2[n-1] seconds ------ Bh = 1024 seconds Fh - Ch = Reserved Reset Source: vbus_amod_g_rst_n
39	RESERVED	NONE	1h	Reserved

38	DRIVERD_SUPPORT	R	0h	This bit indicates support of Driver Type D for 1.8 Signaling. '0' Driver Type D is Not supported, '1' Driver Type D is supported
				`1 Driver Type D is Supported`
				`0 Driver Type D is not Supported`

37	DRIVERC_SUPPORT	R	0h	This bit indicates support of Driver Type C for 1.8 Signaling. '0' Driver Type C is Not supported, '1' Driver Type C is supported
				`1 Driver Type C is Supported`
				`0 Driver Type C is not Supported`

36	DRIVERA_SUPPORT	R	0h	This bit indicates support of Driver Type A for 1.8 Signaling. '0' Driver Type A is Not supported, '1' Driver Type A is supported
				`1 Driver Type A is Supported`
				`0 Driver Type A is not Supported`

35	UHS2_SUPPORT	R	0h	This bit indicates whether Host controller supports UHS-II. If this bit is set to 1, 1.8V VDD2 Support shall be set to 1 [Host Sys- tem shall support VDD2 power supply]. 1 UHS-II is Supported 0 UHS-II is Not Supported
				`1 UHS-II is Supported`
				`0 UHS-II is not Supported`

Table 14-13413. MMCSD_CTL_CFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
34	DDR50_SUPPORT	R	1h	This bit indicates whether DDR50 is supported or not. 1 `DDR50 is Supported` 0 `DDR50 is not Supported`
33	SDR104_SUPPORT	R	1h	This bit indicates whether SDR104 is supported or not.SDR104 requires tuning. 1 `SDR104 is Supported` 0 `SDR104 is not Supported`
32	SDR50_SUPPORT	R	1h	If SDR104 is supported, this bit shall be set to 1. Bit 40 indicates whether SDR50 requires tuning or not. 1 `SDR50 is Supported` 0 `SDR50 is not Supported`
31:30	SLOT_TYPE	R	0h	This field indicates usage of a slot by a specific Host System. [A host controller register set is defined perslot.] Embedded slot for one device [01b] means that only one non-removable device is connected to a SD bus slot. Shared Bus Slot [10b] can be set if Host Controller supports Shared Bus Control register. The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus [10b], the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System. 3 2 1 0
29	ASYNCH_INTR_SUPPORT	R	1h	Refer to SDIO Specification Version 3.00 about asynchronous interrupt. 1 `Asynchronous Interrupt Supported` 0 `Asynchronous Interrupt not Supported`
28	ADDR_64BIT_SUPPORT_V3	R	1h	IMeaning of this bit is different depends on Versions [Refer to Table 2-35 for more details]. Host Controller Version 3.00 and Ver4.10 use this bit as 64-bit System Address support for V3 mode. Host Con- troller Version 4.00 uses this bit as 64-bit System Address support for both V3 and V4 modes. SDMA cannot be used in 64-bit Address-ing in Version 3 mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor may be enabled as follows: In case of Host Controller Version 3, 64-bit ADMA2 is enabled by DMA Select =11b in the Host Control 1 register. In case of Host Controller Version 4, 64-bitADMA2 for Version 3 is enabled by setting Host Version 4 Enable =0 and DMA Select = 11b. 1 - 64-bit System Address for V3 is Supported 0 - 64-bit System Address for V3 is not Supported 1 `64-bit System Address for V3 is Supported` 0 `64-bit System Address for V3 is not Supported`
27	ADDR_64BIT_SUPPORT_V4	R	1h	This bit is added from Version 4.10. Set-ting 1 to this bit indicates that the Host Controller supports 64-bit System Addressing of Version 4 mode [Refer to Table 2-35 for the summary of 64-bit system address support].. When this bit is set to 1, full or a part of 64-bit address should be used to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to 64bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Address-ing for Version 4 is enabled by setting Host Version 4 Enable =1, 64-bit Address-ing =1 in the Host Control 2 register.SDMA can be used and ADMA2 uses 128-bit Descriptor. 1 `64-bit System Address for V4 is Supported` 0 `64-bit System Address for V4 is not Supported`

Table 14-13413. MMCSD_CTL_CFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	VOLT_1P8_SUPPORT	R	1h	This bit indicates whether the HC supports 1.8V. 1 `1.8V Supported` 0 `1.8V Not Supported`
25	VOLT_3P0_SUPPORT	R	0h	This bit indicates whether the HC supports 3.0V. 1 `3.3V Supported` 0 `3.0V Not Supported`
24	VOLT_3P3_SUPPORT	R	1h	This bit indicates whether the HC supports 3.3V. 1 `3.3V Supported` 0 `3.3V Not Supported`
23	SUSP_RES_SUPPORT	R	1h	This bit indicates whether the HC supports Suspend / Resume functionality. If this bit is 0, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend / Resume commands. 1 `Suspend and Resume mechanism Supported` 0 `Suspend and Resume mechanism Not Supported`
22	SDMA_SUPPORT	R	1h	This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly.Version 4.10 Host Controller shall support SDMA if ADMA2 is supported. 1 `SDMA Supported` 0 `SDMA Not Supported`
21	HIGH_SPEED_SUPPORT	R	1h	This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25Mhz to 50 Mhz [for SD]/ 20MHz to 52MHz [for MMC]. 1 `High Speed Supported` 0 `High Speed Not Supported`
20	RESERVED	NONE	0h	Reserved
19	ADMA2_SUPPORT	R	1h	'0' ADMA2 Not Supported '1' ADMA2 Supported 1 `ADMA2 Supported` 0 `ADMA2 Not Supported`
18	BUS_8BIT_SUPPORT	R	1h	This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. This bit is not effective when Slot Type is set to 10b. In this case, refer to Bus Width Preset in the Shared Bus resister. 1 `Extended Media Bus Supported` 0 `Extended Media Bus Not Supported`
17:16	MAX_BLK_LENGTH	R	0h	This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. 3 2 1 0

Table 14-13413. MMCSD_CTL_CFG_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	BASE_CLK_FREQ	R	c8h	[1]6-bit Base Clock Frequency: This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are 1MHz. The supported clock range is 10MHz to 63MHz. '11xx xxxxb' Not Supported '0011 1111b' 63MHz '0000 0010b' 2MHz '0000 0001b' 1MHz '0000 0000b'Get Information via another method [2]8-bit Base Clock Frequency: This mode is supported by the Host Controller Version 3.00.Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. 'FFh' 255MHz '02h' 2MHz '01h' 1MHz '00h' Get Information via another method. If the real frequency is 16.5MHz, the lager value shall be set 0001 0001b [17MHz] because the Host Driver use this value to calculate the clock divider value [Refer to the SDCLK Frequency Select in the Clock Control register.] and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method. Reset Source: vbus_amod_g_rst_n
7	TIMEOUT_CLK_UNIT	R	0h	This bit shows the unit of base clock frequency used to detect Data Timeout Error. 1 `MHz` 0 `KHz`
6	RESERVED	NONE	0h	Reserved
5:0	TIMEOUT_CLK_FREQ	R	1h	This bit shows the base clock frequency used to detect Data Timeout Error. '000000' Get Information via another method, 'not 0' 1KHz to 63KHz/1MHz to 63MHz Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.60 MMCSD_CTL_CFG_MAX_CURRENT_CAP Register

14.7.4.6.2.60.1 MMCSD_CTL_CFG_MAX_CURRENT_CAP Register (Offset = 48h) [reset = 0h]

This register indicates maximum current capability for each voltage

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Table 14-13414. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0048h

Figure 14-6619. MMCSD_CTL_CFG_MAX_CURRENT_CAP Name Register

63	62	61	60	59	58	57	
RESERVED							
NONE							
0h							
56	55	54	53	52	51	50	49
RESERVED							
NONE							
0h							
48	47	46	45	44	43	42	41
RESERVED							
NONE							
0h							
40	39	38	37	36	35	34	33
VDD2_1P8V							
R							
0h							
16	15	14	13	12	11	10	9
VDD1_3P0V							
R							
0h							
8	7	6	5	4	3	2	1
VDD1_3P3V							
R							
0h							

Table 14-13415. MMCSD_CTL_CFG_MAX_CURRENT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	0h	Reserved
39:32	VDD2_1P8V	R	0h	Maximum Current for 1.8V VDD2 Reset Source: vbus_amod_g_rst_n
31:24	RESERVED	NONE	0h	Reserved
23:16	VDD1_1P8V	R	0h	Maximum Current for 1.8V VDD1 Reset Source: vbus_amod_g_rst_n
15:8	VDD1_3P0V	R	0h	Maximum Current for 3.0V VDD1 Reset Source: vbus_amod_g_rst_n
7:0	VDD1_3P3V	R	0h	Maximum Current for 3.3V VDD1 Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.61 MMCSD_CTL_CFG_FORCE_EVNT_ACMD_ERR_STS Register

14.7.4.6.2.61.1 MMCSD_CTL_CFG_FORCE_EVNT_ACMD_ERR_STS Register (Offset = 50h) [reset = 0h]

This register is not physically implemented, rather it is an address where Auto CMD Error Status register can be written. Writing 1 : set each bit of the Auto CMD12 Error Status Register Writing 0 : no effect.

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Table 14-13416. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0050h

Figure 14-6620. MMCSD_CTL_CFG_FORCE_EVNT_ACMD_ERR_STS Name Register

16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
CMD_NOT_ISS	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD_NOT_EXEC
W	NONE	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13417. MMCSD_CTL_CFG_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7	CMD_NOT_ISS	W	0h	Force Event for Command Not Issued by AUTO CMD12 Error. 1 `Interrupt is generated` 0 `No Interrupt`
6	RESERVED	NONE	0h	Reserved
5	RESP	W	0h	Force Event for AUTO CMD Response Error.. 1 `Interrupt is generated` 0 `No Interrupt`
4	INDEX	W	0h	Force Event for AUTO CMD Index Error.. 1 `Interrupt is generated` 0 `No Interrupt`
3	ENDBIT	W	0h	Force Event for AUTO CMD End Bit Error. 1 `Interrupt is generated` 0 `No Interrupt`
2	CRC	W	0h	Force Event for AUTO CMD Timeout Error. 1 `Interrupt is generated` 0 `No Interrupt`
1	TIMEOUT	W	0h	Force Event for AUTO CMD Timeout Error. 1 `Interrupt is generated` 0 `No Interrupt`
0	ACMD_NOT_EXEC	W	0h	Force Event for AUTO CMD12 Not Executed. 1 `Interrupt is generated` 0 `No Interrupt`

14.7.4.6.2.62 MMCSD_CTL_CFG_FORCE_EVNT_ERR_INT_STS Register

14.7.4.6.2.62.1 MMCSD_CTL_CFG_FORCE_EVNT_ERR_INT_STS Register (Offset = 52h) [reset = 0h]

This register is not physically implemented, rather it is an address where Error Interrupt Status register can be written.

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Table 14-13418. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0052h

Figure 14-6621. MMCSD_CTL_CFG_FORCE_EVNT_ERR_INT_STS Name Register

16	15	14	13	12	11	10	9
RESERVED			HOST	RESP	TUNING	ADMA	AUTO_CMD
NONE			W	W	W	W	W
0h			0h	0h	0h	0h	0h
8	7	6	5	4	3	2	1
CURR_LIM	DAT_ENDBIT	DAT_CRC	DAT_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13419. MMCSD_CTL_CFG_FORCE_EVNT_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12	HOST	W	0h	Force Event for Host Error 1 Interrupt is generated 0 No Interrupt
11	RESP	W	0h	Force Event for Response Error 1 Interrupt is generated 0 No Interrupt
10	TUNING	W	0h	Force Event for Tuning Error. 1 Interrupt is generated 0 No Interrupt
9	ADMA	W	0h	Force Event for ADMA Error. 1 Interrupt is generated 0 No Interrupt
8	AUTO_CMD	W	0h	Force Event for Auto CMD Error. 1 Interrupt is generated 0 No Interrupt
7	CURR_LIM	W	0h	Force Event for Current Limit Error. 1 Interrupt is generated 0 No Interrupt
6	DAT_ENDBIT	W	0h	Force Event for Data End Bit Error. 1 Interrupt is generated 0 No Interrupt
5	DAT_CRC	W	0h	Force Event for Data CRC Error. 1 Interrupt is generated 0 No Interrupt
4	DAT_TIMEOUT	W	0h	Force Event for Data Timeout Error. 1 Interrupt is generated 0 No Interrupt

Table 14-13419. MMCSD_CTL_CFG_FORCE_EVNT_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMD_INDEX	W	0h	Force Event for Command Index Error 1 `Interrupt is generated` 0 `No Interrupt`
2	CMD_ENDBIT	W	0h	Force Event for Command End Bit Error. 1 `Interrupt is generated` 0 `No Interrupt`
1	CMD_CRC	W	0h	Force Event for Command CRC Error. 1 `Interrupt is generated` 0 `No Interrupt`
0	CMD_TIMEOUT	W	0h	Force Event for CMD Timeout Error. 1 `Interrupt is generated` 0 `No Interrupt`

14.7.4.6.2.63 MMCSD_CTL_CFG_ADMA_ERR_STATUS Register

14.7.4.6.2.63.1 MMCSD_CTL_CFG_ADMA_ERR_STATUS Register (Offset = 54h) [reset = 0h]

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

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Table 14-13420. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0054h

Figure 14-6622. MMCSD_CTL_CFG_ADMA_ERR_STATUS Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
RESERVED					ADMA_LENGTH_ERR	ADMA_ERR_STATE	
NONE					R	R	
0h					0h	0h	

Table 14-13421. MMCSD_CTL_CFG_ADMA_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	NONE	0h	Reserved
2	ADMA_LENGTH_ERR	R	0h	This error occurs in the following 2 cases. While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 1 `Error set` 0 `No Error`
1:0	ADMA_ERR_STATE	R	0h	This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 D00 : ADMA Error State when error occurred Contents of SYS_SDR register. 3 `ST_TFR(Transfer Data) Points to the next of the error descriptor` 2 `Never set this state(Not Used)` 1 `ST_FDS(Fetch Descriptor)Points to the error descriptor` 0 `ST_STOP(Stop DMA) Points to next of the error descriptor`

14.7.4.6.2.64 MMCSD_CTL_CFG_ADMA_SYS_ADDRESS Register

14.7.4.6.2.64.1 MMCSD_CTL_CFG_ADMA_SYS_ADDRESS Register (Offset = 58h) [reset = 0h]

This register contains the physical address used for ADMA data transfer

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Table 14-13422. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0058h

Figure 14-6623. MMCSD_CTL_CFG_ADMA_SYS_ADDRESS Name Register

63	62	61	60	59	58	57	
ADMA_ADDR							
R/W							
0h							
56	55	54	53	52	51	50	49
ADMA_ADDR							
R/W							
0h							
48	47	46	45	44	43	42	41
ADMA_ADDR							
R/W							
0h							
40	39	38	37	36	35	34	33
ADMA_ADDR							
R/W							
0h							
16	15	14	13	12	11	10	9
ADMA_ADDR							
R/W							
0h							
8	7	6	5	4	3	2	1
ADMA_ADDR							
R/W							
0h							

Table 14-13423. MMCSD_CTL_CFG_ADMA_SYS_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	ADMA_ADDR	R/W	0h	The 32-bit addressing Host Driver uses lower 32-bit of this register [upper 32-bit should be set to 0] and shall program Descriptor Table on 32-bit boundary andset 32-bit boundary address to this register. DMA2/3 ignores lower 2-bit of this register and assumes it to be 00b. DMA in 64-bit addressing. The 64-bit addressing Host Driver uses all bits of this register and shall program Descriptor Table on 64-bit boundary and set 64-bit boundary address to this register. DMA2/3 ignores lower 3-bit of this register andassumes it to be 000b. SDMA If Host Version 4.00 Enable is set to 1, SDMA use this register to indicate System Address of data location instead of using SDMA System Address register [Offset 003-000h]. SDMA can be used in 32-bit and 64-bit addressing in Version 4.00. ADMA2 This register holds byte address of executing command of the Descriptor table. At the start of ADMA2, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. ADMA3 This register is set by ADMA3. Host Driver is not necessary to set this register. The ADMA3 increments address of this register,which points to next line, when every time fetching a Descriptor line. When Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state. Register Value - 00000000_xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.65 MMCSD_CTL_CFG_PRESET_VALUE0 Register

14.7.4.6.2.65.1 MMCSD_CTL_CFG_PRESET_VALUE0 Register (Offset = 60h) [reset = 100h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13424. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0060h

Figure 14-6624. MMCSD_CTL_CFG_PRESET_VALUE0 Name Register

16	15	14	13	12	11	10	9
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	100h	
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDCLK_FRQSEL							
R							
100h							

Table 14-13425. MMCSD_CTL_CFG_PRESET_VALUE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	100h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.66 MMCSD_CTL_CFG_PRESET_VALUE1 Register

14.7.4.6.2.66.1 MMCSD_CTL_CFG_PRESET_VALUE1 Register (Offset = 62h) [reset = 4h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13426. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0062h

Figure 14-6625. MMCSD_CTL_CFG_PRESET_VALUE1 Name Register

16	15	14	13	12	11	10	9
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	4h	
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDCLK_FRQSEL							
R							
4h							

Table 14-13427. MMCSD_CTL_CFG_PRESET_VALUE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	4h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.67 MMCSD_CTL_CFG_PRESET_VALUE2 Register

14.7.4.6.2.67.1 MMCSD_CTL_CFG_PRESET_VALUE2 Register (Offset = 64h) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13428. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0064h

Figure 14-6626. MMCSD_CTL_CFG_PRESET_VALUE2 Name Register

16	15	14	13	12	11	10	9
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	2h	
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDCLK_FRQSEL							
R							
2h							

Table 14-13429. MMCSD_CTL_CFG_PRESET_VALUE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.68 MMCSD_CTL_CFG_PRESET_VALUE3 Register

14.7.4.6.2.68.1 MMCSD_CTL_CFG_PRESET_VALUE3 Register (Offset = 66h) [reset = 4h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13430. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0066h

Figure 14-6627. MMCSD_CTL_CFG_PRESET_VALUE3 Name Register

16	15	14	13	12	11	10	9
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	4h	
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDCLK_FRQSEL							
R							
4h							

Table 14-13431. MMCSD_CTL_CFG_PRESET_VALUE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	4h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.69 MMCSD_CTL_CFG_PRESET_VALUE4 Register

14.7.4.6.2.69.1 MMCSD_CTL_CFG_PRESET_VALUE4 Register (Offset = 68h) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13432. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0068h

Figure 14-6628. MMCSD_CTL_CFG_PRESET_VALUE4 Name Register

<table>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="2">DRIVER_STRENGTH_SEL</td><td colspan="3">RESERVED</td><td>CLOCK_GENSEL</td><td colspan="2">SDCLK_FRQSEL</td></tr>
<tr><td colspan="2">R</td><td colspan="3">NONE</td><td>R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td>0h</td><td colspan="2">2h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">SDCLK_FRQSEL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-13433. MMCSD_CTL_CFG_PRESET_VALUE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.70 MMCSD_CTL_CFG_PRESET_VALUE5 Register

14.7.4.6.2.70.1 MMCSD_CTL_CFG_PRESET_VALUE5 Register (Offset = 6Ah) [reset = 1h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13434. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 006Ah

Figure 14-6629. MMCSD_CTL_CFG_PRESET_VALUE5 Name Register

16	15	14	13	12	11	10	9
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	1h	
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDCLK_FRQSEL							
R							
1h							

Table 14-13435. MMCSD_CTL_CFG_PRESET_VALUE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	1h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.71 MMCSD_CTL_CFG_PRESET_VALUE6 Register

14.7.4.6.2.71.1 MMCSD_CTL_CFG_PRESET_VALUE6 Register (Offset = 6Ch) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13436. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 006Ch

Figure 14-6630. MMCSD_CTL_CFG_PRESET_VALUE6 Name Register

16	15	14	13	12	11	10	9
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	0h	
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDCLK_FRQSEL							
R							
0h							

Table 14-13437. MMCSD_CTL_CFG_PRESET_VALUE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.72 MMCSD_CTL_CFG_PRESET_VALUE7 Register

14.7.4.6.2.72.1 MMCSD_CTL_CFG_PRESET_VALUE7 Register (Offset = 6Eh) [reset = 2h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13438. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 006Eh

Figure 14-6631. MMCSD_CTL_CFG_PRESET_VALUE7 Name Register

16	15	14	13	12	11	10	9
DRIVER_STRENGTH_SEL		RESERVED			CLOCK_GENSEL	SDCLK_FRQSEL	
R		NONE			R	R	
0h		0h			0h	2h	
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
SDCLK_FRQSEL							
R							
2h							

Table 14-13439. MMCSD_CTL_CFG_PRESET_VALUE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	2h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.73 MMCSD_CTL_CFG_PRESET_VALUE8 Register

14.7.4.6.2.73.1 MMCSD_CTL_CFG_PRESET_VALUE8 Register (Offset = 72h) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13440. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0072h

Figure 14-6632. MMCSD_CTL_CFG_PRESET_VALUE8 Name Register

<table>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="2">DRIVER_STRENGTH_SEL</td><td colspan="3">RESERVED</td><td>CLOCK_GENSEL</td><td colspan="2">SDCLK_FRQSEL</td></tr>
<tr><td colspan="2">R</td><td colspan="3">NONE</td><td>R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">SDCLK_FRQSEL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13441. MMCSD_CTL_CFG_PRESET_VALUE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.74 MMCSD_CTL_CFG_PRESET_VALUE10 Register

14.7.4.6.2.74.1 MMCSD_CTL_CFG_PRESET_VALUE10 Register (Offset = 74h) [reset = 0h]

This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

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Table 14-13442. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0074h

Figure 14-6633. MMCSD_CTL_CFG_PRESET_VALUE10 Name Register

<table>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="2">DRIVER_STRENGTH_SEL</td><td colspan="3">RESERVED</td><td>CLOCK_GENSEL</td><td colspan="2">SDCLK_FRQSEL</td></tr>
<tr><td colspan="2">R</td><td colspan="3">NONE</td><td>R</td><td colspan="2">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">SDCLK_FRQSEL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13443. MMCSD_CTL_CFG_PRESET_VALUE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 3 2 1 0
13:11	RESERVED	NONE	0h	Reserved
10	CLOCK_GENSEL	R	0h	This bit is effective when Host Controller supports programmable clock '0' Host Controller Ver2.00 Compatible Clock Generator '1' Programmable Clock Generator Reset Source: vbus_amod_g_rst_n
9:0	SDCLK_FRQSEL	R	0h	10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.75 MMCSD_CTL_CFG_ADMA3_DESC_ADDRESS Register

14.7.4.6.2.75.1 MMCSD_CTL_CFG_ADMA3_DESC_ADDRESS Register (Offset = 78h) [reset = 0h]

The start address of Integrated DMA Descriptor is set to this register.

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Table 14-13444. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0078h

Figure 14-6634. MMCSD_CTL_CFG_ADMA3_DESC_ADDRESS Name Register

63	62	61	60	59	58	57	
INTG_DESC_ADDR							
R/W							
0h							
56	55	54	53	52	51	50	49
INTG_DESC_ADDR							
R/W							
0h							
48	47	46	45	44	43	42	41
INTG_DESC_ADDR							
R/W							
0h							
40	39	38	37	36	35	34	33
INTG_DESC_ADDR							
R/W							
0h							
16	15	14	13	12	11	10	9
INTG_DESC_ADDR							
R/W							
0h							
8	7	6	5	4	3	2	1
INTG_DESC_ADDR							
R/W							
0h							

Table 14-13445. MMCSD_CTL_CFG_ADMA3_DESC_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:0	INTG_DESC_ADDR	R/W	0h	The start address of Integrated DMA Descriptor is set to this register. Writing to a specific address starts ADMA3 depends on 32-bit/64-bit address-ing. The ADMA3 fetches one Descriptor Address and increments this field to indicate the next Descriptor address. The 32-bit addressing Host Driver uses lower 32- bit of this register and shall program Descriptor Table on 32-bit boundary.ADMA3 ignores lower 2-bit of this register and assumes it to be 00b. Writing to 07Bh starts ADMA3 data transfer. The 64-bit addressing Host Driver uses all 64-bit of this register and shall program Descriptor Table on 64-bit boundary. ADMA3 ignores lower 3-bit of this register and assumes it to be 000b. Writing to 07Fh starts ADMA3 data transfer. Register Value- 00000000_xxxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxxh Addressing Mode - 64-bit System Address Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.76 MMCSD_CTL_CFG_UHS2_BLOCK_SIZE Register

14.7.4.6.2.76.1 MMCSD_CTL_CFG_UHS2_BLOCK_SIZE Register (Offset = 80h) [reset = 0h]

This register is used to configure the number of bytes in a data block

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Table 14-13446. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0080h

Figure 14-6635. MMCSD_CTL_CFG_UHS2_BLOCK_SIZE Name Register

16	15	14	13	12	11	10	9
RESERVED	SDMA_BUF_BOUNDARY			XFER_BLK_SIZE			
NONE	R/W			R/W			
0h	0h			0h			
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
XFER_BLK_SIZE							
R/W							
0h							

Table 14-13447. MMCSD_CTL_CFG_UHS2_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	NONE	0h	Reserved
14:12	SDMA_BUF_BOUNDARY	R/W	0h	When system memory is managed by paging, SDMA data transfer is performed in unit of paging. A page size of sys-tem memory management is set to this field. Host Controller generates the DMA Interrupt at the page boundary and requests the Host Driver to update the ADMA System Address register. SDMA waits until the ADMA System Address register is written. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the UHS-II Transfer Mode register is set to 1. ADMA does not use this field. 7 6 5 4 3 2 1 0
11:0	XFER_BLK_SIZE	R/W	0h	This register specifies the block size of data packet. SD Memory Card uses a fixed block size of 512 bytes. Vari-able block size may be used for SDIO. The maximum value is 2048 Bytes because CRC16 covers up to 2048 bytes. This register is effective when Data Present is set to 1 in UHS-II Command register. 2048 512 2 1 0

14.7.4.6.2.77 MMCSD_CTL_CFG_UHS2_BLOCK_COUNT Register

14.7.4.6.2.77.1 MMCSD_CTL_CFG_UHS2_BLOCK_COUNT Register (Offset = 84h) [reset = 0h]

This register is used to configure the number of data blocks

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Table 14-13448. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0084h

Figure 14-6636. MMCSD_CTL_CFG_UHS2_BLOCK_COUNT Name Register

32	31	30	29	28	27	26	25
XFER_BLK_COUNT							
R/W							
0h							
24	23	22	21	20	19	18	17
XFER_BLK_COUNT							
R/W							
0h							
16	15	14	13	12	11	10	9
XFER_BLK_COUNT							
R/W							
0h							
8	7	6	5	4	3	2	1
XFER_BLK_COUNT							
R/W							
0h							

Table 14-13449. MMCSD_CTL_CFG_UHS2_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	XFER_BLK_COUNT	R/W	0h	This register is effective when Data Present is set to 1 in UHS-II Command register and is enabled when Block Count Enable is set to 1 and Block / Byte Mode is set to 0 in the UHS-II Transfer Mode register. Data transfer stops when the count reaches zero. Setting the block count to 0 results in no data blocks is transferred. This register should be accessed only when no transaction is executing [i.e.,after transactions are stopped]. During data transfer, read operations on this register may return an invalid value and write operations are ignored. 00000000h - Stop Count 00000001h - 1 block 00000002h - 2 blocks .... FFFFFFFFh - 4G blocks -1. 42949 67295 3 2 1 0

14.7.4.6.2.78 MMCSD_CTL_CFG_UHS2_COMMAND_PKT Register

14.7.4.6.2.78.1 MMCSD_CTL_CFG_UHS2_COMMAND_PKT Register (Offset = 88h) [reset = 0h]

UHS-II Command Packet image is set to this register. The maximum length is 20 bytes. The command length varies depends on a Command Packet type. The length is specified by the UHS-II Command register.

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Table 14-13450. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0088h

Figure 14-6637. MMCSD_CTL_CFG_UHS2_COMMAND_PKT Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
CMD_PKT_BYTE							
R/W							
0h							

Table 14-13451. MMCSD_CTL_CFG_UHS2_COMMAND_PKT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CMD_PKT_BYTE	R/W	0h	UHS-II Command Packet image is set to this register.The command length varies depends on a Command Packet type. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.79 MMCSD_CTL_CFG_UHS2_XFER_MODE Register

14.7.4.6.2.79.1 MMCSD_CTL_CFG_UHS2_XFER_MODE Register (Offset = 9Ch) [reset = 0h]

This register is used to control the operations of data transfers

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Table 14-13452. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 009Ch

Figure 14-6638. MMCSD_CTL_CFG_UHS2_XFER_MODE Name Register

16	15	14	13	12	11	10	9
DUPLEX_SELECT	EBSY_WAIT	RESERVED					RESP_INTR_DIS
R/W	R/W	NONE					R/W
0h	0h	0h					0h
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
RESP_ERR_CHK_ENA	RESP_TYPE	BYTE_MODE	DATA_XFER_DIR	RESERVED		BLK_CNT_ENA	DMA_ENA
R/W	R/W	R/W	R/W	NONE		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-13453. MMCSD_CTL_CFG_UHS2_XFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DUPLEX_SELECT	R/W	0h	Use of 2 lane half duplex mode is determined by Host Driver. 1 0
14	EBSY_WAIT	R/W	0h	This bit is set when issuing a command which is accompanied by EBSY packet to indicate end of command execution. Busy is expected for CCMD with R1b/R5b type and DCMD with data transfer.If this bit is set to 1, Host Controller waits receiving of EBSY packet and on receiving EBSY packet, Transfer Com-plete in the Normal Interrupt Status reg-ister is set to 1 to indicate end ofbusy. If an error is indicated in EBSY packet [ex. Memory Error], EBSY Error in the UHS-II Error Interrupt Status register is set to 1. Setting of EBSY Error also sets Error Interrupt to 1 in the Normal Inter-rupt Status register. Error Interrupt and Transfer Complete shall be set together. '1' Wait EBSY, '0' Issue a command without busy. Reset Source: vbus_amod_g_rst_n
13:9	RESERVED	NONE	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0 and waits Command Complete Interrupt and then check the response register. If Host Controller checks response error, sets this bit to 1 and sets Response Error Check Enable to 1. Command Complete Interrupt is disabled by this bit regardless of Com-mand Complete Signal Enable. 1 Disable Response Interrupt 0 Enable Response Interrupt

Table 14-13453. MMCSD_CTL_CFG_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESP_ERR_CHK_ENA	R/W	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver.Only R1 or R5 can be checked. If Host Driver checks response error, this bit is set to 0 and Response Inter-rupt Disable is set to 0. If Host Control-ler checks response error, sets this bit to 1 and sets Response Interrupt Dis-able to 1. Response Type R1 / R5 selects either R1 or R5 response type. If an error is detected, RES Packet Error Interrupt is generated in the UHS-II Error Interrupt Status register. 1 `Enable Response Error Check` 0 `Disable Response Error Check`
6	RESP_TYPE	R/W	0h	When response error check is enabled, this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1 Bit31 OUT_OF_RANGE Bit30 ADDRESS_ERROR Bit29 BLOCK_LEN_ERROR Bit26 WP_VIOLATION Bit25 CARD_IS_LOCKED Bit23 COM_CRC_ERROR Bit21 CARD_ECC_FAILED Bit20 CC_ERROR Bit19 ERROR Response Flags Checked in R5 .Bit07 COM_CRC_ERROR .Bit03 ERROR .Bit01 FUNCTION_NUMBER .Bit00 OUT_OF_RANGE 1 `SDIO` 0 `Memory`
5	BYTE_MODE	R/W	0h	This bit specifies whether data transfer is in byte mode or block mode when Data Present is set to 1. This bit is effective to a command with data trans-fer. 1 0
4	DATA_XFER_DIR	R/W	0h	This bit specifies direction of data trans-fer when Data Present is set to 1. This bit is effective to a command with data transfer. 0 - Read [Card to Host] 1 - Write [Host to Card] 1 `Write from Host to Card` 0 `Read from Card to Host`
3:2	RESERVED	NONE	0h	Reserved
1	BLK_CNT_ENA	R/W	0h	This bit specifies whether data transfer usesUHS-II Block Count register. If this bit is set to 1, data transfer is terminated by Block Count. Setting to UHS-II Block Count register shall be equivalent to TLEN in UHS-II Command Packet reg-ister. 1 `Enable Block count` 0 `Disable Block count`
0	DMA_ENA	R/W	0h	This bit selects whether DMA is used or not and is effective to a command with data transfer. One of DMA types is selected by DMA Select in the Host Control 1 register. 1 `DMA mode is Enabled` 0 `DMA mode is Disabled`

14.7.4.6.2.80 MMCSD_CTL_CFG_UHS2_COMMAND Register

14.7.4.6.2.80.1 MMCSD_CTL_CFG_UHS2_COMMAND Register (Offset = 9Eh) [reset = 0h]

This register is used to program the Command for host controller

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Table 14-13454. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 009Eh

Figure 14-6639. MMCSD_CTL_CFG_UHS2_COMMAND Name Register

16	15	14	13	12	11	10	9
RESERVED			PKT_LENGTH				
NONE			R/W				
0h			0h				
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
CMD_TYPE		DATA_PRESENT	RESERVED		SUB_COMMAND	RESERVED	
R/W		R/W	NONE		R/W	NONE	
0h		0h	0h		0h	0h	

Table 14-13455. MMCSD_CTL_CFG_UHS2_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE	0h	Reserved
12:8	PKT_LENGTH	R/W	0h	A command packet length, which is set in the UHS-II Command Packet register, is set to this register. 00011b - 00000b - 3-0 Bytes [Not used] 00100b - 4 Bytes .... 10100b - 20 Bytes 11111b 10101b Reset Source: vbus_amod_g_rst_n
7:6	CMD_TYPE	R/W	0h	This field is used to distinguish a spe-cific command like abort command. If this field is set to 00b, the UHS-II RES Packet is stored in UHS-II Response register [0B3h-0A0h]. To avoid overwrit-ing the UHS-II Response register, when this filed is set to 01b, the RES Packet [4 bytes length] of TRANS_ABORT CCMD is stored in the Response regis-ter [013h-010h] and when this filed is set to 10b, the RES Packet [8 bytes length] of memory or SDIO abort com-mand [CMD12 or SDIO Abort com-mand] is stored in the Response register [01Fh-018h]. When this filed is set to 11b, Host Controller controls lane to go into dormant state. '00' Normal Command '01' TRANS_ABORT CCMD '10' CMD12 or SDIO Abort Command '11' Go Dormant Command 3 2 1 0
5	DATA_PRESENT	R/W	0h	This bit specifies whether the command is accompanied by data packet. 1 `Data present` 0 `Data not Present`
4:3	RESERVED	NONE	0h	Reserved
2	SUB_COMMAND	R/W	0h	This bit is added from Version 4.10 to distinguish a main command or sub command [Refer to Section 1.17].When issuing a main command, this bit is set to 0 and when issuing a sub com-mand, this bit is set to 1. Setting of this bit is checked by Sub Command Status in the Present State register. 1 `Sub Command` 0 `Main Command`

Table 14-13455. MMCSD_CTL_CFG_UHS2_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.81 MMCSD_CTL_CFG_UHS2_RESPONSE Register

14.7.4.6.2.81.1 MMCSD_CTL_CFG_UHS2_RESPONSE Register (Offset = A0h) [reset = 0h]

This register is used to store received UHS-II RES Packet image

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Table 14-13456. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00A0h

Figure 14-6640. MMCSD_CTL_CFG_UHS2_RESPONSE Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
RESP_PKT_BYTE							
R							
0h							

Table 14-13457. MMCSD_CTL_CFG_UHS2_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESP_PKT_BYTE	R	0h	Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.82 MMCSD_CTL_CFG_UHS2_MESSAGE_SELECT Register

14.7.4.6.2.82.1 MMCSD_CTL_CFG_UHS2_MESSAGE_SELECT Register (Offset = B4h) [reset = 0h]

This register is used to access internal buffer

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Table 14-13458. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00B4h

Figure 14-6641. MMCSD_CTL_CFG_UHS2_MESSAGE_SELECT Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
RESERVED						MSG_SEL	
NONE						R/W	
0h						0h	

Table 14-13459. MMCSD_CTL_CFG_UHS2_MESSAGE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	NONE	0h	Reserved
1:0	MSG_SEL	R/W	0h	Host Controller holds 4 MSG packets in FIFO buffer.One of 4 MSGs can be read from the UHS-II MSG register [0BB-0B8h] by setting this register.[Assumed for debug usage.] '00' The latest MSG '01' One MSG before '10' Two MSGs before '11' Three MSGs before Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.83 MMCSD_CTL_CFG_UHS2_MESSAGE Register

14.7.4.6.2.83.1 MMCSD_CTL_CFG_UHS2_MESSAGE Register (Offset = B8h) [reset = 0h]

This register is used to access internal buffer

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Table 14-13460. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00B8h

Figure 14-6642. MMCSD_CTL_CFG_UHS2_MESSAGE Name Register

32	31	30	29	28	27	26	25
MSG_BYTE3							
R							
0h							
24	23	22	21	20	19	18	17
MSG_BYTE2							
R							
0h							
16	15	14	13	12	11	10	9
MSG_BYTE1							
R							
0h							
8	7	6	5	4	3	2	1
MSG_BYTE0							
R							
0h							

Table 14-13461. MMCSD_CTL_CFG_UHS2_MESSAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSG_BYTE3	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n
23:16	MSG_BYTE2	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n
15:8	MSG_BYTE1	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n
7:0	MSG_BYTE0	R	0h	Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs [length is 4 bytes] can be read fromthis register by setting UHS-II MSG Select register. Usually 2 duplicate MSG packets are sent from/toUHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in theUHS-II MSG Register. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.84 MMCSD_CTL_CFG_UHS2_DEVICE_INTR_STATUS Register

14.7.4.6.2.84.1 MMCSD_CTL_CFG_UHS2_DEVICE_INTR_STATUS Register (Offset = BCh) [reset = 0h]

This register shows receipt of INT MSG from which device

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Table 14-13462. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00BCh

Figure 14-6643. MMCSD_CTL_CFG_UHS2_DEVICE_INTR_STATUS Name Register

16	15	14	13	12	11	10	9
DEV_INT_STS							
R/W1TC							
0h							
8	7	6	5	4	3	2	1
DEV_INT_STS							
R/W1TC							
0h							

Table 14-13463. MMCSD_CTL_CFG_UHS2_DEVICE_INTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DEV_INT_STS	R/W1TC	0h	This register shows receipt of INT MSG from which device and is effective when INT MSG Enable is set to 1 in the UHS- II Device Select register. On receiving INT MSG from a device, Host Controller saves the INT MSG to UHS-II Device Interrupt Code register. A bit of this register, which is corre- spondent to Device ID, is set to 1 and generate Card Interrupt in Normal Interrupt Status register. Writing a bit to 1 clears the status bit [interrupt is treated] and writing a bit to 0 keeps the status value [interrupt is untreated]. If INT MSG Enable is set to 0, this register is cleared to 0 and Host Controller ignores receipt of INT MSG. Effective bit range of this register is determined by Number of Devices Supported in the UHS-II General Capabilities regis-ter. If N devices are supported, bits 1 to N are effective. Then Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. A bit of unsupported Device ID in this register shall be indicated to 0. D00 - Not used [Reserved] D01 - Setting 1 means INT MSG is received from Device ID 1 D02 - Setting 1 means INT MSG is received from Device ID 2 .... D15 - Setting 1 means INT MSG is received from Device ID 15 Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.85 MMCSD_CTL_CFG_UHS2_DEVICE_SELECT Register

14.7.4.6.2.85.1 MMCSD_CTL_CFG_UHS2_DEVICE_SELECT Register (Offset = BEh) [reset = 0h]

UHS-II Device Select Register

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Table 14-13464. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00BEh

Figure 14-6644. MMCSD_CTL_CFG_UHS2_DEVICE_SELECT Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
INT_MSG_ENA	RESERVED			DEV_SEL			
R/W	NONE			R/W			
0h	0h			0h			

Table 14-13465. MMCSD_CTL_CFG_UHS2_DEVICE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MSG_ENA	R/W	0h	This bit enables receipt of INT MSG. If this bit is set to 1,receipt of INT MSG is informed by Card Interrupt in the Nor-mal Interrupt Status register. If this bit is set to 0, Host Con-troller ignores receipt of INT MSG and may not set the UHS-II Device Interrupt Code register. Support of INT MSG Interrupt is optional. If trying to set this bit to 1 but still this bit is read 0, INT MSG Interrupt is not sup-ported by the Host Controller. In this case, UHS-II Device Interrupt Status register always shall be read 0 and UHS-II Device Interrupt Code register may not be implemented. '0' Disabled '1' Enabled Reset Source: vbus_amod_g_rst_n
6:4	RESERVED	NONE	0h	Reserved
3:0	DEV_SEL	R/W	0h	Host Controller holds an INT MSG packet per device. One of INT MSGs [up to 15] can be selected by this field and read from the UHS-II Device Interrupt Code Register [0BFh]. This field is effective when INT MSG Enable is set to 1. The number of devices implemented in the Host Controller is indicated by Number of Devices supported in the UHS-II General Capabilities register. 0h Unselected [Default] 1h INT MSG of Device ID 1 is selected 2h INT MSG of Device ID 2 is selected .... Fh INT MSG of Device ID 15 is selected Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.86 MMCSD_CTL_CFG_UHS2_DEVICE_INT_CODE Register

14.7.4.6.2.86.1 MMCSD_CTL_CFG_UHS2_DEVICE_INT_CODE Register (Offset = BFh) [reset = 0h]

This register is effective when INT MSG Enable is set to 1 in the UHS-II Device Select register.

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Table 14-13466. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00BFh

Figure 14-6645. MMCSD_CTL_CFG_UHS2_DEVICE_INT_CODE Name Register

16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1
DEV_INTR							
R							
0h							

Table 14-13467. MMCSD_CTL_CFG_UHS2_DEVICE_INT_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_INTR	R	0h	This register is effective when INT MSG Enable is set to 1 in the UHS-II Device Select register. Host Controller holds an INT MSG packet per device. One of INT MSGs [Code length is 1 byte] up to 15 can be read from this register by select-ing UHS-II Device Select. The number of the registers to hold INT MSGs is determined by Number of Devices Sup-ported in the UHS-II General Capabili-ties register. Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.87 MMCSD_CTL_CFG_UHS2_SOFTWARE_RESET Register

14.7.4.6.2.87.1 MMCSD_CTL_CFG_UHS2_SOFTWARE_RESET Register (Offset = C0h) [reset = 0h]

UHS-II Software Reset Register

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Table 14-13468. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00C0h

Figure 14-6646. MMCSD_CTL_CFG_UHS2_SOFTWARE_RESET Name Register

16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
RESERVED						HOST_SDTRAN_RESET	HOST_FULL_RESET
NONE						R/W	R/W
0h						0h	0h

Table 14-13469. MMCSD_CTL_CFG_UHS2_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	NONE	0h	Reserved
1	HOST_SDTRAN_RESET	R/W	0h	Host Driver set this bit to 1 to reset SD-TRAN layer when CMD0 is issued to Device or data transfer error occurs. This bit is cleared automatically at completionof SD-TRAN reset. If CMD0 is issued, SD-TRAN Initial- ization sequence from CMD8 is required to use UHS-II mode. Assuming that bus power is maintained and CM-TRAN Initialization is not required. '0' Not Affected '1' Reset SD TRAN Host Controller requires to do followings: [1] SD Clock Enable is maintained.[Continue to provide RCLK]. [2] All setting register is maintained. [3] Internal sequencers are reset to just after power on.be able to issue a command. [4] All Interrupt Status, Status Enable and Signal Enable are cleared. [5] Data transfer is terminated and data in buffer is dis-carded. 1 Reset SDTRAN 0 Not Affected
0	HOST_FULL_RESET	R/W	0h	On issuing FULL_RESET CCMD, Host Driver set this bit to 1 to reset Host Controller. This bit is cleared auto-matically at completion of Host Controller reset. Initial- ization sequence from PHY Initialization is required to use UHS-II mode. Assuming that bus power is maintained. Host Controller requires to do followings: [1] SD Clock Enable is cleared. [Internal Clock is still synchronized]. [2] All setting register is cleared. [3] Internal sequencers are reset to just after power on. [4] All Interrupt Status, Status Enable and Signal Enable are cleared. 1 Reset Host Conroller 0 Not Affected

14.7.4.6.2.88 MMCSD_CTL_CFG_UHS2_TIMER_CONTROL Register

14.7.4.6.2.88.1 MMCSD_CTL_CFG_UHS2_TIMER_CONTROL Register (Offset = C2h) [reset = 0h]

UHS-II Timeout Control Register

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Table 14-13470. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00C2h

Figure 14-6647. MMCSD_CTL_CFG_UHS2_TIMER_CONTROL Name Register

<table>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="4">DEADLOCK_TIMEOUT_CTR</td><td colspan="4">CMDRESP_TIMEOUT_CTR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13471. MMCSD_CTL_CFG_UHS2_TIMER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7:4	DEADLOCK_TIMEOUT_CTR	R/W	0h	This value determines the deadlock period while host expecting to receive a packet [1 second]. Tim-eout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for Deadlock [in the UHS-II Error Interrupt Status Enable register] 1111b Reserved 1110b TMCLK x 2^27 .... 0001b TMCLK x 2^14 0000b TMCLK x 2^13 Reset Source: vbus_amod_g_rst_n
3:0	CMDRESP_TIMEOUT_CTR	R/W	0h	This value determines the interval between com-mand packet and response packet [5ms]. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for CMD_RES [in the UHS-II Error Interrupt Status Enable register] 1111b Reserved 1110b TMCLK x 2^27 .... 0001b TMCLK x 2^14 0000b TMCLK x 2^13 Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.89 MMCSD_CTL_CFG_UHS2_ERR_INTR_STS Register

14.7.4.6.2.89.1 MMCSD_CTL_CFG_UHS2_ERR_INTR_STS Register (Offset = C4h) [reset = 0h]

This register gives the status of all UHS-II interrupts

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Table 14-13472. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00C4h

Figure 14-6648. MMCSD_CTL_CFG_UHS2_ERR_INTR_STS Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="5">VENDOR_SPECFIC_ERR</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W1TC</td><td colspan="3">NONE</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="6">RESERVED</td><td>DEADLOCK_TIMEOUT</td><td>CMD_RESP_TIMEOUT</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td>ADMA2_ADMA3</td><td colspan="6">RESERVED</td><td>EBSY</td></tr>
<tr><td>R/W1TC</td><td colspan="6">NONE</td><td>R/W1TC</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td>UNRECOVERABLE</td><td>RESERVED</td><td>TID</td><td>FRAMING</td><td>CRC</td><td>RETRY_EXPIRED</td><td>RESP_PKT</td><td>HEADER</td></tr>
<tr><td>R/W1TC</td><td>NONE</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13473. MMCSD_CTL_CFG_UHS2_ERR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC_ERR	R/W1TC	0h	Vendor may use this field for vendor specific error status. '0' Interrupt is not generated '1' Vendor Specific Error Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W1TC	0h	Setting of this bit means that deadlock timeout occurs. Host expects to receive a packet but not received in a specified timeout [1 second]. Timeout value is determined by the setting of Timeout Counter Value for Deadlock in UHS-II Timer Control register. 1 `Deadlock Error` 0 `No Error`
16	CMD_RESP_TIMEOUT	R/W1TC	0h	Setting of this bit means that RES Packet timeout occurs. Host expects to receive RES packet but not received in a specified timeout [5ms]. Timeout value is determined by the setting of Timeout Counter Value for CMD_RES in UHS-II Timer Control register. 1 `Resp packet timeout Error` 0 `No Error`
15	ADMA2_ADMA3	R/W1TC	0h	Setting of this bit means that ADMA2/3 Error occurs in UHS-II mode. ADMA2/3 Error Status is indicated to the ADMA Error Status [054h], which is defined in the Host spec 3.00. 1 `ADMA2/3 Error` 0 `No Error`

Table 14-13473. MMCSD_CTL_CFG_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:9	RESERVED	NONE	0h	Reserved
8	EBSY	R/W1TC	0h	On receiving EBSY packet, if the packet indicates an error, this bit is set to 1. Setting of this bit also sets Error Interrupt and Transfer Completer together in the Normal Interrupt Status register. This error check is effective for a command with setting EBSY Wait in the UHS-II Transfer Mode register. 1 `EBSY Error` 0 `No Error`
7	UNRECOVERABLE	R/W1TC	0h	Setting of this bit means that Unrecoverable Error is set in a packet from a device. 1 `Device Unrecoverable Error` 0 `No Error`
6	RESERVED	NONE	0h	Reserved
5	TID	R/W1TC	0h	Setting of this bit means that TID Error occurs. 1 `TID Error` 0 `No Error`
4	FRAMING	R/W1TC	0h	Setting of this bit means that Framing Error occurs during a packet receiving. 1 `Framing Error` 0 `No Error`
3	CRC	R/W1TC	0h	Setting of this bit means that CRC Error occurs during a packet receiving. 1 `CRC Error` 0 `No Error`
2	RETRY_EXPIRED	R/W1TC	0h	Setting of this bit means that Retry Counter Expired Error occurs during data transfer.If this bit is set,either Framing Error or CRC Error in this register shall be set. 1 `Retry Expired Error` 0 `No Error`
1	RESP_PKT	R/W1TC	0h	Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to1 in the UHS- II Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response,this bit is set to 1. 1 `Resp packet Error` 0 `No Error`
0	HEADER	R/W1TC	0h	Setting of this bit means that Header Error occurs in a received packet. 1 `Header Error` 0 `No Error`

14.7.4.6.2.90 MMCSD_CTL_CFG_UHS2_ERR_INTR_STS_ENA Register

14.7.4.6.2.90.1 MMCSD_CTL_CFG_UHS2_ERR_INTR_STS_ENA Register (Offset = C8h) [reset = 0h]

This register is used to enable the UHS-II Error Interrupt Status register fields

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Table 14-13474. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00C8h

Figure 14-6649. MMCSD_CTL_CFG_UHS2_ERR_INTR_STS_ENA Name Register

32	31	30	29	28	27	26	25
VENDOR_SPECFIC					RESERVED		
R/W					NONE		
0h					0h		
24	23	22	21	20	19	18	17
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
NONE						R/W	R/W
0h						0h	0h
16	15	14	13	12	11	10	9
ADMA2_ADMA3	RESERVED						EBSY
R/W	NONE						R/W
0h	0h						0h
8	7	6	5	4	3	2	1
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13475. MMCSD_CTL_CFG_UHS2_ERR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC	R/W	0h	Setting this bit to 1 enables setting of Vendor Specific Error bit in the UHS-II Error Interrupt Status register. 0h - Status is Disabled 1h - Status is Enabled Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved

17	DEADLOCK_TIMEOUT	R/W	0h	Setting this bit to 1 enables setting of Timeout for Dead lock bit in the UHS-II Error Interrupt Status register.
				`1 Status is Enabled`
				`0 Status is Disabled`

16	CMD_RESP_TIMEOUT	R/W	0h	Setting this bit to 1 enables setting of Timeout for CMD_RES bit in the UHS-II Error Interrupt Status register.
				`1 Status is Enabled`
				`0 Status is Disabled`

15	ADMA2_ADMA3	R/W	0h	Setting this bit to 1 enables setting of ADMA2/3 Error bit in the UHS-II Error Interrupt Status register.
				`1 Status is Enabled`
				`0 Status is Disabled`

14:9	RESERVED	NONE	0h	Reserved

Table 14-13475. MMCSD_CTL_CFG_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	EBSY	R/W	0h	Setting this bit to 1 enables setting of EBSY Error bit in the UHS-II Error Interrupt Status register. 1 Status is Enabled 0 Status is Disabled
7	UNRECOVERABLE	R/W	0h	Setting this bit to 1 enables setting of Unrecoverable Error bit in the UHS-II Error Interrupt Status register. 1 Status is Enabled 0 Status is Disabled
6	RESERVED	NONE	0h	Reserved
5	TID	R/W	0h	Setting this bit to 1 enables setting of TID Error bit in the UHS-II Error Interrupt Status register. 1 Status is Enabled 0 Status is Disabled
4	FRAMING	R/W	0h	Setting this bit to 1 enables setting of Framing Error bit in the UHS-II Error Interrupt Status register. 1 Status is Enabled 0 Status is Disabled
3	CRC	R/W	0h	Setting this bit to 1 enables setting of CRC Error bit in the UHS-II Error Interrupt Status register. 1 Status is Enabled 0 Status is Disabled
2	RETRY_EXPIRED	R/W	0h	Setting this bit to 1 enables setting of Retry Expired bit in the UHS-II Error Interrupt Status register. 1 Status is Enabled 0 Status is Disabled
1	RESP_PKT	R/W	0h	Setting this bit to 1 enables setting of RES Packet Error bit in the UHS-II Error Interrupt Status register. 1 Status is Enabled 0 Status is Disabled
0	HEADER	R/W	0h	Setting this bit to 1 enables setting of Header Error bit in the UHS-II Error Interrupt Status Register. 1 Status is Enabled 0 Status is Disabled

14.7.4.6.2.91 MMCSD_CTL_CFG_UHS2_ERR_INTR_SIG_ENA Register

14.7.4.6.2.91.1 MMCSD_CTL_CFG_UHS2_ERR_INTR_SIG_ENA Register (Offset = CCh) [reset = 0h]

This register is used to generate UHS-II Interrupt signals

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Table 14-13476. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00CCh

Figure 14-6650. MMCSD_CTL_CFG_UHS2_ERR_INTR_SIG_ENA Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="5">VENDOR_SPECFIC</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="6">RESERVED</td><td>DEADLOCK_TIMEOUT</td><td>CMD_RESP_TIMEOUT</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td>ADMA2_ADMA3</td><td colspan="6">RESERVED</td><td>EBSY</td></tr>
<tr><td>R/W</td><td colspan="6">NONE</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="6">0h</td><td>0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td>UNRECOVERABLE</td><td>RESERVED</td><td>TID</td><td>FRAMING</td><td>CRC</td><td>RETRY_EXPIRED_SIG_ENA</td><td>RESP_PKT</td><td>HEADER</td></tr>
<tr><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13477. MMCSD_CTL_CFG_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECFIC	R/W	0h	Setting of a bit to 1 in this field enables generating interrupt signal when corre-spondent bit of Vendor Specific Error is set in the UHS-II Error Interrupt Status Register. 0h - Interrupt Signal is Disabled 1h - Interrupt Signal is Enabled Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Timeout for Dead lock bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
16	CMD_RESP_TIMEOUT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Timeout for CMD_RES bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
15	ADMA2_ADMA3	R/W	0h	Setting this bit to 1 enables generating interrupt signal when ADMA2/3 Error bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
14:9	RESERVED	NONE	0h	Reserved

Table 14-13477. MMCSD_CTL_CFG_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	EBSY	R/W	0h	Setting this bit to 1 enables generating interrupt signal when EBSY Error bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
7	UNRECOVERABLE	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Unrecoverable Error bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
6	RESERVED	NONE	0h	Reserved
5	TID	R/W	0h	Setting this bit to 1 enables generating interrupt signal when TID Error bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
4	FRAMING	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Framing Error bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
3	CRC	R/W	0h	Setting this bit to 1 enables generating interrupt signal when CRC Error bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
2	RETRY_EXPIRED_SIG_ENA	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Retry Expired bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
1	RESP_PKT	R/W	0h	Setting this bit to 1 enables generating interrupt signal when RES Packet Error bit is set in the UHS-II Error InterruptStatus Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`
0	HEADER	R/W	0h	Setting this bit to 1 enables generating interrupt signal when Header Error bit is set in the UHS-II Error Interrupt Status Register. 1 `Interrupt Signal is Enabled` 0 `Interrupt Signal is Disabled`

14.7.4.6.2.92 MMCSD_CTL_CFG_UHS2_SETTINGS_PTR Register

14.7.4.6.2.92.1 MMCSD_CTL_CFG_UHS2_SETTINGS_PTR Register (Offset = E0h) [reset = 100h]

This register is pointer for UHS-II settings.

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Table 14-13478. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00E0h

Figure 14-6651. MMCSD_CTL_CFG_UHS2_SETTINGS_PTR Name Register

16	15	14	13	12	11	10	9
UHS2_SETTINGS_PTR							
R							
100h							
8	7	6	5	4	3	2	1
UHS2_SETTINGS_PTR							
R							
100h							

Table 14-13479. MMCSD_CTL_CFG_UHS2_SETTINGS_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_SETTINGS_PTR	R	100h	Pointer for UHS-II Settings Register Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.93 MMCSD_CTL_CFG_UHS2_CAPABILITIES_PTR Register

14.7.4.6.2.93.1 MMCSD_CTL_CFG_UHS2_CAPABILITIES_PTR Register (Offset = E2h) [reset = 110h]

This register is pointer for UHS-II Capabilities Register.

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Table 14-13480. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00E2h

Figure 14-6652. MMCSD_CTL_CFG_UHS2_CAPABILITIES_PTR Name Register

16	15	14	13	12	11	10	9
UHS2_CAPABILITIES_PTR							
R							
110h							
8	7	6	5	4	3	2	1
UHS2_CAPABILITIES_PTR							
R							
110h							

Table 14-13481. MMCSD_CTL_CFG_UHS2_CAPABILITIES_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_CAPABILITIES_PTR	R	110h	Pointer for UHS-II Capabilities Register Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.94 MMCSD_CTL_CFG_UHS2_TEST_PTR Register

14.7.4.6.2.94.1 MMCSD_CTL_CFG_UHS2_TEST_PTR Register (Offset = E4h) [reset = 120h]

This register is pointer for UHS-II Test Register.

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Table 14-13482. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00E4h

Figure 14-6653. MMCSD_CTL_CFG_UHS2_TEST_PTR Name Register

16	15	14	13	12	11	10	9
UHS2_TEST_PTR							
R							
120h							
8	7	6	5	4	3	2	1
UHS2_TEST_PTR							
R							
120h							

Table 14-13483. MMCSD_CTL_CFG_UHS2_TEST_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UHS2_TEST_PTR	R	120h	Pointer for UHS-II Test Register Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.95 MMCSD_CTL_CFG_SHARED_BUS_CTRL_PTR Register

14.7.4.6.2.95.1 MMCSD_CTL_CFG_SHARED_BUS_CTRL_PTR Register (Offset = E6h) [reset = 130h]

This register is pointer for UHS-II Shared Bus Control Register.

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Table 14-13484. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00E6h

Figure 14-6654. MMCSD_CTL_CFG_SHARED_BUS_CTRL_PTR Name Register

16	15	14	13	12	11	10	9
SHARED_BUS_CTRL_PTR							
R							
130h							
8	7	6	5	4	3	2	1
SHARED_BUS_CTRL_PTR							
R							
130h							

Table 14-13485. MMCSD_CTL_CFG_SHARED_BUS_CTRL_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SHARED_BUS_CTRL_PTR	R	130h	Pointer for Shared Bus Control Register Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.96 MMCSD_CTL_CFG_VENDOR_SPECFIC_PTR Register

14.7.4.6.2.96.1 MMCSD_CTL_CFG_VENDOR_SPECFIC_PTR Register (Offset = E8h) [reset = 140h]

This register is pointer for UHS-II Vendor Specific Pointer Register.

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Table 14-13486. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00E8h

Figure 14-6655. MMCSD_CTL_CFG_VENDOR_SPECFIC_PTR Name Register

16	15	14	13	12	11	10	9
VENDOR_SPECFIC_PTR							
R							
140h							
8	7	6	5	4	3	2	1
VENDOR_SPECFIC_PTR							
R							
140h							

Table 14-13487. MMCSD_CTL_CFG_VENDOR_SPECFIC_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	VENDOR_SPECFIC_PTR	R	140h	Pointer for Vendor Specific Area Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.97 MMCSD_CTL_CFG_BOOT_TIMEOUT_CONTROL Register

14.7.4.6.2.97.1 MMCSD_CTL_CFG_BOOT_TIMEOUT_CONTROL Register (Offset = F4h) [reset = 0h]

This is used to program the boot timeout value counter

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Table 14-13488. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00F4h

Figure 14-6656. MMCSD_CTL_CFG_BOOT_TIMEOUT_CONTROL Name Register

32	31	30	29	28	27	26	25
DATA_TIMEOUT_CNT							
R/W							
0h							
24	23	22	21	20	19	18	17
DATA_TIMEOUT_CNT							
R/W							
0h							
16	15	14	13	12	11	10	9
DATA_TIMEOUT_CNT							
R/W							
0h							
8	7	6	5	4	3	2	1
DATA_TIMEOUT_CNT							
R/W							
0h							

Table 14-13489. MMCSD_CTL_CFG_BOOT_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_TIMEOUT_CNT	R/W	0h	This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC4.4 card.The value is in number of sd clock. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.98 MMCSD_CTL_CFG_VENDOR_REGISTER Register

14.7.4.6.2.98.1 MMCSD_CTL_CFG_VENDOR_REGISTER Register (Offset = F8h) [reset = 4E20h]

Vendor register added for autogate sdclk, cmd11 power down timer, enhancedstrobe and eMMC hardware reset

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Table 14-13490. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00F8h

Figure 14-6657. MMCSD_CTL_CFG_VENDOR_REGISTER Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">91AE40F5610h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="7">RESERVED</td><td>AUTOGATE_SDCLK</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">91AE40F5610h</td><td>0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">CMD11_PD_TIMER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1388h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="6">CMD11_PD_TIMER</td><td>EMMC_HW_RESET</td><td>ENHANCED_STROBE</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">1388h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13491. MMCSD_CTL_CFG_VENDOR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	91AE40F5610h	Reserved
16	AUTOGATE_SDCLK	R/W	0h	If this bit is set, SD CLK will be gated automatically when there is no transfer. This is applicable only for Embedded Device 1 `Autogating of sdclk is Enabled` 0 `Autogating of sdclk is Disabled`
15:2	CMD11_PD_TIMER	R/W	1388h	cmd11 power-down timer value Reset Source: vbus_amod_g_rst_n
1	EMMC_HW_RESET	R/W	0h	Hardware reset signal is generared for eMMC card when this bit is set 1 `Drives the hardware reset pin as ZERO (Active LOW to eMMC card)` 0 `Deassert the hardware reset pin`
0	ENHANCED_STROBE	R/W	0h	This bit enables the enhanced strobe logic of the Host Controller 1 `Enhanced strobe is Enabled` 0 `Enhanced strobe is Disabled`

14.7.4.6.2.99 MMCSD_CTL_CFG_SLOT_INT_STS Register

14.7.4.6.2.99.1 MMCSD_CTL_CFG_SLOT_INT_STS Register (Offset = FCh) [reset = 0h]

This register is used to read the interrupt signal for each slot.

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Table 14-13492. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00FCh

Figure 14-6658. MMCSD_CTL_CFG_SLOT_INT_STS Name Register

<table>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">INTR_SIG</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13493. MMCSD_CTL_CFG_SLOT_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	NONE	0h	Reserved
7:0	INTR_SIG	R	0h	These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.100 MMCSD_CTL_CFG_HOST_CONTROLLER_VER Register

14.7.4.6.2.100.1 MMCSD_CTL_CFG_HOST_CONTROLLER_VER Register (Offset = FEh) [reset = 1004h]

This register is used to read the vendor version number and specification version number

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Table 14-13494. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 00FEh

Figure 14-6659. MMCSD_CTL_CFG_HOST_CONTROLLER_VER Name Register

<table>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">VEN_VER_NUM</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">10h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">SPEC_VER_NUM</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-13495. MMCSD_CTL_CFG_HOST_CONTROLLER_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	VEN_VER_NUM	R	10h	The Vendor Version Number is set to 0x10 [1.0] Reset Source: vbus_amod_g_rst_n
7:0	SPEC_VER_NUM	R	4h	This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. 00h - SD Host Controller Specification Version 1.00 01h - SD Host Controller Specification Version 2.00 Including the feature of the ADMA and Test Register 02h - SD Host Controller Specification Version 3.00 03h - SD Host Controller Specification Version 4.00 04h - SD Host Controller Specification Version 4.10 'others' Reserved 4 3 2 1 0

14.7.4.6.2.101 MMCSD_CTL_CFG_UHS2_GEN_SETTINGS Register

14.7.4.6.2.101.1 MMCSD_CTL_CFG_UHS2_GEN_SETTINGS Register (Offset = 100h) [reset = 0h]

Start Address of General settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-13496. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0100h

Figure 14-6660. MMCSD_CTL_CFG_UHS2_GEN_SETTINGS Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED		NUMLANES					
NONE		R/W					
0h		0h					
8	7	6	5	4	3	2	1
RESERVED							POWER_MODE
NONE							R/W
0h							0h

Table 14-13497. MMCSD_CTL_CFG_UHS2_GEN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	NUMLANES	R/W	0h	The lane configuration of a Host System is set to this field depends on the capability among Host Controller and connected devices. 2 Lanes FD mode is mandatory and the others modes are optional. 0000b - 2 Lanes FD or 2L-HD 0001b - Not Used 0010b - 3 Lanes 2D1U-FD [Embedded] 0011b - 3 Lanes 1D2U-FD [Embedded] 0100b - 4 Lanes 2D2U-FD [Embedded] others - Reserved Reset Source: vbus_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved
0	POWER_MODE	R/W	0h	This field determines either Fast mode or Low Power mode.Host and all devices connected to the host shall be set to the same mode. 1 Low power mode 0 Fast mode

14.7.4.6.2.102 MMCSD_CTL_CFG_UHS2_PHY_SETTINGS Register

14.7.4.6.2.102.1 MMCSD_CTL_CFG_UHS2_PHY_SETTINGS Register (Offset = 104h) [reset = 0h]

Start Address of PHY settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-13498. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0104h

Figure 14-6661. MMCSD_CTL_CFG_UHS2_PHY_SETTINGS Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
N_LSS_DIR				N_LSS_SYN			
R/W				R/W			
0h				0h			
16	15	14	13	12	11	10	9
HIBERNATE_ENA	RESERVED						
R/W	NONE						
0h	0h						
8	7	6	5	4	3	2	1
SPEED_RANGE		RESERVED					
R/W		NONE					
0h		0h					

Table 14-13499. MMCSD_CTL_CFG_UHS2_PHY_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:20	N_LSS_DIR	R/W	0h	The largest value of N_LSS_DIR capabilities among the Host Controller and Connected Devices is set to this field. 0h - 8 x16 LSS 1h - 8 x 1 LSS 2h - 8 x 2 LSS 3h - 8 x 3 LSS .... Fh - 8 x 15 LSS Reset Source: vbus_amod_g_rst_n
19:16	N_LSS_SYN	R/W	0h	The largest value of N_LSS_SYN capabilities among the Host Controller and Connected Devices is set to this field. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n
15	HIBERNATE_ENA	R/W	0h	After checking card capability of Hibernate mode, if all devices support Hibernate mode, this bit may be set. This bit determines whether Host remains in Dormant state or goes to Hibernate state. In Hibernate mode, VDD1 Power may be off. 1 `Hibernate Enabled` 0 `Hibernate Disabled`
14:8	RESERVED	NONE	0h	Reserved

Table 14-13499. MMCSD_CTL_CFG_UHS2_PHY_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	SPEED_RANGE	R/W	0h	PLL multiplier is selected by this field.Change of PLL Multiplier is not effective immediately and is applied from exiting Dormant State. '00' Range A [Default] '01' Range B '10' Reserved '11' Reserved 3 Reserved 2 Reserved 1 Range B 0 Range A (Default)
5:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.103 MMCSD_CTL_CFG_UHS2_LNK_TRN_SETTINGS Register

14.7.4.6.2.103.1 MMCSD_CTL_CFG_UHS2_LNK_TRN_SETTINGS Register (Offset = 108h) [reset = 0h]

Start Address of LINK/TRAN settings is pointed by Pointer for UHS-II Setting Register.

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Table 14-13500. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0108h

Figure 14-6662. MMCSD_CTL_CFG_UHS2_LNK_TRN_SETTINGS Name Register

63	62	61	60	59	58	57	
RESERVED							
NONE							
0h							
56	55	54	53	52	51	50	49
RESERVED							
NONE							
0h							
48	47	46	45	44	43	42	41
RESERVED							
NONE							
0h							
40	39	38	37	36	35	34	33
N_DATA_GAP							
R/W							
0h							
16	15	14	13	12	11	10	9
HOST_NFCU							
R/W							
0h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
0h							

Table 14-13501. MMCSD_CTL_CFG_UHS2_LNK_TRN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	0h	Reserved
39:32	N_DATA_GAP	R/W	0h	The largest value of N_DATA_GAP capabilities among the Host Controller and Connected Devices is set to this field. 00h - No Gap 01h - 1 LSS 02h - 2 LSS 03h - 3 LSS .... FFh - 255 LSS 255 3 2 1 0
31:18	RESERVED	NONE	0h	Reserved

Table 14-13501. MMCSD_CTL_CFG_UHS2_LNK_TRN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	RETRY_COUNT	R/W	0h	Data Burst retry count is set to this field. '00' Retry Disabled '01' 1 time '10' 2 times '11' 3 times 3 Retry 3times 2 Retry 2times 1 Retry 1time 0 Retry Disabled
15:8	HOST_NFCU	R/W	0h	Host Driver sets the number of blocks in Data Burst [Flow Control] to this field.The value shall be smaller than or equal to N_FCU capabilities among the Host Controller and connected card and devices. Setting 1 to 4 blocks is recommended considering buffer size. 00h - 256 Blocks 01h - 1 Block 02h - 2 Blocks 03h - 3 Blocks .... FFh - 255 Blocks 255 3 2 1 0
7:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.104 MMCSD_CTL_CFG_UHS2_GEN_CAP Register

14.7.4.6.2.104.1 MMCSD_CTL_CFG_UHS2_GEN_CAP Register (Offset = 110h) [reset = 44F11h]

Start Address of General Capabilities is pointed by Pointer for UHS-II Host Capabilities Register.

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Table 14-13502. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0110h

Figure 14-6663. MMCSD_CTL_CFG_UHS2_GEN_CAP Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
3E8h							
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
CORECFG_UHS2_BUS_TOPLOGY		CORECFG_UHS2_MAX_DEVICES				DEVICE_TYPE	
R		R				R	
0h		1h				0h	
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
RESERVED	CFG_64BIT_ADDRESSING	NUM_LANES					
NONE	R	R					
0h	1h	fh					
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
GAP				DAP			
R				R			
1h				1h			

Table 14-13503. MMCSD_CTL_CFG_UHS2_GEN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	3E8h	Reserved
23:22	CORECFG_UHS2_BUS_TOPLOGY	R	0h	This field indicates one of bus topologies configured by a Host system. '00' P2P Connection '01' Ring Connection '10' HUB Connection '11' HUB is connected in Ring 3 HUB is connected in Ring 2 HUB Connection 1 Ring Connection 0 P2P Connection
21:18	CORECFG_UHS2_MAX_DEVICES	R	1h	This field indicates the maximum number of devices supported by the Host Controller. 0h - Not used 1h - 1 Devices 2h - 2 Devices .... Fh - 15 Devices 15 15 Devices 2 2 Devices 1 1 Device 0 Not used
17:16	DEVICE_TYPE	R	0h	This field indicates device type configured by a Host system. '00' Removable Card[P2P] '01' Embedded Devices '10' Embedded Devices+Removable Card '11' Reserved Reset Source: vbus_amod_g_rst_n
15	RESERVED	NONE	0h	Reserved

Table 14-13503. MMCSD_CTL_CFG_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	CFG_64BIT_ADDRESSING	R	1h	This field indicates support of 64-bit addressing by the Host Controller. '0' 32-bit Addressing is supported '1' 32-bit and 64-bit Addressing is supported Reset Source: vbus_amod_g_rst_n
13:8	NUM_LANES	R	fh	This field indicates support of lanes by the Host Controller.0 mean not supported and 1 means supported. D08 - 2L-HD D09 - 2D1U-FD D10 - 1D2U-FD D11 - 2D2U-FD D12 - Reserved D13 - Reserved Reset Source: vbus_amod_g_rst_n
7:4	GAP	R	1h	This field indicates the maximum capability of host power supply for a group configured by a Host system.This field is used to set the argument of DEVICE_INIT CCMD 0h -Not used 1h - 360 mW 2h - 720 mW .... Fh - 360x15 mW Reset Source: vbus_amod_g_rst_n
3:0	DAP	R	1h	This field indicates the maximum capability of host power supply for a device configured by a Host system.This field is used to set the argument of DEVICE_INIT CCMD 0h -360 mW [Default] 1h - 360 mW 2h - 720 mW .... Fh - 360 x15 mW Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.105 MMCSD_CTL_CFG_UHS2_PHY_CAP Register

14.7.4.6.2.105.1 MMCSD_CTL_CFG_UHS2_PHY_CAP Register (Offset = 114h) [reset = 110000h]

Start Address of PHY Capabilities is pointed by Pointer for UHS-II Host Capabilities Register.

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Table 14-13504. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0114h

Figure 14-6664. MMCSD_CTL_CFG_UHS2_PHY_CAP Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
N_LSS_DIR				N_LSS_SYN			
R				R			
1h				1h			
16	15	14	13	12	11	10	9
RESERVED							
NONE							
3E8h							
8	7	6	5	4	3	2	1
SPEED_RANGE		RESERVED					
R		NONE					
0h		0h					

Table 14-13505. MMCSD_CTL_CFG_UHS2_PHY_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:20	N_LSS_DIR	R	1h	This field indicates the minimum N_LSS_DIR required by the Host Controller. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n
19:16	N_LSS_SYN	R	1h	This field indicates the minimum N_LSS_SYN required by the Host Controller. 0h - 4 x16 LSS 1h - 4 x 1 LSS 2h - 4 x 2 LSS 3h - 4 x 3 LSS .... Fh - 4 x 15 LSS Reset Source: vbus_amod_g_rst_n
15:8	RESERVED	NONE	3E8h	Reserved
7:6	SPEED_RANGE	R	0h	This field indicates supported Speed Range by the Host Controller '00' Range A [Default] '01' Range A and Range B '10' Reserved '11' Reserved 3 Reserved 2 Reserved 1 Range A and Range B 0 Range A (Default)
5:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.106 MMCSD_CTL_CFG_UHS2_LNK_TRN_CAP Register

14.7.4.6.2.106.1 MMCSD_CTL_CFG_UHS2_LNK_TRN_CAP Register (Offset = 118h) [reset = 8120000100h]

Start Address of LINK/TRAN settings is pointed by Pointer for UHS-II Capabilities Register.

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Table 14-13506. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0118h

Figure 14-6665. MMCSD_CTL_CFG_UHS2_LNK_TRN_CAP Name Register

63	62	61	60	59	58	57	
RESERVED							
NONE							
989680h							
56	55	54	53	52	51	50	49
RESERVED							
NONE							
989680h							
48	47	46	45	44	43	42	41
RESERVED							
NONE							
989680h							
40	39	38	37	36	35	34	33
N_DATA_GAP							
R							
81h							
16	15	14	13	12	11	10	9
N_FCU							
R							
1h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
0h							

Table 14-13507. MMCSD_CTL_CFG_UHS2_LNK_TRN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63:40	RESERVED	NONE	989680h	Reserved
39:32	N_DATA_GAP	R	81h	This field indicates the minimum number of data gap[DIDL] supported by the Host Controller. 00h - No Gap 01h - 1 LSS 02h - 2 LSS 03h - 3 LSS .... FFh - 255 LSS 255 3 2 1 0
31:20	MAX_BLK_LENGTH	R	200h	This field indicates maximum block length by the Host Controller. 000h - Not Used 001h - 1 byte 002h - 2 bytes .... 200h - 512 bytes .... 800h - 2048 bytes 801h-FFFh -Not Used Reset Source: vbus_amod_g_rst_n
19:16	RESERVED	NONE	0h	Reserved

Table 14-13507. MMCSD_CTL_CFG_UHS2_LNK_TRN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	N_FCU	R	1h	This field indicates maximum the number of blocks in a Flow Control unit by the Host Controller.This value is determined by supported buffer size. 00h - 256 Blocks 01h - 1 Block 02h - 2 Block 03h - 3 Block .... FFh - 255 Blocks 255 3 2 1 0
7:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.107 MMCSD_CTL_CFG_FORCE_UHSII_ERR_INT_STS Register

14.7.4.6.2.107.1 MMCSD_CTL_CFG_FORCE_UHSII_ERR_INT_STS Register (Offset = 120h) [reset = 0h]

This register is not physically implemented, rather it is an address where UHS-II Error Interrupt Status register can be written.

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Table 14-13508. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0120h

Figure 14-6666. MMCSD_CTL_CFG_FORCE_UHSII_ERR_INT_STS Name Register

32	31	30	29	28	27	26	25
VENDOR_SPECIFIC					RESERVED		
W					NONE		
0h					0h		
24	23	22	21	20	19	18	17
RESERVED						TIMEOUT_DEADLOCK	TIMEOUT_CMD_RES
NONE						W	W
0h						0h	0h
16	15	14	13	12	11	10	9
ADMA	RESERVED						EBSY
W	NONE						W
0h	0h						0h
8	7	6	5	4	3	2	1
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RES_PKT	HEADER
W	NONE	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13509. MMCSD_CTL_CFG_FORCE_UHSII_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	VENDOR_SPECIFIC	W	0h	Force Event for Vendor Specific Error 0h - Not Affected 1h - Vendor Specific Error Status is set Reset Source: vbus_amod_g_rst_n
26:18	RESERVED	NONE	0h	Reserved

17	TIMEOUT_DEADLOCK	W	0h	Setting this bit forces the Host Controller to set Timeout for Deadlock in the UHS-II Error Interrupt Status register.
				`1 Timeout for Deadlock Error status is set`
				`0 No Interrupt`

16	TIMEOUT_CMD_RES	W	0h	Setting this bit forces the Host Controller to set Timeout for CMD_RES in the UHS-II Error Interrupt Status register.
				`1 Timout for CMD_RES Status is set`
				`0 No Interrupt`

15	ADMA	W	0h	Setting this bit forces the Host Controller to set ADMA Error in the UHS-II Error Interrupt Status register.
				`1 ADMA error status is set`
				`0 No Interrupt`

14:9	RESERVED	NONE	0h	Reserved

Table 14-13509. MMCSD_CTL_CFG_FORCE_UHSII_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	EBSY	W	0h	Setting this bit forces the Host Controller to set EBSY Error in the UHS-II Error Interrupt Status register. 1 `EBSY error status is set` 0 `No Interrupt`
7	UNRECOVERABLE	W	0h	Setting this bit forces the Host Controller to set Unrecover-able Error in the UHS-II Error Interrupt Status register. 1 `Unrecoverable error status is set` 0 `No Interrupt`
6	RESERVED	NONE	0h	Reserved
5	TID	W	0h	Setting this bit forces the Host Controller to set TID Error in the UHS-II Error Interrupt Status register. 1 `TID error status is set` 0 `No Interrupt`
4	FRAMING	W	0h	Setting this bit forces the Host Controller to set Framing Error in the UHS-II Error Interrupt Status register. 1 `Framing error status is set` 0 `No Interrupt`
3	CRC	W	0h	Setting this bit forces the Host Controller to set CRC Error in the UHS-II Error Interrupt Status register. 1 `CRC error status is set` 0 `No Interrupt`
2	RETRY_EXPIRED	W	0h	Setting this bit forces the Host Controller to set Retry Expired in the UHS-II Error Interrupt Status register. 1 `Retry expired error status is set` 0 `No Interrupt`
1	RES_PKT	W	0h	Setting this bit forces the Host Controller to set RES Packet Error in the UHS-II Error Interrupt Status register. 1 `RES packet error status is set` 0 `No Interrupt`
0	HEADER	W	0h	Setting this bit forces the Host Controller to set Header Error in the UHS-II Error Interrupt Status register. 1 `Header error status is set` 0 `No Interrupt`

14.7.4.6.2.108 MMCSD_CTL_CFG_CQ_VERSION Register

14.7.4.6.2.108.1 MMCSD_CTL_CFG_CQ_VERSION Register (Offset = 200h) [reset = 510h]

This register provides information about the version of the eMMC CQ standard which is 285 implemented by the CQE, in BCD format. The current version is rev 5.1 The following table describes the CQBASE+00h: CQVReservedER Command Queueing Version.

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Table 14-13510. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0200h

Figure 14-6667. MMCSD_CTL_CFG_CQ_VERSION Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
3C336468h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
3C336468h							
16	15	14	13	12	11	10	9
RESERVED				EMMC_MAJOR_VER_NUM			
NONE				R			
3C336468h				5h			
8	7	6	5	4	3	2	1
EMMC_MINOR_VER_NUM				EMMC_VERSION_SUFFIX			
R				R			
1h				0h			

Table 14-13511. MMCSD_CTL_CFG_CQ_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	3C336468h	Reserved
11:8	EMMC_MAJOR_VER_NUM	R	5h	eMMC Major Version Number [digit left of decimal point],in BCD format Reset Source: vbus_amod_g_rst_n
7:4	EMMC_MINOR_VER_NUM	R	1h	eMMC Minor Version Number [digit right of decimal point], in BCD format Reset Source: vbus_amod_g_rst_n
3:0	EMMC_VERSION_SUFFIX	R	0h	eMMC Version Suffix [2nd digit right of decimal point], in BCD format Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.109 MMCSD_CTL_CFG_CQ_CAPABILITIES Register

14.7.4.6.2.109.1 MMCSD_CTL_CFG_CQ_CAPABILITIES Register (Offset = 204h) [reset = 30C8h]

This register is reserved for capability indication.

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Table 14-13512. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0204h

Figure 14-6668. MMCSD_CTL_CFG_CQ_CAPABILITIES Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
1001D2CC144h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
1001D2CC144h							
16	15	14	13	12	11	10	9
CF_MUL				RESERVED		CF_VAL	
R				NONE		R	
3h				0h		c8h	
8	7	6	5	4	3	2	1
CF_VAL							
R							
c8h							

Table 14-13513. MMCSD_CTL_CFG_CQ_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	1001D2CC144h	Reserved
15:12	CF_MUL	R	3h	Internal Timer Clock Frequency Multiplier [ITCFMUL] ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for deter-mining the SQS polling period. See ITCFVAL definition for details. Field Value Description: 0h = 0.001 MHz 1h = 0.01 MHz 2h = 0.1 MHz 3h = 1 MHz 4h = 10 MHz Other values are reserved 4 3
11:10	RESERVED	NONE	0h	Reserved
9:0	CF_VAL	R	c8h	Internal Timer Clock Frequency Value [ITCFVAL] TCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for deter-mining the polling period when using periodic SEND_QUEUE_ STATUS [CMD13] polling. The clock frequency is calculated as ITCFVAL*ITCFMUL. For example, to encode 19.2 MHz ITCFVAL shall be C0h [= 192 decimal] and ITCFMUL shall be 2h [0.1 MHz 192 * 0.1 MHz 19.2 MHz] Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.110 MMCSD_CTL_CFG_CQ_CONFIG Register

14.7.4.6.2.110.1 MMCSD_CTL_CFG_CQ_CONFIG Register (Offset = 208h) [reset = 0h]

This register controls CQE behavior affecting the general operation of command queueing 290 module or operation of multiple tasks in the same time.

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Table 14-13514. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0208h

Figure 14-6669. MMCSD_CTL_CFG_CQ_CONFIG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
RESERVED							
NONE							
0h							
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
RESERVED			DCMD_ENA	RESERVED			TASK_DESC_SIZE
NONE			R/W	NONE			R/W
0h			0h	0h			0h
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
RESERVED							CQ_ENABLE
NONE							R/W
0h							0h

Table 14-13515. MMCSD_CTL_CFG_CQ_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	DCMD_ENA	R/W	0h	Direct Command [DCMD] Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 1 = Task descriptor in slot #31 is a DCMD Task Descrip-tor 0 = Task descriptor in slot #31 is a Data Transfer Task Descriptor 1 0
11:9	RESERVED	NONE	0h	Reserved
8	TASK_DESC_SIZE	R/W	0h	Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. This bit can only be configured when Command Queueing Enable bit is 0 [command queueing is disabled] Bit Value Description 1 = Task descriptor size is 128 bits 0 = Task descriptor size is 64 bits 1 0
7:1	RESERVED	NONE	0h	Reserved

Table 14-13515. MMCSD_CTL_CFG_CQ_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CQ_ENABLE	R/W	0h	Command Queueing Enable Software shall write 1 this bit when in order to enable command queueing mode [i.e. enable CQE]. When this bit is 0, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes 1 to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queueing mode,it shall clear all previous tasks if such exist before setting this bit to 0. 1 Command Queueing mode is Enabled 0 Command Queueing mode is Disabled

14.7.4.6.2.111 MMCSD_CTL_CFG_CQ_CONTROL Register

14.7.4.6.2.111.1 MMCSD_CTL_CFG_CQ_CONTROL Register (Offset = 20Ch) [reset = 0h]

This register controls CQE behavior affecting the general operation of command queueing 293 module or operation of multiple tasks in the same time.

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Table 14-13516. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 020Ch

Figure 14-6670. MMCSD_CTL_CFG_CQ_CONTROL Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							CLEAR_ALL_TASKS
NONE							R/W
0h							0h
8	7	6	5	4	3	2	1
RESERVED							HALT_BIT
NONE							R/W
0h							0h

Table 14-13517. MMCSD_CTL_CFG_CQ_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CLEAR_ALL_TASKS	R/W	0h	Clear All Tasks Software shall write 1 this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state [i.e.Halt bit is 1]. When software writes 1, the value of the register is updated to 1, and CQE shall reset CQTDBR register and all other context information for all unfinished tasks. Then CQE will clear this bit.Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is softwares responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0 to this register shall have no effect. Reset Source: vbus_amod_g_rst_n
7:1	RESERVED	NONE	0h	Reserved

Table 14-13517. MMCSD_CTL_CFG_CQ_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_BIT	R/W	0h	Halt Host software shall write 1 to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command [CMDQ_TASK_MGMT] When software writes 1, CQE shall complete the ongo-ing task if such a task is in progress. Once the task is completed and CQE is in idle state,CQE shall not issue new commands and shall indicate so to software by setting this bit to 1. Software may poll on this bit until it is set to 1, and may only then send commands on the eMMC bus. In order to exit halt state [i.e. resume CQE activity], soft-ware shall clear this bit [write 0]. Writing 0 when thevalue is already 0 shall have no effect. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.112 MMCSD_CTL_CFG_CQ_INTR_STS Register

14.7.4.6.2.112.1 MMCSD_CTL_CFG_CQ_INTR_STS Register (Offset = 210h) [reset = 0h]

This register indicates pending interrupts that require service. Each bit in this registers is asserted 296 in response a specific event, only if the respective bit is set in CQ ISTE register.

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Table 14-13518. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0210h

Figure 14-6671. MMCSD_CTL_CFG_CQ_INTR_STS Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-13519. MMCSD_CTL_CFG_CQ_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

4	TASK_ERROR	R/W1TC	0h	Task Error Interrupt [TERR] This bit is asserted when task error is detected due to invalid task descriptor
				`1 Task Error interrupt is generated`
				`0 No Interrupt`

3	TASK_CLEARED	R/W1TC	0h	Task Cleared [TCL] This status bit is asserted [if CQISTE.TCL=1] when a task clear operation is completed by CQE. The com-pleted task clear operation is either an individual task clear [CQTCLR] or clearing of all tasks [CQCTL].
				`1 Task clear interrupt is generated`
				`0 No Interrupt`

2	RESP_ERR_DET	R/W1TC	0h	Response Error Detected Interrupt [RED] This status bit is asserted [if CQISTE.RED=1] when a response is received with an error bit set in the device status field. The contents of the device status field are listed in Section 6.13.Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked. Reset Source: vbus_amod_g_rst_n

Table 14-13519. MMCSD_CTL_CFG_CQ_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TASK_COMPLETE	R/W1TC	0h	Task Complete Interrupt [TCC] This status bit is asserted [if CQISTE.TCC=1] when atleast one of the following two conditions are met: [1] A task is completed and the INT bit is set in its Task Descriptor [2] Interrupt caused by Interrupt Coalescing logic [see Section C.4.9] 1 `Task complete interrupt is generated` 0 `No Interrupt`
0	HALT_COMPLETE	R/W1TC	0h	Halt Complete Interrupt [HAC] This status bit is asserted [if CQISTE.HAC=1] when halt bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state. 1 `Halt complete interrupt is generated` 0 `No Interrupt`

14.7.4.6.2.113 MMCSD_CTL_CFG_CQ_INTR_STS_ENA Register

14.7.4.6.2.113.1 MMCSD_CTL_CFG_CQ_INTR_STS_ENA Register (Offset = 214h) [reset = 0h]

This register enables and disables the reporting of the corresponding interrupt to host soft-ware in 299 CQIS register. When a bit is set (1) and the corresponding interrupt c -ondition is active, then the 300 bit is CQIS is asserted. Interrupt sources that are disabled (0) are not indicated in the CQIS 301 register. This register is bit-index matched to CQIS register.

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Table 14-13520. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0214h

Figure 14-6672. MMCSD_CTL_CFG_CQ_INTR_STS_ENA Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-13521. MMCSD_CTL_CFG_CQ_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Status Enable 1 = CQIS.TERR will be set when its interrupt condition is active 0 = CQIS.TERR is disabled 1 0
3	TASK_CLEARED	R/W	0h	Task Cleared Status Enable [TCL] 1 = CQIS.TCL will be set when its interrupt condition is active 0 = CQIS.TCL is disabled 1 0
2	RESP_ERR_DET	R/W	0h	Response Error Detected Status Enable [RED] 1 = CQIS.RED will be set when its interrupt condition is active 0 = CQIS.RED is disabled 1 0
1	TASK_COMPLETE	R/W	0h	Task Complete Status Enable [TCC] 1 = CQIS.TCC will be set when its interrupt condition is active 0 = CQIS.TCC is disabled 1 0

Table 14-13521. MMCSD_CTL_CFG_CQ_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_COMPLETE	R/W	0h	Halt Complete Status Enable [HAC] 1 = CQIS.HAC will be set when its interrupt condition is active 0 = CQIS.HAC is disabled 1 0

14.7.4.6.2.114 MMCSD_CTL_CFG_CQ_INTR_SIG_ENA Register

14.7.4.6.2.114.1 MMCSD_CTL_CFG_CQ_INTR_SIG_ENA Register (Offset = 218h) [reset = 0h]

This register enables and disables the generation of interrupts to host software. When a bit is set 304 (1) and the corresponding bit in CQIS is set, then an interrupt is gene -rated. Interrupt sources 305 that are disabled (0) are still indicated in the CQIS register. This register is bit-index matched 306 to CQIS register.

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Table 14-13522. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0218h

Figure 14-6673. MMCSD_CTL_CFG_CQ_INTR_SIG_ENA Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-13523. MMCSD_CTL_CFG_CQ_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Signal Enable [TERR] When set and CQIS.TERR is asserted, the CQE shall generate an interrupt 1 0
3	TASK_CLEARED	R/W	0h	Task Cleared Signal Enable [TCL] When set and CQIS.TCL is asserted, the CQE shall generate an interrupt 1 0
2	RESP_ERR_DET	R/W	0h	Response Error Detected Signal Enable [TCC] When set and CQIS.RED is asserted, the CQE shall generate an interrupt 1 0
1	TASK_COMPLETE	R/W	0h	Task Complete Signal Enable [TCC] When set and CQIS.TCC is asserted, the CQE shall generate an interrupt 1 0

Table 14-13523. MMCSD_CTL_CFG_CQ_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_COMPLETE	R/W	0h	Halt Complete Signal Enable [HAC] When set and CQIS.HAC is asserted, the CQE shall generate an interrupt 1 0

14.7.4.6.2.115 MMCSD_CTL_CFG_CQ_INTR_COALESCING Register

14.7.4.6.2.115.1 MMCSD_CTL_CFG_CQ_INTR_COALESCING Register (Offset = 21Ch) [reset = 0h]

This register controls the interrupt coalescing feature.

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Table 14-13524. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 021Ch

Figure 14-6674. MMCSD_CTL_CFG_CQ_INTR_COALESCING Name Register

32	31	30	29	28	27	26	25
CQINTCOALESC_ENABLE	RESERVED						
R/W	NONE						
0h	0h						
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
RESERVED			IC_STATUS	RESERVED			
NONE			R	NONE			
0h			0h	0h			
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
RESERVED			CTR_THRESHOLD				
NONE			R/W				
0h			0h				
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
RESERVED	TIMEOUT_VAL						
NONE	R/W						
0h	0h						

Table 14-13525. MMCSD_CTL_CFG_CQ_INTR_COALESCING Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CQINTCOALESC_ENABLE	R/W	0h	When set to 0 by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT=1 in the Task Descriptor. When set to 1, the interrupt coalescing mechanism is enabled and coalesced interrupts are generated. Reset Source: vbus_amod_g_rst_n
30:21	RESERVED	NONE	0h	Reserved
20	IC_STATUS	R	0h	This bit indicates to software whether any tasks [with INT=0] have completed and counted towards interrupt coalescing [i.e., ICSB is set if and only if IC counter > 0]. Bit Value Description 1 = At least one task completion has been counted [IC counter >0] 0 = No task completions have occurred since last counter reset [IC counter =0] Reset Source: vbus_amod_g_rst_n
19:13	RESERVED	NONE	0h	Reserved

Table 14-13525. MMCSD_CTL_CFG_CQ_INTR_COALESCING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:8	CTR_THRESHOLD	R/W	0h	Interrupt Coalescing Counter Threshold [ICCTH]: Software uses this field to configure the number of task completions [only tasks with INT=0 in the Task Descriptor] which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31 NOTE : When ICCTH is 0, task completions are not counted, and counting-based interrupts are not generated.In order to write to this field, the ICCTHWEN bit must be set at the same write operation. Reset Source: vbus_amod_g_rst_n
7	RESERVED	NONE	0h	Reserved
6:0	TIMEOUT_VAL	R/W	0h	Interrupt Coalescing Timeout Value [ICTOVAL]: Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timers unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register.The minimum value is 01h [1024 clock periods] and the maximum value is 7Fh [127*1024 clock periods]. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency [period = 52.08 ns]. If the setting in ICTOVAL is 10h, the calculated polling period is 16*1024*52.08 ns= 853.33 us NOTE: When ICTOVAL is 0, the timer is not running, and timer-based interrupts are not generated. In order to write to this field, the ICTOVALWEN bit must be set at the same write operation. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.116 MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR Register

14.7.4.6.2.116.1 MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR Register (Offset = 220h) [reset = 0h]

This register is used for configuring the lower 32 bits of the byte address of the head of the Task 312 Descriptor List in the host memory.

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Table 14-13526. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0220h

Figure 14-6675. MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR Name Register

32	31	30	29	28	27	26	25
CQTDLBA_LO							
R/W							
0h							
24	23	22	21	20	19	18	17
CQTDLBA_LO							
R/W							
0h							
16	15	14	13	12	11	10	9
CQTDLBA_LO							
R/W							
0h							
8	7	6	5	4	3	2	1
CQTDLBA_LO							
R/W							
0h							

Table 14-13527. MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDLBA_LO	R/W	0h	Task Descriptor List Base Address [TDLBA] This register stores the LSB bits [bits 31:0] of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * [Task Descrip-tor size + Transfer Descriptor size] as configured by Host driver. This address shall be set on Byte1 KByte boundary.: The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.117 MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR_UPBITS Register

14.7.4.6.2.117.1 MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR_UPBITS Register (Offset = 224h) [reset = 0h]

This register is used for configuring the upper 32 bits of the byte address of the head of the Task 316 Descriptor List in the host memory.

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Table 14-13528. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0224h

Figure 14-6676. MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR_UPBITS Name Register

32	31	30	29	28	27	26	25
CQTDLBA_HI							
R/W							
0h							
24	23	22	21	20	19	18	17
CQTDLBA_HI							
R/W							
0h							
16	15	14	13	12	11	10	9
CQTDLBA_HI							
R/W							
0h							
8	7	6	5	4	3	2	1
CQTDLBA_HI							
R/W							
0h							

Table 14-13529. MMCSD_CTL_CFG_CQ_TDL_BASE_ADDR_UPBITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDLBA_HI	R/W	0h	Task Descriptor List Base Address [TDLBA] This register stores the MSB bits [bits 63:32] of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * [Task Descrip-tor size + Transfer Descriptor size] as configured by Host driver. This register is reserved when using 32-bit addressing mode. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.118 MMCSD_CTL_CFG_CQ_TASK_DOOR_BELL Register

14.7.4.6.2.118.1 MMCSD_CTL_CFG_CQ_TASK_DOOR_BELL Register (Offset = 228h) [reset = 0h]

Using this register, software triggers CQE to process a new task.

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Table 14-13530. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0228h

Figure 14-6677. MMCSD_CTL_CFG_CQ_TASK_DOOR_BELL Name Register

32	31	30	29	28	27	26	25
CQTDB_VAL							
R/W1TS							
0h							
24	23	22	21	20	19	18	17
CQTDB_VAL							
R/W1TS							
0h							
16	15	14	13	12	11	10	9
CQTDB_VAL							
R/W1TS							
0h							
8	7	6	5	4	3	2	1
CQTDB_VAL							
R/W1TS							
0h							

Table 14-13531. MMCSD_CTL_CFG_CQ_TASK_DOOR_BELL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTDB_VAL	R/W1TS	0h	Command Queueing Task Doorbell Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start pro-cessing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transac-tions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS[CMD44] and QUEUED_TASK_ADDRESS [CMD45]commands to the device. CQE processes DCMD tasks [in slot #31, when enabled]by reading the Task Descriptor, and generating the com-mand encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: [a] When a task execution is completed [with success or error] [b] The task is cleared using CQTCLR register [c] All tasks are cleared using CQCTL register [d] CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time [batch submission] by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index,starting with the lowest index. If one or more tasks in the batch are marked with QBR,the ordering of execution will be based on said process-ing order. Writing 0 by software shall have no impact on the hard-ware, and will not change the value of the register bit. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.119 MMCSD_CTL_CFG_CQ_TASK_COMP_NOTIF Register

14.7.4.6.2.119.1 MMCSD_CTL_CFG_CQ_TASK_COMP_NOTIF Register (Offset = 22Ch) [reset = 0h]

This register is used by CQE to notify software about completed tasks.

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Table 14-13532. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 022Ch

Figure 14-6678. MMCSD_CTL_CFG_CQ_TASK_COMP_NOTIF Name Register

32	31	30	29	28	27	26	25
CQTCN_VAL							
R/W1TC							
0h							
24	23	22	21	20	19	18	17
CQTCN_VAL							
R/W1TC							
0h							
16	15	14	13	12	11	10	9
CQTCN_VAL							
R/W1TC							
0h							
8	7	6	5	4	3	2	1
CQTCN_VAL							
R/W1TC							
0h							

Table 14-13533. MMCSD_CTL_CFG_CQ_TASK_COMP_NOTIF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTCN_VAL	R/W1TC	0h	CQE shall set bit n of this register [at the same time it clears bit n of CQTDBR] when a task execution is com-pleted [with success or error]. When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the rele-vant bit fields by writing 1 to the corresponding bits. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.120 MMCSD_CTL_CFG_CQ_DEV_QUEUE_STATUS Register

14.7.4.6.2.120.1 MMCSD_CTL_CFG_CQ_DEV_QUEUE_STATUS Register (Offset = 230h) [reset = 0h]

This register stores the most recent value of the device s queue status.

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Table 14-13534. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0230h

Figure 14-6679. MMCSD_CTL_CFG_CQ_DEV_QUEUE_STATUS Name Register

32	31	30	29	28	27	26	25
CQDQ_STS							
R							
0h							
24	23	22	21	20	19	18	17
CQDQ_STS							
R							
0h							
16	15	14	13	12	11	10	9
CQDQ_STS							
R							
0h							
8	7	6	5	4	3	2	1
CQDQ_STS							
R							
0h							

Table 14-13535. MMCSD_CTL_CFG_CQ_DEV_QUEUE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQDQ_STS	R	0h	Every time the Host controller receives a queue status register [QSR] from the device, it updates this register with the response of status command, i.e. the devices queue status. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.121 MMCSD_CTL_CFG_CQ_DEV_PENDING_TASKS Register

14.7.4.6.2.121.1 MMCSD_CTL_CFG_CQ_DEV_PENDING_TASKS Register (Offset = 234h) [reset = 0h]

This register indicates to software which tasks are queued in the device, awaiting execution.

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Table 14-13536. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0234h

Figure 14-6680. MMCSD_CTL_CFG_CQ_DEV_PENDING_TASKS Name Register

32	31	30	29	28	27	26	25
CQDP_TSKS							
R							
0h							
24	23	22	21	20	19	18	17
CQDP_TSKS							
R							
0h							
16	15	14	13	12	11	10	9
CQDP_TSKS							
R							
0h							
8	7	6	5	4	3	2	1
CQDP_TSKS							
R							
0h							

Table 14-13537. MMCSD_CTL_CFG_CQ_DEV_PENDING_TASKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQDP_TSKS	R	0h	Bit n of this register is set if and only if QUEUED_TASK_PARAMS [CMD44] and QUEUED_TASK_ADDRESS [CMD45] were sent for this specific task and if this task hasnt been executed yet.CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution.Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued,the driver sends a CMDQ_TASK_MGMT [CMD48] to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using CQCTL register. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.122 MMCSD_CTL_CFG_CQ_TASK_CLEAR Register

14.7.4.6.2.122.1 MMCSD_CTL_CFG_CQ_TASK_CLEAR Register (Offset = 238h) [reset = 0h]

This register is used for removing an outstanding task in the CQE. 327. The register should be used only when CQE is in Halt state.

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Table 14-13538. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0238h

Figure 14-6681. MMCSD_CTL_CFG_CQ_TASK_CLEAR Name Register

32	31	30	29	28	27	26	25
CQTCLR							
R/W							
0h							
24	23	22	21	20	19	18	17
CQTCLR							
R/W							
0h							
16	15	14	13	12	11	10	9
CQTCLR							
R/W							
0h							
8	7	6	5	4	3	2	1
CQTCLR							
R/W							
0h							

Table 14-13539. MMCSD_CTL_CFG_CQ_TASK_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQTCLR	R/W	0h	Writing 1 to bit n of this register orders CQE to clear a task which software has previously issued.This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit.When software writes 1 to a bit in this register,CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields [sets a value of 0] in CQTCLR and in CQTDBR once clear operation is complete.Software should poll on the CQTCLR until it is cleared to verify clear operation was complete.Writing to this register only clears the task in the CQE and does not have impact on the device. In order to dis-card the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state.Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using CQCTL register.Writing 0 to a register bit shall have no impact. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.123 MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG1 Register

14.7.4.6.2.123.1 MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG1 Register (Offset = 240h) [reset = 11000h]

The register controls the when SEND_QUEUE_STATUS commands are sent.

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Table 14-13540. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0240h

Figure 14-6682. MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG1 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							

24	23	22	21	20	19	18	17
RESERVED				CMD_BLK_CNTR			
NONE				R/W			
0h				1h			

16	15	14	13	12	11	10	9
CMD_IDLE_TIMER							
R/W							
1000h							

8	7	6	5	4	3	2	1
CMD_IDLE_TIMER							
R/W							
1000h							

Table 14-13541. MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	CMD_BLK_CNTR	R/W	1h	This field indicates to CQE when to send SEND_QUEUE_STATUS [CMD13] command to inquire the status of the devices task queue.A value of n means CQE shall send status command on the CMD line, during the transfer of data block BLOCK_CNT-n, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction.A value of 0 means that SEND_QUEUE_STATUS [CMD13] command shall not be sent during the transac-tion. Instead it will be sent only when the data lines are idle.A value of 1 means that STATUS command is to be sent during the last block of the transaction. Reset Source: vbus_amod_g_rst_n

Table 14-13541. MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	CMD_IDLE_TIMER	R/W	1000h	This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS [CMD13] polling.Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS.Timer units are clock periods of theclock whose fre-quency is specified in the Internal Timer Clock Fre-quency field CQCAP register.The minimum value is 0001h [1 clock period] and the maximum value is FFFFh [65535 clock periods]. Default interval is: 4096 clock periods. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency [period = 52.08 ns]. If the setting in CQSST is 1000h, the calcu.lated polling period is 4096*52.08 ns= 213.33 us. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.124 MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG2 Register

14.7.4.6.2.124.1 MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG2 Register (Offset = 244h) [reset = 0h]

This register is used for 333 configuring RCA field in SEND_QUEUE_STATUS command argu-ment.

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Table 14-13542. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0244h

Figure 14-6683. MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG2 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
QUEUE_RCA							
R/W							
0h							
8	7	6	5	4	3	2	1
QUEUE_RCA							
R/W							
0h							

Table 14-13543. MMCSD_CTL_CFG_CQ_SEND_STS_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_RCA	R/W	0h	This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_ STATUS [CMD13] com-mand. argument. CQE shall copy this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS [CMD13] command. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.125 MMCSD_CTL_CFG_CQ_DCMD_RESPONSE Register

14.7.4.6.2.125.1 MMCSD_CTL_CFG_CQ_DCMD_RESPONSE Register (Offset = 248h) [reset = 0h]

This register is used for passing the response of a DCMD task to software.

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Table 14-13544. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0248h

Figure 14-6684. MMCSD_CTL_CFG_CQ_DCMD_RESPONSE Name Register

32	31	30	29	28	27	26	25
LAST_RESP							
R							
0h							
24	23	22	21	20	19	18	17
LAST_RESP							
R							
0h							
16	15	14	13	12	11	10	9
LAST_RESP							
R							
0h							
8	7	6	5	4	3	2	1
LAST_RESP							
R							
0h							

Table 14-13545. MMCSD_CTL_CFG_CQ_DCMD_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LAST_RESP	R	0h	This register contains the response of the command generated by the last direct-command [DCMD] task which was sent.CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of CQT-DBR register is cleared by CQE. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.126 MMCSD_CTL_CFG_CQ_RESP_ERR_MASK Register

14.7.4.6.2.126.1 MMCSD_CTL_CFG_CQ_RESP_ERR_MASK Register (Offset = 250h) [reset = FDF9A080h]

This register controls the generation of Response Error Detection (RED) interrupt.

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Table 14-13546. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0250h

Figure 14-6685. MMCSD_CTL_CFG_CQ_RESP_ERR_MASK Name Register

32	31	30	29	28	27	26	25
CQRMEM							
R/W							
fdf9a080h							
24	23	22	21	20	19	18	17
CQRMEM							
R/W							
fdf9a080h							
16	15	14	13	12	11	10	9
CQRMEM							
R/W							
fdf9a080h							
8	7	6	5	4	3	2	1
CQRMEM							
R/W							
fdf9a080h							

Table 14-13547. MMCSD_CTL_CFG_CQ_RESP_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CQRMEM	R/W	fdf9a080h	This bit is used as in interrupt mask on the device status filed which is received in R1/R1b responses.Bit Value Description [for any bit i]:1 = When a R1/R1b response is received, with bit i in the device status set, a RED interrupt is generated 0 = When a R1/R1b response is received, bit i in the device status is ignored The reset value of this register is set to trigger an inter-rupt on all Error type bits in the device status, as defined in Section 6.13.NOTE: Responses to CMD13 [SQS] encode the QSR,so they are ignored by this logic Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.127 MMCSD_CTL_CFG_CQ_TASK_ERR_INFO Register

14.7.4.6.2.127.1 MMCSD_CTL_CFG_CQ_TASK_ERR_INFO Register (Offset = 254h) [reset = 0h]

This register is updated by CQE when an error occurs on data or command related to a task activity. When such error is detected by CQE or indicated by the eMMC controller CQE stores in CQTERRI the task IDs and the command indices of the commands which were executed on the 343 command line and data lines when the error occurred.Software is expected to use this information in the error recovery procedure.

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Table 14-13548. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0254h

Figure 14-6686. MMCSD_CTL_CFG_CQ_TASK_ERR_INFO Name Register

32	31	30	29	28	27	26	25
DATERR_VALID	RESERVED		DATERR_TASK_ID				
R	NONE		R				
0h	0h		0h				
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
RESERVED		DATERR_CMD_INDEX					
NONE		R					
0h		0h					
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
RESP_MODE_VALID	RESERVED		RESP_MODE_TASK_ID				
R	NONE		R				
0h	0h		0h				
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
RESERVED		RESP_MODE_CMD_INDEX					
NONE		R					
0h		0h					

Table 14-13549. MMCSD_CTL_CFG_CQ_TASK_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DATERR_VALID	R	0h	Data Transfer Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1. If a no data transfer is in progress when the error is detected/ indicated, the bit is cleared to 0. Reset Source: vbus_amod_g_rst_n
30:29	RESERVED	NONE	0h	Reserved
28:24	DATERR_TASK_ID	R	0h	Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller Reset Source: vbus_amod_g_rst_n
23:22	RESERVED	NONE	0h	Reserved

Table 14-13549. MMCSD_CTL_CFG_CQ_TASK_ERR_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21:16	DATERR_CMD_INDEX	R	0h	Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK[CMD46] or EXECUTE_WRITE_TASK [CMD47] accord-ing to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n
15	RESP_MODE_VALID	R	0h	Response Mode Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0. Reset Source: vbus_amod_g_rst_n
14:13	RESERVED	NONE	0h	Reserved
12:8	RESP_MODE_TASK_ID	R	0h	Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:0	RESP_MODE_CMD_INDEX	R	0h	Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.128 MMCSD_CTL_CFG_CQ_CMD_RESP_INDEX Register

14.7.4.6.2.128.1 MMCSD_CTL_CFG_CQ_CMD_RESP_INDEX Register (Offset = 258h) [reset = 0h]

This register stores the index of the last received command response.

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Table 14-13550. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0258h

Figure 14-6687. MMCSD_CTL_CFG_CQ_CMD_RESP_INDEX Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">LAST_CRI</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-13551. MMCSD_CTL_CFG_CQ_CMD_RESP_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	LAST_CRI	R	0h	This field stores the index of the last received command response. CQE shall update the value every time a com-mand response is received. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.129 MMCSD_CTL_CFG_CQ_CMD_RESP_ARG Register

14.7.4.6.2.129.1 MMCSD_CTL_CFG_CQ_CMD_RESP_ARG Register (Offset = 25Ch) [reset = 0h]

This register stores the index of the last received command response.

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Table 14-13552. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 025Ch

Figure 14-6688. MMCSD_CTL_CFG_CQ_CMD_RESP_ARG Name Register

32	31	30	29	28	27	26	25
LAST_CRA							
R							
0h							
24	23	22	21	20	19	18	17
LAST_CRA							
R							
0h							
16	15	14	13	12	11	10	9
LAST_CRA							
R							
0h							
8	7	6	5	4	3	2	1
LAST_CRA							
R							
0h							

Table 14-13553. MMCSD_CTL_CFG_CQ_CMD_RESP_ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LAST_CRA	R	0h	This field stores the argument of the last received com-mand. CQE shall update the value every time a com-mand response is received. Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.130 MMCSD_CTL_CFG_CQ_ERROR_TASK_ID Register

14.7.4.6.2.130.1 MMCSD_CTL_CFG_CQ_ERROR_TASK_ID Register (Offset = 260h) [reset = 0h]

CQ Error Task ID Register

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Table 14-13554. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 0260h

Figure 14-6689. MMCSD_CTL_CFG_CQ_ERROR_TASK_ID Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED			TERR_ID				
NONE			R				
0h			0h				

Table 14-13555. MMCSD_CTL_CFG_CQ_ERROR_TASK_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	TERR_ID	R	0h	Task Error ID Reset Source: vbus_amod_g_rst_n

14.7.4.6.2.131 MMCSD_SS_CFG_SS_ID_REV_REG Register

14.7.4.6.2.131.1 MMCSD_SS_CFG_SS_ID_REV_REG Register (Offset = 0h) [reset = 68421A00h]

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem

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Table 14-13556. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8000h

Figure 14-6690. MMCSD_SS_CFG_SS_ID_REV_REG Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">MOD_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6842h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">MOD_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6842h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="5">RTL_VER</td><td colspan="3">MAJ_REV</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">3h</td><td colspan="3">2h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MIN_REV</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-13557. MMCSD_SS_CFG_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MOD_ID	R	6842h	Module ID Reset Source: vbus_smod_g_rst_n
15:11	RTL_VER	R	3h	RTL version Reset Source: vbus_smod_g_rst_n
10:8	MAJ_REV	R	2h	Major revision Reset Source: vbus_smod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: vbus_smod_g_rst_n
5:0	MIN_REV	R	0h	Minor revision Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.132 MMCSD_SS_CFG_CTL_CFG_1_REG Register

14.7.4.6.2.132.1 MMCSD_SS_CFG_CTL_CFG_1_REG Register (Offset = 10h) [reset = 201030C8h]

The Controller Config 1 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2.

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Table 14-13558. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8010h

Figure 14-6691. MMCSD_SS_CFG_CTL_CFG_1_REG Name Register

32	31	30	29	28	27	26	25
RESERVED		TUNINGCOUNT					
NONE		R/W					
0h		20h					
24	23	22	21	20	19	18	17
RESERVED			ASYNCWKUPENA	RESERVED			
NONE			R/W	NONE			
0h			1h	1h			
16	15	14	13	12	11	10	9
CQFMUL				RESERVED		CQFVAL	
R/W				NONE		R/W	
3h				0h		c8h	
8	7	6	5	4	3	2	1
CQFVAL							
R/W							
c8h							

Table 14-13559. MMCSD_SS_CFG_CTL_CFG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	TUNINGCOUNT	R/W	20h	Configures the Number of Taps (Phases) of the RX clock that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the RX clock during the Tuning Procedure. Reset Source: vbus_smod_g_rst_n
23:21	RESERVED	NONE	0h	Reserved
20	ASYNCWKUPENA	R/W	1h	Determines the Wakeup Signal Generation Mode. 0: Synchronous Wakeup Mode: The xin_clk has to be running for this mode. The Card Insertion/Removal/Interrupt events are detected synchronously on the xin_clk and the Wakeup Event is generated. The Assertion and deassertion of the wakeup Event signal synchronous to xin_clk. 1: Asyncrhonous Wakeup Mode: The xin_clk and the host_clk can be stopped in this mode and the Wake up Event is asynchronously generated based on the Card Insertion/Removal/Interrupt Events. The Assertion and deassertion of the wakeup Event signal is asynchronous. Reset Source: vbus_smod_g_rst_n
19:16	RESERVED	NONE	1h	Reserved
15:12	CQFMUL	R/W	3h	FMUL for the CQ Internal Timer Clock Frequency Reset Source: vbus_smod_g_rst_n

Table 14-13559. MMCSD_SS_CFG_CTL_CFG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	RESERVED	NONE	0h	Reserved
9:0	CQFVAL	R/W	c8h	FVAL for the CQ Internal Timer Clock Frequency Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.133 MMCSD_SS_CFG_CTL_CFG_2_REG Register

14.7.4.6.2.133.1 MMCSD_SS_CFG_CTL_CFG_2_REG Register (Offset = 14h) [reset = 25ECC801h]

The Controller Config 2 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the lsb fields in the Capabilities Register inside the Arasan eMMC/SD Controller.

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Table 14-13560. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8014h

Figure 14-6692. MMCSD_SS_CFG_CTL_CFG_2_REG Name Register

32	31	30	29	28	27	26	25
SLOTTYPE		ASYNCHINTRSUPPORT	RESERVED		SUPPORT1P8VOLT	SUPPORT3P0VOLT	SUPPORT3P3VOLT
R/W		R/W	NONE		R/W	R/W	R/W
0h		1h	0h		1h	0h	1h
24	23	22	21	20	19	18	17
SUSPRESSUPPORT	SDMASUPPORT	HIGHSPEEDSUPPORT	RESERVED	ADMA2SUPPORT	SUPPORT8BIT	MAXBLKLENGTH	
R/W	R/W	R/W	NONE	R/W	R/W	R/W	
1h	1h	1h	1h	1h	1h	0h	
16	15	14	13	12	11	10	9
BASECLKFREQ							
R/W							
c8h							
8	7	6	5	4	3	2	1
TIMEOUTCLKUNIT	RESERVED	TIMEOUTCLKFREQ					
R/W	NONE	R/W					
0h	0h	1h					

Table 14-13561. MMCSD_SS_CFG_CTL_CFG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SLOTTYPE	R/W	0h	Slot Type. Should be set based on the final product usage. 00 - Removable SCard Slot, 01 - Embedded Slot for One Device, 10 - Shared Bus Slot, 11 - Reserved. Reset Source: vbus_smod_g_rst_n
29	ASYNCHINTRSUPPORT	R/W	1h	Asynchronous Interrupt Support. Suggested Value is 1'b1 (The Core supports monitoring of Asynchronous Interrupt). Reset Source: vbus_smod_g_rst_n
28:27	RESERVED	NONE	0h	Reserved
26	SUPPORT1P8VOLT	R/W	1h	1.8V Support. Suggested Value is 1'b1 (The 1.8 Volt Switching is supported by Core). Optionally can be set to 1'b0 if the application doesn't want 1.8V switching (SD3.0). Reset Source: vbus_smod_g_rst_n
25	SUPPORT3P0VOLT	R/W	0h	3.0V Support. Should be set based on whether 3.0V is supported on the SD Interface. Reset Source: vbus_smod_g_rst_n

Table 14-13561. MMCSD_SS_CFG_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	SUPPORT3P3VOLT	R/W	1h	3.3V Support. Suggested Value is 1'b1 as the 3.3 V is the default voltage on the SD Interface. Reset Source: vbus_smod_g_rst_n
23	SUSPRESSUPPORT	R/W	1h	Suspend/Resume Support. Suggested Value is 1'b1 (The Suspend/ Resume is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support Suspend/Resume Mode. Reset Source: vbus_smod_g_rst_n
22	SDMASUPPORT	R/W	1h	SDMA Support. Suggested Value is 1'b1 (The SDMA is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support SDMA Mode. Reset Source: vbus_smod_g_rst_n
21	HIGHSPEEDSUPPORT	R/W	1h	High Speed Support. Suggested Value is 1'b1 (The High Speed mode is supported by Core). Reset Source: vbus_smod_g_rst_n
20	RESERVED	NONE	1h	Reserved
19	ADMA2SUPPORT	R/W	1h	ADMA2 Support. Suggested Value is 1'b1 (The ADMA2 is supported by Core). Optionally can be set to 1'b0 if the application doesn't want to support ADMA2 Mode. Reset Source: vbus_smod_g_rst_n
18	SUPPORT8BIT	R/W	1h	8-bit Support for Embedded Device. Suggested Value is 1'b1 (The Core supports 8-bit Interface). Optionally an be set to 1'b0 if the Application supports only 4-bit SD Interface. Reset Source: vbus_smod_g_rst_n
17:16	MAXBLKLENGTH	R/W	0h	Max Block Length. Maximum Block Length supported by the Core/ Device. 00: 512 (Bytes), 01: 1024, 10: 2048, 11: Reserved. Reset Source: vbus_smod_g_rst_n
15:8	BASECLKFREQ	R/W	c8h	Base Clock Frequency for SD Clock. This is the frequency of the xin_clk. Reset Source: vbus_smod_g_rst_n
7	TIMEOUTCLKUNIT	R/W	0h	Timeout Clock Unit. Suggested Value is 1'b0 (KHz). Reset Source: vbus_smod_g_rst_n
6	RESERVED	NONE	0h	Reserved
5:0	TIMEOUTCLKFREQ	R/W	1h	Timeout Clock Frequency. Suggested Value is 1 KHz. Internally the 1msec Timer is used for Timeout Detection. The 1msec Timer is generated from the xin_clk. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.134 MMCSD_SS_CFG_CTL_CFG_3_REG Register

14.7.4.6.2.134.1 MMCSD_SS_CFG_CTL_CFG_3_REG Register (Offset = 18h) [reset = 18000407h]

The Controller Config 3 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the msb fields in the Capabilities Register inside the Arasan eMMC/SD Controller.

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Table 14-13562. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8018h

Figure 14-6693. MMCSD_SS_CFG_CTL_CFG_3_REG Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="3">RESERVED</td><td>SUPPORT1P8VDD2</td><td>ADMA3SUPPORT</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="3">Bh</td><td>1h</td><td>1h</td><td colspan="3">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">CLOCKMULTIPLIER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="2">RETUNINGMODES</td><td>TUNINGFORSDR50</td><td>RESERVED</td><td colspan="4">RETUNINGTIMERCNT</td></tr>
<tr><td colspan="2">R/W</td><td>R/W</td><td>NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="4">4h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td>TYPE4SUPPORT</td><td>DDRIVERSUPPORT</td><td>CDRIVERSUPPORT</td><td>ADRIVERSUPPORT</td><td>RESERVED</td><td>DDR50SUPPORT</td><td>SDR104SUPPORT</td><td>SDR50SUPPORT</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-13563. MMCSD_SS_CFG_CTL_CFG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	Bh	Reserved
28	SUPPORT1P8VDD2	R/W	1h	1.8V VDD2 Support. Reset Source: vbus_smod_g_rst_n
27	ADMA3SUPPORT	R/W	1h	ADMA3 Support. Reset Source: vbus_smod_g_rst_n
26:24	RESERVED	NONE	0h	Reserved
23:16	CLOCKMULTIPLIER	R/W	0h	Clock Multiplier. This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator. FFh Clock Multiplier M = 256, ..., 02h Clock Multiplier M = 3, 01h Clock Multiplier M = 2, 00h Clock Multiplier is Not Supported. Reset Source: vbus_smod_g_rst_n
15:14	RETUNINGMODES	R/W	0h	Re-Tuning Modes. Should be set to 2'b00 as the Core supports only the Software Timer based Re-Tuning. Reset Source: vbus_smod_g_rst_n

Table 14-13563. MMCSD_SS_CFG_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TUNINGFORSDR50	R/W	0h	Use Tuning for SDR50. This bit should be set if the Application wants Tuning be used for SDR50 Modes. The Core operates with or with out tuning for SDR50 mode as long as the Clock can be manually tuned using tap delay. Reset Source: vbus_smod_g_rst_n
12	RESERVED	NONE	0h	Reserved
11:8	RETUNINGTIMERCNT	R/W	4h	Timer Count for Re-Tuning. This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4'b0 disables Re-Tuning Timer. Reset Source: vbus_smod_g_rst_n
7	TYPE4SUPPORT	R/W	0h	Driver Type 4 Support. This bit should be set based on whether Driver Type 4 for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
6	DDRIVERSUPPORT	R/W	0h	Driver Type D Support. This bit should be set based on whether Driver Type D for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
5	CDRIVERSUPPORT	R/W	0h	Driver Type C Support. This bit should be set based on whether Driver Type C for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
4	ADRIVERSUPPORT	R/W	0h	Driver Type A Support. This bit should be set based on whether Driver Type A for 1.8 Signalling is supported or not. Reset Source: vbus_smod_g_rst_n
3	RESERVED	NONE	1h	Reserved
2	DDR50SUPPORT	R/W	1h	DDR50 Support. Suggested Value is 1'b1 (The Core supports DDR50 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support DDR50. Reset Source: vbus_smod_g_rst_n
1	SDR104SUPPORT	R/W	1h	SDR104 Support. Suggested Value is 1'b1 (The Core supports SDR104 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support SDR104. Reset Source: vbus_smod_g_rst_n
0	SDR50SUPPORT	R/W	1h	SDR50 Support. Suggested Value is 1'b1 (The Core supports SDR50 mode of operation). Optionally can be set to 1'b0 if the application doesn't want to support SDR50. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.135 MMCSD_SS_CFG_CTL_CFG_4_REG Register

14.7.4.6.2.135.1 MMCSD_SS_CFG_CTL_CFG_4_REG Register (Offset = 1Ch) [reset = 0h]

The Controller Config 4 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the lsb fields in the Maximum Current Capabilities Register inside the Arasan eMMC/SD Controller.

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Table 14-13564. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 801Ch

Figure 14-6694. MMCSD_SS_CFG_CTL_CFG_4_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
MAXCURRENT1P8V							
R/W							
0h							
16	15	14	13	12	11	10	9
MAXCURRENT3P0V							
R/W							
0h							
8	7	6	5	4	3	2	1
MAXCURRENT3P3V							
R/W							
0h							

Table 14-13565. MMCSD_SS_CFG_CTL_CFG_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	MAXCURRENT1P8V	R/W	0h	Maximum Current for 1.8V. Reset Source: vbus_smod_g_rst_n
15:8	MAXCURRENT3P0V	R/W	0h	Maximum Current for 3.0V. Reset Source: vbus_smod_g_rst_n
7:0	MAXCURRENT3P3V	R/W	0h	Maximum Current for 3.3V. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.136 MMCSD_SS_CFG_CTL_CFG_5_REG Register

14.7.4.6.2.136.1 MMCSD_SS_CFG_CTL_CFG_5_REG Register (Offset = 20h) [reset = 0h]

The Controller Config 5 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the msb fields in the Maximum Current Capabilities Register inside the Arasan eMMC/SD Controller.

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Table 14-13566. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8020h

Figure 14-6695. MMCSD_SS_CFG_CTL_CFG_5_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
MAXCURRENTVDD2							
R/W							
0h							

Table 14-13567. MMCSD_SS_CFG_CTL_CFG_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MAXCURRENTVDD2	R/W	0h	Maximum Current for 1.8 V (VDD2). Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.137 MMCSD_SS_CFG_CTL_CFG_6_REG Register

14.7.4.6.2.137.1 MMCSD_SS_CFG_CTL_CFG_6_REG Register (Offset = 24h) [reset = 100h]

The Controller Config 6 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for Initialization inside the Arasan eMMC/SD Controller.

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Table 14-13568. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8024h

Figure 14-6696. MMCSD_SS_CFG_CTL_CFG_6_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
989680h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
989680h							
16	15	14	13	12	11	10	9
RESERVED			INITPRESETVAL				
NONE			R/W				
989680h			100h				
8	7	6	5	4	3	2	1
INITPRESETVAL							
R/W							
100h							

Table 14-13569. MMCSD_SS_CFG_CTL_CFG_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	989680h	Reserved
12:0	INITPRESETVAL	R/W	100h	Preset Value for Initialization. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.138 MMCSD_SS_CFG_CTL_CFG_7_REG Register

14.7.4.6.2.138.1 MMCSD_SS_CFG_CTL_CFG_7_REG Register (Offset = 28h) [reset = 4h]

The Controller Config 7 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for Default Speed inside the Arasan eMMC/SD Controller.

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Table 14-13570. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8028h

Figure 14-6697. MMCSD_SS_CFG_CTL_CFG_7_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
Ah							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
Ah							
16	15	14	13	12	11	10	9
RESERVED			DSPDPRESETVAL				
NONE			R/W				
Ah			4h				
8	7	6	5	4	3	2	1
DSPDPRESETVAL							
R/W							
4h							

Table 14-13571. MMCSD_SS_CFG_CTL_CFG_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	Ah	Reserved
12:0	DSPDPRESETVAL	R/W	4h	Preset Value for Default Speed. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.139 MMCSD_SS_CFG_CTL_CFG_8_REG Register

14.7.4.6.2.139.1 MMCSD_SS_CFG_CTL_CFG_8_REG Register (Offset = 2Ch) [reset = 2h]

The Controller Config 8 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for High Speed inside the Arasan eMMC/SD Controller.

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Table 14-13572. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 802Ch

Figure 14-6698. MMCSD_SS_CFG_CTL_CFG_8_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
1h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
1h							
16	15	14	13	12	11	10	9
RESERVED			HSPDPRESETVAL				
NONE			R/W				
1h			2h				
8	7	6	5	4	3	2	1
HSPDPRESETVAL							
R/W							
2h							

Table 14-13573. MMCSD_SS_CFG_CTL_CFG_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	1h	Reserved
12:0	HSPDPRESETVAL	R/W	2h	Preset Value for High Speed. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.140 MMCSD_SS_CFG_CTL_CFG_9_REG Register

14.7.4.6.2.140.1 MMCSD_SS_CFG_CTL_CFG_9_REG Register (Offset = 30h) [reset = 4h]

The Controller Config 9 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for SDR12 inside the Arasan eMMC/SD Controller.

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Table 14-13574. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8030h

Figure 14-6699. MMCSD_SS_CFG_CTL_CFG_9_REG Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">Ah</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">Ah</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">SDR12PRESETVAL</td></tr>
<tr><td colspan="3">NONE</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">Ah</td><td colspan="5">4h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">SDR12PRESETVAL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">4h</td></tr>
</table>

Table 14-13575. MMCSD_SS_CFG_CTL_CFG_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	Ah	Reserved
12:0	SDR12PRESETVAL	R/W	4h	Preset Value for SDR12. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.141 MMCSD_SS_CFG_CTL_CFG_10_REG Register

14.7.4.6.2.141.1 MMCSD_SS_CFG_CTL_CFG_10_REG Register (Offset = 34h) [reset = 2h]

The Controller Config 10 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for SDR25 inside the Arasan eMMC/SD Controller.

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Table 14-13576. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8034h

Figure 14-6700. MMCSD_SS_CFG_CTL_CFG_10_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
1h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
1h							
16	15	14	13	12	11	10	9
RESERVED			SDR25PRESETVAL				
NONE			R/W				
1h			2h				
8	7	6	5	4	3	2	1
SDR25PRESETVAL							
R/W							
2h							

Table 14-13577. MMCSD_SS_CFG_CTL_CFG_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	1h	Reserved
12:0	SDR25PRESETVAL	R/W	2h	Preset Value for SDR25. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.142 MMCSD_SS_CFG_CTL_CFG_11_REG Register

14.7.4.6.2.142.1 MMCSD_SS_CFG_CTL_CFG_11_REG Register (Offset = 38h) [reset = 1h]

The Controller Config 11 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for SDR50 inside the Arasan eMMC/SD Controller.

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Table 14-13578. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8038h

Figure 14-6701. MMCSD_SS_CFG_CTL_CFG_11_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED			SDR50PRESETVAL				
NONE			R/W				
0h			1h				
8	7	6	5	4	3	2	1
SDR50PRESETVAL							
R/W							
1h							

Table 14-13579. MMCSD_SS_CFG_CTL_CFG_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR50PRESETVAL	R/W	1h	Preset Value for SDR50. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.143 MMCSD_SS_CFG_CTL_CFG_12_REG Register

14.7.4.6.2.143.1 MMCSD_SS_CFG_CTL_CFG_12_REG Register (Offset = 3Ch) [reset = 0h]

The Controller Config 12 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for SDR104 inside the Arasan eMMC/SD Controller.

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Table 14-13580. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 803Ch

Figure 14-6702. MMCSD_SS_CFG_CTL_CFG_12_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED			SDR104PRESETVAL				
NONE			R/W				
0h			0h				
8	7	6	5	4	3	2	1
SDR104PRESETVAL							
R/W							
0h							

Table 14-13581. MMCSD_SS_CFG_CTL_CFG_12_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:0	SDR104PRESETVAL	R/W	0h	Preset Value for SDR104. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.144 MMCSD_SS_CFG_CTL_CFG_13_REG Register

14.7.4.6.2.144.1 MMCSD_SS_CFG_CTL_CFG_13_REG Register (Offset = 40h) [reset = 2h]

The Controller Config 13 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for DDR50 inside the Arasan eMMC/SD Controller.

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Table 14-13582. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8040h

Figure 14-6703. MMCSD_SS_CFG_CTL_CFG_13_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
1h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
1h							
16	15	14	13	12	11	10	9
RESERVED			DDR50PRESETVAL				
NONE			R/W				
1h			2h				
8	7	6	5	4	3	2	1
DDR50PRESETVAL							
R/W							
2h							

Table 14-13583. MMCSD_SS_CFG_CTL_CFG_13_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	1h	Reserved
12:0	DDR50PRESETVAL	R/W	2h	Preset Value for DDR50. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.145 MMCSD_SS_CFG_CTL_CFG_14_REG Register

14.7.4.6.2.145.1 MMCSD_SS_CFG_CTL_CFG_14_REG Register (Offset = 44h) [reset = 0h]

The Controller Config 14 Register contains various fields to control the configuration ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller configuration ports please refer to its specification listed in Section 1.2. This register sets the fields in the Preset Values Register for HS400 inside the Arasan eMMC/SD Controller.

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Table 14-13584. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8044h

Figure 14-6704. MMCSD_SS_CFG_CTL_CFG_14_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
0h							

Table 14-13585. MMCSD_SS_CFG_CTL_CFG_14_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.146 MMCSD_SS_CFG_CTL_STAT_1_REG Register

14.7.4.6.2.146.1 MMCSD_SS_CFG_CTL_STAT_1_REG Register (Offset = 60h) [reset = 80000000h]

The Controller Status 1 Register contains various fields to reflect the status of the debug ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-13586. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8060h

Figure 14-6705. MMCSD_SS_CFG_CTL_STAT_1_REG Name Register

32	31	30	29	28	27	26	25
SDHC_CMDIDLE	RESERVED		RXCLKTAPSEL				
R	NONE		R				
1h	0h		0h				
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
RESERVED							
NONE							
0h							
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
DMADEBUGBUS							
R							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
DMADEBUGBUS							
R							
0h							

Table 14-13587. MMCSD_SS_CFG_CTL_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDHC_CMDIDLE	R	1h	Idle signal to enable S/W to gate off the clocks. Reset Source: vbus_smod_g_rst_n
30:29	RESERVED	NONE	0h	Reserved
28:24	RXCLKTAPSEL	R	0h	Controller HW tunning RX clock tap selection value. Reset Source: vbus_smod_g_rst_n
23:16	RESERVED	NONE	0h	Reserved
15:0	DMADEBUGBUS	R	0h	DMA_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.147 MMCSD_SS_CFG_CTL_STAT_2_REG Register

14.7.4.6.2.147.1 MMCSD_SS_CFG_CTL_STAT_2_REG Register (Offset = 64h) [reset = 10h]

The Controller Status 2 Register contains various fields to reflect the status of the debug ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-13588. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8064h

Figure 14-6706. MMCSD_SS_CFG_CTL_STAT_2_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
3E8h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
3E8h							
16	15	14	13	12	11	10	9
CMDDEBUGBUS							
R							
10h							
8	7	6	5	4	3	2	1
CMDDEBUGBUS							
R							
10h							

Table 14-13589. MMCSD_SS_CFG_CTL_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	3E8h	Reserved
15:0	CMDDEBUGBUS	R	10h	CMD_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.148 MMCSD_SS_CFG_CTL_STAT_3_REG Register

14.7.4.6.2.148.1 MMCSD_SS_CFG_CTL_STAT_3_REG Register (Offset = 68h) [reset = 0h]

The Controller Status 3 Register contains various fields to reflect the status of the debug ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-13590. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8068h

Figure 14-6707. MMCSD_SS_CFG_CTL_STAT_3_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
TXDDEBUGBUS							
R							
0h							
8	7	6	5	4	3	2	1
TXDDEBUGBUS							
R							
0h							

Table 14-13591. MMCSD_SS_CFG_CTL_STAT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TXDDEBUGBUS	R	0h	TXD_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.149 MMCSD_SS_CFG_CTL_STAT_4_REG Register

14.7.4.6.2.149.1 MMCSD_SS_CFG_CTL_STAT_4_REG Register (Offset = 6Ch) [reset = 0h]

The Controller Status 4 Register contains various fields to reflect the status of the debug ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-13592. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 806Ch

Figure 14-6708. MMCSD_SS_CFG_CTL_STAT_4_REG Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RXDDEBUGBUS0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">RXDDEBUGBUS0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13593. MMCSD_SS_CFG_CTL_STAT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RXDDEBUGBUS0	R	0h	RXD_CTRL Debug Bus (SD CLK). Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.150 MMCSD_SS_CFG_CTL_STAT_5_REG Register

14.7.4.6.2.150.1 MMCSD_SS_CFG_CTL_STAT_5_REG Register (Offset = 70h) [reset = 8h]

The Controller Status 5 Register contains various fields to reflect the status of the debug ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-13594. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8070h

Figure 14-6709. MMCSD_SS_CFG_CTL_STAT_5_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
64h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
64h							
16	15	14	13	12	11	10	9
RXDDEBUGBUS1							
R							
8h							
8	7	6	5	4	3	2	1
RXDDEBUGBUS1							
R							
8h							

Table 14-13595. MMCSD_SS_CFG_CTL_STAT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	64h	Reserved
15:0	RXDDEBUGBUS1	R	8h	RXD_CTRL Debug Bus (RX CLK). Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.151 MMCSD_SS_CFG_CTL_STAT_6_REG Register

14.7.4.6.2.151.1 MMCSD_SS_CFG_CTL_STAT_6_REG Register (Offset = 74h) [reset = 0h]

The Controller Status 6 Register contains various fields to reflect the status of the debug ports on the Arasan eMMC/SD Controller. For detailed functionality of the Arasan eMMC/SD Controller debug ports please refer to its specification listed in Section 1.2.

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Table 14-13596. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8074h

Figure 14-6710. MMCSD_SS_CFG_CTL_STAT_6_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
TUNDEBUGBUS							
R							
0h							
8	7	6	5	4	3	2	1
TUNDEBUGBUS							
R							
0h							

Table 14-13597. MMCSD_SS_CFG_CTL_STAT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TUNDEBUGBUS	R	0h	TUN_CTRL Debug Bus. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.152 MMCSD_SS_CFG_PHY_CTRL_1_REG Register

14.7.4.6.2.152.1 MMCSD_SS_CFG_PHY_CTRL_1_REG Register (Offset = 100h) [reset = 80000000h]

The PHY Control 1 Register contains various fields to control the ports on the Arasan eMMC/SD PHY. For detailed functionality of the Arasan eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-13598. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8100h

Figure 14-6711. MMCSD_SS_CFG_PHY_CTRL_1_REG Name Register

32	31	30	29	28	27	26	25
IOMUX_ENABLE	DQ_7_4_IOMUX_EN	RESERVED					
R/W	R/W	NONE					
1h	0h	204FCE5E3E25026110000000h					
24	23	22	21	20	19	18	17
RESERVED							
NONE							
204FCE5E3E25026110000000h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
204FCE5E3E25026110000000h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
204FCE5E3E25026110000000h							

Table 14-13599. MMCSD_SS_CFG_PHY_CTRL_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IOMUX_ENABLE	R/W	1h	IO mux enable. Set 1 for GPIO. Set 0 for eMMC/SD Reset Source: vbus_smod_g_rst_n
30	DQ_7_4_IOMUX_EN	R/W	0h	IO mux enable for data lines 7 through 4 when eMMC/SD is used in 4 bit mode. Set 1 for GPIO. Set 0 for eMMC/SD Reset Source: vbus_smod_g_rst_n
29:0	RESERVED	NONE	204FCE5E3E25026110000000h	Reserved

14.7.4.6.2.153 MMCSD_SS_CFG_PHY_CTRL_2_REG Register

14.7.4.6.2.153.1 MMCSD_SS_CFG_PHY_CTRL_2_REG Register (Offset = 104h) [reset = 0h]

The PHY Control 2 Register contains various fields to control the ports on the Arasan eMMC/SD PHY. For detailed functionality of the Arasan eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-13600. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8104h

Figure 14-6712. MMCSD_SS_CFG_PHY_CTRL_2_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
0h							

Table 14-13601. MMCSD_SS_CFG_PHY_CTRL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.154 MMCSD_SS_CFG_PHY_CTRL_3_REG Register

14.7.4.6.2.154.1 MMCSD_SS_CFG_PHY_CTRL_3_REG Register (Offset = 108h) [reset = 0h]

The PHY Control 3 Register contains various fields to control the ports on the Arasan eMMC/SD PHY. For detailed functionality of the Arasan eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-13602. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8108h

Figure 14-6713. MMCSD_SS_CFG_PHY_CTRL_3_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
0h							

Table 14-13603. MMCSD_SS_CFG_PHY_CTRL_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.155 MMCSD_SS_CFG_PHY_CTRL_4_REG Register

14.7.4.6.2.155.1 MMCSD_SS_CFG_PHY_CTRL_4_REG Register (Offset = 10Ch) [reset = 0h]

The PHY Control 4 Register contains various fields to control the ports on the Arasan eMMC/SD PHY. For detailed functionality of the Arasan eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-13604. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 810Ch

Figure 14-6714. MMCSD_SS_CFG_PHY_CTRL_4_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED			OTAPDLYENA	RESERVED			OTAPDLYSEL
NONE			R/W	NONE			R/W
0h			0h	0h			0h
16	15	14	13	12	11	10	9
OTAPDLYSEL				RESERVED		ITAPCHGWIN	ITAPDLYENA
R/W				NONE		R/W	R/W
0h				0h		0h	0h
8	7	6	5	4	3	2	1
RESERVED			ITAPDLYSEL				
NONE			R/W				
0h			0h				

Table 14-13605. MMCSD_SS_CFG_PHY_CTRL_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20	OTAPDLYENA	R/W	0h	Output Tap Delay Enable. Enables manual control of the TX clock tap delay, for clocking the final stage flops for maintaining Hold requirements on EMMC Interface. Reset Source: vbus_smod_g_rst_n
19:17	RESERVED	NONE	0h	Reserved
16:12	OTAPDLYSEL	R/W	0h	Output Tap Delay Select. Manual control of the TX clock tap delay for clocking the final stage flops for maintaining Hold requirements on EMMC Interface. Reset Source: vbus_smod_g_rst_n
11:10	RESERVED	NONE	0h	Reserved
9	ITAPCHGWIN	R/W	0h	Input Tap Change Window. It gets asserted by the controller while changing the itapdlysel. Used to gate of the RX clock during switching the clock source while tap is changing to avoid clock glitches. Reset Source: vbus_smod_g_rst_n
8	ITAPDLYENA	R/W	0h	Input Tap Delay Enable. This is used for the manual control of the RX clock Tap Delay in non HS200/HS400 modes. Reset Source: vbus_smod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved

Table 14-13605. MMCSD_SS_CFG_PHY_CTRL_4_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	ITAPDLYSEL	R/W	0h	Input Tap Delay Select. Manual control of the RX clock Tap Delay in the non HS200/HS400 modes. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.156 MMCSD_SS_CFG_PHY_CTRL_5_REG Register

14.7.4.6.2.156.1 MMCSD_SS_CFG_PHY_CTRL_5_REG Register (Offset = 110h) [reset = 0h]

The PHY Control 5 Register contains various fields to control the ports on the Arasan eMMC/SD PHY. For detailed functionality of the Arasan eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-13606. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8110h

Figure 14-6715. MMCSD_SS_CFG_PHY_CTRL_5_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED					CLKBUFSEL		
NONE					R/W		
0h					0h		

Table 14-13607. MMCSD_SS_CFG_PHY_CTRL_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CLKBUFSEL	R/W	0h	Clock Delay Buffer Select. Selects one of the eight taps in the CLK Delay Buffer based on PVT variation. Reset Source: vbus_smod_g_rst_n

14.7.4.6.2.157 MMCSD_SS_CFG_PHY_CTRL_6_REG Register

14.7.4.6.2.157.1 MMCSD_SS_CFG_PHY_CTRL_6_REG Register (Offset = 114h) [reset = 0h]

The PHY Control 6 Register contains various fields to control the ports on the Arasan eMMC/SD PHY. For detailed functionality of the Arasan eMMC/SD PHY control ports please refer to its specification listed in Section 1.2.

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Table 14-13608. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8114h

Figure 14-6716. MMCSD_SS_CFG_PHY_CTRL_6_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
0h							

Table 14-13609. MMCSD_SS_CFG_PHY_CTRL_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.158 MMCSD_SS_CFG_PHY_STAT_1_REG Register

14.7.4.6.2.158.1 MMCSD_SS_CFG_PHY_STAT_1_REG Register (Offset = 130h) [reset = 0h]

The PHY Status 1 Register contains various fields to reflect the status of the Arasan eMMC/SD PHY ports. For detailed functionality of the Arasan eMMC/SD PHY status ports please refer to its specification listed in Section 1.2.

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Table 14-13610. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8130h

Figure 14-6717. MMCSD_SS_CFG_PHY_STAT_1_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
0h							

Table 14-13611. MMCSD_SS_CFG_PHY_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.4.6.2.159 MMCSD_SS_CFG_PHY_STAT_2_REG Register

14.7.4.6.2.159.1 MMCSD_SS_CFG_PHY_STAT_2_REG Register (Offset = 134h) [reset = 0h]

The PHY Status 2 Register contains various fields to reflect the status of the Arasan eMMC/SD PHY ports. For detailed functionality of the Arasan eMMC/SD PHY status ports please refer to its specification listed in Section 1.2.

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Table 14-13612. Instance Table

Instance Name	Physical Address
MMCSD0	0FA0 8134h

Figure 14-6718. MMCSD_SS_CFG_PHY_STAT_2_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							
NONE							
0h							

Table 14-13613. MMCSD_SS_CFG_PHY_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

14.7.5 Industrial and Control Interfaces Registers

14.7.5.1 MCAN

MCAN

14.7.5.1.1 MCAN Summaries

MCAN Summaries

Table 14-13614. MCAN Registers, Base Address=2070 0000h, Length=256

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	MCAN_PID	2070 0000h	2071 0000h	2072 0000h
4h	32	MCAN_CTRL	2070 0004h	2071 0004h	2072 0004h
8h	32	MCAN_STAT	2070 0008h	2071 0008h	2072 0008h
Ch	32	MCAN_ICS	2070 000Ch	2071 000Ch	2072 000Ch
10h	32	MCAN_IRS	2070 0010h	2071 0010h	2072 0010h
14h	32	MCAN_IECS	2070 0014h	2071 0014h	2072 0014h
18h	32	MCAN_IE	2070 0018h	2071 0018h	2072 0018h
1Ch	32	MCAN_IES	2070 001Ch	2071 001Ch	2072 001Ch
20h	32	MCAN_EOI	2070 0020h	2071 0020h	2072 0020h
24h	32	MCAN_EXT_TS_PRESCALER	2070 0024h	2071 0024h	2072 0024h
28h	32	MCAN_EXT_TS_UNSERVICED_INTR_CNTR	2070 0028h	2071 0028h	2072 0028h

Table 14-13615. MCAN Registers, Base Address=2070 0000h, Length=256

Offset	Length	Register Name	MCAN3 Physical Address	MCAN4 Physical Address
0h	32	MCAN_PID	2073 0000h	2074 0000h
4h	32	MCAN_CTRL	2073 0004h	2074 0004h
8h	32	MCAN_STAT	2073 0008h	2074 0008h
Ch	32	MCAN_ICS	2073 000Ch	2074 000Ch
10h	32	MCAN_IRS	2073 0010h	2074 0010h
14h	32	MCAN_IECS	2073 0014h	2074 0014h
18h	32	MCAN_IE	2073 0018h	2074 0018h
1Ch	32	MCAN_IES	2073 001Ch	2074 001Ch
20h	32	MCAN_EOI	2073 0020h	2074 0020h
24h	32	MCAN_EXT_TS_PRESCALER	2073 0024h	2074 0024h
28h	32	MCAN_EXT_TS_UNSERVICED_INTR_CNTR	2073 0028h	2074 0028h

14.7.5.1.1.1 ECAP_CTL_STS_TSCNT Register

14.7.5.1.1.1.1 ECAP_CTL_STS_TSCNT Register (Offset = 0h) [reset = 0h]

Time Stamp Counter Register

Table 14-13616. Instance Table

Instance Name	Physical Address
ECAP0	2310 0000h
ECAP1	2311 0000h
ECAP2	2312 0000h
ECAP3	2313 0000h
ECAP4	2314 0000h
ECAP5	2315 0000h

Figure 14-6719. ECAP_CTL_STS_TSCNT Name Register

32	31	30	29	28	27	26	25
TSCNT							
R/W							
0h							
24	23	22	21	20	19	18	17
TSCNT							
R/W							
0h							
16	15	14	13	12	11	10	9
TSCNT							
R/W							
0h							
8	7	6	5	4	3	2	1
TSCNT							
R/W							
0h							

Table 14-13617. ECAP_CTL_STS_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSCNT	R/W	0h	Active 32 bit Counter register which is used as the Capture time-base Reset Source: vbus_rst_mod_g_rst_n

Table 14-13618. MCAN_MSGMEM_RAM Registers, Base Address=2070 8000h, Length=32768

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	MCAN_MSGMEM_RAM_RAM_REG_J	2070 8000h + formula	2071 8000h + formula	2072 8000h + formula

Table 14-13619. MCAN_MSGMEM_RAM Registers, Base Address=2070 8000h, Length=32768

Offset	Length	Register Name	MCAN3 Physical Address	MCAN4 Physical Address
0h	32	MCAN_MSGMEM_RAM_RAM_REG_J	2073 8000h + formula	2074 8000h + formula

Table 14-13620. ECC_AGGR Registers, Base Address=2401 8000h, Length=1024

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	ECC_AGGR_REV	2401 8000h	2401 9000h	2401 A000h
8h	32	ECC_AGGR_VECTOR	2401 8008h	2401 9008h	2401 A008h
Ch	32	ECC_AGGR_STAT	2401 800Ch	2401 900Ch	2401 A00Ch
3Ch	32	ECC_AGGR_SEC_EOI_REG	2401 803Ch	2401 903Ch	2401 A03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	2401 8040h	2401 9040h	2401 A040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	2401 8080h	2401 9080h	2401 A080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	2401 80C0h	2401 90C0h	2401 A0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	2401 813Ch	2401 913Ch	2401 A13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	2401 8140h	2401 9140h	2401 A140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	2401 8180h	2401 9180h	2401 A180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	2401 81C0h	2401 91C0h	2401 A1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	2401 8200h	2401 9200h	2401 A200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	2401 8204h	2401 9204h	2401 A204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	2401 8208h	2401 9208h	2401 A208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	2401 820Ch	2401 920Ch	2401 A20Ch

Table 14-13621. ECC_AGGR Registers, Base Address=2401 8000h, Length=1024

Offset	Length	Register Name	MCAN3 Physical Address	MCAN4 Physical Address
0h	32	ECC_AGGR_REV	2401 B000h	2401 C000h
8h	32	ECC_AGGR_VECTOR	2401 B008h	2401 C008h
Ch	32	ECC_AGGR_STAT	2401 B00Ch	2401 C00Ch
3Ch	32	ECC_AGGR_SEC_EOI_REG	2401 B03Ch	2401 C03Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	2401 B040h	2401 C040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	2401 B080h	2401 C080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	2401 B0C0h	2401 C0C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	2401 B13Ch	2401 C13Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	2401 B140h	2401 C140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	2401 B180h	2401 C180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	2401 B1C0h	2401 C1C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	2401 B200h	2401 C200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	2401 B204h	2401 C204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	2401 B208h	2401 C208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	2401 B20Ch	2401 C20Ch

14.7.5.1.2 MCAN Registers

MCAN Registers

14.7.5.1.2.1 MCAN_PID Register

14.7.5.1.2.1.1 MCAN_PID Register (Offset = 0h) [reset = 68E05901h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-13622. Instance Table

Instance Name	Physical Address
MCAN0	2070 0000h
MCAN1	2071 0000h
MCAN2	2072 0000h
MCAN3	2073 0000h
MCAN4	2074 0000h

Figure 14-6720. MCAN_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		8E0h			

23	22	21	20	19	18	17	16
MODULE_ID							
R							
8E0h							

15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Bh					1h		

7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 14-13623. MCAN_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: hsrst_n
29:28	BU	R	2h	Business Unit 2h Processors
27:16	MODULE_ID	R	8E0h	Module ID Reset Source: hsrst_n
15:11	RTL	R	Bh	RTL Revision Reset Source: hsrst_n
10:8	MAJOR	R	1h	Major Revision Reset Source: hsrst_n
7:6	CUSTOM	R	0h	Custom Reset Source: hsrst_n
5:0	MINOR	R	1h	Minor Revision Reset Source: hsrst_n

14.7.5.1.2.2 MCAN_CTRL Register

14.7.5.1.2.2.1 MCAN_CTRL Register (Offset = 4h) [reset = 8h]

The Control Register contains general control bits for the MCANSS

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Table 14-13624. Instance Table

Instance Name	Physical Address
MCAN0	2070 0004h
MCAN1	2071 0004h
MCAN2	2072 0004h
MCAN3	2073 0004h
MCAN4	2074 0004h

Figure 14-6721. MCAN_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREQEN	DBGSUSP_FREE	RESERVED		
NONE	R/W	R/W	R/W	R/W	NONE		
0h	0h	0h	0h	1h	0h		

Table 14-13625. MCAN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	EXT_TS_CNTR_EN	R/W	0h	External Timestamp Counter Enable Reset Source: hsrst_n
5	AUTOWAKEUP	R/W	0h	Automatic Wakeup Enable Reset Source: hsrst_n
4	WAKEUPREQEN	R/W	0h	Wakeup Request Enable Reset Source: hsrst_n

3	DBGSUSP_FREE	R/W	1h	Debug Suspend
				`0h Honor debug suspend`
				`1h Disregard debug suspend`

2:0	RESERVED	NONE	0h	Reserved

14.7.5.1.2.3 MCAN_STAT Register

14.7.5.1.2.3.1 MCAN_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the MCANSS

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Table 14-13626. Instance Table

Instance Name	Physical Address
MCAN0	2070 0008h
MCAN1	2071 0008h
MCAN2	2072 0008h
MCAN3	2073 0008h
MCAN4	2074 0008h

Figure 14-6722. MCAN_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_FDOE	MEM_INIT_DONE	RESERVED
NONE					R	R	NONE
0h					0h	0h	0h

Table 14-13627. MCAN_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	ENABLE_FDOE	R	0h	Enable FD (Flexible Data-Rate) Configuration Reflects the value of mcanss_enable_fdoe configuration port, `xh      mcanss_enable_fdoe.`

1	MEM_INIT_DONE	R	0h	Memory Initialization
				`0h      Memory initialization is in progress`
				`1h      Memory intialization done`

0	RESERVED	NONE	0h	Reserved

14.7.5.1.2.4 MCAN_ICS Register

14.7.5.1.2.4.1 MCAN_ICS Register (Offset = Ch) [reset = 0h]

Write to clear interrupt bits

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Table 14-13628. Instance Table

Instance Name	Physical Address
MCAN0	2070 000Ch
MCAN1	2071 000Ch
MCAN2	2072 000Ch
MCAN3	2073 000Ch
MCAN4	2074 000Ch

Figure 14-6723. MCAN_ICS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							W
0h							0h

Table 14-13629. MCAN_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	W	0h	External Timestamp Counter Overflow Interrupt Status Write 1h to clear bits. Reset Source: hsrst_n

14.7.5.1.2.5 MCAN_IRS Register

14.7.5.1.2.5.1 MCAN_IRS Register (Offset = 10h) [reset = 0h]

Read raw interrupt status. Write '1' to set interrupt bits.

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Table 14-13630. Instance Table

Instance Name	Physical Address
MCAN0	2070 0010h
MCAN1	2071 0010h
MCAN2	2072 0010h
MCAN3	2073 0010h
MCAN4	2074 0010h

Figure 14-6724. MCAN_IRS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							R/W1TS
0h							0h

Table 14-13631. MCAN_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R/W1TS	0h	External Timestamp Counter Overflow Interrupt Status Write 1h to set bits. Reset Source: hsrst_n

14.7.5.1.2.6 MCAN_IECS Register

14.7.5.1.2.6.1 MCAN_IECS Register (Offset = 14h) [reset = 0h]

Write to clear interrupt enable bits

Return to Summary Table

Table 14-13632. Instance Table

Instance Name	Physical Address
MCAN0	2070 0014h
MCAN1	2071 0014h
MCAN2	2072 0014h
MCAN3	2073 0014h
MCAN4	2074 0014h

Figure 14-6725. MCAN_IECS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EXT_TS_CNTR_OVFL</td></tr>
<tr><td colspan="7">NONE</td><td>W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13633. MCAN_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	W1TC	0h	External Timestamp Counter Overflow Interrupt Write 1h to clear bits. Reset Source: hsrst_n

14.7.5.1.2.7 MCAN_IE Register

14.7.5.1.2.7.1 MCAN_IE Register (Offset = 18h) [reset = 0h]

Read interrupt Enable

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Table 14-13634. Instance Table

Instance Name	Physical Address
MCAN0	2070 0018h
MCAN1	2071 0018h
MCAN2	2072 0018h
MCAN3	2073 0018h
MCAN4	2074 0018h

Figure 14-6726. MCAN_IE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							R/W1TS
0h							0h

Table 14-13635. MCAN_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R/W1TS	0h	External Timestamp Counter Overflow Interrupt Write 1h to set bits. Reset Source: hsrst_n

14.7.5.1.2.8 MCAN_IES Register

14.7.5.1.2.8.1 MCAN_IES Register (Offset = 1Ch) [reset = 0h]

Read Enabled Interrupts

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Table 14-13636. Instance Table

Instance Name	Physical Address
MCAN0	2070 001Ch
MCAN1	2071 001Ch
MCAN2	2072 001Ch
MCAN3	2073 001Ch
MCAN4	2074 001Ch

Figure 14-6727. MCAN_IES Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
NONE							R
0h							0h

Table 14-13637. MCAN_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EXT_TS_CNTR_OVFL	R	0h	External Timestamp Counter Overflow Interrupt Reset Source: hsrst_n

14.7.5.1.2.9 MCAN_EOI Register

14.7.5.1.2.9.1 MCAN_EOI Register (Offset = 20h) [reset = 0h]

End of Interrupt Register

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Table 14-13638. Instance Table

Instance Name	Physical Address
MCAN0	2070 0020h
MCAN1	2071 0020h
MCAN2	2072 0020h
MCAN3	2073 0020h
MCAN4	2074 0020h

Figure 14-6728. MCAN_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI							
W							
0h							

Table 14-13639. MCAN_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI	W	0h	End Of Interrupt Write with bit position of the targeted interrupt (example: external timestamp is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1h will issue another pulse interrupt. 0h EOI value for external timestamp interrupt 1h EOI value for mcan[0] interrupt 2h EOI value for mcan[1] interrupt

14.7.5.1.2.10 MCAN_EXT_TS_PRESCALER Register

14.7.5.1.2.10.1 MCAN_EXT_TS_PRESCALER Register (Offset = 24h) [reset = 0h]

External TImeStamp PreScaler

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Table 14-13640. Instance Table

Instance Name	Physical Address
MCAN0	2070 0024h
MCAN1	2071 0024h
MCAN2	2072 0024h
MCAN3	2073 0024h
MCAN4	2074 0024h

Figure 14-6729. MCAN_EXT_TS_PRESCALER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRESCALER							
R/W							
0h							
15	14	13	12	11	10	9	8
PRESCALER							
R/W							
0h							
7	6	5	4	3	2	1	0
PRESCALER							
R/W							
0h							

Table 14-13641. MCAN_EXT_TS_PRESCALER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	PRESCALER	R/W	0h	External Timestamp Prescaler Reload Value External timestamp count rate is host clock rate divided by this value with one exception - a value of 0h has the same effect as 1h. Reset Source: hsrst_n

14.7.5.1.2.11 MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register

14.7.5.1.2.11.1 MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register (Offset = 28h) [reset = 0h]

External TImeStamp Unserviced Interrupts Counter

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Table 14-13642. Instance Table

Instance Name	Physical Address
MCAN0	2070 0028h
MCAN1	2071 0028h
MCAN2	2072 0028h
MCAN3	2073 0028h
MCAN4	2074 0028h

Figure 14-6730. MCAN_EXT_TS_UNSERVICED_INTR_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EXT_TS_INTR_CNTR				
NONE			R				
0h			0h				

Table 14-13643. MCAN_EXT_TS_UNSERVICED_INTR_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	EXT_TS_INTR_CNTR	R	0h	Number of Unserviced Rollover Interrupts If > 1h an EOI write will issue another pulse interrupt. Reset Source: hsrst_n

14.7.5.1.2.12 MMCSD_ECC_AGGR_RXMEM_REV Register

14.7.5.1.2.12.1 MMCSD_ECC_AGGR_RXMEM_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-13644. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8000h

Figure 14-6731. MMCSD_ECC_AGGR_RXMEM_REV Name Register

32	31	30	29	28	27	26	25
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6a0h			
24	23	22	21	20	19	18	17
MODULE_ID							
R							
6a0h							
16	15	14	13	12	11	10	9
REVRTL					REVMAJ		
R					R		
7h					2h		
8	7	6	5	4	3	2	1
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-13645. MMCSD_ECC_AGGR_RXMEM_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6a0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.5.1.2.13 MMCSD_ECC_AGGR_RXMEM_VECTOR Register

14.7.5.1.2.13.1 MMCSD_ECC_AGGR_RXMEM_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-13646. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8008h

Figure 14-6732. MMCSD_ECC_AGGR_RXMEM_VECTOR Name Register

32	31	30	29	28	27	26	25
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
24	23	22	21	20	19	18	17
RD_SVBUS_ADDRESS							
R/W							
0h							
16	15	14	13	12	11	10	9
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
8	7	6	5	4	3	2	1
ECC_VECTOR							
R/W							
0h							

Table 14-13647. MMCSD_ECC_AGGR_RXMEM_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.5.1.2.14 MMCSD_ECC_AGGR_RXMEM_STAT Register

14.7.5.1.2.14.1 MMCSD_ECC_AGGR_RXMEM_STAT Register (Offset = Ch) [reset = 1h]

Misc Status

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Table 14-13648. Instance Table

Instance Name	Physical Address
MMCSD0	0070 800Ch

Figure 14-6733. MMCSD_ECC_AGGR_RXMEM_STAT Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
8	7	6	5	4	3	2	1
NUM_RAMS							
R							
1h							

Table 14-13649. MMCSD_ECC_AGGR_RXMEM_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

14.7.5.1.2.15 MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS Register

14.7.5.1.2.15.1 MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-13650. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8010h

Figure 14-6734. MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS Name Register

32	31	30	29	28	27	26	25
DATA							
R/W							
0h							
24	23	22	21	20	19	18	17
DATA							
R/W							
0h							
16	15	14	13	12	11	10	9
DATA							
R/W							
0h							
8	7	6	5	4	3	2	1
DATA							
R/W							
0h							

Table 14-13651. MMCSD_ECC_AGGR_RXMEM_RESERVED_SVBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.5.1.2.16 MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG Register

14.7.5.1.2.16.1 MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-13652. Instance Table

Instance Name	Physical Address
MMCSD0	0070 803Ch

Figure 14-6735. MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-13653. MMCSD_ECC_AGGR_RXMEM_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.5.1.2.17 MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0 Register

14.7.5.1.2.17.1 MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-13654. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8040h

Figure 14-6736. MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-13655. MMCSD_ECC_AGGR_RXMEM_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for rxmem_pend

14.7.5.1.2.18 MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0 Register

14.7.5.1.2.18.1 MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-13656. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8080h

Figure 14-6737. MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-13657. MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rxmem_pend

14.7.5.1.2.19 MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0 Register

14.7.5.1.2.19.1 MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-13658. Instance Table

Instance Name	Physical Address
MMCSD0	0070 80C0h

Figure 14-6738. MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0 Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="7">RESERVED</td><td>RXMEM_ENABLE_CLR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13659. MMCSD_ECC_AGGR_RXMEM_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rxmem_pend

14.7.5.1.2.20 MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG Register

14.7.5.1.2.20.1 MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

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Table 14-13660. Instance Table

Instance Name	Physical Address
MMCSD0	0070 813Ch

Figure 14-6739. MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-13661. MMCSD_ECC_AGGR_RXMEM_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.5.1.2.21 MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0 Register

14.7.5.1.2.21.1 MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 14-13662. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8140h

Figure 14-6740. MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_PEND
NONE							R/W1TS
0h							0h

Table 14-13663. MMCSD_ECC_AGGR_RXMEM_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_PEND	R/W1TS	0h	Interrupt Pending Status for rxmem_pend

14.7.5.1.2.22 MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0 Register

14.7.5.1.2.22.1 MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-13664. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8180h

Figure 14-6741. MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 14-13665. MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for rxmem_pend

14.7.5.1.2.23 MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0 Register

14.7.5.1.2.23.1 MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-13666. Instance Table

Instance Name	Physical Address
MMCSD0	0070 81C0h

Figure 14-6742. MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0 Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED							RXMEM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 14-13667. MMCSD_ECC_AGGR_RXMEM_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for rxmem_pend

14.7.5.1.2.24 MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET Register

14.7.5.1.2.24.1 MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-13668. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8200h

Figure 14-6743. MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13669. MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.5.1.2.25 MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR Register

14.7.5.1.2.25.1 MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-13670. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8204h

Figure 14-6744. MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-13671. MMCSD_ECC_AGGR_RXMEM_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.5.1.2.26 MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET Register

14.7.5.1.2.26.1 MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-13672. Instance Table

Instance Name	Physical Address
MMCSD0	0070 8208h

Figure 14-6745. MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="2">TIMEOUT</td><td colspan="2">PARITY</td></tr>
<tr><td colspan="4">NONE</td><td colspan="2">R/WI</td><td colspan="2">R/WI</td></tr>
<tr><td colspan="4">0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-13673. MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.5.1.2.27 MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR Register

14.7.5.1.2.27.1 MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-13674. Instance Table

Instance Name	Physical Address
MMCSD0	0070 820Ch

Figure 14-6746. MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-13675. MMCSD_ECC_AGGR_RXMEM_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.7.5.1.2.28 MCAN_MSGMEM_RAM_RAM_REG_J Register

14.7.5.1.2.28.1 MCAN_MSGMEM_RAM_RAM_REG_J Register (Offset = 0h) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

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Table 14-13676. Instance Table

Instance Name	Physical Address
MCAN0	2070 8000h + formula
MCAN1	2071 8000h + formula
MCAN2	2072 8000h + formula
MCAN3	2073 8000h + formula
MCAN4	2074 8000h + formula

Figure 14-6747. MCAN_MSGMEM_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 14-13677. MCAN_MSGMEM_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte Reset Source: rst_mod_g_rst_n
23:16	BYTE2	R/W	0h	This is the UM byte Reset Source: rst_mod_g_rst_n
15:8	BYTE1	R/W	0h	This is the LM byte Reset Source: rst_mod_g_rst_n
7:0	BYTE0	R/W	0h	This is the LS byte Reset Source: rst_mod_g_rst_n

14.7.5.1.2.29 ECC_AGGR_REV Register

14.7.5.1.2.29.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-13678. Instance Table

Instance Name	Physical Address
MCAN0	2401 8000h
MCAN1	2401 9000h
MCAN2	2401 A000h
MCAN3	2401 B000h
MCAN4	2401 C000h

Figure 14-6748. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
7h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 14-13679. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL Version
10:8	REVMAJ	R	2h	Major Version
7:6	CUSTOM	R	0h	Custom Version
5:0	REVMIN	R	1h	Minor Version

14.7.5.1.2.30 ECC_AGGR_VECTOR Register

14.7.5.1.2.30.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-13680. Instance Table

Instance Name	Physical Address
MCAN0	2401 8008h
MCAN1	2401 9008h
MCAN2	2401 A008h
MCAN3	2401 B008h
MCAN4	2401 C008h

Figure 14-6749. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13681. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1TS	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

14.7.5.1.2.31 ECC_AGGR_STAT Register

14.7.5.1.2.31.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 2h]

Misc Status

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Table 14-13682. Instance Table

Instance Name	Physical Address
MCAN0	2401 800Ch
MCAN1	2401 900Ch
MCAN2	2401 A00Ch
MCAN3	2401 B00Ch
MCAN4	2401 C00Ch

Figure 14-6750. ECC_AGGR_STAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 14-13683. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	2h	Number of RAMs Indicates the number of RAMs serviced by the ECC Aggregator.

14.7.5.1.2.32 ECC_AGGR_SEC_EOI_REG Register

14.7.5.1.2.32.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-13684. Instance Table

Instance Name	Physical Address
MCAN0	2401 803Ch
MCAN1	2401 903Ch
MCAN2	2401 A03Ch
MCAN3	2401 B03Ch
MCAN4	2401 C03Ch

Figure 14-6751. ECC_AGGR_SEC_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-13685. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	Single Error Correction End Of Interrupt (SEC EOI)

14.7.5.1.2.33 ECC_AGGR_SEC_STATUS_REG0 Register

14.7.5.1.2.33.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-13686. Instance Table

Instance Name	Physical Address
MCAN0	2401 8040h
MCAN1	2401 9040h
MCAN2	2401 A040h
MCAN3	2401 B040h
MCAN4	2401 C040h

Figure 14-6752. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						CTRL_EDC_VBUSS_PEND	MSGMEM_PEND
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13687. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	R/W1TS	0h	Interrupt Pending Status for CTRL_EDC_VBUSS_PEND
0	MSGMEM_PEND	R/W1TS	0h	Interrupt Pending Status for MSGMEM_PEND

14.7.5.1.2.34 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.7.5.1.2.34.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-13688. Instance Table

Instance Name	Physical Address
MCAN0	2401 8080h
MCAN1	2401 9080h
MCAN2	2401 A080h
MCAN3	2401 B080h
MCAN4	2401 C080h

Figure 14-6753. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CTRL_EDC_VBUSS_ENABLE_SET</td><td>MSGMEM_ENABLE_SET</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13689. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for MSGMEM_PEND

14.7.5.1.2.35 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.7.5.1.2.35.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-13690. Instance Table

Instance Name	Physical Address
MCAN0	2401 80C0h
MCAN1	2401 90C0h
MCAN2	2401 A0C0h
MCAN3	2401 B0C0h
MCAN4	2401 C0C0h

Figure 14-6754. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_CLR	MSGMEM_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-13691. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for MSGMEM_PEND

14.7.5.1.2.36 ECC_AGGR_DED_EOI_REG Register

14.7.5.1.2.36.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-13692. Instance Table

Instance Name	Physical Address
MCAN0	2401 813Ch
MCAN1	2401 913Ch
MCAN2	2401 A13Ch
MCAN3	2401 B13Ch
MCAN4	2401 C13Ch

Figure 14-6755. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-13693. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	Double Error Correction End Of Interrupt (DED EOI)

14.7.5.1.2.37 ECC_AGGR_DED_STATUS_REG0 Register

14.7.5.1.2.37.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-13694. Instance Table

Instance Name	Physical Address
MCAN0	2401 8140h
MCAN1	2401 9140h
MCAN2	2401 A140h
MCAN3	2401 B140h
MCAN4	2401 C140h

Figure 14-6756. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_PEND	MSGMEM_PEND
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13695. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	R/W1TS	0h	Interrupt Pending Status for CTRL_EDC_VBUSS_PEND
0	MSGMEM_PEND	R/W1TS	0h	Interrupt Pending Status for MSGMEM_PEND

14.7.5.1.2.38 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.7.5.1.2.38.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-13696. Instance Table

Instance Name	Physical Address
MCAN0	2401 8180h
MCAN1	2401 9180h
MCAN2	2401 A180h
MCAN3	2401 B180h
MCAN4	2401 C180h

Figure 14-6757. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_SET	MSGMEM_ENABLE_SET
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13697. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set for MSGMEM_PEND

14.7.5.1.2.39 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.7.5.1.2.39.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-13698. Instance Table

Instance Name	Physical Address
MCAN0	2401 81C0h
MCAN1	2401 91C0h
MCAN2	2401 A1C0h
MCAN3	2401 B1C0h
MCAN4	2401 C1C0h

Figure 14-6758. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CTRL_EDC_VBUSS_ENABLE_CLR	MSGMEM_ENABLE_CLR
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-13699. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for CTRL_EDC_VBUSS_PEND
0	MSGMEM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear for MSGMEM_PEND

14.7.5.1.2.40 ECC_AGGR_AGGR_ENABLE_SET Register

14.7.5.1.2.40.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-13700. Instance Table

Instance Name	Physical Address
MCAN0	2401 8200h
MCAN1	2401 9200h
MCAN2	2401 A200h
MCAN3	2401 B200h
MCAN4	2401 C200h

Figure 14-6759. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13701. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt Enable Set for Serial ECC Interface Timeout Errors
0	PARITY	R/W1TS	0h	Interrupt Enable Set for Parity Errors

14.7.5.1.2.41 ECC_AGGR_AGGR_ENABLE_CLR Register

14.7.5.1.2.41.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-13702. Instance Table

Instance Name	Physical Address
MCAN0	2401 8204h
MCAN1	2401 9204h
MCAN2	2401 A204h
MCAN3	2401 B204h
MCAN4	2401 C204h

Figure 14-6760. ECC_AGGR_AGGR_ENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>TIMEOUT</td><td>PARITY</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13703. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt Enable Clear for Serial ECC Interface Timeout Errors
0	PARITY	R/W1TC	0h	Interrupt Enable Clear for Parity Errors

14.7.5.1.2.42 ECC_AGGR_AGGR_STATUS_SET Register

14.7.5.1.2.42.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 14-13704. Instance Table

Instance Name	Physical Address
MCAN0	2401 8208h
MCAN1	2401 9208h
MCAN2	2401 A208h
MCAN3	2401 B208h
MCAN4	2401 C208h

Figure 14-6761. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-13705. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	Interrupt Status Set for Serial ECC Interface Timeout Errors
1:0	PARITY	R/WI	0h	Interrupt Status Set for Parity Errors

14.7.5.1.2.43 ECC_AGGR_AGGR_STATUS_CLR Register

14.7.5.1.2.43.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 14-13706. Instance Table

Instance Name	Physical Address
MCAN0	2401 820Ch
MCAN1	2401 920Ch
MCAN2	2401 A20Ch
MCAN3	2401 B20Ch
MCAN4	2401 C20Ch

Figure 14-6762. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-13707. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	Interrupt Status Clear for Serial ECC Interface Timeout Errors
1:0	PARITY	R/WD	0h	Interrupt Status Clear for Parity Errors

14.7.5.2 ECAP

ECAP

14.7.5.2.1 ECAP Summaries

ECAP Summaries

Table 14-13708. ECAP Registers, Base Address=2310 0000h, Length=256

Offset	Length	Register Name	ECAP0 Physical Address	ECAP1 Physical Address	ECAP2 Physical Address
0h	32	ECAP_TSCNT	2310 0000h	2311 0000h	2312 0000h
4h	32	ECAP_CNTPHS	2310 0004h	2311 0004h	2312 0004h
8h	32	ECAP_CAP1	2310 0008h	2311 0008h	2312 0008h
Ch	32	ECAP_CAP2	2310 000Ch	2311 000Ch	2312 000Ch
10h	32	ECAP_CAP3	2310 0010h	2311 0010h	2312 0010h
14h	32	ECAP_CAP4	2310 0014h	2311 0014h	2312 0014h
28h	32	ECAP_ECCTL	2310 0028h	2311 0028h	2312 0028h
2Ch	32	ECAP_ECINT_EN_FLG	2310 002Ch	2311 002Ch	2312 002Ch
30h	32	ECAP_ECINT_CLR_FRC	2310 0030h	2311 0030h	2312 0030h
5Ch	32	ECAP_PID	2310 005Ch	2311 005Ch	2312 005Ch

Table 14-13709. ECAP Registers, Base Address=2310 0000h, Length=256

Offset	Length	Register Name	ECAP3 Physical Address	ECAP4 Physical Address	ECAP5 Physical Address
0h	32	ECAP_TSCNT	2313 0000h	2314 0000h	2315 0000h
4h	32	ECAP_CNTPHS	2313 0004h	2314 0004h	2315 0004h
8h	32	ECAP_CAP1	2313 0008h	2314 0008h	2315 0008h
Ch	32	ECAP_CAP2	2313 000Ch	2314 000Ch	2315 000Ch
10h	32	ECAP_CAP3	2313 0010h	2314 0010h	2315 0010h
14h	32	ECAP_CAP4	2313 0014h	2314 0014h	2315 0014h
28h	32	ECAP_ECCTL	2313 0028h	2314 0028h	2315 0028h
2Ch	32	ECAP_ECINT_EN_FLG	2313 002Ch	2314 002Ch	2315 002Ch
30h	32	ECAP_ECINT_CLR_FRC	2313 0030h	2314 0030h	2315 0030h
5Ch	32	ECAP_PID	2313 005Ch	2314 005Ch	2315 005Ch

14.7.5.2.2 ECAP Registers

ECAP Registers

14.7.5.2.2.1 ECAP_TSCNT Register

14.7.5.2.2.1.1 ECAP_TSCNT Register (Offset = 0h) [reset = 0h]

Time Stamp Counter Register

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Table 14-13710. Instance Table

Instance Name	Physical Address
ECAP0	2310 0000h
ECAP1	2311 0000h
ECAP2	2312 0000h
ECAP3	2313 0000h
ECAP4	2314 0000h
ECAP5	2315 0000h

Figure 14-6763. ECAP_TSCNT Name Register

31	30	29	28	27	26	25	24
TSCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
TSCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
TSCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
TSCNT							
R/W							
0h							

Table 14-13711. ECAP_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSCNT	R/W	0h	Active 32 bit Counter register which is used as the Capture time-base Reset Source: vbus_rst_mod_g_rst_n

14.7.5.2.2.2 ECAP_CNTPHS Register

14.7.5.2.2.2.1 ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]

Counter Phase Control Register

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Table 14-13712. Instance Table

Instance Name	Physical Address
ECAP0	2310 0004h
ECAP1	2311 0004h
ECAP2	2312 0004h
ECAP3	2313 0004h
ECAP4	2314 0004h
ECAP5	2315 0004h

Figure 14-6764. ECAP_CNTPHS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CNTPHS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CNTPHS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CNTPHS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CNTPHS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13713. ECAP_CNTPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTPHS	R/W	0h	Counter phase value register that can be programmed for phase Lag/Lead. This register shadows the ECAP_TSCNT register and is loaded into the ECAP_TSCNT register upon either a SYNCI event or software force via a control bit. Used to achieve phase control sync with respect to other ECAP and EPWM time-bases. Reset Source: vbus_rst_mod_g_rst_n

14.7.5.2.2.3 ECAP_CAP1 Register

14.7.5.2.2.3.1 ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

Capture-1 Register

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Table 14-13714. Instance Table

Instance Name	Physical Address
ECAP0	2310 0008h
ECAP1	2311 0008h
ECAP2	2312 0008h
ECAP3	2313 0008h
ECAP4	2314 0008h
ECAP5	2315 0008h

Figure 14-6765. ECAP_CAP1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CAP1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CAP1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CAP1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAP1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13715. ECAP_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP1	R/W	0h	This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes/initialisation. 3. APRD shadow register (ECAP_CAP3) when used in APWM mode. Reset Source: vbus_rst_mod_g_rst_n

14.7.5.2.2.4 ECAP_CAP2 Register

14.7.5.2.2.4.1 ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

Capture-2 Register

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Table 14-13716. Instance Table

Instance Name	Physical Address
ECAP0	2310 000Ch
ECAP1	2311 000Ch
ECAP2	2312 000Ch
ECAP3	2313 000Ch
ECAP4	2314 000Ch
ECAP5	2315 000Ch

Figure 14-6766. ECAP_CAP2 Name Register

31	30	29	28	27	26	25	24
CAP2							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP2							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP2							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP2							
R/W							
0h							

Table 14-13717. ECAP_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP2	R/W	0h	This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes. 3. ACMP shadow register (ECAP_CAP4) when used in APWM mode. Reset Source: vbus_rst_mod_g_rst_n

14.7.5.2.2.5 ECAP_CAP3 Register

14.7.5.2.2.5.1 ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

Capture-3 Register

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Table 14-13718. Instance Table

Instance Name	Physical Address
ECAP0	2310 0010h
ECAP1	2311 0010h
ECAP2	2312 0010h
ECAP3	2313 0010h
ECAP4	2314 0010h
ECAP5	2315 0010h

Figure 14-6767. ECAP_CAP3 Name Register

31	30	29	28	27	26	25	24
CAP3							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP3							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP3							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP3							
R/W							
0h							

Table 14-13719. ECAP_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP3	R/W	0h	In CMP mode this is a time-stamp capture register. In APMW mode this is the period shadow (APER) register. User updates the PWM period value via this register. In this mode the ECAP_CAP3 (APRD) register shadows the ECAP_CAP1 register. Reset Source: vbus_rst_mod_g_rst_n

14.7.5.2.2.6 ECAP_CAP4 Register

14.7.5.2.2.6.1 ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

Capture-4 Register

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Table 14-13720. Instance Table

Instance Name	Physical Address
ECAP0	2310 0014h
ECAP1	2311 0014h
ECAP2	2312 0014h
ECAP3	2313 0014h
ECAP4	2314 0014h
ECAP5	2315 0014h

Figure 14-6768. ECAP_CAP4 Name Register

31	30	29	28	27	26	25	24
CAP4							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP4							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP4							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP4							
R/W							
0h							

Table 14-13721. ECAP_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP4	R/W	0h	In CMP mode this is a time-stamp capture register. In APMW mode this is the compare shadow (ACMP) register. User updates the PWM Compare value via this register. In this mode the ECAP_CAP4 (ACMP) register shadows the ECAP_CAP2 register. Reset Source: vbus_rst_mod_g_rst_n

14.7.5.2.2.7 ECAP_ECCTL Register

14.7.5.2.2.7.1 ECAP_ECCTL Register (Offset = 28h) [reset = 60000h]

ECAP Control Register

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Table 14-13722. Instance Table

Instance Name	Physical Address
ECAP0	2310 0028h
ECAP1	2311 0028h
ECAP2	2312 0028h
ECAP3	2313 0028h
ECAP4	2314 0028h
ECAP5	2315 0028h

Figure 14-6769. ECAP_ECCTL Name Register

31	30	29	28	27	26	25	24
FILTER					APWMPOL	CAP_APWM	SWSYNC
R					R/W	R/W	WTC
0h					0h	0h	0h

23	22	21	20	19	18	17	16
SYNCO_SEL		SYNCI_EN	TSCNTSTP	REARM_RESET	STOPVALUE		CONT_ONESHT
R/W		R/W	R/W	WTC	R/W		R/W
0h		0h	0h	0h	3h		0h

15	14	13	12	11	10	9	8
FREE_SOFT		EVTFLTPS					CAPLDEN
R/W		R/W					R/W
0h		0h					0h

7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13723. ECAP_ECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	FILTER	R	0h	Reset Source: vbus_rst_mod_g_rst_n
26	APWMPOL	R/W	0h	APWM Output Polarity Select: Note: This is applicable only in APWM operating mode. Reset Source: vbus_rst_mod_g_rst_n 0h Output is Active High (Compare value defines High time) 1h Output is Active Low (Compare value defines Low time)

Table 14-13723. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CAP_APWM	R/W	0h	CAP/APWM Operating Mode Select: Reset Source: vbus_rst_mod_g_rst_n 0h ECAP module operates in Capture mode. This mode forces the following configuration: 1. Inhibits the ECAP_TSCNT register resets via PRD event. 2. Inhibits the Shadow loads on the ECAP_CAP1 and ECAP_CAP2 registers. 3. Permits user to enable the ECAP_CAP1 to ECAP_CAP4 register load. 4. CAPx/APWMx pin operates as a Capture input. 1h ECAP module operates in APWM mode. This mode forces the following configuration: 1. Resets the ECAP_TSCNT register on PRD event (period boundary) 2. Permits Shadow loading on the ECAP_CAP1 and ECAP_CAP2 registers. 3. Disables loading of Time-stamps into the ECAP_CAP1 - ECAP_CAP4 registers 4. CAPx/APWMx pin operates as a APWM output.
24	SWSYNC	WTC	0h	Software Forced Counter (ECAP_TSCNT) Synchronizing: Reset Source: vbus_rst_mod_g_rst_n 0h Writing a zero has no effect. Reading will always return a zero. 1h Writing a one will force a ECAP_TSCNT shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0h
23:22	SYNCO_SEL	R/W	0h	SyncOut Select: Note: Selection PRD is meaningful only in APWM mode, however can still be chosen in CAP mode if user believes it to be useful. Reset Source: vbus_rst_mod_g_rst_n 0h Select SyncIn event to be the SyncOut signal (pass through) 1h Select PRD event to be the SyncOut signal 2h Disable SyncOut Signal 3h Disable SyncOut Signal
21	SYNCI_EN	R/W	0h	Counter (ECAP_TSCNT) SyncIn select mode: Reset Source: vbus_rst_mod_g_rst_n 0h Disable SyncIn option 1h Enable Counter (ECAP_TSCNT) to be loaded from the ECAP_CNTPHS register upon either a SYNCI signal or a software force event.
20	TSCNTSTP	R/W	0h	Counter Stop (freeze) Control: Reset Source: vbus_rst_mod_g_rst_n 0h Counter Stopped 1h Counter Free Running
19	REARM_RESET	WTC	0h	One-Shot Re-arming Control Wait for stop trigger: Reset Source: vbus_rst_mod_g_rst_n 0h Has no effect. Reading always returns a 0h 1h Arms the One-Shot sequence: 1. Resets the Mod4 counter to zero. 2. Un-freezes the Mod4 counter. 3. Enables Capture Register Loads.

Table 14-13723. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:17	STOPVALUE	R/W	3h	Stop Value for One-Shot Mode: This is the number (between 1 and 4) of captures allowed to occur before the ECAP_CAP1 through ECAP_CAP4 registers are frozen (capture sequence is stopped). Notes: [1] STOPVALUE is compared to Mod4 counter, when equal, two actions occur: 1. Mod4 Counter is stopped (frozen) 2. Capture register loads are inhibited [2] In one shot mode, further interrupt events are blocked until we re-arm, once the number of events captured has been reached. Reset Source: vbus_rst_mod_g_rst_n 0h Stop after Capture Event 1 1h Stop after Capture Event 2 2h Stop after Capture Event 3 3h Stop after Capture Event 4
16	CONT_ONESHT	R/W	0h	Continuous or One-shot Mode Control (applicable only in Capture mode): Reset Source: vbus_rst_mod_g_rst_n 0h Operate in Continuous mode 1h Operate in One-Shot mode
15:14	FREE_SOFT	R/W	0h	Emulation Control Reset Source: vbus_rst_mod_g_rst_n 0h ECAP_TSCNT Counter stops immediately on emulation suspend 1h ECAP_TSCNT Counter runs until = 0h 3h ECAP_TSCNT Counter is unaffected by emulation suspend (Run Free)
13:9	EVTFLTPS	R/W	0h	Event Filter Prescale Select: Reset Source: vbus_rst_mod_g_rst_n 0h Divide by 1 (no prescale, by-pass the prescaler) 1Eh Divide by 60 1Fh Divide by 62 1h Divide by 2 2h Divide by 4 3h Divide by 6 4h Divide by 8 5h Divide by 10
8	CAPLDEN	R/W	0h	Enable Loading of the ECAP_CAP1 to ECAP_CAP4 registers on a capture event: Reset Source: vbus_rst_mod_g_rst_n 0h Disable ECAP_CAP1 to ECAP_CAP4 register loads at capture event time. 1h Enable ECAP_CAP1 to ECAP_CAP4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4: Reset Source: vbus_rst_mod_g_rst_n 0h Do Not reset Counter on Capture Event 4 (absolute time stamp) 1h Reset counter after Event 4 time-stamp has been captured (used in Difference mode operation)
6	CAP4POL	R/W	0h	Capture Event 4 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 4 triggered on a Rising Edge (RE) 1h Capture event 4 triggered on a Falling Edge (FE)

Table 14-13723. ECAP_ECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 3 (absolute time stamp) 1h Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 3 triggered on a Rising Edge (RE) 1h Capture event 3 triggered on a Falling Edge (FE)
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 2 (absolute time stamp) 1h Reset Counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 2 triggered on a Rising Edge (RE) 1h Capture event 2 triggered on a Falling Edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1: Reset Source: vbus_rst_mod_g_rst_n 0h Do not reset counter on Capture Event 1 (absolute time stamp) 1h Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity Select: Reset Source: vbus_rst_mod_g_rst_n 0h Capture event 1 triggered on a Rising Edge (RE) 1h Capture event 1 triggered on a Falling Edge (FE)

14.7.5.2.2.8 ECAP_ECINT_EN_FLG Register

14.7.5.2.2.8.1 ECAP_ECINT_EN_FLG Register (Offset = 2Ch) [reset = 0h]

ECAP Interrupt Enable and Flag Register

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Table 14-13724. Instance Table

Instance Name	Physical Address
ECAP0	2310 002Ch
ECAP1	2311 002Ch
ECAP2	2312 002Ch
ECAP3	2313 002Ch
ECAP4	2314 002Ch
ECAP5	2315 002Ch

Figure 14-6770. ECAP_ECINT_EN_FLG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CMPEQ_FLG	PRDEQ_FLG	CNTOVF_FLG	CEVT4_FLG	CEVT3_FLG	CEVT2_FLG	CEVT1_FLG	INT_FLG
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CMPEQ_EN	PRDEQ_EN	CNTOVF_EN	CEVT4_EN	CEVT3_EN	CEVT2_EN	CEVT1_EN	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13725. ECAP_ECINT_EN_FLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	CMPEQ_FLG	R	0h	Compare Equal Status Flag: Note: This flag is only active in APWM mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred 1h Indicates the counter (ECAP_TSCNT) reached the Compare register value (ACMP)
22	PRDEQ_FLG	R	0h	Period Equal Status Flag: Note: This flag is only active in APWM mode. Reset Source: vbus_rst_mod_g_rst_n 0h Indicates no event occurred 1h Indicates the Counter (ECAP_TSCNT) reached the Period register value (APER) and was reset.

Table 14-13725. ECAP_ECINT_EN_FLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

21	CNTOVF_FLG	R	0h	Counter Overflow Status Flag:
				Note: This flag is active in CAP and APWM mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Indicates no event occurred.`
				`1h` `Indicates the Counter (ECAP_TSCNT) has made the transition from FFFF FFFFh to 0000 0000h`

20	CEVT4_FLG	R	0h	Capture Event 4 Status Flag:
				Note: This flag is only active in CAP mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Indicates no event occurred.`
				`1h` `Indicates the fourth event occurred at ECAPx pin.`

19	CEVT3_FLG	R	0h	Capture Event 3 Status Flag:
				Note: This flag is only active in CAP mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Indicates no event occurred.`
				`1h` `Indicates the third event occurred at ECAPx pin.`

18	CEVT2_FLG	R	0h	Capture Event 2 Status Flag:
				Note: This flag is only active in CAP mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Indicates no event occurred.`
				`1h` `Indicates the second event occurred at ECAPx pin.`

17	CEVT1_FLG	R	0h	Capture Event 1 Status Flag:
				Note: This flag is only active in CAP mode.
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Indicates no event occurred.`
				`1h` `Indicates the first event occurred at ECAPx pin.`

16	INT_FLG	R	0h	Global Interrupt Status Flag:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Indicates no interrupt generated.`
				`1h` `Indicates that an interrupt was generated from one of the following events.`

15:8	RESERVED	NONE	0h	Reserved

7	CMPEQ_EN	R/W	0h	Compare Equal Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Compare Equal as an Interrupt source`
				`1h` `Enable Compare Equal as an Interrupt source`

6	PRDEQ_EN	R/W	0h	Period Equal Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Period Equal as an Interrupt source`
				`1h` `Enable Period Equal as an Interrupt source`

5	CNTOVF_EN	R/W	0h	Counter Overflow Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Counter Overflow as an Interrupt source`
				`1h` `Enable Counter Overflow as an Interrupt source`

Table 14-13725. ECAP_ECINT_EN_FLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

4	CEVT4_EN	R/W	0h	Capture Event 4 Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Capture Event 4 as an Interrupt source:`
				`1h` `Enable Capture Event 4 as an Interrupt source`

3	CEVT3_EN	R/W	0h	Capture Event 3 Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Capture Event 3 as an Interrupt source:`
				`1h` `Enable Capture Event 3 as an Interrupt source`

2	CEVT2_EN	R/W	0h	Capture Event 2 Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Capture Event 2 as an Interrupt source:`
				`1h` `Enable Capture Event 2 as an Interrupt source`

1	CEVT1_EN	R/W	0h	Capture Event 1 Interrupt Enable:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h` `Disabled Capture Event 1 as an Interrupt source:`
				`1h` `Enable Capture Event 1 as an Interrupt source`

0	RESERVED	NONE	0h	Reserved

14.7.5.2.2.9 ECAP_ECINT_CLR_FRC Register

14.7.5.2.2.9.1 ECAP_ECINT_CLR_FRC Register (Offset = 30h) [reset = 0h]

ECAP Interrupt Clear and Forcing Register

Return to Summary Table

Table 14-13726. Instance Table

Instance Name	Physical Address
ECAP0	2310 0030h
ECAP1	2311 0030h
ECAP2	2312 0030h
ECAP3	2313 0030h
ECAP4	2314 0030h
ECAP5	2315 0030h

Figure 14-6771. ECAP_ECINT_CLR_FRC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CMPEQ_FRC	PRDEQ_FRC	CNTOVF_FRC	CEVT4_FRC	CEVT3_FRC	CEVT2_FRC	CEVT1_FRC	RESERVED
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	NONE
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CMPEQ_CLR	PRDEQ_CLR	CNTOVF_CLR	CEVT4_CLR	CEVT3_CLR	CEVT2_CLR	CEVT1_CLR	INT_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13727. ECAP_ECINT_CLR_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

23	CMPEQ_FRC	W1TS	0h	Force Compare Equal:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h No effect. Always reads back a 0h`
				`1h Writing a 1h to this bit will set the CMPEQ_FLG flag bit.`

22	PRDEQ_FRC	W1TS	0h	Force Period Equal:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h No effect. Always reads back a 0.`
				`1h Writing a 1h to this bit will set the PRDEQ_FLG flag bit.`

21	CNTOVF_FRC	W1TS	0h	Force Counter Overflow:
				Reset Source: vbus_rst_mod_g_rst_n
				`0h No effect. Always reads back a 0.`
				`1h Writing a 1h to this bit will set the CNTOVF_FLG flag bit.`

Table 14-13727. ECAP_ECINT_CLR_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	CEVT4_FRC	W1TS	0h	Force Capture Event 4: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h to this bit will set the CEVT4_FLG flag bit.
19	CEVT3_FRC	W1TS	0h	Force Capture Event 3: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h to this bit will set the CEVT3_FLG flag bit.
18	CEVT2_FRC	W1TS	0h	Force Capture Event 2: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h to this bit will set the CEVT2_FLG flag bit.
17	CEVT1_FRC	W1TS	0h	Force Capture Event 1: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h to this bit will set the CEVT1_FLG flag bit.
16:8	RESERVED	NONE	0h	Reserved
7	CMPEQ_CLR	W1TC	0h	Compare Equal Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CMPEQ_FLG flag condition.
6	PRDEQ_CLR	W1TC	0h	Period Equal Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the PRDEQ_FLG flag condition.
5	CNTOVF_CLR	W1TC	0h	Counter Overflow Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CNTOVF_FLG flag condition.
4	CEVT4_CLR	W1TC	0h	Capture Event 4 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT4_FLG flag condition.
3	CEVT3_CLR	W1TC	0h	Capture Event 3 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT3_FLG flag condition.
2	CEVT2_CLR	W1TC	0h	Capture Event 2 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT2_FLG flag condition.

Table 14-13727. ECAP_ECINT_CLR_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1_CLR	W1TC	0h	Capture Event 1 Status Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the CEVT1_FLG flag condition.
0	INT_CLR	W1TC	0h	Global Interrupt Clear Flag: Reset Source: vbus_rst_mod_g_rst_n 0h No effect. Always reads back a 0. 1h Writing a 1h will clear the INT_FLG flag and enable further interrupts to be generated if any of the event flags are set to 1h.

14.7.5.2.2.10 ECAP_PID Register

14.7.5.2.2.10.1 ECAP_PID Register (Offset = 5Ch) [reset = 44D24100h]

Peripheral ID Register

Return to Summary Table

Table 14-13728. Instance Table

Instance Name	Physical Address
ECAP0	2310 005Ch
ECAP1	2311 005Ch
ECAP2	2312 005Ch
ECAP3	2313 005Ch
ECAP4	2314 005Ch
ECAP5	2315 005Ch

Figure 14-6772. ECAP_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">RESERVED</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">0h</td><td colspan="4">4D2h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">4D2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">8h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-13729. ECAP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Reset Source: vbus_rst_mod_g_rst_n
29:28	RESERVED	R	0h	
27:16	FUNCTION	R	4D2h	Reset Source: vbus_rst_mod_g_rst_n
15:11	RTL	R	8h	Reset Source: vbus_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Reset Source: vbus_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Reset Source: vbus_rst_mod_g_rst_n
5:0	MINOR	R	0h	Reset Source: vbus_rst_mod_g_rst_n

14.7.5.3 EPWM

EPWM

14.7.5.3.1 EPWM Summaries

EPWM Summaries

Table 14-13730. EPWM Registers, Base Address=2300 0000h, Length=256

Offset	Length	Register Name	EPWM0 Physical Address	EPWM1 Physical Address	EPWM2 Physical Address
0h	16	EPWM_TBCTL	2300 0000h	2301 0000h	2302 0000h
2h	16	EPWM_TBSTS	2300 0002h	2301 0002h	2302 0002h
4h	16	EPWM_TBPHSHR	2300 0004h	2301 0004h	2302 0004h
6h	16	EPWM_TBPHS	2300 0006h	2301 0006h	2302 0006h
8h	16	EPWM_TBCNT	2300 0008h	2301 0008h	2302 0008h
Ah	16	EPWM_TBPRD	2300 000Ah	2301 000Ah	2302 000Ah
Eh	16	EPWM_CMPCTL	2300 000Eh	2301 000Eh	2302 000Eh
10h	16	EPWM_CMPAHR	2300 0010h	2301 0010h	2302 0010h
12h	16	EPWM_CMPA	2300 0012h	2301 0012h	2302 0012h
14h	16	EPWM_CMPB	2300 0014h	2301 0014h	2302 0014h
16h	16	EPWM_AQCTLA	2300 0016h	2301 0016h	2302 0016h
18h	16	EPWM_AQCTLB	2300 0018h	2301 0018h	2302 0018h
1Ah	16	EPWM_AQSFRC	2300 001Ah	2301 001Ah	2302 001Ah
1Ch	16	EPWM_AQCSFRC	2300 001Ch	2301 001Ch	2302 001Ch
1Eh	16	EPWM_DBCTL	2300 001Eh	2301 001Eh	2302 001Eh
20h	16	EPWM_DBRED	2300 0020h	2301 0020h	2302 0020h
22h	16	EPWM_DBFED	2300 0022h	2301 0022h	2302 0022h
24h	16	EPWM_TZSEL	2300 0024h	2301 0024h	2302 0024h
28h	16	EPWM_TZCTL	2300 0028h	2301 0028h	2302 0028h
2Ah	16	EPWM_TZEINT	2300 002Ah	2301 002Ah	2302 002Ah
2Ch	16	EPWM_TZFLG	2300 002Ch	2301 002Ch	2302 002Ch
2Eh	16	EPWM_TZCLR	2300 002Eh	2301 002Eh	2302 002Eh
30h	16	EPWM_TZFRC	2300 0030h	2301 0030h	2302 0030h
32h	16	EPWM_ETSEL	2300 0032h	2301 0032h	2302 0032h
34h	16	EPWM_ETPS	2300 0034h	2301 0034h	2302 0034h
36h	16	EPWM_ETFLG	2300 0036h	2301 0036h	2302 0036h
38h	16	EPWM_ETCLR	2300 0038h	2301 0038h	2302 0038h
3Ah	16	EPWM_ETFRC	2300 003Ah	2301 003Ah	2302 003Ah
3Ch	16	EPWM_PCCTL	2300 003Ch	2301 003Ch	2302 003Ch
5Ch	32	EPWM_PID	2300 005Ch	2301 005Ch	2302 005Ch

14.7.5.3.2 EPWM Registers

EPWM Registers

14.7.5.3.2.1 EPWM_TBCTL Register

14.7.5.3.2.1.1 EPWM_TBCTL Register (Offset = 0h) [reset = 83h]

Time-Base Control Register

Return to Summary Table

Table 14-13731. Instance Table

Instance Name	Physical Address
EPWM0	2300 0000h
EPWM1	2301 0000h
EPWM2	2302 0000h

Figure 14-6773. EPWM_TBCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR	CLKDIV			HSPCLKDIV	
R/W		R/W	R/W			R/W	
0h		0h	0h			1h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSPCLKDIV	SWFSYNC	SYNCOSEL		PRDLD	PHSEN	CTRMODE	
R/W	R/W	R/W		R/W	R/W	R/W	
1h	0h	0h		0h	0h	3h	

Table 14-13732. EPWM_TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation Mode Bits These bits select the behavior of the ePWM time-base counter during emulation events: 0h Stop after the next time-base counter increment or decrement 1h Stop when counter completes a whole cycle (a) Up-count mode: stop when the time-base counter = period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD). (b) Down-count mode: stop when the time-base counter = 0000 (EPWM_TBCNT[15-0] TBCNT = 0000h) 2h Free run 3h Free run
13	PHSDIR	R/W	0h	Phase Direction Bit This bit is only used when the time-base counter is configured in the up-down-count mode The PHSDIR bit indicates the direction the time-base counter [TBCNT] will count after a synchronization event occurs and a new phase value is loaded from the phase [TBPHS] register This is irrespective of the direction of the counter before the synchronization event In the up-count and down-count modes this bit is ignored 0h Count down after the synchronization event 1h Count up after the synchronization event
12:10	CLKDIV	R/W	0h	Time-base Clock Prescale Bits These bits determine part of the time-base clock prescale value TBCLK = SYSCLKOUT/[HSPCLKDIV - CLKDIV] 0h /1 (default on reset) 1h /2 2h /4 3h /8 4h /16 5h /32 6h /64 7h /128

Table 14-13732. EPWM_TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:7	HSPCLKDIV	R/W	1h	High-Speed Time-base Clock Prescale Bits These bits determine part of the time-base clock prescale value TBCLK = SYSCLKOUT/[HSPCLKDIV - CLKDIV] This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager [EV] peripheral 0h /1 1h /2 (default on reset) 2h /4 3h /6 4h /8 5h /10 6h /12 7h /14
6	SWFSYNC	R/W	0h	Software Forced Synchronization Pulse 0h Writing a 0h 1h Writing a 1h
5:4	SYNCOSEL	R/W	0h	Synchronization Output Select These bits select the source of the EPWMxSYNCO signal 0h EPWMxSYNC 1h TBCNT = 0: Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h) 2h TBCNT = CMPB: Time-base counter equal to counter-compare B (EPWM_TBCNT[15-0] TBCNT = EPWM_CMPB[15-0] CMPB) 3h Disable EPWMxSYNCO signal
3	PRDLD	R/W	0h	Active Period Register Load From Shadow Register Select 0h The period register (EPWM_TBPRD) is loaded from its shadow register when the time-base counter, EPWM_TBCNT[15-0] TBCNT, is equal to zero. A write or read to the EPWM_TBPRD register accesses the shadow register. 1h Load the EPWM_TBPRD register immediately without using a shadow register. A write or read to the EPWM_TBPRD register directly accesses the active register.
2	PHSEN	R/W	0h	Counter Register Load From Phase Register Enable 0h Do not load the time-base counter (EPWM_TBCNT) from the time-base phase register (EPWM_TBPHS) 1h Load the time-base counter with the phase register when an EPWMxSYNCI input signal occurs or when a software synchronization is forced by the SWFSYNC bit.
1:0	CTRMODE	R/W	3h	Counter Mode The time-base counter mode is normally configured once and not changed during normal operation If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change These bits set the time-base counter mode of operation as follows: 0h Up-count mode 1h Down-count mode 2h Up-down-count mode 3h Stop-freeze counter operation (default on reset)

14.7.5.3.2.2 EPWM_TBSTS Register

14.7.5.3.2.2.1 EPWM_TBSTS Register (Offset = 2h) [reset = 0h]

Time-Base Status Register

Return to Summary Table

Table 14-13733. Instance Table

Instance Name	Physical Address
EPWM0	2300 0002h
EPWM1	2301 0002h
EPWM2	2302 0002h

Figure 14-6774. EPWM_TBSTS Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED1</td><td>CTRMAX</td><td>SYNCI</td><td>CTRDIR</td></tr>
<tr><td colspan="5">R</td><td>R/W1TC</td><td>R/W1TC</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13734. EPWM_TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	CTRMAX	R/W1TC	0h	Time-Base Counter Max Latched Status Bit 0h `Reading a 0h` 1h `Reading a 1h`
1	SYNCI	R/W1TC	0h	Input Synchronization Latched Status Bit 0h `Writing a 0h` 1h `Reading a 1h`
0	CTRDIR	R	0h	Time-Base Counter Direction Status Bit At reset, the counter is frozen, therefore, this bit has no meaning To make this bit meaningful, you must first set the appropriate mode via TBCTL[CTRMODE] 0h `Time-Base Counter is currently counting down` 1h `Time-Base Counter is currently counting up`

14.7.5.3.2.3 EPWM_TBPHSHR Register

14.7.5.3.2.3.1 EPWM_TBPHSHR Register (Offset = 4h) [reset = 0h]

Time Base Phase High Resolution Register

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Table 14-13735. Instance Table

Instance Name	Physical Address
EPWM0	2300 0004h
EPWM1	2301 0004h
EPWM2	2302 0004h

Figure 14-6775. EPWM_TBPHSHR Name Register

15	14	13	12	11	10	9	8
TBPHSH							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1							
R							
0h							

Table 14-13736. EPWM_TBPHSHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TBPHSH	R/W	0h	Time-base phase high-resolution bits
7:0	RESERVED1	R	0h	Reserved

14.7.5.3.2.4 EPWM_TBPHS Register

14.7.5.3.2.4.1 EPWM_TBPHS Register (Offset = 6h) [reset = 0h]

Time Base Phase Register. This register is only available on ePWM instances that include the high-resolution PWM (HRPWM) extension, otherwise, this location is reserved.

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Table 14-13737. Instance Table

Instance Name	Physical Address
EPWM0	2300 0006h
EPWM1	2301 0006h
EPWM2	2302 0006h

Figure 14-6776. EPWM_TBPHS Name Register

15	14	13	12	11	10	9	8
TBPHS							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBPHS							
R/W							
0h							

Table 14-13738. EPWM_TBPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBPHS	R/W	0h	These bits set time-base counter phase of the selected ePWM relative to the time-base that is supplying the synchronization input signal [a] If TBCTL[PHSEN] = 0, then the synchronization event is ignored and the time-base counter is not loaded with the phase [b] If TBCTL[PHSEN] = 1, then the time-base counter [TBCNT] will be loaded with the phase [TBPHS] when a synchronization event occurs The synchronization event can be initiated by the input synchronization signal [EPWMxSYNCI] or by a software forced synchronization

14.7.5.3.2.5 EPWM_TBCNT Register

14.7.5.3.2.5.1 EPWM_TBCNT Register (Offset = 8h) [reset = 0h]

Time Base Counter Register

Return to Summary Table

Table 14-13739. Instance Table

Instance Name	Physical Address
EPWM0	2300 0008h
EPWM1	2301 0008h
EPWM2	2302 0008h

Figure 14-6777. EPWM_TBCNT Name Register

15	14	13	12	11	10	9	8
TBCNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBCNT							
R/W							
0h							

Table 14-13740. EPWM_TBCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBCNT	R/W	0h	Reading these bits gives the current time-base counter value Writing to these bits sets the current time-base counter value The update happens as soon as the write occurs The write is NOT synchronized to the time-base clock [TBCLK] and the register is not shadowed

14.7.5.3.2.6 EPWM_TBPRD Register

14.7.5.3.2.6.1 EPWM_TBPRD Register (Offset = Ah) [reset = 0h]

Time Base Period Register

Return to Summary Table

Table 14-13741. Instance Table

Instance Name	Physical Address
EPWM0	2300 000Ah
EPWM1	2301 000Ah
EPWM2	2302 000Ah

Figure 14-6778. EPWM_TBPRD Name Register

15	14	13	12	11	10	9	8
TBPRD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBPRD							
R/W							
0h							

Table 14-13742. EPWM_TBPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBPRD	R/W	0h	These bits determine the period of the time-base counter This sets the PWM frequency Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit By default this register is shadowed [a] If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the active register will be loaded from the shadow register when the time-base counter equals zero [b] If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [c] The active and shadow registers share the same memory map address

14.7.5.3.2.7 EPWM_CMPCTL Register

14.7.5.3.2.7.1 EPWM_CMPCTL Register (Offset = Eh) [reset = 0h]

Counter Compare Control Register

Return to Summary Table

Table 14-13743. Instance Table

Instance Name	Physical Address
EPWM0	2300 000Eh
EPWM1	2301 000Eh
EPWM2	2302 000Eh

Figure 14-6779. EPWM_CMPCTL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td>SHDWBFULL</td><td>SHDWAFULL</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED2</td><td>SHDWBMODE</td><td>RESERVED3</td><td>SHDWAMODE</td><td colspan="2">LOADBMODE</td><td colspan="2">LOADAMODE</td></tr>
<tr><td>R</td><td>R/W</td><td>R</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-13744. EPWM_CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved
9	SHDWBFULL	R	0h	Counter-compare B [CMPB] Shadow Register Full Status Flag This bit self clears once a load-strobe occurs 0h CMPB shadow FIFO not full yet 1h Indicates the CMPB shadow FIFO is full. A CPU write will overwrite current shadow value.
8	SHDWAFULL	R	0h	Counter-compare A [CMPA] Shadow Register Full Status Flag The flag bit is set when a 32 bit write to CMPA:CMPAHR register or a 16 bit write to CMPA register is made A 16 bit write to CMPAHR register will not affect the flag This bit self clears once a load-strobe occurs 0h CMPA shadow FIFO not full yet 1h Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value
7	RESERVED2	R	0h	Reserved
6	SHDWBMODE	R/W	0h	Counter-compare B [CMPB] Register Operating Mode 0h Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register. 1h Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action.
5	RESERVED3	R	0h	Reserved
4	SHDWAMODE	R/W	0h	Counter-compare A [CMPA] Register Operating Mode 0h Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register. 1h Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action.

Table 14-13744. EPWM_CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LOADBMODE	R/W	0h	Active Counter-Compare B [CMPB] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWBMODE] = 1] 0h Load on EPWM_TBCNT[15-0] TBCNT = 0h Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT= 0000h) 1h Load on EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD: Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD) 2h Load on either EPWM_TBCNT[15-0] TBCNT = 0 or EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD 3h Freeze (no loads possible)
1:0	LOADAMODE	R/W	0h	Active Counter-Compare A [CMPA] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWAMODE] = 1] 0h Load on TBCNT = 0h Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h) 1h Load on TBCNT = TBPRD: Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT= EPWM_TBPRD[15-0] TBPRD) 2h Load on either EPWM_TBCNT[15-0] TBCNT = 0h 3h Freeze (no loads possible)

14.7.5.3.2.8 EPWM_CMPAHR Register

14.7.5.3.2.8.1 EPWM_CMPAHR Register (Offset = 10h) [reset = 0h]

Counter Compare A High Resolution Register. This register is only available on ePWM instances that include the high-resolution PWM (HRPWM) extension; otherwise, this location is reserved.

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Table 14-13745. Instance Table

Instance Name	Physical Address
EPWM0	2300 0010h
EPWM1	2301 0010h
EPWM2	2302 0010h

Figure 14-6780. EPWM_CMPAHR Name Register

15	14	13	12	11	10	9	8
CMPAHR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1							
R							
0h							

Table 14-13746. EPWM_CMPAHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CMPAHR	R/W	0h	Compare A High-Resolution register bits for MEP step control A minimum value of 1h is needed to enable HRPWM capabilities Valid MEP range of operation 1-255h
7:0	RESERVED1	R	0h	Reserved

14.7.5.3.2.9 EPWM_CMPA Register

14.7.5.3.2.9.1 EPWM_CMPA Register (Offset = 12h) [reset = 0h]

Counter Compare A Register

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Table 14-13747. Instance Table

Instance Name	Physical Address
EPWM0	2300 0012h
EPWM1	2301 0012h
EPWM2	2302 0012h

Figure 14-6781. EPWM_CMPA Name Register

15	14	13	12	11	10	9	8
CMPA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPA							
R/W							
0h							

Table 14-13748. EPWM_CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPA	R/W	0h	The value in the active CMPA register is continuously compared to the time-base counter [TBCNT] When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event This event is sent to the action-qualifier where it is qualified and converted it into one or more actions These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers The actions that can be defined in the AQCTLA and AQCTLB registers include the following [a] Do nothing the event is ignored [b] Clear: Pull the EPWMxA and/or EPWMxB signal low [c] Set: Pull the EPWMxA and/or EPWMxB signal high [d] Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit By default this register is shadowed [a] If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register [b] Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full [c] If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [d] In either mode, the active and shadow registers share the same memory map address

14.7.5.3.2.10 EPWM_CMPB Register

14.7.5.3.2.10.1 EPWM_CMPB Register (Offset = 14h) [reset = 0h]

Counter Compare B Register

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Table 14-13749. Instance Table

Instance Name	Physical Address
EPWM0	2300 0014h
EPWM1	2301 0014h
EPWM2	2302 0014h

Figure 14-6782. EPWM_CMPB Name Register

15	14	13	12	11	10	9	8
CMPB							
R/W							
0h							
7	6	5	4	3	2	1	0
CMPB							
R/W							
0h							

Table 14-13750. EPWM_CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPB	R/W	0h	The value in the active CMPB register is continuously compared to the time-base counter [TBCNT] When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare B" event This event is sent to the action-qualifier where it is qualified and converted it into one or more actions These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers The actions that can be defined in the AQCTLA and AQCTLB registers include the following [a] Do nothing, the event is ignored [b] Clear: Pull the EPWMxA and/or EPWMxB signal low [c] Set: Pull the EPWMxA and/or EPWMxB signal high [d] Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWBMODE] bit By default this register is shadowed [a] If CMPCTL[SHDWBMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register In this case, the CMPCTL[LOADBMODE] bit field determines which event will load the active register from the shadow register: [b] Before a write, the CMPCTL[SHDWBFULL] bit can be read to determine if the shadow register is currently full [c] If CMPCTL[SHDWBMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware [d] In either mode, the active and shadow registers share the same memory map address

14.7.5.3.2.11 EPWM_AQCTLA Register

14.7.5.3.2.11.1 EPWM_AQCTLA Register (Offset = 16h) [reset = 0h]

Action Qualifier Control Register For Output A

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Table 14-13751. Instance Table

Instance Name	Physical Address
EPWM0	2300 0016h
EPWM1	2301 0016h
EPWM2	2302 0016h

Figure 14-6783. EPWM_AQCTLA Name Register

15	14	13	12	11	10	9	8
RESERVED1				CBD		CBU	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-13752. EPWM_AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED1	R	0h	Reserved
11:10	CBD	R/W	0h	Action when the time-base counter equals the active CMPB register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
9:8	CBU	R/W	0h	Action when the counter equals the active CMPB register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
7:6	CAD	R/W	0h	Action when the counter equals the active CMPA register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
5:4	CAU	R/W	0h	Action when the counter equals the active CMPA register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxA output low 2h Set: force EPWMxA output high 3h Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low

Table 14-13752. EPWM_AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	PRD	R/W	0h	Action when the counter equals the period Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down 0h `Do nothing (action disabled)` 1h `Clear: force EPWMxA output low` 2h `Set: force EPWMxA output high` 3h `Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low`
1:0	ZRO	R/W	0h	Action when counter equals zero Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up 0h `Do nothing (action disabled)` 1h `Clear: force EPWMxA output low` 2h `Set: force EPWMxA output high` 3h `Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low`

14.7.5.3.2.12 EPWM_AQCTLB Register

14.7.5.3.2.12.1 EPWM_AQCTLB Register (Offset = 18h) [reset = 0h]

Action Qualifier Control Register For Output B

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Table 14-13753. Instance Table

Instance Name	Physical Address
EPWM0	2300 0018h
EPWM1	2301 0018h
EPWM2	2302 0018h

Figure 14-6784. EPWM_AQCTLB Name Register

15	14	13	12	11	10	9	8
RESERVED1				CBD		CBU	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-13754. EPWM_AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED1	R	0h	Reserved
11:10	CBD	R/W	0h	Action when the counter equals the active CMPB register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
9:8	CBU	R/W	0h	Action when the counter equals the active CMPB register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
7:6	CAD	R/W	0h	Action when the counter equals the active CMPA register and the counter is decrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
5:4	CAU	R/W	0h	Action when the counter equals the active CMPA register and the counter is incrementing 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low

Table 14-13754. EPWM_AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	PRD	R/W	0h	Action when the counter equals the period Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low
1:0	ZRO	R/W	0h	Action when counter equals zero Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up 0h Do nothing (action disabled) 1h Clear: force EPWMxB output low 2h Set: force EPWMxB output high 3h Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low

14.7.5.3.2.13 EPWM_AQSFRC Register

14.7.5.3.2.13.1 EPWM_AQSFRC Register (Offset = 1Ah) [reset = 0h]

Action Qualifier Software Force Register

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Table 14-13755. Instance Table

Instance Name	Physical Address
EPWM0	2300 001Ah
EPWM1	2301 001Ah
EPWM2	2302 001Ah

Figure 14-6785. EPWM_AQSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RLDCSF		OTSFB	ACTSFB		OTSFA	ACTSFA	
R/W		R/W1TC	R/W		R/W1TC	R/W	
0h		0h	0h		0h	0h	

Table 14-13756. EPWM_AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED1	R	0h	Reserved
7:6	RLDCSF	R/W	0h	AQCSFRC Active Register Reload From Shadow Options
5	OTSFB	R/W1TC	0h	One-Time Software Forced Event on Output B 0h Writing a 0h (1h Initiates a single s/w forced event
4:3	ACTSFB	R/W	0h	Action when One-Time Software Force B Is invoked 0h Does nothing (action disabled) 1h Clear (low) 2h Set (high) 3h Toggle (Low -> High, High -> Low).
2	OTSFA	R/W1TC	0h	One-Time Software Forced Event on Output A 0h Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (that is, a forced event is initiated). 1h Initiates a single software forced event.
1:0	ACTSFA	R/W	0h	Action When One-Time Software Force A Is Invoked 0h Does nothing (action disabled). 1h Clear (low). 2h Set (high). 3h Toggle (Low -> High, High -> Low).

14.7.5.3.2.14 EPWM_AQCSFRC Register

14.7.5.3.2.14.1 EPWM_AQCSFRC Register (Offset = 1Ch) [reset = 0h]

Action Qualifier Continuous S/W Force Register

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Table 14-13757. Instance Table

Instance Name	Physical Address
EPWM0	2300 001Ch
EPWM1	2301 001Ch
EPWM2	2302 001Ch

Figure 14-6786. EPWM_AQCSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				CSFB		CSFA	
R				R/W		R/W	
0h				0h		0h	

Table 14-13758. EPWM_AQCSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved

3:2	CSFB	R/W	0h	Continuous Software Force on Output B In immediate mode, a continuous force takes effect on the next TBCLK edge In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register To configure shadow mode, use AQSFRC[RLDCSF]
				`0h` `Forcing disabled, that is, has no effect`
				`1h` `Forces a continuous low on output B`
				`2h` `Forces a continuous high on output B`
				`3h` `Software forcing is disabled and has no effect`

1:0	CSFA	R/W	0h	Continuous Software Force on Output A In immediate mode, a continuous force takes effect on the next TBCLK edge In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register
				`0h` `Forcing disabled, that is, has no effect`
				`1h` `Forces a continuous low on output A`
				`2h` `Forces a continuous high on output A`
				`3h` `Software forcing is disabled and has no effect`

14.7.5.3.2.15 EPWM_DBCTL Register

14.7.5.3.2.15.1 EPWM_DBCTL Register (Offset = 1Eh) [reset = 0h]

Dead-Band Generator Control Register

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Table 14-13759. Instance Table

Instance Name	Physical Address
EPWM0	2300 001Eh
EPWM1	2301 001Eh
EPWM2	2302 001Eh

Figure 14-6787. EPWM_DBCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1		IN_MODE		POLSEL		OUT_MODE	
R		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 14-13760. EPWM_DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED1	R	0h	Reserved
5:4	IN_MODE	R/W	0h	Dead Band Input Mode Control Bit 5 controls the S5 switch and bit 4 controls the S4 switch This allows you to select the input source to the falling-edge and rising-edge delay To produce classical dead-band waveforms, the default is EPWMxA In is the source for both falling and rising-edge delays 0h EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay. 1h EPWMxB In (from the action-qualifier) is the source for rising- edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal. 2h EPWMxA In (from the action-qualifier) is the source for rising- edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal. 3h EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.
3:2	POLSEL	R/W	0h	Polarity Select Control Bit 3 controls the S3 switch and bit 2 controls the S2 switch This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0,0 Other enhanced modes are also possible, but not regarded as typical usage modes 0h Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default). 1h Active low complementary (ALC) mode. EPWMxA is inverted. 2h Active high complementary (AHC). EPWMxB is inverted. 3h Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.

Table 14-13760. EPWM_DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	OUT_MODE	R/W	0h	Dead-band Output Mode Control Bit 1 controls the S1 switch and bit 0 controls the S0 switch This allows you to selectively enable or bypass the dead-band generation for the falling-edge and rising-edge delay 0h Dead-band generation is bypassed for both output signals. In this mode, both the EPWMxA and EPWMxB output signals from the action-qualifier are passed directly to the PWM-chopper submodule. In this mode, the POLSEL and IN_MODE bits have no effect. 1h Disable rising-edge delay. The EPWMxA signal from the action- qualifier is passed straight through to the EPWMxA input of the PWM-chopper submodule. The falling-edge delayed signal is seen on output EPWMxB. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field. 2h Disable falling-edge delay. The EPWMxB signal from the action- qualifier is passed straight through to the EPWMxB input of the PWM-chopper submodule. The rising-edge delayed signal is seen on output EPWMxA. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field. 3h Dead-band is fully enabled for both rising-edge delay on output EPWMxA and falling-edge delay on output EPWMxB. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field.

14.7.5.3.2.16 EPWM_DBRED Register

14.7.5.3.2.16.1 EPWM_DBRED Register (Offset = 20h) [reset = 0h]

Dead-Band Generator Rising Edge Delay Count Register

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Table 14-13761. Instance Table

Instance Name	Physical Address
EPWM0	2300 0020h
EPWM1	2301 0020h
EPWM2	2302 0020h

Figure 14-6788. EPWM_DBRED Name Register

15	14	13	12	11	10	9	8
RESERVED1						DEL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEL							
R/W							
0h							

Table 14-13762. EPWM_DBRED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved
9:0	DEL	R/W	0h	Rising Edge Delay Count 10 bit counter

14.7.5.3.2.17 EPWM_DBFED Register

14.7.5.3.2.17.1 EPWM_DBFED Register (Offset = 22h) [reset = 0h]

Dead-Band Generator Falling Edge Delay Count Register

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Table 14-13763. Instance Table

Instance Name	Physical Address
EPWM0	2300 0022h
EPWM1	2301 0022h
EPWM2	2302 0022h

Figure 14-6789. EPWM_DBFED Name Register

15	14	13	12	11	10	9	8
RESERVED1						DEL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEL							
R/W							
0h							

Table 14-13764. EPWM_DBFED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED1	R	0h	Reserved
9:0	DEL	R/W	0h	Falling Edge Delay Count 10 bit counter

14.7.5.3.2.18 EPWM_TZSEL Register

14.7.5.3.2.18.1 EPWM_TZSEL Register (Offset = 24h) [reset = 0h]

Trip Zone Select Register

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Table 14-13765. Instance Table

Instance Name	Physical Address
EPWM0	2300 0024h
EPWM1	2301 0024h
EPWM2	2302 0024h

Figure 14-6790. EPWM_TZSEL Name Register

15	14	13	12	11	10	9	8
OSHTN							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CBCN							
R/W							
0h							

Table 14-13766. EPWM_TZSEL Register Field Descriptions

Bit	Field	Type	Reset	Description

15:8	OSHTN	R/W	0h	Trip-zone n [TZn] select One-Shot [OSHT] trip-zone enable/disable When any of the enabled pins go low, a one-shot trip event occurs for this ePWM module When the event occurs, the action defined in the TZCTL register is taken on the EPWMxA and EPWMxB outputs The one-shot trip condition remains latched until you clear the condition via the TZCLR register
				`0h` `Disable TZn as a one-shot trip source for this EPWM module`
				`1h` `Enable TZn as a one-shot trip source for this EPWM module`

7:0	CBCN	R/W	0h	Trip-zone n [TZn] select Cycle-by-Cycle [CBC] trip-zone enable/disable When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this ePWM module When the event occurs, the action defined in the TZCTL register is taken on the EPWMxA and EPWMxB outputs A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero
				`0h` `Disable TZn as a CBC trip source for this EPWM module`
				`1h` `Enable TZn as a CBC trip source for this EPWM module`

14.7.5.3.2.19 EPWM_TZCTL Register

14.7.5.3.2.19.1 EPWM_TZCTL Register (Offset = 28h) [reset = 0h]

Trip Zone Control Register

Return to Summary Table

Table 14-13767. Instance Table

Instance Name	Physical Address
EPWM0	2300 0028h
EPWM1	2301 0028h
EPWM2	2302 0028h

Figure 14-6791. EPWM_TZCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				TZB		TZA	
R				R/W		R/W	
0h				0h		0h	

Table 14-13768. EPWM_TZCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved
3:2	TZB	R/W	0h	When a trip event occurs the following action is taken on output EPWMxB Which trip-zone pins can cause an event is defined in the TZSEL register 0h `High impedance (EPWMxB = High-impedance state)` 1h `Force EPWMxB to a high state` 2h `Force EPWMxB to a low state` 3h `Do nothing, no action is taken on EPWMxB.`
1:0	TZA	R/W	0h	When a trip event occurs the following action is taken on output EPWMxA Which trip-zone pins can cause an event is defined in the TZSEL register 0h `High impedance (EPWMxA = High-impedance state)` 1h `Force EPWMxA to a high state` 2h `Force EPWMxA to a low state` 3h `Do nothing, no action is taken on EPWMxA.`

14.7.5.3.2.20 EPWM_TZEINT Register

14.7.5.3.2.20.1 EPWM_TZEINT Register (Offset = 2Ah) [reset = 0h]

Trip Zone Enable Interrupt Register

Return to Summary Table

Table 14-13769. Instance Table

Instance Name	Physical Address
EPWM0	2300 002Ah
EPWM1	2301 002Ah
EPWM2	2302 002Ah

Figure 14-6792. EPWM_TZEINT Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED1</td><td>OST</td><td>CBC</td><td>RESERVED2</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13770. EPWM_TZEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R/W	0h	Trip-zone One-Shot Interrupt Enable 0h `Disable one-shot interrupt generation` 1h `Enable Interrupt generation a one-shot trip event will cause a EPWMxTZINT interrupt.`
1	CBC	R/W	0h	Trip-zone Cycle-by-Cycle Interrupt Enable 0h `Disable cycle-by-cycle interrupt generation` 1h `Enable interrupt generation a cycle-by-cycle trip event will cause an EPWMxTZINT interrupt.`
0	RESERVED2	R	0h	Reserved

14.7.5.3.2.21 EPWM_TZFLG Register

14.7.5.3.2.21.1 EPWM_TZFLG Register (Offset = 2Ch) [reset = 0h]

Trip Zone Flag Register

Return to Summary Table

Table 14-13771. Instance Table

Instance Name	Physical Address
EPWM0	2300 002Ch
EPWM1	2301 002Ch
EPWM2	2302 002Ch

Figure 14-6793. EPWM_TZFLG Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED1					OST	CBC	INT
R					R	R	R
0h					0h	0h	0h

Table 14-13772. EPWM_TZFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R	0h	Latched Status Flag for A One-Shot Trip Event 0h No one-shot trip event has occurred 1h Indicates a trip event has occurred on a pin selected as a one-shot trip source. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register.
1	CBC	R	0h	Latched Status Flag for Cycle-By-Cycle Trip Event 0h No cycle-by-cycle trip event has occurred 1h Indicates a trip event has occurred on a pin selected as a cycle-by-cycle trip source. The EPWM_TZFLG[1] CBC bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the pins is automatically cleared when the EPWM time-base counter reaches zero (EPWM_TBCNT[15-0] TBCNT = 0000h)
0	INT	R	0h	Latched Trip Interrupt Status Flag 0h Indicates no interrupt has been generated 1h Indicates an EPWMxTZINT interrupt was generated because of a trip condition. No further EPWMxTZINT interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register.

14.7.5.3.2.22 EPWM_TZCLR Register

14.7.5.3.2.22.1 EPWM_TZCLR Register (Offset = 2Eh) [reset = 0h]

Trip Zone Clear Register

Return to Summary Table

Table 14-13773. Instance Table

Instance Name	Physical Address
EPWM0	2300 002Eh
EPWM1	2301 002Eh
EPWM2	2302 002Eh

Figure 14-6794. EPWM_TZCLR Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED1</td><td>OST</td><td>CBC</td><td>INT</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13774. EPWM_TZCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved
2	OST	R/W	0h	Clear Flag for One-Shot Trip [OST] Latch 0h Has no effect. Always reads back a 0h 1h Clears this Trip (set) condition
1	CBC	R/W	0h	Clear Flag for Cycle-By-Cycle [CBC] Trip Latch 0h Has no effect. Always reads back a 0h 1h Clears this Trip (set) condition
0	INT	R/W	0h	Global Interrupt Clear Flag 0h Has no effect. Always reads back a 0h 1h Clears the trip-interrupt flag for this EPWM module (EPWM_TZFLG[0] INT)

14.7.5.3.2.23 EPWM_TZFRC Register

14.7.5.3.2.23.1 EPWM_TZFRC Register (Offset = 30h) [reset = 0h]

Trip Zone Force Register

Return to Summary Table

Table 14-13775. Instance Table

Instance Name	Physical Address
EPWM0	2300 0030h
EPWM1	2301 0030h
EPWM2	2302 0030h

Figure 14-6795. EPWM_TZFRC Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED1</td><td>OST</td><td>CBC</td><td>RESERVED2</td></tr>
<tr><td colspan="5">R</td><td>R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13776. EPWM_TZFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED1	R	0h	Reserved

2	OST	R/W	0h	Force a One-Shot Trip Event via Software
				`0h` `Writing of 0h`
				`1h` `Forces a one-shot trip event and sets the EPWM_TZFLG[2] OST bit.`

1	CBC	R/W	0h	Force a Cycle-by-Cycle Trip Event via Software
				`0h` `Writing of 0h`
				`1h` `Forces a cycle-by-cycle trip event and sets the EPWM_TZFLG[1] CBC bit.`

0	RESERVED2	R	0h	Reserved

14.7.5.3.2.24 EPWM_ETSEL Register

14.7.5.3.2.24.1 EPWM_ETSEL Register (Offset = 32h) [reset = 0h]

Event Trigger Selection Register

Return to Summary Table

Table 14-13777. Instance Table

Instance Name	Physical Address
EPWM0	2300 0032h
EPWM1	2301 0032h
EPWM2	2302 0032h

Figure 14-6796. EPWM_ETSEL Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				INTEN	INTSEL		
R				R/W	R/W		
0h				0h	0h		

Table 14-13778. EPWM_ETSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved

3	INTEN	R/W	0h	Enable ePWM Interrupt [EPWMx_INT] Generation
				`0h Disable EPWMx_INT generation`
				`1h Enable EPWMx_INT generation`

2:0	INTSEL	R/W	0h	ePWM Interrupt [EPWMx_INT] Selection Options
				`0h Reserved`
				`1h Enable event time-base counter equal to zero. (EPWM_TBCNT = 0000h)`
				`2h Enable event time-base counter equal to period (EPWM_TBCNT = EPWM_TBPRD)`
				`3h Reserved`
				`4h Enable event time-base counter equal to CMPA when the timer is incrementing`
				`5h Enable event time-base counter equal to CMPA when the timer is decrementing`
				`6h Enable event time-base counter equal to CMPB when the timer is incrementing`
				`7h Enable event time-base counter equal to CMPB when the timer is decrementing`

14.7.5.3.2.25 EPWM_ETPS Register

14.7.5.3.2.25.1 EPWM_ETPS Register (Offset = 34h) [reset = 0h]

Event Trigger Pre-Scale Register

Return to Summary Table

Table 14-13779. Instance Table

Instance Name	Physical Address
EPWM0	2300 0034h
EPWM1	2301 0034h
EPWM2	2302 0034h

Figure 14-6797. EPWM_ETPS Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				INTCNT		INTPRD	
R				R		R/W	
0h				0h		0h	

Table 14-13780. EPWM_ETPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED1	R	0h	Reserved
3:2	INTCNT	R	0h	ePWM Interrupt Event [EPWMx_INT] Counter Register These bits indicate how many selected ETSEL[INTSEL] events have occurred These bits are automatically cleared when an interrupt pulse is generated If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD] 0h No events have occurred 1h 1 event has occurred 2h 2 events have occurred 3h 3 events have occurred
1:0	INTPRD	R/W	0h	ePWM Interrupt [EPWMx_INT] Period Select These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated To be generated, the interrupt must be enabled [ETSEL[INT] = 1] If the interrupt status flag is set from a previous interrupt [ETFLG[INT] = 1] then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit This allows for one interrupt to be pending while another is still being serviced Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear Writing a INTPRD value that is less than the current counter value will result in an undefined state If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented 0h Disable the interrupt event counter. No interrupt will be generated and the EPWM_ETFRC[0] INT bit is ignored. 1h Generate an interrupt on the first event INTCNT = 0b01 (first event) 2h Generate interrupt on the EPWM_ETPS[3-2] INTCNT = 0b10 (second event) 3h Generate interrupt on the EPWM_ETPS[3-2] INTCNT = 0b11 (third event)

14.7.5.3.2.26 EPWM_ETFLG Register

14.7.5.3.2.26.1 EPWM_ETFLG Register (Offset = 36h) [reset = 0h]

Event Trigger Flag Register

Return to Summary Table

Table 14-13781. Instance Table

Instance Name	Physical Address
EPWM0	2300 0036h
EPWM1	2301 0036h
EPWM2	2302 0036h

Figure 14-6798. EPWM_ETFLG Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED1							INT
R							R
0h							0h

Table 14-13782. EPWM_ETFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved
0	INT	R	0h	Latched ePWM Interrupt [EPWMx_INT] Status Flag 0h Indicates no event occurred. 1h Indicates that an EPWMx interrupt (EWPMx_INT) was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the EPWM_ETFLG[0] INT bit is still set. If an interrupt is pending, it will not be generated until after the EPWM_ETFLG[0] INT bit is cleared.

14.7.5.3.2.27 EPWM_ETCLR Register

14.7.5.3.2.27.1 EPWM_ETCLR Register (Offset = 38h) [reset = 0h]

Event Trigger Clear Register

Return to Summary Table

Table 14-13783. Instance Table

Instance Name	Physical Address
EPWM0	2300 0038h
EPWM1	2301 0038h
EPWM2	2302 0038h

Figure 14-6799. EPWM_ETCLR Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1							INT
R							R
0h							0h

Table 14-13784. EPWM_ETCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved
0	INT	R	0h	ePWM Interrupt [EPWMx_INT] Flag Clear Bit

14.7.5.3.2.28 EPWM_ETFRC Register

14.7.5.3.2.28.1 EPWM_ETFRC Register (Offset = 3Ah) [reset = 0h]

Event Trigger Force Register

Return to Summary Table

Table 14-13785. Instance Table

Instance Name	Physical Address
EPWM0	2300 003Ah
EPWM1	2301 003Ah
EPWM2	2302 003Ah

Figure 14-6800. EPWM_ETFRC Name Register

15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED1							INT
R							R
0h							0h

Table 14-13786. EPWM_ETFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED1	R	0h	Reserved
0	INT	R	0h	INT Force Bit The interrupt will only be generated if the event is enabled in the ETSEL register The INT flag bit will be set regardless 0h `Writing a 0 has no effect. Always reads back a 0h` 1h `Writing 1 clears the EPWM_ETFLG[0] INT flag bit and enable further interrupts pulses to be generated.`

14.7.5.3.2.29 EPWM_PCCTL Register

14.7.5.3.2.29.1 EPWM_PCCTL Register (Offset = 3Ch) [reset = 0h]

PWM Chopper Control Register

Return to Summary Table

Table 14-13787. Instance Table

Instance Name	Physical Address
EPWM0	2300 003Ch
EPWM1	2301 003Ch
EPWM2	2302 003Ch

Figure 14-6801. EPWM_PCCTL Name Register

15	14	13	12	11	10	9	8
RESERVED1					CHPDUTY		
R					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHPFREQ			OSHTWTH				CHPEN
R/W			R/W				R/W
0h			0h				0h

Table 14-13788. EPWM_PCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED1	R	0h	Reserved
10:8	CHPDUTY	R/W	0h	Chopping Clock Duty Cycle 0h Duty = 1/8 (12.5%) 1h Duty = 2/8 (25.0%) 2h Duty = 3/8 (37.5%) 3h Duty = 4/8 (50.0%) 4h Duty = 5/8 (62.5%) 5h Duty = 6/8 (75.0%) 6h Duty = 7/8 (87.5%) 7h Reserved
7:5	CHPFREQ	R/W	0h	Chopping Clock Frequency 0h Divide by 1 (no prescale) 1h Divide by 2 2h Divide by 3 3h Divide by 4 4h Divide by 5 5h Divide by 6 6h Divide by 7 7h Divide by 8
4:1	OSHTWTH	R/W	0h	One-Shot Pulse Width 0h 1 - SYSCLKOUT/8 wide 1h 2 - SYSCLKOUT/8 wide 2h 3 - SYSCLKOUT/8 wide 3h 4 - SYSCLKOUT/8 wide 3h 4 - SYSCLKOUT/8 wide
0	CHPEN	R/W	0h	PWM-chopping Enable 0h Disable (bypass) PWM chopping function 1h Enable chopping function

14.7.5.3.2.30 EPWM_PID Register

14.7.5.3.2.30.1 EPWM_PID Register (Offset = 5Ch) [reset = 44D10903h]

EHRPWM Peripheral ID Register. The IP revision register is used by software to track features, bugs, and compatibility.

Return to Summary Table

Table 14-13789. Instance Table

Instance Name	Physical Address
EPWM0	2300 005Ch
EPWM1	2301 005Ch
EPWM2	2302 005Ch

Figure 14-6802. EPWM_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED1		FUNC			
R		R		R			
1h		0h		4D1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
4D1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_RTL					X_MAJOR		
R					R		
1h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		Y_MINOR					
R		R					
0h		3h					

Table 14-13790. EPWM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between the old scheme and current
29:28	RESERVED1	R	0h	Reserved
27:16	FUNC	R	4D1h	FUNC
15:11	R_RTL	R	1h	RTL version [R], maintained by IP design owner
10:8	X_MAJOR	R	1h	Major revision [X]
7:6	CUSTOM	R	0h	CUSTOM
5:0	Y_MINOR	R	3h	Minor revision [Y]

14.7.5.4 adcss

adcss

14.7.5.4.1 adcss Summaries

adcss Summaries

Table 14-13791. ADC Registers, Base Address=2060 8000h, Length=1024

Offset	Length	Register Name	ADC0 Physical Address
100h	32	ADC_DATA0	2060 8100h
200h	32	ADC_DATA1	2060 8200h

Table 14-13792. ADC Registers, Base Address=2060 0000h, Length=1024

Offset	Length	Register Name	ADC0 Physical Address
0h	32	ADC_REVISION	2060 0000h
38h	32	ADC_DMAENABLE_SET	2060 0038h
3Ch	32	ADC_DMAENABLE_CLR	2060 003Ch
40h	32	ADC_CTRL	2060 0040h
44h	32	ADC_ADCSTAT	2060 0044h
48h	32	ADC_ADCRANGE	2060 0048h
50h	32	ADC_MISC	2060 0050h
54h	32	ADC_STEPENABLE	2060 0054h
E4h	32	ADC_FIFOCOUNT0	2060 00E4h
E8h	32	ADC_FIFOTHRESHOLD0	2060 00E8h
ECh	32	ADC_DMAREQ0	2060 00ECh
F0h	32	ADC_FIFOCOUNT1	2060 00F0h
F4h	32	ADC_FIFOTHRESHOLD1	2060 00F4h
F8h	32	ADC_DMAREQ1	2060 00F8h
100h	32	ADC_FIFODATA0	2060 0100h
200h	32	ADC_FIFODATA1	2060 0200h
0h	32	ADC_IRQ_EOI	2060 0020h
4h	32	ADC_IRQSTATUS_RAW	2060 0024h
8h	32	ADC_IRQSTATUS	2060 0028h
Ch	32	ADC_IRQENABLE_SET	2060 002Ch
10h	32	ADC_IRQENABLE_CLR	2060 0030h
0h	32	ADC_STEPCONFIG_J	2060 0000h + formula
4h	32	ADC_STEPDELAY_J	2060 0004h + formula

14.7.5.4.2 adcss Registers

adcss Registers

14.7.5.4.2.1 ADC_DATA0 Register

14.7.5.4.2.1.1 ADC_DATA0 Register (Offset = 100h) [reset = 0h]

DMA sample FIFO

Return to Summary Table

Table 14-13793. Instance Table

Instance Name	Physical Address
ADC0	2060 8100h

Figure 14-6803. ADC_DATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED1</td><td colspan="4">ADCCHANLID</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">ADCDATA</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ADCDATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13794. ADC_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	Reserved
19:16	ADCCHANLID	R	0h	Optional ID tag of channel that captured the data. If tag option is disabled, these bits will be 0 Reset Source: rst_mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ADCDATA	R	0h	sampled ADC converted data value stored in FIFO Reset Source: rst_mod_g_rst_n

14.7.5.4.2.2 ADC_DATA1 Register

14.7.5.4.2.2.1 ADC_DATA1 Register (Offset = 200h) [reset = 0h]

DMA sample FIFO

Return to Summary Table

Table 14-13795. Instance Table

Instance Name	Physical Address
ADC0	2060 8200h

Figure 14-6804. ADC_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1				ADCCHANLID			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				ADCDATA			
NONE				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADCDATA							
R							
0h							

Table 14-13796. ADC_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	Reserved
19:16	ADCCHANLID	R	0h	Optional ID tag of channel that captured the data. If tag option is disabled, these bits will be 0 Reset Source: rst_mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ADCDATA	R	0h	sampled ADC converted data value stored in FIFO Reset Source: rst_mod_g_rst_n

14.7.5.4.2.3 ADC_REVISION Register

14.7.5.4.2.3.1 ADC_REVISION Register (Offset = 0h) [reset = 69C03900h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 14-13797. Instance Table

Instance Name	Physical Address
ADC0	2060 0000h

Figure 14-6805. ADC_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
69C0h							
23	22	21	20	19	18	17	16
MODID							
R							
69C0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					1h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 14-13798. ADC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	69C0h	Module ID field Reset Source: rst_mod_g_rst_n
15:11	REVRTL	R	7h	RTL revision. Will vary depending on release. Reset Source: rst_mod_g_rst_n
10:8	REVMAJ	R	1h	Major revision Reset Source: rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: rst_mod_g_rst_n
5:0	REVMIN	R	0h	Minor revision Reset Source: rst_mod_g_rst_n

14.7.5.4.2.4 ADC_DMAENABLE_SET Register

14.7.5.4.2.4.1 ADC_DMAENABLE_SET Register (Offset = 38h) [reset = 0h]

The DMAENABLE_SET register allows the enabling of DMA requests

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Table 14-13799. Instance Table

Instance Name	Physical Address
ADC0	2060 0038h

Figure 14-6806. ADC_DMAENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED0						
NONE	R						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED0							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED0							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED0						ENABLE1	ENABLE0
R						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13800. ADC_DMAENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:2	RESERVED0	R	0h	Reserved
1	ENABLE1	R/W1TS	0h	enable DMA reguest FIFO1 Reset Source: rst_mod_g_rst_n
0	ENABLE0	R/W1TS	0h	enable DMA reguest FIFO0 Reset Source: rst_mod_g_rst_n

14.7.5.4.2.5 ADC_DMAENABLE_CLR Register

14.7.5.4.2.5.1 ADC_DMAENABLE_CLR Register (Offset = 3Ch) [reset = 0h]

The DMAENABLE_CLR register allows the disabling of DMA requests

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Table 14-13801. Instance Table

Instance Name	Physical Address
ADC0	2060 003Ch

Figure 14-6807. ADC_DMAENABLE_CLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RESERVED</td><td colspan="7">RESERVED0</td></tr>
<tr><td>NONE</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED0</td><td>ENABLE1</td><td>ENABLE0</td></tr>
<tr><td colspan="6">R</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13802. ADC_DMAENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:2	RESERVED0	R	0h	Reserved
1	ENABLE1	R/W1TC	0h	clears the enable of the DMA reguest FIFO1. Disables DMA request when Writing 1 Reset Source: rst_mod_g_rst_n
0	ENABLE0	R/W1TC	0h	clears the enable of the DMA reguest FIFO0. Disables DMA request when Writing 1 Reset Source: rst_mod_g_rst_n

14.7.5.4.2.6 ADC_CTRL Register

14.7.5.4.2.6.1 ADC_CTRL Register (Offset = 40h) [reset = 10h]

Controls various parameters of the cotroller state.

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Table 14-13803. Instance Table

Instance Name	Physical Address
ADC0	2060 0040h

Figure 14-6808. ADC_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				HI_MID_SEL	HI_MID_EN	HW_PREEMPT	HW_MAP
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED2			PD	BIAS_SEL	RESERVED0	STEP_ID_EN	MODULE_ENABLE
R			R/W	R/W	R	R/W	R/W
0h			1h	0h	0h	0h	0h

Table 14-13804. ADC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED1	R	0h	Reserved
11	HI_MID_SEL	R/W	0h	Functional safety debug mode. =1 choose ADCREFP, =0 VMID reference input to ADC Reset Source: rst_mod_g_rst_n
10	HI_MID_EN	R/W	0h	Functional safety debug mode. enable fixed reference to ADC for testing Reset Source: rst_mod_g_rst_n
9	HW_PREEMPT	R/W	0h	1 steps are preempted Reset Source: rst_mod_g_rst_n
8	HW_MAP	R/W	0h	1 = hw events enabled Reset Source: rst_mod_g_rst_n
7:5	RESERVED2	R	0h	Reserved
4	PD	R/W	1h	AFE powered down Reset Source: rst_mod_g_rst_n
3	BIAS_SEL	R/W	0h	AFE select bias control Reset Source: rst_mod_g_rst_n
2	RESERVED0	R	0h	Reserved
1	STEP_ID_EN	R/W	0h	Writing 1 will store the stepid number with the captured adc data in the fifo Reset Source: rst_mod_g_rst_n

Table 14-13804. ADC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MODULE_ENABLE	R/W	0h	ADC12_SS module enable bit. After programming all the configuration and step enable registers, write a 1 to this bit to start conversion. Writing a 0 will disable the module after the current conversion. Before turning on again, the ADC_SEQUENCER_STATUS register show read back STEP_ID=Idle and FSM_BUSY=0. Enabling the controller will be held off until mem_init_done =1. Reset Source: rst_mod_g_rst_n

14.7.5.4.2.7 ADC_ADCSTAT Register

14.7.5.4.2.7.1 ADC_ADCSTAT Register (Offset = 44h) [reset = 20h]

SW can read this register to find out the currently scheduled step id being converted on the ADC port. If you want to turn the controller off and then back on, the step_id bit should be checked and compared to IDLE before enabling the ADC12_SS module again. Also, before enabling the controller again, the user should wait for the FSM bit 5 to read idl.

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Table 14-13805. Instance Table

Instance Name	Physical Address
ADC0	2060 0044h

Figure 14-6809. ADC_ADCSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							GPADC_BUSY
R							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED2	MEM_INIT_DONE	FSM_BUSY	STEP_IDLE				
R	R	R	R				
0h	X	1h	0h				

Table 14-13806. ADC_ADCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved
8	GPADC_BUSY	R	0h	Monitor the AFE internal calibration, busy bit Reset Source: rst_mod_g_rst_n
7	RESERVED2	R	0h	Reserved
6	MEM_INIT_DONE	R	X	status of ram initialization, 1= ram initialization to 0 after reset is done. Reset Source: rst_mod_g_rst_n
5	FSM_BUSY	R	1h	status of fsm, 1= conversion in progress Reset Source: rst_mod_g_rst_n
4:0	STEP_IDLE	R	0h	10000 = idle, 000000 -> 01111 corresponds to step 1 -> step 16 Reset Source: rst_mod_g_rst_n

14.7.5.4.2.8 ADC_ADCRANGE Register

14.7.5.4.2.8.1 ADC_ADCRANGE Register (Offset = 48h) [reset = 0h]

This feature requires the range check interrupt bit to be enabled first. The user can decide which channel input is compared by programming the RangeCheck bit of the StepConfig Registers. It is up to software to sort through FIFO data to determine which channel data was out of range. Software should only use LSB 10 bits for comparison and make sure bits 11,12 are 0.

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Table 14-13807. Instance Table

Instance Name	Physical Address
ADC0	2060 0048h

Figure 14-6810. ADC_ADCRANGE Name Register

31	30	29	28	27	26	25	24
RESERVED1				HIRANGE			
R				R/W			
0h				0h			
23	22	21	20	19	18	17	16
HIRANGE							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED2				LOWRANGE			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LOWRANGE							
R/W							
0h							

Table 14-13808. ADC_ADCRANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED1	R	0h	Reserved
27:16	HIRANGE	R/W	0h	If the sampled data is > value, then interrupt is generated Reset Source: rst_mod_g_rst_n
15:12	RESERVED2	R	0h	Reserved
11:0	LOWRANGE	R/W	0h	If the sampled data is < value, then interrupt is generated Reset Source: rst_mod_g_rst_n

14.7.5.4.2.9 ADC_MISC Register

14.7.5.4.2.9.1 ADC_MISC Register (Offset = 50h) [reset = 0h]

Spare inputs of the AFE are driven by this register, spare outputs from the AFE are read.

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Table 14-13809. Instance Table

Instance Name	Physical Address
ADC0	2060 0050h

Figure 14-6811. ADC_MISC Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED2</td><td colspan="4">AFE_SPARE_OUT</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td colspan="4">AFE_SPARE_IN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13810. ADC_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED2	R	0h	Reserved
11:8	AFE_SPARE_OUT	R	0h	Spare outputs from AFE Reset Source: rst_mod_g_rst_n
7:4	RESERVED1	R	0h	Reserved
3:0	AFE_SPARE_IN	R/W	0h	Spare inputs to AFE Reset Source: rst_mod_g_rst_n

14.7.5.4.2.10 ADC_STEPENABLE Register

14.7.5.4.2.10.1 ADC_STEPENABLE Register (Offset = 54h) [reset = 0h]

Contains the enable bit for each step in the sequencer. When all steps are disabled, the FSM will stay in IDLE state. These bits can be enabled or disabled dynamically during operation. When a write to this register occurs during operational mode, the HW will make sure the new settings are updated after the END_OF_SEQUENCE event

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Table 14-13811. Instance Table

Instance Name	Physical Address
ADC0	2060 0054h

Figure 14-6812. ADC_STEPENABLE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">RESERVED1</td><td>STEP16</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>STEP15</td><td>STEP14</td><td>STEP13</td><td>STEP12</td><td>STEP11</td><td>STEP10</td><td>STEP9</td><td>STEP8</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>STEP7</td><td>STEP6</td><td>STEP5</td><td>STEP4</td><td>STEP3</td><td>STEP2</td><td>STEP1</td><td>RESERVED2</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13812. ADC_STEPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED1	R	0h	Reserved
16	STEP16	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
15	STEP15	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
14	STEP14	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
13	STEP13	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
12	STEP12	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
11	STEP11	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
10	STEP10	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
9	STEP9	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n

Table 14-13812. ADC_STEPENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	STEP8	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
7	STEP7	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
6	STEP6	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
5	STEP5	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
4	STEP4	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
3	STEP3	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
2	STEP2	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
1	STEP1	R/W	0h	Enable step Reset Source: rst_mod_g_rst_n
0	RESERVED2	R	0h	Reserved

14.7.5.4.2.11 ADC_FIFOCOUNT0 Register

14.7.5.4.2.11.1 ADC_FIFOCOUNT0 Register (Offset = E4h) [reset = 0h]

FIFO word count status

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Table 14-13813. Instance Table

Instance Name	Physical Address
ADC0	2060 00E4h

Figure 14-6813. ADC_FIFOCOUNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							NUMWDS
R							R
0h							0h
7	6	5	4	3	2	1	0
NUMWDS							
R							
0h							

Table 14-13814. ADC_FIFOCOUNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved
8:0	NUMWDS	R	0h	number of words in the FIFO Reset Source: rst_mod_g_rst_n

14.7.5.4.2.12 ADC_FIFOTHRESHOLD0 Register

14.7.5.4.2.12.1 ADC_FIFOTHRESHOLD0 Register (Offset = E8h) [reset = 0h]

FIFO threshold

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Table 14-13815. Instance Table

Instance Name	Physical Address
ADC0	2060 00E8h

Figure 14-6814. ADC_FIFOTHRESHOLD0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-13816. ADC_FIFOTHRESHOLD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reserved
7:0	THRESHOLD	R/W	0h	Program the desired FIFO0 data sample level minus 1 to reach before generating interrupt to CPU Reset Source: rst_mod_g_rst_n

14.7.5.4.2.13 ADC_DMAREQ0 Register

14.7.5.4.2.13.1 ADC_DMAREQ0 Register (Offset = ECh) [reset = 0h]

dma request.

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Table 14-13817. Instance Table

Instance Name	Physical Address
ADC0	2060 00ECh

Figure 14-6815. ADC_DMAREQ0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
DMAREQLEVEL							
R/W							
0h							

Table 14-13818. ADC_DMAREQ0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reserved
7:0	DMAREQLEVEL	R/W	0h	Number of words minus 1 in FIFO0 before generating a DMA request Reset Source: rst_mod_g_rst_n

14.7.5.4.2.14 ADC_FIFOCOUNT1 Register

14.7.5.4.2.14.1 ADC_FIFOCOUNT1 Register (Offset = F0h) [reset = 0h]

FIFO word count status

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Table 14-13819. Instance Table

Instance Name	Physical Address
ADC0	2060 00F0h

Figure 14-6816. ADC_FIFOCOUNT1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							NUMWDS
R							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUMWDS							
R							
0h							

Table 14-13820. ADC_FIFOCOUNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved
8:0	NUMWDS	R	0h	number of words in the FIFO Reset Source: rst_mod_g_rst_n

14.7.5.4.2.15 ADC_FIFOTHRESHOLD1 Register

14.7.5.4.2.15.1 ADC_FIFOTHRESHOLD1 Register (Offset = F4h) [reset = 0h]

FIFO threshold

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Table 14-13821. Instance Table

Instance Name	Physical Address
ADC0	2060 00F4h

Figure 14-6817. ADC_FIFOTHRESHOLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 14-13822. ADC_FIFOTHRESHOLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reserved
7:0	THRESHOLD	R/W	0h	Program the desired FIFO1 data sample level minus 1 to reach before generating interrupt to CPU Reset Source: rst_mod_g_rst_n

14.7.5.4.2.16 ADC_DMAREQ1 Register

14.7.5.4.2.16.1 ADC_DMAREQ1 Register (Offset = F8h) [reset = 0h]

dma request.

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Table 14-13823. Instance Table

Instance Name	Physical Address
ADC0	2060 00F8h

Figure 14-6818. ADC_DMAREQ1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
DMAREQLEVEL							
R/W							
0h							

Table 14-13824. ADC_DMAREQ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reserved
7:0	DMAREQLEVEL	R/W	0h	Number of words minus 1 in FIFO1 before generating a DMA request Reset Source: rst_mod_g_rst_n

14.7.5.4.2.17 ADC_FIFODATA0 Register

14.7.5.4.2.17.1 ADC_FIFODATA0 Register (Offset = 100h) [reset = 0h]

A read from this register will auto increment the FIFO read pointer. If you read when FIFO is empty,it will trigger an underflow interrupt

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Table 14-13825. Instance Table

Instance Name	Physical Address
ADC0	2060 0100h

Figure 14-6819. ADC_FIFODATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1				ADCCHANLID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				ADCDATA			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
ADCDATA							
R							
0h							

Table 14-13826. ADC_FIFODATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	Reserved
19:16	ADCCHANLID	R	0h	Optional ID tag of channel that captured the data. If tag option is disabled, these bits will be 0 Reset Source: rst_mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ADCDATA	R	0h	sampled ADC converted data value stored in FIFO Reset Source: rst_mod_g_rst_n

14.7.5.4.2.18 ADC_FIFODATA1 Register

14.7.5.4.2.18.1 ADC_FIFODATA1 Register (Offset = 200h) [reset = 0h]

A read from this register will auto increment the FIFO read pointer. If you read when FIFO is empty,it will trigger an underflow interrupt

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Table 14-13827. Instance Table

Instance Name	Physical Address
ADC0	2060 0200h

Figure 14-6820. ADC_FIFODATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1				ADCCHANLID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				ADCDATA			
NONE				R			
0h				0h			
7	6	5	4	3	2	1	0
ADCDATA							
R							
0h							

Table 14-13828. ADC_FIFODATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	Reserved
19:16	ADCCHANLID	R	0h	Optional ID tag of channel that captured the data. If tag option is disabled, these bits will be 0 Reset Source: rst_mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved
11:0	ADCDATA	R	0h	sampled ADC converted data value stored in FIFO Reset Source: rst_mod_g_rst_n

14.7.5.4.2.19 ADC_IRQ_EOI Register

14.7.5.4.2.19.1 ADC_IRQ_EOI Register (Offset = 20h) [reset = 0h]

The End of Interrupt (EOI) MISC Register allows the CPU to acknowledge completion of an interrupt by writing to the EOI for MISC interrupt sources. An eoi_write signal will be generated and another interrupt will be triggered if interrupt sources remain. This register will be reset one cycle after it has been written to.

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Table 14-13829. Instance Table

Instance Name	Physical Address
ADC0	2060 0020h

Figure 14-6821. ADC_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED31_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED31_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED31_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED31_1							LINENUMEOI
R							W
0h							0h

Table 14-13830. ADC_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED31_1	R	0h	Reserved
0	LINENUMEOI	W	0h	Write 0 to flag End Of Interrupt. Reset Source: rst_mod_g_rst_n

14.7.5.4.2.20 ADC_IRQSTATUS_RAW Register

14.7.5.4.2.20.1 ADC_IRQSTATUS_RAW Register (Offset = 24h) [reset = 0h]

The IRQ_STATUS_RAW register allows the adc12 interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 14-13831. Instance Table

Instance Name	Physical Address
ADC0	2060 0024h

Figure 14-6822. ADC_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							OUTOFRANGE
R							R/W1TS
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUENCE	AFE_EOC_MISSING
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13832. ADC_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved
8	OUTOFRANGE	R/W1TS	0h	sample out of range Reset Source: rst_mod_g_rst_n
7	FIFO1UNFL	R/W1TS	0h	fifo under flow Reset Source: rst_mod_g_rst_n
6	FIFO1OVFL	R/W1TS	0h	fifo over flow Reset Source: rst_mod_g_rst_n
5	FIFO1THRS	R/W1TS	0h	fifo thresholds met Reset Source: rst_mod_g_rst_n
4	FIFO0UNFL	R/W1TS	0h	fifo under flow Reset Source: rst_mod_g_rst_n
3	FIFO0OVFL	R/W1TS	0h	fifo over flow Reset Source: rst_mod_g_rst_n
2	FIFO0THRS	R/W1TS	0h	fifo thresholds met Reset Source: rst_mod_g_rst_n
1	ENDOFEQUENCE	R/W1TS	0h	end of sequence Reset Source: rst_mod_g_rst_n

Table 14-13832. ADC_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AFE_EOC_MISSING	R/W1TS	0h	eoc from the analog front end missing at expected time after soc Reset Source: rst_mod_g_rst_n

14.7.5.4.2.21 ADC_IRQSTATUS Register

14.7.5.4.2.21.1 ADC_IRQSTATUS Register (Offset = 28h) [reset = 0h]

The IRQ_STATUS register allows the adc12 interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 14-13833. Instance Table

Instance Name	Physical Address
ADC0	2060 0028h

Figure 14-6823. ADC_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							OUTOFRANGE
R							R/W1TC
0h							0h
7	6	5	4	3	2	1	0
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUENCE	AFE_EOC_MISSING
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13834. ADC_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved
8	OUTOFRANGE	R/W1TC	0h	sample out of range Reset Source: rst_mod_g_rst_n
7	FIFO1UNFL	R/W1TC	0h	fifo under flow Reset Source: rst_mod_g_rst_n
6	FIFO1OVFL	R/W1TC	0h	fifo over flow Reset Source: rst_mod_g_rst_n
5	FIFO1THRS	R/W1TC	0h	fifo thresholds met Reset Source: rst_mod_g_rst_n
4	FIFO0UNFL	R/W1TC	0h	fifo under flow Reset Source: rst_mod_g_rst_n
3	FIFO0OVFL	R/W1TC	0h	fifo over flow Reset Source: rst_mod_g_rst_n
2	FIFO0THRS	R/W1TC	0h	fifo thresholds met Reset Source: rst_mod_g_rst_n
1	ENDOFEQUENCE	R/W1TC	0h	end of sequence Reset Source: rst_mod_g_rst_n

Table 14-13834. ADC_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AFE_EOC_MISSING	R/W1TC	0h	eoc from the analog front end missing at expected time after soc Reset Source: rst_mod_g_rst_n

14.7.5.4.2.22 ADC_IRQENABLE_SET Register

14.7.5.4.2.22.1 ADC_IRQENABLE_SET Register (Offset = 2Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the adc12 interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-13835. Instance Table

Instance Name	Physical Address
ADC0	2060 002Ch

Figure 14-6824. ADC_IRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							OUTOFRANGE
R							R/W1TS
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUENCE	AFE_EOC_MISSING
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13836. ADC_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved
8	OUTOFRANGE	R/W1TS	0h	sample out of range Reset Source: rst_mod_g_rst_n
7	FIFO1UNFL	R/W1TS	0h	fifo under flow Reset Source: rst_mod_g_rst_n
6	FIFO1OVFL	R/W1TS	0h	fifo over flow Reset Source: rst_mod_g_rst_n
5	FIFO1THRS	R/W1TS	0h	fifo thresholds met Reset Source: rst_mod_g_rst_n
4	FIFO0UNFL	R/W1TS	0h	fifo under flow Reset Source: rst_mod_g_rst_n
3	FIFO0OVFL	R/W1TS	0h	fifo over flow Reset Source: rst_mod_g_rst_n
2	FIFO0THRS	R/W1TS	0h	fifo thresholds met Reset Source: rst_mod_g_rst_n
1	ENDOFEQUENCE	R/W1TS	0h	end of sequence Reset Source: rst_mod_g_rst_n

Table 14-13836. ADC_IRQENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AFE_EOC_MISSING	R/W1TS	0h	eoc from the analog front end missing at expected time after soc Reset Source: rst_mod_g_rst_n

14.7.5.4.2.23 ADC_IRQENABLE_CLR Register

14.7.5.4.2.23.1 ADC_IRQENABLE_CLR Register (Offset = 30h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the adc12 interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 14-13837. Instance Table

Instance Name	Physical Address
ADC0	2060 0030h

Figure 14-6825. ADC_IRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							OUTOFRANGE
R							R/W1TC
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUENCE	AFE_EOC_MISSING
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-13838. ADC_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved
8	OUTOFRANGE	R/W1TC	0h	sample out of range Reset Source: rst_mod_g_rst_n
7	FIFO1UNFL	R/W1TC	0h	fifo under flow Reset Source: rst_mod_g_rst_n
6	FIFO1OVFL	R/W1TC	0h	fifo over flow Reset Source: rst_mod_g_rst_n
5	FIFO1THRS	R/W1TC	0h	fifo thresholds met Reset Source: rst_mod_g_rst_n
4	FIFO0UNFL	R/W1TC	0h	fifo under flow Reset Source: rst_mod_g_rst_n
3	FIFO0OVFL	R/W1TC	0h	fifo over flow Reset Source: rst_mod_g_rst_n
2	FIFO0THRS	R/W1TC	0h	fifo thresholds met Reset Source: rst_mod_g_rst_n
1	ENDOFEQUENCE	R/W1TC	0h	end of sequence Reset Source: rst_mod_g_rst_n

Table 14-13838. ADC_IRQENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AFE_EOC_MISSING	R/W1TC	0h	eoc from the analog front end missing at expected time after soc Reset Source: rst_mod_g_rst_n

14.7.5.4.2.24 ADC_STEPCONFIG_j Register

14.7.5.4.2.24.1 ADC_STEPCONFIG_j Register (Offset = 0h) [reset = 40000h]

The user should write to this register the values of the input pins send to the AFE during step 1. the StepConfig WriteEnable bit should be set to 1 before a write can occur.

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Table 14-13839. Instance Table

Instance Name	Physical Address
ADC0	2060 0000h + formula

Figure 14-6826. ADC_STEPCONFIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED2				RANGECHECK	FIFOSEL	DIFF_CNTRL	RESERVED1
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED1	SEL_INP_SWC				SEL_INM_SWM		
R/W	R/W				R/W		
0h	0h				8h		
15	14	13	12	11	10	9	8
SEL_INM_SWM	RESERVED0						
R/W	R/W						
8h	0h						
7	6	5	4	3	2	1	0
RESERVED0			AVERAGING			MODE	
R/W			R/W			R/W	
0h			0h			0h	

Table 14-13840. ADC_STEPCONFIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED2	R	0h	Reserved
27	RANGECHECK	R/W	0h	0 = no range sel 1 = compare ADC data with range Reset Source: rst_mod_g_rst_n
26	FIFOSEL	R/W	0h	Sampled data will be stored in FIFO0 when = 0, FIFO1 when = 1 Reset Source: rst_mod_g_rst_n
25	DIFF_CNTRL	R/W	0h	Differential control. Single ended when = 0, differential input when = 1 Reset Source: rst_mod_g_rst_n
24:23	RESERVED1	R/W	0h	Reserved
22:19	SEL_INP_SWC	R/W	0h	SEL_INP pins SW configuration Reset Source: rst_mod_g_rst_n
18:15	SEL_INM_SWM	R/W	8h	SEL_INM pins, negative differential Reset Source: rst_mod_g_rst_n
14:5	RESERVED0	R/W	0h	Reserved

Table 14-13840. ADC_STEPCONFIG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:2	AVERAGING	R/W	0h	000 -> no average 001 -> 2 samples average 010 -> 4 samples average 011 -> 8 samples average 100 -> 16 samples average Reset Source: rst_mod_g_rst_n
1:0	MODE	R/W	0h	00 SW enabled one shot 01 SW enabled continuous 10 HW synchronized one-shot 11 HW synchronized continuous Reset Source: rst_mod_g_rst_n

14.7.5.4.2.25 ADC_STEPDELAY_j Register

14.7.5.4.2.25.1 ADC_STEPDELAY_j Register (Offset = 4h) [reset = 0h]

Controls number of clock periods to sample and delay

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Table 14-13841. Instance Table

Instance Name	Physical Address
ADC0	2060 0004h + formula

Figure 14-6827. ADC_STEPDELAY_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SAMPLEDELAY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED1</td><td colspan="2">OPENDELAY</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OPENDELAY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OPENDELAY</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13842. ADC_STEPDELAY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SAMPLEDELAY	R/W	0h	number of ADC clock cycles to sample. Any value programmed here will be added to the minimum requirement of 1 clock cycle. Reset Source: rst_mod_g_rst_n
23:18	RESERVED1	R	0h	Reserved
17:0	OPENDELAY	R/W	0h	Program the number of ADC clock cycles to wait after applying the step configuration registers and before sending the start of ADC conversion Reset Source: rst_mod_g_rst_n

14.7.6 Timer Module Registers

14.7.6.1 GTC

GTC

14.7.6.1.1 GTC Summaries

GTC Summaries

Table 14-13843. GTC_CFG0 Registers, Base Address=00A8 0000h, Length=1024

Offset	Length	Register Name	WKUP_GTC0 Physical Address
0h	32	GTC_CFG0_PID	00A8 0000h
4h	32	GTC_CFG0_GTC_PID	00A8 0004h
8h	32	GTC_CFG0_PUSHEVT	00A8 0008h

Table 14-13844. GTC_CFG1 Registers, Base Address=00A9 0000h, Length=16384

Offset	Length	Register Name	WKUP_GTC0 Physical Address
0h	32	GTC_CFG1_CNTCR	00A9 0000h
4h	32	GTC_CFG1_CNTSR	00A9 0004h
8h	32	GTC_CFG1_CNTCV_LO	00A9 0008h
Ch	32	GTC_CFG1_CNTCV_HI	00A9 000Ch
20h	32	GTC_CFG1_CNTFID0	00A9 0020h
24h	32	GTC_CFG1_CNTFID1	00A9 0024h

Table 14-13845. GTC_CFG2 Registers, Base Address=00AA 0000h, Length=16384

Offset	Length	Register Name	WKUP_GTC0 Physical Address
0h	32	GTC_CFG2_CNTCVS_LO	00AA 0000h
4h	32	GTC_CFG2_CNTCVS_HI	00AA 0004h

Table 14-13846. GTC_CFG3 Registers, Base Address=00AB 0000h, Length=16384

Offset	Length	Register Name	WKUP_GTC0 Physical Address
8h	32	GTC_CFG3_CNTTIDR	00AB 0008h

14.7.6.1.2 GTC Registers

GTC Registers

14.7.6.1.2.1 GTC_CFG0_PID Register

14.7.6.1.2.1.1 GTC_CFG0_PID Register (Offset = 0h) [reset = 61800209h]

PID register

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Table 14-13847. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A8 0000h

Figure 14-6828. GTC_CFG0_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PID_MSB16</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6180h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PID_MISC</td><td colspan="3">PID_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PID_CUSTOM</td><td colspan="6">PID_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">9h</td></tr>
</table>

Table 14-13848. GTC_CFG0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	9h	Reset Source: mod_g_rst_n

14.7.6.1.2.2 GTC_CFG0_GTC_PID Register

14.7.6.1.2.2.1 GTC_CFG0_GTC_PID Register (Offset = 4h) [reset = 661A0000h]

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Table 14-13849. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A8 0004h

Figure 14-6829. GTC_CFG0_GTC_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">GTC_PID_SCHEME</td><td colspan="2">GTC_PID_BU</td><td colspan="4">GTC_PID_FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">61Ah</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">GTC_PID_FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">61Ah</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">GTC_PID_R_RTL</td><td colspan="3">GTC_PID_X_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">X</td><td colspan="3">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">GTC_PID_CUSTOM</td><td colspan="6">GTC_PID_Y_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">X</td><td colspan="6">X</td></tr>
</table>

Table 14-13850. GTC_CFG0_GTC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	GTC_PID_SCHEME	R	1h	PID follows new scheme Reset Source: mod_por_rst_n
29:28	GTC_PID_BU	R	2h	Business unit - Processors Reset Source: mod_por_rst_n
27:16	GTC_PID_FUNC	R	61Ah	Module functional identifier - GTC module Reset Source: mod_por_rst_n
15:11	GTC_PID_R_RTL	R	X	RTL revision number - actual value determined by RTL Reset Source: mod_por_rst_n
10:8	GTC_PID_X_MAJOR	R	X	Major revision number - actual value determined by RTL Reset Source: mod_por_rst_n
7:6	GTC_PID_CUSTOM	R	X	Custom revision number - actual value determined by RTL Reset Source: mod_por_rst_n
5:0	GTC_PID_Y_MINOR	R	X	Minor revision number - actual value determined by RTL Reset Source: mod_por_rst_n

14.7.6.1.2.3 GTC_CFG0_PUSHEVT Register

14.7.6.1.2.3.1 GTC_CFG0_PUSHEVT Register (Offset = 8h) [reset = 0h]

Selects which bit of the count value to output as a push event for global timesync

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Table 14-13851. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A8 0008h

Figure 14-6830. GTC_CFG0_PUSHEVT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		PUSHEVT_EXPBIT_SEL					
NONE		R/W					
0h		0h					

Table 14-13852. GTC_CFG0_PUSHEVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	PUSHEVT_EXPBIT_SEL	R/W	0h	Selects which bit [63:0] of the System Counter value is exported on the push_evt output. This field controls the 64:1 mux that drives the push_evt output. Reset Source: mod_por_rst_n

14.7.6.1.2.4 GTC_CFG1_CNTCR Register

14.7.6.1.2.4.1 GTC_CFG1_CNTCR Register (Offset = 0h) [reset = 0h]

Enables the System Counter and controls counter operation during debug

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Table 14-13853. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A9 0000h

Figure 14-6831. GTC_CFG1_CNTCR Name Register

31	30	29	28	27	26	25	24
CNTCR_FCREQ							
R							
0h							
23	22	21	20	19	18	17	16
CNTCR_FCREQ							
R							
0h							
15	14	13	12	11	10	9	8
CNTCR_FCREQ							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						CNTCR_HDBG	CNTCR_EN
NONE						R/W	R/W
0h						0h	0h

Table 14-13854. GTC_CFG1_CNTCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CNTCR_FCREQ	R	0h	Frequency Change Request Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1	CNTCR_HDBG	R/W	0h	Halt on Debug Reset Source: mod_por_rst_n
0	CNTCR_EN	R/W	0h	Enable System Counter Reset Source: mod_por_rst_n

14.7.6.1.2.5 GTC_CFG1_CNTSR Register

14.7.6.1.2.5.1 GTC_CFG1_CNTSR Register (Offset = 4h) [reset = 0h]

Provides System Counter frequency status information

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Table 14-13855. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A9 0004h

Figure 14-6832. GTC_CFG1_CNTSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CNTSR_FCACK</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CNTSR_FCACK</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CNTSR_FCACK</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>CNTSR_DBGH</td><td>RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="6">0h</td><td>X</td><td>0h</td></tr>
</table>

Table 14-13856. GTC_CFG1_CNTSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	CNTSR_FCACK	R	0h	Frequency Change Ackowledge Reset Source: mod_por_rst_n
7:2	RESERVED	NONE	0h	Reserved
1	CNTSR_DBGH	R	X	Debug Halt Reset Source: mod_por_rst_n
0	RESERVED	NONE	0h	Reserved

14.7.6.1.2.6 GTC_CFG1_CNTCV_LO Register

14.7.6.1.2.6.1 GTC_CFG1_CNTCV_LO Register (Offset = 8h) [reset = 0h]

Indicates the current System Counter count value and can be used to set the System Counter count value

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Table 14-13857. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A9 0008h

Figure 14-6833. GTC_CFG1_CNTCV_LO Name Register

31	30	29	28	27	26	25	24
CNTCV_LO_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCV_LO_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCV_LO_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCV_LO_COUNTVALUE							
R							
X							

Table 14-13858. GTC_CFG1_CNTCV_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCV_LO_COUNTVALUE	R	X	Indicates bits [31:0] of the System Counter value. Reset Source: mod_por_rst_n

14.7.6.1.2.7 GTC_CFG1_CNTCV_HI Register

14.7.6.1.2.7.1 GTC_CFG1_CNTCV_HI Register (Offset = Ch) [reset = 0h]

Indicates the current System Counter count value and can be used to set the System Counter count value

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Table 14-13859. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A9 000Ch

Figure 14-6834. GTC_CFG1_CNTCV_HI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CNTCV_HI_COUNTVALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CNTCV_HI_COUNTVALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CNTCV_HI_COUNTVALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CNTCV_HI_COUNTVALUE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">X</td></tr>
</table>

Table 14-13860. GTC_CFG1_CNTCV_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCV_HI_COUNTVALUE	R	X	Indicates bits [63:32] of the System Counter value. Reset Source: mod_por_rst_n

14.7.6.1.2.8 GTC_CFG1_CNTFID0 Register

14.7.6.1.2.8.1 GTC_CFG1_CNTFID0 Register (Offset = 20h) [reset = 0h]

Indicates base frequency of the System Counter

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Table 14-13861. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A9 0020h

Figure 14-6835. GTC_CFG1_CNTFID0 Name Register

31	30	29	28	27	26	25	24
CNTFID0_FREQVALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
CNTFID0_FREQVALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
CNTFID0_FREQVALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTFID0_FREQVALUE							
R/W							
0h							

Table 14-13862. GTC_CFG1_CNTFID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTFID0_FREQVALUE	R/W	0h	Indicates the base update frequency of the System Counter in Hz. Reset Source: mod_por_rst_n

14.7.6.1.2.9 GTC_CFG1_CNTFID1 Register

14.7.6.1.2.9.1 GTC_CFG1_CNTFID1 Register (Offset = 24h) [reset = 0h]

Indicates base frequency of the System Counter

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Table 14-13863. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00A9 0024h

Figure 14-6836. GTC_CFG1_CNTFID1 Name Register

31	30	29	28	27	26	25	24
CNTFID1_FREQVALUE							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CNTFID1_FREQVALUE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CNTFID1_FREQVALUE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CNTFID1_FREQVALUE							
R							
0h							

Table 14-13864. GTC_CFG1_CNTFID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTFID1_FREQVALUE	R	0h	Frequency table end indicator Reset Source: mod_por_rst_n

14.7.6.1.2.10 GTC_CFG2_CNTCVS_LO Register

14.7.6.1.2.10.1 GTC_CFG2_CNTCVS_LO Register (Offset = 0h) [reset = 0h]

Return to Summary Table

Table 14-13865. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00AA 0000h

Figure 14-6837. GTC_CFG2_CNTCVS_LO Name Register

31	30	29	28	27	26	25	24
CNTCVS_LO_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCVS_LO_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCVS_LO_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCVS_LO_COUNTVALUE							
R							
X							

Table 14-13866. GTC_CFG2_CNTCVS_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCVS_LO_COUNTVALUE	R	X	Indicates bits [31:0] of the System Counter value. Reset Source: mod_por_rst_n

14.7.6.1.2.11 GTC_CFG2_CNTCVS_HI Register

14.7.6.1.2.11.1 GTC_CFG2_CNTCVS_HI Register (Offset = 4h) [reset = 0h]

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Table 14-13867. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00AA 0004h

Figure 14-6838. GTC_CFG2_CNTCVS_HI Name Register

31	30	29	28	27	26	25	24
CNTCVS_HI_COUNTVALUE							
R							
X							
23	22	21	20	19	18	17	16
CNTCVS_HI_COUNTVALUE							
R							
X							
15	14	13	12	11	10	9	8
CNTCVS_HI_COUNTVALUE							
R							
X							
7	6	5	4	3	2	1	0
CNTCVS_HI_COUNTVALUE							
R							
X							

Table 14-13868. GTC_CFG2_CNTCVS_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTCVS_HI_COUNTVALUE	R	X	Indicates bits [63:32] of the System Counter value. Reset Source: mod_por_rst_n

14.7.6.1.2.12 GTC_CFG3_CNTTIDR Register

14.7.6.1.2.12.1 GTC_CFG3_CNTTIDR Register (Offset = 8h) [reset = 0h]

This register is set to all 0s.

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Table 14-13869. Instance Table

Instance Name	Physical Address
WKUP_GTC0	00AB 0008h

Figure 14-6839. GTC_CFG3_CNTTIDR Name Register

31	30	29	28	27	26	25	24
CNTTIDR_FRAME7				CNTTIDR_FRAME6			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
CNTTIDR_FRAME5				CNTTIDR_FRAME4			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
CNTTIDR_FRAME3				CNTTIDR_FRAME2			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
CNTTIDR_FRAME1				CNTTIDR_FRAME0			
R				R			
0h				0h			

Table 14-13870. GTC_CFG3_CNTTIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	CNTTIDR_FRAME7	R	0h	Indicates the features of timer frame7. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
27:24	CNTTIDR_FRAME6	R	0h	Indicates the features of timer frame6. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
23:20	CNTTIDR_FRAME5	R	0h	Indicates the features of timer frame5. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
19:16	CNTTIDR_FRAME4	R	0h	Indicates the features of timer frame4. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
15:12	CNTTIDR_FRAME3	R	0h	Indicates the features of timer frame3. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
11:8	CNTTIDR_FRAME2	R	0h	Indicates the features of timer frame2. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n
7:4	CNTTIDR_FRAME1	R	0h	Indicates the features of timer frame1. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n

Table 14-13870. GTC_CFG3_CNTTIDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CNTTIDR_FRAME0	R	0h	Indicates the features of timer frame0. Each 4 bit field has the following meaning: Reset Source: mod_por_rst_n

14.7.6.2 RTI_CFG1

RTI_CFG1

14.7.6.2.1 RTI_CFG1 Summaries

RTI_CFG1 Summaries

Table 14-13871. RTI_CFG1_RTI Registers, Base Address=0E00 0000h, Length=256

Offset	Length	Register Name	RTI4 Physical Address	RTI5 Physical Address	RTI0 Physical Address
0h	32	RTI_CFG1_RTI_RTIGCTRL	0E00 0000h	0E01 0000h	2080 0000h
4h	32	RTI_CFG1_RTI_RTITBCTRL	0E00 0004h	0E01 0004h	2080 0004h
8h	32	RTI_CFG1_RTI_RTICAPCTRL	0E00 0008h	0E01 0008h	2080 0008h
Ch	32	RTI_CFG1_RTI_RTICOMPCTRL	0E00 000Ch	0E01 000Ch	2080 000Ch
10h	32	RTI_CFG1_RTI_RTIFRC0	0E00 0010h	0E01 0010h	2080 0010h
14h	32	RTI_CFG1_RTI_RTIUC0	0E00 0014h	0E01 0014h	2080 0014h
18h	32	RTI_CFG1_RTI_RTICPUC0	0E00 0018h	0E01 0018h	2080 0018h
20h	32	RTI_CFG1_RTI_RTICAFRC0	0E00 0020h	0E01 0020h	2080 0020h
24h	32	RTI_CFG1_RTI_RTICAUC0	0E00 0024h	0E01 0024h	2080 0024h
30h	32	RTI_CFG1_RTI_RTIFRC1	0E00 0030h	0E01 0030h	2080 0030h
34h	32	RTI_CFG1_RTI_RTIUC1	0E00 0034h	0E01 0034h	2080 0034h
38h	32	RTI_CFG1_RTI_RTICPUC1	0E00 0038h	0E01 0038h	2080 0038h
40h	32	RTI_CFG1_RTI_RTICAFRC1	0E00 0040h	0E01 0040h	2080 0040h
44h	32	RTI_CFG1_RTI_RTICAUC1	0E00 0044h	0E01 0044h	2080 0044h
50h	32	RTI_CFG1_RTI_RTICOMP0	0E00 0050h	0E01 0050h	2080 0050h
54h	32	RTI_CFG1_RTI_RTIUDCP0	0E00 0054h	0E01 0054h	2080 0054h
58h	32	RTI_CFG1_RTI_RTICOMP1	0E00 0058h	0E01 0058h	2080 0058h
5Ch	32	RTI_CFG1_RTI_RTIUDCP1	0E00 005Ch	0E01 005Ch	2080 005Ch
60h	32	RTI_CFG1_RTI_RTICOMP2	0E00 0060h	0E01 0060h	2080 0060h
64h	32	RTI_CFG1_RTI_RTIUDCP2	0E00 0064h	0E01 0064h	2080 0064h
68h	32	RTI_CFG1_RTI_RTICOMP3	0E00 0068h	0E01 0068h	2080 0068h
6Ch	32	RTI_CFG1_RTI_RTIUDCP3	0E00 006Ch	0E01 006Ch	2080 006Ch
70h	32	RTI_CFG1_RTI_RTITBLCOMP	0E00 0070h	0E01 0070h	2080 0070h
74h	32	RTI_CFG1_RTI_RTITBHCOMP	0E00 0074h	0E01 0074h	2080 0074h
80h	32	RTI_CFG1_RTI_RTISETINT	0E00 0080h	0E01 0080h	2080 0080h
84h	32	RTI_CFG1_RTI_RTICLEARINT	0E00 0084h	0E01 0084h	2080 0084h
88h	32	RTI_CFG1_RTI_RTIINTFLAG	0E00 0088h	0E01 0088h	2080 0088h
90h	32	RTI_CFG1_RTI_RTIDWDCTRL	0E00 0090h	0E01 0090h	2080 0090h
94h	32	RTI_CFG1_RTI_RTIDWDPRLD	0E00 0094h	0E01 0094h	2080 0094h
98h	32	RTI_CFG1_RTI_RTIWDSTATUS	0E00 0098h	0E01 0098h	2080 0098h
9Ch	32	RTI_CFG1_RTI_RTIWDKEY	0E00 009Ch	0E01 009Ch	2080 009Ch
A0h	32	RTI_CFG1_RTI_RTIDWDCNTR	0E00 00A0h	0E01 00A0h	2080 00A0h
A4h	32	RTI_CFG1_RTI_RTIDWWDRXNCTRL	0E00 00A4h	0E01 00A4h	2080 00A4h
A8h	32	RTI_CFG1_RTI_RTIDWWDSIZECTRL	0E00 00A8h	0E01 00A8h	2080 00A8h
ACh	32	RTI_CFG1_RTI_RTIINTCLRENABLE	0E00 00ACh	0E01 00ACh	2080 00ACh
B0h	32	RTI_CFG1_RTI_RTICOMP0CLR	0E00 00B0h	0E01 00B0h	2080 00B0h
B4h	32	RTI_CFG1_RTI_RTICOMP1CLR	0E00 00B4h	0E01 00B4h	2080 00B4h
B8h	32	RTI_CFG1_RTI_RTICOMP2CLR	0E00 00B8h	0E01 00B8h	2080 00B8h

Table 14-13871. RTI_CFG1_RTI Registers, Base Address=0E00 0000h, Length=256 (continued)

Offset	Length	Register Name	RTI4 Physical Address	RTI5 Physical Address	RTI0 Physical Address
BCh	32	RTI_CFG1_RTI_RTICOMP3CLR	0E00 00BCh	0E01 00BCh	2080 00BCh

Table 14-13872. RTI_CFG1_RTI Registers, Base Address=0E00 0000h, Length=256

Offset	Length	Register Name	RTI1 Physical Address	RTI2 Physical Address	RTI3 Physical Address
0h	32	RTI_CFG1_RTI_RTIGCTRL	2081 0000h	2082 0000h	2083 0000h
4h	32	RTI_CFG1_RTI_RTITBCTRL	2081 0004h	2082 0004h	2083 0004h
8h	32	RTI_CFG1_RTI_RTICAPCTRL	2081 0008h	2082 0008h	2083 0008h
Ch	32	RTI_CFG1_RTI_RTICOMPCTRL	2081 000Ch	2082 000Ch	2083 000Ch
10h	32	RTI_CFG1_RTI_RTIFRC0	2081 0010h	2082 0010h	2083 0010h
14h	32	RTI_CFG1_RTI_RTIUC0	2081 0014h	2082 0014h	2083 0014h
18h	32	RTI_CFG1_RTI_RTICPUC0	2081 0018h	2082 0018h	2083 0018h
20h	32	RTI_CFG1_RTI_RTICAFRC0	2081 0020h	2082 0020h	2083 0020h
24h	32	RTI_CFG1_RTI_RTICAUC0	2081 0024h	2082 0024h	2083 0024h
30h	32	RTI_CFG1_RTI_RTIFRC1	2081 0030h	2082 0030h	2083 0030h
34h	32	RTI_CFG1_RTI_RTIUC1	2081 0034h	2082 0034h	2083 0034h
38h	32	RTI_CFG1_RTI_RTICPUC1	2081 0038h	2082 0038h	2083 0038h
40h	32	RTI_CFG1_RTI_RTICAFRC1	2081 0040h	2082 0040h	2083 0040h
44h	32	RTI_CFG1_RTI_RTICAUC1	2081 0044h	2082 0044h	2083 0044h
50h	32	RTI_CFG1_RTI_RTICOMP0	2081 0050h	2082 0050h	2083 0050h
54h	32	RTI_CFG1_RTI_RTIUDCP0	2081 0054h	2082 0054h	2083 0054h
58h	32	RTI_CFG1_RTI_RTICOMP1	2081 0058h	2082 0058h	2083 0058h
5Ch	32	RTI_CFG1_RTI_RTIUDCP1	2081 005Ch	2082 005Ch	2083 005Ch
60h	32	RTI_CFG1_RTI_RTICOMP2	2081 0060h	2082 0060h	2083 0060h
64h	32	RTI_CFG1_RTI_RTIUDCP2	2081 0064h	2082 0064h	2083 0064h
68h	32	RTI_CFG1_RTI_RTICOMP3	2081 0068h	2082 0068h	2083 0068h
6Ch	32	RTI_CFG1_RTI_RTIUDCP3	2081 006Ch	2082 006Ch	2083 006Ch
70h	32	RTI_CFG1_RTI_RTITBLCOMP	2081 0070h	2082 0070h	2083 0070h
74h	32	RTI_CFG1_RTI_RTITBHCOMP	2081 0074h	2082 0074h	2083 0074h
80h	32	RTI_CFG1_RTI_RTISETINT	2081 0080h	2082 0080h	2083 0080h
84h	32	RTI_CFG1_RTI_RTICLEARINT	2081 0084h	2082 0084h	2083 0084h
88h	32	RTI_CFG1_RTI_RTIINTFLAG	2081 0088h	2082 0088h	2083 0088h
90h	32	RTI_CFG1_RTI_RTIDWDCTRL	2081 0090h	2082 0090h	2083 0090h
94h	32	RTI_CFG1_RTI_RTIDWDPRLD	2081 0094h	2082 0094h	2083 0094h
98h	32	RTI_CFG1_RTI_RTIWDSTATUS	2081 0098h	2082 0098h	2083 0098h
9Ch	32	RTI_CFG1_RTI_RTIWDKEY	2081 009Ch	2082 009Ch	2083 009Ch
A0h	32	RTI_CFG1_RTI_RTIDWDCNTR	2081 00A0h	2082 00A0h	2083 00A0h
A4h	32	RTI_CFG1_RTI_RTIDWWDRXNCTRL	2081 00A4h	2082 00A4h	2083 00A4h
A8h	32	RTI_CFG1_RTI_RTIDWWDSIZECTRL	2081 00A8h	2082 00A8h	2083 00A8h
ACh	32	RTI_CFG1_RTI_RTIINTCLRENABLE	2081 00ACh	2082 00ACh	2083 00ACh
B0h	32	RTI_CFG1_RTI_RTICOMP0CLR	2081 00B0h	2082 00B0h	2083 00B0h
B4h	32	RTI_CFG1_RTI_RTICOMP1CLR	2081 00B4h	2082 00B4h	2083 00B4h
B8h	32	RTI_CFG1_RTI_RTICOMP2CLR	2081 00B8h	2082 00B8h	2083 00B8h
BCh	32	RTI_CFG1_RTI_RTICOMP3CLR	2081 00BCh	2082 00BCh	2083 00BCh

14.7.6.2.2 RTI_CFG1 Registers

RTI_CFG1 Registers

14.7.6.2.2.1 RTI_CFG1_RTI_RTIGCTRL Register

14.7.6.2.2.1.1 RTI_CFG1_RTI_RTIGCTRL Register (Offset = 0h) [reset = 0h]

RTI Global Control Register

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Table 14-13873. Instance Table

Instance Name	Physical Address
RTI4	0E00 0000h
RTI5	0E01 0000h
RTI0	2080 0000h
RTI1	2081 0000h
RTI2	2082 0000h
RTI3	2083 0000h
WKUP_RTI0	2B00 0000h

Figure 14-6840. RTI_CFG1_RTI_RTIGCTRL Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED				NTUSEL			
NONE				R/W			
0h				0h			
16	15	14	13	12	11	10	9
COS	RESERVED						
R/W	NONE						
0h	0h						
8	7	6	5	4	3	2	1
RESERVED						CNT1EN	CNT0EN
NONE						R/W	R/W
0h						0h	0h

Table 14-13874. RTI_CFG1_RTI_RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	NTUSEL	R/W	0h	These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL. User and privilege mode (read): 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to '0' Privilege mode (write): 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to '0' Reset Source: mod_g_rst_n
15	COS	R/W	0h	This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting. User and privilege mode (read): 0 = counters are stopped while in debug mode 1 = counters are running while in debug mode Privilege mode (write): 0 = stop counters in debug mode 1 = continue counting in debug mode Reset Source: mod_g_rst_n

Table 14-13874. RTI_CFG1_RTI_RTIGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:2	RESERVED	NONE	0h	Reserved
1	CNT1EN	R/W	0h	The CNT1EN bit starts and stops the operation of counter block 1 (UC1 and FRC1). User and privilege mode (read): 0 = counters are stopped 1 = counters are running Privilege mode (write): 0 = stop counters 1 = start counters Reset Source: mod_g_rst_n
0	CNT0EN	R/W	0h	The CNT0EN bit starts and stops the operation of counter block 0 (UC0 and FRC0). User and privilege mode (read): 0 = counters are stopped 1 = counters are running Privilege mode (write): 0 = stop counters 1 = start counters Reset Source: mod_g_rst_n

14.7.6.2.2.2 RTI_CFG1_RTI_RTITBCTRL Register

14.7.6.2.2.2.1 RTI_CFG1_RTI_RTITBCTRL Register (Offset = 4h) [reset = 0h]

RTI Timebase Control Register

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Table 14-13875. Instance Table

Instance Name	Physical Address
RTI4	0E00 0004h
RTI5	0E01 0004h
RTI0	2080 0004h
RTI1	2081 0004h
RTI2	2082 0004h
RTI3	2083 0004h
WKUP_RTI0	2B00 0004h

Figure 14-6841. RTI_CFG1_RTI_RTITBCTRL Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="6">RESERVED</td><td>INC</td><td>TBEXT</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-13876. RTI_CFG1_RTI_RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	INC	R/W	0h	This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected. User and privilege mode (read): 0 = FRC0 will not be incremented 1 = FRC0 will be incremented Privilege mode (write): 0 = Do not increment FRC0 on failing external clock 1 = Increment FRC0 on failing external clock Reset Source: mod_g_rst_n

Table 14-13876. RTI_CFG1_RTI_RTITBCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TBEXT	R/W	0h	The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx. When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset. The selection if the external signal should be used, can only be done by software. User and privilege mode (read): 0 = UC0 clocks FRC0 1 = NTUx clocks FRC0 Privilege mode (write): 0 = MUX is switched to internal UC0 clocking scheme 1 = MUX is switched to external NTUx clocking scheme Reset Source: mod_g_rst_n

14.7.6.2.2.3 RTI_CFG1_RTI_RTICAPCTRL Register

14.7.6.2.2.3.1 RTI_CFG1_RTI_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

RTI Capture Control Register

Return to Summary Table

Table 14-13877. Instance Table

Instance Name	Physical Address
RTI4	0E00 0008h
RTI5	0E01 0008h
RTI0	2080 0008h
RTI1	2081 0008h
RTI2	2082 0008h
RTI3	2083 0008h
WKUP_RTI0	2B00 0008h

Figure 14-6842. RTI_CFG1_RTI_RTICAPCTRL Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
RESERVED							
NONE							
0h							
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
RESERVED							
NONE							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
RESERVED						CAPCNTR1	CAPCNTR0
NONE						R/W	R/W
0h						0h	0h

Table 14-13878. RTI_CFG1_RTI_RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	CAPCNTR1	R/W	0h	This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1. User and privilege mode (read): 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode (write): 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 Reset Source: mod_g_rst_n
0	CAPCNTR0	R/W	0h	This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0. User and privilege mode (read): 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode (write): 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 Reset Source: mod_g_rst_n

14.7.6.2.2.4 RTI_CFG1_RTI_RTICOMPCTRL Register

14.7.6.2.2.4.1 RTI_CFG1_RTI_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

RTI Compare Control Register

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Table 14-13879. Instance Table

Instance Name	Physical Address
RTI4	0E00 000Ch
RTI5	0E01 000Ch
RTI0	2080 000Ch
RTI1	2081 000Ch
RTI2	2082 000Ch
RTI3	2083 000Ch
WKUP_RTI0	2B00 000Ch

Figure 14-6843. RTI_CFG1_RTI_RTICOMPCTRL Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="3">RESERVED</td><td>COMPSEL3</td><td colspan="3">RESERVED</td><td>COMPSEL2</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="3">RESERVED</td><td>COMPSEL1</td><td colspan="3">RESERVED</td><td>COMPSEL0</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="3">NONE</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-13880. RTI_CFG1_RTI_RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	COMPSEL3	R/W	0h	This bit determines the counter with which the compare value hold in compare register 3 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE	0h	Reserved
8	COMPSEL2	R/W	0h	This bit determines the counter with which the compare value hold in compare register 2 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE	0h	Reserved

Table 14-13880. RTI_CFG1_RTI_RTICOMPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	COMPSEL1	R/W	0h	This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE	0h	Reserved
0	COMPSEL0	R/W	0h	This bit determines the counter with which the compare value hold in compare register 0 is compared. User and privilege mode (read): 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode (write): 0 = enable compare with FRC 0 1 = enable compare with FRC 1 Reset Source: mod_g_rst_n

14.7.6.2.2.5 RTI_CFG1_RTI_RTIFRC0 Register

14.7.6.2.2.5.1 RTI_CFG1_RTI_RTIFRC0 Register (Offset = 10h) [reset = 0h]

RTI Free Running Counter 0 Register

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Table 14-13881. Instance Table

Instance Name	Physical Address
RTI4	0E00 0010h
RTI5	0E01 0010h
RTI0	2080 0010h
RTI1	2081 0010h
RTI2	2082 0010h
RTI3	2083 0010h
WKUP_RTI0	2B00 0010h

Figure 14-6844. RTI_CFG1_RTI_RTIFRC0 Name Register

32	31	30	29	28	27	26	25
FRC0							
R/W							
0h							
24	23	22	21	20	19	18	17
FRC0							
R/W							
0h							
16	15	14	13	12	11	10	9
FRC0							
R/W							
0h							
8	7	6	5	4	3	2	1
FRC0							
R/W							
0h							

Table 14-13882. RTI_CFG1_RTI_RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC0	R/W	0h	This registers holds the current value of the Free Running Counter 0 and will be updated continuously. User and privilege mode (read): current value of the counter Privilege mode (write): The counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Reset Source: mod_g_rst_n

14.7.6.2.2.6 RTI_CFG1_RTI_RTIUC0 Register

14.7.6.2.2.6.1 RTI_CFG1_RTI_RTIUC0 Register (Offset = 14h) [reset = 0h]

RTI Up Counter 0 Register

Return to Summary Table

Table 14-13883. Instance Table

Instance Name	Physical Address
RTI4	0E00 0014h
RTI5	0E01 0014h
RTI0	2080 0014h
RTI1	2081 0014h
RTI2	2082 0014h
RTI3	2083 0014h
WKUP_RTI0	2B00 0014h

Figure 14-6845. RTI_CFG1_RTI_RTIUC0 Name Register

32	31	30	29	28	27	26	25
UC0							
R/W							
0h							
24	23	22	21	20	19	18	17
UC0							
R/W							
0h							
16	15	14	13	12	11	10	9
UC0							
R/W							
0h							
8	7	6	5	4	3	2	1
UC0							
R/W							
0h							

Table 14-13884. RTI_CFG1_RTI_RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC0	R/W	0h	This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0. User and privilege mode (read): value of the counter when the Free Running Counter 0 was read Privilege mode (write): the counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows. Reset Source: mod_g_rst_n

14.7.6.2.2.7 RTI_CFG1_RTI_RTICPUC0 Register

14.7.6.2.2.7.1 RTI_CFG1_RTI_RTICPUC0 Register (Offset = 18h) [reset = 0h]

RTI Compare Up Counter 0 Register

Return to Summary Table

Table 14-13885. Instance Table

Instance Name	Physical Address
RTI4	0E00 0018h
RTI5	0E01 0018h
RTI0	2080 0018h
RTI1	2081 0018h
RTI2	2082 0018h
RTI3	2083 0018h
WKUP_RTI0	2B00 0018h

Figure 14-6846. RTI_CFG1_RTI_RTICPUC0 Name Register

32	31	30	29	28	27	26	25
CPUC0							
R/W							
0h							
24	23	22	21	20	19	18	17
CPUC0							
R/W							
0h							
16	15	14	13	12	11	10	9
CPUC0							
R/W							
0h							
8	7	6	5	4	3	2	1
CPUC0							
R/W							
0h							

Table 14-13886. RTI_CFG1_RTI_RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC0	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock. If CPUC0 = 0: fFRC0 = R-----T---I---C----L----K-- 232 If CPUC0 0: fFRC0 = ----R----T----I--C-----L---K------- CPUC0 + 1 User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Reset Source: mod_g_rst_n

14.7.6.2.2.8 RTI_CFG1_RTI_RTICAFRC0 Register

14.7.6.2.2.8.1 RTI_CFG1_RTI_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

RTI Capture Free Running Counter 0 Register

Return to Summary Table

Table 14-13887. Instance Table

Instance Name	Physical Address
RTI4	0E00 0020h
RTI5	0E01 0020h
RTI0	2080 0020h
RTI1	2081 0020h
RTI2	2082 0020h
RTI3	2083 0020h
WKUP_RTI0	2B00 0020h

Figure 14-6847. RTI_CFG1_RTI_RTICAFRC0 Name Register

32	31	30	29	28	27	26	25
CAFRC0							
R							
0h							
24	23	22	21	20	19	18	17
CAFRC0							
R							
0h							
16	15	14	13	12	11	10	9
CAFRC0							
R							
0h							
8	7	6	5	4	3	2	1
CAFRC0							
R							
0h							

Table 14-13888. RTI_CFG1_RTI_RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC0	R	0h	This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block. User and privilege mode (read): value of Free Running Counter 0 on a capture event Reset Source: mod_g_rst_n

14.7.6.2.2.9 RTI_CFG1_RTI_RTICAUC0 Register

14.7.6.2.2.9.1 RTI_CFG1_RTI_RTICAUC0 Register (Offset = 24h) [reset = 0h]

RTI Capture Up Counter 0 Register

Return to Summary Table

Table 14-13889. Instance Table

Instance Name	Physical Address
RTI4	0E00 0024h
RTI5	0E01 0024h
RTI0	2080 0024h
RTI1	2081 0024h
RTI2	2082 0024h
RTI3	2083 0024h
WKUP_RTI0	2B00 0024h

Figure 14-6848. RTI_CFG1_RTI_RTICAUC0 Name Register

32	31	30	29	28	27	26	25
CAUC0							
R							
0h							
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
CAUC0							
R							
0h							
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
CAUC0							
R							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
CAUC0							
R							
0h							

Table 14-13890. RTI_CFG1_RTI_RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC0	R	0h	This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode (read): value of Up Counter 0 on a capture event Reset Source: mod_g_rst_n

14.7.6.2.2.10 RTI_CFG1_RTI_RTIFRC1 Register

14.7.6.2.2.10.1 RTI_CFG1_RTI_RTIFRC1 Register (Offset = 30h) [reset = 0h]

RTI Free Running Counter 1 Register

Return to Summary Table

Table 14-13891. Instance Table

Instance Name	Physical Address
RTI4	0E00 0030h
RTI5	0E01 0030h
RTI0	2080 0030h
RTI1	2081 0030h
RTI2	2082 0030h
RTI3	2083 0030h
WKUP_RTI0	2B00 0030h

Figure 14-6849. RTI_CFG1_RTI_RTIFRC1 Name Register

32	31	30	29	28	27	26	25
FRC1							
R/W							
0h							
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
FRC1							
R/W							
0h							
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
FRC1							
R/W							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
FRC1							
R/W							
0h							

Table 14-13892. RTI_CFG1_RTI_RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC1	R/W	0h	This registers holds the current value of the Free Running Counter 1 and will be updated continuously. User and privilege mode (read): current value of the counter Privilege mode (write): the counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1. Reset Source: mod_g_rst_n

14.7.6.2.2.11 RTI_CFG1_RTI_RTIUC1 Register

14.7.6.2.2.11.1 RTI_CFG1_RTI_RTIUC1 Register (Offset = 34h) [reset = 0h]

RTI Up Counter 1 Register

Return to Summary Table

Table 14-13893. Instance Table

Instance Name	Physical Address
RTI4	0E00 0034h
RTI5	0E01 0034h
RTI0	2080 0034h
RTI1	2081 0034h
RTI2	2082 0034h
RTI3	2083 0034h
WKUP_RTI0	2B00 0034h

Figure 14-6850. RTI_CFG1_RTI_RTIUC1 Name Register

32	31	30	29	28	27	26	25
UC1							
R/W							
0h							
24	23	22	21	20	19	18	17
UC1							
R/W							
0h							
16	15	14	13	12	11	10	9
UC1							
R/W							
0h							
8	7	6	5	4	3	2	1
UC1							
R/W							
0h							

Table 14-13894. RTI_CFG1_RTI_RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC1	R/W	0h	This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1. User and privilege mode (read): value of the counter when the Free Running Counter 1 was read Privilege mode (write): the counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be disabled in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since UC1 has to count up until it overflows. Reset Source: mod_g_rst_n

14.7.6.2.2.12 RTI_CFG1_RTI_RTICPUC1 Register

14.7.6.2.2.12.1 RTI_CFG1_RTI_RTICPUC1 Register (Offset = 38h) [reset = 0h]

RTI Compare Up Counter 1 Register

Return to Summary Table

Table 14-13895. Instance Table

Instance Name	Physical Address
RTI4	0E00 0038h
RTI5	0E01 0038h
RTI0	2080 0038h
RTI1	2081 0038h
RTI2	2082 0038h
RTI3	2083 0038h
WKUP_RTI0	2B00 0038h

Figure 14-6851. RTI_CFG1_RTI_RTICPUC1 Name Register

32	31	30	29	28	27	26	25
CPUC1							
R/W							
0h							
24	23	22	21	20	19	18	17
CPUC1							
R/W							
0h							
16	15	14	13	12	11	10	9
CPUC1							
R/W							
0h							
8	7	6	5	4	3	2	1
CPUC1							
R/W							
0h							

Table 14-13896. RTI_CFG1_RTI_RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC1	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock. If CPUC1 = 0: fFRC1 = R-----T---I---C----L----K-- 232 If CPUC1 0: fFRC1 = ----R----T----I--C-----L---K------- CPUC1 + 1 User and privilege mode (read): current compare value Privilege mode (write): the compare value is updated Reset Source: mod_g_rst_n

14.7.6.2.2.13 RTI_CFG1_RTI_RTICAFRC1 Register

14.7.6.2.2.13.1 RTI_CFG1_RTI_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

RTI Capture Free Running Counter 1 Register

Return to Summary Table

Table 14-13897. Instance Table

Instance Name	Physical Address
RTI4	0E00 0040h
RTI5	0E01 0040h
RTI0	2080 0040h
RTI1	2081 0040h
RTI2	2082 0040h
RTI3	2083 0040h
WKUP_RTI0	2B00 0040h

Figure 14-6852. RTI_CFG1_RTI_RTICAFRC1 Name Register

32	31	30	29	28	27	26	25
CAFRC1							
R							
0h							
24	23	22	21	20	19	18	17
CAFRC1							
R							
0h							
16	15	14	13	12	11	10	9
CAFRC1							
R							
0h							
8	7	6	5	4	3	2	1
CAFRC1							
R							
0h							

Table 14-13898. RTI_CFG1_RTI_RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC1	R	0h	This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block. User and privilege mode (read): value of Free Running Counter 1 on a capture event Reset Source: mod_g_rst_n

14.7.6.2.2.14 RTI_CFG1_RTI_RTICAUC1 Register

14.7.6.2.2.14.1 RTI_CFG1_RTI_RTICAUC1 Register (Offset = 44h) [reset = 0h]

RTI Capture Up Counter 1 Register

Return to Summary Table

Table 14-13899. Instance Table

Instance Name	Physical Address
RTI4	0E00 0044h
RTI5	0E01 0044h
RTI0	2080 0044h
RTI1	2081 0044h
RTI2	2082 0044h
RTI3	2083 0044h
WKUP_RTI0	2B00 0044h

Figure 14-6853. RTI_CFG1_RTI_RTICAUC1 Name Register

32	31	30	29	28	27	26	25
CAUC1							
R							
0h							
24	23	22	21	20	19	18	17
CAUC1							
R							
0h							
16	15	14	13	12	11	10	9
CAUC1							
R							
0h							
8	7	6	5	4	3	2	1
CAUC1							
R							
0h							

Table 14-13900. RTI_CFG1_RTI_RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC1	R	0h	This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode (read): value of Up Counter 1 on a capture event Reset Source: mod_g_rst_n

14.7.6.2.2.15 RTI_CFG1_RTI_RTICOMP0 Register

14.7.6.2.2.15.1 RTI_CFG1_RTI_RTICOMP0 Register (Offset = 50h) [reset = 0h]

RTI Compare 0 Register

Return to Summary Table

Table 14-13901. Instance Table

Instance Name	Physical Address
RTI4	0E00 0050h
RTI5	0E01 0050h
RTI0	2080 0050h
RTI1	2081 0050h
RTI2	2082 0050h
RTI3	2083 0050h
WKUP_RTI0	2B00 0050h

Figure 14-6854. RTI_CFG1_RTI_RTICOMP0 Name Register

32	31	30	29	28	27	26	25
COMP0							
R/W							
0h							
24	23	22	21	20	19	18	17
COMP0							
R/W							
0h							
16	15	14	13	12	11	10	9
COMP0							
R/W							
0h							
8	7	6	5	4	3	2	1
COMP0							
R/W							
0h							

Table 14-13902. RTI_CFG1_RTI_RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.7.6.2.2.16 RTI_CFG1_RTI_RTIUDCP0 Register

14.7.6.2.2.16.1 RTI_CFG1_RTI_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

RTI Update Compare 0 Register

Return to Summary Table

Table 14-13903. Instance Table

Instance Name	Physical Address
RTI4	0E00 0054h
RTI5	0E01 0054h
RTI0	2080 0054h
RTI1	2081 0054h
RTI2	2082 0054h
RTI3	2083 0054h
WKUP_RTI0	2B00 0054h

Figure 14-6855. RTI_CFG1_RTI_RTIUDCP0 Name Register

32	31	30	29	28	27	26	25
UDCP0							
R/W							
0h							
24	23	22	21	20	19	18	17
UDCP0							
R/W							
0h							
16	15	14	13	12	11	10	9
UDCP0							
R/W							
0h							
8	7	6	5	4	3	2	1
UDCP0							
R/W							
0h							

Table 14-13904. RTI_CFG1_RTI_RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP0	R/W	0h	This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 0 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.7.6.2.2.17 RTI_CFG1_RTI_RTICOMP1 Register

14.7.6.2.2.17.1 RTI_CFG1_RTI_RTICOMP1 Register (Offset = 58h) [reset = 0h]

RTI Compare 1 Register

Return to Summary Table

Table 14-13905. Instance Table

Instance Name	Physical Address
RTI4	0E00 0058h
RTI5	0E01 0058h
RTI0	2080 0058h
RTI1	2081 0058h
RTI2	2082 0058h
RTI3	2083 0058h
WKUP_RTI0	2B00 0058h

Figure 14-6856. RTI_CFG1_RTI_RTICOMP1 Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">COMP1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">COMP1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">COMP1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">COMP1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13906. RTI_CFG1_RTI_RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.7.6.2.2.18 RTI_CFG1_RTI_RTIUDCP1 Register

14.7.6.2.2.18.1 RTI_CFG1_RTI_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

RTI Update Compare 1 Register

Return to Summary Table

Table 14-13907. Instance Table

Instance Name	Physical Address
RTI4	0E00 005Ch
RTI5	0E01 005Ch
RTI0	2080 005Ch
RTI1	2081 005Ch
RTI2	2082 005Ch
RTI3	2083 005Ch
WKUP_RTI0	2B00 005Ch

Figure 14-6857. RTI_CFG1_RTI_RTIUDCP1 Name Register

32	31	30	29	28	27	26	25
UDCP1							
R/W							
0h							
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
UDCP1							
R/W							
0h							
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
UDCP1							
R/W							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
UDCP1							
R/W							
0h							

Table 14-13908. RTI_CFG1_RTI_RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP1	R/W	0h	This registers holds a value, which is added to the value in the compare 1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 1 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.7.6.2.2.19 RTI_CFG1_RTI_RTICOMP2 Register

14.7.6.2.2.19.1 RTI_CFG1_RTI_RTICOMP2 Register (Offset = 60h) [reset = 0h]

RTI Compare 2 Register

Return to Summary Table

Table 14-13909. Instance Table

Instance Name	Physical Address
RTI4	0E00 0060h
RTI5	0E01 0060h
RTI0	2080 0060h
RTI1	2081 0060h
RTI2	2082 0060h
RTI3	2083 0060h
WKUP_RTI0	2B00 0060h

Figure 14-6858. RTI_CFG1_RTI_RTICOMP2 Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">COMP2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">COMP2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">COMP2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">COMP2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13910. RTI_CFG1_RTI_RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.7.6.2.2.20 RTI_CFG1_RTI_RTIUDCP2 Register

14.7.6.2.2.20.1 RTI_CFG1_RTI_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

RTI Update Compare 2 Register

Return to Summary Table

Table 14-13911. Instance Table

Instance Name	Physical Address
RTI4	0E00 0064h
RTI5	0E01 0064h
RTI0	2080 0064h
RTI1	2081 0064h
RTI2	2082 0064h
RTI3	2083 0064h
WKUP_RTI0	2B00 0064h

Figure 14-6859. RTI_CFG1_RTI_RTIUDCP2 Name Register

32	31	30	29	28	27	26	25
UDCP2							
R/W							
0h							
24	23	22	21	20	19	18	17
UDCP2							
R/W							
0h							
16	15	14	13	12	11	10	9
UDCP2							
R/W							
0h							
8	7	6	5	4	3	2	1
UDCP2							
R/W							
0h							

Table 14-13912. RTI_CFG1_RTI_RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP2	R/W	0h	This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 2 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.7.6.2.2.21 RTI_CFG1_RTI_RTICOMP3 Register

14.7.6.2.2.21.1 RTI_CFG1_RTI_RTICOMP3 Register (Offset = 68h) [reset = 0h]

RTI Compare 3 Register

Return to Summary Table

Table 14-13913. Instance Table

Instance Name	Physical Address
RTI4	0E00 0068h
RTI5	0E01 0068h
RTI0	2080 0068h
RTI1	2081 0068h
RTI2	2082 0068h
RTI3	2083 0068h
WKUP_RTI0	2B00 0068h

Figure 14-6860. RTI_CFG1_RTI_RTICOMP3 Name Register

32	31	30	29	28	27	26	25
COMP3							
R/W							
0h							
24	23	22	21	20	19	18	17
COMP3							
R/W							
0h							
16	15	14	13	12	11	10	9
COMP3							
R/W							
0h							
8	7	6	5	4	3	2	1
COMP3							
R/W							
0h							

Table 14-13914. RTI_CFG1_RTI_RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.7.6.2.2.22 RTI_CFG1_RTI_RTIUDCP3 Register

14.7.6.2.2.22.1 RTI_CFG1_RTI_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

RTI Update Compare 3 Register

Return to Summary Table

Table 14-13915. Instance Table

Instance Name	Physical Address
RTI4	0E00 006Ch
RTI5	0E01 006Ch
RTI0	2080 006Ch
RTI1	2081 006Ch
RTI2	2082 006Ch
RTI3	2083 006Ch
WKUP_RTI0	2B00 006Ch

Figure 14-6861. RTI_CFG1_RTI_RTIUDCP3 Name Register

32	31	30	29	28	27	26	25
UDCP3							
R/W							
0h							
24	23	22	21	20	19	18	17
UDCP3							
R/W							
0h							
16	15	14	13	12	11	10	9
UDCP3							
R/W							
0h							
8	7	6	5	4	3	2	1
UDCP3							
R/W							
0h							

Table 14-13916. RTI_CFG1_RTI_RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP3	R/W	0h	This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): value to be added to the compare 3 register on the next compare match Privilege mode (write): new update value Reset Source: mod_g_rst_n

14.7.6.2.2.23 RTI_CFG1_RTI_RTITBLCOMP Register

14.7.6.2.2.23.1 RTI_CFG1_RTI_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

RTI External Clock Timebase Low Compare Register

Return to Summary Table

Table 14-13917. Instance Table

Instance Name	Physical Address
RTI4	0E00 0070h
RTI5	0E01 0070h
RTI0	2080 0070h
RTI1	2081 0070h
RTI2	2082 0070h
RTI3	2083 0070h
WKUP_RTI0	2B00 0070h

Figure 14-6862. RTI_CFG1_RTI_RTITBLCOMP Name Register

32	31	30	29	28	27	26	25
TBLCOMP							
R/W							
0h							
24	**23**	**22**	**21**	**20**	**19**	**18**	**17**
TBLCOMP							
R/W							
0h							
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**
TBLCOMP							
R/W							
0h							
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
TBLCOMP							
R/W							
0h							

Table 14-13918. RTI_CFG1_RTI_RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBLCOMP	R/W	0h	This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0. User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Note: Reset behavior A reset does not generate a compare match. Reset Source: mod_g_rst_n

14.7.6.2.2.24 RTI_CFG1_RTI_RTITBHCOMP Register

14.7.6.2.2.24.1 RTI_CFG1_RTI_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

RTI External Clock Timebase High Compare Register

Return to Summary Table

Table 14-13919. Instance Table

Instance Name	Physical Address
RTI4	0E00 0074h
RTI5	0E01 0074h
RTI0	2080 0074h
RTI1	2081 0074h
RTI2	2082 0074h
RTI3	2083 0074h
WKUP_RTI0	2B00 0074h

Figure 14-6863. RTI_CFG1_RTI_RTITBHCOMP Name Register

32	31	30	29	28	27	26	25
TBHCOMP							
R/W							
0h							
24	23	22	21	20	19	18	17
TBHCOMP							
R/W							
0h							
16	15	14	13	12	11	10	9
TBHCOMP							
R/W							
0h							
8	7	6	5	4	3	2	1
TBHCOMP							
R/W							
0h							

Table 14-13920. RTI_CFG1_RTI_RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBHCOMP	R/W	0h	This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0. RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached. Example: The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0. RTICPUC0 = 0x00000050 RTITBLCOMP = 0x000046 RTITBHCOMP = 0x00000009 User and privilege mode (read): current compare value Privilege mode (write when TBEXT = 0): the compare value is updated Privilege mode (write when TBEXT = 1): the compare value is not changed Note: Reset behavior A reset does not generate a compare match. Reset Source: mod_g_rst_n

14.7.6.2.2.25 RTI_CFG1_RTI_RTISETINT Register

14.7.6.2.2.25.1 RTI_CFG1_RTI_RTISETINT Register (Offset = 80h) [reset = 0h]

RTI Set/Status Interrupt Register

Return to Summary Table

Table 14-13921. Instance Table

Instance Name	Physical Address
RTI4	0E00 0080h
RTI5	0E01 0080h
RTI0	2080 0080h
RTI1	2081 0080h
RTI2	2082 0080h
RTI3	2083 0080h
WKUP_RTI0	2B00 0080h

Figure 14-6864. RTI_CFG1_RTI_RTISETINT Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							

24	23	22	21	20	19	18	17
RESERVED					SETOVL1INT	SETOVL0INT	SETTBINT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

16	15	14	13	12	11	10	9
RESERVED				SETDMA3	SETDMA2	SETDMA1	SETDMA0
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

8	7	6	5	4	3	2	1
RESERVED				SETINT3	SETINT2	SETINT1	SETINT0
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 14-13922. RTI_CFG1_RTI_RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	SETOVL1INT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
17	SETOVL0INT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
16	SETTBINT	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved

Table 14-13922. RTI_CFG1_RTI_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SETDMA3	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
10	SETDMA2	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
9	SETDMA1	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
8	SETDMA0	R/W1TS	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable DMA request Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3	SETINT3	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
2	SETINT2	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
1	SETINT1	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n
0	SETINT0	R/W1TS	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = enable interrupt Reset Source: mod_g_rst_n

14.7.6.2.2.26 RTI_CFG1_RTI_RTICLEARINT Register

14.7.6.2.2.26.1 RTI_CFG1_RTI_RTICLEARINT Register (Offset = 84h) [reset = 0h]

RTI Clear/Status Interrupt Register

Return to Summary Table

Table 14-13923. Instance Table

Instance Name	Physical Address
RTI4	0E00 0084h
RTI5	0E01 0084h
RTI0	2080 0084h
RTI1	2081 0084h
RTI2	2082 0084h
RTI3	2083 0084h
WKUP_RTI0	2B00 0084h

Figure 14-6865. RTI_CFG1_RTI_RTICLEARINT Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED					CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
16	15	14	13	12	11	10	9
RESERVED				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
8	7	6	5	4	3	2	1
RESERVED				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-13924. RTI_CFG1_RTI_RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	CLEAROVL1INT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
17	CLEAROVL0INT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
16	CLEARTBINT	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	0h	Reserved

Table 14-13924. RTI_CFG1_RTI_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CLEARDMA3	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
10	CLEARDMA2	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
9	CLEARDMA1	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
8	CLEARDMA0	R/W1TC	0h	User and privilege mode (read): 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable DMA request Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	0h	Reserved
3	CLEARINT3	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
2	CLEARINT2	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
1	CLEARINT1	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n
0	CLEARINT0	R/W1TC	0h	User and privilege mode (read): 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode (write): 0 = leaves the corresponding bit unchanged 1 = disable interrupt Reset Source: mod_g_rst_n

14.7.6.2.2.27 RTI_CFG1_RTI_RTIINTFLAG Register

14.7.6.2.2.27.1 RTI_CFG1_RTI_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

RTI Interrupt Flag Register

Return to Summary Table

Table 14-13925. Instance Table

Instance Name	Physical Address
RTI4	0E00 0088h
RTI5	0E01 0088h
RTI0	2080 0088h
RTI1	2081 0088h
RTI2	2082 0088h
RTI3	2083 0088h
WKUP_RTI0	2B00 0088h

Figure 14-6866. RTI_CFG1_RTI_RTIINTFLAG Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED					OVL1INT	OVL0INT	TBINT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED				INT3	INT2	INT1	INT0
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 14-13926. RTI_CFG1_RTI_RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	OVL1INT	R/W1TC	0h	User and privilege mode (read): determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
17	OVL0INT	R/W1TC	0h	User and privilege mode (read): determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
16	TBINT	R/W1TC	0h	User and privilege mode (read): this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software. determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
15:4	RESERVED	NONE	0h	Reserved

Table 14-13926. RTI_CFG1_RTI_RTIINTFLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT3	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
2	INT2	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
1	INT1	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n
0	INT0	R/W1TC	0h	User and privilege mode (read): determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode (write): 0 = leaves the bit unchanged 1 = set the bit to 0 Reset Source: mod_g_rst_n

14.7.6.2.2.28 RTI_CFG1_RTI_RTIDWDCTRL Register

14.7.6.2.2.28.1 RTI_CFG1_RTI_RTIDWDCTRL Register (Offset = 90h) [reset = 5312ACEDh]

Digital Watchdog Control Register

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Table 14-13927. Instance Table

Instance Name	Physical Address
RTI4	0E00 0090h
RTI5	0E01 0090h
RTI0	2080 0090h
RTI1	2081 0090h
RTI2	2082 0090h
RTI3	2083 0090h
WKUP_RTI0	2B00 0090h

Figure 14-6867. RTI_CFG1_RTI_RTIDWDCTRL Name Register

32	31	30	29	28	27	26	25
DWDCTRL							
R/W							
5312acedh							
24	23	22	21	20	19	18	17
DWDCTRL							
R/W							
5312acedh							
16	15	14	13	12	11	10	9
DWDCTRL							
R/W							
5312acedh							
8	7	6	5	4	3	2	1
DWDCTRL							
R/W							
5312acedh							

Table 14-13928. RTI_CFG1_RTI_RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DWDCTRL	R/W	5312acedh	User and priviledge mode (read): 0x5312ACED = DWD counter is disabled. This is the default value. 0xA98559DA = DWD counter is enabled Any other value = DWD counter state is unchanged (enabled or disabled) Priviledge mode (write): 0xA98559DA = DWD counter is enabled Any other value = State of DWD counter is unchanged (stays enabled or disabled) Note: One-Write Functionality of DWDCTRL Register The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again. Reset Source: mod_g_rst_n

14.7.6.2.2.29 RTI_CFG1_RTI_RTIDWDPRLD Register

14.7.6.2.2.29.1 RTI_CFG1_RTI_RTIDWDPRLD Register (Offset = 94h) [reset = FFFh]

Digital Watchdog Preload Register

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Table 14-13929. Instance Table

Instance Name	Physical Address
RTI4	0E00 0094h
RTI5	0E01 0094h
RTI0	2080 0094h
RTI1	2081 0094h
RTI2	2082 0094h
RTI3	2083 0094h
WKUP_RTI0	2B00 0094h

Figure 14-6868. RTI_CFG1_RTI_RTIDWDPRLD Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">2964619C7h</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">2964619C7h</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">DWDPRLD</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">2964619C7h</td><td colspan="4">fffh</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="8">DWDPRLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">fffh</td></tr>
</table>

Table 14-13930. RTI_CFG1_RTI_RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	2964619C7h	Reserved

Table 14-13930. RTI_CFG1_RTI_RTIDWDPRLD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	DWDPRLD	R/W	fffh	User and priviledge mode (read): A read from this register in any CPU mode returns the current preload value. Priviledge mode (write): If the DWD is always enabled after reset is released: The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF. The application can configure the DWD preload register any time before this down counter expires. When the application services the DWD, the preload register contents are copied left- justified into the DWD down counter and it starts counting down from that value. If the DWD is implemented such that the down counter is enabled by software: The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter. The expiration time of the DWD Down Counter can be determined with following equation: texp = (RTIDWDPRLD+1) x 2^{13} / RTICLK1 where: RTIDWDPRLD = 0...4095 Reset Source: mod_g_rst_n

14.7.6.2.2.30 RTI_CFG1_RTI_RTIWDSTATUS Register

14.7.6.2.2.30.1 RTI_CFG1_RTI_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Watchdog Status Register

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Table 14-13931. Instance Table

Instance Name	Physical Address
RTI4	0E00 0098h
RTI5	0E01 0098h
RTI0	2080 0098h
RTI1	2081 0098h
RTI2	2082 0098h
RTI3	2083 0098h
WKUP_RTI0	2B00 0098h

Figure 14-6869. RTI_CFG1_RTI_RTIWDSTATUS Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
0h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
0h							
16	15	14	13	12	11	10	9
RESERVED							
NONE							
0h							
8	7	6	5	4	3	2	1
RESERVED		DWWD	END	START	KEYST	DWDST	AWDST
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h		0h	0h	0h	0h	0h	0h

Table 14-13932. RTI_CFG1_RTI_RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	DWWD	R/W1TC	0h	This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog. User and priviledge mode (read): 0 = no time-window violation has occurred. 1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS reg- ister except for the AWD ST flag. Clearing of the status flags will deassert the non- maskable interrupt generated due to violation of the DWWD. Reset Source: mod_g_rst_n

Table 14-13932. RTI_CFG1_RTI_RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	END	R/W1TC	0h	This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag. User and priviledge mode (read): 0 = no end-time window violation has occurred. 1 = the end-time defined by the windowed watchdog configuration has been violated. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. Reset Source: mod_g_rst_n
3	START	R/W1TC	0h	This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened. User and priviledge mode (read): 0 = no start-time window violation has occurred. 1 = the start-time defined by the windowed watchdog configuration has been violated. Priviledge mode (write): 0 = leaves the current value unchanged. 1 = clears the bit to 0. Reset Source: mod_g_rst_n
2	KEYST	R/W1TC	0h	This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register. User and priviledge mode (read): 0 = no wrong key or key-sequence written 1 = wrong key or key-sequence written to RTIWDKEY register Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n
1	DWDST	R/W1TC	0h	status flag and is maintained for compatibility reasons. User and priviledge mode (read): 0 = DWD timeout period not expired 1 = DWD timeout period has expired Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n
0	AWDST	R/W1TC	0h	User and priviledge mode (read): 0 = AWD pin 0 > 1 threshold not exceeded 1 = AWD pin 0 > 1 threshold exceeded Priviledge mode (write): 0 = leaves the current value unchanged 1 = clears the bit to 0 Reset Source: mod_g_rst_n

14.7.6.2.2.31 RTI_CFG1_RTI_RTIWDKEY Register

14.7.6.2.2.31.1 RTI_CFG1_RTI_RTIWDKEY Register (Offset = 9Ch) [reset = A35Ch]

Watchdog Key Register

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Table 14-13933. Instance Table

Instance Name	Physical Address
RTI4	0E00 009Ch
RTI5	0E01 009Ch
RTI0	2080 009Ch
RTI1	2081 009Ch
RTI2	2082 009Ch
RTI3	2083 009Ch
WKUP_RTI0	2B00 009Ch

Figure 14-6870. RTI_CFG1_RTI_RTIWDKEY Name Register

32	31	30	29	28	27	26	25
RESERVED							
NONE							
5BDBEBAF5276h							
24	23	22	21	20	19	18	17
RESERVED							
NONE							
5BDBEBAF5276h							
16	15	14	13	12	11	10	9
WDKEY							
R/W							
a35ch							
8	7	6	5	4	3	2	1
WDKEY							
R/W							
a35ch							

Table 14-13934. RTI_CFG1_RTI_RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	5BDBEBAF 5276h	Reserved

Table 14-13934. RTI_CFG1_RTI_RTIWDKEY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	WDKEY	R/W	a35ch	User and privilege mode reads are indeterminate. Privilege mode (write): A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1's. Writing any other value causes a digital watchdog reset, as shown in Table 1-3. Note: Register write access time precaution The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation. Table 2. Example of a WDKEY sequence Value written to Step WDKEY Result 1 0x0A35C No Action 2 0x0A35C No Action 3 0x0E51A WDKEY is enabled for reset by next 0x0A35C 4 0x0E51A WDKEY is enabled for reset by next 0x0A35C 5 0x0E51A WDKEY is enabled for reset by next 0x0A35C 6 0x0A35C Watchdog is reset 7 0x0A35C No Action 8 0x0E51A WDKEY is enabled for reset by next 0x0A35C 9 0x0A35C Watchdog is reset 10 0x0E51A WDKEY is enabled for reset by next 0x0A35C 11 0x02345 System reset; incorrect value written to WDKEY Reset Source: mod_g_rst_n

14.7.6.2.2.32 RTI_CFG1_RTI_RTIDWDCNTR Register

14.7.6.2.2.32.1 RTI_CFG1_RTI_RTIDWDCNTR Register (Offset = A0h) [reset = 1FFFFFFh]

Digital Watchdog Down Counter

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Table 14-13935. Instance Table

Instance Name	Physical Address
RTI4	0E00 00A0h
RTI5	0E01 00A0h
RTI0	2080 00A0h
RTI1	2081 00A0h
RTI2	2082 00A0h
RTI3	2083 00A0h
WKUP_RTI0	2B00 00A0h

Figure 14-6871. RTI_CFG1_RTI_RTIDWDCNTR Name Register

32	31	30	29	28	27	26	25
RESERVED							DWDCNTR
NONE							R
1B207h							1fffffh
24	23	22	21	20	19	18	17
DWDCNTR							
R							
1fffffh							
16	15	14	13	12	11	10	9
DWDCNTR							
R							
1fffffh							
8	7	6	5	4	3	2	1
DWDCNTR							
R							
1fffffh							

Table 14-13936. RTI_CFG1_RTI_RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	1B207h	Reserved
24:0	DWDCNTR	R	1fffffh	The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second. User and privilege mode (read): Reads return the current counter value. Privilege mode (write): Writes don't have an effect. Reset Source: mod_g_rst_n

14.7.6.2.2.33 RTI_CFG1_RTI_RTIDWWDRXNCTRL Register

14.7.6.2.2.33.1 RTI_CFG1_RTI_RTIDWWDRXNCTRL Register (Offset = A4h) [reset = 5h]

Digital Windowed Watchdog Reaction Control

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Table 14-13937. Instance Table

Instance Name	Physical Address
RTI4	0E00 00A4h
RTI5	0E01 00A4h
RTI0	2080 00A4h
RTI1	2081 00A4h
RTI2	2082 00A4h
RTI3	2083 00A4h
WKUP_RTI0	2B00 00A4h

Figure 14-6872. RTI_CFG1_RTI_RTIDWWDRXNCTRL Name Register

<table>
<tr><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">Ah</td></tr>
<tr><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">Ah</td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">Ah</td></tr>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">WWDRXN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">Ah</td><td colspan="4">5h</td></tr>
</table>

Table 14-13938. RTI_CFG1_RTI_RTIDWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	Ah	Reserved

Table 14-13938. RTI_CFG1_RTI_RTIDWWDRXNCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	WWDRXN	R/W	5h	User and privilege mode (read), privileged mode (write): 0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. 0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Note: Configuration of DWWD Reaction The DWWD reaction can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced. Reset Source: mod_g_rst_n

14.7.6.2.2.34 RTI_CFG1_RTI_RTIDWWDSIZECTRL Register

14.7.6.2.2.34.1 RTI_CFG1_RTI_RTIDWWDSIZECTRL Register (Offset = A8h) [reset = 5h]

Digital Windowed Watchdog Window Size Control

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Table 14-13939. Instance Table

Instance Name	Physical Address
RTI4	0E00 00A8h
RTI5	0E01 00A8h
RTI0	2080 00A8h
RTI1	2081 00A8h
RTI2	2082 00A8h
RTI3	2083 00A8h
WKUP_RTI0	2B00 00A8h

Figure 14-6873. RTI_CFG1_RTI_RTIDWWDSIZECTRL Name Register

32	31	30	29	28	27	26	25
WWDSIZE							
R/W							
5h							
24	23	22	21	20	19	18	17
WWDSIZE							
R/W							
5h							
16	15	14	13	12	11	10	9
WWDSIZE							
R/W							
5h							
8	7	6	5	4	3	2	1
WWDSIZE							
R/W							
5h							

Table 14-13940. RTI_CFG1_RTI_RTIDWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WWDSIZE	R/W	5h	User and privilege mode (read), privileged mode (write): Table 3. Windowed Watchdog Window Size Configuration Value written to WWDSIZE Window Size 0x00000005 100% (The functionality is the same as the standard time-out digital watchdog.) 0x00000050 50% 0x00000500 25% 0x00005000 12.5% 0x00050000 6.25% 0x00500000 3.125% Any other 3.125% value Note: Incorrect value being written to watchdog window size control register If an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration. Note: Configuration of DWWD Window Size The DWWD window size can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDSIZE is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced. Reset Source: mod_g_rst_n

14.7.6.2.2.35 RTI_CFG1_RTI_RTIINTCLRENABLE Register

14.7.6.2.2.35.1 RTI_CFG1_RTI_RTIINTCLRENABLE Register (Offset = ACh) [reset = 5050505h]

RTI Compare Interrupt Clear Enable Register

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Table 14-13941. Instance Table

Instance Name	Physical Address
RTI4	0E00 00ACh
RTI5	0E01 00ACh
RTI0	2080 00ACh
RTI1	2081 00ACh
RTI2	2082 00ACh
RTI3	2083 00ACh
WKUP_RTI0	2B00 00ACh

Figure 14-6874. RTI_CFG1_RTI_RTIINTCLRENABLE Name Register

32	31	30	29	28	27	26	25
RESERVED				INTCLRENABLE3			
NONE				R/W			
Ah				5h			
24	23	22	21	20	19	18	17
RESERVED				INTCLRENABLE2			
NONE				R/W			
Ah				5h			
16	15	14	13	12	11	10	9
RESERVED				INTCLRENABLE1			
NONE				R/W			
Ah				5h			
8	7	6	5	4	3	2	1
RESERVED				INTCLRENABLE0			
NONE				R/W			
Ah				5h			

Table 14-13942. RTI_CFG1_RTI_RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	Ah	Reserved
27:24	INTCLRENABLE3	R/W	5h	Enables the auto-clear functionality on the compare 3 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 3 interrupt is disabled. Any other value = Auto-clear for compare 3 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 3 interrupt. Any other value = Enables the auto-clear functionality on the compare 3 interrupt. Reset Source: mod_g_rst_n
23:20	RESERVED	NONE	Ah	Reserved
19:16	INTCLRENABLE2	R/W	5h	Enables the auto-clear functionality on the compare 2 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 2 interrupt is disabled. Any other value = Auto-clear for compare 2 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 2 interrupt. Any other value = Enables the auto-clear functionality on the compare 2 interrupt. Reset Source: mod_g_rst_n
15:12	RESERVED	NONE	Ah	Reserved

Table 14-13942. RTI_CFG1_RTI_RTIINTCLRENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	INTCLRENABLE1	R/W	5h	Enables the auto-clear functionality on the compare 1 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 1 interrupt is disabled. Any other value = Auto-clear for compare 1 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 1 interrupt. Any other value = Enables the auto-clear functionality on the compare 1 interrupt. Reset Source: mod_g_rst_n
7:4	RESERVED	NONE	Ah	Reserved
3:0	INTCLRENABLE0	R/W	5h	Enables the auto-clear functionality on the compare 0 interrupt. User and Privileged mode (read): 0x5 = Auto-clear for compare 0 interrupt is disabled. Any other value = Auto-clear for compare 0 interrupt is enabled. Privileged mode (write): 0x5 = Disables the auto-clear functionality on the compare 0 interrupt. Any other value = Enables the auto-clear functionality on the compare 0 interrupt. Note: Hook-up of Compare Interrupt to a device pin The RTI module generates up to 4 compare interrupts. The connection between one or more of these compare interrupt(s) to a device pin is completely device-dependent. Refer to the device datasheet to identify the actual pin(s) that connects to the compare interrupt(s). Reset Source: mod_g_rst_n

14.7.6.2.2.36 RTI_CFG1_RTI_RTICOMP0CLR Register

14.7.6.2.2.36.1 RTI_CFG1_RTI_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

RTI Compare 0 Clear Register

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Table 14-13943. Instance Table

Instance Name	Physical Address
RTI4	0E00 00B0h
RTI5	0E01 00B0h
RTI0	2080 00B0h
RTI1	2081 00B0h
RTI2	2082 00B0h
RTI3	2083 00B0h
WKUP_RTI0	2B00 00B0h

Figure 14-6875. RTI_CFG1_RTI_RTICOMP0CLR Name Register

32	31	30	29	28	27	26	25
COMP0CLR							
R/W							
0h							
24	23	22	21	20	19	18	17
COMP0CLR							
R/W							
0h							
16	15	14	13	12	11	10	9
COMP0CLR							
R/W							
0h							
8	7	6	5	4	3	2	1
COMP0CLR							
R/W							
0h							

Table 14-13944. RTI_CFG1_RTI_RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.7.6.2.2.37 RTI_CFG1_RTI_RTICOMP1CLR Register

14.7.6.2.2.37.1 RTI_CFG1_RTI_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

RTI Compare 1 Clear Register

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Table 14-13945. Instance Table

Instance Name	Physical Address
RTI4	0E00 00B4h
RTI5	0E01 00B4h
RTI0	2080 00B4h
RTI1	2081 00B4h
RTI2	2082 00B4h
RTI3	2083 00B4h
WKUP_RTI0	2B00 00B4h

Figure 14-6876. RTI_CFG1_RTI_RTICOMP1CLR Name Register

32	31	30	29	28	27	26	25
COMP1CLR							
R/W							
0h							
24	23	22	21	20	19	18	17
COMP1CLR							
R/W							
0h							
16	15	14	13	12	11	10	9
COMP1CLR							
R/W							
0h							
8	7	6	5	4	3	2	1
COMP1CLR							
R/W							
0h							

Table 14-13946. RTI_CFG1_RTI_RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 1 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.7.6.2.2.38 RTI_CFG1_RTI_RTICOMP2CLR Register

14.7.6.2.2.38.1 RTI_CFG1_RTI_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

RTI Compare 2 Clear Register

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Table 14-13947. Instance Table

Instance Name	Physical Address
RTI4	0E00 00B8h
RTI5	0E01 00B8h
RTI0	2080 00B8h
RTI1	2081 00B8h
RTI2	2082 00B8h
RTI3	2083 00B8h
WKUP_RTI0	2B00 00B8h

Figure 14-6877. RTI_CFG1_RTI_RTICOMP2CLR Name Register

32	31	30	29	28	27	26	25
COMP2CLR							
R/W							
0h							
24	23	22	21	20	19	18	17
COMP2CLR							
R/W							
0h							
16	15	14	13	12	11	10	9
COMP2CLR							
R/W							
0h							
8	7	6	5	4	3	2	1
COMP2CLR							
R/W							
0h							

Table 14-13948. RTI_CFG1_RTI_RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 2 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.7.6.2.2.39 RTI_CFG1_RTI_RTICOMP3CLR Register

14.7.6.2.2.39.1 RTI_CFG1_RTI_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

RTI Compare 3 Clear Register

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Table 14-13949. Instance Table

Instance Name	Physical Address
RTI4	0E00 00BCh
RTI5	0E01 00BCh
RTI0	2080 00BCh
RTI1	2081 00BCh
RTI2	2082 00BCh
RTI3	2083 00BCh
WKUP_RTI0	2B00 00BCh

Figure 14-6878. RTI_CFG1_RTI_RTICOMP3CLR Name Register

32	31	30	29	28	27	26	25
COMP3CLR							
R/W							
0h							
24	23	22	21	20	19	18	17
COMP3CLR							
R/W							
0h							
16	15	14	13	12	11	10	9
COMP3CLR							
R/W							
0h							
8	7	6	5	4	3	2	1
COMP3CLR							
R/W							
0h							

Table 14-13950. RTI_CFG1_RTI_RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3CLR	R/W	0h	This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 3 interrupt or DMA request line is cleared. User and privilege mode (read): current compare value Privilege mode (write): update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled. Reset Source: mod_g_rst_n

14.7.6.3 rtcss

rtcss

14.7.6.3.1 rtcss Summaries

rtcss Summaries

Table 14-13951. RTC Registers, Base Address=2B1F 0000h, Length=128

Offset	Length	Register Name	WKUP_rtcss0 Physical Address
0h	32	RTC_MOD_VER	2B1F 0000h + formula
4h	32	RTC_SUB_S_CNT	2B1F 0004h + formula
8h	32	RTC_S_CNT_LSW	2B1F 0008h + formula
Ch	32	RTC_S_CNT_MSW	2B1F 000Ch + formula
10h	32	RTC_COMP	2B1F 0010h + formula
18h	32	RTC_OFF_ON_S_CNT_LSW	2B1F 0018h + formula
1Ch	32	RTC_OFF_ON_S_CNT_MSW	2B1F 001Ch + formula
20h	32	RTC_ON_OFF_S_CNT_LSW	2B1F 0020h + formula
24h	32	RTC_ON_OFF_S_CNT_MSW	2B1F 0024h + formula
28h	32	RTC_DEBOUNCE	2B1F 0028h + formula
2Ch	32	RTC_ANALOG	2B1F 002Ch + formula
30h	32	RTC_SCRATCH0_J	2B1F 0030h + formula
50h	32	RTC_GENRAL_CTL	2B1F 0050h + formula
54h	32	RTC_IRQSTATUS_RAW_SYS	2B1F 0054h + formula
58h	32	RTC_IRQSTATUS_SYS	2B1F 0058h + formula
5Ch	32	RTC_IRQENABLE_SET_SYS	2B1F 005Ch + formula
60h	32	RTC_IRQENABLE_CLR_SYS	2B1F 0060h + formula
68h	32	RTC_SYNCPEND	2B1F 0068h + formula
70h	32	RTC_KICK0	2B1F 0070h + formula
74h	32	RTC_KICK1	2B1F 0074h + formula

14.7.6.3.2 rtcss Registers

rtcss Registers

14.7.6.3.2.1 RTC_MOD_VER Register

14.7.6.3.2.1.1 RTC_MOD_VER Register (Offset = 0h) [reset = 68C00101h]

The Module and Version Register identifies the module identifier and revision of the RTC module.

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Table 14-13952. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0000h + formula

Figure 14-6879. RTC_MOD_VER Name Register

31	30	29	28	27	26	25	24
MODULE_ID							
R							
68C0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
68C0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VERSION					MAJOR_REVISION		
R					R		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM_REVISION		MINOR_REVISION					
R		R					
0h		1h					

Table 14-13953. RTC_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODULE_ID	R	68C0h	RTC module ID.
15:11	RTL_VERSION	R	0h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	1h	Minor Revision.

14.7.6.3.2.2 RTC_SUB_S_CNT Register

14.7.6.3.2.2.1 RTC_SUB_S_CNT Register (Offset = 4h) [reset = 0h]

This register counts the 32768 Hz clock events

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Table 14-13954. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0004h + formula

Figure 14-6880. RTC_SUB_S_CNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="7">SUB_S_CNT</td></tr>
<tr><td>NONE</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUB_S_CNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13955. RTC_SUB_S_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:0	SUB_S_CNT	R/W	0h	This counts the 32768 Hz clock events to achive 1 sec event for the sec counter, rollvers after 0x7fff or 1 Sec running on 32768Hz

14.7.6.3.2.3 RTC_S_CNT_LSW Register

14.7.6.3.2.3.1 RTC_S_CNT_LSW Register (Offset = 8h) [reset = 0h]

The lower word of the seconds counter

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Table 14-13956. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0008h + formula

Figure 14-6881. RTC_S_CNT_LSW Name Register

31	30	29	28	27	26	25	24
S_CNT_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
S_CNT_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
S_CNT_LSW							
R/W							
0h							
7	6	5	4	3	2	1	0
S_CNT_LSW							
R/W							
0h							

Table 14-13957. RTC_S_CNT_LSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	S_CNT_LSW	R/W	0h	This counts the 1 sec events, it is the lower 32 bits of the 48 bit counter, 1 = 1 Seconds, 2 = 2 Seconds, N = N Seconds

14.7.6.3.2.4 RTC_S_CNT_MSW Register

14.7.6.3.2.4.1 RTC_S_CNT_MSW Register (Offset = Ch) [reset = 0h]

The upper word of the seconds counter

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Table 14-13958. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 000Ch + formula

Figure 14-6882. RTC_S_CNT_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
S_CNT_MSW							
R/W							
0h							
7	6	5	4	3	2	1	0
S_CNT_MSW							
R/W							
0h							

Table 14-13959. RTC_S_CNT_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	S_CNT_MSW	R/W	0h	This counts the 1 sec events, it is the upper 16 bits of the 48 bit counter

14.7.6.3.2.5 RTC_COMP Register

14.7.6.3.2.5.1 RTC_COMP Register (Offset = 10h) [reset = 0h]

This register used to program the value of the 32768 periods to be added to the 32768 counter every 4096 Secs. This is used to compensate the oscillator drift.

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Table 14-13960. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0010h + formula

Figure 14-6883. RTC_COMP Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MSB_COMP							
R/W							
0h							
7	6	5	4	3	2	1	0
LSB_COMP							
R/W							
0h							

Table 14-13961. RTC_COMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MSB_COMP	R/W	0h	Indicates number of 32-kHz periods to be added into the 32-kHz counter every 4096 Secs, twos complement That means that to add one 32-kHz oscillator period every hour, the SW must write FFFF into COMP_MSB and COMP_LSB. To remove one 32-kHz oscillator period every hour, the SW must write 0001 into RTC_COMP_MSB and RTC_COMP_LSB. The 7FFF value is forbidden.
7:0	LSB_COMP	R/W	0h	Indicates number of 32-kHz periods to be added into the 32-kHz counter every 4096 Secs, twos complement That means that to add one 32-kHz oscillator period every hour, the SW must write FFFF into COMP_MSB and COMP_LSB. To remove one 32-kHz oscillator period every hour, the SW must write 0001 into RTC_COMP_MSB and RTC_COMP_LSB. The 7FFF value is forbidden.

14.7.6.3.2.6 RTC_OFF_ON_S_CNT_LSW Register

14.7.6.3.2.6.1 RTC_OFF_ON_S_CNT_LSW Register (Offset = 18h) [reset = 1h]

This register defines the OFF to ON time event

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Table 14-13962. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0018h + formula

Figure 14-6884. RTC_OFF_ON_S_CNT_LSW Name Register

31	30	29	28	27	26	25	24
OFF_ON_S_CNT_LSW							
R/W							
1h							
23	22	21	20	19	18	17	16
OFF_ON_S_CNT_LSW							
R/W							
1h							
15	14	13	12	11	10	9	8
OFF_ON_S_CNT_LSW							
R/W							
1h							
7	6	5	4	3	2	1	0
OFF_ON_S_CNT_LSW							
R/W							
1h							

Table 14-13963. RTC_OFF_ON_S_CNT_LSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OFF_ON_S_CNT_LSW	R/W	1h	The lower word of the OFF to ON time

14.7.6.3.2.7 RTC_OFF_ON_S_CNT_MSW Register

14.7.6.3.2.7.1 RTC_OFF_ON_S_CNT_MSW Register (Offset = 1Ch) [reset = 8000h]

This register defines the OFF to ON time event

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Table 14-13964. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 001Ch + formula

Figure 14-6885. RTC_OFF_ON_S_CNT_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OFF_ON_S_CNT_MSW							
R/W							
8000h							
7	6	5	4	3	2	1	0
OFF_ON_S_CNT_MSW							
R/W							
8000h							

Table 14-13965. RTC_OFF_ON_S_CNT_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OFF_ON_S_CNT_MSW	R/W	8000h	The

14.7.6.3.2.8 RTC_ON_OFF_S_CNT_LSW Register

14.7.6.3.2.8.1 RTC_ON_OFF_S_CNT_LSW Register (Offset = 20h) [reset = 1h]

This register defines the ON to OFF time event

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Table 14-13966. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0020h + formula

Figure 14-6886. RTC_ON_OFF_S_CNT_LSW Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ON_OFF_S_CNT_LSW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ON_OFF_S_CNT_LSW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ON_OFF_S_CNT_LSW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ON_OFF_S_CNT_LSW</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-13967. RTC_ON_OFF_S_CNT_LSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ON_OFF_S_CNT_LSW	R/W	1h	The

14.7.6.3.2.9 RTC_ON_OFF_S_CNT_MSW Register

14.7.6.3.2.9.1 RTC_ON_OFF_S_CNT_MSW Register (Offset = 24h) [reset = 8000h]

This register defines the ON to OFF time event

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Table 14-13968. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0024h + formula

Figure 14-6887. RTC_ON_OFF_S_CNT_MSW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ON_OFF_S_CNT_MSW							
R/W							
8000h							
7	6	5	4	3	2	1	0
ON_OFF_S_CNT_MSW							
R/W							
8000h							

Table 14-13969. RTC_ON_OFF_S_CNT_MSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ON_OFF_S_CNT_MSW	R/W	8000h	The

14.7.6.3.2.10 RTC_DEBOUNCE Register

14.7.6.3.2.10.1 RTC_DEBOUNCE Register (Offset = 28h) [reset = 0h]

The Debounce register defines the debounce timer useing the 32768 Hz clock. It allows choosing the timing or the accuracy of

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Table 14-13970. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0028h + formula

Figure 14-6888. RTC_DEBOUNCE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEBOUNCE							
R/W							
0h							

Table 14-13971. RTC_DEBOUNCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEBOUNCE	R/W	0h	Debounce time 0 debounce time is 30.52 uS N debounce time is 30.52us*(N+1)

14.7.6.3.2.11 RTC_ANALOG Register

14.7.6.3.2.11.1 RTC_ANALOG Register (Offset = 2Ch) [reset = 0h]

This register goes to the Analog Block

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Table 14-13972. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 002Ch + formula

Figure 14-6889. RTC_ANALOG Name Register

31	30	29	28	27	26	25	24
ANALOG							
R/W							
0h							
23	22	21	20	19	18	17	16
ANALOG							
R/W							
0h							
15	14	13	12	11	10	9	8
ANALOG							
R/W							
0h							
7	6	5	4	3	2	1	0
ANALOG							
R/W							
0h							

Table 14-13973. RTC_ANALOG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ANALOG	R/W	0h	Analog Configuration MMR

14.7.6.3.2.12 RTC_SCRATCH0_J Register

14.7.6.3.2.12.1 RTC_SCRATCH0_J Register (Offset = 30h) [reset = 0h]

The Scratch Storage Registers can be used to hold information in the battery backuped domain while the device is powered down.

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Table 14-13974. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0030h + formula

Figure 14-6890. RTC_SCRATCH0_j Name Register

31	30	29	28	27	26	25	24
SCRATCH0							
R/W							
0h							
23	22	21	20	19	18	17	16
SCRATCH0							
R/W							
0h							
15	14	13	12	11	10	9	8
SCRATCH0							
R/W							
0h							
7	6	5	4	3	2	1	0
SCRATCH0							
R/W							
0h							

Table 14-13975. RTC_SCRATCH0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SCRATCH0	R/W	0h	The scratch0 holds data in the battery backed domain for use by the device when powered on. This would typically be used to store signatures other information of similar ilk.

14.7.6.3.2.13 RTC_GENRAL_CTL Register

14.7.6.3.2.13.1 RTC_GENRAL_CTL Register (Offset = 50h) [reset = 0h]

This is the main RTC control register

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Table 14-13976. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0050h + formula

Figure 14-6891. RTC_GENRAL_CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CNT_FMODE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>UNLOCK</td><td>RESERVED</td><td>O32K_OSC_DEP_EN</td><td colspan="3">RESERVED</td><td>SW_OFF</td><td>PWR_OFF_EN</td></tr>
<tr><td>R</td><td>NONE</td><td>R/W</td><td colspan="3">NONE</td><td>W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">WKUP_DB_EN</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">WKUP_POL</td><td colspan="4">WKUP_EN</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-13977. RTC_GENRAL_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CNT_FMODE	R/W	0h	This defines which read freeze mode is enabled, 10 = S_CNT_LSW When SW reads S_CNT_LSW it will snap S_CNT_MSW 01 = SUB_S_CNT When SW reads SUB_S_CNT it will snap S_CNT_MSW and S_CNT_LSW 00 = Disable
23	UNLOCK	R	0h	The status of the UNLOCKED state, 1 = UnLocked 0 = Locked
22	RESERVED	NONE	0h	Reserved
21	O32K_OSC_DEP_EN	R/W	0h	This controls if a high to low transition dependence is required before the CORE domain can read or write the ON domain, 1 = Enable 0 = Disable
20:18	RESERVED	NONE	0h	Reserved
17	SW_OFF	W	0h	The SW can issue a ON_OFF event, Wrt 1 for OFF event Wrt 0 has no effect, The OFF event will occur within 31uS and relock the core
16	PWR_OFF_EN	R/W	0h	This allows the PMIC_ENABLE to go from a ON to OFF state by SW or ON_OFF event
15:12	RESERVED	NONE	0h	Reserved
11:8	WKUP_DB_EN	R/W	0h	External Wakeup Debounce Enable 1 = Enable 0 = Disable
7:4	WKUP_POL	R/W	0h	External Wakeup Polarity 1 = Active High = Active Low

Table 14-13977. RTC_GENRAL_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	WKUP_EN	R/W	0h	External Wakeup Enable 1 = Enable 0 = Disable

14.7.6.3.2.14 RTC_IRQSTATUS_RAW_SYS Register

14.7.6.3.2.14.1 RTC_IRQSTATUS_RAW_SYS Register (Offset = 54h) [reset = 0h]

Interrupt Raw Status Register

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Table 14-13978. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0054h + formula

Figure 14-6892. RTC_IRQSTATUS_RAW_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EVENT_OFF_ON	EVENT_ON_OFF
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13979. RTC_IRQSTATUS_RAW_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EVENT_OFF_ON	R/W1TS	0h	Raw status of OFF_ON interrupt for event_off_on. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
0	EVENT_ON_OFF	R/W1TS	0h	Raw status of ON_OFF interrupt for event_on_off. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.

14.7.6.3.2.15 RTC_IRQSTATUS_SYS Register

14.7.6.3.2.15.1 RTC_IRQSTATUS_SYS Register (Offset = 58h) [reset = 0h]

The EXT_WAKEUP events are level-sensitive and not edge-sensitive. When debounce is enabled, clearing an EXT_WAKEUP event may have no effect because the interrupt triggers again immediately. See the Interrupt Service Routine section of the Programming Usage Guide.

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Table 14-13980. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0058h + formula

Figure 14-6893. RTC_IRQSTATUS_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EVENT_OFF_ON	EVENT_ON_OFF
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-13981. RTC_IRQSTATUS_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EVENT_OFF_ON	R/W1TC	0h	Enabled status of OFF_ON interrupt for event_off_on. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
0	EVENT_ON_OFF	R/W1TC	0h	Enabled status of ON_OFF interrupt for event_on_off. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

14.7.6.3.2.16 RTC_IRQENABLE_SET_SYS Register

14.7.6.3.2.16.1 RTC_IRQENABLE_SET_SYS Register (Offset = 5Ch) [reset = 0h]

Interrupt Enable Set Register

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Table 14-13982. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 005Ch + formula

Figure 14-6894. RTC_IRQENABLE_SET_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						EN_EVENT_OFF_ON	EN_EVENT_ON_OFF
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-13983. RTC_IRQENABLE_SET_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EN_EVENT_OFF_ON	R/W1TS	0h	Enable set for OFF_ON interrupt for event_off_on. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
0	EN_EVENT_ON_OFF	R/W1TS	0h	Enable set for ON_OFF interrupt for event_on_off. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

14.7.6.3.2.17 RTC_IRQENABLE_CLR_SYS Register

14.7.6.3.2.17.1 RTC_IRQENABLE_CLR_SYS Register (Offset = 60h) [reset = 0h]

Interrupt Enable Clear Register

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Table 14-13984. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0060h + formula

Figure 14-6895. RTC_IRQENABLE_CLR_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						EN_EVENT_OFF_ON	EN_EVENT_ON_OFF
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-13985. RTC_IRQENABLE_CLR_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EN_EVENT_OFF_ON	R/W1TC	0h	Enable clear for OFF_ON interrupt for event_off_on. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
0	EN_EVENT_ON_OFF	R/W1TC	0h	Enable clear for ON_OFF interrupt for event_on_off. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

14.7.6.3.2.18 RTC_SYNCPEND Register

14.7.6.3.2.18.1 RTC_SYNCPEND Register (Offset = 68h) [reset = 0h]

The SW can determine status of wrt and rd access along with other status from the ON domain
This register is located in the CORE domain and provides the control and status of the MMR Sync state machine. The RELOAD_FROM_BBD bit directly controls the the MMR Sync state machine in the DIG_CORE domain and ignores the Functional Protection state machine. The RELOAD_FROM_BBD bit can be written with 1 regardless of if RTC is locked or unlocked. RTC will ignore a write of 1 to the RELOAD_FROM_BBD bit if RTC_SYNCPEND.RD_PEND is 1, or if RTC_SYNCPEND.WR_PEND is 1, or if any interrupt status bit in the RTC_IRQSTATUS_RAW_SYS register is 1.

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Table 14-13986. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0068h + formula

Figure 14-6896. RTC_SYNCPEND Name Register

31	30	29	28	27	26	25	24
RELOAD_FROM_BBD	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							PWR_ENABLE_ST
NONE							R
0h							0h
7	6	5	4	3	2	1	0
WKUP_DB_ST				WRT_ERR	O32K_CLK_OBS	RD_PEND	WR_PEND
R				R/W1TC	R	R/W	R/W
0h				0h	0h	0h	0h

Table 14-13987. RTC_SYNCPEND Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RELOAD_FROM_BBD	R/W	0h	The reload_from_bbd allows the registers to be reloaded from the battery backed domain. This is only allowed when the battery backed domain interface state machine is idle. Writing 1 triggers the MMR Sync to read the registers from the battery backed domain. This requires RD_PEND, WR_PEND, and all interrupts' raw status to be 0 when this is written. This operation affects the RD_PEND bit.
30:9	RESERVED	NONE	0h	Reserved
8	PWR_ENABLE_ST	R	0h	The SW can read the state of PIMIC_ENABLE pin, this is raw state
7:4	WKUP_DB_ST	R	0h	The SW can read the state of EXT_WAKEUP pins, this is raw state

Table 14-13987. RTC_SYNCPEND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

3	WRT_ERR	R/W1TC	0h	Write Error Condition
				Wrt 1 to Clr
				Set when SW tries to Wrt when RTL is LOCKED or Wrt when RD_PEND is set
				`0` `Not Occurred`
				`1` `Occurred`

2	O32K_CLK_OBS	R	0h	The SW can read the state of the main 32k clock

1	RD_PEND	R/W	0h	Status of synchronization from ON Domain after CORE reset or RELOAD_FROM_BBD
				`0` `Completed`
				`1` `Pending or active`

0	WR_PEND	R/W	0h	Status of synchronization to ON Domain after writing to CORE Domain over VBUS
				`0` `Completed`
				`1` `Pending or active`

14.7.6.3.2.19 RTC_KICK0 Register

14.7.6.3.2.19.1 RTC_KICK0 Register (Offset = 70h) [reset = 0h]

The written data must be 0x83e70b13 to unlock this register. It must be written before the Kick1 register. The normal procedure to re-lock the functional protection mechanism is to write 0 to this register.

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Table 14-13988. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0070h + formula

Figure 14-6897. RTC_KICK0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">KICK0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">KICK0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">KICK0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">KICK0</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-13989. RTC_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KICK0	W	0h	Kick0 MMR, must write 0x83e70b13 to unlock this register

14.7.6.3.2.20 RTC_KICK1 Register

14.7.6.3.2.20.1 RTC_KICK1 Register (Offset = 74h) [reset = 0h]

The Kick1 register allows writing to unlock the kick1 data and the kicker mechanism to write to other MMRs. The written data must be 0x95a4f1e0 to unlock this register. If this is unlocked after the kick0 register is unlocked then the kicker mechanism is unlocked
The HOST must ensure that there is at least 60 microseconds of delay between a "new" lock state to a "new" unlock state. This should be implemented by ensuring that RTC_SYNCPEND.WR_PEND is 0 before performing the unlock writes. This is a consequence of the limitation that the functional unlock sequence must not be written while the mechanism is unlocked; if the unlock sequence is written at the wrong time, then the core domain and battery domain will not agree about their unlocked status. This will not be diagnosable in software and there is no recommended error recovery sequence for this condition.
For No Analog support, leave it unlocked.

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Table 14-13990. Instance Table

Instance Name	Physical Address
WKUP_RTCSS0	2B1F 0074h + formula

Figure 14-6898. RTC_KICK1 Name Register

31	30	29	28	27	26	25	24
KICK1							
W							
0h							
23	22	21	20	19	18	17	16
KICK1							
W							
0h							
15	14	13	12	11	10	9	8
KICK1							
W							
0h							
7	6	5	4	3	2	1	0
KICK1							
W							
0h							

Table 14-13991. RTC_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	KICK1	W	0h	Kick1 MMR, must write 0x95a4f1e0 to unlock this register and the other MMRs

14.7.6.4 TIMER

TIMER

14.7.6.4.1 TIMER Summaries

TIMER Summaries

Table 14-13992. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER0 Physical Address	TIMER1 Physical Address	TIMER10 Physical Address
0h	32	DMTIMER1MS_TIDR	0240 0000h	0241 0000h	0242 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0240 0010h	0241 0010h	0242 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0240 0020h	0241 0020h	0242 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0240 0024h	0241 0024h	0242 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0240 0028h	0241 0028h	0242 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0240 002Ch	0241 002Ch	0242 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0240 0030h	0241 0030h	0242 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0240 0034h	0241 0034h	0242 0034h
38h	32	DMTIMER1MS_TCLR	0240 0038h	0241 0038h	0242 0038h
3Ch	32	DMTIMER1MS_TCRR	0240 003Ch	0241 003Ch	0242 003Ch
40h	32	DMTIMER1MS_TLDR	0240 0040h	0241 0040h	0242 0040h
44h	32	DMTIMER1MS_TTGR	0240 0044h	0241 0044h	0242 0044h
48h	32	DMTIMER1MS_TWPS	0240 0048h	0241 0048h	0242 0048h
4Ch	32	DMTIMER1MS_TMAR	0240 004Ch	0241 004Ch	0242 004Ch
50h	32	DMTIMER1MS_TCAR1	0240 0050h	0241 0050h	0242 0050h
54h	32	DMTIMER1MS_TSICR	0240 0054h	0241 0054h	0242 0054h
58h	32	DMTIMER1MS_TCAR2	0240 0058h	0241 0058h	0242 0058h
5Ch	32	DMTIMER1MS_TPIR	0240 005Ch	0241 005Ch	0242 005Ch
60h	32	DMTIMER1MS_TNIR	0240 0060h	0241 0060h	0242 0060h
64h	32	DMTIMER1MS_TCVR	0240 0064h	0241 0064h	0242 0064h
68h	32	DMTIMER1MS_TOCR	0240 0068h	0241 0068h	0242 0068h
6Ch	32	DMTIMER1MS_TOWR	0240 006Ch	0241 006Ch	0242 006Ch

Table 14-13993. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER11 Physical Address	TIMER12 Physical Address	TIMER13 Physical Address
0h	32	DMTIMER1MS_TIDR	0243 0000h	0244 0000h	0245 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0243 0010h	0244 0010h	0245 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0243 0020h	0244 0020h	0245 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0243 0024h	0244 0024h	0245 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0243 0028h	0244 0028h	0245 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0243 002Ch	0244 002Ch	0245 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0243 0030h	0244 0030h	0245 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0243 0034h	0244 0034h	0245 0034h
38h	32	DMTIMER1MS_TCLR	0243 0038h	0244 0038h	0245 0038h
3Ch	32	DMTIMER1MS_TCRR	0243 003Ch	0244 003Ch	0245 003Ch
40h	32	DMTIMER1MS_TLDR	0243 0040h	0244 0040h	0245 0040h
44h	32	DMTIMER1MS_TTGR	0243 0044h	0244 0044h	0245 0044h
48h	32	DMTIMER1MS_TWPS	0243 0048h	0244 0048h	0245 0048h

Table 14-13993. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	TIMER11 Physical Address	TIMER12 Physical Address	TIMER13 Physical Address
4Ch	32	DMTIMER1MS_TMAR	0243 004Ch	0244 004Ch	0245 004Ch
50h	32	DMTIMER1MS_TCAR1	0243 0050h	0244 0050h	0245 0050h
54h	32	DMTIMER1MS_TSICR	0243 0054h	0244 0054h	0245 0054h
58h	32	DMTIMER1MS_TCAR2	0243 0058h	0244 0058h	0245 0058h
5Ch	32	DMTIMER1MS_TPIR	0243 005Ch	0244 005Ch	0245 005Ch
60h	32	DMTIMER1MS_TNIR	0243 0060h	0244 0060h	0245 0060h
64h	32	DMTIMER1MS_TCVR	0243 0064h	0244 0064h	0245 0064h
68h	32	DMTIMER1MS_TOCR	0243 0068h	0244 0068h	0245 0068h
6Ch	32	DMTIMER1MS_TOWR	0243 006Ch	0244 006Ch	0245 006Ch

Table 14-13994. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER14 Physical Address	TIMER15 Physical Address	TIMER2 Physical Address
0h	32	DMTIMER1MS_TIDR	0246 0000h	0247 0000h	0248 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0246 0010h	0247 0010h	0248 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0246 0020h	0247 0020h	0248 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0246 0024h	0247 0024h	0248 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0246 0028h	0247 0028h	0248 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0246 002Ch	0247 002Ch	0248 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0246 0030h	0247 0030h	0248 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	0246 0034h	0247 0034h	0248 0034h
38h	32	DMTIMER1MS_TCLR	0246 0038h	0247 0038h	0248 0038h
3Ch	32	DMTIMER1MS_TCRR	0246 003Ch	0247 003Ch	0248 003Ch
40h	32	DMTIMER1MS_TLDR	0246 0040h	0247 0040h	0248 0040h
44h	32	DMTIMER1MS_TTGR	0246 0044h	0247 0044h	0248 0044h
48h	32	DMTIMER1MS_TWPS	0246 0048h	0247 0048h	0248 0048h
4Ch	32	DMTIMER1MS_TMAR	0246 004Ch	0247 004Ch	0248 004Ch
50h	32	DMTIMER1MS_TCAR1	0246 0050h	0247 0050h	0248 0050h
54h	32	DMTIMER1MS_TSICR	0246 0054h	0247 0054h	0248 0054h
58h	32	DMTIMER1MS_TCAR2	0246 0058h	0247 0058h	0248 0058h
5Ch	32	DMTIMER1MS_TPIR	0246 005Ch	0247 005Ch	0248 005Ch
60h	32	DMTIMER1MS_TNIR	0246 0060h	0247 0060h	0248 0060h
64h	32	DMTIMER1MS_TCVR	0246 0064h	0247 0064h	0248 0064h
68h	32	DMTIMER1MS_TOCR	0246 0068h	0247 0068h	0248 0068h
6Ch	32	DMTIMER1MS_TOWR	0246 006Ch	0247 006Ch	0248 006Ch

Table 14-13995. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER3 Physical Address	TIMER4 Physical Address	TIMER5 Physical Address
0h	32	DMTIMER1MS_TIDR	0249 0000h	024A 0000h	024B 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	0249 0010h	024A 0010h	024B 0010h
20h	32	DMTIMER1MS_IRQ_EOI	0249 0020h	024A 0020h	024B 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	0249 0024h	024A 0024h	024B 0024h
28h	32	DMTIMER1MS_IRQSTATUS	0249 0028h	024A 0028h	024B 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	0249 002Ch	024A 002Ch	024B 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	0249 0030h	024A 0030h	024B 0030h

Table 14-13995. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	TIMER3 Physical Address	TIMER4 Physical Address	TIMER5 Physical Address
34h	32	DMTIMER1MS_IRQWAKEEN	0249 0034h	024A 0034h	024B 0034h
38h	32	DMTIMER1MS_TCLR	0249 0038h	024A 0038h	024B 0038h
3Ch	32	DMTIMER1MS_TCRR	0249 003Ch	024A 003Ch	024B 003Ch
40h	32	DMTIMER1MS_TLDR	0249 0040h	024A 0040h	024B 0040h
44h	32	DMTIMER1MS_TTGR	0249 0044h	024A 0044h	024B 0044h
48h	32	DMTIMER1MS_TWPS	0249 0048h	024A 0048h	024B 0048h
4Ch	32	DMTIMER1MS_TMAR	0249 004Ch	024A 004Ch	024B 004Ch
50h	32	DMTIMER1MS_TCAR1	0249 0050h	024A 0050h	024B 0050h
54h	32	DMTIMER1MS_TSICR	0249 0054h	024A 0054h	024B 0054h
58h	32	DMTIMER1MS_TCAR2	0249 0058h	024A 0058h	024B 0058h
5Ch	32	DMTIMER1MS_TPIR	0249 005Ch	024A 005Ch	024B 005Ch
60h	32	DMTIMER1MS_TNIR	0249 0060h	024A 0060h	024B 0060h
64h	32	DMTIMER1MS_TCVR	0249 0064h	024A 0064h	024B 0064h
68h	32	DMTIMER1MS_TOCR	0249 0068h	024A 0068h	024B 0068h
6Ch	32	DMTIMER1MS_TOWR	0249 006Ch	024A 006Ch	024B 006Ch

Table 14-13996. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER6 Physical Address	TIMER7 Physical Address	TIMER8 Physical Address
0h	32	DMTIMER1MS_TIDR	024C 0000h	024D 0000h	024E 0000h
10h	32	DMTIMER1MS_TIOCP_CFG	024C 0010h	024D 0010h	024E 0010h
20h	32	DMTIMER1MS_IRQ_EOI	024C 0020h	024D 0020h	024E 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	024C 0024h	024D 0024h	024E 0024h
28h	32	DMTIMER1MS_IRQSTATUS	024C 0028h	024D 0028h	024E 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	024C 002Ch	024D 002Ch	024E 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	024C 0030h	024D 0030h	024E 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	024C 0034h	024D 0034h	024E 0034h
38h	32	DMTIMER1MS_TCLR	024C 0038h	024D 0038h	024E 0038h
3Ch	32	DMTIMER1MS_TCRR	024C 003Ch	024D 003Ch	024E 003Ch
40h	32	DMTIMER1MS_TLDR	024C 0040h	024D 0040h	024E 0040h
44h	32	DMTIMER1MS_TTGR	024C 0044h	024D 0044h	024E 0044h
48h	32	DMTIMER1MS_TWPS	024C 0048h	024D 0048h	024E 0048h
4Ch	32	DMTIMER1MS_TMAR	024C 004Ch	024D 004Ch	024E 004Ch
50h	32	DMTIMER1MS_TCAR1	024C 0050h	024D 0050h	024E 0050h
54h	32	DMTIMER1MS_TSICR	024C 0054h	024D 0054h	024E 0054h
58h	32	DMTIMER1MS_TCAR2	024C 0058h	024D 0058h	024E 0058h
5Ch	32	DMTIMER1MS_TPIR	024C 005Ch	024D 005Ch	024E 005Ch
60h	32	DMTIMER1MS_TNIR	024C 0060h	024D 0060h	024E 0060h
64h	32	DMTIMER1MS_TCVR	024C 0064h	024D 0064h	024E 0064h
68h	32	DMTIMER1MS_TOCR	024C 0068h	024D 0068h	024E 0068h
6Ch	32	DMTIMER1MS_TOWR	024C 006Ch	024D 006Ch	024E 006Ch

Table 14-13997. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024

Offset	Length	Register Name	TIMER9 Physical Address	WKUP_TIMER0 Physical Address	WKUP_TIMER1 Physical Address
0h	32	DMTIMER1MS_TIDR	024F 0000h	2B10 0000h	2B11 0000h

Table 14-13997. DMTIMER1MS Registers, Base Address=0240 0000h, Length=1024 (continued)

Offset	Length	Register Name	TIMER9 Physical Address	WKUP_TIMER0 Physical Address	WKUP_TIMER1 Physical Address
10h	32	DMTIMER1MS_TIOCP_CFG	024F 0010h	2B10 0010h	2B11 0010h
20h	32	DMTIMER1MS_IRQ_EOI	024F 0020h	2B10 0020h	2B11 0020h
24h	32	DMTIMER1MS_IRQSTATUS_RAW	024F 0024h	2B10 0024h	2B11 0024h
28h	32	DMTIMER1MS_IRQSTATUS	024F 0028h	2B10 0028h	2B11 0028h
2Ch	32	DMTIMER1MS_IRQSTATUS_SET	024F 002Ch	2B10 002Ch	2B11 002Ch
30h	32	DMTIMER1MS_IRQSTATUS_CLR	024F 0030h	2B10 0030h	2B11 0030h
34h	32	DMTIMER1MS_IRQWAKEEN	024F 0034h	2B10 0034h	2B11 0034h
38h	32	DMTIMER1MS_TCLR	024F 0038h	2B10 0038h	2B11 0038h
3Ch	32	DMTIMER1MS_TCRR	024F 003Ch	2B10 003Ch	2B11 003Ch
40h	32	DMTIMER1MS_TLDR	024F 0040h	2B10 0040h	2B11 0040h
44h	32	DMTIMER1MS_TTGR	024F 0044h	2B10 0044h	2B11 0044h
48h	32	DMTIMER1MS_TWPS	024F 0048h	2B10 0048h	2B11 0048h
4Ch	32	DMTIMER1MS_TMAR	024F 004Ch	2B10 004Ch	2B11 004Ch
50h	32	DMTIMER1MS_TCAR1	024F 0050h	2B10 0050h	2B11 0050h
54h	32	DMTIMER1MS_TSICR	024F 0054h	2B10 0054h	2B11 0054h
58h	32	DMTIMER1MS_TCAR2	024F 0058h	2B10 0058h	2B11 0058h
5Ch	32	DMTIMER1MS_TPIR	024F 005Ch	2B10 005Ch	2B11 005Ch
60h	32	DMTIMER1MS_TNIR	024F 0060h	2B10 0060h	2B11 0060h
64h	32	DMTIMER1MS_TCVR	024F 0064h	2B10 0064h	2B11 0064h
68h	32	DMTIMER1MS_TOCR	024F 0068h	2B10 0068h	2B11 0068h
6Ch	32	DMTIMER1MS_TOWR	024F 006Ch	2B10 006Ch	2B11 006Ch

14.7.6.4.2 TIMER Registers

TIMER Registers

14.7.6.4.2.1 DMTIMER1MS_TIDR Register

14.7.6.4.2.1.1 DMTIMER1MS_TIDR Register (Offset = 0h) [reset = 50003900h]

Peripheral ID

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Table 14-13998. Instance Table

Instance Name	Physical Address
TIMER0	0240 0000h
TIMER1	0241 0000h
TIMER2	0242 0000h
TIMER3	0243 0000h
TIMER4	0244 0000h
TIMER5	0245 0000h
TIMER6	0246 0000h
TIMER7	0247 0000h
TIMER8	0248 0000h
TIMER9	0249 0000h
TIMER10	024A 0000h
TIMER11	024B 0000h
TIMER12	024C 0000h
TIMER13	024D 0000h
TIMER14	024E 0000h
TIMER15	024F 0000h
WKUP_TIMER0	2B10 0000h
WKUP_TIMER1	2B11 0000h

Figure 14-6899. DMTIMER1MS_TIDR Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		1h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
7h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-13999. DMTIMER1MS_TIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: mod_g_rst_n

Table 14-13999. DMTIMER1MS_TIDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description

29:28	BU	R	1h	Business Unit
				`1 Wireless BU`
				`2 Processors BU`

27:16	MODULE_ID	R	0h	Module ID Reset Source: mod_g_rst_n
15:11	RTL	R	7h	RTL revision. Will vary depending on release. Reset Source: mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: mod_g_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: mod_g_rst_n

14.7.6.4.2.2 DMTIMER1MS_TIOCP_CFG Register

14.7.6.4.2.2.1 DMTIMER1MS_TIOCP_CFG Register (Offset = 10h) [reset = 8h]

This register controls the various parameters of the OCP interface

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Table 14-14000. Instance Table

Instance Name	Physical Address
TIMER0	0240 0010h
TIMER1	0241 0010h
TIMER2	0242 0010h
TIMER3	0243 0010h
TIMER4	0244 0010h
TIMER5	0245 0010h
TIMER6	0246 0010h
TIMER7	0247 0010h
TIMER8	0248 0010h
TIMER9	0249 0010h
TIMER10	024A 0010h
TIMER11	024B 0010h
TIMER12	024C 0010h
TIMER13	024D 0010h
TIMER14	024E 0010h
TIMER15	024F 0010h
WKUP_TIMER0	2B10 0010h
WKUP_TIMER1	2B11 0010h

Figure 14-6900. DMTIMER1MS_TIOCP_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				IDLEMODE		EMUFREE	SOFTRESET
NONE				R/W		R/W	R/W
0h				2h		0h	0h

Table 14-14001. DMTIMER1MS_TIOCP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved

Table 14-14001. DMTIMER1MS_TIOCP_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	IDLEMODE	R/W	2h	Idle Mode 0 local target's idle state follows (acknowledges) the system's idle reuquests unconditionaly, i.e. regardless of the IP module's internal requirments. Back mode, for debug only. 1 local target never enteres idle state. Back mode, for debug only. 2 local target's idle state eventually follows (acknowledges) the systems' idle requests, depending on the IP module's internal requirments. IP module shall not generate (IRQ- or DMA-request-releated) wakuep events. 3 local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirents. IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state. Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) impolemented.
1	EMUFREE	R/W	0h	Emulation Mode 0 The timer is frozen in emulation mode (PI_SUSPEND signal active) 1 The timer runs free, regardless of PI_SUSPEND value
0	SOFTRESET	R/W	0h	Software reset 0 Read: Reset Done, no pending action Write: no action 1 Read: Reset ongoing Write: initiate software reset

14.7.6.4.2.3 DMTIMER1MS_IRQ_EOI Register

14.7.6.4.2.3.1 DMTIMER1MS_IRQ_EOI Register (Offset = 20h) [reset = 0h]

Allows the generation of further pulses on the interrupt line, if an new interrupt event is pending, when using the pulsed output. Unused when using the level interrupt line

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Table 14-14002. Instance Table

Instance Name	Physical Address
TIMER0	0240 0020h
TIMER1	0241 0020h
TIMER2	0242 0020h
TIMER3	0243 0020h
TIMER4	0244 0020h
TIMER5	0245 0020h
TIMER6	0246 0020h
TIMER7	0247 0020h
TIMER8	0248 0020h
TIMER9	0249 0020h
TIMER10	024A 0020h
TIMER11	024B 0020h
TIMER12	024C 0020h
TIMER13	024D 0020h
TIMER14	024E 0020h
TIMER15	024F 0020h
WKUP_TIMER0	2B10 0020h
WKUP_TIMER1	2B11 0020h

Figure 14-6901. DMTIMER1MS_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINE_NUMBER
NONE							R/W
0h							0h

Table 14-14003. DMTIMER1MS_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved

Table 14-14003. DMTIMER1MS_IRQ_EOI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LINE_NUMBER	R/W	0h	Idle Mode 0 `End of interrupt`

14.7.6.4.2.4 DMTIMER1MS_IRQSTATUS_RAW Register

14.7.6.4.2.4.1 DMTIMER1MS_IRQSTATUS_RAW Register (Offset = 24h) [reset = 0h]

Component interrupt request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug

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Table 14-14004. Instance Table

Instance Name	Physical Address
TIMER0	0240 0024h
TIMER1	0241 0024h
TIMER2	0242 0024h
TIMER3	0243 0024h
TIMER4	0244 0024h
TIMER5	0245 0024h
TIMER6	0246 0024h
TIMER7	0247 0024h
TIMER8	0248 0024h
TIMER9	0249 0024h
TIMER10	024A 0024h
TIMER11	024B 0024h
TIMER12	024C 0024h
TIMER13	024D 0024h
TIMER14	024E 0024h
TIMER15	024F 0024h
WKUP_TIMER0	2B10 0024h
WKUP_TIMER1	2B11 0024h

Figure 14-6902. DMTIMER1MS_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 14-14005. DMTIMER1MS_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-14005. DMTIMER1MS_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TCAR_IT_FLAG	R/W1TS	0h	Capture Interrupt Reset Source: mod_g_rst_n
1	OVF_IT_FLAG	R/W1TS	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TS	0h	Match Interrupt Reset Source: mod_g_rst_n

14.7.6.4.2.5 DMTIMER1MS_IRQSTATUS Register

14.7.6.4.2.5.1 DMTIMER1MS_IRQSTATUS Register (Offset = 28h) [reset = 0h]

Component interrupt request status. Check the corresponding secondary status register.Enabled status isn't set unless event is enabled.Write 1 to clear the status after interrupt has been serviced;raw status gets cleared, i.e. even if not enabled

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Table 14-14006. Instance Table

Instance Name	Physical Address
TIMER0	0240 0028h
TIMER1	0241 0028h
TIMER2	0242 0028h
TIMER3	0243 0028h
TIMER4	0244 0028h
TIMER5	0245 0028h
TIMER6	0246 0028h
TIMER7	0247 0028h
TIMER8	0248 0028h
TIMER9	0249 0028h
TIMER10	024A 0028h
TIMER11	024B 0028h
TIMER12	024C 0028h
TIMER13	024D 0028h
TIMER14	024E 0028h
TIMER15	024F 0028h
WKUP_TIMER0	2B10 0028h
WKUP_TIMER1	2B11 0028h

Figure 14-6903. DMTIMER1MS_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-14007. DMTIMER1MS_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	TCAR_IT_FLAG	R/W1TC	0h	Capture Interrupt Reset Source: mod_g_rst_n
1	OVF_IT_FLAG	R/W1TC	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TC	0h	Match Interrupt Reset Source: mod_g_rst_n

14.7.6.4.2.6 DMTIMER1MS_IRQSTATUS_SET Register

14.7.6.4.2.6.1 DMTIMER1MS_IRQSTATUS_SET Register (Offset = 2Ch) [reset = 0h]

Component interrupt request enable Write 1 to set;enable interrupt. Readout equal to corresponding _CLR register.

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Table 14-14008. Instance Table

Instance Name	Physical Address
TIMER0	0240 002Ch
TIMER1	0241 002Ch
TIMER2	0242 002Ch
TIMER3	0243 002Ch
TIMER4	0244 002Ch
TIMER5	0245 002Ch
TIMER6	0246 002Ch
TIMER7	0247 002Ch
TIMER8	0248 002Ch
TIMER9	0249 002Ch
TIMER10	024A 002Ch
TIMER11	024B 002Ch
TIMER12	024C 002Ch
TIMER13	024D 002Ch
TIMER14	024E 002Ch
TIMER15	024F 002Ch
WKUP_TIMER0	2B10 002Ch
WKUP_TIMER1	2B11 002Ch

Figure 14-6904. DMTIMER1MS_IRQSTATUS_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td>TCAR_IT_FLAG</td><td>OVF_IT_FLAG</td><td>MAT_IT_FLAG</td></tr>
<tr><td colspan="5">NONE</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="5">0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14009. DMTIMER1MS_IRQSTATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-14009. DMTIMER1MS_IRQSTATUS_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TCAR_IT_FLAG	R/W1TS	0h	Capture Interrupt Reset Source: mod_g_rst_n
1	OVF_IT_FLAG	R/W1TS	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TS	0h	Match Interrupt Reset Source: mod_g_rst_n

14.7.6.4.2.7 DMTIMER1MS_IRQSTATUS_CLR Register

14.7.6.4.2.7.1 DMTIMER1MS_IRQSTATUS_CLR Register (Offset = 30h) [reset = 0h]

Component interrupt request enable. Write 1 to clear; disable interrupt. Readout equal to corresponding _SET register

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Table 14-14010. Instance Table

Instance Name	Physical Address
TIMER0	0240 0030h
TIMER1	0241 0030h
TIMER2	0242 0030h
TIMER3	0243 0030h
TIMER4	0244 0030h
TIMER5	0245 0030h
TIMER6	0246 0030h
TIMER7	0247 0030h
TIMER8	0248 0030h
TIMER9	0249 0030h
TIMER10	024A 0030h
TIMER11	024B 0030h
TIMER12	024C 0030h
TIMER13	024D 0030h
TIMER14	024E 0030h
TIMER15	024F 0030h
WKUP_TIMER0	2B10 0030h
WKUP_TIMER1	2B11 0030h

Figure 14-6905. DMTIMER1MS_IRQSTATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 14-14011. DMTIMER1MS_IRQSTATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-14011. DMTIMER1MS_IRQSTATUS_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TCAR_IT_FLAG	R/W1TC	0h	Capture Interrupt Reset Source: mod_g_rst_n
1	OVF_IT_FLAG	R/W1TC	0h	Overflow Interrupt Reset Source: mod_g_rst_n
0	MAT_IT_FLAG	R/W1TC	0h	Match Interrupt Reset Source: mod_g_rst_n

14.7.6.4.2.8 DMTIMER1MS_IRQWAKEEN Register

14.7.6.4.2.8.1 DMTIMER1MS_IRQWAKEEN Register (Offset = 34h) [reset = 0h]

Wakeup-enabled events taking place when module is idle shall generate an asynchronous wakeup

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Table 14-14012. Instance Table

Instance Name	Physical Address
TIMER0	0240 0034h
TIMER1	0241 0034h
TIMER2	0242 0034h
TIMER3	0243 0034h
TIMER4	0244 0034h
TIMER5	0245 0034h
TIMER6	0246 0034h
TIMER7	0247 0034h
TIMER8	0248 0034h
TIMER9	0249 0034h
TIMER10	024A 0034h
TIMER11	024B 0034h
TIMER12	024C 0034h
TIMER13	024D 0034h
TIMER14	024E 0034h
TIMER15	024F 0034h
WKUP_TIMER0	2B10 0034h
WKUP_TIMER1	2B11 0034h

Figure 14-6906. DMTIMER1MS_IRQWAKEEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MAT_WUP_ENA	OVF_WUP_ENA	TCAR_WUP_ENA
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 14-14013. DMTIMER1MS_IRQWAKEEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved

Table 14-14013. DMTIMER1MS_IRQWAKEEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MAT_WUP_ENA	R/W	0h	Match Wakeup Enable Reset Source: mod_g_rst_n
1	OVF_WUP_ENA	R/W	0h	Overflow Wakeup Enable Reset Source: mod_g_rst_n
0	TCAR_WUP_ENA	R/W	0h	Capture Wakeup Enable Reset Source: mod_g_rst_n

14.7.6.4.2.9 DMTIMER1MS_TCLR Register

14.7.6.4.2.9.1 DMTIMER1MS_TCLR Register (Offset = 38h) [reset = 0h]

This register controls optional features specific to the timer functionality

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Table 14-14014. Instance Table

Instance Name	Physical Address
TIMER0	0240 0038h
TIMER1	0241 0038h
TIMER2	0242 0038h
TIMER3	0243 0038h
TIMER4	0244 0038h
TIMER5	0245 0038h
TIMER6	0246 0038h
TIMER7	0247 0038h
TIMER8	0248 0038h
TIMER9	0249 0038h
TIMER10	024A 0038h
TIMER11	024B 0038h
TIMER12	024C 0038h
TIMER13	024D 0038h
TIMER14	024E 0038h
TIMER15	024F 0038h
WKUP_TIMER0	2B10 0038h
WKUP_TIMER1	2B11 0038h

Figure 14-6907. DMTIMER1MS_TCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td>GPO_CFG</td><td>CAPT_MODE</td><td>PT</td><td colspan="2">TRG</td><td colspan="2">TCM</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SCPWM</td><td>CE</td><td>PRE</td><td colspan="3">PTV</td><td>AR</td><td>ST</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="3">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="3">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14015. DMTIMER1MS_TCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	GPO_CFG	R/W	0h	This field drives directly the timer_gpocfg port Reset Source: mod_g_rst_n

Table 14-14015. DMTIMER1MS_TCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CAPT_MODE	R/W	0h	Capture mode select bit; First/second 0 `Capture first enabled capture event in TCAR1` 1 `Capture first enabled capture event in TCAR2`
12	PT	R/W	0h	Pulse or Toggle select bit 0 `Pulse modulation` 0 `Toggle modulation`
11:10	TRG	R/W	0h	Trigger Output Mode 0 `No Trigger` 1 `Overflow Trigger` 2 `Overflow and match Trigger`
9:8	TCM	R/W	0h	Transition Capture Mode 0 `No capture` 1 `Capture on rising edges of PI_EVNETCAPT` 2 `Capture on falling edges of PI_EVENTCAPT` 3 `Capture on both edges of PI_EVNENTCAPT`
7	SCPWM	R/W	0h	Pulse Width Modulation output pin default value Reset Source: mod_g_rst_n
6	CE	R/W	0h	Compare Enable 0 `compare disabled` 1 `compare enabled`
5	PRE	R/W	0h	Prescaler Enable 0 `Prescaler disabeld` 1 `Prescaler Enabled`
4:2	PTV	R/W	0h	Trigger Output Mode. The timer counter is prescaled with the value: 2^PTV Reset Source: mod_g_rst_n
1	AR	R/W	0h	Auto-reload mode 0 `One shot mode overflow` 1 `Auto-reload mode overflow`
0	ST	R/W	0h	Start/Stop timer control 0 `Stop the timer` 1 `Start the timer`

14.7.6.4.2.10 DMTIMER1MS_TCRR Register

14.7.6.4.2.10.1 DMTIMER1MS_TCRR Register (Offset = 3Ch) [reset = 0h]

This register holds the value of the internal counter

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Table 14-14016. Instance Table

Instance Name	Physical Address
TIMER0	0240 003Ch
TIMER1	0241 003Ch
TIMER2	0242 003Ch
TIMER3	0243 003Ch
TIMER4	0244 003Ch
TIMER5	0245 003Ch
TIMER6	0246 003Ch
TIMER7	0247 003Ch
TIMER8	0248 003Ch
TIMER9	0249 003Ch
TIMER10	024A 003Ch
TIMER11	024B 003Ch
TIMER12	024C 003Ch
TIMER13	024D 003Ch
TIMER14	024E 003Ch
TIMER15	024F 003Ch
WKUP_TIMER0	2B10 003Ch
WKUP_TIMER1	2B11 003Ch

Figure 14-6908. DMTIMER1MS_TCRR Name Register

31	30	29	28	27	26	25	24
TIMER_COUNTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TIMER_COUNTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TIMER_COUNTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TIMER_COUNTER							
R/W							
0h							

Table 14-14017. DMTIMER1MS_TCRR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIMER_COUNTER	R/W	0h	Timer Counter Reset Source: mod_g_rst_n

14.7.6.4.2.11 DMTIMER1MS_TLDR Register

14.7.6.4.2.11.1 DMTIMER1MS_TLDR Register (Offset = 40h) [reset = 0h]

This register holds the timer's load value

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Table 14-14018. Instance Table

Instance Name	Physical Address
TIMER0	0240 0040h
TIMER1	0241 0040h
TIMER2	0242 0040h
TIMER3	0243 0040h
TIMER4	0244 0040h
TIMER5	0245 0040h
TIMER6	0246 0040h
TIMER7	0247 0040h
TIMER8	0248 0040h
TIMER9	0249 0040h
TIMER10	024A 0040h
TIMER11	024B 0040h
TIMER12	024C 0040h
TIMER13	024D 0040h
TIMER14	024E 0040h
TIMER15	024F 0040h
WKUP_TIMER0	2B10 0040h
WKUP_TIMER1	2B11 0040h

Figure 14-6909. DMTIMER1MS_TLDR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOAD_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOAD_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOAD_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOAD_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14019. DMTIMER1MS_TLDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOAD_VALUE	R/W	0h	Timer Counter Reset Source: mod_g_rst_n

14.7.6.4.2.12 DMTIMER1MS_TTGR Register

14.7.6.4.2.12.1 DMTIMER1MS_TTGR Register (Offset = 44h) [reset = 0h]

This register triggers a counter reload of timer by writing any value in it

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Table 14-14020. Instance Table

Instance Name	Physical Address
TIMER0	0240 0044h
TIMER1	0241 0044h
TIMER2	0242 0044h
TIMER3	0243 0044h
TIMER4	0244 0044h
TIMER5	0245 0044h
TIMER6	0246 0044h
TIMER7	0247 0044h
TIMER8	0248 0044h
TIMER9	0249 0044h
TIMER10	024A 0044h
TIMER11	024B 0044h
TIMER12	024C 0044h
TIMER13	024D 0044h
TIMER14	024E 0044h
TIMER15	024F 0044h
WKUP_TIMER0	2B10 0044h
WKUP_TIMER1	2B11 0044h

Figure 14-6910. DMTIMER1MS_TTGR Name Register

31	30	29	28	27	26	25	24
TTRG_VLAUE							
R/W							
0h							
23	22	21	20	19	18	17	16
TTRG_VLAUE							
R/W							
0h							
15	14	13	12	11	10	9	8
TTRG_VLAUE							
R/W							
0h							
7	6	5	4	3	2	1	0
TTRG_VLAUE							
R/W							
0h							

Table 14-14021. DMTIMER1MS_TTGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TTRG_VLAUE	R/W	0h	The value of the trigger register. During reads, it always return 0xFFFF_FFFF Reset Source: mod_g_rst_n

14.7.6.4.2.13 DMTIMER1MS_TWPS Register

14.7.6.4.2.13.1 DMTIMER1MS_TWPS Register (Offset = 48h) [reset = 0h]

This register contains the write posting bits for all writ-able functional registers

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Table 14-14022. Instance Table

Instance Name	Physical Address
TIMER0	0240 0048h
TIMER1	0241 0048h
TIMER2	0242 0048h
TIMER3	0243 0048h
TIMER4	0244 0048h
TIMER5	0245 0048h
TIMER6	0246 0048h
TIMER7	0247 0048h
TIMER8	0248 0048h
TIMER9	0249 0048h
TIMER10	024A 0048h
TIMER11	024B 0048h
TIMER12	024C 0048h
TIMER13	024D 0048h
TIMER14	024E 0048h
TIMER15	024F 0048h
WKUP_TIMER0	2B10 0048h
WKUP_TIMER1	2B11 0048h

Figure 14-6911. DMTIMER1MS_TWPS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						W_PEND_TOWR	W_PEND_TOCR
NONE						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
W_PEND_TCVR	W_PEND_TNIR	W_PEND_TPIR	W_PEND_TMAR	W_PEND_TTGR	W_PEND_TLDR	W_PEND_TCRR	W_PEND_TCLR
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14023. DMTIMER1MS_TWPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved

Table 14-14023. DMTIMER1MS_TWPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	W_PEND_TOWR	R	0h	Write pending for register TOWR Reset Source: mod_g_rst_n
8	W_PEND_TOCR	R	0h	Write pending for register TOCR Reset Source: mod_g_rst_n
7	W_PEND_TCVR	R	0h	Write pending for register TCVR Reset Source: mod_g_rst_n
6	W_PEND_TNIR	R	0h	Write pending for register TNIR Reset Source: mod_g_rst_n
5	W_PEND_TPIR	R	0h	Write pending for register TPIR Reset Source: mod_g_rst_n
4	W_PEND_TMAR	R	0h	Write pending for register TMAR Reset Source: mod_g_rst_n
3	W_PEND_TTGR	R	0h	Write pending for register TTGR Reset Source: mod_g_rst_n
2	W_PEND_TLDR	R	0h	Write pending for register TLDR Reset Source: mod_g_rst_n
1	W_PEND_TCRR	R	0h	Write pending for register TCRR Reset Source: mod_g_rst_n
0	W_PEND_TCLR	R	0h	Write pending for register TCLR Reset Source: mod_g_rst_n

14.7.6.4.2.14 DMTIMER1MS_TMAR Register

14.7.6.4.2.14.1 DMTIMER1MS_TMAR Register (Offset = 4Ch) [reset = 0h]

This register holds the match value to be compared with the counter's value

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Table 14-14024. Instance Table

Instance Name	Physical Address
TIMER0	0240 004Ch
TIMER1	0241 004Ch
TIMER2	0242 004Ch
TIMER3	0243 004Ch
TIMER4	0244 004Ch
TIMER5	0245 004Ch
TIMER6	0246 004Ch
TIMER7	0247 004Ch
TIMER8	0248 004Ch
TIMER9	0249 004Ch
TIMER10	024A 004Ch
TIMER11	024B 004Ch
TIMER12	024C 004Ch
TIMER13	024D 004Ch
TIMER14	024E 004Ch
TIMER15	024F 004Ch
WKUP_TIMER0	2B10 004Ch
WKUP_TIMER1	2B11 004Ch

Figure 14-6912. DMTIMER1MS_TMAR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COMPARE_VLAUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COMPARE_VLAUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COMPARE_VLAUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMPARE_VLAUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14025. DMTIMER1MS_TMAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMPARE_VLAUE	R/W	0h	The value of the match register Reset Source: mod_g_rst_n

14.7.6.4.2.15 DMTIMER1MS_TCAR1 Register

14.7.6.4.2.15.1 DMTIMER1MS_TCAR1 Register (Offset = 50h) [reset = 0h]

This register holds the value of the first counter register capture

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Table 14-14026. Instance Table

Instance Name	Physical Address
TIMER0	0240 0050h
TIMER1	0241 0050h
TIMER2	0242 0050h
TIMER3	0243 0050h
TIMER4	0244 0050h
TIMER5	0245 0050h
TIMER6	0246 0050h
TIMER7	0247 0050h
TIMER8	0248 0050h
TIMER9	0249 0050h
TIMER10	024A 0050h
TIMER11	024B 0050h
TIMER12	024C 0050h
TIMER13	024D 0050h
TIMER14	024E 0050h
TIMER15	024F 0050h
WKUP_TIMER0	2B10 0050h
WKUP_TIMER1	2B11 0050h

Figure 14-6913. DMTIMER1MS_TCAR1 Name Register

31	30	29	28	27	26	25	24
CAPTURE_VALUE1							
R							
0h							
23	22	21	20	19	18	17	16
CAPTURE_VALUE1							
R							
0h							
15	14	13	12	11	10	9	8
CAPTURE_VALUE1							
R							
0h							
7	6	5	4	3	2	1	0
CAPTURE_VALUE1							
R							
0h							

Table 14-14027. DMTIMER1MS_TCAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPTURE_VALUE1	R	0h	The value of first captured counter register Reset Source: mod_g_rst_n

14.7.6.4.2.16 DMTIMER1MS_TSICR Register

14.7.6.4.2.16.1 DMTIMER1MS_TSICR Register (Offset = 54h) [reset = 0h]

Timer Synchronous Interface Control Register

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Table 14-14028. Instance Table

Instance Name	Physical Address
TIMER0	0240 0054h
TIMER1	0241 0054h
TIMER2	0242 0054h
TIMER3	0243 0054h
TIMER4	0244 0054h
TIMER5	0245 0054h
TIMER6	0246 0054h
TIMER7	0247 0054h
TIMER8	0248 0054h
TIMER9	0249 0054h
TIMER10	024A 0054h
TIMER11	024B 0054h
TIMER12	024C 0054h
TIMER13	024D 0054h
TIMER14	024E 0054h
TIMER15	024F 0054h
WKUP_TIMER0	2B10 0054h
WKUP_TIMER1	2B11 0054h

Figure 14-6914. DMTIMER1MS_TSICR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			READ_AFTER_IDLE	READ_MODE	POSTED	SFT	RESERVED
NONE			W	W	R/W	R/W	NONE
0h			0h	0h	0h	0h	0h

Table 14-14029. DMTIMER1MS_TSICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved

Table 14-14029. DMTIMER1MS_TSICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	READ_AFTER_IDLE	W	0h	Select if the synchronization mechanism used for first TCRR read operation after IDLE state is active 0 The synchronization mechanism is enabled 1 The synchronization mechanism is disabled
3	READ_MODE	W	0h	Select posted/non-posted mode for read operation. This bit is not used when configured in posted mode 0 when the module is configurated in non-posted mode the read operation is executed as posted read 1 when the module is configured in non-posted mode the read operation is executed as read non-posted
2	POSTED	R/W	0h	Reset value of POSTED depends on hardware integration module at design time. Software must read POSTED field to get the hardwar module configuration 0 Posted mode inactive: will delay the command accept output signal 1 Posted mode active
1	SFT	R/W	0h	This bit reset all the functional part of teh module 0 Software reset is disabled 1 Software reset is enabled
0	RESERVED	NONE	0h	Reserved

14.7.6.4.2.17 DMTIMER1MS_TCAR2 Register

14.7.6.4.2.17.1 DMTIMER1MS_TCAR2 Register (Offset = 58h) [reset = 0h]

This register holds the value of the second counter register capture

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Table 14-14030. Instance Table

Instance Name	Physical Address
TIMER0	0240 0058h
TIMER1	0241 0058h
TIMER2	0242 0058h
TIMER3	0243 0058h
TIMER4	0244 0058h
TIMER5	0245 0058h
TIMER6	0246 0058h
TIMER7	0247 0058h
TIMER8	0248 0058h
TIMER9	0249 0058h
TIMER10	024A 0058h
TIMER11	024B 0058h
TIMER12	024C 0058h
TIMER13	024D 0058h
TIMER14	024E 0058h
TIMER15	024F 0058h
WKUP_TIMER0	2B10 0058h
WKUP_TIMER1	2B11 0058h

Figure 14-6915. DMTIMER1MS_TCAR2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CAPTURE_VALUE2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CAPTURE_VALUE2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CAPTURE_VALUE2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CAPTURE_VALUE2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14031. DMTIMER1MS_TCAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPTURE_VALUE2	R	0h	The value of second captured counter register Reset Source: mod_g_rst_n

14.7.6.4.2.18 DMTIMER1MS_TPIR Register

14.7.6.4.2.18.1 DMTIMER1MS_TPIR Register (Offset = 5Ch) [reset = 0h]

This register is used for 1ms tick generation. The TPIR register holds the value of the positive increment. The value of this register is added with the value of the TCVR to define whether next value loaded in TCRR will be the sub-period value or the over-period value

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Table 14-14032. Instance Table

Instance Name	Physical Address
TIMER0	0240 005Ch
TIMER1	0241 005Ch
TIMER2	0242 005Ch
TIMER3	0243 005Ch
TIMER4	0244 005Ch
TIMER5	0245 005Ch
TIMER6	0246 005Ch
TIMER7	0247 005Ch
TIMER8	0248 005Ch
TIMER9	0249 005Ch
TIMER10	024A 005Ch
TIMER11	024B 005Ch
TIMER12	024C 005Ch
TIMER13	024D 005Ch
TIMER14	024E 005Ch
TIMER15	024F 005Ch
WKUP_TIMER0	2B10 005Ch
WKUP_TIMER1	2B11 005Ch

Figure 14-6916. DMTIMER1MS_TPIR Name Register

31	30	29	28	27	26	25	24
POSITIVE_INC_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
POSITIVE_INC_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
POSITIVE_INC_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
POSITIVE_INC_VALUE							
R/W							
0h							

Table 14-14033. DMTIMER1MS_TPIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POSITIVE_INC_VALUE	R/W	0h	The value of the positive increment Reset Source: mod_g_rst_n

14.7.6.4.2.19 DMTIMER1MS_TNIR Register

14.7.6.4.2.19.1 DMTIMER1MS_TNIR Register (Offset = 60h) [reset = 0h]

This register is used for 1ms tick generation. The TNIR register holds the value of the negative increment. The value of this register is added with the value of the TCVR to define whether next value loaded in TCRR will be the sub-period value or the over-period value

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Table 14-14034. Instance Table

Instance Name	Physical Address
TIMER0	0240 0060h
TIMER1	0241 0060h
TIMER2	0242 0060h
TIMER3	0243 0060h
TIMER4	0244 0060h
TIMER5	0245 0060h
TIMER6	0246 0060h
TIMER7	0247 0060h
TIMER8	0248 0060h
TIMER9	0249 0060h
TIMER10	024A 0060h
TIMER11	024B 0060h
TIMER12	024C 0060h
TIMER13	024D 0060h
TIMER14	024E 0060h
TIMER15	024F 0060h
WKUP_TIMER0	2B10 0060h
WKUP_TIMER1	2B11 0060h

Figure 14-6917. DMTIMER1MS_TNIR Name Register

31	30	29	28	27	26	25	24
NEGATIVE_INC_VALUE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NEGATIVE_INC_VALUE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NEGATIVE_INC_VALUE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEGATIVE_INC_VALUE							
R/W							
0h							

Table 14-14035. DMTIMER1MS_TNIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NEGATIVE_INC_VALUE	R/W	0h	The value of the negative increment Reset Source: mod_g_rst_n

14.7.6.4.2.20 DMTIMER1MS_TCVR Register

14.7.6.4.2.20.1 DMTIMER1MS_TCVR Register (Offset = 64h) [reset = 0h]

This register is used for 1ms tick generation. The TCVR register defines whether next value loaded in TCRR will be the sub-period value or the over-period value

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Table 14-14036. Instance Table

Instance Name	Physical Address
TIMER0	0240 0064h
TIMER1	0241 0064h
TIMER2	0242 0064h
TIMER3	0243 0064h
TIMER4	0244 0064h
TIMER5	0245 0064h
TIMER6	0246 0064h
TIMER7	0247 0064h
TIMER8	0248 0064h
TIMER9	0249 0064h
TIMER10	024A 0064h
TIMER11	024B 0064h
TIMER12	024C 0064h
TIMER13	024D 0064h
TIMER14	024E 0064h
TIMER15	024F 0064h
WKUP_TIMER0	2B10 0064h
WKUP_TIMER1	2B11 0064h

Figure 14-6918. DMTIMER1MS_TCVR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">COUNTER_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNTER_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNTER_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNTER_VALUE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14037. DMTIMER1MS_TCVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNTER_VALUE	R/W	0h	The value of CVR counter Reset Source: mod_g_rst_n

14.7.6.4.2.21 DMTIMER1MS_TOCR Register

14.7.6.4.2.21.1 DMTIMER1MS_TOCR Register (Offset = 68h) [reset = 0h]

This register is used to mask the tick interrupt for a selected number of ticks

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Table 14-14038. Instance Table

Instance Name	Physical Address
TIMER0	0240 0068h
TIMER1	0241 0068h
TIMER2	0242 0068h
TIMER3	0243 0068h
TIMER4	0244 0068h
TIMER5	0245 0068h
TIMER6	0246 0068h
TIMER7	0247 0068h
TIMER8	0248 0068h
TIMER9	0249 0068h
TIMER10	024A 0068h
TIMER11	024B 0068h
TIMER12	024C 0068h
TIMER13	024D 0068h
TIMER14	024E 0068h
TIMER15	024F 0068h
WKUP_TIMER0	2B10 0068h
WKUP_TIMER1	2B11 0068h

Figure 14-6919. DMTIMER1MS_TOCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OVF_COUNTER_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
OVF_COUNTER_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
OVF_COUNTER_VALUE							
R/W							
0h							

Table 14-14039. DMTIMER1MS_TOCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

Table 14-14039. DMTIMER1MS_TOCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	OVF_COUNTER_VALUE	R/W	0h	The number of overflow events Reset Source: mod_g_rst_n

14.7.6.4.2.22 DMTIMER1MS_TOWR Register

14.7.6.4.2.22.1 DMTIMER1MS_TOWR Register (Offset = 6Ch) [reset = 0h]

This register holds the number of masked overflow interrupts

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Table 14-14040. Instance Table

Instance Name	Physical Address
TIMER0	0240 006Ch
TIMER1	0241 006Ch
TIMER2	0242 006Ch
TIMER3	0243 006Ch
TIMER4	0244 006Ch
TIMER5	0245 006Ch
TIMER6	0246 006Ch
TIMER7	0247 006Ch
TIMER8	0248 006Ch
TIMER9	0249 006Ch
TIMER10	024A 006Ch
TIMER11	024B 006Ch
TIMER12	024C 006Ch
TIMER13	024D 006Ch
TIMER14	024E 006Ch
TIMER15	024F 006Ch
WKUP_TIMER0	2B10 006Ch
WKUP_TIMER1	2B11 006Ch

Figure 14-6920. DMTIMER1MS_TOWR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OVF_WRAPPING_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
OVF_WRAPPING_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
OVF_WRAPPING_VALUE							
R/W							
0h							

Table 14-14041. DMTIMER1MS_TOWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

Table 14-14041. DMTIMER1MS_TOWR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	OVF_WRAPPING_VALUE	R/W	0h	The number of masked interrupts Reset Source: mod_g_rst_n

14.7.7 Internal Diagnostics Modules Registers

14.7.7.1 DCC

DCC

14.7.7.1.1 DCC Summaries

DCC Summaries

Table 14-14042. DCC2 Registers, Base Address=0080 0000h, Length=64

Offset	Length	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
0h	32	DCC2_DCCGCTRL	0080 0000h	0080 4000h	0080 8000h
4h	32	DCC2_DCCREV	0080 0004h	0080 4004h	0080 8004h
8h	32	DCC2_DCCCNTSEED0	0080 0008h	0080 4008h	0080 8008h
Ch	32	DCC2_DCCVALIDSEED0	0080 000Ch	0080 400Ch	0080 800Ch
10h	32	DCC2_DCCCNTSEED1	0080 0010h	0080 4010h	0080 8010h
14h	32	DCC2_DCCSTATUS	0080 0014h	0080 4014h	0080 8014h
18h	32	DCC2_DCCCNT0	0080 0018h	0080 4018h	0080 8018h
1Ch	32	DCC2_DCCVALID0	0080 001Ch	0080 401Ch	0080 801Ch
20h	32	DCC2_DCCCNT1	0080 0020h	0080 4020h	0080 8020h
24h	32	DCC2_DCCCLKSRC1	0080 0024h	0080 4024h	0080 8024h
28h	32	DCC2_DCCCLKSRC0	0080 0028h	0080 4028h	0080 8028h
2Ch	32	DCC2_DCCGCTRL2	0080 002Ch	0080 402Ch	0080 802Ch
30h	32	DCC2_DCCSTATUS2	0080 0030h	0080 4030h	0080 8030h
34h	32	DCC2_DCCERRCNT	0080 0034h	0080 4034h	0080 8034h

Table 14-14043. DCC2 Registers, Base Address=0080 0000h, Length=64

Offset	Length	Register Name	DCC3 Physical Address	DCC4 Physical Address	DCC5 Physical Address
0h	32	DCC2_DCCGCTRL	0080 C000h	0081 0000h	0081 4000h
4h	32	DCC2_DCCREV	0080 C004h	0081 0004h	0081 4004h
8h	32	DCC2_DCCCNTSEED0	0080 C008h	0081 0008h	0081 4008h
Ch	32	DCC2_DCCVALIDSEED0	0080 C00Ch	0081 000Ch	0081 400Ch
10h	32	DCC2_DCCCNTSEED1	0080 C010h	0081 0010h	0081 4010h
14h	32	DCC2_DCCSTATUS	0080 C014h	0081 0014h	0081 4014h
18h	32	DCC2_DCCCNT0	0080 C018h	0081 0018h	0081 4018h
1Ch	32	DCC2_DCCVALID0	0080 C01Ch	0081 001Ch	0081 401Ch
20h	32	DCC2_DCCCNT1	0080 C020h	0081 0020h	0081 4020h
24h	32	DCC2_DCCCLKSRC1	0080 C024h	0081 0024h	0081 4024h
28h	32	DCC2_DCCCLKSRC0	0080 C028h	0081 0028h	0081 4028h
2Ch	32	DCC2_DCCGCTRL2	0080 C02Ch	0081 002Ch	0081 402Ch
30h	32	DCC2_DCCSTATUS2	0080 C030h	0081 0030h	0081 4030h
34h	32	DCC2_DCCERRCNT	0080 C034h	0081 0034h	0081 4034h

Table 14-14044. DCC2 Registers, Base Address=0080 0000h, Length=64

Offset	Length	Register Name	DCC6 Physical Address	DCC7 Physical Address	DCC8 Physical Address
0h	32	DCC2_DCCGCTRL	0081 8000h	0081 C000h	0082 0000h
4h	32	DCC2_DCCREV	0081 8004h	0081 C004h	0082 0004h
8h	32	DCC2_DCCCNTSEED0	0081 8008h	0081 C008h	0082 0008h
Ch	32	DCC2_DCCVALIDSEED0	0081 800Ch	0081 C00Ch	0082 000Ch
10h	32	DCC2_DCCCNTSEED1	0081 8010h	0081 C010h	0082 0010h

Table 14-14044. DCC2 Registers, Base Address=0080 0000h, Length=64 (continued)

Offset	Length	Register Name	DCC6 Physical Address	DCC7 Physical Address	DCC8 Physical Address
14h	32	DCC2_DCCSTATUS	0081 8014h	0081 C014h	0082 0014h
18h	32	DCC2_DCCCNT0	0081 8018h	0081 C018h	0082 0018h
1Ch	32	DCC2_DCCVALID0	0081 801Ch	0081 C01Ch	0082 001Ch
20h	32	DCC2_DCCCNT1	0081 8020h	0081 C020h	0082 0020h
24h	32	DCC2_DCCCLKSRC1	0081 8024h	0081 C024h	0082 0024h
28h	32	DCC2_DCCCLKSRC0	0081 8028h	0081 C028h	0082 0028h
2Ch	32	DCC2_DCCGCTRL2	0081 802Ch	0081 C02Ch	0082 002Ch
30h	32	DCC2_DCCSTATUS2	0081 8030h	0081 C030h	0082 0030h
34h	32	DCC2_DCCERRCNT	0081 8034h	0081 C034h	0082 0034h

Table 14-14045. DCC2 Registers, Base Address=0080 0000h, Length=64

Offset	Length	Register Name	MCU_DCC0 Physical Address	MCU_DCC1 Physical Address
0h	32	DCC2_DCCGCTRL	04C0 0000h	04C1 0000h
4h	32	DCC2_DCCREV	04C0 0004h	04C1 0004h
8h	32	DCC2_DCCCNTSEED0	04C0 0008h	04C1 0008h
Ch	32	DCC2_DCCVALIDSEED0	04C0 000Ch	04C1 000Ch
10h	32	DCC2_DCCCNTSEED1	04C0 0010h	04C1 0010h
14h	32	DCC2_DCCSTATUS	04C0 0014h	04C1 0014h
18h	32	DCC2_DCCCNT0	04C0 0018h	04C1 0018h
1Ch	32	DCC2_DCCVALID0	04C0 001Ch	04C1 001Ch
20h	32	DCC2_DCCCNT1	04C0 0020h	04C1 0020h
24h	32	DCC2_DCCCLKSRC1	04C0 0024h	04C1 0024h
28h	32	DCC2_DCCCLKSRC0	04C0 0028h	04C1 0028h
2Ch	32	DCC2_DCCGCTRL2	04C0 002Ch	04C1 002Ch
30h	32	DCC2_DCCSTATUS2	04C0 0030h	04C1 0030h
34h	32	DCC2_DCCERRCNT	04C0 0034h	04C1 0034h

14.7.7.1.2 DCC Registers

DCC Registers

14.7.7.1.2.1 DCC2_DCCGCTRL Register

14.7.7.1.2.1.1 DCC2_DCCGCTRL Register (Offset = 0h) [reset = 5555h]

Starts / stops the counters. Clears the error signal.

Return to Summary Table

Table 14-14046. Instance Table

Instance Name	Physical Address
DCC0	0080 0000h
DCC1	0080 4000h
DCC2	0080 8000h
DCC3	0080 C000h
DCC4	0081 0000h
DCC5	0081 4000h
DCC6	0081 8000h
DCC7	0081 C000h
DCC8	0082 0000h
MCU_DCC0	04C0 0000h
MCU_DCC1	04C1 0000h

Figure 14-6921. DCC2_DCCGCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DONEENA				SINGLESHOT			
R/W				R/W			
5h				5h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERRENA				DCCENA			
R/W				R/W			
5h				5h			

Table 14-14047. DCC2_DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	DONEENA	R/W	5h	The DONEENA bit enables/disables the done interrupt signal, but has no effect on the done status flag in DCCSTAT register. User, privilege, and debug mode (read): 0101 = the done signal is disabled others = the done signal is enabled Privilege and debug mode (write): 0101 = disable done signal generation others = enable done signal generation

Table 14-14047. DCC2_DCCGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	SINGLESHOT	R/W	5h	The SINGLESHOT bit enables/disables repetitive operation of the DCC. User, privilege, and debug mode (read): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error) Privilege and debug mode (write): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error)
7:4	ERRENA	R/W	5h	The ERRENA bit enables/disables the error signal. User, privilege, and debug mode (read): 0101 = the error signal is disabled others = the error signal is enabled Privilege and debug mode (write): 0101 = disable error signal generation others = enable error signal generation
3:0	DCCENA	R/W	5h	The DCCENA bit starts and stops the operation of the dcc. User, privilege, and debug mode (read): 0101 = counters are stopped others = counters are running Privilege and debug mode (write): 0101 = stop counters and error-checking others = load the counters with their seed values and begin counting

14.7.7.1.2.2 DCC2_DCCREV Register

14.7.7.1.2.2.1 DCC2_DCCREV Register (Offset = 4h) [reset = 40010B00h]

Specifies the module version.

Return to Summary Table

Table 14-14048. Instance Table

Instance Name	Physical Address
DCC0	0080 0004h
DCC1	0080 4004h
DCC2	0080 8004h
DCC3	0080 C004h
DCC4	0081 0004h
DCC5	0081 4004h
DCC6	0081 8004h
DCC7	0081 C004h
DCC8	0082 0004h
MCU_DCC0	04C0 0004h
MCU_DCC1	04C1 0004h

Figure 14-6922. DCC2_DCCREV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">RESERVED</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">0h</td><td colspan="4">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">1h</td><td colspan="3">3h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-14049. DCC2_DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	User, privilege, and debug mode (read): Returns 01. Privilege and debug mode (write): Writes have no effect.
29:28	RESERVED	NONE	0h	Reserved
27:16	FUNC	R	1h	Reflects software-compatability. If there is no level of software compatability, a unique func number is assigned; for compatible modules, the same number is maintained. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.

Table 14-14049. DCC2_DCCREV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:11	RTL	R	1h	Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented. User, privilege, and debug mode (read): 0x1 Privilege and debug mode (write): Writes have no effect.
10:8	MAJOR	R	3h	Represents major changes to the module (e.g. entirely new features are added/changed). The major revision number for this module. User, privilege, and debug mode (read): 0x2 Privilege and debug mode (write): Writes have no effect.
7:6	CUSTOM	R	0h	Indicates a special version of the module. May not be supported by standard software. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
5:0	MINOR	R	0h	Represents minor changes to the module (e.g. enhancements to existing features). The minor revision number for this module. User, privilege, and debug mode (read): 0x4 Privilege and debug mode (write): Writes have no effect.

14.7.7.1.2.3 DCC2_DCCCNTSEED0 Register

14.7.7.1.2.3.1 DCC2_DCCCNTSEED0 Register (Offset = 8h) [reset = 0h]

Seed value for the counter attached to clock source 0

Return to Summary Table

Table 14-14050. Instance Table

Instance Name	Physical Address
DCC0	0080 0008h
DCC1	0080 4008h
DCC2	0080 8008h
DCC3	0080 C008h
DCC4	0081 0008h
DCC5	0081 4008h
DCC6	0081 8008h
DCC7	0081 C008h
DCC8	0082 0008h
MCU_DCC0	04C0 0008h
MCU_DCC1	04C1 0008h

Figure 14-6923. DCC2_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				COUNTSEED0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNTSEED0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNTSEED0							
R/W							
0h							

Table 14-14051. DCC2_DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNTSEED0	R/W	0h	This field contains the seed value that gets loaded into counter 0 (clock source 0). User, privilege, and debug mode (read): Returns the current seed value for counter 0. Privilege and debug mode (write): Sets the current seed value for counter 0. NOTE - Operating the DCC with 0 in the COUNTSEED0 register will result in undefined operation. NOTE: Operating the DCC with 0 in the COUNTSEED0 register will result in undefined operation.

14.7.7.1.2.4 DCC2_DCCVALIDSEED0 Register

14.7.7.1.2.4.1 DCC2_DCCVALIDSEED0 Register (Offset = Ch) [reset = 0h]

Seed value for the timeout counter attached to clock source 0.

Return to Summary Table

Table 14-14052. Instance Table

Instance Name	Physical Address
DCC0	0080 000Ch
DCC1	0080 400Ch
DCC2	0080 800Ch
DCC3	0080 C00Ch
DCC4	0081 000Ch
DCC5	0081 400Ch
DCC6	0081 800Ch
DCC7	0081 C00Ch
DCC8	0082 000Ch
MCU_DCC0	04C0 000Ch
MCU_DCC1	04C1 000Ch

Figure 14-6924. DCC2_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VALIDSEED0							
R/W							
0h							
7	6	5	4	3	2	1	0
VALIDSEED0							
R/W							
0h							

Table 14-14053. DCC2_DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved

Table 14-14053. DCC2_DCCVALIDSEED0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	VALIDSEED0	R/W	0h	This field contains the seed value that gets loaded into the valid duration counter for clock source 0. User, privilege, and debug mode (read): Returns the current seed value for VALID0. Privilege and debug mode (write): Sets the current seed value for VALID0. NOTE - Operating the DCC with 0 in the VALIDSEED0 register will result in undefined operation. VALID0 defines a window in which COUNT1 expires. This window is meant to be at least four cycles wide. Do not program a value less than 4 into the VALID0 register. NOTE: Operating the DCC with 0 in the VALIDSEED0 register will result in undefined operation. VALID0 defines a window in which COUNT1 expires. This window is meant to be at least four cycles wide. Do not program a value less than 4 into the VALID0 register.

14.7.7.1.2.5 DCC2_DCCCNTSEED1 Register

14.7.7.1.2.5.1 DCC2_DCCCNTSEED1 Register (Offset = 10h) [reset = 0h]

Seed value for the counter attached to clock source 1.

Return to Summary Table

Table 14-14054. Instance Table

Instance Name	Physical Address
DCC0	0080 0010h
DCC1	0080 4010h
DCC2	0080 8010h
DCC3	0080 C010h
DCC4	0081 0010h
DCC5	0081 4010h
DCC6	0081 8010h
DCC7	0081 C010h
DCC8	0082 0010h
MCU_DCC0	04C0 0010h
MCU_DCC1	04C1 0010h

Figure 14-6925. DCC2_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				COUNTSEED1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
COUNTSEED1							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEED1							
R/W							
0h							

Table 14-14055. DCC2_DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNTSEED1	R/W	0h	This field contains the seed value that gets loaded into counter 1 (clock source 1). User, privilege, and debug mode (read): Returns the current seed value for counter 1. Privilege and debug mode (write): Sets the current seed value for counter 1. NOTE - Operating the DCC with 0 in the COUNTSEED1 register will result in undefined operation. NOTE: Operating the DCC with 0 in the COUNTSEED1 register will result in undefined operation.

14.7.7.1.2.6 DCC2_DCCSTATUS Register

14.7.7.1.2.6.1 DCC2_DCCSTATUS Register (Offset = 14h) [reset = 0h]

Specifies the status of the DCC Module.

Return to Summary Table

Table 14-14056. Instance Table

Instance Name	Physical Address
DCC0	0080 0014h
DCC1	0080 4014h
DCC2	0080 8014h
DCC3	0080 C014h
DCC4	0081 0014h
DCC5	0081 4014h
DCC6	0081 8014h
DCC7	0081 C014h
DCC8	0082 0014h
MCU_DCC0	04C0 0014h
MCU_DCC1	04C1 0014h

Figure 14-6926. DCC2_DCCSTATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>DONEFLG</td><td>ERRFLG</td></tr>
<tr><td colspan="6">NONE</td><td>R/W1TC</td><td>R/W1TC</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14057. DCC2_DCCSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DONEFLG	R/W1TC	0h	Indicates when single-shot mode is complete without error. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = single-shot mode is not done 1 = single-shot mode is done Privilege and debug mode (write): 0 = no effect 1 = clear the done flag

Table 14-14057. DCC2_DCCSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ERRFLG	R/W1TC	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = an error has not occurred 1 = an error has occurred Privilege and debug mode (write): 0 = no effect 1 = clear the error flag

14.7.7.1.2.7 DCC2_DCCCNT0 Register

14.7.7.1.2.7.1 DCC2_DCCCNT0 Register (Offset = 18h) [reset = 0h]

Value of the counter attached to clock source 0.

Return to Summary Table

Table 14-14058. Instance Table

Instance Name	Physical Address
DCC0	0080 0018h
DCC1	0080 4018h
DCC2	0080 8018h
DCC3	0080 C018h
DCC4	0081 0018h
DCC5	0081 4018h
DCC6	0081 8018h
DCC7	0081 C018h
DCC8	0082 0018h
MCU_DCC0	04C0 0018h
MCU_DCC1	04C1 0018h

Figure 14-6927. DCC2_DCCCNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				COUNT0			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
COUNT0							
R							
0h							
7	6	5	4	3	2	1	0
COUNT0							
R							
0h							

Table 14-14059. DCC2_DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNT0	R	0h	This field contains the current value of counter 0. User, privilege, and debug mode (read): Returns the current value for counter 0. Privilege and debug mode (write): Writes have no effect. NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.7.7.1.2.8 DCC2_DCCVALID0 Register

14.7.7.1.2.8.1 DCC2_DCCVALID0 Register (Offset = 1Ch) [reset = 0h]

Value of the valid counter attached to clock source 0.

Return to Summary Table

Table 14-14060. Instance Table

Instance Name	Physical Address
DCC0	0080 001Ch
DCC1	0080 401Ch
DCC2	0080 801Ch
DCC3	0080 C01Ch
DCC4	0081 001Ch
DCC5	0081 401Ch
DCC6	0081 801Ch
DCC7	0081 C01Ch
DCC8	0082 001Ch
MCU_DCC0	04C0 001Ch
MCU_DCC1	04C1 001Ch

Figure 14-6928. DCC2_DCCVALID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VALID0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VALID0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14061. DCC2_DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VALID0	R	0h	This field contains the current value of valid counter 0. User, privilege, and debug mode (read): Returns the current value for valid counter 0. Privilege and debug mode (write): writes have no effect. NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.7.7.1.2.9 DCC2_DCCCNT1 Register

14.7.7.1.2.9.1 DCC2_DCCCNT1 Register (Offset = 20h) [reset = 0h]

Value of the counter attached to clock source 1.

Return to Summary Table

Table 14-14062. Instance Table

Instance Name	Physical Address
DCC0	0080 0020h
DCC1	0080 4020h
DCC2	0080 8020h
DCC3	0080 C020h
DCC4	0081 0020h
DCC5	0081 4020h
DCC6	0081 8020h
DCC7	0081 C020h
DCC8	0082 0020h
MCU_DCC0	04C0 0020h
MCU_DCC1	04C1 0020h

Figure 14-6929. DCC2_DCCCNT1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">COUNT1</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14063. DCC2_DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNT1	R	0h	This field contains the current value of counter 1. User, privilege, and debug mode (read): Returns the current value for counter 1. Privilege and debug mode (write): writes have no effect. NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock. NOTE: Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

14.7.7.1.2.10 DCC2_DCCCLKSRC1 Register

14.7.7.1.2.10.1 DCC2_DCCCLKSRC1 Register (Offset = 24h) [reset = 0h]

Selects the clock source for counter 1.

Return to Summary Table

Table 14-14064. Instance Table

Instance Name	Physical Address
DCC0	0080 0024h
DCC1	0080 4024h
DCC2	0080 8024h
DCC3	0080 C024h
DCC4	0081 0024h
DCC5	0081 4024h
DCC6	0081 8024h
DCC7	0081 C024h
DCC8	0082 0024h
MCU_DCC0	04C0 0024h
MCU_DCC1	04C1 0024h

Figure 14-6930. DCC2_DCCCLKSRC1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
KEY				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED			CLKSRC1				
NONE			R/W				
0h			0h				

Table 14-14065. DCC2_DCCCLKSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 1. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 1. others: Clock source selection is disabled. The secondary oscillator (clock source 1) is selected for counter 1.
11:5	RESERVED	NONE	0h	Reserved

Table 14-14065. DCC2_DCCCLKSRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	CLKSRC1	R/W	0h	This field specifies the clock source for counter 1, when the KEY field enables this feature. User, privilege, and debug mode (read): Returns the current value of CLKSRC. Privilege and debug mode (write): Sets the value of CLKSRC. NOTE: DCC does not generate an error when the clock source is VCLK and VCLK is not present. Note: newer versions of DCC only provide one encoding for VCLK selection (MS encodings are tied off) 0000 Clk source 0 is selected for COUNT1 0001 Clk source 1 is selected for COUNT1 0010 Clk source 2 is selected for COUNT1 0011 Clk source 3 is selected for COUNT1 0100 Clk source 4 is selected for COUNT1 0101 Clk source 5 is selected for COUNT1 0110 Clk source 6 is selected for COUNT1 0111 Clk source 7 is selected for COUNT1 1000-1111 VCLK is selected for COUNT1

14.7.7.1.2.11 DCC2_DCCCLKSRC0 Register

14.7.7.1.2.11.1 DCC2_DCCCLKSRC0 Register (Offset = 28h) [reset = 0h]

Selects the clock source for counter 0.

Return to Summary Table

Table 14-14066. Instance Table

Instance Name	Physical Address
DCC0	0080 0028h
DCC1	0080 4028h
DCC2	0080 8028h
DCC3	0080 C028h
DCC4	0081 0028h
DCC5	0081 4028h
DCC6	0081 8028h
DCC7	0081 C028h
DCC8	0082 0028h
MCU_DCC0	04C0 0028h
MCU_DCC1	04C1 0028h

Figure 14-6931. DCC2_DCCCLKSRC0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY				RESERVED			
R/W				NONE			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLKSRC0			
NONE				R/W			
0h				0h			

Table 14-14067. DCC2_DCCCLKSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 0. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 0. others: Clock source selection is disabled. The external oscillator (XTAL) is selected for counter 0.
11:4	RESERVED	NONE	0h	Reserved

Table 14-14067. DCC2_DCCCLKSRC0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CLKSRC0	R/W	0h	This field specifies the clock source for counter 0. User, privilege, and debug mode (read): Returns the current value of CLKSRC0. Privilege and debug mode (write): Sets the value of CLKSRC0. NOTE: DCC does not generate an error when the clock source is VCLK and VCLK is not present. Note: newer versions of DCC only provide one encoding for VCLK selection (MS encodings are tied off) NOTE: DCC does not generate an error when the clock source is VCLK and VCLK is not present. Note: newer versions of DCC only provide one encoding for VCLK selection (MS encodings are tied off) 0000 Clock0[0] is selected as source for COUNT0 0001 Clock0[1] is selected as source for COUNT0 0010 Clock0[2] is selected as source for COUNT0 Other Values VCLK is selected as source for COUNT0

14.7.7.1.2.12 DCC2_DCCGCTRL2 Register

14.7.7.1.2.12.1 DCC2_DCCGCTRL2 Register (Offset = 2Ch) [reset = 555h]

Allows configuring different modes of operation for DCC.

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Table 14-14068. Instance Table

Instance Name	Physical Address
DCC0	0080 002Ch
DCC1	0080 402Ch
DCC2	0080 802Ch
DCC3	0080 C02Ch
DCC4	0081 002Ch
DCC5	0081 402Ch
DCC6	0081 802Ch
DCC7	0081 C02Ch
DCC8	0082 002Ch
MCU_DCC0	04C0 002Ch
MCU_DCC1	04C1 002Ch

Figure 14-6932. DCC2_DCCGCTRL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">FIFO_NONERR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">5h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">FIFO_READ</td><td colspan="4">CONT_ON_ERR</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">5h</td><td colspan="4">5h</td></tr>
</table>

Table 14-14069. DCC2_DCCGCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved

Table 14-14069. DCC2_DCCGCTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	FIFO_NONERR	R/W	5h	Enables/disables FIFO writes without the error event on completion of comparison window. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter values are captured to non-full FIFO only upon Error event. Others: Write counter values to non-full FIFO upon completion of comparison window regardless of error or not. Note: this setting is applicable only in Continuous mode; in single shot mode FIFO captures counts only on Error. Note: The user should write 1010 to these enable fields to enable each feature to avoid single soft errors.
7:4	FIFO_READ	R/W	5h	Enables the counter read registers reflect FIFO output instead of the live counter value. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter value is read directly. Others: Counters FIFO output is read. Note: The user should write 1010 to these enable fields to enable each feature to avoid single soft errors.
3:0	CONT_ON_ERR	R/W	5h	Continues to next window of comparison despite the error condition. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Enable values: 0101: Comparison and counter reload is stopped from advancing if error is detected. Others: Counters get reloaded with seed and continue counting despite the error condition. Note: The user should write 1010 to these enable fields to enable each feature to avoid single soft errors.

14.7.7.1.2.13 DCC2_DCCSTATUS2 Register

14.7.7.1.2.13.1 DCC2_DCCSTATUS2 Register (Offset = 30h) [reset = 7h]

Specifies the status of the DCC FIFOs.

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Table 14-14070. Instance Table

Instance Name	Physical Address
DCC0	0080 0030h
DCC1	0080 4030h
DCC2	0080 8030h
DCC3	0080 C030h
DCC4	0081 0030h
DCC5	0081 4030h
DCC6	0081 8030h
DCC7	0081 C030h
DCC8	0082 0030h
MCU_DCC0	04C0 0030h
MCU_DCC1	04C1 0030h

Figure 14-6933. DCC2_DCCSTATUS2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		COUNT1_FIFO_FULL	VALID0_FIFO_FULL	COUNT0_FIFO_FULL	COUNT1_FIFO_EMPTY	VALID0_FIFO_EMPTY	COUNT0_FIFO_EMPTY
NONE		R	R	R	R	R	R
0h		0h	0h	0h	1h	1h	1h

Table 14-14071. DCC2_DCCSTATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	COUNT1_FIFO_FULL	R	0h	Count1 FIFO Full. Indicates whether Count1 FIFO is full. User, privilege, and debug mode (read): 0: Count1 FIFO is not full 1: Count1 FIFO is full. Privilege and debug mode (write): Writes have no effect.
4	VALID0_FIFO_FULL	R	0h	Valid0 FIFO Full. Indicates whether Valid0 FIFO is full. User, privilege, and debug mode (read): 0: Valid0 FIFO is not full 1: Valid0 FIFO is full. Privilege and debug mode (write): Writes have no effect.

Table 14-14071. DCC2_DCCSTATUS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	COUNT0_FIFO_FULL	R	0h	Count0 FIFO Full. Indicates whether Count0 FIFO is full. User, privilege, and debug mode (read): 0: Count0 FIFO is not full 1: Count0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
2	COUNT1_FIFO_EMPTY	R	1h	Count1 FIFO Empty. Indicates whether Count1 FIFO is empty. User, privilege, and debug mode (read): 0: Count1 FIFO is not empty 1: Count1 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
1	VALID0_FIFO_EMPTY	R	1h	Valid0 FIFO Empty. Indicates whether Valid0 FIFO is empty. User, privilege, and debug mode (read): 0: Valid0 FIFO is not empty 1: Valid0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
0	COUNT0_FIFO_EMPTY	R	1h	Count0 FIFO Empty. Indicates whether Count0 FIFO is empty. User, privilege, and debug mode (read): 0: Count0 FIFO is not empty 1: Count0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.

14.7.7.1.2.14 DCC2_DCCERRCNT Register

14.7.7.1.2.14.1 DCC2_DCCERRCNT Register (Offset = 34h) [reset = 0h]

Counts number of errors since last clear.

Return to Summary Table

Table 14-14072. Instance Table

Instance Name	Physical Address
DCC0	0080 0034h
DCC1	0080 4034h
DCC2	0080 8034h
DCC3	0080 C034h
DCC4	0081 0034h
DCC5	0081 4034h
DCC6	0081 8034h
DCC7	0081 C034h
DCC8	0082 0034h
MCU_DCC0	04C0 0034h
MCU_DCC1	04C1 0034h

Figure 14-6934. DCC2_DCCERRCNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">ERRCNT</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ERRCNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14073. DCC2_DCCERRCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	ERRCNT	R/W	0h	Counts the number of errors after the last write to this register or reset. If reached terminal count the count freezes. User needs to clear it.

14.7.7.2 ESM

ESM

14.7.7.2.1 ESM Summaries

ESM Summaries

Table 14-14074. ESM Registers, Base Address=0410 0000h, Length=4096

Offset	Length	Register Name	WKUP_ESM0 Physical Address
0h	32	ESM_PID	0410 0000h
4h	32	ESM_INFO	0410 0004h
8h	32	ESM_EN	0410 0008h
Ch	32	ESM_SFT_RST	0410 000Ch
10h	32	ESM_ERR_RAW	0410 0010h
14h	32	ESM_ERR_STS	0410 0014h
18h	32	ESM_ERR_EN_SET	0410 0018h
1Ch	32	ESM_ERR_EN_CLR	0410 001Ch
20h	32	ESM_LOW_PRI	0410 0020h
24h	32	ESM_HI_PRI	0410 0024h
28h	32	ESM_LOW	0410 0028h
2Ch	32	ESM_HI	0410 002Ch
30h	32	ESM_EOI	0410 0030h
40h	32	ESM_PIN_CTRL	0410 0040h
44h	32	ESM_PIN_STS	0410 0044h
48h	32	ESM_PIN_CNTR	0410 0048h
4Ch	32	ESM_PIN_CNTR_PRE	0410 004Ch
50h	32	ESM_PWMH_PIN_CNTR	0410 0050h
54h	32	ESM_PWMH_PIN_CNTR_PRE	0410 0054h
58h	32	ESM_PWML_PIN_CNTR	0410 0058h
5Ch	32	ESM_PWML_PIN_CNTR_PRE	0410 005Ch
400h	32	ESM_ERR_GRP_RAW_J	0410 0400h + formula
404h	32	ESM_ERR_GRP_STS_J	0410 0404h + formula
408h	32	ESM_ERR_GRP_INTR_EN_SET_J	0410 0408h + formula
40Ch	32	ESM_ERR_GRP_INTR_EN_CLR_J	0410 040Ch + formula
410h	32	ESM_ERR_GRP_INT_PRIO_J	0410 0410h + formula
414h	32	ESM_ERR_GRP_PIN_EN_SET_J	0410 0414h + formula
418h	32	ESM_ERR_GRP_PIN_EN_CLR_J	0410 0418h + formula

14.7.7.2.2 ESM Registers

ESM Registers

14.7.7.2.2.1 ESM_PID Register

14.7.7.2.2.1.1 ESM_PID Register (Offset = 0h) [reset = 6FE04900h]

The Revision Register contains the major and minor revisions for the module.

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Table 14-14075. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0000h

Figure 14-6935. ESM_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		FE0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
FE0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
9h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-14076. ESM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: por_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: por_rst_n
27:16	FUNC	R	FE0h	Module ID Reset Source: por_rst_n
15:11	RTL	R	9h	RTL revision. Will vary depending on release. Reset Source: por_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: por_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: por_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: por_rst_n

14.7.7.2.2.2 ESM_INFO Register

14.7.7.2.2.2.1 ESM_INFO Register (Offset = 4h) [reset = 103h]

The Info Register gives the configuration Inforrmation of this ESM.

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Table 14-14077. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0004h

Figure 14-6936. ESM_INFO Name Register

31	30	29	28	27	26	25	24
LAST_RESET	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PULSE_GROUPS							
R							
1h							
7	6	5	4	3	2	1	0
GROUPS							
R							
3h							

Table 14-14078. ESM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	R	0h	Indicates the Source of the last Reset Reset Source: por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	PULSE_GROUPS	R	1h	Number of Pulse Error Groups Reset Source: por_rst_n
7:0	GROUPS	R	3h	Total number of Error Groups Reset Source: por_rst_n

14.7.7.2.2.3 ESM_EN Register

14.7.7.2.2.3.1 ESM_EN Register (Offset = 8h) [reset = 0h]

The Global Enable Register has the initiator interrupt mask

Return to Summary Table

Table 14-14079. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0008h

Figure 14-6937. ESM_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				KEY			
NONE				R/W			
0h				0h			

Table 14-14080. ESM_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	R/W	0h	Global Enable Reset Source: por_rst_n

14.7.7.2.2.4 ESM_SFT_RST Register

14.7.7.2.2.4.1 ESM_SFT_RST Register (Offset = Ch) [reset = 0h]

The Global Soft Reset Register controls the global clear for raw status and enables

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Table 14-14081. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 000Ch

Figure 14-6938. ESM_SFT_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				W			
0h				0h			

Table 14-14082. ESM_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	W	0h	Global Soft Reset Reset Source: por_rst_n

14.7.7.2.2.5 ESM_ERR_RAW Register

14.7.7.2.2.5.1 ESM_ERR_RAW Register (Offset = 10h) [reset = 0h]

Raw Status/Set Register for Configuration Errors

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Table 14-14083. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0010h

Figure 14-6939. ESM_ERR_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					STS		
NONE					R/W1TS		
0h					0h		

Table 14-14084. ESM_ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	STS	R/W1TS	0h	This is the raw status for config errors Reset Source: por_rst_n

14.7.7.2.2.6 ESM_ERR_STS Register

14.7.7.2.2.6.1 ESM_ERR_STS Register (Offset = 14h) [reset = 0h]

Config Error Enable and Clear Register

Return to Summary Table

Table 14-14085. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0014h

Figure 14-6940. ESM_ERR_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSK		
NONE					R/W1TC		
0h					0h		

Table 14-14086. ESM_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSK	R/W1TC	0h	This is the masked status/clear for config errors Reset Source: por_rst_n

14.7.7.2.2.7 ESM_ERR_EN_SET Register

14.7.7.2.2.7.1 ESM_ERR_EN_SET Register (Offset = 18h) [reset = 0h]

Config Error Enable Set Register

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Table 14-14087. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0018h

Figure 14-6941. ESM_ERR_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSK		
NONE					R/W1TS		
0h					0h		

Table 14-14088. ESM_ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSK	R/W1TS	0h	This is the mask enable set for config errors Reset Source: por_rst_n

14.7.7.2.2.8 ESM_ERR_EN_CLR Register

14.7.7.2.2.8.1 ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = 0h]

Config Error Interrupt Enabled Clear register

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Table 14-14089. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 001Ch

Figure 14-6942. ESM_ERR_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSK		
NONE					R/W1TC		
0h					0h		

Table 14-14090. ESM_ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSK	R/W1TC	0h	This is the mask enable clear for config errors Reset Source: por_rst_n

14.7.7.2.2.9 ESM_LOW_PRI Register

14.7.7.2.2.9.1 ESM_LOW_PRI Register (Offset = 20h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding low priority interrupt

Return to Summary Table

Table 14-14091. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0020h

Figure 14-6943. ESM_LOW_PRI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PLS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PLS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LVL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LVL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-14092. ESM_LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding low priority pulse interrupt Reset Source: por_rst_n
15:0	LVL	R	FFFFh	This is the highest priority outstanding low priority level interrupt Reset Source: por_rst_n

14.7.7.2.2.10 ESM_HI_PRI Register

14.7.7.2.2.10.1 ESM_HI_PRI Register (Offset = 24h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding high priority interrupt

Return to Summary Table

Table 14-14093. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0024h

Figure 14-6944. ESM_HI_PRI Name Register

31	30	29	28	27	26	25	24
PLS							
R							
FFFFh							
23	22	21	20	19	18	17	16
PLS							
R							
FFFFh							
15	14	13	12	11	10	9	8
LVL							
R							
FFFFh							
7	6	5	4	3	2	1	0
LVL							
R							
FFFFh							

Table 14-14094. ESM_HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding high priority pulse interrupt Reset Source: por_rst_n
15:0	LVL	R	FFFFh	This is the highest priority outstanding high priority level interrupt Reset Source: por_rst_n

14.7.7.2.2.11 ESM_LOW Register

14.7.7.2.2.11.1 ESM_LOW Register (Offset = 28h) [reset = 0h]

Shows which groups have oustanding low priority interrupts

Return to Summary Table

Table 14-14095. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0028h

Figure 14-6945. ESM_LOW Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 14-14096. ESM_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors Reset Source: por_rst_n

14.7.7.2.2.12 ESM_HI Register

14.7.7.2.2.12.1 ESM_HI Register (Offset = 2Ch) [reset = 0h]

Shows which groups have oustanding high priority interrupts

Return to Summary Table

Table 14-14097. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 002Ch

Figure 14-6946. ESM_HI Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 14-14098. ESM_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors Reset Source: por_rst_n

14.7.7.2.2.13 ESM_EOI Register

14.7.7.2.2.13.1 ESM_EOI Register (Offset = 30h) [reset = 0h]

End of Interrupt Register

Return to Summary Table

Table 14-14099. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0030h

Figure 14-6947. ESM_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					KEY		
NONE					W		
0h					0h		
7	6	5	4	3	2	1	0
KEY							
W							
0h							

Table 14-14100. ESM_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	KEY	W	0h	This is the interrupt being serviced Reset Source: por_rst_n

14.7.7.2.2.14 ESM_PIN_CTRL Register

14.7.7.2.2.14.1 ESM_PIN_CTRL Register (Offset = 40h) [reset = 0h]

This register controls the error_pin_n output

Return to Summary Table

Table 14-14101. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0040h

Figure 14-6948. ESM_PIN_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWM_EN</td><td colspan="4">KEY</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14102. ESM_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	PWM_EN	R/W	0h	PWM enable Reset Source: por_rst_n
3:0	KEY	R/W	0h	Pin Control Key Reset Source: por_rst_n

14.7.7.2.2.15 ESM_PIN_STS Register

14.7.7.2.2.15.1 ESM_PIN_STS Register (Offset = 44h) [reset = 0h]

This register reflects the status of the error_pin_n output

Return to Summary Table

Table 14-14103. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0044h

Figure 14-6949. ESM_PIN_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							VAL
NONE							R
0h							0h

Table 14-14104. ESM_PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	VAL	R	0h	Value of the error_pin_n Reset Source: por_rst_n

14.7.7.2.2.16 ESM_PIN_CNTR Register

14.7.7.2.2.16.1 ESM_PIN_CNTR Register (Offset = 48h) [reset = 0h]

This register shows the current value of the error pin counter

Return to Summary Table

Table 14-14105. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0048h

Figure 14-6950. ESM_PIN_CNTR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14106. ESM_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.7.7.2.2.17 ESM_PIN_CNTR_PRE Register

14.7.7.2.2.17.1 ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = 0h]

This register contains the value that is loaded in to the Error Counter

Return to Summary Table

Table 14-14107. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 004Ch

Figure 14-6951. ESM_PIN_CNTR_PRE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14108. ESM_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.7.7.2.2.18 ESM_PWMH_PIN_CNTR Register

14.7.7.2.2.18.1 ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = 0h]

This register shows the current value of the error pin PWM high counter

Return to Summary Table

Table 14-14109. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0050h

Figure 14-6952. ESM_PWMH_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-14110. ESM_PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.7.7.2.2.19 ESM_PWMH_PIN_CNTR_PRE Register

14.7.7.2.2.19.1 ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = 0h]

This register contains the value that is loaded in to the Error PWM High Counter

Return to Summary Table

Table 14-14111. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0054h

Figure 14-6953. ESM_PWMH_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-14112. ESM_PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.7.7.2.2.20 ESM_PWML_PIN_CNTR Register

14.7.7.2.2.20.1 ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = 0h]

This register shows the current value of the error pin PWM low counter

Return to Summary Table

Table 14-14113. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0058h

Figure 14-6954. ESM_PWML_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-14114. ESM_PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.7.7.2.2.21 ESM_PWML_PIN_CNTR_PRE Register

14.7.7.2.2.21.1 ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = 0h]

This register contains the value that is loaded in to the Error PWM Low Counter

Return to Summary Table

Table 14-14115. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 005Ch

Figure 14-6955. ESM_PWML_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-14116. ESM_PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.7.7.2.2.22 ESM_ERR_GRP_RAW_J Register

14.7.7.2.2.22.1 ESM_ERR_GRP_RAW_J Register (Offset = 400h) [reset = 0h]

Raw Status/Set Register for Group A Errors

Return to Summary Table

Table 14-14117. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0400h + formula

Figure 14-6956. ESM_ERR_GRP_RAW_j Name Register

31	30	29	28	27	26	25	24
STS							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
STS							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
STS							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
STS							
R/W1TS							
0h							

Table 14-14118. ESM_ERR_GRP_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R/W1TS	0h	This is the raw status/set for errors Group A Reset Source: por_rst_n

14.7.7.2.2.23 ESM_ERR_GRP_STS_J Register

14.7.7.2.2.23.1 ESM_ERR_GRP_STS_J Register (Offset = 404h) [reset = 0h]

Error Enable and Clear Register

Return to Summary Table

Table 14-14119. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0404h + formula

Figure 14-6957. ESM_ERR_GRP_STS_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-14120. ESM_ERR_GRP_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the masked status/clear for errors in Group A Reset Source: por_rst_n

14.7.7.2.2.24 ESM_ERR_GRP_INTR_EN_SET_J Register

14.7.7.2.2.24.1 ESM_ERR_GRP_INTR_EN_SET_J Register (Offset = 408h) [reset = 0h]

Level Error Enable Set Register

Return to Summary Table

Table 14-14121. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0408h + formula

Figure 14-6958. ESM_ERR_GRP_INTR_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 14-14122. ESM_ERR_GRP_INTR_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the mask enable set for errors in Group A Reset Source: por_rst_n

14.7.7.2.2.25 ESM_ERR_GRP_INTR_EN_CLR_J Register

14.7.7.2.2.25.1 ESM_ERR_GRP_INTR_EN_CLR_J Register (Offset = 40Ch) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-14123. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 040Ch + formula

Figure 14-6959. ESM_ERR_GRP_INTR_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-14124. ESM_ERR_GRP_INTR_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the mask enable clear for errors in Group A Reset Source: por_rst_n

14.7.7.2.2.26 ESM_ERR_GRP_INT_PRIO_J Register

14.7.7.2.2.26.1 ESM_ERR_GRP_INT_PRIO_J Register (Offset = 410h) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-14125. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0410h + formula

Figure 14-6960. ESM_ERR_GRP_INT_PRIO_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W							
0h							

Table 14-14126. ESM_ERR_GRP_INT_PRIO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W	0h	This is interrupt priority for errors in Group A Reset Source: por_rst_n

14.7.7.2.2.27 ESM_ERR_GRP_PIN_EN_SET_J Register

14.7.7.2.2.27.1 ESM_ERR_GRP_PIN_EN_SET_J Register (Offset = 414h) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-14127. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0414h + formula

Figure 14-6961. ESM_ERR_GRP_PIN_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 14-14128. ESM_ERR_GRP_PIN_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the error pin influence enable set for errors in Group A Reset Source: por_rst_n

14.7.7.2.2.28 ESM_ERR_GRP_PIN_EN_CLR_J Register

14.7.7.2.2.28.1 ESM_ERR_GRP_PIN_EN_CLR_J Register (Offset = 418h) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-14129. Instance Table

Instance Name	Physical Address
WKUP_ESM0	0410 0418h + formula

Figure 14-6962. ESM_ERR_GRP_PIN_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-14130. ESM_ERR_GRP_PIN_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the error pin influence enable clear for errors in Group A Reset Source: por_rst_n

14.7.7.3 ESM

ESM

14.7.7.3.1 ESM Summaries

ESM Summaries

Table 14-14131. ESM Registers, Base Address=0042 0000h, Length=4096

Offset	Length	Register Name	ESM0 Physical Address
0h	32	ESM_PID	0042 0000h
4h	32	ESM_INFO	0042 0004h
8h	32	ESM_EN	0042 0008h
Ch	32	ESM_SFT_RST	0042 000Ch
10h	32	ESM_ERR_RAW	0042 0010h
14h	32	ESM_ERR_STS	0042 0014h
18h	32	ESM_ERR_EN_SET	0042 0018h
1Ch	32	ESM_ERR_EN_CLR	0042 001Ch
20h	32	ESM_LOW_PRI	0042 0020h
24h	32	ESM_HI_PRI	0042 0024h
28h	32	ESM_LOW	0042 0028h
2Ch	32	ESM_HI	0042 002Ch
30h	32	ESM_EOI	0042 0030h
40h	32	ESM_PIN_CTRL	0042 0040h
44h	32	ESM_PIN_STS	0042 0044h
48h	32	ESM_PIN_CNTR	0042 0048h
4Ch	32	ESM_PIN_CNTR_PRE	0042 004Ch
50h	32	ESM_PWMH_PIN_CNTR	0042 0050h
54h	32	ESM_PWMH_PIN_CNTR_PRE	0042 0054h
58h	32	ESM_PWML_PIN_CNTR	0042 0058h
5Ch	32	ESM_PWML_PIN_CNTR_PRE	0042 005Ch
400h	32	ESM_ERR_GRP_RAW_J	0042 0400h + formula
404h	32	ESM_ERR_GRP_STS_J	0042 0404h + formula
408h	32	ESM_ERR_GRP_INTR_EN_SET_J	0042 0408h + formula
40Ch	32	ESM_ERR_GRP_INTR_EN_CLR_J	0042 040Ch + formula
410h	32	ESM_ERR_GRP_INT_PRIO_J	0042 0410h + formula
414h	32	ESM_ERR_GRP_PIN_EN_SET_J	0042 0414h + formula
418h	32	ESM_ERR_GRP_PIN_EN_CLR_J	0042 0418h + formula

14.7.7.3.2 ESM Registers

ESM Registers

14.7.7.3.2.1 ESM_PID Register

14.7.7.3.2.1.1 ESM_PID Register (Offset = 0h) [reset = 6FE04900h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 14-14132. Instance Table

Instance Name	Physical Address
ESM0	0042 0000h

Figure 14-6963. ESM_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">FE0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FE0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">9h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-14133. ESM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: por_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: por_rst_n
27:16	FUNC	R	FE0h	Module ID Reset Source: por_rst_n
15:11	RTL	R	9h	RTL revision. Will vary depending on release. Reset Source: por_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: por_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: por_rst_n
5:0	MINOR	R	0h	Minor revision Reset Source: por_rst_n

14.7.7.3.2.2 ESM_INFO Register

14.7.7.3.2.2.1 ESM_INFO Register (Offset = 4h) [reset = 108h]

The Info Register gives the configuration Inforrmation of this ESM.

Return to Summary Table

Table 14-14134. Instance Table

Instance Name	Physical Address
ESM0	0042 0004h

Figure 14-6964. ESM_INFO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>LAST_RESET</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PULSE_GROUPS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GROUPS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">8h</td></tr>
</table>

Table 14-14135. ESM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	R	0h	Indicates the Source of the last Reset Reset Source: por_rst_n
30:16	RESERVED	NONE	0h	Reserved
15:8	PULSE_GROUPS	R	1h	Number of Pulse Error Groups Reset Source: por_rst_n
7:0	GROUPS	R	8h	Total number of Error Groups Reset Source: por_rst_n

14.7.7.3.2.3 ESM_EN Register

14.7.7.3.2.3.1 ESM_EN Register (Offset = 8h) [reset = 0h]

The Global Enable Register has the initiator interrupt mask

Return to Summary Table

Table 14-14136. Instance Table

Instance Name	Physical Address
ESM0	0042 0008h

Figure 14-6965. ESM_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				R/W			
0h				0h			

Table 14-14137. ESM_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	R/W	0h	Global Enable Reset Source: por_rst_n

14.7.7.3.2.4 ESM_SFT_RST Register

14.7.7.3.2.4.1 ESM_SFT_RST Register (Offset = Ch) [reset = 0h]

The Global Soft Reset Register controls the global clear for raw status and enables

Return to Summary Table

Table 14-14138. Instance Table

Instance Name	Physical Address
ESM0	0042 000Ch

Figure 14-6966. ESM_SFT_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				W			
0h				0h			

Table 14-14139. ESM_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	W	0h	Global Soft Reset Reset Source: por_rst_n

14.7.7.3.2.5 ESM_ERR_RAW Register

14.7.7.3.2.5.1 ESM_ERR_RAW Register (Offset = 10h) [reset = 0h]

Raw Status/Set Register for Configuration Errors

Return to Summary Table

Table 14-14140. Instance Table

Instance Name	Physical Address
ESM0	0042 0010h

Figure 14-6967. ESM_ERR_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
STS							
R/W1TS							
0h							

Table 14-14141. ESM_ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	STS	R/W1TS	0h	This is the raw status for config errors Reset Source: por_rst_n

14.7.7.3.2.6 ESM_ERR_STS Register

14.7.7.3.2.6.1 ESM_ERR_STS Register (Offset = 14h) [reset = 0h]

Config Error Enable and Clear Register

Return to Summary Table

Table 14-14142. Instance Table

Instance Name	Physical Address
ESM0	0042 0014h

Figure 14-6968. ESM_ERR_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-14143. ESM_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MSK	R/W1TC	0h	This is the masked status/clear for config errors Reset Source: por_rst_n

14.7.7.3.2.7 ESM_ERR_EN_SET Register

14.7.7.3.2.7.1 ESM_ERR_EN_SET Register (Offset = 18h) [reset = 0h]

Config Error Enable Set Register

Return to Summary Table

Table 14-14144. Instance Table

Instance Name	Physical Address
ESM0	0042 0018h

Figure 14-6969. ESM_ERR_EN_SET Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MSK</td></tr>
<tr><td colspan="8">R/W1TS</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14145. ESM_ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MSK	R/W1TS	0h	This is the mask enable set for config errors Reset Source: por_rst_n

14.7.7.3.2.8 ESM_ERR_EN_CLR Register

14.7.7.3.2.8.1 ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = 0h]

Config Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-14146. Instance Table

Instance Name	Physical Address
ESM0	0042 001Ch

Figure 14-6970. ESM_ERR_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-14147. ESM_ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MSK	R/W1TC	0h	This is the mask enable clear for config errors Reset Source: por_rst_n

14.7.7.3.2.9 ESM_LOW_PRI Register

14.7.7.3.2.9.1 ESM_LOW_PRI Register (Offset = 20h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding low priority interrupt

Return to Summary Table

Table 14-14148. Instance Table

Instance Name	Physical Address
ESM0	0042 0020h

Figure 14-6971. ESM_LOW_PRI Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PLS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PLS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LVL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LVL</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">FFFFh</td></tr>
</table>

Table 14-14149. ESM_LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding low priority pulse interrupt Reset Source: por_rst_n
15:0	LVL	R	FFFFh	This is the highest priority outstanding low priority level interrupt Reset Source: por_rst_n

14.7.7.3.2.10 ESM_HI_PRI Register

14.7.7.3.2.10.1 ESM_HI_PRI Register (Offset = 24h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding high priority interrupt

Return to Summary Table

Table 14-14150. Instance Table

Instance Name	Physical Address
ESM0	0042 0024h

Figure 14-6972. ESM_HI_PRI Name Register

31	30	29	28	27	26	25	24
PLS							
R							
FFFFh							
23	22	21	20	19	18	17	16
PLS							
R							
FFFFh							
15	14	13	12	11	10	9	8
LVL							
R							
FFFFh							
7	6	5	4	3	2	1	0
LVL							
R							
FFFFh							

Table 14-14151. ESM_HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding high priority pulse interrupt Reset Source: por_rst_n
15:0	LVL	R	FFFFh	This is the highest priority outstanding high priority level interrupt Reset Source: por_rst_n

14.7.7.3.2.11 ESM_LOW Register

14.7.7.3.2.11.1 ESM_LOW Register (Offset = 28h) [reset = 0h]

Shows which groups have oustanding low priority interrupts

Return to Summary Table

Table 14-14152. Instance Table

Instance Name	Physical Address
ESM0	0042 0028h

Figure 14-6973. ESM_LOW Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 14-14153. ESM_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors Reset Source: por_rst_n

14.7.7.3.2.12 ESM_HI Register

14.7.7.3.2.12.1 ESM_HI Register (Offset = 2Ch) [reset = 0h]

Shows which groups have oustanding high priority interrupts

Return to Summary Table

Table 14-14154. Instance Table

Instance Name	Physical Address
ESM0	0042 002Ch

Figure 14-6974. ESM_HI Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 14-14155. ESM_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors Reset Source: por_rst_n

14.7.7.3.2.13 ESM_EOI Register

14.7.7.3.2.13.1 ESM_EOI Register (Offset = 30h) [reset = 0h]

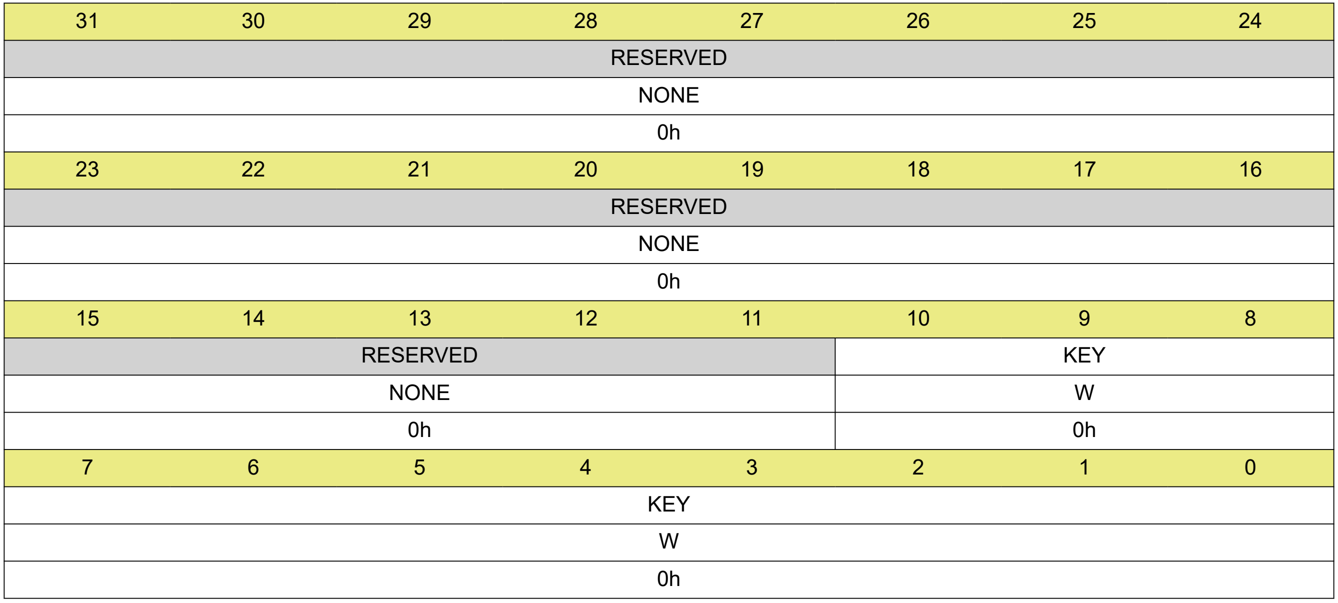
End of Interrupt Register

Return to Summary Table

Table 14-14156. Instance Table

Instance Name	Physical Address
ESM0	0042 0030h

Figure 14-6975. ESM_EOI Name Register



<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">KEY</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">KEY</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14157. ESM_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	KEY	W	0h	This is the interrupt being serviced Reset Source: por_rst_n

14.7.7.3.2.14 ESM_PIN_CTRL Register

14.7.7.3.2.14.1 ESM_PIN_CTRL Register (Offset = 40h) [reset = 0h]

This register controls the error_pin_n output

Return to Summary Table

Table 14-14158. Instance Table

Instance Name	Physical Address
ESM0	0042 0040h

Figure 14-6976. ESM_PIN_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PWM_EN				KEY			
R/W				R/W			
0h				0h			

Table 14-14159. ESM_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	PWM_EN	R/W	0h	PWM enable Reset Source: por_rst_n
3:0	KEY	R/W	0h	Pin Control Key Reset Source: por_rst_n

14.7.7.3.2.15 ESM_PIN_STS Register

14.7.7.3.2.15.1 ESM_PIN_STS Register (Offset = 44h) [reset = 0h]

This register reflects the status of the error_pin_n output

Return to Summary Table

Table 14-14160. Instance Table

Instance Name	Physical Address
ESM0	0042 0044h

Figure 14-6977. ESM_PIN_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							VAL
NONE							R
0h							0h

Table 14-14161. ESM_PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	VAL	R	0h	Value of the error_pin_n Reset Source: por_rst_n

14.7.7.3.2.16 ESM_PIN_CNTR Register

14.7.7.3.2.16.1 ESM_PIN_CNTR Register (Offset = 48h) [reset = 0h]

This register shows the current value of the error pin counter

Return to Summary Table

Table 14-14162. Instance Table

Instance Name	Physical Address
ESM0	0042 0048h

Figure 14-6978. ESM_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-14163. ESM_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.7.7.3.2.17 ESM_PIN_CNTR_PRE Register

14.7.7.3.2.17.1 ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = 0h]

This register contains the value that is loaded in to the Error Counter

Return to Summary Table

Table 14-14164. Instance Table

Instance Name	Physical Address
ESM0	0042 004Ch

Figure 14-6979. ESM_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-14165. ESM_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.7.7.3.2.18 ESM_PWMH_PIN_CNTR Register

14.7.7.3.2.18.1 ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = 0h]

This register shows the current value of the error pin PWM high counter

Return to Summary Table

Table 14-14166. Instance Table

Instance Name	Physical Address
ESM0	0042 0050h

Figure 14-6980. ESM_PWMH_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-14167. ESM_PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.7.7.3.2.19 ESM_PWMH_PIN_CNTR_PRE Register

14.7.7.3.2.19.1 ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = 0h]

This register contains the value that is loaded in to the Error PWM High Counter

Return to Summary Table

Table 14-14168. Instance Table

Instance Name	Physical Address
ESM0	0042 0054h

Figure 14-6981. ESM_PWMH_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-14169. ESM_PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.7.7.3.2.20 ESM_PWML_PIN_CNTR Register

14.7.7.3.2.20.1 ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = 0h]

This register shows the current value of the error pin PWM low counter

Return to Summary Table

Table 14-14170. Instance Table

Instance Name	Physical Address
ESM0	0042 0058h

Figure 14-6982. ESM_PWML_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 14-14171. ESM_PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value Reset Source: por_rst_n

14.7.7.3.2.21 ESM_PWML_PIN_CNTR_PRE Register

14.7.7.3.2.21.1 ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = 0h]

This register contains the value that is loaded in to the Error PWM Low Counter

Return to Summary Table

Table 14-14172. Instance Table

Instance Name	Physical Address
ESM0	0042 005Ch

Figure 14-6983. ESM_PWML_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 14-14173. ESM_PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value Reset Source: por_rst_n

14.7.7.3.2.22 ESM_ERR_GRP_RAW_J Register

14.7.7.3.2.22.1 ESM_ERR_GRP_RAW_J Register (Offset = 400h) [reset = 0h]

Raw Status/Set Register for Group A Errors

Return to Summary Table

Table 14-14174. Instance Table

Instance Name	Physical Address
ESM0	0042 0400h + formula

Figure 14-6984. ESM_ERR_GRP_RAW_j Name Register

31	30	29	28	27	26	25	24
STS							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
STS							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
STS							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
STS							
R/W1TS							
0h							

Table 14-14175. ESM_ERR_GRP_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R/W1TS	0h	This is the raw status/set for errors Group A Reset Source: por_rst_n

14.7.7.3.2.23 ESM_ERR_GRP_STS_J Register

14.7.7.3.2.23.1 ESM_ERR_GRP_STS_J Register (Offset = 404h) [reset = 0h]

Error Enable and Clear Register

Return to Summary Table

Table 14-14176. Instance Table

Instance Name	Physical Address
ESM0	0042 0404h + formula

Figure 14-6985. ESM_ERR_GRP_STS_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-14177. ESM_ERR_GRP_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the masked status/clear for errors in Group A Reset Source: por_rst_n

14.7.7.3.2.24 ESM_ERR_GRP_INTR_EN_SET_J Register

14.7.7.3.2.24.1 ESM_ERR_GRP_INTR_EN_SET_J Register (Offset = 408h) [reset = 0h]

Level Error Enable Set Register

Return to Summary Table

Table 14-14178. Instance Table

Instance Name	Physical Address
ESM0	0042 0408h + formula

Figure 14-6986. ESM_ERR_GRP_INTR_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 14-14179. ESM_ERR_GRP_INTR_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the mask enable set for errors in Group A Reset Source: por_rst_n

14.7.7.3.2.25 ESM_ERR_GRP_INTR_EN_CLR_J Register

14.7.7.3.2.25.1 ESM_ERR_GRP_INTR_EN_CLR_J Register (Offset = 40Ch) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-14180. Instance Table

Instance Name	Physical Address
ESM0	0042 040Ch + formula

Figure 14-6987. ESM_ERR_GRP_INTR_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-14181. ESM_ERR_GRP_INTR_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the mask enable clear for errors in Group A Reset Source: por_rst_n

14.7.7.3.2.26 ESM_ERR_GRP_INT_PRIO_J Register

14.7.7.3.2.26.1 ESM_ERR_GRP_INT_PRIO_J Register (Offset = 410h) [reset = 0h]

Level Error Interrupt Enabled Clear register

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Table 14-14182. Instance Table

Instance Name	Physical Address
ESM0	0042 0410h + formula

Figure 14-6988. ESM_ERR_GRP_INT_PRIO_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W							
0h							

Table 14-14183. ESM_ERR_GRP_INT_PRIO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W	0h	This is interrupt priority for errors in Group A Reset Source: por_rst_n

14.7.7.3.2.27 ESM_ERR_GRP_PIN_EN_SET_J Register

14.7.7.3.2.27.1 ESM_ERR_GRP_PIN_EN_SET_J Register (Offset = 414h) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-14184. Instance Table

Instance Name	Physical Address
ESM0	0042 0414h + formula

Figure 14-6989. ESM_ERR_GRP_PIN_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 14-14185. ESM_ERR_GRP_PIN_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the error pin influence enable set for errors in Group A Reset Source: por_rst_n

14.7.7.3.2.28 ESM_ERR_GRP_PIN_EN_CLR_J Register

14.7.7.3.2.28.1 ESM_ERR_GRP_PIN_EN_CLR_J Register (Offset = 418h) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Table 14-14186. Instance Table

Instance Name	Physical Address
ESM0	0042 0418h + formula

Figure 14-6990. ESM_ERR_GRP_PIN_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 14-14187. ESM_ERR_GRP_PIN_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the error pin influence enable clear for errors in Group A Reset Source: por_rst_n

14.7.7.4 MCRC64

MCRC64

14.7.7.4.1 MCRC64 Summaries

MCRC64 Summaries

Table 14-14188. CRC Registers, Base Address=3030 0000h, Length=4096

Offset	Length	Register Name	MCRC64_0 Physical Address
0h	32	CRC_CTRL0	3030 0000h + formula
8h	32	CRC_CTRL1	3030 0008h + formula
10h	32	CRC_CTRL2	3030 0010h + formula
18h	32	CRC_INTS	3030 0018h + formula
20h	32	CRC_INTR	3030 0020h + formula
28h	32	CRC_STATUS	3030 0028h + formula
30h	32	CRC_INT_OFFSET_REG	3030 0030h + formula
38h	32	CRC_BUSY	3030 0038h + formula
40h	32	CRC_PCOUNT_REG1	3030 0040h + formula
44h	32	CRC_SCOUNT_REG1	3030 0044h + formula
48h	32	CRC_CURSEC_REG1	3030 0048h + formula
4Ch	32	CRC_WDTOPLD1	3030 004Ch + formula
50h	32	CRC_BCTOPLD1	3030 0050h + formula
60h	32	CRC_PSA_SIGREGL1	3030 0060h + formula
64h	32	CRC_PSA_SIGREGH1	3030 0064h + formula
68h	32	CRC_REGL1	3030 0068h + formula
6Ch	32	CRC_REGH1	3030 006Ch + formula
70h	32	CRC_PSA_SECSIGREGL1	3030 0070h + formula
74h	32	CRC_PSA_SECSIGREGH1	3030 0074h + formula
78h	32	CRC_RAW_DATAREGL1	3030 0078h + formula
7Ch	32	CRC_RAW_DATAREGH1	3030 007Ch + formula
80h	32	CRC_PCOUNT_REG2	3030 0080h + formula
84h	32	CRC_SCOUNT_REG2	3030 0084h + formula
88h	32	CRC_CURSEC_REG2	3030 0088h + formula
8Ch	32	CRC_WDTOPLD2	3030 008Ch + formula
90h	32	CRC_BCTOPLD2	3030 0090h + formula
A0h	32	CRC_PSA_SIGREGL2	3030 00A0h + formula
A4h	32	CRC_PSA_SIGREGH2	3030 00A4h + formula
A8h	32	CRC_REGL2	3030 00A8h + formula
ACh	32	CRC_REGH2	3030 00ACh + formula
B0h	32	CRC_PSA_SECSIGREGL2	3030 00B0h + formula
B4h	32	CRC_PSA_SECSIGREGH2	3030 00B4h + formula
B8h	32	CRC_RAW_DATAREGL2	3030 00B8h + formula
BCh	32	CRC_RAW_DATAREGH2	3030 00BCh + formula
C0h	32	CRC_PCOUNT_REG3	3030 00C0h + formula
C4h	32	CRC_SCOUNT_REG3	3030 00C4h + formula
C8h	32	CRC_CURSEC_REG3	3030 00C8h + formula
CCh	32	CRC_WDTOPLD3	3030 00CCh + formula
D0h	32	CRC_BCTOPLD3	3030 00D0h + formula
E0h	32	CRC_PSA_SIGREGL3	3030 00E0h + formula

Table 14-14188. CRC Registers, Base Address=3030 0000h, Length=4096 (continued)

Offset	Length	Register Name	MCRC64_0 Physical Address
E4h	32	CRC_PSA_SIGREGH3	3030 00E4h + formula
E8h	32	CRC_REGL3	3030 00E8h + formula
ECh	32	CRC_REGH3	3030 00ECh + formula
F0h	32	CRC_PSA_SECSIGREGL3	3030 00F0h + formula
F4h	32	CRC_PSA_SECSIGREGH3	3030 00F4h + formula
F8h	32	CRC_RAW_DATAREGL3	3030 00F8h + formula
FCh	32	CRC_RAW_DATAREGH3	3030 00FCh + formula
100h	32	CRC_PCOUNT_REG4	3030 0100h + formula
104h	32	CRC_SCOUNT_REG4	3030 0104h + formula
108h	32	CRC_CURSEC_REG4	3030 0108h + formula
10Ch	32	CRC_WDTOPLD4	3030 010Ch + formula
110h	32	CRC_BCTOPLD4	3030 0110h + formula
120h	32	CRC_PSA_SIGREGL4	3030 0120h + formula
124h	32	CRC_PSA_SIGREGH4	3030 0124h + formula
128h	32	CRC_REGL4	3030 0128h + formula
12Ch	32	CRC_REGH4	3030 012Ch + formula
130h	32	CRC_PSA_SECSIGREGL4	3030 0130h + formula
134h	32	CRC_PSA_SECSIGREGH4	3030 0134h + formula
138h	32	CRC_RAW_DATAREGL4	3030 0138h + formula
13Ch	32	CRC_RAW_DATAREGH4	3030 013Ch + formula
140h	32	CRC_MBUS_SEL	3030 0140h + formula
200h	32	CRC_I0_PSA_SIGREG1_CPY_J	3030 0200h + formula
280h	32	CRC_I0_PSA_SIGREG2_CPY_J	3030 0280h + formula
300h	32	CRC_I0_PSA_SIGREG3_CPY_J	3030 0300h + formula
380h	32	CRC_I0_PSA_SIGREG4_CPY_J	3030 0380h + formula

14.7.7.4.2 MCRC64 Registers

MCRC64 Registers

14.7.7.4.2.1 CRC_CTRL0 Register

14.7.7.4.2.1.1 CRC_CTRL0 Register (Offset = 0h) [reset = 0h]

CRC Global Control Register 0

Return to Summary Table

Table 14-14189. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0000h + formula

Figure 14-6991. CRC_CTRL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							CH4_PSA_SWRE
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CH3_PSA_SWRE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CH2_PSA_SWRE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CH1_PSA_SWRE
NONE							R/W
0h							0h

Table 14-14190. CRC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CH4_PSA_SWRE	R/W	0h	Channel 4 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
23:17	RESERVED	NONE	0h	Reserved
16	CH3_PSA_SWRE	R/W	0h	Channel 3 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
15:9	RESERVED	NONE	0h	Reserved
8	CH2_PSA_SWRE	R/W	0h	Channel 2 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
7:1	RESERVED	NONE	0h	Reserved

Table 14-14190. CRC_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_PSA_SWRE	R/W	0h	Channel 1 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset

14.7.7.4.2.2 CRC_CTRL1 Register

14.7.7.4.2.2.1 CRC_CTRL1 Register (Offset = 8h) [reset = 0h]

CRC Global Control Register 1

Return to Summary Table

Table 14-14191. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0008h + formula

Figure 14-6992. CRC_CTRL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PWDN</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14192. CRC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PWDN	R/W	0h	Power Down. When set, MCRC moduleMCRC Module is put in power down mode. 0 = MCRC is not in power down mode. 1 = MCRC is in power down mode.

14.7.7.4.2.3 CRC_CTRL2 Register

14.7.7.4.2.3.1 CRC_CTRL2 Register (Offset = 10h) [reset = 0h]

Data capture mode is especially useful when it is used in conjunction when data trace (CH1_TRACEEN) for channel 1. The seed value can be planted in PSA Signature Register during data capture mode by writing a seed value into PSA Signature Register. Data trace enable bit is then set to snoop and compress any read transaction on Data buses. When trace enable bit is set, CH1_MODE is automatically reset to data capture mode. To change mode from one to another in the middle of an on-going mode user should take the following steps:

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Table 14-14193. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0010h + formula

Figure 14-6993. CRC_CTRL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CH4_MODE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CH3_MODE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">CH2_MODE</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>CH1_TRACEEN</td><td colspan="2">RESERVED</td><td colspan="2">CH1_MODE</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="2">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
</table>

Table 14-14194. CRC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:24	CH4_MODE	R/W	0h	Channel 4 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode For all four channels the seed value can be first planted into PSA register before the Channel Mode is switched to Full-CPU mode since host CPU controls the amount of data for compression. During AUTO mode, the PSA register is automatically reset to zero at the end of each sector compression.
23:18	RESERVED	NONE	0h	Reserved

Table 14-14194. CRC_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	CH3_MODE	R/W	0h	Channel 3 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode
15:10	RESERVED	NONE	0h	Reserved
9:8	CH2_MODE	R/W	0h	Channel 2 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TRACEEN	R/W	0h	Channel 1 Data Trace Enable When set, the channel is put into data trace mode. The channel snoops on the CPU VBUSM, ITCM, DTCM buses for any read transaction. Any read data on these buses is compressed by the PSA Signature Register. When suspend is on, the PSA Signature Register does not compress any read data on these buses. 0 = Data Trace disable 1 = Data Trace enable
3:2	RESERVED	NONE	0h	Reserved
1:0	CH1_MODE	R/W	0h	Channel 1 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode

14.7.7.4.2.4 CRC_INTS Register

14.7.7.4.2.4.1 CRC_INTS Register (Offset = 18h) [reset = 0h]

CRC Interrupt Enable Set Register

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Table 14-14195. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0018h + formula

Figure 14-6994. CRC_INTS Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT_ENS_	CH4_UNDERENS	CH4_OVERENS	CH4_CRC_FAILENS	CH4_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			CH3_TIME_OUT_ENS	CH3_UNDERENS	CH3_OVERENS	CH3_CRC_FAILENS	CH3_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			CH2_TIME_OUT_ENS_	CH2_UNDERENS	CH2_OVERENS	CH2_CRC_FAILENS	CH2_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH1_TIME_OUT_ENS_	CH1_UNDERENS	CH1_OVERENS	CH1_CRC_FAILENS	CH1_CCITENS
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 14-14196. CRC_INTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT_ENS_	R/W1TS	0h	Channel 4 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
27	CH4_UNDERENS	R/W1TS	0h	Channel 4 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
26	CH4_OVERENS	R/W1TS	0h	Channel 4 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable

Table 14-14196. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CH4_CRC_FAILENS	R/W1TS	0h	Channel 4 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
24	CH4_CCITENS	R/W1TS	0h	Channel 4 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
23:21	RESERVED	NONE	0h	Reserved
20	CH3_TIME_OUT_ENS	R/W1TS	0h	Channel 3 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
19	CH3_UNDERENS	R/W1TS	0h	Channel 3 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
18	CH3_OVERENS	R/W1TS	0h	Channel 3 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
17	CH3_CRC_FAILENS	R/W1TS	0h	Channel 3 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
16	CH3_CCITENS	R/W1TS	0h	Channel 3 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT_ENS_	R/W1TS	0h	Channel 2 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable

Table 14-14196. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CH2_UNDERENS	R/W1TS	0h	Channel 2 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
10	CH2_OVERENS	R/W1TS	0h	Channel 2 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
9	CH2_CRC_FAILENS	R/W1TS	0h	Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
8	CH2_CCITENS	R/W1TS	0h	Channel 2 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT_ENS_	R/W1TS	0h	Channel 1 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
3	CH1_UNDERENS	R/W1TS	0h	Channel 1 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
2	CH1_OVERENS	R/W1TS	0h	Channel 1 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
1	CH1_CRC_FAILENS	R/W1TS	0h	Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable

Table 14-14196. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_CCITENS	R/W1TS	0h	Channel 1 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable

14.7.7.4.2.5 CRC_INTR Register

14.7.7.4.2.5.1 CRC_INTR Register (Offset = 20h) [reset = 0h]

CRC Interrupt Enable Reset Register

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Table 14-14197. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0020h + formula

Figure 14-6995. CRC_INTR Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT_ENR	CH4_UNDERENR	CH4_OVERENR	CH4_CRC_FAILENR	CH4_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED			CH3_TIME_OUT_ENR_	CH3_UNDERENR	CH3_OVERENR	CH3_CRC_FAILENR	CH3_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED			CH2_TIME_OUT_ENR_	CH2_UNDERENR	CH2_OVERENR	CH2_CRC_FAILENR	CH2_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED			CH1_TIME_OUT_ENR_	CH1_UNDERENR	CH1_OVERENR	CH1_CRC_FAILENR	CH1_CCITENR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-14198. CRC_INTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT_ENR	R/W1TC	0h	Channel 4 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
27	CH4_UNDERENR	R/W1TC	0h	Channel 4 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
26	CH4_OVERENR	R/W1TC	0h	Channel 4 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable

Table 14-14198. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CH4_CRC_FAILENR	R/W1TC	0h	Channel 4 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
24	CH4_CCITENR	R/W1TC	0h	Channel 4 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
23:21	RESERVED	NONE	0h	Reserved
20	CH3_TIME_OUT_ENR_	R/W1TC	0h	Channel 3 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
19	CH3_UNDERENR	R/W1TC	0h	Channel 3 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
18	CH3_OVERENR	R/W1TC	0h	Channel 3 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
17	CH3_CRC_FAILENR	R/W1TC	0h	Channel 3 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
16	CH3_CCITENR	R/W1TC	0h	Channel 3 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT_ENR_	R/W1TC	0h	Channel 2 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable

Table 14-14198. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CH2_UNDERENR	R/W1TC	0h	Channel 2 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
10	CH2_OVERENR	R/W1TC	0h	Channel 2 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
9	CH2_CRC_FAILENR	R/W1TC	0h	Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
8	CH2_CCITENR	R/W1TC	0h	Channel 2 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT_ENR_	R/W1TC	0h	Channel 1 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
3	CH1_UNDERENR	R/W1TC	0h	Channel 1 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
2	CH1_OVERENR	R/W1TC	0h	Channel 1 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
1	CH1_CRC_FAILENR	R/W1TC	0h	Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable

Table 14-14198. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_CCITENR	R/W1TC	0h	Channel 1 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable

14.7.7.4.2.6 CRC_STATUS Register

14.7.7.4.2.6.1 CRC_STATUS Register (Offset = 28h) [reset = 0h]

CRC Interrupt Status Register

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Table 14-14199. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0028h + formula

Figure 14-6996. CRC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED			CH4_TIME_OUT	CH4_UNDER	CH4_OVER	CH4_CRC_FAIL	CH4_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			CH3_TIME_OUT	CH3_UNDER	CH3_OVER	CH3_CRC_FAIL	CH3_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			CH2_TIME_OUT	CH2_UNDER	CH2_OVER	CH2_CRC_FAIL	CH2_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CH1_TIME_OUT	CH1_UNDER	CH1_OVER	CH1_CRC_FAIL	CH1_CCIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 14-14200. CRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CH4_TIME_OUT	R/W1TC	0h	Channel 4 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
27	CH4_UNDER	R/W1TC	0h	Channel 4 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
26	CH4_OVER	R/W1TC	0h	Channel 4 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
25	CH4_CRC_FAIL	R/W1TC	0h	Channel 4 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
24	CH4_CCIT	R/W1TC	0h	Channel 4 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active
23:21	RESERVED	NONE	0h	Reserved

Table 14-14200. CRC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	CH3_TIME_OUT	R/W1TC	0h	Channel 3 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
19	CH3_UNDER	R/W1TC	0h	Channel 3 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
18	CH3_OVER	R/W1TC	0h	Channel 3 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
17	CH3_CRC_FAIL	R/W1TC	0h	Channel 3 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
16	CH3_CCIT	R/W1TC	0h	Channel 3 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active
15:13	RESERVED	NONE	0h	Reserved
12	CH2_TIME_OUT	R/W1TC	0h	Channel 2 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
11	CH2_UNDER	R/W1TC	0h	Channel 2 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
10	CH2_OVER	R/W1TC	0h	Channel 2 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
9	CH2_CRC_FAIL	R/W1TC	0h	Channel 2 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
8	CH2_CCIT	R/W1TC	0h	Channel 2 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active
7:5	RESERVED	NONE	0h	Reserved
4	CH1_TIME_OUT	R/W1TC	0h	Channel 1 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
3	CH1_UNDER	R/W1TC	0h	Channel 1 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
2	CH1_OVER	R/W1TC	0h	Channel 1 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
1	CH1_CRC_FAIL	R/W1TC	0h	Channel 1 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
0	CH1_CCIT	R/W1TC	0h	Channel 1 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active

14.7.7.4.2.7 CRC_INT_OFFSET_REG Register

14.7.7.4.2.7.1 CRC_INT_OFFSET_REG Register (Offset = 30h) [reset = 0h]

CRC Interrupt Offset

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Table 14-14201. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0030h + formula

Figure 14-6997. CRC_INT_OFFSET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CRC							
R							
0h							

Table 14-14202. CRC_INT_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CRC	R	0h	Interrupt Offset. This register indicates the highest priority pending interrupt vector address. Reading the offset register automatically clears the respective interrupt flag.

14.7.7.4.2.8 CRC_BUSY Register

14.7.7.4.2.8.1 CRC_BUSY Register (Offset = 38h) [reset = 0h]

CRC Busy Register

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Table 14-14203. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0038h + formula

Figure 14-6998. CRC_BUSY Name Register

31	30	29	28	27	26	25	24
RESERVED							CH4_BUSY
NONE							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED							CH3_BUSY
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							CH2_BUSY
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED							CH1_BUSY
NONE							R
0h							0h

Table 14-14204. CRC_BUSY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CH4_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
23:17	RESERVED	NONE	0h	Reserved
16	CH3_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
15:9	RESERVED	NONE	0h	Reserved
8	CH2_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
7:1	RESERVED	NONE	0h	Reserved
0	CH1_BUSY	R	0h	During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.

14.7.7.4.2.9 CRC_PCOUNT_REG1 Register

14.7.7.4.2.9.1 CRC_PCOUNT_REG1 Register (Offset = 40h) [reset = 0h]

CRC Pattern Counter Preload Register1

Return to Summary Table

Table 14-14205. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0040h + formula

Figure 14-6999. CRC_PCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CRC_PAT_COUNT1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT1							
R/W							
0h							

Table 14-14206. CRC_PCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT1	R/W	0h	Channel 1 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.7.7.4.2.10 CRC_SCOUNT_REG1 Register

14.7.7.4.2.10.1 CRC_SCOUNT_REG1 Register (Offset = 44h) [reset = 0h]

CRC Sector Counter Preload Register1

Return to Summary Table

Table 14-14207. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0044h + formula

Figure 14-7000. CRC_SCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT1							
R/W							
0h							

Table 14-14208. CRC_SCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT1	R/W	0h	Channel 1 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.7.7.4.2.11 CRC_CURSEC_REG1 Register

14.7.7.4.2.11.1 CRC_CURSEC_REG1 Register (Offset = 48h) [reset = 0h]

CRC Current Sector Register 1

Return to Summary Table

Table 14-14209. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0048h + formula

Figure 14-7001. CRC_CURSEC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC1							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC1							
R							
0h							

Table 14-14210. CRC_CURSEC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC1	R	0h	Channel 1 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.7.7.4.2.12 CRC_WDTOPLD1 Register

14.7.7.4.2.12.1 CRC_WDTOPLD1 Register (Offset = 4Ch) [reset = 0h]

CRC channel 1 Watchdog Timeout Preload Register A

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Table 14-14211. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 004Ch + formula

Figure 14-7002. CRC_WDTOPLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_WDTOPLD1							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_WDTOPLD1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_WDTOPLD1							
R/W							
0h							

Table 14-14212. CRC_WDTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD1	R/W	0h	Channel 1 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.7.7.4.2.13 CRC_BCTOPLD1 Register

14.7.7.4.2.13.1 CRC_BCTOPLD1 Register (Offset = 50h) [reset = 0h]

CRC channel 1 Block Complete Timeout Preload Register B

Return to Summary Table

Table 14-14213. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0050h + formula

Figure 14-7003. CRC_BCTOPLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD1							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD1							
R/W							
0h							

Table 14-14214. CRC_BCTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD1	R/W	0h	Channel 1 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated.

14.7.7.4.2.14 CRC_PSA_SIGREGL1 Register

14.7.7.4.2.14.1 CRC_PSA_SIGREGL1 Register (Offset = 60h) [reset = 0h]

Channel 1 PSA signature low register

Return to Summary Table

Table 14-14215. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0060h + formula

Figure 14-7004. CRC_PSA_SIGREGL1 Name Register

31	30	29	28	27	26	25	24
PSASIG1							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG1							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG1							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG1							
R/W							
0h							

Table 14-14216. CRC_PSA_SIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG1	R/W	0h	Channel 1 PSA Signature Low Register. This register contains the value stored at PSASIG1[31:0] register.

14.7.7.4.2.15 CRC_PSA_SIGREGH1 Register

14.7.7.4.2.15.1 CRC_PSA_SIGREGH1 Register (Offset = 64h) [reset = 0h]

Channel 1 PSA signature high register

Return to Summary Table

Table 14-14217. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0064h + formula

Figure 14-7005. CRC_PSA_SIGREGH1 Name Register

31	30	29	28	27	26	25	24
PSASIG1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG1_63_32							
R/W							
0h							

Table 14-14218. CRC_PSA_SIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG1_63_32	R/W	0h	Channel 1 PSA Signature High Register. This register contains the value stored at PSASIG1[63:32] register.

14.7.7.4.2.16 CRC_REGL1 Register

14.7.7.4.2.16.1 CRC_REGL1 Register (Offset = 68h) [reset = 0h]

Channel 1 CRC value low register

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Table 14-14219. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0068h + formula

Figure 14-7006. CRC_REGL1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CRC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CRC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14220. CRC_REGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1	R/W	0h	Channel 1 CRC Value Low Register. This register contains the current known good signature value stored at CRC1[31:0] register.

14.7.7.4.2.17 CRC_REGH1 Register

14.7.7.4.2.17.1 CRC_REGH1 Register (Offset = 6Ch) [reset = 0h]

Channel 1 CRC value high register

Return to Summary Table

Table 14-14221. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 006Ch + formula

Figure 14-7007. CRC_REGH1 Name Register

31	30	29	28	27	26	25	24
CRC1_47_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC1_47_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC1_47_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC1_47_32							
R/W							
0h							

Table 14-14222. CRC_REGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1_47_32	R/W	0h	Channel 1 CRC Value High Register. This register contains the current known good signature value stored at CRC1[63:32] register.

14.7.7.4.2.18 CRC_PSA_SECSIGREGL1 Register

14.7.7.4.2.18.1 CRC_PSA_SECSIGREGL1 Register (Offset = 70h) [reset = 0h]

Channel 1 PSA sector signature low register

Return to Summary Table

Table 14-14223. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0070h + formula

Figure 14-7008. CRC_PSA_SECSIGREGL1 Name Register

31	30	29	28	27	26	25	24
PSASECSIG1							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG1							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG1							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG1							
R							
0h							

Table 14-14224. CRC_PSA_SECSIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1	R	0h	Channel 1 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG1[31:0] register.

14.7.7.4.2.19 CRC_PSA_SECSIGREGH1 Register

14.7.7.4.2.19.1 CRC_PSA_SECSIGREGH1 Register (Offset = 74h) [reset = 0h]

Channel 1 PSA sector signature high register

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Table 14-14225. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0074h + formula

Figure 14-7009. CRC_PSA_SECSIGREGH1 Name Register

31	30	29	28	27	26	25	24
PSASECSIG1_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG1_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG1_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG1_63_32							
R							
0h							

Table 14-14226. CRC_PSA_SECSIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1_63_32	R	0h	Channel 1 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG1[63:32] register.

14.7.7.4.2.20 CRC_RAW_DATAREGL1 Register

14.7.7.4.2.20.1 CRC_RAW_DATAREGL1 Register (Offset = 78h) [reset = 0h]

Channel 1 Raw Data Low Register

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Table 14-14227. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0078h + formula

Figure 14-7010. CRC_RAW_DATAREGL1 Name Register

31	30	29	28	27	26	25	24
RAW_DATA1							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA1							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA1							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA1							
R							
0h							

Table 14-14228. CRC_RAW_DATAREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1	R	0h	Channel 1 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.7.7.4.2.21 CRC_RAW_DATAREGH1 Register

14.7.7.4.2.21.1 CRC_RAW_DATAREGH1 Register (Offset = 7Ch) [reset = 0h]

Channel 1 Raw Data High Register

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Table 14-14229. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 007Ch + formula

Figure 14-7011. CRC_RAW_DATAREGH1 Name Register

31	30	29	28	27	26	25	24
RAW_DATA1_47_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA1_47_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA1_47_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA1_47_32							
R							
0h							

Table 14-14230. CRC_RAW_DATAREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1_47_32	R	0h	Channel 1 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.7.7.4.2.22 CRC_PCOUNT_REG2 Register

14.7.7.4.2.22.1 CRC_PCOUNT_REG2 Register (Offset = 80h) [reset = 0h]

CRC Pattern Counter Preload Register2

Return to Summary Table

Table 14-14231. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0080h + formula

Figure 14-7012. CRC_PCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CRC_PAT_COUNT2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT2							
R/W							
0h							

Table 14-14232. CRC_PCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT2	R/W	0h	CRC Pattern Counter Preload Register 2 This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.7.7.4.2.23 CRC_SCOUNT_REG2 Register

14.7.7.4.2.23.1 CRC_SCOUNT_REG2 Register (Offset = 84h) [reset = 0h]

CRC Sector Counter Preload Register2

Return to Summary Table

Table 14-14233. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0084h + formula

Figure 14-7013. CRC_SCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT2							
R/W							
0h							

Table 14-14234. CRC_SCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT2	R/W	0h	Channel 2 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.7.7.4.2.24 CRC_CURSEC_REG2 Register

14.7.7.4.2.24.1 CRC_CURSEC_REG2 Register (Offset = 88h) [reset = 0h]

CRC Current Sector Register 2

Return to Summary Table

Table 14-14235. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0088h + formula

Figure 14-7014. CRC_CURSEC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC2							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC2							
R							
0h							

Table 14-14236. CRC_CURSEC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC2	R	0h	Channel 2 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.7.7.4.2.25 CRC_WDTOPLD2 Register

14.7.7.4.2.25.1 CRC_WDTOPLD2 Register (Offset = 8Ch) [reset = 0h]

CRC channel 2 Watchdog Timeout Preload Register

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Table 14-14237. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 008Ch + formula

Figure 14-7015. CRC_WDTOPLD2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_WDTOPLD2							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_WDTOPLD2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_WDTOPLD2							
R/W							
0h							

Table 14-14238. CRC_WDTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD2	R/W	0h	Channel 2 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.7.7.4.2.26 CRC_BCTOPLD2 Register

14.7.7.4.2.26.1 CRC_BCTOPLD2 Register (Offset = 90h) [reset = 0h]

CRC channel 2 Block Complete Timeout Preload Register

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Table 14-14239. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0090h + formula

Figure 14-7016. CRC_BCTOPLD2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CRC_BCTOPLD2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_BCTOPLD2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_BCTOPLD2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14240. CRC_BCTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD2	R/W	0h	Channel 2 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.7.7.4.2.27 CRC_PSA_SIGREGL2 Register

14.7.7.4.2.27.1 CRC_PSA_SIGREGL2 Register (Offset = A0h) [reset = 0h]

Channel 2 PSA signature low register

Return to Summary Table

Table 14-14241. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00A0h + formula

Figure 14-7017. CRC_PSA_SIGREGL2 Name Register

31	30	29	28	27	26	25	24
PSASIG2							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG2							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG2							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG2							
R/W							
0h							

Table 14-14242. CRC_PSA_SIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG2	R/W	0h	Channel 2 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register.

14.7.7.4.2.28 CRC_PSA_SIGREGH2 Register

14.7.7.4.2.28.1 CRC_PSA_SIGREGH2 Register (Offset = A4h) [reset = 0h]

Channel 2 PSA signature high register

Return to Summary Table

Table 14-14243. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00A4h + formula

Figure 14-7018. CRC_PSA_SIGREGH2 Name Register

31	30	29	28	27	26	25	24
PSASIG2_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG2_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG2_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG2_63_32							
R/W							
0h							

Table 14-14244. CRC_PSA_SIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG2_63_32	R/W	0h	Channel 2 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register.

14.7.7.4.2.29 CRC_REGL2 Register

14.7.7.4.2.29.1 CRC_REGL2 Register (Offset = A8h) [reset = 0h]

Channel 2 CRC value low register

Return to Summary Table

Table 14-14245. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00A8h + formula

Figure 14-7019. CRC_REGL2 Name Register

31	30	29	28	27	26	25	24
CRC2							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC2							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC2							
R/W							
0h							

Table 14-14246. CRC_REGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2	R/W	0h	Channel 2 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register.

14.7.7.4.2.30 CRC_REGH2 Register

14.7.7.4.2.30.1 CRC_REGH2 Register (Offset = ACh) [reset = 0h]

Channel 2 CRC value high register

Return to Summary Table

Table 14-14247. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00ACh + formula

Figure 14-7020. CRC_REGH2 Name Register

31	30	29	28	27	26	25	24
CRC2_63_32							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC2_63_32							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC2_63_32							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC2_63_32							
R/W							
0h							

Table 14-14248. CRC_REGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2_63_32	R/W	0h	Channel 2 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register.

14.7.7.4.2.31 CRC_PSA_SECSIGREGL2 Register

14.7.7.4.2.31.1 CRC_PSA_SECSIGREGL2 Register (Offset = B0h) [reset = 0h]

Channel 2 PSA sector signature low register

Return to Summary Table

Table 14-14249. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00B0h + formula

Figure 14-7021. CRC_PSA_SECSIGREGL2 Name Register

31	30	29	28	27	26	25	24
PSASECSIG2							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG2							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG2							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG2							
R							
0h							

Table 14-14250. CRC_PSA_SECSIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2	R	0h	Channel 2 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register.

14.7.7.4.2.32 CRC_PSA_SECSIGREGH2 Register

14.7.7.4.2.32.1 CRC_PSA_SECSIGREGH2 Register (Offset = B4h) [reset = 0h]

Channel 2 PSA sector signature high register

Return to Summary Table

Table 14-14251. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00B4h + formula

Figure 14-7022. CRC_PSA_SECSIGREGH2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PSASECSIG2_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PSASECSIG2_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PSASECSIG2_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PSASECSIG2_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14252. CRC_PSA_SECSIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2_63_32	R	0h	Channel 2 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register.

14.7.7.4.2.33 CRC_RAW_DATAREGL2 Register

14.7.7.4.2.33.1 CRC_RAW_DATAREGL2 Register (Offset = B8h) [reset = 0h]

Channel 2 Raw Data Low Register

Return to Summary Table

Table 14-14253. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00B8h + formula

Figure 14-7023. CRC_RAW_DATAREGL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RAW_DATA2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RAW_DATA2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RAW_DATA2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RAW_DATA2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14254. CRC_RAW_DATAREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2	R	0h	Channel 2 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.7.7.4.2.34 CRC_RAW_DATAREGH2 Register

14.7.7.4.2.34.1 CRC_RAW_DATAREGH2 Register (Offset = BCh) [reset = 0h]

Channel 2 Raw Data High Register

Return to Summary Table

Table 14-14255. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00BCh + formula

Figure 14-7024. CRC_RAW_DATAREGH2 Name Register

31	30	29	28	27	26	25	24
RAW_DATA2_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA2_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA2_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA2_63_32							
R							
0h							

Table 14-14256. CRC_RAW_DATAREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2_63_32	R	0h	Channel 2 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.7.7.4.2.35 CRC_PCOUNT_REG3 Register

14.7.7.4.2.35.1 CRC_PCOUNT_REG3 Register (Offset = C0h) [reset = 0h]

CRC Pattern Counter Preload Register3

Return to Summary Table

Table 14-14257. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00C0h + formula

Figure 14-7025. CRC_PCOUNT_REG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CRC_PAT_COUNT3</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_PAT_COUNT3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_PAT_COUNT3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14258. CRC_PCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT3	R/W	0h	Channel 3 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.7.7.4.2.36 CRC_SCOUNT_REG3 Register

14.7.7.4.2.36.1 CRC_SCOUNT_REG3 Register (Offset = C4h) [reset = 0h]

CRC Sector Counter Preload Register3

Return to Summary Table

Table 14-14259. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00C4h + formula

Figure 14-7026. CRC_SCOUNT_REG3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_SEC_COUNT3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_SEC_COUNT3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14260. CRC_SCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT3	R/W	0h	Channel 3 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.7.7.4.2.37 CRC_CURSEC_REG3 Register

14.7.7.4.2.37.1 CRC_CURSEC_REG3 Register (Offset = C8h) [reset = 0h]

CRC Current Sector Register 3

Return to Summary Table

Table 14-14261. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00C8h + formula

Figure 14-7027. CRC_CURSEC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC3							
R							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC3							
R							
0h							

Table 14-14262. CRC_CURSEC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC3	R	0h	Channel 3 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

14.7.7.4.2.38 CRC_WDTOPLD3 Register

14.7.7.4.2.38.1 CRC_WDTOPLD3 Register (Offset = CCh) [reset = 0h]

CRC channel 3 Watchdog Timeout Preload Register

Return to Summary Table

Table 14-14263. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00CCh + formula

Figure 14-7028. CRC_WDTOPLD3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CRC_WDTOPLD3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_WDTOPLD3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_WDTOPLD3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14264. CRC_WDTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD3	R/W	0h	Channel 3 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.7.7.4.2.39 CRC_BCTOPLD3 Register

14.7.7.4.2.39.1 CRC_BCTOPLD3 Register (Offset = D0h) [reset = 0h]

CRC channel 3 Block Complete Timeout Preload Register

Return to Summary Table

Table 14-14265. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00D0h + formula

Figure 14-7029. CRC_BCTOPLD3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD3							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD3							
R/W							
0h							

Table 14-14266. CRC_BCTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD3	R/W	0h	Channel 3 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.7.7.4.2.40 CRC_PSA_SIGREGL3 Register

14.7.7.4.2.40.1 CRC_PSA_SIGREGL3 Register (Offset = E0h) [reset = 0h]

Channel 3 PSA signature low register

Return to Summary Table

Table 14-14267. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00E0h + formula

Figure 14-7030. CRC_PSA_SIGREGL3 Name Register

31	30	29	28	27	26	25	24
PSASIG3							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG3							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG3							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG3							
R/W							
0h							

Table 14-14268. CRC_PSA_SIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG3	R/W	0h	Channel 3 PSA Signature Low Register. This register contains the value stored at PSASIG3[31:0] register.

14.7.7.4.2.41 CRC_PSA_SIGREGH3 Register

14.7.7.4.2.41.1 CRC_PSA_SIGREGH3 Register (Offset = E4h) [reset = 0h]

Channel 3 PSA signature high register

Return to Summary Table

Table 14-14269. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00E4h + formula

Figure 14-7031. CRC_PSA_SIGREGH3 Name Register

31	30	29	28	27	26	25	24
PSASIG3_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG3_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG3_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG3_63_32							
R/W							
0h							

Table 14-14270. CRC_PSA_SIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG3_63_32	R/W	0h	Channel 3 PSA Signature High Register. This register contains the value stored at PSASIG3[63:32] register.

14.7.7.4.2.42 CRC_REGL3 Register

14.7.7.4.2.42.1 CRC_REGL3 Register (Offset = E8h) [reset = 0h]

Channel 3 CRC value low register

Return to Summary Table

Table 14-14271. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00E8h + formula

Figure 14-7032. CRC_REGL3 Name Register

31	30	29	28	27	26	25	24
CRC3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC3							
R/W							
0h							

Table 14-14272. CRC_REGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC3	R/W	0h	Channel 3 CRC Value Low Register. This register contains the current known good signature value stored at CRC3[31:0] register.

14.7.7.4.2.43 CRC_REGH3 Register

14.7.7.4.2.43.1 CRC_REGH3 Register (Offset = ECh) [reset = 0h]

Channel 3 CRC value high register

Return to Summary Table

Table 14-14273. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00ECh + formula

Figure 14-7033. CRC_REGH3 Name Register

31	30	29	28	27	26	25	24
CRC3_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC3_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC3_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC3_63_32							
R/W							
0h							

Table 14-14274. CRC_REGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC3_63_32	R/W	0h	Channel 3 CRC Value High Register. This register contains the current known good signature value stored at CRC3[63:32] register.

14.7.7.4.2.44 CRC_PSA_SECSIGREGL3 Register

14.7.7.4.2.44.1 CRC_PSA_SECSIGREGL3 Register (Offset = F0h) [reset = 0h]

Channel 3 PSA sector signature low register

Return to Summary Table

Table 14-14275. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00F0h + formula

Figure 14-7034. CRC_PSA_SECSIGREGL3 Name Register

31	30	29	28	27	26	25	24
PSASECSIG3							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG3							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG3							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG3							
R							
0h							

Table 14-14276. CRC_PSA_SECSIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG3	R	0h	Channel 3 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG3[31:0] register.

14.7.7.4.2.45 CRC_PSA_SECSIGREGH3 Register

14.7.7.4.2.45.1 CRC_PSA_SECSIGREGH3 Register (Offset = F4h) [reset = 0h]

Channel 3 PSA sector signature high register

Return to Summary Table

Table 14-14277. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00F4h + formula

Figure 14-7035. CRC_PSA_SECSIGREGH3 Name Register

31	30	29	28	27	26	25	24
PSASECSIG3_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG3_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG3_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG3_63_32							
R							
0h							

Table 14-14278. CRC_PSA_SECSIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG3_63_32	R	0h	Channel 3 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG3[63:32] register.

14.7.7.4.2.46 CRC_RAW_DATAREGL3 Register

14.7.7.4.2.46.1 CRC_RAW_DATAREGL3 Register (Offset = F8h) [reset = 0h]

Channel 3 Raw Data Low Register

Return to Summary Table

Table 14-14279. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00F8h + formula

Figure 14-7036. CRC_RAW_DATAREGL3 Name Register

31	30	29	28	27	26	25	24
RAW_DATA3							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA3							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA3							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA3							
R							
0h							

Table 14-14280. CRC_RAW_DATAREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA3	R	0h	Channel 3 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.7.7.4.2.47 CRC_RAW_DATAREGH3 Register

14.7.7.4.2.47.1 CRC_RAW_DATAREGH3 Register (Offset = FCh) [reset = 0h]

Channel 3 Raw Data High Register

Return to Summary Table

Table 14-14281. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 00FCh + formula

Figure 14-7037. CRC_RAW_DATAREGH3 Name Register

31	30	29	28	27	26	25	24
RAW_DATA3_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA3_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA3_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA3_63_32							
R							
0h							

Table 14-14282. CRC_RAW_DATAREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA3_63_32	R	0h	Channel 3 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.7.7.4.2.48 CRC_PCOUNT_REG4 Register

14.7.7.4.2.48.1 CRC_PCOUNT_REG4 Register (Offset = 100h) [reset = 0h]

CRC Pattern Counter Preload Register4

Return to Summary Table

Table 14-14283. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0100h + formula

Figure 14-7038. CRC_PCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CRC_PAT_COUNT4			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT4							
R/W							
0h							

Table 14-14284. CRC_PCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	CRC_PAT_COUNT4	R/W	0h	Channel 4 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

14.7.7.4.2.49 CRC_SCOUNT_REG4 Register

14.7.7.4.2.49.1 CRC_SCOUNT_REG4 Register (Offset = 104h) [reset = 0h]

CRC Sector Counter Preload Register4

Return to Summary Table

Table 14-14285. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0104h + formula

Figure 14-7039. CRC_SCOUNT_REG4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_SEC_COUNT4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_SEC_COUNT4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14286. CRC_SCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_SEC_COUNT4	R/W	0h	Channel 4 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

14.7.7.4.2.50 CRC_CURSEC_REG4 Register

14.7.7.4.2.50.1 CRC_CURSEC_REG4 Register (Offset = 108h) [reset = 0h]

CRC Current Sector Register 4

Return to Summary Table

Table 14-14287. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0108h + formula

Figure 14-7040. CRC_CURSEC_REG4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_CURSEC4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_CURSEC4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14288. CRC_CURSEC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CRC_CURSEC4	R	0h	In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. In Semi-CPU mode, this register is used to indicate the sector number for which the compression complete has last happened.

14.7.7.4.2.51 CRC_WDTOPLD4 Register

14.7.7.4.2.51.1 CRC_WDTOPLD4 Register (Offset = 10Ch) [reset = 0h]

CRC channel 4 Watchdog Timeout Preload Register

Return to Summary Table

Table 14-14289. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 010Ch + formula

Figure 14-7041. CRC_WDTOPLD4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CRC_WDTOPLD4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CRC_WDTOPLD4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CRC_WDTOPLD4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14290. CRC_WDTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_WDTOPLD4	R/W	0h	This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

14.7.7.4.2.52 CRC_BCTOPLD4 Register

14.7.7.4.2.52.1 CRC_BCTOPLD4 Register (Offset = 110h) [reset = 0h]

CRC channel 4 Block Complete Timeout Preload Register

Return to Summary Table

Table 14-14291. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0110h + formula

Figure 14-7042. CRC_BCTOPLD4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD4							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD4							
R/W							
0h							

Table 14-14292. CRC_BCTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	CRC_BCTOPLD4	R/W	0h	This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated.

14.7.7.4.2.53 CRC_PSA_SIGREGL4 Register

14.7.7.4.2.53.1 CRC_PSA_SIGREGL4 Register (Offset = 120h) [reset = 0h]

Channel 4 PSA signature low register

Return to Summary Table

Table 14-14293. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0120h + formula

Figure 14-7043. CRC_PSA_SIGREGL4 Name Register

31	30	29	28	27	26	25	24
PSASIG4							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG4							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG4							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG4							
R/W							
0h							

Table 14-14294. CRC_PSA_SIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG4	R/W	0h	This register contains the value stored at PSASIG4[31:0] register.

14.7.7.4.2.54 CRC_PSA_SIGREGH4 Register

14.7.7.4.2.54.1 CRC_PSA_SIGREGH4 Register (Offset = 124h) [reset = 0h]

Channel 4 PSA signature high register

Return to Summary Table

Table 14-14295. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0124h + formula

Figure 14-7044. CRC_PSA_SIGREGH4 Name Register

31	30	29	28	27	26	25	24
PSASIG4_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG4_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG4_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG4_63_32							
R/W							
0h							

Table 14-14296. CRC_PSA_SIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG4_63_32	R/W	0h	This register contains the value stored at PSASIG4[63:32] register.

14.7.7.4.2.55 CRC_REGL4 Register

14.7.7.4.2.55.1 CRC_REGL4 Register (Offset = 128h) [reset = 0h]

Channel 4 CRC value low register

Return to Summary Table

Table 14-14297. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0128h + formula

Figure 14-7045. CRC_REGL4 Name Register

31	30	29	28	27	26	25	24
CRC4							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC4							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC4							
R/W							
0h							

Table 14-14298. CRC_REGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC4	R/W	0h	Channel 4 CRC Value Low Register.

14.7.7.4.2.56 CRC_REGH4 Register

14.7.7.4.2.56.1 CRC_REGH4 Register (Offset = 12Ch) [reset = 0h]

Channel 4 CRC value high register

Return to Summary Table

Table 14-14299. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 012Ch + formula

Figure 14-7046. CRC_REGH4 Name Register

31	30	29	28	27	26	25	24
CRC4_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC4_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC4_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC4_63_32							
R/W							
0h							

Table 14-14300. CRC_REGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC4_63_32	R/W	0h	Channel 4 CRC Value High Register.

14.7.7.4.2.57 CRC_PSA_SECSIGREGL4 Register

14.7.7.4.2.57.1 CRC_PSA_SECSIGREGL4 Register (Offset = 130h) [reset = 0h]

Channel 4 PSA sector signature low register

Return to Summary Table

Table 14-14301. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0130h + formula

Figure 14-7047. CRC_PSA_SECSIGREGL4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">PSASECSIG4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">PSASECSIG4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PSASECSIG4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PSASECSIG4</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14302. CRC_PSA_SECSIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG4	R	0h	Channel 4 PSA Sector Signature Low Register.

14.7.7.4.2.58 CRC_PSA_SECSIGREGH4 Register

14.7.7.4.2.58.1 CRC_PSA_SECSIGREGH4 Register (Offset = 134h) [reset = 0h]

Channel 4 PSA sector signature high register

Return to Summary Table

Table 14-14303. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0134h + formula

Figure 14-7048. CRC_PSA_SECSIGREGH4 Name Register

31	30	29	28	27	26	25	24
PSASECSIG4_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG4_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG4_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG4_63_32							
R							
0h							

Table 14-14304. CRC_PSA_SECSIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG4_63_32	R	0h	Channel 4 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG4[63:32] register.

14.7.7.4.2.59 CRC_RAW_DATAREGL4 Register

14.7.7.4.2.59.1 CRC_RAW_DATAREGL4 Register (Offset = 138h) [reset = 0h]

Channel 4 Raw Data Low Register

Return to Summary Table

Table 14-14305. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0138h + formula

Figure 14-7049. CRC_RAW_DATAREGL4 Name Register

31	30	29	28	27	26	25	24
RAW_DATA4							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA4							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA4							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA4							
R							
0h							

Table 14-14306. CRC_RAW_DATAREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA4	R	0h	Channel 4 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data.

14.7.7.4.2.60 CRC_RAW_DATAREGH4 Register

14.7.7.4.2.60.1 CRC_RAW_DATAREGH4 Register (Offset = 13Ch) [reset = 0h]

Channel 4 Raw Data High Register

Return to Summary Table

Table 14-14307. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 013Ch + formula

Figure 14-7050. CRC_RAW_DATAREGH4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RAW_DATA4_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RAW_DATA4_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RAW_DATA4_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RAW_DATA4_63_32</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14308. CRC_RAW_DATAREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA4_63_32	R	0h	Channel 4 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data.

14.7.7.4.2.61 CRC_MBUS_SEL Register

14.7.7.4.2.61.1 CRC_MBUS_SEL Register (Offset = 140h) [reset = 7h]

Data bus tracing selection

Return to Summary Table

Table 14-14309. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0140h + formula

Figure 14-7051. CRC_MBUS_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MEN	DTC_MEN	ITC_MEN
NONE					R/W	R/W	R/W
0h					1h	1h	1h

Table 14-14310. CRC_MBUS_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MEN	R/W	1h	Enable/disables the tracing of VBUSM 0: Tracing of VBUSM controller bus has been disabled 1: Tracing of VBUSM controller bus has been enabled
1	DTC_MEN	R/W	1h	Enable/disables the tracing of data TCM 0: Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled 1: Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled
0	ITC_MEN	R/W	1h	Enable/disables the tracing of instruction TCM 0: Tracing of ITCM bus has been disabled 1: Tracing of ITCM bus has been enabled Please refer the description of CPU Data trace at page 1-21 for the priority between different data buses.

14.7.7.4.2.62 CRC_I0_PSA_SIGREG1_CPY_J Register

14.7.7.4.2.62.1 CRC_I0_PSA_SIGREG1_CPY_J Register (Offset = 200h) [reset = 0h]

Region for Channel 1 PSA signature block used by DMA based systems.

Return to Summary Table

Table 14-14311. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0200h + formula

Figure 14-7052. CRC_I0_PSA_SIGREG1_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG1_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG1_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG1_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG1_CPY0							
W							
0h							

Table 14-14312. CRC_I0_PSA_SIGREG1_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG1_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG1 register for DMA destination, it is write only, the result can be found in the PSASIG1 register.

14.7.7.4.2.63 CRC_I0_PSA_SIGREG2_CPY_J Register

14.7.7.4.2.63.1 CRC_I0_PSA_SIGREG2_CPY_J Register (Offset = 280h) [reset = 0h]

Region for Channel 2 PSA signature block used by DMA based systems.

Return to Summary Table

Table 14-14313. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0280h + formula

Figure 14-7053. CRC_I0_PSA_SIGREG2_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG2_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG2_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG2_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG2_CPY0							
W							
0h							

Table 14-14314. CRC_I0_PSA_SIGREG2_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG2_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG2 register for DMA destination, it is write only, the result can be found in the PSASIG2 register.

14.7.7.4.2.64 CRC_I0_PSA_SIGREG3_CPY_J Register

14.7.7.4.2.64.1 CRC_I0_PSA_SIGREG3_CPY_J Register (Offset = 300h) [reset = 0h]

Region for Channel 3 PSA signature block used by DMA based systems.

Return to Summary Table

Table 14-14315. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0300h + formula

Figure 14-7054. CRC_I0_PSA_SIGREG3_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG3_CPY0							
W							
0h							
23	22	21	20	19	18	17	16
I0_PSASIG3_CPY0							
W							
0h							
15	14	13	12	11	10	9	8
I0_PSASIG3_CPY0							
W							
0h							
7	6	5	4	3	2	1	0
I0_PSASIG3_CPY0							
W							
0h							

Table 14-14316. CRC_I0_PSA_SIGREG3_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG3_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG3 register for DMA destination, it is write only, the result can be found in the PSASIG3 register.

14.7.7.4.2.65 CRC_I0_PSA_SIGREG4_CPY_J Register

14.7.7.4.2.65.1 CRC_I0_PSA_SIGREG4_CPY_J Register (Offset = 380h) [reset = 0h]

Region for Channel 4 PSA signature block used by DMA based systems.

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Table 14-14317. Instance Table

Instance Name	Physical Address
MCRC64_0	3030 0380h + formula

Figure 14-7055. CRC_I0_PSA_SIGREG4_CPY_j Name Register

31	30	29	28	27	26	25	24
I0_PSASIG4_CPY0							
W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
I0_PSASIG4_CPY0							
W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
I0_PSASIG4_CPY0							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I0_PSASIG4_CPY0							
W							
0h							

Table 14-14318. CRC_I0_PSA_SIGREG4_CPY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	I0_PSASIG4_CPY0	W	0h	This register is a 128 byte block copy of the PSASIG4 register for DMA destination, it is write only, the result can be found in the PSASIG4 register.

14.7.7.5 ECC_AGGR

ECC_AGGR

14.7.7.5.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 14-14319. ECC_AGGR Registers, Base Address=0403 0000h, Length=1024

Offset	Length	Register Name	WKUP_ECC_AGGR2 Physical Address
0h	32	ECC_AGGR_REV	0403 0000h
8h	32	ECC_AGGR_VECTOR	0403 0008h
Ch	32	ECC_AGGR_STAT	0403 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	0403 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	0403 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	0403 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	0403 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	0403 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	0403 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	0403 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	0403 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	0403 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	0403 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	0403 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	0403 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	0403 020Ch

14.7.7.5.2 ECC_AGGR Registers

ECC_AGGR Registers

14.7.7.5.2.1 ECC_AGGR_REV Register

14.7.7.5.2.1.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters

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Table 14-14320. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0000h

Figure 14-7056. ECC_AGGR_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">MODULE_ID</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">6A0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MODULE_ID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">6A0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">REVRTL</td><td colspan="3">REVMAJ</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">7h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">REVMIN</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">1h</td></tr>
</table>

Table 14-14321. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

14.7.7.5.2.2 ECC_AGGR_VECTOR Register

14.7.7.5.2.2.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register

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Table 14-14322. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0008h

Figure 14-7057. ECC_AGGR_VECTOR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="7">RESERVED</td><td>RD_SVBUS_DONE</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TC</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RD_SVBUS_ADDRESS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RD_SVBUS</td><td colspan="4">RESERVED</td><td colspan="3">ECC_VECTOR</td></tr>
<tr><td>R/W1TS</td><td colspan="4">NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ECC_VECTOR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14323. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.7.7.5.2.3 ECC_AGGR_STAT Register

14.7.7.5.2.3.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = Fh]

Misc Status

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Table 14-14324. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 000Ch

Figure 14-7058. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					NUM_RAMS		
NONE					R		
0h					Fh		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_RAMS							
R							
Fh							

Table 14-14325. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	Fh	Indicates the number of RAMS serviced by the ECC aggregator

14.7.7.5.2.4 ECC_AGGR_RESERVED_SVBUS_J Register

14.7.7.5.2.4.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 14-14326. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0010h + formula

Figure 14-7059. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 14-14327. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

14.7.7.5.2.5 ECC_AGGR_SEC_EOI_REG Register

14.7.7.5.2.5.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register

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Table 14-14328. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 003Ch

Figure 14-7060. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 14-14329. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.7.5.2.6 ECC_AGGR_SEC_STATUS_REG0 Register

14.7.7.5.2.6.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 14-14330. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0040h

Figure 14-7061. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED	ECCAGG_PEND	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_PEND
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_PEND	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_PEND	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_PEND	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14331. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
13	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
12	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_err_scr_am275_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
11	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
10	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_cbass_default_err_am275_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
9	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_edc_ctrl_busecc_pend
8	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_busecc_pend
7	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_busecc_pend
6	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_m2p_bridge_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_bridge_busecc_pend
5	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend
4	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend

Table 14-14331. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.7.7.5.2.7 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

14.7.7.5.2.7.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 14-14332. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0080h

Figure 14-7062. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ECCAGG_ENABLE_SET	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_ENABLE_SET
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_SET	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_SET	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_SET	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14333. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
13	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
12	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_err_scr_am275_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
11	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
10	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_cbass_default_err_am275_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
9	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_edc_ctrl_busecc_pend
8	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_busecc_pend
7	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_busecc_pend
6	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_m2p_bridge_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_bridge_busecc_pend
5	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend

Table 14-14333. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.7.7.5.2.8 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

14.7.7.5.2.8.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 14-14334. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 00C0h

Figure 14-7063. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED	ECCAGG_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_ENABLE_CLR
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_CLR	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_CLR	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14335. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
13	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
12	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_err_scr_am275_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
11	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
10	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_cbass_default_err_am275_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
9	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_edc_ctrl_busecc_pend
8	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_busecc_pend
7	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_busecc_pend
6	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_m2p_bridge_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_bridge_busecc_pend
5	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend

Table 14-14335. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.7.7.5.2.9 ECC_AGGR_DED_EOI_REG Register

14.7.7.5.2.9.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 14-14336. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 013Ch

Figure 14-7064. ECC_AGGR_DED_EOI_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>EOI_WR</td></tr>
<tr><td colspan="7">NONE</td><td>R/W1TS</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14337. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

14.7.7.5.2.10 ECC_AGGR_DED_STATUS_REG0 Register

14.7.7.5.2.10.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 14-14338. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0140h

Figure 14-7065. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	ECCAGG_PEND	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_PEND
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_PEND	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_PEND	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_PEND	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_PEND	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14339. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	ECCAGG_PEND	R/W1TS	0h	Interrupt Pending Status for eccagg_pend
13	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
12	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_err_scr_am275_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
11	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
10	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_cbass_default_err_am275_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
9	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_edc_ctrl_busecc_pend
8	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_busecc_pend
7	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_busecc_pend
6	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_wkup_safe_cbass_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_m2p_bridge_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_bridge_busecc_pend
5	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend
4	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend

Table 14-14339. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_PEND	R/W1TS	0h	Interrupt Pending Status for am275_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.7.7.5.2.11 ECC_AGGR_DED_ENABLE_SET_REG0 Register

14.7.7.5.2.11.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 14-14340. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0180h

Figure 14-7066. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ECCAGG_ENABLE_SET	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_ENABLE_SET
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_ENABLE_SET	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_SET	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_SET	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_SET	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14341. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	ECCAGG_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for eccagg_pend
13	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
12	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_err_scr_am275_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
11	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
10	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_cbass_default_err_am275_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
9	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_edc_ctrl_busecc_pend
8	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_busecc_pend
7	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_busecc_pend
6	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_wkup_safe_cbass_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_m2p_bridge_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_bridge_busecc_pend
5	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend

Table 14-14341. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for am275_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.7.7.5.2.12 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

14.7.7.5.2.12.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 14-14342. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 01C0h

Figure 14-7067. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED	ECCAGG_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_ENABLE_CLR
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_ENABLE_CLR	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_CLR	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_CLR	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-14343. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14	ECCAGG_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for eccagg_pend
13	AM275_WKUP_SAFE_CBASS_MCU_SYSCLK0_4_CLK_EDC_CTRL_CBASS_INT_MCU_SYSCLK0_4_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_MCU_SYSCLK0_4_clk_edc_ctrl_cbass_int_MCU_SYSCLK0_4_busecc_pend
12	AM275_WKUP_SAFE_CBASS_ERR_SCR_AM275_WKUP_SAFE_CBASS_ERR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_err_scr_am275_wkup_safe_cbass_err_scr_edc_ctrl_busecc_pend
11	AM275_WKUP_SAFE_CBASS_ERR_SLV_P2P_BRIDGE_ERR_SLV_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_err_slv_p2p_bridge_err_slv_bridge_busecc_pend
10	AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_AM275_WKUP_SAFE_CBASS_CBASS_DEFAULT_ERR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_cbass_default_err_am275_wkup_safe_cbass_cbass_default_err_edc_ctrl_busecc_pend
9	AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_AM275_WKUP_SAFE_CBASS_SCRP_32_SAFE_MCU_CLK4_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_am275_wkup_safe_cbass_SCRP_32_SAFE_MCU_CLK4_scr_edc_ctrl_busecc_pend
8	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_IAM275_WKUP_SAFE_CBASS_WKUP_0_CBASS_ERR_SLV_P2P_GASKET_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_Iam275_wkup_safe_cbass_wkup_0_cbass_err_slv_p2p_gasket_busecc_pend
7	AM275_WKUP_SAFE_CBASS_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_IAM275_WKUP_SAFE_ECC_AGGR_WKUP_0_CFG_P2P_GASKET_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_Iam275_wkup_safe_ecc_aggr_wkup_0_cfg_p2p_gasket_busecc_pend
6	AM275_WKUP_SAFE_CBASS_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_M2P_BRIDGE_EXPORT_AM275_WKUP_DM_CBASS_TO_AM275_WKUP_SAFE_CBASS_DATA_L0_BRIDGE_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_wkup_safe_cbass_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_m2p_bridge_export_am275_wkup_dm_cbass_to_am275_wkup_safe_cbass_data_l0_bridge_busecc_pend
5	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_2_pend

Table 14-14343. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_1_pend
3	AM275_MCU_PADCFG_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_padcfg_ctrl_mmr_edc_ctrl_busecc_0_pend
2	AM275_MCU_PLL_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_pll_mmr_edc_ctrl_busecc_pend
1	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_ctrl_mmr_edc_ctrl_busecc_1_pend
0	AM275_MCU_CTRL_MMR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for am275_mcu_ctrl_mmr_edc_ctrl_busecc_0_pend

14.7.7.5.2.13 ECC_AGGR_AGGR_ENABLE_SET Register

14.7.7.5.2.13.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register

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Table 14-14344. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0200h

Figure 14-7068. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 14-14345. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

14.7.7.5.2.14 ECC_AGGR_AGGR_ENABLE_CLR Register

14.7.7.5.2.14.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register

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Table 14-14346. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0204h

Figure 14-7069. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 14-14347. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

14.7.7.5.2.15 ECC_AGGR_AGGR_STATUS_SET Register

14.7.7.5.2.15.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register

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Table 14-14348. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 0208h

Figure 14-7070. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 14-14349. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

14.7.7.5.2.16 ECC_AGGR_AGGR_STATUS_CLR Register

14.7.7.5.2.16.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register

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Table 14-14350. Instance Table

Instance Name	Physical Address
WKUP_ECC_AGGR2	0403 020Ch

Figure 14-7071. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 14-14351. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

14.8 On-Chip Debug Registers

14.8.1 DEBUGSS_WRAP

DEBUGSS_WRAP

14.8.1.1 DEBUGSS_WRAP Summaries

DEBUGSS_WRAP Summaries

Table 14-14352. ROM_TABLE_0_0 Registers, Base Address=0007 0000 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	ROM_TABLE_0_0_ROM_ENTRY0	0007 0000 0000h
4h	32	ROM_TABLE_0_0_ROM_ENTRY1	0007 0000 0004h
8h	32	ROM_TABLE_0_0_ROM_ENTRY2	0007 0000 0008h
8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY0	0007 0000 0008h
Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY1	0007 0000 000Ch
10h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY2	0007 0000 0010h
14h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY3	0007 0000 0014h
18h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY4	0007 0000 0018h
1Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY5	0007 0000 001Ch
20h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY6	0007 0000 0020h
24h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY7	0007 0000 0024h
28h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY8	0007 0000 0028h
2Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY9	0007 0000 002Ch
30h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY10	0007 0000 0030h
34h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY11	0007 0000 0034h
38h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY12	0007 0000 0038h
3Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY13	0007 0000 003Ch
40h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY14	0007 0000 0040h
44h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY15	0007 0000 0044h
48h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY16	0007 0000 0048h
4Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY17	0007 0000 004Ch
50h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY18	0007 0000 0050h
54h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY19	0007 0000 0054h
58h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY20	0007 0000 0058h
5Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY21	0007 0000 005Ch
60h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY22	0007 0000 0060h
64h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY23	0007 0000 0064h
68h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY24	0007 0000 0068h
6Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY25	0007 0000 006Ch
70h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY26	0007 0000 0070h
74h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY27	0007 0000 0074h
78h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY28	0007 0000 0078h
7Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY29	0007 0000 007Ch
80h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY30	0007 0000 0080h
84h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY31	0007 0000 0084h
88h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY32	0007 0000 0088h
8Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY33	0007 0000 008Ch
90h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY34	0007 0000 0090h
94h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY35	0007 0000 0094h
98h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY36	0007 0000 0098h

Table 14-14352. ROM_TABLE_0_0 Registers, Base Address=0007 0000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
9Ch	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY37	0007 0000 009Ch
A0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY38	0007 0000 00A0h
A4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY39	0007 0000 00A4h
A8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY40	0007 0000 00A8h
ACh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY41	0007 0000 00ACh
B0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY42	0007 0000 00B0h
B4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY43	0007 0000 00B4h
B8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY44	0007 0000 00B8h
BCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY45	0007 0000 00BCh
C0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY46	0007 0000 00C0h
C4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY47	0007 0000 00C4h
C8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY48	0007 0000 00C8h
CCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY49	0007 0000 00CCh
D0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY50	0007 0000 00D0h
D4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY51	0007 0000 00D4h
D8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY52	0007 0000 00D8h
DCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY53	0007 0000 00DCh
E0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY54	0007 0000 00E0h
E4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY55	0007 0000 00E4h
E8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY56	0007 0000 00E8h
ECh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY57	0007 0000 00ECh
F0h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY58	0007 0000 00F0h
F4h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY59	0007 0000 00F4h
F8h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY60	0007 0000 00F8h
FCh	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY61	0007 0000 00FCh
100h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY62	0007 0000 0100h
104h	32	ROM_TABLE_0_0_ROM_MANUAL_ENTRY63	0007 0000 0104h
108h	32	ROM_TABLE_0_0_PERIPHID0	0007 0000 0108h
10Ch	32	ROM_TABLE_0_0_PERIPHID1	0007 0000 010Ch
110h	32	ROM_TABLE_0_0_PERIPHID2	0007 0000 0110h
114h	32	ROM_TABLE_0_0_PERIPHID3	0007 0000 0114h
118h	32	ROM_TABLE_0_0_PERIPHID4	0007 0000 0118h
3FCh	32	ROM_TABLE_0_0_COMPID0	0007 0000 03FCh
3FCh	32	ROM_TABLE_0_0_COMPID1	0007 0000 03FCh
3FCh	32	ROM_TABLE_0_0_COMPID2	0007 0000 03FCh
3FCh	32	ROM_TABLE_0_0_COMPID3	0007 0000 03FCh

Table 14-14353. CFGAP_CFG_0 Registers, Base Address=0007 0000 2000h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CFGAP_CFG_0_JTAGID_REG	0007 0000 2000h
4h	32	CFGAP_CFG_0_USERID_REG	0007 0000 2004h
8h	32	CFGAP_CFG_0_VERSION_REG	0007 0000 2008h
FCh	32	CFGAP_CFG_0_APID_REGISTER	0007 0000 20FCh

Table 14-14354. APBAP_CFG_0 Registers, Base Address=0007 0000 2100h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	APBAP_CFG_0_CSWREG	0007 0000 2100h
Ch	32	APBAP_CFG_0_DRWREG	0007 0000 210Ch
10h	32	APBAP_CFG_0_BD0REG	0007 0000 2110h
14h	32	APBAP_CFG_0_BD1REG	0007 0000 2114h
18h	32	APBAP_CFG_0_BD2REG	0007 0000 2118h
1Ch	32	APBAP_CFG_0_BD3REG	0007 0000 211Ch
F8h	32	APBAP_CFG_0_ROM_REGISTER	0007 0000 21F8h
FCh	32	APBAP_CFG_0_ID_REGISTER	0007 0000 21FCh

Table 14-14355. AXIAP_CFG_0 Registers, Base Address=0007 0000 2200h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	AXIAP_CFG_0_CSWREG	0007 0000 2200h
Ch	32	AXIAP_CFG_0_DRWREG	0007 0000 220Ch
10h	32	AXIAP_CFG_0_BD0REG	0007 0000 2210h
14h	32	AXIAP_CFG_0_BD1REG	0007 0000 2214h
18h	32	AXIAP_CFG_0_BD2REG	0007 0000 2218h
1Ch	32	AXIAP_CFG_0_BD3REG	0007 0000 221Ch
20h	32	AXIAP_CFG_0_MBT_REGISTER	0007 0000 2220h
F0h	32	AXIAP_CFG_0_ROM_HI_REGISTER	0007 0000 22F0h
F4h	32	AXIAP_CFG_0_CFG_REGISTER	0007 0000 22F4h
F8h	32	AXIAP_CFG_0_ROM_LO_REGISTER	0007 0000 22F8h
FCh	32	AXIAP_CFG_0_ID_REGISTER	0007 0000 22FCh

Table 14-14356. PWRAP_CFG_0 Registers, Base Address=0007 0000 2300h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FCh	32	PWRAP_CFG_0_ID_REGISTER	0007 0000 23FCh

Table 14-14357. PVIEW_CFG_0 Registers, Base Address=0007 0000 2400h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	PVIEW_CFG_0_PVIEW_STATE0	0007 0000 2400h
F0h	32	PVIEW_CFG_0_PVIEW_CAPABILITY	0007 0000 24F0h
FCh	32	PVIEW_CFG_0_ID_REGISTER	0007 0000 24FCh

Table 14-14358. JTAGAP_CFG_0 Registers, Base Address=0007 0000 2500h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	JTAGAP_CFG_0_CSW	0007 0000 2500h
4h	32	JTAGAP_CFG_0_PSEL_REG	0007 0000 2504h
8h	32	JTAGAP_CFG_0_PSTA_REG	0007 0000 2508h
10h	32	JTAGAP_CFG_0_BYTEFIFO1	0007 0000 2510h
14h	32	JTAGAP_CFG_0_BYTEFIFO2	0007 0000 2514h
18h	32	JTAGAP_CFG_0_BYTEFIFO3	0007 0000 2518h
1Ch	32	JTAGAP_CFG_0_BYTEFIFO4	0007 0000 251Ch
FCh	32	JTAGAP_CFG_0_ID_REGISTER	0007 0000 25FCh

Table 14-14359. SECAP_CFG_0 Registers, Base Address=0007 0000 2600h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	SECAP_CFG_0_TXDATA	0007 0000 2600h
4h	32	SECAP_CFG_0_TXCTRL	0007 0000 2604h
8h	32	SECAP_CFG_0_RXDATA	0007 0000 2608h
Ch	32	SECAP_CFG_0_RXCTRL	0007 0000 260Ch

Table 14-14360. CORTEX0_CFG_0 Registers, Base Address=0007 0000 2700h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX0_CFG_0_CSWREG	0007 0000 2700h
Ch	32	CORTEX0_CFG_0_DRWREG	0007 0000 270Ch
10h	32	CORTEX0_CFG_0_BD0REG	0007 0000 2710h
14h	32	CORTEX0_CFG_0_BD1REG	0007 0000 2714h
18h	32	CORTEX0_CFG_0_BD2REG	0007 0000 2718h
1Ch	32	CORTEX0_CFG_0_BD3REG	0007 0000 271Ch
F8h	32	CORTEX0_CFG_0_ROM_REGISTER	0007 0000 27F8h
FCh	32	CORTEX0_CFG_0_ID_REGISTER	0007 0000 27FCh

Table 14-14361. CORTEX1_CFG_0 Registers, Base Address=0007 0000 2800h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX1_CFG_0_CSWREG	0007 0000 2800h
Ch	32	CORTEX1_CFG_0_DRWREG	0007 0000 280Ch
10h	32	CORTEX1_CFG_0_BD0REG	0007 0000 2810h
14h	32	CORTEX1_CFG_0_BD1REG	0007 0000 2814h
18h	32	CORTEX1_CFG_0_BD2REG	0007 0000 2818h
1Ch	32	CORTEX1_CFG_0_BD3REG	0007 0000 281Ch
F8h	32	CORTEX1_CFG_0_ROM_REGISTER	0007 0000 28F8h
FCh	32	CORTEX1_CFG_0_ID_REGISTER	0007 0000 28FCh

Table 14-14362. CORTEX2_CFG_0 Registers, Base Address=0007 0000 2900h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX2_CFG_0_CSWREG	0007 0000 2900h
Ch	32	CORTEX2_CFG_0_DRWREG	0007 0000 290Ch
10h	32	CORTEX2_CFG_0_BD0REG	0007 0000 2910h
14h	32	CORTEX2_CFG_0_BD1REG	0007 0000 2914h
18h	32	CORTEX2_CFG_0_BD2REG	0007 0000 2918h
1Ch	32	CORTEX2_CFG_0_BD3REG	0007 0000 291Ch
F8h	32	CORTEX2_CFG_0_ROM_REGISTER	0007 0000 29F8h
FCh	32	CORTEX2_CFG_0_ID_REGISTER	0007 0000 29FCh

Table 14-14363. CORTEX3_CFG_0 Registers, Base Address=0007 0000 2A00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX3_CFG_0_CSWREG	0007 0000 2A00h
Ch	32	CORTEX3_CFG_0_DRWREG	0007 0000 2A0Ch
10h	32	CORTEX3_CFG_0_BD0REG	0007 0000 2A10h
14h	32	CORTEX3_CFG_0_BD1REG	0007 0000 2A14h
18h	32	CORTEX3_CFG_0_BD2REG	0007 0000 2A18h

Table 14-14363. CORTEX3_CFG_0 Registers, Base Address=0007 0000 2A00h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
1Ch	32	CORTEX3_CFG_0_BD3REG	0007 0000 2A1Ch
F8h	32	CORTEX3_CFG_0_ROM_REGISTER	0007 0000 2AF8h
FCh	32	CORTEX3_CFG_0_ID_REGISTER	0007 0000 2AFCh

Table 14-14364. CORTEX4_CFG_0 Registers, Base Address=0007 0000 2B00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX4_CFG_0_CSWREG	0007 0000 2B00h
Ch	32	CORTEX4_CFG_0_DRWREG	0007 0000 2B0Ch
10h	32	CORTEX4_CFG_0_BD0REG	0007 0000 2B10h
14h	32	CORTEX4_CFG_0_BD1REG	0007 0000 2B14h
18h	32	CORTEX4_CFG_0_BD2REG	0007 0000 2B18h
1Ch	32	CORTEX4_CFG_0_BD3REG	0007 0000 2B1Ch
F8h	32	CORTEX4_CFG_0_ROM_REGISTER	0007 0000 2BF8h
FCh	32	CORTEX4_CFG_0_ID_REGISTER	0007 0000 2BFCh

Table 14-14365. CORTEX5_CFG_0 Registers, Base Address=0007 0000 2C00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX5_CFG_0_CSWREG	0007 0000 2C00h
Ch	32	CORTEX5_CFG_0_DRWREG	0007 0000 2C0Ch
10h	32	CORTEX5_CFG_0_BD0REG	0007 0000 2C10h
14h	32	CORTEX5_CFG_0_BD1REG	0007 0000 2C14h
18h	32	CORTEX5_CFG_0_BD2REG	0007 0000 2C18h
1Ch	32	CORTEX5_CFG_0_BD3REG	0007 0000 2C1Ch
F8h	32	CORTEX5_CFG_0_ROM_REGISTER	0007 0000 2CF8h
FCh	32	CORTEX5_CFG_0_ID_REGISTER	0007 0000 2CFCh

Table 14-14366. CORTEX6_CFG_0 Registers, Base Address=0007 0000 2D00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX6_CFG_0_CSWREG	0007 0000 2D00h
Ch	32	CORTEX6_CFG_0_DRWREG	0007 0000 2D0Ch
10h	32	CORTEX6_CFG_0_BD0REG	0007 0000 2D10h
14h	32	CORTEX6_CFG_0_BD1REG	0007 0000 2D14h
18h	32	CORTEX6_CFG_0_BD2REG	0007 0000 2D18h
1Ch	32	CORTEX6_CFG_0_BD3REG	0007 0000 2D1Ch
F8h	32	CORTEX6_CFG_0_ROM_REGISTER	0007 0000 2DF8h
FCh	32	CORTEX6_CFG_0_ID_REGISTER	0007 0000 2DFCh

Table 14-14367. CORTEX7_CFG_0 Registers, Base Address=0007 0000 2E00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX7_CFG_0_CSWREG	0007 0000 2E00h
Ch	32	CORTEX7_CFG_0_DRWREG	0007 0000 2E0Ch
10h	32	CORTEX7_CFG_0_BD0REG	0007 0000 2E10h
14h	32	CORTEX7_CFG_0_BD1REG	0007 0000 2E14h
18h	32	CORTEX7_CFG_0_BD2REG	0007 0000 2E18h
1Ch	32	CORTEX7_CFG_0_BD3REG	0007 0000 2E1Ch

Table 14-14367. CORTEX7_CFG_0 Registers, Base Address=0007 0000 2E00h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
F8h	32	CORTEX7_CFG_0_ROM_REGISTER	0007 0000 2EF8h
FCh	32	CORTEX7_CFG_0_ID_REGISTER	0007 0000 2EFCh

Table 14-14368. CORTEX8_CFG_0 Registers, Base Address=0007 0000 2F00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX8_CFG_0_CSWREG	0007 0000 2F00h
Ch	32	CORTEX8_CFG_0_DRWREG	0007 0000 2F0Ch
10h	32	CORTEX8_CFG_0_BD0REG	0007 0000 2F10h
14h	32	CORTEX8_CFG_0_BD1REG	0007 0000 2F14h
18h	32	CORTEX8_CFG_0_BD2REG	0007 0000 2F18h
1Ch	32	CORTEX8_CFG_0_BD3REG	0007 0000 2F1Ch
F8h	32	CORTEX8_CFG_0_ROM_REGISTER	0007 0000 2FF8h
FCh	32	CORTEX8_CFG_0_ID_REGISTER	0007 0000 2FFCh

Table 14-14369. ROM_TABLE_1_0 Registers, Base Address=0007 2000 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	ROM_TABLE_1_0_ROM_ENTRY0	0007 2000 0000h
4h	32	ROM_TABLE_1_0_ROM_ENTRY1	0007 2000 0004h
8h	32	ROM_TABLE_1_0_ROM_ENTRY2	0007 2000 0008h
Ch	32	ROM_TABLE_1_0_ROM_ENTRY3	0007 2000 000Ch
10h	32	ROM_TABLE_1_0_ROM_ENTRY4	0007 2000 0010h
14h	32	ROM_TABLE_1_0_ROM_ENTRY5	0007 2000 0014h
18h	32	ROM_TABLE_1_0_COMPUTE_CLUSTER0	0007 2000 0018h
1Ch	32	ROM_TABLE_1_0_COMPUTE_CLUSTER1	0007 2000 001Ch
20h	32	ROM_TABLE_1_0_COMPUTE_CLUSTER2	0007 2000 0020h
24h	32	ROM_TABLE_1_0_DEBUG_CELL0	0007 2000 0024h
28h	32	ROM_TABLE_1_0_DEBUG_CELL1	0007 2000 0028h
2Ch	32	ROM_TABLE_1_0_DEBUG_CELL2	0007 2000 002Ch
30h	32	ROM_TABLE_1_0_DEBUG_CELL3	0007 2000 0030h
34h	32	ROM_TABLE_1_0_DEBUG_CELL4	0007 2000 0034h
38h	32	ROM_TABLE_1_0_DEBUG_CELL5	0007 2000 0038h
3Ch	32	ROM_TABLE_1_0_DEBUG_CELL6	0007 2000 003Ch
40h	32	ROM_TABLE_1_0_DEBUG_CELL7	0007 2000 0040h
44h	32	ROM_TABLE_1_0_DEBUG_CELL8	0007 2000 0044h
48h	32	ROM_TABLE_1_0_DEBUG_CELL9	0007 2000 0048h
4Ch	32	ROM_TABLE_1_0_DEBUG_CELL10	0007 2000 004Ch
50h	32	ROM_TABLE_1_0_DEBUG_CELL11	0007 2000 0050h
50h	32	ROM_TABLE_1_0_EXTCSCOMP0	0007 2000 0050h
54h	32	ROM_TABLE_1_0_EXTCSCOMP1	0007 2000 0054h
58h	32	ROM_TABLE_1_0_EXTCSCOMP2	0007 2000 0058h
5Ch	32	ROM_TABLE_1_0_EXTCSCOMP3	0007 2000 005Ch
60h	32	ROM_TABLE_1_0_EXTCSCOMP4	0007 2000 0060h
64h	32	ROM_TABLE_1_0_EXTCSCOMP5	0007 2000 0064h
68h	32	ROM_TABLE_1_0_EXTCSCOMP6	0007 2000 0068h
6Ch	32	ROM_TABLE_1_0_EXTCSCOMP7	0007 2000 006Ch
70h	32	ROM_TABLE_1_0_EXTCSCOMP8	0007 2000 0070h

Table 14-14369. ROM_TABLE_1_0 Registers, Base Address=0007 2000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
74h	32	ROM_TABLE_1_0_EXTCSCOMP9	0007 2000 0074h
78h	32	ROM_TABLE_1_0_EXTCSCOMP10	0007 2000 0078h
7Ch	32	ROM_TABLE_1_0_EXTCSCOMP11	0007 2000 007Ch

Table 14-14370. CSCTI Registers, Base Address=0007 2000 1000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CSCTI_CTICONTROL	0007 2000 1000h
10h	32	CSCTI_CTIINTACK	0007 2000 1010h
14h	32	CSCTI_CTIAPPSET	0007 2000 1014h
18h	32	CSCTI_CTIAPPCLR	0007 2000 1018h
1Ch	32	CSCTI_CTIAPPPULSE	0007 2000 101Ch
20h	32	CSCTI_CTIINEN0	0007 2000 1020h
24h	32	CSCTI_CTIINEN1	0007 2000 1024h
28h	32	CSCTI_CTIINEN2	0007 2000 1028h
2Ch	32	CSCTI_CTIINEN3	0007 2000 102Ch
30h	32	CSCTI_CTIINEN4	0007 2000 1030h
34h	32	CSCTI_CTIINEN5	0007 2000 1034h
38h	32	CSCTI_CTIINEN6	0007 2000 1038h
3Ch	32	CSCTI_CTIINEN7	0007 2000 103Ch
A0h	32	CSCTI_CTIOUTEN0	0007 2000 10A0h
A4h	32	CSCTI_CTIOUTEN1	0007 2000 10A4h
A8h	32	CSCTI_CTIOUTEN2	0007 2000 10A8h
ACh	32	CSCTI_CTIOUTEN3	0007 2000 10ACh
B0h	32	CSCTI_CTIOUTEN4	0007 2000 10B0h
B4h	32	CSCTI_CTIOUTEN5	0007 2000 10B4h
B8h	32	CSCTI_CTIOUTEN6	0007 2000 10B8h
BCh	32	CSCTI_CTIOUTEN7	0007 2000 10BCh
130h	32	CSCTI_CTITRIGINSTATUS	0007 2000 1130h
134h	32	CSCTI_CTITRIGOUTSTATUS	0007 2000 1134h
138h	32	CSCTI_CTICHINSTATUS	0007 2000 1138h
13Ch	32	CSCTI_CTICHOUTSTATUS	0007 2000 113Ch
140h	32	CSCTI_CTIGATE	0007 2000 1140h
144h	32	CSCTI_ASICCTL	0007 2000 1144h
EDCh	32	CSCTI_ITCHINACK	0007 2000 1EDCh
EE0h	32	CSCTI_ITTRIGINACK	0007 2000 1EE0h
EE4h	32	CSCTI_ITCHOUT	0007 2000 1EE4h
EE8h	32	CSCTI_ITTRIGOUT	0007 2000 1EE8h
EECh	32	CSCTI_ITCHOUTACK	0007 2000 1EECh
EF0h	32	CSCTI_ITTRIGOUTACK	0007 2000 1EF0h
EF4h	32	CSCTI_ITCHIN	0007 2000 1EF4h
EF8h	32	CSCTI_ITTRIGIN	0007 2000 1EF8h
F00h	32	CSCTI_ITCTRL	0007 2000 1F00h
FA0h	32	CSCTI_CLAIMSET	0007 2000 1FA0h
FA4h	32	CSCTI_CLAIMCLR	0007 2000 1FA4h
FB0h	32	CSCTI_LOCKACCESS	0007 2000 1FB0h
FB4h	32	CSCTI_LOCKSTATUS	0007 2000 1FB4h

Table 14-14370. CSCTI Registers, Base Address=0007 2000 1000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FB8h	32	CSCTI_AUTHSTATUS	0007 2000 1FB8h
FC8h	32	CSCTI_DEVID	0007 2000 1FC8h
FCCh	32	CSCTI_DEVTYPE	0007 2000 1FCCh
FD0h	32	CSCTI_PERIPHID4	0007 2000 1FD0h
FE0h	32	CSCTI_PERIPHID0	0007 2000 1FE0h
FE4h	32	CSCTI_PERIPHID1	0007 2000 1FE4h
FE8h	32	CSCTI_PERIPHID2	0007 2000 1FE8h
FECh	32	CSCTI_PERIPHID3	0007 2000 1FECh
FF0h	32	CSCTI_COMPONID0	0007 2000 1FF0h
FF4h	32	CSCTI_COMPONID1	0007 2000 1FF4h
FF8h	32	CSCTI_COMPONID2	0007 2000 1FF8h
FFCh	32	CSCTI_COMPONID3	0007 2000 1FFCh

Table 14-14371. DRM_CFG_0 Registers, Base Address=0007 2000 2000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	DRM_CFG_0_PERIPH_ID	0007 2000 2000h
4h	32	DRM_CFG_0_VERSION	0007 2000 2004h
8h	32	DRM_CFG_0_CAPABILITY	0007 2000 2008h
Ch	32	DRM_CFG_0_TRACE_CTRL	0007 2000 200Ch
10h	32	DRM_CFG_0_VBUSM_CTRL	0007 2000 2010h
14h	32	DRM_CFG_0_DAP_TIMEOUT	0007 2000 2014h
18h	32	DRM_CFG_0_CONFIG	0007 2000 2018h
1Ch	32	DRM_CFG_0_EMUTRIGEN	0007 2000 201Ch
20h	32	DRM_CFG_0_BINVALLO	0007 2000 2020h
24h	32	DRM_CFG_0_BINVALHI	0007 2000 2024h
200h	32	DRM_CFG_0_SUSPEND_REG0	0007 2000 2200h
204h	32	DRM_CFG_0_SUSPEND_REG1	0007 2000 2204h
208h	32	DRM_CFG_0_SUSPEND_REG2	0007 2000 2208h
20Ch	32	DRM_CFG_0_SUSPEND_REG3	0007 2000 220Ch
210h	32	DRM_CFG_0_SUSPEND_REG4	0007 2000 2210h
214h	32	DRM_CFG_0_SUSPEND_REG5	0007 2000 2214h
218h	32	DRM_CFG_0_SUSPEND_REG6	0007 2000 2218h
21Ch	32	DRM_CFG_0_SUSPEND_REG7	0007 2000 221Ch
220h	32	DRM_CFG_0_SUSPEND_REG8	0007 2000 2220h
224h	32	DRM_CFG_0_SUSPEND_REG9	0007 2000 2224h
228h	32	DRM_CFG_0_SUSPEND_REG10	0007 2000 2228h
22Ch	32	DRM_CFG_0_SUSPEND_REG11	0007 2000 222Ch
230h	32	DRM_CFG_0_SUSPEND_REG12	0007 2000 2230h
234h	32	DRM_CFG_0_SUSPEND_REG13	0007 2000 2234h
238h	32	DRM_CFG_0_SUSPEND_REG14	0007 2000 2238h
23Ch	32	DRM_CFG_0_SUSPEND_REG15	0007 2000 223Ch
240h	32	DRM_CFG_0_SUSPEND_REG16	0007 2000 2240h
244h	32	DRM_CFG_0_SUSPEND_REG17	0007 2000 2244h
248h	32	DRM_CFG_0_SUSPEND_REG18	0007 2000 2248h
24Ch	32	DRM_CFG_0_SUSPEND_REG19	0007 2000 224Ch
250h	32	DRM_CFG_0_SUSPEND_REG20	0007 2000 2250h

Table 14-14371. DRM_CFG_0 Registers, Base Address=0007 2000 2000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
254h	32	DRM_CFG_0_SUSPEND_REG21	0007 2000 2254h
258h	32	DRM_CFG_0_SUSPEND_REG22	0007 2000 2258h
25Ch	32	DRM_CFG_0_SUSPEND_REG23	0007 2000 225Ch
260h	32	DRM_CFG_0_SUSPEND_REG24	0007 2000 2260h
264h	32	DRM_CFG_0_SUSPEND_REG25	0007 2000 2264h
268h	32	DRM_CFG_0_SUSPEND_REG26	0007 2000 2268h
26Ch	32	DRM_CFG_0_SUSPEND_REG27	0007 2000 226Ch
270h	32	DRM_CFG_0_SUSPEND_REG28	0007 2000 2270h
274h	32	DRM_CFG_0_SUSPEND_REG29	0007 2000 2274h
278h	32	DRM_CFG_0_SUSPEND_REG30	0007 2000 2278h
27Ch	32	DRM_CFG_0_SUSPEND_REG31	0007 2000 227Ch

Table 14-14372. CSTPIU_CFG_0 Registers, Base Address=0007 2000 4000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CSTPIU_CFG_0_SUPPORTSIZE	0007 2000 4000h
4h	32	CSTPIU_CFG_0_CURPORTSIZE	0007 2000 4004h
100h	32	CSTPIU_CFG_0_TRIGMODEREG	0007 2000 4100h
104h	32	CSTPIU_CFG_0_TRIGCTRREG	0007 2000 4104h
108h	32	CSTPIU_CFG_0_TRIGMPYREG	0007 2000 4108h
200h	32	CSTPIU_CFG_0_SUPTESTPAT	0007 2000 4200h
204h	32	CSTPIU_CFG_0_CURTESTPAT	0007 2000 4204h
208h	32	CSTPIU_CFG_0_TESTPATCNT	0007 2000 4208h
300h	32	CSTPIU_CFG_0_FORMFLUSHSTAT	0007 2000 4300h
304h	32	CSTPIU_CFG_0_FORMFLUSHCTL	0007 2000 4304h
308h	32	CSTPIU_CFG_0_FORMSYNCCTR	0007 2000 4308h
400h	32	CSTPIU_CFG_0_EXTCTLIN	0007 2000 4400h
404h	32	CSTPIU_CFG_0_EXTCTLOUT	0007 2000 4404h
EE4h	32	CSTPIU_CFG_0_ITTRFLINACK	0007 2000 4EE4h
EE8h	32	CSTPIU_CFG_0_ITTRFLIN	0007 2000 4EE8h
EECh	32	CSTPIU_CFG_0_ITATBDATA0	0007 2000 4EECh
EF0h	32	CSTPIU_CFG_0_ITATBCTR2	0007 2000 4EF0h
EF4h	32	CSTPIU_CFG_0_ITATBCTR1	0007 2000 4EF4h
EF8h	32	CSTPIU_CFG_0_ITATBCTR0	0007 2000 4EF8h
F00h	32	CSTPIU_CFG_0_INTCTRL	0007 2000 4F00h
FA0h	32	CSTPIU_CFG_0_CTSET	0007 2000 4FA0h
FA4h	32	CSTPIU_CFG_0_CTCLR	0007 2000 4FA4h
FB0h	32	CSTPIU_CFG_0_LAREG	0007 2000 4FB0h
FB4h	32	CSTPIU_CFG_0_LSREG	0007 2000 4FB4h
FB8h	32	CSTPIU_CFG_0_AUTHST	0007 2000 4FB8h
FC8h	32	CSTPIU_CFG_0_DEVID	0007 2000 4FC8h
FCCh	32	CSTPIU_CFG_0_DEVTYPE	0007 2000 4FCCh
FD0h	32	CSTPIU_CFG_0_PERID4	0007 2000 4FD0h
FE0h	32	CSTPIU_CFG_0_PERID0	0007 2000 4FE0h
FE4h	32	CSTPIU_CFG_0_PERID1	0007 2000 4FE4h
FE8h	32	CSTPIU_CFG_0_PERID2	0007 2000 4FE8h
FECh	32	CSTPIU_CFG_0_PERID3	0007 2000 4FECh

Table 14-14372. CSTPIU_CFG_0 Registers, Base Address=0007 2000 4000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FF0h	32	CSTPIU_CFG_0_COMPID0	0007 2000 4FF0h
FF4h	32	CSTPIU_CFG_0_COMPID1	0007 2000 4FF4h
FF8h	32	CSTPIU_CFG_0_COMPID2	0007 2000 4FF8h
FFCh	32	CSTPIU_CFG_0_COMPID3	0007 2000 4FFCh

Table 14-14373. CTF_CFG_0 Registers, Base Address=0007 2000 5000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CTF_CFG_0_CSTFCTLREG	0007 2000 5000h
4h	32	CTF_CFG_0_PRIORCTLREG	0007 2000 5004h
EECh	32	CTF_CFG_0_ITATBDATA0	0007 2000 5EECh
EF0h	32	CTF_CFG_0_ITATBCTR2	0007 2000 5EF0h
EF4h	32	CTF_CFG_0_ITATBCTR1	0007 2000 5EF4h
EF8h	32	CTF_CFG_0_ITATBCTR0	0007 2000 5EF8h
F00h	32	CTF_CFG_0_INTCTRL	0007 2000 5F00h
FA0h	32	CTF_CFG_0_CTSET	0007 2000 5FA0h
FA4h	32	CTF_CFG_0_CTCLR	0007 2000 5FA4h
FB0h	32	CTF_CFG_0_LAREG	0007 2000 5FB0h
FB4h	32	CTF_CFG_0_LSREG	0007 2000 5FB4h
FB8h	32	CTF_CFG_0_AUTHST	0007 2000 5FB8h
FC8h	32	CTF_CFG_0_DEVID	0007 2000 5FC8h
FCCh	32	CTF_CFG_0_DEVTYPEID	0007 2000 5FCCh
FD0h	32	CTF_CFG_0_PERID4	0007 2000 5FD0h
FD4h	32	CTF_CFG_0_PERID5	0007 2000 5FD4h
FD8h	32	CTF_CFG_0_PERID6	0007 2000 5FD8h
FDCh	32	CTF_CFG_0_PERID7	0007 2000 5FDCh
FE0h	32	CTF_CFG_0_PERID0	0007 2000 5FE0h
FE4h	32	CTF_CFG_0_PERID1	0007 2000 5FE4h
FE8h	32	CTF_CFG_0_PERID2	0007 2000 5FE8h
FECh	32	CTF_CFG_0_PERID3	0007 2000 5FECh
FF0h	32	CTF_CFG_0_COMPID0	0007 2000 5FF0h
FF4h	32	CTF_CFG_0_COMPID1	0007 2000 5FF4h
FF8h	32	CTF_CFG_0_COMPID2	0007 2000 5FF8h
FFCh	32	CTF_CFG_0_COMPID3	0007 2000 5FFCh

Table 14-14374. ROM_TABLE_0_1 Registers, Base Address=0007 4000 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	ROM_TABLE_0_1_ROM_ENTRY0	0007 4000 0000h
4h	32	ROM_TABLE_0_1_ROM_ENTRY1	0007 4000 0004h
8h	32	ROM_TABLE_0_1_ROM_ENTRY2	0007 4000 0008h
8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY0	0007 4000 0008h
Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY1	0007 4000 000Ch
10h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY2	0007 4000 0010h
14h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY3	0007 4000 0014h
18h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY4	0007 4000 0018h
1Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY5	0007 4000 001Ch
20h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY6	0007 4000 0020h

Table 14-14374. ROM_TABLE_0_1 Registers, Base Address=0007 4000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
24h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY7	0007 4000 0024h
28h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY8	0007 4000 0028h
2Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY9	0007 4000 002Ch
30h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY10	0007 4000 0030h
34h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY11	0007 4000 0034h
38h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY12	0007 4000 0038h
3Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY13	0007 4000 003Ch
40h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY14	0007 4000 0040h
44h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY15	0007 4000 0044h
48h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY16	0007 4000 0048h
4Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY17	0007 4000 004Ch
50h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY18	0007 4000 0050h
54h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY19	0007 4000 0054h
58h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY20	0007 4000 0058h
5Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY21	0007 4000 005Ch
60h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY22	0007 4000 0060h
64h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY23	0007 4000 0064h
68h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY24	0007 4000 0068h
6Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY25	0007 4000 006Ch
70h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY26	0007 4000 0070h
74h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY27	0007 4000 0074h
78h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY28	0007 4000 0078h
7Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY29	0007 4000 007Ch
80h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY30	0007 4000 0080h
84h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY31	0007 4000 0084h
88h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY32	0007 4000 0088h
8Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY33	0007 4000 008Ch
90h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY34	0007 4000 0090h
94h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY35	0007 4000 0094h
98h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY36	0007 4000 0098h
9Ch	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY37	0007 4000 009Ch
A0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY38	0007 4000 00A0h
A4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY39	0007 4000 00A4h
A8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY40	0007 4000 00A8h
ACh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY41	0007 4000 00ACh
B0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY42	0007 4000 00B0h
B4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY43	0007 4000 00B4h
B8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY44	0007 4000 00B8h
BCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY45	0007 4000 00BCh
C0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY46	0007 4000 00C0h
C4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY47	0007 4000 00C4h
C8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY48	0007 4000 00C8h
CCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY49	0007 4000 00CCh
D0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY50	0007 4000 00D0h
D4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY51	0007 4000 00D4h
D8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY52	0007 4000 00D8h
DCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY53	0007 4000 00DCh

Table 14-14374. ROM_TABLE_0_1 Registers, Base Address=0007 4000 0000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
E0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY54	0007 4000 00E0h
E4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY55	0007 4000 00E4h
E8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY56	0007 4000 00E8h
ECh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY57	0007 4000 00ECh
F0h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY58	0007 4000 00F0h
F4h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY59	0007 4000 00F4h
F8h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY60	0007 4000 00F8h
FCh	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY61	0007 4000 00FCh
100h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY62	0007 4000 0100h
104h	32	ROM_TABLE_0_1_ROM_MANUAL_ENTRY63	0007 4000 0104h
108h	32	ROM_TABLE_0_1_PERIPHID0	0007 4000 0108h
10Ch	32	ROM_TABLE_0_1_PERIPHID1	0007 4000 010Ch
110h	32	ROM_TABLE_0_1_PERIPHID2	0007 4000 0110h
114h	32	ROM_TABLE_0_1_PERIPHID3	0007 4000 0114h
118h	32	ROM_TABLE_0_1_PERIPHID4	0007 4000 0118h
3FCh	32	ROM_TABLE_0_1_COMPID0	0007 4000 03FCh
3FCh	32	ROM_TABLE_0_1_COMPID1	0007 4000 03FCh
3FCh	32	ROM_TABLE_0_1_COMPID2	0007 4000 03FCh
3FCh	32	ROM_TABLE_0_1_COMPID3	0007 4000 03FCh

Table 14-14375. CFGAP_CFG_1 Registers, Base Address=0007 4000 2000h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CFGAP_CFG_1_JTAGID_REG	0007 4000 2000h
4h	32	CFGAP_CFG_1_USERID_REG	0007 4000 2004h
8h	32	CFGAP_CFG_1_VERSION_REG	0007 4000 2008h
FCh	32	CFGAP_CFG_1_APID_REGISTER	0007 4000 20FCh

Table 14-14376. APBAP_CFG_1 Registers, Base Address=0007 4000 2100h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	APBAP_CFG_1_CSWREG	0007 4000 2100h
Ch	32	APBAP_CFG_1_DRWREG	0007 4000 210Ch
10h	32	APBAP_CFG_1_BD0REG	0007 4000 2110h
14h	32	APBAP_CFG_1_BD1REG	0007 4000 2114h
18h	32	APBAP_CFG_1_BD2REG	0007 4000 2118h
1Ch	32	APBAP_CFG_1_BD3REG	0007 4000 211Ch
F8h	32	APBAP_CFG_1_ROM_REGISTER	0007 4000 21F8h
FCh	32	APBAP_CFG_1_ID_REGISTER	0007 4000 21FCh

Table 14-14377. AXIAP_CFG_1 Registers, Base Address=0007 4000 2200h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	AXIAP_CFG_1_CSWREG	0007 4000 2200h
Ch	32	AXIAP_CFG_1_DRWREG	0007 4000 220Ch
10h	32	AXIAP_CFG_1_BD0REG	0007 4000 2210h
14h	32	AXIAP_CFG_1_BD1REG	0007 4000 2214h
18h	32	AXIAP_CFG_1_BD2REG	0007 4000 2218h

Table 14-14377. AXIAP_CFG_1 Registers, Base Address=0007 4000 2200h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
1Ch	32	AXIAP_CFG_1_BD3REG	0007 4000 221Ch
20h	32	AXIAP_CFG_1_MBT_REGISTER	0007 4000 2220h
F0h	32	AXIAP_CFG_1_ROM_HI_REGISTER	0007 4000 22F0h
F4h	32	AXIAP_CFG_1_CFG_REGISTER	0007 4000 22F4h
F8h	32	AXIAP_CFG_1_ROM_LO_REGISTER	0007 4000 22F8h
FCh	32	AXIAP_CFG_1_ID_REGISTER	0007 4000 22FCh

Table 14-14378. PWRAP_CFG_1 Registers, Base Address=0007 4000 2300h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FCh	32	PWRAP_CFG_1_ID_REGISTER	0007 4000 23FCh

Table 14-14379. PVIEW_CFG_1 Registers, Base Address=0007 4000 2400h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	PVIEW_CFG_1_PVIEW_STATE0	0007 4000 2400h
F0h	32	PVIEW_CFG_1_PVIEW_CAPABILITY	0007 4000 24F0h
FCh	32	PVIEW_CFG_1_ID_REGISTER	0007 4000 24FCh

Table 14-14380. JTAGAP_CFG_1 Registers, Base Address=0007 4000 2500h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	JTAGAP_CFG_1_CSW	0007 4000 2500h
4h	32	JTAGAP_CFG_1_PSEL_REG	0007 4000 2504h
8h	32	JTAGAP_CFG_1_PSTA_REG	0007 4000 2508h
10h	32	JTAGAP_CFG_1_BYTEFIFO1	0007 4000 2510h
14h	32	JTAGAP_CFG_1_BYTEFIFO2	0007 4000 2514h
18h	32	JTAGAP_CFG_1_BYTEFIFO3	0007 4000 2518h
1Ch	32	JTAGAP_CFG_1_BYTEFIFO4	0007 4000 251Ch
FCh	32	JTAGAP_CFG_1_ID_REGISTER	0007 4000 25FCh

Table 14-14381. SECAP_CFG_1 Registers, Base Address=0007 4000 2600h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	SECAP_CFG_1_TXDATA	0007 4000 2600h
4h	32	SECAP_CFG_1_TXCTRL	0007 4000 2604h
8h	32	SECAP_CFG_1_RXDATA	0007 4000 2608h
Ch	32	SECAP_CFG_1_RXCTRL	0007 4000 260Ch

Table 14-14382. CORTEX0_CFG_1 Registers, Base Address=0007 4000 2700h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX0_CFG_1_CSWREG	0007 4000 2700h
Ch	32	CORTEX0_CFG_1_DRWREG	0007 4000 270Ch
10h	32	CORTEX0_CFG_1_BD0REG	0007 4000 2710h
14h	32	CORTEX0_CFG_1_BD1REG	0007 4000 2714h
18h	32	CORTEX0_CFG_1_BD2REG	0007 4000 2718h
1Ch	32	CORTEX0_CFG_1_BD3REG	0007 4000 271Ch
F8h	32	CORTEX0_CFG_1_ROM_REGISTER	0007 4000 27F8h

Table 14-14382. CORTEX0_CFG_1 Registers, Base Address=0007 4000 2700h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FCh	32	CORTEX0_CFG_1_ID_REGISTER	0007 4000 27FCh

Table 14-14383. CORTEX1_CFG_1 Registers, Base Address=0007 4000 2800h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX1_CFG_1_CSWREG	0007 4000 2800h
Ch	32	CORTEX1_CFG_1_DRWREG	0007 4000 280Ch
10h	32	CORTEX1_CFG_1_BD0REG	0007 4000 2810h
14h	32	CORTEX1_CFG_1_BD1REG	0007 4000 2814h
18h	32	CORTEX1_CFG_1_BD2REG	0007 4000 2818h
1Ch	32	CORTEX1_CFG_1_BD3REG	0007 4000 281Ch
F8h	32	CORTEX1_CFG_1_ROM_REGISTER	0007 4000 28F8h
FCh	32	CORTEX1_CFG_1_ID_REGISTER	0007 4000 28FCh

Table 14-14384. CORTEX2_CFG_1 Registers, Base Address=0007 4000 2900h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX2_CFG_1_CSWREG	0007 4000 2900h
Ch	32	CORTEX2_CFG_1_DRWREG	0007 4000 290Ch
10h	32	CORTEX2_CFG_1_BD0REG	0007 4000 2910h
14h	32	CORTEX2_CFG_1_BD1REG	0007 4000 2914h
18h	32	CORTEX2_CFG_1_BD2REG	0007 4000 2918h
1Ch	32	CORTEX2_CFG_1_BD3REG	0007 4000 291Ch
F8h	32	CORTEX2_CFG_1_ROM_REGISTER	0007 4000 29F8h
FCh	32	CORTEX2_CFG_1_ID_REGISTER	0007 4000 29FCh

Table 14-14385. CORTEX3_CFG_1 Registers, Base Address=0007 4000 2A00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX3_CFG_1_CSWREG	0007 4000 2A00h
Ch	32	CORTEX3_CFG_1_DRWREG	0007 4000 2A0Ch
10h	32	CORTEX3_CFG_1_BD0REG	0007 4000 2A10h
14h	32	CORTEX3_CFG_1_BD1REG	0007 4000 2A14h
18h	32	CORTEX3_CFG_1_BD2REG	0007 4000 2A18h
1Ch	32	CORTEX3_CFG_1_BD3REG	0007 4000 2A1Ch
F8h	32	CORTEX3_CFG_1_ROM_REGISTER	0007 4000 2AF8h
FCh	32	CORTEX3_CFG_1_ID_REGISTER	0007 4000 2AFCh

Table 14-14386. CORTEX4_CFG_1 Registers, Base Address=0007 4000 2B00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX4_CFG_1_CSWREG	0007 4000 2B00h
Ch	32	CORTEX4_CFG_1_DRWREG	0007 4000 2B0Ch
10h	32	CORTEX4_CFG_1_BD0REG	0007 4000 2B10h
14h	32	CORTEX4_CFG_1_BD1REG	0007 4000 2B14h
18h	32	CORTEX4_CFG_1_BD2REG	0007 4000 2B18h
1Ch	32	CORTEX4_CFG_1_BD3REG	0007 4000 2B1Ch
F8h	32	CORTEX4_CFG_1_ROM_REGISTER	0007 4000 2BF8h

Table 14-14386. CORTEX4_CFG_1 Registers, Base Address=0007 4000 2B00h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FCh	32	CORTEX4_CFG_1_ID_REGISTER	0007 4000 2BFCh

Table 14-14387. CORTEX5_CFG_1 Registers, Base Address=0007 4000 2C00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX5_CFG_1_CSWREG	0007 4000 2C00h
Ch	32	CORTEX5_CFG_1_DRWREG	0007 4000 2C0Ch
10h	32	CORTEX5_CFG_1_BD0REG	0007 4000 2C10h
14h	32	CORTEX5_CFG_1_BD1REG	0007 4000 2C14h
18h	32	CORTEX5_CFG_1_BD2REG	0007 4000 2C18h
1Ch	32	CORTEX5_CFG_1_BD3REG	0007 4000 2C1Ch
F8h	32	CORTEX5_CFG_1_ROM_REGISTER	0007 4000 2CF8h
FCh	32	CORTEX5_CFG_1_ID_REGISTER	0007 4000 2CFCh

Table 14-14388. CORTEX6_CFG_1 Registers, Base Address=0007 4000 2D00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX6_CFG_1_CSWREG	0007 4000 2D00h
Ch	32	CORTEX6_CFG_1_DRWREG	0007 4000 2D0Ch
10h	32	CORTEX6_CFG_1_BD0REG	0007 4000 2D10h
14h	32	CORTEX6_CFG_1_BD1REG	0007 4000 2D14h
18h	32	CORTEX6_CFG_1_BD2REG	0007 4000 2D18h
1Ch	32	CORTEX6_CFG_1_BD3REG	0007 4000 2D1Ch
F8h	32	CORTEX6_CFG_1_ROM_REGISTER	0007 4000 2DF8h
FCh	32	CORTEX6_CFG_1_ID_REGISTER	0007 4000 2DFCh

Table 14-14389. CORTEX7_CFG_1 Registers, Base Address=0007 4000 2E00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX7_CFG_1_CSWREG	0007 4000 2E00h
Ch	32	CORTEX7_CFG_1_DRWREG	0007 4000 2E0Ch
10h	32	CORTEX7_CFG_1_BD0REG	0007 4000 2E10h
14h	32	CORTEX7_CFG_1_BD1REG	0007 4000 2E14h
18h	32	CORTEX7_CFG_1_BD2REG	0007 4000 2E18h
1Ch	32	CORTEX7_CFG_1_BD3REG	0007 4000 2E1Ch
F8h	32	CORTEX7_CFG_1_ROM_REGISTER	0007 4000 2EF8h
FCh	32	CORTEX7_CFG_1_ID_REGISTER	0007 4000 2EFCh

Table 14-14390. CORTEX8_CFG_1 Registers, Base Address=0007 4000 2F00h, Length=256

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CORTEX8_CFG_1_CSWREG	0007 4000 2F00h
Ch	32	CORTEX8_CFG_1_DRWREG	0007 4000 2F0Ch
10h	32	CORTEX8_CFG_1_BD0REG	0007 4000 2F10h
14h	32	CORTEX8_CFG_1_BD1REG	0007 4000 2F14h
18h	32	CORTEX8_CFG_1_BD2REG	0007 4000 2F18h
1Ch	32	CORTEX8_CFG_1_BD3REG	0007 4000 2F1Ch
F8h	32	CORTEX8_CFG_1_ROM_REGISTER	0007 4000 2FF8h

Table 14-14390. CORTEX8_CFG_1 Registers, Base Address=0007 4000 2F00h, Length=256 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FCh	32	CORTEX8_CFG_1_ID_REGISTER	0007 4000 2FFCh

Table 14-14391. ROM_TABLE_1_1 Registers, Base Address=0007 6000 0000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	ROM_TABLE_1_1_ROM_ENTRY0	0007 6000 0000h
4h	32	ROM_TABLE_1_1_ROM_ENTRY1	0007 6000 0004h
8h	32	ROM_TABLE_1_1_ROM_ENTRY2	0007 6000 0008h
Ch	32	ROM_TABLE_1_1_ROM_ENTRY3	0007 6000 000Ch
10h	32	ROM_TABLE_1_1_ROM_ENTRY4	0007 6000 0010h
14h	32	ROM_TABLE_1_1_ROM_ENTRY5	0007 6000 0014h
18h	32	ROM_TABLE_1_1_COMPUTE_CLUSTER0	0007 6000 0018h
1Ch	32	ROM_TABLE_1_1_COMPUTE_CLUSTER1	0007 6000 001Ch
20h	32	ROM_TABLE_1_1_COMPUTE_CLUSTER2	0007 6000 0020h
24h	32	ROM_TABLE_1_1_DEBUG_CELL0	0007 6000 0024h
28h	32	ROM_TABLE_1_1_DEBUG_CELL1	0007 6000 0028h
2Ch	32	ROM_TABLE_1_1_DEBUG_CELL2	0007 6000 002Ch
30h	32	ROM_TABLE_1_1_DEBUG_CELL3	0007 6000 0030h
34h	32	ROM_TABLE_1_1_DEBUG_CELL4	0007 6000 0034h
38h	32	ROM_TABLE_1_1_DEBUG_CELL5	0007 6000 0038h
3Ch	32	ROM_TABLE_1_1_DEBUG_CELL6	0007 6000 003Ch
40h	32	ROM_TABLE_1_1_DEBUG_CELL7	0007 6000 0040h
44h	32	ROM_TABLE_1_1_DEBUG_CELL8	0007 6000 0044h
48h	32	ROM_TABLE_1_1_DEBUG_CELL9	0007 6000 0048h
4Ch	32	ROM_TABLE_1_1_DEBUG_CELL10	0007 6000 004Ch
50h	32	ROM_TABLE_1_1_DEBUG_CELL11	0007 6000 0050h
50h	32	ROM_TABLE_1_1_EXTCSCOMP0	0007 6000 0050h
54h	32	ROM_TABLE_1_1_EXTCSCOMP1	0007 6000 0054h
58h	32	ROM_TABLE_1_1_EXTCSCOMP2	0007 6000 0058h
5Ch	32	ROM_TABLE_1_1_EXTCSCOMP3	0007 6000 005Ch
60h	32	ROM_TABLE_1_1_EXTCSCOMP4	0007 6000 0060h
64h	32	ROM_TABLE_1_1_EXTCSCOMP5	0007 6000 0064h
68h	32	ROM_TABLE_1_1_EXTCSCOMP6	0007 6000 0068h
6Ch	32	ROM_TABLE_1_1_EXTCSCOMP7	0007 6000 006Ch
70h	32	ROM_TABLE_1_1_EXTCSCOMP8	0007 6000 0070h
74h	32	ROM_TABLE_1_1_EXTCSCOMP9	0007 6000 0074h
78h	32	ROM_TABLE_1_1_EXTCSCOMP10	0007 6000 0078h
7Ch	32	ROM_TABLE_1_1_EXTCSCOMP11	0007 6000 007Ch

Table 14-14392. CSCTI Registers, Base Address=0007 6000 1000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CSCTI_CTICONTROL	0007 6000 1000h
10h	32	CSCTI_CTIINTACK	0007 6000 1010h
14h	32	CSCTI_CTIAPPSET	0007 6000 1014h
18h	32	CSCTI_CTIAPPCLR	0007 6000 1018h
1Ch	32	CSCTI_CTIAPPPULSE	0007 6000 101Ch
20h	32	CSCTI_CTIINEN0	0007 6000 1020h

Table 14-14392. CSCTI Registers, Base Address=0007 6000 1000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
24h	32	CSCTI_CTIINEN1	0007 6000 1024h
28h	32	CSCTI_CTIINEN2	0007 6000 1028h
2Ch	32	CSCTI_CTIINEN3	0007 6000 102Ch
30h	32	CSCTI_CTIINEN4	0007 6000 1030h
34h	32	CSCTI_CTIINEN5	0007 6000 1034h
38h	32	CSCTI_CTIINEN6	0007 6000 1038h
3Ch	32	CSCTI_CTIINEN7	0007 6000 103Ch
A0h	32	CSCTI_CTIOUTEN0	0007 6000 10A0h
A4h	32	CSCTI_CTIOUTEN1	0007 6000 10A4h
A8h	32	CSCTI_CTIOUTEN2	0007 6000 10A8h
ACh	32	CSCTI_CTIOUTEN3	0007 6000 10ACh
B0h	32	CSCTI_CTIOUTEN4	0007 6000 10B0h
B4h	32	CSCTI_CTIOUTEN5	0007 6000 10B4h
B8h	32	CSCTI_CTIOUTEN6	0007 6000 10B8h
BCh	32	CSCTI_CTIOUTEN7	0007 6000 10BCh
130h	32	CSCTI_CTITRIGINSTATUS	0007 6000 1130h
134h	32	CSCTI_CTITRIGOUTSTATUS	0007 6000 1134h
138h	32	CSCTI_CTICHINSTATUS	0007 6000 1138h
13Ch	32	CSCTI_CTICHOUTSTATUS	0007 6000 113Ch
140h	32	CSCTI_CTIGATE	0007 6000 1140h
144h	32	CSCTI_ASICCTL	0007 6000 1144h
EDCh	32	CSCTI_ITCHINACK	0007 6000 1EDCh
EE0h	32	CSCTI_ITTRIGINACK	0007 6000 1EE0h
EE4h	32	CSCTI_ITCHOUT	0007 6000 1EE4h
EE8h	32	CSCTI_ITTRIGOUT	0007 6000 1EE8h
EECh	32	CSCTI_ITCHOUTACK	0007 6000 1EECh
EF0h	32	CSCTI_ITTRIGOUTACK	0007 6000 1EF0h
EF4h	32	CSCTI_ITCHIN	0007 6000 1EF4h
EF8h	32	CSCTI_ITTRIGIN	0007 6000 1EF8h
F00h	32	CSCTI_ITCTRL	0007 6000 1F00h
FA0h	32	CSCTI_CLAIMSET	0007 6000 1FA0h
FA4h	32	CSCTI_CLAIMCLR	0007 6000 1FA4h
FB0h	32	CSCTI_LOCKACCESS	0007 6000 1FB0h
FB4h	32	CSCTI_LOCKSTATUS	0007 6000 1FB4h
FB8h	32	CSCTI_AUTHSTATUS	0007 6000 1FB8h
FC8h	32	CSCTI_DEVID	0007 6000 1FC8h
FCCh	32	CSCTI_DEVTYPE	0007 6000 1FCCh
FD0h	32	CSCTI_PERIPHID4	0007 6000 1FD0h
FE0h	32	CSCTI_PERIPHID0	0007 6000 1FE0h
FE4h	32	CSCTI_PERIPHID1	0007 6000 1FE4h
FE8h	32	CSCTI_PERIPHID2	0007 6000 1FE8h
FECh	32	CSCTI_PERIPHID3	0007 6000 1FECh
FF0h	32	CSCTI_COMPONID0	0007 6000 1FF0h
FF4h	32	CSCTI_COMPONID1	0007 6000 1FF4h
FF8h	32	CSCTI_COMPONID2	0007 6000 1FF8h
FFCh	32	CSCTI_COMPONID3	0007 6000 1FFCh

Table 14-14393. DRM_CFG_1 Registers, Base Address=0007 6000 2000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	DRM_CFG_1_PERIPH_ID	0007 6000 2000h
4h	32	DRM_CFG_1_VERSION	0007 6000 2004h
8h	32	DRM_CFG_1_CAPABILITY	0007 6000 2008h
Ch	32	DRM_CFG_1_TRACE_CTRL	0007 6000 200Ch
10h	32	DRM_CFG_1_VBUSM_CTRL	0007 6000 2010h
14h	32	DRM_CFG_1_DAP_TIMEOUT	0007 6000 2014h
18h	32	DRM_CFG_1_CONFIG	0007 6000 2018h
1Ch	32	DRM_CFG_1_EMUTRIGEN	0007 6000 201Ch
20h	32	DRM_CFG_1_BINVALLO	0007 6000 2020h
24h	32	DRM_CFG_1_BINVALHI	0007 6000 2024h
200h	32	DRM_CFG_1_SUSPEND_REG0	0007 6000 2200h
204h	32	DRM_CFG_1_SUSPEND_REG1	0007 6000 2204h
208h	32	DRM_CFG_1_SUSPEND_REG2	0007 6000 2208h
20Ch	32	DRM_CFG_1_SUSPEND_REG3	0007 6000 220Ch
210h	32	DRM_CFG_1_SUSPEND_REG4	0007 6000 2210h
214h	32	DRM_CFG_1_SUSPEND_REG5	0007 6000 2214h
218h	32	DRM_CFG_1_SUSPEND_REG6	0007 6000 2218h
21Ch	32	DRM_CFG_1_SUSPEND_REG7	0007 6000 221Ch
220h	32	DRM_CFG_1_SUSPEND_REG8	0007 6000 2220h
224h	32	DRM_CFG_1_SUSPEND_REG9	0007 6000 2224h
228h	32	DRM_CFG_1_SUSPEND_REG10	0007 6000 2228h
22Ch	32	DRM_CFG_1_SUSPEND_REG11	0007 6000 222Ch
230h	32	DRM_CFG_1_SUSPEND_REG12	0007 6000 2230h
234h	32	DRM_CFG_1_SUSPEND_REG13	0007 6000 2234h
238h	32	DRM_CFG_1_SUSPEND_REG14	0007 6000 2238h
23Ch	32	DRM_CFG_1_SUSPEND_REG15	0007 6000 223Ch
240h	32	DRM_CFG_1_SUSPEND_REG16	0007 6000 2240h
244h	32	DRM_CFG_1_SUSPEND_REG17	0007 6000 2244h
248h	32	DRM_CFG_1_SUSPEND_REG18	0007 6000 2248h
24Ch	32	DRM_CFG_1_SUSPEND_REG19	0007 6000 224Ch
250h	32	DRM_CFG_1_SUSPEND_REG20	0007 6000 2250h
254h	32	DRM_CFG_1_SUSPEND_REG21	0007 6000 2254h
258h	32	DRM_CFG_1_SUSPEND_REG22	0007 6000 2258h
25Ch	32	DRM_CFG_1_SUSPEND_REG23	0007 6000 225Ch
260h	32	DRM_CFG_1_SUSPEND_REG24	0007 6000 2260h
264h	32	DRM_CFG_1_SUSPEND_REG25	0007 6000 2264h
268h	32	DRM_CFG_1_SUSPEND_REG26	0007 6000 2268h
26Ch	32	DRM_CFG_1_SUSPEND_REG27	0007 6000 226Ch
270h	32	DRM_CFG_1_SUSPEND_REG28	0007 6000 2270h
274h	32	DRM_CFG_1_SUSPEND_REG29	0007 6000 2274h
278h	32	DRM_CFG_1_SUSPEND_REG30	0007 6000 2278h
27Ch	32	DRM_CFG_1_SUSPEND_REG31	0007 6000 227Ch

Table 14-14394. CSTPIU_CFG_1 Registers, Base Address=0007 6000 4000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CSTPIU_CFG_1_SUPPORTSIZE	0007 6000 4000h
4h	32	CSTPIU_CFG_1_CURPORTSIZE	0007 6000 4004h
100h	32	CSTPIU_CFG_1_TRIGMODEREG	0007 6000 4100h
104h	32	CSTPIU_CFG_1_TRIGCTRREG	0007 6000 4104h
108h	32	CSTPIU_CFG_1_TRIGMPYREG	0007 6000 4108h
200h	32	CSTPIU_CFG_1_SUPTESTPAT	0007 6000 4200h
204h	32	CSTPIU_CFG_1_CURTESTPAT	0007 6000 4204h
208h	32	CSTPIU_CFG_1_TESTPATCNT	0007 6000 4208h
300h	32	CSTPIU_CFG_1_FORMFLUSHSTAT	0007 6000 4300h
304h	32	CSTPIU_CFG_1_FORMFLUSHCTL	0007 6000 4304h
308h	32	CSTPIU_CFG_1_FORMSYNCCTR	0007 6000 4308h
400h	32	CSTPIU_CFG_1_EXTCTLIN	0007 6000 4400h
404h	32	CSTPIU_CFG_1_EXTCTLOUT	0007 6000 4404h
EE4h	32	CSTPIU_CFG_1_ITTRFLINACK	0007 6000 4EE4h
EE8h	32	CSTPIU_CFG_1_ITTRFLIN	0007 6000 4EE8h
EECh	32	CSTPIU_CFG_1_ITATBDATA0	0007 6000 4EECh
EF0h	32	CSTPIU_CFG_1_ITATBCTR2	0007 6000 4EF0h
EF4h	32	CSTPIU_CFG_1_ITATBCTR1	0007 6000 4EF4h
EF8h	32	CSTPIU_CFG_1_ITATBCTR0	0007 6000 4EF8h
F00h	32	CSTPIU_CFG_1_INTCTRL	0007 6000 4F00h
FA0h	32	CSTPIU_CFG_1_CTSET	0007 6000 4FA0h
FA4h	32	CSTPIU_CFG_1_CTCLR	0007 6000 4FA4h
FB0h	32	CSTPIU_CFG_1_LAREG	0007 6000 4FB0h
FB4h	32	CSTPIU_CFG_1_LSREG	0007 6000 4FB4h
FB8h	32	CSTPIU_CFG_1_AUTHST	0007 6000 4FB8h
FC8h	32	CSTPIU_CFG_1_DEVID	0007 6000 4FC8h
FCCh	32	CSTPIU_CFG_1_DEVTYPE	0007 6000 4FCCh
FD0h	32	CSTPIU_CFG_1_PERID4	0007 6000 4FD0h
FE0h	32	CSTPIU_CFG_1_PERID0	0007 6000 4FE0h
FE4h	32	CSTPIU_CFG_1_PERID1	0007 6000 4FE4h
FE8h	32	CSTPIU_CFG_1_PERID2	0007 6000 4FE8h
FECh	32	CSTPIU_CFG_1_PERID3	0007 6000 4FECh
FF0h	32	CSTPIU_CFG_1_COMPID0	0007 6000 4FF0h
FF4h	32	CSTPIU_CFG_1_COMPID1	0007 6000 4FF4h
FF8h	32	CSTPIU_CFG_1_COMPID2	0007 6000 4FF8h
FFCh	32	CSTPIU_CFG_1_COMPID3	0007 6000 4FFCh

Table 14-14395. CTF_CFG_1 Registers, Base Address=0007 6000 5000h, Length=4096

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
0h	32	CTF_CFG_1_CSTFCTLREG	0007 6000 5000h
4h	32	CTF_CFG_1_PRIORCTLREG	0007 6000 5004h
EECh	32	CTF_CFG_1_ITATBDATA0	0007 6000 5EECh
EF0h	32	CTF_CFG_1_ITATBCTR2	0007 6000 5EF0h
EF4h	32	CTF_CFG_1_ITATBCTR1	0007 6000 5EF4h
EF8h	32	CTF_CFG_1_ITATBCTR0	0007 6000 5EF8h
F00h	32	CTF_CFG_1_INTCTRL	0007 6000 5F00h

Table 14-14395. CTF_CFG_1 Registers, Base Address=0007 6000 5000h, Length=4096 (continued)

Offset	Length	Register Name	DEBUGSS_WRAP0 Physical Address
FA0h	32	CTF_CFG_1_CTSET	0007 6000 5FA0h
FA4h	32	CTF_CFG_1_CTCLR	0007 6000 5FA4h
FB0h	32	CTF_CFG_1_LAREG	0007 6000 5FB0h
FB4h	32	CTF_CFG_1_LSREG	0007 6000 5FB4h
FB8h	32	CTF_CFG_1_AUTHST	0007 6000 5FB8h
FC8h	32	CTF_CFG_1_DEVID	0007 6000 5FC8h
FCCh	32	CTF_CFG_1_DEVTYPEID	0007 6000 5FCCh
FD0h	32	CTF_CFG_1_PERID4	0007 6000 5FD0h
FD4h	32	CTF_CFG_1_PERID5	0007 6000 5FD4h
FD8h	32	CTF_CFG_1_PERID6	0007 6000 5FD8h
FDCh	32	CTF_CFG_1_PERID7	0007 6000 5FDCh
FE0h	32	CTF_CFG_1_PERID0	0007 6000 5FE0h
FE4h	32	CTF_CFG_1_PERID1	0007 6000 5FE4h
FE8h	32	CTF_CFG_1_PERID2	0007 6000 5FE8h
FECh	32	CTF_CFG_1_PERID3	0007 6000 5FECh
FF0h	32	CTF_CFG_1_COMPID0	0007 6000 5FF0h
FF4h	32	CTF_CFG_1_COMPID1	0007 6000 5FF4h
FF8h	32	CTF_CFG_1_COMPID2	0007 6000 5FF8h
FFCh	32	CTF_CFG_1_COMPID3	0007 6000 5FFCh

14.8.1.2 DEBUGSS_WRAP Registers

DEBUGSS_WRAP Registers

14.8.1.2.1 ROM_TABLE_0_0_ROM_ENTRY0 Register

14.8.1.2.1.1 ROM_TABLE_0_0_ROM_ENTRY0 Register (Offset = 0h) [reset = 2003h]

rom table entry 0

Return to Summary Table

Table 14-14396. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0000h

Figure 14-7072. ROM_TABLE_0_0_ROM_ENTRY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">2h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">2h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-14397. ROM_TABLE_0_0_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.2 ROM_TABLE_0_0_ROM_ENTRY1 Register

14.8.1.2.2.1 ROM_TABLE_0_0_ROM_ENTRY1 Register (Offset = 4h) [reset = 2000003h]

rom table entry 1

Return to Summary Table

Table 14-14398. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0004h

Figure 14-7073. ROM_TABLE_0_0_ROM_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">2000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">2000h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-14399. ROM_TABLE_0_0_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.3 ROM_TABLE_0_0_ROM_ENTRY2 Register

14.8.1.2.3.1 ROM_TABLE_0_0_ROM_ENTRY2 Register (Offset = 8h) [reset = 3h]

rom table entry 2

Return to Summary Table

Table 14-14400. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0008h

Figure 14-7074. ROM_TABLE_0_0_ROM_ENTRY2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-14401. ROM_TABLE_0_0_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	RESERVED	NONE	0h	Reserved
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.4 ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register

14.8.1.2.4.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register (Offset = 8h) [reset = 10h]

rom table manual entry 0

Return to Summary Table

Table 14-14402. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0008h

Figure 14-7075. ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14403. ROM_TABLE_0_0_ROM_MANUAL_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.5 ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register

14.8.1.2.5.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register (Offset = Ch) [reset = 10h]

rom table manual entry 1

Return to Summary Table

Table 14-14404. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 000Ch

Figure 14-7076. ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14405. ROM_TABLE_0_0_ROM_MANUAL_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.6 ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register

14.8.1.2.6.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register (Offset = 10h) [reset = 10h]

rom table manual entry 2

Return to Summary Table

Table 14-14406. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0010h

Figure 14-7077. ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14407. ROM_TABLE_0_0_ROM_MANUAL_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.7 ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register

14.8.1.2.7.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register (Offset = 14h) [reset = 10h]

rom table manual entry 3

Return to Summary Table

Table 14-14408. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0014h

Figure 14-7078. ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14409. ROM_TABLE_0_0_ROM_MANUAL_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.8 ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register

14.8.1.2.8.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register (Offset = 18h) [reset = 10h]

rom table manual entry 4

Return to Summary Table

Table 14-14410. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0018h

Figure 14-7079. ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14411. ROM_TABLE_0_0_ROM_MANUAL_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.9 ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register

14.8.1.2.9.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register (Offset = 1Ch) [reset = 10h]

rom table manual entry 5

Return to Summary Table

Table 14-14412. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 001Ch

Figure 14-7080. ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14413. ROM_TABLE_0_0_ROM_MANUAL_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.10 ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register

14.8.1.2.10.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register (Offset = 20h) [reset = 10h]

rom table manual entry 6

Return to Summary Table

Table 14-14414. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0020h

Figure 14-7081. ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14415. ROM_TABLE_0_0_ROM_MANUAL_ENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.11 ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register

14.8.1.2.11.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register (Offset = 24h) [reset = 10h]

rom table manual entry 7

Return to Summary Table

Table 14-14416. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0024h

Figure 14-7082. ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14417. ROM_TABLE_0_0_ROM_MANUAL_ENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.12 ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register

14.8.1.2.12.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register (Offset = 28h) [reset = 10h]

rom table manual entry 8

Return to Summary Table

Table 14-14418. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0028h

Figure 14-7083. ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14419. ROM_TABLE_0_0_ROM_MANUAL_ENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.13 ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register

14.8.1.2.13.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register (Offset = 2Ch) [reset = 10h]

rom table manual entry 9

Return to Summary Table

Table 14-14420. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 002Ch

Figure 14-7084. ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14421. ROM_TABLE_0_0_ROM_MANUAL_ENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.14 ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register

14.8.1.2.14.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register (Offset = 30h) [reset = 10h]

rom table manual entry 10

Return to Summary Table

Table 14-14422. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0030h

Figure 14-7085. ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14423. ROM_TABLE_0_0_ROM_MANUAL_ENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.15 ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register

14.8.1.2.15.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register (Offset = 34h) [reset = 10h]

rom table manual entry 11

Return to Summary Table

Table 14-14424. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0034h

Figure 14-7086. ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14425. ROM_TABLE_0_0_ROM_MANUAL_ENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.16 ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register

14.8.1.2.16.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register (Offset = 38h) [reset = 10h]

rom table manual entry 12

Return to Summary Table

Table 14-14426. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0038h

Figure 14-7087. ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14427. ROM_TABLE_0_0_ROM_MANUAL_ENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.17 ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register

14.8.1.2.17.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register (Offset = 3Ch) [reset = 10h]

rom table manual entry 13

Return to Summary Table

Table 14-14428. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 003Ch

Figure 14-7088. ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14429. ROM_TABLE_0_0_ROM_MANUAL_ENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.18 ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register

14.8.1.2.18.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register (Offset = 40h) [reset = 10h]

rom table manual entry 14

Return to Summary Table

Table 14-14430. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0040h

Figure 14-7089. ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14431. ROM_TABLE_0_0_ROM_MANUAL_ENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.19 ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register

14.8.1.2.19.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register (Offset = 44h) [reset = 10h]

rom table manual entry 15

Return to Summary Table

Table 14-14432. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0044h

Figure 14-7090. ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14433. ROM_TABLE_0_0_ROM_MANUAL_ENTRY15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.20 ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register

14.8.1.2.20.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register (Offset = 48h) [reset = 10h]

rom table manual entry 16

Return to Summary Table

Table 14-14434. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0048h

Figure 14-7091. ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14435. ROM_TABLE_0_0_ROM_MANUAL_ENTRY16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.21 ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register

14.8.1.2.21.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register (Offset = 4Ch) [reset = 10h]

rom table manual entry 17

Return to Summary Table

Table 14-14436. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 004Ch

Figure 14-7092. ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14437. ROM_TABLE_0_0_ROM_MANUAL_ENTRY17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.22 ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register

14.8.1.2.22.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register (Offset = 50h) [reset = 10h]

rom table manual entry 18

Return to Summary Table

Table 14-14438. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0050h

Figure 14-7093. ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14439. ROM_TABLE_0_0_ROM_MANUAL_ENTRY18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.23 ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register

14.8.1.2.23.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register (Offset = 54h) [reset = 10h]

rom table manual entry 19

Return to Summary Table

Table 14-14440. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0054h

Figure 14-7094. ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14441. ROM_TABLE_0_0_ROM_MANUAL_ENTRY19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.24 ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register

14.8.1.2.24.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register (Offset = 58h) [reset = 10h]

rom table manual entry 20

Return to Summary Table

Table 14-14442. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0058h

Figure 14-7095. ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14443. ROM_TABLE_0_0_ROM_MANUAL_ENTRY20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.25 ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register

14.8.1.2.25.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register (Offset = 5Ch) [reset = 10h]

rom table manual entry 21

Return to Summary Table

Table 14-14444. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 005Ch

Figure 14-7096. ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14445. ROM_TABLE_0_0_ROM_MANUAL_ENTRY21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.26 ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register

14.8.1.2.26.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register (Offset = 60h) [reset = 10h]

rom table manual entry 22

Return to Summary Table

Table 14-14446. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0060h

Figure 14-7097. ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14447. ROM_TABLE_0_0_ROM_MANUAL_ENTRY22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.27 ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register

14.8.1.2.27.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register (Offset = 64h) [reset = 10h]

rom table manual entry 23

Return to Summary Table

Table 14-14448. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0064h

Figure 14-7098. ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14449. ROM_TABLE_0_0_ROM_MANUAL_ENTRY23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.28 ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register

14.8.1.2.28.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register (Offset = 68h) [reset = 10h]

rom table manual entry 24

Return to Summary Table

Table 14-14450. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0068h

Figure 14-7099. ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14451. ROM_TABLE_0_0_ROM_MANUAL_ENTRY24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.29 ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register

14.8.1.2.29.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register (Offset = 6Ch) [reset = 10h]

rom table manual entry 25

Return to Summary Table

Table 14-14452. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 006Ch

Figure 14-7100. ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14453. ROM_TABLE_0_0_ROM_MANUAL_ENTRY25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.30 ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register

14.8.1.2.30.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register (Offset = 70h) [reset = 10h]

rom table manual entry 26

Return to Summary Table

Table 14-14454. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0070h

Figure 14-7101. ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14455. ROM_TABLE_0_0_ROM_MANUAL_ENTRY26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.31 ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register

14.8.1.2.31.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register (Offset = 74h) [reset = 10h]

rom table manual entry 27

Return to Summary Table

Table 14-14456. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0074h

Figure 14-7102. ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14457. ROM_TABLE_0_0_ROM_MANUAL_ENTRY27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.32 ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register

14.8.1.2.32.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register (Offset = 78h) [reset = 10h]

rom table manual entry 28

Return to Summary Table

Table 14-14458. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0078h

Figure 14-7103. ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14459. ROM_TABLE_0_0_ROM_MANUAL_ENTRY28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.33 ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register

14.8.1.2.33.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register (Offset = 7Ch) [reset = 10h]

rom table manual entry 29

Return to Summary Table

Table 14-14460. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 007Ch

Figure 14-7104. ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14461. ROM_TABLE_0_0_ROM_MANUAL_ENTRY29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.34 ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register

14.8.1.2.34.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register (Offset = 80h) [reset = 10h]

rom table manual entry 30

Return to Summary Table

Table 14-14462. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0080h

Figure 14-7105. ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14463. ROM_TABLE_0_0_ROM_MANUAL_ENTRY30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.35 ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register

14.8.1.2.35.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register (Offset = 84h) [reset = 10h]

rom table manual entry 31

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Table 14-14464. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0084h

Figure 14-7106. ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14465. ROM_TABLE_0_0_ROM_MANUAL_ENTRY31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.36 ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register

14.8.1.2.36.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register (Offset = 88h) [reset = 10h]

rom table manual entry 32

Return to Summary Table

Table 14-14466. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0088h

Figure 14-7107. ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14467. ROM_TABLE_0_0_ROM_MANUAL_ENTRY32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.37 ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register

14.8.1.2.37.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register (Offset = 8Ch) [reset = 10h]

rom table manual entry 33

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Table 14-14468. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 008Ch

Figure 14-7108. ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14469. ROM_TABLE_0_0_ROM_MANUAL_ENTRY33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.38 ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register

14.8.1.2.38.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register (Offset = 90h) [reset = 10h]

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Return to Summary Table

Table 14-14470. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0090h

Figure 14-7109. ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14471. ROM_TABLE_0_0_ROM_MANUAL_ENTRY34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.39 ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register

14.8.1.2.39.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register (Offset = 94h) [reset = 10h]

rom table manual entry 35

Return to Summary Table

Table 14-14472. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0094h

Figure 14-7110. ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14473. ROM_TABLE_0_0_ROM_MANUAL_ENTRY35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.40 ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register

14.8.1.2.40.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register (Offset = 98h) [reset = 10h]

rom table manual entry 36

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Table 14-14474. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0098h

Figure 14-7111. ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14475. ROM_TABLE_0_0_ROM_MANUAL_ENTRY36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.41 ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register

14.8.1.2.41.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register (Offset = 9Ch) [reset = 10h]

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Table 14-14476. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 009Ch

Figure 14-7112. ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14477. ROM_TABLE_0_0_ROM_MANUAL_ENTRY37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.42 ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register

14.8.1.2.42.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register (Offset = A0h) [reset = 10h]

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Table 14-14478. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00A0h

Figure 14-7113. ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14479. ROM_TABLE_0_0_ROM_MANUAL_ENTRY38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.43 ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register

14.8.1.2.43.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register (Offset = A4h) [reset = 10h]

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Table 14-14480. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00A4h

Figure 14-7114. ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14481. ROM_TABLE_0_0_ROM_MANUAL_ENTRY39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.44 ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register

14.8.1.2.44.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register (Offset = A8h) [reset = 10h]

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Table 14-14482. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00A8h

Figure 14-7115. ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14483. ROM_TABLE_0_0_ROM_MANUAL_ENTRY40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.45 ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register

14.8.1.2.45.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register (Offset = ACh) [reset = 10h]

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Table 14-14484. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00ACh

Figure 14-7116. ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14485. ROM_TABLE_0_0_ROM_MANUAL_ENTRY41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.46 ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register

14.8.1.2.46.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register (Offset = B0h) [reset = 10h]

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Table 14-14486. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00B0h

Figure 14-7117. ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14487. ROM_TABLE_0_0_ROM_MANUAL_ENTRY42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.47 ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register

14.8.1.2.47.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register (Offset = B4h) [reset = 10h]

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Table 14-14488. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00B4h

Figure 14-7118. ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14489. ROM_TABLE_0_0_ROM_MANUAL_ENTRY43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.48 ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register

14.8.1.2.48.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register (Offset = B8h) [reset = 10h]

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Table 14-14490. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00B8h

Figure 14-7119. ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14491. ROM_TABLE_0_0_ROM_MANUAL_ENTRY44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.49 ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register

14.8.1.2.49.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register (Offset = BCh) [reset = 10h]

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Table 14-14492. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00BCh

Figure 14-7120. ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14493. ROM_TABLE_0_0_ROM_MANUAL_ENTRY45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.50 ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register

14.8.1.2.50.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register (Offset = C0h) [reset = 10h]

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Table 14-14494. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00C0h

Figure 14-7121. ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14495. ROM_TABLE_0_0_ROM_MANUAL_ENTRY46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.51 ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register

14.8.1.2.51.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register (Offset = C4h) [reset = 10h]

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Return to Summary Table

Table 14-14496. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00C4h

Figure 14-7122. ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14497. ROM_TABLE_0_0_ROM_MANUAL_ENTRY47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.52 ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register

14.8.1.2.52.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register (Offset = C8h) [reset = 10h]

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Table 14-14498. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00C8h

Figure 14-7123. ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14499. ROM_TABLE_0_0_ROM_MANUAL_ENTRY48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.53 ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register

14.8.1.2.53.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register (Offset = CCh) [reset = 10h]

rom table manual entry 49

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Table 14-14500. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00CCh

Figure 14-7124. ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14501. ROM_TABLE_0_0_ROM_MANUAL_ENTRY49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.54 ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register

14.8.1.2.54.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register (Offset = D0h) [reset = 10h]

rom table manual entry 50

Return to Summary Table

Table 14-14502. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00D0h

Figure 14-7125. ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14503. ROM_TABLE_0_0_ROM_MANUAL_ENTRY50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.55 ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register

14.8.1.2.55.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register (Offset = D4h) [reset = 10h]

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Return to Summary Table

Table 14-14504. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00D4h

Figure 14-7126. ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14505. ROM_TABLE_0_0_ROM_MANUAL_ENTRY51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.56 ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register

14.8.1.2.56.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register (Offset = D8h) [reset = 10h]

rom table manual entry 52

Return to Summary Table

Table 14-14506. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00D8h

Figure 14-7127. ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14507. ROM_TABLE_0_0_ROM_MANUAL_ENTRY52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.57 ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register

14.8.1.2.57.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register (Offset = DCh) [reset = 10h]

rom table manual entry 53

Return to Summary Table

Table 14-14508. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00DCh

Figure 14-7128. ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14509. ROM_TABLE_0_0_ROM_MANUAL_ENTRY53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.58 ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register

14.8.1.2.58.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register (Offset = E0h) [reset = 10h]

rom table manual entry 54

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Table 14-14510. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00E0h

Figure 14-7129. ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14511. ROM_TABLE_0_0_ROM_MANUAL_ENTRY54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.59 ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register

14.8.1.2.59.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register (Offset = E4h) [reset = 10h]

rom table manual entry 55

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Table 14-14512. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00E4h

Figure 14-7130. ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14513. ROM_TABLE_0_0_ROM_MANUAL_ENTRY55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.60 ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register

14.8.1.2.60.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register (Offset = E8h) [reset = 10h]

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Table 14-14514. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00E8h

Figure 14-7131. ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14515. ROM_TABLE_0_0_ROM_MANUAL_ENTRY56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.61 ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register

14.8.1.2.61.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register (Offset = ECh) [reset = 10h]

rom table manual entry 57

Return to Summary Table

Table 14-14516. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00ECh

Figure 14-7132. ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14517. ROM_TABLE_0_0_ROM_MANUAL_ENTRY57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.62 ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register

14.8.1.2.62.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register (Offset = F0h) [reset = 10h]

rom table manual entry 58

Return to Summary Table

Table 14-14518. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00F0h

Figure 14-7133. ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14519. ROM_TABLE_0_0_ROM_MANUAL_ENTRY58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.63 ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register

14.8.1.2.63.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register (Offset = F4h) [reset = 10h]

rom table manual entry 59

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Table 14-14520. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00F4h

Figure 14-7134. ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14521. ROM_TABLE_0_0_ROM_MANUAL_ENTRY59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.64 ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register

14.8.1.2.64.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register (Offset = F8h) [reset = 10h]

rom table manual entry 60

Return to Summary Table

Table 14-14522. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00F8h

Figure 14-7135. ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14523. ROM_TABLE_0_0_ROM_MANUAL_ENTRY60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.65 ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register

14.8.1.2.65.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register (Offset = FCh) [reset = 10h]

rom table manual entry 61

Return to Summary Table

Table 14-14524. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 00FCh

Figure 14-7136. ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14525. ROM_TABLE_0_0_ROM_MANUAL_ENTRY61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.66 ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register

14.8.1.2.66.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register (Offset = 100h) [reset = 10h]

rom table manual entry 62

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Table 14-14526. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0100h

Figure 14-7137. ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14527. ROM_TABLE_0_0_ROM_MANUAL_ENTRY62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.67 ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register

14.8.1.2.67.1 ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register (Offset = 104h) [reset = 10h]

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Table 14-14528. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0104h

Figure 14-7138. ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-14529. ROM_TABLE_0_0_ROM_MANUAL_ENTRY63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.68 ROM_TABLE_0_0_PERIPHID0 Register

14.8.1.2.68.1 ROM_TABLE_0_0_PERIPHID0 Register (Offset = 108h) [reset = 2h]

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Table 14-14530. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0108h

Figure 14-7139. ROM_TABLE_0_0_PERIPHID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14531. ROM_TABLE_0_0_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.69 ROM_TABLE_0_0_PERIPHID1 Register

14.8.1.2.69.1 ROM_TABLE_0_0_PERIPHID1 Register (Offset = 10Ch) [reset = 2h]

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Table 14-14532. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 010Ch

Figure 14-7140. ROM_TABLE_0_0_PERIPHID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14533. ROM_TABLE_0_0_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.70 ROM_TABLE_0_0_PERIPHID2 Register

14.8.1.2.70.1 ROM_TABLE_0_0_PERIPHID2 Register (Offset = 110h) [reset = 2h]

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Table 14-14534. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0110h

Figure 14-7141. ROM_TABLE_0_0_PERIPHID2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14535. ROM_TABLE_0_0_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.71 ROM_TABLE_0_0_PERIPHID3 Register

14.8.1.2.71.1 ROM_TABLE_0_0_PERIPHID3 Register (Offset = 114h) [reset = 2h]

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Table 14-14536. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0114h

Figure 14-7142. ROM_TABLE_0_0_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14537. ROM_TABLE_0_0_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.72 ROM_TABLE_0_0_PERIPHID4 Register

14.8.1.2.72.1 ROM_TABLE_0_0_PERIPHID4 Register (Offset = 118h) [reset = 2h]

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Table 14-14538. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 0118h

Figure 14-7143. ROM_TABLE_0_0_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14539. ROM_TABLE_0_0_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.73 ROM_TABLE_0_0_COMPID0 Register

14.8.1.2.73.1 ROM_TABLE_0_0_COMPID0 Register (Offset = 3FCh) [reset = Dh]

component id

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Table 14-14540. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 03FCh

Figure 14-7144. ROM_TABLE_0_0_COMPID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Dh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Dh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Dh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">Dh</td></tr>
</table>

Table 14-14541. ROM_TABLE_0_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	Dh	Component id0

14.8.1.2.74 ROM_TABLE_0_0_COMPID1 Register

14.8.1.2.74.1 ROM_TABLE_0_0_COMPID1 Register (Offset = 3FCh) [reset = 10h]

component id

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Table 14-14542. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 03FCh

Figure 14-7145. ROM_TABLE_0_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
10h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VAR							
R							
10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VAR							
R							
10h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VAR							
R							
10h							

Table 14-14543. ROM_TABLE_0_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	10h	Component id1

14.8.1.2.75 ROM_TABLE_0_0_COMPID2 Register

14.8.1.2.75.1 ROM_TABLE_0_0_COMPID2 Register (Offset = 3FCh) [reset = 5h]

component id

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Table 14-14544. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 03FCh

Figure 14-7146. ROM_TABLE_0_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
5h							
23	22	21	20	19	18	17	16
VAR							
R							
5h							
15	14	13	12	11	10	9	8
VAR							
R							
5h							
7	6	5	4	3	2	1	0
VAR							
R							
5h							

Table 14-14545. ROM_TABLE_0_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	5h	Component id2

14.8.1.2.76 ROM_TABLE_0_0_COMPID3 Register

14.8.1.2.76.1 ROM_TABLE_0_0_COMPID3 Register (Offset = 3FCh) [reset = B1h]

component id

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Table 14-14546. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 03FCh

Figure 14-7147. ROM_TABLE_0_0_COMPID3 Name Register

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">B1h</td></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">VAR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">B1h</td></tr>
</table>

Table 14-14547. ROM_TABLE_0_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	B1h	Component id3

14.8.1.2.77 CFGAP_CFG_0_JTAGID_REG Register

14.8.1.2.77.1 CFGAP_CFG_0_JTAGID_REG Register (Offset = 0h) [reset = 0h]

This register returns the JTAG ID tieoff of the device. The reset value depends on the tie off

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Table 14-14548. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2000h

Figure 14-7148. CFGAP_CFG_0_JTAGID_REG Name Register

31	30	29	28	27	26	25	24
JTAG_ID							
R							
0h							
23	22	21	20	19	18	17	16
JTAG_ID							
R							
0h							
15	14	13	12	11	10	9	8
JTAG_ID							
R							
0h							
7	6	5	4	3	2	1	0
JTAG_ID							
R							
0h							

Table 14-14549. CFGAP_CFG_0_JTAGID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_ID	R	0h	The JTAG ID of the device

14.8.1.2.78 CFGAP_CFG_0_USERID_REG Register

14.8.1.2.78.1 CFGAP_CFG_0_USERID_REG Register (Offset = 4h) [reset = 0h]

This register returns the Chip Spin ID tieoff value of the device. The reset value depends on the tieoff

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Table 14-14550. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2004h

Figure 14-7149. CFGAP_CFG_0_USERID_REG Name Register

31	30	29	28	27	26	25	24
USER_ID							
R							
0h							
23	22	21	20	19	18	17	16
USER_ID							
R							
0h							
15	14	13	12	11	10	9	8
USER_ID							
R							
0h							
7	6	5	4	3	2	1	0
USER_ID							
R							
0h							

Table 14-14551. CFGAP_CFG_0_USERID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USER_ID	R	0h	The USER ID of the device

14.8.1.2.79 CFGAP_CFG_0_VERSION_REG Register

14.8.1.2.79.1 CFGAP_CFG_0_VERSION_REG Register (Offset = 8h) [reset = 0h]

This register is used to read the RTL version information and to determine which modules are included in the rtl build. The reset value depends on the build options

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Table 14-14552. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2008h

Figure 14-7150. CFGAP_CFG_0_VERSION_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">MAJOR_REV</td><td colspan="4">MINOR_REV</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED</td><td>JTAG_AP</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>POWERAP</td><td>AXIAP</td><td>APBAP</td><td>SECURITYAP</td><td>SPARE</td><td>ICEPICKM</td><td>TRIGGERSUPPORT</td><td>TRACESUPPORT</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14553. CFGAP_CFG_0_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	MAJOR_REV	R	0h	RTL Major revision [5]
27:24	MINOR_REV	R	0h	RTL Minor revision [0]
23:9	RESERVED	R	0h	Reserved, returns 0
8	JTAG_AP	R	0h	a 1 indicates JTAG AP is supported
7	POWERAP	R	0h	A 1 indicates that the Power AP is supported
6	AXIAP	R	0h	A 1 indicates that the AXIAP exists and system memory accesses are supported
5	APBAP	R	0h	A 1 indicates that the APBAP exisits and accesses to external debug logic are supported
4	SECURITYAP	R	0h	A 1 indicates that the Security AP is supported
3	SPARE	R	0h	This is a spare bit, returns 0
2	ICEPICKM	R	0h	A 1 indicates that ICEPick M is present inthe design
1	TRIGGERSUPPORT	R	0h	A 1 indicates that cross triggering is supported
0	TRACESUPPORT	R	0h	A 1 indicates that hardware trace export is supported

14.8.1.2.80 CFGAP_CFG_0_APID_REGISTER Register

14.8.1.2.80.1 CFGAP_CFG_0_APID_REGISTER Register (Offset = FCh) [reset = 20E0001h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-14554. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 20FCh

Figure 14-7151. CFGAP_CFG_0_APID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">107h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">107h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">1h</td></tr>
</table>

Table 14-14555. CFGAP_CFG_0_APID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	107h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	1h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.81 APBAP_CFG_0_CSWREG Register

14.8.1.2.81.1 APBAP_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

Control/Status Register

Return to Summary Table

Table 14-14556. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2100h

Figure 14-7152. APBAP_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14557. APBAP_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.82 APBAP_CFG_0_DRWREG Register

14.8.1.2.82.1 APBAP_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-14558. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 210Ch

Figure 14-7153. APBAP_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14559. APBAP_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.83 APBAP_CFG_0_BD0REG Register

14.8.1.2.83.1 APBAP_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14560. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2110h

Figure 14-7154. APBAP_CFG_0_BD0REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14561. APBAP_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.84 APBAP_CFG_0_BD1REG Register

14.8.1.2.84.1 APBAP_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14562. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2114h

Figure 14-7155. APBAP_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14563. APBAP_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.85 APBAP_CFG_0_BD2REG Register

14.8.1.2.85.1 APBAP_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14564. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2118h

Figure 14-7156. APBAP_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14565. APBAP_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.86 APBAP_CFG_0_BD3REG Register

14.8.1.2.86.1 APBAP_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14566. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 211Ch

Figure 14-7157. APBAP_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14567. APBAP_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.87 APBAP_CFG_0_ROM_REGISTER Register

14.8.1.2.87.1 APBAP_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the APB ROM Address.

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Table 14-14568. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 21F8h

Figure 14-7158. APBAP_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER_ADDRESS							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER_ADDRESS							
R							
0h							

Table 14-14569. APBAP_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER_ADDRESS	R	0h	Reading this register returns the APB ROM Address

14.8.1.2.88 APBAP_CFG_0_ID_REGISTER Register

14.8.1.2.88.1 APBAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-14570. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 21FCh

Figure 14-7159. APBAP_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-14571. APBAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.8.1.2.89 AXIAP_CFG_0_CSWREG Register

14.8.1.2.89.1 AXIAP_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This is the control/status register

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Table 14-14572. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2200h

Figure 14-7160. AXIAP_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DBGSWEN</td><td colspan="7">TYPEEXT</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>SPIDEN</td><td colspan="7">RESERVED2</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">TYPE</td><td colspan="4">MODE</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>TRINPROG</td><td>RESERVED1</td><td colspan="2">ADDR_INC</td><td>RESERVED0</td><td colspan="3">SIZE</td></tr>
<tr><td>R</td><td>R</td><td colspan="2">R/W</td><td>R</td><td colspan="3">R</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-14573. AXIAP_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBGSWEN	R/W	0h	Indicates whether accesses should treated as application or debug
30:24	TYPEEXT	R/W	0h	
23	SPIDEN	R	0h	When 1, secure accesses are enabled
22:16	RESERVED2	R	0h	Reserved, reads return 0
15:12	TYPE	R/W	0h	Sets Prot, Type attributes for the access
11:8	MODE	R/W	0h	Sets mode of operation 0000=basic, 0001=Barrier extensions, all other values reserved
7	TRINPROG	R	0h	This bit is set to 1 while a transfer is in progress on the connection to the memory system, and is set to 0 while the connection is idle
6	RESERVED1	R	0h	This bit is reserved and reads return 0
5:4	ADDR_INC	R/W	0h	Address Auto Increment and packing mode
3	RESERVED0	R	0h	reserved, returns 0
2:0	SIZE	R	0h	This specifies the size of the access For this implementation, the access is always 32 bits [010]

14.8.1.2.90 AXIAP_CFG_0_DRWREG Register

14.8.1.2.90.1 AXIAP_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-14574. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 220Ch

Figure 14-7161. AXIAP_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14575. AXIAP_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.91 AXIAP_CFG_0_BD0REG Register

14.8.1.2.91.1 AXIAP_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14576. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2210h

Figure 14-7162. AXIAP_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-14577. AXIAP_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.92 AXIAP_CFG_0_BD1REG Register

14.8.1.2.92.1 AXIAP_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14578. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2214h

Figure 14-7163. AXIAP_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14579. AXIAP_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.93 AXIAP_CFG_0_BD2REG Register

14.8.1.2.93.1 AXIAP_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14580. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2218h

Figure 14-7164. AXIAP_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14581. AXIAP_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.94 AXIAP_CFG_0_BD3REG Register

14.8.1.2.94.1 AXIAP_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14582. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 221Ch

Figure 14-7165. AXIAP_CFG_0_BD3REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_3_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_3_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_3_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_3_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14583. AXIAP_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.95 AXIAP_CFG_0_MBT_REGISTER Register

14.8.1.2.95.1 AXIAP_CFG_0_MBT_REGISTER Register (Offset = 20h) [reset = 0h]

This register sets memory barrier attributes

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Table 14-14584. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2220h

Figure 14-7166. AXIAP_CFG_0_MBT_REGISTER Name Register

31	30	29	28	27	26	25	24
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							

Table 14-14585. AXIAP_CFG_0_MBT_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEMORY_BARRIER_TRANSFER_REGISTER	R/W	0h	This register sets memory barrier attributes

14.8.1.2.96 AXIAP_CFG_0_ROM_HI_REGISTER Register

14.8.1.2.96.1 AXIAP_CFG_0_ROM_HI_REGISTER Register (Offset = F0h) [reset = 0h]

Reading this register returns the AXI ROM Address (63-32).

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Table 14-14586. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 22F0h

Figure 14-7167. AXIAP_CFG_0_ROM_HI_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_HI_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_HI_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_HI_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_HI_REGISTER_ADDRESS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14587. AXIAP_CFG_0_ROM_HI_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_HI_REGISTER_ADDRESS	R	0h	Reading this register returns the upper ROM Address

14.8.1.2.97 AXIAP_CFG_0_CFG_REGISTER Register

14.8.1.2.97.1 AXIAP_CFG_0_CFG_REGISTER Register (Offset = F4h) [reset = 0h]

The CFG register provides information about how the MEM-AP implementation is configured.

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Table 14-14588. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 22F4h

Figure 14-7168. AXIAP_CFG_0_CFG_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					LD	LA	BE
R					R	R	R
0h					0h	0h	0h

Table 14-14589. AXIAP_CFG_0_CFG_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved bit, return 0
2	LD	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Data Extension, that provides support for data items larger than 32-bits, it is 0
1	LA	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Physical Address Extension, that supports physical addresses of more than 32-bits:
0	BE	R	0h	ADIv52 obsoletes support for big-endian MEM-AP, and this bit must RAZ

14.8.1.2.98 AXIAP_CFG_0_ROM_LO_REGISTER Register

14.8.1.2.98.1 AXIAP_CFG_0_ROM_LO_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AXI ROM Address (31:12) .

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Table 14-14590. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 22F8h

Figure 14-7169. AXIAP_CFG_0_ROM_LO_REGISTER Name Register

31	30	29	28	27	26	25	24
LOWBASE							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOWBASE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOWBASE				RESERVED			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						FORMAT	PRESENT
R						R	R
0h						0h	0h

Table 14-14591. AXIAP_CFG_0_ROM_LO_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	LOWBASE	R	0h	Bits 31:12 of the base address
11:2	RESERVED	R	0h	Reserved, returns 0
1	FORMAT	R	0h	Base address register format [0]
0	PRESENT	R	0h	This field indicates whether a debug entry is present for this MEM-AP: 0 No debug entry present 1 Debug entry present

14.8.1.2.99 AXIAP_CFG_0_ID_REGISTER Register

14.8.1.2.99.1 AXIAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-14592. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 22FCh

Figure 14-7170. AXIAP_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14593. AXIAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB, 4=AXI [4]

14.8.1.2.100 PWRAP_CFG_0_ID_REGISTER Register

14.8.1.2.100.1 PWRAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 2E0002h]

Reading this register returns the ID information for this AP.

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Table 14-14594. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 23FCh

Figure 14-7171. PWRAP_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				17h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
17h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				2h			

Table 14-14595. PWRAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	17h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	2h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.8.1.2.101 PVIEW_CFG_0_PVIEW_STATE0 Register

14.8.1.2.101.1 PVIEW_CFG_0_PVIEW_STATE0 Register (Offset = 0h) [reset = 0h]

This register provides the device specific power status. A read of Power View State Register will lock the values for all other Power View State Registers. A read from the last Power View State register will unlock them so they can update

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Table 14-14596. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2400h

Figure 14-7172. PVIEW_CFG_0_PVIEW_STATE0 Name Register

31	30	29	28	27	26	25	24
POWER_VIEW_STATE_REG0							
R							
0h							
23	22	21	20	19	18	17	16
POWER_VIEW_STATE_REG0							
R							
0h							
15	14	13	12	11	10	9	8
POWER_VIEW_STATE_REG0							
R							
0h							
7	6	5	4	3	2	1	0
POWER_VIEW_STATE_REG0							
R							
0h							

Table 14-14597. PVIEW_CFG_0_PVIEW_STATE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POWER_VIEW_STATE_REG0	R	0h	

14.8.1.2.102 PVIEW_CFG_0_PVIEW_CAPABILITY Register

14.8.1.2.102.1 PVIEW_CFG_0_PVIEW_CAPABILITY Register (Offset = F0h) [reset = 0h]

The Capability Register provides information on the number of Power State registers implemented in the AP

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Table 14-14598. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 24F0h

Figure 14-7173. PVIEW_CFG_0_PVIEW_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		NUMSTATREG					
R		R					
0h		0h					

Table 14-14599. PVIEW_CFG_0_PVIEW_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved, returns 0
5:0	NUMSTATREG	R	0h	The value read indicates the number of valid Power State Registers that are implemented in the system The maximum number is 60 and the minimum number is 1 The registers are always implemented at contiguous addresses so a value of 7 means that registers 0-6 are valid

14.8.1.2.103 PVIEW_CFG_0_ID_REGISTER Register

14.8.1.2.103.1 PVIEW_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-14600. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 24FCh

Figure 14-7174. PVIEW_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-14601. PVIEW_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	0h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type = 3

14.8.1.2.104 JTAGAP_CFG_0_CSW Register

14.8.1.2.104.1 JTAGAP_CFG_0_CSW Register (Offset = 0h) [reset = 0h]

This register provides control and status information

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Table 14-14602. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2500h

Figure 14-7175. JTAGAP_CFG_0_CSW Name Register

31	30	29	28	27	26	25	24
SERACTV	WFIFOCNT			RSV27	RFIFOCNT		
R	R			R	R		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PORT_CONNECTED_STATUS	SRST_STATUS	TRST_ASSERT	SRST_ASSERT
R				R	R	R/W	R/W
0h				0h	0h	0h	0h

Table 14-14603. JTAGAP_CFG_0_CSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SERACTV	R	0h	JTAG Serializer active
30:28	WFIFOCNT	R	0h	Outstanding Write FIFO Byte Count
27	RSV27	R	0h	Reserved, returns 0
26:24	RFIFOCNT	R	0h	Outstanding Read FIFO Byte Count
23:4	RESERVED	R	0h	Reserved, returns 0
3	PORT_CONNECTED_STATUS	R	0h	Reading this returns the Port connected status of the selected port
2	SRST_STATUS	R	0h	Reading this returns the SRST status of the selected port If multiple ports are selected, it is the AND of all the SRSTCONNECTED inputs from the selected ports
1	TRST_ASSERT	R/W	0h	Writing a 1 causes TRST to be asserted
0	SRST_ASSERT	R/W	0h	Writing a 1 causes SRST to be asserted

14.8.1.2.105 JTAGAP_CFG_0_PSEL_REG Register

14.8.1.2.105.1 JTAGAP_CFG_0_PSEL_REG Register (Offset = 4h) [reset = 0h]

This 8-bit register is used to select the JTAG port.

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Table 14-14604. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2504h

Figure 14-7176. JTAGAP_CFG_0_PSEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_SELECT_REGISTER							
R/W							
0h							

Table 14-14605. JTAGAP_CFG_0_PSEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	read as 0
7:0	PORT_SELECT_REGISTER	R/W	0h	

14.8.1.2.106 JTAGAP_CFG_0_PSTA_REG Register

14.8.1.2.106.1 JTAGAP_CFG_0_PSTA_REG Register (Offset = 8h) [reset = 0h]

A bit value of 1 indicates that a selected and enabled port has gone inactive. These bits are sticky. Writing a 1 to them clears them.

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Table 14-14606. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2508h

Figure 14-7177. JTAGAP_CFG_0_PSTA_REG Name Register

31	30	29	28	27	26	25	24
PORT_STATUS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
PORT_STATUS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
PORT_STATUS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_STATUS_REGISTER							
R/W							
0h							

Table 14-14607. JTAGAP_CFG_0_PSTA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_STATUS_REGISTER	R/W	0h	

14.8.1.2.107 JTAGAP_CFG_0_BYTEFIFO1 Register

14.8.1.2.107.1 JTAGAP_CFG_0_BYTEFIFO1 Register (Offset = 10h) [reset = 0h]

Reading this location reads a byte from the FIFO. Writing it loads a byte into the FIFO. Reset value is UNDEFINED

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Table 14-14608. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2510h

Figure 14-7178. JTAGAP_CFG_0_BYTEFIFO1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_1							
R/W							
0h							

Table 14-14609. JTAGAP_CFG_0_BYTEFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	
7:0	BYTE_FIFO_1	R/W	0h	

14.8.1.2.108 JTAGAP_CFG_0_BYTEFIFO2 Register

14.8.1.2.108.1 JTAGAP_CFG_0_BYTEFIFO2 Register (Offset = 14h) [reset = 0h]

Reading this location reads a 16 bits from the FIFO. Writing it loads 16 bits into the FIFO. Reset value is UNDEFINED

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Table 14-14610. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2514h

Figure 14-7179. JTAGAP_CFG_0_BYTEFIFO2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_2							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_2							
R/W							
0h							

Table 14-14611. JTAGAP_CFG_0_BYTEFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	
15:0	BYTE_FIFO_2	R/W	0h	

14.8.1.2.109 JTAGAP_CFG_0_BYTEFIFO3 Register

14.8.1.2.109.1 JTAGAP_CFG_0_BYTEFIFO3 Register (Offset = 18h) [reset = 0h]

Reading this location reads a 24 bits from the FIFO. Writing it loads 24 bits into the FIFO. Reset value is UNDEFINED

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Table 14-14612. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2518h

Figure 14-7180. JTAGAP_CFG_0_BYTEFIFO3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYTE_FIFO_3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BYTE_FIFO_3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BYTE_FIFO_3							
R/W							
0h							

Table 14-14613. JTAGAP_CFG_0_BYTEFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R/W	0h	
23:0	BYTE_FIFO_3	R/W	0h	

14.8.1.2.110 JTAGAP_CFG_0_BYTEFIFO4 Register

14.8.1.2.110.1 JTAGAP_CFG_0_BYTEFIFO4 Register (Offset = 1Ch) [reset = 0h]

Reading this location reads a 32 bits from the FIFO. Writing it loads 32 bits into the FIFO. Reset value is UNDEFINED

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Table 14-14614. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 251Ch

Figure 14-7181. JTAGAP_CFG_0_BYTEFIFO4 Name Register

31	30	29	28	27	26	25	24
BYTE_FIFO_4							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_4							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_4							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_4							
R/W							
0h							

Table 14-14615. JTAGAP_CFG_0_BYTEFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BYTE_FIFO_4	R/W	0h	

14.8.1.2.111 JTAGAP_CFG_0_ID_REGISTER Register

14.8.1.2.111.1 JTAGAP_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-14616. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 25FCh

Figure 14-7182. JTAGAP_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-14617. JTAGAP_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [1]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [0]

14.8.1.2.112 SECAP_CFG_0_TXDATA Register

14.8.1.2.112.1 SECAP_CFG_0_TXDATA Register (Offset = 0h) [reset = 0h]

Data value to send to security controller. APLLication specific

Return to Summary Table

Table 14-14618. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2600h

Figure 14-7183. SECAP_CFG_0_TXDATA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_DATA_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TX_DATA_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TX_DATA_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_DATA_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14619. SECAP_CFG_0_TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TX_DATA_REGISTER	R/W	0h	Transmit Data. Writing this sets the TXDATAVAIL bit in the Transmit Control Register

14.8.1.2.113 SECAP_CFG_0_TXCTRL Register

14.8.1.2.113.1 SECAP_CFG_0_TXCTRL Register (Offset = 4h) [reset = 0h]

Register to send control information to the Security Controller, Application specific

Return to Summary Table

Table 14-14620. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2604h

Figure 14-7184. SECAP_CFG_0_TXCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">TX_CONTROL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">TX_CONTROL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TX_CONTROL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">TX_CONTROL</td><td>TXDAV</td></tr>
<tr><td colspan="7">R/W</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14621. SECAP_CFG_0_TXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	TX_CONTROL	R/W	0h	31 bits to send to security controller, Application specific
0	TXDAV	R	0h	TX Data Available

14.8.1.2.114 SECAP_CFG_0_RXDATA Register

14.8.1.2.114.1 SECAP_CFG_0_RXDATA Register (Offset = 8h) [reset = 0h]

Data value from the security controller. Application specific

Return to Summary Table

Table 14-14622. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2608h

Figure 14-7185. SECAP_CFG_0_RXDATA Name Register

31	30	29	28	27	26	25	24
RX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
RX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_DATA_REGISTER							
R/W							
0h							

Table 14-14623. SECAP_CFG_0_RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RX_DATA_REGISTER	R/W	0h	Recieve Data. Writing this sets the RXDATAVAIL bit in the Recieve Control Register

14.8.1.2.115 SECAP_CFG_0_RXCTRL Register

14.8.1.2.115.1 SECAP_CFG_0_RXCTRL Register (Offset = Ch) [reset = 0h]

Register to receive control information from the Security Controller

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Table 14-14624. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 260Ch

Figure 14-7186. SECAP_CFG_0_RXCTRL Name Register

31	30	29	28	27	26	25	24
RX_CONTROL							
R							
0h							
23	22	21	20	19	18	17	16
RX_CONTROL							
R							
0h							
15	14	13	12	11	10	9	8
RX_CONTROL							
R							
0h							
7	6	5	4	3	2	1	0
RX_CONTROL							RXDAV
R							R
0h							0h

Table 14-14625. SECAP_CFG_0_RXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RX_CONTROL	R	0h	31 bits from the security controller, Application specific
0	RXDAV	R	0h	TX Data Available

14.8.1.2.116 CORTEX0_CFG_0_CSWREG Register

14.8.1.2.116.1 CORTEX0_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-14626. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2700h

Figure 14-7187. CORTEX0_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-14627. CORTEX0_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.117 CORTEX0_CFG_0_DRWREG Register

14.8.1.2.117.1 CORTEX0_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-14628. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 270Ch

Figure 14-7188. CORTEX0_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14629. CORTEX0_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.118 CORTEX0_CFG_0_BD0REG Register

14.8.1.2.118.1 CORTEX0_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14630. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2710h

Figure 14-7189. CORTEX0_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-14631. CORTEX0_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.119 CORTEX0_CFG_0_BD1REG Register

14.8.1.2.119.1 CORTEX0_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14632. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2714h

Figure 14-7190. CORTEX0_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14633. CORTEX0_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.120 CORTEX0_CFG_0_BD2REG Register

14.8.1.2.120.1 CORTEX0_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14634. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2718h

Figure 14-7191. CORTEX0_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14635. CORTEX0_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.121 CORTEX0_CFG_0_BD3REG Register

14.8.1.2.121.1 CORTEX0_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14636. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 271Ch

Figure 14-7192. CORTEX0_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14637. CORTEX0_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.122 CORTEX0_CFG_0_ROM_REGISTER Register

14.8.1.2.122.1 CORTEX0_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-14638. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 27F8h

Figure 14-7193. CORTEX0_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-14639. CORTEX0_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.123 CORTEX0_CFG_0_ID_REGISTER Register

14.8.1.2.123.1 CORTEX0_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-14640. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 27FCh

Figure 14-7194. CORTEX0_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14641. CORTEX0_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.124 CORTEX1_CFG_0_CSWREG Register

14.8.1.2.124.1 CORTEX1_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-14642. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2800h

Figure 14-7195. CORTEX1_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14643. CORTEX1_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.125 CORTEX1_CFG_0_DRWREG Register

14.8.1.2.125.1 CORTEX1_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-14644. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 280Ch

Figure 14-7196. CORTEX1_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14645. CORTEX1_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.126 CORTEX1_CFG_0_BD0REG Register

14.8.1.2.126.1 CORTEX1_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14646. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2810h

Figure 14-7197. CORTEX1_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-14647. CORTEX1_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.127 CORTEX1_CFG_0_BD1REG Register

14.8.1.2.127.1 CORTEX1_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14648. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2814h

Figure 14-7198. CORTEX1_CFG_0_BD1REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_1_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_1_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_1_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_1_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14649. CORTEX1_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.128 CORTEX1_CFG_0_BD2REG Register

14.8.1.2.128.1 CORTEX1_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14650. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2818h

Figure 14-7199. CORTEX1_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14651. CORTEX1_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.129 CORTEX1_CFG_0_BD3REG Register

14.8.1.2.129.1 CORTEX1_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14652. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 281Ch

Figure 14-7200. CORTEX1_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14653. CORTEX1_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.130 CORTEX1_CFG_0_ROM_REGISTER Register

14.8.1.2.130.1 CORTEX1_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-14654. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 28F8h

Figure 14-7201. CORTEX1_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-14655. CORTEX1_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.131 CORTEX1_CFG_0_ID_REGISTER Register

14.8.1.2.131.1 CORTEX1_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-14656. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 28FCh

Figure 14-7202. CORTEX1_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14657. CORTEX1_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.132 CORTEX2_CFG_0_CSWREG Register

14.8.1.2.132.1 CORTEX2_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-14658. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2900h

Figure 14-7203. CORTEX2_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-14659. CORTEX2_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.133 CORTEX2_CFG_0_DRWREG Register

14.8.1.2.133.1 CORTEX2_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-14660. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 290Ch

Figure 14-7204. CORTEX2_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14661. CORTEX2_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.134 CORTEX2_CFG_0_BD0REG Register

14.8.1.2.134.1 CORTEX2_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14662. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2910h

Figure 14-7205. CORTEX2_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-14663. CORTEX2_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.135 CORTEX2_CFG_0_BD1REG Register

14.8.1.2.135.1 CORTEX2_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14664. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2914h

Figure 14-7206. CORTEX2_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14665. CORTEX2_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.136 CORTEX2_CFG_0_BD2REG Register

14.8.1.2.136.1 CORTEX2_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14666. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2918h

Figure 14-7207. CORTEX2_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14667. CORTEX2_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.137 CORTEX2_CFG_0_BD3REG Register

14.8.1.2.137.1 CORTEX2_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14668. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 291Ch

Figure 14-7208. CORTEX2_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14669. CORTEX2_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.138 CORTEX2_CFG_0_ROM_REGISTER Register

14.8.1.2.138.1 CORTEX2_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-14670. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 29F8h

Figure 14-7209. CORTEX2_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-14671. CORTEX2_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.139 CORTEX2_CFG_0_ID_REGISTER Register

14.8.1.2.139.1 CORTEX2_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-14672. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 29FCh

Figure 14-7210. CORTEX2_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14673. CORTEX2_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.140 CORTEX3_CFG_0_CSWREG Register

14.8.1.2.140.1 CORTEX3_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-14674. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2A00h

Figure 14-7211. CORTEX3_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14675. CORTEX3_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.141 CORTEX3_CFG_0_DRWREG Register

14.8.1.2.141.1 CORTEX3_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-14676. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2A0Ch

Figure 14-7212. CORTEX3_CFG_0_DRWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14677. CORTEX3_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.142 CORTEX3_CFG_0_BD0REG Register

14.8.1.2.142.1 CORTEX3_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14678. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2A10h

Figure 14-7213. CORTEX3_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-14679. CORTEX3_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.143 CORTEX3_CFG_0_BD1REG Register

14.8.1.2.143.1 CORTEX3_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14680. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2A14h

Figure 14-7214. CORTEX3_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14681. CORTEX3_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.144 CORTEX3_CFG_0_BD2REG Register

14.8.1.2.144.1 CORTEX3_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14682. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2A18h

Figure 14-7215. CORTEX3_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14683. CORTEX3_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.145 CORTEX3_CFG_0_BD3REG Register

14.8.1.2.145.1 CORTEX3_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14684. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2A1Ch

Figure 14-7216. CORTEX3_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14685. CORTEX3_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.146 CORTEX3_CFG_0_ROM_REGISTER Register

14.8.1.2.146.1 CORTEX3_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-14686. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2AF8h

Figure 14-7217. CORTEX3_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-14687. CORTEX3_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.147 CORTEX3_CFG_0_ID_REGISTER Register

14.8.1.2.147.1 CORTEX3_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-14688. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2AFCh

Figure 14-7218. CORTEX3_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14689. CORTEX3_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.148 CORTEX4_CFG_0_CSWREG Register

14.8.1.2.148.1 CORTEX4_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-14690. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2B00h

Figure 14-7219. CORTEX4_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14691. CORTEX4_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.149 CORTEX4_CFG_0_DRWREG Register

14.8.1.2.149.1 CORTEX4_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-14692. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2B0Ch

Figure 14-7220. CORTEX4_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14693. CORTEX4_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.150 CORTEX4_CFG_0_BD0REG Register

14.8.1.2.150.1 CORTEX4_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14694. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2B10h

Figure 14-7221. CORTEX4_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-14695. CORTEX4_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.151 CORTEX4_CFG_0_BD1REG Register

14.8.1.2.151.1 CORTEX4_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14696. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2B14h

Figure 14-7222. CORTEX4_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14697. CORTEX4_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.152 CORTEX4_CFG_0_BD2REG Register

14.8.1.2.152.1 CORTEX4_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14698. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2B18h

Figure 14-7223. CORTEX4_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14699. CORTEX4_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.153 CORTEX4_CFG_0_BD3REG Register

14.8.1.2.153.1 CORTEX4_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14700. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2B1Ch

Figure 14-7224. CORTEX4_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14701. CORTEX4_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.154 CORTEX4_CFG_0_ROM_REGISTER Register

14.8.1.2.154.1 CORTEX4_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-14702. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2BF8h

Figure 14-7225. CORTEX4_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-14703. CORTEX4_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.155 CORTEX4_CFG_0_ID_REGISTER Register

14.8.1.2.155.1 CORTEX4_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-14704. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2BFCh

Figure 14-7226. CORTEX4_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14705. CORTEX4_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.156 CORTEX5_CFG_0_CSWREG Register

14.8.1.2.156.1 CORTEX5_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-14706. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2C00h

Figure 14-7227. CORTEX5_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-14707. CORTEX5_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.157 CORTEX5_CFG_0_DRWREG Register

14.8.1.2.157.1 CORTEX5_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-14708. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2C0Ch

Figure 14-7228. CORTEX5_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14709. CORTEX5_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.158 CORTEX5_CFG_0_BD0REG Register

14.8.1.2.158.1 CORTEX5_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14710. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2C10h

Figure 14-7229. CORTEX5_CFG_0_BD0REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14711. CORTEX5_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.159 CORTEX5_CFG_0_BD1REG Register

14.8.1.2.159.1 CORTEX5_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14712. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2C14h

Figure 14-7230. CORTEX5_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14713. CORTEX5_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.160 CORTEX5_CFG_0_BD2REG Register

14.8.1.2.160.1 CORTEX5_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14714. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2C18h

Figure 14-7231. CORTEX5_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14715. CORTEX5_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.161 CORTEX5_CFG_0_BD3REG Register

14.8.1.2.161.1 CORTEX5_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14716. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2C1Ch

Figure 14-7232. CORTEX5_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14717. CORTEX5_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.162 CORTEX5_CFG_0_ROM_REGISTER Register

14.8.1.2.162.1 CORTEX5_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-14718. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2CF8h

Figure 14-7233. CORTEX5_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-14719. CORTEX5_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.163 CORTEX5_CFG_0_ID_REGISTER Register

14.8.1.2.163.1 CORTEX5_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-14720. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2CFCh

Figure 14-7234. CORTEX5_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-14721. CORTEX5_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.164 CORTEX6_CFG_0_CSWREG Register

14.8.1.2.164.1 CORTEX6_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-14722. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2D00h

Figure 14-7235. CORTEX6_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-14723. CORTEX6_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.165 CORTEX6_CFG_0_DRWREG Register

14.8.1.2.165.1 CORTEX6_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-14724. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2D0Ch

Figure 14-7236. CORTEX6_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14725. CORTEX6_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.166 CORTEX6_CFG_0_BD0REG Register

14.8.1.2.166.1 CORTEX6_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14726. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2D10h

Figure 14-7237. CORTEX6_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-14727. CORTEX6_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.167 CORTEX6_CFG_0_BD1REG Register

14.8.1.2.167.1 CORTEX6_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14728. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2D14h

Figure 14-7238. CORTEX6_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14729. CORTEX6_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.168 CORTEX6_CFG_0_BD2REG Register

14.8.1.2.168.1 CORTEX6_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14730. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2D18h

Figure 14-7239. CORTEX6_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14731. CORTEX6_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.169 CORTEX6_CFG_0_BD3REG Register

14.8.1.2.169.1 CORTEX6_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14732. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2D1Ch

Figure 14-7240. CORTEX6_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14733. CORTEX6_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.170 CORTEX6_CFG_0_ROM_REGISTER Register

14.8.1.2.170.1 CORTEX6_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-14734. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2DF8h

Figure 14-7241. CORTEX6_CFG_0_ROM_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14735. CORTEX6_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.171 CORTEX6_CFG_0_ID_REGISTER Register

14.8.1.2.171.1 CORTEX6_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-14736. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2DFCh

Figure 14-7242. CORTEX6_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
0h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-14737. CORTEX6_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.172 CORTEX7_CFG_0_CSWREG Register

14.8.1.2.172.1 CORTEX7_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-14738. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2E00h

Figure 14-7243. CORTEX7_CFG_0_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14739. CORTEX7_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.173 CORTEX7_CFG_0_DRWREG Register

14.8.1.2.173.1 CORTEX7_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-14740. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2E0Ch

Figure 14-7244. CORTEX7_CFG_0_DRWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14741. CORTEX7_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.174 CORTEX7_CFG_0_BD0REG Register

14.8.1.2.174.1 CORTEX7_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14742. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2E10h

Figure 14-7245. CORTEX7_CFG_0_BD0REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14743. CORTEX7_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.175 CORTEX7_CFG_0_BD1REG Register

14.8.1.2.175.1 CORTEX7_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14744. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2E14h

Figure 14-7246. CORTEX7_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14745. CORTEX7_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.176 CORTEX7_CFG_0_BD2REG Register

14.8.1.2.176.1 CORTEX7_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14746. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2E18h

Figure 14-7247. CORTEX7_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14747. CORTEX7_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.177 CORTEX7_CFG_0_BD3REG Register

14.8.1.2.177.1 CORTEX7_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14748. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2E1Ch

Figure 14-7248. CORTEX7_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14749. CORTEX7_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.178 CORTEX7_CFG_0_ROM_REGISTER Register

14.8.1.2.178.1 CORTEX7_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-14750. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2EF8h

Figure 14-7249. CORTEX7_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-14751. CORTEX7_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.179 CORTEX7_CFG_0_ID_REGISTER Register

14.8.1.2.179.1 CORTEX7_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-14752. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2EFCh

Figure 14-7250. CORTEX7_CFG_0_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-14753. CORTEX7_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.180 CORTEX8_CFG_0_CSWREG Register

14.8.1.2.180.1 CORTEX8_CFG_0_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-14754. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2F00h

Figure 14-7251. CORTEX8_CFG_0_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-14755. CORTEX8_CFG_0_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.181 CORTEX8_CFG_0_DRWREG Register

14.8.1.2.181.1 CORTEX8_CFG_0_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-14756. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2F0Ch

Figure 14-7252. CORTEX8_CFG_0_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-14757. CORTEX8_CFG_0_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.182 CORTEX8_CFG_0_BD0REG Register

14.8.1.2.182.1 CORTEX8_CFG_0_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14758. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2F10h

Figure 14-7253. CORTEX8_CFG_0_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-14759. CORTEX8_CFG_0_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.183 CORTEX8_CFG_0_BD1REG Register

14.8.1.2.183.1 CORTEX8_CFG_0_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14760. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2F14h

Figure 14-7254. CORTEX8_CFG_0_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-14761. CORTEX8_CFG_0_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.184 CORTEX8_CFG_0_BD2REG Register

14.8.1.2.184.1 CORTEX8_CFG_0_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-14762. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2F18h

Figure 14-7255. CORTEX8_CFG_0_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-14763. CORTEX8_CFG_0_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.185 CORTEX8_CFG_0_BD3REG Register

14.8.1.2.185.1 CORTEX8_CFG_0_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-14764. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2F1Ch

Figure 14-7256. CORTEX8_CFG_0_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-14765. CORTEX8_CFG_0_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.186 CORTEX8_CFG_0_ROM_REGISTER Register

14.8.1.2.186.1 CORTEX8_CFG_0_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-14766. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2FF8h

Figure 14-7257. CORTEX8_CFG_0_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-14767. CORTEX8_CFG_0_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.187 CORTEX8_CFG_0_ID_REGISTER Register

14.8.1.2.187.1 CORTEX8_CFG_0_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-14768. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 0000 2FFCh

Figure 14-7258. CORTEX8_CFG_0_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14769. CORTEX8_CFG_0_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.188 ROM_TABLE_1_0_ROM_ENTRY0 Register

14.8.1.2.188.1 ROM_TABLE_1_0_ROM_ENTRY0 Register (Offset = 0h) [reset = 1003h]

rom table entry 0

Return to Summary Table

Table 14-14770. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0000h

Figure 14-7259. ROM_TABLE_1_0_ROM_ENTRY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-14771. ROM_TABLE_1_0_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.189 ROM_TABLE_1_0_ROM_ENTRY1 Register

14.8.1.2.189.1 ROM_TABLE_1_0_ROM_ENTRY1 Register (Offset = 4h) [reset = 2003h]

rom table entry 1

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Table 14-14772. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0004h

Figure 14-7260. ROM_TABLE_1_0_ROM_ENTRY1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">2h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">2h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-14773. ROM_TABLE_1_0_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.190 ROM_TABLE_1_0_ROM_ENTRY2 Register

14.8.1.2.190.1 ROM_TABLE_1_0_ROM_ENTRY2 Register (Offset = 8h) [reset = 3003h]

rom table entry 2

Return to Summary Table

Table 14-14774. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0008h

Figure 14-7261. ROM_TABLE_1_0_ROM_ENTRY2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">3h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">3h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">3h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-14775. ROM_TABLE_1_0_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	3h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.191 ROM_TABLE_1_0_ROM_ENTRY3 Register

14.8.1.2.191.1 ROM_TABLE_1_0_ROM_ENTRY3 Register (Offset = Ch) [reset = 4003h]

rom table entry 3

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Table 14-14776. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 000Ch

Figure 14-7262. ROM_TABLE_1_0_ROM_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	4h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
4h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
4h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-14777. ROM_TABLE_1_0_ROM_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	4h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.192 ROM_TABLE_1_0_ROM_ENTRY4 Register

14.8.1.2.192.1 ROM_TABLE_1_0_ROM_ENTRY4 Register (Offset = 10h) [reset = 5003h]

rom table entry 4

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Table 14-14778. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0010h

Figure 14-7263. ROM_TABLE_1_0_ROM_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	5h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
5h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
5h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-14779. ROM_TABLE_1_0_ROM_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	5h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.193 ROM_TABLE_1_0_ROM_ENTRY5 Register

14.8.1.2.193.1 ROM_TABLE_1_0_ROM_ENTRY5 Register (Offset = 14h) [reset = 1000003h]

rom table entry 5

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Table 14-14780. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0014h

Figure 14-7264. ROM_TABLE_1_0_ROM_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1000h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-14781. ROM_TABLE_1_0_ROM_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.194 ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register

14.8.1.2.194.1 ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register (Offset = 18h) [reset = 1000002h]

compute cluster rom table entry 0

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Table 14-14782. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0018h

Figure 14-7265. ROM_TABLE_1_0_COMPUTE_CLUSTER0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
1000h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14783. ROM_TABLE_1_0_COMPUTE_CLUSTER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.195 ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register

14.8.1.2.195.1 ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register (Offset = 1Ch) [reset = 1400002h]

compute cluster rom table entry 1

Return to Summary Table

Table 14-14784. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 001Ch

Figure 14-7266. ROM_TABLE_1_0_COMPUTE_CLUSTER1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1400h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1400h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1400h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14785. ROM_TABLE_1_0_COMPUTE_CLUSTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1400h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.196 ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register

14.8.1.2.196.1 ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register (Offset = 20h) [reset = 1800002h]

compute cluster rom table entry 2

Return to Summary Table

Table 14-14786. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0020h

Figure 14-7267. ROM_TABLE_1_0_COMPUTE_CLUSTER2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1800h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1800h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1800h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14787. ROM_TABLE_1_0_COMPUTE_CLUSTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1800h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.197 ROM_TABLE_1_0_DEBUG_CELL0 Register

14.8.1.2.197.1 ROM_TABLE_1_0_DEBUG_CELL0 Register (Offset = 24h) [reset = 1C00002h]

debug cell rom table entry 0

Return to Summary Table

Table 14-14788. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0024h

Figure 14-7268. ROM_TABLE_1_0_DEBUG_CELL0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C00h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C00h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C00h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14789. ROM_TABLE_1_0_DEBUG_CELL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.198 ROM_TABLE_1_0_DEBUG_CELL1 Register

14.8.1.2.198.1 ROM_TABLE_1_0_DEBUG_CELL1 Register (Offset = 28h) [reset = 1C10002h]

debug cell rom table entry 1

Return to Summary Table

Table 14-14790. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0028h

Figure 14-7269. ROM_TABLE_1_0_DEBUG_CELL1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C10h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C10h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14791. ROM_TABLE_1_0_DEBUG_CELL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.199 ROM_TABLE_1_0_DEBUG_CELL2 Register

14.8.1.2.199.1 ROM_TABLE_1_0_DEBUG_CELL2 Register (Offset = 2Ch) [reset = 1C20002h]

debug cell rom table entry 2

Return to Summary Table

Table 14-14792. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 002Ch

Figure 14-7270. ROM_TABLE_1_0_DEBUG_CELL2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1C20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1C20h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14793. ROM_TABLE_1_0_DEBUG_CELL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.200 ROM_TABLE_1_0_DEBUG_CELL3 Register

14.8.1.2.200.1 ROM_TABLE_1_0_DEBUG_CELL3 Register (Offset = 30h) [reset = 1C30002h]

debug cell rom table entry 3

Return to Summary Table

Table 14-14794. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0030h

Figure 14-7271. ROM_TABLE_1_0_DEBUG_CELL3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1C30h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C30h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1C30h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14795. ROM_TABLE_1_0_DEBUG_CELL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.201 ROM_TABLE_1_0_DEBUG_CELL4 Register

14.8.1.2.201.1 ROM_TABLE_1_0_DEBUG_CELL4 Register (Offset = 34h) [reset = 1C40002h]

debug cell rom table entry 4

Return to Summary Table

Table 14-14796. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0034h

Figure 14-7272. ROM_TABLE_1_0_DEBUG_CELL4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C40h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C40h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14797. ROM_TABLE_1_0_DEBUG_CELL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.202 ROM_TABLE_1_0_DEBUG_CELL5 Register

14.8.1.2.202.1 ROM_TABLE_1_0_DEBUG_CELL5 Register (Offset = 38h) [reset = 1C50002h]

debug cell rom table entry 5

Return to Summary Table

Table 14-14798. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0038h

Figure 14-7273. ROM_TABLE_1_0_DEBUG_CELL5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1C50h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C50h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1C50h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14799. ROM_TABLE_1_0_DEBUG_CELL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.203 ROM_TABLE_1_0_DEBUG_CELL6 Register

14.8.1.2.203.1 ROM_TABLE_1_0_DEBUG_CELL6 Register (Offset = 3Ch) [reset = 1C60002h]

debug cell rom table entry 6

Return to Summary Table

Table 14-14800. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 003Ch

Figure 14-7274. ROM_TABLE_1_0_DEBUG_CELL6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C60h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C60h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C60h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14801. ROM_TABLE_1_0_DEBUG_CELL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.204 ROM_TABLE_1_0_DEBUG_CELL7 Register

14.8.1.2.204.1 ROM_TABLE_1_0_DEBUG_CELL7 Register (Offset = 40h) [reset = 1C70002h]

debug cell rom table entry 7

Return to Summary Table

Table 14-14802. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0040h

Figure 14-7275. ROM_TABLE_1_0_DEBUG_CELL7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1C70h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C70h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1C70h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14803. ROM_TABLE_1_0_DEBUG_CELL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.205 ROM_TABLE_1_0_DEBUG_CELL8 Register

14.8.1.2.205.1 ROM_TABLE_1_0_DEBUG_CELL8 Register (Offset = 44h) [reset = 1C80002h]

debug cell rom table entry 8

Return to Summary Table

Table 14-14804. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0044h

Figure 14-7276. ROM_TABLE_1_0_DEBUG_CELL8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C80h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C80h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C80h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14805. ROM_TABLE_1_0_DEBUG_CELL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.206 ROM_TABLE_1_0_DEBUG_CELL9 Register

14.8.1.2.206.1 ROM_TABLE_1_0_DEBUG_CELL9 Register (Offset = 48h) [reset = 1C90002h]

debug cell rom table entry 9

Return to Summary Table

Table 14-14806. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0048h

Figure 14-7277. ROM_TABLE_1_0_DEBUG_CELL9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C90h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C90h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C90h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14807. ROM_TABLE_1_0_DEBUG_CELL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.207 ROM_TABLE_1_0_DEBUG_CELL10 Register

14.8.1.2.207.1 ROM_TABLE_1_0_DEBUG_CELL10 Register (Offset = 4Ch) [reset = 1CA0002h]

debug cell rom table entry 10

Return to Summary Table

Table 14-14808. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 004Ch

Figure 14-7278. ROM_TABLE_1_0_DEBUG_CELL10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1CA0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1CA0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1CA0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14809. ROM_TABLE_1_0_DEBUG_CELL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.208 ROM_TABLE_1_0_DEBUG_CELL11 Register

14.8.1.2.208.1 ROM_TABLE_1_0_DEBUG_CELL11 Register (Offset = 50h) [reset = 1CB0002h]

debug cell rom table entry 11

Return to Summary Table

Table 14-14810. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0050h

Figure 14-7279. ROM_TABLE_1_0_DEBUG_CELL11 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1CB0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1CB0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1CB0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14811. ROM_TABLE_1_0_DEBUG_CELL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.209 ROM_TABLE_1_0_EXTCSCOMP0 Register

14.8.1.2.209.1 ROM_TABLE_1_0_EXTCSCOMP0 Register (Offset = 50h) [reset = 1D00002h]

external coresight componenet rom table entry 0

Return to Summary Table

Table 14-14812. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0050h

Figure 14-7280. ROM_TABLE_1_0_EXTCSCOMP0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D00h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D00h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D00h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14813. ROM_TABLE_1_0_EXTCSCOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.210 ROM_TABLE_1_0_EXTCSCOMP1 Register

14.8.1.2.210.1 ROM_TABLE_1_0_EXTCSCOMP1 Register (Offset = 54h) [reset = 1D10002h]

external coresight componenet rom table entry 1

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Table 14-14814. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0054h

Figure 14-7281. ROM_TABLE_1_0_EXTCSCOMP1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D10h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D10h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14815. ROM_TABLE_1_0_EXTCSCOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.211 ROM_TABLE_1_0_EXTCSCOMP2 Register

14.8.1.2.211.1 ROM_TABLE_1_0_EXTCSCOMP2 Register (Offset = 58h) [reset = 1D20002h]

external coresight componenet rom table entry 2

Return to Summary Table

Table 14-14816. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0058h

Figure 14-7282. ROM_TABLE_1_0_EXTCSCOMP2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D20h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D20h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D20h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14817. ROM_TABLE_1_0_EXTCSCOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.212 ROM_TABLE_1_0_EXTCSCOMP3 Register

14.8.1.2.212.1 ROM_TABLE_1_0_EXTCSCOMP3 Register (Offset = 5Ch) [reset = 1D30002h]

external coresight componenet rom table entry 3

Return to Summary Table

Table 14-14818. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 005Ch

Figure 14-7283. ROM_TABLE_1_0_EXTCSCOMP3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D30h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D30h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D30h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14819. ROM_TABLE_1_0_EXTCSCOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.213 ROM_TABLE_1_0_EXTCSCOMP4 Register

14.8.1.2.213.1 ROM_TABLE_1_0_EXTCSCOMP4 Register (Offset = 60h) [reset = 1D40002h]

external coresight componenet rom table entry 4

Return to Summary Table

Table 14-14820. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0060h

Figure 14-7284. ROM_TABLE_1_0_EXTCSCOMP4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D40h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D40h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14821. ROM_TABLE_1_0_EXTCSCOMP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.214 ROM_TABLE_1_0_EXTCSCOMP5 Register

14.8.1.2.214.1 ROM_TABLE_1_0_EXTCSCOMP5 Register (Offset = 64h) [reset = 1D50002h]

external coresight componenet rom table entry 5

Return to Summary Table

Table 14-14822. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0064h

Figure 14-7285. ROM_TABLE_1_0_EXTCSCOMP5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D50h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D50h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D50h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14823. ROM_TABLE_1_0_EXTCSCOMP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.215 ROM_TABLE_1_0_EXTCSCOMP6 Register

14.8.1.2.215.1 ROM_TABLE_1_0_EXTCSCOMP6 Register (Offset = 68h) [reset = 1D60002h]

external coresight componenet rom table entry 6

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Table 14-14824. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0068h

Figure 14-7286. ROM_TABLE_1_0_EXTCSCOMP6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D60h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D60h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D60h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14825. ROM_TABLE_1_0_EXTCSCOMP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.216 ROM_TABLE_1_0_EXTCSCOMP7 Register

14.8.1.2.216.1 ROM_TABLE_1_0_EXTCSCOMP7 Register (Offset = 6Ch) [reset = 1D70002h]

external coresight componenet rom table entry 7

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Table 14-14826. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 006Ch

Figure 14-7287. ROM_TABLE_1_0_EXTCSCOMP7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D70h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D70h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D70h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14827. ROM_TABLE_1_0_EXTCSCOMP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.217 ROM_TABLE_1_0_EXTCSCOMP8 Register

14.8.1.2.217.1 ROM_TABLE_1_0_EXTCSCOMP8 Register (Offset = 70h) [reset = 1D80002h]

external coresight componenet rom table entry 8

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Table 14-14828. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0070h

Figure 14-7288. ROM_TABLE_1_0_EXTCSCOMP8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D80h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D80h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D80h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14829. ROM_TABLE_1_0_EXTCSCOMP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.218 ROM_TABLE_1_0_EXTCSCOMP9 Register

14.8.1.2.218.1 ROM_TABLE_1_0_EXTCSCOMP9 Register (Offset = 74h) [reset = 1D90002h]

external coresight componenet rom table entry 9

Return to Summary Table

Table 14-14830. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0074h

Figure 14-7289. ROM_TABLE_1_0_EXTCSCOMP9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D90h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D90h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D90h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-14831. ROM_TABLE_1_0_EXTCSCOMP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.219 ROM_TABLE_1_0_EXTCSCOMP10 Register

14.8.1.2.219.1 ROM_TABLE_1_0_EXTCSCOMP10 Register (Offset = 78h) [reset = 1DA0002h]

external coresight componenet rom table entry 10

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Table 14-14832. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 0078h

Figure 14-7290. ROM_TABLE_1_0_EXTCSCOMP10 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1DA0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1DA0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1DA0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14833. ROM_TABLE_1_0_EXTCSCOMP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.220 ROM_TABLE_1_0_EXTCSCOMP11 Register

14.8.1.2.220.1 ROM_TABLE_1_0_EXTCSCOMP11 Register (Offset = 7Ch) [reset = 1DB0002h]

external coresight componenet rom table entry 11

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Table 14-14834. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 007Ch

Figure 14-7291. ROM_TABLE_1_0_EXTCSCOMP11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1DB0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1DB0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1DB0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-14835. ROM_TABLE_1_0_EXTCSCOMP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.221 CSCTI_CTICONTROL Register

14.8.1.2.221.1 CSCTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register.

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Table 14-14836. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1000h

Figure 14-7292. CSCTI_CTICONTROL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>GLBEN</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14837. CSCTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	GLBEN	R/W	0h	Enables or disables the Embedded Cross Trigger, 1=enabled

14.8.1.2.222 CSCTI_CTIINTACK Register

14.8.1.2.222.1 CSCTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Interrupt Acknowledge Register.

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Table 14-14838. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1010h

Figure 14-7293. CSCTI_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-14839. CSCTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INTACK	R/W	0h	Acknowledges the corresponding CTITRIGOUT output Write 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW There is one bit of the register for each CTITRIGOUT output

14.8.1.2.223 CSCTI_CTIAPPSET Register

14.8.1.2.223.1 CSCTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register.

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Table 14-14840. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1014h

Figure 14-7294. CSCTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
R				R/W			
0h				0h			

Table 14-14841. CSCTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPSET	R/W	0h	The CTI Application Trigger Set Register is read/write A write to this register causes a channel event to be raised, corresponding to the bit written to

14.8.1.2.224 CSCTI_CTIAPPCLR Register

14.8.1.2.224.1 CSCTI_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register.

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Table 14-14842. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1018h

Figure 14-7295. CSCTI_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLR			
R				R/W			
0h				0h			

Table 14-14843. CSCTI_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPCLR	R/W	0h	The CTI Application Trigger Clear Register is write-only A write to this register causes a channel event to be cleared, corresponding to the bit written to

14.8.1.2.225 CSCTI_CTIAPPPULSE Register

14.8.1.2.225.1 CSCTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Trigger Pulse Register.

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Table 14-14844. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 101Ch

Figure 14-7296. CSCTI_CTIAPPPULSE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">APPPULSE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14845. CSCTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPPULSE	R/W	0h	The CTI Application Pulse Register is write-only A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to This register clears itself immediately

14.8.1.2.226 CSCTI_CTIINEN0 Register

14.8.1.2.226.1 CSCTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 0

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Table 14-14846. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1020h

Figure 14-7297. CSCTI_CTIINEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14847. CSCTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.227 CSCTI_CTIINEN1 Register

14.8.1.2.227.1 CSCTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 1

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Table 14-14848. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1024h

Figure 14-7298. CSCTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	TRIGINEN		
R				NONE	R/W		
0h				0h	0h		

Table 14-14849. CSCTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.228 CSCTI_CTIINEN2 Register

14.8.1.2.228.1 CSCTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 2

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Table 14-14850. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1028h

Figure 14-7299. CSCTI_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-14851. CSCTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.229 CSCTI_CTIINEN3 Register

14.8.1.2.229.1 CSCTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Application Trigger to Channel Enable Register 3

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Table 14-14852. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 102Ch

Figure 14-7300. CSCTI_CTIINEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-14853. CSCTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.230 CSCTI_CTIINEN4 Register

14.8.1.2.230.1 CSCTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 4

Return to Summary Table

Table 14-14854. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1030h

Figure 14-7301. CSCTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-14855. CSCTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.231 CSCTI_CTIINEN5 Register

14.8.1.2.231.1 CSCTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 5

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Table 14-14856. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1034h

Figure 14-7302. CSCTI_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-14857. CSCTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.232 CSCTI_CTIINEN6 Register

14.8.1.2.232.1 CSCTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 6

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Table 14-14858. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1038h

Figure 14-7303. CSCTI_CTIINEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-14859. CSCTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.233 CSCTI_CTIINEN7 Register

14.8.1.2.233.1 CSCTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Application Trigger to Channel Enable Register 7

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Table 14-14860. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 103Ch

Figure 14-7304. CSCTI_CTIINEN7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14861. CSCTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.234 CSCTI_CTIOUTEN0 Register

14.8.1.2.234.1 CSCTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Channel to Trigger Enable Register 0

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Table 14-14862. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10A0h

Figure 14-7305. CSCTI_CTIOUTEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14863. CSCTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.235 CSCTI_CTIOUTEN1 Register

14.8.1.2.235.1 CSCTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Channel to Trigger Enable Register 1

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Table 14-14864. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10A4h

Figure 14-7306. CSCTI_CTIOUTEN1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14865. CSCTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.236 CSCTI_CTIOUTEN2 Register

14.8.1.2.236.1 CSCTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Channel to Trigger Enable Register 2

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Table 14-14866. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10A8h

Figure 14-7307. CSCTI_CTIOUTEN2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGOUTEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14867. CSCTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.237 CSCTI_CTIOUTEN3 Register

14.8.1.2.237.1 CSCTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Channel to Trigger Enable Register 3

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Table 14-14868. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10ACh

Figure 14-7308. CSCTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-14869. CSCTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.238 CSCTI_CTIOUTEN4 Register

14.8.1.2.238.1 CSCTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Channel to Trigger Enable Register 4

Return to Summary Table

Table 14-14870. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10B0h

Figure 14-7309. CSCTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-14871. CSCTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.239 CSCTI_CTIOUTEN5 Register

14.8.1.2.239.1 CSCTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Channel to Trigger Enable Register 5

Return to Summary Table

Table 14-14872. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10B4h

Figure 14-7310. CSCTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-14873. CSCTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.240 CSCTI_CTIOUTEN6 Register

14.8.1.2.240.1 CSCTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Channel to Trigger Enable Register 6

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Table 14-14874. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10B8h

Figure 14-7311. CSCTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-14875. CSCTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.241 CSCTI_CTIOUTEN7 Register

14.8.1.2.241.1 CSCTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Channel to Trigger Enable Register 7

Return to Summary Table

Table 14-14876. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10BCh

Figure 14-7312. CSCTI_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-14877. CSCTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.242 CSCTI_CTITRIGINSTATUS Register

14.8.1.2.242.1 CSCTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

Return to Summary Table

Table 14-14878. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1130h

Figure 14-7313. CSCTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGINSTATUS							
R							
0h							

Table 14-14879. CSCTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGINSTATUS	R	0h	Shows the status of the CTITRIGIN inputs: 1=CTITRIGIN is active, 0=CTITRIGIN is inactive

14.8.1.2.243 CSCTI_CTITRIGOUTSTATUS Register

14.8.1.2.243.1 CSCTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

Return to Summary Table

Table 14-14880. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1134h

Figure 14-7314. CSCTI_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-14881. CSCTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the CTITRIGOUT outputs: 1=CTITRIGOUT is active, 0=CTITRIGOUT is inactive

14.8.1.2.244 CSCTI_CTICHINSTATUS Register

14.8.1.2.244.1 CSCTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

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Table 14-14882. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1138h

Figure 14-7315. CSCTI_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CHINSTATUS			
R				R			
0h				0h			

Table 14-14883. CSCTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHINSTATUS	R	0h	Shows the status of the CTICHIN inputs: 1=CTICHIN is active, 0=CTICHIN is inactive

14.8.1.2.245 CSCTI_CTICHOUTSTATUS Register

14.8.1.2.245.1 CSCTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

Return to Summary Table

Table 14-14884. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 113Ch

Figure 14-7316. CSCTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CHOUTSTATUS			
R				R			
0h				0h			

Table 14-14885. CSCTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHOUTSTATUS	R	0h	Shows the status of the CTICHOUT outputs: 1=CTICHOUT is active, 0=CTICHOUT is inactive

14.8.1.2.246 CSCTI_CTIGATE Register

14.8.1.2.246.1 CSCTI_CTIGATE Register (Offset = 140h) [reset = 0h]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs.

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Table 14-14886. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1140h

Figure 14-7317. CSCTI_CTIGATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CTIGATEEN			
R				R			
0h				0h			

Table 14-14887. CSCTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTIGATEEN	R	0h	Gate enable for the four channels [1 per bit]

14.8.1.2.247 CSCTI_ASICCTL Register

14.8.1.2.247.1 CSCTI_ASICCTL Register (Offset = 144h) [reset = 0h]

Allows external multiplexing of the trigger signals

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Table 14-14888. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1144h

Figure 14-7318. CSCTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-14889. CSCTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]

14.8.1.2.248 CSCTI_ITCHINACK Register

14.8.1.2.248.1 CSCTI_ITCHINACK Register (Offset = EDCh) [reset = 0h]

Integration and Test register

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Table 14-14890. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EDCh

Figure 14-7319. CSCTI_ITCHINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHINACK			
R				R/W			
0h				0h			

Table 14-14891. CSCTI_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHINACK	R/W	0h	Sets the value of the CTCHINACK outputs

14.8.1.2.249 CSCTI_ITTRIGINACK Register

14.8.1.2.249.1 CSCTI_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

ITTRIGINACK Register

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Table 14-14892. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EE0h

Figure 14-7320. CSCTI_ITTRIGINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGINACK							
R/W							
0h							

Table 14-14893. CSCTI_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGINACK	R/W	0h	Sets the value of the CTTRIGINACK outputs

14.8.1.2.250 CSCTI_ITCHOUT Register

14.8.1.2.250.1 CSCTI_ITCHOUT Register (Offset = EE4h) [reset = 0h]

ITCHOUT Register

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Table 14-14894. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EE4h

Figure 14-7321. CSCTI_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
R				R/W			
0h				0h			

Table 14-14895. CSCTI_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHOUT	R/W	0h	Sets the value of the CTCHOUT outputs

14.8.1.2.251 CSCTI_ITTRIGOUT Register

14.8.1.2.251.1 CSCTI_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

ITTRIGOUT Register

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Table 14-14896. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EE8h

Figure 14-7322. CSCTI_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-14897. CSCTI_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUT	R/W	0h	Sets the value of the CTTRIGOUT outputs

14.8.1.2.252 CSCTI_ITCHOUTACK Register

14.8.1.2.252.1 CSCTI_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

ITCHOUTACK Register

Return to Summary Table

Table 14-14898. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EECh

Figure 14-7323. CSCTI_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTCHOUTACK							
R/W							
0h							

Table 14-14899. CSCTI_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTCHOUTACK	R/W	0h	Sets the value of the CTCHOUTACK outputs

14.8.1.2.253 CSCTI_ITTRIGOUTACK Register

14.8.1.2.253.1 CSCTI_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

ITTRIGOUTACK Register

Return to Summary Table

Table 14-14900. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EF0h

Figure 14-7324. CSCTI_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTTRIGOUTACK							
R							
0h							

Table 14-14901. CSCTI_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUTACK	R	0h	Reads the value of the CTTRIGOUTACK inputs

14.8.1.2.254 CSCTI_ITCHIN Register

14.8.1.2.254.1 CSCTI_ITCHIN Register (Offset = EF4h) [reset = 0h]

ITCHIN Register

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Table 14-14902. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EF4h

Figure 14-7325. CSCTI_ITCHIN Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHIN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-14903. CSCTI_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHIN	R	0h	Reads the value of the CTCHIN inputs

14.8.1.2.255 CSCTI_ITTRIGIN Register

14.8.1.2.255.1 CSCTI_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

ITTRIGIN Register

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Table 14-14904. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EF8h

Figure 14-7326. CSCTI_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-14905. CSCTI_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGIN	R	0h	Reads the value of the CTTRIGIN inputs

14.8.1.2.256 CSCTI_ITCTRL Register

14.8.1.2.256.1 CSCTI_ITCTRL Register (Offset = F00h) [reset = 0h]

ITCTRL Register

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Table 14-14906. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1F00h

Figure 14-7327. CSCTI_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							ITEN
R							R/W
0h							0h

Table 14-14907. CSCTI_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	ITEN	R/W	0h	Integration Test control enable

14.8.1.2.257 CSCTI_CLAIMSET Register

14.8.1.2.257.1 CSCTI_CLAIMSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-14908. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FA0h

Figure 14-7328. CSCTI_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-14909. CSCTI_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.8.1.2.258 CSCTI_CLAIMCLR Register

14.8.1.2.258.1 CSCTI_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-14910. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FA4h

Figure 14-7329. CSCTI_CLAIMCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-14911. CSCTI_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.8.1.2.259 CSCTI_LOCKACCESS Register

14.8.1.2.259.1 CSCTI_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-14912. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FB0h

Figure 14-7330. CSCTI_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
LOCKACCESSREG							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKACCESSREG							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKACCESSREG							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKACCESSREG							
R/W							
0h							

Table 14-14913. CSCTI_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKACCESSREG	R/W	0h	Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers If paddrdbg31 is high, this is ignored

14.8.1.2.260 CSCTI_LOCKSTATUS Register

14.8.1.2.260.1 CSCTI_LOCKSTATUS Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-14914. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FB4h

Figure 14-7331. CSCTI_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-14915. CSCTI_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.8.1.2.261 CSCTI_AUTHSTATUS Register

14.8.1.2.261.1 CSCTI_AUTHSTATUS Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-14916. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FB8h

Figure 14-7332. CSCTI_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-14917. CSCTI_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.8.1.2.262 CSCTI_DEVID Register

14.8.1.2.262.1 CSCTI_DEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-14918. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FC8h

Figure 14-7333. CSCTI_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUM_ECT_CHANNELS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUM_ECT_TRIGGERS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED7_5</td><td colspan="5">IMPLEMENTATION_DEFINED</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-14919. CSCTI_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	R	0h	Reserved, returns 0
19:16	NUM_ECT_CHANNELS	R	0h	Number of ECT Channels available
15:8	NUM_ECT_TRIGGERS	R	0h	Number of ECT trigger available
7:5	RESERVED7_5	R	0h	Reserved, returns 0
4:0	IMPLEMENTATION_DEFINED	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Outputs using ASICCTL Defailt value of 0 indicates no multiplexing present

14.8.1.2.263 CSCTI_DEVTYPE Register

14.8.1.2.263.1 CSCTI_DEVTYPE Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

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Table 14-14920. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FCCh

Figure 14-7334. CSCTI_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-14921. CSCTI_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.8.1.2.264 CSCTI_PERIPHID4 Register

14.8.1.2.264.1 CSCTI_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

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Table 14-14922. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FD0h

Figure 14-7335. CSCTI_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERIPH_ID4							
R							
0h							

Table 14-14923. CSCTI_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.8.1.2.265 CSCTI_PERIPHID0 Register

14.8.1.2.265.1 CSCTI_PERIPHID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

Return to Summary Table

Table 14-14924. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FE0h

Figure 14-7336. CSCTI_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-14925. CSCTI_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.8.1.2.266 CSCTI_PERIPHID1 Register

14.8.1.2.266.1 CSCTI_PERIPHID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

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Table 14-14926. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FE4h

Figure 14-7337. CSCTI_PERIPHID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERIPH_ID1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14927. CSCTI_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.8.1.2.267 CSCTI_PERIPHID2 Register

14.8.1.2.267.1 CSCTI_PERIPHID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

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Table 14-14928. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FE8h

Figure 14-7338. CSCTI_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-14929. CSCTI_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.8.1.2.268 CSCTI_PERIPHID3 Register

14.8.1.2.268.1 CSCTI_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

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Table 14-14930. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FECh

Figure 14-7339. CSCTI_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERPIH_ID3							
R							
0h							

Table 14-14931. CSCTI_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.8.1.2.269 CSCTI_COMPONID0 Register

14.8.1.2.269.1 CSCTI_COMPONID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

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Table 14-14932. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FF0h

Figure 14-7340. CSCTI_COMPONID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-14933. CSCTI_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.270 CSCTI_COMPONID1 Register

14.8.1.2.270.1 CSCTI_COMPONID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

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Table 14-14934. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FF4h

Figure 14-7341. CSCTI_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-14935. CSCTI_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.271 CSCTI_COMPONID2 Register

14.8.1.2.271.1 CSCTI_COMPONID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

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Table 14-14936. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FF8h

Figure 14-7342. CSCTI_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-14937. CSCTI_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.272 CSCTI_COMPONID3 Register

14.8.1.2.272.1 CSCTI_COMPONID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

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Table 14-14938. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FFCh

Figure 14-7343. CSCTI_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-14939. CSCTI_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.273 DRM_CFG_0_PERIPH_ID Register

14.8.1.2.273.1 DRM_CFG_0_PERIPH_ID Register (Offset = 0h) [reset = 62836100h]

This register is used to determine what the functionality of this peripheral is.

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Table 14-14940. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2000h

Figure 14-7344. DRM_CFG_0_PERIPH_ID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">BU</td><td colspan="4">FUNCTION</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">2h</td><td colspan="4">283h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNCTION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">283h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTLREV</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">Ch</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 14-14941. DRM_CFG_0_PERIPH_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Peripheral ID Scheme [0]
29:28	BU	R	2h	Reserved, returns 0
27:16	FUNCTION	R	283h	DRM Function ID [0x211]
15:11	RTLREV	R	Ch	RTL Revision [0]
10:8	MAJOR	R	1h	Major Peripheral Revision [0]
7:6	CUSTOM	R	0h	Custon Peripheral ID version [0]
5:0	MINOR	R	0h	Minor Peripheral Revision [0]

14.8.1.2.274 DRM_CFG_0_VERSION Register

14.8.1.2.274.1 DRM_CFG_0_VERSION Register (Offset = 4h) [reset = 0h]

This register is used to enable the Time Generator. For application access, the DTG must be unlocked first.

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Table 14-14942. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2004h

Figure 14-7345. DRM_CFG_0_VERSION Name Register

31	30	29	28	27	26	25	24
MAJOR_VERSION							
R							
0h							
23	22	21	20	19	18	17	16
MAJOR_VERSION							
R							
0h							
15	14	13	12	11	10	9	8
MINOR_VERSION							
R							
0h							
7	6	5	4	3	2	1	0
MINOR_VERSION							
R							
0h							

Table 14-14943. DRM_CFG_0_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MAJOR_VERSION	R	0h	Contains the major version value [1]
15:0	MINOR_VERSION	R	0h	Contains the minor version value [0]

14.8.1.2.275 DRM_CFG_0_CAPABILITY Register

14.8.1.2.275.1 DRM_CFG_0_CAPABILITY Register (Offset = 8h) [reset = 0h]

This register can be read to determine the number of suspend signals and number of peripherals.

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Table 14-14944. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2008h

Figure 14-7346. DRM_CFG_0_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		NUM_SUSPENDS					
R		R					
0h		0h					
7	6	5	4	3	2	1	0
NUM_PERIPHERALS							
R							
0h							

Table 14-14945. DRM_CFG_0_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13:8	NUM_SUSPENDS	R	0h	Contains the number of Suspend signals supported, max of 32 There should be one signal per processor This value is set by a parameter at synthesis time
7:0	NUM_PERIPHERALS	R	0h	Contains the number of peripherals supported, max of 128 This affects the number of SUSPEND_REG registers This is set by a parameter during synthesis

14.8.1.2.276 DRM_CFG_0_TRACE_CTRL Register

14.8.1.2.276.1 DRM_CFG_0_TRACE_CTRL Register (Offset = Ch) [reset = 0h]

This register is used to set the trace sampling mode to center(1) or edge(0).

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Table 14-14946. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 200Ch

Figure 14-7347. DRM_CFG_0_TRACE_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>CENTER_SAMPLING</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-14947. DRM_CFG_0_TRACE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	CENTER_SAMPLING	R/W	0h	Sets trace to center sampled

14.8.1.2.277 DRM_CFG_0_VBUSM_CTRL Register

14.8.1.2.277.1 DRM_CFG_0_VBUSM_CTRL Register (Offset = 10h) [reset = 0h]

This register is used to set attributes on the VBUSM memory accesses and to read the Debug Operating Mode

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Table 14-14948. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2010h

Figure 14-7348. DRM_CFG_0_VBUSM_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DOM_INPUT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">DOM_INPUT</td><td colspan="5">RESERVED</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">VBUSM_PRIV</td><td>VBUSM_SECURE</td><td>VBUSM_DEBUG</td><td colspan="2">CTL_PRIV</td><td>CTL_SECURE</td><td>EMUDBG</td></tr>
<tr><td colspan="2">R</td><td>R</td><td>R</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-14949. DRM_CFG_0_VBUSM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	DOM_INPUT	R	0h	This returns the DOM security input The upper 3 bits are the debug operating mode and the lower 8 bits are the priviledge ID for VBUSM transaction
20:8	RESERVED	R	0h	Reserved bits, return 0
7:6	VBUSM_PRIV	R	0h	These two bits show the currently state of the priv bits
5	VBUSM_SECURE	R	0h	This bit shows the currently active state of the VBUSM secure bit
4	VBUSM_DEBUG	R	0h	This is the currently active state of the VBUSM emudbg bit
3:2	CTL_PRIV	R/W	0h	These two bits determine the priviledge type for VBUSM accesses unless overridden by the DOM input [0 is user level privilege, 1 is supervisor level privilege, 2 is hypervisor level privilege and 3 is reserved]
1	CTL_SECURE	R/W	0h	When set [and DOM permits it], the VBUSM accesses will have the secure bit set
0	EMUDBG	R/W	0h	Sets the emudbg bit during access to make the debug or non-debug

14.8.1.2.278 DRM_CFG_0_DAP_TIMEOUT Register

14.8.1.2.278.1 DRM_CFG_0_DAP_TIMEOUT Register (Offset = 14h) [reset = 0h]

This register is used to set the maximum wait time for the DAP to complete a memory access.

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Table 14-14950. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2014h

Figure 14-7349. DRM_CFG_0_DAP_TIMEOUT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DAP_TIMEOUT_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DAP_TIMEOUT_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DAP_TIMEOUT_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DAP_TIMEOUT_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14951. DRM_CFG_0_DAP_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAP_TIMEOUT_REGISTER	R/W	0h	

14.8.1.2.279 DRM_CFG_0_CONFIG Register

14.8.1.2.279.1 DRM_CFG_0_CONFIG Register (Offset = 18h) [reset = 0h]

This register adds softreset capability to the suspend module.

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Table 14-14952. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2018h

Figure 14-7350. DRM_CFG_0_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFTRESET
R							R/W
0h							0h

Table 14-14953. DRM_CFG_0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	Software controlled reset of the DRM

14.8.1.2.280 DRM_CFG_0_EMUTRIGEN Register

14.8.1.2.280.1 DRM_CFG_0_EMUTRIGEN Register (Offset = 1Ch) [reset = 0h]

This register is used to enable EMU triggers.

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Table 14-14954. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 201Ch

Figure 14-7351. DRM_CFG_0_EMUTRIGEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						EMU1TRIGEN	EMU0TRIGEN
R						R/W	R/W
0h						0h	0h

Table 14-14955. DRM_CFG_0_EMUTRIGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1	EMU1TRIGEN	R/W	0h	EMU 1 Trigger En
0	EMU0TRIGEN	R/W	0h	EMU 0 Trigger En

14.8.1.2.281 DRM_CFG_0_BINVALLO Register

14.8.1.2.281.1 DRM_CFG_0_BINVALLO Register (Offset = 20h) [reset = 0h]

Reading this register returns the lower 32 bits of the binary debug time.

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Table 14-14956. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2020h

Figure 14-7352. DRM_CFG_0_BINVALLO Name Register

31	30	29	28	27	26	25	24
DTG_BINARY_TIME_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
DTG_BINARY_TIME_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
DTG_BINARY_TIME_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
DTG_BINARY_TIME_LOW							
R/W							
0h							

Table 14-14957. DRM_CFG_0_BINVALLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DTG_BINARY_TIME_LOW	R/W	0h	

14.8.1.2.282 DRM_CFG_0_BINVALHI Register

14.8.1.2.282.1 DRM_CFG_0_BINVALHI Register (Offset = 24h) [reset = 0h]

Reading this register returns the upper 16 bits of the binary debug time and causes the lower 32 bits to be latched.

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Table 14-14958. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2024h

Figure 14-7353. DRM_CFG_0_BINVALHI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	BINTIMEHI						
NONE	R						
0h	0h						
7	6	5	4	3	2	1	0
BINTIMEHI							
R							
0h							

Table 14-14959. DRM_CFG_0_BINVALHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	BINTIMEHI	R	0h	Upper 16 bits of the timer

14.8.1.2.283 DRM_CFG_0_SUSPEND_REG0 Register

14.8.1.2.283.1 DRM_CFG_0_SUSPEND_REG0 Register (Offset = 200h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. There can be upto 128 of these registers (See NUM_PERIPHERALS in the DRM_CAPABILITY register)

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Table 14-14960. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2200h

Figure 14-7354. DRM_CFG_0_SUSPEND_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							SELECT
R							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELECT				RESERVED0			SUSPEND_CTL
R/W				R			R/W
0h				0h			0h

Table 14-14961. DRM_CFG_0_SUSPEND_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8:4	SELECT	R/W	0h	Selects which suspend control line [1-32] goes to the peripheral
3:1	RESERVED0	R	0h	Reserved, returns 0
0	SUSPEND_CTL	R/W	0h	When 1, the peripheral is sensitive to the suspend signal, when 0, it ignore it

14.8.1.2.284 DRM_CFG_0_SUSPEND_REG1 Register

14.8.1.2.284.1 DRM_CFG_0_SUSPEND_REG1 Register (Offset = 204h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14962. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2204h

Figure 14-7355. DRM_CFG_0_SUSPEND_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14963. DRM_CFG_0_SUSPEND_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_1	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.285 DRM_CFG_0_SUSPEND_REG2 Register

14.8.1.2.285.1 DRM_CFG_0_SUSPEND_REG2 Register (Offset = 208h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14964. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2208h

Figure 14-7356. DRM_CFG_0_SUSPEND_REG2 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SUSPEND_REG_2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SUSPEND_REG_2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUSPEND_REG_2							
R/W							
0h							

Table 14-14965. DRM_CFG_0_SUSPEND_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_2	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.286 DRM_CFG_0_SUSPEND_REG3 Register

14.8.1.2.286.1 DRM_CFG_0_SUSPEND_REG3 Register (Offset = 20Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14966. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 220Ch

Figure 14-7357. DRM_CFG_0_SUSPEND_REG3 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_3							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_3							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_3							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_3							
R/W							
0h							

Table 14-14967. DRM_CFG_0_SUSPEND_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_3	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.287 DRM_CFG_0_SUSPEND_REG4 Register

14.8.1.2.287.1 DRM_CFG_0_SUSPEND_REG4 Register (Offset = 210h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14968. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2210h

Figure 14-7358. DRM_CFG_0_SUSPEND_REG4 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_4							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_4							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_4							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_4							
R/W							
0h							

Table 14-14969. DRM_CFG_0_SUSPEND_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_4	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.288 DRM_CFG_0_SUSPEND_REG5 Register

14.8.1.2.288.1 DRM_CFG_0_SUSPEND_REG5 Register (Offset = 214h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14970. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2214h

Figure 14-7359. DRM_CFG_0_SUSPEND_REG5 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_5							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_5							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_5							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_5							
R/W							
0h							

Table 14-14971. DRM_CFG_0_SUSPEND_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_5	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.289 DRM_CFG_0_SUSPEND_REG6 Register

14.8.1.2.289.1 DRM_CFG_0_SUSPEND_REG6 Register (Offset = 218h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14972. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2218h

Figure 14-7360. DRM_CFG_0_SUSPEND_REG6 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_6							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_6							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_6							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_6							
R/W							
0h							

Table 14-14973. DRM_CFG_0_SUSPEND_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_6	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.290 DRM_CFG_0_SUSPEND_REG7 Register

14.8.1.2.290.1 DRM_CFG_0_SUSPEND_REG7 Register (Offset = 21Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14974. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 221Ch

Figure 14-7361. DRM_CFG_0_SUSPEND_REG7 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_7							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_7							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_7							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_7							
R/W							
0h							

Table 14-14975. DRM_CFG_0_SUSPEND_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_7	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.291 DRM_CFG_0_SUSPEND_REG8 Register

14.8.1.2.291.1 DRM_CFG_0_SUSPEND_REG8 Register (Offset = 220h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14976. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2220h

Figure 14-7362. DRM_CFG_0_SUSPEND_REG8 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_8							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_8							
R/W							
0h							

Table 14-14977. DRM_CFG_0_SUSPEND_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_8	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.292 DRM_CFG_0_SUSPEND_REG9 Register

14.8.1.2.292.1 DRM_CFG_0_SUSPEND_REG9 Register (Offset = 224h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14978. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2224h

Figure 14-7363. DRM_CFG_0_SUSPEND_REG9 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_9							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_9							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_9							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_9							
R/W							
0h							

Table 14-14979. DRM_CFG_0_SUSPEND_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_9	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.293 DRM_CFG_0_SUSPEND_REG10 Register

14.8.1.2.293.1 DRM_CFG_0_SUSPEND_REG10 Register (Offset = 228h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14980. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2228h

Figure 14-7364. DRM_CFG_0_SUSPEND_REG10 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_10							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_10							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_10							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_10							
R/W							
0h							

Table 14-14981. DRM_CFG_0_SUSPEND_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_10	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.294 DRM_CFG_0_SUSPEND_REG11 Register

14.8.1.2.294.1 DRM_CFG_0_SUSPEND_REG11 Register (Offset = 22Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14982. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 222Ch

Figure 14-7365. DRM_CFG_0_SUSPEND_REG11 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_11							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_11							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_11							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_11							
R/W							
0h							

Table 14-14983. DRM_CFG_0_SUSPEND_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_11	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.295 DRM_CFG_0_SUSPEND_REG12 Register

14.8.1.2.295.1 DRM_CFG_0_SUSPEND_REG12 Register (Offset = 230h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14984. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2230h

Figure 14-7366. DRM_CFG_0_SUSPEND_REG12 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_12</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14985. DRM_CFG_0_SUSPEND_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_12	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.296 DRM_CFG_0_SUSPEND_REG13 Register

14.8.1.2.296.1 DRM_CFG_0_SUSPEND_REG13 Register (Offset = 234h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14986. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2234h

Figure 14-7367. DRM_CFG_0_SUSPEND_REG13 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_13</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-14987. DRM_CFG_0_SUSPEND_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_13	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.297 DRM_CFG_0_SUSPEND_REG14 Register

14.8.1.2.297.1 DRM_CFG_0_SUSPEND_REG14 Register (Offset = 238h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14988. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2238h

Figure 14-7368. DRM_CFG_0_SUSPEND_REG14 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_14							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_14							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_14							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_14							
R/W							
0h							

Table 14-14989. DRM_CFG_0_SUSPEND_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_14	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.298 DRM_CFG_0_SUSPEND_REG15 Register

14.8.1.2.298.1 DRM_CFG_0_SUSPEND_REG15 Register (Offset = 23Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14990. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 223Ch

Figure 14-7369. DRM_CFG_0_SUSPEND_REG15 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_15							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_15							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_15							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_15							
R/W							
0h							

Table 14-14991. DRM_CFG_0_SUSPEND_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_15	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.299 DRM_CFG_0_SUSPEND_REG16 Register

14.8.1.2.299.1 DRM_CFG_0_SUSPEND_REG16 Register (Offset = 240h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14992. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2240h

Figure 14-7370. DRM_CFG_0_SUSPEND_REG16 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_16							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_16							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_16							
R/W							
0h							

Table 14-14993. DRM_CFG_0_SUSPEND_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_16	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.300 DRM_CFG_0_SUSPEND_REG17 Register

14.8.1.2.300.1 DRM_CFG_0_SUSPEND_REG17 Register (Offset = 244h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14994. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2244h

Figure 14-7371. DRM_CFG_0_SUSPEND_REG17 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_17							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_17							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_17							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_17							
R/W							
0h							

Table 14-14995. DRM_CFG_0_SUSPEND_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_17	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.301 DRM_CFG_0_SUSPEND_REG18 Register

14.8.1.2.301.1 DRM_CFG_0_SUSPEND_REG18 Register (Offset = 248h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14996. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2248h

Figure 14-7372. DRM_CFG_0_SUSPEND_REG18 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_18							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_18							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_18							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_18							
R/W							
0h							

Table 14-14997. DRM_CFG_0_SUSPEND_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_18	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.302 DRM_CFG_0_SUSPEND_REG19 Register

14.8.1.2.302.1 DRM_CFG_0_SUSPEND_REG19 Register (Offset = 24Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-14998. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 224Ch

Figure 14-7373. DRM_CFG_0_SUSPEND_REG19 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_19							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_19							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_19							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_19							
R/W							
0h							

Table 14-14999. DRM_CFG_0_SUSPEND_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_19	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.303 DRM_CFG_0_SUSPEND_REG20 Register

14.8.1.2.303.1 DRM_CFG_0_SUSPEND_REG20 Register (Offset = 250h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15000. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2250h

Figure 14-7374. DRM_CFG_0_SUSPEND_REG20 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_20							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SUSPEND_REG_20							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SUSPEND_REG_20							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUSPEND_REG_20							
R/W							
0h							

Table 14-15001. DRM_CFG_0_SUSPEND_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_20	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.304 DRM_CFG_0_SUSPEND_REG21 Register

14.8.1.2.304.1 DRM_CFG_0_SUSPEND_REG21 Register (Offset = 254h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15002. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2254h

Figure 14-7375. DRM_CFG_0_SUSPEND_REG21 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_21</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_21</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_21</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_21</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15003. DRM_CFG_0_SUSPEND_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_21	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.305 DRM_CFG_0_SUSPEND_REG22 Register

14.8.1.2.305.1 DRM_CFG_0_SUSPEND_REG22 Register (Offset = 258h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15004. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2258h

Figure 14-7376. DRM_CFG_0_SUSPEND_REG22 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_22							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_22							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_22							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_22							
R/W							
0h							

Table 14-15005. DRM_CFG_0_SUSPEND_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_22	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.306 DRM_CFG_0_SUSPEND_REG23 Register

14.8.1.2.306.1 DRM_CFG_0_SUSPEND_REG23 Register (Offset = 25Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15006. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 225Ch

Figure 14-7377. DRM_CFG_0_SUSPEND_REG23 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_23							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_23							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_23							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_23							
R/W							
0h							

Table 14-15007. DRM_CFG_0_SUSPEND_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_23	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.307 DRM_CFG_0_SUSPEND_REG24 Register

14.8.1.2.307.1 DRM_CFG_0_SUSPEND_REG24 Register (Offset = 260h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15008. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2260h

Figure 14-7378. DRM_CFG_0_SUSPEND_REG24 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_24							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_24							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_24							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_24							
R/W							
0h							

Table 14-15009. DRM_CFG_0_SUSPEND_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_24	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.308 DRM_CFG_0_SUSPEND_REG25 Register

14.8.1.2.308.1 DRM_CFG_0_SUSPEND_REG25 Register (Offset = 264h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15010. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2264h

Figure 14-7379. DRM_CFG_0_SUSPEND_REG25 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_25</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_25</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_25</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_25</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15011. DRM_CFG_0_SUSPEND_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_25	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.309 DRM_CFG_0_SUSPEND_REG26 Register

14.8.1.2.309.1 DRM_CFG_0_SUSPEND_REG26 Register (Offset = 268h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15012. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2268h

Figure 14-7380. DRM_CFG_0_SUSPEND_REG26 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_26							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_26							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_26							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_26							
R/W							
0h							

Table 14-15013. DRM_CFG_0_SUSPEND_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_26	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.310 DRM_CFG_0_SUSPEND_REG27 Register

14.8.1.2.310.1 DRM_CFG_0_SUSPEND_REG27 Register (Offset = 26Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15014. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 226Ch

Figure 14-7381. DRM_CFG_0_SUSPEND_REG27 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_27							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_27							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_27							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_27							
R/W							
0h							

Table 14-15015. DRM_CFG_0_SUSPEND_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_27	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.311 DRM_CFG_0_SUSPEND_REG28 Register

14.8.1.2.311.1 DRM_CFG_0_SUSPEND_REG28 Register (Offset = 270h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15016. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2270h

Figure 14-7382. DRM_CFG_0_SUSPEND_REG28 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_28							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_28							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_28							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_28							
R/W							
0h							

Table 14-15017. DRM_CFG_0_SUSPEND_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_28	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.312 DRM_CFG_0_SUSPEND_REG29 Register

14.8.1.2.312.1 DRM_CFG_0_SUSPEND_REG29 Register (Offset = 274h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15018. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2274h

Figure 14-7383. DRM_CFG_0_SUSPEND_REG29 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_29							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_29							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_29							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_29							
R/W							
0h							

Table 14-15019. DRM_CFG_0_SUSPEND_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_29	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.313 DRM_CFG_0_SUSPEND_REG30 Register

14.8.1.2.313.1 DRM_CFG_0_SUSPEND_REG30 Register (Offset = 278h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15020. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 2278h

Figure 14-7384. DRM_CFG_0_SUSPEND_REG30 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_30							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_30							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_30							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_30							
R/W							
0h							

Table 14-15021. DRM_CFG_0_SUSPEND_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_30	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.314 DRM_CFG_0_SUSPEND_REG31 Register

14.8.1.2.314.1 DRM_CFG_0_SUSPEND_REG31 Register (Offset = 27Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15022. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 227Ch

Figure 14-7385. DRM_CFG_0_SUSPEND_REG31 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_31</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15023. DRM_CFG_0_SUSPEND_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_31	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.315 CSTPIU_CFG_0_SUPPORTSIZE Register

14.8.1.2.315.1 CSTPIU_CFG_0_SUPPORTSIZE Register (Offset = 0h) [reset = FFFFFFFFh]

This register indicates how many trace pins are available for export. One pin per bit, right justified

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Table 14-15024. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4000h

Figure 14-7386. CSTPIU_CFG_0_SUPPORTSIZE Name Register

31	30	29	28	27	26	25	24
SUPPORTSIZEREG							
R							
FFFFFFFFh							
23	22	21	20	19	18	17	16
SUPPORTSIZEREG							
R							
FFFFFFFFh							
15	14	13	12	11	10	9	8
SUPPORTSIZEREG							
R							
FFFFFFFFh							
7	6	5	4	3	2	1	0
SUPPORTSIZEREG							
R							
FFFFFFFFh							

Table 14-15025. CSTPIU_CFG_0_SUPPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUPPORTSIZEREG	R	FFFFFFFFh	This register indicates how many trace pins are available for export. One pin per bit, right justified

14.8.1.2.316 CSTPIU_CFG_0_CURPORTSIZE Register

14.8.1.2.316.1 CSTPIU_CFG_0_CURPORTSIZE Register (Offset = 4h) [reset = 1h]

The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

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Table 14-15026. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4004h

Figure 14-7387. CSTPIU_CFG_0_CURPORTSIZE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CURRENTPORTSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CURRENTPORTSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CURRENTPORTSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CURRENTPORTSIZE</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">1h</td></tr>
</table>

Table 14-15027. CSTPIU_CFG_0_CURPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CURRENTPORTSIZE	R/W	1h	The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

14.8.1.2.317 CSTPIU_CFG_0_TRIGMODEREG Register

14.8.1.2.317.1 CSTPIU_CFG_0_TRIGMODEREG Register (Offset = 100h) [reset = 0h]

This register indicates the implemented Trigger Counter multipliers and other supported features of the trigger system

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Table 14-15028. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4100h

Figure 14-7388. CSTPIU_CFG_0_TRIGMODEREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED						TRGRUN	TRIGGERED
R						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED2							TCOUNT8
R							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED1			MUILTPLIERS				
R			R				
0h			0h				

Table 14-15029. CSTPIU_CFG_0_TRIGMODEREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17	TRGRUN	R	0h	Trigger Counter running. A trigger has occurred but the counter is not at zero.
16	TRIGGERED	R	0h	A trigger has occurred and the counter has reached zero.
15:9	RESERVED2	R	0h	Reserved, returns 0
8	TCOUNT8	R	0h	An 8-bit wide counter register implemented.
7:5	RESERVED1	R	0h	Reserved, returns 0
4:0	MUILTPLIERS	R	0h	Multiply the Trigger Counter by 2, 4, 16, 256, 64K supported. Each bit is a mpy value.

14.8.1.2.318 CSTPIU_CFG_0_TRIGCTRREG Register

14.8.1.2.318.1 CSTPIU_CFG_0_TRIGCTRREG Register (Offset = 104h) [reset = 0h]

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Table 14-15030. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4104h

Figure 14-7389. CSTPIU_CFG_0_TRIGCTRREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGCOUNT							
R/W							
0h							

Table 14-15031. CSTPIU_CFG_0_TRIGCTRREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGCOUNT	R/W	0h	8-bit counter value for the number of words to be output from the formatter before a trigger is inserted.

14.8.1.2.319 CSTPIU_CFG_0_TRIGMPYREG Register

14.8.1.2.319.1 CSTPIU_CFG_0_TRIGMPYREG Register (Offset = 108h) [reset = 0h]

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Table 14-15032. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4108h

Figure 14-7390. CSTPIU_CFG_0_TRIGMPYREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">MULTIPLIER</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-15033. CSTPIU_CFG_0_TRIGMPYREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4:0	MULTIPLIER	R/W	0h	Trigger multiply value bit0=x2, bit1=x4, bit2=x16, bit3=x256, bit4=x64K.

14.8.1.2.320 CSTPIU_CFG_0_SUPTESTPAT Register

14.8.1.2.320.1 CSTPIU_CFG_0_SUPTESTPAT Register (Offset = 200h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-15034. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4200h

Figure 14-7391. CSTPIU_CFG_0_SUPTESTPAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MODE</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td colspan="4">PATTERN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15035. CSTPIU_CFG_0_SUPTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R	0h	bit 16 is Timed Mode, bit 17 is continuous mode
15:4	RESERVED1	R	0h	Reserved, returns 0
3:0	PATTERN	R	0h	bit0=Walking 1 pattern, bit1=walking 0, bit2=AA/55 pattern, bit3=FF/00 pattern

14.8.1.2.321 CSTPIU_CFG_0_CURTESTPAT Register

14.8.1.2.321.1 CSTPIU_CFG_0_CURTESTPAT Register (Offset = 204h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-15036. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4204h

Figure 14-7392. CSTPIU_CFG_0_CURTESTPAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						MODE	
R						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1				RESERVED	PATTERN		
R				NONE	R/W		
0h				0h	0h		

Table 14-15037. CSTPIU_CFG_0_CURTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R/W	0h	Select the Pattern Timer Mode, see Supported Patterns reg
15:4	RESERVED1	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	PATTERN	R/W	0h	Select the pattern to run, set Supported Patterns Reg

14.8.1.2.322 CSTPIU_CFG_0_TESTPATCNT Register

14.8.1.2.322.1 CSTPIU_CFG_0_TESTPATCNT Register (Offset = 208h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-15038. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4208h

Figure 14-7393. CSTPIU_CFG_0_TESTPATCNT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PATTERNCOUNT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15039. CSTPIU_CFG_0_TESTPATCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PATTERNCOUNT	R/W	0h	Number of clocks a pattern should run before going to the next pattern

14.8.1.2.323 CSTPIU_CFG_0_FORMFLUSHSTAT Register

14.8.1.2.323.1 CSTPIU_CFG_0_FORMFLUSHSTAT Register (Offset = 300h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-15040. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4300h

Figure 14-7394. CSTPIU_CFG_0_FORMFLUSHSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCPRESENT	FTSTOPPED	FLINPROG
R					R	R	R
0h					0h	0h	0h

Table 14-15041. CSTPIU_CFG_0_FORMFLUSHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	TCPRESENT	R	0h	If this bit is set then TRACECTL is present. If no TRACECTL pin is present, then the data formatter must be used and only in continuous mode
1	FTSTOPPED	R	0h	Formatter stopped. The formatter has received a stop request signal and all trace data and post-amble has been output.
0	FLINPROG	R	0h	Flush In Progress. This is an indication of the current state of AFVALIDS.

14.8.1.2.324 CSTPIU_CFG_0_FORMFLUSHCTL Register

14.8.1.2.324.1 CSTPIU_CFG_0_FORMFLUSHCTL Register (Offset = 304h) [reset = 0h]

This register controls the generation of stop, trigger, and flush events.

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Table 14-15042. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4304h

Figure 14-7395. CSTPIU_CFG_0_FORMFLUSHCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		STOPTRIG	STOPFL	RESERVED3	TRIGFL	TRIGEVT	TRIGIN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	FONMAN	FONTRIG	FONFIIN	RESERVED1		ENFCONT	ENFTC
R	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-15043. CSTPIU_CFG_0_FORMFLUSHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13	STOPTRIG	R/W	0h	Stop the formatter after a Trigger Event is observed
12	STOPFL	R/W	0h	Stop the formatter after a flush completes [return of AFREADYS].
11	RESERVED3	R	0h	Reserved, returns 0
10	TRIGFL	R/W	0h	Indicates a trigger on Flush completion on AFREADYS being returned
9	TRIGEVT	R/W	0h	Indicate a trigger on a Trigger Event.
8	TRIGIN	R/W	0h	Indicate a trigger on TRIGIN being asserted.
7	RESERVED2	R	0h	Reserved, returns 0
6	FONMAN	R/W	0h	Manually generate a flush of the system. It is cleared when this flush has been serviced.
5	FONTRIG	R/W	0h	Generate flush using Trigger event
4	FONFIIN	R/W	0h	Generate flush using the FLUSHIN interface.
3:2	RESERVED1	R	0h	Reserved, returns 0
1	ENFCONT	R/W	0h	Continuous Formatting. Embed in trigger packets and indicate null cycles using Sync packets
0	ENFTC	R/W	0h	Enable Formatting. Do not embed Triggers into the formatted stream

14.8.1.2.325 CSTPIU_CFG_0_FORMSYNCCTR Register

14.8.1.2.325.1 CSTPIU_CFG_0_FORMSYNCCTR Register (Offset = 308h) [reset = 40h]

This counter is the number of formatter frames since the last synchronization packet of 128 bits, and is a 12-bit counter with a maximum count value of 4096

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Table 14-15044. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4308h

Figure 14-7396. CSTPIU_CFG_0_FORMSYNCCTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				CYCCOUNT			
R				R/W			
0h				40h			
7	6	5	4	3	2	1	0
CYCCOUNT							
R/W							
40h							

Table 14-15045. CSTPIU_CFG_0_FORMSYNCCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:0	CYCCOUNT	R/W	40h	12-bit counter value to indicate the number of complete frames between full sync packets.

14.8.1.2.326 CSTPIU_CFG_0_EXTCTLIN Register

14.8.1.2.326.1 CSTPIU_CFG_0_EXTCTLIN Register (Offset = 400h) [reset = 0h]

This register inputs data from an external port (if used)

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Table 14-15046. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4400h

Figure 14-7397. CSTPIU_CFG_0_EXTCTLIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_INPUT_REGISTER							
R							
0h							

Table 14-15047. CSTPIU_CFG_0_EXTCTLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	reserved, returns 0
7:0	EXCTL_PORT_INPUT_REGISTER	R	0h	

14.8.1.2.327 CSTPIU_CFG_0_EXTCTLOUT Register

14.8.1.2.327.1 CSTPIU_CFG_0_EXTCTLOUT Register (Offset = 404h) [reset = 0h]

This register is output to an external port (if used)

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Table 14-15048. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4404h

Figure 14-7398. CSTPIU_CFG_0_EXTCTLOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_OUTPUT_REGISTER							
R/W							
0h							

Table 14-15049. CSTPIU_CFG_0_EXTCTLOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	returns 0
7:0	EXCTL_PORT_OUTPUT_REGISTER	R/W	0h	

14.8.1.2.328 CSTPIU_CFG_0_ITTRFLINACK Register

14.8.1.2.328.1 CSTPIU_CFG_0_ITTRFLINACK Register (Offset = EE4h) [reset = 0h]

Integration Test Trigger In and Flush In Acknowledge.

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Table 14-15050. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4EE4h

Figure 14-7399. CSTPIU_CFG_0_ITTRFLINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						FLUSHINACK	TRIGINACK
W						W	W
0h						0h	0h

Table 14-15051. CSTPIU_CFG_0_ITTRFLINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	W	0h	Reserved, returns 0
1	FLUSHINACK	W	0h	Writing this register sets the value of FLUSHINACK. Reading it returns the value of FLUSHINACK.
0	TRIGINACK	W	0h	Writing this register sets the value of TRIGINACK. Reading it returns the value of TRIGINACK.

14.8.1.2.329 CSTPIU_CFG_0_ITTRFLIN Register

14.8.1.2.329.1 CSTPIU_CFG_0_ITTRFLIN Register (Offset = EE8h) [reset = 0h]

Integration Test Trigger In and Flush In Register.

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Table 14-15052. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4EE8h

Figure 14-7400. CSTPIU_CFG_0_ITTRFLIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED						FLUSHIN	TRIGIN
R						R	R
0h						0h	0h

Table 14-15053. CSTPIU_CFG_0_ITTRFLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1	FLUSHIN	R	0h	Reads the value of FlushIn
0	TRIGIN	R	0h	Reads the value of Trigin

14.8.1.2.330 CSTPIU_CFG_0_ITATBDATA0 Register

14.8.1.2.330.1 CSTPIU_CFG_0_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Integration Test ATB Data Register 0

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Table 14-15054. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4EECh

Figure 14-7401. CSTPIU_CFG_0_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			ATDATA_31	ATDATA_23	ATDATA_15	ATDATA_7	ATDATA_0
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h

Table 14-15055. CSTPIU_CFG_0_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
32:5	RESERVED	R	0h	return 0
4	ATDATA_31	R	0h	Reads the value of atdatas[31]
3	ATDATA_23	R	0h	Reads the value of atdatas[23]
2	ATDATA_15	R	0h	Reads the value of atdatas[15]
1	ATDATA_7	R	0h	Reads the value of atdatas[7]
0	ATDATA_0	R	0h	Reads the value of atdatas[0]

14.8.1.2.331 CSTPIU_CFG_0_ITATBCTR2 Register

14.8.1.2.331.1 CSTPIU_CFG_0_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Integration Test ATB Control Register 2.

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Table 14-15056. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4EF0h

Figure 14-7402. CSTPIU_CFG_0_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						AFVALID	ATREADY
R						W	W
0h						0h	0h

Table 14-15057. CSTPIU_CFG_0_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	return 0
1	AFVALID	W	0h	Sets the value of afvalid
0	ATREADY	W	0h	Sets the value of atready

14.8.1.2.332 CSTPIU_CFG_0_ITATBCTR1 Register

14.8.1.2.332.1 CSTPIU_CFG_0_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Integration Test ATB Control Register 1.

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Table 14-15058. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4EF4h

Figure 14-7403. CSTPIU_CFG_0_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	ATID						
R	R						
0h	0h						

Table 14-15059. CSTPIU_CFG_0_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	returns 0
6:0	ATID	R	0h	Reads the value of atids

14.8.1.2.333 CSTPIU_CFG_0_ITATBCTR0 Register

14.8.1.2.333.1 CSTPIU_CFG_0_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Integration Test ATB Control Register 0.

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Table 14-15060. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4EF8h

Figure 14-7404. CSTPIU_CFG_0_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED						ABYTES	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						AFREADY	ATVALID
NONE						R	R
0h						0h	0h

Table 14-15061. CSTPIU_CFG_0_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	R	0h	Reads return 0 Reads return 0
9:8	ABYTES	R	0h	Reads the value of the atbytess
7:2	RESERVED	NONE	0h	Reserved
1	AFREADY	R	0h	Reads the value of afreadys
0	ATVALID	R	0h	Reads the value of atvalids

14.8.1.2.334 CSTPIU_CFG_0_INTCTRL Register

14.8.1.2.334.1 CSTPIU_CFG_0_INTCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Register

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Table 14-15062. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4F00h

Figure 14-7405. CSTPIU_CFG_0_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							IME
R							R/W
0h							0h

Table 14-15063. CSTPIU_CFG_0_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	IME	R/W	0h	Integration Mode Enable.

14.8.1.2.335 CSTPIU_CFG_0_CTSET Register

14.8.1.2.335.1 CSTPIU_CFG_0_CTSET Register (Offset = FA0h) [reset = Fh]

Claim Tag Set Register

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Table 14-15064. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FA0h

Figure 14-7406. CSTPIU_CFG_0_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				Fh			

Table 14-15065. CSTPIU_CFG_0_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	Fh	Claim Tag Set Register

14.8.1.2.336 CSTPIU_CFG_0_CTCLR Register

14.8.1.2.336.1 CSTPIU_CFG_0_CTCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-15066. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FA4h

Figure 14-7407. CSTPIU_CFG_0_CTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-15067. CSTPIU_CFG_0_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.8.1.2.337 CSTPIU_CFG_0_LAREG Register

14.8.1.2.337.1 CSTPIU_CFG_0_LAREG Register (Offset = FB0h) [reset = 0h]

Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-15068. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FB0h

Figure 14-7408. CSTPIU_CFG_0_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
W							
0h							

Table 14-15069. CSTPIU_CFG_0_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	W	0h	

14.8.1.2.338 CSTPIU_CFG_0_LSREG Register

14.8.1.2.338.1 CSTPIU_CFG_0_LSREG Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-15070. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FB4h

Figure 14-7409. CSTPIU_CFG_0_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					NTT	LOCK_STATUS	SLI
R					R	R	R
0h					0h	0h	0h

Table 14-15071. CSTPIU_CFG_0_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	NTT	R	0h	Register size Indicator. Always 0. Indiates that the LAR is implemented as 32-bit
1	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked. Application must write to the LAREG to gain access.
0	SLI	R	0h	Software Lock Implemented. Indicates that a lock control mechanism is present from this interface

14.8.1.2.339 CSTPIU_CFG_0_AUTHST Register

14.8.1.2.339.1 CSTPIU_CFG_0_AUTHST Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-15072. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FB8h

Figure 14-7410. CSTPIU_CFG_0_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		0h		0h	

Table 14-15073. CSTPIU_CFG_0_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reads return 0
7:6	SNID	R	0h	Indicates the security level for Secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for Secure invasive debug
3:2	NSNID	R	0h	Indicates the security level for Non-secure non-invasive debug.
1:0	NSID	R	0h	Indicates the security level for Non-secure invasive debug.

14.8.1.2.340 CSTPIU_CFG_0_DEVID Register

14.8.1.2.340.1 CSTPIU_CFG_0_DEVID Register (Offset = FC8h) [reset = A0h]

This shows the characteristics of the TPIU

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Table 14-15074. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FC8h

Figure 14-7411. CSTPIU_CFG_0_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				SWOUARTNRZ	SWOMAN	TCLKDATA	FIFO_SIZE
R				R	R	R	R
0h				0h	0h	0h	2h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FIFO_SIZE		CLKRELAT	MUXNUM				
R		R	R				
2h		1h	0h				

Table 14-15075. CSTPIU_CFG_0_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11	SWOUARTNRZ	R	0h	Indicates Serial Wire Output [UART/NRZ] is not supported. Defaul = 0
10	SWOMAN	R	0h	Indicates Serial Wire Output [Manchester] is not supported. Default = 0
9	TCLKDATA	R	0h	Indicates trace clock + data is supported.
8:6	FIFO_SIZE	R	2h	FIFO size in powers of 2. A value of 2 gives a FIFO size of 4 entries, 16 bytes. Default is3'b010
5	CLKRELAT	R	1h	Indicates the relationship between ATCLK and TRACECLKIN. 0x1 indicates asynchronous.
4:0	MUXNUM	R	0h	When nonzero this value indicates the type/number of ATB multiplexing present on the input to the ATB. Currently only 0x00 is supported, that is, no multiplexing present.

14.8.1.2.341 CSTPIU_CFG_0_DEVTYPE Register

14.8.1.2.341.1 CSTPIU_CFG_0_DEVTYPE Register (Offset = FCCh) [reset = 11h]

Device Type Identifier Register

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Table 14-15076. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FCCh

Figure 14-7412. CSTPIU_CFG_0_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SUB				MAJOR			
R				R			
1h				1h			

Table 14-15077. CSTPIU_CFG_0_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:4	SUB	R	1h	Sub-classification of the type of the debug component as specified in the Arm Architecture Specification within the major classification as specified in the MAJOR field
3:0	MAJOR	R	1h	Major classification of the type of the debug component as specified in the Arm Architecture Specification for this debug and trace component

14.8.1.2.342 CSTPIU_CFG_0_PERID4 Register

14.8.1.2.342.1 CSTPIU_CFG_0_PERID4 Register (Offset = FD0h) [reset = 4h]

Peripheral ID4 Register

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Table 14-15078. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FD0h

Figure 14-7413. CSTPIU_CFG_0_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SIZE				DES_2			
R				R			
0h				4h			

Table 14-15079. CSTPIU_CFG_0_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:4	SIZE	R	0h	Always 0b0000. Indicates that the device only occupies 4KB memory
3:0	DES_2	R	4h	PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES2 identify the designer of the component

14.8.1.2.343 CSTPIU_CFG_0_PERID0 Register

14.8.1.2.343.1 CSTPIU_CFG_0_PERID0 Register (Offset = FE0h) [reset = 12h]

Peripheral ID0 Register

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Table 14-15080. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FE0h

Figure 14-7414. CSTPIU_CFG_0_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PART_0							
R							
12h							

Table 14-15081. CSTPIU_CFG_0_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PART_0	R	12h	Perpiheral ID 0, returns the 12-bit part number of the component.

14.8.1.2.344 CSTPIU_CFG_0_PERID1 Register

14.8.1.2.344.1 CSTPIU_CFG_0_PERID1 Register (Offset = FE4h) [reset = B9h]

Peripheral ID1 Register

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Table 14-15082. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FE4h

Figure 14-7415. CSTPIU_CFG_0_PERID1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">DES_0</td><td colspan="4">PART_1</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">Bh</td><td colspan="4">9h</td></tr>
</table>

Table 14-15083. CSTPIU_CFG_0_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:4	DES_0	R	Bh	return 0xB. Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component
3:0	PART_1	R	9h	Peripheral ID 1, returns 0x9

14.8.1.2.345 CSTPIU_CFG_0_PERID2 Register

14.8.1.2.345.1 CSTPIU_CFG_0_PERID2 Register (Offset = FE8h) [reset = 5Bh]

Peripheral ID2 Register

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Table 14-15084. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FE8h

Figure 14-7416. CSTPIU_CFG_0_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC	DES_1		
R				R	R		
5h				1h	3h		

Table 14-15085. CSTPIU_CFG_0_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:4	REVISION	R	5h	always return 0x5
3	JEDEC	R	1h	always return 1. Indicates that the JEDEC-assigned designer ID is used
2:0	DES_1	R	3h	Return 0x3. Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component

14.8.1.2.346 CSTPIU_CFG_0_PERID3 Register

14.8.1.2.346.1 CSTPIU_CFG_0_PERID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

Return to Summary Table

Table 14-15086. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FECh

Figure 14-7417. CSTPIU_CFG_0_PERID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">REVAND</td><td colspan="4">CMOD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15087. CSTPIU_CFG_0_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:4	REVAND	R	0h	return 0000. Indicates that there are no extra fixes to this component
3:0	CMOD	R	0h	Customer Modified. returns 0x00 to indicate that the customer has not modified this component.

14.8.1.2.347 CSTPIU_CFG_0_COMPID0 Register

14.8.1.2.347.1 CSTPIU_CFG_0_COMPID0 Register (Offset = FF0h) [reset = Dh]

Component ID0 Register

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Table 14-15088. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FF0h

Figure 14-7418. CSTPIU_CFG_0_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-15089. CSTPIU_CFG_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	PRMBL_0	R	Dh	Preamble_0. return 0xD. Component ID register contains bits 7:0 of the component ID

14.8.1.2.348 CSTPIU_CFG_0_COMPID1 Register

14.8.1.2.348.1 CSTPIU_CFG_0_COMPID1 Register (Offset = FF4h) [reset = 90h]

Component ID1 Register

Return to Summary Table

Table 14-15090. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FF4h

Figure 14-7419. CSTPIU_CFG_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-15091. CSTPIU_CFG_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:4	CLASS	R	9h	Return 0x9. Class of the component. Contain bits [15:12] of the component ID.
3:0	PRMBL_1	R	0h	Component ID register contains bits16:8 of the component ID

14.8.1.2.349 CSTPIU_CFG_0_COMPID2 Register

14.8.1.2.349.1 CSTPIU_CFG_0_COMPID2 Register (Offset = FF8h) [reset = 5h]

Component ID2 Register

Return to Summary Table

Table 14-15092. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FF8h

Figure 14-7420. CSTPIU_CFG_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
5h							

Table 14-15093. CSTPIU_CFG_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	5h	A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

14.8.1.2.350 CSTPIU_CFG_0_COMPID3 Register

14.8.1.2.350.1 CSTPIU_CFG_0_COMPID3 Register (Offset = FFCh) [reset = B1h]

Component ID3 Register

Return to Summary Table

Table 14-15094. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 4FFCh

Figure 14-7421. CSTPIU_CFG_0_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
B1h							

Table 14-15095. CSTPIU_CFG_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	B1h	A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

14.8.1.2.351 CTF_CFG_0_CSTFCTLREG Register

14.8.1.2.351.1 CTF_CFG_0_CSTFCTLREG Register (Offset = 0h) [reset = 0h]

It enables the target ports and defines the hold time of the target ports.

Return to Summary Table

Table 14-15096. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5000h

Figure 14-7422. CTF_CFG_0_CSTFCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				MINHOLDTIME			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
SLVPORTEN							
R/W							
0h							

Table 14-15097. CTF_CFG_0_CSTFCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:8	MINHOLDTIME	R/W	0h	Minimum Hold time Hold time refers to the number of transactions that are output on the funnel initiator port from the same target while that target port ATVALIDSx is HIGH The CSTF holds for the minimum hold time and one additional cycle The maximum value that can be entered is 0xE and this equates to 15 cycles 0xF is reserved
7:0	SLVPORTEN	R/W	0h	Target Port Enables Setting these bits enables the corresponding input, or target port If a bit is not set then this has the effect of excluding that port from the priority selection scheme

14.8.1.2.352 CTF_CFG_0_PRIORCTLREG Register

14.8.1.2.352.1 CTF_CFG_0_PRIORCTLREG Register (Offset = 4h) [reset = 0h]

Defines the order in which inputs are selected. This register must only be altered when the trace sources are off and the system is drained.

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Table 14-15098. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5004h

Figure 14-7423. CTF_CFG_0_PRIORCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
PRIPORT7			PRIPORT6			PRIPORT5	
R/W			R/W			R/W	
0h			0h			0h	
15	14	13	12	11	10	9	8
PRIPORT5	PRIPORT4			PRIPORT3			PRIPORT2
R/W	R/W			R/W			R/W
0h	0h			0h			0h
7	6	5	4	3	2	1	0
PRIPORT2		PRIPORT1			PRIPORT0		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-15099. CTF_CFG_0_PRIORCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23:21	PRIPORT7	R/W	0h	Priority value of the eighth target port Highest priority goes to the lowest value
20:18	PRIPORT6	R/W	0h	Priority value of the seventh target port Highest priority goes to the lowest value
17:15	PRIPORT5	R/W	0h	Priority value of the sixth target port Highest priority goes to the lowest value
14:12	PRIPORT4	R/W	0h	Priority value of the fifth target port Highest priority goes to the lowest value
11:9	PRIPORT3	R/W	0h	Priority value of the fourth target port Highest priority goes to the lowest value
8:6	PRIPORT2	R/W	0h	Priority value of the third target port Highest priority goes to the lowest value
5:3	PRIPORT1	R/W	0h	Priority value of the second target port Highest priority goes to the lowest value
2:0	PRIPORT0	R/W	0h	Priority value of the first target port Highest priority goes to the lowest value

14.8.1.2.353 CTF_CFG_0_ITATBDATA0 Register

14.8.1.2.353.1 CTF_CFG_0_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Integration Test Register.

Return to Summary Table

Table 14-15100. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5EECh

Figure 14-7424. CTF_CFG_0_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ATDATA31	ATDATA23	ATDATA15	ATDATA7	ATDATA0
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-15101. CTF_CFG_0_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4	ATDATA31	R/W	0h	A write outputs data on ATDATAM[31] A read returns the value of ATDATAS[31]
3	ATDATA23	R/W	0h	A write outputs data on ATDATAM[23] A read returns the value of ATDATAS[23]
2	ATDATA15	R/W	0h	A write outputs data on ATDATAM[15] A read returns the value of ATDATAS[15]
1	ATDATA7	R/W	0h	A write outputs data on ATDATAM[7] A read returns the value of ATDATAS[7]
0	ATDATA0	R/W	0h	A write outputs data on ATDATAM[0] A read returns the value of ATDATAS[0]

14.8.1.2.354 CTF_CFG_0_ITATBCTR2 Register

14.8.1.2.354.1 CTF_CFG_0_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Integration Test Control Register 2.

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Table 14-15102. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5EF0h

Figure 14-7425. CTF_CFG_0_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED		AFVALID	ATREADY
R				NONE		R/W	R/W
0h				0h		0h	0h

Table 14-15103. CTF_CFG_0_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:2	RESERVED	NONE	0h	Reserved
1	AFVALID	R/W	0h	Reading this bit returns the value of AFVALIDM Writing this bit sets the AFVALIDS[n] bit where n is enabled by the CSTFCTLREG
0	ATREADY	R/W	0h	Reading this bit returns the value of ATREADYM Writing this bit sets the AFREADYS[n] bit where n is enabled by the CSTFCTLREG

14.8.1.2.355 CTF_CFG_0_ITATBCTR1 Register

14.8.1.2.355.1 CTF_CFG_0_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Integration Test Control Register 1.

Return to Summary Table

Table 14-15104. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5EF4h

Figure 14-7426. CTF_CFG_0_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	ATID					
R	NONE	R/W					
0h	0h	0h					

Table 14-15105. CTF_CFG_0_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6	RESERVED	NONE	0h	Reserved
5:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.8.1.2.356 CTF_CFG_0_ITATBCTR0 Register

14.8.1.2.356.1 CTF_CFG_0_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Integration Test Control Register 0.

Return to Summary Table

Table 14-15106. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5EF8h

Figure 14-7427. CTF_CFG_0_ITATBCTR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED1</td><td colspan="2">ATBYTES</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>AFREADY</td><td>ATVALID</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15107. CTF_CFG_0_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED1	R	0h	Reserved, returns 0
9:8	ATBYTES	R/W	0h	Writing this field sets the value of ATBYTESM Reading it returns the value of ATBYTSS[n]
7:2	RESERVED	R	0h	Reserved, returns 0
1	AFREADY	R/W	0h	Writing this field sets the value of AFREADYM Reading it returns the value of AFREADYS[n]
0	ATVALID	R/W	0h	Writing this field sets the value of ATVALIDM Reading it returns the value of ATVALIDS[n]

14.8.1.2.357 CTF_CFG_0_INTCTRL Register

14.8.1.2.357.1 CTF_CFG_0_INTCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Register

Return to Summary Table

Table 14-15108. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5F00h

Figure 14-7428. CTF_CFG_0_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-15109. CTF_CFG_0_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.8.1.2.358 CTF_CFG_0_CTSET Register

14.8.1.2.358.1 CTF_CFG_0_CTSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

Return to Summary Table

Table 14-15110. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FA0h

Figure 14-7429. CTF_CFG_0_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-15111. CTF_CFG_0_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.8.1.2.359 CTF_CFG_0_CTCLR Register

14.8.1.2.359.1 CTF_CFG_0_CTCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

Return to Summary Table

Table 14-15112. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FA4h

Figure 14-7430. CTF_CFG_0_CTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-15113. CTF_CFG_0_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.8.1.2.360 CTF_CFG_0_LAREG Register

14.8.1.2.360.1 CTF_CFG_0_LAREG Register (Offset = FB0h) [reset = 0h]

Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-15114. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FB0h

Figure 14-7431. CTF_CFG_0_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
R/W							
0h							

Table 14-15115. CTF_CFG_0_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.8.1.2.361 CTF_CFG_0_LSREG Register

14.8.1.2.361.1 CTF_CFG_0_LSREG Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-15116. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FB4h

Figure 14-7432. CTF_CFG_0_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-15117. CTF_CFG_0_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.8.1.2.362 CTF_CFG_0_AUTHST Register

14.8.1.2.362.1 CTF_CFG_0_AUTHST Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-15118. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FB8h

Figure 14-7433. CTF_CFG_0_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-15119. CTF_CFG_0_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.8.1.2.363 CTF_CFG_0_DEVID Register

14.8.1.2.363.1 CTF_CFG_0_DEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-15120. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FC8h

Figure 14-7434. CTF_CFG_0_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PRIOTITY_SCHEME				PORTCOUNT			
R				R			
0h				0h			

Table 14-15121. CTF_CFG_0_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, return 0s
7:4	PRIOTITY_SCHEME	R	0h	The CSTF implements a static priority scheme Value = 0x2
3:0	PORTCOUNT	R	0h	This is the value of the Verilog define PORTCOUNT and represents the number of input ports connected By default all 8 ports are connected 0x0 and 0x1 are illegal values

14.8.1.2.364 CTF_CFG_0_DEVTYPEID Register

14.8.1.2.364.1 CTF_CFG_0_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

Return to Summary Table

Table 14-15122. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FCCh

Figure 14-7435. CTF_CFG_0_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-15123. CTF_CFG_0_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	A value of 0x12 identifies this device as a trace link [0x2] and specifically as a funnel/router [0x1]

14.8.1.2.365 CTF_CFG_0_PERID4 Register

14.8.1.2.365.1 CTF_CFG_0_PERID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

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Table 14-15124. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FD0h

Figure 14-7436. CTF_CFG_0_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-15125. CTF_CFG_0_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.8.1.2.366 CTF_CFG_0_PERID5 Register

14.8.1.2.366.1 CTF_CFG_0_PERID5 Register (Offset = FD4h) [reset = 0h]

Peripheral ID5 Register

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Table 14-15126. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FD4h

Figure 14-7437. CTF_CFG_0_PERID5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID5							
R							
0h							

Table 14-15127. CTF_CFG_0_PERID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID5	R	0h	Peripheral ID 5, returns 0x0

14.8.1.2.367 CTF_CFG_0_PERID6 Register

14.8.1.2.367.1 CTF_CFG_0_PERID6 Register (Offset = FD8h) [reset = 0h]

Peripheral ID6 Register

Return to Summary Table

Table 14-15128. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FD8h

Figure 14-7438. CTF_CFG_0_PERID6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID6							
R							
0h							

Table 14-15129. CTF_CFG_0_PERID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID6	R	0h	Peripheral ID 6, returns 0x0

14.8.1.2.368 CTF_CFG_0_PERID7 Register

14.8.1.2.368.1 CTF_CFG_0_PERID7 Register (Offset = FDCh) [reset = 0h]

Peripheral ID7 Register

Return to Summary Table

Table 14-15130. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FDCh

Figure 14-7439. CTF_CFG_0_PERID7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID7							
R							
0h							

Table 14-15131. CTF_CFG_0_PERID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID7	R	0h	Peripheral ID 7, returns 0x0

14.8.1.2.369 CTF_CFG_0_PERID0 Register

14.8.1.2.369.1 CTF_CFG_0_PERID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

Return to Summary Table

Table 14-15132. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FE0h

Figure 14-7440. CTF_CFG_0_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-15133. CTF_CFG_0_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.8.1.2.370 CTF_CFG_0_PERID1 Register

14.8.1.2.370.1 CTF_CFG_0_PERID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

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Table 14-15134. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FE4h

Figure 14-7441. CTF_CFG_0_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-15135. CTF_CFG_0_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.8.1.2.371 CTF_CFG_0_PERID2 Register

14.8.1.2.371.1 CTF_CFG_0_PERID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

Return to Summary Table

Table 14-15136. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FE8h

Figure 14-7442. CTF_CFG_0_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-15137. CTF_CFG_0_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.8.1.2.372 CTF_CFG_0_PERID3 Register

14.8.1.2.372.1 CTF_CFG_0_PERID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

Return to Summary Table

Table 14-15138. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FECh

Figure 14-7443. CTF_CFG_0_PERID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERPIH_ID3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15139. CTF_CFG_0_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.8.1.2.373 CTF_CFG_0_COMPID0 Register

14.8.1.2.373.1 CTF_CFG_0_COMPID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

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Table 14-15140. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FF0h

Figure 14-7444. CTF_CFG_0_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-15141. CTF_CFG_0_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.374 CTF_CFG_0_COMPID1 Register

14.8.1.2.374.1 CTF_CFG_0_COMPID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

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Table 14-15142. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FF4h

Figure 14-7445. CTF_CFG_0_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-15143. CTF_CFG_0_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.375 CTF_CFG_0_COMPID2 Register

14.8.1.2.375.1 CTF_CFG_0_COMPID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

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Table 14-15144. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FF8h

Figure 14-7446. CTF_CFG_0_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-15145. CTF_CFG_0_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.376 CTF_CFG_0_COMPID3 Register

14.8.1.2.376.1 CTF_CFG_0_COMPID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

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Table 14-15146. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 2000 5FFCh

Figure 14-7447. CTF_CFG_0_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-15147. CTF_CFG_0_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.377 ROM_TABLE_0_1_ROM_ENTRY0 Register

14.8.1.2.377.1 ROM_TABLE_0_1_ROM_ENTRY0 Register (Offset = 0h) [reset = 2003h]

rom table entry 0

Return to Summary Table

Table 14-15148. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0000h

Figure 14-7448. ROM_TABLE_0_1_ROM_ENTRY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">2h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">2h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">2h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-15149. ROM_TABLE_0_1_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.378 ROM_TABLE_0_1_ROM_ENTRY1 Register

14.8.1.2.378.1 ROM_TABLE_0_1_ROM_ENTRY1 Register (Offset = 4h) [reset = 2000003h]

rom table entry 1

Return to Summary Table

Table 14-15150. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0004h

Figure 14-7449. ROM_TABLE_0_1_ROM_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2000h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
2000h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
2000h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-15151. ROM_TABLE_0_1_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.379 ROM_TABLE_0_1_ROM_ENTRY2 Register

14.8.1.2.379.1 ROM_TABLE_0_1_ROM_ENTRY2 Register (Offset = 8h) [reset = 3h]

rom table entry 2

Return to Summary Table

Table 14-15152. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0008h

Figure 14-7450. ROM_TABLE_0_1_ROM_ENTRY2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">RESERVED</td></tr>
<tr><td>R</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">NONE</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-15153. ROM_TABLE_0_1_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	RESERVED	NONE	0h	Reserved
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.380 ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register

14.8.1.2.380.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register (Offset = 8h) [reset = 10h]

rom table manual entry 0

Return to Summary Table

Table 14-15154. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0008h

Figure 14-7451. ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15155. ROM_TABLE_0_1_ROM_MANUAL_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.381 ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register

14.8.1.2.381.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register (Offset = Ch) [reset = 10h]

rom table manual entry 1

Return to Summary Table

Table 14-15156. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 000Ch

Figure 14-7452. ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15157. ROM_TABLE_0_1_ROM_MANUAL_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.382 ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register

14.8.1.2.382.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register (Offset = 10h) [reset = 10h]

rom table manual entry 2

Return to Summary Table

Table 14-15158. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0010h

Figure 14-7453. ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15159. ROM_TABLE_0_1_ROM_MANUAL_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.383 ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register

14.8.1.2.383.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register (Offset = 14h) [reset = 10h]

rom table manual entry 3

Return to Summary Table

Table 14-15160. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0014h

Figure 14-7454. ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15161. ROM_TABLE_0_1_ROM_MANUAL_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.384 ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register

14.8.1.2.384.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register (Offset = 18h) [reset = 10h]

rom table manual entry 4

Return to Summary Table

Table 14-15162. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0018h

Figure 14-7455. ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15163. ROM_TABLE_0_1_ROM_MANUAL_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.385 ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register

14.8.1.2.385.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register (Offset = 1Ch) [reset = 10h]

rom table manual entry 5

Return to Summary Table

Table 14-15164. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 001Ch

Figure 14-7456. ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15165. ROM_TABLE_0_1_ROM_MANUAL_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.386 ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register

14.8.1.2.386.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register (Offset = 20h) [reset = 10h]

rom table manual entry 6

Return to Summary Table

Table 14-15166. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0020h

Figure 14-7457. ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15167. ROM_TABLE_0_1_ROM_MANUAL_ENTRY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.387 ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register

14.8.1.2.387.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register (Offset = 24h) [reset = 10h]

rom table manual entry 7

Return to Summary Table

Table 14-15168. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0024h

Figure 14-7458. ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15169. ROM_TABLE_0_1_ROM_MANUAL_ENTRY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.388 ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register

14.8.1.2.388.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register (Offset = 28h) [reset = 10h]

rom table manual entry 8

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Table 14-15170. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0028h

Figure 14-7459. ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15171. ROM_TABLE_0_1_ROM_MANUAL_ENTRY8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.389 ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register

14.8.1.2.389.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register (Offset = 2Ch) [reset = 10h]

rom table manual entry 9

Return to Summary Table

Table 14-15172. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 002Ch

Figure 14-7460. ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15173. ROM_TABLE_0_1_ROM_MANUAL_ENTRY9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.390 ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register

14.8.1.2.390.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register (Offset = 30h) [reset = 10h]

rom table manual entry 10

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Table 14-15174. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0030h

Figure 14-7461. ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15175. ROM_TABLE_0_1_ROM_MANUAL_ENTRY10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.391 ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register

14.8.1.2.391.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register (Offset = 34h) [reset = 10h]

rom table manual entry 11

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Table 14-15176. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0034h

Figure 14-7462. ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15177. ROM_TABLE_0_1_ROM_MANUAL_ENTRY11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.392 ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register

14.8.1.2.392.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register (Offset = 38h) [reset = 10h]

rom table manual entry 12

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Table 14-15178. Instance Table

Instance Name	**Physical Address**
DEBUGSS_WRAP0	0007 4000 0038h

Figure 14-7463. ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15179. ROM_TABLE_0_1_ROM_MANUAL_ENTRY12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.393 ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register

14.8.1.2.393.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register (Offset = 3Ch) [reset = 10h]

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Return to Summary Table

Table 14-15180. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 003Ch

Figure 14-7464. ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15181. ROM_TABLE_0_1_ROM_MANUAL_ENTRY13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.394 ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register

14.8.1.2.394.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register (Offset = 40h) [reset = 10h]

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Table 14-15182. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0040h

Figure 14-7465. ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15183. ROM_TABLE_0_1_ROM_MANUAL_ENTRY14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.395 ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register

14.8.1.2.395.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register (Offset = 44h) [reset = 10h]

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Table 14-15184. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0044h

Figure 14-7466. ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15185. ROM_TABLE_0_1_ROM_MANUAL_ENTRY15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.396 ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register

14.8.1.2.396.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register (Offset = 48h) [reset = 10h]

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Return to Summary Table

Table 14-15186. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0048h

Figure 14-7467. ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15187. ROM_TABLE_0_1_ROM_MANUAL_ENTRY16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.397 ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register

14.8.1.2.397.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register (Offset = 4Ch) [reset = 10h]

rom table manual entry 17

Return to Summary Table

Table 14-15188. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 004Ch

Figure 14-7468. ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15189. ROM_TABLE_0_1_ROM_MANUAL_ENTRY17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.398 ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register

14.8.1.2.398.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register (Offset = 50h) [reset = 10h]

rom table manual entry 18

Return to Summary Table

Table 14-15190. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0050h

Figure 14-7469. ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15191. ROM_TABLE_0_1_ROM_MANUAL_ENTRY18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.399 ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register

14.8.1.2.399.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register (Offset = 54h) [reset = 10h]

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Table 14-15192. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0054h

Figure 14-7470. ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15193. ROM_TABLE_0_1_ROM_MANUAL_ENTRY19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.400 ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register

14.8.1.2.400.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register (Offset = 58h) [reset = 10h]

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Table 14-15194. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0058h

Figure 14-7471. ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15195. ROM_TABLE_0_1_ROM_MANUAL_ENTRY20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.401 ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register

14.8.1.2.401.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register (Offset = 5Ch) [reset = 10h]

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Table 14-15196. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 005Ch

Figure 14-7472. ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15197. ROM_TABLE_0_1_ROM_MANUAL_ENTRY21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.402 ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register

14.8.1.2.402.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register (Offset = 60h) [reset = 10h]

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Table 14-15198. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0060h

Figure 14-7473. ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15199. ROM_TABLE_0_1_ROM_MANUAL_ENTRY22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.403 ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register

14.8.1.2.403.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register (Offset = 64h) [reset = 10h]

rom table manual entry 23

Return to Summary Table

Table 14-15200. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0064h

Figure 14-7474. ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15201. ROM_TABLE_0_1_ROM_MANUAL_ENTRY23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.404 ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register

14.8.1.2.404.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register (Offset = 68h) [reset = 10h]

rom table manual entry 24

Return to Summary Table

Table 14-15202. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0068h

Figure 14-7475. ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15203. ROM_TABLE_0_1_ROM_MANUAL_ENTRY24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.405 ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register

14.8.1.2.405.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register (Offset = 6Ch) [reset = 10h]

rom table manual entry 25

Return to Summary Table

Table 14-15204. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 006Ch

Figure 14-7476. ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15205. ROM_TABLE_0_1_ROM_MANUAL_ENTRY25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.406 ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register

14.8.1.2.406.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register (Offset = 70h) [reset = 10h]

rom table manual entry 26

Return to Summary Table

Table 14-15206. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0070h

Figure 14-7477. ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15207. ROM_TABLE_0_1_ROM_MANUAL_ENTRY26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.407 ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register

14.8.1.2.407.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register (Offset = 74h) [reset = 10h]

rom table manual entry 27

Return to Summary Table

Table 14-15208. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0074h

Figure 14-7478. ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15209. ROM_TABLE_0_1_ROM_MANUAL_ENTRY27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.408 ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register

14.8.1.2.408.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register (Offset = 78h) [reset = 10h]

rom table manual entry 28

Return to Summary Table

Table 14-15210. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0078h

Figure 14-7479. ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15211. ROM_TABLE_0_1_ROM_MANUAL_ENTRY28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.409 ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register

14.8.1.2.409.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register (Offset = 7Ch) [reset = 10h]

rom table manual entry 29

Return to Summary Table

Table 14-15212. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 007Ch

Figure 14-7480. ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15213. ROM_TABLE_0_1_ROM_MANUAL_ENTRY29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.410 ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register

14.8.1.2.410.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register (Offset = 80h) [reset = 10h]

rom table manual entry 30

Return to Summary Table

Table 14-15214. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0080h

Figure 14-7481. ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15215. ROM_TABLE_0_1_ROM_MANUAL_ENTRY30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.411 ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register

14.8.1.2.411.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register (Offset = 84h) [reset = 10h]

rom table manual entry 31

Return to Summary Table

Table 14-15216. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0084h

Figure 14-7482. ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15217. ROM_TABLE_0_1_ROM_MANUAL_ENTRY31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.412 ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register

14.8.1.2.412.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register (Offset = 88h) [reset = 10h]

rom table manual entry 32

Return to Summary Table

Table 14-15218. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0088h

Figure 14-7483. ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15219. ROM_TABLE_0_1_ROM_MANUAL_ENTRY32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.413 ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register

14.8.1.2.413.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register (Offset = 8Ch) [reset = 10h]

rom table manual entry 33

Return to Summary Table

Table 14-15220. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 008Ch

Figure 14-7484. ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15221. ROM_TABLE_0_1_ROM_MANUAL_ENTRY33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.414 ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register

14.8.1.2.414.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register (Offset = 90h) [reset = 10h]

rom table manual entry 34

Return to Summary Table

Table 14-15222. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0090h

Figure 14-7485. ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15223. ROM_TABLE_0_1_ROM_MANUAL_ENTRY34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.415 ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register

14.8.1.2.415.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register (Offset = 94h) [reset = 10h]

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Table 14-15224. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0094h

Figure 14-7486. ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15225. ROM_TABLE_0_1_ROM_MANUAL_ENTRY35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.416 ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register

14.8.1.2.416.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register (Offset = 98h) [reset = 10h]

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Table 14-15226. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0098h

Figure 14-7487. ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15227. ROM_TABLE_0_1_ROM_MANUAL_ENTRY36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.417 ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register

14.8.1.2.417.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register (Offset = 9Ch) [reset = 10h]

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Table 14-15228. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 009Ch

Figure 14-7488. ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15229. ROM_TABLE_0_1_ROM_MANUAL_ENTRY37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.418 ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register

14.8.1.2.418.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register (Offset = A0h) [reset = 10h]

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Table 14-15230. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00A0h

Figure 14-7489. ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15231. ROM_TABLE_0_1_ROM_MANUAL_ENTRY38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.419 ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register

14.8.1.2.419.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register (Offset = A4h) [reset = 10h]

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Table 14-15232. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00A4h

Figure 14-7490. ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15233. ROM_TABLE_0_1_ROM_MANUAL_ENTRY39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.420 ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register

14.8.1.2.420.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register (Offset = A8h) [reset = 10h]

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Table 14-15234. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00A8h

Figure 14-7491. ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15235. ROM_TABLE_0_1_ROM_MANUAL_ENTRY40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.421 ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register

14.8.1.2.421.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register (Offset = ACh) [reset = 10h]

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Table 14-15236. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00ACh

Figure 14-7492. ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15237. ROM_TABLE_0_1_ROM_MANUAL_ENTRY41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.422 ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register

14.8.1.2.422.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register (Offset = B0h) [reset = 10h]

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Table 14-15238. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00B0h

Figure 14-7493. ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15239. ROM_TABLE_0_1_ROM_MANUAL_ENTRY42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.423 ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register

14.8.1.2.423.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register (Offset = B4h) [reset = 10h]

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Table 14-15240. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00B4h

Figure 14-7494. ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15241. ROM_TABLE_0_1_ROM_MANUAL_ENTRY43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.424 ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register

14.8.1.2.424.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register (Offset = B8h) [reset = 10h]

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Table 14-15242. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00B8h

Figure 14-7495. ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15243. ROM_TABLE_0_1_ROM_MANUAL_ENTRY44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.425 ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register

14.8.1.2.425.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register (Offset = BCh) [reset = 10h]

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Table 14-15244. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00BCh

Figure 14-7496. ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15245. ROM_TABLE_0_1_ROM_MANUAL_ENTRY45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.426 ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register

14.8.1.2.426.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register (Offset = C0h) [reset = 10h]

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Table 14-15246. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00C0h

Figure 14-7497. ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15247. ROM_TABLE_0_1_ROM_MANUAL_ENTRY46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.427 ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register

14.8.1.2.427.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register (Offset = C4h) [reset = 10h]

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Table 14-15248. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00C4h

Figure 14-7498. ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15249. ROM_TABLE_0_1_ROM_MANUAL_ENTRY47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.428 ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register

14.8.1.2.428.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register (Offset = C8h) [reset = 10h]

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Table 14-15250. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00C8h

Figure 14-7499. ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15251. ROM_TABLE_0_1_ROM_MANUAL_ENTRY48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.429 ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register

14.8.1.2.429.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register (Offset = CCh) [reset = 10h]

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Table 14-15252. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00CCh

Figure 14-7500. ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>RESERVED</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>NONE</td></tr>
<tr><td colspan="4">1h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15253. ROM_TABLE_0_1_ROM_MANUAL_ENTRY49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.430 ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register

14.8.1.2.430.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register (Offset = D0h) [reset = 10h]

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Table 14-15254. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00D0h

Figure 14-7501. ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15255. ROM_TABLE_0_1_ROM_MANUAL_ENTRY50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.431 ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register

14.8.1.2.431.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register (Offset = D4h) [reset = 10h]

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Table 14-15256. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00D4h

Figure 14-7502. ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15257. ROM_TABLE_0_1_ROM_MANUAL_ENTRY51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.432 ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register

14.8.1.2.432.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register (Offset = D8h) [reset = 10h]

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Table 14-15258. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00D8h

Figure 14-7503. ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15259. ROM_TABLE_0_1_ROM_MANUAL_ENTRY52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.433 ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register

14.8.1.2.433.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register (Offset = DCh) [reset = 10h]

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Table 14-15260. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00DCh

Figure 14-7504. ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15261. ROM_TABLE_0_1_ROM_MANUAL_ENTRY53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.434 ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register

14.8.1.2.434.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register (Offset = E0h) [reset = 10h]

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Table 14-15262. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00E0h

Figure 14-7505. ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15263. ROM_TABLE_0_1_ROM_MANUAL_ENTRY54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.435 ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register

14.8.1.2.435.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register (Offset = E4h) [reset = 10h]

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Table 14-15264. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00E4h

Figure 14-7506. ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15265. ROM_TABLE_0_1_ROM_MANUAL_ENTRY55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.436 ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register

14.8.1.2.436.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register (Offset = E8h) [reset = 10h]

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Table 14-15266. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00E8h

Figure 14-7507. ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15267. ROM_TABLE_0_1_ROM_MANUAL_ENTRY56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.437 ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register

14.8.1.2.437.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register (Offset = ECh) [reset = 10h]

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Table 14-15268. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00ECh

Figure 14-7508. ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15269. ROM_TABLE_0_1_ROM_MANUAL_ENTRY57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.438 ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register

14.8.1.2.438.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register (Offset = F0h) [reset = 10h]

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Table 14-15270. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00F0h

Figure 14-7509. ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15271. ROM_TABLE_0_1_ROM_MANUAL_ENTRY58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.439 ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register

14.8.1.2.439.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register (Offset = F4h) [reset = 10h]

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Table 14-15272. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00F4h

Figure 14-7510. ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15273. ROM_TABLE_0_1_ROM_MANUAL_ENTRY59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.440 ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register

14.8.1.2.440.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register (Offset = F8h) [reset = 10h]

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Table 14-15274. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00F8h

Figure 14-7511. ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15275. ROM_TABLE_0_1_ROM_MANUAL_ENTRY60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.441 ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register

14.8.1.2.441.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register (Offset = FCh) [reset = 10h]

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Table 14-15276. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 00FCh

Figure 14-7512. ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15277. ROM_TABLE_0_1_ROM_MANUAL_ENTRY61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.442 ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register

14.8.1.2.442.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register (Offset = 100h) [reset = 10h]

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Table 14-15278. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0100h

Figure 14-7513. ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15279. ROM_TABLE_0_1_ROM_MANUAL_ENTRY62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.443 ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register

14.8.1.2.443.1 ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register (Offset = 104h) [reset = 10h]

rom table manual entry 63

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Table 14-15280. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0104h

Figure 14-7514. ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	RESERVED
R				R	R	R	NONE
1h				0h	0h	0h	0h

Table 14-15281. ROM_TABLE_0_1_ROM_MANUAL_ENTRY63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	1h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	0h	always read as 1
0	RESERVED	NONE	0h	Reserved

14.8.1.2.444 ROM_TABLE_0_1_PERIPHID0 Register

14.8.1.2.444.1 ROM_TABLE_0_1_PERIPHID0 Register (Offset = 108h) [reset = 2h]

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Table 14-15282. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0108h

Figure 14-7515. ROM_TABLE_0_1_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15283. ROM_TABLE_0_1_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.445 ROM_TABLE_0_1_PERIPHID1 Register

14.8.1.2.445.1 ROM_TABLE_0_1_PERIPHID1 Register (Offset = 10Ch) [reset = 2h]

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Table 14-15284. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 010Ch

Figure 14-7516. ROM_TABLE_0_1_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15285. ROM_TABLE_0_1_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.446 ROM_TABLE_0_1_PERIPHID2 Register

14.8.1.2.446.1 ROM_TABLE_0_1_PERIPHID2 Register (Offset = 110h) [reset = 2h]

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Table 14-15286. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0110h

Figure 14-7517. ROM_TABLE_0_1_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15287. ROM_TABLE_0_1_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.447 ROM_TABLE_0_1_PERIPHID3 Register

14.8.1.2.447.1 ROM_TABLE_0_1_PERIPHID3 Register (Offset = 114h) [reset = 2h]

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Table 14-15288. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0114h

Figure 14-7518. ROM_TABLE_0_1_PERIPHID3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15289. ROM_TABLE_0_1_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.448 ROM_TABLE_0_1_PERIPHID4 Register

14.8.1.2.448.1 ROM_TABLE_0_1_PERIPHID4 Register (Offset = 118h) [reset = 2h]

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Table 14-15290. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 0118h

Figure 14-7519. ROM_TABLE_0_1_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
0h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
0h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15291. ROM_TABLE_0_1_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.449 ROM_TABLE_0_1_COMPID0 Register

14.8.1.2.449.1 ROM_TABLE_0_1_COMPID0 Register (Offset = 3FCh) [reset = Dh]

component id

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Table 14-15292. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 03FCh

Figure 14-7520. ROM_TABLE_0_1_COMPID0 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
Dh							
23	22	21	20	19	18	17	16
VAR							
R							
Dh							
15	14	13	12	11	10	9	8
VAR							
R							
Dh							
7	6	5	4	3	2	1	0
VAR							
R							
Dh							

Table 14-15293. ROM_TABLE_0_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	Dh	Component id0

14.8.1.2.450 ROM_TABLE_0_1_COMPID1 Register

14.8.1.2.450.1 ROM_TABLE_0_1_COMPID1 Register (Offset = 3FCh) [reset = 10h]

component id

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Table 14-15294. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 03FCh

Figure 14-7521. ROM_TABLE_0_1_COMPID1 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
10h							
23	22	21	20	19	18	17	16
VAR							
R							
10h							
15	14	13	12	11	10	9	8
VAR							
R							
10h							
7	6	5	4	3	2	1	0
VAR							
R							
10h							

Table 14-15295. ROM_TABLE_0_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	10h	Component id1

14.8.1.2.451 ROM_TABLE_0_1_COMPID2 Register

14.8.1.2.451.1 ROM_TABLE_0_1_COMPID2 Register (Offset = 3FCh) [reset = 5h]

component id

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Table 14-15296. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 03FCh

Figure 14-7522. ROM_TABLE_0_1_COMPID2 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
5h							
23	22	21	20	19	18	17	16
VAR							
R							
5h							
15	14	13	12	11	10	9	8
VAR							
R							
5h							
7	6	5	4	3	2	1	0
VAR							
R							
5h							

Table 14-15297. ROM_TABLE_0_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	5h	Component id2

14.8.1.2.452 ROM_TABLE_0_1_COMPID3 Register

14.8.1.2.452.1 ROM_TABLE_0_1_COMPID3 Register (Offset = 3FCh) [reset = B1h]

component id

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Table 14-15298. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 03FCh

Figure 14-7523. ROM_TABLE_0_1_COMPID3 Name Register

31	30	29	28	27	26	25	24
VAR							
R							
B1h							
23	22	21	20	19	18	17	16
VAR							
R							
B1h							
15	14	13	12	11	10	9	8
VAR							
R							
B1h							
7	6	5	4	3	2	1	0
VAR							
R							
B1h							

Table 14-15299. ROM_TABLE_0_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAR	R	B1h	Component id3

14.8.1.2.453 CFGAP_CFG_1_JTAGID_REG Register

14.8.1.2.453.1 CFGAP_CFG_1_JTAGID_REG Register (Offset = 0h) [reset = 0h]

This register returns the JTAG ID tieoff of the device. The reset value depends on the tie off

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Table 14-15300. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2000h

Figure 14-7524. CFGAP_CFG_1_JTAGID_REG Name Register

31	30	29	28	27	26	25	24
JTAG_ID							
R							
0h							
23	22	21	20	19	18	17	16
JTAG_ID							
R							
0h							
15	14	13	12	11	10	9	8
JTAG_ID							
R							
0h							
7	6	5	4	3	2	1	0
JTAG_ID							
R							
0h							

Table 14-15301. CFGAP_CFG_1_JTAGID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	JTAG_ID	R	0h	The JTAG ID of the device

14.8.1.2.454 CFGAP_CFG_1_USERID_REG Register

14.8.1.2.454.1 CFGAP_CFG_1_USERID_REG Register (Offset = 4h) [reset = 0h]

This register returns the Chip Spin ID tieoff value of the device. The reset value depends on the tieoff

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Table 14-15302. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2004h

Figure 14-7525. CFGAP_CFG_1_USERID_REG Name Register

31	30	29	28	27	26	25	24
USER_ID							
R							
0h							
23	22	21	20	19	18	17	16
USER_ID							
R							
0h							
15	14	13	12	11	10	9	8
USER_ID							
R							
0h							
7	6	5	4	3	2	1	0
USER_ID							
R							
0h							

Table 14-15303. CFGAP_CFG_1_USERID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USER_ID	R	0h	The USER ID of the device

14.8.1.2.455 CFGAP_CFG_1_VERSION_REG Register

14.8.1.2.455.1 CFGAP_CFG_1_VERSION_REG Register (Offset = 8h) [reset = 0h]

This register is used to read the RTL version information and to determine which modules are included in the rtl build. The reset value depends on the build options

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Table 14-15304. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2008h

Figure 14-7526. CFGAP_CFG_1_VERSION_REG Name Register

31	30	29	28	27	26	25	24
MAJOR_REV				MINOR_REV			
R				R			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							JTAG_AP
R							R
0h							0h
7	6	5	4	3	2	1	0
POWERAP	AXIAP	APBAP	SECURITYAP	SPARE	ICEPICKM	TRIGGERSUPPORT	TRACESUPPORT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-15305. CFGAP_CFG_1_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	MAJOR_REV	R	0h	RTL Major revision [5]
27:24	MINOR_REV	R	0h	RTL Minor revision [0]
23:9	RESERVED	R	0h	Reserved, returns 0
8	JTAG_AP	R	0h	a 1 indicates JTAG AP is supported
7	POWERAP	R	0h	A 1 indicates that the Power AP is supported
6	AXIAP	R	0h	A 1 indicates that the AXIAP exists and system memory accesses are supported
5	APBAP	R	0h	A 1 indicates that the APBAP exisits and accesses to external debug logic are supported
4	SECURITYAP	R	0h	A 1 indicates that the Security AP is supported
3	SPARE	R	0h	This is a spare bit, returns 0
2	ICEPICKM	R	0h	A 1 indicates that ICEPick M is present inthe design
1	TRIGGERSUPPORT	R	0h	A 1 indicates that cross triggering is supported
0	TRACESUPPORT	R	0h	A 1 indicates that hardware trace export is supported

14.8.1.2.456 CFGAP_CFG_1_APID_REGISTER Register

14.8.1.2.456.1 CFGAP_CFG_1_APID_REGISTER Register (Offset = FCh) [reset = 20E0001h]

Reading this register returns the ID information for this AP.

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Table 14-15306. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 20FCh

Figure 14-7527. CFGAP_CFG_1_APID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				107h			
23	22	21	20	19	18	17	16
JEP_CODE							CLASS
R							R
107h							0h
15	14	13	12	11	10	9	8
SPARE							
R							
0h							
7	6	5	4	3	2	1	0
VARIANT				TYPE			
R				R			
0h				1h			

Table 14-15307. CFGAP_CFG_1_APID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	107h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	1h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.457 APBAP_CFG_1_CSWREG Register

14.8.1.2.457.1 APBAP_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

Control/Status Register

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Table 14-15308. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2100h

Figure 14-7528. APBAP_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-15309. APBAP_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.458 APBAP_CFG_1_DRWREG Register

14.8.1.2.458.1 APBAP_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-15310. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 210Ch

Figure 14-7529. APBAP_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15311. APBAP_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.459 APBAP_CFG_1_BD0REG Register

14.8.1.2.459.1 APBAP_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15312. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2110h

Figure 14-7530. APBAP_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15313. APBAP_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.460 APBAP_CFG_1_BD1REG Register

14.8.1.2.460.1 APBAP_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15314. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2114h

Figure 14-7531. APBAP_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15315. APBAP_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.461 APBAP_CFG_1_BD2REG Register

14.8.1.2.461.1 APBAP_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15316. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2118h

Figure 14-7532. APBAP_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15317. APBAP_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.462 APBAP_CFG_1_BD3REG Register

14.8.1.2.462.1 APBAP_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15318. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 211Ch

Figure 14-7533. APBAP_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15319. APBAP_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.463 APBAP_CFG_1_ROM_REGISTER Register

14.8.1.2.463.1 APBAP_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the APB ROM Address.

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Table 14-15320. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 21F8h

Figure 14-7534. APBAP_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER_ADDRESS							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER_ADDRESS							
R							
0h							

Table 14-15321. APBAP_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER_ADDRESS	R	0h	Reading this register returns the APB ROM Address

14.8.1.2.464 APBAP_CFG_1_ID_REGISTER Register

14.8.1.2.464.1 APBAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-15322. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 21FCh

Figure 14-7535. APBAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15323. APBAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.8.1.2.465 AXIAP_CFG_1_CSWREG Register

14.8.1.2.465.1 AXIAP_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This is the control/status register

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Table 14-15324. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2200h

Figure 14-7536. AXIAP_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
DBGSWEN	TYPEEXT						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPIDEN	RESERVED2						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TYPE				MODE			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRINPROG	RESERVED1	ADDR_INC		RESERVED0	SIZE		
R	R	R/W		R	R		
0h	0h	0h		0h	0h		

Table 14-15325. AXIAP_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBGSWEN	R/W	0h	Indicates whether accesses should treated as application or debug
30:24	TYPEEXT	R/W	0h	
23	SPIDEN	R	0h	When 1, secure accesses are enabled
22:16	RESERVED2	R	0h	Reserved, reads return 0
15:12	TYPE	R/W	0h	Sets Prot, Type attributes for the access
11:8	MODE	R/W	0h	Sets mode of operation 0000=basic, 0001=Barrier extensions, all other values reserved
7	TRINPROG	R	0h	This bit is set to 1 while a transfer is in progress on the connection to the memory system, and is set to 0 while the connection is idle
6	RESERVED1	R	0h	This bit is reserved and reads return 0
5:4	ADDR_INC	R/W	0h	Address Auto Increment and packing mode
3	RESERVED0	R	0h	reserved, returns 0
2:0	SIZE	R	0h	This specifies the size of the access For this implementation, the access is always 32 bits [010]

14.8.1.2.466 AXIAP_CFG_1_DRWREG Register

14.8.1.2.466.1 AXIAP_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-15326. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 220Ch

Figure 14-7537. AXIAP_CFG_1_DRWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15327. AXIAP_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.467 AXIAP_CFG_1_BD0REG Register

14.8.1.2.467.1 AXIAP_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15328. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2210h

Figure 14-7538. AXIAP_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15329. AXIAP_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.468 AXIAP_CFG_1_BD1REG Register

14.8.1.2.468.1 AXIAP_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15330. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2214h

Figure 14-7539. AXIAP_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15331. AXIAP_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.469 AXIAP_CFG_1_BD2REG Register

14.8.1.2.469.1 AXIAP_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15332. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2218h

Figure 14-7540. AXIAP_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15333. AXIAP_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.470 AXIAP_CFG_1_BD3REG Register

14.8.1.2.470.1 AXIAP_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15334. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 221Ch

Figure 14-7541. AXIAP_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15335. AXIAP_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.471 AXIAP_CFG_1_MBT_REGISTER Register

14.8.1.2.471.1 AXIAP_CFG_1_MBT_REGISTER Register (Offset = 20h) [reset = 0h]

This register sets memory barrier attributes

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Table 14-15336. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2220h

Figure 14-7542. AXIAP_CFG_1_MBT_REGISTER Name Register

31	30	29	28	27	26	25	24
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
MEMORY_BARRIER_TRANSFER_REGISTER							
R/W							
0h							

Table 14-15337. AXIAP_CFG_1_MBT_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEMORY_BARRIER_TRANSFER_REGISTER	R/W	0h	This register sets memory barrier attributes

14.8.1.2.472 AXIAP_CFG_1_ROM_HI_REGISTER Register

14.8.1.2.472.1 AXIAP_CFG_1_ROM_HI_REGISTER Register (Offset = F0h) [reset = 0h]

Reading this register returns the AXI ROM Address (63-32).

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Table 14-15338. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 22F0h

Figure 14-7543. AXIAP_CFG_1_ROM_HI_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_HI_REGISTER_ADDRESS							
R							
0h							
23	22	21	20	19	18	17	16
ROM_HI_REGISTER_ADDRESS							
R							
0h							
15	14	13	12	11	10	9	8
ROM_HI_REGISTER_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
ROM_HI_REGISTER_ADDRESS							
R							
0h							

Table 14-15339. AXIAP_CFG_1_ROM_HI_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_HI_REGISTER_ADDRESS	R	0h	Reading this register returns the upper ROM Address

14.8.1.2.473 AXIAP_CFG_1_CFG_REGISTER Register

14.8.1.2.473.1 AXIAP_CFG_1_CFG_REGISTER Register (Offset = F4h) [reset = 0h]

The CFG register provides information about how the MEM-AP implementation is configured.

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Table 14-15340. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 22F4h

Figure 14-7544. AXIAP_CFG_1_CFG_REGISTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					LD	LA	BE
R					R	R	R
0h					0h	0h	0h

Table 14-15341. AXIAP_CFG_1_CFG_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved bit, return 0
2	LD	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Data Extension, that provides support for data items larger than 32-bits, it is 0
1	LA	R	0h	This bit indicates whether the MEM-AP implementation includes the Large Physical Address Extension, that supports physical addresses of more than 32-bits:
0	BE	R	0h	ADIv52 obsoletes support for big-endian MEM-AP, and this bit must RAZ

14.8.1.2.474 AXIAP_CFG_1_ROM_LO_REGISTER Register

14.8.1.2.474.1 AXIAP_CFG_1_ROM_LO_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AXI ROM Address (31:12) .

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Table 14-15342. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 22F8h

Figure 14-7545. AXIAP_CFG_1_ROM_LO_REGISTER Name Register

31	30	29	28	27	26	25	24
LOWBASE							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOWBASE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOWBASE				RESERVED			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						FORMAT	PRESENT
R						R	R
0h						0h	0h

Table 14-15343. AXIAP_CFG_1_ROM_LO_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	LOWBASE	R	0h	Bits 31:12 of the base address
11:2	RESERVED	R	0h	Reserved, returns 0
1	FORMAT	R	0h	Base address register format [0]
0	PRESENT	R	0h	This field indicates whether a debug entry is present for this MEM-AP: 0 No debug entry present 1 Debug entry present

14.8.1.2.475 AXIAP_CFG_1_ID_REGISTER Register

14.8.1.2.475.1 AXIAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-15344. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 22FCh

Figure 14-7546. AXIAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15345. AXIAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB, 4=AXI [4]

14.8.1.2.476 PWRAP_CFG_1_ID_REGISTER Register

14.8.1.2.476.1 PWRAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 2E0002h]

Reading this register returns the ID information for this AP.

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Table 14-15346. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 23FCh

Figure 14-7547. PWRAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">17h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">17h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">2h</td></tr>
</table>

Table 14-15347. PWRAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	17h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	2h	Device Type: 0=JTAG, 1=AHB, 2=APB [2]

14.8.1.2.477 PVIEW_CFG_1_PVIEW_STATE0 Register

14.8.1.2.477.1 PVIEW_CFG_1_PVIEW_STATE0 Register (Offset = 0h) [reset = 0h]

This register provides the device specific power status. A read of Power View State Register will lock the values for all other Power View State Registers. A read from the last Power View State register will unlock them so they can update

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Table 14-15348. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2400h

Figure 14-7548. PVIEW_CFG_1_PVIEW_STATE0 Name Register

31	30	29	28	27	26	25	24
POWER_VIEW_STATE_REG0							
R							
0h							
23	22	21	20	19	18	17	16
POWER_VIEW_STATE_REG0							
R							
0h							
15	14	13	12	11	10	9	8
POWER_VIEW_STATE_REG0							
R							
0h							
7	6	5	4	3	2	1	0
POWER_VIEW_STATE_REG0							
R							
0h							

Table 14-15349. PVIEW_CFG_1_PVIEW_STATE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POWER_VIEW_STATE_REG0	R	0h	

14.8.1.2.478 PVIEW_CFG_1_PVIEW_CAPABILITY Register

14.8.1.2.478.1 PVIEW_CFG_1_PVIEW_CAPABILITY Register (Offset = F0h) [reset = 0h]

The Capability Register provides information on the number of Power State registers implemented in the AP

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Table 14-15350. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 24F0h

Figure 14-7549. PVIEW_CFG_1_PVIEW_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		NUMSTATREG					
R		R					
0h		0h					

Table 14-15351. PVIEW_CFG_1_PVIEW_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	Reserved, returns 0
5:0	NUMSTATREG	R	0h	The value read indicates the number of valid Power State Registers that are implemented in the system The maximum number is 60 and the minimum number is 1 The registers are always implemented at contiguous addresses so a value of 7 means that registers 0-6 are valid

14.8.1.2.479 PVIEW_CFG_1_ID_REGISTER Register

14.8.1.2.479.1 PVIEW_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-15352. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 24FCh

Figure 14-7550. PVIEW_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15353. PVIEW_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [0]
27:17	JEP_CODE	R	0h	Device JEP Code [0x017]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [0]
3:0	TYPE	R	0h	Device Type = 3

14.8.1.2.480 JTAGAP_CFG_1_CSW Register

14.8.1.2.480.1 JTAGAP_CFG_1_CSW Register (Offset = 0h) [reset = 0h]

This register provides control and status information

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Table 14-15354. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2500h

Figure 14-7551. JTAGAP_CFG_1_CSW Name Register

31	30	29	28	27	26	25	24
SERACTV	WFIFOCNT			RSV27	RFIFOCNT		
R	R			R	R		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PORT_CONNECTED_STATUS	SRST_STATUS	TRST_ASSERT	SRST_ASSERT
R				R	R	R/W	R/W
0h				0h	0h	0h	0h

Table 14-15355. JTAGAP_CFG_1_CSW Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SERACTV	R	0h	JTAG Serializer active
30:28	WFIFOCNT	R	0h	Outstanding Write FIFO Byte Count
27	RSV27	R	0h	Reserved, returns 0
26:24	RFIFOCNT	R	0h	Outstanding Read FIFO Byte Count
23:4	RESERVED	R	0h	Reserved, returns 0
3	PORT_CONNECTED_STATUS	R	0h	Reading this returns the Port connected status of the selected port
2	SRST_STATUS	R	0h	Reading this returns the SRST status of the selected port If multiple ports are selected, it is the AND of all the SRSTCONNECTED inputs from the selected ports
1	TRST_ASSERT	R/W	0h	Writing a 1 causes TRST to be asserted
0	SRST_ASSERT	R/W	0h	Writing a 1 causes SRST to be asserted

14.8.1.2.481 JTAGAP_CFG_1_PSEL_REG Register

14.8.1.2.481.1 JTAGAP_CFG_1_PSEL_REG Register (Offset = 4h) [reset = 0h]

This 8-bit register is used to select the JTAG port.

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Table 14-15356. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2504h

Figure 14-7552. JTAGAP_CFG_1_PSEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_SELECT_REGISTER							
R/W							
0h							

Table 14-15357. JTAGAP_CFG_1_PSEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	read as 0
7:0	PORT_SELECT_REGISTER	R/W	0h	

14.8.1.2.482 JTAGAP_CFG_1_PSTA_REG Register

14.8.1.2.482.1 JTAGAP_CFG_1_PSTA_REG Register (Offset = 8h) [reset = 0h]

A bit value of 1 indicates that a selected and enabled port has gone inactive. These bits are sticky. Writing a 1 to them clears them.

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Table 14-15358. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2508h

Figure 14-7553. JTAGAP_CFG_1_PSTA_REG Name Register

31	30	29	28	27	26	25	24
PORT_STATUS_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
PORT_STATUS_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
PORT_STATUS_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
PORT_STATUS_REGISTER							
R/W							
0h							

Table 14-15359. JTAGAP_CFG_1_PSTA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PORT_STATUS_REGISTER	R/W	0h	

14.8.1.2.483 JTAGAP_CFG_1_BYTEFIFO1 Register

14.8.1.2.483.1 JTAGAP_CFG_1_BYTEFIFO1 Register (Offset = 10h) [reset = 0h]

Reading this location reads a byte from the FIFO. Writing it loads a byte into the FIFO. Reset value is UNDEFINED

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Table 14-15360. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2510h

Figure 14-7554. JTAGAP_CFG_1_BYTEFIFO1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_1							
R/W							
0h							

Table 14-15361. JTAGAP_CFG_1_BYTEFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	
7:0	BYTE_FIFO_1	R/W	0h	

14.8.1.2.484 JTAGAP_CFG_1_BYTEFIFO2 Register

14.8.1.2.484.1 JTAGAP_CFG_1_BYTEFIFO2 Register (Offset = 14h) [reset = 0h]

Reading this location reads a 16 bits from the FIFO. Writing it loads 16 bits into the FIFO. Reset value is UNDEFINED

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Table 14-15362. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2514h

Figure 14-7555. JTAGAP_CFG_1_BYTEFIFO2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_2							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_2							
R/W							
0h							

Table 14-15363. JTAGAP_CFG_1_BYTEFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R/W	0h	
15:0	BYTE_FIFO_2	R/W	0h	

14.8.1.2.485 JTAGAP_CFG_1_BYTEFIFO3 Register

14.8.1.2.485.1 JTAGAP_CFG_1_BYTEFIFO3 Register (Offset = 18h) [reset = 0h]

Reading this location reads a 24 bits from the FIFO. Writing it loads 24 bits into the FIFO. Reset value is UNDEFINED

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Table 14-15364. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2518h

Figure 14-7556. JTAGAP_CFG_1_BYTEFIFO3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_3							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_3							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_3							
R/W							
0h							

Table 14-15365. JTAGAP_CFG_1_BYTEFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R/W	0h	
23:0	BYTE_FIFO_3	R/W	0h	

14.8.1.2.486 JTAGAP_CFG_1_BYTEFIFO4 Register

14.8.1.2.486.1 JTAGAP_CFG_1_BYTEFIFO4 Register (Offset = 1Ch) [reset = 0h]

Reading this location reads a 32 bits from the FIFO. Writing it loads 32 bits into the FIFO. Reset value is UNDEFINED

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Table 14-15366. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 251Ch

Figure 14-7557. JTAGAP_CFG_1_BYTEFIFO4 Name Register

31	30	29	28	27	26	25	24
BYTE_FIFO_4							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE_FIFO_4							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE_FIFO_4							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE_FIFO_4							
R/W							
0h							

Table 14-15367. JTAGAP_CFG_1_BYTEFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BYTE_FIFO_4	R/W	0h	

14.8.1.2.487 JTAGAP_CFG_1_ID_REGISTER Register

14.8.1.2.487.1 JTAGAP_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-15368. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 25FCh

Figure 14-7558. JTAGAP_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15369. JTAGAP_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [1]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[0] [not a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [0]

14.8.1.2.488 SECAP_CFG_1_TXDATA Register

14.8.1.2.488.1 SECAP_CFG_1_TXDATA Register (Offset = 0h) [reset = 0h]

Data value to send to security controller. APLLication specific

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Table 14-15370. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2600h

Figure 14-7559. SECAP_CFG_1_TXDATA Name Register

31	30	29	28	27	26	25	24
TX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
TX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_DATA_REGISTER							
R/W							
0h							

Table 14-15371. SECAP_CFG_1_TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TX_DATA_REGISTER	R/W	0h	

14.8.1.2.489 SECAP_CFG_1_TXCTRL Register

14.8.1.2.489.1 SECAP_CFG_1_TXCTRL Register (Offset = 4h) [reset = 0h]

Register to send control information to the Security Controller, Application specific

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Table 14-15372. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2604h

Figure 14-7560. SECAP_CFG_1_TXCTRL Name Register

31	30	29	28	27	26	25	24
TX_CONTROL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_CONTROL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TX_CONTROL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_CONTROL							TXDAV
R/W							R
0h							0h

Table 14-15373. SECAP_CFG_1_TXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	TX_CONTROL	R/W	0h	31 bits to send to security controller, Application specific
0	TXDAV	R	0h	TX Data Available

14.8.1.2.490 SECAP_CFG_1_RXDATA Register

14.8.1.2.490.1 SECAP_CFG_1_RXDATA Register (Offset = 8h) [reset = 0h]

Data value from the security controller. APLLication specific

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Table 14-15374. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2608h

Figure 14-7561. SECAP_CFG_1_RXDATA Name Register

31	30	29	28	27	26	25	24
RX_DATA_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_DATA_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
RX_DATA_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_DATA_REGISTER							
R/W							
0h							

Table 14-15375. SECAP_CFG_1_RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RX_DATA_REGISTER	R/W	0h	

14.8.1.2.491 SECAP_CFG_1_RXCTRL Register

14.8.1.2.491.1 SECAP_CFG_1_RXCTRL Register (Offset = Ch) [reset = 0h]

Register to receive control information from the Security Controller

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Table 14-15376. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 260Ch

Figure 14-7562. SECAP_CFG_1_RXCTRL Name Register

31	30	29	28	27	26	25	24
RX_CONTROL							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CONTROL							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_CONTROL							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_CONTROL							RXDAV
R							R
0h							0h

Table 14-15377. SECAP_CFG_1_RXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RX_CONTROL	R	0h	31 bits from the security controller, Application specific
0	RXDAV	R	0h	TX Data Available

14.8.1.2.492 CORTEX0_CFG_1_CSWREG Register

14.8.1.2.492.1 CORTEX0_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-15378. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2700h

Figure 14-7563. CORTEX0_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-15379. CORTEX0_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.493 CORTEX0_CFG_1_DRWREG Register

14.8.1.2.493.1 CORTEX0_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-15380. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 270Ch

Figure 14-7564. CORTEX0_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15381. CORTEX0_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.494 CORTEX0_CFG_1_BD0REG Register

14.8.1.2.494.1 CORTEX0_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15382. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2710h

Figure 14-7565. CORTEX0_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15383. CORTEX0_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.495 CORTEX0_CFG_1_BD1REG Register

14.8.1.2.495.1 CORTEX0_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15384. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2714h

Figure 14-7566. CORTEX0_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15385. CORTEX0_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.496 CORTEX0_CFG_1_BD2REG Register

14.8.1.2.496.1 CORTEX0_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15386. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2718h

Figure 14-7567. CORTEX0_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15387. CORTEX0_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.497 CORTEX0_CFG_1_BD3REG Register

14.8.1.2.497.1 CORTEX0_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15388. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 271Ch

Figure 14-7568. CORTEX0_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15389. CORTEX0_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.498 CORTEX0_CFG_1_ROM_REGISTER Register

14.8.1.2.498.1 CORTEX0_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-15390. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 27F8h

Figure 14-7569. CORTEX0_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-15391. CORTEX0_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.499 CORTEX0_CFG_1_ID_REGISTER Register

14.8.1.2.499.1 CORTEX0_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-15392. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 27FCh

Figure 14-7570. CORTEX0_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15393. CORTEX0_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.500 CORTEX1_CFG_1_CSWREG Register

14.8.1.2.500.1 CORTEX1_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-15394. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2800h

Figure 14-7571. CORTEX1_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-15395. CORTEX1_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.501 CORTEX1_CFG_1_DRWREG Register

14.8.1.2.501.1 CORTEX1_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-15396. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 280Ch

Figure 14-7572. CORTEX1_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15397. CORTEX1_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.502 CORTEX1_CFG_1_BD0REG Register

14.8.1.2.502.1 CORTEX1_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15398. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2810h

Figure 14-7573. CORTEX1_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15399. CORTEX1_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.503 CORTEX1_CFG_1_BD1REG Register

14.8.1.2.503.1 CORTEX1_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15400. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2814h

Figure 14-7574. CORTEX1_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15401. CORTEX1_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.504 CORTEX1_CFG_1_BD2REG Register

14.8.1.2.504.1 CORTEX1_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15402. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2818h

Figure 14-7575. CORTEX1_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15403. CORTEX1_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.505 CORTEX1_CFG_1_BD3REG Register

14.8.1.2.505.1 CORTEX1_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15404. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 281Ch

Figure 14-7576. CORTEX1_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15405. CORTEX1_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.506 CORTEX1_CFG_1_ROM_REGISTER Register

14.8.1.2.506.1 CORTEX1_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-15406. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 28F8h

Figure 14-7577. CORTEX1_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-15407. CORTEX1_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.507 CORTEX1_CFG_1_ID_REGISTER Register

14.8.1.2.507.1 CORTEX1_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-15408. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 28FCh

Figure 14-7578. CORTEX1_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15409. CORTEX1_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.508 CORTEX2_CFG_1_CSWREG Register

14.8.1.2.508.1 CORTEX2_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

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Table 14-15410. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2900h

Figure 14-7579. CORTEX2_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-15411. CORTEX2_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.509 CORTEX2_CFG_1_DRWREG Register

14.8.1.2.509.1 CORTEX2_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

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Table 14-15412. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 290Ch

Figure 14-7580. CORTEX2_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15413. CORTEX2_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.510 CORTEX2_CFG_1_BD0REG Register

14.8.1.2.510.1 CORTEX2_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15414. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2910h

Figure 14-7581. CORTEX2_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15415. CORTEX2_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.511 CORTEX2_CFG_1_BD1REG Register

14.8.1.2.511.1 CORTEX2_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15416. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2914h

Figure 14-7582. CORTEX2_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15417. CORTEX2_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.512 CORTEX2_CFG_1_BD2REG Register

14.8.1.2.512.1 CORTEX2_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15418. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2918h

Figure 14-7583. CORTEX2_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15419. CORTEX2_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.513 CORTEX2_CFG_1_BD3REG Register

14.8.1.2.513.1 CORTEX2_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15420. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 291Ch

Figure 14-7584. CORTEX2_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15421. CORTEX2_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.514 CORTEX2_CFG_1_ROM_REGISTER Register

14.8.1.2.514.1 CORTEX2_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-15422. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 29F8h

Figure 14-7585. CORTEX2_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-15423. CORTEX2_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.515 CORTEX2_CFG_1_ID_REGISTER Register

14.8.1.2.515.1 CORTEX2_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-15424. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 29FCh

Figure 14-7586. CORTEX2_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15425. CORTEX2_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.516 CORTEX3_CFG_1_CSWREG Register

14.8.1.2.516.1 CORTEX3_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-15426. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2A00h

Figure 14-7587. CORTEX3_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15427. CORTEX3_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.517 CORTEX3_CFG_1_DRWREG Register

14.8.1.2.517.1 CORTEX3_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-15428. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2A0Ch

Figure 14-7588. CORTEX3_CFG_1_DRWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA_READ_WRITE_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15429. CORTEX3_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.518 CORTEX3_CFG_1_BD0REG Register

14.8.1.2.518.1 CORTEX3_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15430. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2A10h

Figure 14-7589. CORTEX3_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15431. CORTEX3_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.519 CORTEX3_CFG_1_BD1REG Register

14.8.1.2.519.1 CORTEX3_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15432. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2A14h

Figure 14-7590. CORTEX3_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15433. CORTEX3_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.520 CORTEX3_CFG_1_BD2REG Register

14.8.1.2.520.1 CORTEX3_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15434. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2A18h

Figure 14-7591. CORTEX3_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15435. CORTEX3_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.521 CORTEX3_CFG_1_BD3REG Register

14.8.1.2.521.1 CORTEX3_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15436. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2A1Ch

Figure 14-7592. CORTEX3_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15437. CORTEX3_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.522 CORTEX3_CFG_1_ROM_REGISTER Register

14.8.1.2.522.1 CORTEX3_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-15438. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2AF8h

Figure 14-7593. CORTEX3_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-15439. CORTEX3_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.523 CORTEX3_CFG_1_ID_REGISTER Register

14.8.1.2.523.1 CORTEX3_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-15440. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2AFCh

Figure 14-7594. CORTEX3_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15441. CORTEX3_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.524 CORTEX4_CFG_1_CSWREG Register

14.8.1.2.524.1 CORTEX4_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-15442. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2B00h

Figure 14-7595. CORTEX4_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-15443. CORTEX4_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.525 CORTEX4_CFG_1_DRWREG Register

14.8.1.2.525.1 CORTEX4_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-15444. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2B0Ch

Figure 14-7596. CORTEX4_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15445. CORTEX4_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.526 CORTEX4_CFG_1_BD0REG Register

14.8.1.2.526.1 CORTEX4_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15446. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2B10h

Figure 14-7597. CORTEX4_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15447. CORTEX4_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.527 CORTEX4_CFG_1_BD1REG Register

14.8.1.2.527.1 CORTEX4_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15448. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2B14h

Figure 14-7598. CORTEX4_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15449. CORTEX4_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.528 CORTEX4_CFG_1_BD2REG Register

14.8.1.2.528.1 CORTEX4_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15450. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2B18h

Figure 14-7599. CORTEX4_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15451. CORTEX4_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.529 CORTEX4_CFG_1_BD3REG Register

14.8.1.2.529.1 CORTEX4_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15452. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2B1Ch

Figure 14-7600. CORTEX4_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15453. CORTEX4_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.530 CORTEX4_CFG_1_ROM_REGISTER Register

14.8.1.2.530.1 CORTEX4_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-15454. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2BF8h

Figure 14-7601. CORTEX4_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-15455. CORTEX4_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.531 CORTEX4_CFG_1_ID_REGISTER Register

14.8.1.2.531.1 CORTEX4_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-15456. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2BFCh

Figure 14-7602. CORTEX4_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-15457. CORTEX4_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.532 CORTEX5_CFG_1_CSWREG Register

14.8.1.2.532.1 CORTEX5_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-15458. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2C00h

Figure 14-7603. CORTEX5_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-15459. CORTEX5_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.533 CORTEX5_CFG_1_DRWREG Register

14.8.1.2.533.1 CORTEX5_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-15460. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2C0Ch

Figure 14-7604. CORTEX5_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15461. CORTEX5_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.534 CORTEX5_CFG_1_BD0REG Register

14.8.1.2.534.1 CORTEX5_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15462. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2C10h

Figure 14-7605. CORTEX5_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15463. CORTEX5_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.535 CORTEX5_CFG_1_BD1REG Register

14.8.1.2.535.1 CORTEX5_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15464. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2C14h

Figure 14-7606. CORTEX5_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15465. CORTEX5_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.536 CORTEX5_CFG_1_BD2REG Register

14.8.1.2.536.1 CORTEX5_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15466. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2C18h

Figure 14-7607. CORTEX5_CFG_1_BD2REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_2_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15467. CORTEX5_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.537 CORTEX5_CFG_1_BD3REG Register

14.8.1.2.537.1 CORTEX5_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15468. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2C1Ch

Figure 14-7608. CORTEX5_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15469. CORTEX5_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.538 CORTEX5_CFG_1_ROM_REGISTER Register

14.8.1.2.538.1 CORTEX5_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-15470. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2CF8h

Figure 14-7609. CORTEX5_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-15471. CORTEX5_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.539 CORTEX5_CFG_1_ID_REGISTER Register

14.8.1.2.539.1 CORTEX5_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-15472. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2CFCh

Figure 14-7610. CORTEX5_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15473. CORTEX5_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.540 CORTEX6_CFG_1_CSWREG Register

14.8.1.2.540.1 CORTEX6_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-15474. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2D00h

Figure 14-7611. CORTEX6_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-15475. CORTEX6_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.541 CORTEX6_CFG_1_DRWREG Register

14.8.1.2.541.1 CORTEX6_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-15476. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2D0Ch

Figure 14-7612. CORTEX6_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15477. CORTEX6_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.542 CORTEX6_CFG_1_BD0REG Register

14.8.1.2.542.1 CORTEX6_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15478. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2D10h

Figure 14-7613. CORTEX6_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15479. CORTEX6_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.543 CORTEX6_CFG_1_BD1REG Register

14.8.1.2.543.1 CORTEX6_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15480. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2D14h

Figure 14-7614. CORTEX6_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15481. CORTEX6_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.544 CORTEX6_CFG_1_BD2REG Register

14.8.1.2.544.1 CORTEX6_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15482. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2D18h

Figure 14-7615. CORTEX6_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15483. CORTEX6_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.545 CORTEX6_CFG_1_BD3REG Register

14.8.1.2.545.1 CORTEX6_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15484. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2D1Ch

Figure 14-7616. CORTEX6_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15485. CORTEX6_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.546 CORTEX6_CFG_1_ROM_REGISTER Register

14.8.1.2.546.1 CORTEX6_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-15486. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2DF8h

Figure 14-7617. CORTEX6_CFG_1_ROM_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15487. CORTEX6_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.547 CORTEX6_CFG_1_ID_REGISTER Register

14.8.1.2.547.1 CORTEX6_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-15488. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2DFCh

Figure 14-7618. CORTEX6_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15489. CORTEX6_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.548 CORTEX7_CFG_1_CSWREG Register

14.8.1.2.548.1 CORTEX7_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-15490. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2E00h

Figure 14-7619. CORTEX7_CFG_1_CSWREG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1			ADDR_INC	RESERVED0			
R			R/W	R			
0h			0h	0h			

Table 14-15491. CORTEX7_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.549 CORTEX7_CFG_1_DRWREG Register

14.8.1.2.549.1 CORTEX7_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-15492. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2E0Ch

Figure 14-7620. CORTEX7_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15493. CORTEX7_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.550 CORTEX7_CFG_1_BD0REG Register

14.8.1.2.550.1 CORTEX7_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15494. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2E10h

Figure 14-7621. CORTEX7_CFG_1_BD0REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_0_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_0_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_0_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_0_REGISTER							
R/W							
0h							

Table 14-15495. CORTEX7_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.551 CORTEX7_CFG_1_BD1REG Register

14.8.1.2.551.1 CORTEX7_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15496. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2E14h

Figure 14-7622. CORTEX7_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15497. CORTEX7_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.552 CORTEX7_CFG_1_BD2REG Register

14.8.1.2.552.1 CORTEX7_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15498. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2E18h

Figure 14-7623. CORTEX7_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15499. CORTEX7_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.553 CORTEX7_CFG_1_BD3REG Register

14.8.1.2.553.1 CORTEX7_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

Return to Summary Table

Table 14-15500. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2E1Ch

Figure 14-7624. CORTEX7_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15501. CORTEX7_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.554 CORTEX7_CFG_1_ROM_REGISTER Register

14.8.1.2.554.1 CORTEX7_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

Return to Summary Table

Table 14-15502. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2EF8h

Figure 14-7625. CORTEX7_CFG_1_ROM_REGISTER Name Register

31	30	29	28	27	26	25	24
ROM_REGISTER							
R							
0h							
23	22	21	20	19	18	17	16
ROM_REGISTER							
R							
0h							
15	14	13	12	11	10	9	8
ROM_REGISTER							
R							
0h							
7	6	5	4	3	2	1	0
ROM_REGISTER							
R							
0h							

Table 14-15503. CORTEX7_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.555 CORTEX7_CFG_1_ID_REGISTER Register

14.8.1.2.555.1 CORTEX7_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

Return to Summary Table

Table 14-15504. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2EFCh

Figure 14-7626. CORTEX7_CFG_1_ID_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">REVISION</td><td colspan="4">JEP_CODE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">JEP_CODE</td><td>CLASS</td></tr>
<tr><td colspan="7">R</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SPARE</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">VARIANT</td><td colspan="4">TYPE</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15505. CORTEX7_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.556 CORTEX8_CFG_1_CSWREG Register

14.8.1.2.556.1 CORTEX8_CFG_1_CSWREG Register (Offset = 0h) [reset = 0h]

This register contains the Addressing control bit

Return to Summary Table

Table 14-15506. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2F00h

Figure 14-7627. CORTEX8_CFG_1_CSWREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED1</td><td>ADDR_INC</td><td colspan="4">RESERVED0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15507. CORTEX8_CFG_1_CSWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED1	R	0h	Reserved, returns 0
4	ADDR_INC	R/W	0h	Address Increment Enable
3:0	RESERVED0	R	0h	reserved, returns 0

14.8.1.2.557 CORTEX8_CFG_1_DRWREG Register

14.8.1.2.557.1 CORTEX8_CFG_1_DRWREG Register (Offset = Ch) [reset = 0h]

This register is used to write data to the TA location or read it back from the TA location.

Return to Summary Table

Table 14-15508. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2F0Ch

Figure 14-7628. CORTEX8_CFG_1_DRWREG Name Register

31	30	29	28	27	26	25	24
DATA_READ_WRITE_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_READ_WRITE_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_READ_WRITE_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_READ_WRITE_REGISTER							
R/W							
0h							

Table 14-15509. CORTEX8_CFG_1_DRWREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_READ_WRITE_REGISTER	R/W	0h	This register is used to read or write data

14.8.1.2.558 CORTEX8_CFG_1_BD0REG Register

14.8.1.2.558.1 CORTEX8_CFG_1_BD0REG Register (Offset = 10h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15510. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2F10h

Figure 14-7629. CORTEX8_CFG_1_BD0REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">BANKED_DATA_0_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15511. CORTEX8_CFG_1_BD0REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_0_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.559 CORTEX8_CFG_1_BD1REG Register

14.8.1.2.559.1 CORTEX8_CFG_1_BD1REG Register (Offset = 14h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15512. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2F14h

Figure 14-7630. CORTEX8_CFG_1_BD1REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_1_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_1_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_1_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_1_REGISTER							
R/W							
0h							

Table 14-15513. CORTEX8_CFG_1_BD1REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_1_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.560 CORTEX8_CFG_1_BD2REG Register

14.8.1.2.560.1 CORTEX8_CFG_1_BD2REG Register (Offset = 18h) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15514. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2F18h

Figure 14-7631. CORTEX8_CFG_1_BD2REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_2_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_2_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_2_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_2_REGISTER							
R/W							
0h							

Table 14-15515. CORTEX8_CFG_1_BD2REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_2_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.561 CORTEX8_CFG_1_BD3REG Register

14.8.1.2.561.1 CORTEX8_CFG_1_BD3REG Register (Offset = 1Ch) [reset = 0h]

This register is used to transfer data when doing banked data operations.

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Table 14-15516. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2F1Ch

Figure 14-7632. CORTEX8_CFG_1_BD3REG Name Register

31	30	29	28	27	26	25	24
BANKED_DATA_3_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
BANKED_DATA_3_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
BANKED_DATA_3_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
BANKED_DATA_3_REGISTER							
R/W							
0h							

Table 14-15517. CORTEX8_CFG_1_BD3REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BANKED_DATA_3_REGISTER	R/W	0h	This register is used to transfer data when doing banked data operations

14.8.1.2.562 CORTEX8_CFG_1_ROM_REGISTER Register

14.8.1.2.562.1 CORTEX8_CFG_1_ROM_REGISTER Register (Offset = F8h) [reset = 0h]

Reading this register returns the AHB ROM Address.

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Table 14-15518. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2FF8h

Figure 14-7633. CORTEX8_CFG_1_ROM_REGISTER Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ROM_REGISTER</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15519. CORTEX8_CFG_1_ROM_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_REGISTER	R	0h	Reading this register returns the ROM Address

14.8.1.2.563 CORTEX8_CFG_1_ID_REGISTER Register

14.8.1.2.563.1 CORTEX8_CFG_1_ID_REGISTER Register (Offset = FCh) [reset = 0h]

Reading this register returns the ID information for this AP.

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Table 14-15520. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 4000 2FFCh

Figure 14-7634. CORTEX8_CFG_1_ID_REGISTER Name Register

31	30	29	28	27	26	25	24
REVISION				JEP_CODE			
R				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
JEP_CODE							CLASS
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPARE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VARIANT				TYPE			
R				R			
0h				0h			

Table 14-15521. CORTEX8_CFG_1_ID_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REVISION	R	0h	Device Revision [4]
27:17	JEP_CODE	R	0h	Device JEP Code [0x23B]
16	CLASS	R	0h	Device Class[1] [a memory access port]
15:8	SPARE	R	0h	Spare, returns 0
7:4	VARIANT	R	0h	Device Variant [1]
3:0	TYPE	R	0h	Device Type: 0=JTAG, 1=AHB, 2=APB [1]

14.8.1.2.564 ROM_TABLE_1_1_ROM_ENTRY0 Register

14.8.1.2.564.1 ROM_TABLE_1_1_ROM_ENTRY0 Register (Offset = 0h) [reset = 1003h]

rom table entry 0

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Table 14-15522. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0000h

Figure 14-7635. ROM_TABLE_1_1_ROM_ENTRY0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-15523. ROM_TABLE_1_1_ROM_ENTRY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.565 ROM_TABLE_1_1_ROM_ENTRY1 Register

14.8.1.2.565.1 ROM_TABLE_1_1_ROM_ENTRY1 Register (Offset = 4h) [reset = 2003h]

rom table entry 1

Return to Summary Table

Table 14-15524. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0004h

Figure 14-7636. ROM_TABLE_1_1_ROM_ENTRY1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	2h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
2h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
2h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-15525. ROM_TABLE_1_1_ROM_ENTRY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	2h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.566 ROM_TABLE_1_1_ROM_ENTRY2 Register

14.8.1.2.566.1 ROM_TABLE_1_1_ROM_ENTRY2 Register (Offset = 8h) [reset = 3003h]

rom table entry 2

Return to Summary Table

Table 14-15526. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0008h

Figure 14-7637. ROM_TABLE_1_1_ROM_ENTRY2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	3h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
3h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
3h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-15527. ROM_TABLE_1_1_ROM_ENTRY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	3h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.567 ROM_TABLE_1_1_ROM_ENTRY3 Register

14.8.1.2.567.1 ROM_TABLE_1_1_ROM_ENTRY3 Register (Offset = Ch) [reset = 4003h]

rom table entry 3

Return to Summary Table

Table 14-15528. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 000Ch

Figure 14-7638. ROM_TABLE_1_1_ROM_ENTRY3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	4h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
4h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-15529. ROM_TABLE_1_1_ROM_ENTRY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	4h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.568 ROM_TABLE_1_1_ROM_ENTRY4 Register

14.8.1.2.568.1 ROM_TABLE_1_1_ROM_ENTRY4 Register (Offset = 10h) [reset = 5003h]

rom table entry 4

Return to Summary Table

Table 14-15530. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0010h

Figure 14-7639. ROM_TABLE_1_1_ROM_ENTRY4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	5h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
5h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
5h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	1h

Table 14-15531. ROM_TABLE_1_1_ROM_ENTRY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	5h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.569 ROM_TABLE_1_1_ROM_ENTRY5 Register

14.8.1.2.569.1 ROM_TABLE_1_1_ROM_ENTRY5 Register (Offset = 14h) [reset = 1000003h]

rom table entry 5

Return to Summary Table

Table 14-15532. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0014h

Figure 14-7640. ROM_TABLE_1_1_ROM_ENTRY5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1000h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1000h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>1h</td></tr>
</table>

Table 14-15533. ROM_TABLE_1_1_ROM_ENTRY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	1h	Component present,1, or not present,0, status bit

14.8.1.2.570 ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register

14.8.1.2.570.1 ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register (Offset = 18h) [reset = 1000002h]

compute cluster rom table entry 0

Return to Summary Table

Table 14-15534. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0018h

Figure 14-7641. ROM_TABLE_1_1_COMPUTE_CLUSTER0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1000h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1000h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1000h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15535. ROM_TABLE_1_1_COMPUTE_CLUSTER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1000h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.571 ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register

14.8.1.2.571.1 ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register (Offset = 1Ch) [reset = 1400002h]

compute cluster rom table entry 1

Return to Summary Table

Table 14-15536. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 001Ch

Figure 14-7642. ROM_TABLE_1_1_COMPUTE_CLUSTER1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1400h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1400h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1400h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15537. ROM_TABLE_1_1_COMPUTE_CLUSTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1400h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.572 ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register

14.8.1.2.572.1 ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register (Offset = 20h) [reset = 1800002h]

compute cluster rom table entry 2

Return to Summary Table

Table 14-15538. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0020h

Figure 14-7643. ROM_TABLE_1_1_COMPUTE_CLUSTER2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1800h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
1800h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1800h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15539. ROM_TABLE_1_1_COMPUTE_CLUSTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1800h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.573 ROM_TABLE_1_1_DEBUG_CELL0 Register

14.8.1.2.573.1 ROM_TABLE_1_1_DEBUG_CELL0 Register (Offset = 24h) [reset = 1C00002h]

debug cell rom table entry 0

Return to Summary Table

Table 14-15540. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0024h

Figure 14-7644. ROM_TABLE_1_1_DEBUG_CELL0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C00h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C00h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C00h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15541. ROM_TABLE_1_1_DEBUG_CELL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.574 ROM_TABLE_1_1_DEBUG_CELL1 Register

14.8.1.2.574.1 ROM_TABLE_1_1_DEBUG_CELL1 Register (Offset = 28h) [reset = 1C10002h]

debug cell rom table entry 1

Return to Summary Table

Table 14-15542. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0028h

Figure 14-7645. ROM_TABLE_1_1_DEBUG_CELL1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C10h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C10h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C10h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15543. ROM_TABLE_1_1_DEBUG_CELL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.575 ROM_TABLE_1_1_DEBUG_CELL2 Register

14.8.1.2.575.1 ROM_TABLE_1_1_DEBUG_CELL2 Register (Offset = 2Ch) [reset = 1C20002h]

debug cell rom table entry 2

Return to Summary Table

Table 14-15544. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 002Ch

Figure 14-7646. ROM_TABLE_1_1_DEBUG_CELL2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C20h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C20h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C20h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15545. ROM_TABLE_1_1_DEBUG_CELL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.576 ROM_TABLE_1_1_DEBUG_CELL3 Register

14.8.1.2.576.1 ROM_TABLE_1_1_DEBUG_CELL3 Register (Offset = 30h) [reset = 1C30002h]

debug cell rom table entry 3

Return to Summary Table

Table 14-15546. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0030h

Figure 14-7647. ROM_TABLE_1_1_DEBUG_CELL3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1C30h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1C30h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1C30h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-15547. ROM_TABLE_1_1_DEBUG_CELL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.577 ROM_TABLE_1_1_DEBUG_CELL4 Register

14.8.1.2.577.1 ROM_TABLE_1_1_DEBUG_CELL4 Register (Offset = 34h) [reset = 1C40002h]

debug cell rom table entry 4

Return to Summary Table

Table 14-15548. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0034h

Figure 14-7648. ROM_TABLE_1_1_DEBUG_CELL4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C40h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C40h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C40h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15549. ROM_TABLE_1_1_DEBUG_CELL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.578 ROM_TABLE_1_1_DEBUG_CELL5 Register

14.8.1.2.578.1 ROM_TABLE_1_1_DEBUG_CELL5 Register (Offset = 38h) [reset = 1C50002h]

debug cell rom table entry 5

Return to Summary Table

Table 14-15550. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0038h

Figure 14-7649. ROM_TABLE_1_1_DEBUG_CELL5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C50h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C50h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C50h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15551. ROM_TABLE_1_1_DEBUG_CELL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.579 ROM_TABLE_1_1_DEBUG_CELL6 Register

14.8.1.2.579.1 ROM_TABLE_1_1_DEBUG_CELL6 Register (Offset = 3Ch) [reset = 1C60002h]

debug cell rom table entry 6

Return to Summary Table

Table 14-15552. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 003Ch

Figure 14-7650. ROM_TABLE_1_1_DEBUG_CELL6 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C60h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C60h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C60h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15553. ROM_TABLE_1_1_DEBUG_CELL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.580 ROM_TABLE_1_1_DEBUG_CELL7 Register

14.8.1.2.580.1 ROM_TABLE_1_1_DEBUG_CELL7 Register (Offset = 40h) [reset = 1C70002h]

debug cell rom table entry 7

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Table 14-15554. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0040h

Figure 14-7651. ROM_TABLE_1_1_DEBUG_CELL7 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C70h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C70h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C70h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15555. ROM_TABLE_1_1_DEBUG_CELL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.581 ROM_TABLE_1_1_DEBUG_CELL8 Register

14.8.1.2.581.1 ROM_TABLE_1_1_DEBUG_CELL8 Register (Offset = 44h) [reset = 1C80002h]

debug cell rom table entry 8

Return to Summary Table

Table 14-15556. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0044h

Figure 14-7652. ROM_TABLE_1_1_DEBUG_CELL8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C80h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1C80h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1C80h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15557. ROM_TABLE_1_1_DEBUG_CELL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.582 ROM_TABLE_1_1_DEBUG_CELL9 Register

14.8.1.2.582.1 ROM_TABLE_1_1_DEBUG_CELL9 Register (Offset = 48h) [reset = 1C90002h]

debug cell rom table entry 9

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Table 14-15558. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0048h

Figure 14-7653. ROM_TABLE_1_1_DEBUG_CELL9 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1C90h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1C90h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1C90h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15559. ROM_TABLE_1_1_DEBUG_CELL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1C90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.583 ROM_TABLE_1_1_DEBUG_CELL10 Register

14.8.1.2.583.1 ROM_TABLE_1_1_DEBUG_CELL10 Register (Offset = 4Ch) [reset = 1CA0002h]

debug cell rom table entry 10

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Table 14-15560. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 004Ch

Figure 14-7654. ROM_TABLE_1_1_DEBUG_CELL10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1CA0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1CA0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1CA0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-15561. ROM_TABLE_1_1_DEBUG_CELL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.584 ROM_TABLE_1_1_DEBUG_CELL11 Register

14.8.1.2.584.1 ROM_TABLE_1_1_DEBUG_CELL11 Register (Offset = 50h) [reset = 1CB0002h]

debug cell rom table entry 11

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Table 14-15562. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0050h

Figure 14-7655. ROM_TABLE_1_1_DEBUG_CELL11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1CB0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1CB0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1CB0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15563. ROM_TABLE_1_1_DEBUG_CELL11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1CB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.585 ROM_TABLE_1_1_EXTCSCOMP0 Register

14.8.1.2.585.1 ROM_TABLE_1_1_EXTCSCOMP0 Register (Offset = 50h) [reset = 1D00002h]

external coresight componenet rom table entry 0

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Table 14-15564. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0050h

Figure 14-7656. ROM_TABLE_1_1_EXTCSCOMP0 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D00h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D00h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D00h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15565. ROM_TABLE_1_1_EXTCSCOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D00h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.586 ROM_TABLE_1_1_EXTCSCOMP1 Register

14.8.1.2.586.1 ROM_TABLE_1_1_EXTCSCOMP1 Register (Offset = 54h) [reset = 1D10002h]

external coresight componenet rom table entry 1

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Table 14-15566. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0054h

Figure 14-7657. ROM_TABLE_1_1_EXTCSCOMP1 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D10h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D10h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D10h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15567. ROM_TABLE_1_1_EXTCSCOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D10h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.587 ROM_TABLE_1_1_EXTCSCOMP2 Register

14.8.1.2.587.1 ROM_TABLE_1_1_EXTCSCOMP2 Register (Offset = 58h) [reset = 1D20002h]

external coresight componenet rom table entry 2

Return to Summary Table

Table 14-15568. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0058h

Figure 14-7658. ROM_TABLE_1_1_EXTCSCOMP2 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D20h						
23	22	21	20	19	18	17	16
BASEADDR							
R							
1D20h							
15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D20h				0h			0h
7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15569. ROM_TABLE_1_1_EXTCSCOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D20h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.588 ROM_TABLE_1_1_EXTCSCOMP3 Register

14.8.1.2.588.1 ROM_TABLE_1_1_EXTCSCOMP3 Register (Offset = 5Ch) [reset = 1D30002h]

external coresight componenet rom table entry 3

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Table 14-15570. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 005Ch

Figure 14-7659. ROM_TABLE_1_1_EXTCSCOMP3 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D30h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D30h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D30h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15571. ROM_TABLE_1_1_EXTCSCOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D30h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.589 ROM_TABLE_1_1_EXTCSCOMP4 Register

14.8.1.2.589.1 ROM_TABLE_1_1_EXTCSCOMP4 Register (Offset = 60h) [reset = 1D40002h]

external coresight componenet rom table entry 4

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Table 14-15572. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0060h

Figure 14-7660. ROM_TABLE_1_1_EXTCSCOMP4 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D40h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D40h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15573. ROM_TABLE_1_1_EXTCSCOMP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D40h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.590 ROM_TABLE_1_1_EXTCSCOMP5 Register

14.8.1.2.590.1 ROM_TABLE_1_1_EXTCSCOMP5 Register (Offset = 64h) [reset = 1D50002h]

external coresight componenet rom table entry 5

Return to Summary Table

Table 14-15574. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0064h

Figure 14-7661. ROM_TABLE_1_1_EXTCSCOMP5 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D50h						

23	22	21	20	19	18	17	16
BASEADDR							
R							
1D50h							

15	14	13	12	11	10	9	8
BASEADDR				RA30			PWRID
R				R			R
1D50h				0h			0h

7	6	5	4	3	2	1	0
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15575. ROM_TABLE_1_1_EXTCSCOMP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D50h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.591 ROM_TABLE_1_1_EXTCSCOMP6 Register

14.8.1.2.591.1 ROM_TABLE_1_1_EXTCSCOMP6 Register (Offset = 68h) [reset = 1D60002h]

external coresight componenet rom table entry 6

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Table 14-15576. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0068h

Figure 14-7662. ROM_TABLE_1_1_EXTCSCOMP6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D60h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D60h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D60h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-15577. ROM_TABLE_1_1_EXTCSCOMP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D60h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.592 ROM_TABLE_1_1_EXTCSCOMP7 Register

14.8.1.2.592.1 ROM_TABLE_1_1_EXTCSCOMP7 Register (Offset = 6Ch) [reset = 1D70002h]

external coresight componenet rom table entry 7

Return to Summary Table

Table 14-15578. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 006Ch

Figure 14-7663. ROM_TABLE_1_1_EXTCSCOMP7 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D70h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D70h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D70h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-15579. ROM_TABLE_1_1_EXTCSCOMP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D70h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.593 ROM_TABLE_1_1_EXTCSCOMP8 Register

14.8.1.2.593.1 ROM_TABLE_1_1_EXTCSCOMP8 Register (Offset = 70h) [reset = 1D80002h]

external coresight componenet rom table entry 8

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Table 14-15580. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0070h

Figure 14-7664. ROM_TABLE_1_1_EXTCSCOMP8 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1D80h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1D80h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1D80h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15581. ROM_TABLE_1_1_EXTCSCOMP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D80h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.594 ROM_TABLE_1_1_EXTCSCOMP9 Register

14.8.1.2.594.1 ROM_TABLE_1_1_EXTCSCOMP9 Register (Offset = 74h) [reset = 1D90002h]

external coresight componenet rom table entry 9

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Table 14-15582. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0074h

Figure 14-7665. ROM_TABLE_1_1_EXTCSCOMP9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1D90h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1D90h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1D90h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-15583. ROM_TABLE_1_1_EXTCSCOMP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1D90h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.595 ROM_TABLE_1_1_EXTCSCOMP10 Register

14.8.1.2.595.1 ROM_TABLE_1_1_EXTCSCOMP10 Register (Offset = 78h) [reset = 1DA0002h]

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Table 14-15584. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 0078h

Figure 14-7666. ROM_TABLE_1_1_EXTCSCOMP10 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RA00</td><td colspan="7">BASEADDR</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">1DA0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">BASEADDR</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1DA0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">BASEADDR</td><td colspan="3">RA30</td><td>PWRID</td></tr>
<tr><td colspan="4">R</td><td colspan="3">R</td><td>R</td></tr>
<tr><td colspan="4">1DA0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PWRID</td><td>RA0</td><td>PWRIDVAL</td><td>RA1</td><td>VALID</td></tr>
<tr><td colspan="4">R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td>0h</td><td>1h</td><td>0h</td></tr>
</table>

Table 14-15585. ROM_TABLE_1_1_EXTCSCOMP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DA0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.596 ROM_TABLE_1_1_EXTCSCOMP11 Register

14.8.1.2.596.1 ROM_TABLE_1_1_EXTCSCOMP11 Register (Offset = 7Ch) [reset = 1DB0002h]

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Table 14-15586. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 007Ch

Figure 14-7667. ROM_TABLE_1_1_EXTCSCOMP11 Name Register

31	30	29	28	27	26	25	24
RA00	BASEADDR						
R	R						
0h	1DB0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASEADDR							
R							
1DB0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BASEADDR				RA30			PWRID
R				R			R
1DB0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWRID				RA0	PWRIDVAL	RA1	VALID
R				R	R	R	R
0h				0h	0h	1h	0h

Table 14-15587. ROM_TABLE_1_1_EXTCSCOMP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RA00	R	0h	always read as 0
30:12	BASEADDR	R	1DB0h	Component base address
11:9	RA30	R	0h	always read as 0
8:4	PWRID	R	0h	always read as 0
3	RA0	R	0h	always read as 0
2	PWRIDVAL	R	0h	power id valid
1	RA1	R	1h	always read as 1
0	VALID	R	0h	Component present,1, or not present,0, status bit

14.8.1.2.597 CSCTI_CTICONTROL Register

14.8.1.2.597.1 CSCTI_CTICONTROL Register (Offset = 0h) [reset = 0h]

CTI Control Register.

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Table 14-15588. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1000h

Figure 14-7668. CSCTI_CTICONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							GLBEN
R							R/W
0h							0h

Table 14-15589. CSCTI_CTICONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	GLBEN	R/W	0h	Enables or disables the Embedded Cross Trigger, 1=enabled

14.8.1.2.598 CSCTI_CTIINTACK Register

14.8.1.2.598.1 CSCTI_CTIINTACK Register (Offset = 10h) [reset = 0h]

CTI Interrupt Acknowledge Register.

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Table 14-15590. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1010h

Figure 14-7669. CSCTI_CTIINTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
INTACK							
R/W							
0h							

Table 14-15591. CSCTI_CTIINTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	INTACK	R/W	0h	Acknowledges the corresponding CTITRIGOUT output Write 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW There is one bit of the register for each CTITRIGOUT output

14.8.1.2.599 CSCTI_CTIAPPSET Register

14.8.1.2.599.1 CSCTI_CTIAPPSET Register (Offset = 14h) [reset = 0h]

CTI Application Trigger Set Register.

Return to Summary Table

Table 14-15592. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1014h

Figure 14-7670. CSCTI_CTIAPPSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPSET			
R				R/W			
0h				0h			

Table 14-15593. CSCTI_CTIAPPSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPSET	R/W	0h	The CTI Application Trigger Set Register is read/write A write to this register causes a channel event to be raised, corresponding to the bit written to

14.8.1.2.600 CSCTI_CTIAPPCLR Register

14.8.1.2.600.1 CSCTI_CTIAPPCLR Register (Offset = 18h) [reset = 0h]

CTI Application Trigger Clear Register.

Return to Summary Table

Table 14-15594. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1018h

Figure 14-7671. CSCTI_CTIAPPCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPCLR			
R				R/W			
0h				0h			

Table 14-15595. CSCTI_CTIAPPCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPCLR	R/W	0h	The CTI Application Trigger Clear Register is write-only A write to this register causes a channel event to be cleared, corresponding to the bit written to

14.8.1.2.601 CSCTI_CTIAPPPULSE Register

14.8.1.2.601.1 CSCTI_CTIAPPPULSE Register (Offset = 1Ch) [reset = 0h]

CTI Application Trigger Pulse Register.

Return to Summary Table

Table 14-15596. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 101Ch

Figure 14-7672. CSCTI_CTIAPPPULSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				APPPULSE			
R				R/W			
0h				0h			

Table 14-15597. CSCTI_CTIAPPPULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	APPPULSE	R/W	0h	The CTI Application Pulse Register is write-only A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to This register clears itself immediately

14.8.1.2.602 CSCTI_CTIINEN0 Register

14.8.1.2.602.1 CSCTI_CTIINEN0 Register (Offset = 20h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 0

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Table 14-15598. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1020h

Figure 14-7673. CSCTI_CTIINEN0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15599. CSCTI_CTIINEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.603 CSCTI_CTIINEN1 Register

14.8.1.2.603.1 CSCTI_CTIINEN1 Register (Offset = 24h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 1

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Table 14-15600. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1024h

Figure 14-7674. CSCTI_CTIINEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	TRIGINEN		
R				NONE	R/W		
0h				0h	0h		

Table 14-15601. CSCTI_CTIINEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.604 CSCTI_CTIINEN2 Register

14.8.1.2.604.1 CSCTI_CTIINEN2 Register (Offset = 28h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 2

Return to Summary Table

Table 14-15602. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1028h

Figure 14-7675. CSCTI_CTIINEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-15603. CSCTI_CTIINEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.605 CSCTI_CTIINEN3 Register

14.8.1.2.605.1 CSCTI_CTIINEN3 Register (Offset = 2Ch) [reset = 0h]

CTI Application Trigger to Channel Enable Register 3

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Table 14-15604. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 102Ch

Figure 14-7676. CSCTI_CTIINEN3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15605. CSCTI_CTIINEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.606 CSCTI_CTIINEN4 Register

14.8.1.2.606.1 CSCTI_CTIINEN4 Register (Offset = 30h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 4

Return to Summary Table

Table 14-15606. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1030h

Figure 14-7677. CSCTI_CTIINEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-15607. CSCTI_CTIINEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.607 CSCTI_CTIINEN5 Register

14.8.1.2.607.1 CSCTI_CTIINEN5 Register (Offset = 34h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 5

Return to Summary Table

Table 14-15608. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1034h

Figure 14-7678. CSCTI_CTIINEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-15609. CSCTI_CTIINEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.608 CSCTI_CTIINEN6 Register

14.8.1.2.608.1 CSCTI_CTIINEN6 Register (Offset = 38h) [reset = 0h]

CTI Application Trigger to Channel Enable Register 6

Return to Summary Table

Table 14-15610. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1038h

Figure 14-7679. CSCTI_CTIINEN6 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">TRIGINEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15611. CSCTI_CTIINEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.609 CSCTI_CTIINEN7 Register

14.8.1.2.609.1 CSCTI_CTIINEN7 Register (Offset = 3Ch) [reset = 0h]

CTI Application Trigger to Channel Enable Register 7

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Table 14-15612. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 103Ch

Figure 14-7680. CSCTI_CTIINEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGINEN			
R				R/W			
0h				0h			

Table 14-15613. CSCTI_CTIINEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGINEN	R/W	0h	The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI There is one register for each of the eight CTITRIGIN inputs Within each register there is one bit for each of the four channels implemented These registers do not affect the application trigger operations

14.8.1.2.610 CSCTI_CTIOUTEN0 Register

14.8.1.2.610.1 CSCTI_CTIOUTEN0 Register (Offset = A0h) [reset = 0h]

CTI Channel to Trigger Enable Register 0

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Table 14-15614. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10A0h

Figure 14-7681. CSCTI_CTIOUTEN0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-15615. CSCTI_CTIOUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.611 CSCTI_CTIOUTEN1 Register

14.8.1.2.611.1 CSCTI_CTIOUTEN1 Register (Offset = A4h) [reset = 0h]

CTI Channel to Trigger Enable Register 1

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Table 14-15616. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10A4h

Figure 14-7682. CSCTI_CTIOUTEN1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-15617. CSCTI_CTIOUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.612 CSCTI_CTIOUTEN2 Register

14.8.1.2.612.1 CSCTI_CTIOUTEN2 Register (Offset = A8h) [reset = 0h]

CTI Channel to Trigger Enable Register 2

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Table 14-15618. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10A8h

Figure 14-7683. CSCTI_CTIOUTEN2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-15619. CSCTI_CTIOUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.613 CSCTI_CTIOUTEN3 Register

14.8.1.2.613.1 CSCTI_CTIOUTEN3 Register (Offset = ACh) [reset = 0h]

CTI Channel to Trigger Enable Register 3

Return to Summary Table

Table 14-15620. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10ACh

Figure 14-7684. CSCTI_CTIOUTEN3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-15621. CSCTI_CTIOUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.614 CSCTI_CTIOUTEN4 Register

14.8.1.2.614.1 CSCTI_CTIOUTEN4 Register (Offset = B0h) [reset = 0h]

CTI Channel to Trigger Enable Register 4

Return to Summary Table

Table 14-15622. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10B0h

Figure 14-7685. CSCTI_CTIOUTEN4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-15623. CSCTI_CTIOUTEN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.615 CSCTI_CTIOUTEN5 Register

14.8.1.2.615.1 CSCTI_CTIOUTEN5 Register (Offset = B4h) [reset = 0h]

CTI Channel to Trigger Enable Register 5

Return to Summary Table

Table 14-15624. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10B4h

Figure 14-7686. CSCTI_CTIOUTEN5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-15625. CSCTI_CTIOUTEN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.616 CSCTI_CTIOUTEN6 Register

14.8.1.2.616.1 CSCTI_CTIOUTEN6 Register (Offset = B8h) [reset = 0h]

CTI Channel to Trigger Enable Register 6

Return to Summary Table

Table 14-15626. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10B8h

Figure 14-7687. CSCTI_CTIOUTEN6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-15627. CSCTI_CTIOUTEN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.617 CSCTI_CTIOUTEN7 Register

14.8.1.2.617.1 CSCTI_CTIOUTEN7 Register (Offset = BCh) [reset = 0h]

CTI Channel to Trigger Enable Register 7

Return to Summary Table

Table 14-15628. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 10BCh

Figure 14-7688. CSCTI_CTIOUTEN7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				TRIGOUTEN			
R				R/W			
0h				0h			

Table 14-15629. CSCTI_CTIOUTEN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	TRIGOUTEN	R/W	0h	The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output There is one register for each of the eight CTITRIGOUT outputs Within each register there is one bit for each of the four channels implemented These registers affect the mapping from application trigger to trigger outputs

14.8.1.2.618 CSCTI_CTITRIGINSTATUS Register

14.8.1.2.618.1 CSCTI_CTITRIGINSTATUS Register (Offset = 130h) [reset = 0h]

CTI Trigger In Status Register

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Table 14-15630. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1130h

Figure 14-7689. CSCTI_CTITRIGINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGINSTATUS							
R							
0h							

Table 14-15631. CSCTI_CTITRIGINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGINSTATUS	R	0h	Shows the status of the CTITRIGIN inputs: 1=CTITRIGIN is active, 0=CTITRIGIN is inactive

14.8.1.2.619 CSCTI_CTITRIGOUTSTATUS Register

14.8.1.2.619.1 CSCTI_CTITRIGOUTSTATUS Register (Offset = 134h) [reset = 0h]

CTI Trigger Out Status Register

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Table 14-15632. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1134h

Figure 14-7690. CSCTI_CTITRIGOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGOUTSTATUS							
R							
0h							

Table 14-15633. CSCTI_CTITRIGOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGOUTSTATUS	R	0h	Shows the status of the CTITRIGOUT outputs: 1=CTITRIGOUT is active, 0=CTITRIGOUT is inactive

14.8.1.2.620 CSCTI_CTICHINSTATUS Register

14.8.1.2.620.1 CSCTI_CTICHINSTATUS Register (Offset = 138h) [reset = 0h]

CTI Channel In Status Register

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Table 14-15634. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1138h

Figure 14-7691. CSCTI_CTICHINSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CHINSTATUS			
R				R			
0h				0h			

Table 14-15635. CSCTI_CTICHINSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHINSTATUS	R	0h	Shows the status of the CTICHIN inputs: 1=CTICHIN is active, 0=CTICHIN is inactive

14.8.1.2.621 CSCTI_CTICHOUTSTATUS Register

14.8.1.2.621.1 CSCTI_CTICHOUTSTATUS Register (Offset = 13Ch) [reset = 0h]

CTI Channel Out Status Register

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Table 14-15636. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 113Ch

Figure 14-7692. CSCTI_CTICHOUTSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CHOUTSTATUS			
R				R			
0h				0h			

Table 14-15637. CSCTI_CTICHOUTSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CHOUTSTATUS	R	0h	Shows the status of the CTICHOUT outputs: 1=CTICHOUT is active, 0=CTICHOUT is inactive

14.8.1.2.622 CSCTI_CTIGATE Register

14.8.1.2.622.1 CSCTI_CTIGATE Register (Offset = 140h) [reset = 0h]

The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs.

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Table 14-15638. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1140h

Figure 14-7693. CSCTI_CTIGATE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTIGATEEN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15639. CSCTI_CTIGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTIGATEEN	R	0h	Gate enable for the four channels [1 per bit]

14.8.1.2.623 CSCTI_ASICCTL Register

14.8.1.2.623.1 CSCTI_ASICCTL Register (Offset = 144h) [reset = 0h]

Allows external multiplexing of the trigger signals

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Table 14-15640. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1144h

Figure 14-7694. CSCTI_ASICCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
ASICCTL							
R/W							
0h							

Table 14-15641. CSCTI_ASICCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	ASICCTL	R/W	0h	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]

14.8.1.2.624 CSCTI_ITCHINACK Register

14.8.1.2.624.1 CSCTI_ITCHINACK Register (Offset = EDCh) [reset = 0h]

Integration and Test register

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Table 14-15642. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EDCh

Figure 14-7695. CSCTI_ITCHINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CTCHINACK</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15643. CSCTI_ITCHINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHINACK	R/W	0h	Sets the value of the CTCHINACK outputs

14.8.1.2.625 CSCTI_ITTRIGINACK Register

14.8.1.2.625.1 CSCTI_ITTRIGINACK Register (Offset = EE0h) [reset = 0h]

ITTRIGINACK Register

Return to Summary Table

Table 14-15644. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EE0h

Figure 14-7696. CSCTI_ITTRIGINACK Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CTTRIGINACK</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15645. CSCTI_ITTRIGINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGINACK	R/W	0h	Sets the value of the CTTRIGINACK outputs

14.8.1.2.626 CSCTI_ITCHOUT Register

14.8.1.2.626.1 CSCTI_ITCHOUT Register (Offset = EE4h) [reset = 0h]

ITCHOUT Register

Return to Summary Table

Table 14-15646. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EE4h

Figure 14-7697. CSCTI_ITCHOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHOUT			
R				R/W			
0h				0h			

Table 14-15647. CSCTI_ITCHOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHOUT	R/W	0h	Sets the value of the CTCHOUT outputs

14.8.1.2.627 CSCTI_ITTRIGOUT Register

14.8.1.2.627.1 CSCTI_ITTRIGOUT Register (Offset = EE8h) [reset = 0h]

ITTRIGOUT Register

Return to Summary Table

Table 14-15648. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EE8h

Figure 14-7698. CSCTI_ITTRIGOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUT							
R/W							
0h							

Table 14-15649. CSCTI_ITTRIGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUT	R/W	0h	Sets the value of the CTTRIGOUT outputs

14.8.1.2.628 CSCTI_ITCHOUTACK Register

14.8.1.2.628.1 CSCTI_ITCHOUTACK Register (Offset = EECh) [reset = 0h]

ITCHOUTACK Register

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Table 14-15650. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EECh

Figure 14-7699. CSCTI_ITCHOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTCHOUTACK							
R/W							
0h							

Table 14-15651. CSCTI_ITCHOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTCHOUTACK	R/W	0h	Sets the value of the CTCHOUTACK outputs

14.8.1.2.629 CSCTI_ITTRIGOUTACK Register

14.8.1.2.629.1 CSCTI_ITTRIGOUTACK Register (Offset = EF0h) [reset = 0h]

ITTRIGOUTACK Register

Return to Summary Table

Table 14-15652. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EF0h

Figure 14-7700. CSCTI_ITTRIGOUTACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGOUTACK							
R							
0h							

Table 14-15653. CSCTI_ITTRIGOUTACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGOUTACK	R	0h	Reads the value of the CTTRIGOUTACK inputs

14.8.1.2.630 CSCTI_ITCHIN Register

14.8.1.2.630.1 CSCTI_ITCHIN Register (Offset = EF4h) [reset = 0h]

ITCHIN Register

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Table 14-15654. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EF4h

Figure 14-7701. CSCTI_ITCHIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CTCHIN			
R				R			
0h				0h			

Table 14-15655. CSCTI_ITCHIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CTCHIN	R	0h	Reads the value of the CTCHIN inputs

14.8.1.2.631 CSCTI_ITTRIGIN Register

14.8.1.2.631.1 CSCTI_ITTRIGIN Register (Offset = EF8h) [reset = 0h]

ITTRIGIN Register

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Table 14-15656. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1EF8h

Figure 14-7702. CSCTI_ITTRIGIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTTRIGIN							
R							
0h							

Table 14-15657. CSCTI_ITTRIGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	CTTRIGIN	R	0h	Reads the value of the CTTRIGIN inputs

14.8.1.2.632 CSCTI_ITCTRL Register

14.8.1.2.632.1 CSCTI_ITCTRL Register (Offset = F00h) [reset = 0h]

ITCTRL Register

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Table 14-15658. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1F00h

Figure 14-7703. CSCTI_ITCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							ITEN
R							R/W
0h							0h

Table 14-15659. CSCTI_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	ITEN	R/W	0h	Integration Test control enable

14.8.1.2.633 CSCTI_CLAIMSET Register

14.8.1.2.633.1 CSCTI_CLAIMSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-15660. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FA0h

Figure 14-7704. CSCTI_CLAIMSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-15661. CSCTI_CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.8.1.2.634 CSCTI_CLAIMCLR Register

14.8.1.2.634.1 CSCTI_CLAIMCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-15662. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FA4h

Figure 14-7705. CSCTI_CLAIMCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_CLEAR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15663. CSCTI_CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.8.1.2.635 CSCTI_LOCKACCESS Register

14.8.1.2.635.1 CSCTI_LOCKACCESS Register (Offset = FB0h) [reset = 0h]

Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-15664. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FB0h

Figure 14-7706. CSCTI_LOCKACCESS Name Register

31	30	29	28	27	26	25	24
LOCKACCESSREG							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCKACCESSREG							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCKACCESSREG							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCKACCESSREG							
R/W							
0h							

Table 14-15665. CSCTI_LOCKACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCKACCESSREG	R/W	0h	Software must write 0xC5ACCE55 to this register in order for application to gain access to the other registers If paddrdbg31 is high, this is ignored

14.8.1.2.636 CSCTI_LOCKSTATUS Register

14.8.1.2.636.1 CSCTI_LOCKSTATUS Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-15666. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FB4h

Figure 14-7707. CSCTI_LOCKSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-15667. CSCTI_LOCKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.8.1.2.637 CSCTI_AUTHSTATUS Register

14.8.1.2.637.1 CSCTI_AUTHSTATUS Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-15668. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FB8h

Figure 14-7708. CSCTI_AUTHSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				AUTHENTICATION_STATUS			
R				R			
0h				0h			

Table 14-15669. CSCTI_AUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.8.1.2.638 CSCTI_DEVID Register

14.8.1.2.638.1 CSCTI_DEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-15670. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FC8h

Figure 14-7709. CSCTI_DEVID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">NUM_ECT_CHANNELS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NUM_ECT_TRIGGERS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED7_5</td><td colspan="5">IMPLEMENTATION_DEFINED</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
</table>

Table 14-15671. CSCTI_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	R	0h	Reserved, returns 0
19:16	NUM_ECT_CHANNELS	R	0h	Number of ECT Channels available
15:8	NUM_ECT_TRIGGERS	R	0h	Number of ECT trigger available
7:5	RESERVED7_5	R	0h	Reserved, returns 0
4:0	IMPLEMENTATION_DEFINED	R	0h	Indicates the number of multiplexing available on Trigger Inputs and Outputs using ASICCTL Defailt value of 0 indicates no multiplexing present

14.8.1.2.639 CSCTI_DEVTYPE Register

14.8.1.2.639.1 CSCTI_DEVTYPE Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

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Table 14-15672. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FCCh

Figure 14-7710. CSCTI_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-15673. CSCTI_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	Device Type Identifier

14.8.1.2.640 CSCTI_PERIPHID4 Register

14.8.1.2.640.1 CSCTI_PERIPHID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

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Table 14-15674. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FD0h

Figure 14-7711. CSCTI_PERIPHID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-15675. CSCTI_PERIPHID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.8.1.2.641 CSCTI_PERIPHID0 Register

14.8.1.2.641.1 CSCTI_PERIPHID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

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Table 14-15676. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FE0h

Figure 14-7712. CSCTI_PERIPHID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-15677. CSCTI_PERIPHID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.8.1.2.642 CSCTI_PERIPHID1 Register

14.8.1.2.642.1 CSCTI_PERIPHID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

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Table 14-15678. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FE4h

Figure 14-7713. CSCTI_PERIPHID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID1							
R							
0h							

Table 14-15679. CSCTI_PERIPHID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.8.1.2.643 CSCTI_PERIPHID2 Register

14.8.1.2.643.1 CSCTI_PERIPHID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

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Table 14-15680. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FE8h

Figure 14-7714. CSCTI_PERIPHID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-15681. CSCTI_PERIPHID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.8.1.2.644 CSCTI_PERIPHID3 Register

14.8.1.2.644.1 CSCTI_PERIPHID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

Return to Summary Table

Table 14-15682. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FECh

Figure 14-7715. CSCTI_PERIPHID3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PERPIH_ID3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15683. CSCTI_PERIPHID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.8.1.2.645 CSCTI_COMPONID0 Register

14.8.1.2.645.1 CSCTI_COMPONID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

Return to Summary Table

Table 14-15684. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FF0h

Figure 14-7716. CSCTI_COMPONID0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP_ID0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15685. CSCTI_COMPONID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.646 CSCTI_COMPONID1 Register

14.8.1.2.646.1 CSCTI_COMPONID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

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Table 14-15686. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FF4h

Figure 14-7717. CSCTI_COMPONID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-15687. CSCTI_COMPONID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.647 CSCTI_COMPONID2 Register

14.8.1.2.647.1 CSCTI_COMPONID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

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Table 14-15688. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FF8h

Figure 14-7718. CSCTI_COMPONID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
0h							

Table 14-15689. CSCTI_COMPONID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.648 CSCTI_COMPONID3 Register

14.8.1.2.648.1 CSCTI_COMPONID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

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Table 14-15690. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 1FFCh

Figure 14-7719. CSCTI_COMPONID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-15691. CSCTI_COMPONID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.649 DRM_CFG_1_PERIPH_ID Register

14.8.1.2.649.1 DRM_CFG_1_PERIPH_ID Register (Offset = 0h) [reset = 62836100h]

This register is used to determine what the functionality of this peripheral is.

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Table 14-15692. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2000h

Figure 14-7720. DRM_CFG_1_PERIPH_ID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		283h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
283h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLREV					MAJOR		
R					R		
Ch					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 14-15693. DRM_CFG_1_PERIPH_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Peripheral ID Scheme [0]
29:28	BU	R	2h	Reserved, returns 0
27:16	FUNCTION	R	283h	DRM Function ID [0x211]
15:11	RTLREV	R	Ch	RTL Revision [0]
10:8	MAJOR	R	1h	Major Peripheral Revision [0]
7:6	CUSTOM	R	0h	Custon Peripheral ID version [0]
5:0	MINOR	R	0h	Minor Peripheral Revision [0]

14.8.1.2.650 DRM_CFG_1_VERSION Register

14.8.1.2.650.1 DRM_CFG_1_VERSION Register (Offset = 4h) [reset = 0h]

This register is used to enable the Time Generator. For application access, the DTG must be unlocked first.

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Table 14-15694. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2004h

Figure 14-7721. DRM_CFG_1_VERSION Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">MAJOR_VERSION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">MAJOR_VERSION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MINOR_VERSION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MINOR_VERSION</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15695. DRM_CFG_1_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MAJOR_VERSION	R	0h	Contains the major version value [1]
15:0	MINOR_VERSION	R	0h	Contains the minor version value [0]

14.8.1.2.651 DRM_CFG_1_CAPABILITY Register

14.8.1.2.651.1 DRM_CFG_1_CAPABILITY Register (Offset = 8h) [reset = 0h]

This register can be read to determine the number of suspend signals and number of peripherals.

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Table 14-15696. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2008h

Figure 14-7722. DRM_CFG_1_CAPABILITY Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		NUM_SUSPENDS					
R		R					
0h		0h					
7	6	5	4	3	2	1	0
NUM_PERIPHERALS							
R							
0h							

Table 14-15697. DRM_CFG_1_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13:8	NUM_SUSPENDS	R	0h	Contains the number of Suspend signals supported, max of 32 There should be one signal per processor This value is set by a parameter at synthesis time
7:0	NUM_PERIPHERALS	R	0h	Contains the number of peripherals supported, max of 128 This affects the number of SUSPEND_REG registers This is set by a parameter during synthesis

14.8.1.2.652 DRM_CFG_1_TRACE_CTRL Register

14.8.1.2.652.1 DRM_CFG_1_TRACE_CTRL Register (Offset = Ch) [reset = 0h]

This register is used to set the trace sampling mode to center(1) or edge(0).

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Table 14-15698. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 200Ch

Figure 14-7723. DRM_CFG_1_TRACE_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							CENTER_SAMPLING
R							R/W
0h							0h

Table 14-15699. DRM_CFG_1_TRACE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	CENTER_SAMPLING	R/W	0h	Sets trace to center sampled

14.8.1.2.653 DRM_CFG_1_VBUSM_CTRL Register

14.8.1.2.653.1 DRM_CFG_1_VBUSM_CTRL Register (Offset = 10h) [reset = 0h]

This register is used to set attributes on the VBUSM memory accesses and to read the Debug Operating Mode

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Table 14-15700. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2010h

Figure 14-7724. DRM_CFG_1_VBUSM_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">DOM_INPUT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">DOM_INPUT</td><td colspan="5">RESERVED</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">VBUSM_PRIV</td><td>VBUSM_SECURE</td><td>VBUSM_DEBUG</td><td colspan="2">CTL_PRIV</td><td>CTL_SECURE</td><td>EMUDBG</td></tr>
<tr><td colspan="2">R</td><td>R</td><td>R</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15701. DRM_CFG_1_VBUSM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	DOM_INPUT	R	0h	This returns the DOM security input The upper 3 bits are the debug operating mode and the lower 8 bits are the priviledge ID for VBUSM transaction
20:8	RESERVED	R	0h	Reserved bits, return 0
7:6	VBUSM_PRIV	R	0h	These two bits show the currently state of the priv bits
5	VBUSM_SECURE	R	0h	This bit shows the currently active state of the VBUSM secure bit
4	VBUSM_DEBUG	R	0h	This is the currently active state of the VBUSM emudbg bit
3:2	CTL_PRIV	R/W	0h	These two bits determine the priviledge type for VBUSM accesses unless overridden by the DOM input [0 is user level privilege, 1 is supervisor level privilege, 2 is hypervisor level privilege and 3 is reserved]
1	CTL_SECURE	R/W	0h	When set [and DOM permits it], the VBUSM accesses will have the secure bit set
0	EMUDBG	R/W	0h	Sets the emudbg bit during access to make the debug or non-debug

14.8.1.2.654 DRM_CFG_1_DAP_TIMEOUT Register

14.8.1.2.654.1 DRM_CFG_1_DAP_TIMEOUT Register (Offset = 14h) [reset = 0h]

This register is used to set the maximum wait time for the DAP to complete a memory access.

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Table 14-15702. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2014h

Figure 14-7725. DRM_CFG_1_DAP_TIMEOUT Name Register

31	30	29	28	27	26	25	24
DAP_TIMEOUT_REGISTER							
R/W							
0h							
23	22	21	20	19	18	17	16
DAP_TIMEOUT_REGISTER							
R/W							
0h							
15	14	13	12	11	10	9	8
DAP_TIMEOUT_REGISTER							
R/W							
0h							
7	6	5	4	3	2	1	0
DAP_TIMEOUT_REGISTER							
R/W							
0h							

Table 14-15703. DRM_CFG_1_DAP_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAP_TIMEOUT_REGISTER	R/W	0h	

14.8.1.2.655 DRM_CFG_1_CONFIG Register

14.8.1.2.655.1 DRM_CFG_1_CONFIG Register (Offset = 18h) [reset = 0h]

This register adds softreset capability to the suspend module.

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Table 14-15704. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2018h

Figure 14-7726. DRM_CFG_1_CONFIG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>SOFTRESET</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-15705. DRM_CFG_1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	SOFTRESET	R/W	0h	Software controlled reset of the DRM

14.8.1.2.656 DRM_CFG_1_EMUTRIGEN Register

14.8.1.2.656.1 DRM_CFG_1_EMUTRIGEN Register (Offset = 1Ch) [reset = 0h]

This register is used to enable EMU triggers.

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Table 14-15706. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 201Ch

Figure 14-7727. DRM_CFG_1_EMUTRIGEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						EMU1TRIGEN	EMU0TRIGEN
R						R/W	R/W
0h						0h	0h

Table 14-15707. DRM_CFG_1_EMUTRIGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1	EMU1TRIGEN	R/W	0h	EMU 1 Trigger En
0	EMU0TRIGEN	R/W	0h	EMU 0 Trigger En

14.8.1.2.657 DRM_CFG_1_BINVALLO Register

14.8.1.2.657.1 DRM_CFG_1_BINVALLO Register (Offset = 20h) [reset = 0h]

Reading this register returns the lower 32 bits of the binary debug time.

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Table 14-15708. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2020h

Figure 14-7728. DRM_CFG_1_BINVALLO Name Register

31	30	29	28	27	26	25	24
DTG_BINARY_TIME_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
DTG_BINARY_TIME_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
DTG_BINARY_TIME_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
DTG_BINARY_TIME_LOW							
R/W							
0h							

Table 14-15709. DRM_CFG_1_BINVALLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DTG_BINARY_TIME_LOW	R/W	0h	

14.8.1.2.658 DRM_CFG_1_BINVALHI Register

14.8.1.2.658.1 DRM_CFG_1_BINVALHI Register (Offset = 24h) [reset = 0h]

Reading this register returns the upper 16 bits of the binary debug time and causes the lower 32 bits to be latched.

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Table 14-15710. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2024h

Figure 14-7729. DRM_CFG_1_BINVALHI Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED	BINTIMEHI						
NONE	R						
0h	0h						
7	6	5	4	3	2	1	0
BINTIMEHI							
R							
0h							

Table 14-15711. DRM_CFG_1_BINVALHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	Reserved, returns 0
15	RESERVED	NONE	0h	Reserved
14:0	BINTIMEHI	R	0h	Upper 16 bits of the timer

14.8.1.2.659 DRM_CFG_1_SUSPEND_REG0 Register

14.8.1.2.659.1 DRM_CFG_1_SUSPEND_REG0 Register (Offset = 200h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. There can be upto 128 of these registers (See NUM_PERIPHERALS in the DRM_CAPABILITY register)

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Table 14-15712. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2200h

Figure 14-7730. DRM_CFG_1_SUSPEND_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED1</td><td>SELECT</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SELECT</td><td colspan="3">RESERVED0</td><td>SUSPEND_CTL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="3">0h</td><td>0h</td></tr>
</table>

Table 14-15713. DRM_CFG_1_SUSPEND_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED1	R	0h	Reserved, returns 0
8:4	SELECT	R/W	0h	Selects which suspend control line [1-32] goes to the peripheral
3:1	RESERVED0	R	0h	Reserved, returns 0
0	SUSPEND_CTL	R/W	0h	When 1, the peripheral is sensitive to the suspend signal, when 0, it ignore it

14.8.1.2.660 DRM_CFG_1_SUSPEND_REG1 Register

14.8.1.2.660.1 DRM_CFG_1_SUSPEND_REG1 Register (Offset = 204h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15714. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2204h

Figure 14-7731. DRM_CFG_1_SUSPEND_REG1 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_1							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_1							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_1							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_1							
R/W							
0h							

Table 14-15715. DRM_CFG_1_SUSPEND_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_1	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.661 DRM_CFG_1_SUSPEND_REG2 Register

14.8.1.2.661.1 DRM_CFG_1_SUSPEND_REG2 Register (Offset = 208h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15716. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2208h

Figure 14-7732. DRM_CFG_1_SUSPEND_REG2 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_2							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_2							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_2							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_2							
R/W							
0h							

Table 14-15717. DRM_CFG_1_SUSPEND_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_2	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.662 DRM_CFG_1_SUSPEND_REG3 Register

14.8.1.2.662.1 DRM_CFG_1_SUSPEND_REG3 Register (Offset = 20Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15718. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 220Ch

Figure 14-7733. DRM_CFG_1_SUSPEND_REG3 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_3							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_3							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_3							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_3							
R/W							
0h							

Table 14-15719. DRM_CFG_1_SUSPEND_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_3	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.663 DRM_CFG_1_SUSPEND_REG4 Register

14.8.1.2.663.1 DRM_CFG_1_SUSPEND_REG4 Register (Offset = 210h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15720. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2210h

Figure 14-7734. DRM_CFG_1_SUSPEND_REG4 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_4							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_4							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_4							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_4							
R/W							
0h							

Table 14-15721. DRM_CFG_1_SUSPEND_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_4	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.664 DRM_CFG_1_SUSPEND_REG5 Register

14.8.1.2.664.1 DRM_CFG_1_SUSPEND_REG5 Register (Offset = 214h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15722. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2214h

Figure 14-7735. DRM_CFG_1_SUSPEND_REG5 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_5							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_5							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_5							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_5							
R/W							
0h							

Table 14-15723. DRM_CFG_1_SUSPEND_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_5	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.665 DRM_CFG_1_SUSPEND_REG6 Register

14.8.1.2.665.1 DRM_CFG_1_SUSPEND_REG6 Register (Offset = 218h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15724. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2218h

Figure 14-7736. DRM_CFG_1_SUSPEND_REG6 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_6							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_6							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_6							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_6							
R/W							
0h							

Table 14-15725. DRM_CFG_1_SUSPEND_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_6	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.666 DRM_CFG_1_SUSPEND_REG7 Register

14.8.1.2.666.1 DRM_CFG_1_SUSPEND_REG7 Register (Offset = 21Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15726. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 221Ch

Figure 14-7737. DRM_CFG_1_SUSPEND_REG7 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_7							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_7							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_7							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_7							
R/W							
0h							

Table 14-15727. DRM_CFG_1_SUSPEND_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_7	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.667 DRM_CFG_1_SUSPEND_REG8 Register

14.8.1.2.667.1 DRM_CFG_1_SUSPEND_REG8 Register (Offset = 220h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15728. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2220h

Figure 14-7738. DRM_CFG_1_SUSPEND_REG8 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_8							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_8							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_8							
R/W							
0h							

Table 14-15729. DRM_CFG_1_SUSPEND_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_8	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.668 DRM_CFG_1_SUSPEND_REG9 Register

14.8.1.2.668.1 DRM_CFG_1_SUSPEND_REG9 Register (Offset = 224h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15730. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2224h

Figure 14-7739. DRM_CFG_1_SUSPEND_REG9 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_9							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SUSPEND_REG_9							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SUSPEND_REG_9							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUSPEND_REG_9							
R/W							
0h							

Table 14-15731. DRM_CFG_1_SUSPEND_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_9	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.669 DRM_CFG_1_SUSPEND_REG10 Register

14.8.1.2.669.1 DRM_CFG_1_SUSPEND_REG10 Register (Offset = 228h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15732. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2228h

Figure 14-7740. DRM_CFG_1_SUSPEND_REG10 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_10							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_10							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_10							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_10							
R/W							
0h							

Table 14-15733. DRM_CFG_1_SUSPEND_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_10	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.670 DRM_CFG_1_SUSPEND_REG11 Register

14.8.1.2.670.1 DRM_CFG_1_SUSPEND_REG11 Register (Offset = 22Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15734. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 222Ch

Figure 14-7741. DRM_CFG_1_SUSPEND_REG11 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_11							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_11							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_11							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_11							
R/W							
0h							

Table 14-15735. DRM_CFG_1_SUSPEND_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_11	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.671 DRM_CFG_1_SUSPEND_REG12 Register

14.8.1.2.671.1 DRM_CFG_1_SUSPEND_REG12 Register (Offset = 230h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15736. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2230h

Figure 14-7742. DRM_CFG_1_SUSPEND_REG12 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_12							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_12							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_12							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_12							
R/W							
0h							

Table 14-15737. DRM_CFG_1_SUSPEND_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_12	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.672 DRM_CFG_1_SUSPEND_REG13 Register

14.8.1.2.672.1 DRM_CFG_1_SUSPEND_REG13 Register (Offset = 234h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15738. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2234h

Figure 14-7743. DRM_CFG_1_SUSPEND_REG13 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_13							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_13							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_13							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_13							
R/W							
0h							

Table 14-15739. DRM_CFG_1_SUSPEND_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_13	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.673 DRM_CFG_1_SUSPEND_REG14 Register

14.8.1.2.673.1 DRM_CFG_1_SUSPEND_REG14 Register (Offset = 238h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15740. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2238h

Figure 14-7744. DRM_CFG_1_SUSPEND_REG14 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_14							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_14							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_14							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_14							
R/W							
0h							

Table 14-15741. DRM_CFG_1_SUSPEND_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_14	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.674 DRM_CFG_1_SUSPEND_REG15 Register

14.8.1.2.674.1 DRM_CFG_1_SUSPEND_REG15 Register (Offset = 23Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15742. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 223Ch

Figure 14-7745. DRM_CFG_1_SUSPEND_REG15 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_15							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_15							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_15							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_15							
R/W							
0h							

Table 14-15743. DRM_CFG_1_SUSPEND_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_15	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.675 DRM_CFG_1_SUSPEND_REG16 Register

14.8.1.2.675.1 DRM_CFG_1_SUSPEND_REG16 Register (Offset = 240h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15744. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2240h

Figure 14-7746. DRM_CFG_1_SUSPEND_REG16 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_16							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_16							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_16							
R/W							
0h							

Table 14-15745. DRM_CFG_1_SUSPEND_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_16	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.676 DRM_CFG_1_SUSPEND_REG17 Register

14.8.1.2.676.1 DRM_CFG_1_SUSPEND_REG17 Register (Offset = 244h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15746. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2244h

Figure 14-7747. DRM_CFG_1_SUSPEND_REG17 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_17							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_17							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_17							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_17							
R/W							
0h							

Table 14-15747. DRM_CFG_1_SUSPEND_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_17	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.677 DRM_CFG_1_SUSPEND_REG18 Register

14.8.1.2.677.1 DRM_CFG_1_SUSPEND_REG18 Register (Offset = 248h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15748. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2248h

Figure 14-7748. DRM_CFG_1_SUSPEND_REG18 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_18							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_18							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_18							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_18							
R/W							
0h							

Table 14-15749. DRM_CFG_1_SUSPEND_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_18	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.678 DRM_CFG_1_SUSPEND_REG19 Register

14.8.1.2.678.1 DRM_CFG_1_SUSPEND_REG19 Register (Offset = 24Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15750. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 224Ch

Figure 14-7749. DRM_CFG_1_SUSPEND_REG19 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_19							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_19							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_19							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_19							
R/W							
0h							

Table 14-15751. DRM_CFG_1_SUSPEND_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_19	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.679 DRM_CFG_1_SUSPEND_REG20 Register

14.8.1.2.679.1 DRM_CFG_1_SUSPEND_REG20 Register (Offset = 250h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15752. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2250h

Figure 14-7750. DRM_CFG_1_SUSPEND_REG20 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_20							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_20							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_20							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_20							
R/W							
0h							

Table 14-15753. DRM_CFG_1_SUSPEND_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_20	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.680 DRM_CFG_1_SUSPEND_REG21 Register

14.8.1.2.680.1 DRM_CFG_1_SUSPEND_REG21 Register (Offset = 254h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15754. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2254h

Figure 14-7751. DRM_CFG_1_SUSPEND_REG21 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_21							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_21							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_21							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_21							
R/W							
0h							

Table 14-15755. DRM_CFG_1_SUSPEND_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_21	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.681 DRM_CFG_1_SUSPEND_REG22 Register

14.8.1.2.681.1 DRM_CFG_1_SUSPEND_REG22 Register (Offset = 258h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15756. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2258h

Figure 14-7752. DRM_CFG_1_SUSPEND_REG22 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_22							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_22							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_22							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_22							
R/W							
0h							

Table 14-15757. DRM_CFG_1_SUSPEND_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_22	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.682 DRM_CFG_1_SUSPEND_REG23 Register

14.8.1.2.682.1 DRM_CFG_1_SUSPEND_REG23 Register (Offset = 25Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15758. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 225Ch

Figure 14-7753. DRM_CFG_1_SUSPEND_REG23 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_23							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_23							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_23							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_23							
R/W							
0h							

Table 14-15759. DRM_CFG_1_SUSPEND_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_23	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.683 DRM_CFG_1_SUSPEND_REG24 Register

14.8.1.2.683.1 DRM_CFG_1_SUSPEND_REG24 Register (Offset = 260h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15760. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2260h

Figure 14-7754. DRM_CFG_1_SUSPEND_REG24 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_24							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_24							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_24							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_24							
R/W							
0h							

Table 14-15761. DRM_CFG_1_SUSPEND_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_24	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.684 DRM_CFG_1_SUSPEND_REG25 Register

14.8.1.2.684.1 DRM_CFG_1_SUSPEND_REG25 Register (Offset = 264h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15762. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2264h

Figure 14-7755. DRM_CFG_1_SUSPEND_REG25 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_25							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_25							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_25							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_25							
R/W							
0h							

Table 14-15763. DRM_CFG_1_SUSPEND_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_25	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.685 DRM_CFG_1_SUSPEND_REG26 Register

14.8.1.2.685.1 DRM_CFG_1_SUSPEND_REG26 Register (Offset = 268h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15764. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2268h

Figure 14-7756. DRM_CFG_1_SUSPEND_REG26 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_26							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_26							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_26							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_26							
R/W							
0h							

Table 14-15765. DRM_CFG_1_SUSPEND_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_26	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.686 DRM_CFG_1_SUSPEND_REG27 Register

14.8.1.2.686.1 DRM_CFG_1_SUSPEND_REG27 Register (Offset = 26Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15766. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 226Ch

Figure 14-7757. DRM_CFG_1_SUSPEND_REG27 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">SUSPEND_REG_27</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">SUSPEND_REG_27</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">SUSPEND_REG_27</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">SUSPEND_REG_27</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15767. DRM_CFG_1_SUSPEND_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_27	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.687 DRM_CFG_1_SUSPEND_REG28 Register

14.8.1.2.687.1 DRM_CFG_1_SUSPEND_REG28 Register (Offset = 270h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15768. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2270h

Figure 14-7758. DRM_CFG_1_SUSPEND_REG28 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_28							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_28							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_28							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_28							
R/W							
0h							

Table 14-15769. DRM_CFG_1_SUSPEND_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_28	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.688 DRM_CFG_1_SUSPEND_REG29 Register

14.8.1.2.688.1 DRM_CFG_1_SUSPEND_REG29 Register (Offset = 274h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15770. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2274h

Figure 14-7759. DRM_CFG_1_SUSPEND_REG29 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_29							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_29							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_29							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_29							
R/W							
0h							

Table 14-15771. DRM_CFG_1_SUSPEND_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_29	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.689 DRM_CFG_1_SUSPEND_REG30 Register

14.8.1.2.689.1 DRM_CFG_1_SUSPEND_REG30 Register (Offset = 278h) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15772. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 2278h

Figure 14-7760. DRM_CFG_1_SUSPEND_REG30 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_30							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_30							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_30							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_30							
R/W							
0h							

Table 14-15773. DRM_CFG_1_SUSPEND_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_30	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.690 DRM_CFG_1_SUSPEND_REG31 Register

14.8.1.2.690.1 DRM_CFG_1_SUSPEND_REG31 Register (Offset = 27Ch) [reset = 0h]

The DRM Suspend Registers merge the emulation suspend signals sent by various processors, when it wishes to suspend the activity of connected peripherals during debugging. See Suspend Reg 0 for details

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Table 14-15774. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 227Ch

Figure 14-7761. DRM_CFG_1_SUSPEND_REG31 Name Register

31	30	29	28	27	26	25	24
SUSPEND_REG_31							
R/W							
0h							
23	22	21	20	19	18	17	16
SUSPEND_REG_31							
R/W							
0h							
15	14	13	12	11	10	9	8
SUSPEND_REG_31							
R/W							
0h							
7	6	5	4	3	2	1	0
SUSPEND_REG_31							
R/W							
0h							

Table 14-15775. DRM_CFG_1_SUSPEND_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUSPEND_REG_31	R/W	0h	See Suspend Reg 0 for field information

14.8.1.2.691 CSTPIU_CFG_1_SUPPORTSIZE Register

14.8.1.2.691.1 CSTPIU_CFG_1_SUPPORTSIZE Register (Offset = 0h) [reset = FFFFFFFFh]

This register indicates how many trace pins are available for export. One pin per bit, right justified

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Table 14-15776. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4000h

Figure 14-7762. CSTPIU_CFG_1_SUPPORTSIZE Name Register

31	30	29	28	27	26	25	24
SUPPORTSIZEREG							
R							
FFFFFFFFh							
23	22	21	20	19	18	17	16
SUPPORTSIZEREG							
R							
FFFFFFFFh							
15	14	13	12	11	10	9	8
SUPPORTSIZEREG							
R							
FFFFFFFFh							
7	6	5	4	3	2	1	0
SUPPORTSIZEREG							
R							
FFFFFFFFh							

Table 14-15777. CSTPIU_CFG_1_SUPPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUPPORTSIZEREG	R	FFFFFFFFh	This register indicates how many trace pins are available for export. One pin per bit, right justified

14.8.1.2.692 CSTPIU_CFG_1_CURPORTSIZE Register

14.8.1.2.692.1 CSTPIU_CFG_1_CURPORTSIZE Register (Offset = 4h) [reset = 1h]

The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

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Table 14-15778. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4004h

Figure 14-7763. CSTPIU_CFG_1_CURPORTSIZE Name Register

31	30	29	28	27	26	25	24
CURRENTPORTSIZE							
R/W							
1h							
23	22	21	20	19	18	17	16
CURRENTPORTSIZE							
R/W							
1h							
15	14	13	12	11	10	9	8
CURRENTPORTSIZE							
R/W							
1h							
7	6	5	4	3	2	1	0
CURRENTPORTSIZE							
R/W							
1h							

Table 14-15779. CSTPIU_CFG_1_CURPORTSIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CURRENTPORTSIZE	R/W	1h	The Current Port Size Register has the same format as the Supported Port Sizes register but only one bit is set, and all others must be zero

14.8.1.2.693 CSTPIU_CFG_1_TRIGMODEREG Register

14.8.1.2.693.1 CSTPIU_CFG_1_TRIGMODEREG Register (Offset = 100h) [reset = 0h]

This register indicates the implemented Trigger Counter multipliers and other supported features of the trigger system

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Table 14-15780. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4100h

Figure 14-7764. CSTPIU_CFG_1_TRIGMODEREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED						TRGRUN	TRIGGERED
R						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED2							TCOUNT8
R							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED1			MUILTPLIERS				
R			R				
0h			0h				

Table 14-15781. CSTPIU_CFG_1_TRIGMODEREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17	TRGRUN	R	0h	Trigger Counter running. A trigger has occurred but the counter is not at zero.
16	TRIGGERED	R	0h	A trigger has occurred and the counter has reached zero.
15:9	RESERVED2	R	0h	Reserved, returns 0
8	TCOUNT8	R	0h	An 8-bit wide counter register implemented.
7:5	RESERVED1	R	0h	Reserved, returns 0
4:0	MUILTPLIERS	R	0h	Multiply the Trigger Counter by 2, 4, 16, 256, 64K supported. Each bit is a mpy value.

14.8.1.2.694 CSTPIU_CFG_1_TRIGCTRREG Register

14.8.1.2.694.1 CSTPIU_CFG_1_TRIGCTRREG Register (Offset = 104h) [reset = 0h]

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Table 14-15782. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4104h

Figure 14-7765. CSTPIU_CFG_1_TRIGCTRREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TRIGCOUNT							
R/W							
0h							

Table 14-15783. CSTPIU_CFG_1_TRIGCTRREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	TRIGCOUNT	R/W	0h	8-bit counter value for the number of words to be output from the formatter before a trigger is inserted.

14.8.1.2.695 CSTPIU_CFG_1_TRIGMPYREG Register

14.8.1.2.695.1 CSTPIU_CFG_1_TRIGMPYREG Register (Offset = 108h) [reset = 0h]

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Table 14-15784. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4108h

Figure 14-7766. CSTPIU_CFG_1_TRIGMPYREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED			MULTIPLIER				
R			R/W				
0h			0h				

Table 14-15785. CSTPIU_CFG_1_TRIGMPYREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4:0	MULTIPLIER	R/W	0h	Trigger multiply value bit0=x2, bit1=x4, bit2=x16, bit3=x256, bit4=x64K.

14.8.1.2.696 CSTPIU_CFG_1_SUPTESTPAT Register

14.8.1.2.696.1 CSTPIU_CFG_1_SUPTESTPAT Register (Offset = 200h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-15786. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4200h

Figure 14-7767. CSTPIU_CFG_1_SUPTESTPAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MODE</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td colspan="4">PATTERN</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15787. CSTPIU_CFG_1_SUPTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R	0h	bit 16 is Timed Mode, bit 17 is continuous mode
15:4	RESERVED1	R	0h	Reserved, returns 0
3:0	PATTERN	R	0h	bit0=Walking 1 pattern, bit1=walking 0, bit2=AA/55 pattern, bit3=FF/00 pattern

14.8.1.2.697 CSTPIU_CFG_1_CURTESTPAT Register

14.8.1.2.697.1 CSTPIU_CFG_1_CURTESTPAT Register (Offset = 204h) [reset = 0h]

This register displays the supported patterns and modes for calibration

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Table 14-15788. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4204h

Figure 14-7768. CSTPIU_CFG_1_CURTESTPAT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">MODE</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED1</td><td>RESERVED</td><td colspan="3">PATTERN</td></tr>
<tr><td colspan="4">R</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 14-15789. CSTPIU_CFG_1_CURTESTPAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	R	0h	Reserved, returns 0
17:16	MODE	R/W	0h	Select the Pattern Timer Mode, see Supported Patterns reg
15:4	RESERVED1	R	0h	Reserved, returns 0
3	RESERVED	NONE	0h	Reserved
2:0	PATTERN	R/W	0h	Select the pattern to run, set Supported Patterns Reg

14.8.1.2.698 CSTPIU_CFG_1_TESTPATCNT Register

14.8.1.2.698.1 CSTPIU_CFG_1_TESTPATCNT Register (Offset = 208h) [reset = 0h]

This register displays the supported patterns and modes for calibration

Return to Summary Table

Table 14-15790. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4208h

Figure 14-7769. CSTPIU_CFG_1_TESTPATCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PATTERNCOUNT							
R/W							
0h							

Table 14-15791. CSTPIU_CFG_1_TESTPATCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PATTERNCOUNT	R/W	0h	Number of clocks a pattern should run before going to the next pattern

14.8.1.2.699 CSTPIU_CFG_1_FORMFLUSHSTAT Register

14.8.1.2.699.1 CSTPIU_CFG_1_FORMFLUSHSTAT Register (Offset = 300h) [reset = 0h]

This register displays the supported patterns and modes for calibration

Return to Summary Table

Table 14-15792. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4300h

Figure 14-7770. CSTPIU_CFG_1_FORMFLUSHSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					TCPRESENT	FTSTOPPED	FLINPROG
R					R	R	R
0h					0h	0h	0h

Table 14-15793. CSTPIU_CFG_1_FORMFLUSHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	TCPRESENT	R	0h	If this bit is set then TRACECTL is present. If no TRACECTL pin is present, then the data formatter must be used and only in continuous mode
1	FTSTOPPED	R	0h	Formatter stopped. The formatter has received a stop request signal and all trace data and post-amble has been output.
0	FLINPROG	R	0h	Flush In Progress. This is an indication of the current state of AFVALIDS.

14.8.1.2.700 CSTPIU_CFG_1_FORMFLUSHCTL Register

14.8.1.2.700.1 CSTPIU_CFG_1_FORMFLUSHCTL Register (Offset = 304h) [reset = 0h]

This register controls the generation of stop, trigger, and flush events.

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Table 14-15794. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4304h

Figure 14-7771. CSTPIU_CFG_1_FORMFLUSHCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		STOPTRIG	STOPFL	RESERVED3	TRIGFL	TRIGEVT	TRIGIN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2	FONMAN	FONTRIG	FONFIIN	RESERVED1		ENFCONT	ENFTC
R	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h

Table 14-15795. CSTPIU_CFG_1_FORMFLUSHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	R	0h	Reserved, returns 0
13	STOPTRIG	R/W	0h	Stop the formatter after a Trigger Event is observed
12	STOPFL	R/W	0h	Stop the formatter after a flush completes [return of AFREADYS].
11	RESERVED3	R	0h	Reserved, returns 0
10	TRIGFL	R/W	0h	Indicates a trigger on Flush completion on AFREADYS being returned
9	TRIGEVT	R/W	0h	Indicate a trigger on a Trigger Event.
8	TRIGIN	R/W	0h	Indicate a trigger on TRIGIN being asserted.
7	RESERVED2	R	0h	Reserved, returns 0
6	FONMAN	R/W	0h	Manually generate a flush of the system. It is cleared when this flush has been serviced.
5	FONTRIG	R/W	0h	Generate flush using Trigger event
4	FONFIIN	R/W	0h	Generate flush using the FLUSHIN interface.
3:2	RESERVED1	R	0h	Reserved, returns 0
1	ENFCONT	R/W	0h	Continuous Formatting. Embed in trigger packets and indicate null cycles using Sync packets
0	ENFTC	R/W	0h	Enable Formatting. Do not embed Triggers into the formatted stream

14.8.1.2.701 CSTPIU_CFG_1_FORMSYNCCTR Register

14.8.1.2.701.1 CSTPIU_CFG_1_FORMSYNCCTR Register (Offset = 308h) [reset = 40h]

This counter is the number of formatter frames since the last synchronization packet of 128 bits, and is a 12-bit counter with a maximum count value of 4096

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Table 14-15796. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4308h

Figure 14-7772. CSTPIU_CFG_1_FORMSYNCCTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				CYCCOUNT			
R				R/W			
0h				40h			
7	6	5	4	3	2	1	0
CYCCOUNT							
R/W							
40h							

Table 14-15797. CSTPIU_CFG_1_FORMSYNCCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:0	CYCCOUNT	R/W	40h	12-bit counter value to indicate the number of complete frames between full sync packets.

14.8.1.2.702 CSTPIU_CFG_1_EXTCTLIN Register

14.8.1.2.702.1 CSTPIU_CFG_1_EXTCTLIN Register (Offset = 400h) [reset = 0h]

This register inputs data from an external port (if used)

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Table 14-15798. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4400h

Figure 14-7773. CSTPIU_CFG_1_EXTCTLIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_INPUT_REGISTER							
R							
0h							

Table 14-15799. CSTPIU_CFG_1_EXTCTLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	reserved, returns 0
7:0	EXCTL_PORT_INPUT_REGISTER	R	0h	

14.8.1.2.703 CSTPIU_CFG_1_EXTCTLOUT Register

14.8.1.2.703.1 CSTPIU_CFG_1_EXTCTLOUT Register (Offset = 404h) [reset = 0h]

This register is output to an external port (if used)

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Table 14-15800. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4404h

Figure 14-7774. CSTPIU_CFG_1_EXTCTLOUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCTL_PORT_OUTPUT_REGISTER							
R/W							
0h							

Table 14-15801. CSTPIU_CFG_1_EXTCTLOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R/W	0h	returns 0
7:0	EXCTL_PORT_OUTPUT_REGISTER	R/W	0h	

14.8.1.2.704 CSTPIU_CFG_1_ITTRFLINACK Register

14.8.1.2.704.1 CSTPIU_CFG_1_ITTRFLINACK Register (Offset = EE4h) [reset = 0h]

Integration Test Trigger In and Flush In Acknowledge.

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Table 14-15802. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4EE4h

Figure 14-7775. CSTPIU_CFG_1_ITTRFLINACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
W							
0h							
23	22	21	20	19	18	17	16
RESERVED							
W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
W							
0h							
7	6	5	4	3	2	1	0
RESERVED						FLUSHINACK	TRIGINACK
W						W	W
0h						0h	0h

Table 14-15803. CSTPIU_CFG_1_ITTRFLINACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	W	0h	Reserved, returns 0
1	FLUSHINACK	W	0h	Writing this register sets the value of FLUSHINACK. Reading it returns the value of FLUSHINACK.
0	TRIGINACK	W	0h	Writing this register sets the value of TRIGINACK. Reading it returns the value of TRIGINACK.

14.8.1.2.705 CSTPIU_CFG_1_ITTRFLIN Register

14.8.1.2.705.1 CSTPIU_CFG_1_ITTRFLIN Register (Offset = EE8h) [reset = 0h]

Integration Test Trigger In and Flush In Register.

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Table 14-15804. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4EE8h

Figure 14-7776. CSTPIU_CFG_1_ITTRFLIN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						FLUSHIN	TRIGIN
R						R	R
0h						0h	0h

Table 14-15805. CSTPIU_CFG_1_ITTRFLIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1	FLUSHIN	R	0h	Reads the value of FlushIn
0	TRIGIN	R	0h	Reads the value of Trigin

14.8.1.2.706 CSTPIU_CFG_1_ITATBDATA0 Register

14.8.1.2.706.1 CSTPIU_CFG_1_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Integration Test ATB Data Register 0

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Table 14-15806. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4EECh

Figure 14-7777. CSTPIU_CFG_1_ITATBDATA0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>ATDATA_31</td><td>ATDATA_23</td><td>ATDATA_15</td><td>ATDATA_7</td><td>ATDATA_0</td></tr>
<tr><td colspan="3">R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15807. CSTPIU_CFG_1_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
32:5	RESERVED	R	0h	return 0
4	ATDATA_31	R	0h	Reads the value of atdatas[31]
3	ATDATA_23	R	0h	Reads the value of atdatas[23]
2	ATDATA_15	R	0h	Reads the value of atdatas[15]
1	ATDATA_7	R	0h	Reads the value of atdatas[7]
0	ATDATA_0	R	0h	Reads the value of atdatas[0]

14.8.1.2.707 CSTPIU_CFG_1_ITATBCTR2 Register

14.8.1.2.707.1 CSTPIU_CFG_1_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Integration Test ATB Control Register 2.

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Table 14-15808. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4EF0h

Figure 14-7778. CSTPIU_CFG_1_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						AFVALID	ATREADY
R						W	W
0h						0h	0h

Table 14-15809. CSTPIU_CFG_1_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	return 0
1	AFVALID	W	0h	Sets the value of afvalid
0	ATREADY	W	0h	Sets the value of atready

14.8.1.2.708 CSTPIU_CFG_1_ITATBCTR1 Register

14.8.1.2.708.1 CSTPIU_CFG_1_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Integration Test ATB Control Register 1.

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Table 14-15810. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4EF4h

Figure 14-7779. CSTPIU_CFG_1_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	ATID						
R	R						
0h	0h						

Table 14-15811. CSTPIU_CFG_1_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	returns 0
6:0	ATID	R	0h	Reads the value of atids

14.8.1.2.709 CSTPIU_CFG_1_ITATBCTR0 Register

14.8.1.2.709.1 CSTPIU_CFG_1_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Integration Test ATB Control Register 0.

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Table 14-15812. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4EF8h

Figure 14-7780. CSTPIU_CFG_1_ITATBCTR0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">ABYTES</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>AFREADY</td><td>ATVALID</td></tr>
<tr><td colspan="6">NONE</td><td>R</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-15813. CSTPIU_CFG_1_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	R	0h	Reads return 0 Reads return 0
9:8	ABYTES	R	0h	Reads the value of the atbytess
7:2	RESERVED	NONE	0h	Reserved
1	AFREADY	R	0h	Reads the value of afreadys
0	ATVALID	R	0h	Reads the value of atvalids

14.8.1.2.710 CSTPIU_CFG_1_INTCTRL Register

14.8.1.2.710.1 CSTPIU_CFG_1_INTCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Register

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Table 14-15814. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4F00h

Figure 14-7781. CSTPIU_CFG_1_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							IME
R							R/W
0h							0h

Table 14-15815. CSTPIU_CFG_1_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	IME	R/W	0h	Integration Mode Enable.

14.8.1.2.711 CSTPIU_CFG_1_CTSET Register

14.8.1.2.711.1 CSTPIU_CFG_1_CTSET Register (Offset = FA0h) [reset = Fh]

Claim Tag Set Register

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Table 14-15816. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FA0h

Figure 14-7782. CSTPIU_CFG_1_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				Fh			

Table 14-15817. CSTPIU_CFG_1_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	Fh	Claim Tag Set Register

14.8.1.2.712 CSTPIU_CFG_1_CTCLR Register

14.8.1.2.712.1 CSTPIU_CFG_1_CTCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-15818. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FA4h

Figure 14-7783. CSTPIU_CFG_1_CTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_CLEAR			
R				R/W			
0h				0h			

Table 14-15819. CSTPIU_CFG_1_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.8.1.2.713 CSTPIU_CFG_1_LAREG Register

14.8.1.2.713.1 CSTPIU_CFG_1_LAREG Register (Offset = FB0h) [reset = 0h]

Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-15820. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FB0h

Figure 14-7784. CSTPIU_CFG_1_LAREG Name Register

31	30	29	28	27	26	25	24
LOCK_ACCESS_REGISTER							
W							
0h							
23	22	21	20	19	18	17	16
LOCK_ACCESS_REGISTER							
W							
0h							
15	14	13	12	11	10	9	8
LOCK_ACCESS_REGISTER							
W							
0h							
7	6	5	4	3	2	1	0
LOCK_ACCESS_REGISTER							
W							
0h							

Table 14-15821. CSTPIU_CFG_1_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	W	0h	

14.8.1.2.714 CSTPIU_CFG_1_LSREG Register

14.8.1.2.714.1 CSTPIU_CFG_1_LSREG Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-15822. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FB4h

Figure 14-7785. CSTPIU_CFG_1_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					NTT	LOCK_STATUS	SLI
R					R	R	R
0h					0h	0h	0h

Table 14-15823. CSTPIU_CFG_1_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	Reserved, returns 0
2	NTT	R	0h	Register size Indicator. Always 0. Indiates that the LAR is implemented as 32-bit
1	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked. Application must write to the LAREG to gain access.
0	SLI	R	0h	Software Lock Implemented. Indicates that a lock control mechanism is present from this interface

14.8.1.2.715 CSTPIU_CFG_1_AUTHST Register

14.8.1.2.715.1 CSTPIU_CFG_1_AUTHST Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-15824. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FB8h

Figure 14-7786. CSTPIU_CFG_1_AUTHST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
SNID		SID		NSNID		NSID	
R		R		R		R	
0h		0h		0h		0h	

Table 14-15825. CSTPIU_CFG_1_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reads return 0
7:6	SNID	R	0h	Indicates the security level for Secure non-invasive debug
5:4	SID	R	0h	Indicates the security level for Secure invasive debug
3:2	NSNID	R	0h	Indicates the security level for Non-secure non-invasive debug.
1:0	NSID	R	0h	Indicates the security level for Non-secure invasive debug.

14.8.1.2.716 CSTPIU_CFG_1_DEVID Register

14.8.1.2.716.1 CSTPIU_CFG_1_DEVID Register (Offset = FC8h) [reset = A0h]

This shows the characteristics of the TPIU

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Table 14-15826. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FC8h

Figure 14-7787. CSTPIU_CFG_1_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				SWOUARTNRZ	SWOMAN	TCLKDATA	FIFO_SIZE
R				R	R	R	R
0h				0h	0h	0h	2h
7	6	5	4	3	2	1	0
FIFO_SIZE		CLKRELAT	MUXNUM				
R		R	R				
2h		1h	0h				

Table 14-15827. CSTPIU_CFG_1_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11	SWOUARTNRZ	R	0h	Indicates Serial Wire Output [UART/NRZ] is not supported. Defaul = 0
10	SWOMAN	R	0h	Indicates Serial Wire Output [Manchester] is not supported. Default = 0
9	TCLKDATA	R	0h	Indicates trace clock + data is supported.
8:6	FIFO_SIZE	R	2h	FIFO size in powers of 2. A value of 2 gives a FIFO size of 4 entries, 16 bytes. Default is3'b010
5	CLKRELAT	R	1h	Indicates the relationship between ATCLK and TRACECLKIN. 0x1 indicates asynchronous.
4:0	MUXNUM	R	0h	When nonzero this value indicates the type/number of ATB multiplexing present on the input to the ATB. Currently only 0x00 is supported, that is, no multiplexing present.

14.8.1.2.717 CSTPIU_CFG_1_DEVTYPE Register

14.8.1.2.717.1 CSTPIU_CFG_1_DEVTYPE Register (Offset = FCCh) [reset = 11h]

Device Type Identifier Register

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Table 14-15828. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FCCh

Figure 14-7788. CSTPIU_CFG_1_DEVTYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB				MAJOR			
R				R			
1h				1h			

Table 14-15829. CSTPIU_CFG_1_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:4	SUB	R	1h	Sub-classification of the type of the debug component as specified in the Arm Architecture Specification within the major classification as specified in the MAJOR field
3:0	MAJOR	R	1h	Major classification of the type of the debug component as specified in the Arm Architecture Specification for this debug and trace component

14.8.1.2.718 CSTPIU_CFG_1_PERID4 Register

14.8.1.2.718.1 CSTPIU_CFG_1_PERID4 Register (Offset = FD0h) [reset = 4h]

Peripheral ID4 Register

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Table 14-15830. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FD0h

Figure 14-7789. CSTPIU_CFG_1_PERID4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SIZE</td><td colspan="4">DES_2</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">4h</td></tr>
</table>

Table 14-15831. CSTPIU_CFG_1_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:4	SIZE	R	0h	Always 0b0000. Indicates that the device only occupies 4KB memory
3:0	DES_2	R	4h	PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES2 identify the designer of the component

14.8.1.2.719 CSTPIU_CFG_1_PERID0 Register

14.8.1.2.719.1 CSTPIU_CFG_1_PERID0 Register (Offset = FE0h) [reset = 12h]

Peripheral ID0 Register

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Table 14-15832. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FE0h

Figure 14-7790. CSTPIU_CFG_1_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PART_0							
R							
12h							

Table 14-15833. CSTPIU_CFG_1_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PART_0	R	12h	Perpiheral ID 0, returns the 12-bit part number of the component.

14.8.1.2.720 CSTPIU_CFG_1_PERID1 Register

14.8.1.2.720.1 CSTPIU_CFG_1_PERID1 Register (Offset = FE4h) [reset = B9h]

Peripheral ID1 Register

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Table 14-15834. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FE4h

Figure 14-7791. CSTPIU_CFG_1_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DES_0				PART_1			
R				R			
Bh				9h			

Table 14-15835. CSTPIU_CFG_1_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:4	DES_0	R	Bh	return 0xB. Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component
3:0	PART_1	R	9h	Peripheral ID 1, returns 0x9

14.8.1.2.721 CSTPIU_CFG_1_PERID2 Register

14.8.1.2.721.1 CSTPIU_CFG_1_PERID2 Register (Offset = FE8h) [reset = 5Bh]

Peripheral ID2 Register

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Table 14-15836. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FE8h

Figure 14-7792. CSTPIU_CFG_1_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVISION				JEDEC	DES_1		
R				R	R		
5h				1h	3h		

Table 14-15837. CSTPIU_CFG_1_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:4	REVISION	R	5h	always return 0x5
3	JEDEC	R	1h	always return 1. Indicates that the JEDEC-assigned designer ID is used
2:0	DES_1	R	3h	Return 0x3. Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component

14.8.1.2.722 CSTPIU_CFG_1_PERID3 Register

14.8.1.2.722.1 CSTPIU_CFG_1_PERID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

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Table 14-15838. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FECh

Figure 14-7793. CSTPIU_CFG_1_PERID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVAND				CMOD			
R				R			
0h				0h			

Table 14-15839. CSTPIU_CFG_1_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:4	REVAND	R	0h	return 0000. Indicates that there are no extra fixes to this component
3:0	CMOD	R	0h	Customer Modified. returns 0x00 to indicate that the customer has not modified this component.

14.8.1.2.723 CSTPIU_CFG_1_COMPID0 Register

14.8.1.2.723.1 CSTPIU_CFG_1_COMPID0 Register (Offset = FF0h) [reset = Dh]

Component ID0 Register

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Table 14-15840. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FF0h

Figure 14-7794. CSTPIU_CFG_1_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PRMBL_0							
R							
Dh							

Table 14-15841. CSTPIU_CFG_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	PRMBL_0	R	Dh	Preamble_0. return 0xD. Component ID register contains bits 7:0 of the component ID

14.8.1.2.724 CSTPIU_CFG_1_COMPID1 Register

14.8.1.2.724.1 CSTPIU_CFG_1_COMPID1 Register (Offset = FF4h) [reset = 90h]

Component ID1 Register

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Table 14-15842. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FF4h

Figure 14-7795. CSTPIU_CFG_1_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CLASS				PRMBL_1			
R				R			
9h				0h			

Table 14-15843. CSTPIU_CFG_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:4	CLASS	R	9h	Return 0x9. Class of the component. Contain bits [15:12] of the component ID.
3:0	PRMBL_1	R	0h	Component ID register contains bits16:8 of the component ID

14.8.1.2.725 CSTPIU_CFG_1_COMPID2 Register

14.8.1.2.725.1 CSTPIU_CFG_1_COMPID2 Register (Offset = FF8h) [reset = 5h]

Component ID2 Register

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Table 14-15844. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FF8h

Figure 14-7796. CSTPIU_CFG_1_COMPID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID2							
R							
5h							

Table 14-15845. CSTPIU_CFG_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	5h	A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

14.8.1.2.726 CSTPIU_CFG_1_COMPID3 Register

14.8.1.2.726.1 CSTPIU_CFG_1_COMPID3 Register (Offset = FFCh) [reset = B1h]

Component ID3 Register

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Table 14-15846. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 4FFCh

Figure 14-7797. CSTPIU_CFG_1_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
B1h							

Table 14-15847. CSTPIU_CFG_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	B1h	A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

14.8.1.2.727 CTF_CFG_1_CSTFCTLREG Register

14.8.1.2.727.1 CTF_CFG_1_CSTFCTLREG Register (Offset = 0h) [reset = 0h]

It enables the target ports and defines the hold time of the target ports.

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Table 14-15848. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5000h

Figure 14-7798. CTF_CFG_1_CSTFCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED				MINHOLDTIME			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
SLVPORTEN							
R/W							
0h							

Table 14-15849. CTF_CFG_1_CSTFCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	R	0h	Reserved, returns 0
11:8	MINHOLDTIME	R/W	0h	Minimum Hold time Hold time refers to the number of transactions that are output on the funnel initiator port from the same target while that target port ATVALIDSx is HIGH The CSTF holds for the minimum hold time and one additional cycle The maximum value that can be entered is 0xE and this equates to 15 cycles 0xF is reserved
7:0	SLVPORTEN	R/W	0h	Target Port Enables Setting these bits enables the corresponding input, or target port If a bit is not set then this has the effect of excluding that port from the priority selection scheme

14.8.1.2.728 CTF_CFG_1_PRIORCTLREG Register

14.8.1.2.728.1 CTF_CFG_1_PRIORCTLREG Register (Offset = 4h) [reset = 0h]

Defines the order in which inputs are selected. This register must only be altered when the trace sources are off and the system is drained.

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Table 14-15850. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5004h

Figure 14-7799. CTF_CFG_1_PRIORCTLREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
PRIPORT7			PRIPORT6			PRIPORT5	
R/W			R/W			R/W	
0h			0h			0h	
15	14	13	12	11	10	9	8
PRIPORT5	PRIPORT4			PRIPORT3			PRIPORT2
R/W	R/W			R/W			R/W
0h	0h			0h			0h
7	6	5	4	3	2	1	0
PRIPORT2		PRIPORT1			PRIPORT0		
R/W		R/W			R/W		
0h		0h			0h		

Table 14-15851. CTF_CFG_1_PRIORCTLREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	Reserved, returns 0
23:21	PRIPORT7	R/W	0h	Priority value of the eighth target port Highest priority goes to the lowest value
20:18	PRIPORT6	R/W	0h	Priority value of the seventh target port Highest priority goes to the lowest value
17:15	PRIPORT5	R/W	0h	Priority value of the sixth target port Highest priority goes to the lowest value
14:12	PRIPORT4	R/W	0h	Priority value of the fifth target port Highest priority goes to the lowest value
11:9	PRIPORT3	R/W	0h	Priority value of the fourth target port Highest priority goes to the lowest value
8:6	PRIPORT2	R/W	0h	Priority value of the third target port Highest priority goes to the lowest value
5:3	PRIPORT1	R/W	0h	Priority value of the second target port Highest priority goes to the lowest value
2:0	PRIPORT0	R/W	0h	Priority value of the first target port Highest priority goes to the lowest value

14.8.1.2.729 CTF_CFG_1_ITATBDATA0 Register

14.8.1.2.729.1 CTF_CFG_1_ITATBDATA0 Register (Offset = EECh) [reset = 0h]

Integration Test Register.

Return to Summary Table

Table 14-15852. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5EECh

Figure 14-7800. CTF_CFG_1_ITATBDATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			ATDATA31	ATDATA23	ATDATA15	ATDATA7	ATDATA0
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 14-15853. CTF_CFG_1_ITATBDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	R	0h	Reserved, returns 0
4	ATDATA31	R/W	0h	A write outputs data on ATDATAM[31] A read returns the value of ATDATAS[31]
3	ATDATA23	R/W	0h	A write outputs data on ATDATAM[23] A read returns the value of ATDATAS[23]
2	ATDATA15	R/W	0h	A write outputs data on ATDATAM[15] A read returns the value of ATDATAS[15]
1	ATDATA7	R/W	0h	A write outputs data on ATDATAM[7] A read returns the value of ATDATAS[7]
0	ATDATA0	R/W	0h	A write outputs data on ATDATAM[0] A read returns the value of ATDATAS[0]

14.8.1.2.730 CTF_CFG_1_ITATBCTR2 Register

14.8.1.2.730.1 CTF_CFG_1_ITATBCTR2 Register (Offset = EF0h) [reset = 0h]

Integration Test Control Register 2.

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Table 14-15854. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5EF0h

Figure 14-7801. CTF_CFG_1_ITATBCTR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED		AFVALID	ATREADY
R				NONE		R/W	R/W
0h				0h		0h	0h

Table 14-15855. CTF_CFG_1_ITATBCTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:2	RESERVED	NONE	0h	Reserved
1	AFVALID	R/W	0h	Reading this bit returns the value of AFVALIDM Writing this bit sets the AFVALIDS[n] bit where n is enabled by the CSTFCTLREG
0	ATREADY	R/W	0h	Reading this bit returns the value of ATREADYM Writing this bit sets the AFREADYS[n] bit where n is enabled by the CSTFCTLREG

14.8.1.2.731 CTF_CFG_1_ITATBCTR1 Register

14.8.1.2.731.1 CTF_CFG_1_ITATBCTR1 Register (Offset = EF4h) [reset = 0h]

Integration Test Control Register 1.

Return to Summary Table

Table 14-15856. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5EF4h

Figure 14-7802. CTF_CFG_1_ITATBCTR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RESERVED	ATID					
R	NONE	R/W					
0h	0h	0h					

Table 14-15857. CTF_CFG_1_ITATBCTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	Reserved, returns 0
6	RESERVED	NONE	0h	Reserved
5:0	ATID	R/W	0h	Writing this register sets the value of ATIDM Reading it returns the value of ATIDS

14.8.1.2.732 CTF_CFG_1_ITATBCTR0 Register

14.8.1.2.732.1 CTF_CFG_1_ITATBCTR0 Register (Offset = EF8h) [reset = 0h]

Integration Test Control Register 0.

Return to Summary Table

Table 14-15858. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5EF8h

Figure 14-7803. CTF_CFG_1_ITATBCTR0 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1						ATBYTES	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED						AFREADY	ATVALID
R						R/W	R/W
0h						0h	0h

Table 14-15859. CTF_CFG_1_ITATBCTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED1	R	0h	Reserved, returns 0
9:8	ATBYTES	R/W	0h	Writing this field sets the value of ATBYTESM Reading it returns the value of ATBYTSS[n]
7:2	RESERVED	R	0h	Reserved, returns 0
1	AFREADY	R/W	0h	Writing this field sets the value of AFREADYM Reading it returns the value of AFREADYS[n]
0	ATVALID	R/W	0h	Writing this field sets the value of ATVALIDM Reading it returns the value of ATVALIDS[n]

14.8.1.2.733 CTF_CFG_1_INTCTRL Register

14.8.1.2.733.1 CTF_CFG_1_INTCTRL Register (Offset = F00h) [reset = 0h]

Integration Mode Register

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Table 14-15860. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5F00h

Figure 14-7804. CTF_CFG_1_INTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							INTEGMODEN
R							R/W
0h							0h

Table 14-15861. CTF_CFG_1_INTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Reserved, returns 0
0	INTEGMODEN	R/W	0h	Integration Mode Enable

14.8.1.2.734 CTF_CFG_1_CTSET Register

14.8.1.2.734.1 CTF_CFG_1_CTSET Register (Offset = FA0h) [reset = 0h]

Claim Tag Set Register

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Table 14-15862. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FA0h

Figure 14-7805. CTF_CFG_1_CTSET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				CLAIM_TAG_SET			
R				R/W			
0h				0h			

Table 14-15863. CTF_CFG_1_CTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_SET	R/W	0h	Claim Tag Set Register

14.8.1.2.735 CTF_CFG_1_CTCLR Register

14.8.1.2.735.1 CTF_CFG_1_CTCLR Register (Offset = FA4h) [reset = 0h]

Claim Tag Clear Register

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Table 14-15864. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FA4h

Figure 14-7806. CTF_CFG_1_CTCLR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CLAIM_TAG_CLEAR</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15865. CTF_CFG_1_CTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	CLAIM_TAG_CLEAR	R/W	0h	Claim Tag Clear Register

14.8.1.2.736 CTF_CFG_1_LAREG Register

14.8.1.2.736.1 CTF_CFG_1_LAREG Register (Offset = FB0h) [reset = 0h]

Software must write 0xCSACCE55 to this register in order for application to gain access to the other registers. If paddrdbg31 is high, this is ignored.

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Table 14-15866. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FB0h

Figure 14-7807. CTF_CFG_1_LAREG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">LOCK_ACCESS_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">LOCK_ACCESS_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">LOCK_ACCESS_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">LOCK_ACCESS_REGISTER</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15867. CTF_CFG_1_LAREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK_ACCESS_REGISTER	R/W	0h	

14.8.1.2.737 CTF_CFG_1_LSREG Register

14.8.1.2.737.1 CTF_CFG_1_LSREG Register (Offset = FB4h) [reset = 0h]

The CTI implements two memory maps controlled through PADDRDBG31. When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists. When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset. This indicates a 32-bit lock access mechanism is present and is locked

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Table 14-15868. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FB4h

Figure 14-7808. CTF_CFG_1_LSREG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						LOCK_STATUS	
R						R	
0h						0h	

Table 14-15869. CTF_CFG_1_LSREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Reserved, returns 0
1:0	LOCK_STATUS	R	0h	The CTI implements two memory maps controlled through PADDRDBG31 When PADDRDBG31 is HIGH, the Lock Status Register reads as 0x0 indicating that no lock exists When PADDRDBG31 is LOW, the Lock Status Register reads as 0x3 from reset This indicates a 32-bit lock access mechanism is present and is locked Application must write to the LAREG to gain access

14.8.1.2.738 CTF_CFG_1_AUTHST Register

14.8.1.2.738.1 CTF_CFG_1_AUTHST Register (Offset = FB8h) [reset = 0h]

Reports the required security level.

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Table 14-15870. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FB8h

Figure 14-7809. CTF_CFG_1_AUTHST Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">AUTHENTICATION_STATUS</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-15871. CTF_CFG_1_AUTHST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	R	0h	Reserved, returns 0
3:0	AUTHENTICATION_STATUS	R	0h	Reports the required security level bit 0 indicates Invasive Debug Controlled and bit 1 is the current value Bit 2 indicates non-invasive debug controlled and bit 3 is the current value Returns 0x5

14.8.1.2.739 CTF_CFG_1_DEVID Register

14.8.1.2.739.1 CTF_CFG_1_DEVID Register (Offset = FC8h) [reset = 0h]

Device ID Register

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Table 14-15872. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FC8h

Figure 14-7810. CTF_CFG_1_DEVID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PRIOTITY_SCHEME				PORTCOUNT			
R				R			
0h				0h			

Table 14-15873. CTF_CFG_1_DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, return 0s
7:4	PRIOTITY_SCHEME	R	0h	The CSTF implements a static priority scheme Value = 0x2
3:0	PORTCOUNT	R	0h	This is the value of the Verilog define PORTCOUNT and represents the number of input ports connected By default all 8 ports are connected 0x0 and 0x1 are illegal values

14.8.1.2.740 CTF_CFG_1_DEVTYPEID Register

14.8.1.2.740.1 CTF_CFG_1_DEVTYPEID Register (Offset = FCCh) [reset = 0h]

Device Type Identifier Register

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Table 14-15874. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FCCh

Figure 14-7811. CTF_CFG_1_DEVTYPEID Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
DEV_TYPE_ID							
R							
0h							

Table 14-15875. CTF_CFG_1_DEVTYPEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserveed, returns 0
7:0	DEV_TYPE_ID	R	0h	A value of 0x12 identifies this device as a trace link [0x2] and specifically as a funnel/router [0x1]

14.8.1.2.741 CTF_CFG_1_PERID4 Register

14.8.1.2.741.1 CTF_CFG_1_PERID4 Register (Offset = FD0h) [reset = 0h]

Peripheral ID4 Register

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Table 14-15876. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FD0h

Figure 14-7812. CTF_CFG_1_PERID4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID4							
R							
0h							

Table 14-15877. CTF_CFG_1_PERID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID4	R	0h	Peripheral ID 4, returns 0x4

14.8.1.2.742 CTF_CFG_1_PERID5 Register

14.8.1.2.742.1 CTF_CFG_1_PERID5 Register (Offset = FD4h) [reset = 0h]

Peripheral ID5 Register

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Table 14-15878. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FD4h

Figure 14-7813. CTF_CFG_1_PERID5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID5							
R							
0h							

Table 14-15879. CTF_CFG_1_PERID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID5	R	0h	Peripheral ID 5, returns 0x0

14.8.1.2.743 CTF_CFG_1_PERID6 Register

14.8.1.2.743.1 CTF_CFG_1_PERID6 Register (Offset = FD8h) [reset = 0h]

Peripheral ID6 Register

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Table 14-15880. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FD8h

Figure 14-7814. CTF_CFG_1_PERID6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID6							
R							
0h							

Table 14-15881. CTF_CFG_1_PERID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID6	R	0h	Peripheral ID 6, returns 0x0

14.8.1.2.744 CTF_CFG_1_PERID7 Register

14.8.1.2.744.1 CTF_CFG_1_PERID7 Register (Offset = FDCh) [reset = 0h]

Peripheral ID7 Register

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Table 14-15882. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FDCh

Figure 14-7815. CTF_CFG_1_PERID7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID7							
R							
0h							

Table 14-15883. CTF_CFG_1_PERID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID7	R	0h	Peripheral ID 7, returns 0x0

14.8.1.2.745 CTF_CFG_1_PERID0 Register

14.8.1.2.745.1 CTF_CFG_1_PERID0 Register (Offset = FE0h) [reset = 0h]

Peripheral ID0 Register

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Table 14-15884. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FE0h

Figure 14-7816. CTF_CFG_1_PERID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID0							
R							
0h							

Table 14-15885. CTF_CFG_1_PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID0	R	0h	Perpiheral ID 0, returns 0x06

14.8.1.2.746 CTF_CFG_1_PERID1 Register

14.8.1.2.746.1 CTF_CFG_1_PERID1 Register (Offset = FE4h) [reset = 0h]

Peripheral ID1 Register

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Table 14-15886. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FE4h

Figure 14-7817. CTF_CFG_1_PERID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERIPH_ID1							
R							
0h							

Table 14-15887. CTF_CFG_1_PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID1	R	0h	Peripheral ID 1, returns 0xB9

14.8.1.2.747 CTF_CFG_1_PERID2 Register

14.8.1.2.747.1 CTF_CFG_1_PERID2 Register (Offset = FE8h) [reset = 0h]

Peripheral ID2 Register

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Table 14-15888. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FE8h

Figure 14-7818. CTF_CFG_1_PERID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
PERIPH_ID2							
R							
0h							

Table 14-15889. CTF_CFG_1_PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERIPH_ID2	R	0h	Peripheral ID 2, returns 9x2B

14.8.1.2.748 CTF_CFG_1_PERID3 Register

14.8.1.2.748.1 CTF_CFG_1_PERID3 Register (Offset = FECh) [reset = 0h]

Peripheral ID3 Register

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Table 14-15890. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FECh

Figure 14-7819. CTF_CFG_1_PERID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERPIH_ID3							
R							
0h							

Table 14-15891. CTF_CFG_1_PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Reserved, returns 0
7:0	PERPIH_ID3	R	0h	Peripheral ID3 register, returns 0x00

14.8.1.2.749 CTF_CFG_1_COMPID0 Register

14.8.1.2.749.1 CTF_CFG_1_COMPID0 Register (Offset = FF0h) [reset = 0h]

Component ID0 Register

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Table 14-15892. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FF0h

Figure 14-7820. CTF_CFG_1_COMPID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID0							
R							
0h							

Table 14-15893. CTF_CFG_1_COMPID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID0	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.750 CTF_CFG_1_COMPID1 Register

14.8.1.2.750.1 CTF_CFG_1_COMPID1 Register (Offset = FF4h) [reset = 0h]

Component ID1 Register

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Table 14-15894. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FF4h

Figure 14-7821. CTF_CFG_1_COMPID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID1							
R							
0h							

Table 14-15895. CTF_CFG_1_COMPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Read returns 0
7:0	COMP_ID1	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.751 CTF_CFG_1_COMPID2 Register

14.8.1.2.751.1 CTF_CFG_1_COMPID2 Register (Offset = FF8h) [reset = 0h]

Component ID2 Register

Return to Summary Table

Table 14-15896. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FF8h

Figure 14-7822. CTF_CFG_1_COMPID2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COMP_ID2</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15897. CTF_CFG_1_COMPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	Returns 0
7:0	COMP_ID2	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.1.2.752 CTF_CFG_1_COMPID3 Register

14.8.1.2.752.1 CTF_CFG_1_COMPID3 Register (Offset = FFCh) [reset = 0h]

Component ID3 Register

Return to Summary Table

Table 14-15898. Instance Table

Instance Name	Physical Address
DEBUGSS_WRAP0	0007 6000 5FFCh

Figure 14-7823. CTF_CFG_1_COMPID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
COMP_ID3							
R							
0h							

Table 14-15899. CTF_CFG_1_COMPID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	returns 0 when read
7:0	COMP_ID3	R	0h	A component identification register, that indicates that the identification registers are present This register also indicates the component class

14.8.2 PBIST

PBIST

14.8.2.1 PBIST Summaries

PBIST Summaries

Table 14-15900. PBIST Registers, Base Address=0039 0000h, Length=1024

Offset	Length	Register Name	PBIST0 Physical Address	PBIST1 Physical Address	PBIST2 Physical Address
0h	32	PBIST_RF0L	0039 0000h	003A 0000h	003B 0000h
4h	32	PBIST_RF1L	0039 0004h	003A 0004h	003B 0004h
8h	32	PBIST_RF2L	0039 0008h	003A 0008h	003B 0008h
Ch	32	PBIST_RF3L	0039 000Ch	003A 000Ch	003B 000Ch
10h	32	PBIST_RF4L	0039 0010h	003A 0010h	003B 0010h
14h	32	PBIST_RF5L	0039 0014h	003A 0014h	003B 0014h
18h	32	PBIST_RF6L	0039 0018h	003A 0018h	003B 0018h
1Ch	32	PBIST_RF7L	0039 001Ch	003A 001Ch	003B 001Ch
20h	32	PBIST_RF8L	0039 0020h	003A 0020h	003B 0020h
24h	32	PBIST_RF9L	0039 0024h	003A 0024h	003B 0024h
28h	32	PBIST_RF10L	0039 0028h	003A 0028h	003B 0028h
2Ch	32	PBIST_RF11L	0039 002Ch	003A 002Ch	003B 002Ch
30h	32	PBIST_RF12L	0039 0030h	003A 0030h	003B 0030h
34h	32	PBIST_RF13L	0039 0034h	003A 0034h	003B 0034h
38h	32	PBIST_RF14L	0039 0038h	003A 0038h	003B 0038h
3Ch	32	PBIST_RF15L	0039 003Ch	003A 003Ch	003B 003Ch
40h	32	PBIST_RF0U	0039 0040h	003A 0040h	003B 0040h
44h	32	PBIST_RF1U	0039 0044h	003A 0044h	003B 0044h
48h	32	PBIST_RF2U	0039 0048h	003A 0048h	003B 0048h
4Ch	32	PBIST_RF3U	0039 004Ch	003A 004Ch	003B 004Ch
50h	32	PBIST_RF4U	0039 0050h	003A 0050h	003B 0050h
54h	32	PBIST_RF5U	0039 0054h	003A 0054h	003B 0054h
58h	32	PBIST_RF6U	0039 0058h	003A 0058h	003B 0058h
5Ch	32	PBIST_RF7U	0039 005Ch	003A 005Ch	003B 005Ch
60h	32	PBIST_RF8U	0039 0060h	003A 0060h	003B 0060h
64h	32	PBIST_RF9U	0039 0064h	003A 0064h	003B 0064h
68h	32	PBIST_RF10U	0039 0068h	003A 0068h	003B 0068h
6Ch	32	PBIST_RF11U	0039 006Ch	003A 006Ch	003B 006Ch
70h	32	PBIST_RF12U	0039 0070h	003A 0070h	003B 0070h
74h	32	PBIST_RF13U	0039 0074h	003A 0074h	003B 0074h
78h	32	PBIST_RF14U	0039 0078h	003A 0078h	003B 0078h
7Ch	32	PBIST_RF15U	0039 007Ch	003A 007Ch	003B 007Ch
100h	32	PBIST_A0	0039 0100h	003A 0100h	003B 0100h
104h	32	PBIST_A1	0039 0104h	003A 0104h	003B 0104h
108h	32	PBIST_A2	0039 0108h	003A 0108h	003B 0108h
10Ch	32	PBIST_A3	0039 010Ch	003A 010Ch	003B 010Ch
110h	32	PBIST_L0	0039 0110h	003A 0110h	003B 0110h
114h	32	PBIST_L1	0039 0114h	003A 0114h	003B 0114h
118h	32	PBIST_L2	0039 0118h	003A 0118h	003B 0118h

Table 14-15900. PBIST Registers, Base Address=0039 0000h, Length=1024 (continued)

Offset	Length	Register Name	PBIST0 Physical Address	PBIST1 Physical Address	PBIST2 Physical Address
11Ch	32	PBIST_L3	0039 011Ch	003A 011Ch	003B 011Ch
120h	32	PBIST_D	0039 0120h	003A 0120h	003B 0120h
124h	32	PBIST_E	0039 0124h	003A 0124h	003B 0124h
130h	32	PBIST_CA0	0039 0130h	003A 0130h	003B 0130h
134h	32	PBIST_CA1	0039 0134h	003A 0134h	003B 0134h
138h	32	PBIST_CA2	0039 0138h	003A 0138h	003B 0138h
13Ch	32	PBIST_CA3	0039 013Ch	003A 013Ch	003B 013Ch
140h	32	PBIST_CL0	0039 0140h	003A 0140h	003B 0140h
144h	32	PBIST_CL1	0039 0144h	003A 0144h	003B 0144h
148h	32	PBIST_CL2	0039 0148h	003A 0148h	003B 0148h
14Ch	32	PBIST_CL3	0039 014Ch	003A 014Ch	003B 014Ch
150h	32	PBIST_I0	0039 0150h	003A 0150h	003B 0150h
154h	32	PBIST_I1	0039 0154h	003A 0154h	003B 0154h
158h	32	PBIST_I2	0039 0158h	003A 0158h	003B 0158h
15Ch	32	PBIST_I3	0039 015Ch	003A 015Ch	003B 015Ch
160h	32	PBIST_RAMT	0039 0160h	003A 0160h	003B 0160h
164h	32	PBIST_DLR	0039 0164h	003A 0164h	003B 0164h
168h	32	PBIST_CMS	0039 0168h	003A 0168h	003B 0168h
16Ch	32	PBIST_STR	0039 016Ch	003A 016Ch	003B 016Ch
170h	64	PBIST_SCR	0039 0170h	003A 0170h	003B 0170h
178h	32	PBIST_CSR	0039 0178h	003A 0178h	003B 0178h
17Ch	32	PBIST_FDLY	0039 017Ch	003A 017Ch	003B 017Ch
180h	32	PBIST_PACT	0039 0180h	003A 0180h	003B 0180h
184h	32	PBIST_PID	0039 0184h	003A 0184h	003B 0184h
188h	32	PBIST_OVER	0039 0188h	003A 0188h	003B 0188h
190h	64	PBIST_FSRF	0039 0190h	003A 0190h	003B 0190h
198h	64	PBIST_FSRC	0039 0198h	003A 0198h	003B 0198h
1A0h	64	PBIST_FSRA	0039 01A0h	003A 01A0h	003B 01A0h
1A8h	32	PBIST_FSRDL0	0039 01A8h	003A 01A8h	003B 01A8h
1B0h	32	PBIST_FSRDL1	0039 01B0h	003A 01B0h	003B 01B0h
1B4h	32	PBIST_MARGIN_MODE	0039 01B4h	003A 01B4h	003B 01B4h
1B8h	32	PBIST_WRENZ	0039 01B8h	003A 01B8h	003B 01B8h
1BCh	32	PBIST_PAGE_PGS	0039 01BCh	003A 01BCh	003B 01BCh
1C0h	32	PBIST_ROM	0039 01C0h	003A 01C0h	003B 01C0h
1C4h	32	PBIST_ALGO	0039 01C4h	003A 01C4h	003B 01C4h
1C8h	64	PBIST_RINFO	0039 01C8h	003A 01C8h	003B 01C8h

Table 14-15901. PBIST Registers, Base Address=0039 0000h, Length=1024

Offset	Length	Register Name	PBIST3 Physical Address	PBIST4 Physical Address	PBIST5 Physical Address
0h	32	PBIST_RF0L	003C 0000h	003D 0000h	003E 0000h
4h	32	PBIST_RF1L	003C 0004h	003D 0004h	003E 0004h
8h	32	PBIST_RF2L	003C 0008h	003D 0008h	003E 0008h
Ch	32	PBIST_RF3L	003C 000Ch	003D 000Ch	003E 000Ch
10h	32	PBIST_RF4L	003C 0010h	003D 0010h	003E 0010h
14h	32	PBIST_RF5L	003C 0014h	003D 0014h	003E 0014h

Table 14-15901. PBIST Registers, Base Address=0039 0000h, Length=1024 (continued)

Offset	Length	Register Name	PBIST3 Physical Address	PBIST4 Physical Address	PBIST5 Physical Address
18h	32	PBIST_RF6L	003C 0018h	003D 0018h	003E 0018h
1Ch	32	PBIST_RF7L	003C 001Ch	003D 001Ch	003E 001Ch
20h	32	PBIST_RF8L	003C 0020h	003D 0020h	003E 0020h
24h	32	PBIST_RF9L	003C 0024h	003D 0024h	003E 0024h
28h	32	PBIST_RF10L	003C 0028h	003D 0028h	003E 0028h
2Ch	32	PBIST_RF11L	003C 002Ch	003D 002Ch	003E 002Ch
30h	32	PBIST_RF12L	003C 0030h	003D 0030h	003E 0030h
34h	32	PBIST_RF13L	003C 0034h	003D 0034h	003E 0034h
38h	32	PBIST_RF14L	003C 0038h	003D 0038h	003E 0038h
3Ch	32	PBIST_RF15L	003C 003Ch	003D 003Ch	003E 003Ch
40h	32	PBIST_RF0U	003C 0040h	003D 0040h	003E 0040h
44h	32	PBIST_RF1U	003C 0044h	003D 0044h	003E 0044h
48h	32	PBIST_RF2U	003C 0048h	003D 0048h	003E 0048h
4Ch	32	PBIST_RF3U	003C 004Ch	003D 004Ch	003E 004Ch
50h	32	PBIST_RF4U	003C 0050h	003D 0050h	003E 0050h
54h	32	PBIST_RF5U	003C 0054h	003D 0054h	003E 0054h
58h	32	PBIST_RF6U	003C 0058h	003D 0058h	003E 0058h
5Ch	32	PBIST_RF7U	003C 005Ch	003D 005Ch	003E 005Ch
60h	32	PBIST_RF8U	003C 0060h	003D 0060h	003E 0060h
64h	32	PBIST_RF9U	003C 0064h	003D 0064h	003E 0064h
68h	32	PBIST_RF10U	003C 0068h	003D 0068h	003E 0068h
6Ch	32	PBIST_RF11U	003C 006Ch	003D 006Ch	003E 006Ch
70h	32	PBIST_RF12U	003C 0070h	003D 0070h	003E 0070h
74h	32	PBIST_RF13U	003C 0074h	003D 0074h	003E 0074h
78h	32	PBIST_RF14U	003C 0078h	003D 0078h	003E 0078h
7Ch	32	PBIST_RF15U	003C 007Ch	003D 007Ch	003E 007Ch
100h	32	PBIST_A0	003C 0100h	003D 0100h	003E 0100h
104h	32	PBIST_A1	003C 0104h	003D 0104h	003E 0104h
108h	32	PBIST_A2	003C 0108h	003D 0108h	003E 0108h
10Ch	32	PBIST_A3	003C 010Ch	003D 010Ch	003E 010Ch
110h	32	PBIST_L0	003C 0110h	003D 0110h	003E 0110h
114h	32	PBIST_L1	003C 0114h	003D 0114h	003E 0114h
118h	32	PBIST_L2	003C 0118h	003D 0118h	003E 0118h
11Ch	32	PBIST_L3	003C 011Ch	003D 011Ch	003E 011Ch
120h	32	PBIST_D	003C 0120h	003D 0120h	003E 0120h
124h	32	PBIST_E	003C 0124h	003D 0124h	003E 0124h
130h	32	PBIST_CA0	003C 0130h	003D 0130h	003E 0130h
134h	32	PBIST_CA1	003C 0134h	003D 0134h	003E 0134h
138h	32	PBIST_CA2	003C 0138h	003D 0138h	003E 0138h
13Ch	32	PBIST_CA3	003C 013Ch	003D 013Ch	003E 013Ch
140h	32	PBIST_CL0	003C 0140h	003D 0140h	003E 0140h
144h	32	PBIST_CL1	003C 0144h	003D 0144h	003E 0144h
148h	32	PBIST_CL2	003C 0148h	003D 0148h	003E 0148h
14Ch	32	PBIST_CL3	003C 014Ch	003D 014Ch	003E 014Ch
150h	32	PBIST_I0	003C 0150h	003D 0150h	003E 0150h
154h	32	PBIST_I1	003C 0154h	003D 0154h	003E 0154h

Table 14-15901. PBIST Registers, Base Address=0039 0000h, Length=1024 (continued)

Offset	Length	Register Name	PBIST3 Physical Address	PBIST4 Physical Address	PBIST5 Physical Address
158h	32	PBIST_I2	003C 0158h	003D 0158h	003E 0158h
15Ch	32	PBIST_I3	003C 015Ch	003D 015Ch	003E 015Ch
160h	32	PBIST_RAMT	003C 0160h	003D 0160h	003E 0160h
164h	32	PBIST_DLR	003C 0164h	003D 0164h	003E 0164h
168h	32	PBIST_CMS	003C 0168h	003D 0168h	003E 0168h
16Ch	32	PBIST_STR	003C 016Ch	003D 016Ch	003E 016Ch
170h	64	PBIST_SCR	003C 0170h	003D 0170h	003E 0170h
178h	32	PBIST_CSR	003C 0178h	003D 0178h	003E 0178h
17Ch	32	PBIST_FDLY	003C 017Ch	003D 017Ch	003E 017Ch
180h	32	PBIST_PACT	003C 0180h	003D 0180h	003E 0180h
184h	32	PBIST_PID	003C 0184h	003D 0184h	003E 0184h
188h	32	PBIST_OVER	003C 0188h	003D 0188h	003E 0188h
190h	64	PBIST_FSRF	003C 0190h	003D 0190h	003E 0190h
198h	64	PBIST_FSRC	003C 0198h	003D 0198h	003E 0198h
1A0h	64	PBIST_FSRA	003C 01A0h	003D 01A0h	003E 01A0h
1A8h	32	PBIST_FSRDL0	003C 01A8h	003D 01A8h	003E 01A8h
1B0h	32	PBIST_FSRDL1	003C 01B0h	003D 01B0h	003E 01B0h
1B4h	32	PBIST_MARGIN_MODE	003C 01B4h	003D 01B4h	003E 01B4h
1B8h	32	PBIST_WRENZ	003C 01B8h	003D 01B8h	003E 01B8h
1BCh	32	PBIST_PAGE_PGS	003C 01BCh	003D 01BCh	003E 01BCh
1C0h	32	PBIST_ROM	003C 01C0h	003D 01C0h	003E 01C0h
1C4h	32	PBIST_ALGO	003C 01C4h	003D 01C4h	003E 01C4h
1C8h	64	PBIST_RINFO	003C 01C8h	003D 01C8h	003E 01C8h

Table 14-15902. PBIST Registers, Base Address=0039 0000h, Length=1024

Offset	Length	Register Name	PBIST6 Physical Address	PBIST7 Physical Address	PBIST8 Physical Address
0h	32	PBIST_RF0L	003F 0000h	0034 0000h	0035 0000h
4h	32	PBIST_RF1L	003F 0004h	0034 0004h	0035 0004h
8h	32	PBIST_RF2L	003F 0008h	0034 0008h	0035 0008h
Ch	32	PBIST_RF3L	003F 000Ch	0034 000Ch	0035 000Ch
10h	32	PBIST_RF4L	003F 0010h	0034 0010h	0035 0010h
14h	32	PBIST_RF5L	003F 0014h	0034 0014h	0035 0014h
18h	32	PBIST_RF6L	003F 0018h	0034 0018h	0035 0018h
1Ch	32	PBIST_RF7L	003F 001Ch	0034 001Ch	0035 001Ch
20h	32	PBIST_RF8L	003F 0020h	0034 0020h	0035 0020h
24h	32	PBIST_RF9L	003F 0024h	0034 0024h	0035 0024h
28h	32	PBIST_RF10L	003F 0028h	0034 0028h	0035 0028h
2Ch	32	PBIST_RF11L	003F 002Ch	0034 002Ch	0035 002Ch
30h	32	PBIST_RF12L	003F 0030h	0034 0030h	0035 0030h
34h	32	PBIST_RF13L	003F 0034h	0034 0034h	0035 0034h
38h	32	PBIST_RF14L	003F 0038h	0034 0038h	0035 0038h
3Ch	32	PBIST_RF15L	003F 003Ch	0034 003Ch	0035 003Ch
40h	32	PBIST_RF0U	003F 0040h	0034 0040h	0035 0040h
44h	32	PBIST_RF1U	003F 0044h	0034 0044h	0035 0044h
48h	32	PBIST_RF2U	003F 0048h	0034 0048h	0035 0048h

Table 14-15902. PBIST Registers, Base Address=0039 0000h, Length=1024 (continued)

Offset	Length	Register Name	PBIST6 Physical Address	PBIST7 Physical Address	PBIST8 Physical Address
4Ch	32	PBIST_RF3U	003F 004Ch	0034 004Ch	0035 004Ch
50h	32	PBIST_RF4U	003F 0050h	0034 0050h	0035 0050h
54h	32	PBIST_RF5U	003F 0054h	0034 0054h	0035 0054h
58h	32	PBIST_RF6U	003F 0058h	0034 0058h	0035 0058h
5Ch	32	PBIST_RF7U	003F 005Ch	0034 005Ch	0035 005Ch
60h	32	PBIST_RF8U	003F 0060h	0034 0060h	0035 0060h
64h	32	PBIST_RF9U	003F 0064h	0034 0064h	0035 0064h
68h	32	PBIST_RF10U	003F 0068h	0034 0068h	0035 0068h
6Ch	32	PBIST_RF11U	003F 006Ch	0034 006Ch	0035 006Ch
70h	32	PBIST_RF12U	003F 0070h	0034 0070h	0035 0070h
74h	32	PBIST_RF13U	003F 0074h	0034 0074h	0035 0074h
78h	32	PBIST_RF14U	003F 0078h	0034 0078h	0035 0078h
7Ch	32	PBIST_RF15U	003F 007Ch	0034 007Ch	0035 007Ch
100h	32	PBIST_A0	003F 0100h	0034 0100h	0035 0100h
104h	32	PBIST_A1	003F 0104h	0034 0104h	0035 0104h
108h	32	PBIST_A2	003F 0108h	0034 0108h	0035 0108h
10Ch	32	PBIST_A3	003F 010Ch	0034 010Ch	0035 010Ch
110h	32	PBIST_L0	003F 0110h	0034 0110h	0035 0110h
114h	32	PBIST_L1	003F 0114h	0034 0114h	0035 0114h
118h	32	PBIST_L2	003F 0118h	0034 0118h	0035 0118h
11Ch	32	PBIST_L3	003F 011Ch	0034 011Ch	0035 011Ch
120h	32	PBIST_D	003F 0120h	0034 0120h	0035 0120h
124h	32	PBIST_E	003F 0124h	0034 0124h	0035 0124h
130h	32	PBIST_CA0	003F 0130h	0034 0130h	0035 0130h
134h	32	PBIST_CA1	003F 0134h	0034 0134h	0035 0134h
138h	32	PBIST_CA2	003F 0138h	0034 0138h	0035 0138h
13Ch	32	PBIST_CA3	003F 013Ch	0034 013Ch	0035 013Ch
140h	32	PBIST_CL0	003F 0140h	0034 0140h	0035 0140h
144h	32	PBIST_CL1	003F 0144h	0034 0144h	0035 0144h
148h	32	PBIST_CL2	003F 0148h	0034 0148h	0035 0148h
14Ch	32	PBIST_CL3	003F 014Ch	0034 014Ch	0035 014Ch
150h	32	PBIST_I0	003F 0150h	0034 0150h	0035 0150h
154h	32	PBIST_I1	003F 0154h	0034 0154h	0035 0154h
158h	32	PBIST_I2	003F 0158h	0034 0158h	0035 0158h
15Ch	32	PBIST_I3	003F 015Ch	0034 015Ch	0035 015Ch
160h	32	PBIST_RAMT	003F 0160h	0034 0160h	0035 0160h
164h	32	PBIST_DLR	003F 0164h	0034 0164h	0035 0164h
168h	32	PBIST_CMS	003F 0168h	0034 0168h	0035 0168h
16Ch	32	PBIST_STR	003F 016Ch	0034 016Ch	0035 016Ch
170h	64	PBIST_SCR	003F 0170h	0034 0170h	0035 0170h
178h	32	PBIST_CSR	003F 0178h	0034 0178h	0035 0178h
17Ch	32	PBIST_FDLY	003F 017Ch	0034 017Ch	0035 017Ch
180h	32	PBIST_PACT	003F 0180h	0034 0180h	0035 0180h
184h	32	PBIST_PID	003F 0184h	0034 0184h	0035 0184h
188h	32	PBIST_OVER	003F 0188h	0034 0188h	0035 0188h
190h	64	PBIST_FSRF	003F 0190h	0034 0190h	0035 0190h

Table 14-15902. PBIST Registers, Base Address=0039 0000h, Length=1024 (continued)

Offset	Length	Register Name	PBIST6 Physical Address	PBIST7 Physical Address	PBIST8 Physical Address
198h	64	PBIST_FSRC	003F 0198h	0034 0198h	0035 0198h
1A0h	64	PBIST_FSRA	003F 01A0h	0034 01A0h	0035 01A0h
1A8h	32	PBIST_FSRDL0	003F 01A8h	0034 01A8h	0035 01A8h
1B0h	32	PBIST_FSRDL1	003F 01B0h	0034 01B0h	0035 01B0h
1B4h	32	PBIST_MARGIN_MODE	003F 01B4h	0034 01B4h	0035 01B4h
1B8h	32	PBIST_WRENZ	003F 01B8h	0034 01B8h	0035 01B8h
1BCh	32	PBIST_PAGE_PGS	003F 01BCh	0034 01BCh	0035 01BCh
1C0h	32	PBIST_ROM	003F 01C0h	0034 01C0h	0035 01C0h
1C4h	32	PBIST_ALGO	003F 01C4h	0034 01C4h	0035 01C4h
1C8h	64	PBIST_RINFO	003F 01C8h	0034 01C8h	0035 01C8h

Table 14-15903. PBIST Registers, Base Address=0039 0000h, Length=1024

Offset	Length	Register Name	WKUP_PBIST1 Physical Address	WKUP_PBIST0 Physical Address
0h	32	PBIST_RF0L	2B50 0000h	2B50 1000h
4h	32	PBIST_RF1L	2B50 0004h	2B50 1004h
8h	32	PBIST_RF2L	2B50 0008h	2B50 1008h
Ch	32	PBIST_RF3L	2B50 000Ch	2B50 100Ch
10h	32	PBIST_RF4L	2B50 0010h	2B50 1010h
14h	32	PBIST_RF5L	2B50 0014h	2B50 1014h
18h	32	PBIST_RF6L	2B50 0018h	2B50 1018h
1Ch	32	PBIST_RF7L	2B50 001Ch	2B50 101Ch
20h	32	PBIST_RF8L	2B50 0020h	2B50 1020h
24h	32	PBIST_RF9L	2B50 0024h	2B50 1024h
28h	32	PBIST_RF10L	2B50 0028h	2B50 1028h
2Ch	32	PBIST_RF11L	2B50 002Ch	2B50 102Ch
30h	32	PBIST_RF12L	2B50 0030h	2B50 1030h
34h	32	PBIST_RF13L	2B50 0034h	2B50 1034h
38h	32	PBIST_RF14L	2B50 0038h	2B50 1038h
3Ch	32	PBIST_RF15L	2B50 003Ch	2B50 103Ch
40h	32	PBIST_RF0U	2B50 0040h	2B50 1040h
44h	32	PBIST_RF1U	2B50 0044h	2B50 1044h
48h	32	PBIST_RF2U	2B50 0048h	2B50 1048h
4Ch	32	PBIST_RF3U	2B50 004Ch	2B50 104Ch
50h	32	PBIST_RF4U	2B50 0050h	2B50 1050h
54h	32	PBIST_RF5U	2B50 0054h	2B50 1054h
58h	32	PBIST_RF6U	2B50 0058h	2B50 1058h
5Ch	32	PBIST_RF7U	2B50 005Ch	2B50 105Ch
60h	32	PBIST_RF8U	2B50 0060h	2B50 1060h
64h	32	PBIST_RF9U	2B50 0064h	2B50 1064h
68h	32	PBIST_RF10U	2B50 0068h	2B50 1068h
6Ch	32	PBIST_RF11U	2B50 006Ch	2B50 106Ch
70h	32	PBIST_RF12U	2B50 0070h	2B50 1070h
74h	32	PBIST_RF13U	2B50 0074h	2B50 1074h
78h	32	PBIST_RF14U	2B50 0078h	2B50 1078h
7Ch	32	PBIST_RF15U	2B50 007Ch	2B50 107Ch

Table 14-15903. PBIST Registers, Base Address=0039 0000h, Length=1024 (continued)

Offset	Length	Register Name	WKUP_PBIST1 Physical Address	WKUP_PBIST0 Physical Address
100h	32	PBIST_A0	2B50 0100h	2B50 1100h
104h	32	PBIST_A1	2B50 0104h	2B50 1104h
108h	32	PBIST_A2	2B50 0108h	2B50 1108h
10Ch	32	PBIST_A3	2B50 010Ch	2B50 110Ch
110h	32	PBIST_L0	2B50 0110h	2B50 1110h
114h	32	PBIST_L1	2B50 0114h	2B50 1114h
118h	32	PBIST_L2	2B50 0118h	2B50 1118h
11Ch	32	PBIST_L3	2B50 011Ch	2B50 111Ch
120h	32	PBIST_D	2B50 0120h	2B50 1120h
124h	32	PBIST_E	2B50 0124h	2B50 1124h
130h	32	PBIST_CA0	2B50 0130h	2B50 1130h
134h	32	PBIST_CA1	2B50 0134h	2B50 1134h
138h	32	PBIST_CA2	2B50 0138h	2B50 1138h
13Ch	32	PBIST_CA3	2B50 013Ch	2B50 113Ch
140h	32	PBIST_CL0	2B50 0140h	2B50 1140h
144h	32	PBIST_CL1	2B50 0144h	2B50 1144h
148h	32	PBIST_CL2	2B50 0148h	2B50 1148h
14Ch	32	PBIST_CL3	2B50 014Ch	2B50 114Ch
150h	32	PBIST_I0	2B50 0150h	2B50 1150h
154h	32	PBIST_I1	2B50 0154h	2B50 1154h
158h	32	PBIST_I2	2B50 0158h	2B50 1158h
15Ch	32	PBIST_I3	2B50 015Ch	2B50 115Ch
160h	32	PBIST_RAMT	2B50 0160h	2B50 1160h
164h	32	PBIST_DLR	2B50 0164h	2B50 1164h
168h	32	PBIST_CMS	2B50 0168h	2B50 1168h
16Ch	32	PBIST_STR	2B50 016Ch	2B50 116Ch
170h	64	PBIST_SCR	2B50 0170h	2B50 1170h
178h	32	PBIST_CSR	2B50 0178h	2B50 1178h
17Ch	32	PBIST_FDLY	2B50 017Ch	2B50 117Ch
180h	32	PBIST_PACT	2B50 0180h	2B50 1180h
184h	32	PBIST_PID	2B50 0184h	2B50 1184h
188h	32	PBIST_OVER	2B50 0188h	2B50 1188h
190h	64	PBIST_FSRF	2B50 0190h	2B50 1190h
198h	64	PBIST_FSRC	2B50 0198h	2B50 1198h
1A0h	64	PBIST_FSRA	2B50 01A0h	2B50 11A0h
1A8h	32	PBIST_FSRDL0	2B50 01A8h	2B50 11A8h
1B0h	32	PBIST_FSRDL1	2B50 01B0h	2B50 11B0h
1B4h	32	PBIST_MARGIN_MODE	2B50 01B4h	2B50 11B4h
1B8h	32	PBIST_WRENZ	2B50 01B8h	2B50 11B8h
1BCh	32	PBIST_PAGE_PGS	2B50 01BCh	2B50 11BCh
1C0h	32	PBIST_ROM	2B50 01C0h	2B50 11C0h
1C4h	32	PBIST_ALGO	2B50 01C4h	2B50 11C4h
1C8h	64	PBIST_RINFO	2B50 01C8h	2B50 11C8h

14.8.2.2 PBIST Registers

PBIST Registers

14.8.2.2.1 PBIST_RF0L Register

14.8.2.2.1.1 PBIST_RF0L Register (Offset = 0h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15904. Instance Table

Instance Name	Physical Address
PBIST0	0039 0000h
PBIST1	003A 0000h
PBIST2	003B 0000h
PBIST3	003C 0000h
PBIST4	003D 0000h
PBIST5	003E 0000h
PBIST6	003F 0000h
PBIST7	0034 0000h
PBIST8	0035 0000h
WKUP_PBIST0	2B50 0000h
WKUP_PBIST1	2B50 1000h

Figure 14-7824. PBIST_RF0L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF0L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF0L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF0L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF0L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15905. PBIST_RF0L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF0L	R/W	0h	Register Files / Instruction Registers RF0 lower (RF0L) Reset Source: mod_g_rst_n

14.8.2.2.2 PBIST_RF1L Register

14.8.2.2.2.1 PBIST_RF1L Register (Offset = 4h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15906. Instance Table

Instance Name	Physical Address
PBIST0	0039 0004h
PBIST1	003A 0004h
PBIST2	003B 0004h
PBIST3	003C 0004h
PBIST4	003D 0004h
PBIST5	003E 0004h
PBIST6	003F 0004h
PBIST7	0034 0004h
PBIST8	0035 0004h
WKUP_PBIST0	2B50 0004h
WKUP_PBIST1	2B50 1004h

Figure 14-7825. PBIST_RF1L Name Register

31	30	29	28	27	26	25	24
RF1L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF1L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF1L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF1L							
R/W							
0h							

Table 14-15907. PBIST_RF1L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF1L	R/W	0h	Register Files / Instruction Registers RF1 lower (RF1L) Reset Source: mod_g_rst_n

14.8.2.2.3 PBIST_RF2L Register

14.8.2.2.3.1 PBIST_RF2L Register (Offset = 8h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15908. Instance Table

Instance Name	Physical Address
PBIST0	0039 0008h
PBIST1	003A 0008h
PBIST2	003B 0008h
PBIST3	003C 0008h
PBIST4	003D 0008h
PBIST5	003E 0008h
PBIST6	003F 0008h
PBIST7	0034 0008h
PBIST8	0035 0008h
WKUP_PBIST0	2B50 0008h
WKUP_PBIST1	2B50 1008h

Figure 14-7826. PBIST_RF2L Name Register

31	30	29	28	27	26	25	24
RF2L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF2L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF2L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF2L							
R/W							
0h							

Table 14-15909. PBIST_RF2L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF2L	R/W	0h	Register Files / Instruction Registers RF2 lower (RF2L) Reset Source: mod_g_rst_n

14.8.2.2.4 PBIST_RF3L Register

14.8.2.2.4.1 PBIST_RF3L Register (Offset = Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15910. Instance Table

Instance Name	Physical Address
PBIST0	0039 000Ch
PBIST1	003A 000Ch
PBIST2	003B 000Ch
PBIST3	003C 000Ch
PBIST4	003D 000Ch
PBIST5	003E 000Ch
PBIST6	003F 000Ch
PBIST7	0034 000Ch
PBIST8	0035 000Ch
WKUP_PBIST0	2B50 000Ch
WKUP_PBIST1	2B50 100Ch

Figure 14-7827. PBIST_RF3L Name Register

31	30	29	28	27	26	25	24
RF3L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RF3L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RF3L							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RF3L							
R/W							
0h							

Table 14-15911. PBIST_RF3L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF3L	R/W	0h	Register Files / Instruction Registers RF3 lower (RF3L) Reset Source: mod_g_rst_n

14.8.2.2.5 PBIST_RF4L Register

14.8.2.2.5.1 PBIST_RF4L Register (Offset = 10h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15912. Instance Table

Instance Name	Physical Address
PBIST0	0039 0010h
PBIST1	003A 0010h
PBIST2	003B 0010h
PBIST3	003C 0010h
PBIST4	003D 0010h
PBIST5	003E 0010h
PBIST6	003F 0010h
PBIST7	0034 0010h
PBIST8	0035 0010h
WKUP_PBIST0	2B50 0010h
WKUP_PBIST1	2B50 1010h

Figure 14-7828. PBIST_RF4L Name Register

31	30	29	28	27	26	25	24
RF4L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF4L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF4L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF4L							
R/W							
0h							

Table 14-15913. PBIST_RF4L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF4L	R/W	0h	Register Files / Instruction Registers RF4 lower (RF4L) Reset Source: mod_g_rst_n

14.8.2.2.6 PBIST_RF5L Register

14.8.2.2.6.1 PBIST_RF5L Register (Offset = 14h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15914. Instance Table

Instance Name	Physical Address
PBIST0	0039 0014h
PBIST1	003A 0014h
PBIST2	003B 0014h
PBIST3	003C 0014h
PBIST4	003D 0014h
PBIST5	003E 0014h
PBIST6	003F 0014h
PBIST7	0034 0014h
PBIST8	0035 0014h
WKUP_PBIST0	2B50 0014h
WKUP_PBIST1	2B50 1014h

Figure 14-7829. PBIST_RF5L Name Register

31	30	29	28	27	26	25	24
RF5L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF5L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF5L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF5L							
R/W							
0h							

Table 14-15915. PBIST_RF5L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF5L	R/W	0h	Register Files / Instruction Registers RF5 lower (RF5L) Reset Source: mod_g_rst_n

14.8.2.2.7 PBIST_RF6L Register

14.8.2.2.7.1 PBIST_RF6L Register (Offset = 18h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15916. Instance Table

Instance Name	Physical Address
PBIST0	0039 0018h
PBIST1	003A 0018h
PBIST2	003B 0018h
PBIST3	003C 0018h
PBIST4	003D 0018h
PBIST5	003E 0018h
PBIST6	003F 0018h
PBIST7	0034 0018h
PBIST8	0035 0018h
WKUP_PBIST0	2B50 0018h
WKUP_PBIST1	2B50 1018h

Figure 14-7830. PBIST_RF6L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF6L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF6L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF6L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF6L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15917. PBIST_RF6L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF6L	R/W	0h	Register Files / Instruction Registers RF6 lower (RF6L) Reset Source: mod_g_rst_n

14.8.2.2.8 PBIST_RF7L Register

14.8.2.2.8.1 PBIST_RF7L Register (Offset = 1Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15918. Instance Table

Instance Name	Physical Address
PBIST0	0039 001Ch
PBIST1	003A 001Ch
PBIST2	003B 001Ch
PBIST3	003C 001Ch
PBIST4	003D 001Ch
PBIST5	003E 001Ch
PBIST6	003F 001Ch
PBIST7	0034 001Ch
PBIST8	0035 001Ch
WKUP_PBIST0	2B50 001Ch
WKUP_PBIST1	2B50 101Ch

Figure 14-7831. PBIST_RF7L Name Register

31	30	29	28	27	26	25	24
RF7L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF7L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF7L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF7L							
R/W							
0h							

Table 14-15919. PBIST_RF7L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF7L	R/W	0h	Register Files / Instruction Registers RF7 lower (RF7L) Reset Source: mod_g_rst_n

14.8.2.2.9 PBIST_RF8L Register

14.8.2.2.9.1 PBIST_RF8L Register (Offset = 20h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15920. Instance Table

Instance Name	Physical Address
PBIST0	0039 0020h
PBIST1	003A 0020h
PBIST2	003B 0020h
PBIST3	003C 0020h
PBIST4	003D 0020h
PBIST5	003E 0020h
PBIST6	003F 0020h
PBIST7	0034 0020h
PBIST8	0035 0020h
WKUP_PBIST0	2B50 0020h
WKUP_PBIST1	2B50 1020h

Figure 14-7832. PBIST_RF8L Name Register

31	30	29	28	27	26	25	24
RF8L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF8L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF8L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF8L							
R/W							
0h							

Table 14-15921. PBIST_RF8L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF8L	R/W	0h	Register Files / Instruction Registers RF8 lower (RF8L) Reset Source: mod_g_rst_n

14.8.2.2.10 PBIST_RF9L Register

14.8.2.2.10.1 PBIST_RF9L Register (Offset = 24h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15922. Instance Table

Instance Name	Physical Address
PBIST0	0039 0024h
PBIST1	003A 0024h
PBIST2	003B 0024h
PBIST3	003C 0024h
PBIST4	003D 0024h
PBIST5	003E 0024h
PBIST6	003F 0024h
PBIST7	0034 0024h
PBIST8	0035 0024h
WKUP_PBIST0	2B50 0024h
WKUP_PBIST1	2B50 1024h

Figure 14-7833. PBIST_RF9L Name Register

31	30	29	28	27	26	25	24
RF9L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF9L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF9L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF9L							
R/W							
0h							

Table 14-15923. PBIST_RF9L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF9L	R/W	0h	Register Files / Instruction Registers RF9 lower (RF9L) Reset Source: mod_g_rst_n

14.8.2.2.11 PBIST_RF10L Register

14.8.2.2.11.1 PBIST_RF10L Register (Offset = 28h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15924. Instance Table

Instance Name	Physical Address
PBIST0	0039 0028h
PBIST1	003A 0028h
PBIST2	003B 0028h
PBIST3	003C 0028h
PBIST4	003D 0028h
PBIST5	003E 0028h
PBIST6	003F 0028h
PBIST7	0034 0028h
PBIST8	0035 0028h
WKUP_PBIST0	2B50 0028h
WKUP_PBIST1	2B50 1028h

Figure 14-7834. PBIST_RF10L Name Register

31	30	29	28	27	26	25	24
RF10L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF10L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF10L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF10L							
R/W							
0h							

Table 14-15925. PBIST_RF10L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF10L	R/W	0h	Register Files / Instruction Registers RF10 lower (RF10L) Reset Source: mod_g_rst_n

14.8.2.2.12 PBIST_RF11L Register

14.8.2.2.12.1 PBIST_RF11L Register (Offset = 2Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15926. Instance Table

Instance Name	Physical Address
PBIST0	0039 002Ch
PBIST1	003A 002Ch
PBIST2	003B 002Ch
PBIST3	003C 002Ch
PBIST4	003D 002Ch
PBIST5	003E 002Ch
PBIST6	003F 002Ch
PBIST7	0034 002Ch
PBIST8	0035 002Ch
WKUP_PBIST0	2B50 002Ch
WKUP_PBIST1	2B50 102Ch

Figure 14-7835. PBIST_RF11L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF11L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF11L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF11L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF11L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15927. PBIST_RF11L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF11L	R/W	0h	Register Files / Instruction Registers RF11 lower (RF11L) Reset Source: mod_g_rst_n

14.8.2.2.13 PBIST_RF12L Register

14.8.2.2.13.1 PBIST_RF12L Register (Offset = 30h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15928. Instance Table

Instance Name	Physical Address
PBIST0	0039 0030h
PBIST1	003A 0030h
PBIST2	003B 0030h
PBIST3	003C 0030h
PBIST4	003D 0030h
PBIST5	003E 0030h
PBIST6	003F 0030h
PBIST7	0034 0030h
PBIST8	0035 0030h
WKUP_PBIST0	2B50 0030h
WKUP_PBIST1	2B50 1030h

Figure 14-7836. PBIST_RF12L Name Register

31	30	29	28	27	26	25	24
RF12L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF12L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF12L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF12L							
R/W							
0h							

Table 14-15929. PBIST_RF12L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF12L	R/W	0h	Register Files / Instruction Registers RF12 lower (RF12L) Reset Source: mod_g_rst_n

14.8.2.2.14 PBIST_RF13L Register

14.8.2.2.14.1 PBIST_RF13L Register (Offset = 34h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15930. Instance Table

Instance Name	Physical Address
PBIST0	0039 0034h
PBIST1	003A 0034h
PBIST2	003B 0034h
PBIST3	003C 0034h
PBIST4	003D 0034h
PBIST5	003E 0034h
PBIST6	003F 0034h
PBIST7	0034 0034h
PBIST8	0035 0034h
WKUP_PBIST0	2B50 0034h
WKUP_PBIST1	2B50 1034h

Figure 14-7837. PBIST_RF13L Name Register

31	30	29	28	27	26	25	24
RF13L							
R/W							
0h							
23	22	21	20	19	18	17	16
RF13L							
R/W							
0h							
15	14	13	12	11	10	9	8
RF13L							
R/W							
0h							
7	6	5	4	3	2	1	0
RF13L							
R/W							
0h							

Table 14-15931. PBIST_RF13L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF13L	R/W	0h	Register Files / Instruction Registers RF13 lower (RF13L) Reset Source: mod_g_rst_n

14.8.2.2.15 PBIST_RF14L Register

14.8.2.2.15.1 PBIST_RF14L Register (Offset = 38h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15932. Instance Table

Instance Name	Physical Address
PBIST0	0039 0038h
PBIST1	003A 0038h
PBIST2	003B 0038h
PBIST3	003C 0038h
PBIST4	003D 0038h
PBIST5	003E 0038h
PBIST6	003F 0038h
PBIST7	0034 0038h
PBIST8	0035 0038h
WKUP_PBIST0	2B50 0038h
WKUP_PBIST1	2B50 1038h

Figure 14-7838. PBIST_RF14L Name Register

31	30	29	28	27	26	25	24
RF14L							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RF14L							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RF14L							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RF14L							
R/W							
0h							

Table 14-15933. PBIST_RF14L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF14L	R/W	0h	Register Files / Instruction Registers RF14 lower (RF14L) Reset Source: mod_g_rst_n

14.8.2.2.16 PBIST_RF15L Register

14.8.2.2.16.1 PBIST_RF15L Register (Offset = 3Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15934. Instance Table

Instance Name	Physical Address
PBIST0	0039 003Ch
PBIST1	003A 003Ch
PBIST2	003B 003Ch
PBIST3	003C 003Ch
PBIST4	003D 003Ch
PBIST5	003E 003Ch
PBIST6	003F 003Ch
PBIST7	0034 003Ch
PBIST8	0035 003Ch
WKUP_PBIST0	2B50 003Ch
WKUP_PBIST1	2B50 103Ch

Figure 14-7839. PBIST_RF15L Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF15L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF15L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF15L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF15L</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15935. PBIST_RF15L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF15L	R/W	0h	Register Files / Instruction Registers RF15 lower (RF15L) Reset Source: mod_g_rst_n

14.8.2.2.17 PBIST_RF0U Register

14.8.2.2.17.1 PBIST_RF0U Register (Offset = 40h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15936. Instance Table

Instance Name	Physical Address
PBIST0	0039 0040h
PBIST1	003A 0040h
PBIST2	003B 0040h
PBIST3	003C 0040h
PBIST4	003D 0040h
PBIST5	003E 0040h
PBIST6	003F 0040h
PBIST7	0034 0040h
PBIST8	0035 0040h
WKUP_PBIST0	2B50 0040h
WKUP_PBIST1	2B50 1040h

Figure 14-7840. PBIST_RF0U Name Register

31	30	29	28	27	26	25	24
RF0U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF0U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF0U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF0U							
R/W							
0h							

Table 14-15937. PBIST_RF0U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF0U	R/W	0h	Register Files / Instruction Registers RF0 upper (RF0U) Reset Source: mod_g_rst_n

14.8.2.2.18 PBIST_RF1U Register

14.8.2.2.18.1 PBIST_RF1U Register (Offset = 44h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15938. Instance Table

Instance Name	Physical Address
PBIST0	0039 0044h
PBIST1	003A 0044h
PBIST2	003B 0044h
PBIST3	003C 0044h
PBIST4	003D 0044h
PBIST5	003E 0044h
PBIST6	003F 0044h
PBIST7	0034 0044h
PBIST8	0035 0044h
WKUP_PBIST0	2B50 0044h
WKUP_PBIST1	2B50 1044h

Figure 14-7841. PBIST_RF1U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF1U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF1U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF1U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF1U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15939. PBIST_RF1U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF1U	R/W	0h	Register Files / Instruction Registers RF1 upper (RF1U) Reset Source: mod_g_rst_n

14.8.2.2.19 PBIST_RF2U Register

14.8.2.2.19.1 PBIST_RF2U Register (Offset = 48h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15940. Instance Table

Instance Name	Physical Address
PBIST0	0039 0048h
PBIST1	003A 0048h
PBIST2	003B 0048h
PBIST3	003C 0048h
PBIST4	003D 0048h
PBIST5	003E 0048h
PBIST6	003F 0048h
PBIST7	0034 0048h
PBIST8	0035 0048h
WKUP_PBIST0	2B50 0048h
WKUP_PBIST1	2B50 1048h

Figure 14-7842. PBIST_RF2U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF2U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF2U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF2U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF2U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15941. PBIST_RF2U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF2U	R/W	0h	Register Files / Instruction Registers RF2 upper (RF2U) Reset Source: mod_g_rst_n

14.8.2.2.20 PBIST_RF3U Register

14.8.2.2.20.1 PBIST_RF3U Register (Offset = 4Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15942. Instance Table

Instance Name	Physical Address
PBIST0	0039 004Ch
PBIST1	003A 004Ch
PBIST2	003B 004Ch
PBIST3	003C 004Ch
PBIST4	003D 004Ch
PBIST5	003E 004Ch
PBIST6	003F 004Ch
PBIST7	0034 004Ch
PBIST8	0035 004Ch
WKUP_PBIST0	2B50 004Ch
WKUP_PBIST1	2B50 104Ch

Figure 14-7843. PBIST_RF3U Name Register

31	30	29	28	27	26	25	24
RF3U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF3U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF3U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF3U							
R/W							
0h							

Table 14-15943. PBIST_RF3U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF3U	R/W	0h	Register Files / Instruction Registers RF3 upper (RF3U) Reset Source: mod_g_rst_n

14.8.2.2.21 PBIST_RF4U Register

14.8.2.2.21.1 PBIST_RF4U Register (Offset = 50h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15944. Instance Table

Instance Name	Physical Address
PBIST0	0039 0050h
PBIST1	003A 0050h
PBIST2	003B 0050h
PBIST3	003C 0050h
PBIST4	003D 0050h
PBIST5	003E 0050h
PBIST6	003F 0050h
PBIST7	0034 0050h
PBIST8	0035 0050h
WKUP_PBIST0	2B50 0050h
WKUP_PBIST1	2B50 1050h

Figure 14-7844. PBIST_RF4U Name Register

31	30	29	28	27	26	25	24
RF4U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF4U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF4U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF4U							
R/W							
0h							

Table 14-15945. PBIST_RF4U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF4U	R/W	0h	Register Files / Instruction Registers RF4 upper (RF4U) Reset Source: mod_g_rst_n

14.8.2.2.22 PBIST_RF5U Register

14.8.2.2.22.1 PBIST_RF5U Register (Offset = 54h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15946. Instance Table

Instance Name	Physical Address
PBIST0	0039 0054h
PBIST1	003A 0054h
PBIST2	003B 0054h
PBIST3	003C 0054h
PBIST4	003D 0054h
PBIST5	003E 0054h
PBIST6	003F 0054h
PBIST7	0034 0054h
PBIST8	0035 0054h
WKUP_PBIST0	2B50 0054h
WKUP_PBIST1	2B50 1054h

Figure 14-7845. PBIST_RF5U Name Register

31	30	29	28	27	26	25	24
RF5U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF5U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF5U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF5U							
R/W							
0h							

Table 14-15947. PBIST_RF5U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF5U	R/W	0h	Register Files / Instruction Registers RF5 upper (RF5U) Reset Source: mod_g_rst_n

14.8.2.2.23 PBIST_RF6U Register

14.8.2.2.23.1 PBIST_RF6U Register (Offset = 58h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15948. Instance Table

Instance Name	Physical Address
PBIST0	0039 0058h
PBIST1	003A 0058h
PBIST2	003B 0058h
PBIST3	003C 0058h
PBIST4	003D 0058h
PBIST5	003E 0058h
PBIST6	003F 0058h
PBIST7	0034 0058h
PBIST8	0035 0058h
WKUP_PBIST0	2B50 0058h
WKUP_PBIST1	2B50 1058h

Figure 14-7846. PBIST_RF6U Name Register

31	30	29	28	27	26	25	24
RF6U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF6U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF6U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF6U							
R/W							
0h							

Table 14-15949. PBIST_RF6U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF6U	R/W	0h	Register Files / Instruction Registers RF6 upper (RF6U) Reset Source: mod_g_rst_n

14.8.2.2.24 PBIST_RF7U Register

14.8.2.2.24.1 PBIST_RF7U Register (Offset = 5Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15950. Instance Table

Instance Name	Physical Address
PBIST0	0039 005Ch
PBIST1	003A 005Ch
PBIST2	003B 005Ch
PBIST3	003C 005Ch
PBIST4	003D 005Ch
PBIST5	003E 005Ch
PBIST6	003F 005Ch
PBIST7	0034 005Ch
PBIST8	0035 005Ch
WKUP_PBIST0	2B50 005Ch
WKUP_PBIST1	2B50 105Ch

Figure 14-7847. PBIST_RF7U Name Register

31	30	29	28	27	26	25	24
RF7U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF7U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF7U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF7U							
R/W							
0h							

Table 14-15951. PBIST_RF7U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF7U	R/W	0h	Register Files / Instruction Registers RF7 upper (RF7U) Reset Source: mod_g_rst_n

14.8.2.2.25 PBIST_RF8U Register

14.8.2.2.25.1 PBIST_RF8U Register (Offset = 60h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15952. Instance Table

Instance Name	Physical Address
PBIST0	0039 0060h
PBIST1	003A 0060h
PBIST2	003B 0060h
PBIST3	003C 0060h
PBIST4	003D 0060h
PBIST5	003E 0060h
PBIST6	003F 0060h
PBIST7	0034 0060h
PBIST8	0035 0060h
WKUP_PBIST0	2B50 0060h
WKUP_PBIST1	2B50 1060h

Figure 14-7848. PBIST_RF8U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF8U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF8U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF8U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF8U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15953. PBIST_RF8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF8U	R/W	0h	Register Files / Instruction Registers RF8 upper (RF8U) Reset Source: mod_g_rst_n

14.8.2.2.26 PBIST_RF9U Register

14.8.2.2.26.1 PBIST_RF9U Register (Offset = 64h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15954. Instance Table

Instance Name	Physical Address
PBIST0	0039 0064h
PBIST1	003A 0064h
PBIST2	003B 0064h
PBIST3	003C 0064h
PBIST4	003D 0064h
PBIST5	003E 0064h
PBIST6	003F 0064h
PBIST7	0034 0064h
PBIST8	0035 0064h
WKUP_PBIST0	2B50 0064h
WKUP_PBIST1	2B50 1064h

Figure 14-7849. PBIST_RF9U Name Register

31	30	29	28	27	26	25	24
RF9U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF9U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF9U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF9U							
R/W							
0h							

Table 14-15955. PBIST_RF9U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF9U	R/W	0h	Register Files / Instruction Registers RF9 upper (RF9U) Reset Source: mod_g_rst_n

14.8.2.2.27 PBIST_RF10U Register

14.8.2.2.27.1 PBIST_RF10U Register (Offset = 68h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15956. Instance Table

Instance Name	Physical Address
PBIST0	0039 0068h
PBIST1	003A 0068h
PBIST2	003B 0068h
PBIST3	003C 0068h
PBIST4	003D 0068h
PBIST5	003E 0068h
PBIST6	003F 0068h
PBIST7	0034 0068h
PBIST8	0035 0068h
WKUP_PBIST0	2B50 0068h
WKUP_PBIST1	2B50 1068h

Figure 14-7850. PBIST_RF10U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF10U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF10U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF10U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF10U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15957. PBIST_RF10U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF10U	R/W	0h	Register Files / Instruction Registers RF10 upper (RF10U) Reset Source: mod_g_rst_n

14.8.2.2.28 PBIST_RF11U Register

14.8.2.2.28.1 PBIST_RF11U Register (Offset = 6Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15958. Instance Table

Instance Name	Physical Address
PBIST0	0039 006Ch
PBIST1	003A 006Ch
PBIST2	003B 006Ch
PBIST3	003C 006Ch
PBIST4	003D 006Ch
PBIST5	003E 006Ch
PBIST6	003F 006Ch
PBIST7	0034 006Ch
PBIST8	0035 006Ch
WKUP_PBIST0	2B50 006Ch
WKUP_PBIST1	2B50 106Ch

Figure 14-7851. PBIST_RF11U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF11U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF11U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF11U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF11U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15959. PBIST_RF11U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF11U	R/W	0h	Register Files / Instruction Registers RF11 upper (RF11U) Reset Source: mod_g_rst_n

14.8.2.2.29 PBIST_RF12U Register

14.8.2.2.29.1 PBIST_RF12U Register (Offset = 70h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15960. Instance Table

Instance Name	Physical Address
PBIST0	0039 0070h
PBIST1	003A 0070h
PBIST2	003B 0070h
PBIST3	003C 0070h
PBIST4	003D 0070h
PBIST5	003E 0070h
PBIST6	003F 0070h
PBIST7	0034 0070h
PBIST8	0035 0070h
WKUP_PBIST0	2B50 0070h
WKUP_PBIST1	2B50 1070h

Figure 14-7852. PBIST_RF12U Name Register

31	30	29	28	27	26	25	24
RF12U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF12U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF12U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF12U							
R/W							
0h							

Table 14-15961. PBIST_RF12U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF12U	R/W	0h	Register Files / Instruction Registers RF12 upper (RF12U) Reset Source: mod_g_rst_n

14.8.2.2.30 PBIST_RF13U Register

14.8.2.2.30.1 PBIST_RF13U Register (Offset = 74h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15962. Instance Table

Instance Name	Physical Address
PBIST0	0039 0074h
PBIST1	003A 0074h
PBIST2	003B 0074h
PBIST3	003C 0074h
PBIST4	003D 0074h
PBIST5	003E 0074h
PBIST6	003F 0074h
PBIST7	0034 0074h
PBIST8	0035 0074h
WKUP_PBIST0	2B50 0074h
WKUP_PBIST1	2B50 1074h

Figure 14-7853. PBIST_RF13U Name Register

31	30	29	28	27	26	25	24
RF13U							
R/W							
0h							
23	22	21	20	19	18	17	16
RF13U							
R/W							
0h							
15	14	13	12	11	10	9	8
RF13U							
R/W							
0h							
7	6	5	4	3	2	1	0
RF13U							
R/W							
0h							

Table 14-15963. PBIST_RF13U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF13U	R/W	0h	Register Files / Instruction Registers RF13 upper (RF13U) Reset Source: mod_g_rst_n

14.8.2.2.31 PBIST_RF14U Register

14.8.2.2.31.1 PBIST_RF14U Register (Offset = 78h) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15964. Instance Table

Instance Name	Physical Address
PBIST0	0039 0078h
PBIST1	003A 0078h
PBIST2	003B 0078h
PBIST3	003C 0078h
PBIST4	003D 0078h
PBIST5	003E 0078h
PBIST6	003F 0078h
PBIST7	0034 0078h
PBIST8	0035 0078h
WKUP_PBIST0	2B50 0078h
WKUP_PBIST1	2B50 1078h

Figure 14-7854. PBIST_RF14U Name Register

31	30	29	28	27	26	25	24
RF14U							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RF14U							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RF14U							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RF14U							
R/W							
0h							

Table 14-15965. PBIST_RF14U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF14U	R/W	0h	Register Files / Instruction Registers RF14 upper (RF14U) Reset Source: mod_g_rst_n

14.8.2.2.32 PBIST_RF15U Register

14.8.2.2.32.1 PBIST_RF15U Register (Offset = 7Ch) [reset = 0h]

Register Files / Instruction Registers

Return to Summary Table

Table 14-15966. Instance Table

Instance Name	Physical Address
PBIST0	0039 007Ch
PBIST1	003A 007Ch
PBIST2	003B 007Ch
PBIST3	003C 007Ch
PBIST4	003D 007Ch
PBIST5	003E 007Ch
PBIST6	003F 007Ch
PBIST7	0034 007Ch
PBIST8	0035 007Ch
WKUP_PBIST0	2B50 007Ch
WKUP_PBIST1	2B50 107Ch

Figure 14-7855. PBIST_RF15U Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RF15U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RF15U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RF15U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RF15U</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15967. PBIST_RF15U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RF15U	R/W	0h	Register Files / Instruction Registers RF15 upper (RF15U) Reset Source: mod_g_rst_n

14.8.2.2.33 PBIST_A0 Register

14.8.2.2.33.1 PBIST_A0 Register (Offset = 100h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-15968. Instance Table

Instance Name	Physical Address
PBIST0	0039 0100h
PBIST1	003A 0100h
PBIST2	003B 0100h
PBIST3	003C 0100h
PBIST4	003D 0100h
PBIST5	003E 0100h
PBIST6	003F 0100h
PBIST7	0034 0100h
PBIST8	0035 0100h
WKUP_PBIST0	2B50 0100h
WKUP_PBIST1	2B50 1100h

Figure 14-7856. PBIST_A0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A0							
R/W							
0h							
7	6	5	4	3	2	1	0
A0							
R/W							
0h							

Table 14-15969. PBIST_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A0	R/W	0h	Variable Address Register 0 (A0) Reset Source: mod_g_rst_n

14.8.2.2.34 PBIST_A1 Register

14.8.2.2.34.1 PBIST_A1 Register (Offset = 104h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-15970. Instance Table

Instance Name	Physical Address
PBIST0	0039 0104h
PBIST1	003A 0104h
PBIST2	003B 0104h
PBIST3	003C 0104h
PBIST4	003D 0104h
PBIST5	003E 0104h
PBIST6	003F 0104h
PBIST7	0034 0104h
PBIST8	0035 0104h
WKUP_PBIST0	2B50 0104h
WKUP_PBIST1	2B50 1104h

Figure 14-7857. PBIST_A1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">A1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">A1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15971. PBIST_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A1	R/W	0h	Variable Address Register 1 (A1) Reset Source: mod_g_rst_n

14.8.2.2.35 PBIST_A2 Register

14.8.2.2.35.1 PBIST_A2 Register (Offset = 108h) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-15972. Instance Table

Instance Name	Physical Address
PBIST0	0039 0108h
PBIST1	003A 0108h
PBIST2	003B 0108h
PBIST3	003C 0108h
PBIST4	003D 0108h
PBIST5	003E 0108h
PBIST6	003F 0108h
PBIST7	0034 0108h
PBIST8	0035 0108h
WKUP_PBIST0	2B50 0108h
WKUP_PBIST1	2B50 1108h

Figure 14-7858. PBIST_A2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A2							
R/W							
0h							
7	6	5	4	3	2	1	0
A2							
R/W							
0h							

Table 14-15973. PBIST_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A2	R/W	0h	Variable Address Register 2 (A2) Reset Source: mod_g_rst_n

14.8.2.2.36 PBIST_A3 Register

14.8.2.2.36.1 PBIST_A3 Register (Offset = 10Ch) [reset = 0h]

Variable Address Registers

Return to Summary Table

Table 14-15974. Instance Table

Instance Name	Physical Address
PBIST0	0039 010Ch
PBIST1	003A 010Ch
PBIST2	003B 010Ch
PBIST3	003C 010Ch
PBIST4	003D 010Ch
PBIST5	003E 010Ch
PBIST6	003F 010Ch
PBIST7	0034 010Ch
PBIST8	0035 010Ch
WKUP_PBIST0	2B50 010Ch
WKUP_PBIST1	2B50 110Ch

Figure 14-7859. PBIST_A3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
A3							
R/W							
0h							
7	6	5	4	3	2	1	0
A3							
R/W							
0h							

Table 14-15975. PBIST_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	A3	R/W	0h	Variable Address Register 3 (A3) Reset Source: mod_g_rst_n

14.8.2.2.37 PBIST_L0 Register

14.8.2.2.37.1 PBIST_L0 Register (Offset = 110h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-15976. Instance Table

Instance Name	Physical Address
PBIST0	0039 0110h
PBIST1	003A 0110h
PBIST2	003B 0110h
PBIST3	003C 0110h
PBIST4	003D 0110h
PBIST5	003E 0110h
PBIST6	003F 0110h
PBIST7	0034 0110h
PBIST8	0035 0110h
WKUP_PBIST0	2B50 0110h
WKUP_PBIST1	2B50 1110h

Figure 14-7860. PBIST_L0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L0							
R/W							
0h							
7	6	5	4	3	2	1	0
L0							
R/W							
0h							

Table 14-15977. PBIST_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L0	R/W	0h	Variable Loop Count Register 0 (L0) Reset Source: mod_g_rst_n

14.8.2.2.38 PBIST_L1 Register

14.8.2.2.38.1 PBIST_L1 Register (Offset = 114h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-15978. Instance Table

Instance Name	Physical Address
PBIST0	0039 0114h
PBIST1	003A 0114h
PBIST2	003B 0114h
PBIST3	003C 0114h
PBIST4	003D 0114h
PBIST5	003E 0114h
PBIST6	003F 0114h
PBIST7	0034 0114h
PBIST8	0035 0114h
WKUP_PBIST0	2B50 0114h
WKUP_PBIST1	2B50 1114h

Figure 14-7861. PBIST_L1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L1							
R/W							
0h							
7	6	5	4	3	2	1	0
L1							
R/W							
0h							

Table 14-15979. PBIST_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L1	R/W	0h	Variable Loop Count Register 1 (L1) Reset Source: mod_g_rst_n

14.8.2.2.39 PBIST_L2 Register

14.8.2.2.39.1 PBIST_L2 Register (Offset = 118h) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-15980. Instance Table

Instance Name	Physical Address
PBIST0	0039 0118h
PBIST1	003A 0118h
PBIST2	003B 0118h
PBIST3	003C 0118h
PBIST4	003D 0118h
PBIST5	003E 0118h
PBIST6	003F 0118h
PBIST7	0034 0118h
PBIST8	0035 0118h
WKUP_PBIST0	2B50 0118h
WKUP_PBIST1	2B50 1118h

Figure 14-7862. PBIST_L2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">L2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">L2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15981. PBIST_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L2	R/W	0h	Variable Loop Count Register 2 (L2) Reset Source: mod_g_rst_n

14.8.2.2.40 PBIST_L3 Register

14.8.2.2.40.1 PBIST_L3 Register (Offset = 11Ch) [reset = 0h]

Variable Loop Count Registers

Return to Summary Table

Table 14-15982. Instance Table

Instance Name	Physical Address
PBIST0	0039 011Ch
PBIST1	003A 011Ch
PBIST2	003B 011Ch
PBIST3	003C 011Ch
PBIST4	003D 011Ch
PBIST5	003E 011Ch
PBIST6	003F 011Ch
PBIST7	0034 011Ch
PBIST8	0035 011Ch
WKUP_PBIST0	2B50 011Ch
WKUP_PBIST1	2B50 111Ch

Figure 14-7863. PBIST_L3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L3							
R/W							
0h							
7	6	5	4	3	2	1	0
L3							
R/W							
0h							

Table 14-15983. PBIST_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	L3	R/W	0h	Variable Loop Count Register 3 (L3) Reset Source: mod_g_rst_n

14.8.2.2.41 PBIST_D Register

14.8.2.2.41.1 PBIST_D Register (Offset = 120h) [reset = 0h]

Data Registers

Return to Summary Table

Table 14-15984. Instance Table

Instance Name	Physical Address
PBIST0	0039 0120h
PBIST1	003A 0120h
PBIST2	003B 0120h
PBIST3	003C 0120h
PBIST4	003D 0120h
PBIST5	003E 0120h
PBIST6	003F 0120h
PBIST7	0034 0120h
PBIST8	0035 0120h
WKUP_PBIST0	2B50 0120h
WKUP_PBIST1	2B50 1120h

Figure 14-7864. PBIST_D Name Register

31	30	29	28	27	26	25	24
D1							
R/W							
0h							
23	22	21	20	19	18	17	16
D1							
R/W							
0h							
15	14	13	12	11	10	9	8
D0							
R/W							
0h							
7	6	5	4	3	2	1	0
D0							
R/W							
0h							

Table 14-15985. PBIST_D Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	D1	R/W	0h	DD1 Data Register Upper 16 (D1) Reset Source: mod_g_rst_n
15:0	D0	R/W	0h	DD0 Data Register Lower 16 (D0) Reset Source: mod_g_rst_n

14.8.2.2.42 PBIST_E Register

14.8.2.2.42.1 PBIST_E Register (Offset = 124h) [reset = 0h]

Data Registers

Return to Summary Table

Table 14-15986. Instance Table

Instance Name	Physical Address
PBIST0	0039 0124h
PBIST1	003A 0124h
PBIST2	003B 0124h
PBIST3	003C 0124h
PBIST4	003D 0124h
PBIST5	003E 0124h
PBIST6	003F 0124h
PBIST7	0034 0124h
PBIST8	0035 0124h
WKUP_PBIST0	2B50 0124h
WKUP_PBIST1	2B50 1124h

Figure 14-7865. PBIST_E Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">E1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">E1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">E0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">E0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15987. PBIST_E Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	E1	R/W	0h	EE1 Data Register Upper 16 (E1) Reset Source: mod_g_rst_n
15:0	E0	R/W	0h	EE0 Data Register Lower 16 (E0) Reset Source: mod_g_rst_n

14.8.2.2.43 PBIST_CA0 Register

14.8.2.2.43.1 PBIST_CA0 Register (Offset = 130h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-15988. Instance Table

Instance Name	Physical Address
PBIST0	0039 0130h
PBIST1	003A 0130h
PBIST2	003B 0130h
PBIST3	003C 0130h
PBIST4	003D 0130h
PBIST5	003E 0130h
PBIST6	003F 0130h
PBIST7	0034 0130h
PBIST8	0035 0130h
WKUP_PBIST0	2B50 0130h
WKUP_PBIST1	2B50 1130h

Figure 14-7866. PBIST_CA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CA0							
R/W							
0h							
7	6	5	4	3	2	1	0
CA0							
R/W							
0h							

Table 14-15989. PBIST_CA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA0	R/W	0h	Constant Address Register 0 (CA0) Reset Source: mod_g_rst_n

14.8.2.2.44 PBIST_CA1 Register

14.8.2.2.44.1 PBIST_CA1 Register (Offset = 134h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-15990. Instance Table

Instance Name	Physical Address
PBIST0	0039 0134h
PBIST1	003A 0134h
PBIST2	003B 0134h
PBIST3	003C 0134h
PBIST4	003D 0134h
PBIST5	003E 0134h
PBIST6	003F 0134h
PBIST7	0034 0134h
PBIST8	0035 0134h
WKUP_PBIST0	2B50 0134h
WKUP_PBIST1	2B50 1134h

Figure 14-7867. PBIST_CA1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CA1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CA1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15991. PBIST_CA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA1	R/W	0h	Constant Address Register 1 (CA1) Reset Source: mod_g_rst_n

14.8.2.2.45 PBIST_CA2 Register

14.8.2.2.45.1 PBIST_CA2 Register (Offset = 138h) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-15992. Instance Table

Instance Name	Physical Address
PBIST0	0039 0138h
PBIST1	003A 0138h
PBIST2	003B 0138h
PBIST3	003C 0138h
PBIST4	003D 0138h
PBIST5	003E 0138h
PBIST6	003F 0138h
PBIST7	0034 0138h
PBIST8	0035 0138h
WKUP_PBIST0	2B50 0138h
WKUP_PBIST1	2B50 1138h

Figure 14-7868. PBIST_CA2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CA2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CA2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15993. PBIST_CA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA2	R/W	0h	Constant Address Register 2 (CA2) Reset Source: mod_g_rst_n

14.8.2.2.46 PBIST_CA3 Register

14.8.2.2.46.1 PBIST_CA3 Register (Offset = 13Ch) [reset = 0h]

Constant Address Registers

Return to Summary Table

Table 14-15994. Instance Table

Instance Name	Physical Address
PBIST0	0039 013Ch
PBIST1	003A 013Ch
PBIST2	003B 013Ch
PBIST3	003C 013Ch
PBIST4	003D 013Ch
PBIST5	003E 013Ch
PBIST6	003F 013Ch
PBIST7	0034 013Ch
PBIST8	0035 013Ch
WKUP_PBIST0	2B50 013Ch
WKUP_PBIST1	2B50 113Ch

Figure 14-7869. PBIST_CA3 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CA3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CA3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-15995. PBIST_CA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CA3	R/W	0h	Constant Address Register 3 (CA3) Reset Source: mod_g_rst_n

14.8.2.2.47 PBIST_CL0 Register

14.8.2.2.47.1 PBIST_CL0 Register (Offset = 140h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-15996. Instance Table

Instance Name	Physical Address
PBIST0	0039 0140h
PBIST1	003A 0140h
PBIST2	003B 0140h
PBIST3	003C 0140h
PBIST4	003D 0140h
PBIST5	003E 0140h
PBIST6	003F 0140h
PBIST7	0034 0140h
PBIST8	0035 0140h
WKUP_PBIST0	2B50 0140h
WKUP_PBIST1	2B50 1140h

Figure 14-7870. PBIST_CL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL0							
R/W							
0h							
7	6	5	4	3	2	1	0
CL0							
R/W							
0h							

Table 14-15997. PBIST_CL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL0	R/W	0h	Constant Loop Count Register 0 (CL0) Reset Source: mod_g_rst_n

14.8.2.2.48 PBIST_CL1 Register

14.8.2.2.48.1 PBIST_CL1 Register (Offset = 144h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-15998. Instance Table

Instance Name	Physical Address
PBIST0	0039 0144h
PBIST1	003A 0144h
PBIST2	003B 0144h
PBIST3	003C 0144h
PBIST4	003D 0144h
PBIST5	003E 0144h
PBIST6	003F 0144h
PBIST7	0034 0144h
PBIST8	0035 0144h
WKUP_PBIST0	2B50 0144h
WKUP_PBIST1	2B50 1144h

Figure 14-7871. PBIST_CL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL1							
R/W							
0h							
7	6	5	4	3	2	1	0
CL1							
R/W							
0h							

Table 14-15999. PBIST_CL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL1	R/W	0h	Constant Loop Count Register 1 (CL1) Reset Source: mod_g_rst_n

14.8.2.2.49 PBIST_CL2 Register

14.8.2.2.49.1 PBIST_CL2 Register (Offset = 148h) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-16000. Instance Table

Instance Name	Physical Address
PBIST0	0039 0148h
PBIST1	003A 0148h
PBIST2	003B 0148h
PBIST3	003C 0148h
PBIST4	003D 0148h
PBIST5	003E 0148h
PBIST6	003F 0148h
PBIST7	0034 0148h
PBIST8	0035 0148h
WKUP_PBIST0	2B50 0148h
WKUP_PBIST1	2B50 1148h

Figure 14-7872. PBIST_CL2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL2							
R/W							
0h							
7	6	5	4	3	2	1	0
CL2							
R/W							
0h							

Table 14-16001. PBIST_CL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL2	R/W	0h	Constant Loop Count Register 2 (CL2) Reset Source: mod_g_rst_n

14.8.2.2.50 PBIST_CL3 Register

14.8.2.2.50.1 PBIST_CL3 Register (Offset = 14Ch) [reset = 0h]

Constant Loop Count Registers

Return to Summary Table

Table 14-16002. Instance Table

Instance Name	Physical Address
PBIST0	0039 014Ch
PBIST1	003A 014Ch
PBIST2	003B 014Ch
PBIST3	003C 014Ch
PBIST4	003D 014Ch
PBIST5	003E 014Ch
PBIST6	003F 014Ch
PBIST7	0034 014Ch
PBIST8	0035 014Ch
WKUP_PBIST0	2B50 014Ch
WKUP_PBIST1	2B50 114Ch

Figure 14-7873. PBIST_CL3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CL3							
R/W							
0h							
7	6	5	4	3	2	1	0
CL3							
R/W							
0h							

Table 14-16003. PBIST_CL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CL3	R/W	0h	Constant Loop Count Register 3 (CL3) Reset Source: mod_g_rst_n

14.8.2.2.51 PBIST_I0 Register

14.8.2.2.51.1 PBIST_I0 Register (Offset = 150h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-16004. Instance Table

Instance Name	Physical Address
PBIST0	0039 0150h
PBIST1	003A 0150h
PBIST2	003B 0150h
PBIST3	003C 0150h
PBIST4	003D 0150h
PBIST5	003E 0150h
PBIST6	003F 0150h
PBIST7	0034 0150h
PBIST8	0035 0150h
WKUP_PBIST0	2B50 0150h
WKUP_PBIST1	2B50 1150h

Figure 14-7874. PBIST_I0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-16005. PBIST_I0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 0 (I0) Reset Source: mod_g_rst_n

14.8.2.2.52 PBIST_I1 Register

14.8.2.2.52.1 PBIST_I1 Register (Offset = 154h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-16006. Instance Table

Instance Name	Physical Address
PBIST0	0039 0154h
PBIST1	003A 0154h
PBIST2	003B 0154h
PBIST3	003C 0154h
PBIST4	003D 0154h
PBIST5	003E 0154h
PBIST6	003F 0154h
PBIST7	0034 0154h
PBIST8	0035 0154h
WKUP_PBIST0	2B50 0154h
WKUP_PBIST1	2B50 1154h

Figure 14-7875. PBIST_I1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-16007. PBIST_I1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 1 (I1) Reset Source: mod_g_rst_n

14.8.2.2.53 PBIST_I2 Register

14.8.2.2.53.1 PBIST_I2 Register (Offset = 158h) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-16008. Instance Table

Instance Name	Physical Address
PBIST0	0039 0158h
PBIST1	003A 0158h
PBIST2	003B 0158h
PBIST3	003C 0158h
PBIST4	003D 0158h
PBIST5	003E 0158h
PBIST6	003F 0158h
PBIST7	0034 0158h
PBIST8	0035 0158h
WKUP_PBIST0	2B50 0158h
WKUP_PBIST1	2B50 1158h

Figure 14-7876. PBIST_I2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">I0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">I0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16009. PBIST_I2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 2 (I2) Reset Source: mod_g_rst_n

14.8.2.2.54 PBIST_I3 Register

14.8.2.2.54.1 PBIST_I3 Register (Offset = 15Ch) [reset = 0h]

Constant Increment Registers

Return to Summary Table

Table 14-16010. Instance Table

Instance Name	Physical Address
PBIST0	0039 015Ch
PBIST1	003A 015Ch
PBIST2	003B 015Ch
PBIST3	003C 015Ch
PBIST4	003D 015Ch
PBIST5	003E 015Ch
PBIST6	003F 015Ch
PBIST7	0034 015Ch
PBIST8	0035 015Ch
WKUP_PBIST0	2B50 015Ch
WKUP_PBIST1	2B50 115Ch

Figure 14-7877. PBIST_I3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
I0							
R/W							
0h							
7	6	5	4	3	2	1	0
I0							
R/W							
0h							

Table 14-16011. PBIST_I3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	I0	R/W	0h	Constant Increment Register 3 (I3) Reset Source: mod_g_rst_n

14.8.2.2.55 PBIST_RAMT Register

14.8.2.2.55.1 PBIST_RAMT Register (Offset = 160h) [reset = 0h]

RAM Configuration Register

Return to Summary Table

Table 14-16012. Instance Table

Instance Name	Physical Address
PBIST0	0039 0160h
PBIST1	003A 0160h
PBIST2	003B 0160h
PBIST3	003C 0160h
PBIST4	003D 0160h
PBIST5	003E 0160h
PBIST6	003F 0160h
PBIST7	0034 0160h
PBIST8	0035 0160h
WKUP_PBIST0	2B50 0160h
WKUP_PBIST1	2B50 1160h

Figure 14-7878. PBIST_RAMT Name Register

31	30	29	28	27	26	25	24
RGS							
R/W							
0h							
23	22	21	20	19	18	17	16
RDS							
R/W							
0h							
15	14	13	12	11	10	9	8
DWR							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED		PLS				RLS	
NONE		R/W				R/W	
0h		0h				0h	

Table 14-16013. PBIST_RAMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RGS	R/W	0h	RAM Group Select RGS Reset Source: mod_g_rst_n
23:16	RDS	R/W	0h	Return Data select RDS Reset Source: mod_g_rst_n
15:8	DWR	R/W	0h	Data Width Register DWR Reset Source: mod_g_rst_n
7:6	RESERVED	NONE	0h	Reserved
5:2	PLS	R/W	0h	Pipeline Latency Select Reset Source: mod_g_rst_n

Table 14-16013. PBIST_RAMT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RLS	R/W	0h	RAM Latency Select Reset Source: mod_g_rst_n

14.8.2.2.56 PBIST_DLR Register

14.8.2.2.56.1 PBIST_DLR Register (Offset = 164h) [reset = 208h]

Datalogger Register

Return to Summary Table

Table 14-16014. Instance Table

Instance Name	Physical Address
PBIST0	0039 0164h
PBIST1	003A 0164h
PBIST2	003B 0164h
PBIST3	003C 0164h
PBIST4	003D 0164h
PBIST5	003E 0164h
PBIST6	003F 0164h
PBIST7	0034 0164h
PBIST8	0035 0164h
WKUP_PBIST0	2B50 0164h
WKUP_PBIST1	2B50 1164h

Figure 14-7879. PBIST_DLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
BRP							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED					DLR1_RTM	DLR1_GNG	DLR1_MISR
NONE					R/W	R/W	R/W
0h					0h	1h	0h
7	6	5	4	3	2	1	0
DLR0_TSM	DLR0_CFMM	DLR0_ECAM	DLR0_CAM	DLR0_TCK	DLR0_ROM	DLR0_IDDQ	DLR0_DCM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	1h	0h	0h	0h

Table 14-16015. PBIST_DLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	BRP	R/W	0h	Datalogger 2 (BRP) Reset Source: mod_g_rst_n
15:11	RESERVED	NONE	0h	Reserved
10	DLR1_RTM	R/W	0h	Retention testing mode Reset Source: mod_g_rst_n
9	DLR1_GNG	R/W	1h	GO / NO-GO testing mode Reset Source: mod_g_rst_n

Table 14-16015. PBIST_DLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DLR1_MISR	R/W	0h	MISR testing mode (mainly for ROM testing) Reset Source: mod_g_rst_n
7	DLR0_TSM	R/W	0h	Time stamp mode Reset Source: mod_g_rst_n
6	DLR0_CFMM	R/W	0h	Column Fail Masking mode Reset Source: mod_g_rst_n
5	DLR0_ECAM	R/W	0h	Emulation cache access mode Reset Source: mod_g_rst_n
4	DLR0_CAM	R/W	0h	Config access mode Reset Source: mod_g_rst_n
3	DLR0_TCK	R/W	1h	TCK Gated mode Reset Source: mod_g_rst_n
2	DLR0_ROM	R/W	0h	ROM-based testing mode Reset Source: mod_g_rst_n
1	DLR0_IDDQ	R/W	0h	IDDQ testing mode Reset Source: mod_g_rst_n
0	DLR0_DCM	R/W	0h	Distributed Compare mode Reset Source: mod_g_rst_n

14.8.2.2.57 PBIST_CMS Register

14.8.2.2.57.1 PBIST_CMS Register (Offset = 168h) [reset = 0h]

Clock-Mux Select Register

Return to Summary Table

Table 14-16016. Instance Table

Instance Name	Physical Address
PBIST0	0039 0168h
PBIST1	003A 0168h
PBIST2	003B 0168h
PBIST3	003C 0168h
PBIST4	003D 0168h
PBIST5	003E 0168h
PBIST6	003F 0168h
PBIST7	0034 0168h
PBIST8	0035 0168h
WKUP_PBIST0	2B50 0168h
WKUP_PBIST1	2B50 1168h

Figure 14-7880. PBIST_CMS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">CMS</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 14-16017. PBIST_CMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CMS	R/W	0h	Clock Mux Select (CMS) Reset Source: mod_g_rst_n

14.8.2.2.58 PBIST_STR Register

14.8.2.2.58.1 PBIST_STR Register (Offset = 16Ch) [reset = 0h]

Program Control Register

Return to Summary Table

Table 14-16018. Instance Table

Instance Name	Physical Address
PBIST0	0039 016Ch
PBIST1	003A 016Ch
PBIST2	003B 016Ch
PBIST3	003C 016Ch
PBIST4	003D 016Ch
PBIST5	003E 016Ch
PBIST6	003F 016Ch
PBIST7	0034 016Ch
PBIST8	0035 016Ch
WKUP_PBIST0	2B50 016Ch
WKUP_PBIST1	2B50 116Ch

Figure 14-7881. PBIST_STR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td>CHK</td><td>STEP</td><td>STOP</td><td>RES</td><td>START</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 14-16019. PBIST_STR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	CHK	R/W	0h	Check MISR mode Reset Source: mod_g_rst_n
3	STEP	R/W	0h	Step / Step for emulation mode Reset Source: mod_g_rst_n
2	STOP	R/W	0h	Stop Reset Source: mod_g_rst_n
1	RES	R/W	0h	Resume / Emulation read Reset Source: mod_g_rst_n

Table 14-16019. PBIST_STR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	START	R/W	0h	Start / Time Stamp mode restart Reset Source: mod_g_rst_n

14.8.2.2.59 PBIST_SCR Register

14.8.2.2.59.1 PBIST_SCR Register (Offset = 170h) [reset = FEDCBA9876542F40h]

Address Scrambling Register

Return to Summary Table

Table 14-16020. Instance Table

Instance Name	Physical Address
PBIST0	0039 0170h
PBIST1	003A 0170h
PBIST2	003B 0170h
PBIST3	003C 0170h
PBIST4	003D 0170h
PBIST5	003E 0170h
PBIST6	003F 0170h
PBIST7	0034 0170h
PBIST8	0035 0170h
WKUP_PBIST0	2B50 0170h
WKUP_PBIST1	2B50 1170h

Figure 14-7882. PBIST_SCR Name Register

63	62	61	60	59	58	57	48
SCR7							
R/W							
FEh							
55	54	53	52	51	50	49	48
SCR6							
R/W							
DCh							
47	46	45	44	43	42	41	40
SCR5							
R/W							
BAh							
39	38	37	36	35	34	33	32
SCR4							
R/W							
98h							
15	14	13	12	11	10	9	8
SCR1							
R/W							
32h							
7	6	5	4	3	2	1	0
SCR0							
R/W							
10h							

Table 14-16021. PBIST_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
63:56	SCR7	R/W	FEh	Address Scrambling Register 7 Reset Source: mod_g_rst_n

Table 14-16021. PBIST_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
55:48	SCR6	R/W	DCh	Address Scrambling Register 6 Reset Source: mod_g_rst_n
47:40	SCR5	R/W	BAh	Address Scrambling Register 5 Reset Source: mod_g_rst_n
39:32	SCR4	R/W	98h	Address Scrambling Register 4 Reset Source: mod_g_rst_n
31:24	SCR3	R/W	76h	Address Scrambling Register 3 Reset Source: mod_g_rst_n
23:16	SCR2	R/W	54h	Address Scrambling Register 2 Reset Source: mod_g_rst_n
15:8	SCR1	R/W	32h	Address Scrambling Register 1 Reset Source: mod_g_rst_n
7:0	SCR0	R/W	10h	Address Scrambling Register 0 Reset Source: mod_g_rst_n

14.8.2.2.60 PBIST_CSR Register

14.8.2.2.60.1 PBIST_CSR Register (Offset = 178h) [reset = 0h]

Chip Select Register

Return to Summary Table

Table 14-16022. Instance Table

Instance Name	Physical Address
PBIST0	0039 0178h
PBIST1	003A 0178h
PBIST2	003B 0178h
PBIST3	003C 0178h
PBIST4	003D 0178h
PBIST5	003E 0178h
PBIST6	003F 0178h
PBIST7	0034 0178h
PBIST8	0035 0178h
WKUP_PBIST0	2B50 0178h
WKUP_PBIST1	2B50 1178h

Figure 14-7883. PBIST_CSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">CSR3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">CSR2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CSR1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CSR0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16023. PBIST_CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CSR3	R/W	0h	Chip Select 3 (CSR3) Reset Source: mod_g_rst_n
23:16	CSR2	R/W	0h	Chip Select 2 (CSR2) Reset Source: mod_g_rst_n
15:8	CSR1	R/W	0h	Chip Select 1(CSR1) Reset Source: mod_g_rst_n
7:0	CSR0	R/W	0h	Chip Select 0 (CSR0) Reset Source: mod_g_rst_n

14.8.2.2.61 PBIST_FDLY Register

14.8.2.2.61.1 PBIST_FDLY Register (Offset = 17Ch) [reset = 68h]

Fail Delay Register

Return to Summary Table

Table 14-16024. Instance Table

Instance Name	Physical Address
PBIST0	0039 017Ch
PBIST1	003A 017Ch
PBIST2	003B 017Ch
PBIST3	003C 017Ch
PBIST4	003D 017Ch
PBIST5	003E 017Ch
PBIST6	003F 017Ch
PBIST7	0034 017Ch
PBIST8	0035 017Ch
WKUP_PBIST0	2B50 017Ch
WKUP_PBIST1	2B50 117Ch

Figure 14-7884. PBIST_FDLY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FDLY							
R/W							
68h							

Table 14-16025. PBIST_FDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FDLY	R/W	68h	Fail Delay (FDLY) Reset Source: mod_g_rst_n

14.8.2.2.62 PBIST_PACT Register

14.8.2.2.62.1 PBIST_PACT Register (Offset = 180h) [reset = 0h]

PACT Register

Return to Summary Table

Table 14-16026. Instance Table

Instance Name	Physical Address
PBIST0	0039 0180h
PBIST1	003A 0180h
PBIST2	003B 0180h
PBIST3	003C 0180h
PBIST4	003D 0180h
PBIST5	003E 0180h
PBIST6	003F 0180h
PBIST7	0034 0180h
PBIST8	0035 0180h
WKUP_PBIST0	2B50 0180h
WKUP_PBIST1	2B50 1180h

Figure 14-7885. PBIST_PACT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PACT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 14-16027. PBIST_PACT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PACT	R/W	0h	PBIST Activate (PACT) Reset Source: mod_g_rst_n

14.8.2.2.63 PBIST_PID Register

14.8.2.2.63.1 PBIST_PID Register (Offset = 184h) [reset = 0h]

PBIST_ID Register

Return to Summary Table

Table 14-16028. Instance Table

Instance Name	Physical Address
PBIST0	0039 0184h
PBIST1	003A 0184h
PBIST2	003B 0184h
PBIST3	003C 0184h
PBIST4	003D 0184h
PBIST5	003E 0184h
PBIST6	003F 0184h
PBIST7	0034 0184h
PBIST8	0035 0184h
WKUP_PBIST0	2B50 0184h
WKUP_PBIST1	2B50 1184h

Figure 14-7886. PBIST_PID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PID				
NONE			R/W				
0h			0h				

Table 14-16029. PBIST_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	PID	R/W	0h	PBIST ID Reset Source: mod_g_rst_n

14.8.2.2.64 PBIST_OVER Register

14.8.2.2.64.1 PBIST_OVER Register (Offset = 188h) [reset = 9h]

Override Register

Return to Summary Table

Table 14-16030. Instance Table

Instance Name	Physical Address
PBIST0	0039 0188h
PBIST1	003A 0188h
PBIST2	003B 0188h
PBIST3	003C 0188h
PBIST4	003D 0188h
PBIST5	003E 0188h
PBIST6	003F 0188h
PBIST7	0034 0188h
PBIST8	0035 0188h
WKUP_PBIST0	2B50 0188h
WKUP_PBIST1	2B50 1188h

Figure 14-7887. PBIST_OVER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ALGO	MM	READ	RINFO
NONE				R/W	R/W	R/W	R/W
0h				1h	0h	0h	1h

Table 14-16031. PBIST_OVER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ALGO	R/W	1h	PBIST Override Algorithm Override Reset Source: mod_g_rst_n
2	MM	R/W	0h	PBIST Override Multiple Memory Reset Source: mod_g_rst_n
1	READ	R/W	0h	PBIST Override READ Override Reset Source: mod_g_rst_n
0	RINFO	R/W	1h	PBIST Override RINFO Override Reset Source: mod_g_rst_n

14.8.2.2.65 PBIST_FSRF Register

14.8.2.2.65.1 PBIST_FSRF Register (Offset = 190h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-16032. Instance Table

Instance Name	Physical Address
PBIST0	0039 0190h
PBIST1	003A 0190h
PBIST2	003B 0190h
PBIST3	003C 0190h
PBIST4	003D 0190h
PBIST5	003E 0190h
PBIST6	003F 0190h
PBIST7	0034 0190h
PBIST8	0035 0190h
WKUP_PBIST0	2B50 0190h
WKUP_PBIST1	2B50 1190h

Figure 14-7888. PBIST_FSRF Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED							FRSF1
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FRSF0
NONE							R
0h							0h

Table 14-16033. PBIST_FSRF Register Field Descriptions

Bit	Field	Type	Reset	Description
63:33	RESERVED	NONE	0h	Reserved

Table 14-16033. PBIST_FSRF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
32	FRSF1	R	0h	Fail Status Fail - Port 1 (FSRF1) Reset Source: mod_g_rst_n
31:1	RESERVED	NONE	0h	Reserved
0	FRSF0	R	0h	Fail Status Fail - Port 0 (FSRF0) Reset Source: mod_g_rst_n

14.8.2.2.66 PBIST_FSRC Register

14.8.2.2.66.1 PBIST_FSRC Register (Offset = 198h) [reset = 0h]

Fail Status Count Register

Return to Summary Table

Table 14-16034. Instance Table

Instance Name	Physical Address
PBIST0	0039 0198h
PBIST1	003A 0198h
PBIST2	003B 0198h
PBIST3	003C 0198h
PBIST4	003D 0198h
PBIST5	003E 0198h
PBIST6	003F 0198h
PBIST7	0034 0198h
PBIST8	0035 0198h
WKUP_PBIST0	2B50 0198h
WKUP_PBIST1	2B50 1198h

Figure 14-7889. PBIST_FSRC Name Register

63	62	61	60	59	58	57	48
RESERVED							
NONE							
0h							
55	54	53	52	51	50	49	48
RESERVED							
NONE							
0h							
47	46	45	44	43	42	41	40
RESERVED							
NONE							
0h							
39	38	37	36	35	34	33	32
RESERVED				FSRC1			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				FSRC0			
NONE				R			
0h				0h			

Table 14-16035. PBIST_FSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
63:36	RESERVED	NONE	0h	Reserved

Table 14-16035. PBIST_FSRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
35:32	FSRC1	R	0h	Fail Status Count - Port 1 (FSRC1) Reset Source: mod_g_rst_n
31:4	RESERVED	NONE	0h	Reserved
3:0	FSRC0	R	0h	Fail Status Count - Port 0 (FSRC0) Reset Source: mod_g_rst_n

14.8.2.2.67 PBIST_FSRA Register

14.8.2.2.67.1 PBIST_FSRA Register (Offset = 1A0h) [reset = 0h]

Fail Status Address Register

Return to Summary Table

Table 14-16036. Instance Table

Instance Name	Physical Address
PBIST0	0039 01A0h
PBIST1	003A 01A0h
PBIST2	003B 01A0h
PBIST3	003C 01A0h
PBIST4	003D 01A0h
PBIST5	003E 01A0h
PBIST6	003F 01A0h
PBIST7	0034 01A0h
PBIST8	0035 01A0h
WKUP_PBIST0	2B50 01A0h
WKUP_PBIST1	2B50 11A0h

Figure 14-7890. PBIST_FSRA Name Register

<table>
<tr><td>63</td><td>62</td><td>61</td><td>60</td><td>59</td><td>58</td><td>57</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>55</td><td>54</td><td>53</td><td>52</td><td>51</td><td>50</td><td>49</td><td>48</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">FSRA1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="8">FSRA1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FSRA0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FSRA0</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 14-16037. PBIST_FSRA Register Field Descriptions

Bit	Field	Type	Reset	Description
63:48	RESERVED	NONE	0h	Reserved

Table 14-16037. PBIST_FSRA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
47:32	FSRA1	R	0h	Fail Status Address - Port 1 (FSRA1) Reset Source: mod_g_rst_n
31:16	RESERVED	NONE	0h	Reserved
15:0	FSRA0	R	0h	Fail Status Address - Port 0 (FSRA0) Reset Source: mod_g_rst_n

14.8.2.2.68 PBIST_FSRDL0 Register

14.8.2.2.68.1 PBIST_FSRDL0 Register (Offset = 1A8h) [reset = 0h]

Fail Status Data Registers

Return to Summary Table

Table 14-16038. Instance Table

Instance Name	Physical Address
PBIST0	0039 01A8h
PBIST1	003A 01A8h
PBIST2	003B 01A8h
PBIST3	003C 01A8h
PBIST4	003D 01A8h
PBIST5	003E 01A8h
PBIST6	003F 01A8h
PBIST7	0034 01A8h
PBIST8	0035 01A8h
WKUP_PBIST0	2B50 01A8h
WKUP_PBIST1	2B50 11A8h

Figure 14-7891. PBIST_FSRDL0 Name Register

31	30	29	28	27	26	25	24
FSRDL0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FSRDL0							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FSRDL0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FSRDL0							
R							
0h							

Table 14-16039. PBIST_FSRDL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FSRDL0	R	0h	Fail Status Data - Port 0 (FSRDL0) Reset Source: mod_g_rst_n

14.8.2.2.69 PBIST_FSRDL1 Register

14.8.2.2.69.1 PBIST_FSRDL1 Register (Offset = 1B0h) [reset = 0h]

Fail Status Data Registers

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Table 14-16040. Instance Table

Instance Name	Physical Address
PBIST0	0039 01B0h
PBIST1	003A 01B0h
PBIST2	003B 01B0h
PBIST3	003C 01B0h
PBIST4	003D 01B0h
PBIST5	003E 01B0h
PBIST6	003F 01B0h
PBIST7	0034 01B0h
PBIST8	0035 01B0h
WKUP_PBIST0	2B50 01B0h
WKUP_PBIST1	2B50 11B0h

Figure 14-7892. PBIST_FSRDL1 Name Register

31	30	29	28	27	26	25	24
FSRDL1							
R							
0h							
23	22	21	20	19	18	17	16
FSRDL1							
R							
0h							
15	14	13	12	11	10	9	8
FSRDL1							
R							
0h							
7	6	5	4	3	2	1	0
FSRDL1							
R							
0h							

Table 14-16041. PBIST_FSRDL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FSRDL1	R	0h	Fail Status Data - Port 1 (FSRDL1) Reset Source: mod_g_rst_n

14.8.2.2.70 PBIST_MARGIN_MODE Register

14.8.2.2.70.1 PBIST_MARGIN_MODE Register (Offset = 1B4h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-16042. Instance Table

Instance Name	Physical Address
PBIST0	0039 01B4h
PBIST1	003A 01B4h
PBIST2	003B 01B4h
PBIST3	003C 01B4h
PBIST4	003D 01B4h
PBIST5	003E 01B4h
PBIST6	003F 01B4h
PBIST7	0034 01B4h
PBIST8	0035 01B4h
WKUP_PBIST0	2B50 01B4h
WKUP_PBIST1	2B50 11B4h

Figure 14-7893. PBIST_MARGIN_MODE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PBIST_DFT_READ		PBIST_DFT_WRITE	
NONE				R		R	
0h				0h		0h	

Table 14-16043. PBIST_MARGIN_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	PBIST_DFT_READ	R	0h	pbist_dft_read[1:0] Reset Source: mod_g_rst_n
1:0	PBIST_DFT_WRITE	R	0h	pbist_dft_write[1:0] Reset Source: mod_g_rst_n

14.8.2.2.71 PBIST_WRENZ Register

14.8.2.2.71.1 PBIST_WRENZ Register (Offset = 1B8h) [reset = 0h]

Fail Status Fail Register

Return to Summary Table

Table 14-16044. Instance Table

Instance Name	Physical Address
PBIST0	0039 01B8h
PBIST1	003A 01B8h
PBIST2	003B 01B8h
PBIST3	003C 01B8h
PBIST4	003D 01B8h
PBIST5	003E 01B8h
PBIST6	003F 01B8h
PBIST7	0034 01B8h
PBIST8	0035 01B8h
WKUP_PBIST0	2B50 01B8h
WKUP_PBIST1	2B50 11B8h

Figure 14-7894. PBIST_WRENZ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						WRENZ	
NONE						R	
0h						0h	

Table 14-16045. PBIST_WRENZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	WRENZ	R	0h	pbist_ram_wrenz[1:0] Reset Source: mod_g_rst_n

14.8.2.2.72 PBIST_PAGE_PGS Register

14.8.2.2.72.1 PBIST_PAGE_PGS Register (Offset = 1BCh) [reset = 0h]

Fail Status Fail Register

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Table 14-16046. Instance Table

Instance Name	Physical Address
PBIST0	0039 01BCh
PBIST1	003A 01BCh
PBIST2	003B 01BCh
PBIST3	003C 01BCh
PBIST4	003D 01BCh
PBIST5	003E 01BCh
PBIST6	003F 01BCh
PBIST7	0034 01BCh
PBIST8	0035 01BCh
WKUP_PBIST0	2B50 01BCh
WKUP_PBIST1	2B50 11BCh

Figure 14-7895. PBIST_PAGE_PGS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PGS	
NONE						R	
0h						0h	

Table 14-16047. PBIST_PAGE_PGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	PGS	R	0h	pbist_ram_pgs[1:0] Reset Source: mod_g_rst_n

14.8.2.2.73 PBIST_ROM Register

14.8.2.2.73.1 PBIST_ROM Register (Offset = 1C0h) [reset = 3h]

ROM Mask Register

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Table 14-16048. Instance Table

Instance Name	Physical Address
PBIST0	0039 01C0h
PBIST1	003A 01C0h
PBIST2	003B 01C0h
PBIST3	003C 01C0h
PBIST4	003D 01C0h
PBIST5	003E 01C0h
PBIST6	003F 01C0h
PBIST7	0034 01C0h
PBIST8	0035 01C0h
WKUP_PBIST0	2B50 01C0h
WKUP_PBIST1	2B50 11C0h

Figure 14-7896. PBIST_ROM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						ROM	
NONE						R/W	
0h						3h	

Table 14-16049. PBIST_ROM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	ROM	R/W	3h	ROM Mask (ROM) Reset Source: mod_g_rst_n

14.8.2.2.74 PBIST_ALGO Register

14.8.2.2.74.1 PBIST_ALGO Register (Offset = 1C4h) [reset = FFFFFFFFh]

Algorithm Mask Register

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Table 14-16050. Instance Table

Instance Name	Physical Address
PBIST0	0039 01C4h
PBIST1	003A 01C4h
PBIST2	003B 01C4h
PBIST3	003C 01C4h
PBIST4	003D 01C4h
PBIST5	003E 01C4h
PBIST6	003F 01C4h
PBIST7	0034 01C4h
PBIST8	0035 01C4h
WKUP_PBIST0	2B50 01C4h
WKUP_PBIST1	2B50 11C4h

Figure 14-7897. PBIST_ALGO Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ALGO_3</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ALGO_2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ALGO_1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ALGO_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">FFh</td></tr>
</table>

Table 14-16051. PBIST_ALGO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ALGO_3	R/W	FFh	ROM Algorithm Mask 3 (ALGO 3) Reset Source: mod_g_rst_n
23:16	ALGO_2	R/W	FFh	ROM Algorithm Mask 2 (ALGO 2) Reset Source: mod_g_rst_n
15:8	ALGO_1	R/W	FFh	ROM Algorithm Mask 1 (ALGO 1) Reset Source: mod_g_rst_n
7:0	ALGO_0	R/W	FFh	ROM Algorithm Mask 0 (ALGO 0) Reset Source: mod_g_rst_n

14.8.2.2.75 PBIST_RINFO Register

14.8.2.2.75.1 PBIST_RINFO Register (Offset = 1C8h) [reset = 10000000000000180h]

RAM Info Mask Register

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Table 14-16052. Instance Table

Instance Name	Physical Address
PBIST0	0039 01C8h
PBIST1	003A 01C8h
PBIST2	003B 01C8h
PBIST3	003C 01C8h
PBIST4	003D 01C8h
PBIST5	003E 01C8h
PBIST6	003F 01C8h
PBIST7	0034 01C8h
PBIST8	0035 01C8h
WKUP_PBIST0	2B50 01C8h
WKUP_PBIST1	2B50 11C8h

Figure 14-7898. PBIST_RINFO Name Register

63	62	61	60	59	58	57	48
U3							
R/W							
FFh							
55	54	53	52	51	50	49	48
U2							
R/W							
FFh							
47	46	45	44	43	42	41	40
U1							
R/W							
FFh							
39	38	37	36	35	34	33	32
U0							
R/W							
FFh							
15	14	13	12	11	10	9	8
L1							
R/W							
FFh							
7	6	5	4	3	2	1	0
L0							
R/W							
FFh							

Table 14-16053. PBIST_RINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
63:56	U3	R/W	FFh	RAM Info Mask Upper 3 (RINFOU3) Reset Source: mod_g_rst_n

Table 14-16053. PBIST_RINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
55:48	U2	R/W	FFh	RAM Info Mask Upper 2 (RINFOU2) Reset Source: mod_g_rst_n
47:40	U1	R/W	FFh	RAM Info Mask Upper 1 (RINFOU1) Reset Source: mod_g_rst_n
39:32	U0	R/W	FFh	RAM Info Mask Upper 0 (RINFOU0) Reset Source: mod_g_rst_n
31:24	L3	R/W	FFh	RAM Info Mask Lower 3 (RINFOL3) Reset Source: mod_g_rst_n
23:16	L2	R/W	FFh	RAM Info Mask Lower 2 (RINFOL2) Reset Source: mod_g_rst_n
15:8	L1	R/W	FFh	RAM Info Mask Lower 1 (RINFOL1) Reset Source: mod_g_rst_n
7:0	L0	R/W	FFh	RAM Info Mask Lower 0 (RINFOL0) Reset Source: mod_g_rst_n

15 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 3, 2022 to April 30, 2026 (from Revision A (March 2022) to Revision B (April 2026)) **Page**

- Introduction: Removed under-construction notice........ 8
- Introduction: Expanded WKUP domain definition........ 9
- Introduction: Updated to MMA2F in block diagram........ 10
- Introduction: Added Single and Dual core options to C7x introductory description. Updated MMA name. Removed DRU data compression........ 11
- Update number of rings supported........ 13
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- IPC: Removed under-construction notice 422
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- SPI: Removed duplicate feature topics in PDMA Overview 698
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- Peripherals: Removed under-construction notice 775
- ASRC: Added tables for RXSYNC and TXSYNC 782
- Rename PRU_ICSSG to PRUSS 831
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- Added ATL Ports section 865
- MLBSS: Removed registers not applicable to the device 870
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- Genericize I2C statements 906
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- I2C: Updated note under I2C Block Diagram to clarify the i variables 914
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- I2C: Updated subsection reference to parent of the subsection 923
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- Add addition information to Polarity and Phase regarding data transfer 936
- Rename PRU_ICSSG to PRUSS 962
- SPI: Update Global Initialization of Surrounding Modues to mention not all modules are applicable 962
- Added RX, TX, CTS and RTS signals to main domain. 979
- UART: changed description in *System Using RS-485 Communication* to better align with UART instance used in section's image 980
- Signal names added to UART I/O Signals Table 980
- UART: Changed *IrDA Mode Interface Signals* image and paragraph to be more generic 981
- UART: Made *CIR Mode Interface Signals* diagram and paragraph more generic 988
- Updated the UART Baud Rate Settings table for baud rate up to 12Mbps 1014
- Update DLL and DLH Hex values associated with 160MHz and 192MHz Source Clock 1014
- Register name updates within CPSW3G Chapter 1036

- CPSW: Update interface mode registers to more generic name. 1043
- CPSW: Updated RMII clocking register to more generic name.... 1044
- CPSW: Updated CPSW CPTS CLKSEL to generic bit name.... 1108
- CPSW: Change to generic CPTS_CLKSEL name.... 1110
- Update Event FIFO depth from 10 to 32.... 1111
- Add PORT2 to TX INFO Word 3 Format, SRD_ID field.... 1126
- Add Port 2 to RX INFO Word 2, TO_PORT field.... 1130
- CPSW: updated to generic names for ENET1_CTRL and ENET2_CTRL.... 1137
- FSS: Move the FSS Introduction to be after the section's table of contents. Re-organized the OSPI bullet points into separate bullet points for clarity. Moved a table that outlines mode of operations and allowed interfaces to the intro section.... 1144
- FSS: Removed a duplicate allocation table and allocation paragraph for FSS0.... 1144
- FSS: Updated FSS Environment to mention other FSS0 names.... 1146
- FSS: Updated FSS I/O Signals to point to a subsection that covers the OSPI signals as a whole instead of a specific table. 1146
- FSS: Cleaned up references to other chapters.... 1148
- FSS: Updated Boot Size Configuration to point to CTRL_MMR Registers.... 1148
- FSS1: Removed duplicate overview paragraphs and duplicate sections on unsupported features. Updated diagram to remove reference to unused domains and ospi. 1149
- FSS1: Removed references to unused OSPI1.... 1149
- FSS: Updated FSS1 Typical Application images and tables to use more generic instance names.... 1150
- FSS: Removed FSS Allowed Interface Combinations to improve clarity of chapter as whole. Condensed list to reduce duplicate information. Removed Modes of Operation subsection because information got moved to a different a subsection. Made Block diagram more generic and clear.... 1152
- Update register names in OSPI Chapter.... 1154
- OSPI: Added new subsections to the chapter - OSPI PHY Modiule, PHY Pipeline Mode, Read Data Capturing by the PHY Module.... 1154
- FSS/OSPI: Added new sections about OSPI to help explain OSPI items from FSS diagrams.... 1154
- Maximum bytes supported by STIG is 16.... 1172
- FSS and HyperBus: Added new subsections about HyperBus to provide more details for FSS.... 1182
- FSS: Added sections to provide in-depth details about HyperBus.... 1182
- Added HyperBus Not Supported Features section.... 1183
- HyperBus: Adding HyperRAM and HyperFlash Programming guide.... 1188
- MMCSD Chapter modified to be more generic. Specifics included in module Integration section.... 1198
- Fixed typo of SDIO version from 4.0 to 3.0.... 1198
- Add 3.3V to Legacy MMC, High Speed SDR and High Speed DDR MMC Support.... 1199
- IO Signals made generic for different device types.... 1200
- Remove 33 Ω resistor requirement from MMCi_CLK.... 1200
- MMCSD IO Multiplexer figure added.... 1202
- EPWM I/O Signals Figure and Table updated to be generic for all devices.... 1339
- EPW: Updated instance counts and register names for Time-Base Clocks.... 1347
- Fix statement regarding Case 1 and Case 4.... 1361
- ADC: Updated Overview to be more generic 1392
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- ADC: Replaced registers with more generic names 1397
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- Update register names in GTC Chapter.... 1404
- GTC: Updated CLKSEL register name 1405
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- Timers: Updated paragraph to clarify instance counts. Updated register reference to register name instead of register region....1425
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- Add note that 32-kHz clock is sourced from the LFOSC....1430
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- Updated block diagram to be generic and include all domains. See datasheet for specifics....1453
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- Registers: Removed under-construction notice and updated registers name to clearer format....1499
- Registers: Changed a chapter title....4337
- PDMA Registers: Added note about instance counts....7906

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